COMPOUND SEMICONDUCTOR

October 2001 Volume 7 Number 9

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PROCESSING

Manufacturers tool up for high yield and high volume

ALSO INSIDE

GaAs grown on 12 inch silicon	Nakamura sues Nichia	Veeco snaps up Applied Epi

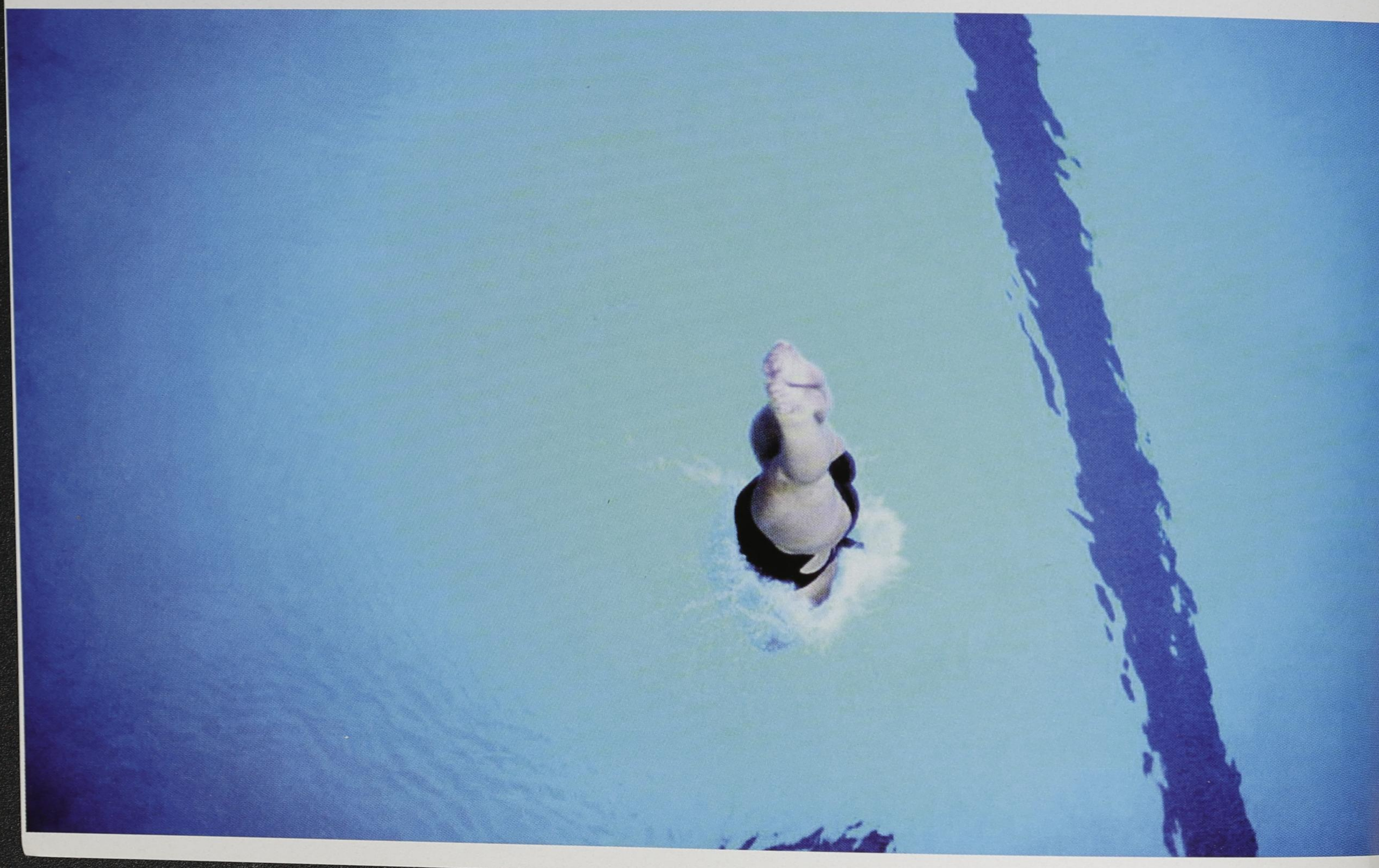
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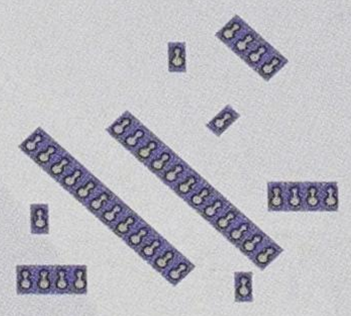
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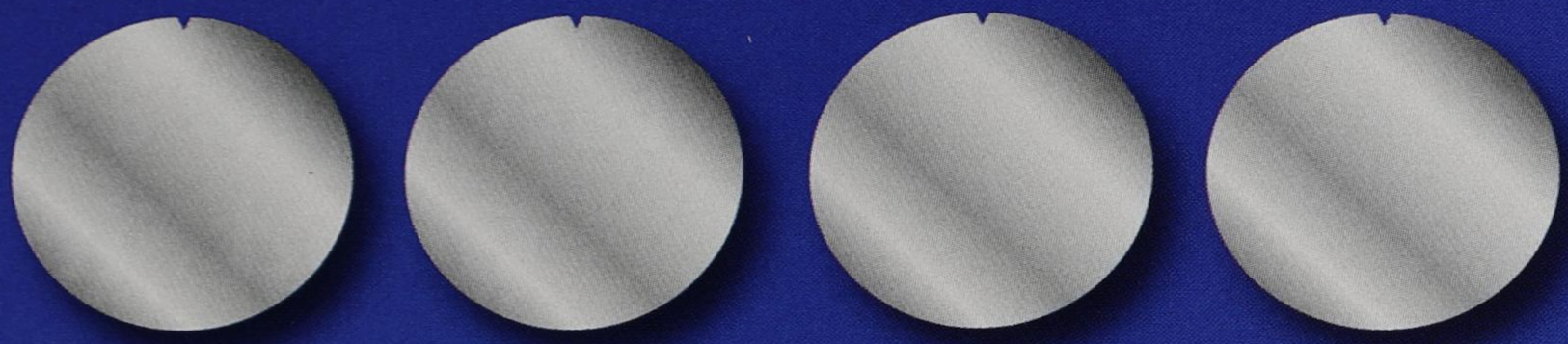
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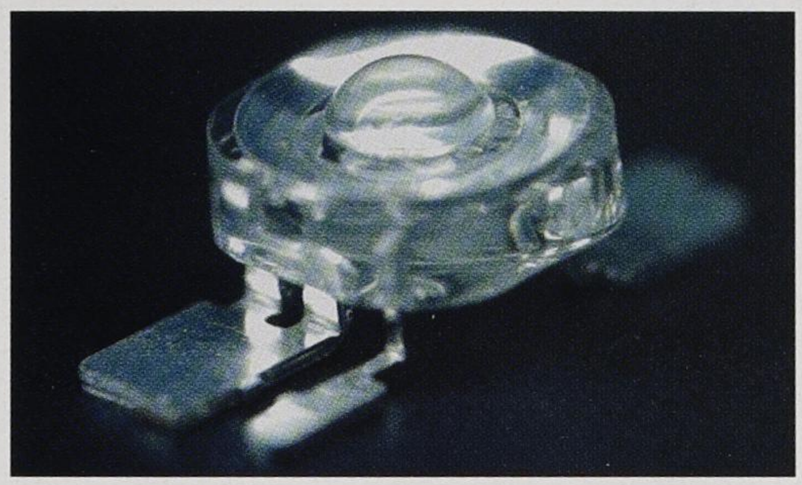
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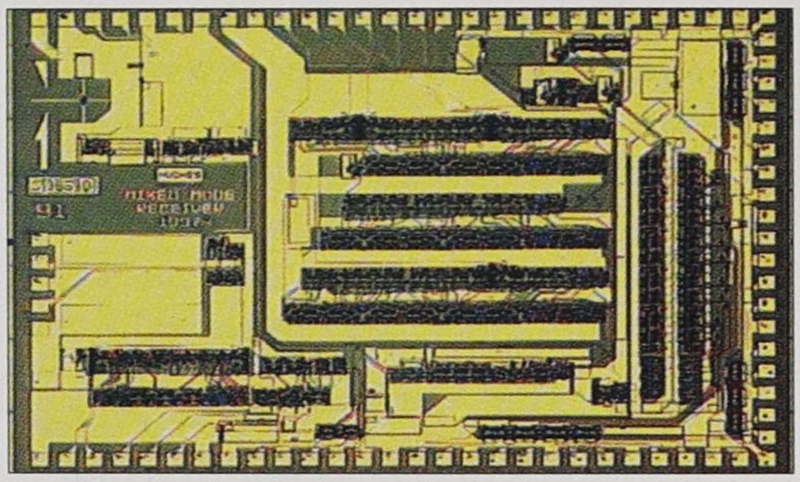
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Omron has increased the brightness of its LEDs using a double reflection package **p15**



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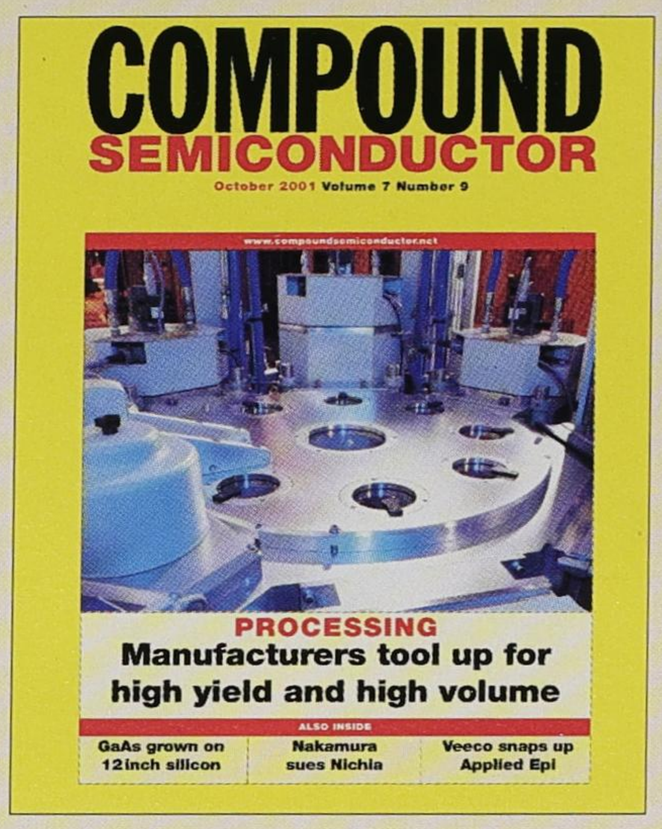
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Compound Semiconductor gets a new look



You may have noticed something different about this issue of *Compound Semiconductor* magazine – a new design scheme that updates our look and makes the content of the magazine more accessible to our readers. Despite these changes, the key strengths of *Compound Semiconductor* magazine remain unchanged – the quality, depth and breadth of our coverage of news and events in the compound semiconductor industry. Perhaps most importantly, the content and direction of *Compound Semiconductor* are still controlled by the same editorial team from Franklin Publishing.

Since its inception in 1995, *Compound Semiconductor* has earned a reputation for the high quality of its content, and this will continue to be the magazine's primary focus. However, the strategic alliance between Franklin Publishing and IOP Publishing has provided access to additional resources, which have already improved the magazine's distribution throughout the world. Now, we have also taken advantage of IOP Publishing's design skills to improve its appearance.

Why undergo a redesign? Some magazines are redesigned to make short articles fit into more space, compensating for a lack of editorial material. Our approach is based on the need to present information to the reader in a more accessible way, focusing on organization and clarity without compromising the quality of the articles and news items.

During the course of this year, we have also introduced new sections to the magazine. These include Headline News, which gives enhanced coverage of the most important stories each month, and Product Showcase, which describes new and innovative products from suppliers.

I hope you enjoy the results of the changes we have made to the magazine, and I welcome any comments you may have about the appearance or content of *Compound Semiconductor*.

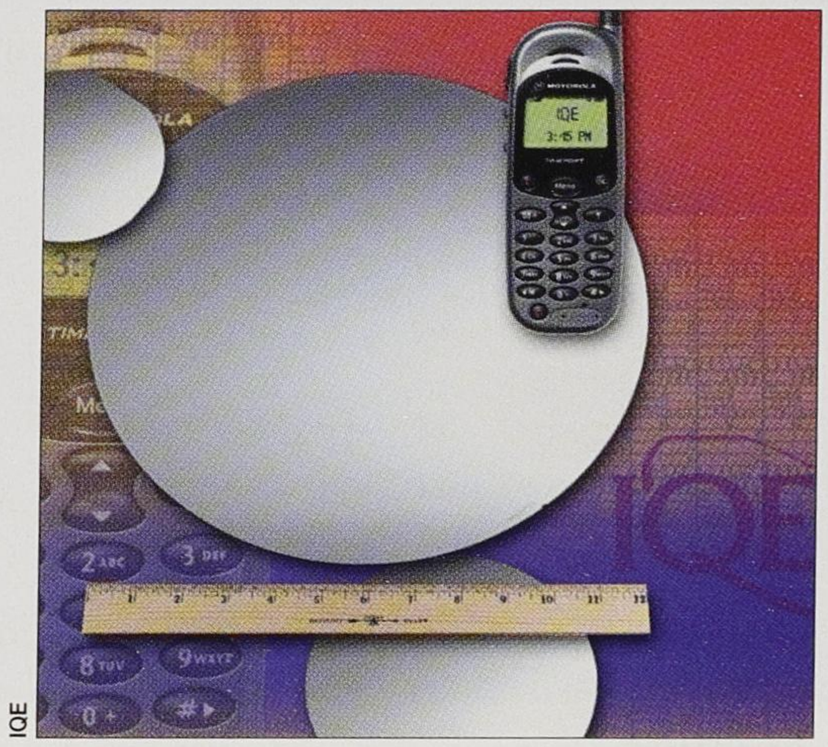
Tim Whitaker
Editor

Motorola and IQE demonstrate growth of GaAs on 8 and 12 inch silicon wafers

Striking a positive note during a gloomy September, the compound semiconductor industry witnessed a genuinely significant breakthrough which received extensive press coverage in the US and elsewhere.

Scientists from Motorola have developed a method to grow GaAs layers on silicon substrates, using a strontium titanate buffer layer (see the feature article on page 47 for full details). The GaAs-on-silicon wafers were without visible cracks or bowing, and there was no sign of the epitaxial layer peeling away from the Si substrate.

In collaboration with epiwafer manufacturer IQE, 8 and 12 inch GaAs-on-silicon wafers were produced. After the Si-STO-GaAs was completed, device structures were fabricated using conventional epitaxial growth and wafer processing technologies. Motorola went so far as to fabricate power amplifiers from FET structures grown on the GaAs-on-silicon wafers, and incorporated these PAs into mobile phones that have been used in live trials. Motorola has submitted a Late News paper to the GaAs IC Symposium, and the team will be working to demonstrate HBTs and HEMTs in the coming months.



IQE

FETs made from GaAs-on-silicon wafers have been used as PAs in mobile phones.

Clearly this is a very interesting development, not least because the successful growth of GaAs on silicon has been the target of research projects for decades. However, this technology is still at least a few years from the market; the timing of the announcement was dictated by the public disclosure of some of the key patents. While 12 inch GaAs-on-silicon substrates offer the tantalizing prospect of very low cost manufacturing of GaAs ICs, this only has real potential in the case of extremely high production volumes or very large digital ICs (or both). The possibilities of integrating silicon ICs with GaAs-based (or, subject to further developments, InP-based) optoelectronic devices also generated a lot of hype, but the complex processing techniques that will be required are not a trivial issue. Even so, this is a highly interesting development, and one which we will no doubt hear much more about in the future.

Terrorist aftershock reverberates through the compound semiconductor industry

By Marie Meyer

The horrific loss of life in the terrorist attacks in New York City, Washington DC and Pennsylvania on 11 September touched companies within the compound semiconductor industry. Employees from Raytheon and MRV Communications were among the passengers on the hijacked airplanes. The economic consequences, although they pale into insignificance alongside the growing tally of dead and missing, will also be huge.

As this issue goes to press the stock markets are reeling from one of their worst weeks since the Great Depression, dashing hopes that "patriotic investing" and aggressive buy-back programs might support share prices. Further details of the financial effects of the attacks are contained in our Portfolio section (p87).

Many are clinging to the hope that the downturn, though steep, might be short. Alan Greenspan, chairman of the Federal Reserve Bank, in his first public appearance after the attacks, acknowledged that economic activity in the US "ground to a halt" for a week – words that did little to stop the sell-off on Wall Street. But he went on to say that prior to the attacks the economy had been showing signs of picking up. And while the magnitude of this event would no doubt "have significant effects on the US economy over the short term," he also said that the economy has become "increasingly resilient to shocks," in part because of deregulation and advances in technology. In the long run, he said, the prospects remained undiminished for faster growth in productivity, which is Greenspan's favorite driver for non-inflationary growth.



POPPERFOTO/©BRAD RICKERBY, REUTERS

The day after the terrorist attacks the famous LED display outside the NASDAQ building in New York City offers condolences to the victims and their families.

What lies ahead?

Not surprisingly, analysts within the compound semiconductor industry have been hard-pressed to identify any silver linings to the massive cloud that is now hanging over the economy – and the American psyche.

Analysts at CIBC World Markets resumed their client advisory service when the markets re-opened on 17 September, despite the fact that their headquarters at One World Financial Center are near to "ground zero" and remain unusable. Amazingly, everyone at CIBC survived the attacks.

In the fiber-optic sector, CIBC's chief "take-away" message is that the impact would be only modest, possibly slightly positive or slightly negative depending on the company in question. CIBC analyst Jim Jungjohann made the following specific points:

- Despite the sudden surge in Internet usage that followed the attacks, there are few indications that bandwidth usage will reaccelerate. "Don't look for a pick-up in WDM spending until possibly the summer of 2002," he advises.
- There may be a short-term upswing in demand for home broadband access – DSL lines, cable modems, etc – but this is just a temporary blip rather than a meaningful, permanent increase in demand patterns.
- Expect to see increased spending on storage-area networks (SANs). Traditionally, only the largest of companies have been spending on SANs; Jim Jungjohann now expects it to spread much further.

Finisar is one of the leading component suppliers in the SAN market. According to chief financial officer Steve Workman, current demand among SAN equipment manufacturers is primarily for 2 Gbit/s components, with both VCSELs and Fabry–Perot lasers being used. The launch of 10 Gbit/s standards is expected soon.

In the wireless area, CIBC analyst Dale Pfau noted how the aftermath of the terrorist attacks showed "the significance of mobile personal communications, and perhaps highlighted the weakness in some of the carrier infrastructure networks." While he did not revise his estimates for wireless handset sales (380–400 million units in 2001; 440–460 million units in 2002), he does believe that the recently renewed interest in mobile communications could help to move sales "closer to the higher part of the ranges". In addition, infrastructure spending may pick up sooner than expected. Pfau said that "the deferred capital spending by the wireless carriers could become painfully evident as coverage and capacity problems throughout the networks are exposed." And, looking at things as optimistically as possible, it could be argued that the introduction of 2.5G phones now looks more promising. Pfau advises that since these phones will have "always on" data communications capability, and constant access to news and updates, they could be the "killer app" that is needed to jump-start sales of the next generation of handsets.

Transportation

The impact of this event on aviation in the US will be profound. Even after any lingering aversion to flying wears off, travelers will have to contend with a whole host of new consequences. Among the possibilities: fewer flights, fewer airlines, more frequent interruptions of service, higher airfares and significantly longer check-in times.

Shipments of goods will also be affected. Immediately after the attacks the FAA banned freight shipments from passenger planes, sending shippers scrambling for alternatives. More than three-quarters of US domestic air cargo moves on dedicated freight-only air-

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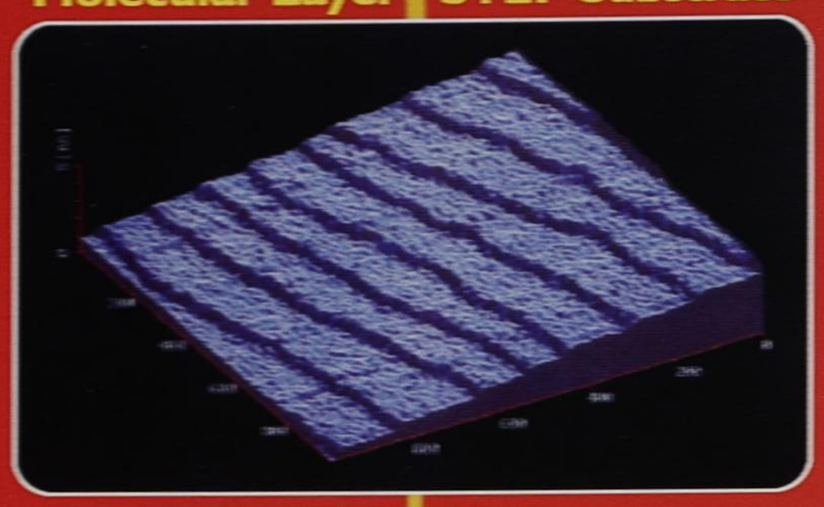
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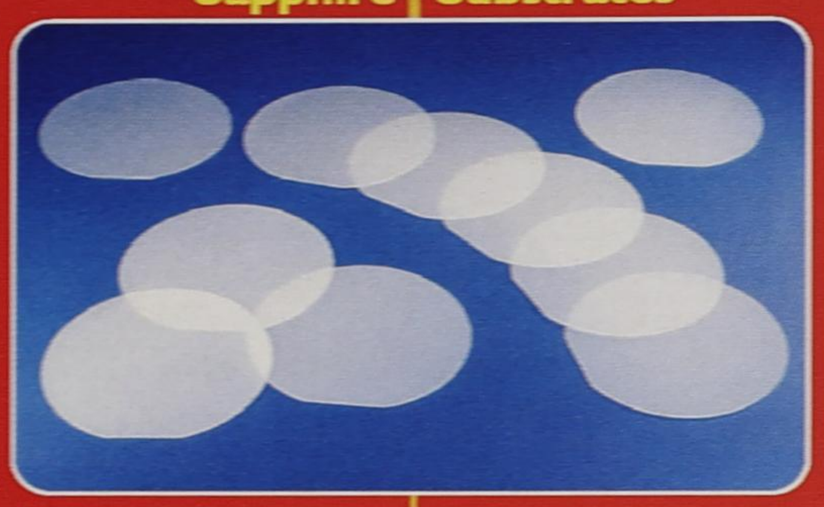
ULTIMATE FLATNESS

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(Orientation) | (0001)
(Roughness on terrace surface) | Ra≦0.05nm
(Step hight) | 0.21nm

Sapphire | Substrates



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lines, but half of all international air freight is carried as "belly cargo" on passenger planes. Within two days of the attacks the semiconductor industry began to see the impact, as shipments between US fabs and their packaging operations in Taiwan and the rest of Asia slammed to a halt.

One week after the attacks the FAA lifted the outright ban, but imposed much more stringent security guidelines on all air cargo. As this issue went to press, carriers were reported to be making good progress on working their way through the accumulated freight backlog. But even after the situation has stabilized it is expected that freight will travel more slowly and that costs will rise. "Just-in-time" inventory control systems at some companies may need to be overhauled in response, especially if future sudden interruptions in service seem likely to occur.

A few of the US compound semiconductor fabs reported that, one week after the attacks, they were beginning to feel the pinch as supplies of some critical materials run low. Suppliers in Europe and Asia who buy materials from the US will also be affected, and not even sea traffic is immune. "We are trying to ship our European ocean freight, which normally ship out of Port Newark or Elizabeth to Europe, via Canada," said John de Neufville of Voltaix, a New Jersey-based producer of germane and other flammable and toxic gases. "We shall see whether this attempt to solve the problem causes more than one week's delay, as presently scheduled. A longer period may cause customer problems."

Defense

The nature of the response to the attacks by the US and other countries is still largely unknown. It is therefore difficult to predict what the impact on the defense industry will be. Defense contracting in the compound semiconductor industry has moved to the back burner in recent years, but it should be noted that as recently as 1995, military applications and related R&D sustained the US compound semiconductor industry. Via US Department of Defense programs such as MIMIC and MAFET the US GaAs industry was a major contributor toward, and a huge beneficiary of, efforts to improve the radar and electronic warfare capabilities of the US military.

It seems likely that new technology efforts will be needed for the war against terrorism. Even the most sophisticated of today's technology was not appropriate to deal with the attacks on 11 September. New ideas (laser-based biometrics, microwave-based transmission of video from the cockpits of airliners to ground control, etc) are already being circulated. However, it is yet to be seen whether increased funds will be available for their development.

On a personal note

In June 1963, when a divided Germany was the front line in the Cold War, US President John F Kennedy visited the Berlin Wall and famously said: "Two thousand years ago the proudest boast was *civis Romanus sum*. Today, in the world of freedom, the proudest boast is *Ich bin ein Berliner*."

While Pfau did not revise his estimates for wireless handset sales (380–400 million units in 2001; 440–460 million units in 2002), he does believe that the recently renewed interest in mobile communications could help to move sales "closer to the higher part of the ranges".

In the aftermath of the attacks, I received an e-mail from a reader in Berlin who expressed his sympathy and his sense of personal involvement in the event by saying that "we are all New Yorkers now".

Within the pages of this magazine we have always avoided political or personal commentary, believing that such content is out of place in a trade publication. But the impact of the events we have just seen is of such a magnitude that they cannot go unremarked. It seems to this author that they were attacks against liberty, individualism, and a belief in the constructive progress of the human race. I also think that these three things are what make high-tech industries tick.

Our industry may be small, but it is very cosmopolitan, with every region of the developed world making important contributions. For myself, for the reader in Berlin, and I'm sure for many others, the devastation at the World Trade Center and the Pentagon has sharpened our understanding of just how interconnected we all are, personally and professionally, across the globe.

Legal battle intensifies as Shuji Nakamura sues Nichia

By Jon Newey

The legal battles surrounding nitride-based blue LEDs took a new turn on 23 August when Shuji Nakamura filed a lawsuit in the Tokyo District Court against his former employer Nichia. Nakamura is claiming ¥2 billion ($17 million) in damages from Nichia for failing to properly compensate him for his work with the firm. He is also claiming rights to one-thousandth of the patent for the basic production method of blue LEDs, which was the key result of his work at Nichia. Nakamura says he is entitled to compensation under Article 35 of Japan's Patent Law which gives inventors the right to "due compensation" for their achievements from employers.

So far most of the legal activity concerning nitride-based blue LEDs has been based around infringement lawsuits between the different companies that develop and manufacture such devices (see *Compound Semiconductor* August 2001, p21). The case will be eyed with close interest, as it is uncommon for credit for a patent to be contested between an individual and his previous employer.

Insufficient compensation

Nakamura's troubled relationship with Nichia has been chronicled in an autobiography (see *Compound Semiconductor* August 2001, p25). Nichia began commercializing blue LED technology in 1993, and Nakamura was largely responsible for the approximately 100 patents the company holds in this field. For any patent applications he filed, Nichia paid him ¥10 000 ($85) with another ¥10 000 paid upon the patent being granted. Given the now-obvious commercial value of the patents arising out of his work, Nakamura clearly feels this was not "due compensation" and more money should be paid to him. After 20 years employment, Nakamura left Nichia at the end of 1999 and headed for the University of California at Santa Barbara (UCSB), where he was recently named as the first recipient of the Cree Chair for Solid State Lighting and Displays (see page 15).

Suits and countersuits

Another factor prompting Nakamura's action was the lawsuit filed against him in December 2000 by Nichia. This was apparently motivated by Nichia's fear that Nakamura would disclose confidential information to UCSB and other organizations including Cree, with whom Nakamura has a consulting contract. "My frustration built up because the Nichia suit took so much time away from my teaching [at UCSB]," explains Nakamura, "and I decided to sue them in return."

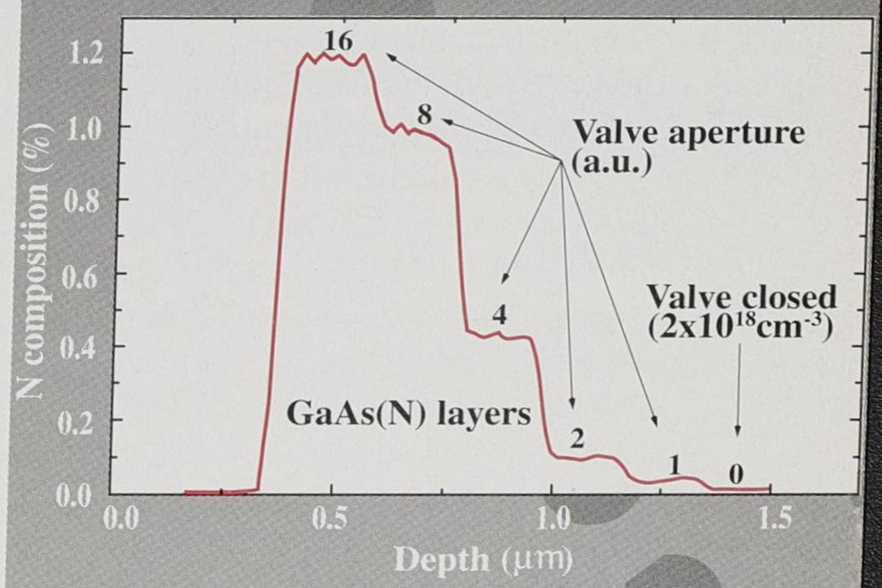
"Japan became an economic giant thanks to manufacturers and their engineers, but Japanese engineers are treated very poorly," continues Nakamura. "Some Japanese companies have begun paying engineers bonuses of ¥10 million ($85 000), but that is almost nothing compared to compensation levels in the US." Nakamura hopes that by filing this suit he might help improve the treatment of engineers in Japan. "They will benefit if I win," he says.

Inventions made while working for a company are usually viewed as company property, and individuals rarely claim rights to their achievements. This pattern may well change as there are a growing number of legal disputes between companies and researchers. Nakamura's case is seen as important because of its high profile, and because the outcome could have major implications for Japanese companies and their employees. In Japan such actions are thought to be the result of the changing labor market and employment system. The job-for-life with regular promotions, bonuses and salary rises is being left behind as Japanese firms cut costs to compete in tough global markets. Employees are far more willing to move to other companies and the reduction in long-term job security means they want to be rewarded for their efforts now, not after decades of service.

In the November issue of
COMPOUND SEMICONDUCTOR
Nitrides
Features and news from the nitrides world, including the challenges of growing GaN LEDs on sapphire and silicon, advances in microelectronics devices and a comprehensive research update.

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Veeco Instruments acquires Applied Epi

By Richard Dixon

Veeco Instruments has acquired Applied Epi, an MBE component and system manufacturer, in a deal worth just over $132 million (approximately 4 million Veeco shares and $30 million in cash). Last year, Applied Epi was looking to raise cash from the equity market, and filed for an IPO in September 2000. With the industry downturn creating a highly unfavorable climate for IPOs, these plans were put on hold indefinitely.

Veeco, which is based in Woodbury, New York, supplies process and metrology equipment to optical communications, data storage, research and semiconductor markets (see box). The company's products include ion-beam etch and deposition equipment, and PVD and CVD systems, in addition to a comprehensive range of test, metrology and characterization tools.

The acquisition of Applied Epi bolsters Veeco's portfolio with the addition of MBE deposition systems for research and production, together with related MBE equipment such as effusion cells. The company also adds key accounts in the optoelectronic and wireless sectors to Veeco's fast-growing telecommunications base, which grew in sales from $20 to $80 million in 2000.

"Applied Epi is a profitable, well-managed technology leader, with a large installed base of MBE systems," said Edward Braun, Veeco's chairman, president and chief executive officer. "By adding its MBE capabilities, we will be well positioned to play a leading role in the future integration of compound semiconductor and silicon device development. This important addition to our breadth of technologies will allow us to extend our customer base for optoelectronic telecommunications and wireless growth opportunities."

Applied Epi is expected to achieve $50 million in sales this year. Based in St Paul, Minnesota, the company has an installed base of over 200 pilot production and research reactors, and more than 5000 deposition cells. Applied Epi recently entered the production MBE market with its GEN200 and GEN2000 systems. The latter is a 7 × 6 inch system designed for high-volume manufacturing. The company has sold at least six production systems to companies such as RFMD, Picogiga, IQE and Agilent. Since the merger was announced, says Edward Braun, Applied Epi has shipped a dual reactor GEN2000 to IQE.

The rise and rise of Veeco Instruments

The acquisition of Applied Epi is the most recent in a spate of deals involving Veeco over the last three years. The Veeco "empire" now includes MBE epitaxial products, deposition and etch systems, and metrology and characterization tools. More than half (56%) of the company's products relate to processing, and 41% are used for metrology.

Veeco recorded $387 million in sales last year, and 44% were in the data storage market. About one-third of sales were in the research and semiconductor (primarily silicon processing equipment) markets, while just under a quarter served the company's fast-growing telecommunications customer base. The latter category includes processing and metrology equipment used in the manufacture of active and passive devices, e.g. pump lasers, dense wavelength-division multiplexing filters and amplifiers.

Veeco employs 1400 staff in more than 20 sales and service locations, and at five manufacturing facilities in the US. Veeco's stable includes:

Applied Epi
Acquired in September 2001, Applied Epi makes production and research MBE reactors and effusion cells.

ThermoMicroscopes
Now named TM Microscopes this former subsidiary of Thermo Electron, acquired by Veeco in July 2001, sells metrology products, including atomic force and scanning probe microscopes.

CVC
In February 2000, Veeco merged with CVC, a publicly-traded manufacturer of cluster-tool equipment for PVD, ion-beam etching and atomic layer deposition.

Monarch Labs
Makes quasistatic testing systems.

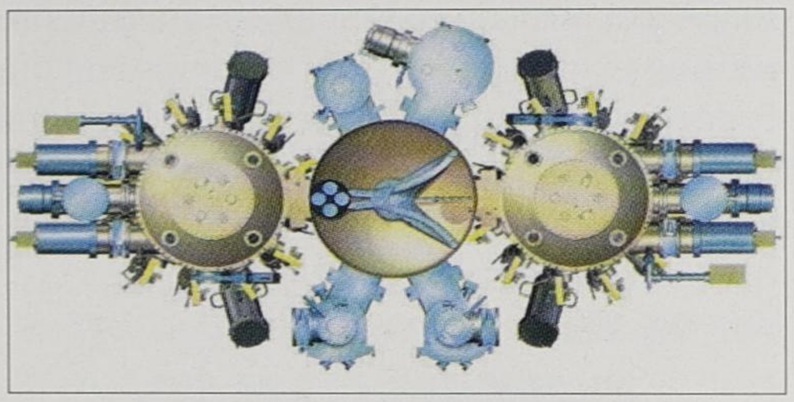
OptiMag
Makes optical defect inspection equipment.

Ion Tech
Makes ion-beam deposition systems.

Digital Instruments
Makes atomic force and scanning probe microscopes.

MRC
Makes PVD systems.

WYKO
Makes laser interferometers and optical profilers.



Top view of a dual-chamber version of Applied Epi's Gen 200 production MBE reactor. The system's high-vacuum cluster tool arrangement lends itself to the integration of further processing and metrology tools.

Silicon manufacturing approach

"Veeco brings the worldwide sales and service support and financial resources we need to serve our expanding customer base," said Applied Epi's president and chief executive officer Dave Reamer. "This merger will also benefit us in our quest to bring a more silicon-style volume manufacturing model to the compound semiconductor market. Veeco and Applied Epi have been on the same track in this respect, and the merger with Veeco solidifies this approach."

"We also foresee a range of possible configurations that leverage the cluster-tool arrangement of our MBE system," added Reamer. "For example, it would be possible to bundle Veeco's mid-level processing and metrology tools with Applied Epi's reactor, which contains the requisite ultra-high vacuum environment."

As part of the deal Reamer will retain his role as the company's president and chief executive officer, while founder Paul Colombo will support Applied Epi in a technical advisory role.

DRY IN/DRY OUT

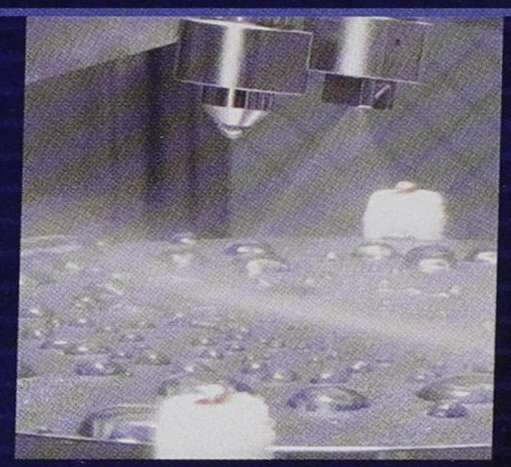
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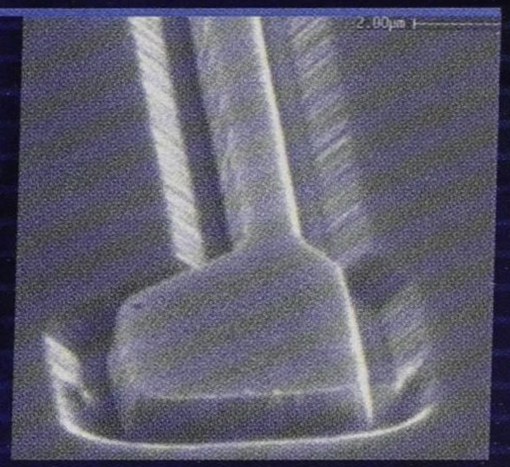
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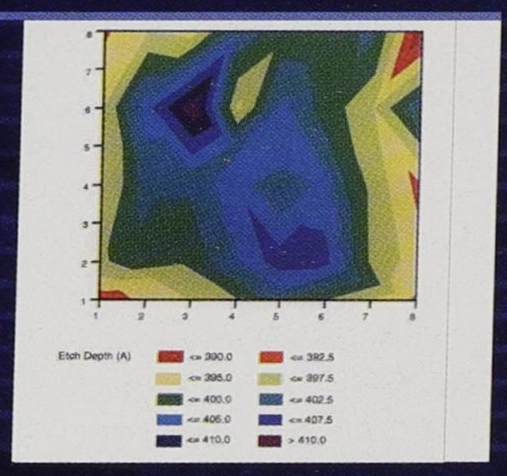


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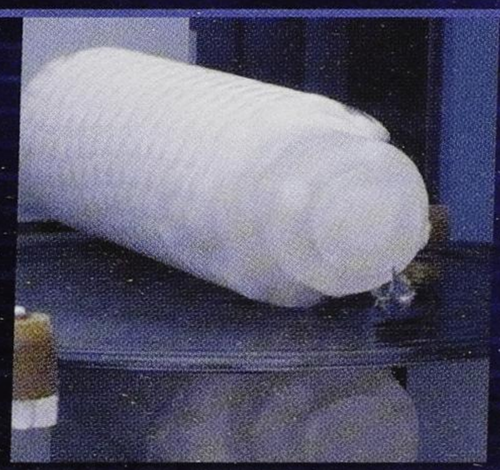


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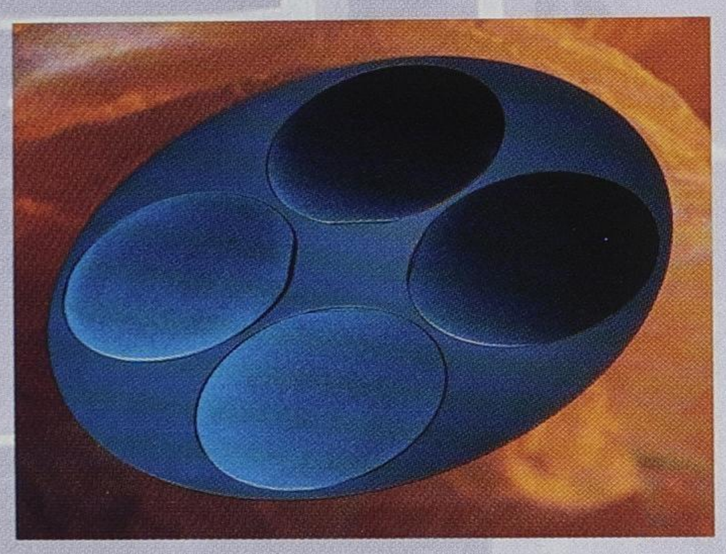
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European Microwave Week draws the crowds in London

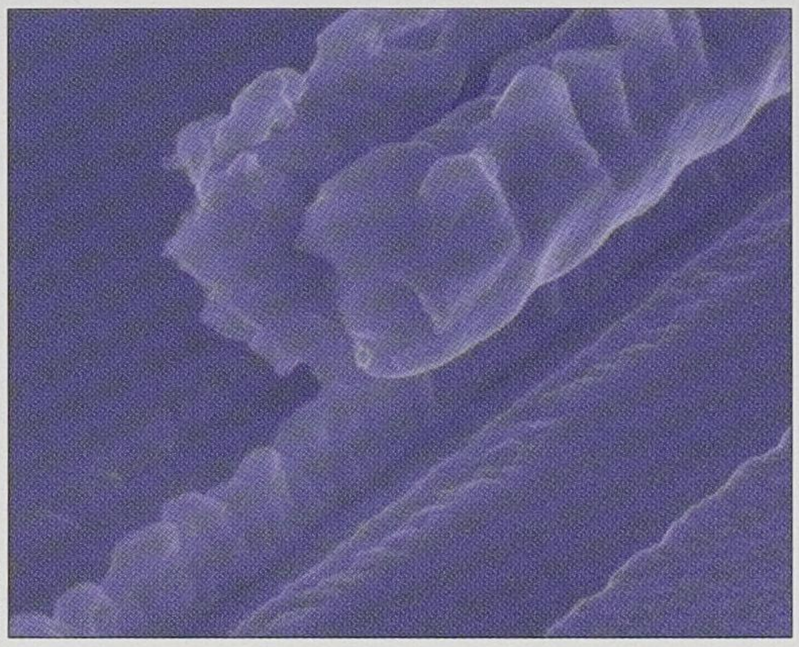
The fourth European Microwave Week, incorporating the Gallium Arsenide Applications Symposium (GAAS 2001), took place in London on 24–27 September. The technical symposia and related workshops and short courses attracted more than 1600 delegates, while about 200 companies had booths in the exhibition, among them some GaAs IC manufacturers. The European slant to the meeting was certainly no deterrent to visitors from the US and Asia, although restrictions on travel caused some companies to withdraw from the exhibition at the last minute. Significantly, Taiwanese companies were well represented, with WIN Semiconductors, Suntek and Hexawave among those present. For the first time, Suntek was publicizing its HBT foundry services; mass production is scheduled for October. Other companies made announcements and launched products, a few of which are described below.

Raytheon, OMMIC launch new MHEMT processes

OMMIC and Raytheon RF Components have separately announced the commercial availability of metamorphic HEMT (MHEMT) processes. Both companies are focusing their new processes on low-noise microwave and millimeter-wave applications, as well as the optical comms market at 40 Gbit/s and above.

Raytheon's process, which uses 4 inch GaAs wafers, routinely gives an f_t greater than 150 GHz and an optimum noise figure (f_{min}) of less than 0.7 dB at 25 GHz. The process achieves high yields through self-alignment and etching the gates selectively. "Transferring the process from the research fab was relatively seamless," said Colin Whelan, senior scientist at Raytheon's Advanced Device Center. "The first production wafers showed nearly identical electrical performance."

The OMMIC process also results in an f_t of 150 GHz, together with a breakdown voltage of 10 V. A 0.13 μm mushroom gate is placed asymmetrically between the drain and source, and a double recess channel enables the high breakdown voltage. OMMIC also offers standard options including backside via holes for low inductance grounding, and the ability to package the MHEMT devices through a bump-bonding process. OMMIC will be offering the process to selected partners through the remainder of 2001.



OMMIC

SEM image showing OMMIC's MHEMT transistor with a 0.13 μm mushroom gate.

MHEMTs have been the subject of considerable research and development efforts over recent years because they enable the fabrication of devices operating at high frequencies with low noise levels on GaAs substrates. This helps reduce costs because high indium-content device layers with high electron mobilities can be grown on GaAs wafers. These are significantly cheaper and more robust than InP wafers, and readily available up to 6 inches in diameter. A metamorphic InGaAs buffer layer is grown on the GaAs substrate, transforming the lattice parameter at the growth surface to enable the further growth of lattice-matched layers with high indium content.

RFMD's PA module cuts design effort

RF Micro Devices has launched a new tri-band high-efficiency PA module. The RF3110 incorporates two GaAs-based HBT power amplifiers and a CMOS power control ASIC, which are surface-mounted on a laminate substrate. The module is designed for use as the final RF amplifier in GSM, DCS and PCS cellular handsets operating in the 880–915, 1710–1785 and 1850–1910 MHz bands.

Integrated power control allows selection of the transmit power level in GSM networks. This reduces costs and simplifies handset design by eliminating the need for separate power control ASICs and other circuitry.

"The implementation of transmitter power control is one of the most engineering-intensive and time-consuming aspects of GSM handset design," said Joe Grzyb, director of RFMD's PA product line. Typically, engineers spend months developing the power control loop and control software to meet all GSM transmitter requirements. "The RF3110 gives engineers the ability to implement the PA and power control within minutes," he added.

The module comes in a 10 × 10 mm package and is priced at $4.10 in quantities of 100 000. Output powers at 3.5 V are +35 dBm and +33 dBm for GSM and DCS/PCS, respectively. RFMD expects to manufacture similar highly integrated solutions in the future, which may include incorporating filters and T/R switches into the PA module.

Best of both worlds for UMS and GCD

United Monolithic Semiconductors (UMS) is joining forces with Global Communications Devices (GCD), a fabless supplier of silicon-based wireless networking components based in North Andover, MA. The agreement is for the development of highly integrated chipsets for the wireless communications market. UMS manufactures GaAs MMICs for microwave and millimeter-wave applications, while GCS is a venture-funded company developing products mainly for the IEEE 802.11 standards for local-area and enterprise networks, as well as Bluetooth applications.

UMS and GCD will combine GCD's silicon-based networking transceivers and mixed signal technology with UMS's high-frequency GaAs components. "This will allow both companies to combine their respective expertise in two different semiconductor technologies," said Geoffrey Dawe, president and chief executive officer of GCD. "It will also allow GCD to benefit from UMS's foundry and worldwide marketing presence."

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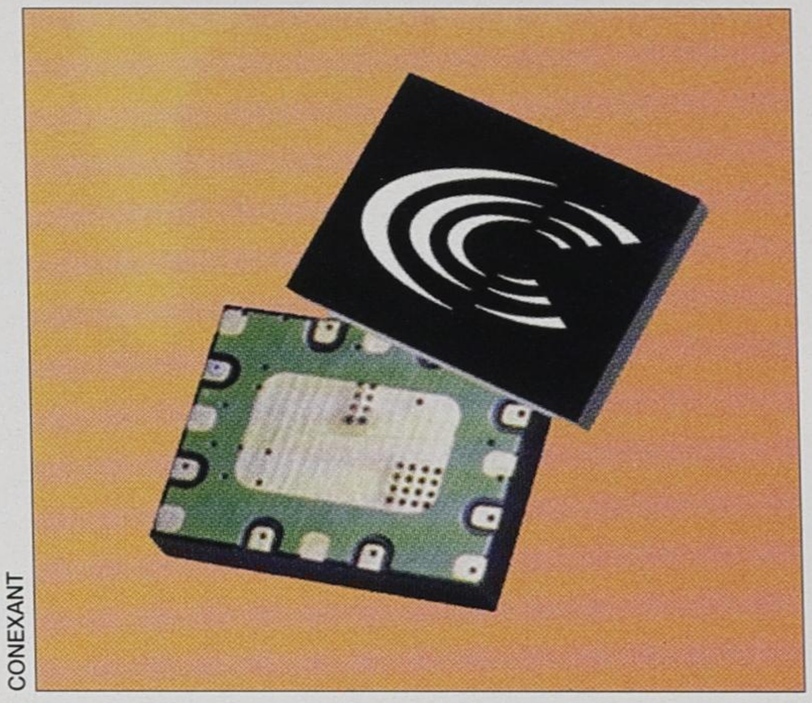
Samsung and Acer buy HBT PA modules from Conexant

Conexant will supply GaAs HBT power amplifier modules to Samsung Electronics and Acer Communications & Multimedia (Acer CM) under separate agreements. The Samsung contract marks the shipment of Conexant's 100 millionth GaAs HBT power amplifier module.

Acer CM selected Conexant's dual-band power amplifier module for use in next-generation digital cellular handsets, primarily for the Asian and European markets. Conexant's CX77301 PA module is based on the 50 GHz GaAs HBT process and suits 900 and 1800 MHz GSM operating bands. The module also supports general packet radio service (GPRS) operation.

Based in Taoyuan, Taiwan, Acer CM launched its own mobile-phone design in 1994. This product replaced desktop monitors as a major revenue stream for the company, which now also services the display, storage, imaging, wireless and broadband markets.

"We're pleased to expand upon our relationship with Conexant and believe that their dual-band power amplifier module will allow us to deliver highly reliable, high-performance products to our customer base in a cost-effective and timely manner," said Irwin Chen, the vice-president and general manager of Acer's wireless communication business.



CONEXANT

The CX77301 PA module contains 50Ω input and output matching. This allows fewer external components and integration of multiple devices and power amplifier circuitry into a small-form-factor package.

Korean handset makers choose TriQuint

TriQuint has received contracts from two Korean manufacturers to supply power amplifier modules for cellular handsets. Samsung Electro-Mechanics Co chose TriQuint's CDMA power amplifier MMICs for use in its CDMA/AMPS and AMPS modules, which are currently being designed into several models of phones for employment both in Korea and the rest of the world.

Meanwhile LG Innotek has selected TriQuint's CDMA power amplifier for use in its LG series CDMA power amplifier module, which is also destined for Korean and worldwide handset markets. Based in Seoul, LG Innotek's interests include components for the telecom and electronic defense industries.

"TriQuint is delighted that its power amplifier solutions have been chosen for these new power amplifier modules," said Rupert Prince, director of marketing at TriQuint. "The CDMA power amplifier has demonstrated a significant improvement in RF performance over the power amplifiers which are currently available on the market. We expect that leading-edge handset makers will rapidly adopt this module solution."

Ericsson receives PAs from RF Micro

RF Micro Devices has begun shipping power amplifiers to Ericsson, which the Swedish mobile-phone manufacturer will use in its T39 and R520 series handsets. These phones allow operation in most countries using the triple-band (900/1800/1900 MHz) GSM standard. Both handsets also feature Bluetooth wireless and general packet radio service (GPRS) technology, which enables high-speed Internet and other types of data communications. RFMD's MMIC PA is based on the company's high-efficiency GaAs HBT process.

"We believe our experience and leadership in the design and manufacture of GaAs HBT power amplifiers together with our ability to support volume production contributed to Ericsson's decision," said Joe Grzyb, RFMD's director of power amplifier products.

Celeritek seals deal with "a major US handset maker"

Celeritek will supply InGaP HBT power amplifier modules to a major US handset manufacturer, believed to be Motorola, for use in developing prototype next-generation handsets capable of CDMA 1X. The modules, CSM2104C and CSM2105C, suit cellular and PCS CDMA and CDMA 1X applications. Celeritek expects production orders in the third quarter of fiscal 2002, and to ramp production up in the fourth quarter.

"The use of our Adaptive power amplifier module represents the next step in our strategy to provide the most integrated solutions based upon InGaP HBT technology," said Tamer Husseini, Celeritek's president and chief executive officer. "While it would be premature to estimate the impact of this order on the current year's revenue, we believe this design win is critical for our future growth."

RF Nitro in global distribution tie-up

RF Nitro Communications has signed a global distribution deal with Richardson Electronics, a supplier of RF and microwave components. The agreement covers RF Nitro's broadband InGaP/GaAs HBT products and power amplifier MMICs (see *Compound Semiconductor* June 2001, page 23). Richardson will also stock die-level products and high-frequency evaluation boards for testing amplifier and transistor prototypes.

"RF Nitro's current high-performance products will effectively fill a market niche in the 6–20 GHz range, and its broadband products will address customer demands in the fiber-optic communications area," said Chris Marshall of Richardson. "We are also excited about the potential of RF Nitro's developing GaN technology." RF Nitro supplies GaN epitaxial materials for the microelectronics market and is developing 4 inch GaN wafer technology to produce amplifiers for high-power, high-frequency applications.

This month's cover story on GaAs processing begins on page 61.



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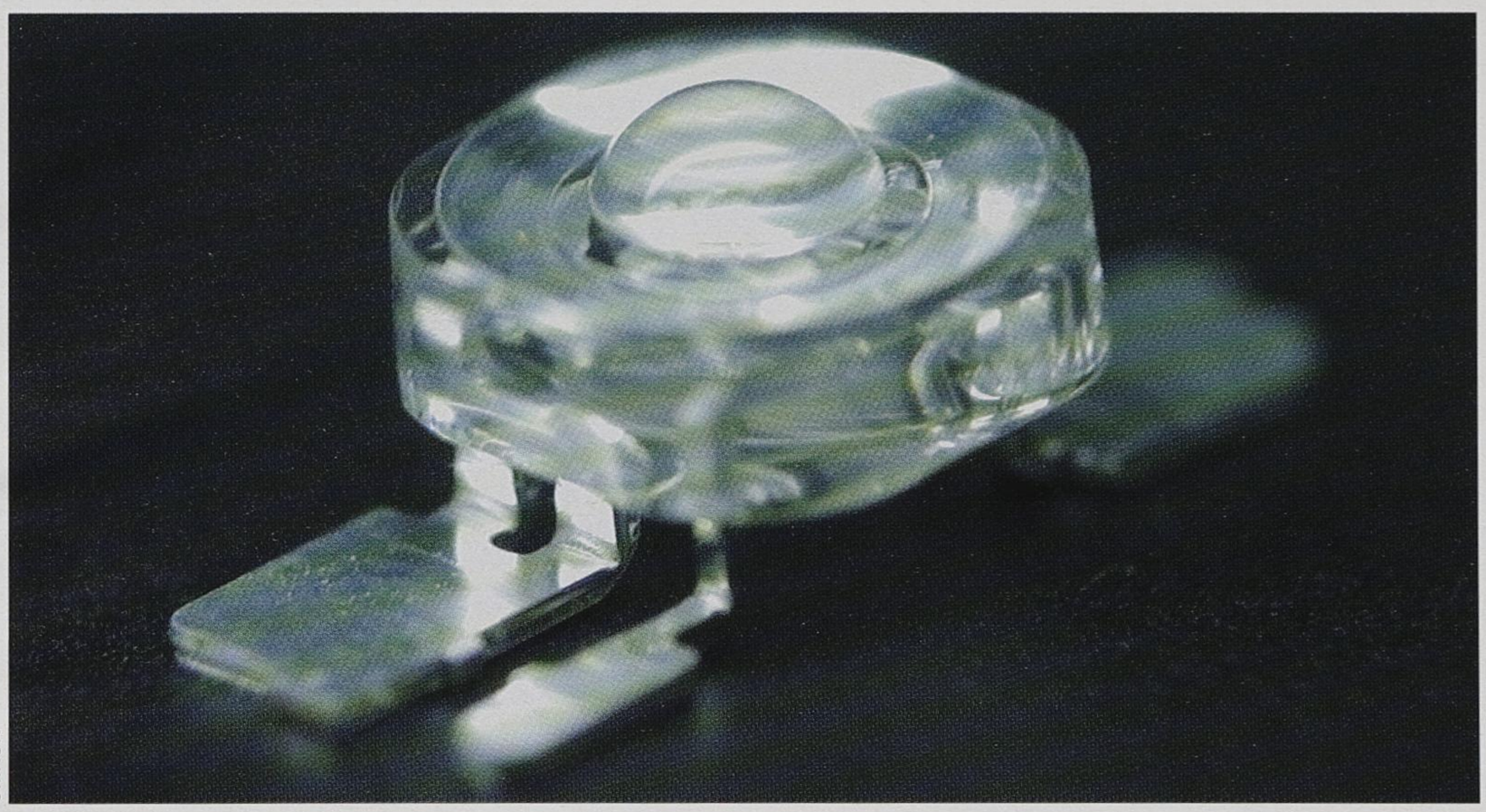
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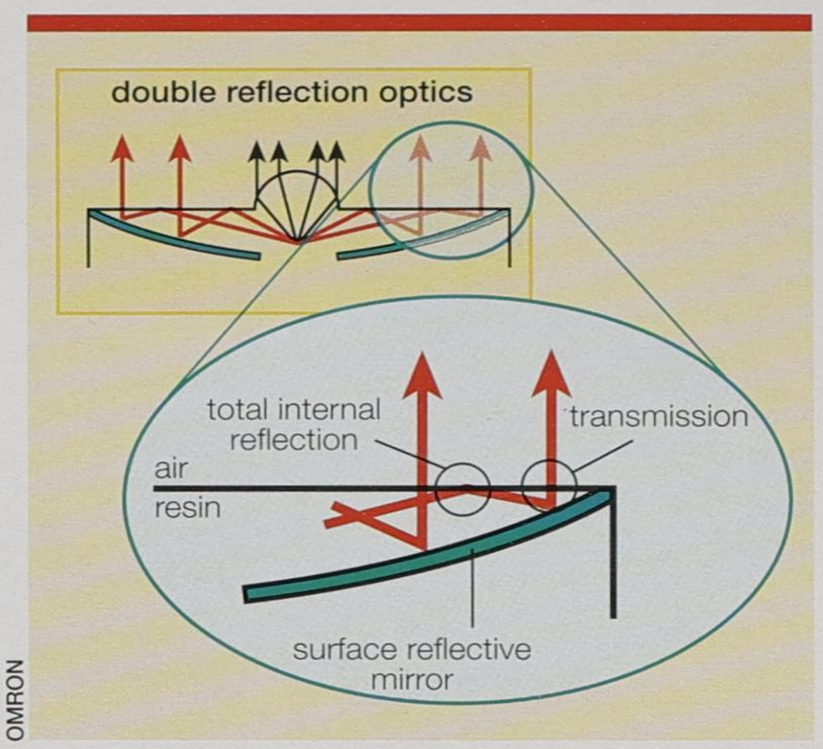
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A packaged LED incorporating Omron's double reflection (DR) LED technology.



OMRON

Schematic showing Omron's DR LED technology, which uses a mirror at the back of the package to counteract total internal reflection at the air–resin interface.

Two Japanese companies, Omron and Stanley Electric, are to collaborate on the development and production of high-luminance LEDs using Omron's double reflection (DR) LED technology, which yields LEDs with approximately twice the brightness of conventionally packaged LEDs. Omron's proprietary optical system improves the extraction of light from packaged LEDs. Light that is prevented from escaping from the surface of the LED package by total internal reflection at the air–epoxy resin interface is reflected from an internal mirror at the back of the package. The optical system allows the efficient use of light from LED chips with a wide emission angle, and is also suitable for creating geometrical shapes such as large circles and ovals. Using the external optical system to improve brightness, instead of changing the properties of the light-emitting semiconductor material, means that improvements are independent of emission wavelength. Omron has successfully doubled the brightness of red, infrared, blue and white LEDs.

Stanley Electric is an established LED manufacturer, and has developed heat dissipation and device production technologies that allow the use of large drive currents of up to 250 mA, some five times higher than conventional lamps. The companies expect these technologies, in combination with the DR-LED optical system, to achieve a tenfold increase in brightness enabling products such as signal lamps to contain significantly fewer LEDs. The collaboration will see Stanley Electric take responsibility for production of the new DR-LEDs, combining technologies from both companies, with Omron and Stanley Electric responsible for marketing the product.

- In more news, Stanley Electric expects consolidated operating profits to drop 25% in the six months ending September 30, compared to the same period one year ago. Sales of lighting products for electronic equipment, such as LEDs for cellular phones and light sources for personal computer LCDs, will fall by 20–30%.

Nakamura is first holder of Cree Chair

Shuji Nakamura has been named as the inaugural recipient of the Cree Chair of Solid State Lighting and Displays at the University of California, Santa Barbara (UCSB). Late last year, Cree pledged $1.2 million to the College of Engineering at UCSB toward the endowment of the Cree Chair, and to support research in the field of GaN-based electronic materials and devices (see *Compound Semiconductor* Dec 2000/Jan 2001, p22).

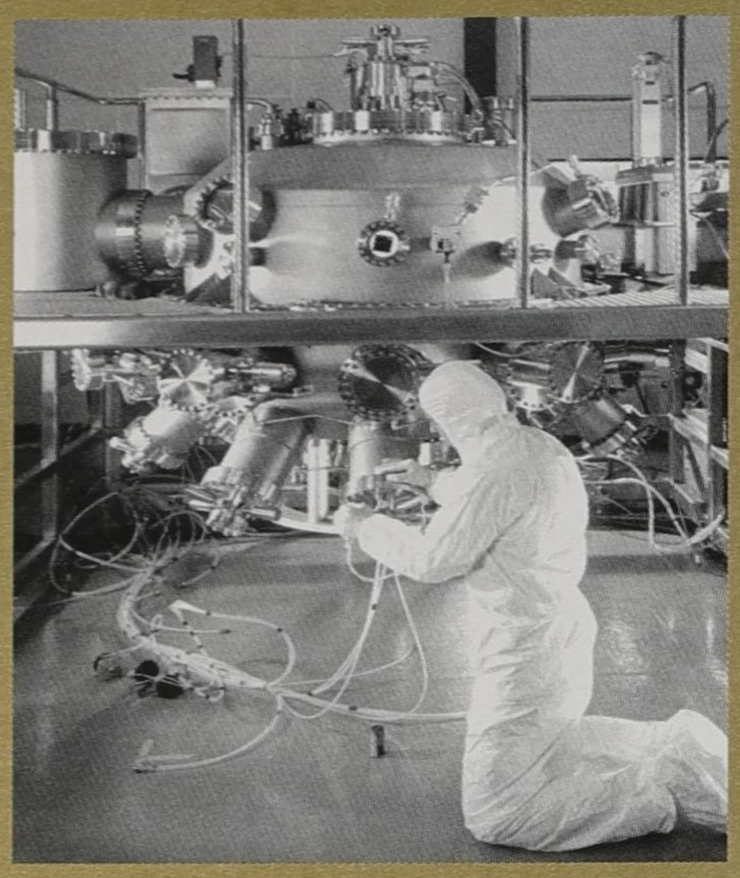
Nakamura is famed for his work on GaN-based LEDs and blue lasers at Nichia, and is the recipient of numerous awards including the Honda Prize, the MRS Medal and the Rank Prize. In late 1999, Nakamura left Nichia and is now a materials professor at UCSB and director of the Center for Solid State Lighting and Displays. He has authored 170 scientific papers and three books, and also consults for Cree.

"We are very pleased to support UCSB's commitment to GaN-based research and are excited that Shuji Nakamura has been named the recipient of the Cree Chair," said Cree's chairman, Neal Hunter. "Shuji Nakamura has been widely recognized for his work on GaN-based LEDs. Energy-efficient white LEDs [based on GaN emitters] are being targeted as replacements for incandescent lights, and are expected to use significantly less energy than conventional incandescent bulbs. We believe a large number of white-light applications will emerge as solid-state illumination technology continues to evolve."

"I am honored to be the first holder of the Cree Chair in Solid State Lighting and Displays," said Shuji Nakamura. "Cree is recognized worldwide as a leader in solid-state lighting and as a key pioneering company in the development of the compound semiconductor technology that uses GaN-on-SiC. Cree financially supported the Solid State Lighting and Displays Center here at UCSB from the beginning, and we are grateful for that support."

- Cree Asia-Pacific has opened a Southeast Asian sales office in Kowloon, Hong Kong, to facilitate business transactions and act as a liaison between Cree's customers in the region and its corporate headquarters in Durham, NC.

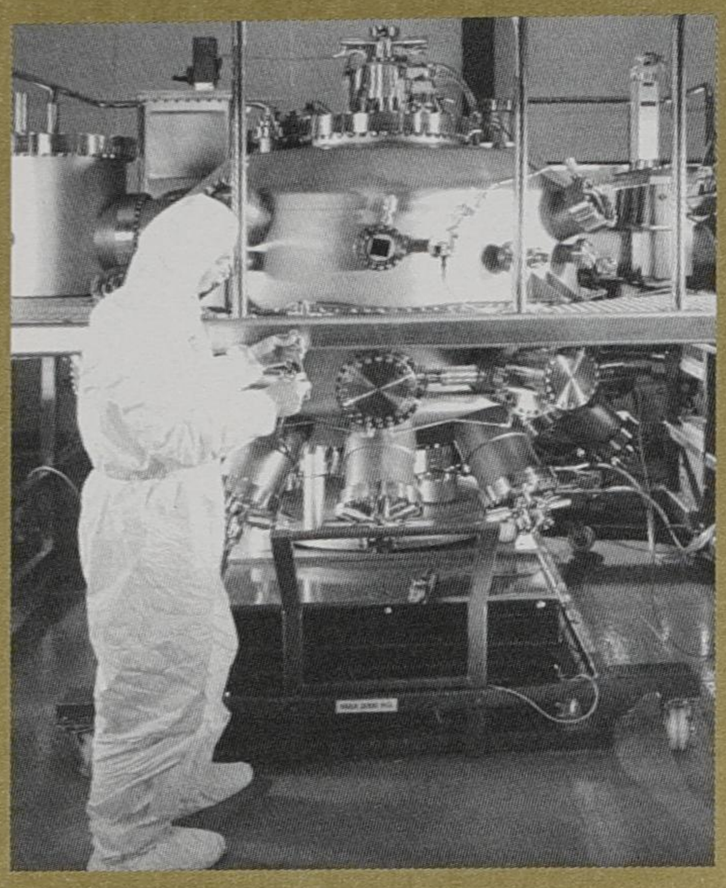
Increasing MBE uptime - it's just become as easy as 1, 2, 3...



1 *The system is vented and quickly prepared for turn round to begin.*

You already know the turn around cycle for MBE - vent, reload, service, pump-down and bake. You don't have to do it very often, but when you do it's a difficult and slow process. And every minute the system is not working is costing you time and money.

Now there's a way to significantly reduce this wasted downtime. VG Semicon's unique and exclusive chamber seal technology means the V150 is the first production MBE system ever that allows quick and easy removal of the entire source assembly.



2 *An hydraulic trolley is rolled underneath and takes the weight of the bottom half of the growth chamber. The four locating bolts are quickly removed.*

You no longer have to access individual sources, you no longer have to clean up the system through small ports. The whole chamber can be opened up in minutes for unrivalled access, giving you fast source reloading and easy clean up.

And when you're ready to get going again, closing the chamber is just as simple and our unique bakeout enclosure and exclusive AsO pumping system then provide the fastest bake in the industry. In fact you'll be up and running in one third of the time of other MBE systems, providing weeks of extra growth time.



3 *The trolley is lowered at the touch of a button and the entire lower section of the growth chanber is wheeled out for easy cleaning and source loading.*

The V150 already gives you the highest wafer throughput of any MBE system, and every added week of uptime will significantly improves your profitability still further. Which, in a business where time is money, means a definite edge over your competitors.

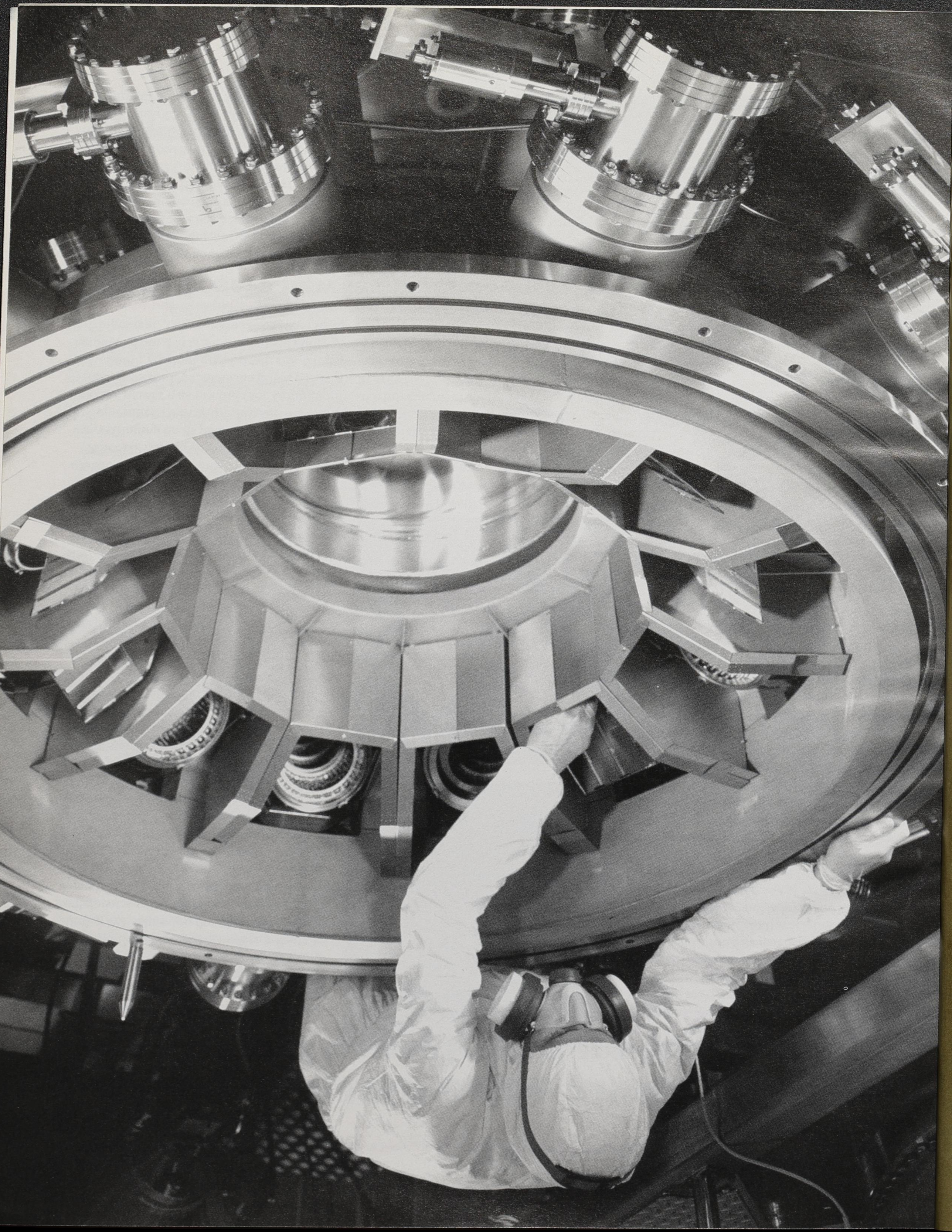
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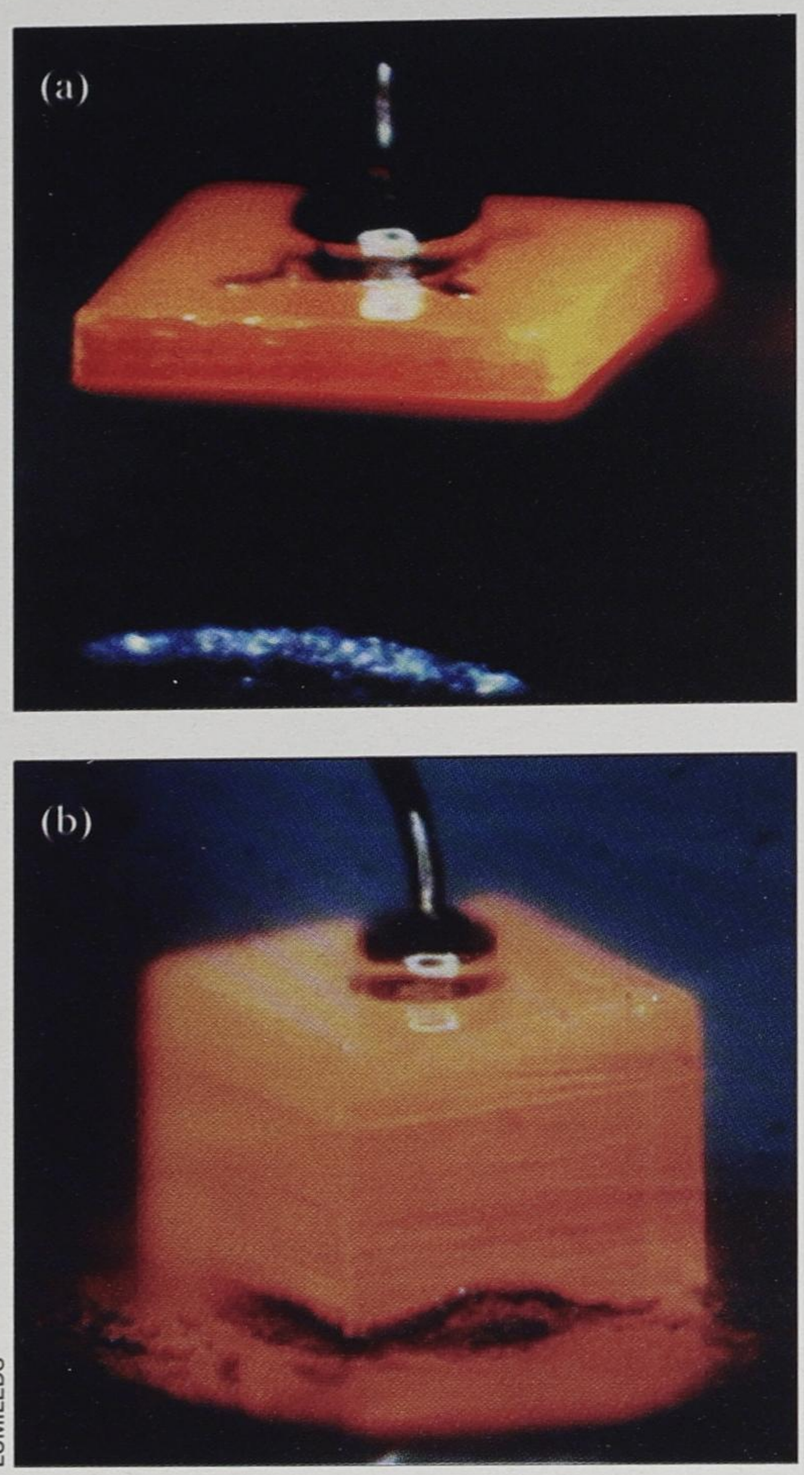


LumiLeds and UEC settle AlInGaP LED litigation and consider future partnerships

LumiLeds Lighting, Agilent Technologies and United Epitaxy Company (UEC) have settled their pending litigation concerning US patent no. 5,008,718, which is now owned by LumiLeds (see *Compound Semiconductor* Sept/Oct 2000, p19). Although the exact terms of the settlement were not disclosed, the parties have agreed to dismiss all claims and counterclaims asserted against each other. In a separate but related agreement, LumiLeds has granted UEC a license relating to several patents, under which UEC will pay a license fee and royalties in undisclosed amounts.

The performance of AlInGaP LEDs in the 560–680 nm range is compromised by poor current spreading and other problems. In 1989 Hewlett-Packard (HP) obtained a patent on a solution to the problem based on the use of a thick (2–30 μm) GaP layer grown on top of the active device. The GaP layer acts as a "window" because it has a higher bandgap compared with AlInGaP and is therefore transparent to light emitted from the LED. The p-type GaP layer is also highly conducting, and therefore reduces the "current crowding" around the top electrode, resulting in more uniform light distribution. Hewlett-Packard claimed that the GaP layer increased the light output by as much as five to ten times. The patent was transferred to Agilent as part of the spin-off from HP, and was subsequently transferred to LumiLeds.

After HP had alleged out of court that UEC was infringing on its patent, UEC responded in September 1999 with a lawsuit claiming that the patent was invalid (see *Compound Semiconductor* Dec 2000/Jan 2001, p13). In July 2000, Agilent and LumiLeds filed a counter-claim that UEC was indeed guilty of infringement. The case was scheduled to go to trial later this year. Sources close to the case said that UEC was defending itself against the infringement charges on the grounds that it was using InGaP rather than GaP in its window layers. They also argued that the patent was invalid because of "obviousness". It is believed that LumiLeds' riposte was that the use of such a strongly lattice-mismatched material was highly "non-obvious". There is a >3% mismatch between GaP and GaAs; ordinarily this would generate enough defects to kill a device like an LED. However, HP was able to make it all work because of the thickness of the window layer and its distance from the active layer.



LUMILEDS

AlGaInP LEDs with (a) an absorbing GaAs substrate and (b) a transparent GaP substrate. Both have a GaP window layer.

Both LumiLeds and UEC expressed pleasure that the dispute has now been resolved, and spoke about the possibility of working together beyond the license arrangements that have been agreed. "We are pleased to reach an agreement in resolving the pending litigation," said Kuo-Hsin Huang, UEC's chairman of the board. "We're also happy that as part of the settlement, LumiLeds has agreed to consider partnering with UEC as a contract manufacturer for certain LumiLeds products."

"We are pleased that UEC recognizes the value of our intellectual property," said Mike Holt, chief executive officer of LumiLeds. "If LumiLeds wants to outsource absorbing substrate AlInGaP production in the future, we would consider using UEC as a supplier." LumiLeds' highest brightness AlInGaP products are transparent substrate LEDs, in which the absorbing GaAs substrate is removed and replaced by GaP using wafer bonding. To date, UEC has manufactured absorbing substrate LEDs but recently announced a fourth-generation design incorporating indirect wafer bonding to a transparent substrate such as glass or sapphire (see *Compound Semiconductor* September 2001, p51).

"UEC will benefit in the expanding LED market from this patent license and a possible business partnership," concluded Kuo-Hsin Huang . "We think this is a win-win settlement for both parties."

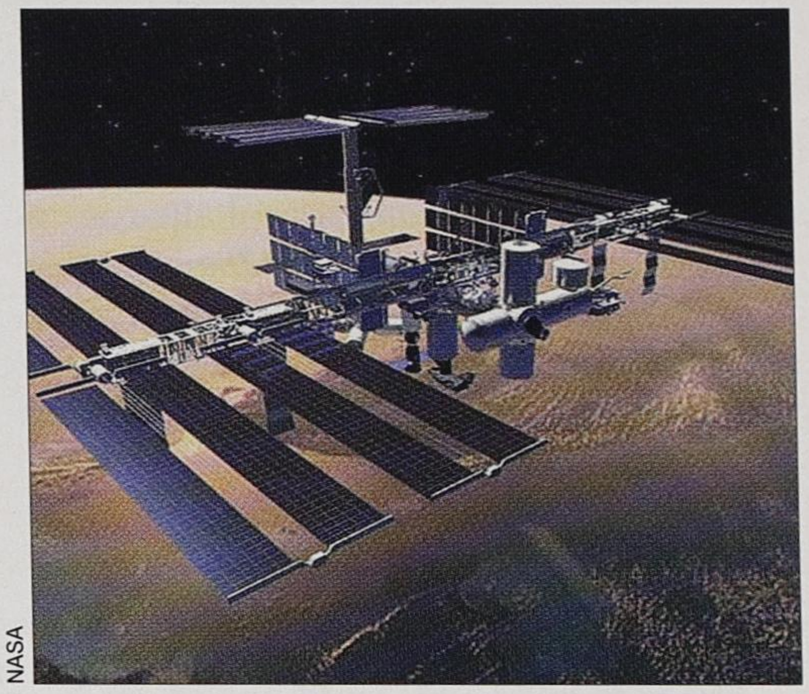
Toyoda Gosei's new lawsuits double the pressure on Nichia

As well as facing court action initiated by its most famous former employee, Shuji Nakamura, Nichia has been hit by two more patent infringement lawsuits filed by Toyoda Gosei, a rival LED manufacturer. Filed in Osaka District Court, the new lawsuits both seek injunctions against Nichia to prevent the manufacturing and sale of GaN-based blue LEDs. A lawsuit filed on August 10 alleges infringement against Japanese patent no. 3,026,102 entitled "A light-emitting GaN-based compound semiconductor device", which relates to LEDs with reduced operating voltage and higher light-emitting efficiency. The second lawsuit, dated September 3, relates to Japanese patent no. 3,209,096 entitled "A light-emitting semiconductor device using a group III nitride compound", which describes LEDs with improved luminous intensity, device characteristics and reliability. Toyoda Gosei alleges that Nichia is infringing both patents by making and selling GaN-based blue LEDs in Japan. In its press releases, Toyoda Gosei states that it "has been litigating against Nichia with respect to a number of patents...and will continue to enforce its intellectual property rights." The total number of lawsuits filed by Nichia and Toyoda Gosei against each other has now reached double figures.

Cree's GaN devices launched into space

GaN microwave devices manufactured by Cree have been installed aboard the International Space Station following the launch of the space shuttle Discovery. Cree, which is based in Durham, North Carolina, supplied GaN epitaxial materials and GaN HEMTs on SiC substrates, which were added to the Materials International Space Station Experiment (MISSE) to determine their radiation hardness for future satellite applications.

The experiment is the result of a joint collaboration between Cree and the Sensors Directorate of the Air Force Research Laboratories (AFRL), under a Dual Use Science and Technology program funded by the Department of Defense and Cree. The objective of MISSE is to develop wide bandgap semiconductors for microwave technology that can operate under extreme conditions such as a crowded or hostile electromagnetic spectrum, as well as within the constraints of mass, volume or prime power imposed by space environments.



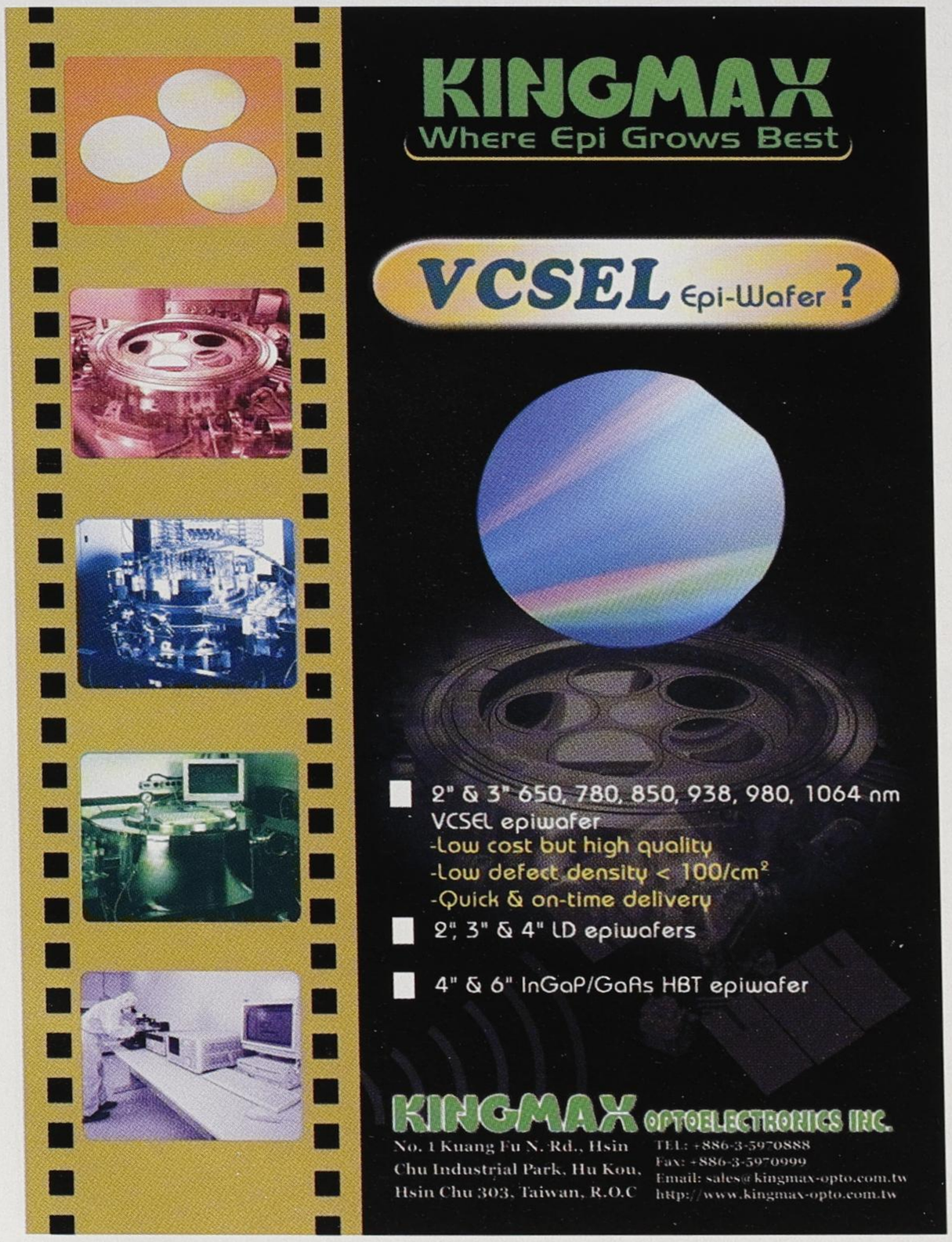
NASA

The International Space Station is currently home to a range of materials experiments, including radiation studies of Cree's GaN-based HEMTs.

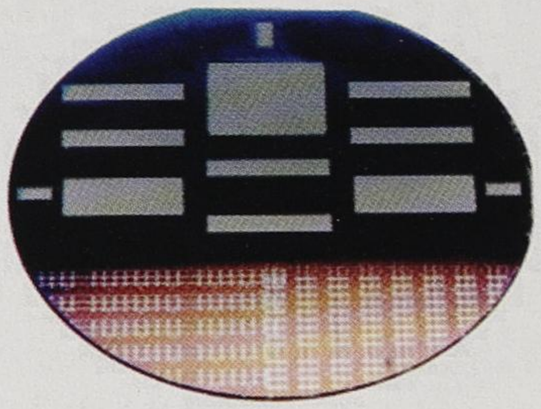
The radiation experiment was mounted onto the outside of the space station's airlock during the first space walk of the mission, and will be retrieved on a future shuttle mission for test and evaluation back on earth.

"We are excited about the rapid progress achieved for GaN microwave devices, and are anxious to determine their applicability to satellite communications and other space-based applications as a result of this experiment," said Thomas Jenkins of AFRL's Sensors Directorate.

Wide bandgap materials hold considerable promise for power applications in extreme conditions. Cree has previously reported total power for GaN microwave devices of 50 W at 10 GHz, and also demonstrated the first GaN MMICs grown on the company's semi-insulating SiC substrates. The latter devices have recently achieved 24 W of pulsed RF output power at 16 GHz, or about three times the highest RF output power of GaAs MMICs available at this frequency range.



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Sterling steps up SiC epitaxy and device production

Sterling Semiconductor, a subsidiary of Uniroyal Technology Corporation (UTC), is expanding its SiC epitaxial and device production through access to Uniroyal Optoelectronics' manufacturing facility in Tampa, FL. Sterling manufactures 4H and 6H SiC substrates and epitaxial thin films on SiC substrates, and is also developing semi-insulating SiC substrates and devices for wireless communications, industrial process control and power amplification.

The link-up with the Tampa facility is intended to accelerate Sterling's epitaxy and device product development significantly. Sterling has also recently extended leases for its facilities in Danbury, CT and Sterling, VA, consistent with the expansion of its SiC wafer business and its development of semi-insulating substrates.

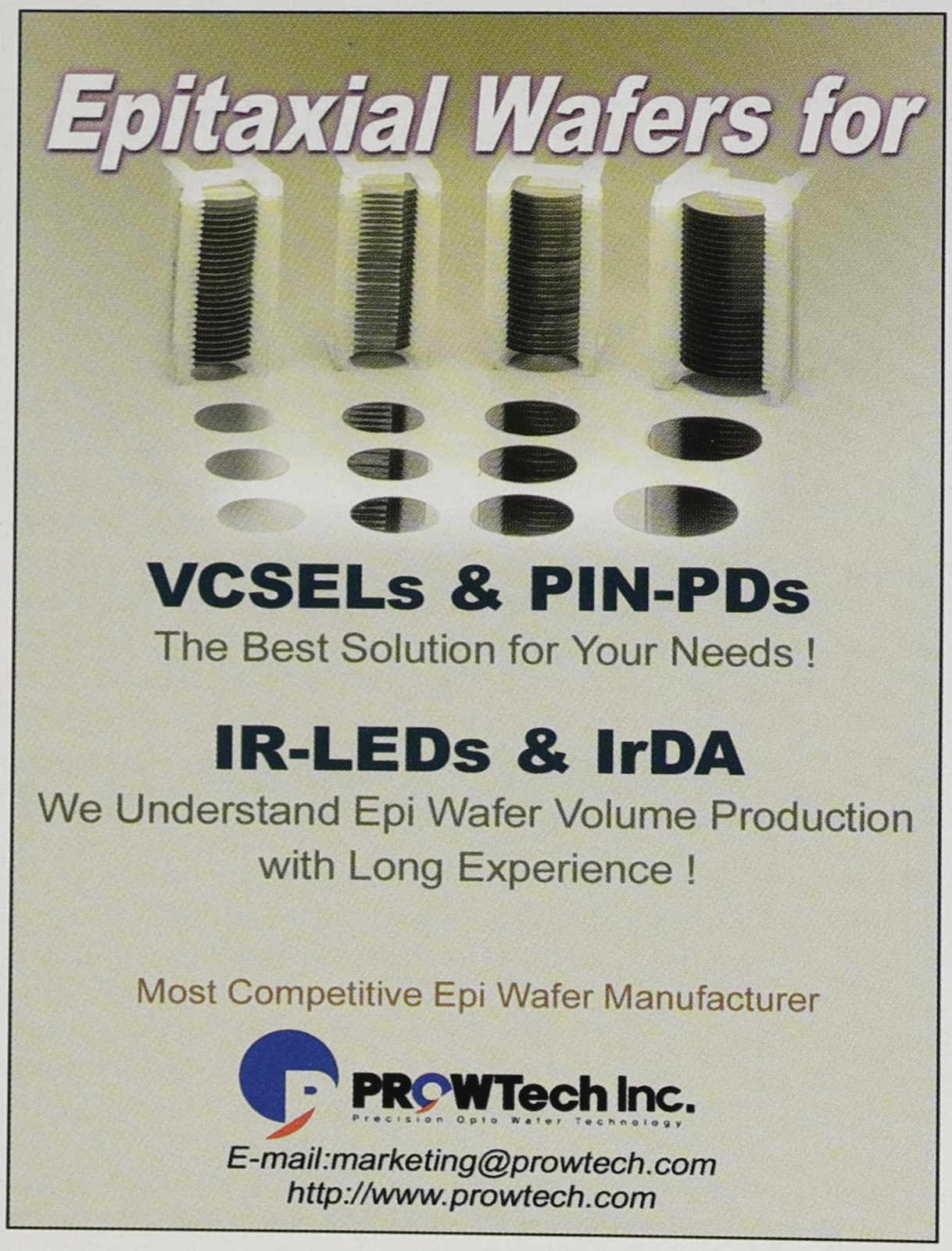
The expansion follows the recent buy-out by UTC of Emcore's minority interest in the LED manufacturing subsidiary, Uniroyal Optoelectronics (see *Compound Semiconductor* September 2001, p4). This gives UTC free reign to direct the operations of Uniroyal Optoelectronics and Sterling at the Tampa facility.

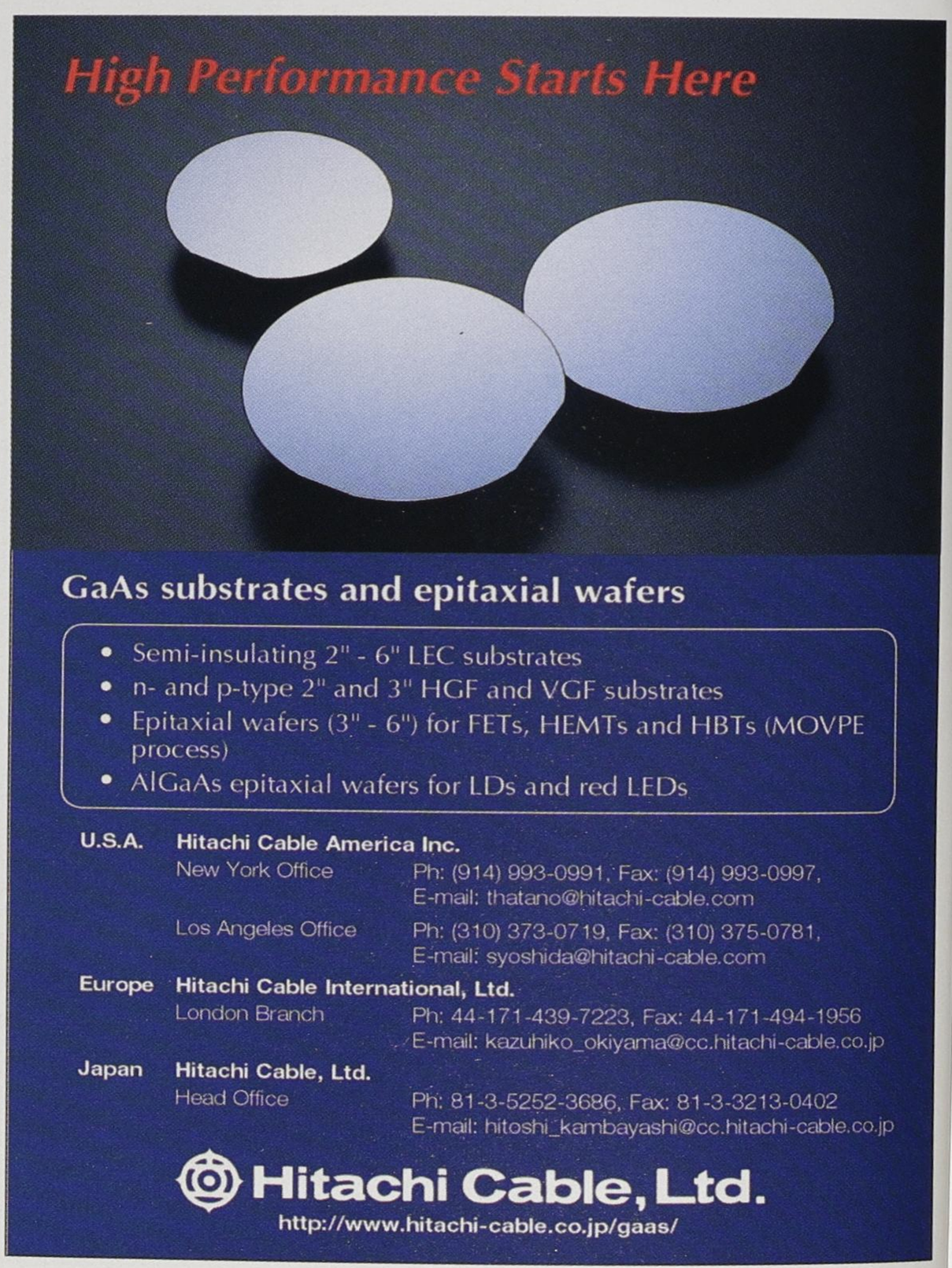
Sterling says it intends to capitalize on existing infrastructure and technological synergies at the Florida plant. The facility produces high-brightness LEDs and is currently undergoing an expansion program, which includes the installation of several new reactors.

"The focus for Sterling continues to be rapid capacity expansion for SiC wafer production, as well as epitaxial and device product development," said Sterling's president, James LeMunyon. "Building our epitaxy and device facility at Uniroyal's Tampa plant provides Sterling with the opportunity to move quickly into these markets, whilst eliminating considerable redundant spending for fabrication, characterization and testing equipment, which is already in place in Tampa." He added that the design of the facility allows Sterling's SiC epitaxy and device facility to operate independently from the operations of Uniroyal Optoelectronics.

"We expect the expansion to accelerate our entry into the commercial epitaxial market by approximately one year, while stepping up Sterling's SiC device product development by approximately two years," added Robert Soran, president and chief operating officer of UTC. "The autonomy achieved through the purchase of Emcore's minority interest in Uniroyal Optoelectronics has made these opportunities possible for Sterling."

Sterling has also received its first MOCVD reactor, which is currently being installed for the production of SiC epitaxial wafers to support product sales and device development at the Tampa site. The company says this reactor will benefit programs such as the recently announced R&D contract with General Electric Corporate Research & Development, which was set up recently to develop and evaluate Schottky diodes using the company's SiC wafers and epitaxy (see *Compound Semiconductor* May 2001, p8).





Princeton Optronics secures $25 million

Component manufacturer Princeton Optronics has received $25 million in second-round funding from a group of venture capitalists. The funds will be used to scale up production of the company's 12.5 Gbit/s receivers and modulator drivers, and to fund the final development of its PowerSweep 2000, a high-power tunable laser (see *Compound Semiconductor* May 2001, page 51).

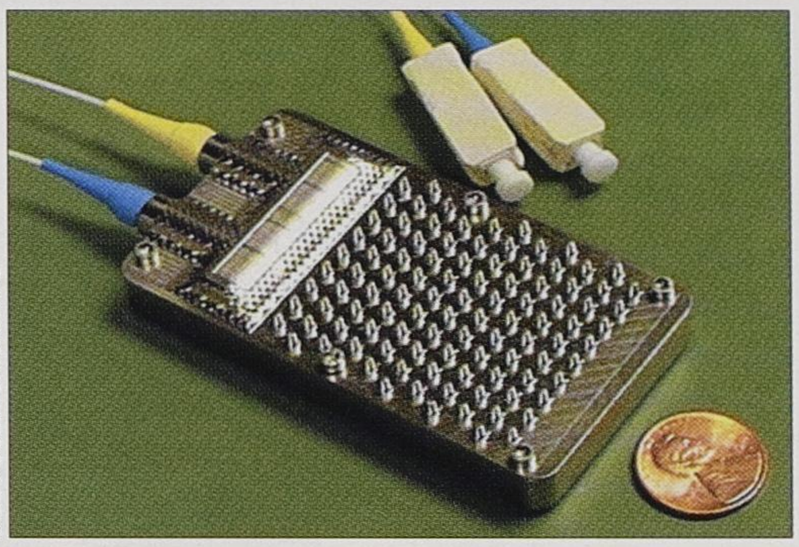
The latter device uses a VCSEL with an external MEMS cavity to select the desired wavelength. High output powers are achieved by optically pumping the VCSEL using a second VCSEL emitting at 980 nm. The laser is tunable across the entire C-band from 1525 to 1565 nm, though the tuning range can be scaled up to 70 nm. Output power is 20 mW (scalable to 50 mW) with 50 GHz linewidth, and a wavelength locker provides ±1 GHz stability. A similar approach is used by competitor CoreTek (now part of Nortel Networks), which employs a MEMS-tunable VCSEL pumped using a 1310 nm edge-emitting laser.

Much of Princeton's intellectual property lies in producing 980 nm VCSELs, and the company claims its tunable laser technology offers major advantages in terms of production costs. The critical step in manufacturing this type of device is aligning the pump laser, VCSEL, tuning cavity and fiber. Normally the alignment is actively adjusted to optimize performance while the laser is operating. But in Princeton's system manufacturing costs are reduced using automatic alignment: components are placed in the best positions first time around without the laser operating.

Vendors demonstrate 10 Gbit/s products

Two optical component suppliers, Cielo Communications and Picolight, have proven the readiness of their 850 nm VCSEL-based transceivers for 10 Gigabit Ethernet short-reach interconnects. Both companies demonstrated 10 Gbit/s serial optical links spanning 450 m, while meeting bit-error-rate requirements of 1×10^{-12}, or one error in every trillion bits. The demonstrations were part of an effort by the 10 Gigabit Ethernet 10BASE S group, whose member companies work independently to develop technologies supporting the emerging IEEE P802.3ae standard. If adopted, these 850 nm links should enable much cheaper high-volume network solutions for metro and access applications compared with today's 1310 nm or 1550 nm devices.

Picolight's optical modules have also been used in a separate demonstration supporting the 10 Gigabit Ethernet standard. The company connected its 850 nm VCSEL transceiver with switches from Foundry and a network performance analysis system from Spirent, over a distance of 300 m. The demonstration supports the viability of extending Ethernet connectivity from the LAN all the way into metro and WAN.



CIELO COMMUNICATIONS

Cielo's VCSEL-based transceivers have been used to demonstrate 10 Gigabit Ethernet short-reach interconnects.

"Spirent, Picolight and Foundry have shown that the technologies are maturing rapidly," said Chris Simoneaux, Picolight's director of product marketing. "This gives the industry confidence that cost-effective, low-power links will soon be widely available."

Agere undergoes internal reorganization

Agere Systems is reorganizing its products into two groups targeting optical network equipment and consumer communications markets. Agere span off from Lucent Technologies earlier this year and is one of the few companies that manufacture both optoelectronic components and ICs.

The company's optoelectronic portfolio comprises active components including lasers, modulators, amplifiers and transceivers, which are used in long-haul optical networks operating at 2.5 Gbit/s and above. IC activities make up 75% of its sales, primarily for communications and computing applications, and focus on silicon; GaAs IC manufacturing is outsourced (see *Compound Semiconductor* February 2001, page 88).

Agere's new Infrastructure Systems group will consolidate its optoelectronics and IC activities. The Client Systems group will handle its wireless data, computer communications and storage systems business. In addition, Agere will combine the manufacturing and supply activities of its optoelectronics components and ICs in a new Operations group.

Velocium gets new HQ and design lab

Velocium, the company recently formed by TRW to commercialize GaAs and InP optical networking and wireless components, has opened a 50 000 sq. ft headquarters and product design laboratory. Located in El Segundo, California, the facility is close to TRW's recently completed InP production line, which produces InP components for wireless and fiber-optic applications. Dwight Streit, Velocium's president, said, "We're bringing TRW's advanced technology to market just when the telecom industry is seeking the high-speed solutions made possible by InP."

MRV to merge with Luminent subsidiary

MRV Communications plans to merge with its majority-owned subsidiary, Luminent, one of the few manufacturers that supplies both active and passive devices for metro optical networks. Luminent spun off from MRV after an initial public offering in November 2000, although MRV retained 92% of the shares (see *Compound Semiconductor* November 2000, page 32). MRV, based in Chatsworth, CA, is currently considering its strategy for Luminent, which manufactures products including lasers and LEDs at its Luminent-Hsinchu Active Components division in Taiwan.

"Unifying Luminent and MRV is expected to enhance our competitive position and generate substantial savings in the consolidated results," said MRV's president and CEO Noam Lotan. The move will also allow Luminent to invest and improve its technology and its bottom line.

Transceivers break the record on size

Sumitomo Electric has begun shipping samples of two new small-form-factor pluggable (SFP) transceivers containing the world's smallest laser diode module. The transceivers incorporate a newly developed transmitter optical subassembly (TOSA) with a maximum diameter of 4 mm. The two transceivers, SCP6828-XL and SCP6808-XL, transmit at 2.5 Gbit/s over 2 km and 15 km respectively at a wavelength of 1310 nm.

The new TOSA has enabled Sumitomo to make the transceivers in its SCP6000 series half the size of those in its earlier SCM6000 line. The transceivers are mounted in industry-standard edge electrical connectors, and comply with the SFP standard.

Sumitomo will also release long-distance models operating at 1550 nm. An additional peripheral interface controller will allow features such as the intensity of the laser emission to be monitored remotely.

Paracer samples products

Born less than a year ago with the aid of $6.5 million in venture capital, Paracer is shipping samples of its first product – a 1 × 12 parallel array with an aggregate capacity of 30 Gbit/s. The array suits very-short-reach (VSR) applications such as board-to-board and unit-to-unit communications, and the firm claims to be shipping to all major OEMs.

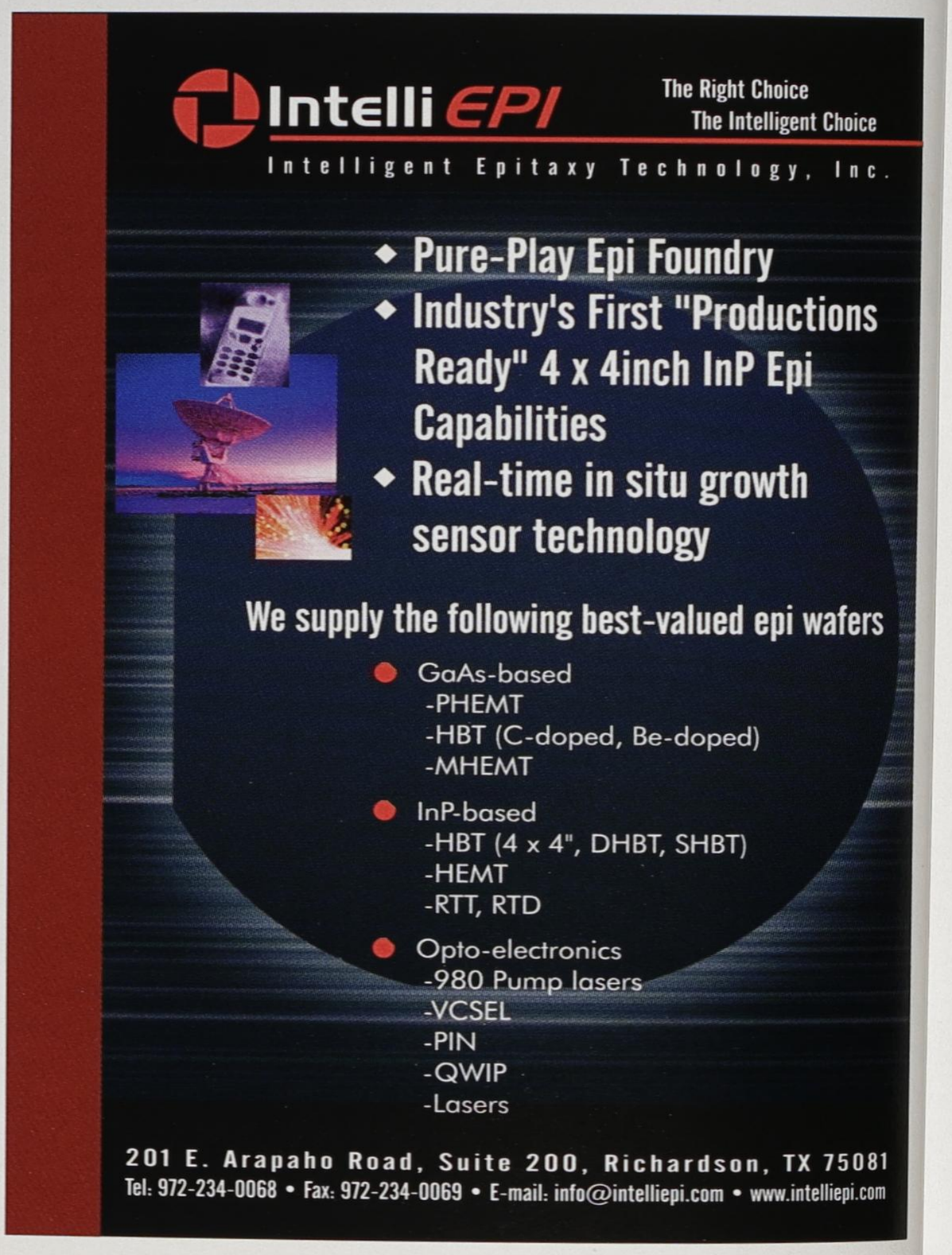
The transmitter and receiver pairs use arrays of 850 nm VCSELs from external suppliers and photodetectors connected by a fiber ribbon cable. Other products released in September are a four-channel (3.125 Gbit/s per channel) transceiver and a transponder compliant with the OC-192 (10 Gbit/s) VSR-1 standard. Paracer says that meeting large-volume orders will not be a problem as the company has an agreement with Foxconn Electronics to outsource volume production.

Like Picolight, Paracer is not soldering modules onto boards but using pluggable modules. These make it possible to test chips before they are placed on a board, and allow repairs or upgrades without replacing an entire board. However, Paracer differs from Picolight because its modules are hot-pluggable – they can be slotted onto a board without removing it from its chassis.

Fujitsu and Nortel agree on receivers

Nortel Networks and Fujitsu Quantum Devices have agreed joint specifications for 10 Gbit/s receivers containing an avalanche photodiode (APD) and a broadband, low-noise pre-amplifier integrated in a small package with SMP connectors. The agreement will provide two sources for receivers with the same package outline and pin allocation for a common board layout. Volume production is due in January 2002.





Spectrolab GaAs cells take solar car to race victory

GaAs solar cells from Spectrolab powered the University of Michigan's solar car to its recent victory in the American Solar Challenge. Designed by the Michigan students, the M-Pulse vehicle used a total of 3000 Spectrolab dual-junction terrestrial solar cells in the race. The team took just nine days to complete the course, which began in Chicago and ended 2248 miles away in California. The winning time was slightly over 56 hours.

The solar panels generated enough power to charge the batteries even when the car was running at 55 mph. Under normal weather conditions, the cells' electrical output was about 1200 W, although they could generate up to 1600 W as a result of solar energy reflected back from clouds.

Headquartered in Sylmar, California, Spectrolab is the largest manufacturer of solar cells for space applications. Spectrolab's dual-junction cells comprise $GaInP_2$ and GaAs regions epitaxially grown in series on Ge substrates. Each junction converts energy from a different portion of the solar spectrum, which increases the efficiency compared with a single junction. The cell is designed to be 23.7% efficient in terrestrial applications.



SPECTROLAB

University of Michigan students used a total of 3000 Spectrolab dual-junction GaAs solar cells to power their solar car from Chicago to California in slightly over 56 hours. The cells were able to generate a maximum output of 1600 W including solar energy reflected back from clouds.

The company also provides triple-junction solar cells that have an efficiency of 29%. Cell manufacturers such as Spectrolab and Tecstar are currently working on solar cells with an increased efficiency of 40% (see *Compound Semiconductor* August 2001, p29).

Tecstar solar cells head out for Mars

Tecstar has announced that its new TEC 3i solar cell has been chosen to power the latest Martian exploration spacecraft being developed by NASA and the Jet Propulsion Laboratory (JPL). The Mars Exploration Rover (MER) is the newest vehicle designed to carry instruments, including cameras and spectrometers, to the surface to find out whether or not water has been present in the planet's history.

Tecstar is working with JPL staff to test and build the solar panels that will give the MER the power to get to Mars. The solar panels will also enable it to travel on the surface as far as 100 km in a Martian day.

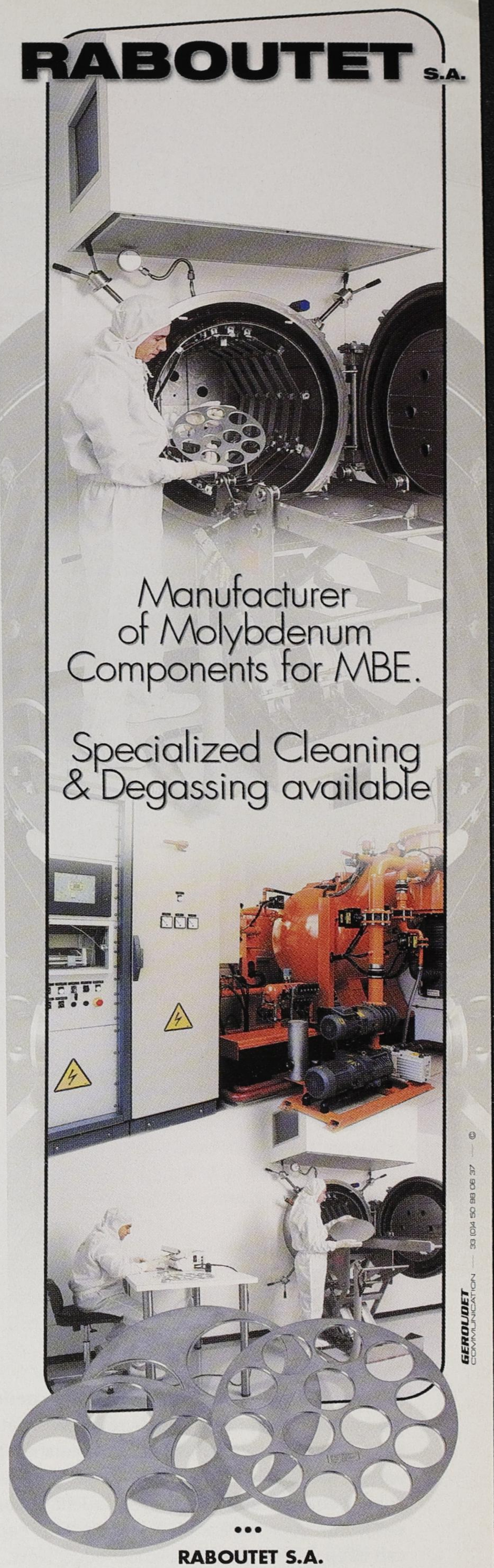
Tecstar claims that the TEC 3i has the largest format of any high-efficiency solar cell available. It incorporates Tecstar's monolithically grown bypass diode that increases cell lifetime but reduces weight. The latter factor is crucial for launch payloads (see *Compound Semiconductor* August 2001, p29).

Replacement arrays on offer from IMC

Industrial Microphotonics Company, a division of Cutting Edge Optronics (CEO) that specializes in laser-diode bars and arrays, is now offering replacement diode arrays compatible with models that are no longer commercially available.

"Owners of diode-pumped lasers that have been working well for the past several years are looking to replace diode arrays that have finally worn out," said IMC's director Ted Konopelski. "Because the original manufacturers of many of these diode arrays no longer develop these products, we have been providing limited quantities of cost-effective replacement arrays."

CEO inherited TRW's laser-produced plasma and extreme-ultraviolet laser activities when TRW purchased the company last year for $19 million in cash. The company's products now range from 1 W semiconductor lasers through to multi-kilowatt diode-pumped solid-state lasers.



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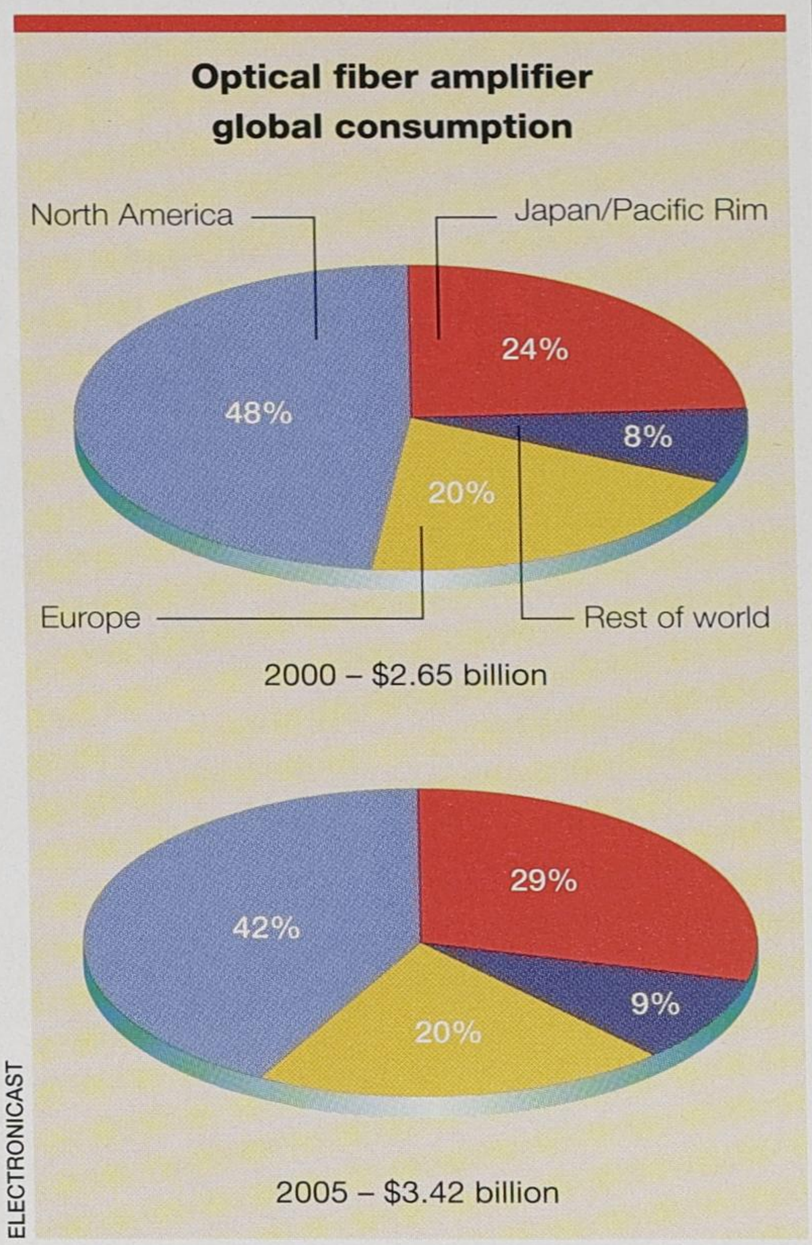
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Fiber amplifiers market to hit $3.4 billion by 2005

Driven by the proliferation of dense wavelength-division multiplexing (DWDM), the optical fiber amplifiers market will grow from $2.65 billion in 2000 to $3.4 billion by 2005, predicts an ElectroniCast report. The report points out that Raman fiber amplifiers will become increasingly widespread as DWDM increases the bandwidth carried by each fiber. Raman amplifiers give higher gain across a wider bandwidth than erbium-doped fiber amplifiers (EDFAs), though they require high pump laser powers to ensure adequate gain. With this application in mind, high-power 14xx nm laser diodes are the subject of much development activity among companies such as Agere and Fitel. The report also explains that Raman amplification is not going to replace EDFAs, but that the two will be used in combination. Raman amplifiers provide additional gain between EDFA stages, meaning that the optical signal never becomes as weak between stages as it does in an EDFA-only system. A stronger signal is thus maintained at each EDFA stage (where most of the noise is introduced), giving an improved signal-to-noise ratio.



The report details the production and consumption of optical amplifiers, components, and passive and active gain blocks on a global basis, and discusses significant applications in the 1310 and 1550 nm wavebands. Between 2000 and 2005 little change is forecast for market consumption in the Europe and Rest-of-World segments. The major changes come in the North American market, where the share of global consumption will fall from 48% to 42%, and in the Japan/Pacific Rim region, where market share will rise from 24% to 29% over the same period.

"*Optical Fiber Amplifier, Gain Block and Components Global Market Forecast*" is available from ElectroniCast – see "www.electronicast.com".

Tunable laser revenues set to exceed $1 billion

A new report from KMI and Sirraya estimates that the tunable laser market will grow rapidly and will soon surpass $1 billion in annual revenues. The main application for tunable lasers is currently for inventory management and sparing. As the wavelength is not fixed, network operators can save large amounts on inventory, especially as optical networks approach 160 channels, sometimes requiring 20 backup lasers per channel.

New applications are also emerging as networks evolve, and tunable lasers are expected to enable bandwidth-on-demand, optical cross-connects, wavelength routing and next-generation metro networking.

The report identifies 26 manufacturers in various stages of developing or offering tunable lasers. These devices are grouped into monolithic cavity edge-emitting lasers, external cavity diode lasers and vertical cavity surface-emitting lasers (VCSELs). The edge-emitter category includes Fabry–Perot, distributed Bragg reflector (DBR) and distributed feedback (DFB) device designs, and incorporates the integration of device elements such as arrays of DFB cavities or new schemes for integrating DBRs. The advantages of this approach include stability, reproducibility and potential cost efficiencies. Thirteen companies have developed such emitters, including ADC, Agere, Agility, Alcatel, ExceLight, Fujitsu, JDSU, Marconi, Multiplex, NEC, NEL, Nortel and Santor.

External cavity lasers (ECLs) employ a simple Fabry–Perot laser in combination with an external reflector or grating to provide feedback (see *Compound Semiconductor* April 2001, p24). This type of laser holds promise as an optical communications solution if the cost advantages, as well as the robustness and reliability, can be developed further. ECDL manufacturers include Blue Sky Research, iolon and New Focus.

VCSELs have the advantage that the tuning cavity is short and can employ a Fabry–Perot design, which results in a lower-cost device. Bandwidth9, Novalux and Princeton Optronics all have VCSELs for the 1550 nm region in various stages of development.

"*Tunable Lasers for Optical Communications: Technology, Products, and Applications*" is available from KMI Corp – see "www.kmicorp.com".

North American optical market in decline

New market figures from RHK show that the North American optical transport market will decline 36% from 2000 levels. The research says that optical transport equipment sales, including DWDM, SONET and cross-connects, is expected to end the year at $12.5 billion, down from $19.6 billion last year. Equipment spending will remain flat well into 2002 as inventory is consumed and service providers lease capacity from wholesale carriers.

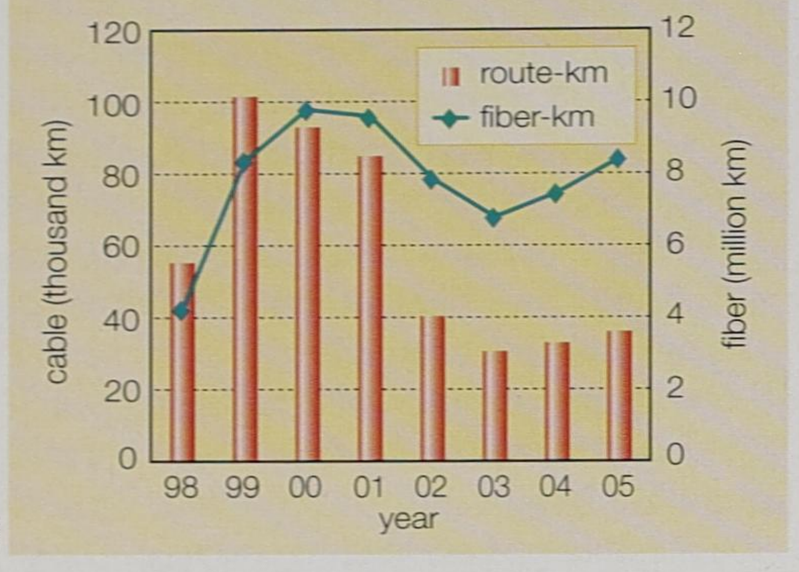
"Since our last forecast, we completed another round of interviews with carriers, who account for 95% of carrier spending," said John Ryan, RHK's principal and chief analyst. "We found that carriers dramatically shifted their purchasing and operational behavior to match the unprecedented changes in competition and economics experienced in this market."

The updated RHK forecast points to significant shifts in carrier spending philosophy, from purchases of new equipment to leasing capacity from other carriers, and a redeployment of in-service equipment to new routes to match traffic demand.

Not all the news is bad; RHK maintains that particular market sectors, including metro transport, ultra-long-haul systems and optical core switches, will experience substantial growth for several years.

More information can be obtained from RHK's North America Long Haul and Metro Transport services – see "www.rhk.com".

Fiber deployment in North America set to slow down



KMI

The fiber capacity required in the US is currently the subject of hot debate (see *Compound Semiconductor* August 2001, p4). Part of this discussion hinges on studies touting a fiber glut. A new report by KMI shows that fiber deployment in North America will slow significantly over the next two to three years, to be replaced by a period of industry consolidation.

At the end of 2000, carriers in the US, Canada and Mexico had deployed a total of 672 000 route-km of fiber-optic cable in long-haul networks. With an average count of 52 fibers per cable, nearly 35 million km of fiber has been laid – five times the amount of four years earlier. At its peak in 1999, the amount of cable being laid was 140 000 route-km, 100 000 route-km of which was in the US.

In the next two years, the acceleration will be checked, and the amount of cable laid in North America annually will fall to 35 000 route-km in 2003. This reduction will be cushioned as more fibers are included in each cable (see figure); in terms of the amount of fiber actually laid per km, the drop is from 9.8 million fiber-km in 2000 to about 7 million fiber-km in 2003.

Beyond 2003, says KMI, improved business conditions and friendlier capital markets will combine with growth in broadband demand as more end users shift away from dial-up modems and put more traffic on the Internet backbone. The resulting demand will lead to positive growth in the amount of fiber laid, although this will be at levels below those of the peak years of 1999 and 2000.

"*Fiber-Optic Networks of Long-Distance Carriers in North America: Market Developments and Forecast*" is available from KMI Corp – see "www.kmicorp.com".

Global integrated optical components market could top $2.6 billion by 2005

Integrated optical components		
market value ($ million)	*2001*	*2005*
transponders	5.4	1617.8
passive DWDM	0.8	102.9
switches	0.8	77.2
amplifiers	3.5	128.6
monitors	1.2	150.0
back-plane	1.0	50.0
other	0.7	498.8
total	**13.4**	**2625.3**

CIR

Building integrated optical circuits similar to those manufactured by the microelectronics industry has been an area of intense research. According to Communications Industry Researchers (CIR), this endeavor is at last beginning to bear fruit, and the worldwide market for integrated optical components is expected to grow from $13.4 million in 2001 to $2.6 billion by 2005.

The most significant growth is expected in transmitters and transceivers, which will grow steeply from $5.4 million this year to $1.6 billion by 2005, largely as a result of accelerating demand for access and metro products. Transponders containing integrated laser and wavelength lockers, and also transceivers containing integrated optics and electronics will form an important part of this market sector.

Integrated optical components will also be enabled by emerging InP technology, says the report, largely due to the ability of InP devices to operate at the high speeds required in next-generation networks, and the ability to integrate optical devices with ICs. This could lead to a total market of $1.1 billion for InP components in 5 years.

"*The Market for Integrated Optical Products: 2001–2005*" is available from CIR – see "www.cir-inc.com".

European cellular market approaches saturation levels

As cellular markets in Western Europe approach saturation, 2002 will represent the last year of double-digit revenue growth. According to a new report by Strategy Analytics, cellular service revenues in the region will increase 20% to reach US$90 billion at the end of the year, followed by a slowdown as subscriber growth rates reduce dramatically.

However, prospects for service revenue growth have been saved by indications that the average revenue per user (ARPU) is reaching the bottom of the curve.

"Average revenues have fallen by one-third over the last three years to reach US$370 per subscriber," said Phil Kendall, director of the Strategy Analytics Global Wireless Practice. "If that trend had continued, prospects for the region would be particularly bleak. But with average voice expenditure levels stabilizing in many markets, and data expenditure continuing to grow strongly, ARPUs will creep up slowly after 2002."

Prospects for the handset market, however, are not as smooth. "Having increased by 46% in 2000, handset sales will contract by 13% in 2001 with only 120 million handsets sold," said Kendall. "Subscriber growth has had little chance of reaching the 72 million net additions recorded in 2000, and the replacement market is failing to fill this gap."

Operators cutting prepaid subsidy levels, and delays in the introduction of GPRS (data) handsets and services, have all played a part in the decline, according to David Kerr, vice-president of the company's Global Wireless Practice. "The good news is that the handset market should rebound quickly as users make their delayed replacement purchases in 2002," said Kerr.

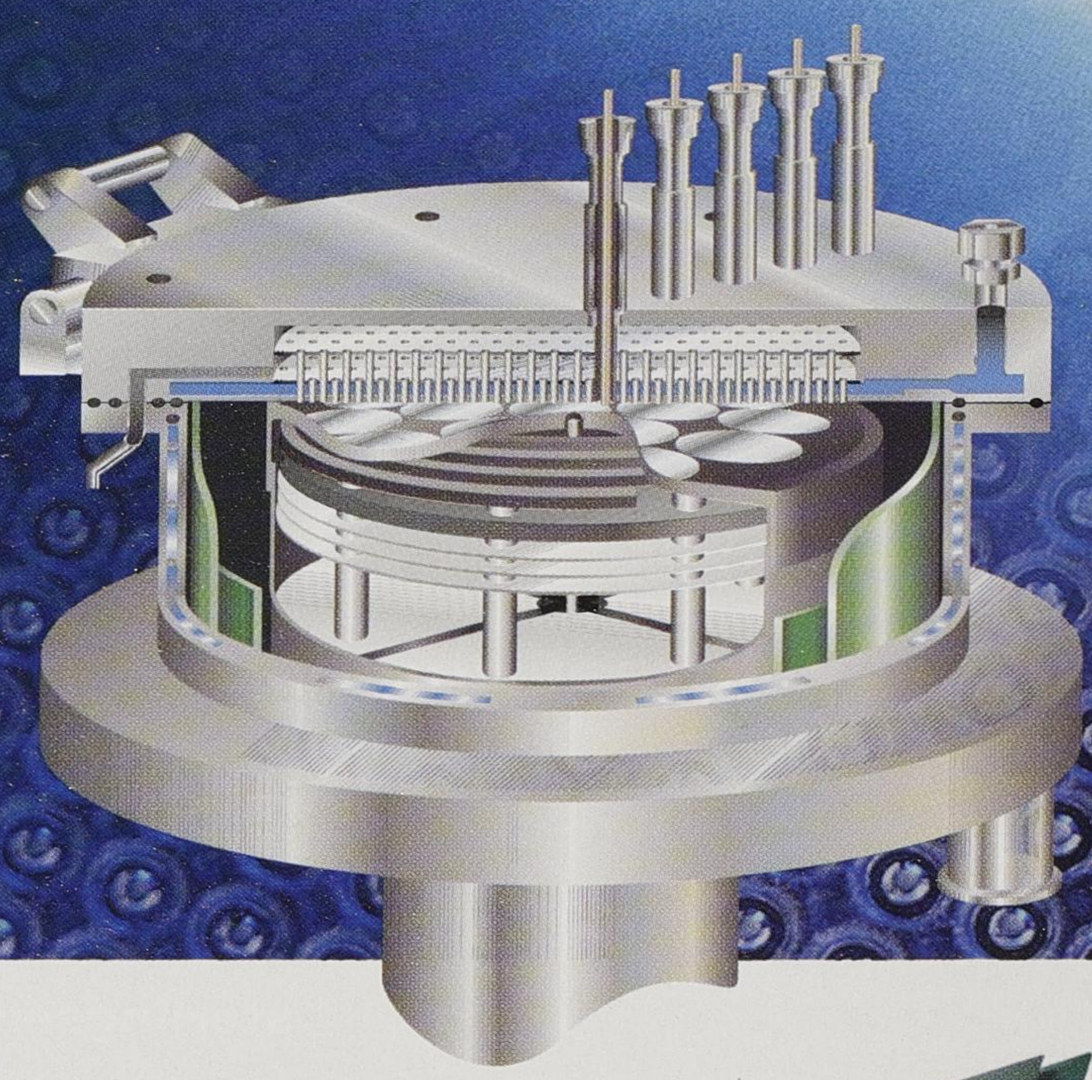
"*Western European Cellular Market Forecast (2001–2006)*" is available from Strategy Analytics – for further information see "www.strategyanalytics.com".

• A related report (*Worldwide Cellular Forecast Update 2001–2006*) predicts that despite the European contraction, the worldwide sales for handsets will grow by 8% to reach 440 million units in 2001. Growth will return to double digits in subsequent years, rebounding to 20% annual growth. Global handset sales will pass the 1 billion mark in 2006, with GSM systems continuing to dominate, accounting for 70% of sales.

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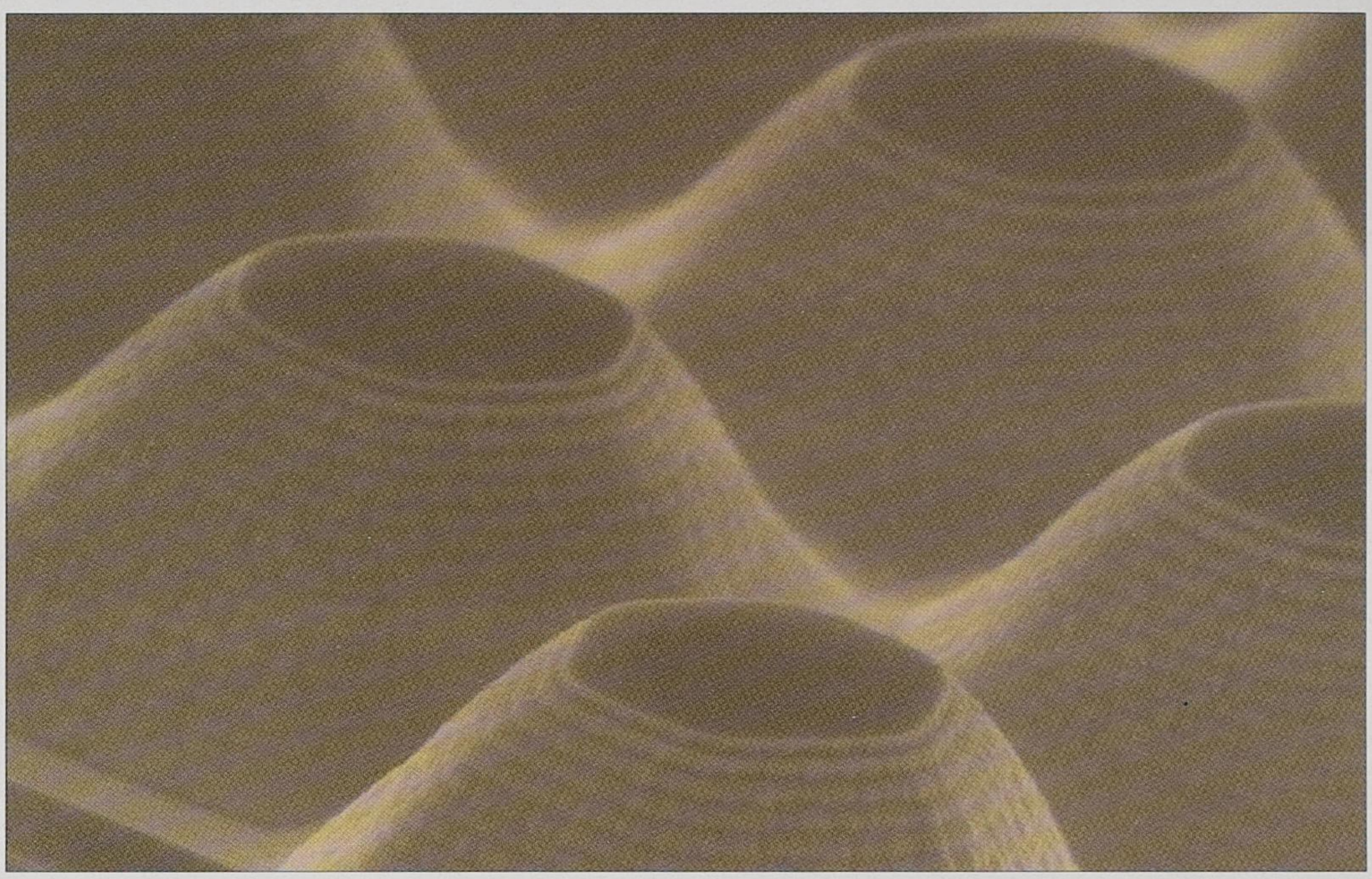
IQE and QinetiQ team up in joint venture

Two UK companies, IQE and QinetiQ, are forming a joint venture to undertake research and development, and assess materials for themselves and their customers. Epiwafer and substrate vendor IQE is based in Cardiff, while QinetiQ operates from a number of sites across the UK. QinetiQ was formerly the Defence Evaluation and Research Agency (DERA) and has an established compound semiconductor works in Malvern.

The venture, based on epitaxial-growth technology, will initially operate from QinetiQ's Malvern facility. It is expected to have eight reactors dedicated to III-Vs and two for silicon, SiGe and SiC. Both companies bring intellectual property and equipment to the table, and IQE will use its established global sales and marketing operations to promote the venture's services.

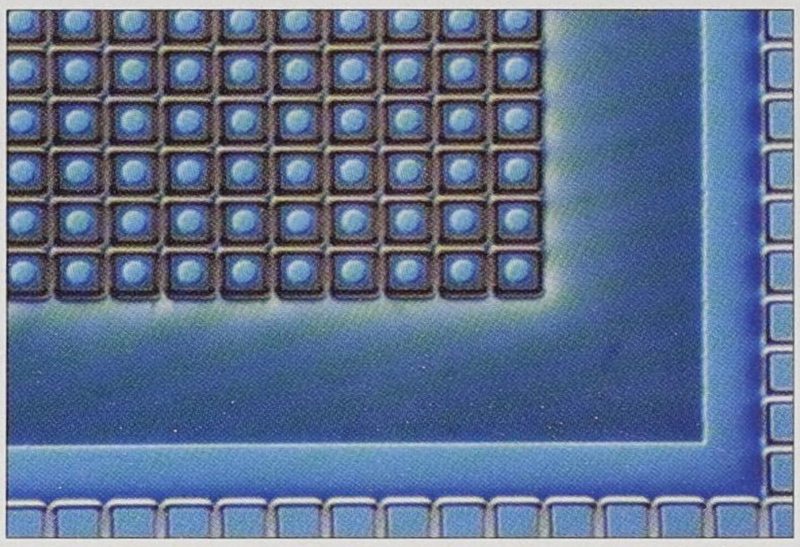
"This joint venture consolidates the positions of both IQE and QinetiQ within the industry, and allows IQE to focus on volume production while offering customers access to a truly world-class research and development center," said Steve Byars, managing director of IQE Europe.

QinetiQ was set up in July this year when DERA was split into two parts. DERA performed the bulk of the non-nuclear research for the UK's Ministry of Defence (MoD). The split saw 75% of DERA become a government-owned public company called QinetiQ, with the remaining 25% staying within the MoD as the Defence Science and Technology Laboratory (DSTL). Shares in QinetiQ are likely to be offered on the London Stock Exchange in early 2002.



QINETIQ

Concentrator cones improve the efficiency of InSb emitters and detectors.



QINETIQ

The corner of a 256 × 256 InSb infrared focal plane array showing the pixels, with the indium bumps clearly visible.

QinetiQ's compound history

QinetiQ's Malvern site has a long history in compound semiconductor materials and micro- and optoelectronics R&D, as well as silicon and SiGe. The site carried out much of the early development in using the Czochralski method to grow bulk compound semiconductor crystals, as was the case with device-quality GaAs grown by MOVPE. The first GaAs FETs from this material were reported by a Malvern team in 1975.

Its current activity covers a broad range of III-V and II-VI device technologies, including InSb-based transistors, magnetic-field sensors, infrared emitters and detectors, and HgCdTe and InSb infrared focal plane arrays (IRFPAs). The military heritage of the site has also seen the growth of activity in GaAs-based millimeter-wave and microwave devices, and the development of an established program for semiconductors based on III-nitrides for high-power electronics.

The concept of negative luminescence was pioneered at the Malvern site. This effectively allows an InSb-based device to switch its background infrared emission off, making it appear cold. Negative luminescence devices have found application as infrared flux references for non-uniformity correction in IRFPAs. QinetiQ was the first to fabricate mid-IR focal-plane arrays from MBE-grown InSb. Their structure allows operation above 77 K, and incorporates an InSb negative luminescence source for correcting array non-uniformity. Arrays up to 1024 × 768 pixels in size have been demonstrated. The development of emitter and detector technologies in the mid-infrared has spurred activity in gas sensors, as many gases of interest have absorption lines in the mid-IR.

The epitaxy of dilute nitride alloys is another technology that enables emission and detection in the infrared. Chemical beam epitaxy (CBE) is being used to grow arsenide nitrides for 1300–1550 nm emitter applications, and nitrogen plasma MBE is being used for antimonide nitrides for long-wavelength infrared detector applications. More recent activity targeting fiber-optic communications includes developing GaAs 40 Gbit/s optical modulators for future optical networks.

GaAs-based circuit and sub-system design focuses on highly integrated millimeter- and microwave multi-function circuits, including MMIC receiver and transmitter front ends for 40–50 GHz operations, and 12–18 GHz single-chip transceivers. Circuits are fabricated through partnerships with commercial foundries. GaAs has also found a place in the millimeter-wave imaging systems being developed by QinetiQ. These systems receive at 35 or 94 GHz and use GaAs or InP MMICs as the receiver elements. One of the applications of millimeter-wave imaging is security, as passive imaging through clothing can reveal hidden weapons.

News in brief

• **Inforcomm Semiconductor Corporation** has acquired an **Aixtron** AIX 2600G3 (5 × 6 inch) production reactor specifically for growing HBT and PHEMT epiwafers. A spin-off from LED manufacturer Epistar, ISC established operations early this year at a 20 000 sq. ft facility in the Hsinchu Science-based Industrial Park in Taiwan. The company supplies epiwafer foundry services for applications in the wireless communications industry.

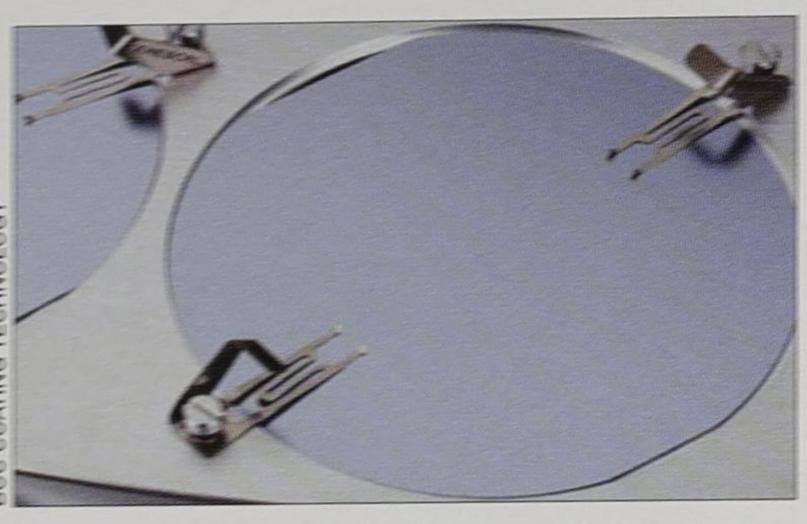
• **Tegal** has received a follow-on order from **Global Communication Technology** for its 901G plasma-etch system. GCT will use the tool at its foundry in Hsinchu, Taiwan to produce PHEMT and HBT devices for wireless, information and networking applications.

• **Nitronex** has purchased a DIVA pulsed I-V measurement system from **Accent Optical Technologies** to aid device characterization and modeling at the company's GaN epitaxy and device processing facility in Raleigh, NC. "We see the pulsed I-V system as instrumental in understanding the sources of current dispersion," explained Ric Borges, director of device engineering at Nitronex. "The DIVA system yields critical information on the thermal and mid-gap energy level time constants in our devices."

• **Aixtron** has also sold two AIX 2000 reactors to **Genoa** (Fremont, CA) for the manufacture of linear optical amplifiers. Genoa's device uses a 1550 nm InP-based VCSEL to amplify multiple wavelengths across the C-band (1525–1560 nm) without introducing cross-talk (see *Compound Semiconductor* May 2001, page 49).

• **Accent Optical Technologies** has made a volume purchase agreement with **Osram Opto Semiconductors**. Under the agreement Osram will purchase optoelectronics process-control tools, including photo-luminescence mappers. The tools will be installed at Osram's new LED production facility in Regensburg, Germany.

Temescal secures patent on substrate handling clips



BOC COATING TECHNOLOGY

The lite-touch wafer clip spreads contact force over a larger area, reducing stress.

BOC Coating Technology has won a patent for an innovative spring clip that allows lighter forces to be applied when working with fragile substrates such as GaAs or InP. Temescal, a member of the BOC Coating Technology group based in Fairfield, CA, uses the clip on thin-film deposition and coating equipment.

"Our original challenge was to adapt the fixtures for extremely thin GaAs wafers used in compound semiconductor applications," said the clip's inventor Cris Kroneberger. "The new design decreases and distributes the contact force over a larger area, reducing the stress on the substrate and the potential for failure."

In more brittle substrates, fractures begin at points where the crystal is already flawed. E-beam deposition fixtures have traditionally used stronger-force wafer clips designed for more robust wafers, and thus are more likely to create micro scratches. "The new clips provide a much lighter yet balanced and controlled contact force," added Gregg Wallace, Temescal's business manager. "The reduction in micro scratches leads to higher yields through all subsequent processing."

MKS consolidates process control lines

MKS Instruments (Andover, MA), a supplier of products for measuring, controlling and analysing gases, as well as products for reactive gas generators and power delivery, has formed the Advanced Process Control group (APC). The group will combine the company's Spectra and On-Line product lines to provide equipment for monitoring and controlling manufacturing processes in semiconductor and optoelectronic applications.

On-Line's portfolio includes FTIR spectroscopy systems for gas and wafer metrology, while Spectra specializes in process monitors and gas analysers.

"The advanced sensor and software technologies of Spectra and On-Line give us complementary solutions in both gas analysis and film metrology," said John Bertucci, chairman and CEO of MKS. "By strengthening our position in process monitoring and control with these diagnostic tools, we are able to develop new products to serve growing requirements in diagnostics and advanced process control."

Zentrix opens new facility in Malaysia

Zentrix Technologies (Tucson, AZ), a specialist in integrating circuitry with packaging for the wireless and fiber-optic communication industries, has opened a facility in Selangor, Malaysia.

It is understood that the new site will be focusing on customer support, giving manufacturing and technical sales advice about wireless and fiber-optic components to customers in Southeast Asia.

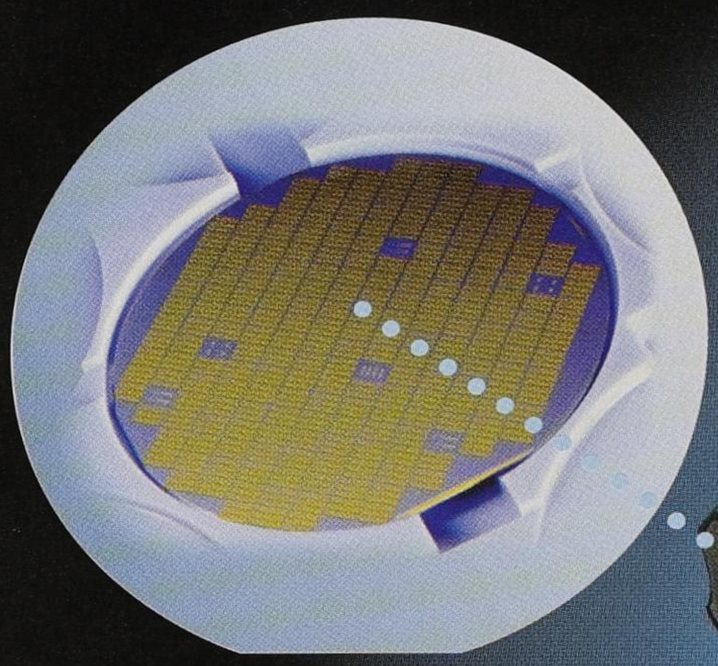
Union Miniere changes name to Umicore

The Belgian producer of polished germanium wafers Union Miniere has changed its name to Umicore. Management at the company said that the old name did not reflect the scope of its current operations.

The company is still divided into three business groups: zinc, copper and precious metals, and the advanced materials group which includes its germanium products. Umicore's germanium products include crystals, wafers and infrared transparent lenses and windows. The germanium wafers are used as substrates in the epitaxial growth of photovoltaic devices and are also being investigated as a cheaper alternative to GaAs for growing metamorphic HEMTs (see page 57).

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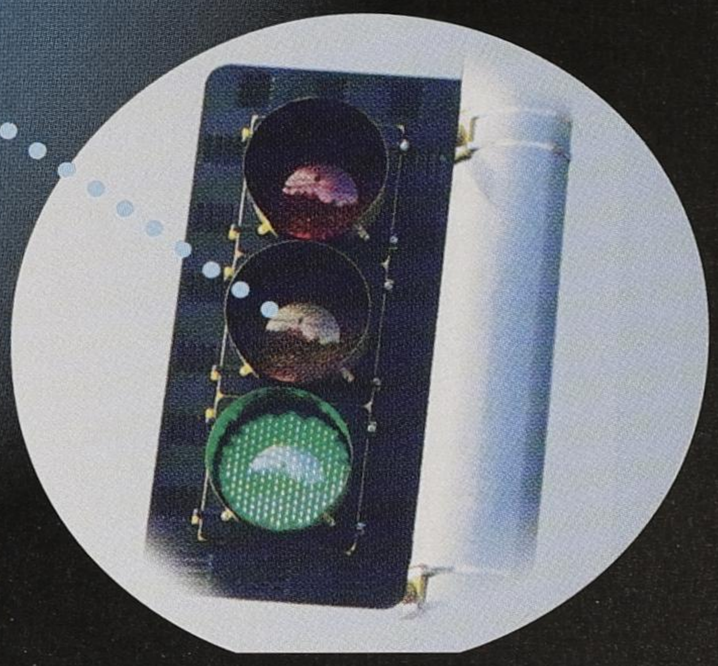




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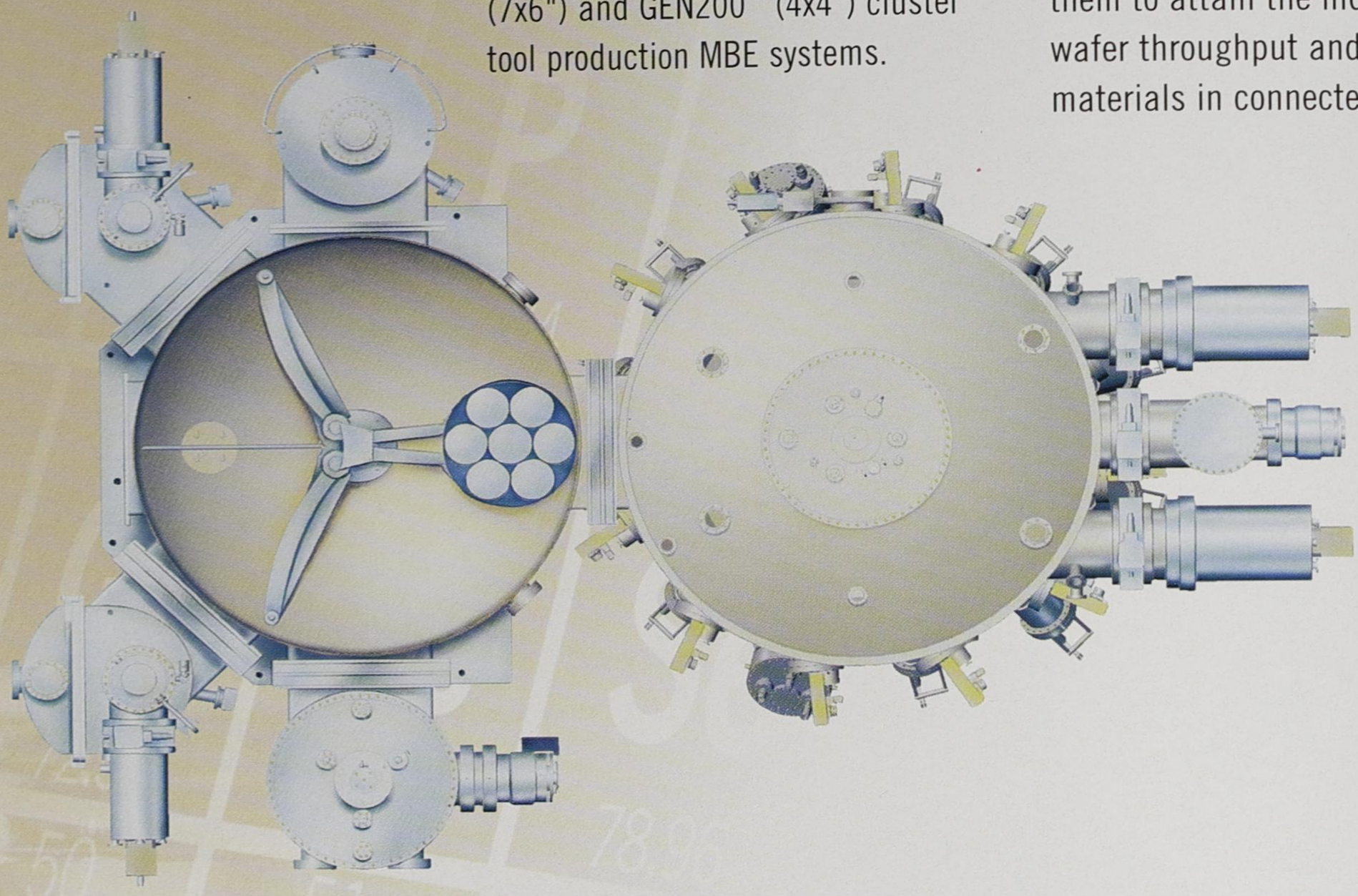
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News in brief

● **Emcore** has made **Larry Kapitan** the vice-president (VP) of its Electronics Materials division. Formerly director of MBE operations at RF Micro Devices, Kapitan has more than 20 years' experience in high-volume GaAs production. **Craig Farley**, who takes on the post of VP of corporate operations and planning, formerly headed Emcore's Electronic Materials division.

● **Accent Optical Technologies** has promoted **Greg Kaiser** to president. Kaiser replaces **Bruce Rhine**, who will continue in his role as chairman and chief executive officer (CEO).

● **Charles Abbe**, formerly chief operations officer of JDS Uniphase, has joined **Nova Crystal's** board of directors. The company selected Abbe for his experience in the optical components market.

● **Sterling Semiconductor,** a subsidiary of Uniroyal Technology, has appointed two renowned SiC scientists to its team. **Olle Kordina** has joined as senior scientist for epitaxy and device production from Linköping University, Sweden. Prior to this he was senior scientist at Cree. Meanwhile **Michael MacMillan** joins as epitaxy scientist and program administrator. MacMillan previously researched SiC and GaN epitaxy for Northrop Grumman.

● **CyOptics,** a supplier of 40 Gbit/s active optical components based in Waltham, MA, has made several changes to its senior management. **Eran Yarkoni** has left CyOptics and will be replaced as president by current CEO **John Pilitsis**, while **Raja Parvez** has joined as chief manufacturing and quality officer. At the same time **Ilan Rabinovich** has relinquished his post as vice-president of engineering to become responsible for product design and development.

● Diode-laser manufacturer **Cutting Edge Optronics** has appointed **Dean Micke** as sales manager of its laser-diode division, IMC. **Kevin O'Donnell** joins the company from Corning as sales manager for industrial lasers.

● **E2O Communications** has named **Julian Cheng** its VP of R&D. Cheng, who previously held posts at Bell Laboratories and JDS Uniphase, will lead its development of long-wavelength VCSELs and 10 and 40 Gbit/s devices.

● **Zentrix,** a supplier of electronics packaging and ceramic products for the wireless and fiber-optic industries, has named **Don Ankrom** its western US regional sales manager.

● **Rodney Masumoto** will head up **Microsemi's** new Product Development Center in Irvine, CA, with a focus on power management, optoelectronics and wireless applications. Masumoto previously worked at Silicon Systems and Texas Instruments.

● Tunable device manufacturer **iolon** has named **Ephraim Suhir** its VP of packaging and reliability, and **Saeid Aramideh** VP of product line management.

● **Philips Analytical** has chosen **Gjalt Kuiperes** to manage its sales, marketing and service units for the X-ray and semiconductor markets in the Americas.

● Swedish fiber-optic transceiver manufacturer **Optillion** has made **Lars Carlson** its new chief financial officer (CFO). Carlson joins from XponCardGroup where he was also CFO.

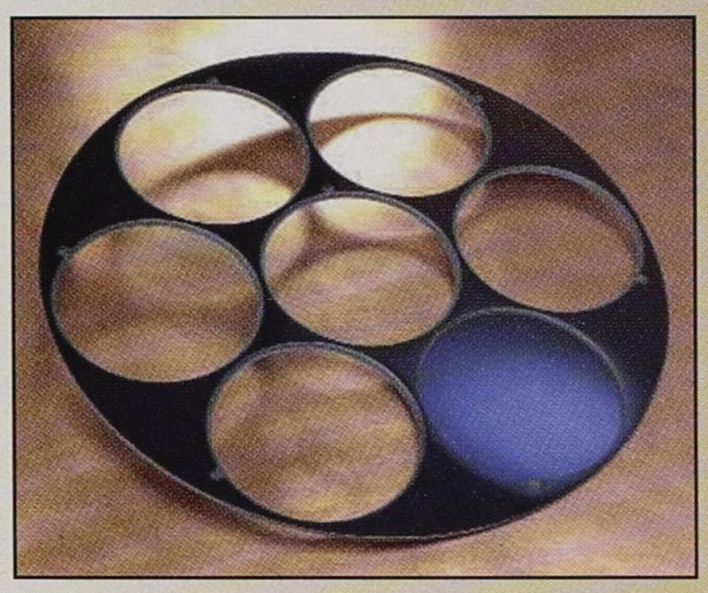
● **Applied Wave Research** (AWR) has made board member **James Spoto** its president and CEO. He replaces **Joseph Pekarek**, who becomes chief technology officer (CTO).

● **Veeco Instruments** has chosen **Clark Taylor** to be VP of marketing for its metrology group. Taylor has assumed responsibility for Veeco's scanning-force microscope, optical and stylus profilers, and defect-review product lines.

● **MKS Instruments** has made **Robert Klimm** the general manager of its ASTeX group, while **William Bintz** has joined the company's materials and analysis group as VP and general manager.

TODAY

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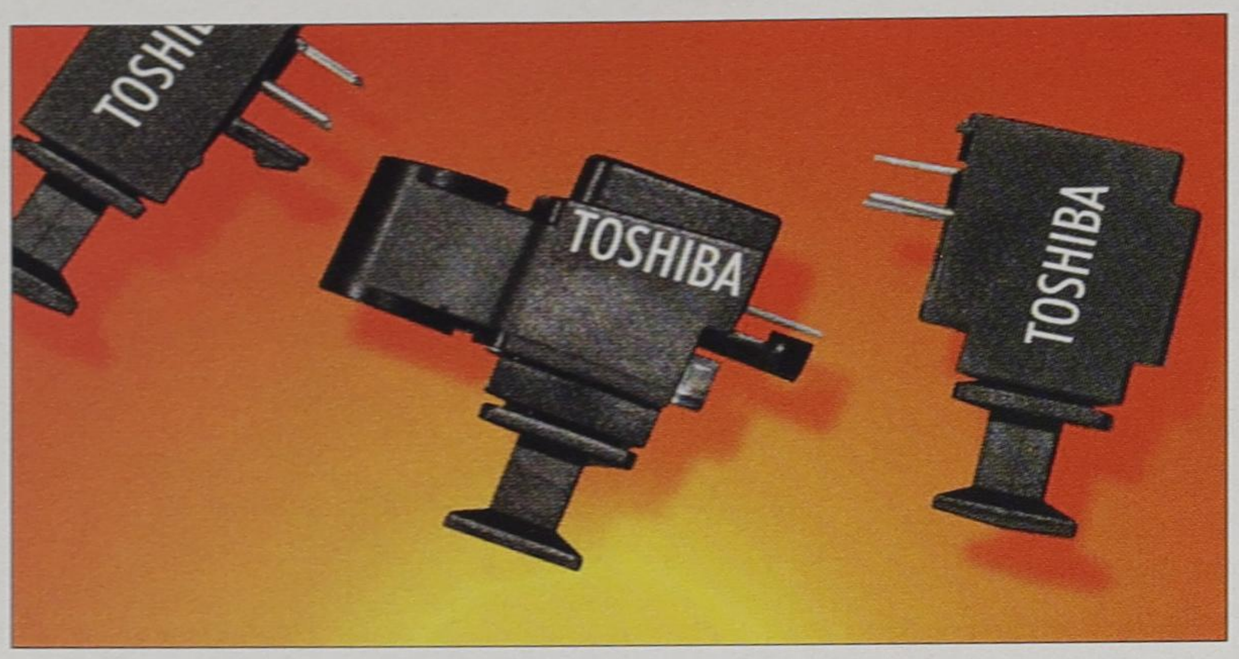
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OPTO PRODUCTS



New transceivers link audio devices

Irvine, CA Toshiba America Electronic Components has unveiled new transmit/receive modules for digital audio optical interconnects. The company's TOSLINK modules employ GaAs LEDs operating in the 650–660 nm range, and are designed for data rates up to 15 Mbit/s in set-top boxes, DVD players, desktop and portable computers, and other commercial appliances.

Operating from a 3.0 V supply, the TOTX141 transmitter provides data rates of 15 Mbit/s and enables as many as five channels of high-definition digital audio. At the receive end of the module a minimum input power of –27 dBm can be accommodated.
www.taec.toshiba.com

Kingbright releases blue SMD LEDs

City of Industry, CA Kingbright has released what it describes as one of the smallest low-cost blue surface-mount (SMD) LEDs available. The GaN-on-SiC chip is designed for low-brightness applications and is centered on a wavelength of 430 nm. The device is housed in the company's 0402 surface mount package, which measures 1.0 × 0.5 × 0.5 mm.

Also available is a 20 bar-graph display consisting of 20 LED segments with a typical output of 2.2 cd.
www.kingbright-led.com

LEDs from Agilent light up displays

Palo Alto, CA Agilent has unveiled new seven-segment LED displays that target home appliances, games, cable set-top boxes, point of sale terminals, answering machines and exercise equipment.

The display family includes single digit (the HDSP-33xx series) character heights of either 0.3 or 0.4 inch (HDSP-31xx), in addition to single and dual-digit versions at up to 0.56 inch. All the displays employ AlGaAs red, GaP high-efficiency red, GaP green and GaP yellow LEDs (0.56 inch dual-digit in AlGaAs red only).

The displays are supplied in industry-standard sizes and pin-outs, and have been designed to offer evenly illuminated segments and uniform segment-to-segment brightness.
www.agilent.com

LumiLeds increases range of SMD LEDs

San Jose, CA LumiLeds Lighting has augmented its range of surface-mount (SMD) LEDs with blue, green and orange devices, which it says complement the red and amber emitters released last year. Applications include automotive dashboard backlighting, as well as full-color video signs and general indicators.

The blue and green emitters employ InGaN for the active regions, while the orange LED active region is AlInGaP-based. Operating at 20 mA, typical intensities of 220 mcd are available for the orange, 200 mcd for green and 100 mcd for the blue LEDs.
www.lumiledslighting.com

OSI samples OC-192 photodetectors

Hawthorne, CA OSI Fibercomm is marketing a new 10 Gbit/s photodetector for fiber-optic applications. Currently available in sample quantities, OSI's FCI-InGaAs-25C is based on an InGaAs/InP high-speed photodiode chip. OSI claims that the planar device architecture leads to a less expensive photodiode in comparison with devices with co-planar contact structures.

Applications include high-speed optical receivers in the 1310–1620 nm wavelength range, and picosecond optical time-measuring instruments. The device achieves a dark current of 100 pA at an operating reverse bias of 5 V. While the InGaAs photo-detector chips are designed and tested at OSI, they are currently manufactured externally.
www.osifibercomm.com

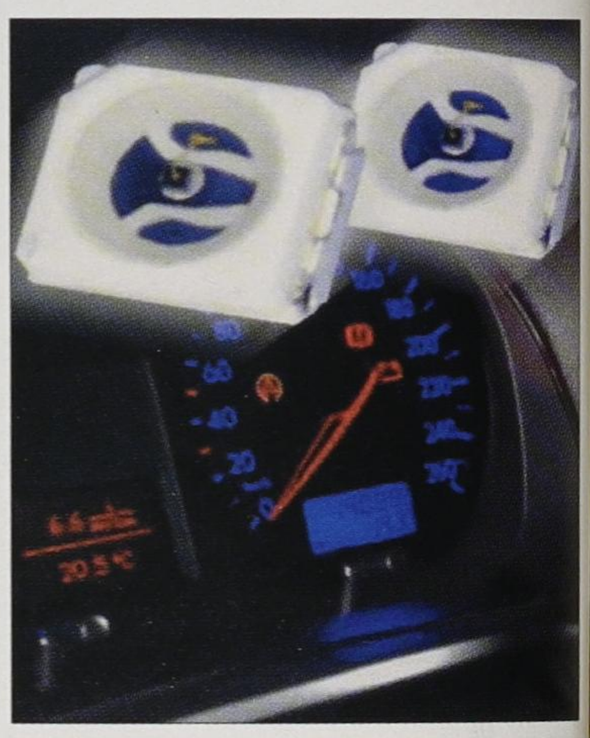
Vishay adds LEDs, Schottky diodes

Malvern, PA Vishay Telefunken has added blue, blue-green and true green emitters to its spectrum of high-brightness surface-mounted LEDs. The applications for the InGaN-on-SiC devices include backlighting and indicators in automobiles, phones, fax machines, and other equipment requiring backlit LCDs.

The emission of the blue device is centered on a wavelength of 470 nm, and the total luminous intensity is 40 mcd. The 505 nm blue-green device and 525 nm green emitters supply 130 and 180 mcd respectively.

All the chips are specified for a 5 V reverse voltage at 20 mA forward current and feature a 60° angle of half intensity. Housed in 1.65 × 2.8 × 2.4 mm thin profile packages, the devices are provided in 8 mm tape and reel form and are available in sample and production quantities.

The company has also introduced new Schottky diodes. The 103 series provides a maximum forward voltage



drop of 0.37 V at 20 mA forward current, and a maximum leakage current of 5 μA for a reverse voltage of 30 V. Each diode is rated for a single surge current of 15 A and typical junction capacitance of 50 pF at a frequency of 1 MHz.

The company suggests a range of applications including steering, biasing and coupling functions in fast-switching logic-level, DC-to-DC converters and low-current power supplies.
www.vishay.com

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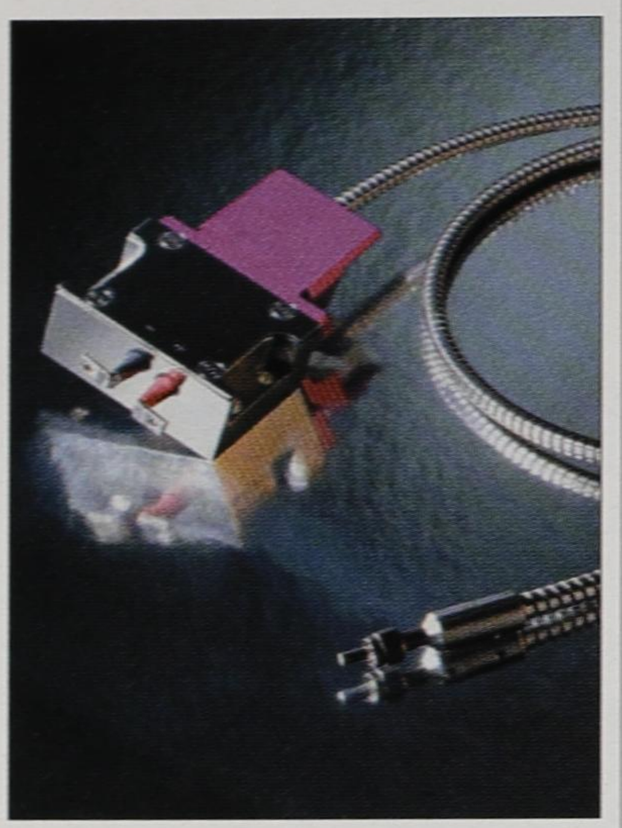
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ENABLING BANDWIDTH...
RIGHT FROM THE START

Fiber laser targets the medical field

Mountain View, CA Spectra-Physics Semiconductor Lasers (formerly Opto Power Corporation) has introduced a 30 W fiber-coupled laser



operating at 980 nm for medical therapeutic and surgical applications, including dermatology, plastic surgery, podiatry and wound care.

The laser delivers more than 80% of its rated power within a 0.12 numerical aperture, and easily couples to surgical fibers 300 μm in diameter and above using available optics.

The company's 30 W fiber-coupled device is available in high volume and can be customized for OEM users.

www.spectra-physics.com

WIRELESS PRODUCTS

Vector modulators suit 3G wireless

Lowell, MA A new vector modulator has been released by M/A-COM. The SA90-0001 is a current-controlled multi-chip module containing GaAs MMIC and silicon technology designed to improve linearity and reduce system costs.

The SA90-0001 targets the 1.94–2.24 GHz band, making it suitable for emerging 3G wireless communications standards. The SA90-0001 also allows the gain to be continuously adjusted over a minimum of 10 dB, while allowing the insertion phase to be adjusted over a full 360° range. This function is accomplished despite the small footprint of the 6 × 4 mm leadless FQFP-N plastic surface-mount package.

www.macom.com

Motorola unveils new SiGe amplifier

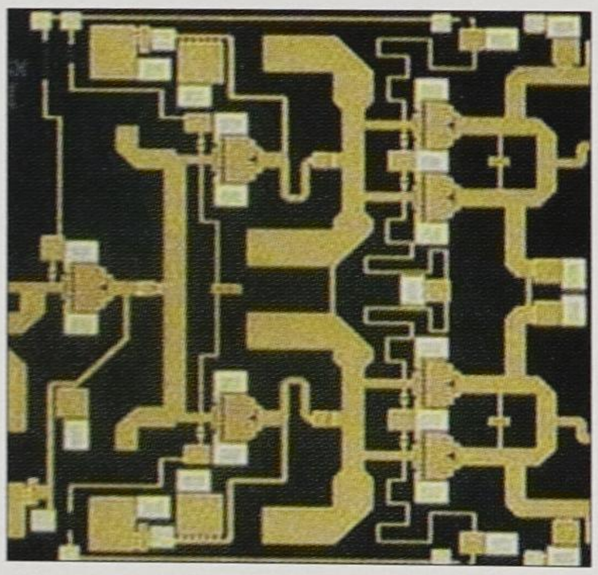
Phoenix, AZ Motorola has introduced a general-purpose wide-band SiGe:C amplifier. Manufactured by the company's RF BiCMOS process, the MBS13916 is housed in a SOT-343R surface-mount package and features on-chip bias control, while matching is achieved off-chip.

The device operates at up to 2.5 GHz, and at 900 MHz offers 19 dB of gain for a noise figure of 0.9 dB. Noise rises to 1.9 dB at 1.9 GHz. Available with a voltage supply range covering 2.7–5.0 V, the circuit offers 45 dB of reverse isolation at the device level (at 900 MHz)

www.motorola.com

Fujitsu releases three-stage MMICs

San Jose, CA Fujitsu Compound Semiconductor has developed a three-stage power



MMIC for VSAT applications in the 13.75–14.5 GHz range. The FMM5051VF offers a linear gain of 31.5 dB and 31.5 dBm output power, and is housed in a metal-ceramic hermetic package.

Three new three-stage GaAs MMIC PAs are also available for point-to-point or point-to-multipoint radio-link applications in the 17.5–23.6 GHz frequency range. The FMM5815X is a high-linearity amplifier operating in the 17.5–20.0 GHz range with an output power of 31 dBm and power gain of 21 dB. The FMM5805GJ-1 covers the 17.7–19.7 GHz band with an output power of 31 dBm and gain of 20 dB. Finally, the FMM5811GJ-1 is a wideband amplifier designed for the 17.7–23.6 GHz range. The device features an output power of 24.5 dBm and power gain of 15.0 dB.

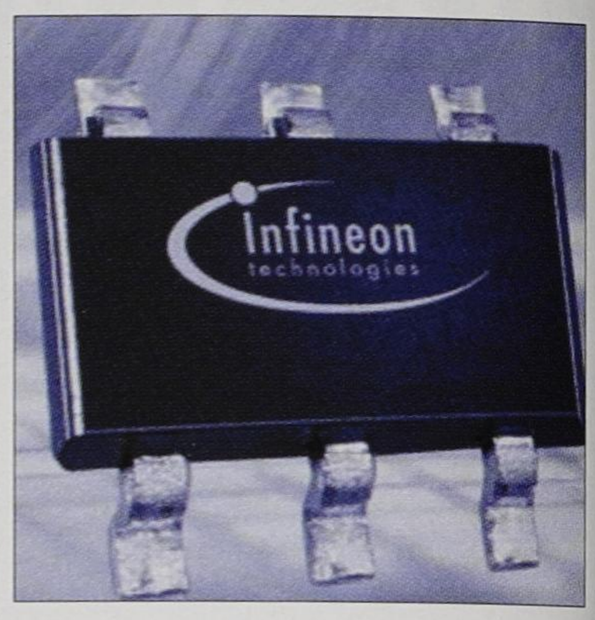
www.fcsi.fujitsu.com

Infineon launches PHEMT switches

Munich, Germany Infineon Technologies has released three GaAs PHEMT switches designed for multiband mobile phones, WLAN and Bluetooth products. The new circuits are suited to transmit/receive antenna switching, filter band selection and LO switching. These PHEMT switches can also be combined with duplexers and SAW filters.

The CSH210 (standard logic) and CSH210R (reverse logic) are general-purpose SPDT switches offered in a SOT363 (2 mm × 2 mm) package. The insertion loss is 0.3 and 0.4 dB at 1 and 2 GHz respectively, while the isolation is better than 24 dB at up to 1 GHz and better than 20 dB at up to 2 GHz.

Both switches achieve a P1dB value of 30 dBm when biased with a +3 V control



voltage. The CSH210P is a higher-power version of the CSH210 that achieves a P(–1dB) of 33 dBm and an IP3 of 56 dBm (at +3 V bias).

The company has manufactured all of the switches in its new 6 inch GaAs wafer fab facility. The switches are available now.

www.infineon.com

Microsemi ships silicon switches

Irvine, CA Microsemi has released a line of silicon antenna switches that compete with GaAs MESFET switches for 802.11a and HiperLAN2 broadband wireless LAN applications in the 5–6 GHz band. A variety of front-end components are on offer including antenna switches, protection, bias circuits, power limiters, power detectors and low-noise preamplifiers.

Microsemi's patented NanoMount design contains a surface-mount PIN diode matrix, which consists of four silicon MMSM PIN devices mounted on a ceramic substrate. These new switches offer configurations that emulate transfer, diversity, transmit/receive and single-pole double-throw (SPDT) functions.

The MNM4200 series offers wide-bandwidth and 10 CW incident power handling with an isolation of 25 dB and insertion loss of 1 dB at 6 GHz.

www.microsemi.com





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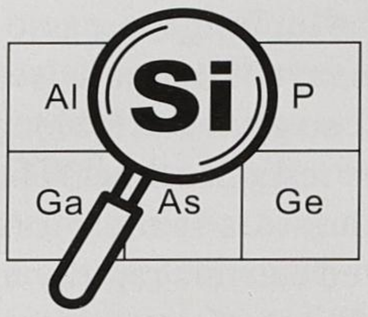
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New technique raises efficiency of Si emitters

Researchers are using techniques from the photovoltaics industry to improve the efficiency of silicon-based light emitters and bring their integration into silicon microelectronics a step closer.



Despite the challenge of using silicon as an emission source, this material has been used for many optical applications.

In a perfect world, silicon would be as wonderful at emitting light as it is at enabling an incredibly wide range of ICs. The ability to produce on-chip light could be used to transport data into and out of circuitry, eliminating the area-intensive problems and parasitics of metal I/Os that are becoming a real bottleneck in the advance of many circuit applications.

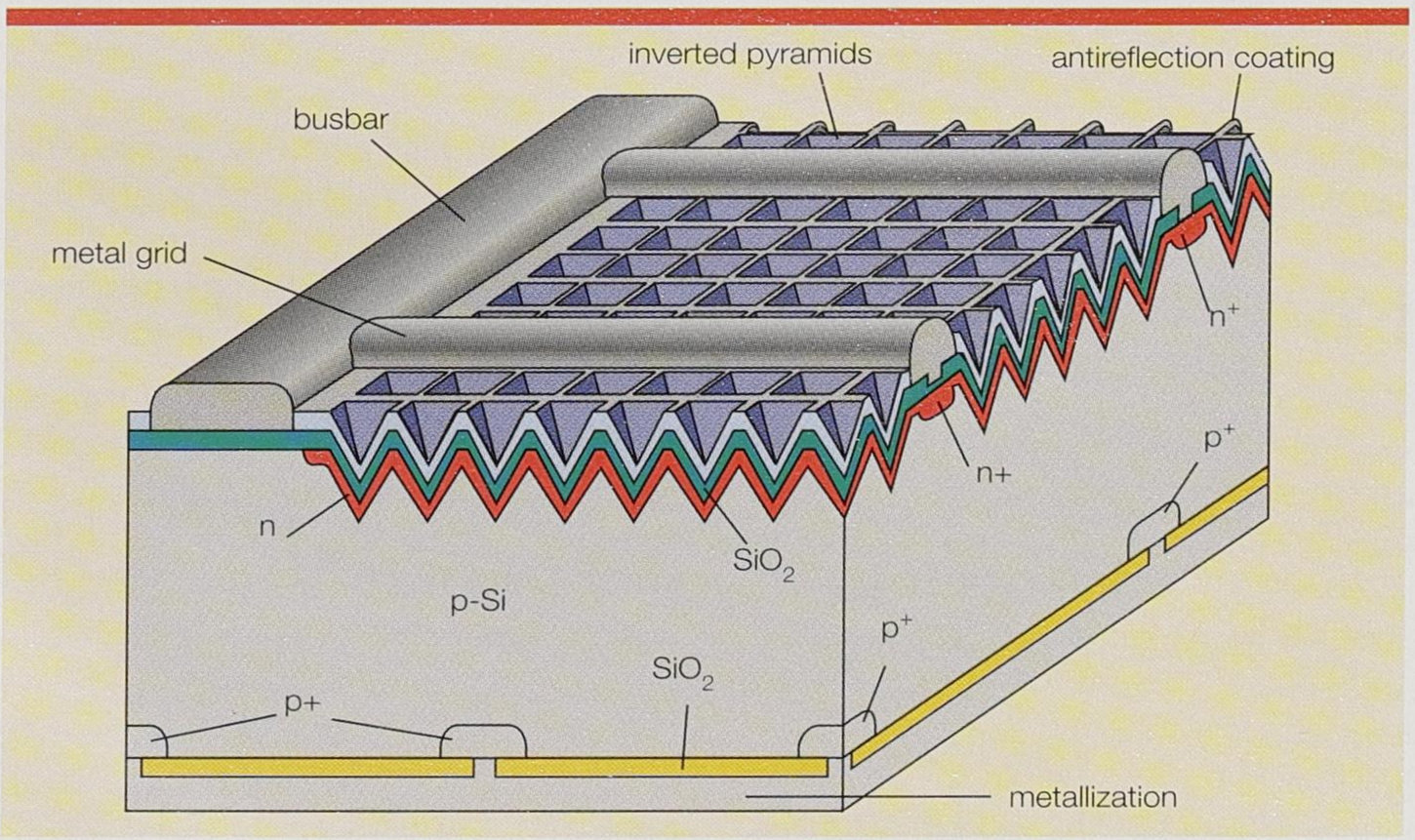
But as we well know, the indirect bandgap of Si makes it a poor emitter of light. The material requires more than simply an electron-hole pair to recombine; it also needs help from phonons. Many III-V materials do not require phonons, which allows them to dominate light-emission applications in the form of light-emitting diodes and lasers.

Decades of research

Because of the potential payoff of an efficient light-emitter in Si, extensive research has been done in this area for decades. This has ranged from basic concepts such as merged epitaxial processes (e.g. GaAs on Si growth), to more esoteric approaches such as the use of porous Si, amorphous Si, complex strained Si-based structures and SiGe/Si superlattices. While all of these approaches have been able to produce some level of optical emission, efficiencies have been incredibly poor, at best reaching 0.01–0.1%. None of these techniques has attained or even suggested a route that might lead to an emission technique that approaches the capabilities of III-V materials.

Despite the great challenge of using silicon as an emission source, this material has been used for many optical applications, in particular solar cells. State-of-the-art Si-based solar cells exhibit conversion efficiencies of 20%, while the very best III-V solar cells (cascaded cells with a wide range of bandgaps) exhibit a 30% conversion efficiency, representing only a 50% improvement over Si. In contrast, the ability of Si to emit light is typically three to four orders of magnitude lower than that obtained by III-V material devices. This discrepancy begs the question – is it possible to learn something from the fabrication of Si solar cells, which can crudely be viewed as light emitters operating in reverse bias? Researchers from the University of New South Wales (UNSW), Australia, have asked this question and found that knowledge gained from Si-based solar cells can be applied to the manufacture of high-efficiency Si light emitters.

As it turns out, Si does not really absorb light very well, especially if you want that absorption to generate an electron-hole pair and not simply heat up the material through the generation of phonons. A great deal of the light passing into a Si solar cell passes through the active and drift regions, through the substrate, and is collected in the backside metallization regions where it generates no power. To combat this limitation, state-of-the-art Si solar cells have textured front and back surfaces. The absorbed light makes many passes back and forth through the device, so more photons are captured and, with the aid of phonons, generate electron-hole pairs within a diffusion length of the device's electrical junction. A general rule of thumb for a material or device is that the better it is at absorbing light, the better it is at emitting it.



UNSW

Structure of the silicon LED developed by researchers at UNSW, Australia. The inverted-pyramid structure reduces reflection and increases absorption.

Turning an absorber into an emitter

The light emitters made by the UNSW researchers rely on the normally weak one- and two-phonon assisted sub-bandgap light emission that takes place in Si. The texturing method in Si photovoltaics to increase absorbance uses what are referred to as small internal escape cones. If the direction of the light entering a semiconductor surface with a refractive index n can have its path randomized, only a small fraction of that light can escape back out the surface. This fraction is proportional

In addition to improving absorption, the researchers took great care to reduce non-radiative recombination.

to $1/2n^2$. As a result, for weak absorption, where phonon assistance is needed to generate electron-hole pairs, absorption improves by a factor of $2n^2$, or about 25 times. Textured surfaces can also be used in solar cells based on III-V semiconductors. However, because electron-hole pairs are generated through direct energy transitions (no phonon assistance is required), the overall enhancement is not so great since conversion takes place before photons can typically escape the III-V material.

In a high-efficiency silicon emitter, inverted pyramid structures enhance effective absorption, in the same way that photovoltaic cells use escape cones (see figure, page 39). Backside reflectors ensure that photons are reflected back to the surface then back into the material at random angles from the pyramid surface. In addition to improving absorption, the researchers took great care with these devices to reduce non-radiative recombination. They accomplished this by using long-lifetime float-zone Si material, passivating all exposed surfaces with high-quality thermal oxides, keeping metal contact areas small, and reducing heavy doping (where free carrier absorption can occur) and keeping it localized to contact regions.

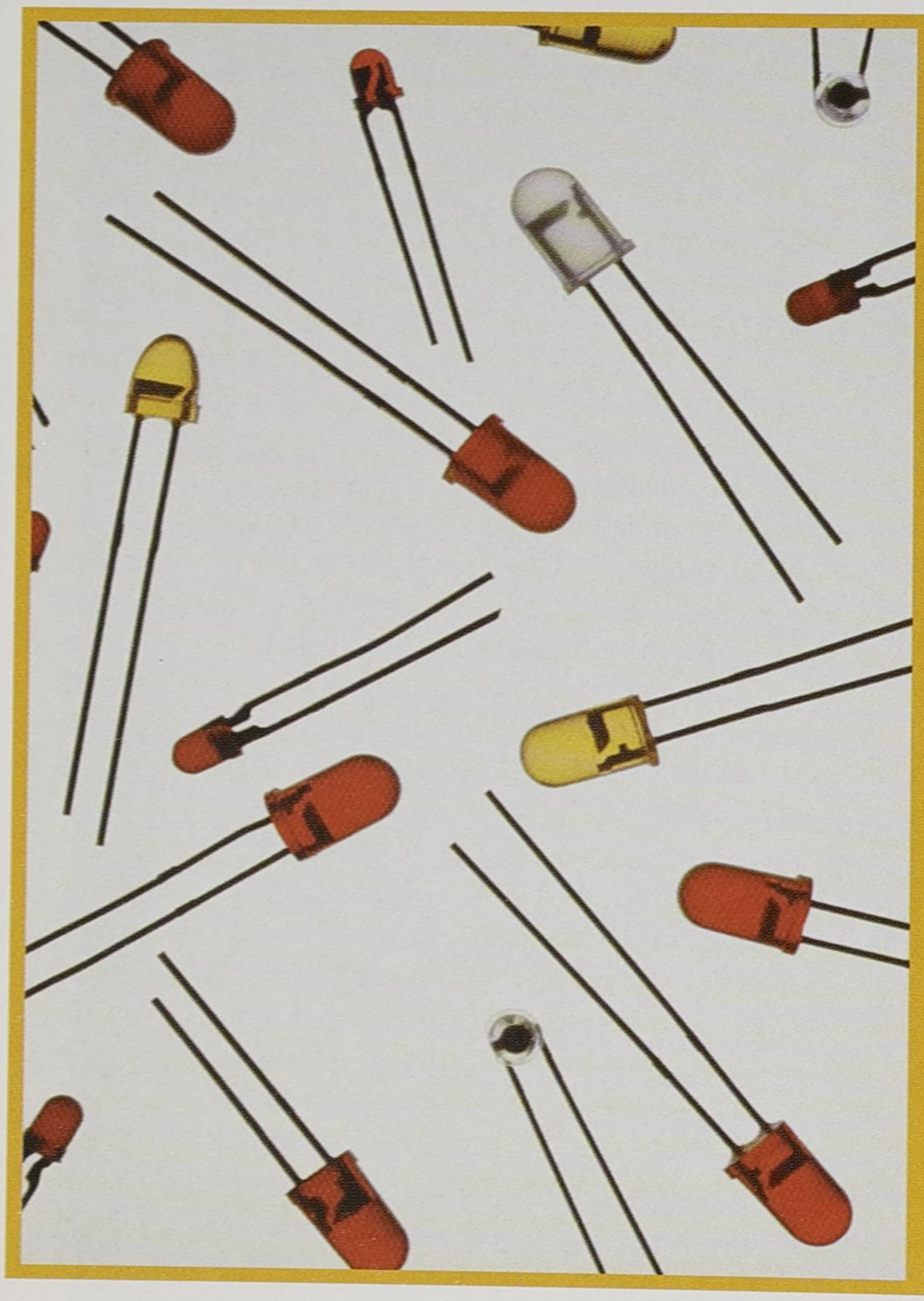
By enhancing absorption and reducing non-radiative recombination, the device shown in the figure emits light with an approximate efficiency of 1%. This represents an improvement of two orders of magnitude on efficiency results from other Si-emitter techniques. While this is still one order of magnitude lower than that obtained by III-V materials, the efficiency should be improved still further by increasing the thickness of the diode, reducing the doping concentrations and improving the reflectivity of the back surface.

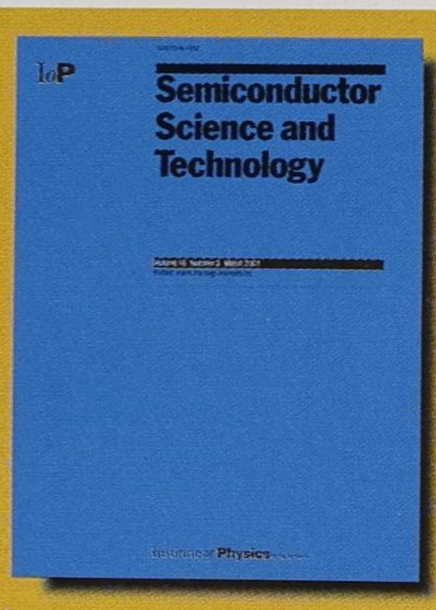
Looking to the future

In fact, this approach may mean that poor electrical-to-photonic efficiency is no longer the limiting issue associated with these devices. The next challenge arises because the material properties are so good that the long lifetimes of carriers make for slow response times. The integration of high-speed modulators is therefore necessary to sweep out long-lived carriers rapidly in order to permit high data rates. These issues aside, it appears that Si can no longer be referred to as a material that lacks the characteristics to make it an adequate emitter of light.

Further reading

M Green *et al.* 2001 Efficient Light-Emitting Diodes *Nature* **412** 805





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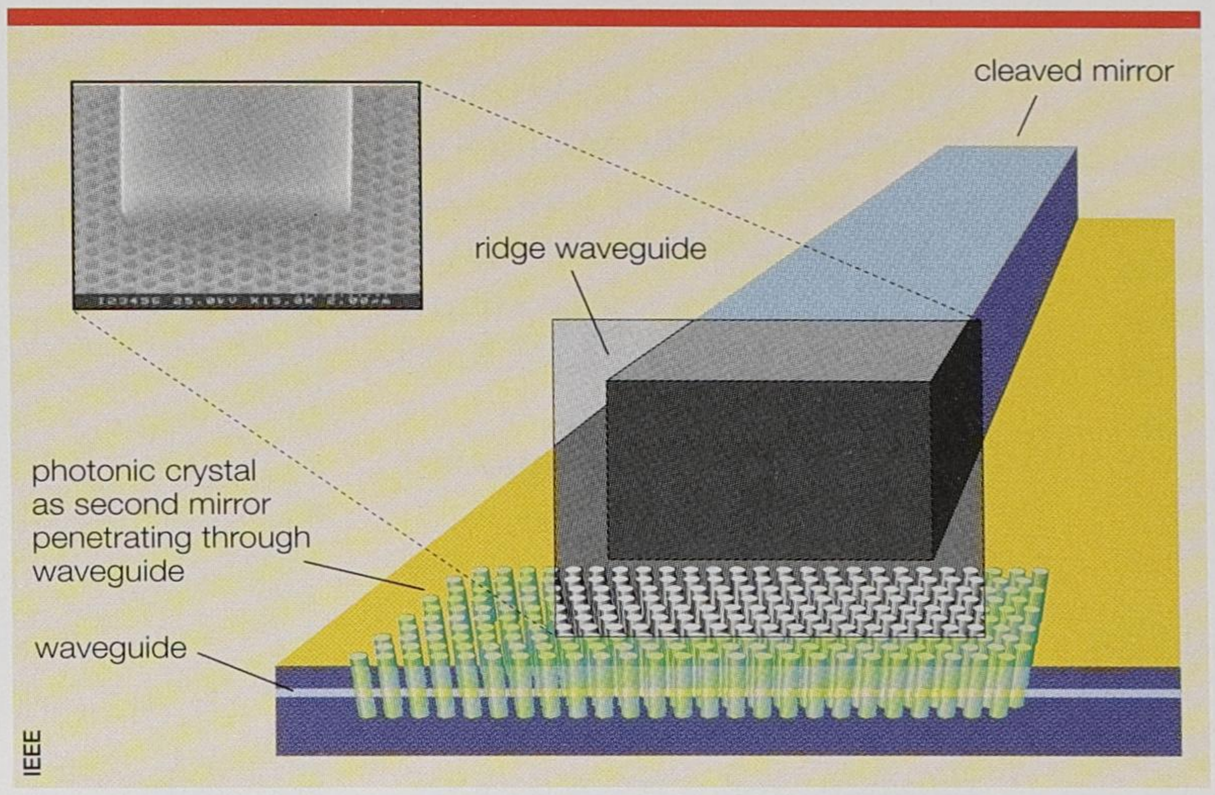
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Photonic crystals as laser mirrors

Photonic crystals are periodic dielectric structures with a bandgap that forbids the propagation of light in a certain frequency range. Such structures have attracted considerable interest, not least because they can be tailored to form waveguides on a scale not possible in a typical index waveguide structure. However, making such crystal structures is difficult, and this forms the focus of a recent paper by Moosburger and coworkers at the University of Wurzburg, Germany (*Phot. Tech. Lett.* 2001, **13(5)** 406). This describes high-quality two-dimensional photonic crystals for use as mirrors in ridge waveguide lasers.



Schematic of the ridge waveguide structure employing a photonic crystal as one of the mirrors by modifying the propagation characteristics of the light. The SEM inset reveals the high quality of the holes close to the ridge facet.

The lasers concerned are MBE-grown InGaAs/AlGaAs SQW GRINSCH structures with a ridge 2 μm wide and 600 μm long, with a photonic crystal as the second mirror. The mirror is formed using a wet-oxidized Al_2O_3 mask, which permits the subsequent dry etching of the holes that form the photonic crystal at one end of the ridge. The photonic crystal is defined using electron-beam lithography and shallow etching through the waveguide, which reaches a final depth of 600 nm. The result is a periodic series of holes at the waveguide facet that modify the bandgap of the photonic density of states. The period of these features changes the wave-guiding properties by controlling how the light propagates through the waveguide inside a "photonic bandgap". Outside of this bandgap, the reflectivity of the photonic crystal quickly drops compared with conventional cleaved facet lasers.

Using this photonic crystal as a mirror, the CW characteristics of the lasers show a decrease in the threshold current and an increase in efficiency compared with reference lasers with both facets cleaved. In addition these parameters markedly depend on the period (or photonic bandgap) of the photonic crystal; mirrors with periods of 200, 225 and 250 nm show a systematic decrease in threshold current and increase in efficiency with increasing photonic crystal period. The best results are obtained for a photonic bandgap of 250 nm, where the threshold current is 16 mA and the slope efficiency reaches 0.34 W/A.

Range of improvements boost AlGaN/GaN HEMTs

GaN-based HEMTs have considerable potential as high-temperature, high-power devices because of their wide bandgap and high saturated-electron drift velocity. In addition, AlGaN/GaN heterostructures exhibit high conduction-band offset and sheet carrier densities in the 10^{13} cm^{-2} range. Recent improvements in the material quality and device processing of AlGaN/GaN HEMTs (with 50 nm gate length) have taken current densities as high as 1.7 A/mm and achieved record f_t and f_{max} values of 100 and 140 GHz respectively.

V Kumar and colleagues (*Electron. Lett.* 2001 **37(13)** 858) have described MBE-grown AlGaN/GaN HEMTs on sapphire substrates with comparable performance and larger gate lengths of 0.25 μm. The devices had undoped layers of 2 μm of GaN, 30 nm of $Al_{0.24}Ga_{0.76}N$ and a 5 nm cap. The sheet carrier concentration was 1.5×10^{13} cm^{-2} and the electron mobility was 1170 cm^2/Vs.

After the device was formed into a structure with a 0.25 μm T-gate, DC measurements revealed a maximum drain current density of 1.39 A/mm at a gate bias of 2 V and drain bias of 7 V. RF measurements at a gate bias of –6.7 V and drain bias of 10 V meant an f_t of 67 GHz and f_{max} of 136 GHz, which the researchers believe are among the highest reported GaN-on-sapphire FETs with this gate length.

Lead-salt VCSELs reduce the lasing threshold

While considerable advances have been made with edge-emitting lasers in the mid-infrared region, only a few attempts have been made to fabricate VCSELs at these wavelengths. These include II-V, II-VI and IV-VI optically pumped VCSELs operating at a wavelength greater than 2.5 μm. A paper, by C Felix *et al.* from the Naval Research Labs and the University of Oklahoma (*Appl. Phys. Lett.* 2001 **78(24)** 3770), reports the operation of a VCSEL with a lead-salt (PbSe) active region. The authors say that this has the potential to lower the lasing threshold by a factor of four.

The structure consists of a (111) BaF_2 substrate, three period $Pb_{1-x}Sr_xSe$(235 nm)/BaF_2(732 nm) bottom mirror stack, and a half-λ cavity containing eight PbSe(30 nm)/$Pb_{1-x}Sr_xSe$(25 nm) QWs. The structure was completed with a three-period $Pb_{1-y}Sr_ySe$(291 nm)/BaF_2(732 nm) top mirror stack and a 10 nm BaF_2 cap layer. The concentrations of x and y are 3% and 15% respectively, and the top and bottom mirrors exhibit reflectivities of 99 and 98%.

The device was optically pumped using 2 μm radiation, and the cavity emitted at an almost constant wavelength of 4.44 μm for operation at 200–280 K. The gain peak resonated at 260 K, where the threshold pump intensity was 10 kW/cm^2, which compares with more than 200 kW/cm^2 for III-V mid-infrared VCSELs at this temperature. A total output power of 330 mW and power conversion efficiency of 0.4% were also recorded. The authors say thinner PbSe QW regions should improve the threshold intensity further.

Announcing Purification for MOCVD Production Tools

Aeronex Infinity Gas Purification Systems provide a continuous supply of pure gas at ambient temperature

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In MOCVD and MBE films, atomic oxygen shifts the emitted wavelength, increases the bandwidth for optical devices, reduces device life through lattice instability, and decreases the carrier mobility in the film, thereby reducing the speed of the device. Aeronex purification technology improves the performance and lifetime of compound semiconductor optoelectronic and wireless devices by removing oxygen and other contaminants.

Without Interruption

As the process moves from R&D to Production, demand increases for purified nitrogen, hydrogen, and ammonia. Previous purification technologies required halting the process to replace the purifier bed. Today's process engineers require a high flow of pure gas and continuous up-time to maximize return. To meet these challenges Aeronex has developed the Infinity GPS™, which delivers a continuous supply of ultra pure gas without interruption.

Performance

Aeronex purifier technology sets the standard for pure gas. The patented media removes contaminants such as moisture, oxygen, CO, CO_2, and hydrocarbons from gas or liquid sources. This unique inorganic media operates at room temperature and handles high flows at very low pressure, a requirement for next generation MOCVD equipment.

To provide a continuous supply of pure gas, the Infinity is designed with two purifier beds in parallel. While one bed is on-line, the second is automatically regenerating. Preconditioning time is eliminated, as is running on a spent or cracked purifier. No special gas blends are needed for start-up and hydrocarbons are never outgassed.



Value

The Aeronex purifier delivers the lowest cost of ownership. The Infinity GPS provides continuous savings through reduced labor and continuous uptime (see graph below). Competitive purifiers become a hazardous waste once spent, generating high costs in time, money, and liability. All related downtime and disposal costs are eliminated.

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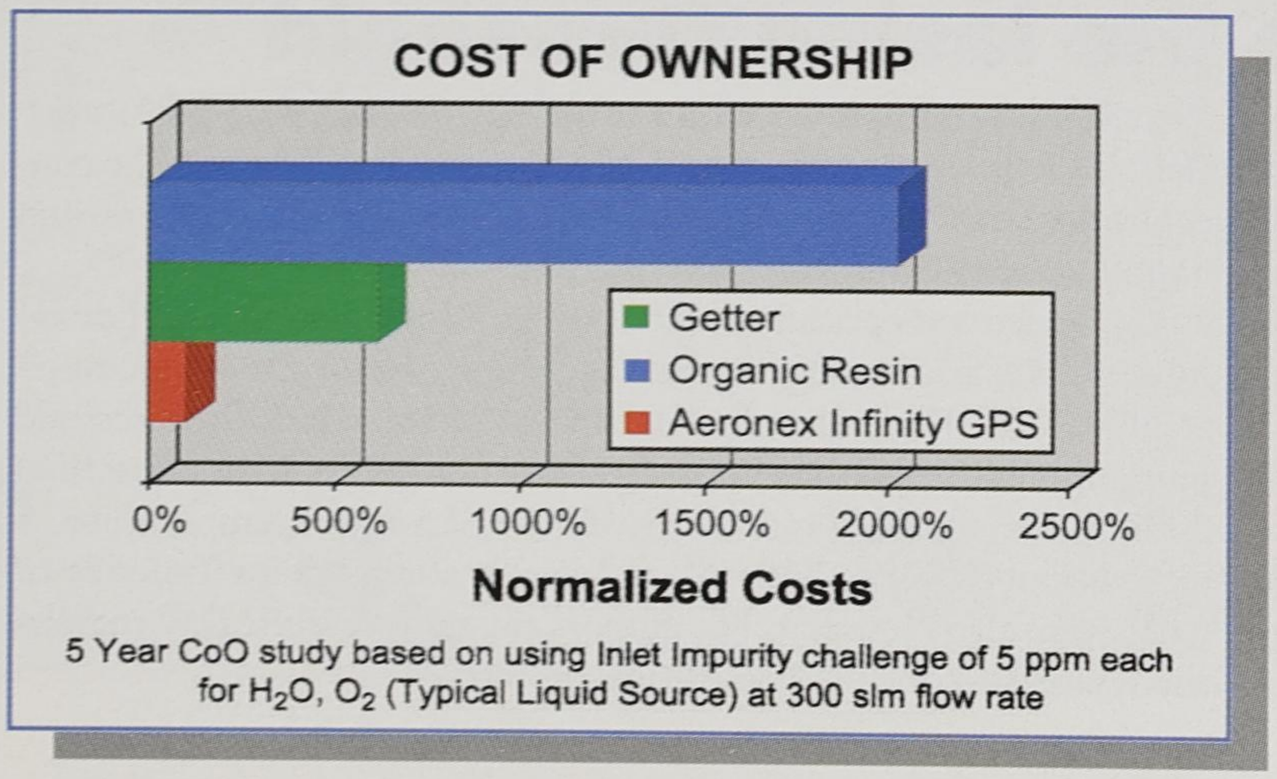
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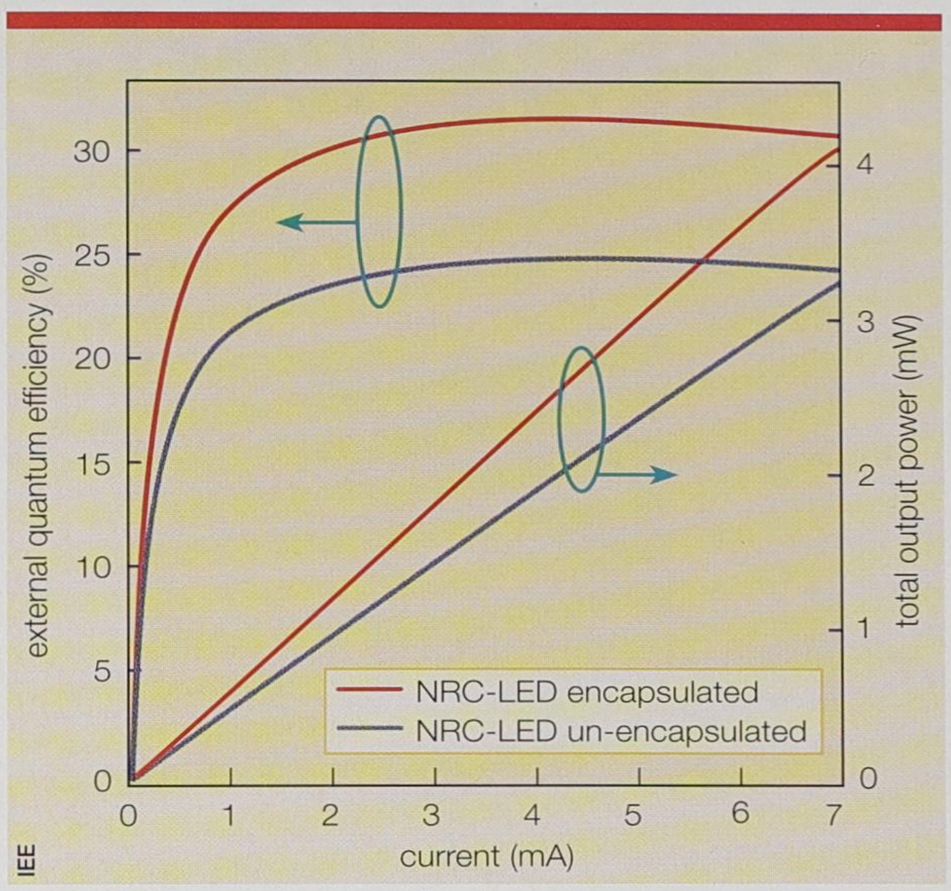
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Thin-film 650 nm LEDs get efficient

The efficiency of light extraction from a semiconductor is limited by the large difference in refractive index between the semiconductor and air. One method for improving the light extraction from surface-emitting LEDs is to texture the light-outcoupling surface and to apply a rear reflector. This gives photons multiple chances to escape from the semiconductor. Such a device is called a non-resonant cavity (NRC) LED. Now surface-textured thin-film LEDs have for the first time been demonstrated on 650 nm GaInP/AlGaInP LEDs by Rooman and colleagues who are working at IMEC, Belgium (*Elec. Lett.* 2001 **37(13)** 852).

The LED structure consists of a 120 nm thick GaInP active layer with AlGaInP carrier confinement layers above and below. Above the upper confinement layer, a 100 nm $Al_{0.98}Ga_{0.02}As$ layer is grown for lateral oxidation followed by a 2000 nm AlGaAs hole-spreading layer. A current-confining aperture 42 μm in diameter is formed by selectively oxidizing the $Al_{0.98}Ga_{0.02}As$ layer. The topside of the devices is roughened using natural lithography, involving ion-beam etching through a mask of randomly distributed polystyrene spheres. The etch causes cylindrical pillars to form underneath each sphere, which act as a diffraction grating. After wet chemical etching removes the original GaAs substrate, the epitaxial film is Van der Waals-bonded on a polyimide-coated Au mirror which is fabricated on a host substrate such as silicon or GaAs.



Performance comparison for encapsulated and un-encapsulated non-resonant cavity LEDs.

The efficiency is improved further by encapsulating the LEDs in hemispherical lenses made from UV-curable glue. The figure shows the optical output power and the external quantum efficiency of the NRC-LEDs before and after the encapsulation process. At 7 mA the LEDs emit 3.2 mW before encapsulation and 4 mW after encapsulation.

The devices reach a maximum external quantum efficiency of 24% before and 31% after encapsulation. This external quantum efficiency is 11 times better than conventional LEDs can achieve. These are the highest external quantum efficiencies so far reported for 650 nm LEDs emitting from a single surface. The researchers say that optimizing the surface texturing parameters and the processing should improve the performance of the device still further.

Annealing can improve luminescence efficiency

Group III arsenide nitrides are promising materials for 1300 and 1550 nm optoelectronic devices grown on GaAs substrates, and studies have shown that annealing significantly improves their luminescence efficiency. This has been attributed to the annealing's reducing the concentration of competing non-radiative defects, but the form of these defects remains unclear. Finnish researchers at the Optoelectronics Research Center at the Tampere University of Technology, the University of Helsinki and the Helsinki University of Technology have now published work on improving the luminescence efficiency of Ga(In)NAs materials by annealing (*Appl. Phys. Lett.* 2001 **79(8)** 1094).

The material was grown by nitrogen plasma MBE. Positron annihilation experiments found the concentration of Ga vacancies to be 4.2×10^{16} cm^{-3} in $GaIn_{0.06}N_{0.02}As$. This suggests that the Ga vacancy defects in N-containing samples are related to the energetic N ion-induced damage. The other source of Ga vacancies is the lower growth temperature used to avoid phase separation in the arsenide-nitride materials. The cations do not migrate far enough at this temperature, contributing to the formation of Ga vacancies.

Nuclear reaction analysis, in conjunction with Rutherford backscattering spectrometry (RBS) used in the channeling geometry, shows that 2.5% of the nitrogen sits at interstitial lattice sites in the as-grown $GaAsN_{0.03}$ material. After annealing at 700 °C for 30 seconds, this decreases to 0.3%, and the interstitial-to-substitutional ratio of RBS yields increases slightly. This indicates that most of the N interstitials reoccupy the substitutional sites, possibly through a kick-out mechanism. Even for the low N-content as-grown sample (x = 0.72%), the concentration of N interstitials is very high (2.3×10^{19}), suggesting that N interstitials are the major defects in arsenide nitrides, due to the strong differences in electronegativity and size between As and N atoms. These defects are believed to be responsible for the low luminescence efficiency of as-grown Ga(In)NAs and the enhanced diffusion process during annealing.

Integrated EAM and DFB laser hits 40 GHz mark

Researchers at Oki Electric in Japan have succeeded in operating a monolithically integrated electroabsorbtion modulator (EAM) and distributed feedback (DFB) laser at 40 Gbit/s (*Phot. Tech. Lett.* 2001 **13(9)** 954). Though such bit rates have been reported before, bandwidths have been below the 41 GHz reported by the Oki group.

The laser and EAM lengths were 350 μm and 100 μm, and were integrated by butt-jointing to allow the sections to be optimized independently. The EAM length was chosen to reduce capacitance to allow 40 Gbit/s operation while maintaining an acceptable extinction ratio.

An open eye diagram with 12 dB extinction ratio was obtained for 40 Gbit/s non-return-to-zero (NRZ) modulation. This was maintained during transmission testing by passing the modulated signal along an 80 km fiber. Output powers were –1.6 dBm and –0.9 dBm for extinction ratios of 12 and 11 dB, respectively, at 40 Gbit/s.

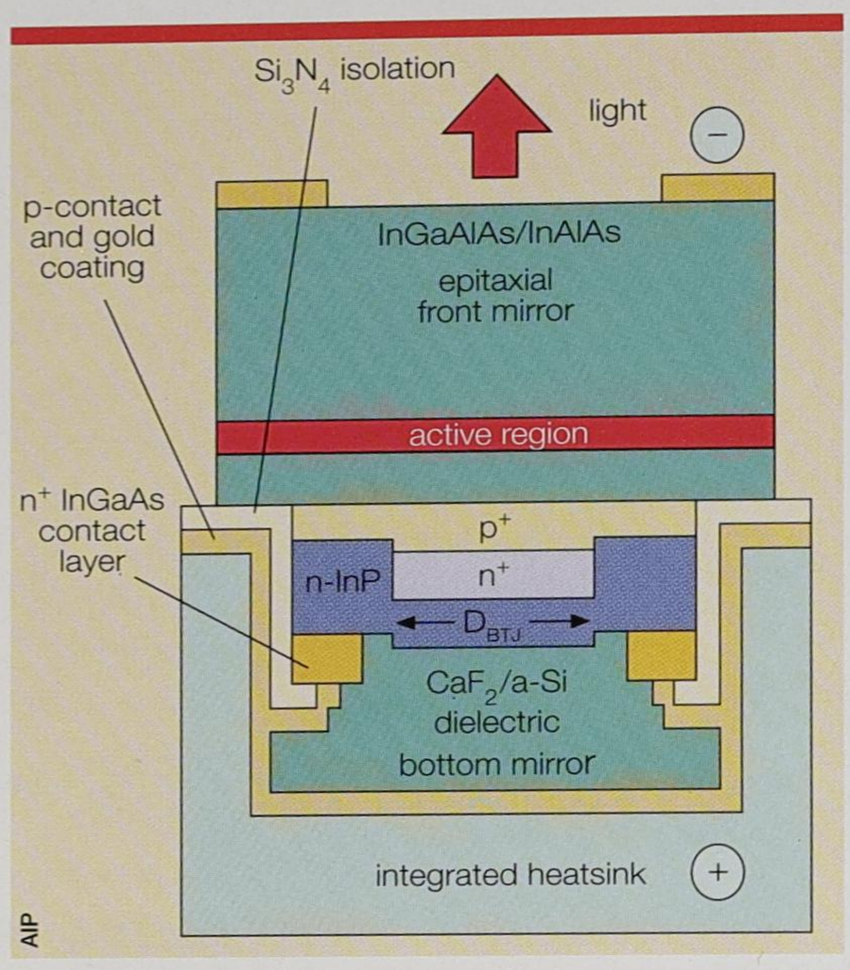
Tunnel junctions enhance long-wavelength VCSEL performance

The development of long-wavelength VCSELs emitting at 1300 nm and above has faced a number of fundamental problems. One is the integration of the InP-based active region with suitable epitaxial Bragg mirrors, as the obvious materials to use for the mirrors may not be compatible with the materials in the active region.

The epitaxial mirror's high thermal resistance and the heat generated by high p-side series resistance make device performance strongly dependent on temperature. Until recently the best performances reported for VCSELs in the 1300–1550 nm range were for devices using AlAs/GaAs DBRs that have been either fused with the active region or grown metamorphically.

In results reported in a paper to be published in *Electronics Letters*, Ortsiefer *et al.* of the Walter Schottky Institute, Germany, have demonstrated a VCSEL emitting at 1550 nm that the authors claim outperforms 1550 nm VCSELs fabricated by any other method. The device uses a buried tunnel junction (BTJ) and dual epitaxial growth to overcome many of the problems of standard fabrication methods (*Appl. Phys. Lett.* 2000 **76(16)** 2179). The front DBR mirror is grown first using MBE and has 35 periods of Si-doped (n-type, 1×10^{18} cm^{-3}) InGaAlAs/InAlAs. The active region comprises five compressively strained 8 nm InGaAlAs quantum wells, separated by 7 nm tensile strained barriers. The active region is surrounded by 50 nm thick InAlAs cladding layers. The final MBE growth step produces a 32 nm thick n^+ InGaAs on a p^+ InGaAlAs layer that forms the BTJ. This is processed laterally to give the tunnel junction the desired cavity diameter (D_{BTJ}).

In the second phase of epitaxy, n^- InP and n^+ InGaAs contact layers for lateral current injection are grown by CBE. The bottom dielectric mirror consists of a 2.5 period CaF_2/a-Si layer deposited by electron-beam evaporation to a thickness of 25% of the desired emission wavelength. The substrate on top is then completely removed and a gold heatsink is applied to the bottom by electroplating. This removes heat passing through the dielectric mirror and provides a low thermal resistance.



The WSI VCSEL structure features an integrated heatsink and buried tunnel junction. Minor changes have enabled researchers to make VCSELs which emit at wavelengths ranging between 1300 nm and 1830 nm.

Using a D_{BTJ} of 20 μm an output power exceeding 7 mW has been achieved at 20 °C with 1550 nm CW emission. Threshold current and voltage were 6 mA and 0.9 V respectively. The combination of low threshold voltage and high output power results from the BTJ's low series resistance. Shrinking D_{BTJ} allows the threshold current to be reduced further, but also limits output power. A D_{BTJ} of 5x6 μm produced a threshold current of 0.92 mA at 40 °C. The maximum lasing temperature exceeded 110 °C, with a CW output power of 0.5 mW at 80 °C.

The group has recently demonstrated modulation at 2.5 Gbit/s and expects the low series resistance to enable 10 Gbit/s operation in the near future. A 1300 nm VCSEL has also been demonstrated using the BTJ structure.

The group has also made VCSELs operating at 1830 nm with minor modifications to the structure (*Phot. Tech. Lett.* 2000 **12(11)** 1435). One application at this wavelength is gas sensing. Sensitive detectors based on laser absorption by a gas require singlemode emission, but also tunability across a range of wavelengths to give access to the absorption bands of different gasses. A device with a D_{BTJ} of 4 μm meant a maximum temperature for CW operation of 90 °C. Between 10 and 50 °C the threshold current varied from 0.30 to 0.36 mA. Using a temperature-controlled Cu submount enabled the laser emission wavelength to be tuned by adjusting the temperature. Between 5 and 85 °C, the wavelength varied from 1829 to 1839 nm.

Tunnel diode improves metal-mirror RCLEDs

Resonant-cavity LEDs (RCLEDs) offer considerably improved emission-source linewidth compared with LEDs, making them a promising optical source for fiber-optic communications. However, some material systems do not have compatible semiconductor DBRs, making them expensive to grow in large stacks to achieve the required reflectivity. Thus the integration of low-cost metal mirrors is highly desirable. The metal layers typically employed with semiconductors are not good reflectors, particularly after they are annealed.

Zhu and colleagues from Purdue University have used a tunnel-diode structure on top of the LED heterojunction, which forms a smooth p-type GaAs surface for metal-mirror attachment (*IEEE Phot. Tech. Lett.* 2001 **13(2)** 103). In this work, Au-Ge-Ni or Au-Zn alloys systems are replaced by Ag for the LED ohmic contact. This provides a smooth Ag–GaAs interface and behaves as a high-reflectivity mirror (with approximately 94% reflectivity).

The RCLED was grown by MBE on a p-GaAs substrate, and consisted of a p-type stack of 20 nm GaAs, 0.5 μm $Al_{0.3}Ga_{0.7}As$, 0.53 μm GaAs and a 15 nm region graded from i-GaAs to i-$Al_{0.3}Ga_{0.7}As$. A 0.5 μm layer of n-$Al_{0.3}Ga_{0.7}As$ precedes the growth of the tunnel diode layers (20 nm n-GaAs and 10 nm p-GaAs) at 450 °C. The device operates at a wavelength of 890 nm, with a spectral linewidth of 20 nm, compared with approximately 50 nm for LEDs. The tunnel diode does not affect the optical performance, indicating its suitability as a contact for RCLED systems in which DBRs are difficult to grow.

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Motorola and IQE grow GaAs on large-area Si substrates

Motorola, in collaboration with IQE, has demonstrated the growth of gallium arsenide on large-area silicon substrates. This could open the way to low-cost GaAs device manufacturing and a multitude of integration possibilities, writes **Marie Meyer**.



MOTOROLA

Motorola research team members Jamal Ramdani (left) and Ravi Droopad display a 12 inch GaAs-on-silicon wafer, grown by MBE using a strontium titanate buffer layer.

Researchers from Motorola are claiming a breakthrough that may enable GaAs and other III-V compounds to be grown on silicon substrates in a commercially viable manner. This technology could lead to significant cost savings as well as monolithic integration of silicon and compound semiconductor devices, and possibly other new device structures. "It is a really disruptive technology," said Ravi Droopad, a member of the research team at Motorola's Physical Science Research Labs in Tempe, Arizona. Working with IQE, Motorola has already demonstrated 8 and 12 inch GaAs-on-Si wafers that are free from cracks and delamination of the epitaxial layers. Droopad says that work is also being done on the growth of InP, and other materials, on silicon.

The key to this new technology is the use of a thin layer of strontium titanate (known variously as strontium titanium oxide, $SrTiO_3$ or STO) between the silicon substrate and the GaAs layer. The STO acts as a compliant buffer layer, reducing the mechanical strain and the thermal mismatch between the epitaxial GaAs layer and the silicon substrate. After the Si-STO-GaAs structure is complete, device structures can be fabricated on top of the GaAs layer using conventional epitaxial growth and wafer processing technologies. "The GaAs layer is thick enough to function as standard GaAs," said Dennis Roberson, chief technology officer of Motorola Labs. "There is no difference whatsoever from bulk GaAs."

Motorola has fabricated power amplifiers from the GaAs-on-Si wafers and incorporated them into mobile phones that have been used in live trials. While many other companies have looked at GaAs-on-Si in the past, this appears to be the most successful effort ever reported. Motorola engineers believe the new technology can also be applied to optoelectronic devices such as LEDs and optical communications components.

Motorola has filed for more than 270 patents on the technology, and a company spokesperson said that some of the early key applications have been approved, providing the impetus for announcing the breakthrough via a press release on 4 September.

Motorola has fabricated power amplifiers from the GaAs-on-Si wafers and incorporated them into mobile phones that have been used in live trials.

Commercialization

Padmasree Warrior, a Motorola vice-president, will head-up efforts to commercialize the new technology. She is the former chief technology officer for Motorola's Semiconductor Products Sector (SPS). However, the commercialization effort will not be part of SPS's operations, but will instead be located in a different area of Motorola's corporate structure – an interesting fact in light of the widely-circulated rumors that Motorola is trying to sell or spin-off SPS.

"Our business model for commercialization is to license the technology broadly into different market segments," said Warrior. She says that Motorola's patent portfolio "covers the whole value chain", beginning with the GaAs-on-Si substrate and continuing with epitaxy, device manufacturing, device/module integration, and on up through systems built using the devices. Warrior indicated that Motorola would be exploring licensing opportunities at each of these five levels. IQE, as a development partner, will apparently enjoy a period of exclusivity with regard to supplying epiwafers based on the new technology.

Motorola SPS is already working on GaAs-on-Si RFICs, with a goal of having products in the marketplace by 2003. Warrior said that applying GaAs-on-Si as a "substitutional technology" to replace existing parts, primarily on the basis of lower costs, is a logical first step. But what she is really excited about are completely new applications, perhaps some that haven't even been imagined yet. "I believe that the technology's biggest impact will come from new opportunities for integration, building circuits with compound semiconductors and silicon on the same chip," she said.

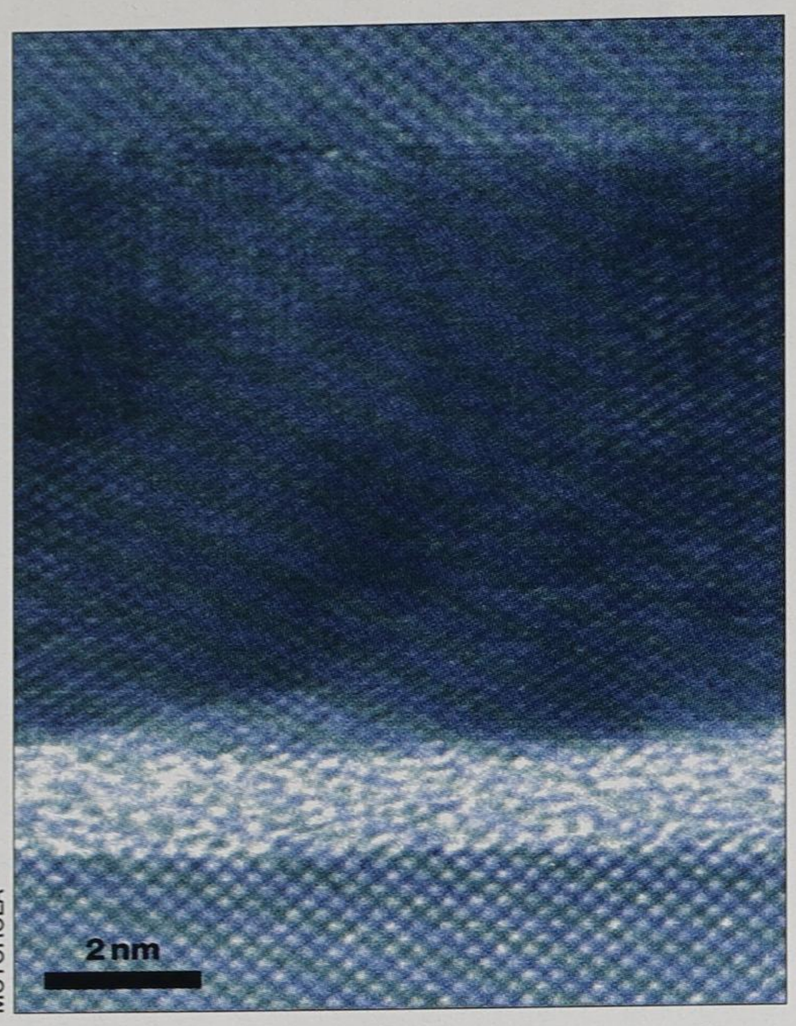
The technology

Motorola's approach has succeeded partly because of the 2.3% lattice mismatch between GaAs and single crystal STO. While this is an improvement over the 4% mismatch that exists between GaAs and silicon, Droopad says this fact alone is not enough to be decisive. He notes that dozens of research groups have reported success in growing GaAs-on-Si, employing a variety of buffer layers and other tricks in the epitaxial growth. "The MRS meetings used to have whole sessions on this topic in the 1980's," he said. However, most of the work was eventually abandoned when it became obvious that the resulting material was not suitable for use in devices. Conquering the lattice mismatch was only part of the problem. The real challenge to be overcome was that the thermal expansion coefficients of GaAs and silicon differ by almost 50%. As a result, when GaAs is grown directly on silicon substrates, significant numbers of defects, or even cracks, occur when the structures are cooled from the growth temperature to room temperature.

Droopad says that Motorola's work began two years ago. The original project was an investigation of STO as a possible replacement for SiO_2 in CMOS devices (see *Compound Semiconductor* September 2001, p35 for details of related work). The team observed that during the growth of the STO layers, oxygen atoms tended to diffuse down toward the Si–STO interface, resulting in an amorphous SiO_x layer. The lattice mismatch between STO and silicon is 1.7%. One of the Motorola researchers, Jamal Ramdani, realized that the amorphous layer removed the strain from the STO, allowing it to relax back to its natural crystal lattice constant. When GaAs is grown on the STO layer, it "sees" only the single crystal lattice of the buffer material (figure 1).

At the same time that this discovery was being made, there was a great deal of interest in the scientific community about "compliant" substrates that could accommodate epitaxial mismatches. Two models were being discussed: use of a viscous buffer layer that allows the substrate to be elastically compliant with the epilayer; and use of a thin twist-bonded layer that plastically deforms to adopt the epilayer lattice. Both models rely on bonding technology, which can be expensive and complex, so the Motorola team began wondering if the amorphous layer might be a way to achieve the same effect without wafer bonding.

The results thus far seem to indicate that it



MOTOROLA

Fig. 1. TEM cross-section of the strontium titanate (STO) buffer region; diffusion of oxygen atoms toward the Si–STO interface results in an amorphous SiO_x layer which removes the strain from the STO layer allowing it to relax back to its natural lattice constant. The layers are, from top to bottom: GaAs; STO; amorphous SiO_x; silicon.

If the technology can be extended to InP, it may be the ideal solution for reducing the costs of integrating and packaging optical components for networking applications.

can. Both Droopad and Tom Hierl of IQE say that the 8 and 12 inch wafers they have grown using this new technique are visibly superior to any previous attempt at GaAs-on-Si growth they have seen; there are no visible cracks or bowing, and no sign of the epitaxial layer peeling away from the silicon substrate. They report that the defect densities are comparable to those found in homoepitaxy of GaAs on LEC GaAs substrates, and Motorola has successfully run samples through their processing lines at the SPS division.

The exact role that the amorphous SiO_x layer plays is not yet understood. But it is believed that it is sufficiently compliant to the materials on either side of it to "soak up" the thermal and mechanical strain in the structure. Droopad says that the amorphous layer is "very pliable, very accommodating" to the stresses around it. Extending the technology to other III-V materials (for example, InP-on-Si or GaN-on-Si) will require substituting another perovskite material for the STO layer, in order to achieve a more suitable lattice constant.

Droopad says that the STO layer is "very thin," and Hierl adds that this is an important key for economic viability. The STO layer is epitaxially grown in the same molecular beam epitaxy (MBE) chamber as the subsequent GaAs growth, using elemental strontium and titanium in standard effusion cells. Oxygen is introduced through a leak valve. While strontium evaporates readily (at a comparable rate to antimony), titanium has a fairly low vapor pressure, requiring the use of very high temperatures and slow growth rates. Thus the thickness of this layer has a big impact on the cost of this step of the process.

IQE has shown that after the STO and GaAs layers have been grown, the wafer can be removed from the MBE system and transferred to a different reactor – MBE or MOCVD – where it can be used as a substrate for the growth of the same types of III-V layers that can be grown on bulk GaAs substrates. Hierl says it may also be possible to grow the STO layer via MOCVD, but this has not yet been tried.

New design considerations?

Whether or not the GaAs-on-Si substrates can serve as direct replacements for conventional GaAs substrates is not yet clear. All existing GaAs IC designs were created with the idea of leveraging the semi-insulating properties of undoped GaAs substrates to achieve small parasitic capacitances, good DC isolation, etc. It remains to be seen whether the new technology can provide a substrate with similarly high resistivity (the current samples have a resistivity of ~100 Ω.cm, whereas the value for a typical SI GaAs substrate is 10^8 Ω.cm). If not, steps will have to be taken to make up for this lost advantage. IQE's Tom Hierl indicated that different types of silicon wafers are being evaluated to increase the resistivity of the substrate. In the meantime, Motorola is using low-temperature (LT) GaAs buffer layers. LT GaAs is non-stoichiometric, with 1–2% excess arsenic atoms. This leads to

a significant increase in resistivity, up to 10^6–10^7 Ω.cm. Droopad says that head-to-head comparisons have been made of conventional GaAs MESFETs and GaAs-on-Si MESFETs with LT GaAs buffer layers, and performance was "95% comparable to commercial FET products".

Optoelectronics applications will face the opposite challenge: here it will be necessary to emulate a conducting substrate. Droopad indicated that the most obvious approach would be to dope the STO layer to make it conductive. "STO can be made pretty conductive," Droopad said. "I don't see any major issues in optoelectronics that can't be overcome by engineering."

A disruptive technology

Conversations with representatives of Motorola and IQE reveal several possible advantages of this new technology – provided that it can be successfully commercialized.

- It could extend the life of current 8 inch silicon fabs, by giving them a cost advantage over 6 inch GaAs fabs, and a performance advantage over CMOS, BiCMOS and SiGe. Only a small re-tooling would be needed to accommodate the new wafers. "The epitaxial growth and the etching process chemistry will be unique to III-Vs," says Droopad, "but all of the other process steps and the wafer handling will be the same as silicon."
- Monolithic integration of GaAs and silicon devices on the same chip could have long-reaching effects. It may also be possible to extend the technology into non-semiconductor materials. Droopad says Motorola is working on adding PZT (lead zirconium titanate) layers to the GaAs-on-Si stack, to be used for filters and waveguides. Another possibility is BST (barium strontium titanate), a ferroelectric material that could be used to make non-volatile memory circuits.
- If the technology can be extended to InP, it may be the ideal solution for reducing the costs of integrating and packaging optical components for networking applications.

Even if exotic new device types can't be realized, the potential cost savings for conventional III-V devices could still be significant. Several generations of wafer size transitions could be skipped. For RFICs, relative die costs could be reduced by 50% by moving from 6 to 8 inch wafers; the move to 12 inch wafers could reduce them by 75%. For optoelectronic devices, the leap would be even bigger, as they are commonly fabricated on 3 and even 2 inch wafers.

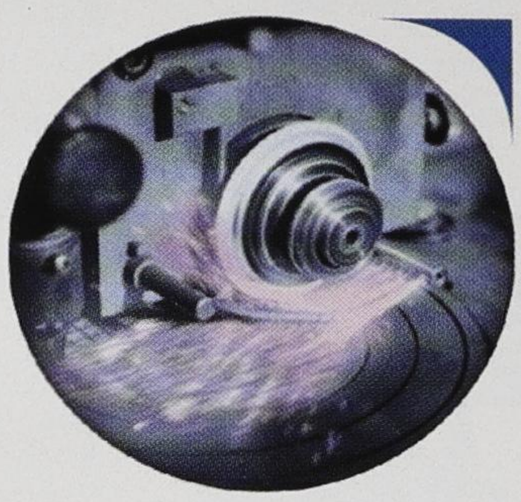
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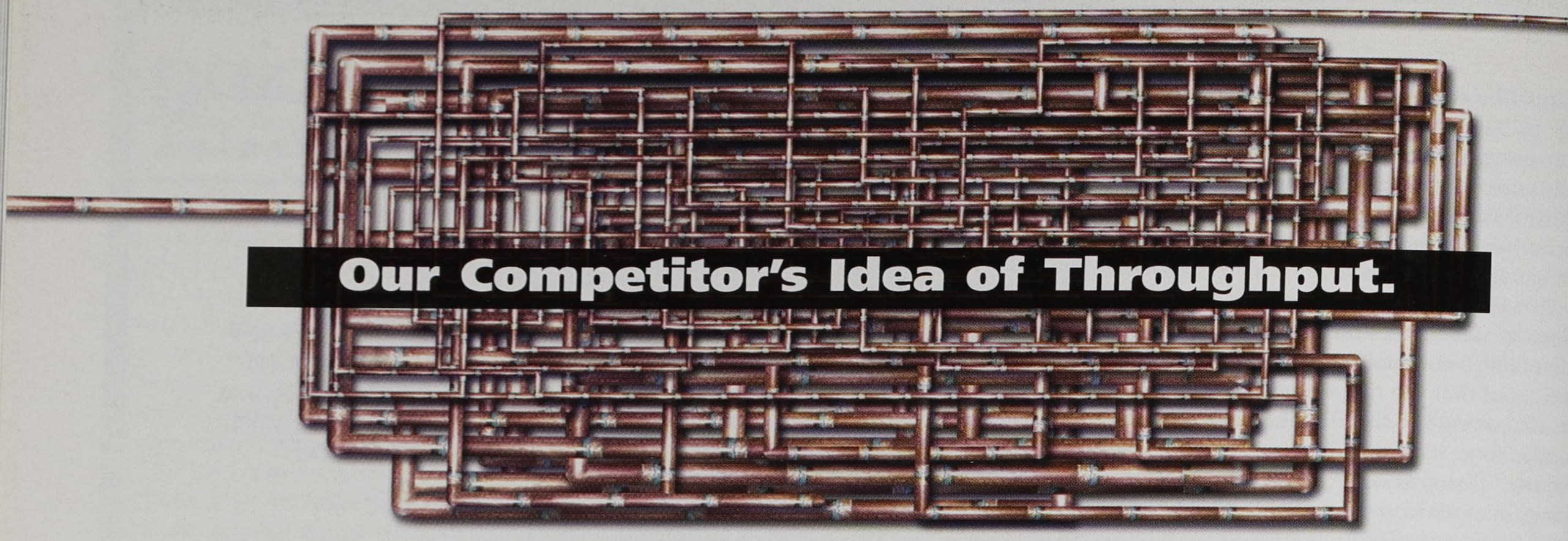
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InP HBT technology targets high-speed communications

InP HBT technology offers several advantages over other technologies for 40 Gbit/s circuits, writes **Marko Sokolich**.

The first transatlantic fiber-optic cable TAT-8 was pressed into service in December 1988 with the intention that it should meet the needs of data and voice communications across the Atlantic until the year 2000. Two years later the cable was filled to capacity. Since then data-transmission capacity across the Atlantic has increased by a factor of 1000. About half that increase (a factor of 35) came from the increase in speed of each channel's electronics, which went from transmission rates of 280 Mbit/s in 1988 to 10 Gbit/s today. The remaining boost in bandwidth was obtained by increasing both the number of fibers and the number of channels per fiber (using WDM). This prototypical long-haul line is just one example of the rapid deployment of the fiber-optic infrastructure. During the same period, over which communication capacity was growing by a factor of 1000, the speed of the fastest electronics (as measured by the maximum clock rates of benchmark circuits) increased by only a factor of three (figure 1).

In 1988 the required bit rate, 280 Mbit/s, was not a difficult target for any of the advanced technologies, including the fastest Si bipolar, GaAs MESFET and advanced CMOS processes. More exotic "laboratory" technologies, such as GaAs HEMT or the newly demonstrated SiGe and InP were certainly not needed. The rapid rate at which bandwidth has been consumed has led a traditionally conservative industry – telecommunications – to lead the way in some of the most exotic technologies. Currently, advanced processes in SiGe, CMOS, GaAs and InP are being evaluated for various OC192 (10 Gbit/s), OC768 (40 Gbit/s) and Gigabit Ethernet (1, 10, 100 Gbit/s) applications. Data-transmission requirements have now caught up with state-of-the-art electronics.

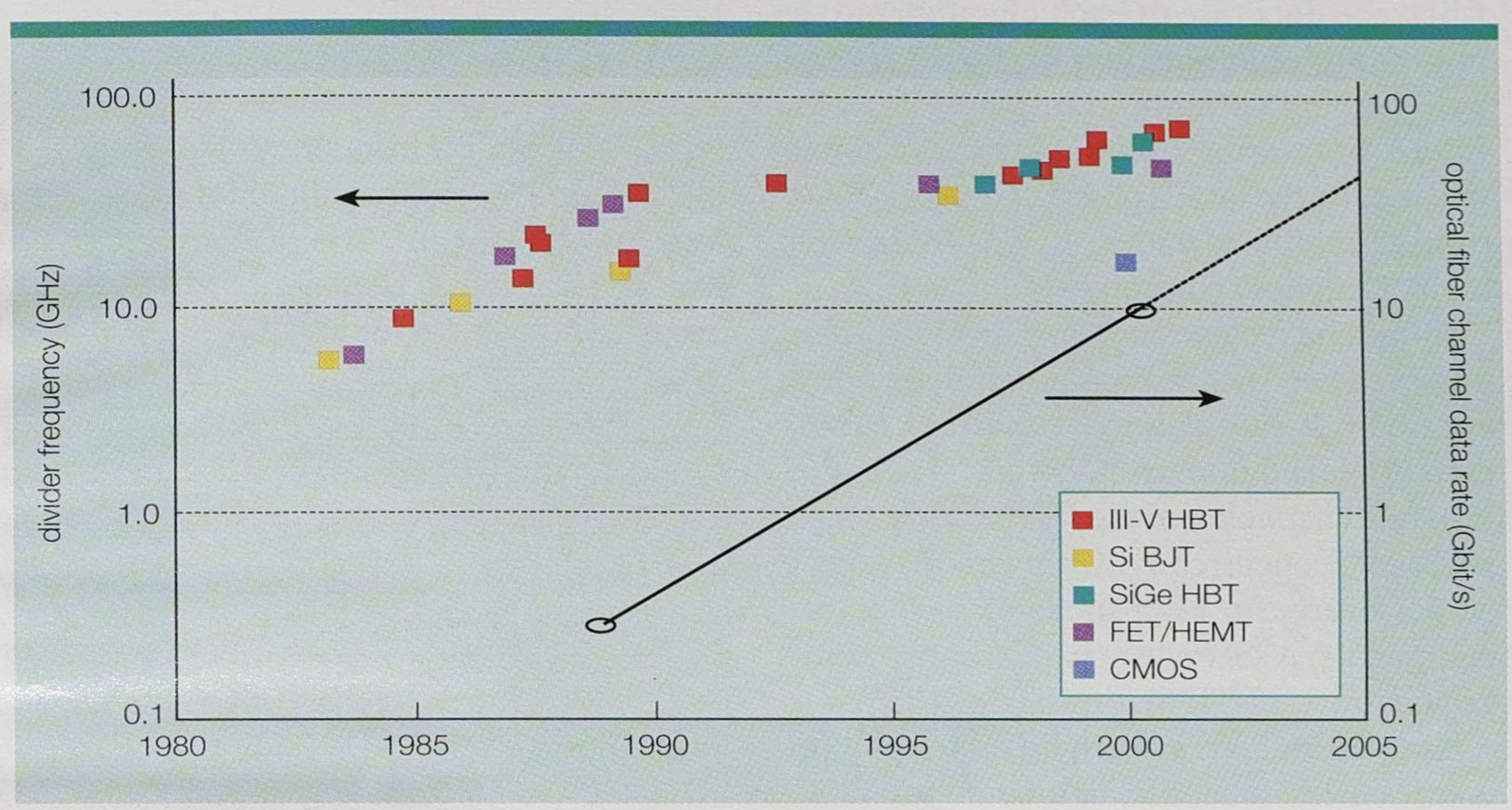


Fig. 1. Results for static frequency dividers from the 1980s to the present. The secondary axis shows the bit rate per channel for both the first-ever cable and the most recent.

The background of the technology

By posting some of the more impressive speed and power benchmark results, material systems lattice-matched to InP have become front-runners in the race to find a technology to support 40 Gbit/s transceivers. Recently, 300 GHz current-gain cut-off frequency (Dvorak *et al.*), 800 MHz maximum frequency of oscillation (Lee *et al.*), 330 GHz gain-bandwidth product (Baeyens *et al.*) and 70+ GHz clock rate (Sokolich *et al.*, Mathew *et al.*) in a static divider have been reported. Some of these results have been demonstrated in IC processes capable of more than 2000 transistor circuits with logic gates operating at a few milliwatts at a clock rate above 30 GHz. HRL Laboratories LLC has been developing InP circuits since that first transatlantic fiber-optic cable went into service. During the course of that pioneering work we have set many of the standards by which high-speed IC technologies are judged, and have demonstrated a number of circuits with both the speed and complexity required to satisfy the needs of high-data-rate communications.

Advantages of InP HBTs

InP HBTs have many advantages over other electron device technologies. As has been clear in the Si industry for many years, the fastest logic is made using bipolar devices in differential logic families because of the exponential turn-on, superior transconductance and better turn-on matching of bipolar transistors. Semiconductors lattice-matched to InP have a significantly lower turn-on than GaAs, and they have a higher cut-off frequency and lower power-delay product than either GaAs or SiGe. InP is lattice-matched to a wider variety of materials to optimize device behavior and is thus more flexible for "bandgap engineering" than either GaAs or SiGe (SiGe is not even lattice-matched to a Si substrate, which limits the thickness of layers that can be realized). The lower surface recombination of InGaAs translates to an ability to scale transistors to obtain both higher speed and lower power relative to GaAs. Recently our laboratory demonstrated 100 GHz f_t and 250 GHz f_{max} at 200 μA of current in a sub-micrometer transistor. In addition, InGaAs is an excellent material for fabricating photodiodes for both 1310 and 1550 nm receivers. The same process that is used to make 40 Gbit/s digital circuits can yield photodiodes with 20 GHz bandwidth with only minor process modification.

InP-based processes are particularly suitable for fiber-optic communication functions. Today's InP processes are capable of yielding fast ICs at moderate levels of complexity. In many data-processing applications, circuit speed can be traded for circuit complexity. Low-rate parallel processing can replace high-rate serial processing. This serial/parallel sub-

stitution is not possible in long-haul optical fiber communications, especially at the optoelectronic interface. The rapid growth in demand for data transmission requires that information travels along the fiber-optic channel at the maximum speed possible. While multiple channels in the fiber (DWDM) can increase the bandwidth, each channel still needs to be as fast as possible to obtain maximum use of the optical "pipe" while minimizing the hardware at the terminals. Until we run into a channel-spacing problem in the fiber, the data rate of each channel and the number of channels in a fiber will remain independent variables. For the foreseeable future, fiber-optic communication channels will require the fastest possible front-end electronics, combined with DWDM in extremely high throughput communication pipes.

Front-end receive and transmit electronics, however, need not be particularly complex. A single high-rate channel in a fiber can be demultiplexed into many (4, 16, 64) parallel low-rate channels and the information can be processed concurrently. The technology need is, therefore, for high speed and moderate complexity. A secondary system constraint is power but only if it limits the ability to realize the overall system by impacting the compactness, reliability or module assembly. InP fits extremely well into this high speed and moderately complex niche. System constraints will often put an upper limit on chip power (e.g. 5 W/chip maximum) based on the requirements of packing density and ambient temperature. Because high speed requires high power, the complexity of the circuit is often limited by a power constraint rather than by a fabrication yield constraint.

Demonstrated performance

A rule of thumb for transistor performance based on the experience of previous generations of optical circuits is to use a transistor that has a cut-off frequency four times higher than the data rate. For 40 Gbit/s this means an f_t of about 160 GHz. Selected circuits have been demonstrated at 40 Gbit/s with transistors of much lower performance through clever circuit design. In such designs margins often suffer and in the end the rough "4×" rule of thumb has held up. Single HBTs of InAlAs/InGaAs lattice-matched to an InP substrate can easily meet this requirement even for small, low-power devices. The unity current gain is not the only important device metric. The unity power gain cut-off, f_{max}, is equally important for bipolar logic circuits and is critical for distributed amplifiers. Typical results for both cut-off frequencies in our most recent generations of HBT technology are shown in figure 2. The figure shows second generation (G2) InP HBT technology, along with an enhanced version of the G2 process (G2+).

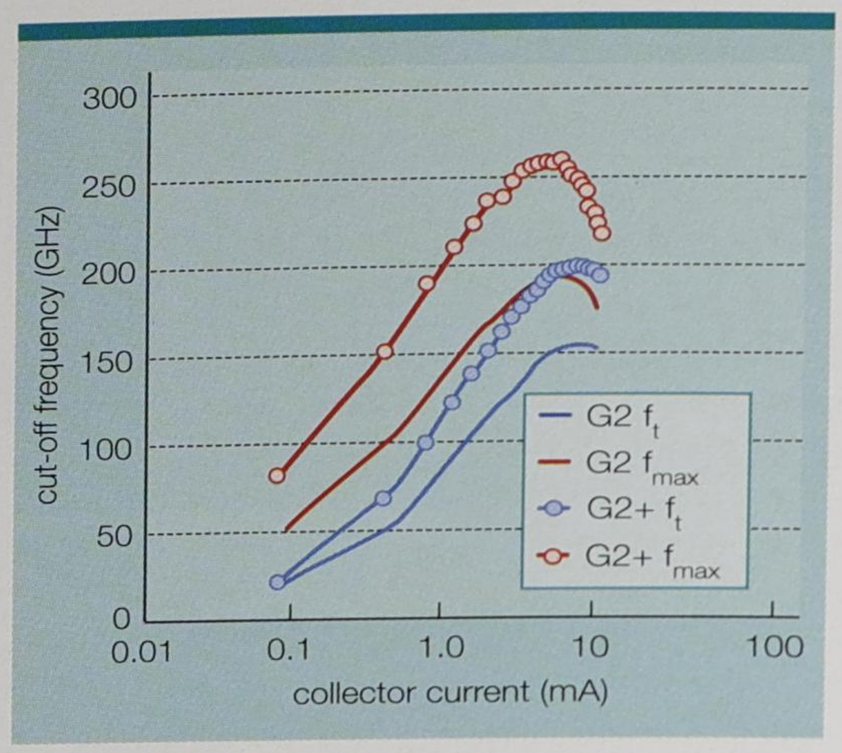


Fig. 2. The cut-off frequency of AlInAs/InGaAs-on-InP HBTs, with an emitter area measuring 1 × 3 μm². The scaling of InP-based HBTs is just beginning, with considerable room for improvement.

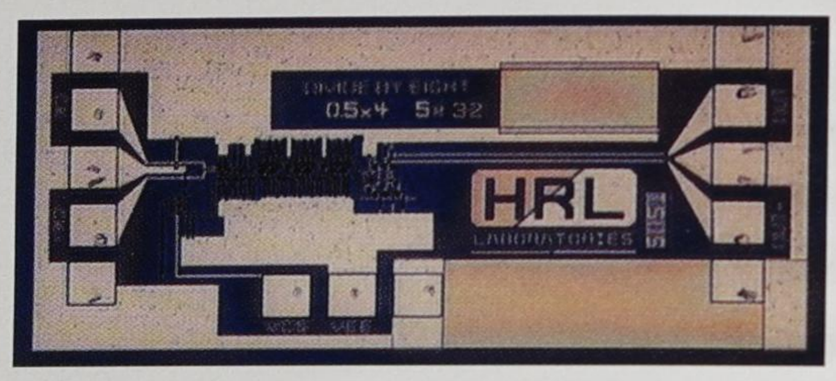


Fig. 3. Static frequency divider in AlInAs/InGaAs on InP, containing about 80 transistors in a 100 × 300 μm² area. This is designed for low power and has a 36 GHz clock rate. A similar circuit designed for high speed operates up to 73 GHz.

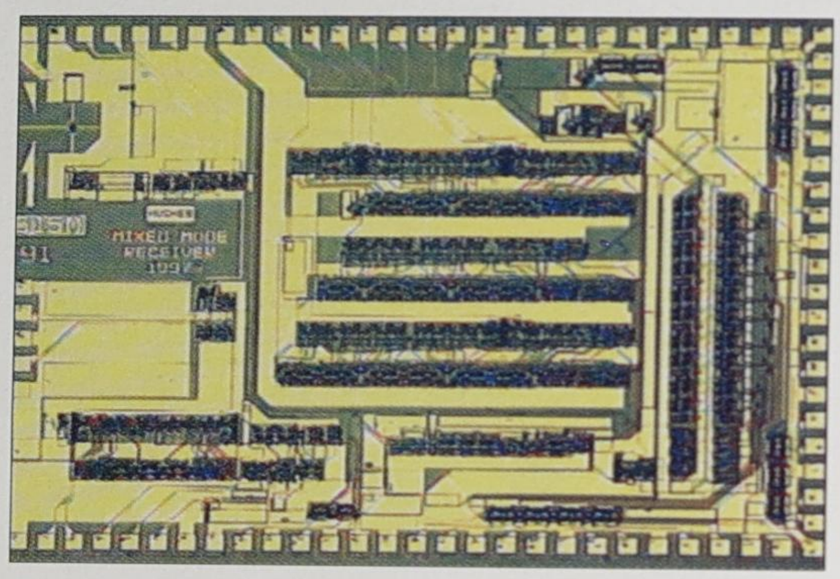


Fig. 4. Fully integrated four-channel, 7.5 Gbit/s optical receiver ASIC in AlInAs/InGaAs on InP. The circuit contains about 2100 transistors in an area 4.15 × 3.1 mm², and has four *pin* photodiodes integrated with the receiver electronics.

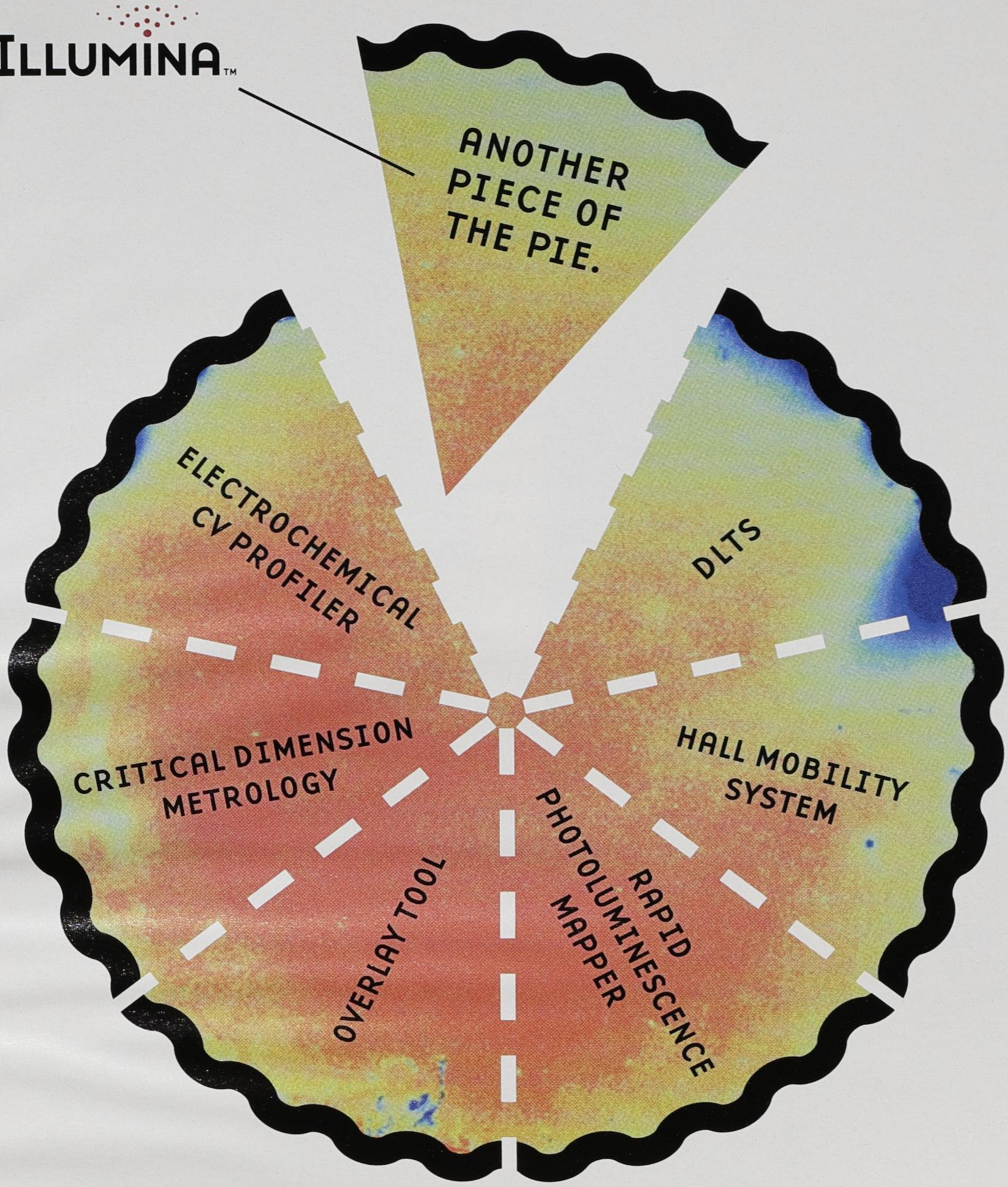
High-speed transistors are a necessary, but not sufficient, condition for circuit performance. Equally important are demonstrations of benchmark circuits that simulate the requirements of transceiver components. As performance approaches the limits of the technology, certain trade-offs can be made that enhance device performance at the expense of circuit performance. We have already mentioned the f_t/f_{max} trade-off, but more subtle trades in device design can increase both f_t and f_{max} but reduce circuit performance. By optimizing device design for circuit performance we have demonstrated a 72.8 GHz static 1/8 divider in AlInAs/GaAs technology. Power dissipation at this upper limit of device performance was 55 mW per flip-flop. By backing off on device current density, a high performance for much less power can be achieved. A similar circuit designed for low-power operation operated at 36 GHz with a 3.1 V supply but dissipated only 6.9 mW per flip-flop – half the speed at one-eighth of the power. A micrograph of the low power divider is shown in figure 3. The performance characteristics outlined here allow the realization of 4:1 MUX and 1:4 DMUX circuits dissipating only a few watts of power.

The final test of the technology is the ability to realize the actual circuit functions typical in an optical transceiver. The more functions that can be integrated, the lower the system cost. We have demonstrated a number of highly integrated circuits containing many of the components required for optical communications, as well as a number of specialized circuits with low levels of integration that can be used stand-alone or integrated with more complex functions.

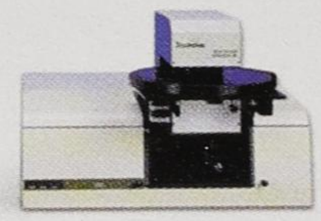
In 1998 we demonstrated a fully integrated 7.5 Gbit/s optical receiver ASIC that monolithically integrated all the components, including the photodiode, the amplifier stage, the clock and data recovery circuit, the demultiplexer and the word-synchronization logic (Yung *et al.*). It consumed 3 W of power and had 2100 transistors (figure 4). This demonstration was done in our mature first generation (G1) technology with 75 GHz f_t and 130 GHz f_{max}. Using this process in 1997, HRL also fabricated a 40 Gbit/s MUX (clocking at 20 GHz) in co-operation with Ericsson Microwave Systems and the Royal Institute of Technology in Sweden (Mokhtari *et al.*).

More recently we fabricated smaller footprint circuits with a wider design margin, also for 40 Gbit/s applications. Lucent

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designed and demonstrated 40 Gbit/s MUX and DMUX circuits as well as a 74 GHz distributed amplifier in our second-generation process (Mattia *et al.*). The 4:1 MUX operated to 50 Gbit/s. Recently we designed and demonstrated a photonic A/D circuit in the more advanced G2 process (Broekaert *et al.*). The circuit consists of an optical receiver, a comparator bank and a pipelined thermometer to binary decoder. Four optical receiver *pin* photodiodes are integrated with the HBT process (figure 5). The bandwidth of the photodiodes is 13 GHz. The 4-bit electronic flash ADC has 3.8 effective bits at low input frequency and 2.1 effective bits at Nyquist, all at 10 GHz sampling frequency. The circuit contains about 1600 transistors, operates from a 4V supply and dissipates 6 W of power. A 3-bit electronic flash ADC has 2.8 effective bits at low input frequency and 2.4 effective bits at Nyquist at 10 GHz sampling frequency; at 18 GHz sampling frequency it has 1.7 effective bits. The 3-bit ADC has about 960 transistors, operates from a 4 V supply and dissipates 4.25 W of power.

We have also demonstrated a 38 GHz MMIC VCO in AlInAs/InGaAs technology (Kurdoghlian *et al.*). The process and design were very robust for this type of application with extensive use of co-planar waveguide. The variation in oscillator frequency across a wafer was about 500 MHz. The designs were optimized for best phase noise and spurious characteristics. The monolithic VCO exhibited a tuning range of 850 MHz with an average output power of about +10 dBm. The phase noise performance of –82 dBc/Hz at 100 kHz offset and –108 dBc/Hz at 1 MHz offset and greater than 80% RF yield illustrates the suitability of the InP HBT technology for high-performance Ka-band and communication system applications.

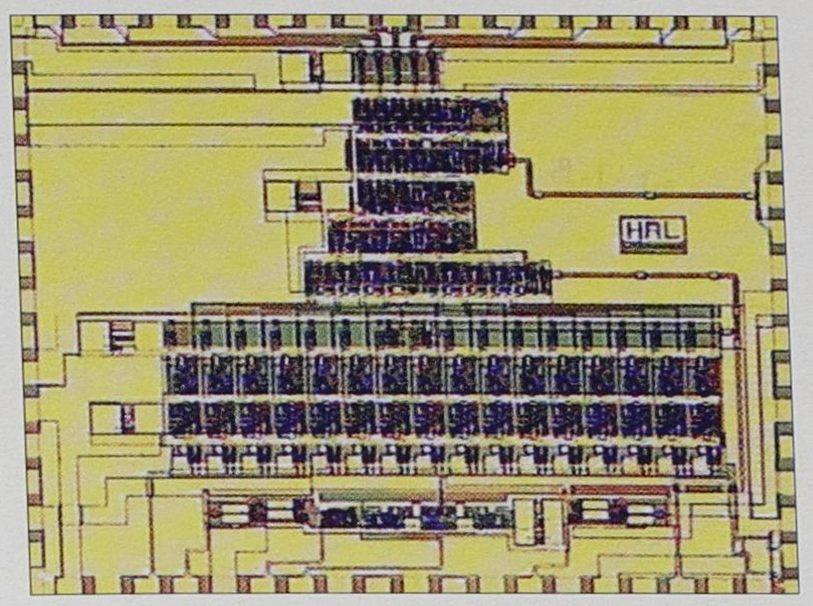


Fig. 5. Integrated photonic A/D with two clock inputs, two data inputs and about 1600 transistors in an area of 3.2 × 2.6 mm^2.

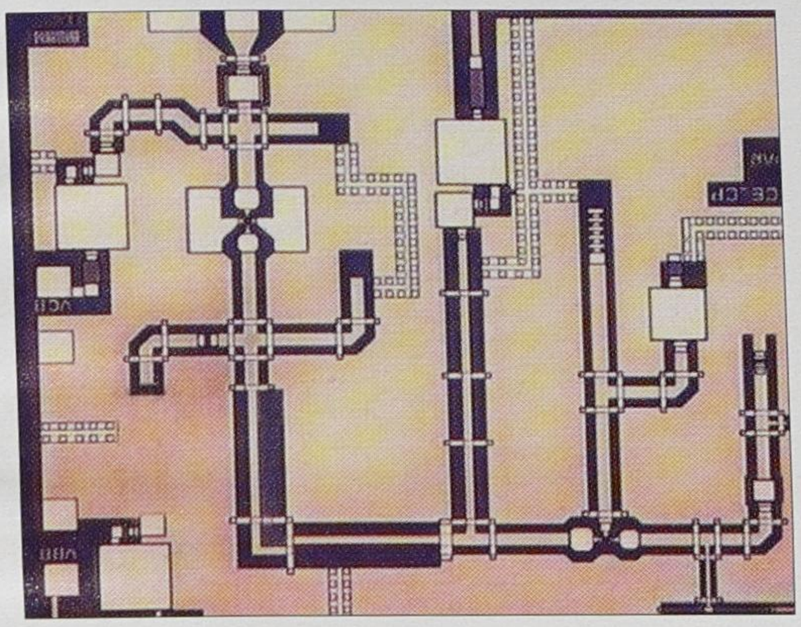


Fig. 6. An example of a 38 GHz MMIC VCO with excellent phase noise characteristics of –82 dBc/Hz at 100 kHz offset.

Technology competition

The technology battle lines for the next generation of optical networking chips are now being drawn. Industry heavyweights are finalizing their vision of the future of 40 Gbit/s transceivers. Some approaches combine InP and 10 Gbit/s CMOS with no SiGe, while others claim to have developed an all-SiGe solution. Many have published both SiGe and InP 40 Gbit/s developmental components. To our knowledge the only published fiber-optic long-haul demonstration system uses neither InP HBT nor SiGe circuits. Instead, small and medium-scale InP HEMTs were used for the critical components (Yoneyama *et al.*). A number of new players have announced their intention to compete in this market. Clearly the jury is still out on which semiconductor technology will carry the day.

The battle is intense and unsettled because, for the first time, the data rates required for optical fiber electronics are approaching the maximum limits of high-speed electronics. It may be years before a clear winner emerges. Nevertheless, InP HBT technology has significant advantages over the other contenders in terms of basic transistor physics, and circuits of the speed, complexity and design margin required for 40 Gbit/s transceivers have already been demonstrated. ●

Further reading

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Ge substrates, metamorphic HEMTs and hybrid integration

Raf Vandersmissen discusses the merits of different HEMT technologies for millimeter-wave devices and outlines IMEC's integration schemes for GaAs and Ge metamorphic HEMTs.

In the last decade the number of applications in the millimeter-wave range has grown tremendously. Critical to this growth has been the development of low-cost MMICs, or hybrid ICs, operating in the Q-band at 40 GHz and the W-band at 94 GHz. The latter frequency is suited to applications such as the high-resolution radars used in airport surveillance. Another emerging millimeter-wave market lies in the automotive industry for GPS navigation systems and collision-avoidance radars that work over a 100–200 m range at 77 GHz.

In the case of optical networks, the transistors must provide f_t and f_{max} values of more than four times the bit rate in order to achieve the required switching speeds and system margins. Thus, current optical systems operating at 10 Gbit/s require GaAs HEMT or HBT technology with a cut-off frequency (f_t) of at least 40 GHz. Moreover, in these optical networks there is a shift away from bare dies towards modules containing a photodetector and TIA on the receiver side, or a laser and modulator on the transmitter side. Such integration can be achieved either in InP technology or by using hybrid schemes such as the multichip module approach developed at IMEC to allow the cost-effective integration of different types of components.

In this article we will compare millimeter-wave MMICs based on InP with metamorphic HEMTs (MHEMTs) employing GaAs and germanium substrates, and we will outline IMEC's recently introduced hybrid integration scheme that would enable active devices, such as MHEMTs, to be composited with passive components.

Substrate economics

MHEMTs grown on GaAs substrates have recently demonstrated a performance level close to that obtained from HEMTs grown lattice-matched to InP substrates. Improvements in backside processing and the availability of 6 inch GaAs substrates will probably induce metamorphic growth as an attractive alternative to InP HEMTs (Van der Zanden *et al.*).



Fig. 1. A schematic diagram that shows a typical double delta-doped metamorphic InAlAs/InGaAs HEMT structure on a strain-relaxed InAlAs graded buffer layer.

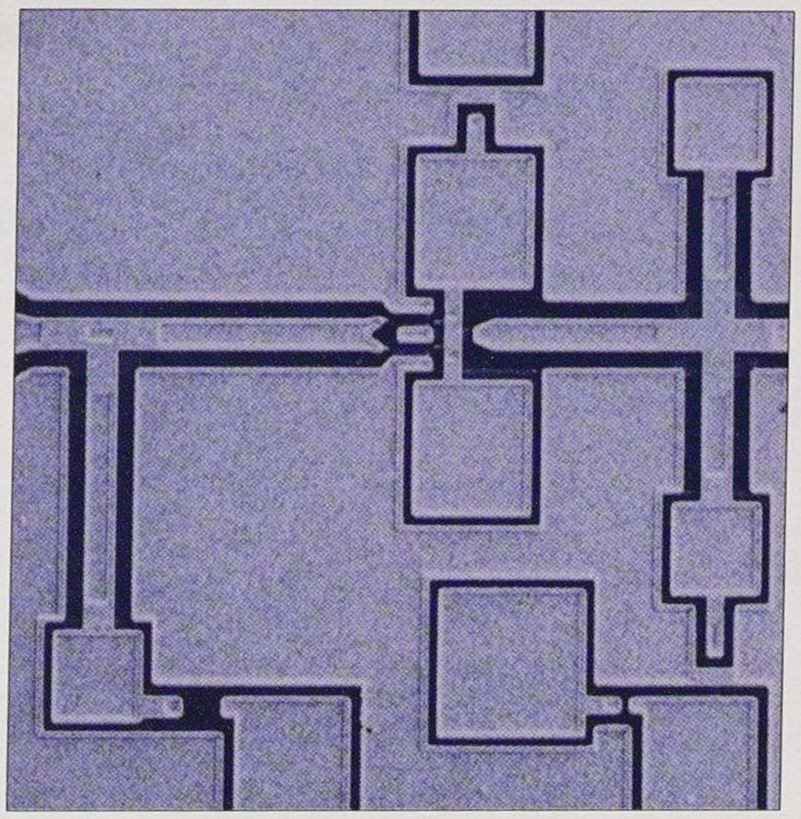


Fig. 2. An SEM image obtained from a 600 × 700 μm² one-stage W-band metamorphic HEMT amplifier circuit.

Further to this, the economic advantages of alternative substrates, such as germanium, which is around 50% less expensive than GaAs, can extend the price advantage even further compared with InP HEMTs. The use of germanium also offers a way to avoid prices for materials spiraling due to the reputed gallium shortage. Germanium is available in diameters of up to 8 inches and has a lower environmental impact than GaAs.

The availability of large-area germanium wafers also lends itself to a hybrid integration approach for the low-cost packaging of MHEMT devices. IMEC's multichip module-dielectric, or MCM-D, technique employs a multilayered interconnection technology consisting of a glass substrate with alternating dielectric and metal layers on top.

A spin-on low-k dielectric polymer layer is used in the integration scheme to attach the components. In this hybrid substrate, microwave passive components are embedded together with thinned active die, such as MHEMTs in a low-cost process described later in this article.

MHEMT device geometry

A typical MBE-grown metamorphic HEMT on a GaAs substrate is shown in figure 1. The 4% lattice mismatch between a GaAs substrate and the InGaAs channel can be overcome by using a GaAs nucleation layer and a 1 μm InAlAs metamorphic buffer, which grades from AlAs to $In_{0.57}Al_{0.43}As$. A 100 nm reverse grade towards $In_{0.52}Al_{0.48}As$ is then added to improve further the crystalline quality of the subsequent top layers. The heterostructure consists of a buffer, a channel layer in between two spacers (which ensures donor-electron separation), two silicon delta-doped InAlAs spacers, and a Schottky layer and cap (Behet *et al.*).

At room temperature, this GaAs-based double delta-doped heterostructure has a low-field mobility of 6.85×10^3 cm²/Vs, an electron density of 5.7×10^{12} cm^{-2} and a square resistance of 159 Ω. Similar results to these have been measured from devices grown on germanium substrates.

IMEC's MHEMTs are fabricated with the same process used for the production of InP HEMTs. This process consists of four ultraviolet-lithography steps (mesa isolation,

DC and RF performance of metamorphic HEMTs

parameter	*units*	*GaAs*	*Ge*	*InP*
transconductance (Gm)	mS/mm	670	720	900
maximum drain-source current (I_{ds})	mA/mm	660	650	450
cut-off frequency (f_t)	GHz	90	45	102
maximum oscillation frequency (f_{max})	GHz	130	68	154

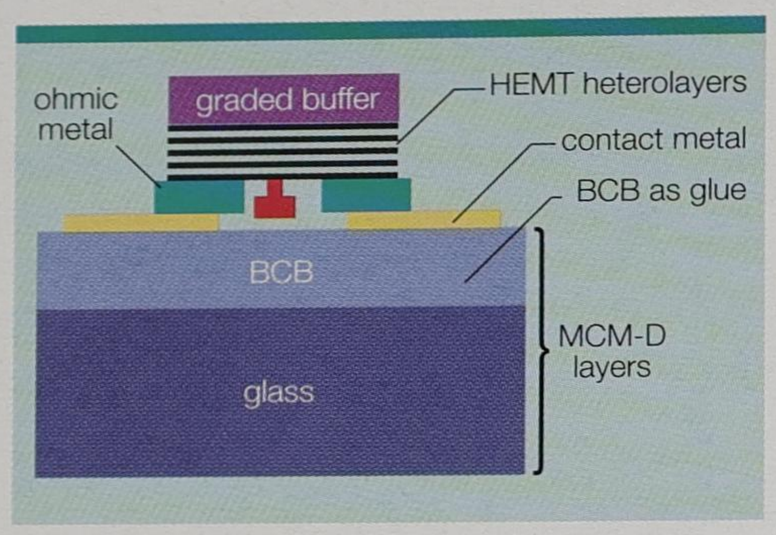


Fig. 3. IMEC's multichip module (MCM) hybrid integration scheme. The substrate is removed after the attachment of a MHEMT device to a glass support with a thin (~ 5 μm) layer of high-temperature polymer film called BCB. This approach provides a low-cost platform that connects the MHEMT to passive components with copper interconnects.

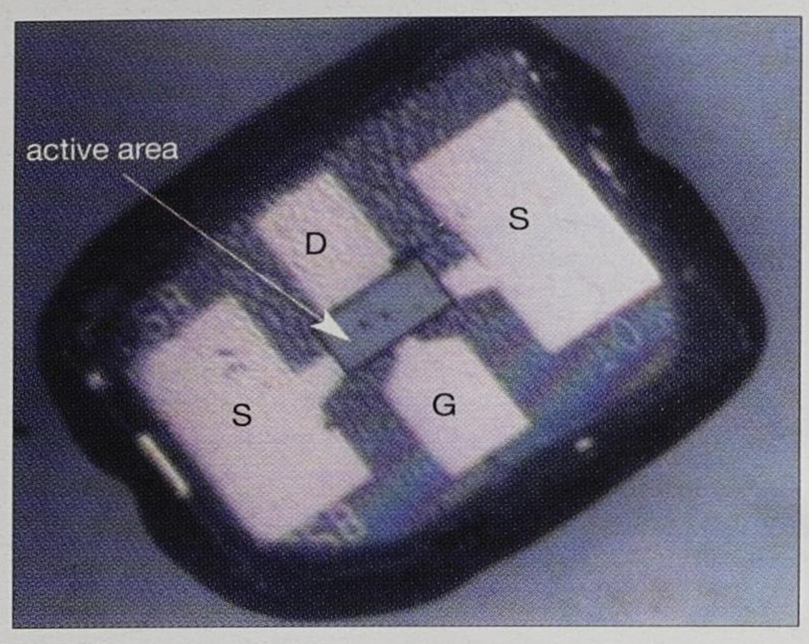


Fig. 4. Optical micrograph obtained from a thin-film Ge MHEMT after substrate removal showing active area, source, drain and gate regions. While offering lower RF performance than InP, removal of the lossy substrate recovers much of the RF performance of Ge MHEMTs.

ohmic metal, contact metal and passivation) and one e-beam lithography step to define the T-shaped gate.

InP HEMTs vs metamorphic HEMTs

The table above compares the DC and RF results of MHEMT devices (0.2 μm gate length) grown on GaAs and germanium substrates with those from lattice-matched HEMTs on InP. The results are obtained on devices processed with a mask set that is not optimized for RF applications (i.e. they exhibit large pad capacitance). Only extrinsic values are given to make a direct comparison between different layer structures.

The germanium MHEMT devices show DC performance parameters that are comparable to the GaAs circuits, and are even comparable to InP HEMTs. However, a large discrepancy is revealed in the much lower RF performance (f_t = 45 GHz and f_{max} = 68 GHz), which is due to the limited resistivity of the germanium substrate. Devices grown on GaAs and InP achieve much higher RF performance because both types of substrate are semi-insulating.

Several co-planar high-gain MMIC amplifiers have been fabricated using MHEMT epilayer structures. Two narrowband high-gain circuits, originally designed to be processed using InP-based circuits, were realized in co-planar waveguide technology.

At 40.5 GHz, the gain reaches a maximum of 17.5 dB and is complemented by an excellent input and output matching of –19 and –27 dB respectively. The corresponding values for the original InP HEMT include a maximum gain of 17 dB and input and output matching of –15 and –20 dB respectively.

However, to compete with InP, the GaAs MHEMT must be able to demonstrate its abilities at frequencies of more than 80 GHz (W-band). Figure 2 shows an SEM photograph of a co-planar W-band amplifier. The layout comprises transmission lines, MIM capacitors and resistors. The original InP circuit demonstrates a gain of 12.4 dB at 94 GHz, whereas the GaAs MMIC yields a maximum gain of 10.5 dB at 84 GHz.

The shift in frequency can be attributed to a lower output conductance due to the high bandgap material (InAlAs) in the metamorphic buffer. An adjustment of the matching network in the GaAs MMIC is required to obtain the maximum gain at 94 GHz.

Hybrid integration of Ge MHEMTs

In the case of germanium MHEMTs, the conductive nature of the substrate makes such devices unsuitable for millimeter-wave applications. The substrate, having served its purpose as a platform for growth, is removed and the MHEMT device is transferred to a hybrid substrate for further integration (figure 3).

Prior to the removal of the substrate, the wafer is diced and a chip containing one MHEMT transistor mounted on a 6 inch glass substrate (with the active side facing the glass) in a 3 μm thick spin-coated polymer layer of benzocyclobutene (BCB). As a low-k dielectric polymer with a high glass transition temperature (of up to 350 °C), BCB is very suitable for RF integration and microelectronics. This polymer film protects the front face of the chip.

The germanium substrate is removed by reactive ion etching in a mixture of CF_4 and O_2. The GaAs buffer is then selectively etched, and the buffer layer is removed from regions surrounding the active area using lithography and a non-selective etch of phosphoric acid. This step reveals the metal contacts of the 2 μm thick devices, which are contacted by probe needles from the back-side. The latter process, which contacts the metal directly, is very straightforward and designed to realize amplifier circuits in the MCM-D technology.

Moreover, to circumvent planarization problems in subsequent MCM-D processing steps, the total thickness of the devices is kept below 5 μm. This requirement is easily maintained due to the removal of the substrate.

Performance of germanium MHEMTs

Figure 4 shows an optical micrograph of a thin-film MHEMT following substrate removal on a glass MCM-D platform. The image is obtained from the back-side to reveal the contact metal and active area. Measurements of hybrid glass germanium MHEMTs reveals only a slightly reduced DC performance – the drain-to-source current (I_{ds}) still reaches a value of just over 600 mA/mm. However, the maximum transconductance (g_m) has dropped to 675 mS/mm. This degradation is attributed to heat generated in the thin active area of the devices.

On the other hand, the RF performance recovers considerably. With an f_t of 70 GHz and an f_{max} equal to 120 GHz, the germanium device is approaching the performance of GaAs MHEMTs. These extrinsic results confirm that the conductivity of the substrate is responsible for most of the degraded performance in germanium MHEMTs, and that this problem can be largely overcome by removing the substrate. >>

Other technologies and the future

The fastest transistor ever built is an InP HEMT, and for almost a decade such devices have offered an optimum combination of high-gain, low-noise and high-speed performance for three-terminal devices. On the other hand, GaAs MHEMT circuits have similar layer structures, with DC and RF performances approaching 90% of those for InP devices, and they are much cheaper. This makes metamorphic MMICs, especially in the W-band, strong competition for InP MMICs in cost-driven mass-market applications.

At IMEC we have also demonstrated the potential of reducing costs even more through the hybrid integration of MHEMTs on germanium substrates. After substrate removal and hybrid integration, such devices exhibit RF results comparable to those of their GaAs MHEMT counterparts. Hybrid integration is often the only feasible solution because of the heterogeneity of components and the complexity of certain RF systems.

MHEMTs grown on GaAs substrates have recently demonstrated performance close to that of HEMTs grown lattice-matched to InP substrates.

Compared with hybrid integration using flip-chip with bumps, IMEC's approach results in smaller parasitic capacitance and allows for stacked three-dimensional circuits. MCM-D integration is well suited to RF applications beyond 50 GHz due to its high definition and the possibility of integrating resistive and capacitive layers. However, while the minimal thickness is advantageous, it limits applications to low-power circuits.

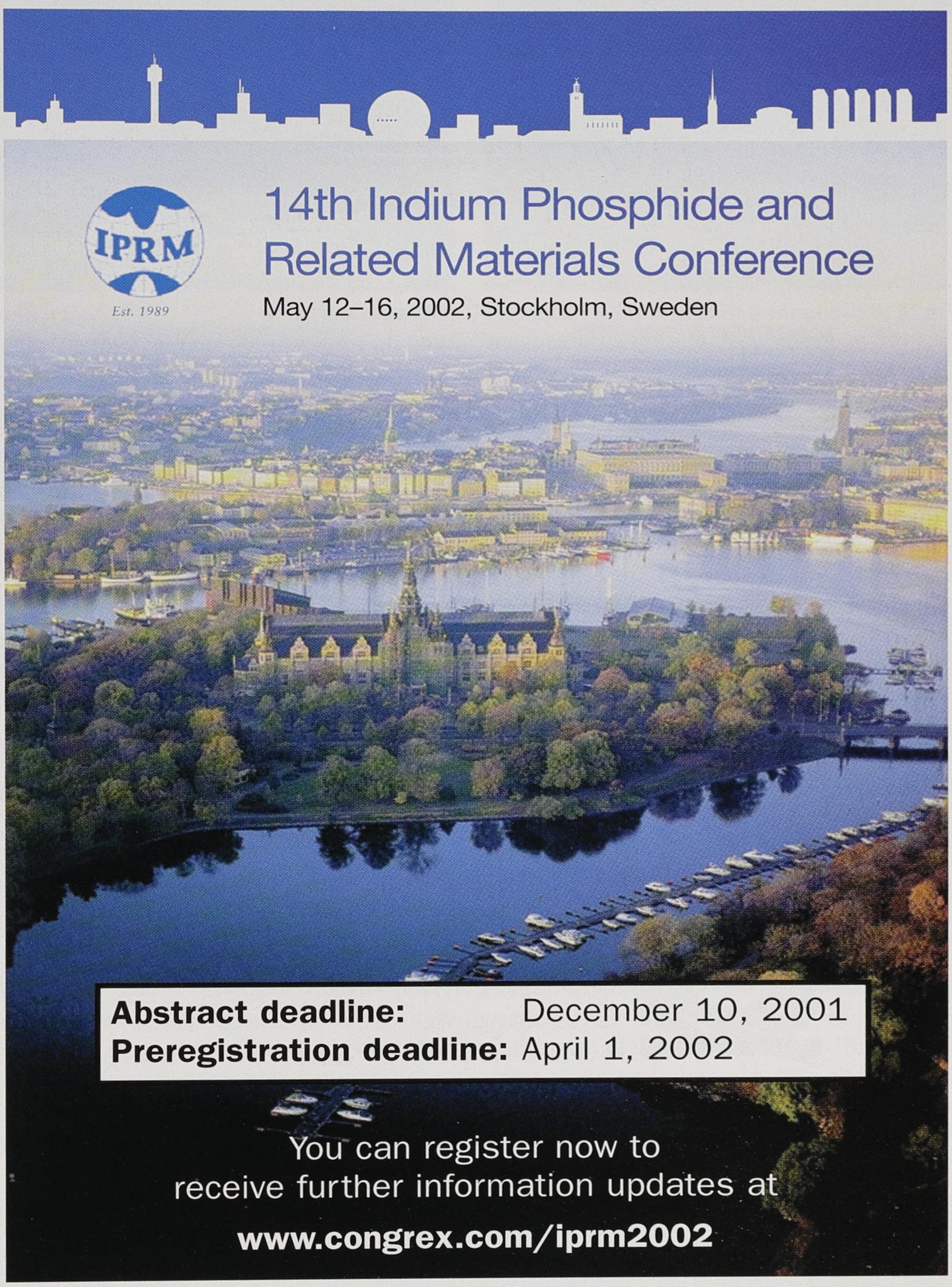
The MCM-D approach will also be feasible for future fiber-optic components, particularly as the evolution to higher levels of integration will lead to transponder modules, such as lasers, MUX and optical amplifier functions on a common glass substrate (Lebby). However, InP will probably be the material of choice for the development of very-high-bit-rate components in optical networks at 40 Gbit/s and above. This material offers the potential for f_t values in excess of 200 GHz and the ability to integrate a sufficient number of transistors along with lasers, detectors and modulators (Deyhimy).

However, because the hybrid integration approach developed at IMEC is a generic one, work in the future will focus on integrating thin-film GaN HEMTs on AlN substrates for power applications. ●

Further reading

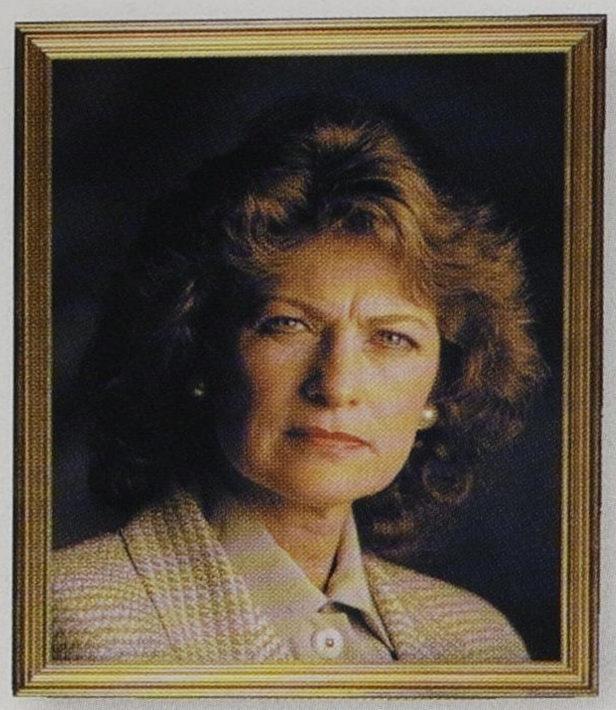
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This feature is taken from an article presented at the Compound Semiconductor Manufacturing Expo (CS-MAX) in Boston, MA on 9–11 July, 2001.





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New methods eliminate etch defects in GaAs IC production

Conexant has had to work hard to identify and eliminate various etch-related defects resulting from a ramp in IC production at its GaAs fab. **Jiang Wang**, **Sam Mony** and **Nercy Ebrahimi** report.

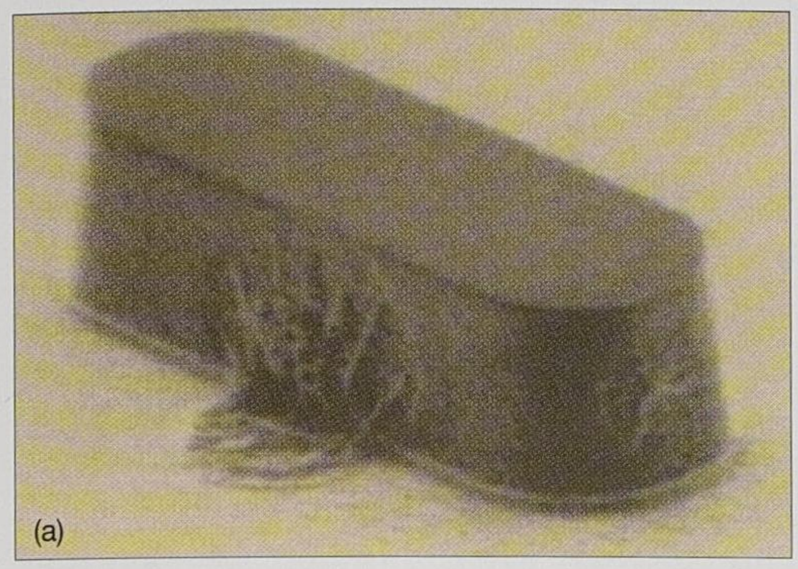


Fig. 1. SEM images of the InGaAs emitter mesa of a GaAs HBT. (a) The structure after the wet etch but before the dry etch. Part of the emitter mesa photoresist has peeled off and flowed onto the substrate. (b) A protrusion at the edge of the emitter mesa.

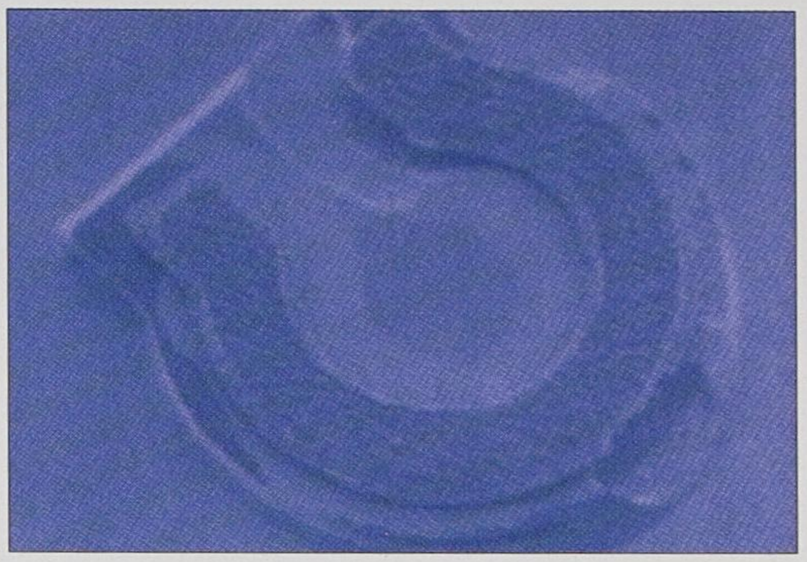


Fig. 2. An SEM image of a mouse-bite at a base-pedestal edge. This is a result of poor adhesion at the resist film edges.

The huge increase in demand for GaAs power amplifiers in mobile communications has led Conexant to expand its efforts to increase its GaAs HBT capacity, achieve high production yields and reduce manufacturing costs. In the last two years Conexant has undertaken a steep production ramp to increase capacity. However, intermittent process defects have emerged that were not obvious at low production volumes, and these defects have lowered yields.

This article discusses three process defects that occurred during the photo/etch stages. The defects were classified as emitter mesa protrusions, base-pedestal mouse-bites and collector-contact gross undercut. Conexant has eliminated these defects, which were related to process conditions during higher production volumes, by implementing a resist film post-develop bake and an oxygen plasma cleaning step after the emitter mesa resist strip. This resist film post-develop bake increases resist film adhesion, and reduces wet etch undercut and resist film dissolution. In addition, a post-bake is an essential step before wet etching, even if an adhesion promoter such as HMDS is used.

Emitter mesa protrusions

Figure 1 shows SEM images of the emitter mesa region. The mesa has a two-layer structure with an emitter metal on the top, and is formed in two etch processes using the same resist film. The first etch is the InGaAs layer wet etch, which is followed by the second anisotropic plasma dry etch. This etches the GaAs layer and results in a vertical profile.

The defects were found to be attached to the bottom layer, and protrude out of the emitter mesa. These emitter mesa protrusion defects occurred intermittently in the production line, and were always associated with the bottom layer formed by the plasma etch.

Figure 1(a) shows an SEM of the structure after the InGaAs emitter mesa wet-etch stage and before the dry etch, which shows that part of the emitter mesa photoresist peels and flows onto the substrate. This is a result of resist dissolution in the wet-etch solution. This fallen resist blocks the dry etch, forming the emitter mesa protrusions seen in figure 1(b). The photoresist flow occurred only when the wet etch was almost complete. This explains why emitter mesa protrusions are always connected to layers formed in the dry etch but never to layers formed in the wet etch.

As a remedy, a resist post-develop bake was introduced into the production process. A post-bake at 115 °C for 1 min hardens the resist film, which completely removes resist dissolution and the protrusion defects. No statistical difference was observed for the key electrical parametric data and emitter mesa critical dimension between processes with and without post-bake. This improvement could have profound effects on the yield and reliability, particularly in view of the small spacing between the emitter mesa and the base-contact metal, and a better geometric integrity of the AlGaAs ledge.

Base-pedestal mouse-bites

The mouse-bite defects occurred during the wet-etch process that forms a base-pedestal structure 500 nm deep. Figure 2 shows the base pedestal with a mouse-bite, which leads to poor geometric integrity after the etch. Base-pedestal mouse-bites always begin at the pedestal edges, as they are caused by poor adhesion at the resist film edges. This enables acid to penetrate beneath the resist film, leading to an etching of the base pedestal.

SEM studies showed that poor resist adhesion is caused largely by the resist residues from the previous emitter mesa resist strip. The combined wet and dry etch processes cause the resist to polymerize, making it difficult to strip.

Oxygen plasma ashes with different ash rates were tested to remove photoresist residues and enhance adhesion. The AlGaAs ledge remaining after the emitter mesa etch is very sensitive, and critical to the reliability of the HBT since it is unprotected at this step (Canfield). For this reason the effects of different ashes on the device were evaluated through high-temperature operation life tests. Based on parametric data, the operation life tests and statistical analysis, we implemented an oxygen plasma ash with an ash rate of

120 nm/min, and a base-pedestal photoresist post-bake at 120 °C for 1 min. The mild oxidation of the AlGaAs layer by the ash improved the adhesion/reaction of HMDS monolayer to the substrate. The post-bake reduces the undercut, as it restores the adhesion weakened by developer penetration along the resist-substrate interface (Dammel). The post-bake alone can reduce mouse-bites, but plasma ash and post-bake can eliminate base-pedestal mouse-bites completely.

Collector-contact undercut

The collector contacts are visible as rectangular windows in the optical micrograph in figure 3. The windows are opened by wet etching to depths ranging from 580 to 880 nm. The etch is conducted at 1.5 °C with a high etch rate, and usually causes a large contact undercut. All the edges of the collector windows close to the base-metal pad are rough, while those far from it are smooth with good geometric definition.

The undercut has three unique features: it happens on the edges closer to the big base metal pads, it never occurs where the base-metal pad is small or no base metal exists, and the defect shows up intermittently. The asymmetric appearance suggests that this undercut must form under the influence of the base-metal pads, and that it is not caused by the wet etch as this is isotropic in nature.

Figure 4 is a schematic of the collector-contact layer showing the structure of the base-metal pad, SiN film, resist film and two collector-contact openings before the etch process. The resist film experiences a shear force (F) that results from the shrinkage of the film toward the base metal. This reduces resist adhesion at edges close to the base-metal pad. The resist film covering the gold metal pad shrinks more due to the weak interactions of the HMDS monolayer with the gold surfaces.

The degree of resist film dehydration and the higher tension at the gold surface could be two other factors causing resist shrinkage. The resist film shrinks more if dehydration is incomplete, and shrinks to surfaces with higher surface tension (Somorjai).

Post-develop baking

To minimize collector-contact undercut a post-develop, 1 min bake at 120 °C was implemented. The post-bake completely eliminated the gross asymmetric undercut, and reduced the normal undercut formed during isotropic wet etching. Process steps such as collector-metal lift-off were also evaluated and no difference was found between processes with and without the post-bake.

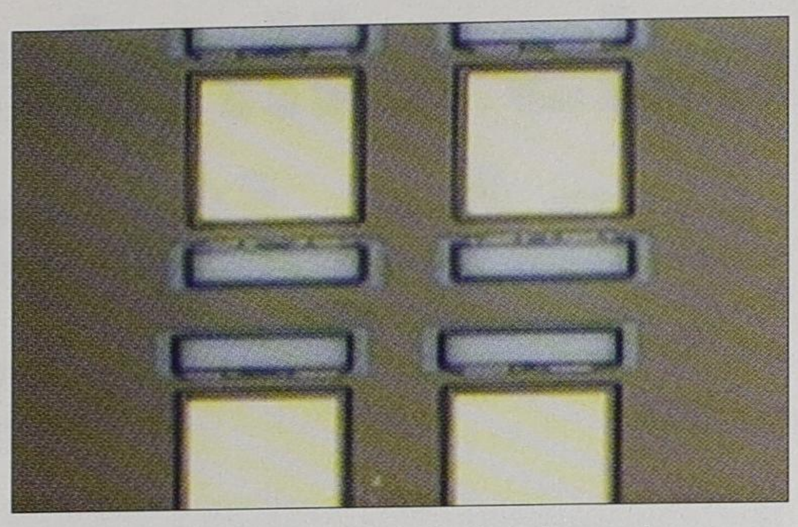


Fig. 3. Collector contacts (rectangular boxes) showing rough edges close to the base-metal pad. These have been caused by undercutting and relate to the shrinkage of the resist film towards the base metal.

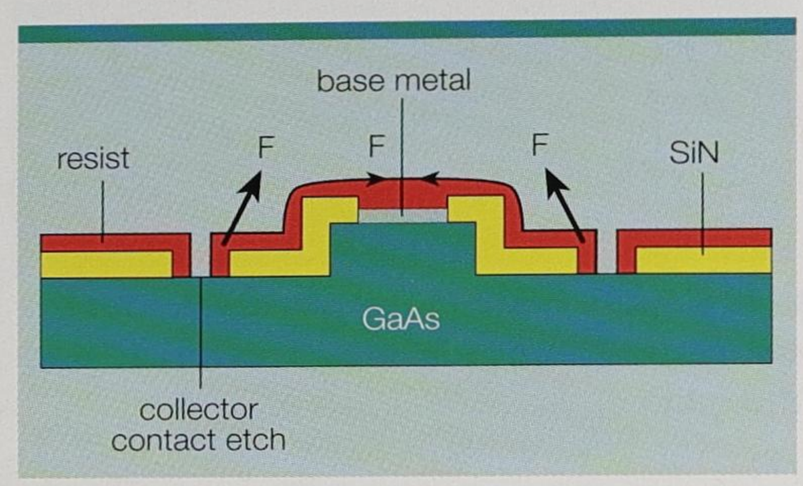


Fig. 4. Schematic showing the pre-etch collector contact, consisting of base-metal pad, SiN film, resist film and two collector-contact openings. The film experiences shear forces (F) which reduce the resist adhesion at edges close the metal pad.

The post-bake process has several advantages. At such high post-bake temperatures, reflow occurs on the top layer of the film. However, at this temperature the resist is still stable and the critical dimension of the collector opening does not change.

A mild resist reflow and profile change is not sensitive to the wet etch since it is highly selective. The bake removes most of the absorbed water and solvent, and produces a melting effect. This can lead to less shrinkage due to the maximization of the contact surface between the resist and the substrate.

Also the high bake temperature may induce interdiffusion between a silylated surface primer and the overlying resist that improves adhesion (Parisi *et al.*). Other groups have noted that the melting of the resin in the resist can act as an adhesive to seal the interface between the resist and substrate, and reduce edge lifting during wet etching (Andrasi).

For the emitter-mesa, base-pedestal and collector-contact layers, the adhesion promoter HMDS is used to treat the substrate before the photoresist coat, and at least one monolayer of HMDS is formed on the substrate. HMDS is less effective at promoting resist adhesion during GaAs processing than it is in Si processing, because GaAs processing leads to surfaces with fewer surface hydroxyl (OH) groups such as SiN. This is especially true of inert gold surfaces. Due to the deficiency of OH groups HMDS cannot form sufficient covalent bonds, so HMDS adhesion to the substrate is weak (Martin). As a result the adhesion of resist film to the substrate will be weak, even though the adhesion between the HMDS layer and resist film is strong.

Conclusions

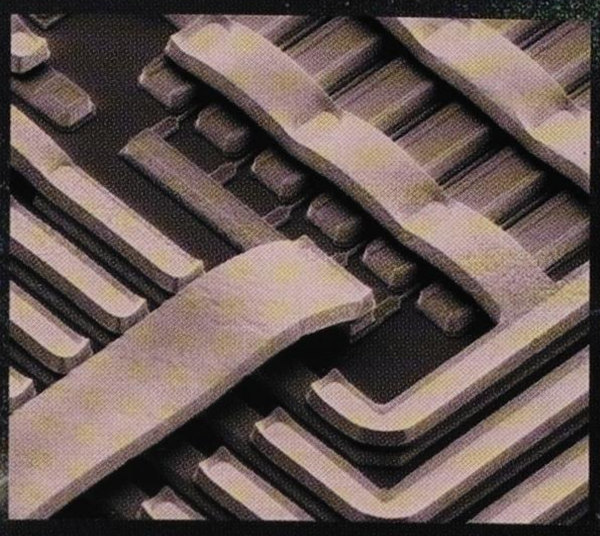
Emitter mesa protrusions, base-pedestal mouse-bites and collector-contact gross undercut defects have been observed intermittently under high-volume production conditions. These defects are caused by poor resist adhesion and resist dissolution during the wet etch. However, a resist post-bake in the resist develop process can completely remove emitter mesa protrusions and collector-contact undercut defects. Also the post-bake and a plasma clean eliminate the pedestal mouse-bite defect. The bake time and temperature were optimized to ensure that there was no drift in the key electrical parameters and critical dimensions. In addition, a resist post-bake and surface clean enhance the adhesion of the photoresist. The resist post-bake is an essential addition to wet etching if gross undercut and defects caused by resist dissolution are to be removed.

Further reading

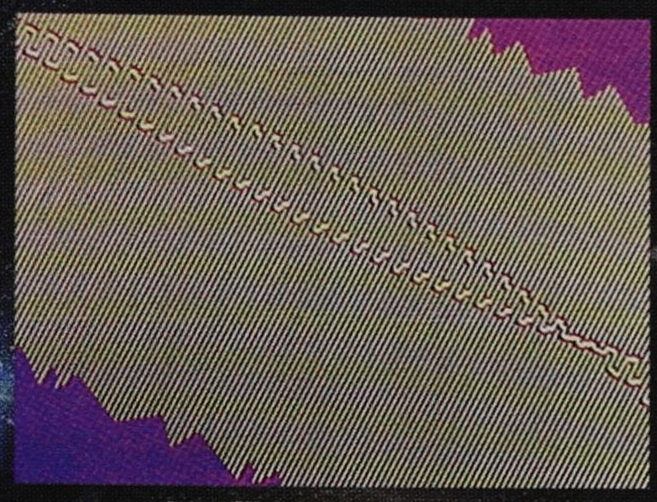
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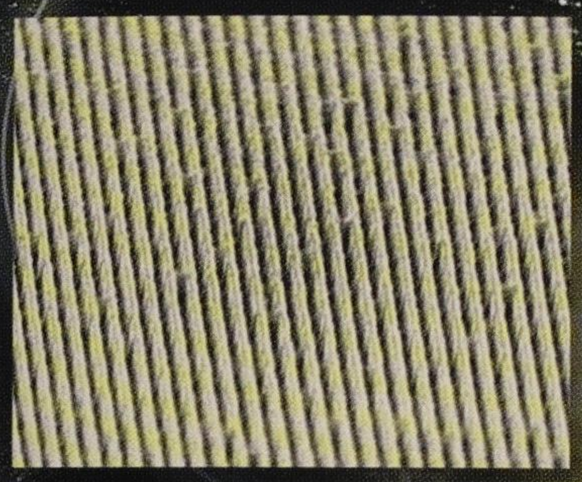


Air bridge on high speed GaAs device, courtesy of M/A-COM

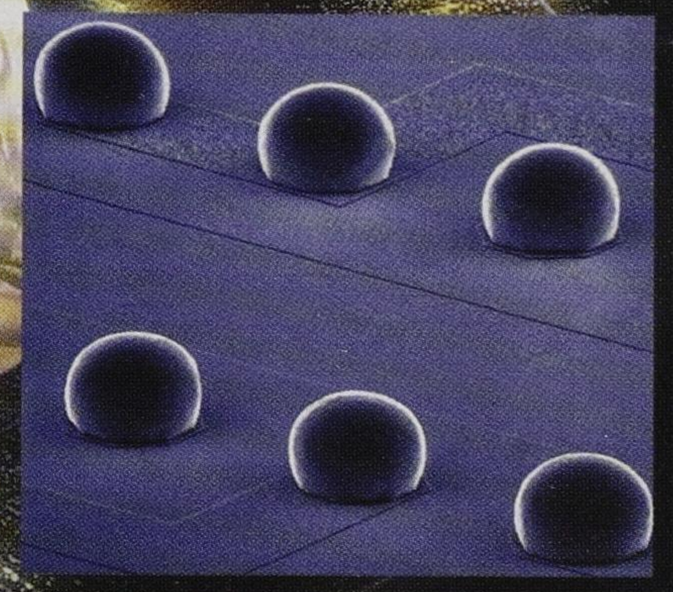


Saw filter, courtesy of AME Space

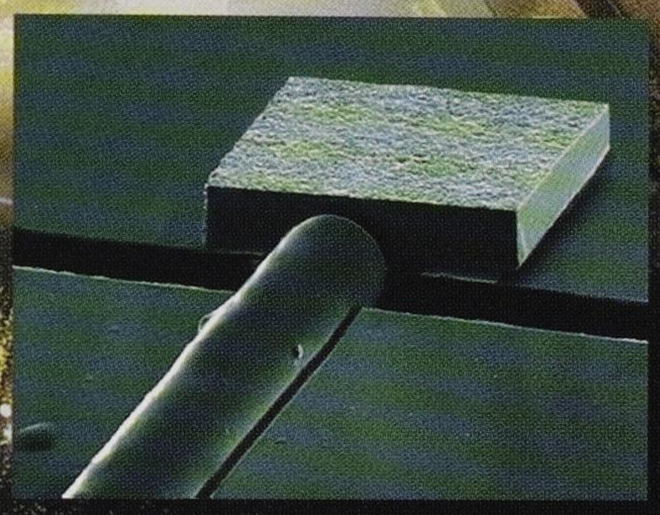




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Reversible wafer bonding and backside processing of GaAs

Fully automated processes such as reversible wafer bonding have the potential to become key enabling technologies for the compound semiconductor industry, claim **Paul Lindner, Christian Schaefer, Josh Palensky** and **Manfred Reiche**.

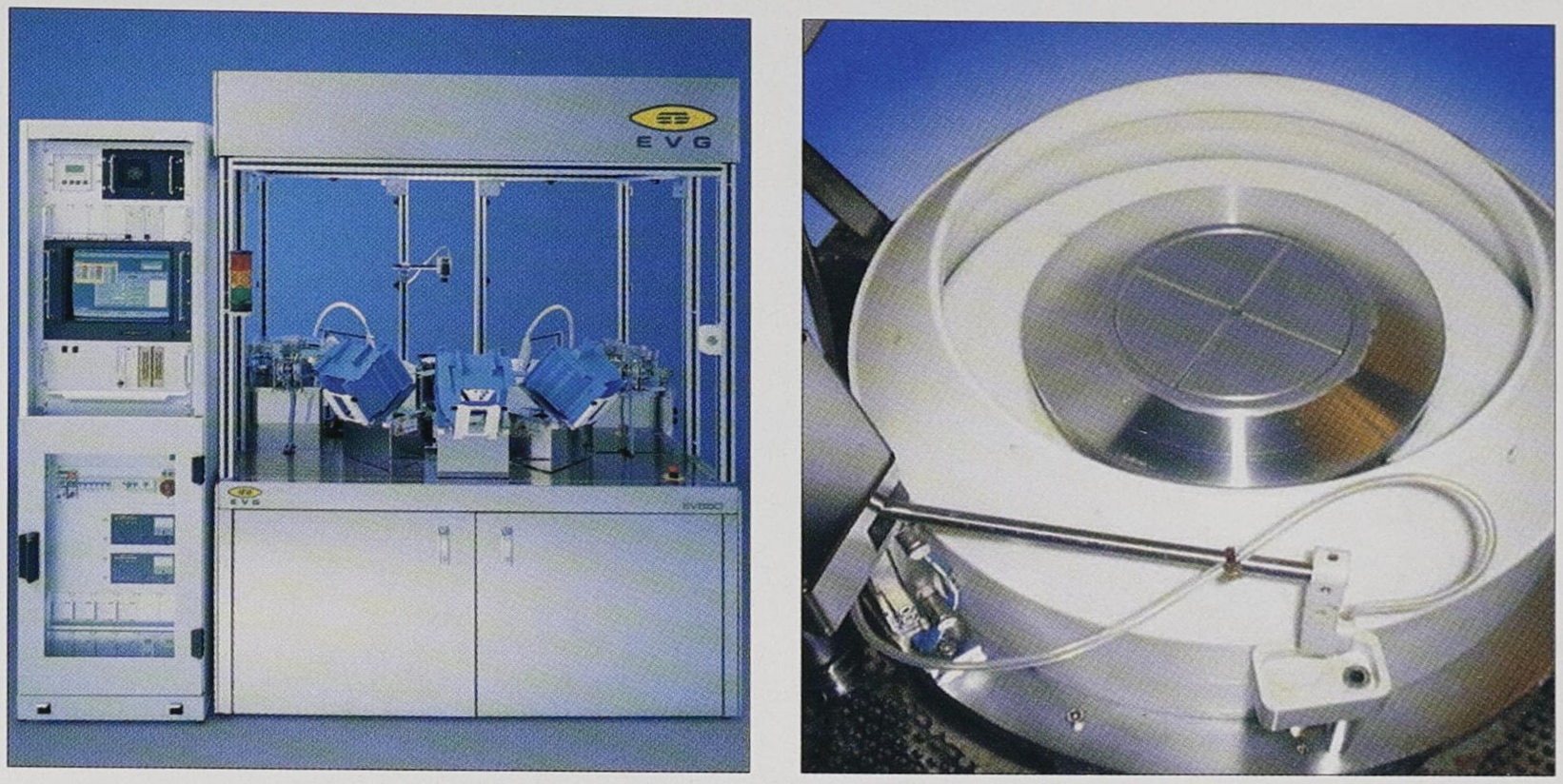


Fig. 1. An EV Group bonder (left), and the coating module and heatable chuck (right).

Fully automated wafer bonding for compound semiconductor processing is a novel and highly promising manufacturing technology that supports new ways of processing thin and large wafers. Reliable back-thinning and backside lithography can be performed on GaAs wafers temporarily bonded to a carrier substrate. In all cases, the bonding processes were initially developed through manual handling which is not suitable for volume manufacturing. This article will describe state-of-the art methods and corresponding results of wafer bonding for manufacturing thin and fragile compound semiconductor wafers in an automated system. Aligned reversible wafer bonding to a rigid carrier substrate is employed for optimum handling of thinned wafers in high-volume production environments.

Aligned reversible wafer bonding to a rigid carrier substrate is employed for handling thinned wafers in high-volume production.

Wafer-bonding techniques

Wafer bonding is a key technology for the production of MEMS and MOEMS (micro-electro and micro-opto-electromechanical systems) as well as for large-scale SOI (silicon-on-insulator) applications. The most widespread permanent wafer-bonding techniques in MEMS and MOEMS are anodic bonding, fusion or silicon direct bonding and thermo-compression bonding. The latter utilizes interface layers of glass frit, metals for eutectic bonding or adhesives. For SOI wafer fabrication, a reversible hydrophilic bond between a bare Si wafer and an oxidized Si wafer is established. In the subsequent annealing process at around 1100 °C the reversible bond is transformed into a permanent bond.

Reversible wafer bonding for compound semiconductor applications is a brand new process, which could establish itself as an important enabling technology in the industry. GaAs and other III-V material processes frequently require back-thinning and backside lithography. However, these steps are extremely tricky – and sometimes impossible – to implement because of the fragility of the materials involved.

Reversible bonding

One solution to these handling problems is reversible bonding. III-V device wafers are coated and then bonded to a carrier substrate. After this, the device wafer can be handled for back-thinning and backside lithography can be performed. Using a carrier substrate improves the mechanical strength while an intermediate layer bonds and further protects the surface of the device wafer during grinding and polishing. This type of bonding is termed reversible because device and carrier substrates can be de-bonded quite easily once back-thinning and backside lithography have been completed.

Different materials, such as sapphire, quartz or even Si wafers, are commonly used as the carrier substrate in reversible bonding. Various intermediate layers are used to form a bond between the wafers; these include spin-on adhesives, laminated dry films and laminated or spun-on waxes.

Integrated systems automate the application of these bonding agents. Spin-on adhesives can be applied using spin-coat modules similar to those in photoresist applications, while dry films are laminated with commercially available equipment. A protective film can then be removed for bonding on a de-liner station of the automated bonding system.

The typical total thickness variation (TTV) in the above methods ranges from 1 to 10 μm. Reversible wafer bonding using high-temperature wax with good TTV requires the layer to be spin-coated in the liquid phase. The results and process steps of a fully automated system for wax bonding will now be reviewed in more detail.

The wax-bonding system

The bonding system developed by EV Group is used in conventional wax-coating and reversible-bonding processes. Figure 1 shows a photograph of the equipment with a close-up of the proprietary wax-coating module, while figure 2 (page 66) shows the typical

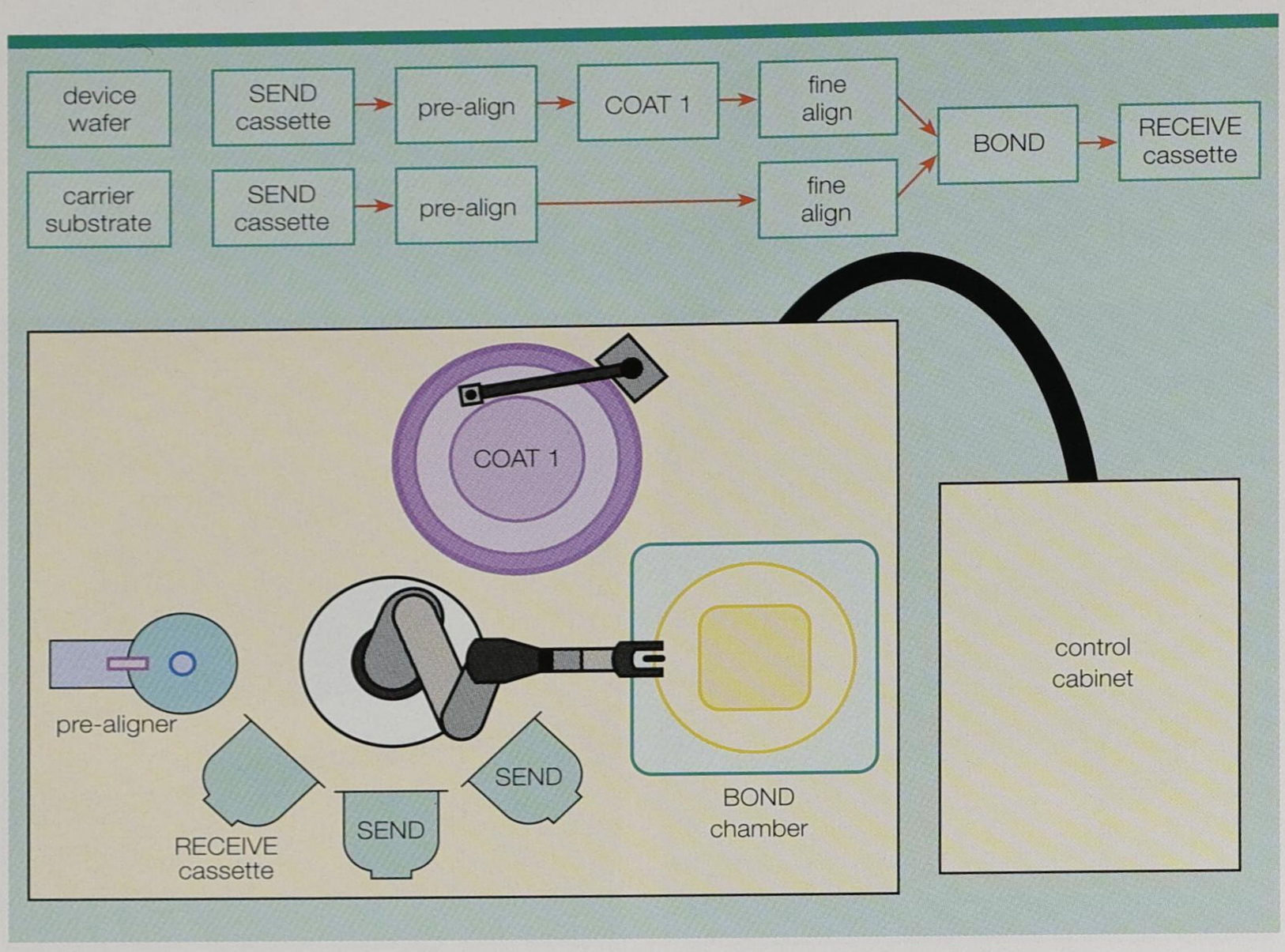


Fig. 2. The process flow for automatic wax coating and bonding, and a schematic top view of the tool for wax bonding the device and carrier wafers.

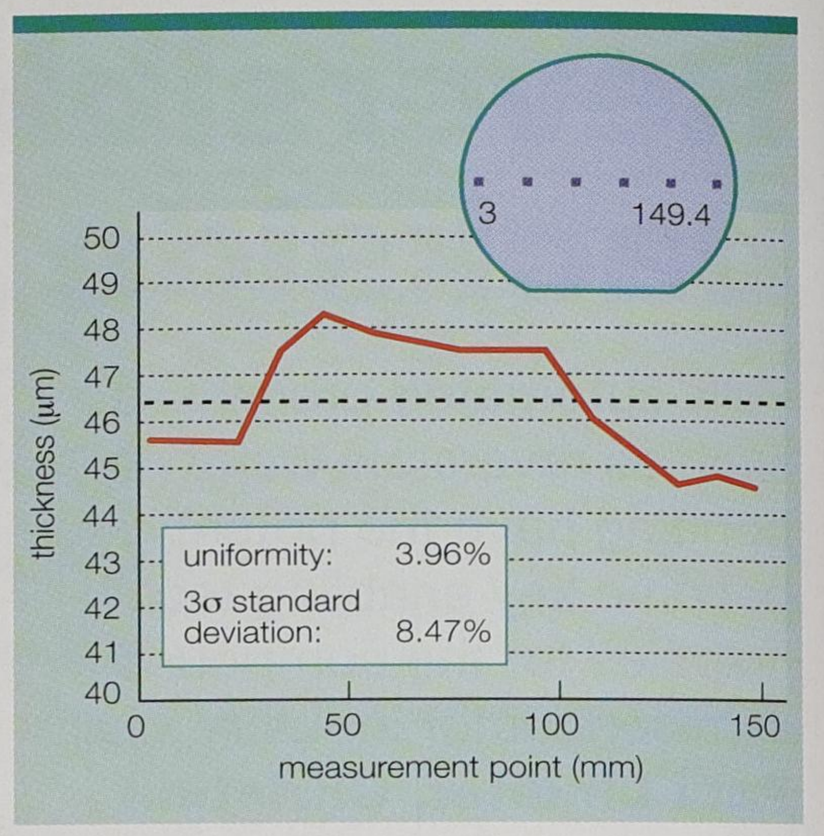


Fig. 3. A graph displaying the final results on wax coating of a 6 inch GaAs wafer.

process flow and layout of an integrated cluster-like wax-bonding system. Device wafers and carrier substrates are stored in individual cassettes for automated loading. After optical pre-alignment, the device wafers are coated in a module, and the wax is dispensed at elevated temperatures onto the active device wafer surface. The components used include heated dispense lines, special dispense pumps and a heatable spinner chuck. The thickness of the wax coating ranges from 20 to 100 µm.

The thickness uniformity of a typical wax layer across a 6 inch GaAs wafer is shown in figure 3. The target thickness was 45 µm with a remarkable uniformity of better than ± 4%. The uniformity is further improved during the bonding process.

After coating, the device and carrier wafers are loaded into the bond chamber where they are aligned to each other. Special techniques are used for the fine alignment, since carrier substrate and device wafers may be different sizes. After bonding, which is fully software controlled, the wafer pair is loaded into a receiving cassette. Further processing at this stage includes the back-thinning of the device wafer and backside lithography. The bonding force exerted by the wax interlayer can withstand the wafer grinding and chemical-mechanical polishing (CMP). For lithography, the wafer is coated with photoresist, aligned to the photo-mask and exposed.

Successful bonding and de-bonding have been achieved with wax and several other intermediate layers at the highest level of automation available.

Optical alignment

Equipment for later process steps can generally handle wafers mounted on carriers. However, one important difference in the handling, is the optical pre-alignment capability of wafers mounted to a carrier. The diameters of the carrier wafers and device wafers vary, though the device wafer is usually slightly smaller than the carrier. The alignment during bonding provides accuracy better than 100 µm and 0.1°. The pre-alignment systems of subsequent production tools (such as mask aligners) are set up to pre-align the device wafer rather than the carrier wafer.

High-volume production uses mask aligners for backside lithography. Systems have to be specifically tooled for these compound semiconductor applications. Special optics are provided in order to perform backside precision alignment on wafers mounted to a carrier substrate. The bottom-side microscope observes the alignment features of the active device wafer through the transparent carrier substrate. The depth of focus of the mask-aligner microscope has to be changeable. This focal-plane change is performed by utilizing the most accurate and repeatable axis of the alignment stage, rather than by refocusing the microscope. After the backside is processed, the automated de-bonding of the device is supported on the same equipment platform used for bonding with thermal release agents.

Conclusions

The move towards high-volume production requires the automation of process steps that were initially developed only for manual handling. Successful bonding and de-bonding have been achieved with wax and several other intermediate layers at the highest level of automation available. The subsequent processing of bonded wafers is performed on specialized lithographic equipment that accommodates the accurate pre-alignment of the device wafer.

High-volume wafer bonding and de-bonding have been demonstrated and achieved on the EV850 system and could become key enabling technologies for the industry.

Paul Lindner, Christian Schaefer and Josh Palensky are with EV Group. Lindner and Schaefer are based in Schärding, Austria while Palensky works in Cranston, RI. Manfred Reiche works for the Max Planck Institute of Microstructure Physics in Halle, Germany. This article is taken from a paper presented at the Compound Semiconductor Manufacturing Expo (CS-MAX) in Boston, MA on 9–11 July, 2001.

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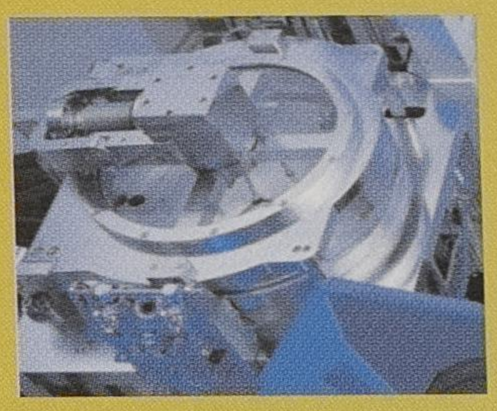
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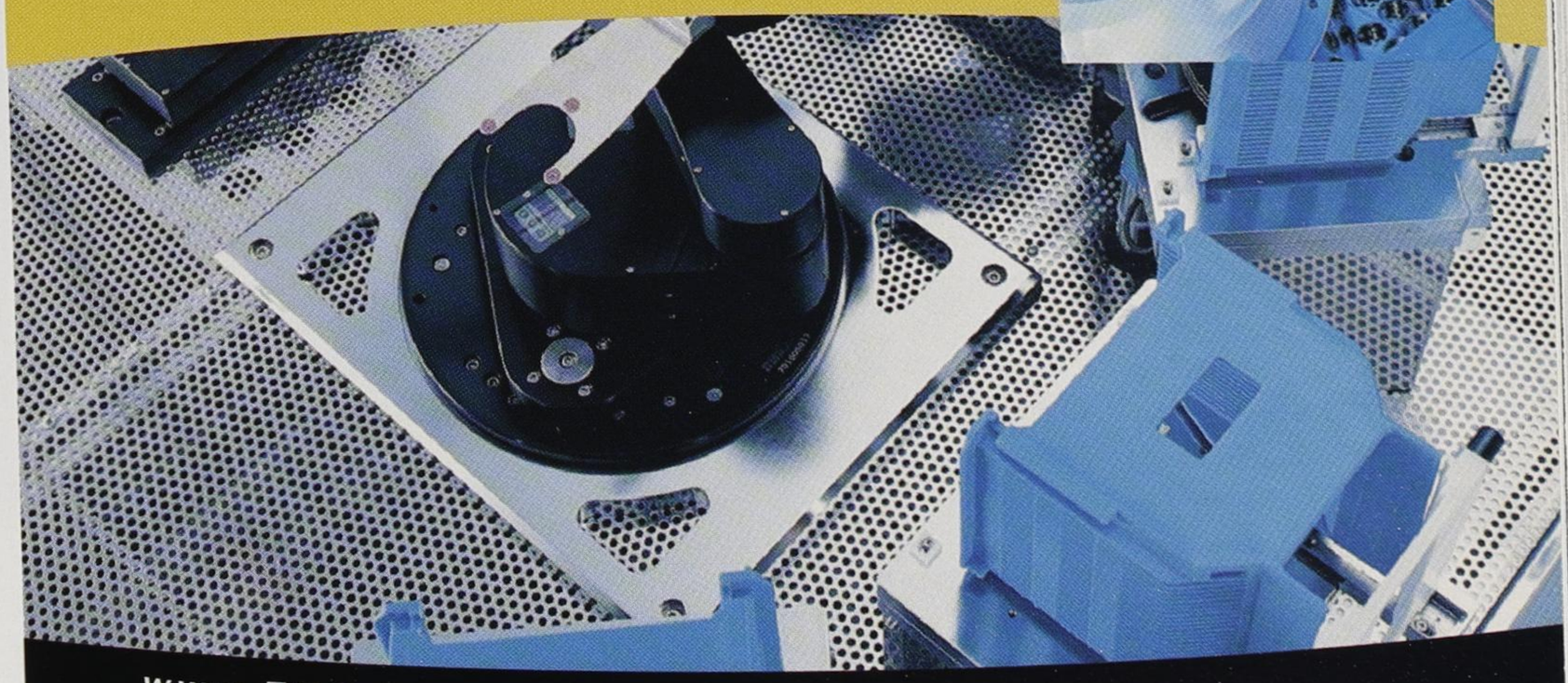
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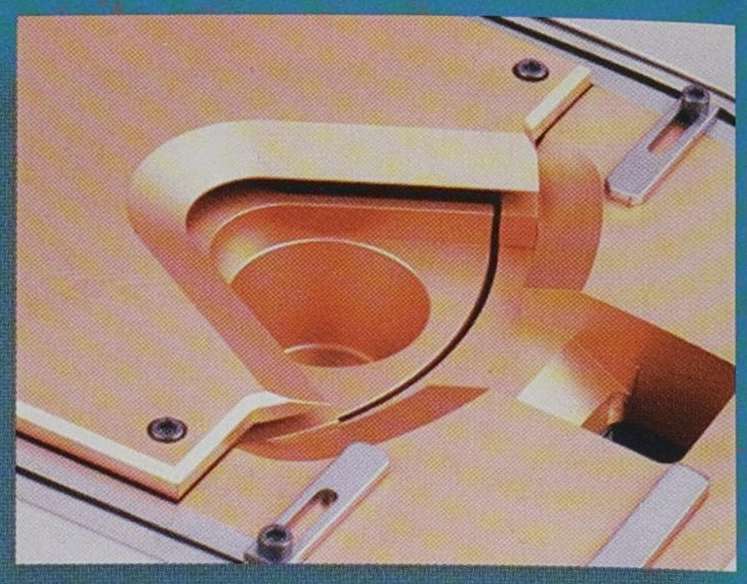
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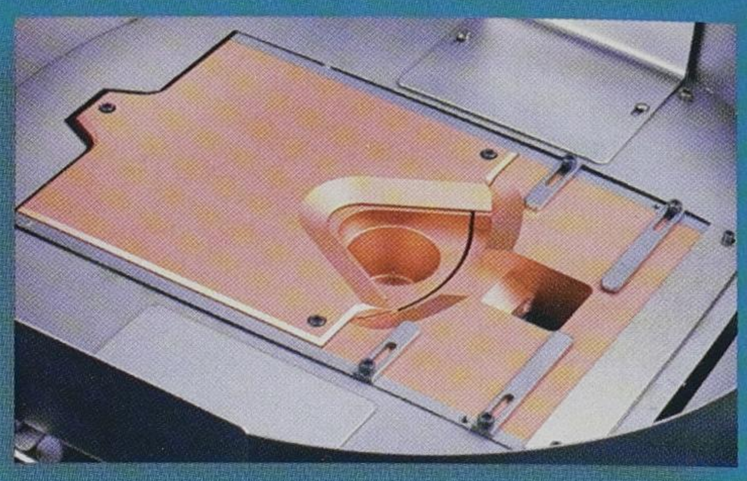
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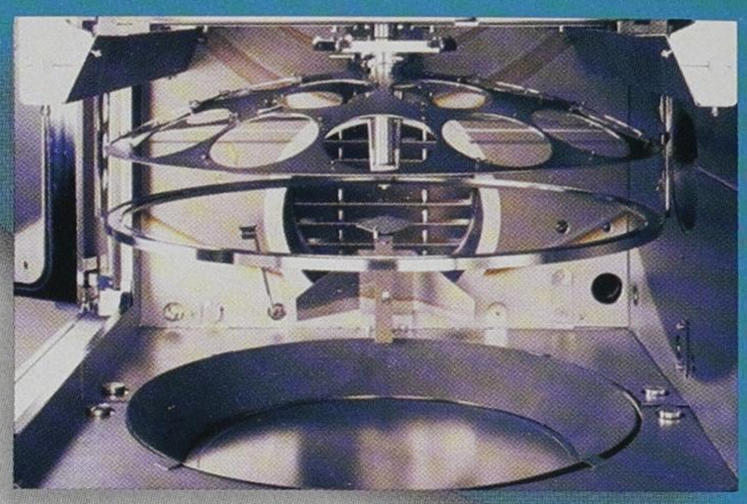


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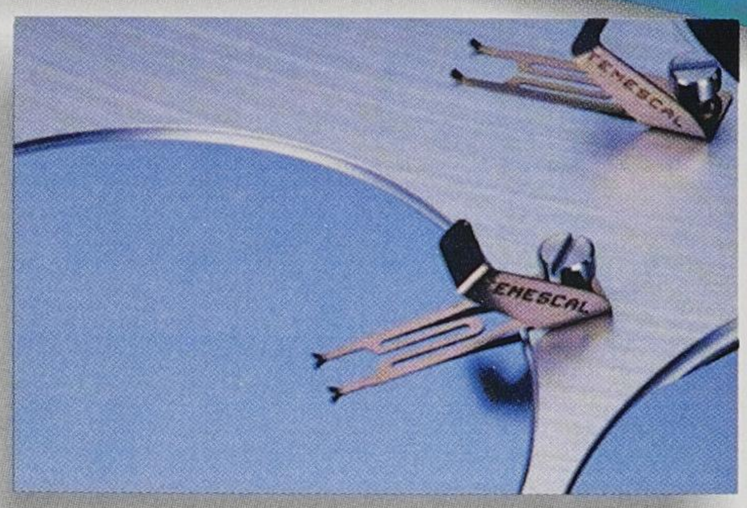


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Masks improve uniformity of lift-off coating processes

The introduction of custom-designed uniformity masks can enhance lift-off processing systems, write **Leszek Malaszewski, Ping Chang** and **Cris Kroneberger**.

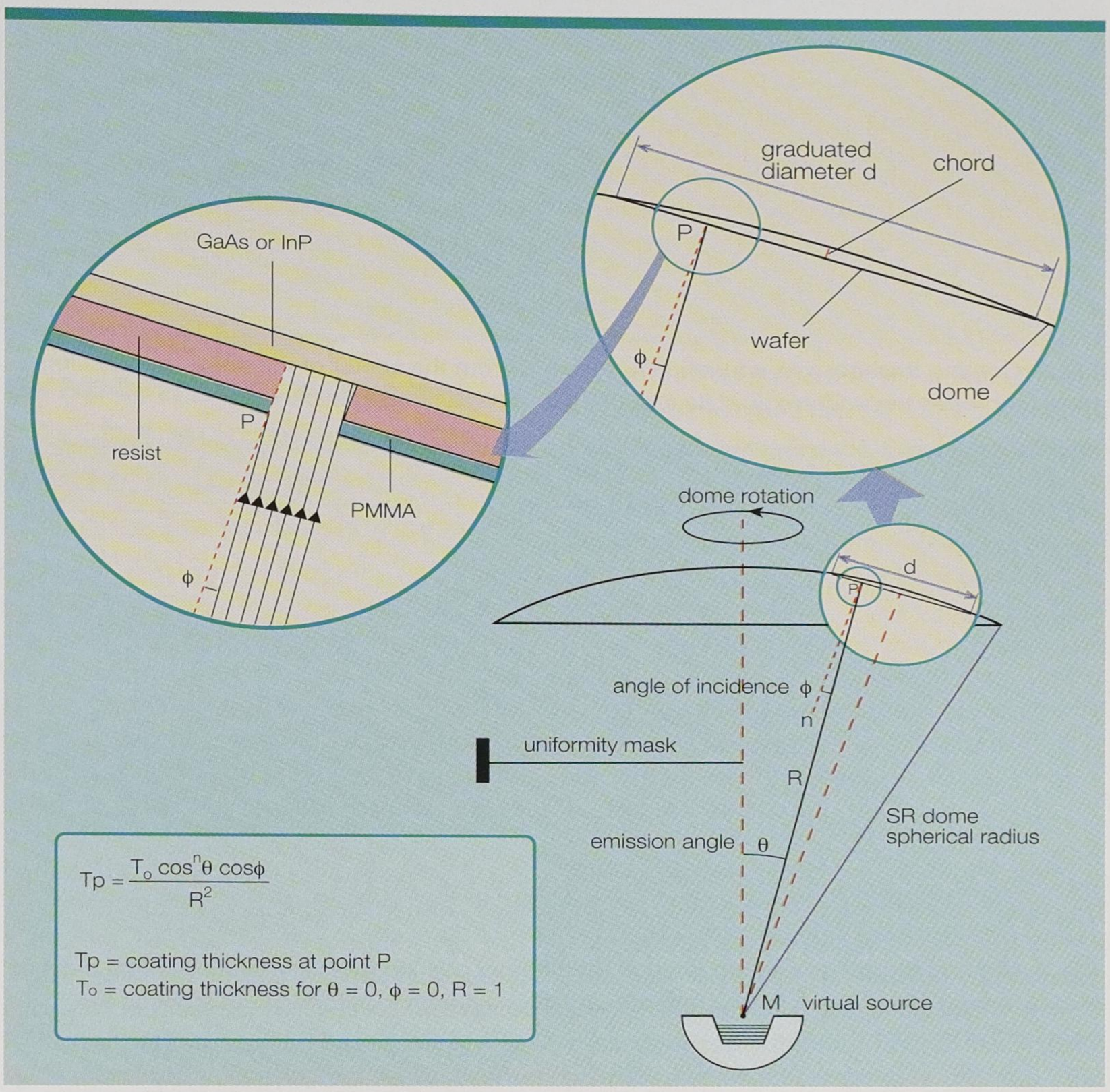


Fig.1. A typical system and component configuration for a lift-off coating process.

Physical-vapor deposition (PVD) is a technique for depositing thin metal layers on semiconductor wafers, and electron-beam evaporation is a method of PVD used more specifically for lift-off processes (Hill). In high-frequency applications, the need for metals that do not have high resistance surface oxides has led to the use of gold for interconnects, junctions and gates on compound semiconductors such as GaAs and InP (Wood). The difficulty in etching the gold (and the underlying metal layers) is avoided when patterning is generated by lift-off.

In the lift-off process photoresist layers are patterned, exposed and developed, and PVD deposits metal across all of the wafer's surface. The unexposed photoresist, together with its metal covering, is then lifted off, leaving metal lines on the wafer. For a lift-off to be successful, material must not be deposited on the side-walls of the photoresist; this requires the substrate to be perpendicular to the impinging vapor stream.

Metalization systems use rotating substrate holders to coat a large number of wafers during one process to maximize throughput and metal utilization. Because of the need for a perpendicular vapor stream, the substrate holder (known as a dome) rotates about the centerline of the evaporation source. To ensure perpendicular vapor deposition with respect to all substrates, this dome is a part of a sphere whose radius should equal the distance between the virtual source and the substrate (Hill and Chang). The typical system and component configuration for the lift-off process is shown in figure 1.

Unfortunately the coating formed on a lift-off dome is not uniform in thickness. Flat or conical planetary systems are used for optical coatings and produce excellent uniformity with the vapor source being offset, but do not fulfill the requirement of normal vapor impingement. Consequently to ensure acceptable uniformity for all wafers, a lift-off dome arrangement must rely on a mask placed between the source and the dome.

Factors affecting coating thickness

The general factors that influence thickness uniformity on a lift-off dome are:

- the distance between source and substrate;
- the rate of evaporation and angular vapor distribution;
- whether a uniformity mask intercepts some of the vapor;
- the relative motion of the substrate (substrate rotation is essential in every case).

The assumptions commonly used in modeling are that the vapor source is a point source (labeled M in figure 1), and that the vapor distribution follows an approximation of the cosine rule. Accordingly, the coating thickness Tp at point P on the wafer surface is a function of θ (the emission angle of the vapor stream from the source), ϕ (the angle of incidence at the wafer surface) and the distance R between vapor source M and point P. The relationship between these is shown in figure 1. Factor n is directly related to the material's evaporation rate and system configuration.

Point M is stationary with respect to the chamber, and point P rotates around the axis of the dome. The theoretical coating distribution across a lift-off dome is plotted in figure 2. When a large flat substrate is fitted on a spherical dome, the flatness of the sub-

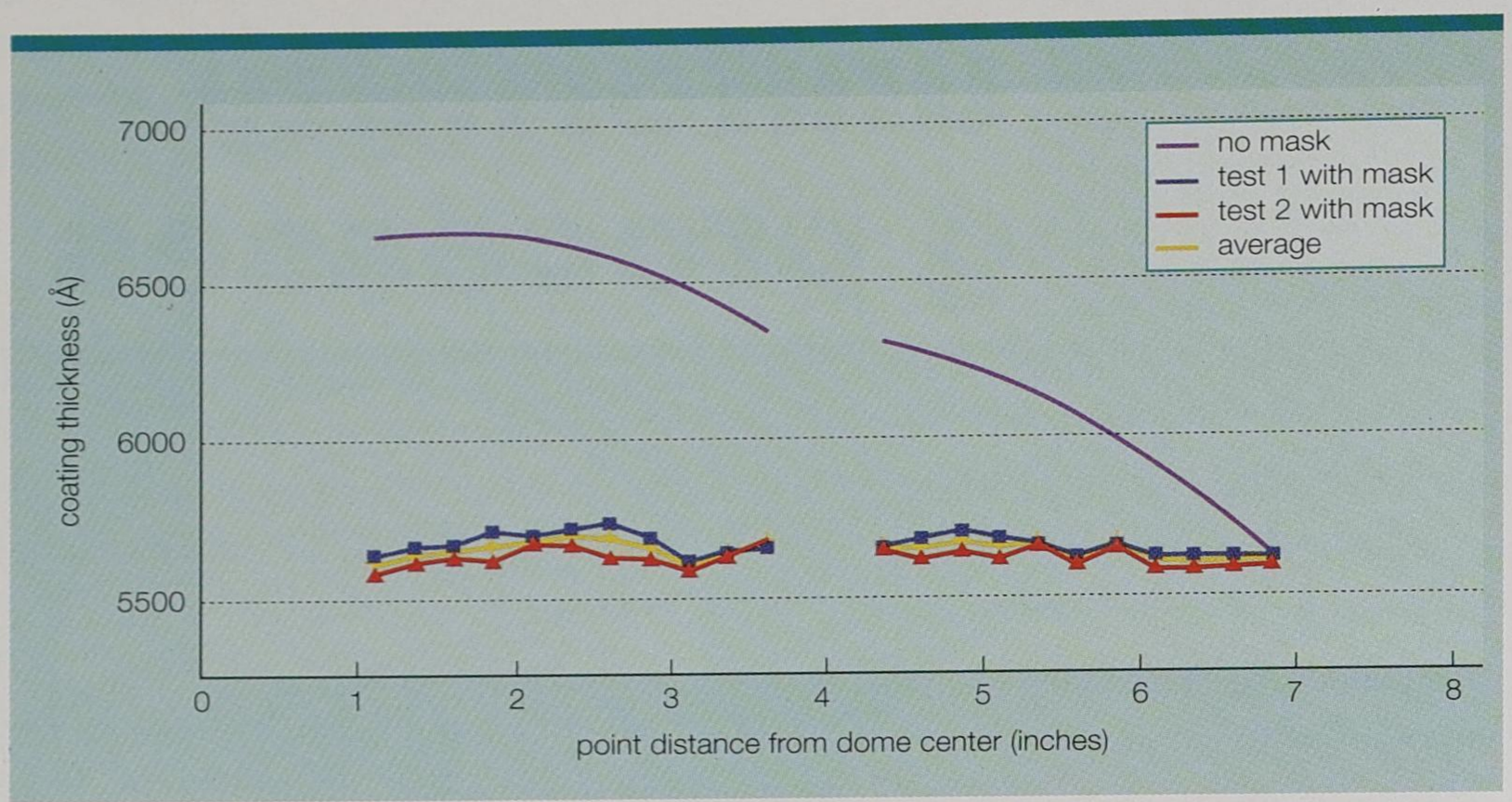


Fig. 2. Coating thickness as a function of distance from the center of the dome. Introducing a mask improves the uniformity while reducing the overall coating thickness.

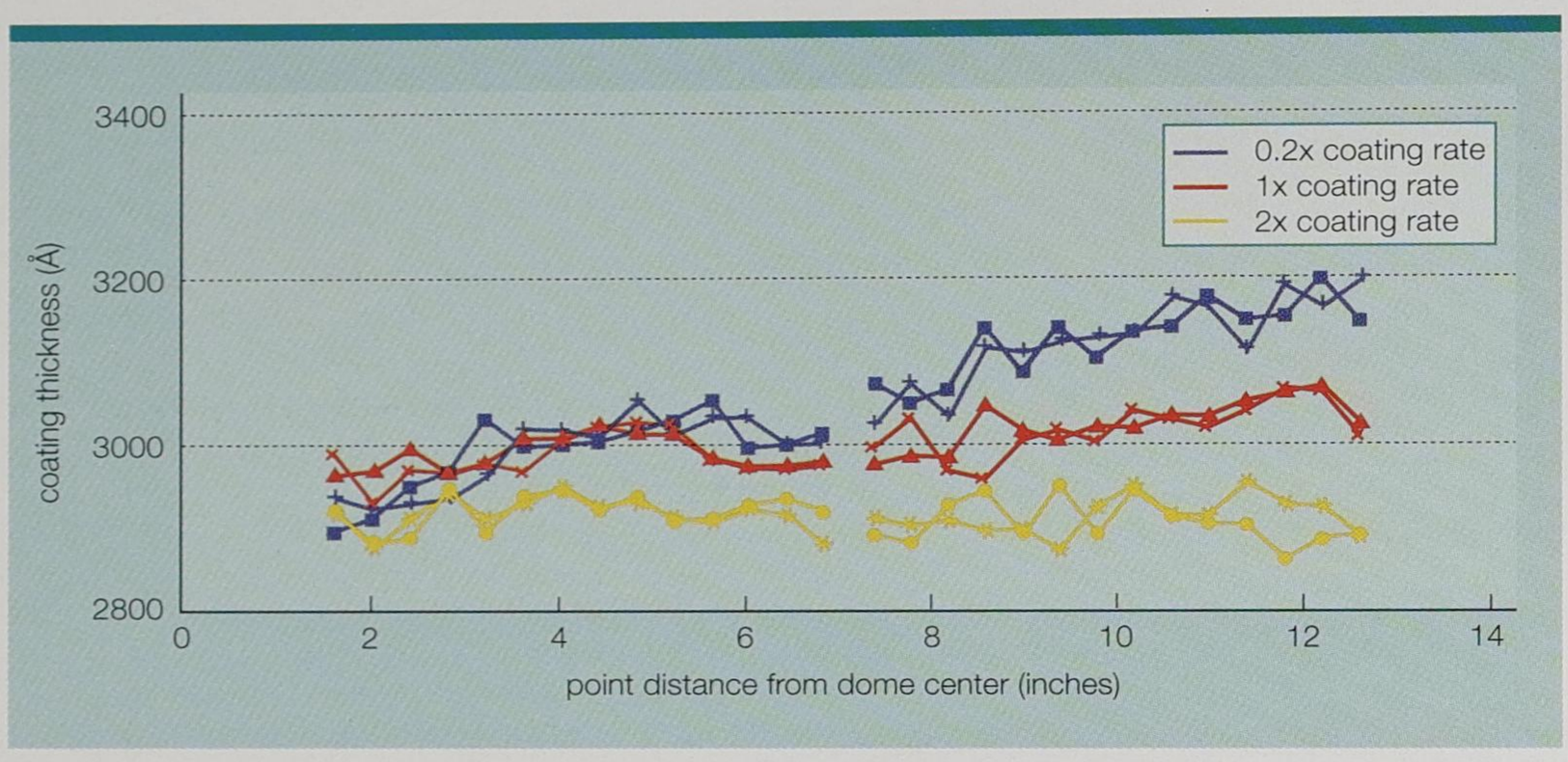


Fig. 3. Coating thickness and distribution for different coating rates in a system with a mask and two rows of wafers. A higher rate of deposition improves uniformity but reduces the coating thickness.

strate will further reduce the uniformity.

Uniformity masks

Because the vapor deposition profile is related to a cosine distribution, in a single rotation almost half of the evaporant flux must be interrupted towards the center line where deposition is fastest. This requires the mask to block the vapor in the areas where normally one would expect thicker deposition layers. Achieving uniformity thus reduces "collection efficiency". Figure 2 also shows a comparison of the typical coating thickness distribution for systems with and without the benefit of masks.

Computer programs have been created for uniformity mask development that allow the graphical representation and analysis of measured coating thickness distribution for each row of wafers on a dome. The programs calculate uniform thickness distribution and generates shape data for mask fabrication. Mask shape outputs are provided with X and Y co-ordinates, and as a polynomial fit for mathematical and statistical analysis. The enhanced mask profiles can be generated remotely from the installed system if the user supplies accurate data. The revised mask profile can then be sent by fax to be incorporated at the user's site.

Figure 2 shows the coating thickness distribution with and without a uniformity mask for a dome configuration with two rows of wafers. Coating uniformity without a mask for depositing Ti was determined to be 2.44% for the first row and 5.67% for the second, giving a 3σ uniformity of 15.73%. After installing a standard Ti uniformity mask, the coating process produced uniformities between 0.76% and 1.11% for both rows of wafers, and a 3σ uniformity between 1.74 and 1.97%.

Standard uniformity masks

The standard domes used in Temescal evaporation systems can handle most wafers between 2 and 6 inches in diameter. Wafers can be positioned in 1–4 rows depending upon dome and wafer size. The shape and location of the installed mask have been optimized for systems with and without a collar. The collar is an extension ring inserted between the source and the substrate to increase the distance between them. A larger distance reduces the angle of incidence toward the wafer edge, improving the thickness uniformity. Each source-to-substrate distance needs its own radius dome. Each of five increasingly larger systems with a lift-off dome has a standard uniformity mask made for evaporating Ti. The standard mask can generate better than ±4% uniformity for wafer diameters of 2–6 inches, regardless of their location on the dome.

Conditions affecting uniformity

Substrate rotation and the rate of evaporation of selected materials massively affect the uniformity of coating thickness in lift-off processes. Additional influences, which make the coating thickness distribution deviate from the simple cosine distribution model, include the following:

- the emission angle of the vapor stream;
- the obstruction of the vapor by crucible wall, shields or other elements;
- the type of material used;
- the level of material inside the crucible;
- the formation of a vapor cloud, instead of a surface, that acts as virtual source.

These effects are minimal in well designed systems where coating is performed under stable conditions.

Multi-layer coating uniformity

Simple III-V compound semiconductor interconnects, junctions and gates consist of a thin titanium adhesor layer and a thin platinum or palladium diffusion barrier, which are finally followed by the thick gold conductor. The thickness uniformities required for each layer and for entire stacks are additional challenges for lift-off processes. The thickness and uniformity of every layer can be adjusted to accommodate the requirements for multi-layer stacks. Each metal's rate of evaporation affects a uniform distribution, but can be used to optimize the material evaporation process.

However, the adhesor and diffusion barrier layers are thin, and even an absolute uniformity figure greater than a few percent may be acceptable. At 200 Å thickness, even a 6% uniformity represents only 12 Å or four atom layers. However, given that the uniformity mask "blocks" deposition for almost half a revolution of the dome, in the case of thin coatings rotation must be fast enough to ensure that each wafer is coated equally. For example, to achieve a coating thickness of 200 Å at a deposition rate of 10 Å/s (a total time of 20 s), deposition should take place over 10 revolutions to ensure adequate averaging. Requiring 10 revolutions in 20 s equates to 30 rpm.

Figure 3 shows that the change in evaporation (and thus deposition) rate affects uniformity. Once a uniformity mask has been developed for a set of conditions, any change in rate can alter the uniformity and may need a modified mask.

Temescal's system designers recognize this problem, and use a multi-mask philosophy in the case of tight specific uniformity tolerances for multi-stacks. Thus a set of specific uniformity masks is designed for each metal with well defined coating-process parameters. Each mask is sequentially moved into position as each metal is deposited. Though this system is more expensive and complex, the performance often offsets the cost with a higher production yield and every layer having an excellent even thickness of coating.

The cheaper way of handling multi-layer metal deposition is to use one mask for all coatings that has been developed for the thickest or most critical layer in the stack. While the other materials are tuned and optimized for rate and dome rotation to ensure acceptable absolute thickness uniformity, the values may be higher if expressed as a percentage.

Very tight uniformity requirements

Coating processes can be improved to yield very tight thickness uniformity as long as they are stable and well optimized. Although standard uniformity masks provide an even 4% thickness for wafers 2–6 inches in diameter, they can be adjusted for the individual wafer diameter and for the specific wafer row as shown in figure 4. Square dots represent the required mask performance in relation to the specific wafers and row locations at constant coating process conditions. The thick line represents a universal polynomial shape that can accommodate any size at any row locations.

As an example, a thickness uniformity of

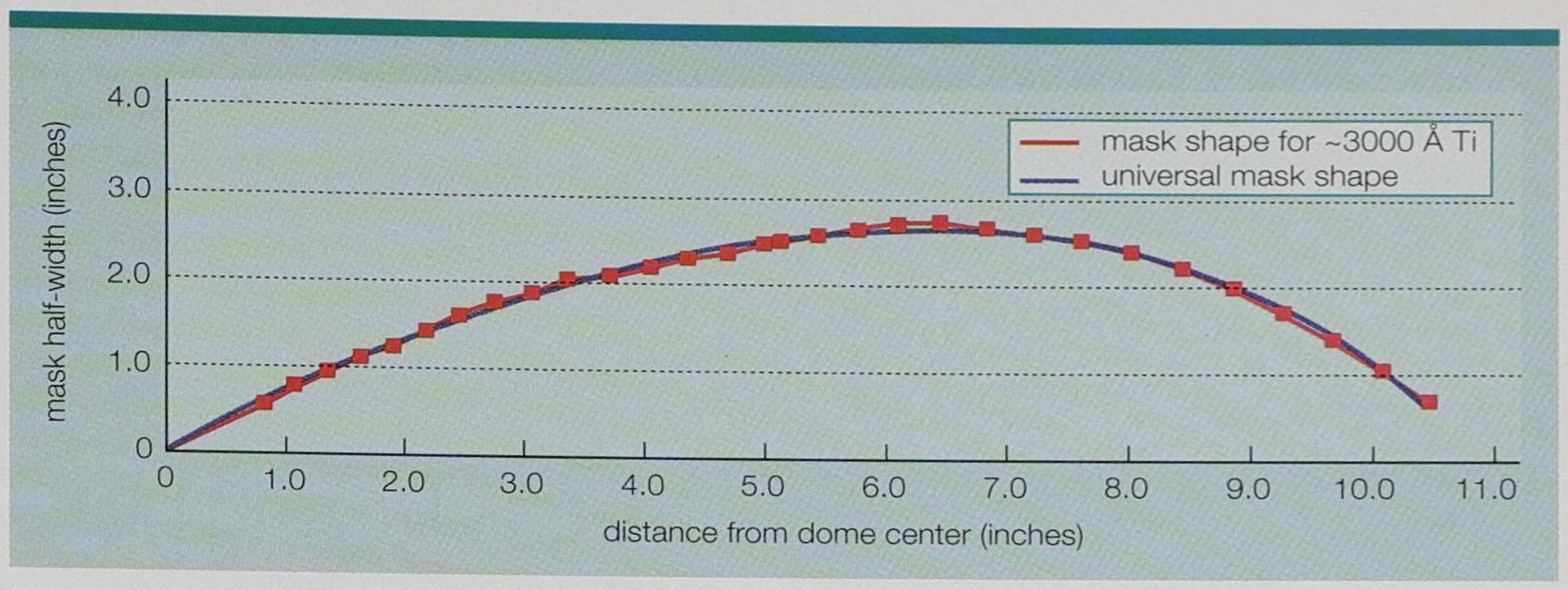


Fig. 4. Mask shapes: the black line represents a universal shape that can accommodate any wafer size at any row location, while the red line represents a mask designed for deposition of ~3000 Å Ti.

Electron-beam evaporation systems can be supplied with custom-designed products to enhance their capabilities.

1% was achieved with an improved mask for gold at a specified evaporation-source pocket size and controlled material level for systems in production at Infineon Technologies in Munich. Usually only two iterations are required to provide total uniformities in the ±1% range.

At Alpha Industries in Woburn, MA, the "no mask" uniformity for gold on 6 inch GaAs wafers held on a 27 inch diameter dome was ±15%. After the program defined the initial mask profile, a simple mask of stainless steel foil was installed. The thickness spread was again measured on new wafers, and a second mask was made and installed. After this was measured it was found to be ±1.25% – well within the specification.

Limitations in mask design

Coating thickness data for uniformity mask development is based on measuring the actual coating thickness layers deposited during the coating process. Wafers must be properly oriented on the dome so that coating thickness distribution on the wafer is measured along the imaginary line extending from the dome center to the dome edge, passing through the wafer center.

Well calibrated thickness-measuring equipment is fundamental for obtaining accurate coating distribution data. It is also necessary to measure film thickness in various locations on the wafers. Temescal recommends a 0.25 inch or 6 mm gap between locations.

It should be noted that the dome is a segment of a sphere and that the wafer is a flat surface attached to the dome. The angle of incidence depends on the actual position on the wafer diameter, so the source-to-substrate distance is slightly different from wafer center to wafer edge. For the sake of a mathematical exercise, one could assume that the source-to-substrate distance R is equal to the dome's spherical radius. Localized thickness distribution on a single wafer is influenced by cos(ϕ), where ϕ represents spherical angle and the cos(ϕ) variation represents the thickness uniformity limit.

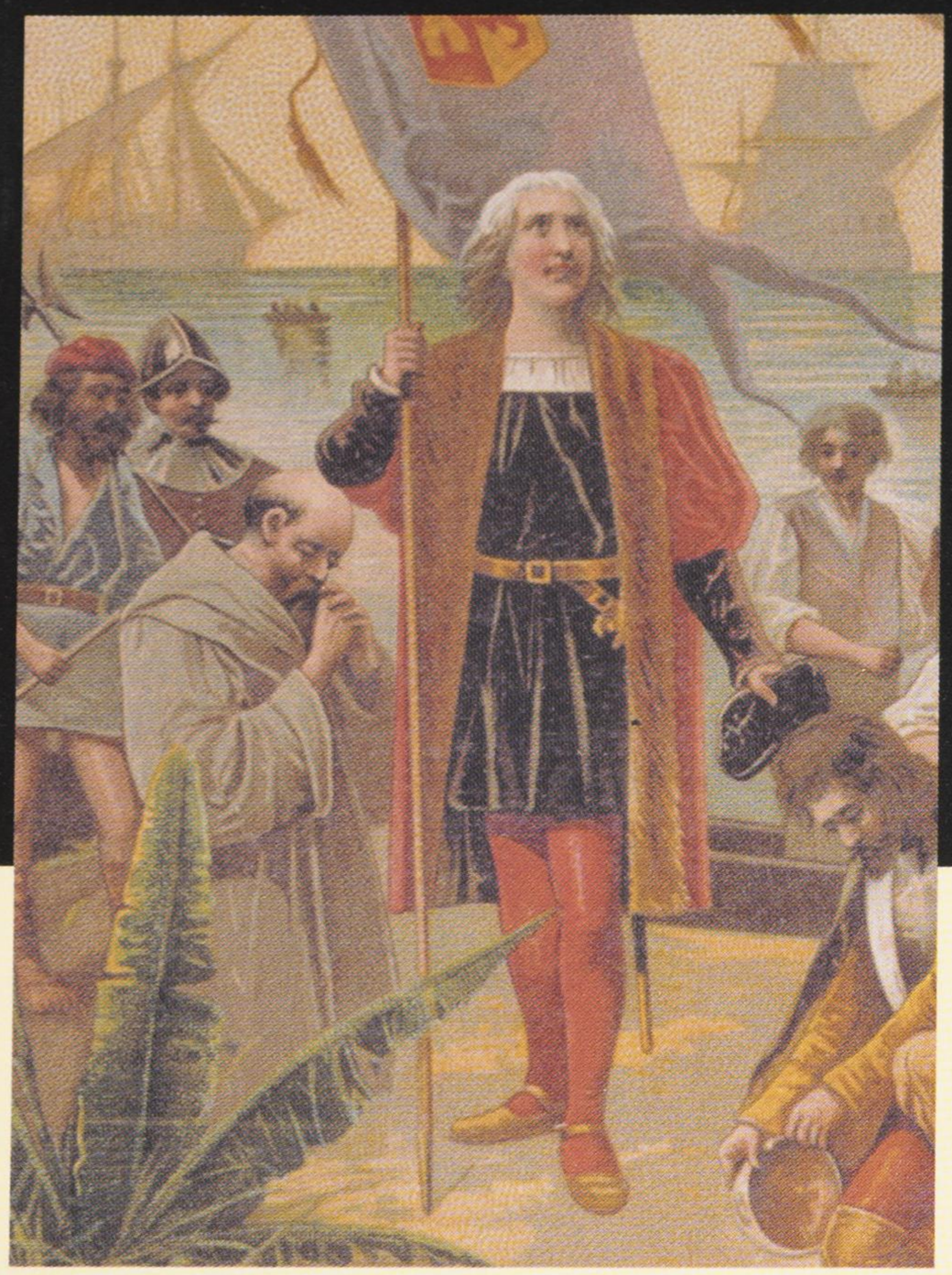
Conclusion

Electron-beam evaporation systems are widely used for lift-off processing, and can be supplied with simple coating uniformity masks or custom-designed products to enhance their capabilities. The enhanced mask profiles can be generated remotely from the installed system, provided the user supplies accurate data. The profile can then be faxed to be incorporated at the user's site.

Further reading

R Hill 1986 *Physical Vapor Deposition* (Temescal, California).
R Hill and P Chang 2001 Electron Beam Evaporation Part II *Vacuum & Coating Technology* 51.
C Wood 2000 Hetero-Structures for High Performance Devices *Handbook of Thin Film Devices* ed. M Francombe (Academic Press, San Diego).

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Sputtering process gives III-V devices a performance boost

The shift from evaporation to sputter deposition for metalization, combined with the use of cluster tools, is yielding great benefits to forward-thinking device manufacturers, writes **Andy Bavin**.

Over the past several years the maturing compound semiconductor market has seen a distinct shift toward high-productivity IC manufacturing techniques. Increasing substrate diameters and higher product volumes create the desire to use the type of mass-production equipment first employed by the silicon semiconductor industry. Although partially driven by the high manufacturing capacities required throughout the boom year of 2000, this shift continues today as forward-thinking device manufacturers reap the rewards offered by the low cost of ownership of silicon-style tools.

The metalization process is one of many that have shown clear advantages from this change in manufacturing philosophy. Metal deposition has traditionally been performed by e-beam or thermal evaporation techniques in batch-style tools, but single-wafer sputtering is becoming increasingly popular in advanced manufacturing facilities. This has only been made possible through the careful adaptation and development of the sputtering process for compound semiconductor applications. In this article we examine the development of sputtering for many III-V metalization processes, including lift-off applications, and look at the benefits obtained through the use of sputtering in contrast to traditional methods.

Cluster tools

Although modern cluster tools often have high initial capital costs, they still offer significant financial savings compared with older batch-style tools. Cassette-to-cassette processing removes the need for the large amount of time and space traditionally used to load batch tools. This reduces the amount of engineering support required by the tool, resulting in a cut in operating costs. By removing the need for manual wafer loading and physical wafer clamping, cluster tools also reduce the risk of damaging the expensive III-V substrates.

Batch-style tools provide high throughputs by processing a large number of wafers at the same time. However, as substrate diameters increase, fewer can be loaded into the tool, so the overall throughput reduces. Cluster tools can provide higher throughputs when processing larger wafers, enabling one tool to replace many. They also feature three levels of vacuum integrity through the vacuum cassettes, wafer handler and ultrahigh vacuum process modules. This buffered approach to vacuum integrity and the control offered by single wafer processing ensures that process contamination is near zero, dramatically increasing the yield of the finished devices.

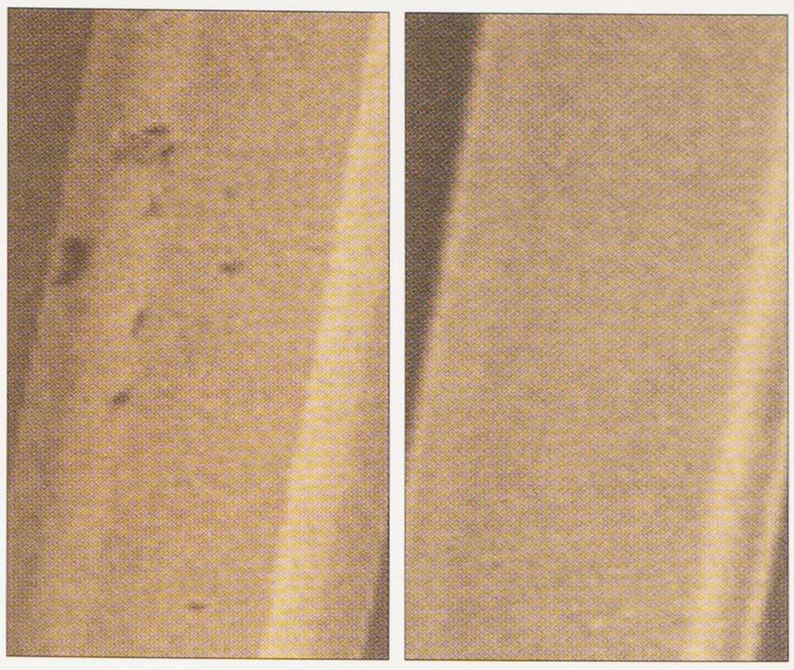


Fig. 1. A comparison between (left) standard deposition and (right) long-throw deposition. The long-throw process results in structures that are more sharply defined.

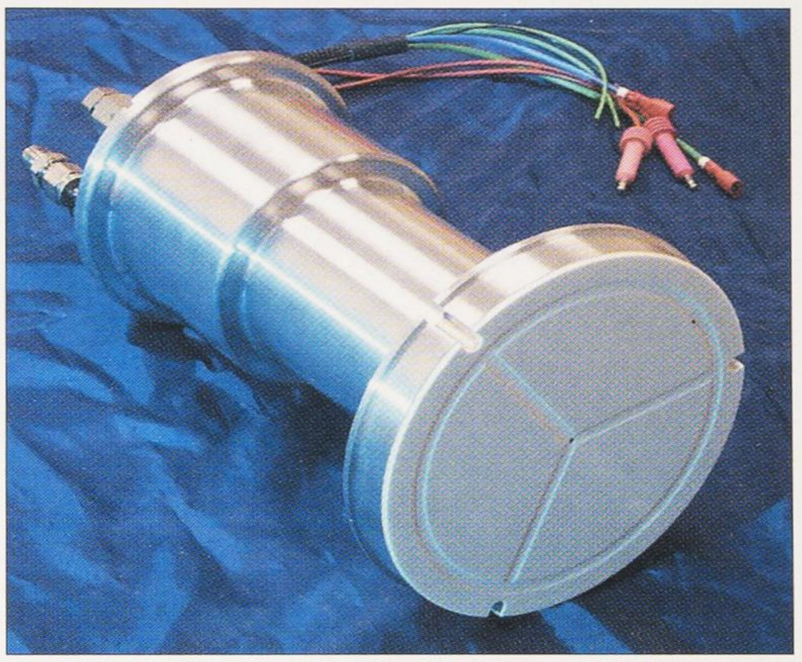


Fig. 2. The gas-cooled electrostatic chuck. Heat passes into the chuck allowing high deposition rates without substantial wafer heating, even for heavy materials.

Benefits of sputtering

Although it was the productivity benefits of cluster tools that first interested metalization engineers in changing from batch evaporation to sputtering, it was soon discovered that the sputtering technique itself offered significant advantages to compound semiconductor device manufacture. The high ion energies associated with sputter deposition produce highly dense metal films. This has been proven to improve the yield of finished devices through increased resistance to contamination and better film adhesion.

Further yield benefits are gained through reduced particulate contamination. Even when running at exceptionally high deposition rates the sputter target will never reach temperatures above 300 °C. This prevents the target material from melting and producing the particulate "splashes" commonly associated with evaporation techniques.

Unlike evaporation, where materials have to be co-deposited from different sources with different deposition rates, sputtering allows the deposition of mixed films from a single target. This ensures that the deposited film has a uniform, repeatable film stoichiometry even when performing reactive depositions in a nitrogen or oxygen process ambient.

Sputtered metals

In spite of all the benefits mentioned, sputtering has taken a long time to become a commercially attractive alternative to batch evaporation. Although sputtering is commonly used to blanket-deposit front and backside pre-plate seeds, it has traditionally been difficult to use for the wider range of lift-off applications. For the lift-off process to be successful the metal deposition has to be directional to prevent resist encapsulation, and cold to prevent resist reticulation. Unlike evaporation, sputtering is neither directional or cold, so it has taken significant hardware and process development to produce a reliable sputter lift-off. >>

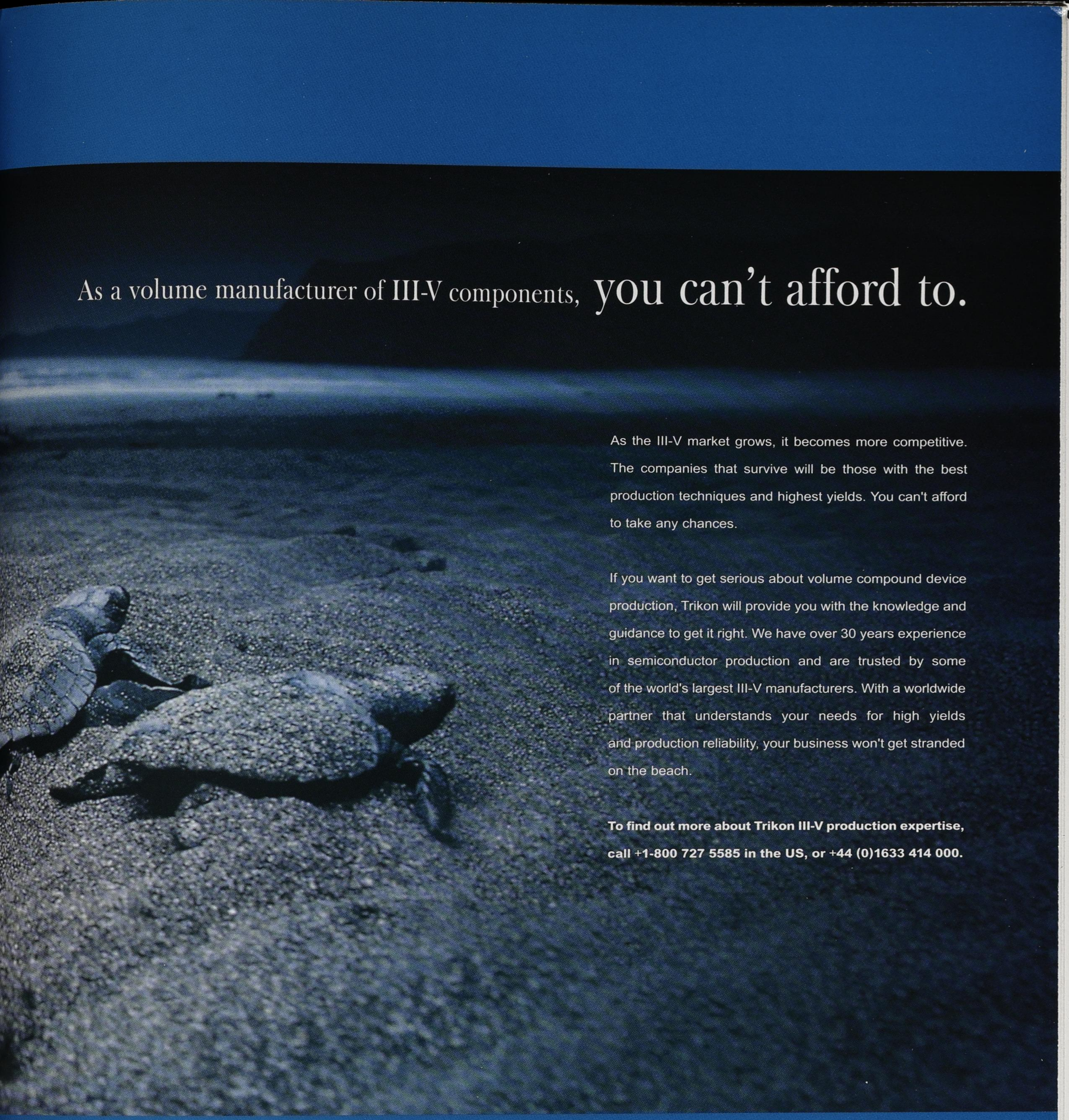
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Hardware developments

The silicon industry initially identified the need for directional sputter deposition when depositing barrier materials into high aspect ratio contact features. This was achieved by increasing the throw distance between the target and the wafer (figure 1, p73). Any material sputtered from the target at a low angle cannot reach the wafer, instead sticking to a shield on the inside of the process chamber. Although this technique reduces the utilization of the sputter target it does not dramatically increase the cost of the deposition, as approximately 80% of the material deposited onto the shields can be reclaimed and reused.

The long-throw deposition process has a number of advantages over competing collimating techniques. Firstly it requires no additional chamber furniture, so the number of possible particle sources within the module is minimized. Secondly, because the plasma is removed from the wafer the temperature of the deposition is reduced significantly. Data obtained in Trikon's applications laboratory have shown a 20% reduction in wafer temperature when the same TaN film was deposited with a longer throw distance. Lastly long-throw is an exceptionally simple solution, enabling high equipment uptimes and reliability and further reducing the cluster tools' cost of ownership.

The temperature of the sputtering process can be controlled by clamping the substrate electrostatically to a cooled chuck (figure 2, p73). Argon, passed between the wafer and the chuck, improves the thermal conductivity of the substrate, allowing the heat generated by the deposition process to pass into the chuck without substantially heating the wafer.

Experiments performed in Trikon's applications laboratory show that the substrate temperature can be kept below 80 °C even when depositing heavy materials such as gold at high deposition rates. The cold electrostatic chuck (ESC) therefore enables sputtered lift-off processes to be performed with exceptionally high throughputs.

Process developments

When depositing at high rates there is a risk of resputtering material from the substrate back onto the sidewall of the open resist window. Loosely attached metal wings can form at the edges of the lift-off feature that can delaminate under physical shock and short-circuit the device. In the worst case, resputtered material completely covers the sidewall. This prevents lift-off by stopping the chemical solvent from reaching the photoresist.

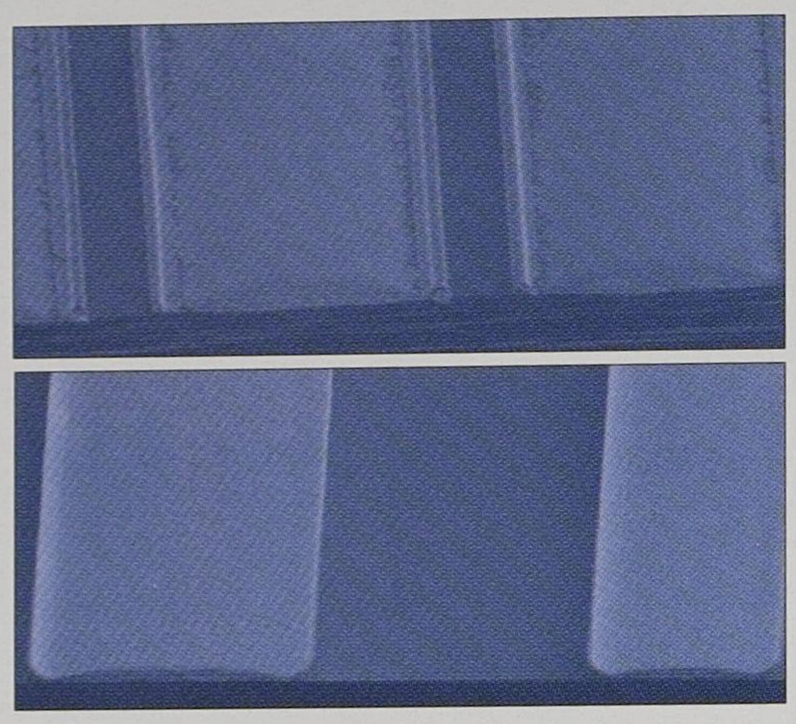


Fig. 3. A comparison of (top) the wings generated by resputtering from the substrate, and (bottom) sharper structures from a process which reduces resputtering.

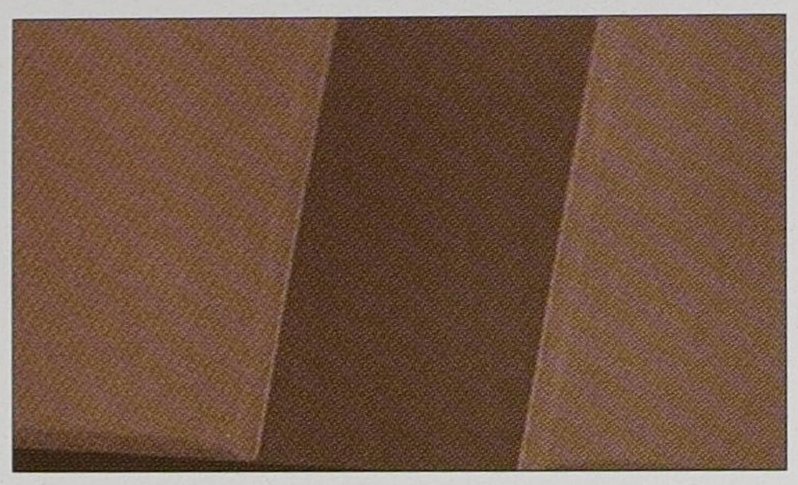


Fig. 4. Well defined metal lines patterned using sputtering and the lift-off technique.

A proprietary process that reduces resputtering has been developed. This enables high-throughput lift-off depositions to be performed with only minimal wing formation, as shown in figure 3. In addition to this a recent project has examined the combined effects of the resist profile, deposition process and post-deposition cleaning (Butler *et al.*). Optimizing the resist profile and sputter conditions, followed by a dry CO_2 treatment after resist removal, produced well defined clean metal patterns (figure 4).

Sputter lift-off in production

Compound semiconductor device manufacturers have been quick to take advantage of sputter lift-off processes in a variety of IC fabrication steps. Sputtering offers a number of benefits to thin-film components, most importantly the repeatable quality and stoichiometry of deposited materials such as tantalum nitride (TaN), nickel chromium (NiCr) and silicon nitride (Si_3N_4). Moreover, as these materials are relatively inexpensive and the components consist of very thin films (less than 1000 Å thick), ultra-long throw distances can be used to provide exceptional deposition directionality without large increases in device costs or reductions in throughput.

Lift-off has traditionally been used to pattern the various metals that form an IC's ohmic contact such as Ti, Pt and Au . In a sputter cluster tool these metals are deposited in individual process chambers, increasing the material that can be reclaimed from the chamber shielding and dramatically reducing the cost of device manufacture. The completed contacts are of exceptionally high quality and production data have shown them to have less contact resistance and increased defense against contamination when compared with evaporated equivalents. This brings increased benefits to the finished device in terms of operational powers and extended reliability.

Trikon's Sigma sputtering tool offers the ability to deposit on both the front and backside of device wafers without changing any hardware. In this way a tool configured for contact metalization can also be used to deposit pre-plate seeds into through-wafer vias. The directionality of the long-throw deposition increases the proportion of sputtered metal that reaches the bottom of the via, enabling continuous coverage with reduced film thickness. The cold ESC is able to clamp through an insulating carrier into the wafer itself, providing excellent wafer cooling without carrier metalization.

Today's sputter cluster tools perform numerous metalization steps in production processes worldwide. Customers for these tools have reported all of the efficiency benefits first seen in the silicon industry: higher productivity, increased throughput, reduced labor requirements and fewer wafer breakages. Interestingly, they have also noticed improvements to the performance of completed devices. Increases in yield, reductions in gate leakage and lower contact resistances have all been attributed to lift-off metalization processes using sputtering.

Further reading

D Butler *et al.* (in press) High Performance, High Productivity Interconnect by Sputtered Metal and Dry Carbon Dioxide Lift-off Techniques *CS-MAX 2001 conference proceedings.*

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Rapid thermal processing improves IC performance

The technique of rapid thermal processing in compound semiconductor manufacturing provides extremely low thermal budgets and excellent temperature and ambient control capability. **Hin Yiu Anthony Chung** and **Martin Drechsler** of Mattson Thermal Products explain.

Thermal processing is a key manufacturing step in the compound semiconductor industry. Processes such as implant annealing, contact annealing and the activation of epilayers are all critical stages that directly influence device performance. These processes require a very repeatable and uniform temperature control as well as a precise process-gas control (ambient control). An ideal thermal process should also expose the wafer to the lowest possible thermal budget to prevent degradation. Rapid thermal processing (RTP) is a well established wafer-processing method in the silicon industry, which provides rapid throughput and excellent temperature and ambient control capabilities. Therefore RTP appears to be an ideal technique for the world of compound semiconductor manufacturing.

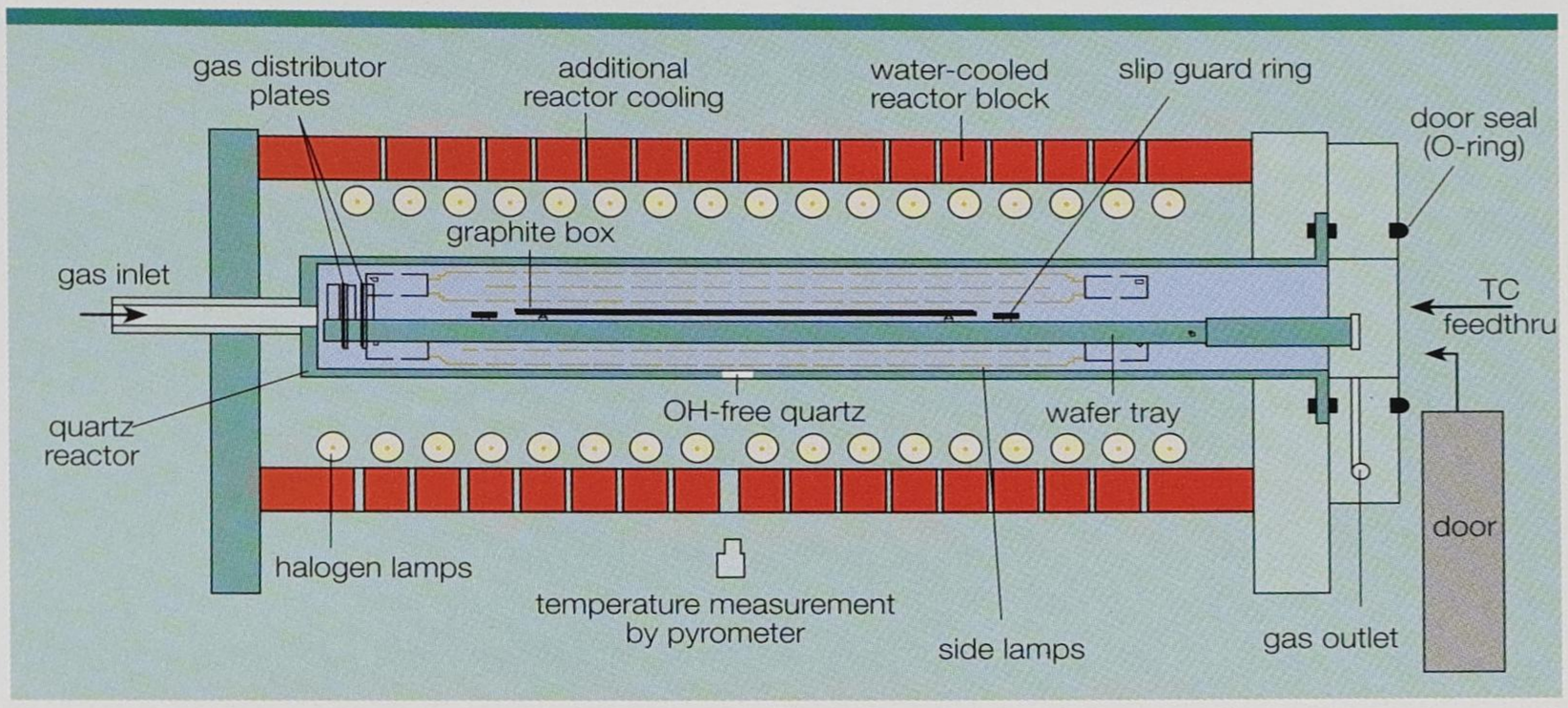


Fig.1. A cross-section of the process chamber of the Mattson 2800CS rapid thermal processing tool. Temperature ramp rates of 30 °C/s or above can be achieved inside.

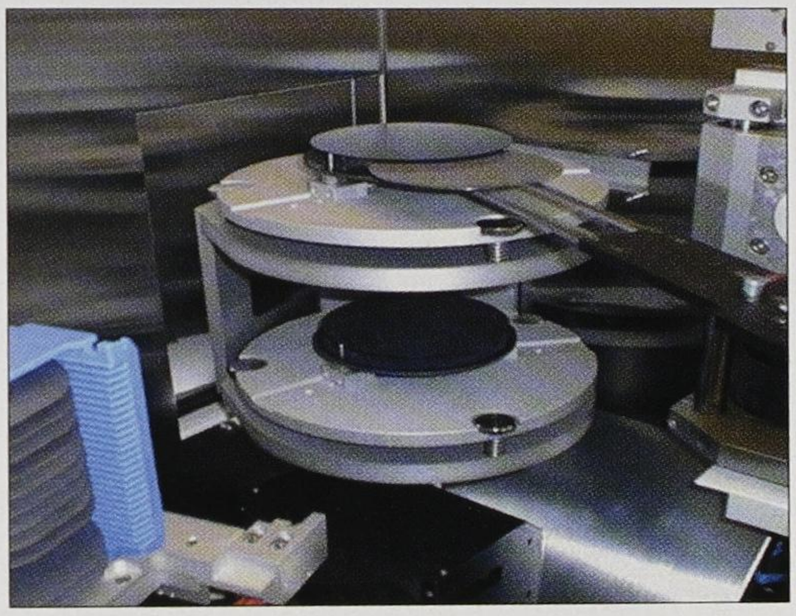


Fig. 2. Fully automatic wafer handling: a 4 inch GaAs wafer is transferred by a robot arm into the graphite box.

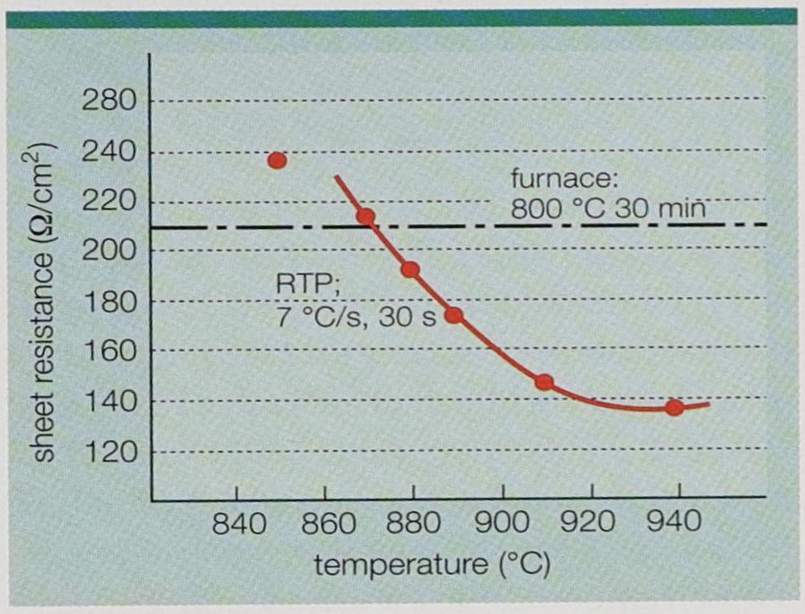


Fig. 3. Comparison of dopant activation by RTP and by a furnace, clearly showing the lower level of defects achieved by RTP.

Key features of an RTP system

The cross-section of a state-of-the-art RTP process chamber (Mattson 2800CS) is shown in figure 1. The wafer is placed inside a graphite enclosure (labeled "graphite box") which prevents the outgassing of group V materials (e.g. arsenic) and cross-contamination between different processes. Linear halogen lamps located above, below and on the left and right sides of the graphite box generate infrared radiation, which is responsible for the heating. Temperature ramp rates of 30 °C/s or above can be routinely achieved inside such an RTP process chamber. The process temperature measurement is carried out by a sophisticated pyrometer, which permits temperature measurements down to 200 °C. Driven by market demand, device manufacturers are now moving from low-volume, small-scale production to high-volume mass production (see *Compound Semiconductor* August 2001, p69). In order to fulfill the requirement for mass-production environments, the RTP tool is based on a cassette-to-cassette concept where the handling of wafers is automatic (see figure 2). Depending on the wafer size and the required throughput, the tool can also be upgraded to process simultaneously seven 2 inch wafers or three 3 inch wafers inside one graphite box. This feature is especially valuable for optoelectronic applications, where small wafer sizes (2 or 3 inches), thin wafers (around 100 μm thick) and high throughput go hand in hand.

Rapid thermal processes

Implant annealing is one of the major processing steps in the manufacturing of GaAs MESFETs. The formation of a conducting channel in the MESFET is achieved by implanting GaAs with silicon atoms, followed by an annealing step. Figure 3 shows a typical curve of sheet resistance against annealing temperature for a GaAs wafer implanted by silicon atoms (10 keV, $1.7 \times 10^{13}/cm^2$). By using RTP (process duration: 30 s, ramp rate: ~7 °C/s), a much lower level of defect generation can be expected when compared with furnace annealing. Therefore, a higher implant activation can be achieved using RTP. Furthermore, owing to the lower thermal budget of the RTP process, less dopant outdiffusion can be expected (figure 4, p78).

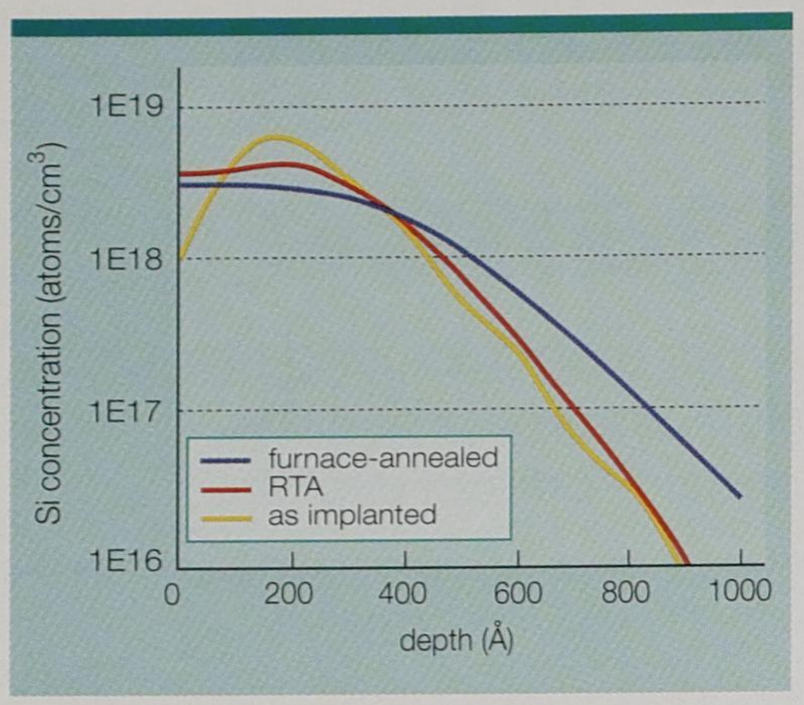


Fig. 4. SIMS profiles of silicon-implanted GaAs, and the dopant out-diffusion caused by different annealing cycles. Less dopant out-diffusion occurs with RTP.

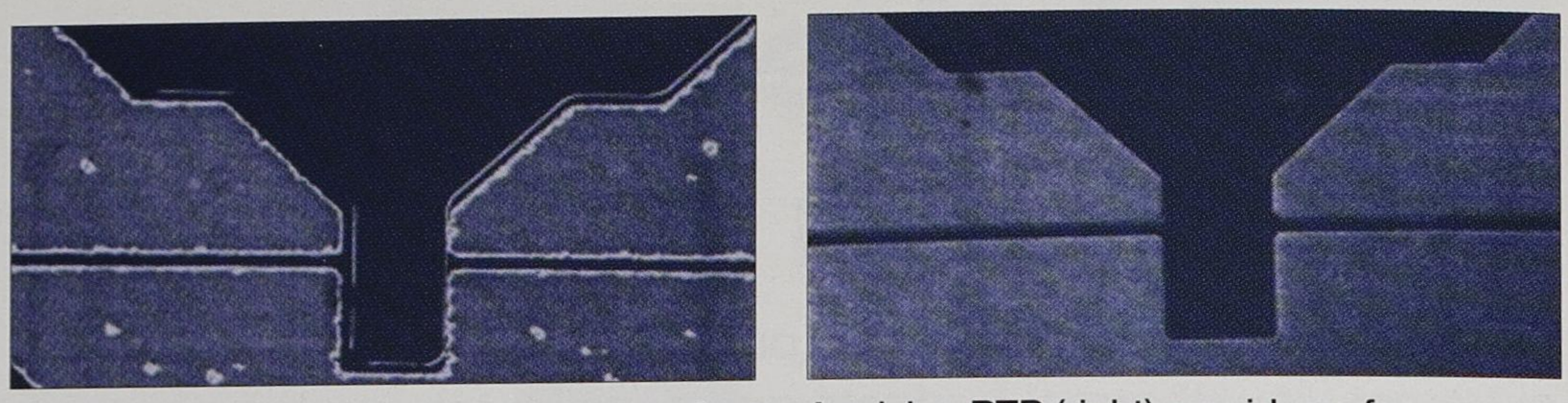


Fig. 5. Morphology of metal contact surfaces. Applying RTP (right) provides a far smoother result than using a furnace for contact annealing (left).

Specific contact resistances achieved by RTP

metal stack	*contact layer*	*dopant concentration (cm^{-3})*	*contact resistance (Ωcm^2)*
Au/Ni/Au/Ge	GaAs, InP	(Si) 1×10^{18}	$\sim 10^{-6}$
Au/Pt/Ti	GaAs	(Be) 1×10^{18}	$\sim 10^{-5}$
Au/Pt/Ti	InGaAs	(Be) 1×10^{20}	$\sim 10^{-5}$

Another key criterion for a successful thermal-processing technique is the temperature uniformity. Excellent temperature uniformity, with a total range of less than 3 °C, can be achieved by RTP across wafers that are up to 6 inches in diameter.

Metal contact annealing is an essential processing step for achieving ohmic contacts in transistor devices like HEMTs or HBTs. By using RTP in contact annealing, state-of-the-art contact resistance can be achieved in typical p- and n-type metal stacks. The table shows typical specific contact resistances obtained after RTP (processing temperature: 400 °C, ramp rate: ~15 °C/s, process duration: 30 s). These values are low enough to provide the good ohmic contacts that are required for manufacturing high-performance HEMTs or HBTs. RTP also generates better morphologies on the metal surfaces. By applying RTP for contact alloying instead of using a furnace, a much smoother surface morphology can be obtained (figure 5).

Modern electronic devices very often contain epitaxial multilayers that are either lattice-matched to the substrate or are pseudomorphic. Thermal treatments on such devices may initiate inter-diffusions between the multilayers, which in turn lead to degradation of the device performance. Therefore it is of great technical interest to investigate the effect of different thermal-treatment techniques on the hetero-interfaces of these devices. In this study pseudomorphic InGaAs layers embedded between two AlGaAs layers were annealed by either RTP (process temperature: 870 °C, ramp rate: ~20 °C/s, process duration: 30 s) or by typical furnace processing. After the annealing, the samples were characterized by high-resolution x-ray diffraction, with the corresponding x-ray rocking curves shown in figure 6. Compared to the curve of the non-annealed sample, there is only a slight displacement of the diffraction peak of the InGaAs layer in the RTP sample. In contrast, the rocking curve of the furnace-annealed sample shows a great change in the diffraction pattern, indicating that a drastic inter-diffusion between the multilayers occurred. These results indicate that RTP creates less inter-diffusion at the hetero-interfaces of multilayer structures than furnace annealing.

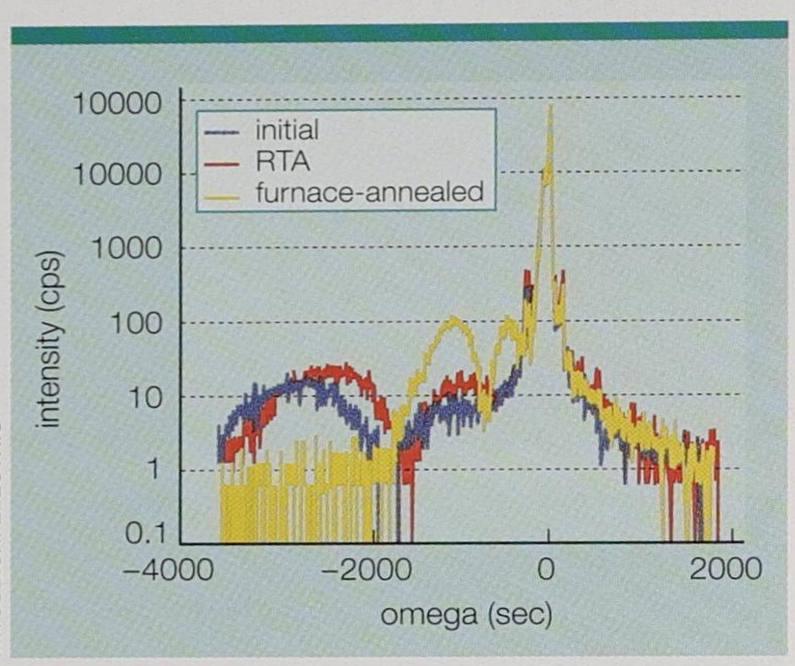


Fig. 6. X-ray rocking curves of InGaAs layers embedded between two AlGaAs layers which have been annealed by either RTP or by a typical furnace process.

Conclusions

The thermal-processing technique of RTP provides an extremely low thermal budget together with excellent temperature and ambient control capability. By using automatic RTP, excellent process results can be obtained under mass-production environments that can hardly be realized by furnace processes. We therefore believe that RTP is the tool of choice for thermal processing in compound semiconductor device manufacturing.

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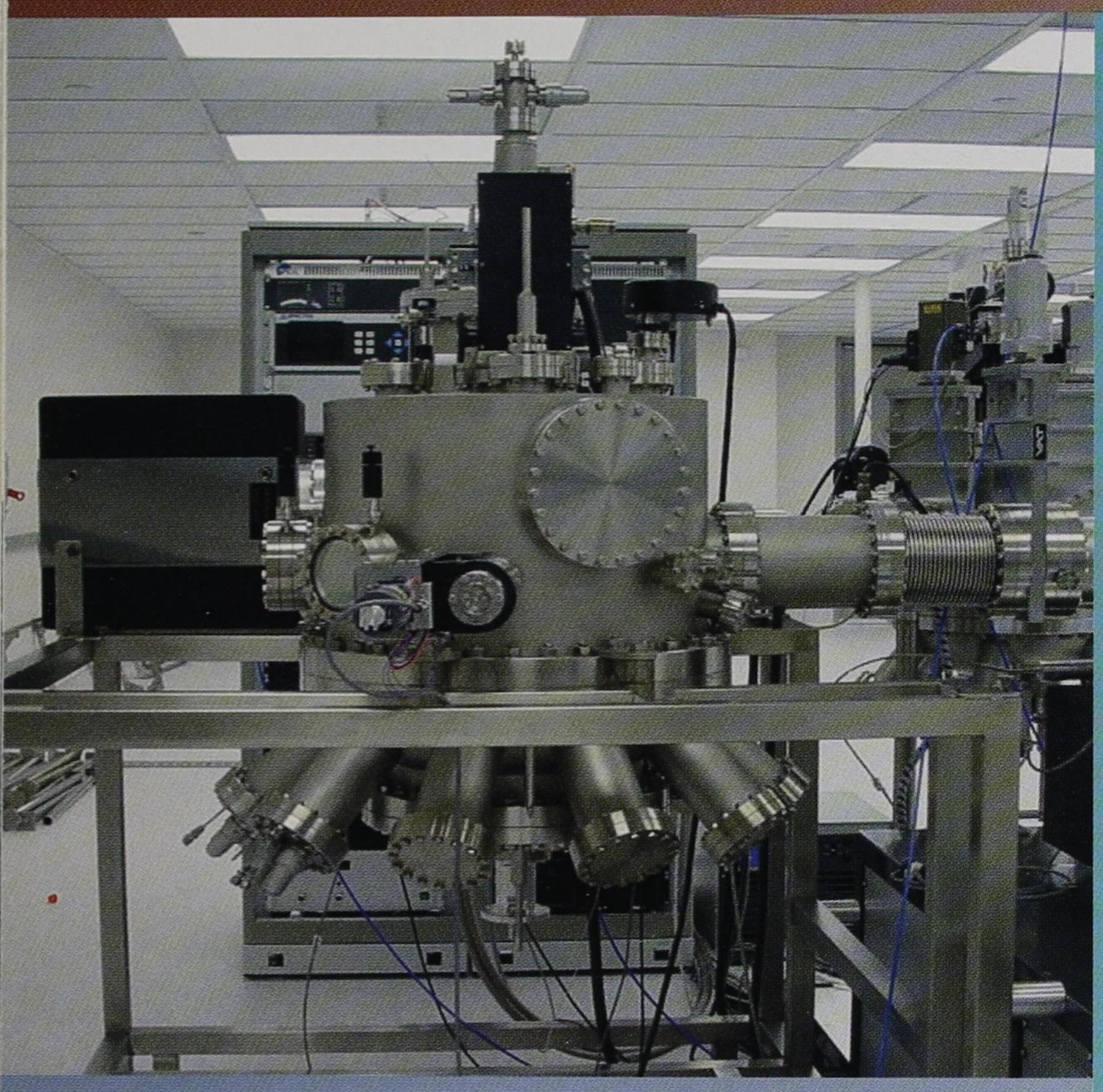
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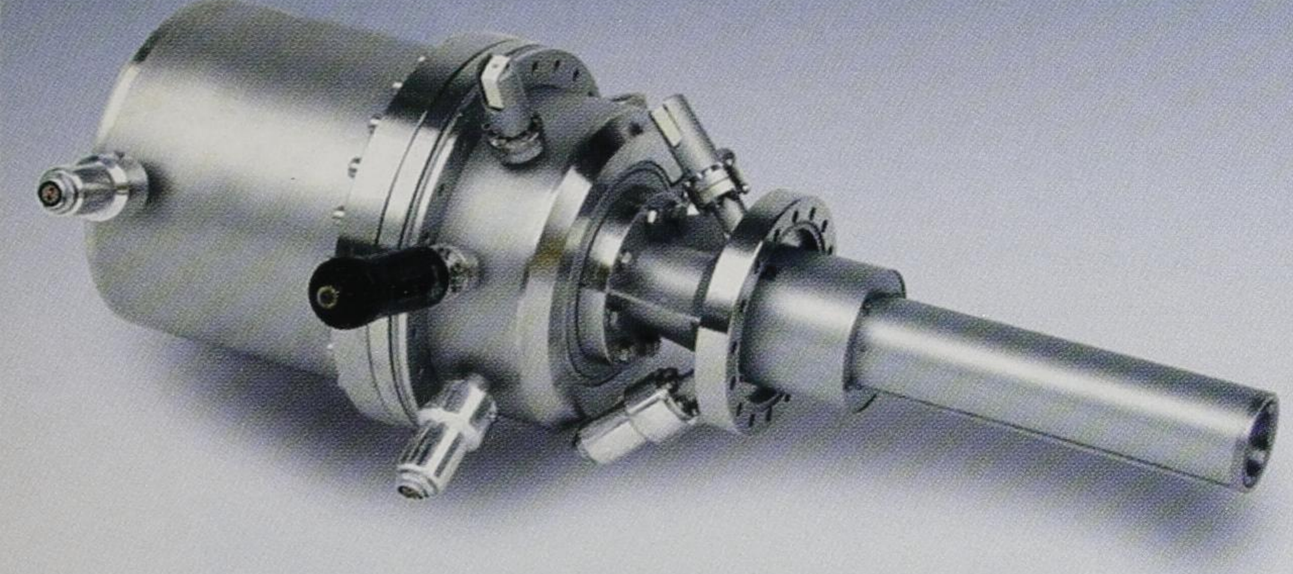
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INSTRUMENTS

Back-side processing poses tough challenges for GaAs

Henry Hendriks, Bharat Patel, Jim Crites and **John Moore** explore the challenges of back-side processing and the developments under way to turn wafer thinning, via hole etching and back-metal deposition into high-yield and high-throughput processes.

Back-side processing of GaAs wafers includes all of the manufacturing process steps beginning just after final front-side electrical test through to die separation and packaging. Detailed reviews of GaAs wafer back-side process flows have recently been published (H Hendricks *et al.*; L Klingbeil *et al.*; C Varmazis *et al.*). The back-side process flow of a typical GaAs fab can be separated into two major branches. The first branch is for GaAs die that do not require back-side via holes or metal. The main process steps involved are wafer thinning, dicing, die inspection and packaging. The second branch is for die that require back-side metal and, in most cases, through substrate via holes. This branch involves several additional process steps, including wafer/carrier mount, back-side photoresist mask definition, via hole etch, photoresist strip, oxygen plasma clean, seed layer deposition and electroplating.

The yield at back-side is crucial to the success of a GaAs fab, as a considerable investment has already been made in front-side processing. Also, major challenges exist in scaling up from 4 to 6 inch diameter wafer platforms. Fab equipment vendors over the past couple of years have taken notice of the growth in demand for GaAs-based devices for wireless applications, and they have started to address some of the tool deficiencies that previously existed in a few of the main back-side process steps. In the current market conditions fab process engineers and managers are carefully reviewing cost-of-ownership models of tools, while at the same time investigating the use and compatibility of innovative materials and unique process designs.

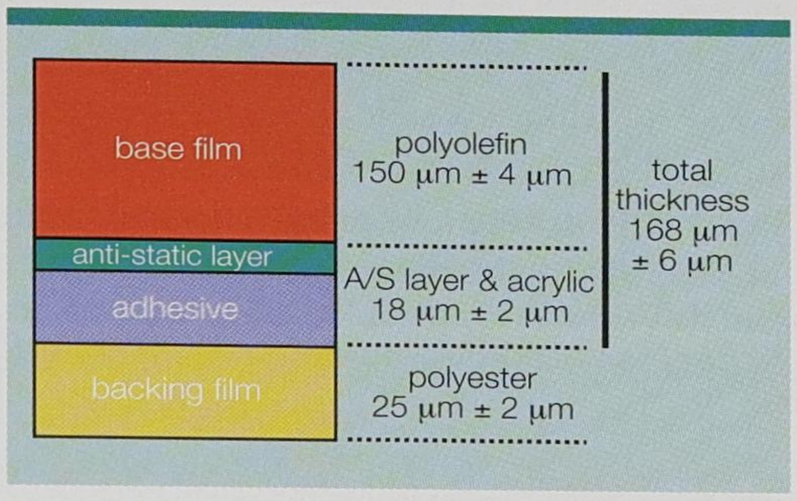


Fig. 1. A cross-section of Ultron Systems' ultraviolet anti-static tape.

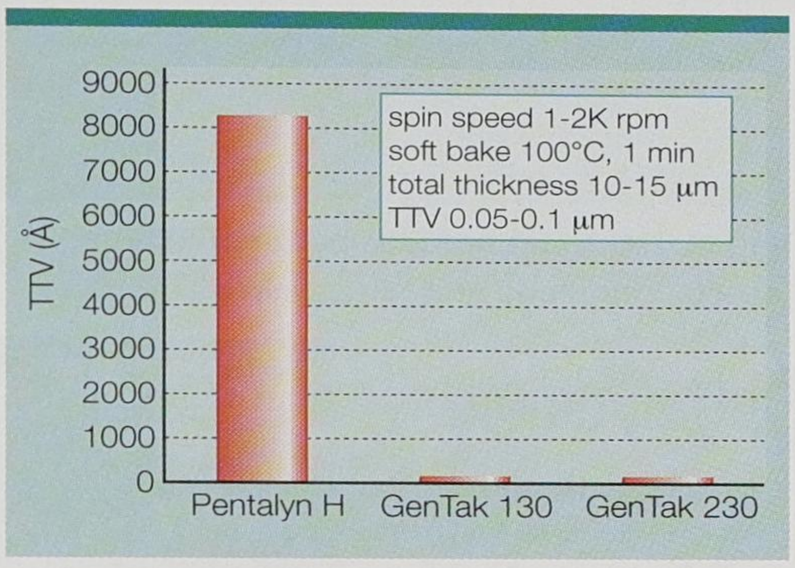


Fig. 2. The total thickness variation (TTV) of three cured spin-on adhesives.

This attention to back-side processing will certainly result in creating simple and robust developments that can be easily ramped during the next market rebound.

Process flow for thinning on tape

For 6 inch diameter wafers that do not require vias and back-metal, an ultraviolet (UV) back-grinding (BG) tape is generally used to protect the wafer front-side (figure 1). If the wafers have air-bridges, a thick photoresist can be applied to protect them during the tape mount and subsequent thinning steps. For high-volume manufacturing, an automatic wafer taper and de-taper with a UV exposure module are typically used (P Heinze, J Muller *et al.*). On UV exposure the adhesive layer strength of the tape is reduced to between 1% and 5%. The UV BG de-tape step should be carried out after the thinned wafers have been mounted on dice tape frames, so that thinned wafers are continuously supported by tape base film from the grind-through dice steps. Wafer tape system vendors are developing automated tools that combine the UV BG de-tape step with the dice tape frame mount step, which are targeted for smart card applications and may soon be available for use on 6 inch GaAs wafers. Some GaAs fabs have recently shown that 6 inch wafers with UV BG tape can be thinned with high yield to a target thickness range of 250–125 µm.

An automated single-wafer/dual-spindle grinder is used to perform most of the wafer thinning, which is followed by a post-grind wet etch or polish to remove the grinding damage layer. The dual-spindle grinder performs a fast, bulk, rough grind followed by a slow, thin, fine grind to achieve high throughput and to minimize the thickness of the grinding damage layer. A spray etch or polish is typically done after the grind to remove the grinding damage layer. Some wafer-thinning vendors offer a single wafer spray etch or polish module as an option for the automated wafer grinder system.

Process flow for vias and back-metal

For wafers that require vias and back-metal, the wafers can be thinned to between 100 and 20 µm. This requires the wafer to be mounted on a carrier using a high-temperature wax, thermoplastic adhesive or heat release tape. Liquid thermoplastic adhesives can be applied using a coat and bake track while dry-film adhesives can be applied using a dry-film vacuum laminator. Perforated sapphire carriers are currently used for 6 inch wafer processing. However, new automated wafer/carrier mount and demount tools may allow for the use of non-perforated carriers. Doped borosilicate glass carriers with a thermal coefficient of expansion close to that of GaAs are being considered as a less expensive alternative to sapphire with a potential cost saving of up to several hundred dollars per carrier.

Maintaining substrate planarity and a tight total thickness variation (TTV) is crucial during wafer-to-carrier mounting, especially when trying to achieve very low target thickness. Liquid spin-on thermoplastic adhesives tend to offer tight TTV, although variations do exist depending on the product used (figure 2). Pentalyn H, a customer's spin-on prepared with resin from Hercules, and GenTak, a

ready-to-use dual polymer system from General Chemical Corporation (GCC), were both spun and baked onto 6 inch GaAs wafers for a 10 μm target thickness and were shown to have a TTV of nearly 10% and 0.03% respectively. GenTak is available in a variety of viscosities, offering flexibility in the application to wafer front-side surfaces with a range of topography and thickness requirements (figure 3).

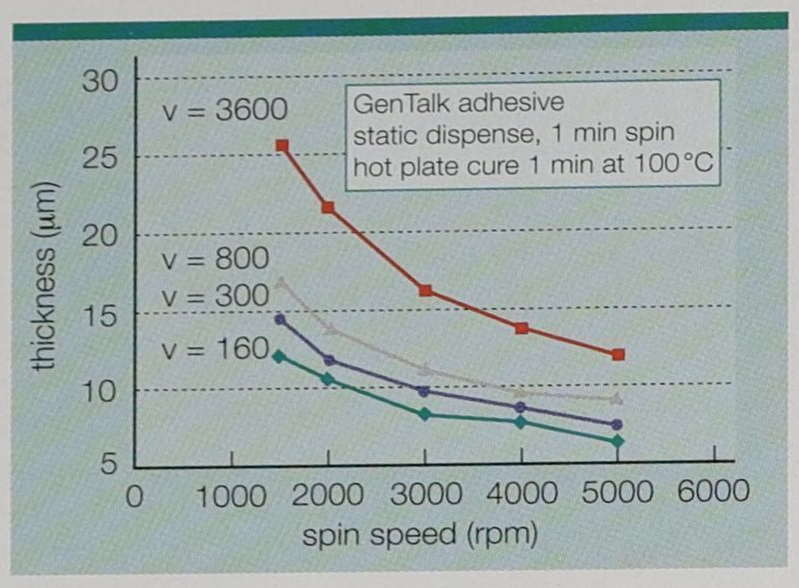


Fig. 3. Spin curves for several different values of viscosity (v) of GenTak liquid adhesive.

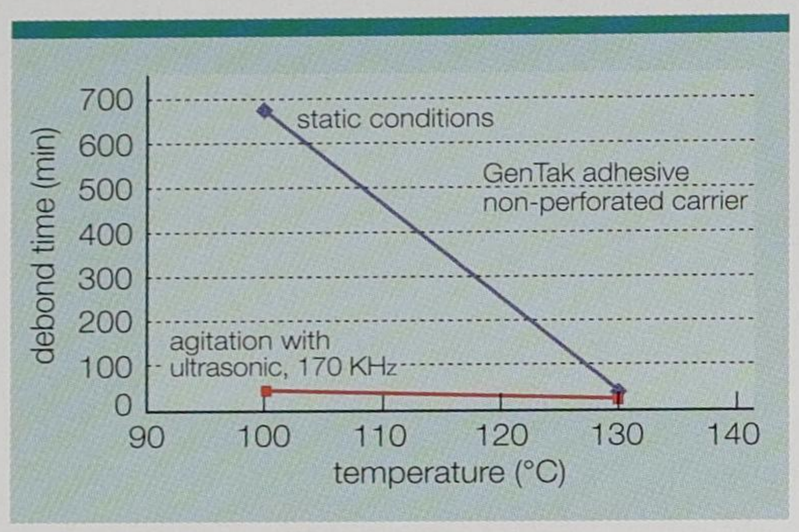


Fig. 4. Demount process parameters for static conditions and ultrasonic agitation.

Via hole etch and metalization

High-density plasma etch tools based on inductively coupled plasma (ICP) and dual frequency enable single 6 inch wafer via etch processing with high throughput, even for individual source vias (ISVs) which fit within 30 μm front-side source pads of power FET devices. This subsequently allows better heat conduction away from the hot active regions of the device. For high-aspect-ratio ISVs, long-throw or collimated sputter deposition may be required to ensure conformal seed layer deposition through the vias. Some 6 inch fabs with ISV capability have gone to a cluster platform with individually configured chambers. However, for fabs with less stringent via aspect ratio requirements, an automated batch sputter system can be used for seed layer deposition.

Wafer electroplating systems with pulse capability and carefully engineered solution circulation, such as fountain or submerged eductor-type platforms, are being used to deposit a conformal thick gold layer (3–8 μm) onto the back-side surface and through the vias. If the die are to be attached to package carriers for module assembly using a high-thermal-conductivity epoxy, then a solder-stop layer inside the vias is unnecessary. If the die are to be attached using Au-Sn eutectic solder preforms, then a solder-stop metal that readily oxidizes, such as Ti, TiW, Ni or Cr, needs to be deposited by either sputtering or plating inside the vias to prevent solder from blowing out the front-side metal pads.

A photolithography/wet-etch process is typically used to clear the solder-stop from the back-side metal plane to minimize voiding at this interface during the die-attach step. For large via openings at the back-side surface, the thick, positive photoresist flows into and fills the via during the dispense step. This enables a flood exposure and develop process to be used after back-side dicing streets have been defined saving one contact mask step. During the resist bake step, it is possible for some solder-stop metal to diffuse slightly into the thick gold layer along grain boundaries. This small concentration of diffused metal can later oxidize and create voiding problems at the solder die-attach step. A quick fix is to implement a short gold wet etch (potassium iodide or cyanide based) to lift off the solder stop metal embedded in the grain boundaries. Finally the resist mask can be wet stripped.

With recent advances in robotics, vendors can now offer fully automated pick and place, hot-forming gas die bonder platforms.

Thinned wafer demount and dicing

The thinned wafers can be demounted from the perforated carriers utilizing specially designed demount cells and a multi-bath solvent system at elevated temperature with agitation. BPS Technologies has recently introduced a semi-automated solvent hood with special vacuum holders to handle the thinned wafers after the carrier has been released from the wafer. The thinned wafers are subsequently released from the vacuum holders into a special cassette while they are submerged in liquid. EVGroup and BLE have recently introduced automated wafer demount tools with special thin wafer handlers that can be used with non-perforated carriers. Also, GCC has shown that it may be possible to demount and clean 6 inch thinned wafers from non-perforated carriers in just a few minutes using GenSolve 500. When heated to elevated temperatures with high-frequency, low-power ultrasonic agitation, wafers can be demounted without damaging front-side gates and air-bridges (figure 4).

Dicing of thinned wafers less than or equal to 100 μm thick may require the use of UV dice tape, especially if the wafers are to be sawn. The structure of UV dice tape is very similar to that of UV BG tape (figure 1, pXX). On UV exposure, which is recommended within 24 h after the wafer is mounted, the adhesive strength of the tape is decreased by almost two orders of magnitude, enabling thin, fragile die to be picked and placed from the dice tape.

Au-Sn eutectic solder die attach

Most GaAs device die with back-metal are attached to packages or module carriers using conductive thermoset epoxy. However, for high-power devices a Au-Sn eutectic solder with a melt temperature of 280 °C may be needed to satisfy the thermal conduction requirements between the active region of the device and the heat sink. With the recent advances made in robotics, vendors can now offer fully automated pick and place, hot-forming gas die bonder platforms. For high power devices that need to be die attached using Au-Sn eutectic solder, a smaller die size is desired to achieve a more robust die attach process. A void-free die attach may be required to ensure the adequate thermal conduction of heat away from the power amplifier active regions. For the pick and place die bonders, larger die typically require a higher forming gas flow to promote an increased heat-transfer rate and to reduce voiding between the solder preform and die back-metal surface. Also, a programmed scrub is needed to break down the tin oxide on the preform prior to the forming gas flow.

C-mode scanning acoustic microscopy (C-SAM) can be used as a periodic screen test to check for excessive voiding between the die and carrier after die attach, and it is also useful in optimizing a die-attach process. The package or module needs to be submerged in DI water, so the test can be destructive if it is non-hermetically sealed. C-SAM images of three Au-Sn eutectic solder preform die

attachments done with a pick and place, gas die bonder are shown in figure 5. The first die attach was essentially void-free because tiny voids occurred only at the vias, which are lined with solder-stop metal. The second die attach had a few large voids as a result of residual solder-stop metal on the die back-metal surface. The third die attach showed a very large void due to the partial wetting of the preform, which was traced to misalignment of the forming gas nozzle.

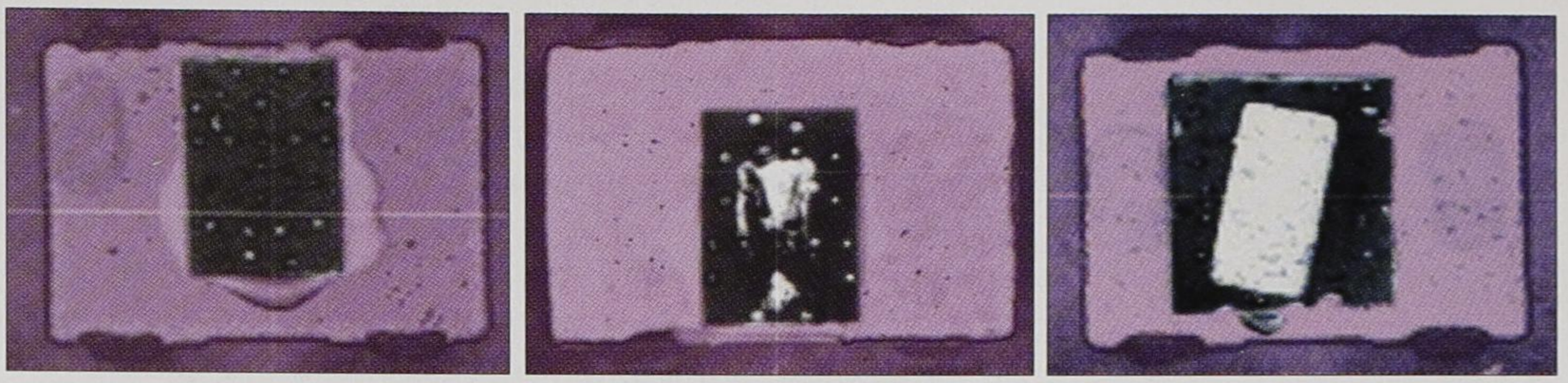


Fig. 5. C-SAM images of void-free and void-problem Au-Sn solder preform die attach. Voids are white. Left to right: good die attach; residual solder-stop metal; gas nozzle mis-aligned.

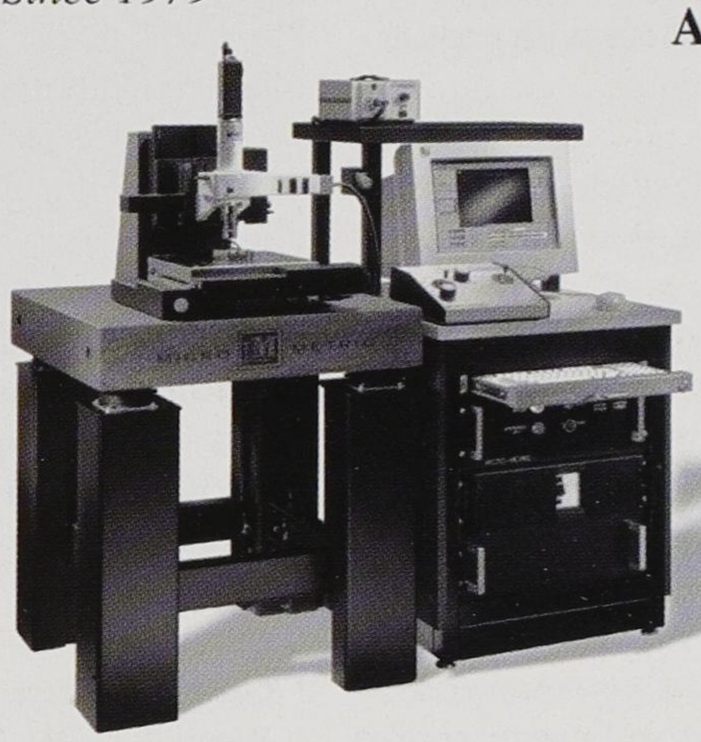
Depositing Au-Sn directly onto the back-side of the wafer is being explored as an alternative to the use of Au-Sn eutectic preforms stamped to accommodate specific die sizes. The Au and Sn can be deposited either sequentially or jointly to try to achieve the eutectic composition needed for die attach. Also, a Au "sealcoat" layer can be deposited to prevent the Sn from oxidizing before or during the die attach. This should lessen the demands on the scrub and hot forming gas flow steps to reduce surface oxides. The eutectic Au-Sn preform thickness is typically about 25 μm, necessitating the use of a solder-stop layer inside the vias. The deposited Au-Sn layer or total composite layer thickness can be tailored to obviate the need for a solder-stop layer. With the recent advances made in wafer electroplating tools, depositing Au-Sn directly onto the wafer back-side may shortly move from the R&D phase into manufacturing. ●

Further reading

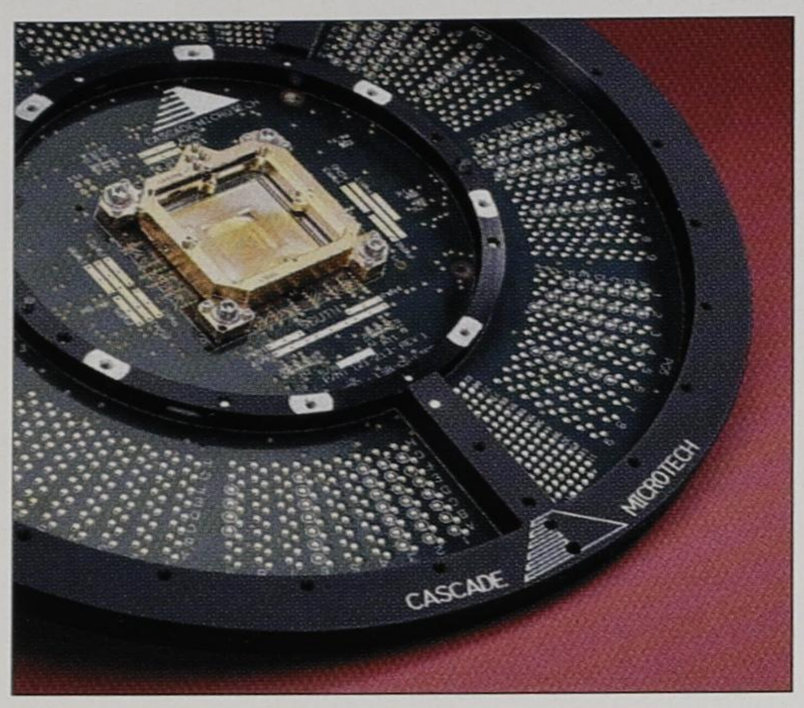
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Pyramid probes cut the cost of wafer tests



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"Our Pyramid Probe cards provide value through our patented MicroScrub capability, along with the photolithographic thin-film process," said Dean Gahagan, director of marketing. "The fine-pitch capability enables semiconductor manufacturers to test devices with pads as small as 0.1 mm."

Contact Ellen Payne, Cascade Microtech, 2430 NW 206th Avenue, Beaverton, OR 97006, USA
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Fax +1 503 601 1002
E-mail ellen_payne@cmicro.com

Resists launched for lift-off processing

MicroChem Corp (MCC) has released a range of resists for the lift-off processing of GaAs, InP and other III-V discrete and MMIC devices, including HBTs, PHEMTs, FETs and VCSELs. Formulations cover a broad range of film thicknesses to permit the clean lift-off of metal deposition layers of thickness less than 5 nm to 2.5 mm and above. Used in bi-layer resist processes, lift-off resists produce sub-micrometer profiles, do not intermix with g-line, i-line and deep-UV resists, and alleviate the need for an exposure step.

"Bi-layer resist processing is relatively new to the compound semiconductor community, but has a long, successful history in thin-film-head manufacturing, where it dominates the lift-off market," said Scott Heidemann, MicroChem's sales and marketing manager.

"While the lift-off resist bi-layer process requires an additional coating step, the pay-off is in having control of the re-entrant sidewall profile, which is paramount to clean lift-off processes. Lift-off resists also leverage the advanced i-line and deep-UV resists and can run high-volume, high-yield processes at 0.35 and 0.25 mm respectively, which is completely unobtainable with other lift-off technologies."

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Fax +1 617 965 5818
E-mail mcc@microchem.com

New lapper/polisher increases throughput

Logitech's new LP600 lapping machine is designed for automated plate control and an increased capacity in the precision lapping/polishing of semiconductor wafers, optoelectronic and DWDM components, and optical fibers. The abrasive auto-feed system enables control of the abrasive while lapping and polishing wafers up to 6 inches in diameter.

Consisting of four workstations, the system features a 22 inch plate capable of accommodating up to four PP5, PP6 or PP8 jigs. The PP8 jig allows heavier loading for the higher throughput required in small batch production environments.

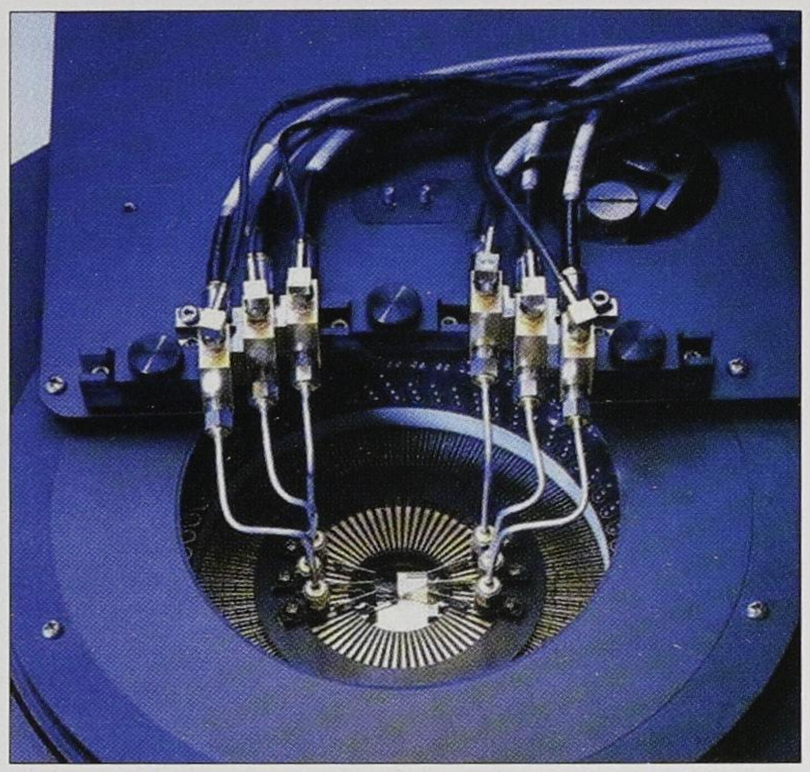
Contact Keith Torrance, Logitech Product Group, Struers Inc, 810 Sharon Drive, Westlake, OH 44145, USA
Tel. +1 440 871 0071
Fax +1 440 871 8188
E-mail info@logitech-us.com

Electrical and optical testers hit the market

While the rapid testing of semiconductor devices at GHz frequencies helps speed reliable products to market, DC parametric testing is still required in the form of separate DC and RF testers and probes.

Keithley Instruments' new S400DC/RF parametric tester is designed for probing RF and DC signals in communications and high-speed digital devices. Able to execute both types of test independently and in parallel, the system incorporates vector network analyser (VNA) and DC/RF probe-card technology. Three configurations are available including single DUT testing at up to either 20 GHz or 40 GHz, and multiple DUT testing at up to 20 GHz.

The company has also introduced an integrating sphere in addition to its L-I-V (light intensity-current-voltage) testing systems. The sphere simplifies the testing of LEDs and other optical components by eliminating common light intensity measurement problems related to detector alignment, beam profile, polarization and

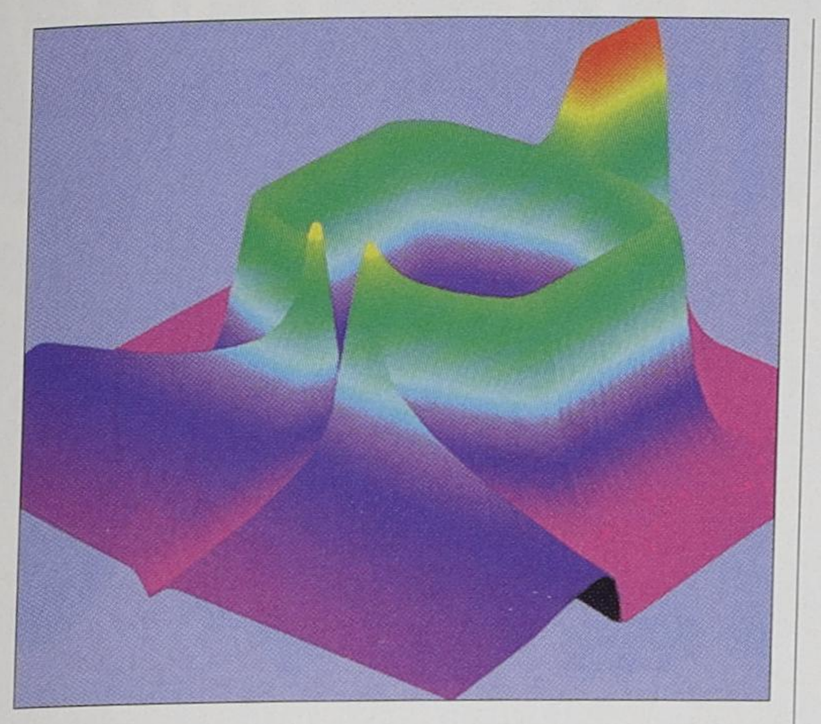


back reflection. In combination with Keithley's 2500 dual photodiode meter, the sphere facilitates the direct measurement of optical power in Watts.

Contact Ellen Modock, Keithley Instruments Inc, 28775 Aurora Road, Cleveland, OH 44139-1891, USA
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RSoft upgrades its simulation software

RSoft has upgraded its BeamPROP simulation and CAD software for the design and analysis of photonic waveguide devices and circuits. Version 5.0 allows circuit designers to break simulations down into zones, a process which until recently required a single set of parameters and resulted in lengthy computation times for complex problems. Each simulation region



then allows specific parameters to be applied to localized regions, decreasing the computer resources required.

Another addition to BeamPROP is the ability to orient the angle and end-faces of different objects arbitrarily for more accuracy and flexibility in mask layout. Other features include the generation of photonic bandgap structures and non-linear capabilities for 3-D simulations.

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Fax +1 914 736 9823
E-mail andrea@rsoftinc.com

OAI launches table-top align and expose tool

A mask alignment and UV expose system is available from OAI. Applications of the table-top system include II-VI and III-V device fabrication, solar cells, SAW devices, thin-film devices, MCMs and MEMS systems.

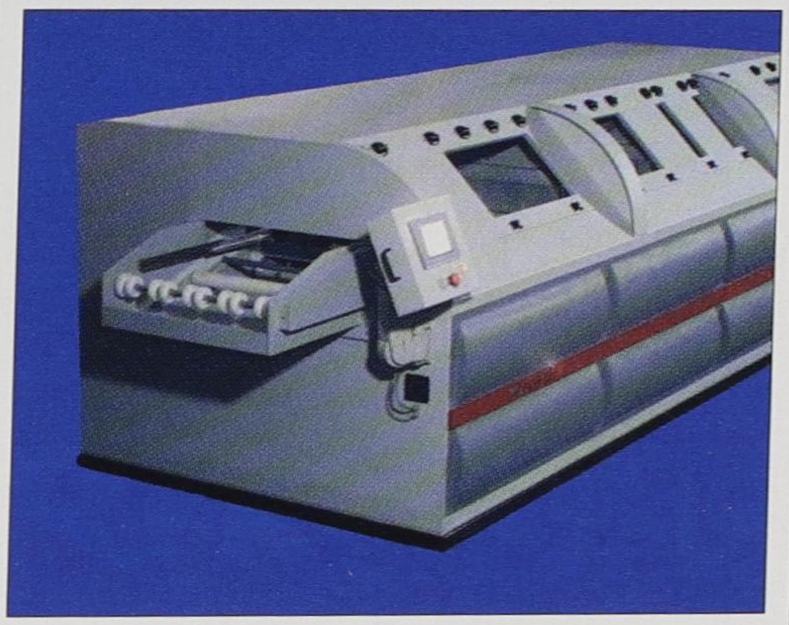
Targeted at development labs, universities and start-up operations, the company's low-cost alignment tool offers printing performance, and features interchangeable mask holders and chucks for substrates up to 8 inches in diameter . The light source provides collimated UV light in the near or deep UV using lamps ranging from 200–2000 W, and a sensor and optical feedback loop ensures constant intensity of exposure to ±2%. While manually operated, the 200 series alignment system tolerates a zero alignment shift when moving to the expose position.

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E-mail sales@oainet.com

Austin's new system cleans as well as dries

Austin American Technology has introduced an automated cleaning and drying system based on its HydroJet Inline Cleaner series. The new unit efficiently cleans and dries delicate flip-chip assemblies at in-line speeds.

Incorporating patented wet-and-dry isolation, the company's HydroJet cleaner also minimizes upstream contamination and improves the life and economy of the closed-loop resin beds. The patented dryer module removes 99.9% of rinse water from under flip-chip bonding schemes where the spacing approaches 1–2 mm at component stand-off, or at small heights up to



3.5 inches. These options are available in several systems with various footprints, including 12.7 ft for the HydroJet I and 16.7 ft for the HydroJet III.

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Pre-heated modules transfer heat uniformly

Vitronics Soltec's new Wavesolder unit is designed for solder fluxes that are formulated with an alcohol solvent, but the flux modules are also suited to applying a fine deposit of VOC-free water-based flux. In the new unit the preheating modules transfer heat at a uniform temperature, increase the topside board temperature and evaporate the water in the flux.

The standard corrosion-resistant coated impellers are also compatible with new lead-free solder alloys. The patented SmartWave has the ability to force the solder to flow into the top of the PCB's through-holes, and filling all the joints – even those with alloys such as SnCu that have marginal solderability.

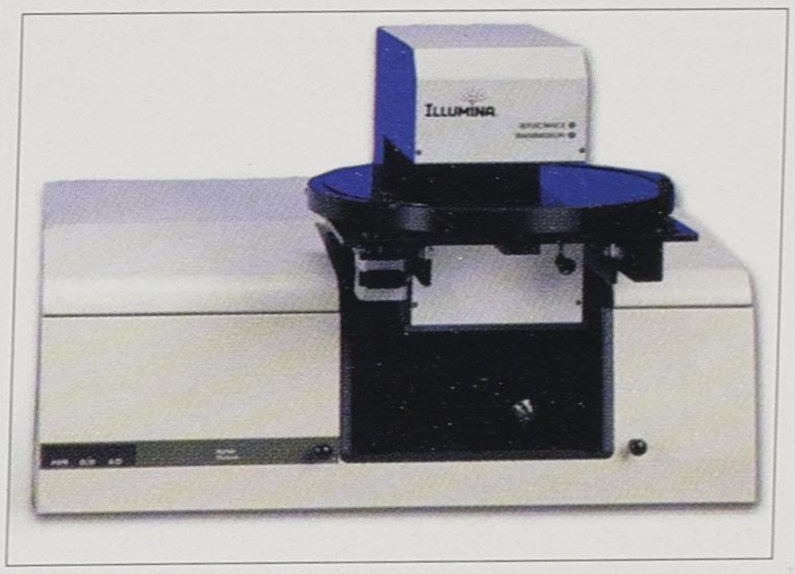
Contact Andre Myny, Vitronics Soltec BV, Karolusstraat 20, 4903 RJ Oosterhout, The Netherlands
Tel. +31 162 48 000
Fax +31 162 483253
Web www.vitronics-soltec.com

Illumina sheds light on wafer parameters

Accent Optical Technologies has released Illumina, a non-contact FTIR metrology tool for characterizing wafer parameters such as epitaxial layer thickness, refractive index and doping concentration. Applications include PIN and avalanche photodiodes, IR lasers, VCSELs, LEDs and waveguides. Key benefits include its high throughput, a small footprint and a thickness-measurement range from less than 0.1 mm to more than 200 mm.

Accent also offers the option of cassette-to-cassette handling for high-volume applications, in addition to cryogenic measurement and an IR microscope accessory for R&D or failure analysis.

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Fax +1 541 318 1966
E-mail ejewell@accentopto.com



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Taking stock of terrorism

Compound semiconductor stocks are hammered as the US markets experience their worst week since the Great Depression. But the wireless and defense industries may offer some comfort.



The decline in the US airline industry may offset any benefits from increased spending on defense.

First the good news. History indicates that the US Stock Market is adept at absorbing shocks to the system. "Disasters leave but a small footprint on the markets" says Mark Hulbert, writing in the *New York Times*. In fact recent scholarly research shows that share prices often climb in the six months after a crisis begins.

And now the bad news. The decline in the market in the week following the 11 September terrorist attack on New York and Washington is almost without precedent. The Dow Jones industrial average fell 14.3%, its worst weekly decline since the Great Depression, and the NASDAQ composite fell 16.1%. When the week was over, three years of gains had been wiped out, with most widely traded stocks having sunk back to levels not seen since 1998, as investors large and small fled the equities market and sought shelter in cash, gold, bonds and other more conservative investments.

To analyse how the compound semiconductor-related companies fared in this hostile environment, I've drawn up a simple "compound semiconductor index". It consists of all of the companies I discuss here in "Portfolio" that are traded in the US (i.e. all those in the table on page 88 except for the European companies). The companies are weighted according to their market capitalization, so that changes in share price for the largest companies in the group (Agilent, JDS Uniphase, Agere, RFMD) have more impact on the index value than do movements among the smaller companies.

Six other indexes were picked for comparison: the Dow Jones industrial average, the NASDAQ composite, and four sector indexes: the AMEX Networking Index, which includes 15 of the largest network equipment stocks such as Nortel, Alcatel, Lucent, 3Com, Cisco and Ciena; the Philadelphia Wireless Index, which includes equipment makers like Nokia, Ericsson and Motorola as well as service providers; the Philadelphia Semiconductor Sector Index, which comprises 16 of the most widely held semiconductor-related stocks; and the SEMIndex, which is made up of 65 global, public companies serving the semiconductor equipment and materials markets.

The wireless sector

The 17% decline in the compound semiconductor stocks was in line with the drop in the Dow Jones industrial average and the NASDAQ composite, as shown in the chart above. But because of the relative strength of the wireless sector, the compound semiconductor index fared somewhat better than the two broader semiconductor indexes, which are largely driven by the computer industry.

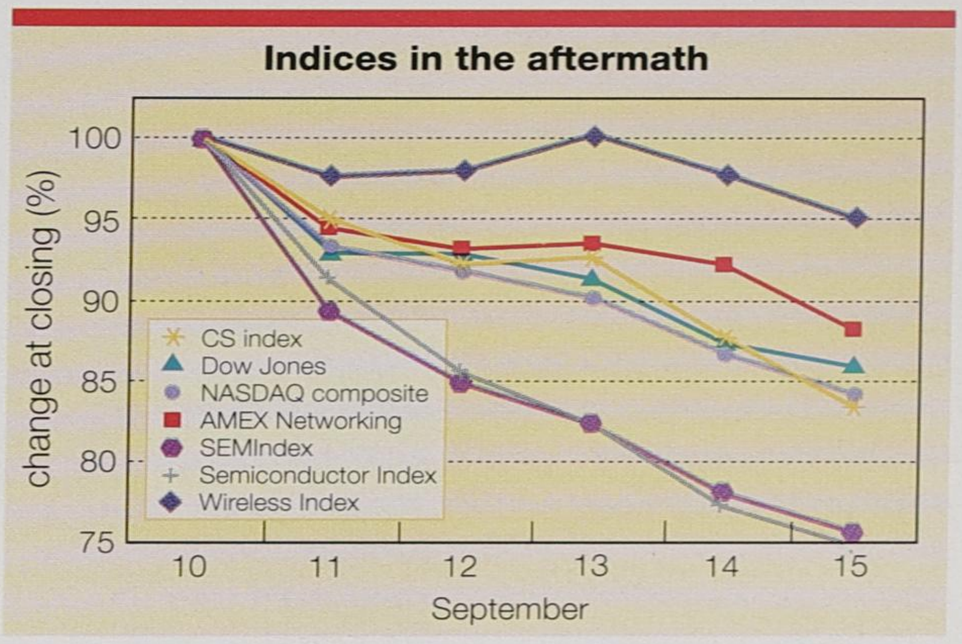


Chart shows the drop in stock prices following the terrorist attack on the US on 11 September 2001.

Wireless penetration rates

Country	*Mobile-owning population*
Finland	>75%
Sweden	>75%
Italy	>70%
United Kingdom	>65%
Hong Kong	>65%
Taiwan	>65%
Germany	~60%
South Korea	~55%
France	~50%
Japan	~47.5%
Australia	>40%
United States	~37.5%

Source: Red Herring, eMarketeer

Less than two weeks after the attack it is fairly evident that more cell phones are being sold in the US, although this may be a temporary blip. The "wired" networking stocks also fared somewhat better than the market as a whole, but unfortunately almost the only explanation that can be offered is that this sector was already so beaten down that it had less far to fall.

The percentage of the US population who own mobile phones is one of the lowest among developed nations – less than 40% (see table above). Finland passed the 40% mark in 1997. The US has traditionally seen the cell phone as a business tool for some and a consumer gadget for many, but several commentators now believe that more Americans will see them as a "must have" for reasons of personal safety and private communications. The Reuters News Service is reporting that US retailers sold a month's worth of phones in the week after 11 September. >>

The decline in the market in the week following the terrorist attack on New York and Washington is almost without precedent.

Market overview

Company	Symbol	Closing price on 21 Sept	52-week low–high	Market cap*	P/E ratio**
GaAs IC companies					
Alpha Industries	AHAA	23.95	13.0625–55.3750	1.053B	53.27
Anadigics	ANAD	13.22	10.5000–27.2500	400.8M	N/A
Celeritek	CLTK	11.76	9.8125–50.0625	141.5M	N/A
Conexant	CNXT	8.31	6.9000–49.7500	2.096B	N/A
Endwave	ENWV	0.90	0.8400–20.6250	31.8M	N/A
Multilink	MLTC	6.20	6.0000–18.4000	579.8M	N/A
RF Microdevices	RFMD	19.89	8.7500–38.1875	3.279B	N/A
Sirenza Microdevices	SMDI	4.15	3.9100–60.2500	122.0M	14.30
TriQuint	TQNT	18.08	10.2500–61.5625	2.345B	27.57
Vitesse	VTSS	8.75	7.9400–93.2500	1.667B	N/A
Opto companies					
Agilent	A	20.15	18.0000–68.0000	9.282B	21.92
Agere	AGRa	3.25	3.1000–9.5000	5.314B	N/A
Alcatel Optronics	ALAO	4.99	4.0400–71.7500	82.3M	3.99
Coherent	COHR	25.75	25.0000–79.8125	728.6M	9.78
Cree	CREE	14.52	12.2100–64.1250	1.059B	41.35
JDS Uniphase	JDSU	5.36	5.1200–111.1875	7.055B	N/A
Stratos Lightwave	STLW	4.27	3.9200–40.5000	273.7M	N/A
Uniroyal Technology	UTCI	3.22	2.7100–17.5000	90.2M	N/A
Semiconductor materials and equipment companies					
ATMI	ATMI	17.29	14.3750–32.7300	524.5M	22.47
AXT	AXTI	10.20	9.9000–46.4375	227.7M	7.82
Emcore	EMKR	10.48	10.0000–55.3750	361.7M	N/A
Kopin	KOPN	7.30	4.0000–24.9375	475.1M	N/A
Tegal	TGAL	1.35	1.0500–4.5000	17.0M	16.75
Trikon	TRKN	8.00	6.9600–18.5625	102.5M	3.83
Veeco	VECO	21.81	19.9000–117.0000	541.0M	16.48
European companies (currency data in €)					
Aixtron	AIX	15.70	15.61–169.00	1.01B	120.70
Bede	BED	1.99	1.83–3.39	63.45M	N/A
Filtronic	FTC	2.35	1.65–7.82	193.8M	N/A
IQE	IQE	1.53	1.53–4.34	261.9M	74.63
Picogiga	PICO	2.94	2.60–36.50	19.0M	N/A
Riber	RIBER	3.00	2.66–31.45	56.16M	N/A
ST Systems	STRS	1.94	1.95–3.91	62.50M	15.88

*Market capitalization = # shares × current share price.; **Price/Earnings ratio = current share price ÷ (income for the last four quarters ÷ # shares).

Even before the tragedy the outlook was improving in the wireless sector, with several firms on track to report solid third-quarter results. On 10 September Nokia announced that it would meet its earnings targets for the quarter, despite the fact that revenue would fall about 5% compared with the year-ago period. Analysts were cheered because this indicated that Nokia was not giving into temptation to slash handset prices in response to the global slowdown in sales. Nokia shares were rising fast in before-the-bell-trading on Wall Street before everything came to a halt on 11 September.

Unfortunately, it appears that Nokia is the only major mobile-phone maker that can produce phones profitably. Its 35% market share is nearly double that of Motorola, the number-two manufacturer. In the week before Nokia's announcement both Motorola and Ericsson, the third-largest player in the handset market, gave more pessimistic assessments of their prospects for the third quarter.

On the same day as the Nokia announcement RF Micro Devices went even further than its biggest customer and announced that its third-quarter results would significantly exceed previous forecasts. The company increased its estimated sequential revenue growth from 10% to 30%, and said that it would break even instead of making a loss of around $5 million. It attributed the turn-around to "increased order activity and revenue growth from multiple customers and across all major air-interface standards."

Along the same lines, TriQuint reported that it would hit its third-quarter objective of 30% sequential growth, climbing to $80 million in revenue. Anadigics forecast

Mixed outlook from Kopin and AXT

Two US companies, Kopin and AXT, have announced rather different expectations for their third-quarter revenues. Kopin, a manufacturer of HBT epiwafers and active matrix liquid-crystal displays, has revised its figures upwards. The company now anticipates revenue for the quarter ending 30 September 2001 to be $11.6–12.0 million, a sequential growth of more than 25%. The epiwafer product line accounts for $5.1–5.3 million of this. John Fan, Kopin's chairman and chief executive officer (CEO), said, "We have seen continued orders from our newer HBT customers, coupled with a resurgence of business from some of the larger wireless customers with whom we have long-term relationships."

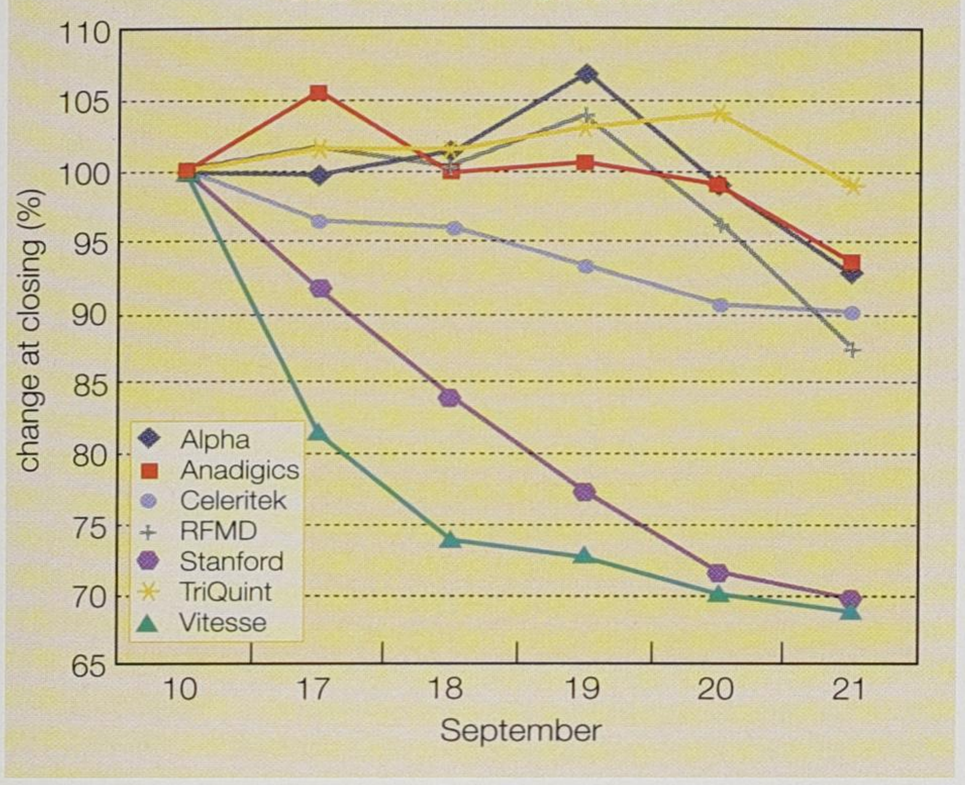
AXT, a manufacturer of compound semiconductor substrates and optoelectronic devices, has also revised its third-quarter forecast. Previous revenue estimates for the period were $26–$28 million, but revenue is now expected to be $22–23 million. AXT blames a weaker demand for GaAs and InP substrates than expected, with the same occurring for optoelectronic products. The company expects to record a loss for the quarter of $0.04–0.06 per share.

Looking ahead, AXT expects a substantial decline in substrate revenue compared with the revised third-quarter figures. However, president and CEO Morris Young said, "AXT has implemented a range of measures to reduce costs and improve efficiency. We believe that our market-leading position in InP substrates and larger-diameter GaAs substrates as well as significant advances in our optoelectronics division will position us well for renewed growth when the economy begins to recover."

Jon Newey

Less than two weeks after the attack it is fairly evident that more cellular phones are being sold in the US.

The value of defense



GaAs companies that have ties to the defense industry held up the best as the market declined.

Major US defense contractors

Company	*Change in share price 10–21 Sept*
Raytheon	+37%
Northrup Grumman	+21%
General Dynamics	+11%
Lockheed Martin	+10%
TRW	–17%
General Electric	–20%
Boeing	–31%
United Technologies	–36%

Source: Morningstar, Yahoo

a wider loss in the current quarter, but on revenue greater than expected: although sales are picking up, customers are buying items with lower profit margins.

Back to defense?

Some defense contractors also did well in the aftermath of the attacks. The table above shows eight of the top 10 companies that received the largest dollar volume of prime defense contracts from the US Defense Department in 2000, according to Morningstar. (The two missing companies are Litton, which was acquired by Northrup Grumman, and Science Applications, which is privately held.) The table hints at how difficult it is to find a single index that provides a helpful measure of the sector's performance, because of the close ties between the defense and aerospace industries. For companies like Boeing, United Technologies and General Electric that have a foot in both camps, the sharp decline in the US airline industry may offset any benefits from increased defense spending. And TRW seems to be being dragged down by concerns about the auto parts industry.

Among the GaAs IC companies, TriQuint derives around 10% of its revenue from the defense industry, which is perhaps why it declined just 2%, in contrast with the other GaAs IC companies that were down 15% on average. Alpha's shares also held up fairly well. In fiscal year 2000 6.5% of its sales were defense-related.

However, one of the many uncertainties about a "war on terrorism" is whether it will result in the sustained increase in military spending that so benefited the GaAs industry in its formative years. This new war may be based on more small-unit, Green Beret or even James Bond-style actions than huge outlays on jets and missiles. Bad for the industry, perhaps, but probably better for mankind.

21–24 October
GaAs IC Symposium
Baltimore, MD, US
Web: www.gaasic.org

28 October – 2 November
Int'l Conference on Silicon Carbide and Related Materials
Tsukuba, Japan
Web: www.icscrm2001.gr.jp

29–31 October
10th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP 2001)
Cambridge, MA, US
Web: www.epep.org

12–15 November
Laser and Electro-Optics Society Annual Meeting (LEOS 2001)
San Diego, CA, US
Web: www.i-leos.org

26–30 November
MRS Fall Meeting
Boston, MA, US
Web: www.mrs.org/meetings

2–5 December
Int'l Electron Devices Meeting (IEDM)
Washington, DC, US
Web: www.his.com/~iedm

20–25 January 2002
Photonics West
San Jose, CA, US
Web: spie.org/app/conferences

7–8 February 2002
Strategies in Light (LED conference organized by Strategies Unlimited)
San Francisco, CA, US
Web: www.strategies-u.com

7–8 March 2002
Key Conference 2002: Compound Semiconductors in Communications
Key West, FL, US
Web: www.keyconference.com

11–15 March 2002
Int'l Symposium on Blue Lasers and LEDs (ISBLLED 2002)
Cordoba, Spain
Web: www.die.upm.es/research/

17–21 March 2002
Optical Fiber Communications Conference (OFC)
Anaheim, CA, US
Web: www.osa.org/mtg_conf/

18–20 March 2002
Int'l Symposium on Quality Electronic Design (ISQED)
San Jose, CA, US
Web: www.isqed.org

1–5 April 2002
MRS Spring Meeting
San Francisco, CA, US
Web: www.mrs.org/meetings/

8–11 April 2002
GaAs Mantech
San Diego, CA, US
Web: www.gaasmantech.com

16–18 April 2002
Semicon Europa
Munich, Germany
Web: www.semi.org/web/wexpositions.nsf

12–16 May 2002
Indium Phosphide and Related Materials (IPRM)
Stockholm, Sweden
Web: www.congrex.com/iprm2002

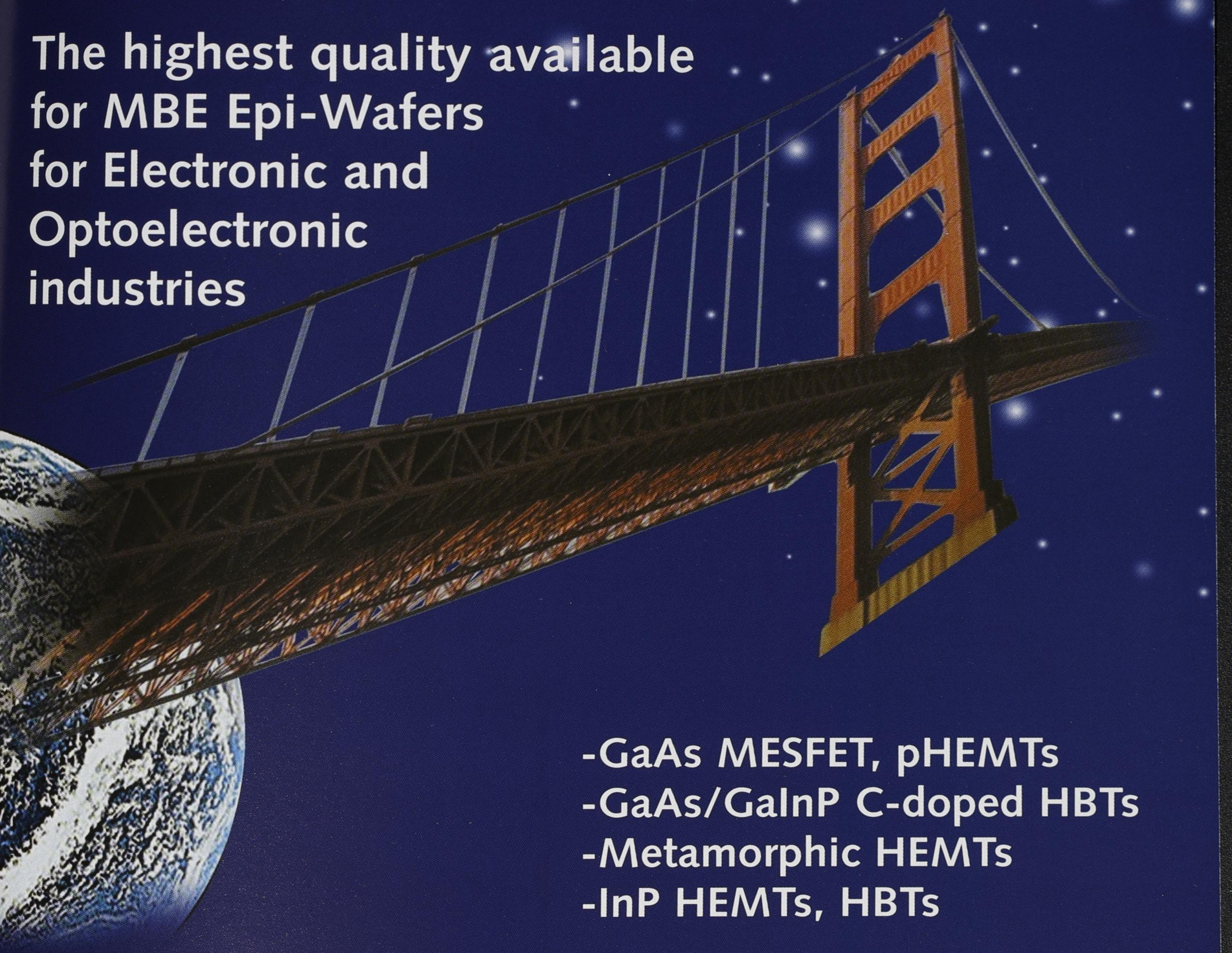
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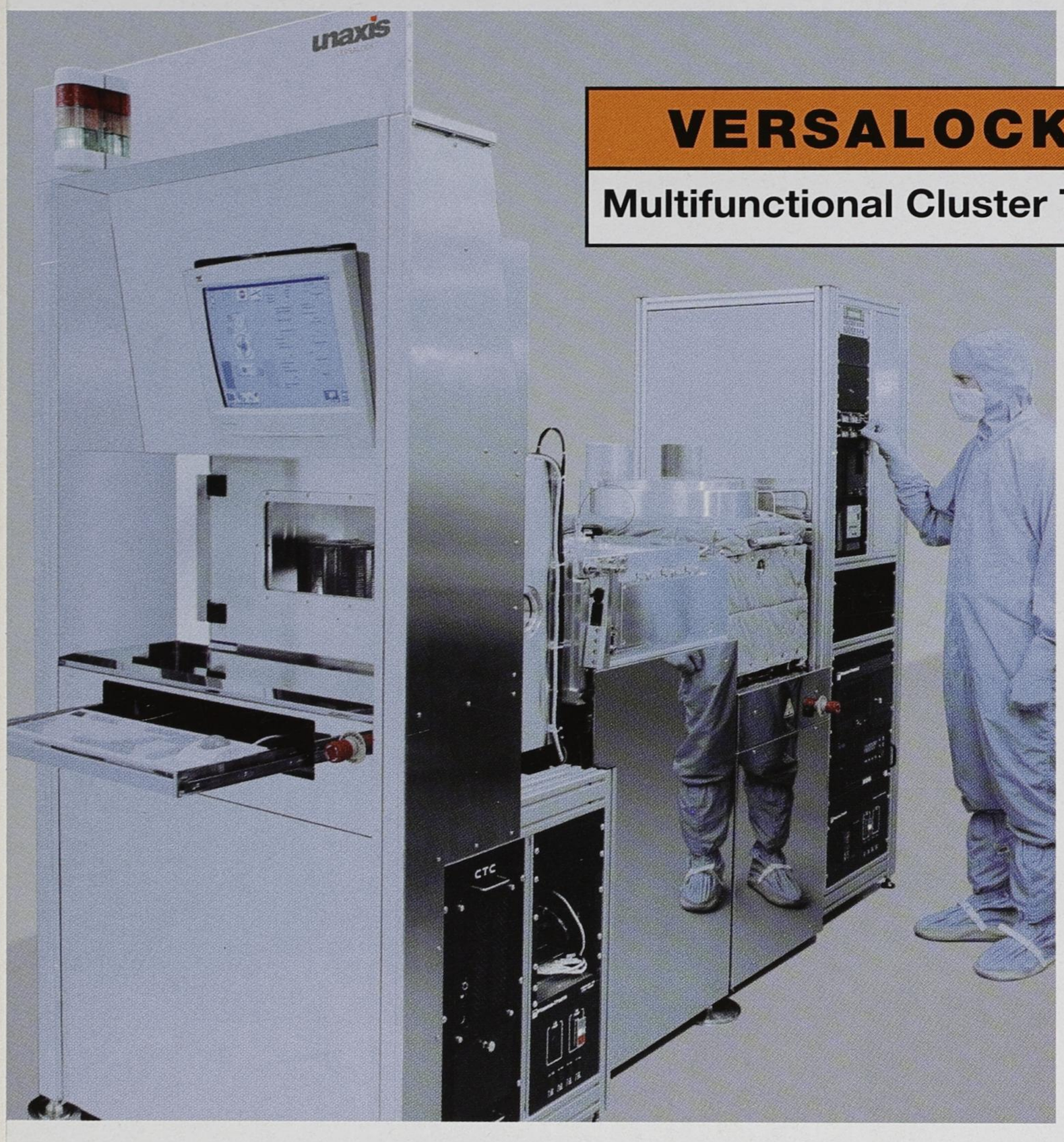
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VERSALOCK

Multifunctional Cluster Tool

With its impressive reputation in high volume manufacturing environments, the VERSALOCK® clustertool is setting milestones in plasma etching and deposition technologies. The proven legendary performance of the VERSALOCK® has been substantiated in a wide variety of applications, including:

- **MMIC Manufacture**
  GaAs Via Etching, Frontside Etching, Low Damage SiN Etching, InP Etching, Deposition of SiN
- **Optoelectronic and Communication Devices**
  Etching of InP, SiO_2, Si_3N_4, InSb, Polyamide, GaN, and SiC, Deposition of silicon-based insulators and SiC films
- **Photomask Fabrication**
  ICP Dry Etch of Chrome, MoSiON, and Quartz
- **M-RAM, GMR and TMR Read/Write Head**
  High Density Dry Etching, PECVD Deposition of Silicon based insulators
- **MEMS Devices**
  Deep Silicon Etching (Bosch Process), Deep Quartz Etching, Deposition of Silicon Dioxide and Silicon Nitride

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