COMPOUND SEMICONDUCTOR

Connecting the Compound Semiconductor Community

Volume 22 Issue 1 January / February 2016 @compoundsemi www.compoundsemiconductor.net

Ferrotec's Temescal Systems

Improving SAW & BAW evaporation

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

AIXTRON

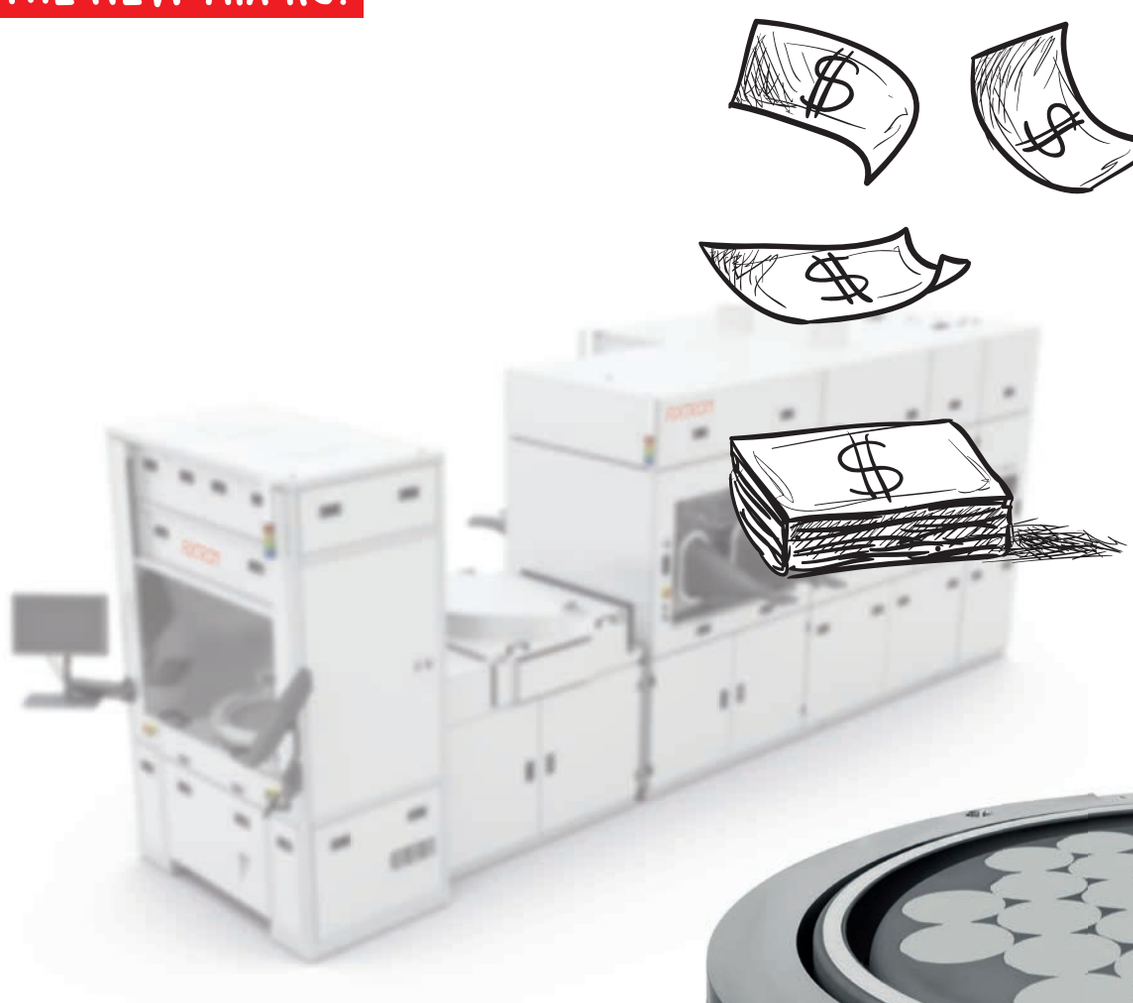
Our technology. Your future.

YOU THINK,

AIXTRON SYSTEMS SHOULD OFFER YOU THE BEST COST OF OWNERSHIP.

WE THINK THAT TOO.

THE NEW AIX R6.



DISCOVER THE NEW AIX R6.

Revolutionizing an industry is not about changing everything. It's about making the good even better. Introducing: The new AIX R6. It has everything you expect from the industry's technology leader plus **better usability, better throughput and better cost of ownership.**

AIXTRON SE · info@aixtron.com · www.aixtron.com

editorial view

by Dr Richard Stevenson, Editor

III-V logic: What's logical?

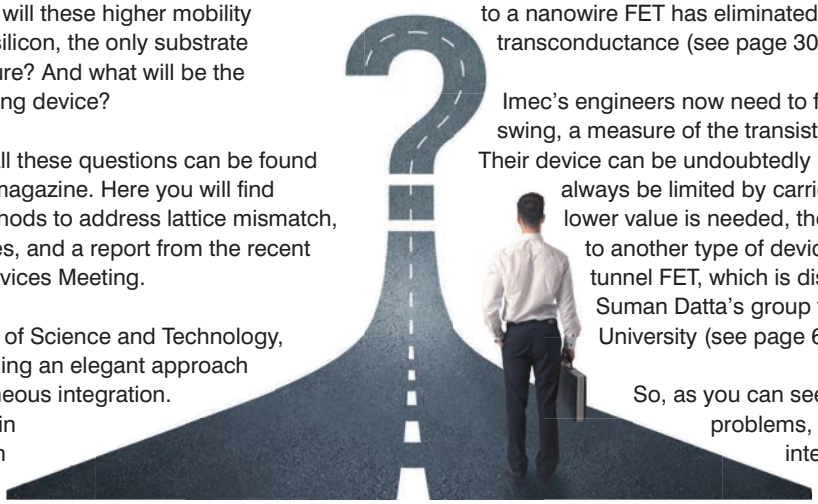
DURING the last decade there has been something of an explosion in the research of alternatives to the silicon MOSFET. This effort has been motivated by a widely accepted view that it will not be possible to maintain the march of Moore's law by simply trimming transistor dimensions. Although the demise of the silicon MOSFET is not imminent – it is believed that Intel's silicon finFET can be scaled to the 7 nm node – it will not be that long before we see the introduction of channels with higher mobilities, which will ultimately lower the power per transistor.

What is not clear is the nature of the devices that will emerge. What materials will be used in the NMOS and PMOS devices paired to form ICs? How will these higher mobility channels be formed on silicon, the only substrate suitable for IC manufacture? And what will be the architecture of the resulting device?

Options for addressing all these questions can be found within the pages of this magazine. Here you will find features on different methods to address lattice mismatch, novel device architectures, and a report from the recent International Electron Devices Meeting.

At Hong Kong University of Science and Technology, Kei May's group is pursuing an elegant approach to the issue of heterogeneous integration. GaAs nanowires, grown in patterned substrates with V-shaped grooves, are enabling high-quality buffer layers just 300 nm-thick (see page64).

The starting point for this approach is similar to that used by engineers at imec, who have previously formed III-V and germanium finFETs by growing material out of trenches. Although the III-V finFETs did not suffer from a high density of dislocations, thanks to annihilation at trench sidewalls, these transistors failed to deliver as good a performance as those grown on a native platform, according to values for transconductance – a measurement that reflects channel mobility. However, switching the transistor architecture to a nanowire FET has eliminated this shortfall in transconductance (see page 30).



Imec's engineers now need to focus on sub-threshold swing, a measure of the transistor's switching capability. Their device can be undoubtedly improved, but it will always be limited by carrier statistics. So, if a lower value is needed, there needs to be a shift to another type of device. This could be a tunnel FET, which is discussed in a feature by Suman Datta's group from Pennsylvania State University (see page 69).

So, as you can see, there are many problems, many solutions, and an interesting road that lies ahead.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718109
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Amy Rogers arogers@brunmedia.com +001 678-714-6775
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

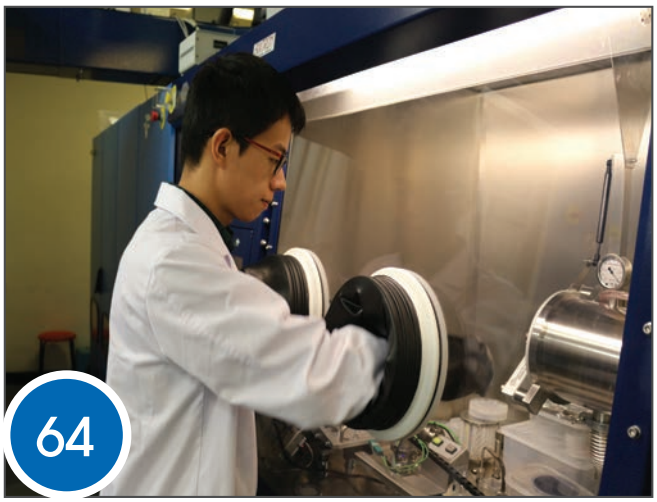
Volume 22 Issue 1 2016

features

news

news analysis

research review



contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

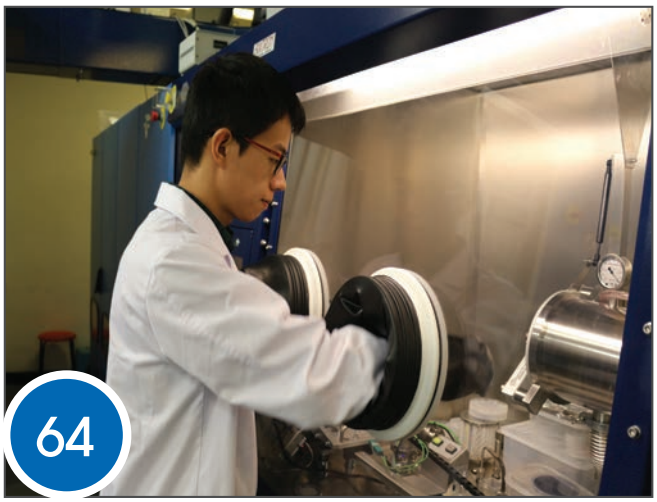
Volume 22 Issue 1 2016

features

news

news analysis

research review



II-VI to acquire EpiWorks and Anadigics for $110 million

US-BASED semiconductor laser firm II-VI has signed agreements to acquire EpiWorks at approximately $43.0 million and Anadigics at around $61.0M ($0.66 per share) in cash.

II-VI, which is headquartered in Saxonburg, Pennsylvania, says the acquisition of these two businesses will expand its technology platforms and production capacity for semiconductor lasers with a scalable 6-inch epitaxial growth and wafer fabrication platform. These acquisitions will also further position the company to serve fast-growing markets addressed by VCSELs, expected to grow at greater than 20 percent a year.

Francis J. Kramer, chairman and CEO said: "VCSELs address the need for increasingly intelligent human-machine interfaces such as gesture recognition in consumer electronics products as well as the growing demand for short-reach high-speed optical connectivity in data centres worldwide. Our engagement with key customers in these and other markets has been sufficiently compelling to lead us to believe that this investment is needed now."

EpiWorks, a compound semiconductor wafer company focused on GaAs and InP is located in Champaign, IL. It has 2015 revenue of approximately $14 million. Its 25,000-square foot, Class 1000 cleanroom epi foundry will provide expansion of II-VI's product portfolio. EpiWorks' expertise dovetails with II-VI's core competencies as an engineered materials company.

"Demand for high-performance semiconductor solutions used in communications, datacentre, cloud and advanced sensor applications continues to increase. EpiWorks has been adding capacity to address market growth and emerging photonics applications, however demand forecasts outpace our ability to add capacity organically. By merging with II-VI, EpiWorks has access to substantial expansion capital, a global footprint and sales support around the world. This will allow us to rapidly deploy our technology to the market and increase our market penetration." said David Ahmari, who will remain responsible for EpiWorks' sales, marketing and technology.
"Teaming with II-VI allows us to go beyond the typical epiwafer foundry model by offering not just scale, but a level of sophistication, flexibility and capability needed in our industry as it is scaling and evolving," he added.

"The combination of II-VI and EpiWorks creates a world class engineered semiconductor materials company. We are excited to join the II-VI family and push the envelope of performance in our industry. We have a creative, multi-year plan for capacity, new capabilities, and novel products that cover a wide range of industries and markets", said Quesnell Hartmann, CEO of EpiWorks, who will continue on as the general manager of the EpiWorks business unit.

EpiWorks will operate as a separate, but wholly-owned division of II-VI, named 'II-VI EpiWorks', and plans to expand production in Illinois. Access to MOCVD capacity at other II-VI sites also offers EpiWorks customers additional capacity, flexibility and redundancy.

Anadigics brings to II-VI a high volume foundry unmatched in the production of 6-inch GaAs wafers. The acquisition of this foundry adds capacity more quickly and economically than building it new.

II-VI believes that controlling a scalable infrastructure is critical for extending the company's laser enterprise product portfolio technology and positioning II-VI as the world leader in VCSEL technology.

Anadigics had year to date (nine months) revenue of $46 million and net assets of approximately $28 million as of October 3, 2015.

The combined value of these acquisitions is $110 million in cash. On a non-GAAP basis, the company expects these transactions to be accretive to continuing operations beginning in the second half of calendar 2017. For the quarters preceding that, the transaction is expected to be dilutive due to investment in the 6-inch platform.

No go for Philips GO scale deal

PHILIPS announced back in March of 2015 that the company planned to sell its majority interest in its combined LED components and automotive lighting business to a Chinese consortium led by GO Scale Capital. Subsequently news broke in October that regulators in the United States had concerns, and on January 22, 2016, Phillips confirmed that the sale was no longer happening.

The news of a Chinese company or investment firm purchasing a western company is not, an uncommon occurrence; however, the consideration now is how this news affects the future of Philips, one of the largest electronics companies in Europe, says IHS in a new Research Note on the landscape for LED components. Lumileds has made steady progress in the market for packaged LEDs. The company rose from fifth ranking globally in 2011 to third, behind first ranked Nichia and second-ranked Osram in 2015.

Recent provisional research from IHS indicates that Lumileds may not have closed the gap any further, as Osram Opto Semiconductors continues to perform well in the automotive sector. It is unclear whether Western LED companies would be comfortable with the idea of a supplier moving from European ownership to Chinese ownership.

Overall the fact that this deal was blocked is not good news for Philips. The current state of both the LED industry and the global economy augurs that the sale of Lumileds will not be an easy one. Blocking of one foreign company does not bode well for the potential sale to other foreign companies, as other buyers will also have concerns over further regulation.

Fujitsu announces high output 75-110GHz GaN power amplifier

FUJITSU LIMITED and Fujitsu Laboratories have announced the development of a high power output GaN HEMT power amplifier for use in W-band (75-110 GHz) transmissions, opening up the possibility of high-speed wireless communications of several Gbps in areas where fibre-optic cable is difficult to lay. Evaluations of the newly developed power amplifier confirmed it to have 1.8 times increased output performance than before, which would translate to an increase of over 30 percent in transmission range when used in a high-speed wireless network.

A portion of this research was conducted as part of a project of the National Institute of Information and Communications Technology (NICT) on 'Agile Deployment Capability of Highly Resilient Optical and Radio Seamless Communication Systems'/ Details of this technology were presented at Power Amplifiers for Wireless and Radio Applications (PAWR2016), opening January 24 in Austin, Texas.

Existing power amplifiers for high-frequency transmissions in the millimetre-wave band (30-300G Hz), built using GaAs or CMOS semiconductors, are limited by their operating voltage to an output of about 0.1 W, and it has not been possible to increase this.

GaN-HEMT power amplifiers have achieved high output performance in the microwave range (3-30 GHz), but the problem up until now was that their output performance declined in the W-band range. To solve these problems, Fujitsu developed a GaN-HEMT device with a unique structure capable of increasing output in the millimeter band.

This uses a layer of InAlGaN, and double-layer SiN passivation film to increase current density by a factor of about 1.4, resulting in 3.0 W of output power from a transistor per 1 mm of gate width, at a high frequency of 100 GHz.
In developing this transistor, Fujitsu collaborated with Yasuyuki Miyamoto of the Tokyo Institute of Technology in developing a device-simulation technology.

Fujitsu's circuit uses pairs of GaN-HEMTs grouped together into compact, high-gain units with low power loss. These units are then connected in a series by the interstage circuits.

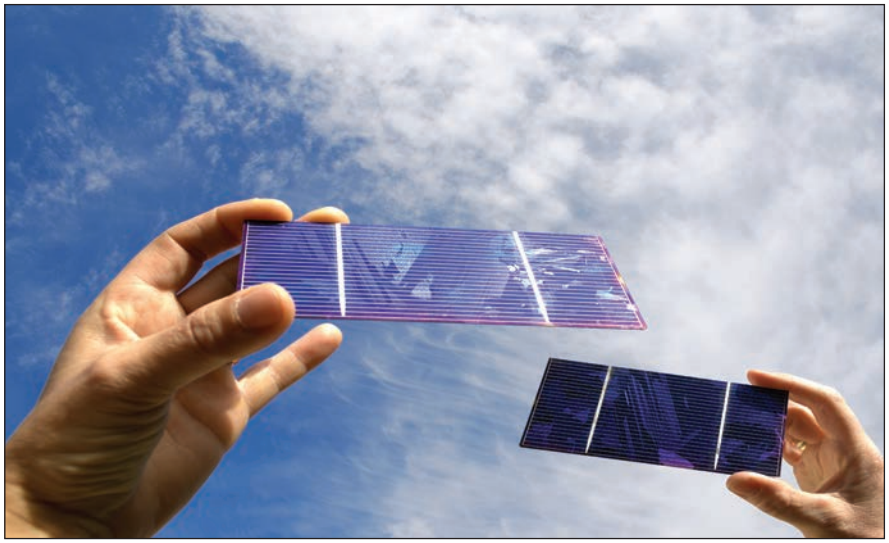
An early prototype power amplifier had amplitude that multiplied its input by a factor of 80, producing 1.15 W of output power. Power output per transistor, a measure of power-amplifier performance, was 3.6 W per 1 mm of gate width, the highest in the world, according to Fujitsu.

Fujitsu plans to apply this power amplifier technology to high-capacity long-range wireless communications, and to implement high-speed wireless communications systems that can be used for high-expediency temporary communications infrastructure for use during special events and when fibre-optic links have been broken in the event of disasters.

III-V solar cells hold promise for indoor energy harvesting

RESEARCHERS working on energy-harvesting systems at Bell Labs, Alcatel-Lucent in Ireland have shown that III-V single-junction solar cells made from GaAs and GaInP significantly outperform amorphous-silicon and dye-sensitised solar cells at low illuminations with two times greater measured power densities.

In their paper 'Performance of III-V Solar Cells as Indoor Light Energy Harvesters' in the *IEEE Journal of Photovoltaics*, Ian Mathews and colleagues showed that credit-card-sized GaAs and GaInP solar cells will provide around 4mW of power under 1000 lx (i.e., in a bright office space).



Power levels of this range will enable autonomous energy systems for IoT sensors providing scalable wireless sensor solutions for use in future telecoms networks. Amorphous-silicon and dye-sensitised solar cells have been tested extensively as indoor light harvesters. Their wide bandgaps are well suited to absorption of the spectra from compact fluorescent lamps (CFL) and LED bulbs.

III-V solar cells are, however, the highest performing PV devices under 1-sun conditions but have not been thoroughly investigated under indoor illumination conditions. Traditionally these cells were viewed as too costly for many applications but new manufacturing methods are improving their economic case.

POET partners with Wavetek

POET TECHNOLOGIES, a developer of opto-electronics fabrication processes, has announced a manufacturing services agreement with Wavetek Microelectronics, a member of UMC's New Business Group.

The POET platform transfer and manufacturing agreement with the Hsinchu Science Park-based GaAs foundry is said to be an acceleration of POET's ultimate objective of working with a 'pure-play' foundry offering a wide range of dedicated, flexible and competitive foundry services.

POET reported that it is encouraged by the promising initial results of its wafers sourced from its epitaxial wafer partners processed in the Wavetek facility using POET's proprietary technology, which has recently been transferred under a nondisclosure agreement between POET and Wavetek. The agreement addresses all current manufacturing requirements (including VCSELs) in POET's ongoing commercialisation initiative. A previously announced subsisting manufacturing services agreement was limited to prototype demonstration of VCSELs.

"Wavetek is respected internationally as a pure-play foundry," said POET chief operations officer Subhash Deshmukh. "Its manufacturing capabilities provide POET the foundry services we need to meet the high volume and cost requirements that are critical to our success in delivering low cost monolithically integrated opto-electronic transceivers. We are extremely pleased to work with an innovative and disruptive technology leader like POET," said Wavetek president C.G. Shih. "Wavetek is excited to provide the high-volume manufacturing capabilities POET needs to spark a rapid expansion of opto-electronics applications such as those enabled by the POET platform."

Osram licenses Unity Opto under white LED program

OSRAM GMBH has granted Taiwan's Unity Opto Technology a royalty-bearing license to produce white LED packages under Osram core patents covering phosphor conversion technology.

This technology is widely used in the LED industry for the generation of white light based on a semiconductor chip emitting blue light that is partially converted into one or more other colours by suitable phosphor materials.

The agreement with Unity Opto follows numerous license agreements between Osram and other producers of white LED packages. In total, more than 20 globally active LED producers are licensed under Osram's core LED patents.

Osram and Unity Opto have also agreed to dismiss the pending patent litigation Osram had brought against Unity Opto's customer ASUS in Germany. The District Court in Düsseldorf had awarded Osram an injunction and found that ASUS had to compensate Osram's damage caused by the patent infringement.

Dieter Boss, Osram Head of Licensing said: "Osram has built up a very strong patent position. We welcome Unity Opto as a licensee under our White LED License Program. To LED producers not licensed by Osram but still making use of our patents, we would like to send the message that Osram will continue to vigorously enforce its patents."

Cree results exceed targets with 5 percent revenue increase

US LED lighting firm Cree has announced revenue of $436 million for its Q2 2016, ended December 27, 2015. This represents a 5 percent increase compared to revenue of $413 million reported for the Q2 2015, and a 2 percent increase compared to Q1 fiscal 2016.

GAAP net income for the Q22016 was $14 million, or $0.14 per diluted share, compared to GAAP net income of $12 million, or $0.10 per diluted share, for the Q22015. On a non-GAAP basis, net income for the Q2 2016 was $30 million, or $0.30 per diluted share, compared to non-GAAP net income for the Q2 2015 of $38 million, or $0.33 per diluted share.

"We delivered on our goal of building financial momentum in Q2, with earnings that exceeded our targets driven by solid revenue growth, good margins and operating expense leverage," stated Chuck Swoboda, Cree Chairman and CEO.

"Our lighting business continues to grow, the LED business has stabilised, and our Wolfspeed Power & RF division continues to make progress. Overall, we had a good first half of fiscal 2016 and are well positioned for a strong second half."

During the second quarter of fiscal 2016, Cree completed its LED business restructuring recognising $3 million of expense for factory capacity and overhead costs reductions. The restructuring charges are included in the GAAP results only.

For its third quarter of fiscal 2016 ending March 27, 2016, Cree targets revenue in a range of $400 million to $430 million, with GAAP gross margin targeted to be 31.0 percent and non-GAAP gross margin targeted to be 31.7 percent .

your

EPITAXIAL GROWTH

partner

Enabling advanced technologies

- World leading technology
- Complete materials range
- MOCVD, MBE, CVD
- Advanced semiconductor wafer products
- Advanced R&D capabilities
- Multiple, manufacturing sites (Europe, Asia, USA)

IQE

www.iqep.com

Plessey to build LEDs in cubic GaN

PLESSEY, Anvil Semiconductors and the University of Cambridge have announced that they are working together to fabricate high efficiency LEDs in cubic GaN grown on Anvil's 3C-SiC / Si substrates.

Cubic GaN has the potential to overcome the problems caused in conventional LEDs by the strong internal electric fields, which impair carrier recombination and contribute to efficiency droop. This is particularly true for green LEDs where the internal electric fields are stronger and are believed to cause a rapid reduction in efficiency at green wavelengths known as "the green gap". The availability of cubic GaN from a readily commercialisable process on large diameter silicon wafers is as a key enabler for increasing the efficiency of green LEDs and reducing the cost of LED lighting.

The collaboration, which is partly funded by Innovate UK under the £14 million Energy Catalyst Programme, follows on from work by Anvil Semiconductors and the Cambridge Centre for GaN at the University of Cambridge where they successfully grew cubic GaN on 3C-SiC on silicon wafers by MOCVD.

The underlying 3C-SiC layers were produced by Anvil using its patented stress relief IP that enables growth of device quality SiC on 100 mm diameter silicon wafers.

The process is readily migrated onto 150 mm diameter wafers and potentially beyond without modification and is therefore suitable for large, industrial-scale applications.

Plessey has started to commercialise LEDs produced in conventional (Hexagonal) GaN grown 150 mm silicon wafers using IP originally developed at The University of Cambridge. Anvil's high quality 3C-SiC on Silicon technology, which is being developed for SiC power devices, provides an effective substrate, to allow single phase cubic GaN epitaxy growth and provides a process which is compatible with Plessey's GaN on Si device technology.

Keith Strickland, the CTO of Plessey commented: "At Plessey we are constantly striving to find novel technology that can enhance our LED products. The work that has previously been carried out at the University of Cambridge in collaboration with Anvil Semiconductors has demonstrated that high quality cubic-GaN can be grown on large area Si substrates compatible with our manufacturing process. This has opened up the possibility to develop green LEDs with high efficiency that will allow us to demonstrate a new generation of efficient and controllable lighting products."

Professor Sir Colin Humphreys, director of the Cambridge Centre for GaN, added: "The properties of Cubic GaN have been explored before, but the challenges of growing this thermodynamically unstable crystal structure have limited its development. The high quality of Anvil's cubic SiC on Si substrates and our experience of developing conventional GaN LED structures on large area wafers have enabled a breakthrough in material quality. This latest project will build on our ongoing collaboration with Plessey to deliver, for the first time, green LED devices with efficiency approaching that in blue and red LEDs."

Cree ships latest commercial LED lights

CREE has announced that IG Series parking garage luminaires and KR Series LED downlights are now available to ship in volume. Both series feature Cree WaveMax Technology, an optical platform that is said to offer a combination of control, uniformity and efficiency.

The IG Series lighting addresses challenges particular to parking garages. It provides low-glare comfort and decreased LED source luminance to cast illumination that maximises detail and defeats shadows. The series delivers energy efficiency and fast payback, according to the company.

"Cree continues to prove that long-lasting LED technology can do infinitely more than save energy and maintenance costs - it's the smarter choice for our bottom line, tenants and buyers experiences," said Steve Maranos, vice president of technology, CMC Group, Inc. "With Cree's IG Series luminaire, we're rethinking what lighting can do. It is unlike any solution on the market - delivering the modern design, controllability and low-glare illumination with performance that exceeds our expectations for any parking application, all while delivering significant ongoing savings at an affordable price."

Florida International University (FIU) in Miami recently installed Cree's KR Series LED downlights to upgrade its Graham Centre Ballroom, their premier event space. Cree's new KR8 downlight brought uniform light distribution and efficiency to the FIU event space.

FIU upgraded its event space lighting from halogen-lamped recessed downlights that produced hotspots and poor light distribution, compounded by the 18 foot mounting height.

CSindustry awards2016

Shortlist: Who wins you decide

Sales of compound semiconductor chips are soaring. This is being driven by an uptake in solid-state lighting; rising revenues for smartphones, which are packed with GaAs chips in their front-ends; a build-out of capacity in optical networks; and greater use energy-saving, SiC and GaN devices in power electronics. These sectors are driven by companies making important progress. But which of them has made the biggest breakthrough this year, or the most important contribution?
To showcase the success of companies within the compound semiconductor industry: we now ask you, the industry, to decide who should receive the recognition in 2016.

Voting is open to all companies, individuals and organisations within the CS industry.

www.csawards.net/vote

Substrates & Materials Award

ALLOS Semiconductors
150 and 200 mm GaN-on-Si epiwafer

AMMONO S.A.
2-inch AMMONO-GaN semiconductor crystals

Imec
GaN on Si materials development with 200 mm wafers

Metrology Award

Lasertec
SICA 88

Renishaw
In-Via microscope for examining SiC substrates

High-Volume Manufacturing Award

AIXTRON SE
AIX G5+C

Skyworks Solutions, Inc
SkyOne® Mini front-end solution

Device Design and Packaging Award

Silvaco
Victory Process & Device TCAD Simulator

Cambridge Electronics
Laptop power converter using GaN

Cree
900-V SiC MOSFET

Innovation Award

Brolis Semiconductors
SensAline tunable laser

Qorvo, Inc
RF Fusion

Osram Opto Semiconductors
Quantum Colours conversion technology

For more information: www.csawards.net

Winners will be presented to on 1 March at the CS International Conference in Brussels.

Designs for light

Could a new design flow from Cadence accelerate the manufacture of photonics ICs? Rebecca Pool investigates.

LATE LAST YEAR, US-based Cadence Design Systems revealed a photonics IC design flow developed to unite the disparate worlds of electronics and photonics.

Joining forces with photonics design tool developer, Lumerical Solutions, Canada, and software design business, PhoeniX Software, The Netherlands, Cadence unveiled a flow for designing photonic ICs based on its so-called Virtuoso custom-design platform.

"We wanted to bring the type of automation and high efficiency that design engineers have been accustomed to in electronics environments, to photonics," highlights Gilles Lamant, distinguished engineer at Cadence and a key member of the company's business management team for the Virtuoso Custom Design platform.

"This is not a silicon photonics flow, there is nothing in the design that makes it suitable for one type of photonic IC," he asserts. "We are really trying to deliver a mainstream design flow that will bring productivity [to photonic IC design.]"

For decades, designers of electronics systems have relied on electronic design automation (EDA) tools to design and analyse semiconductor chips. From design and simulation to analysis, verification and manufacturing preparation, industry heavyweights including Cadence, as well as Synopsys and Mentor Graphics, have delivered design rules for CMOS processes to ease chip development.

But right now, life for designers of photonic IC is very different. Myriad materials and technologies – including III-V semiconductors, silicon photonics as well as hybrid and 3D stacking designs – exist.

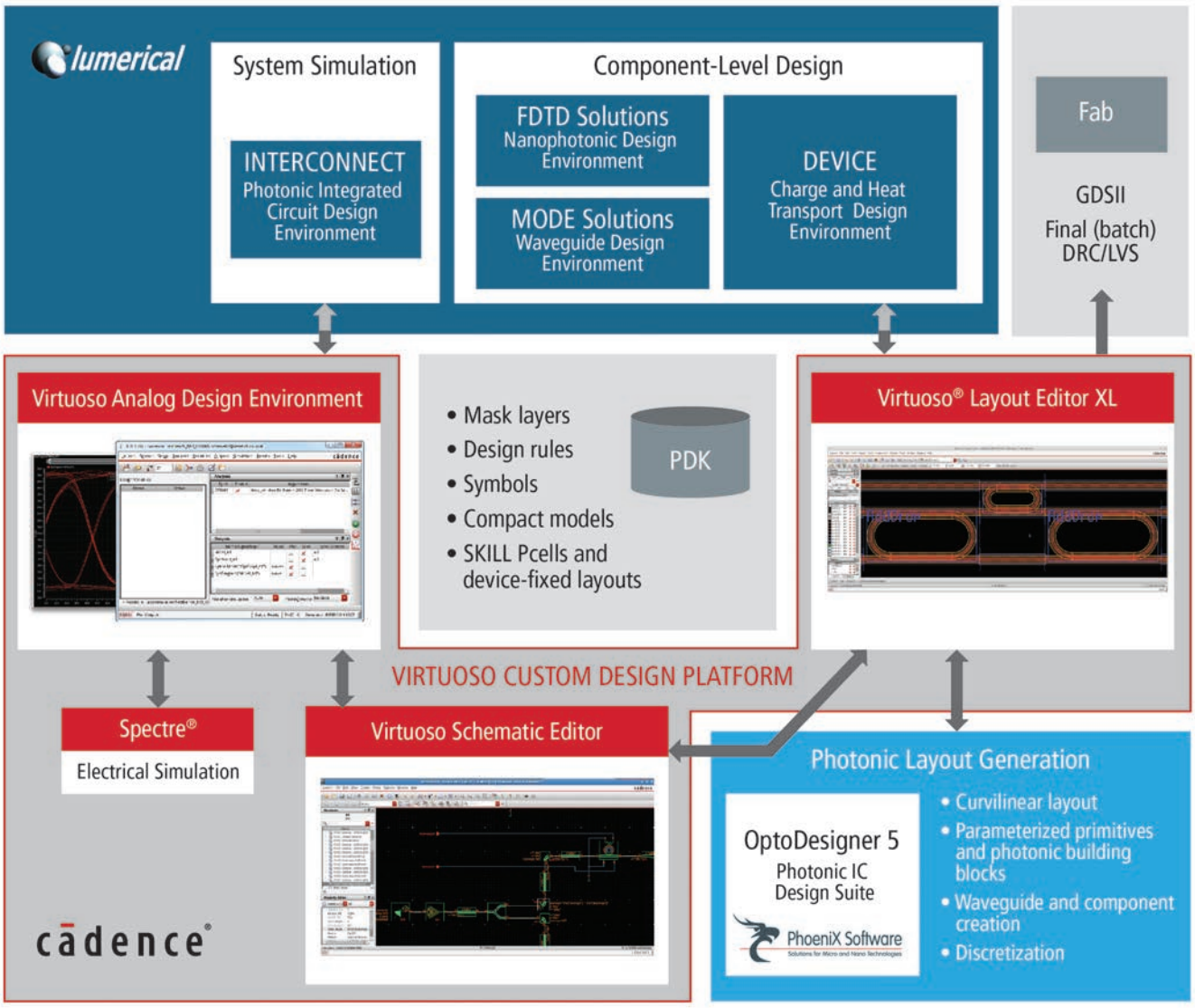
The photonics industry is only just transitioning from PCB to integrated circuit development with numerous small fabs provide manufacturing capacity. And while many software suppliers exist, each provides tools for different parts of a design flow with standardisation amongst tools and processes still emerging.

Indeed, as PhoeniX Software chief executive, Twan Korthorst, recently stated: "Photonics is where electronics was in the 1980s."

And so Cadence's collaboration with Lumerical and PhoeniX marks a crucial step in the delivery of an integrated electronics/photonics design automation (EPDA) flow for photonic integrated circuit designers.

"Many in the EDA industry are not so familiar with photonics. It's seen as exotic or even science fiction," says Lamant.

"So with our partners, we're now trying to say, well the processes are not so new, they've actually been around a long



Photonics IC design: bringing electronic design automation to light.

time," he adds. "What is new, is there's not a unified methodology."

A different design

So what's different about photonic IC design? Due to the nature of light, photonic ICs demand precisely drawn curved structures in mask layout, whereas CMOS ICs typically use rectilinear layout shapes.

Indeed, this need to handle curves is perhaps one of the most significant issues for adapting IC design tools and foundry processes to photonics.

"We're simulating the physics of light at the front-end [of the design flow] and at the back-end – everything's drawn with a curve," highlights Lamant. "Photonics is a very different domain to electronics."

Given this, Lumerical's photonic circuit simulation engine – 'Interconnect' – has been integrated to Cadence's Virtuoso platform to speed analysis and design of photonic IC layouts.

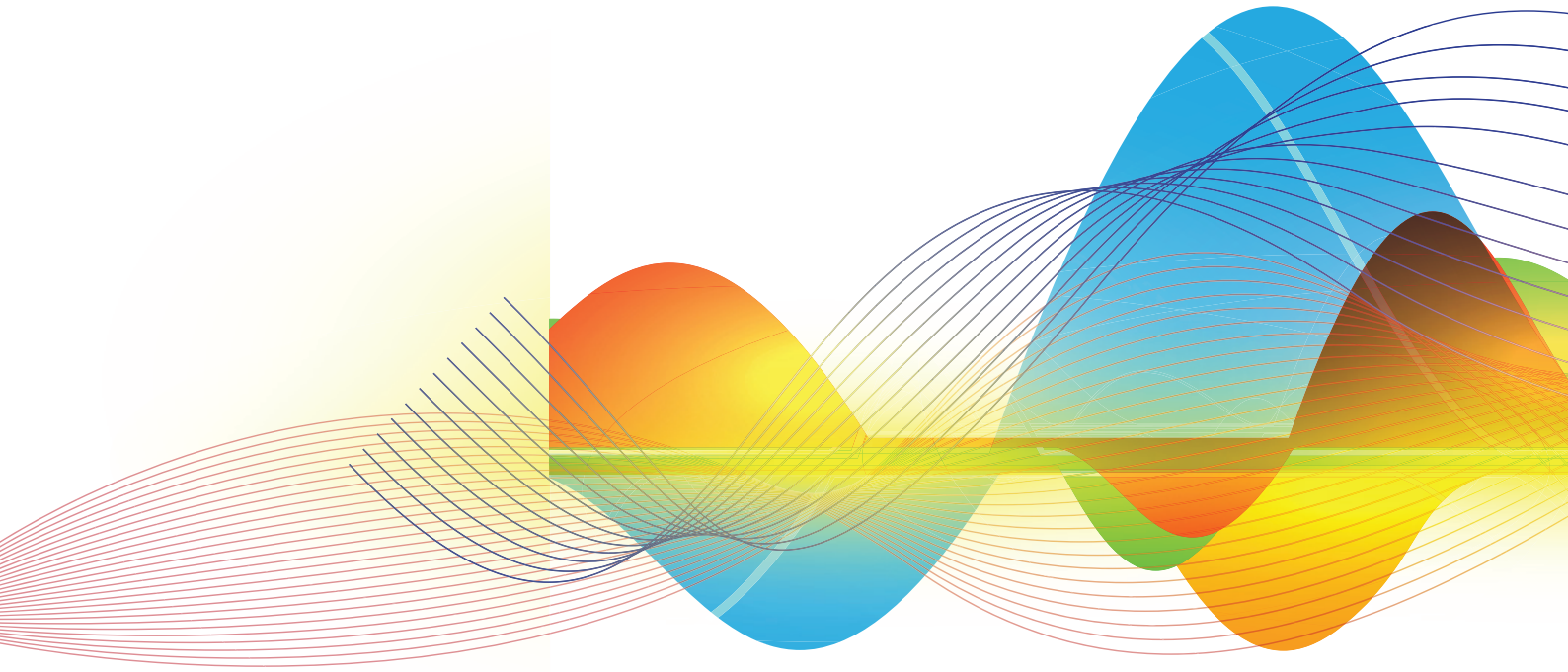
Meanwhile, the additional integration of PhoeniX Software's 'OptoDesigner' photonic chip design software is intended to provide designers with access to non-linear photonic building blocks, to enable, for example, automatic waveguide routing and interactive waveguide creation.

Crucially, as Lamant points out, many photonics tools do not deal with electronic design, whereas clearly EPDA offers both. "You need some electronics around your photonics so we're bringing an environment where you can design your electronics and photonics together," he says. At present, Cadence is in the process of nailing down its design roadmap. According to Lamant, photonic IC packaging will be key.

As he puts it: "How are we going to connect the fibre optics to the photonics and other components?"

And more electronics and photonics co-simulation is on the cards. "This will all come out within a year or two," says Lamant.

"Customers have been suffering from a lot of 'one-offs' but now we are seeing significant photonics growth, they really want an electronics-type of design flow," he adds. "And since we released this [EPDA flow] my mailbox has been full."



Move over Magnetron

Do the latest LDMOS and GaN RF power devices mark the end of the magnetron-based microwave? Rebecca Pool investigates

SOLID-STATE RF energy is set to provide a more controllable power and heating source.

While many in the solid-state RF power industry have been fixated with getting LDMOS, and now GaN-based, power amplifiers into base stations, an up and coming market is now providing power device manufacturers with a lot of food for thought.

Your typical microwave oven currently relies on magnetron tubes to generate the electromagnetic waves required to cook its contents.

But slot in a solid-state RF power source and you could more precisely control the energy delivered to different parts of an oven. Beyond simply controlling power levels, energy delivery can also be optimised by tuning the frequency, according to conditions, and contents within the oven.

Benefits such as this have not been lost on appliance OEMs, such as E.G.O. Elektro-Gerätebau and Whirlpool, and late last year, these industry players joined forces with components manufacturers to form the RF Energy Alliance (RFEA).

The small but growing consortium – including MACOM and recent NXP spin-off, Ampheon – intends to drive the developments of standards to promote solid state RF Energy.

As RFEA executive director, Klaus Werner, tells *Compound Semiconductor*: "Our roadmap is now developed and is going to focus discussions very nicely on the industry sweetspots."

So how exactly would the solid-state RF oven work? According to Werner, the microwaves are generated in fundamentally the same way as traditional RF power generation, using a solid-state RF power amplifier and signal conditioning.

However, instead of being sent to an antenna to transmit data, RF energy is channeled via waveguides into an oven to heat the contents.

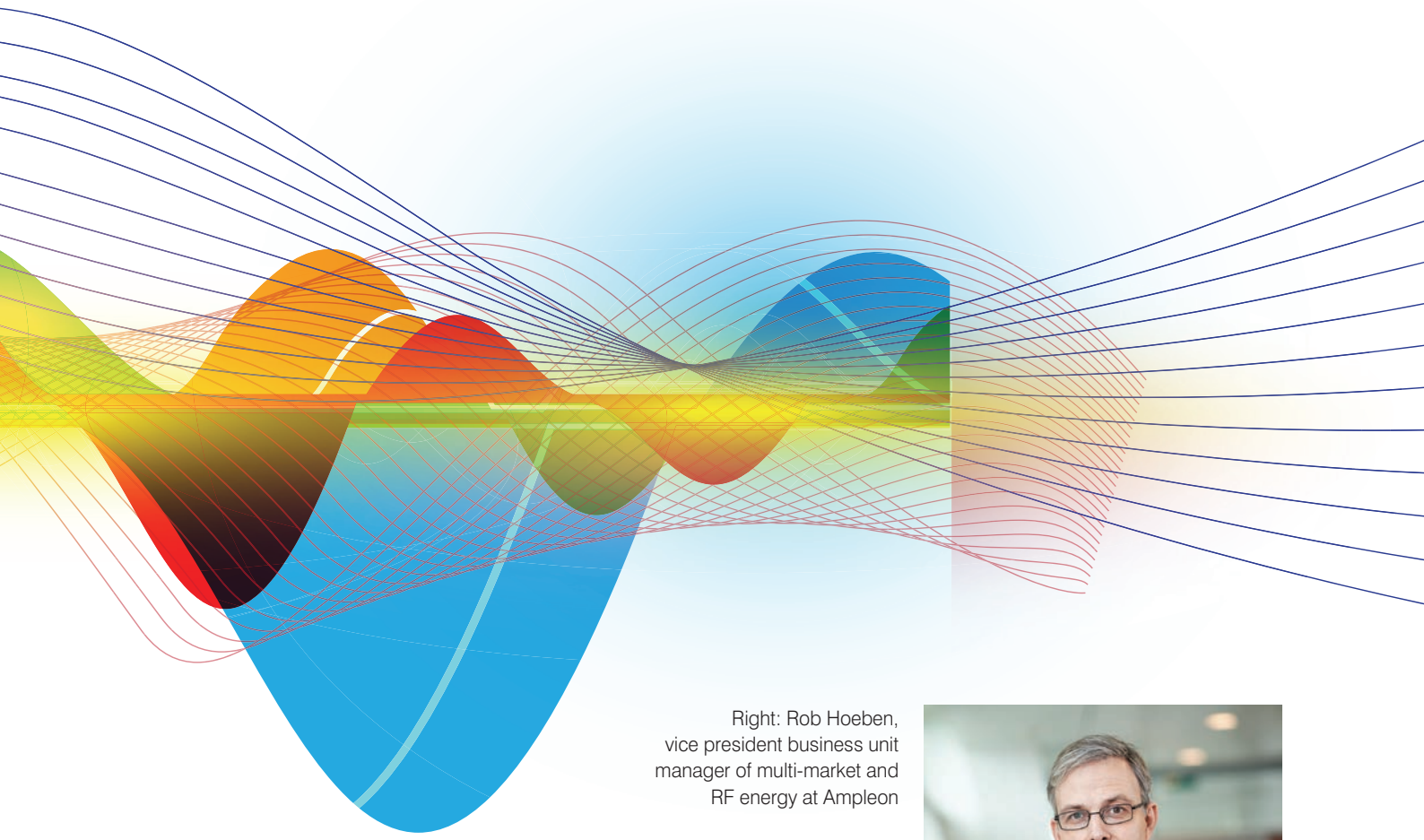
Indeed, earlier this year, NXP Semiconductors unveiled its 'Sage' solid-state RF oven proof-of-concept that promised to control exactly where, when and how much energy was directed into food.

And as Werner highlights: "I also expect to see both Whirlpool and E.G.O. Elektro-Gerätebau with [a solid-state RF oven] in the market place next year and know of related companies that are also looking to launch products in 2016."

"These first-generation ovens will not be able to beat magnetron [products] on price, but will provide better control to the customer," he adds.

Small and efficient

At the heart of these first ovens, lies the all-important LDMOS RF transistor, which has been instrumental to getting solid state RF energy to market.



Right: Rob Hoeben, vice president business unit manager of multi-market and RF energy at Ampleon

Laughingly, Werner refers to past RF power devices as 'beasts', but highlights how the latest generation of smaller and efficient LDMOS devices has enabled solid-state RF power to reach consumer applications.

For example, NXP, for one, has delivered myriad devices operating at 2.45 GHz and 915 MHz for RF energy applications, and its recent spin-off, Ampleon, now hopes to reap the rewards.

As Rob Hoeben, vice-president business unit manager of multi-market and RF energy at the new company puts it: "We have worked relentlessly to design and implement transistors in magnetron-based applications, and now see a lot of growth potential in the market on top of existing base station applications."

"Many customers that have been used to working with magnetron elements are now hoping to adopt solid-state power in their designs. We expect that the market will grow, so this is all good," he adds.

Ampleon's Rob Hoeben: "The cost-sensitive nature of RF Energy applications will favour LDMOS over any GaN technology, at least for the coming five years."

However, Hoeben believes that LDMOS, rather than GaN-on-silicon or GaN-on-SiC, transistors will be the first to find a space in this new market.

"We have both LDMOS and GaN-on-SiC technology amongst our offering but when it comes to RF energy, we are focusing on LDMOS," he says.

"Customers want product consistency and quality at a certain cost-point. Performance and cost are hard to meet with GaN, whatever its flavour."

"And the cost sensitive nature of RF Energy applications will favour LDMOS over any GaN technology, at least for the coming five years," he adds.

Still the vice president is open to change. As he points out, the company currently ships a lot of GaN devices to base station and aerospace markets and will be 'keeping its options open'.

"LDMOS has been through many generations of technology evolution over the last twenty years, but if GaN-on-silicon continues to reduce in cost, then of course the technology has its merits in terms of functional performance," he says.

"We are a fabless company so can consider everything," he adds. Werner has similar thoughts on GaN-on-SiC, simply saying: "I don't currently see GaN-on-SiC in the RF energy world. This industry's players are interested in repeatability and reliability. The efficiencies [that GaN-on-SiC could bring] are not so much of an issue."

But, for the RFEA executive director, GaN-on-silicon is different. "If this technology can be manufactured in an eight inch wafer fab so the cost approaches that of LDMOS, then we really will have a great technology in our hands to work with."

All eyes on **Osram**

As Osram Opto Semiconductor unveils expansion plans, Rebecca Pool talks to CEO, Aldo Kamper, about investment, industry domination, and more.

In the latest of a several moves to strengthen its position in the LED market, Osram is to spend a hefty €1 billion on building its largest fabrication plant to date, in Kulim, Malaysia.

A stone's throw away from its 4-inch InGaN-on-sapphire LED chip plant in Penang, this 6-inch LED production site could eventually churn out 20,000 6-inch wafers every week for general lighting markets worldwide.

"We're in the final stages of preparation and will start building the factory in March 2016," Osram Opto Semiconductor chief executive, Aldo Kamper, tells *Compound Semiconductor* magazine.

"We reckon it will take around a year to build the factory ready for equipment, and then come the fall of 2017, we will probably be ready for mass production," he adds.

Clearly, Osram's weekly wafer quota won't hit 20,000 in 2017, but the latest investment indicates that the Germany-based LED and lighting supplier is very serious about its future position in the general lighting market.

Once open, the Kulim plant is set to be the world's largest 6-inch LED chip production site, and as Osram executives have repeatedly spelled out, it is intended to grow Osram's share in this market segment. The Germany-based lighting manufacturer already has a strong presence in automotive and industrial lighting markets, but has steered away from general lighting market segments in the past.

However, with general lighting having the highest growth potential of all LED markets in the coming years, Osram wants in and Kulim can help to provide this. "Surface-emitting LEDs are a big business for us and are extremely important for many optical systems, projectors and street lighting," highlights Kamper. "But we also have a very competitive volume-emitting chip, so can take a big step into the general lighting space."

"We're successful in automotive and industrial applications, but to continue growing we need a strong position in general lighting, as we are currently under-represented here," he adds. "Today we are number two [in the LED market] and we want to stay there."

Osram-technician at the Wuxi plant, China.

Massive in Malaysia

So how exactly will the €1 billion be spent in Kulim? Kamper will not be drawn on the detail, simply stating a meaningful portion will be spent on the fabric of the factory, with the remainder allocated to chip processing equipment.

"The factory will be multiple times larger than Regensburg and multiple times larger than Penang. We plan to make this major expansion of our capacity over the next years," he says. "If you imagine how big the new fab is, then you'll see we will need several tens of reactors to fill it."

"Until now epitaxial manufacturing has purely taken place at our Regensburg plant in Germany; this will be the first time we will bring epitaxy to Malaysia," he adds.

Chip fabrication at Kumin will take place on 6-inch sapphire wafers, although the new reactors will be upgradable to 8-inch wafer fabrication, if, as Kamper says, 'this becomes relevant one day'.

"We've worked in pre-development on eight inch wafers but given the cost and availability of eight inch substrates, this is not really a key topic for us over the next few years," he explains.

In a similar vein, production will remain firmly on sapphire, not silicon. According to Kamper, the difference in cost between a 6-inch silicon wafer and a 6-inch sapphire wafer has reduced significantly. What's more, reaching the LED performance levels of a sapphire-based LED, on a silicon substrate, isn't easy.

"If you don't achieve the same efficiencies on silicon, then you have to [fabricate] bigger chips, which destroys the cost advantages of using silicon," says Kamper. "We continue to look at silicon and if there is a breakthrough we will use it, but we've done our homework and feel growing on sapphire is the more economical way to go."

And while industry pundits have hinted that Osram could be over-stretching itself with its latest investment spend, Kamper is quite clear on the company's strategy.

"It's the mix that needs to be right," he says, "We are financially very healthy and will continue to invest heavily in automotive and industrial businesses while accelerating the pace in general lighting."

"Playtime is over and with time we are going to see more and more separation amongst competitors, as it will be difficult for everyone to keep pace," he adds. "You have to think in large volumes in this industry if you want to be amongst the largest players."

Left: Will Osram's €1 billion investment in a new Malaysia LED fab bolster its position in general lighting market segments?

Deep UV:

The road to mass production

SETi's recent Nitek acquisition looks set to deliver cheaper UV LEDs, faster than ever before. Rebecca Pool reports.

LATE LAST YEAR, UV LED maker, Sensor Electronic Technology (SETi), bought the commercial operations of competing LED manufacturer, Nitek, a move that propels the company towards cheaper mass production.

As was stated at the time: 'the transaction combines two complementary companies to become the largest UV-focused LED developer and manufacturer in the world with the lowest cost of ownership'.

Renowned for manufacturing deep UV LEDs for spectroscopy as well as aerospace and defence markets, SETi has also been focusing on applications for more consumer-oriented sectors, including disinfection and healthcare. And with Korea-based UV and blue LED maker, Seoul Viosys, and affiliates, taking a major stake in the company earlier this year, the company is primed for the necessary manufacturing expansion that these markets will demand.

"We have in-house capacity at our chip fab and packaging facility in South Carolina and can produce significant volumes of product through this facility – around several million units a year," highlights director of marketing and sales, Tim Bettles.

"And now Seoul Viosys can utilize our epi-wafers and manufacture extremely high volumes through its chip fabrication and packaging facilities as well," he adds.

So what exactly does Nitek bring to SETi right now? The University of South Carolina spin-off launched in 2007 to commercialise III-nitride technologies, and supplies both near-UV and deep-UV LEDs.

However, crucially for SETi, Nitek has developed a cost-effective and high-volume manufacturing process for deep-UV LEDs; not an easy task. While UV-A LEDs, emitting at 400 to 315 nm, are fabricated by growing InGaN-based epilayers on sapphire substrates via the same MOCVD methods used in visible LED markets, UV-B and UV-C wavelengths use a completely different materials structure.

Manufactured by only a handful of companies, these UV-B and UV-C devices – which emit at 315 nm to 280 nm and 280 nm to 210 nm – are fabricated by depositing AlN layers onto either a bulk AlN crystal or a sapphire wafer. SETi has focused on the latter, using migration-enhanced MOCVD and migration-enhanced lateral-epitaxial overgrowth to grow its AlN-on-sapphire UV LEDs. Bettles declines to provide detail on Nitek's manufacturing process, simply stating: "We have secured manufacturing equipment and personnel."

But as he emphasises: "Prior to acquiring Nitek, we had the largest epi-wafer capacity in the world for deep UV LEDs, but Nitek will allow us to reach even higher manufacturing volumes and reduce the cost of our epitaxy processes per chip."

"And now we're seeing design wins into consumer products, this will really help us to drive deeper into these markets," he adds.

> "We all use MOCVD but the process window is very different for deep UV LEDs, which is a large barrier to entry. Low-cost white LED companies in China and the rest of Asia can't move into this market so easily. So we now see ourselves as by far the largest company that is also a total UV LED provider and between Seoul Viosys and SETi. We really want to be the number one UV LED producer."

So where next for SETi? The company launched its surface-mount packaged LEDs around 18 months ago, and market adoption is gathering momentum. It also recently signed a long-term agreement with US-based Wellness Center subsidiary, Psoria-Shield, to develop UV-B LEDs for phototherapy systems. What's more, as part of the Nitek deal, SETi has acquired the exclusive right to sell Seoul Viosys UV-A LEDs to North America.

"We'll be developing our processes to make sure we have the largest capacity and most cost-effective products on the market," says Bettles. Importantly, and unlike longer-wavelength UV-A LED markets, the SETi director doesn't expect imminent competition from Asia-based visible LED manufacturers, keen to tap into new markets.

"We all use MOCVD but the process window is very different for deep UV LEDs, which is a large barrier to entry," he says. "Low-cost white LED companies in China and the rest of Asia can't move into this market so easily."

"So we now see ourselves as by far the largest company that is also a total UV LED provider and between Seoul Viosys and SETi. We really want to be the number one UV LED producer," he adds.

Main image: High power, small footprint: UV LEDs are being developed for water sterilisation, medical analytical instrumentation and more.




6th CS International Conference

2016 Brussels Belgium

CS International 2016 will provide timely, comprehensive coverage of every important sector within the compound semiconductor industry.

The 6th CS International conference will be held at the Sheraton Brussels Airport Hotel, in Belgium on Tuesday 1st & Wednesday 2 March 2016.

The sixth CS International conference will build on the success of its predecessors, with industry-leading insiders delivering 34 presentations spanning industry.

Visit **www.cs-international.net** for further information on this event

Book your place NOW !

Visit www.cs-international.net/register.php to secure your place

TWO DAYS, FIVE THEMES

OVER 30 INSPIRING PRESENTATIONS

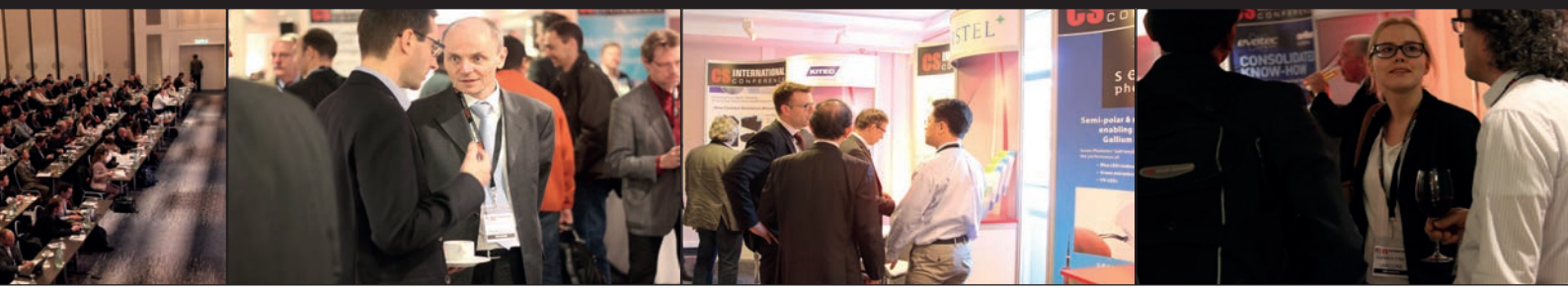
Five key themes lie at the heart of CS International 2016:

- The quest for 5G
- Driving deployment of wide bandgap power devices
- Exploiting opportunities for LEDs and lasers
- Making heterogenous integration a hit
- Capturing light, generating cash

Within each topic there is a key-note presentation from one of the most influential companies within this sector; one talk by a leading market analyst who will discuss trends within the industry and presentations by the leaders of firms developing cutting-edge technology in this field.

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry.



Conference Chair:
Drew Nelson President, CEO, IQE

This two day event covers five themes

The Quest for 5G

What challenges will GaAs and CMOS power amplifiers face in making the transition from 4G to 5G? And will faster data links play into the hands of GaN-based amplifiers for base stations?

KEYNOTE James Klein: Qorvo | Compound semiconductors: At the core of 5G

ANALYST Eric Higham: Strategy Analytics | Will chipmakers and foundries benefit from 5G?

SPEAKERS

Duncan Pilgrim: Peregrine Semiconductor | CMOS: Game on!

Stephen Kovacic: Skyworks Inc | Technology requirements and initiatives for 5G smartphones

Takahisa Kawai: SEDI | GaN for 5G base stations

Philip Greene: Ferrotec | Single-source planetary evaporation of metal alloys

Bernd Heinz: Evatec: | Deposition technology for thin film piezoelectric RF filters

Driving Deployment of Wide Bandgap Power Devices

Is SiC set to displace silicon in electric cars? And how will this material help to revolutionise the efficiency and operation of electrical grids?

KEYNOTE Daniel Fernandez: EU Project SPEED | Silicon carbide wide bandgap devices for energy applications

ANALYST Pallavi Madakasira: Lux Research | Driving adoption of wide bandgap power electronics

SPEAKERS

Peter Ward: Anvil Semiconductors | Driving down the cost of SiC devices for consumer applications

Markus Behet: EpiGan | GaN on silicon – a truly revolutionary semiconductor technology matures

Hans-Joachim Würfl: FBH Berlin | GaN normally-off devices for highly efficient power switching

Marta Borasio: Laytec | Reliability and yield limiting variances - early detection by advanced *in-situ* monitoring

Mark Dineen: Oxford Instruments Plasma Technology | Latest developments in plasma etch processing

Yumin Gao: Evans Analytical Group | Advanced material characterization

Somit Joshi – Veeco Instruments | GaN-Si MOCVD advancements for improved power device performance

Stewart Wilson – Keysight Technologies | Gate charge and capacitance switching loss measurement enhances device modelling

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry.

Exploiting Opportunities for LEDs and Lasers

Can LED bulbs meet the most demanding lighting applications, such as those found in the retail sector? And what are the opportunities for infrared and ultra-violet LEDs?

KEYNOTE Abdelmalek Hanafi: BMW | Doubling driver visibility with laser-based headlights

ANALYST Pierrick Boulay: Yole Développement | Opportunities for IR LEDs

SPEAKERS

David Cheskis: Anadigics | 6-inch VCSEL wafer fabrication manufacturing advances

Augustinas Vizbaras: Brolis Semiconductors | Mid-infrared light sources: manufacturability and applications

Andrea Knigge: Ferdinand-Braun-Institut | High-power, high-efficiency lasers for fibre lasers and other markets

Reinhard Windemuth: Panasonic | Solutions for LED manufacturing

Bedwyr Humphreys: Seren Photonics | Semi-polar gallium nitride enabling super high power automotive LEDs

Jurgen Kreis: Aixtron | Organic vs compound – competitive or complementary materials for particular applications

Making Heterogenous Integration a Hit

III-V channels are poised to make an introduction in next-generation logic circuits. But how will they be introduced, and what impact will they have?

KEYNOTE Yanning Sun: IBM | III-V/Si integration: Moore and more

ANALYST Nadine Collaert: IMEC | Heterogeneous integration of high mobility materials on a 300 mm silicon platform

SPEAKERS

Suresh Venkatesan: POET Technologies | A comprehensive technology platform for opto-electronic Integration

Lukas Czornomaz: IBM | Hybrid IIIV/SiGe technology for CMOS and beyond, opportunities for 3D monolithic integration

Thomas Uhrmann: EV Group | Heterogeneous integration enabled by advanced wafer bonding

Capturing Light, Generating Cash

What is needed to kick-start significant deployment of concentrating photovoltaic technology? And what are the opportunities for III-V detectors operating in the infrared?

KEYNOTE Carlos Algora: Technical University of Madrid | Perspectives of concentrator photovoltaic technology

ANALYST Frank Dimroth: Fraunhofer ISE | Terrestrial III-V solar cells: Challenges and opportunities

SPEAKERS

Paul Sharps: Solaerotech | High efficiency multi-junction solar cells: What is next?

Andreas Umbach: Finisar | Propelling detectors to 100 Gb/s and beyond




Book your place NOW !

Visit www.cs-international.net/register.php to secure your place

PLATINUM SPONSORS

AIXTRON

EAG Evans Analytical Group

EPIGAN

evatec process systems

EVG

KLA-Tencor

KEYSIGHT TECHNOLOGIES

LAYTEC Knowledge is key

OXFORD INSTRUMENTS The Business of Science®

seren photonics

FerroTec

Veeco

YOLE Développement

GOLD SPONSORS

CS CLEAN SYSTEMS® Exhaust Gas Abatement

IQE

kSA k-Space Associates, Inc.

Lasertec

NORSTEL

united monolithic semiconductors

ums

USHIO

ADDITIONAL SPONSORS

Delegate Bag sponsor

qorvo

Lanyard sponsor

PFL

Portfolio sponsors

Plasma-Therm A LEADING SUPPLIER OF PLASMA PROCESS EQUIPMENT

Exhibitor sponsor

INSPECTROLOGY

KITEC microelectronic technologies

Panasonic

semi

Wi-Fi sponsor

BROLIS SEMICONDUCTORS

Supported by

EPIC European Photonics Industry Consortium

Optimising metal alloy deposition with single-source evaporation

Highly uniform metal alloys of precise stoichiometry result from an optimally placed and replenished source in an electron-beam evaporator

BY KUOHSIUNG LI AND PHIL GREENE FROM FERROTEC

Figure 1. Ferrotec's Temescal UEFC-4900 electron-beam evaporator with HULA planetary domes.

SMARTPHONES have freed us from the confines of physical location, allowing us to expand communication and commerce with many distant people or enterprises simultaneously or in rapid succession. Fifth Generation (5G) mobile networks to be rolled out by 2020 will offer tremendous improvement, increasing spectral efficiency 1000 fold, compared to today's widely deployed 4G LTE network. This feat of mobile communication gives us instantaneous 'virtual presence' anytime, anywhere even as we travel the globe. The 5G implementation will place an ever higher premium on spectrum utilization, promoting a broader deployment of acoustic wave filters and resonators in mobile devices to minimize interference among the expanding range of tightly packed frequency bands. For example, 15 to 50 acoustic wave devices are now commonly utilized in a high-end smartphone.

Surface acoustic wave (SAW) devices, key components in most smartphones, often utilize electrodes made of metal alloy to achieve a composite of desirable characteristics. For example, AlCu is a common material for the interdigital transducer in a SAW device. Rich in aluminium, this alloy is hence endowed with the desirable characteristics of low electrical resistivity and low density for

Advanced Energy

WE POWER INNOVATION

ULTRA-FAST. ACCURATE. REPEATABLE.

PYROMETER TEMPERATURE MEASUREMENT

Advanced Energy's new **SEKIDENKO MXE G2** pyrometer combines high-speed temperature and reflectance measurement for industry-leading performance.

- Up to 10 kHz temperature and reflectivity measurement for high-speed applications
- RTP, MOCVD for LED production, epitaxy, and III-V materials
- Measurement wavelength (λ) configurable for a variety of substrates, including Si, SiC, GaAs, graphite, and sapphire
- Temperatures up to 1500°C
- Integrated optical sensor or fiber optic sensor available

To accelerate development cycles, build process understanding, and increase production yield and throughput, **visit us at:**

advanced-energy.com/cs

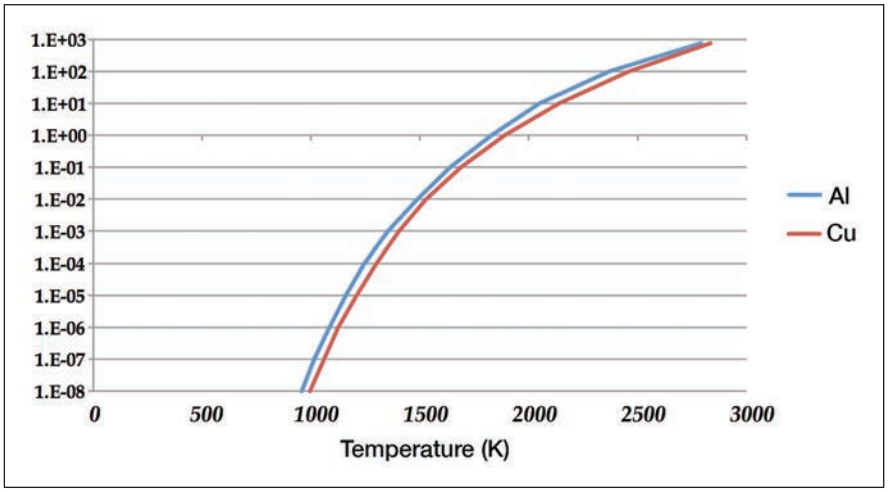


Figure 2. The vapour pressures of aluminium and copper are plotted in log scale as a function of temperature.

optimal frequency response. The role of copper, which accounts for only about 2 percent of the weight of the AlCu alloy, is to serve as a 'glue' between the aluminium grains to reduce hillock and void formation. This improves device reliability by inhibiting electromigration, which can move grain boundaries at high temperatures or high powers. Two percent is the sweet spot in copper concentration. Adding more copper will result in a rise in electrical resistance and too little (<1 percent) copper will render the copper ineffective.

Ferrotec's new generation Temescal evaporators, featuring HULA (High Uniformity Lift-off Assembly) planetary domes, present the solution to the historical challenges on the deposition of metal alloys by either sputtering or co-evaporation. The double-axis planetary rotating wafer domes result in exceptional thickness uniformity within wafers and from wafer to wafer (see Figure 1). Reliable process recipes are further developed for precise stoichiometry control for the single-source electron-beam evaporation of metal alloys.

Sputtering setbacks

Single-source evaporation, the approach we advocate for the deposition of many metal alloys, has been historically overshadowed by sputtering and co-evaporation. In the silicon IC industry, sputtering of AlCu is especially popular. However, unlike electron-beam evaporation, the non-directionality of sputtering makes it an inherently poor choice for the metal lift-off process commonly adopted in the compound semiconductor and acoustic wave industry. One of the biggest drawbacks of non-directionality is that it gives rise to sidewall coverage of metal on photoresist. After the lift-off process with the removal of photoresist, metal 'wings' are left loosely attached to metal features. The resulting yield loss from shorting and defects caused by these metal 'wings' is a particularly onerous problem for the tightly packed interdigital transducer fingers in acoustic wave devices.

Target erosion is another challenge engineers must contend with throughout the lifetime of the sputter target. Since the shape of the target changes over time, the deposition rate for a given process recipe will drift over time as well. As a consequence, sputter process engineers resort to continuously adjusting the process time and/or target power in order to control the deposition rate (and

	Sputtering	Co-evaporation	Single-Source Evaporation using HULA
Lift-off Quality	Poor	Good (Excellent for high ratio alloy)	Excellent
Control of Feature Size	Poor	Good (Excellent for high ratio alloy)	Excellent
Repeatability of Process Recipe	Adjustment throughout target life	Excellent	Excellent
Stoichiometry Control	Excellent	Poor	Excellent
Batch Size	6	25	25
Throughput	Poor	Excellent	Excellent
System Cost	100%	25%	25%
Cost of Ownership	Poor	Good	Excellent

Right: Table 1. Comparative analysis on the deposition approaches of metal alloys in a lift-off process for 6 chamber single-wafer sputtering and Ferrotec's UEFC-4900 (for either co-evaporation or single-source evaporation).

thickness) from wafer lot to wafer lot. Automated adjustment to the changing deposition rate has been recently developed to reduce the significant down time of sputtering systems and the expenditure of engineering resource (as well as test wafers) caused by the manual adjustment process. However, implementing the automated adjustment requires first monitoring the drift in thickness throughout the lifetimes of several targets, and must be done independently for each target type.

In contrast, Ferrotec's Temescal evaporators actively and continuously monitor the deposition rate to facilitate efficient production. This enables the user to simply set the deposition rate in the recipe. The execution of an automatic process parameter feedback loop will maintain the rate at the set point. As an option, our electron-beam source could also be replenished by wire feeding under high vacuum in the source chamber. The frequent wire feeding or source replenishment maintains the source in the same state and gives rise to very consistent run-to-run repeatability.

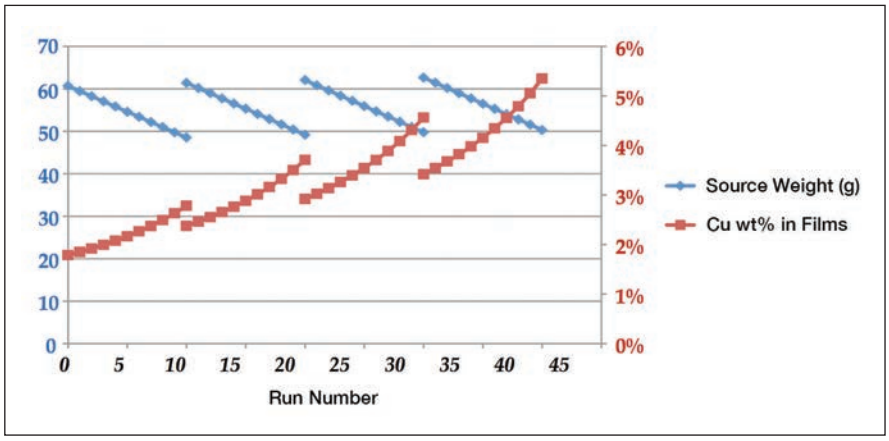


Figure 3. The undesirable effect of replenishing the crucible pocket with material of the same copper concentration as used initially.

Co-evaporation conundrum

Co-evaporation is sometimes employed to simultaneously deposit different materials from two separate electron-beam sources. However, this automatically necessitates the placement of either one or both sources somewhat off the optimal central axis of the dome sphere. The displacement from the central axis will then distort the orthogonal directionality from the source to the substrates and may cause yield loss in the metal lift-off process.

Another drawback of co-evaporation is the difficulty in process control. In the example of AlCu (98 percent/2 percent by weight), the large ratio of aluminium versus copper means that for a total film thickness of 200 nm the effective copper thickness needed is only 1.2 nm. If the aluminium is deposited at 1 nm/s, the copper needs to be evaporated at an exceedingly low rate of 0.006 nm/s. This makes the repeatability of AlCu co-evaporation very challenging to control. Furthermore, in order to ensure a consistent stoichiometry throughout the film, growth rates must not change significantly during the deposition process. Otherwise, rate variation in one source would necessitate the rate alteration of the second source to mirror the change.

The new generation of Temescal evaporators avoids all the above-mentioned issues from sputtering and co-evaporation. Ferrotec's HULA evaporators enable uniform deposition from a single AlCu source located at the very centre of the dome sphere for orthogonal directionality and excellent lift-off yield.

A set of planetary rotating wafer carrier domes change the location of each wafer relative to the evaporants in the source crucible continuously to ensure the utmost within-wafer and wafer-to-wafer uniformity of both thickness and composition via a contactless magnetic drive that generates no particles. The planetary domes are both self rotating and rotating around the central axis to provide each wafer with the same exposure to the source in distance and angles over the evaporation period.

All of these benefits are highly affordable. At about a quarter of the cost of a cluster sputtering tool, Ferrotec's UEFC-4900 evaporators deliver better lift-off and deposition control. Furthermore, they

> "A great strength of the HULA system is its planetary motion. Wafers that could only reside in the richer or poorer copper regions in a single-axis system can now share time in both regions. So advantageous is this location-averaging approach that it minimizes the deviation in within-wafer composition to typically below the limit of detection."

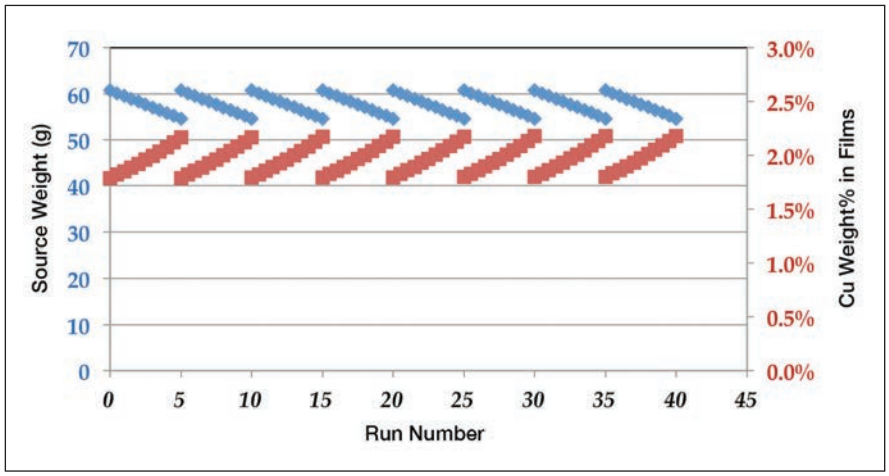


Figure 4. Frequent source replenishment with the AlCu of the correct composition minimises variations in the weight percentage of copper in AlCu films.

offer a far higher throughput than a single-wafer, six-chamber sputtering tool. In the case of an AlCu metal alloy with a high concentration ratio, single-source evaporation is better for the stoichiometry control and overall cost of ownership compared to co-evaporation (see table 1 for an overview of the pros and cons of sputtering, co-evaporation and single-source evaporation).

Single-source supremacy

Single-source evaporation has been used for many years for the deposition of NiCr and AuGe. One of the challenges of this approach is that the elements in the alloys can have distinctly different vapour pressures at a given temperature, leading to the formation of films with a notably different composition ratio from the starting source material. This difference is resulted from the difference in the partial pressures of the materials when mixed together at the evaporation temperature – these pressures can even differ from the partial pressure of the elements in their pure forms.

Fortunately for commonly evaporated alloys, either the partial pressures are not too disparate from one another, or there is a wide tolerance on the film's acceptable composition ratio.
The good news for AlCu is that the vapour pressures of the individual elements are relatively close over a wide range of temperatures (see Figure 2). These curves suggest that an AlCu source consisting of 98 percent aluminium and 2 percent copper (by weight) would initially produce a film of about 99.3 percent aluminium and 0.7 percent copper. That's not far from the composition obtained in practice, which has a typical copper concentration of 0.4 percent.

Obviously, in order to deposit a film with 2 percent copper by weight, the source must have a significantly higher copper concentration. It is quite feasible to determine the exact composition – modelling source behaviour using vapour pressure curves with a couple of empirical fitting terms gives a good indication of the relationship between the composition of the source and the resulting film.

Selecting the source's right initial composition is only the starting point for ensuring the desired film composition. That's because during evaporation, aluminium evaporates more readily than copper, leading to a gradual change in source stoichiometry. This deviation is exacerbated if the crucible is replenished after partial depletion with material of the same copper concentration as used initially (see Figure 3, which shows the modelled results).

The solution is to replenish the crucible pocket with an alloy composition that maintains the intended copper composition in the films. It is possible to understand the relationship between the weight of the source and the copper content in films as the source is regularly replenished with the alloy of correct concentration (see Figure 4).

Although it is not possible to eliminate the variation in the copper content completely as material is evaporated from the source, these deviations can be

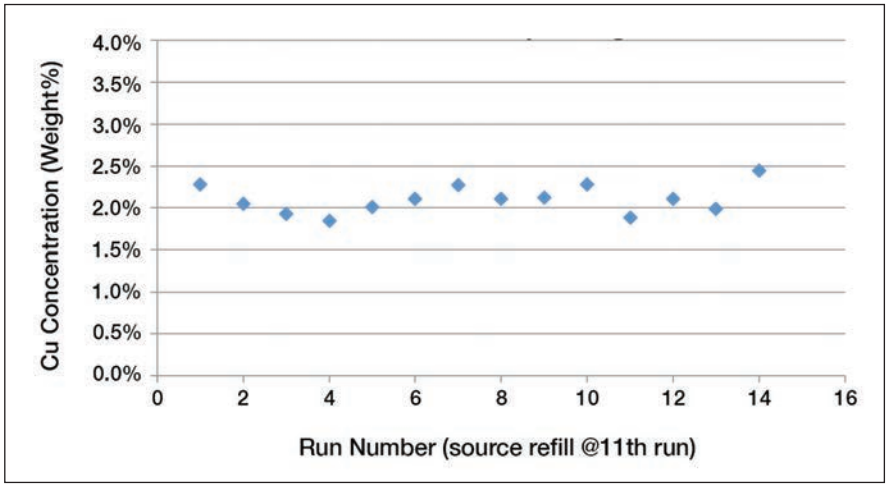


Figure 5. AlCu run-to-run stoichiometry control with a refill of the source crucible before the 11th run.

controlled to within a relatively tight range by frequent source replenishments.

Location, location, location

Ferrotec is not the first company to launch a planetary evaporator. A number of them were already on the market in 2011, when we launched our new generation of evaporators that feature the HULA planetary domes.

However, one critical difference is that the source crucible is placed at the centre of Knudsen sphere in HULA evaporators instead of the edge. A Knudsen sphere is characterized by uniform thickness across any point on the sphere from an evaporating source placed on any fixed point on the sphere. The central location of the source in the HULA evaporators facilitates orthogonal deposition and higher lift-off yield.

With Ferrotec's HULA systems, process engineers can typically achieve within-wafer uniformities for elemental metals of 2 percent, and wafer-to-wafer uniformities of 1 percent. The planetary HULA evaporators particularly excel at the deposition of ultra-thin film (5 nm or less) and typically the uniformities for platinum and nickel are better than 0.5 percent. In the case of AlCu (98 percent/2 percent by weight), the standard deviation of the run-to-run copper concentration is 0.2 percent (see Figure 5), and the within-wafer and run-to-run thickness uniformity are about 1 percent.

The high degree of uniformity, in both composition and thickness, results from the planetary motion of the HULA domes. The pair of elements that make up an alloy source evaporate with different angular distributions, and in the case of AlCu, copper varies more rapidly with angle than aluminium. With single-source evaporation of an alloy, it is not possible to use a different uniformity mask for each element. Consequently, a traditional single-axis system could only maintain a specified aluminium-to-copper ratio over a limited range of deposition angles (see Figure 6 for details). This greatly limits the number of wafers that can be coated at a time.

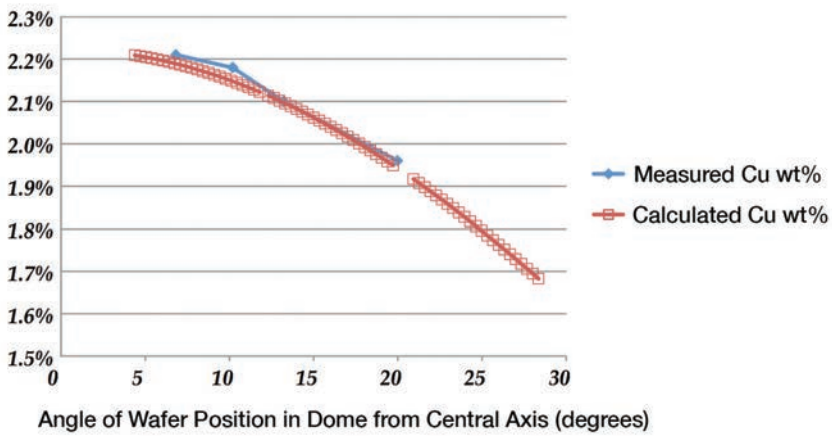


Figure 6. The copper concentration in an AlCu alloy (98%/2%) decreases with evaporation angle in a single-axis dome.

A great strength of the HULA system is its planetary motion. Wafers that could only reside in the richer or poorer copper regions in a single-axis system can now share time in both regions. So advantageous is this location-averaging approach that it minimizes the deviation in within-wafer composition to typically below the limit of detection. Simulation from vapour cloud models further confers that the variation is less than 0.1 percent.

The capability of Ferrotec's Temescal evaporators is also underlined by calculations of the variation in composition of the AuSn eutectic alloy. According to our calculation, the standard deviation in uniformity of AuSn (80 percent/20 percent) is as low as 0.02 percent within-wafer, even without the use of a uniformity mask. The thickness variation is also impressive, with wafer-to-wafer variations for both gold and tin of 0.3 percent, which ensures a highly consistent stoichiometry. This attribute is valued highly, because a 0.75 percent reduction in tin concentration could increase the eutectic melting temperature by 30 °C. With Ferrotec's HULA system, minimising variations in composition ensures uniformity of the eutectic melting temperature, and ultimately plays a significant role in realising high bonding quality.

In summary, two key innovations are incorporated into Ferrotec's Temescal electron-beam evaporators. The first patented technology is double-axis planetary rotating domes with the source crucible at the centre of the Knudsen sphere for orthogonal, directional evaporation.

The second patented technology is the conic chamber that takes into account the shape of evaporated vapour cloud and minimizes the volume and surface area of the product chamber to reduce the pump down time. The typical pump down time to 1 x 10^{-6} Torr for a Temescal UEFC-4900 with 25 6-inch wafer batch size is 18 minutes and for a Temescal UEFC-5700 with 42 6-inch wafer batch size is 11 minutes. Ferrotec's Temescal systems are therefore the best choice for the deposition of a metal alloy in a lift-off process.

Further reading

C. Weng *et. al.* 2015 CS MANTECH Conference
H. Lichtenberger *et. al.* 2012 CS MANTECH Conference

Nanowire FETs for future logic

To maintain the march of Moore's law, silicon foundries may introduce germanium and III-V nanowire FETs at the 5 nm node

BY RICHARD STEVENSON

I BET THAT before you shut the front door, you check that you have your essential items with you. Keys? Yes. Wallet? Yes. Smartphone?

If you have forgotten the latter, it's back inside to hunt for it. And I suggest that you head first for the charger, as there is a good chance that it'll be hooked up there, getting the juice that it needs to last through the day.

This scenario illustrates our love-hate relationship with our mobiles. We cherish them for providing us with entertainment and communication on the go, but are frustrated by battery levels that plummet far too fast.

So, if the makers of smartphones are going to tempt us to splash out on a new model with superior capability, this replacement must not compromise battery life. And that means that its microprocessor must draw no more power than its predecessor, while packing a greater punch, in terms of computing power, thanks to an increase in transistor count.

Since the birth of the silicon industry, increases in IC transistor count have been driven by the introduction of smaller devices consuming less power. Miniaturisation of the transistor has enabled it to operate at a lower voltage, which is a big deal, because active power has a quadratic dependence on the operating voltage.

Unfortunately, it is getting ever harder to reduce the voltage of the silicon MOFSET while maintaining its performance. This impending roadblock has motivated an interest in alternative devices, which feature channels sporting higher mobility materials, such as germanium and the III-Vs. These devices can operate at lower voltages than silicon equivalents, while maintaining their performance.

A great place to find out about the latest developments in non-silicon MOSFETs is the International Electron Devices Meeting (IEDM). Held most-recently in Washington on 7-9 December 2015, delegates at this meeting got to hear about a variety of novel nanowire FETs with the potential to succeed the latest generation of silicon MOSFETs, which are three-dimensional devices with a protruding fin. At IEDM imec reported its latest results with InGaAs nanowire *n*FETs; Peide Ye from Purdue announced the fabrication of a CMOS inverter from germanium nanowire *p*FETs and *n*FETs; and a group from Singapore revealed how to make III-V nanowire *p*FETs and *n*FETs on a substrate sporting an incredibly thin buffer layer.

As a developer of finFETs and silicon and non-silicon nanowire FETs, the European microelectronics centre imec is in a great position to evaluate the prospects for all these technologies.

Discussing this in an interview with *Compound Semiconductor* magazine, Vice-President of Logic at imec, Aaron Thean, said that he expects the silicon finFET to be the dominant technology at the 10 nm node, and also at the 7 nm node, where there might be an introduction of a SiGe channel. "Beyond that, we are out of knobs," explained Thean, arguing that the 'electrostatics' degrade, leading to a hike in leakage current. "It turns out that with the tri-gate structures, the top gate does have electrostatic control – but the taller the fin, the further [the gate] is from the bottom of the fin."

To improve electrostatics at the 5 nm node, the device architecture must move to a nanowire transistor – with this design, the gate wraps all around the channel. Researchers at imec are already evaluating

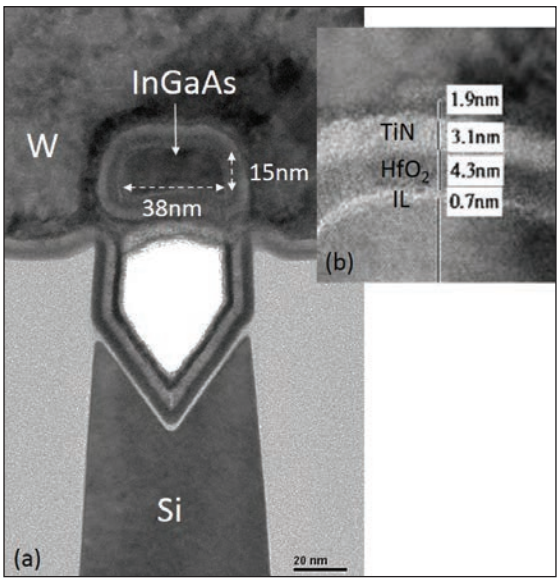
The most recent IEEE International Electron Devices Meeting was held at the Washington Hilton from 7-9 December 2015.

the capability of silicon nanowire transistors, as well as variants incorporating III-Vs for the *n*FETs and germanium for the *p*FETs. In all cases, efforts include the development of a high-yield manufacturing process that can churn out reliable circuits incorporating *p*-type and *n*-type devices in the world's leading foundries.

If these chipmakers are to switch to alternative channel materials in the 2020s, processes will have to be developed that enable device production on silicon substrates with diameters of 300 mm or more. And this is challenging, because there are significant differences between the atomic spacing found in crystalline silicon and that of the alternative channel materials. Due to these differences, when a III-V or germanium is deposited directly on a silicon substrate, strain builds up in the epilayer that leads to device-destroying defects.

At imec, researchers have been working for several years to develop a technology for forming high-quality III-V and germanium devices on silicon substrates. Progress led to the development of a process for making finFETs with non-silicon channels, and this now forms the basis for the production of nanowire transistors.

Fabrication begins by forming trenches in a widely available form of silicon wafer that features shallow trench isolation. With this form of engineered substrate, there are trenches made from silicon, separated by regions of silicon dioxide. The silicon is etched away to create trenches that have V-shaped grooves at the bottom. Depositing InP in these furrows leads to the creation of defects, due to the 8 percent lattice mismatch with silicon. However, the defects – missing planes of atoms aligned at about 45 degrees to the wafer surface – terminate at the trench walls, enabling the growth of high-quality material near the wafer surface.



The imec-led team produced InGaAs nanowire FETs by growing material in trenches with a V-shaped bottom, and then etching material.

InGaAs is grown on top of the InP column, before the latter is removed. Following fabrication of a gate stack, nanowire FETs are formed with a gate length of 50 nm.

In 2014, the team reported early results with this process in the journal *Electron Device Letters*. Since then, improvements have been made to the gate stack, thanks to a strong collaboration with ASM.

Niamh Waldron, a Principal Engineer at imec, and lead-author of the paper describing this work at IEDM, believes that the latest devices represent a major breakthrough, because the performance of these III-V transistors is as good as those made on native substrates.

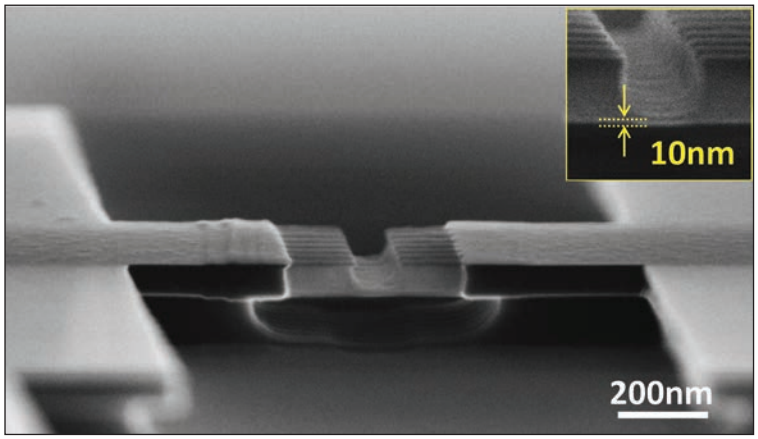
What makes this result even more impressive is that it has been realised on a 300 mm line, using foundry tools. "You are always more worried about process damage, defects in the epi, and whether you can get there in the end," says Waldron.

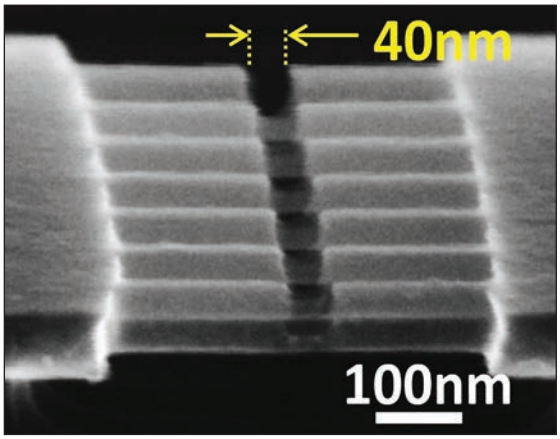
Her claim of a nanowire MOSFET performance that is equal to that of III-V devices is based on a figure for gate transconductance, which reflects the mobility in the channel. In imec's devices, this is 2200 μS/μm for an operating voltage of 0.5 V, which is about two-thirds of the voltage used in circuits made with Intel's 14 nm finFET process.

Another important figure-of-merit for the transistor is its sub-threshold swing. This assesses the quality of the transition between the on-state and the off-state.

The value of the sub-threshold swing plays a critical role in attempts to reduce the operating voltage for the circuit, so that its power consumption falls. If the supply voltage is reduced while the threshold voltage is kept constant, this cuts the current flowing through the device. The obvious way to address this is to trim both the supply voltage and the threshold voltage, but cutting the latter increases leakage. What is actually needed is to introduce devices with a steeper sub-threshold swing, because this allows transistors to operate at a lower threshold voltage while producing the same level of leakage.

For a MOSFET, carrier statistics govern the lowest possible value for the sub-threshold swing: it is 60 mV/decade. For the imec device, the sub-threshold swing is significantly above this, at 110 mV/decade. So, if these devices are to be used in ICs, this value will have to come down. This should not prove too tricky, however, as in 2014, in *Electron Device Letters*, the team reported 4 nm InGaAs nanowires with a sub-threshold swing of about 65 mV/decade. "But we didn't get the on-performance," says Waldron. "It's all about getting good on-performance and the off-state. This is where we have to start thinking outside the box for good passivation, so we can achieve both at the same time."





Peide Ye's team has developed processes to form germanium nanowire nFETs and pFETs, and used this to make inverter circuits.

Thean believes that at the 5 nm node and below, if III-V and germanium nanowire FETs are introduced in foundries, they will not completely replace those made from silicon. Instead, he expects all three devices to co-exist, due to concerns relating to leakage currents: "Anything that is 10 nA and below is very difficult to get with germanium or the III-Vs, and its hard to imagine that people will not care about leakage in the future."

An all III-V approach

Pioneering an approach with III-V *n*FETs and III-V *p*FETs is a collaboration between at team led by Yeo Yee-Chia and Gong Xiao at the National University of Singapore (NUS) and Yoon Soon-Fatt's group Nanyang Technological University (NTU).

"InGaAs is a promising material for *n*FETs, however it is not suitable for *p*FETs, because it has a very low hole mobility," says Gong Xiao from NUS. "So we needed another material for the *p*FET. In this work, we used GaSb, which has a higher hole mobility."

To form these transistors on silicon, engineers insert a buffer structure between the devices and the substrate. This approach is well known, but the buffer used by the Singapore team is much thinner than usual: it is just 150 nm-thick, compared to a typical value of around 1 μm.

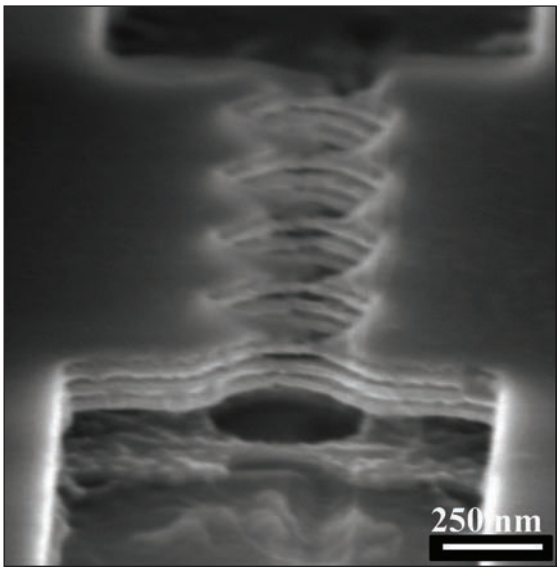
Another strong feature of this work is the architecture of the MOSFET. According to Xiao, if a single nanowire were used to replace a fin, the current that would be delivered would be compromised, due to the reduction in the volume of charge-carrying material. "That's why the nanowires have to be stacked, in order to deliver a high current within a certain footprint. In this work, we not only realised the InAs *n*FET together with the GaSb *p*FET, we made both of them vertically stacked."

Development of the thin buffer technology, which enables significant cost savings associated with less material usage and a higher tool throughput, took place in Yoon Soon-Fatt's group. Here, they started with a 6° offcut germanium-on-insulator wafer with a silicon base and deposited, via MBE, a 70 nm-thick layer of GaAs, followed by a 50 nm-thick layer of GaSb.

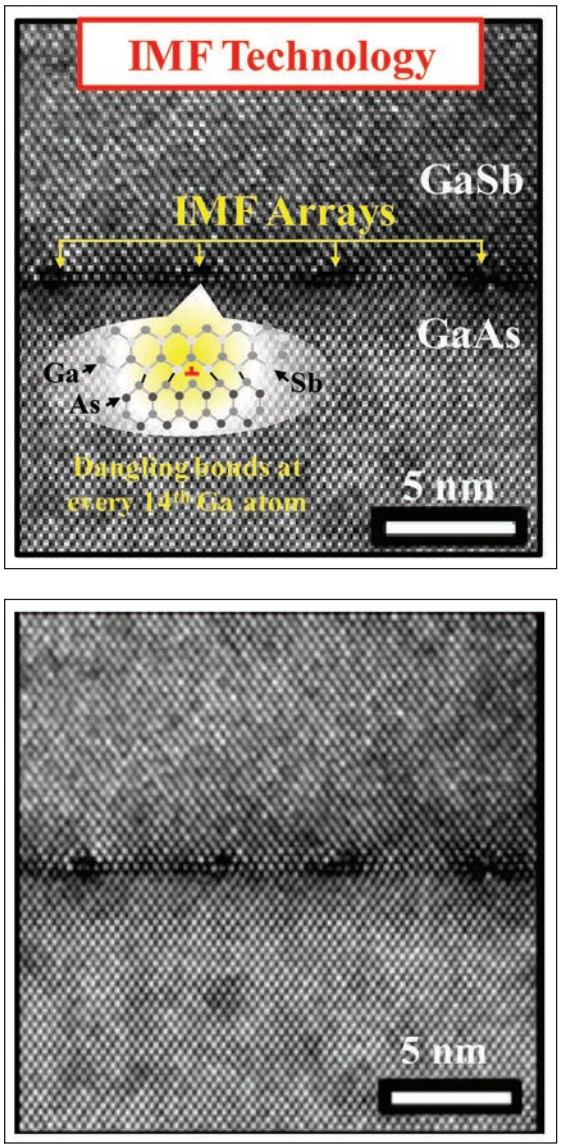
"Under proper growth technology, dangling bonds will form at every fourteenth gallium atom site, to accommodate the large lattice mismatch between GaAs and GaSb," explains Xiao. Defects that result from dangling gallium bonds are confined to the interface, while high-quality material is present 10 nm away from this.

The team produced nanowire FETs from these wafers. Operating at 0.5 V, a *p*FET and an *n*FET with a channel length of 500 nm and 20 nm produced a sub-threshold swing of 188 mV/decade and 126 mV/decade, respectively. Values for transconductance were not reported.

It is not surprising that the device results need to be improved, as this work is still in its infancy. Xiao says that there are plans to: refine the gate stack, which should lead to an increase in the drive current; and to work with better epiwafers. The first devices were made with wafers with a 2.6 nm surface roughness, but recently the team from NTU improved its growth



Vertically stacking nanowires, an approach pursued by researchers from Singapore, enables an increase in current density from the footprint of the device.



High-resolution transmission electron microscopy reveals how interfacial misfit defects can address the issue of strain resulting from the growth of III-Vs onto germanium films.

process, leading to a reduction in roughness to 0.5 nm. "In future we will use these wafers to do device fabrication," says Xiao.

Switching to germanium

Choosing the right material for the *n*FET and *p*FET is a dilemma that Ye has mulled over for a long time. He has been working with III-V transistors for the last 15 years, and has recently expanded his research effort to encompass devices made from germanium, which is an easier material to process.

With germanium, it's easy to make a *p*FET – and much, much harder to make an *n*FET. There are issues associated with Fermi-level pinning that make it very challenging to produce a good *n*-type contact.

"Two-and-a-half years ago, one of my PhD students took a very, very simple approach – he tried to make the *n*-contact using a high doping concentration," explains Ye. "All of a sudden we moved the current one order of magnitude higher than anyone else."

This accomplishment provided the springboard for the first CMOS process for a planar device, followed by the first finFET with germanium CMOS, and now, announced at the recent IEDM, the first nanowire-based germanium CMOS. With this technology, sub-threshold swing for the *n*FET is just 64 mV/decade, and transconductance is 1057 μS/μm. Combining this with a *p*FET enabled the fabrication of an inverter circuit, operating at 1 V, that produced a maximum voltage gain of 54 V/V. Ye claims that this gain is close to that delivered by state-of-the-art silicon nanowire CMOS inverters, and says that he hopes to reduce the operating voltage of his circuits to 0.5 V.

Before Ye's germanium FETs could be introduced in foundries, their dimensions would need to shrink – but not by that much. For example, the width of the nanowires would only need to reduce from 10 nm to about 6 nm, if they were to be introduced at the 7 nm node.

One appealing aspect of Ye's process is that it does not require epitaxial steps. His team uses 200 mm wafers made by Soitec, which feature insulating and germanium layers on a silicon substrate. There is nothing to stop the production of 300 mm variants for processing in the world's leading foundries.

A noteworthy difference between the process used at Purdue and that suitable for high-volume production is associated with the lithography step. The university team uses electron-beam lithography, rather than a self-alignment technique, and this leads to higher capacitances, which prevent measurements of the speed of the circuit.

In contrast, at imec all work is conducted with foundry tools, speeding the path from development to a manufacturing-ready process. Here, one of the biggest concerns for researchers working on III-V FETs is whether the defect level is sufficiently low.

"We have proved that the defectivity of our devices is quite good already," says Thean. "But it is still not completely clear that it is sufficient for a very dense circuit of the future." Efforts will be directed at developing superior techniques for measuring and quantifying defects, and evaluating the relationships between defects and device and circuit yield.

Before III-Vs and germanium nanowire FETs are produced in silicon foundries, there also needs to be an introduction of suitable processing equipment for epitaxial growth and passivation steps.

With the introduction of the 5 nm node around five years away, progress will have to be fast if non-silicon nanowires are to make an impact. But even if these devices miss this boat, they could still be a commercial success. "If you could co-integrate with silicon, you could do RF and other applications," reasons Thean.

Turbocharging the channel

Introducing new channel materials lays the groundwork for slashing the power consumption per transistor

BY SHENGKAI WANG FROM THE INSTITUTE OF MICROELECTRONICS AT CHINESE ACADEMY OF SCIENCES

BACK IN THE 1990s, many families would fork out on a new computer every year or so. Occasionally, they would do this because their current PC had stopped working; but more often they parted with their cash to get their hands on a machine that was faster, and capable of running more powerful software.

Fast-forward to today, and a similar state of affairs is at play. Now it is individuals rather than families that are parting with their earnings, and they are splashing out on better mobiles rather than new desktop PCs.

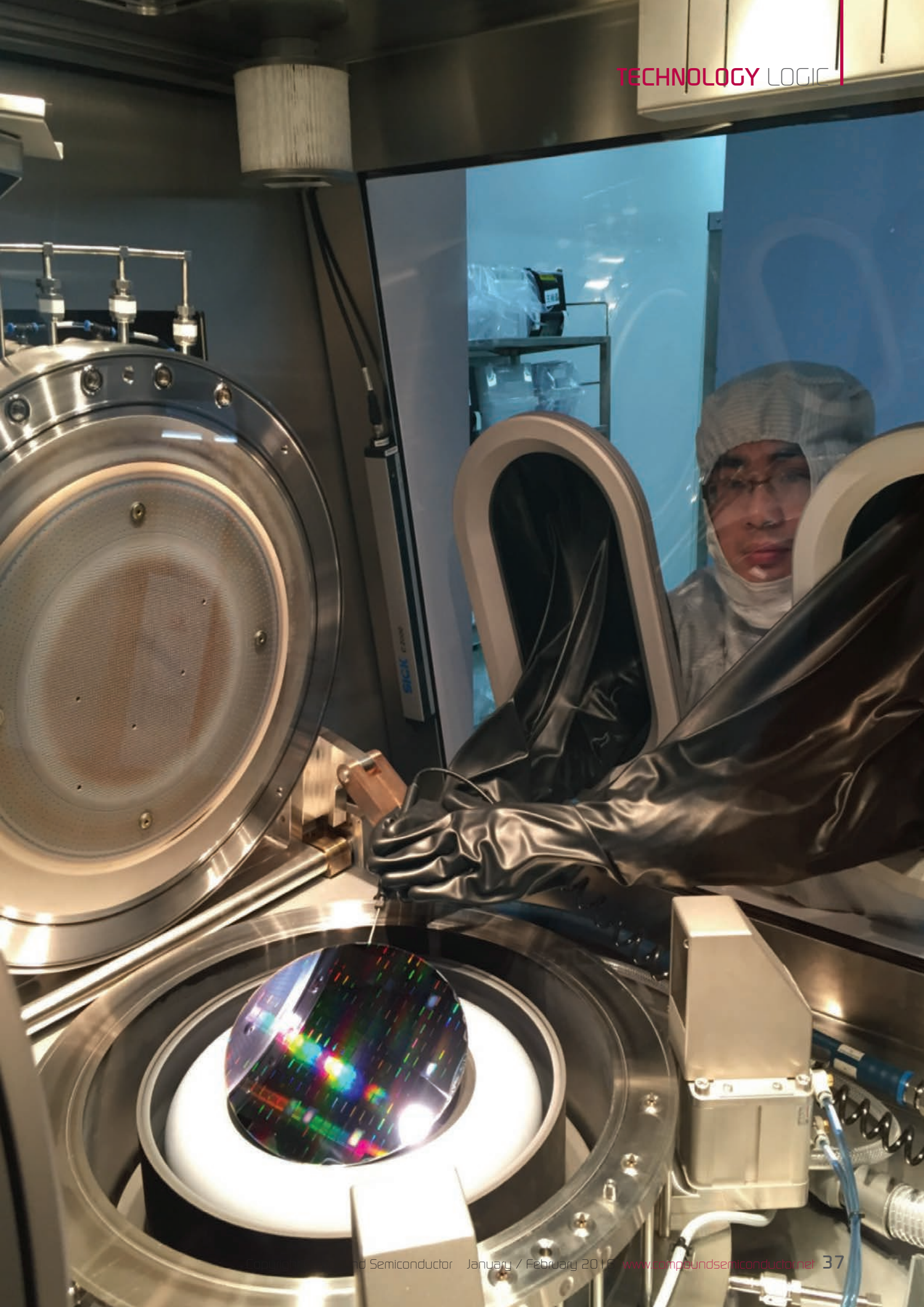
In both of these eras, advances in the performance of the microprocessor underpinned improvements in consumer hardware. Since the 1970s, transistors have got far better, while getting far smaller.

These phenomenal advances in performance will have come as no surprise to Gordon Moore, co-founder of Intel. Back in 1965 he predicted that the number of transistors on a chip will double roughly every two years.

This rate of progress, which is described by Moore's Law, has largely been driven by evolutionary progress in the basic technology – a silicon transistor sporting a silicon dioxide dielectric beneath the gate. However, to keep pace with Moore's Law during the last decade, this device has had to undergo some modifications, such as the introduction of strained silicon-on-insulator structures, high-κ/metal gate technology and non-planar transistor architectures.

Despite these refinements to silicon CMOS, the traditional advances in power consumption per transistor are stalling. This is a major concern, because rising smartphone sales have led to a shifting of priorities for the silicon IC – gains in performance are still valued, but more than ever before, a fall in power consumption per transistor must occur with every new node in order to ensure an acceptable battery life for the handset.

The well-trodden path to realising more efficient transistors is to trim their operating voltage. Today it



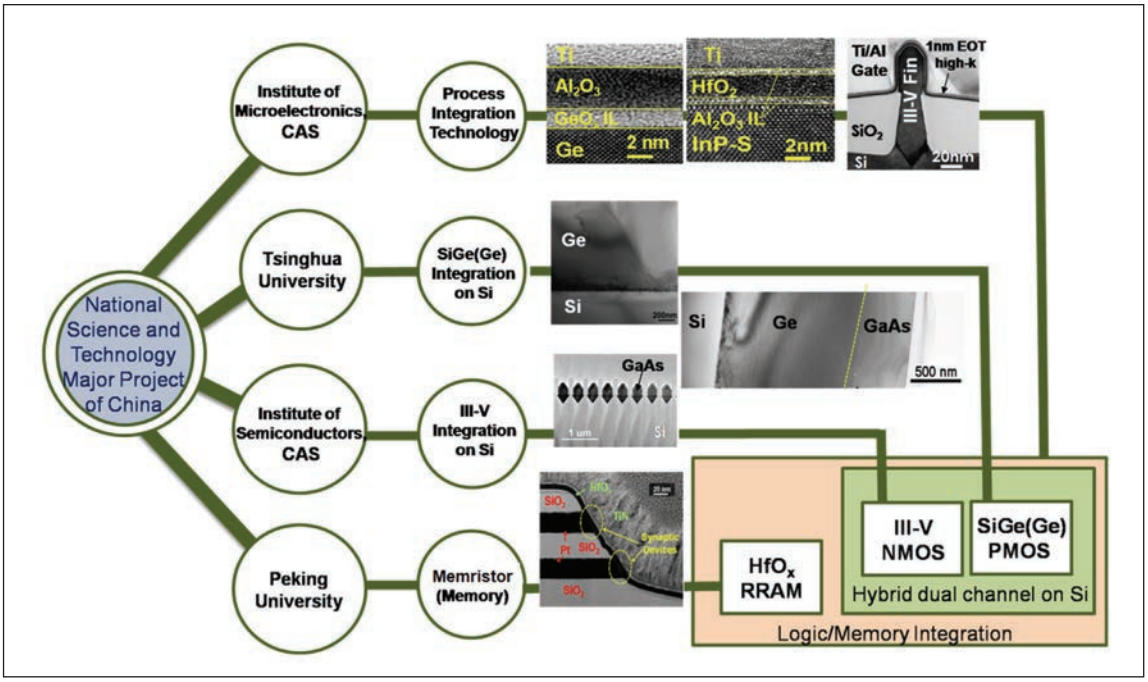
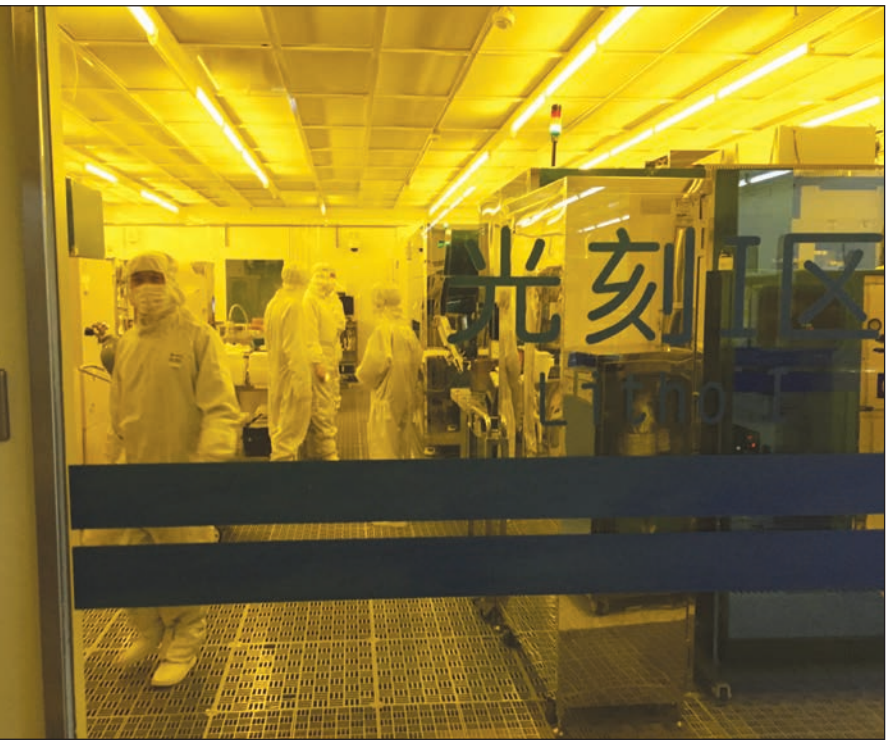


Figure. 1. Supported by the National Science and Technology Major Project of China, four institutions are working together in a project entitled 'Integration Technology for Silicon Based High Mobility Materials and Novel Devices' to develop technologies for next-generation ICs. Researchers at Tsinghua University are focusing on the integration and realization of high quality SiGe or germanium-on-silicon, while a team from the Institute of Semiconductors of CAS is grappling with how to integrate III-Vs with silicon; the Peking University team is concentrating on the memristor development using HfO_x-based resistive random-access memory (RRAM); and the team from the Institute of Microelectronics of CAS is working on process integration technology, including the high-κ stack engineering, and process integration technology development.



stands at 0.8-0.9 V, and the aim is to drive this down to 0.5 V.

One promising way to do this is to rip out the silicon channel and replace it with a material that transports carriers at higher speeds. Success hinges on replicating the high material quality found in the traditional pairing of silicon and SiO_2, a combination that allows charge carriers to pass through the channel without undergoing strong scattering.

With silicon, the electron mobility is a modest 1400 $cm^2 V^{-1} s^{-1}$, while for holes it is just 450 $cm^2 V^{-1} s^{-1}$. To go to higher speeds, this material could be replaced with a combination of III-V and group IV materials, which are strong candidates for future technology nodes. Of particular promise for next-generation logic is the combination of InGaAs, which could sit at the heart of *n*-type transistors, thanks to its electron mobility that can hit 10,000 $cm^2 V^{-1} s^{-1}$; and germanium, which could provide *p*-type transistors with a hole mobility in excess of 1900 $cm^2 V^{-1} s^{-1}$.

Before foundries can churn out hybrid, dual-channel CMOS circuits featuring very-large-scale integration

(VLSI), researchers in this field must find answers to several important questions. They include: How do you build high-quality interfaces that are comparable to those of SiO_2 and silicon? How do you form high-mobility channels with good crystalline quality on a silicon substrate? And how do you build nano-scaled devices based on III-Vs and germanium that are compatible with VLSI?

To try and find the answers to these questions, the Chinese government is backing a programme involving researchers from four institutions: the Institute of Semiconductors of the Chinese Academy of Sciences (CAS), Tsinghua University, the Institute of Microelectronics of CAS, and Peking University. Efforts by this team, which we are a part of, are paying dividends. Five years into an on-going fruitful collaboration, we have succeeded in developing novel engineered substrates and process technologies for high-volume, silicon foundry manufacturing of VLSI circuits featuring compound semiconductor materials (see Figure 1 for an overview of the roles of all the institutions involved in this project).

Gate stack engineering

One of the great strengths of the conventional transistor is the high quality of the interface between silicon and its native oxide. This enables suppression of channel scattering, which could arise from interface traps, and it ensures that MOSFETs produce a nearly ideal sub-threshold swing of 60 mV/dec. Thanks to this steep sub-threshold swing, the operating voltage can be trimmed while maintaining device performance.

It is not easy to replicate the quality of the silicon-SiO_2 gate stacks with germanium – and with III-Vs it is even harder. The interfaces between a high-κ dielectric and either germanium or a III-V have a higher thermodynamic instability than those formed from the traditional pairing of silicon and SiO_2, and this increases the interface trap density by one-to-two orders of magnitude (typical values are 10^{12} - 10^{13} cm^{-2} eV^{-1}). However, efforts by our group at the Institute of Microelectronics of CAS have shown that thermodynamic methods can address these interfacial issues.

Our team has formed NMOS devices that feature an InGaAs channel and a thin InP barrier. With this barrier the channel can be kept apart from the high-κ oxide interface, leading to higher electron mobility in the channel.

To prevent thermal damage to the devices, we use a low-temperature process to form the gate-stack. This process takes place at 300°C, and is based on the atomic layer deposition of Al_2O_3 onto a sulphur-passivated InP surface. By carrying out deposition at

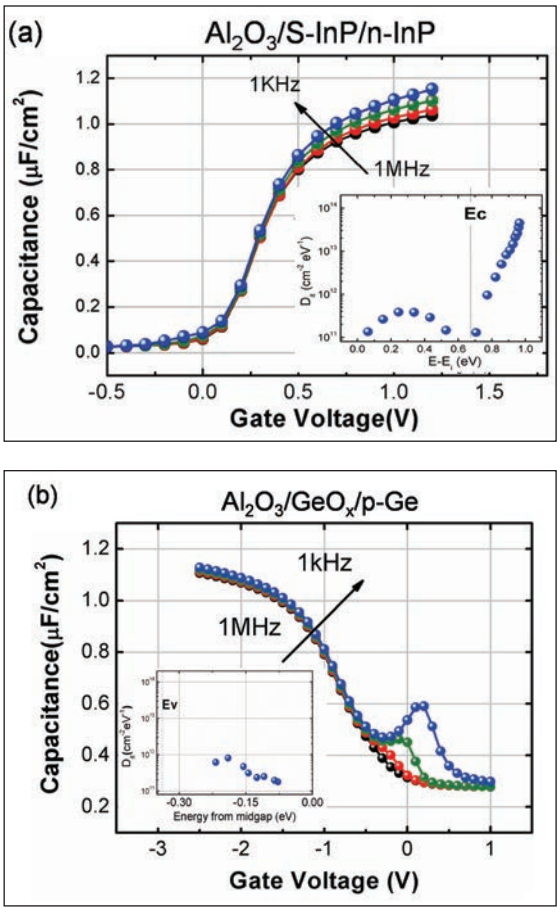


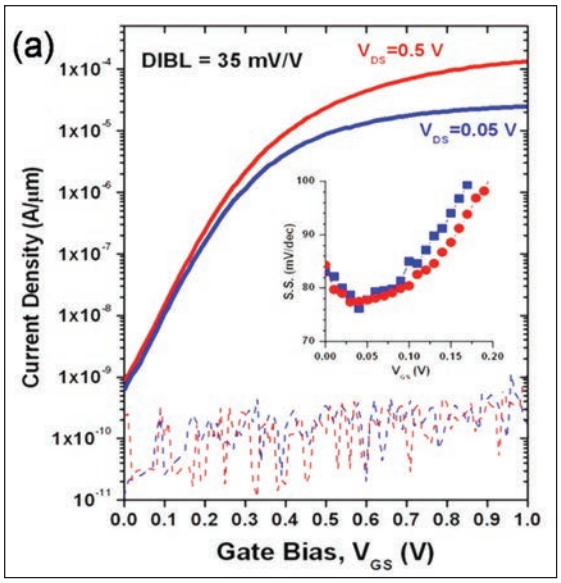
Figure 2. (a) Room-temperature multi-frequency capacitance-voltage characteristics of an Al/Al_2O_3/*n*-InP structure fabricated via a low-temperature process. The inset shows the corresponding distribution of interface trap densities across the bandgap. (b) Room-temperature, multi-frequency, capacitance-voltage characteristics of Ti/Al_2O_3/GeO_x/*p*-Ge fabricated by cycling ozone oxidation. The inset shows the corresponding distribution of interface trap densities across the bandgap.

significantly below 350°C, the temperature at which degradation of the high-κ/InP interface kicks in, we avoid emitting phosphorus atoms from the substrate.

The performance of our transistors is very encouraging. According to capacitance-voltage measurements at a range of frequencies, the interface trap density is 1.2 x $10^{11}$$cm^{-2}$ eV^{-1}. To our knowledge, that is the lowest value ever reported for high-κ/InP stacks.

Damage from high-temperature annealing is a common problem as it also degrades interfaces between germanium and high-κ dielectrics. To prevent this from occurring, we have inserted a high quality interfacial GeO_x layer between the high-κ dielectric and the germanium substrate. We introduce this with a cycling ozone oxidation method, which involves repeatedly depositing Al_2O_3 via atomic layer deposition and then performing *in-situ* ozone oxidation at about 300°C. Transistors that result have a very low density of interface traps, and capacitance-voltage characteristics that are dispersion free (see Figure 2 (b)).

Our efforts at developing high-quality interfaces



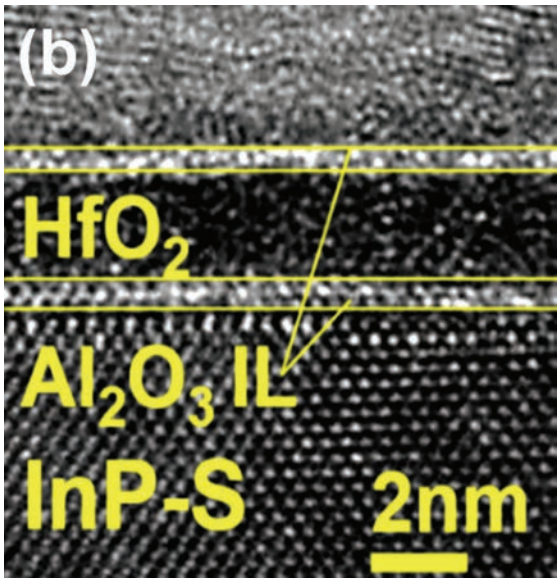


Figure 3. (a) Current-voltage characteristics for a 400 nm-long, enhance-mode, ultra-thin body nMOSFET featuring an InGaAs channel and an InP barrier layer. The on-off ratio is over 10^5, the average sub-threshold swing factor is typically 80mV/dec, and the drain-induced barrier lowering is around 35mV/V. (b) Cross-sectional transmission electron microscopy image of the optimized Ti/HfO_2/Al_2O_3/InP/InGaAs gate stack.

between a high-κ dielectric and epilayers of either germanium or InP have set the foundations for making high-speed *n*-type and *p*-type transistors that are free from significant scattering at interface traps. To showcase the potential of these devices, we have fabricated enhance-mode, 400 nm-long ultra-thin body MOSFETs that feature an InGaAs channel and an InP barrier. These devices deliver a very promising performance, including a sub-threshold swing of 80 mV/dec and a drain-induced barrier lowering that is typically 35 mV/V (see Figure 3).

Hetero-integration

The microelectronic industry is preparing itself for some colossal changes during the coming years. They will not, however, include a change in substrate. So, to enable III-Vs and IV-IVs to be integrated in CMOS production, these materials will have to be formed on a silicon substrate. This is not trivial, because the crystalline structures of germanium and the III-Vs differ from that of silicon.

Our colleagues at Tsinghua University have tackled this issue by developing a process for forming SiGe and germanium on silicon. They employ a cyclical approach; in the case of germanium this involves the growth of this material directly on a silicon (001) substrate at less than 400°C, followed by deposition at a far higher temperature, which can be between 600-670°C.

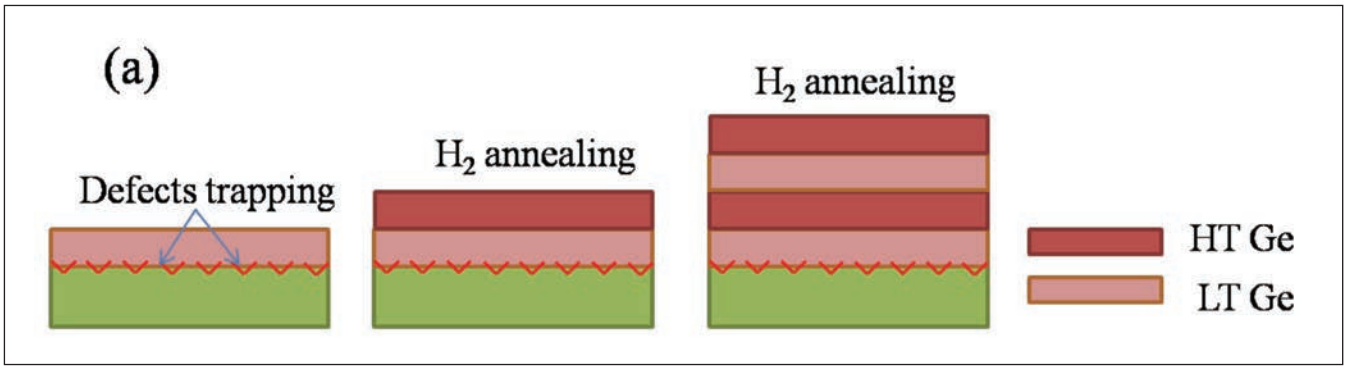
Low-temperature growth generates germanium monolayer islands. This is good news, because it suppresses further island growth and it supports a layer-by-layer growth mode. Note that care is needed to not drop the temperature too low, because this would hamper the formation of a smooth layer with good crystallinity (see Figure 4).

The low-temperature growth does have a downside, as it leads to a very high density of dislocations – they are typically 10^8 - 10^9 cm^{-2} – but this does allow high-temperature growth that follows to relax the maximum amount of strain. When the film is subsequently annealed under hydrogen at 750-825°C, dislocations glide and annihilate. This decreases their density and increases the degree of relaxation in the material. Films with a surface roughness of typically 0.5 nm result, which have a threading dislocation density below 10^5 cm^{-2}.

Within the programme, efforts at integrating III-Vs and silicon have been led by a team at the Institute of Semiconductors of CAS. They have adopted a two-pronged approach, pursuing direct epitaxy of GaAs on germanium/silicon virtual substrates and aspect ratio trapping (ART).

The direct epitaxy approach involves MOCVD of device-quality GaAs on germanium-on-miscut silicon. A high-quality top layer is realised with a two-step approach: a thin buffer is deposited at 360°C, followed by higher temperature growth; and polishing is then performed, followed by a second epitaxial growth. Merits of the thin buffer include the suppression of anti-phase boundaries and threading dislocations – the latter can reach 2.3×10^5 cm^{-2}, according to experiments involving potassium hydroxide etching.

Inspection of these GaAs-on-silicon films with a transmission electron microscope reveals the high quality in the top layers of the III-V (see Figure 5). The



surface roughness of these films can be below 1 nm, which is comparable with that of homo-epitaxial GaAs layers. The low density of defects in these epilayers, and their smooth surfaces, are attributes that are needed for making logic devices.

The biggest challenge for integrating a III-V on large silicon substrates is the significant lattice mismatch between the two materials. ART offers an elegant, cost-effective solution to this problem, and has been employed by researchers at the Institute of Semiconductors to realise selective area growth in 'V-shaped' trenches.

Efforts in this direction began by forming GaAs on silicon (001) using a two-step MOCVD process. Following on from this, high-quality films of InP, InGaAs, and InAs are sequentially grown in trenches lined with a GaAs buffer layer. The material quality of the films is very high, according to transmission electron microscopy (see Figure 6). This approach shows great promise for the realization of high-mobility devices for future CMOS technology nodes.

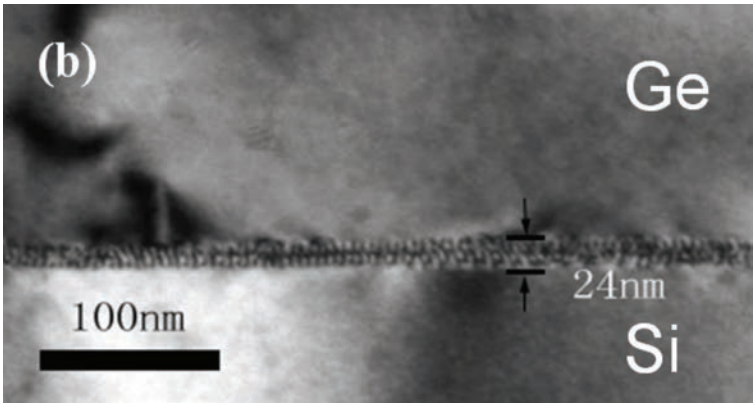


Figure 4. (a) Cycling between low-temperature and high-temperature growth of germanium leads to smooth, high-quality films. (b) Cross-sectional transmission electron microscopy reveals misfit dislocations trapped at the interface between germanium and silicon.

Building devices

Success in our programme has laid the groundwork for making devices. Well-tailored interfaces and high-quality hetero-material integration technology form the starting point for our construction of high-performance, low-power-consumption logic devices. We are also well positioned for trying to realise logic-memory integration on a silicon platform.

In 2014, our team at the Institute of Microelectronics CAS made our first attempt at fabricating small-sized III-V MOSFETs in our 8-inch line, which is intended for research and development. We found that a well-developed replaced-silicon fin technology held the key to realizing a 20 nm-width high-quality InGaAs-fin with an InP barrier layer. During this marriage of materials, which was accomplished on 8-inch silicon, dislocations were restricted to the SiO_2 trench, resulting in a high-quality 'head' (see Figure 7). Despite deploying an optimised, high-κ dielectric with an equivalent-oxide thickness of 1 nm, and a

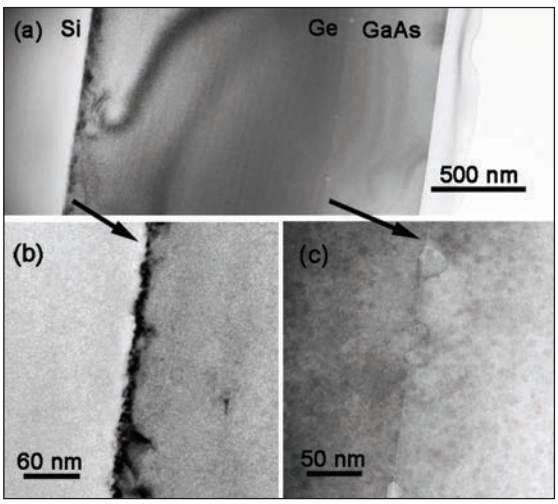


Figure 5. Cross-sectional transmission electron microscopy images highlight the high-quality of the of GaAs/germanium/silicon stack (a), and the interfaces between germanium and silicon (b), and GaAs and germanium (c).

> To make ICs, pMOS and nMOS devices must be formed side by side on the same wafer. In our programme, we grow germanium on silicon, and then add III-Vs to the germanium-on-silicon substrates by either direct epitaxy or ART. Germanium-pMOS transistors are formed first, because they need relatively high temperatures for p-type dopant activation and gate-stack annealing, such as typically 400°C

Ti/Al gate, transistors were hampered by issues arising from process integration, such as bulk leakage. We are working to address these weaknesses.

Our colleagues at Tsinghua University are focusing on PMOS devices, and are pioneering an architecture that promises to abolish the trade-off between performance and power consumption. This team has fabricated junctionless germanium-nanowire transistors on an extremely thin germanium-on-insulator substrate by carefully controlling wet etching. The devices that result have gate lengths and widths below 100 nm, and exhibit good electrical characteristics, such as an on-off drive current ratio of 10^5 at a drain voltage of -1V. These transistors are very promising candidates for PMOS devices in future microprocessors (see Figure 8). To make ICs, PMOS and NMOS devices must be formed side by side on the same wafer. In our programme, we grow germanium on silicon, and then add III-Vs to the germanium-on-silicon substrates by either direct epitaxy or ART. Germanium-PMOS transistors are formed first, because they need relatively high temperatures for *p*-type dopant activation and gate-stack annealing, such as typically 400°C. Fabrication of III-V NMOS devices follow, using InGaAs and an InP barrier layer. Dopants in these *n*-type devices do not require activation, because the source and the drain are formed by etching the epitaxy layer.

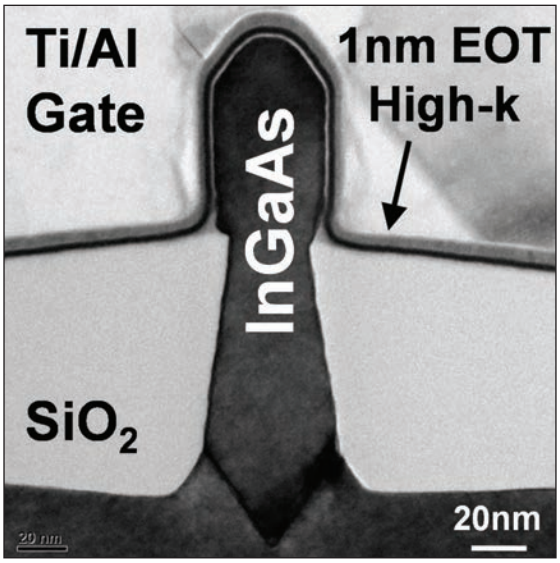


Figure 7. Cross-sectional transmission electron microscopy highlights one of the major successes of the Chinese program: fabrication of a 20 nm-width, high-quality InGaAs-fin (with InP barrier layer) on an 8-inch silicon wafer.

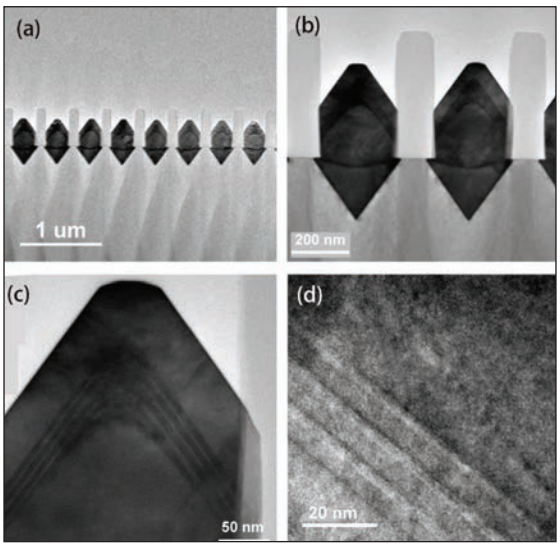


Figure 6. Transmission electron microscopy shows InGaAs multi-quantum wells that are formed in trenches by aspect ratio trapping, using InP and GaAs layers (a) and (b). The wells are uniform, according to images (c) and (d).

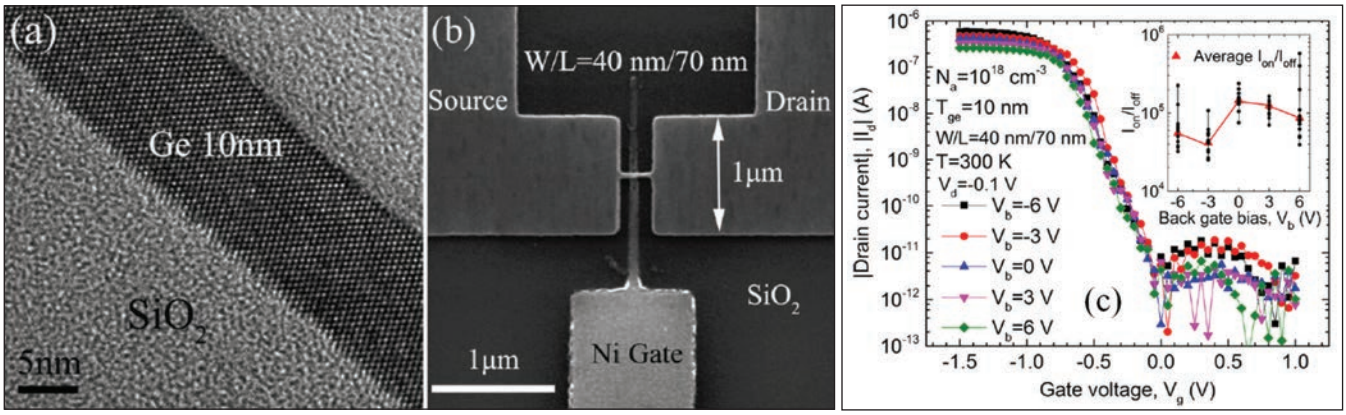


Figure 8. (a) Cross-sectional transmission electron microscopy of an ultra-thin body, germanium-on-insulator structure with a germanium film thinned to 10 nm. (b) Scanning electron microscopy of an ultra-thin body, germanium-on-insulator-based junction nanowire transistor with a 70 nm gate length and a channel width of 40 nm. (c) The back gate bias influences the current-voltage characteristics of this device. The inset shows the influence of bias voltage on the on-off current ratio at a drain voltage of -0.1 V.

Another avenue explored by our programme is the integration of logic-memory for the post 10 nm node. The high mobility of carriers in III-V and germanium channels enables high drive currents at relatively low operating voltages – and this makes this hybrid material approach attractive for both the construction of logic-memory integration blocks and the production of advanced memory devices.

One attractive candidate for next-generation microsystems is the hybrid crossbar memristor – also known as resistive random access memory – that is formed with a high-mobility MOS transistor array. Within our programme, a partnership between our group and a team from Peking University has developed an integration process for a HfO_2-based memristor and a germanium-based pMOS transistor. This effort involved fabricating a memristor with a $Pt/HfO_2/Al_2O_3/TaN$ structure on the drain side of a germanium-based pMOS transistor. With this device, turning the pMOS transistor to its on-state enables operation of the memristor (see Figure 9 for related current-voltage curves).

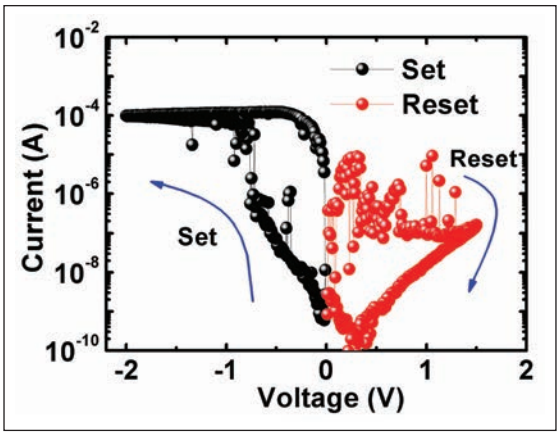


Figure 9. A typical current-voltage curve of HfO_2-based resistive switching device; the current was complied by a germanium-PMOS transistor. 'Set' means resistive switching from a high-resistive state to low-resistive state. 'Reset' means resistive switching from a low-resistive state to high-resistive state.

Our programme continues, and we are working towards several important goals. They include using our successes to date to demonstrate a dual-channel CMOS unit, and investigating in more detail device reliability, with a focus on the gate stack in both *p*-type and *n*-type transistors. Last but not least, we will start to consider making non-planar devices with germanium and III-V channels, as this is a very promising option for maintaining the march of Moore's law.

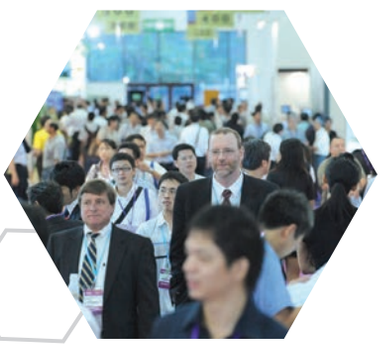
Further reading

S. K. Wang *et. al.* Appl. Phys. Express **8** 091201 (2015)
X. Yang *et. al.* Appl. Phys. Lett. **105** 092101 (2014)
X. Kong *et. al.* IEEE Trans. on Electron Devices **62** 1456 (2015)
S. Li *et. al.*J. Cryst. Growth **426** 147 (2015)
C. Sun *et. al.* Appl. Phys. Lett. **107** 132105 (2015)
C. Sun *et. al.* ECS Solid State Letters **4** 43 (2015)
H. Li *et. al.* Scientific reports **5** 13330 (2015)
B. Gao *et. al.* ACS Nano **8** 6998 (2014)
S. Li *et. al.* Appl. Phys. Lett. **108** 021902 (2016)

semi | Global Expositions

without limits.

EXPAND YOUR BUSINESS WORLDWIDE



Explore Opportunities Without Limits

Whether you are looking to explore new regions, technologies, or markets, SEMI Expositions are the ideal platform to showcase your brand, connect to customers, and grow your business worldwide. Let SEMI help you build an exhibition and marketing program that gains maximum exposure and takes your business to the next level!

Visit www.semiexpos.org

SEMI® Expositions Calendar

SEMICON Japan 2015
December 16–18
Tokyo Big Sight, Japan
www.semiconjapan.org

SEMICON China 2016
March 15–17
Shanghai, China
www.semiconchina.org

SEMICON Southeast Asia 2016
April 26–28
Penang, Malaysia
www.semiconsea.org

SEMICON Taiwan 2016
September 7–9
Taipei, Taiwan
www.semicontaiwan.org

SEMICON Korea 2016
January 27–29
Seoul, Korea
www.semiconkorea.org

FPD China 2016
March 15–17
Shanghai, China
www.fpdchina.org

SEMICON Russia 2016
June 8–9
Moscow, Russia
www.semiconrussia.org

PV Taiwan 2016
October 12–14
Taipei, Taiwan
www.pvtaiwan.com

LED Korea 2016
January 27–29
Seoul, Korea
www.led-korea.org

LED Taiwan 2016
April 13–16
Taipei, Taiwan
www.ledtaiwan.org

SEMICON West 2016
July 12–14
San Francisco, USA
www.semiconwest.org

SEMICON Europa 2016
October 25–27
Grenoble, France
www.semiconeuropa.org

AMERICAS • CHINA • EUROPE • JAPAN • KOREA • RUSSIA • SINGAPORE • TAIWAN

Right: Industrial-grade MOCVD reactor from AIXTRON, used to grow the III-V layers on silicon substrates. In-situ characterization includes full-wafer temperature measurement and curvature measurement.

Building the ICs of the future

The key to producing novel ICs with high efficiency and great functionality is to employ CMOS foundry process flows for the monolithic integration of silicon and III-V devices

BY DAVID KOHEN, ABDUL KADIR, KENNETH LEE, FAYYAZ SINGAPOREWALA AND EUGENE FITZGERALD FROM SINGAPORE-MIT ALLIANCE FOR RESEARCH AND TECHNOLOGY

PREDICTING THE FUTURE is never easy. But it is a good bet that it will involve smart cities, smart homes and the Internet of Things – and underpinning all of this will be an increasing number of interconnected electronic devices.

To make this happen, the electronic devices will have to contain sensors that transmit data wirelessly to a control centre. This means they will have to combine RF capabilities with a small form factor and low operating power. A neat, promising approach to fulfilling all of these objectives is to make a single chip that unites the capabilities of silicon CMOS with those of III-V devices.

Despite its attractiveness, today the monolithic integration of silicon and III-V devices is not that common. Most commercial products are made by taking silicon CMOS chips, plus those based on III-Vs, and bringing them together in a single package. With this system-in-a-package approach, III-V and silicon CMOS devices are fabricated on separate wafers, before being bonded and connected by various methods, including through-silicon vias and bump bonding.

There are several drawbacks with this system-in-a-package approach, including a large form factor and a lower efficiency that stems from high interconnect losses. But these weaknesses could be addressed by turning to monolithic integration: a high performance and a small form-factor are possible when interconnects between III-V and silicon devices are shortened, so that they are comparable with those in conventional CMOS processes. For mature process nodes, CMOS interconnect distances are typically shorter than 5 μm – orders of magnitude lower than those associated with a system-in-a-package. Realising this level of integration slashes interconnect losses and reduces latency between different circuit modules. Self-sensing and self-tuning circuits can follow, enabling the serving of a range of new applications.

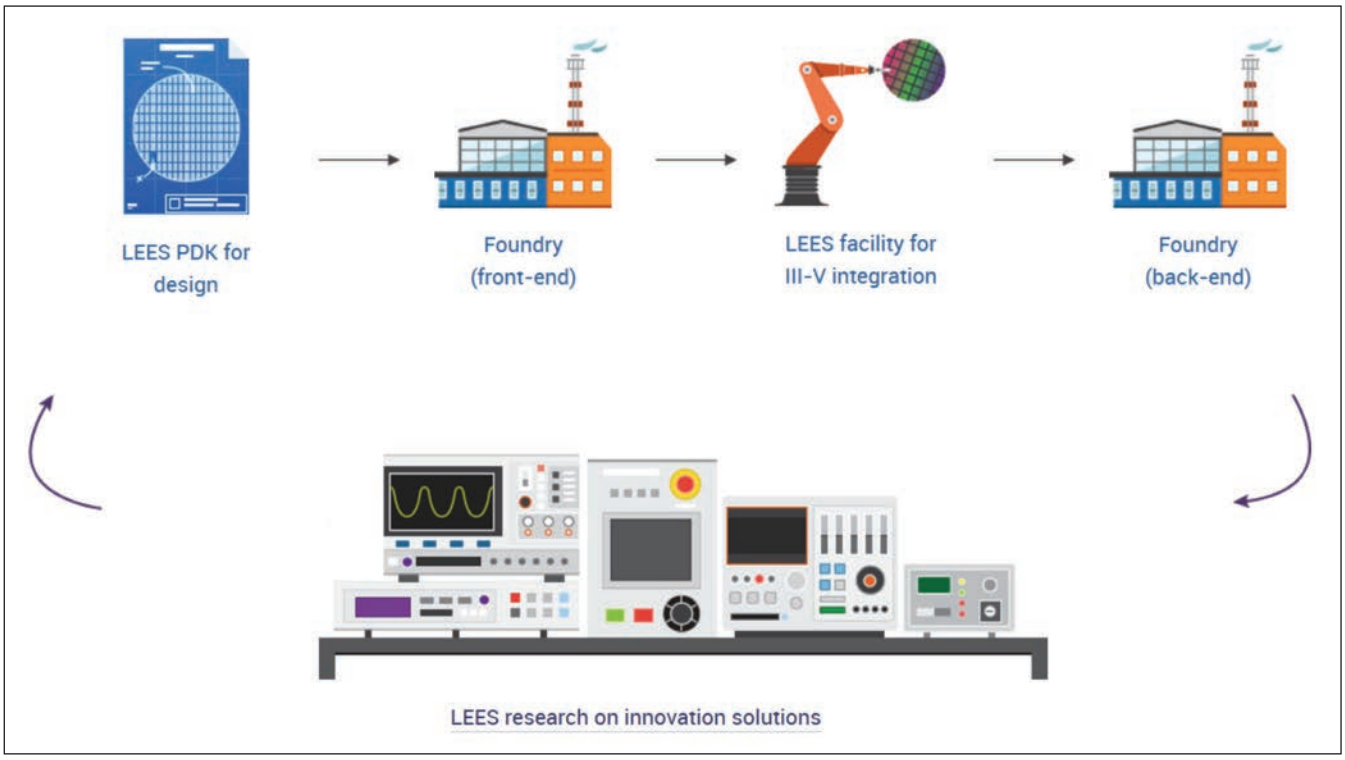
Just one of many examples of a technology that could benefit from the monolithic integration of different materials is the digital CMOS circuit. Access to ultra-efficient devices in a

small form-factor could enable real-time adjustments at far higher rates – and this could address small and transient mismatches or non-linearities in analogue/RF or optical circuits constructed with III-V devices. Hybrid circuits would also be able to operate with greater stability and less noise. A significant increase in circuit functionality, complexity and performance could follow, realised without having to resort to a shrinking of device dimensions and a hike in transistor count.

Success with the monolithic integration of InP HBT and silicon CMOS technologies has been accomplished through the DARPA-funded COSMOS programme (and the subsequent DAHI programme). However, although the approach developed by this effort is technically feasible, integration took place in a research environment. Consequently, the advances that were made failed to offer a clear and ready pathway to scaling up production to high-volume markets.

To drive the industry adoption of a novel IC platform incorporating new materials, there has to be minimal disruption to existing CMOS foundry and processing infrastructure. These are the objectives that our team from Singapore-MIT Alliance for Research and Technology (SMART) set itself, and this has led to the development of a SMART Low Energy Electronic Systems (LEES) integration scheme. At its heart is a production process that begins and ends with standard processing at a silicon foundry, and also involves a series of growth steps associated with the growth of III-Vs on silicon.

Later on in this piece, we will describe our process in greater detail. But before we do this, let us first make the point that the advantages of our technique are not limited to smaller interconnects. Benefits also include the seamless integration of digital logic with III-V devices, which are best suited for photonic, opto-electronic and wireless electronic functions. Products that could result from this complementary marriage of materials include: intelligent LED lighting systems, which could feature integrating adaptive controls; high-speed wireless optical systems (Li-Fi); networks of self-powered drones for logistics and



The approach developed at SMART for monolithic integration begins with a designer using the LEES heterogeneous design kit to create novel circuits with interconnected III-V and silicon CMOS devices. Silicon CMOS devices are then fabricated using standard front-end-of-line processes at a foundry partner (up to the first dielectric layer deposition step). The addition of III-V layers and devices follows at the LEES facility, before wafers are reconstituted, so that they are indistinguishable from regular CMOS wafers. Finally, the foundry partner performs standard back-end-of-line processes on these wafers, such as metallisation, to connect the III-V and the silicon CMOS devices within the die.

monitoring; and self-powered wearable electronics. There is also the possibility of using our hybrid technology in the mobile communications sector, to create an intelligent traffic system. This might help to overcome blind spots and avoid accidents; and it could include other applications, ranging from safety to navigation and law enforcement.

Looking further ahead, our heterogeneous technology could help to make the world a greener place. For example, it could improve the performance of electric vehicles, by providing efficient sensors, and delivering persistent monitoring in harsh environments, to refine combustion processes.

The perfect size

Our LEES facility has been built for 200 mm wafer processing. With this wafer size, CMOS technology nodes are compatible with analogue mixed-signal applications. The 0.18 μm node continues to be heavily used in these markets, and the combination of CMOS and III-V devices allows the design of novel structures using inexpensive trailing-edge silicon manufacturing infrastructure. On top of this advantage, research and development costs are lower with 200 mm wafers than those of a larger size.

Circuit designers that use our facility work with a foundry design kit that has been augmented by LEES. This kit, which includes III-V circuit elements that we are developing, allows engineers to create ICs in design environments that are familiar to them.

Following the design of the IC, silicon CMOS devices are fabricated using standard front-end-of-line processes. CMOS processing is then interrupted, with wafers taken out of the line at the silicon foundry, and sent to our LEES facility, where our team of engineers carry out wafer-bonding and III-V processing steps that are necessary for integration. The hybrid wafers that result, which feature a CMOS device layer and a III-V device layer separated by just one micron or so, are then returned to the foundry. Back there, conventional CMOS back-end-of-line processing realises interconnections between CMOS and III-V devices and also amongst CMOS devices.

One of the great strengths of this approach is that it makes best use of the prior investment into CMOS processing infrastructure. Thanks to this, additional investment is directed at the development of the essential innovative steps that provide seamless integration of new materials into the traditional CMOS process flow.

Growth on silicon

Currently, our research focuses on two families of III-V materials: the nitride family, which is targeting high-power applications and blue and green LEDs; and the arsenide-phosphide family, targeting applications such as ultra-high-frequency power amplifiers, low-noise amplifiers, and yellow and red LEDs.

Epitaxy of the former family, the nitrides, is performed on silicon (111) substrates. AlN is deposited at the beginning of the buffer layer to prevent melt-back etching, which occurs when gallium and silicon atoms interact at high temperatures. A combination of AlN and AlGaN step-graded buffer layers is then used to provide a bridge between the silicon and the GaN lattice constant. Careful selection of the step-graded AlGaN layers results in a compressive stress, which compensates for the tensile stress that originates from the thermal mismatch, and can be an issue during the post-growth cooling.

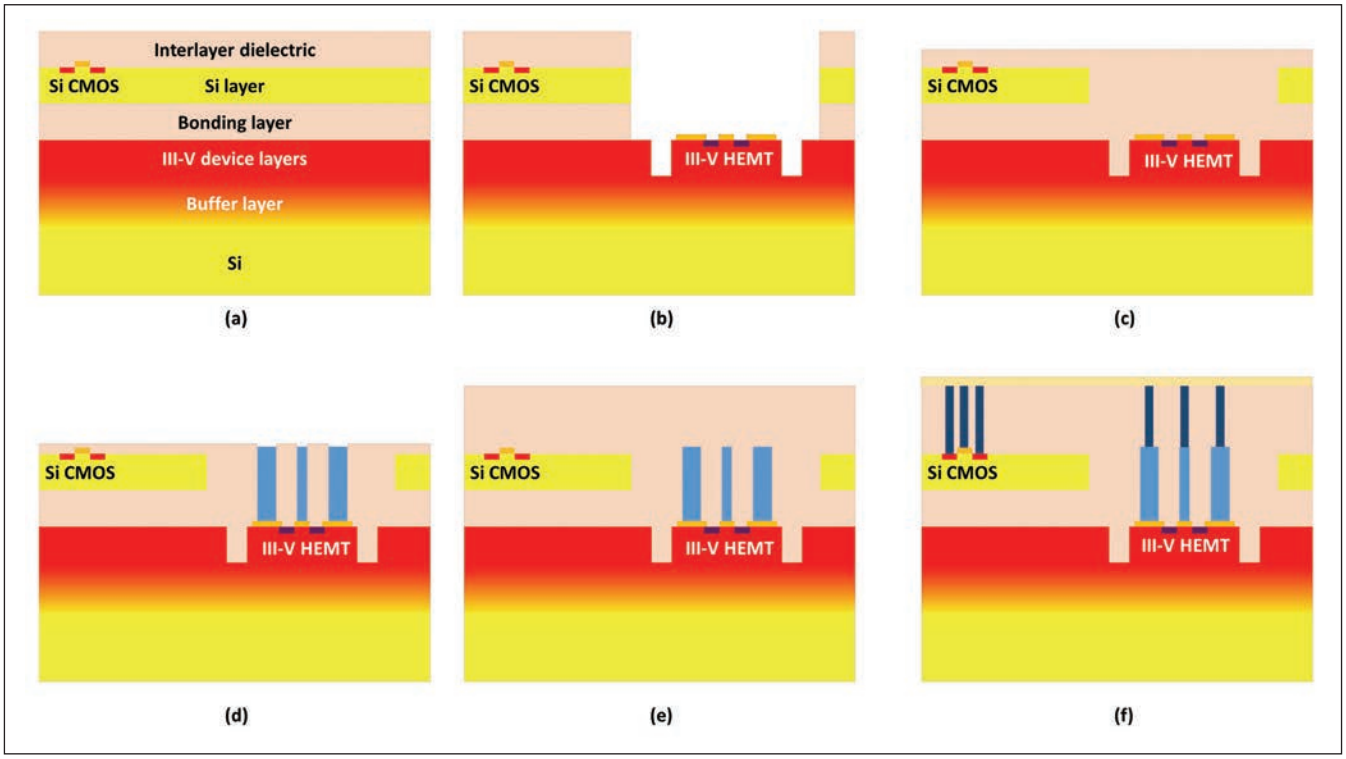
Our development of a GaN-on-silicon growth process draws on research in this area that goes back three decades. Progress has led to processes that have reached industrial acceptance, but success tends to rely on the use of relatively thick silicon (111) substrates. They are typically 1 mm or more, making them incompatible with standard CMOS foundry equipment. For compatibility with silicon foundries, it is necessary to use 725 μm-thick substrates – but they introduce a larger wafer bow, and are more fragile than their thicker cousins.

We have tackled this issue head-on. By developing a detailed understanding of the strain mechanism and by learning how to carefully control the growth process, we are able to grow high-quality GaN HEMTs on 200 mm silicon substrates with a thickness of 725 μm. These epiwafers exhibit excellent crystal quality, and their bow is typically less than 20 μm, well below the value required for processing in silicon lines.

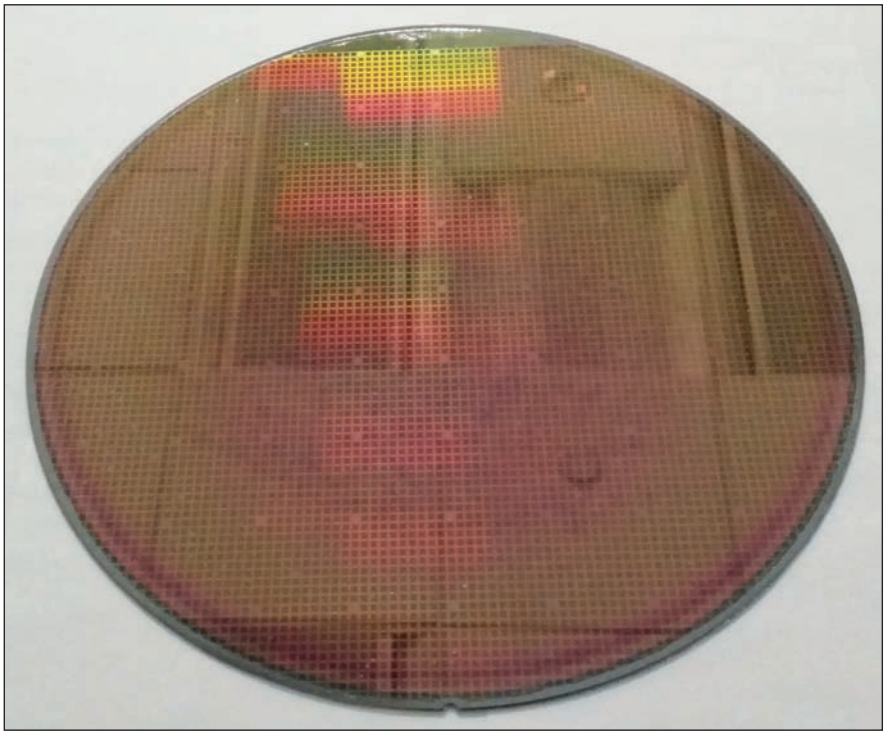
According to high-resolution X-ray diffraction, the full-width-at-half maximum of the diffraction peak for the (002) reflection is just 430 arcsec, and it is only 520 arcsec for the (102) reflection. The electrical properties of our epiwafers are very promising, with a Hall mobility of 1200 $cm^2 V^{-1} s^{-1}$ and a sheet density of $2 \times 10^{13} cm^{-2}$.

For the growth of arsenides on silicon, we start with 725 μm-thick silicon (100) wafers with a 6° offcut. On these substrates, which have an orientation that prevents the formation of anti-phase boundaries, we form InGaAs HEMTs by first depositing a metamorphic buffer comprising a pure germanium layer, a GaAs layer and a compositionally graded InAlAs buffer, all grown *in situ*. To realise this with our MOCVD system, we installed a GeH_4 gas line. This is not common in conventional MOCVD systems.

Using this tool we first deposit a composite buffer, which has an interface



An overview of the LEES processing scheme. (a) A 1 μm-thick silicon CMOS layer is bonded to a III-V-on-silicon wafer, fabricated using epitaxy. (b) Windows are opened in the CMOS-free areas to expose the underlying III-V layers, and III-V devices are then fabricated. (c) The dielectric layer is deposited, before chemical-mechanical polishing yields a flat surface. (d) W-plugs are created to contact III-V devices. (e) The dielectric is deposited and flattened using chemical-mechanical polishing. The wafer is thoroughly cleaned, so that it can re-enter the silicon foundry. (f) The silicon foundry connects the silicon CMOS and III-V devices together, using their typical interconnection scheme, to complete the integration process.



A 200 mm wafer with a silicon dummy CMOS layer integrated with III-V device layers.

between GaAs and germanium that is critical for obtaining high-quality III-V layers. Recently, we have shown that a high arsine partial pressure – in our reactor, it must be between 5 mbar and 10 mbar – must be applied during GaAs growth to prevent anti-phase boundaries from forming. With this approach, our interface between GaAs and germanium is free from anti-phase boundaries, and misfit dislocations are confined at the silicon-germanium interface, according to transmission electron microscopy.

Before transistors are formed on this GaAs layer, we add a 1.5 μm-thick InAlAs buffer. This is formed by linearly grading the indium content up to a composition of $In_{0.30}Al_{0.70}As$ – higher values are not used, because this would lead to phase separation under typical growth conditions. Once we have added this buffer, we deposit our InGaAs HEMTs.

Scrutinising these transistors suggests that they have very promising characteristics. There is strain relaxation in the graded buffer, according to X-ray diffraction measurements and the presence of a regular crosshatched surface; and plan-view transmission electron microscopy reveals a dislocation density in the low 10^7 cm^{-2} range. Electrical characterisation of a typical HEMT with a 10 nm thick $In_{0.30}Ga_{0.70}As$ channel suggests a room-temperature Hall mobility reaching 6000 cm^2 V^{-1} s^{-1} for a carrier density of 3 x 10^{12} cm^{-2}.

Creating a hybrid platform

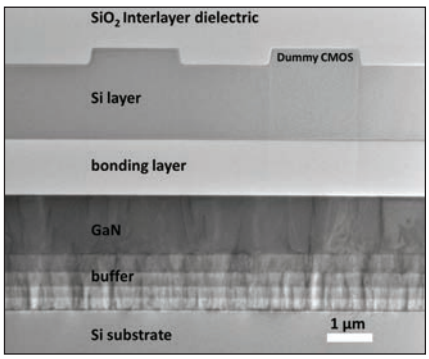
Another challenge we have overcome is how to bring the silicon CMOS and III-V device layers close together. Our success results from fabricating silicon CMOS devices first, up to the point just before the backend interconnection, so that silicon CMOS transistors are covered by an interlayer dielectric. Note that these wafers have CMOS-free areas, which designers have reserved for III-V devices.

At this point, wafers are transferred to our LEES facility for III-V integration and processing. Transfer of the silicon CMOS layers on each wafer to our III-V wafers involves a series of wafer bonding, oxide deposition and chemical-mechanical polishing steps. Bonding is accomplished with a direct fusion bonding process, and its strength is enhanced via a subsequent anneal. Windows opened in the CMOS-free areas expose the underlying III-V layers.

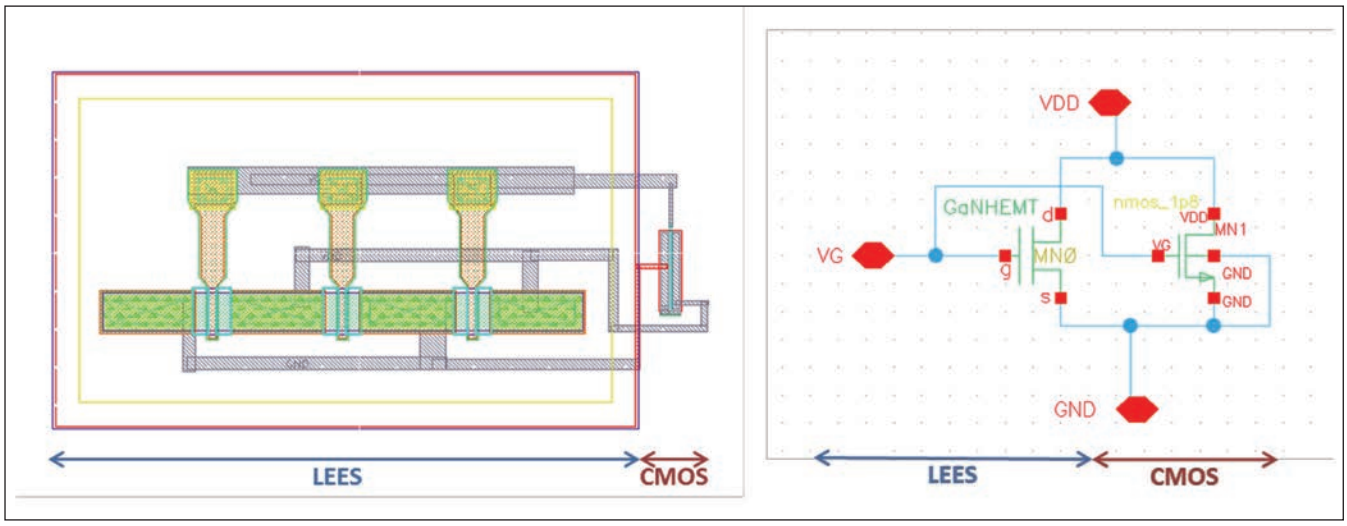
We are constrained with our device fabrication processes, because the integrated wafer must remain CMOS compatible, and we must avoid any modification to the already-fabricated silicon CMOS devices. Working within these restrictions, we have developed and optimised several novel processes. They include the development of: low-temperature ohmic contacts using CMOS compatible metals; etching steps that can replace lift-off steps; and a reduction in thermal budget, so that it is low enough that it avoids impacting the performance of the silicon devices. After carrying out all these processes, we thoroughly clean the wafers before they are returned to the silicon foundry. Careful cleaning ensures that the wafers are free from non-CMOS compatible materials, which may be present on the exposed surfaces.

Once these wafers are back in the silicon line, back-end-of-line processes complete IC fabrication. With this approach, there are no significant changes to the foundry's conventional silicon CMOS flow.

If our approach is to be widely used,



A cross-sectional transmission electron microscopy image of a GaN-on-silicon (111) wafer bonded to a silicon (100) layer containing a dummy CMOS area.



LEES augments silicon CMOS design kits with additional components to allow inclusion and integration of III-V devices into hybrid III-V and CMOS circuits. The heterogeneous LEES and silicon CMOS design kits offer circuit designers a familiar design environment to work within.

designers must have access to a suitable design kit. We have addressed this need, and this has lead to the seamless integration of III-V design components into the existing CMOS design kit. Thanks to this approach, designers have an environment that is familiar, and they can make use of the CMOS digital and analogue IP libraries that are currently available.

To ensure that circuit designers make the best decisions, we have designed physics-based compact models with Verilog-A cores for a range of III-V devices, including those based on GaN and on InGaAs. These models have been qualified and validated with DC and RF data, and implemented in Cadence Spectre for seamless integration with our design kit. This approach also allows our circuit designers to give feedback to device and material researchers as they develop the novel platforms.

When circuits are complex, automated rule-checking is critical, because it can uncover layout and interconnect violations. We have developed a set of design rules for our own processes, and we package them with the standard rules from a given CMOS process. This allows designers to use commercial CAD tools to perform rule-checks on hybrid III-V and CMOS designs, and detect interconnect errors between these two classes of device.

The challenges ahead

We have developed an innovative method to seamlessly integrate III-V devices with silicon CMOS, and thus create novel circuits with new functionalities. However, before applying this technology to mass production, we must overcome several challenges.

One of the most significant of these stems from the designers of silicon CMOS operating in a very different world from those that design III-Vs. That is not surprising: silicon CMOS design involves the integration of millions, if not billions, of devices with mature EDA tools; in contrast, III-V designers are the architects of circuits with a handful of devices, designed using customised models and processes. It is tough to bring the technology of these two very different worlds together, and it will require us to strengthen our design kit, so that it generates a greater level of acceptance by industry players. We can achieve this through greater collaboration with silicon CMOS designers, EDA tool companies and III-V circuit designers.

Another goal of ours is to improve our process so that it is compatible with high-volume manufacturing. Advances must be made in the areas of process robustness, reliability, and device performance homogeneity. Further gains could result from reducing the process complexity through a trimming of the number of steps needed to integrate III-Vs with silicon CMOS.

One additional avenue that we will explore is the integration of silicon CMOS with other types of materials. We are already investigating materials for memory and energy storage, because this promises the creation of circuits with even greater functionality. Armed with more technologies, what can be achieved in future is set to overshadow the accomplishments to date.

Further reading

[1] smart.mit.edu/research/lees/lees.html
[2] www.circuit-innovation.org
[3] K.H. Lee *et. al.* Jap. J. of Appl. Phys. **54** 030209 (2015)
[4] E.A. Fitzgerald *et al. Monolithic 3D integration in a CMOS process flow* 2014 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Milbrae, CA, Oct 2014

Right: Industrial-grade MOCVD reactor from AIXTRON, used to grow the III-V layers on silicon substrates. In-situ characterization includes full-wafer temperature measurement and curvature measurement.

Building the ICs of the future

The key to producing of novel ICs with high efficiency and great functionality is to employ CMOS foundry process flows for the monolithic integration of silicon and III-V devices

BY DAVID KOHEN, ABDUL KADIR, KENNETH LEE, FAYYAZ SINGAPOREWALA AND EUGENE FITZGERALD FROM SINGAPORE-MIT ALLIANCE FOR RESEARCH AND TECHNOLOGY

PREDICTING THE FUTURE is never easy. But it is a good bet that it will involve smart cities, smart homes and the Internet of Things – and underpinning all of this will be an increasing number of interconnected electronic devices.

To make this happen, the electronic devices will have to contain sensors that transmit data wirelessly to a control centre. This means they will have to combine RF capabilities with a small form factor and low operating power. A neat, promising approach to fulfilling all of these objectives is to make a single chip that unites the capabilities of silicon CMOS with those of III-V devices.

Despite its attractiveness, today the monolithic integration of silicon and III-V devices is not that common. Most commercial products are made by taking silicon CMOS chips, plus those based on III-Vs, and bringing them together in a single package. With this system-in-a-package approach, III-V and silicon CMOS devices are fabricated on separate wafers, before being bonded and connected by various methods, including through-silicon vias and bump bonding.

There are several drawbacks with this system-in-a-package approach, including a large form factor and a lower efficiency that stems from high interconnect losses. But these weaknesses could be addressed by turning to monolithic integration: a high performance and a small form-factor are possible when interconnects between III-V and silicon devices are shortened, so that they are comparable with those in conventional CMOS processes. For mature process nodes, CMOS interconnect distances are typically shorter than 5 μm – orders of magnitude lower than those associated with a system-in-a-package. Realising this level of integration slashes interconnect losses and reduces latency between different circuit modules. Self-sensing and self-tuning circuits can follow, enabling the serving of a range of new applications.

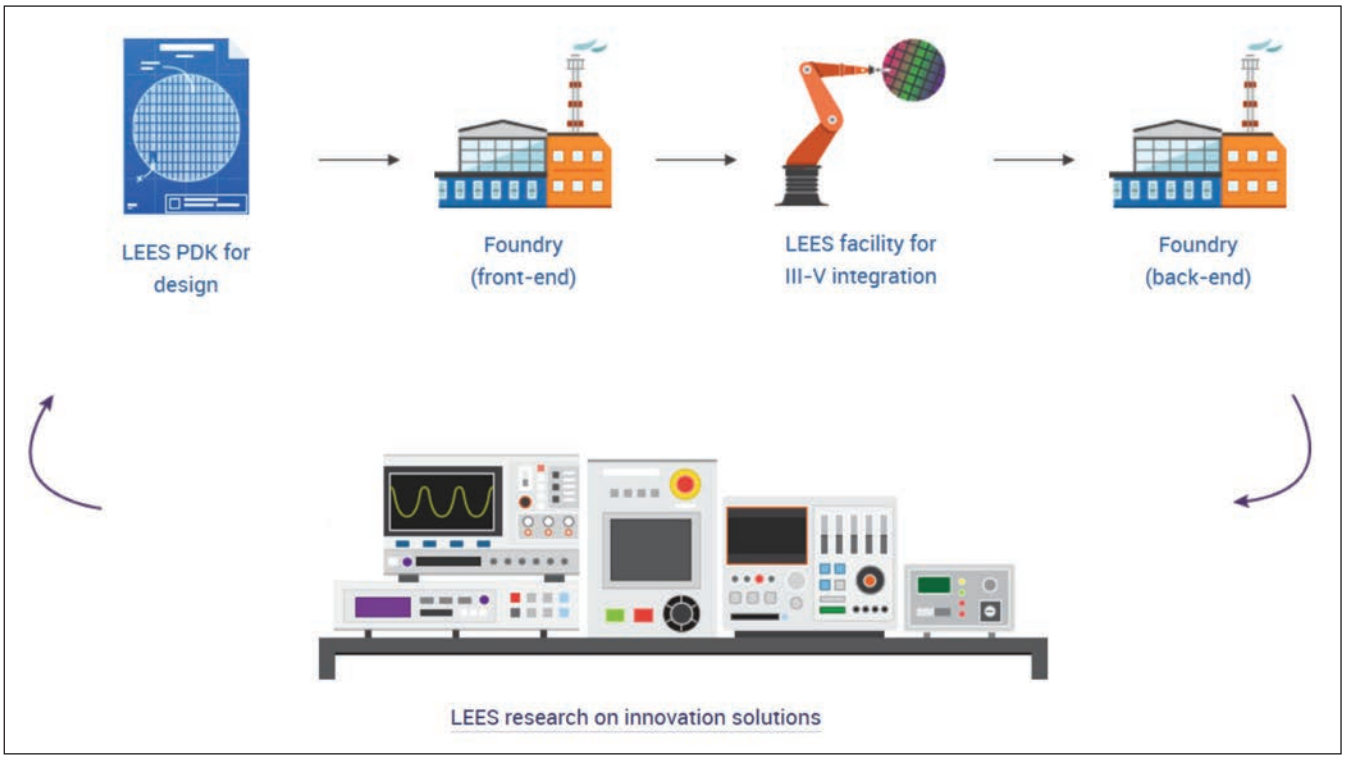
Just one of many examples of a technology that could benefit from the monolithic integration of different materials is the digital CMOS circuit. Access to ultra-efficient devices in a

small form-factor could enable real-time adjustments at far higher rates – and this could address small and transient mismatches or non-linearities in analogue/RF or optical circuits constructed with III-V devices. Hybrid circuits would also be able to operate with greater stability and less noise. A significant increase in circuit functionality, complexity and performance could follow, realised without having to resort to a shrinking of device dimensions and a hike in transistor count.

Success with the monolithic integration of InP HBT and silicon CMOS technologies has been accomplished through the DARPA-funded COSMOS programme (and the subsequent DAHI programme). However, although the approach developed by this effort is technically feasible, integration took place in a research environment. Consequently, the advances that were made failed to offer a clear and ready pathway to scaling up production to high-volume markets.

To drive the industry adoption of a novel IC platform incorporating new materials, there has to be minimal disruption to existing CMOS foundry and processing infrastructure. These are the objectives that our team from Singapore-MIT Alliance for Research and Technology (SMART) set itself, and this has led to the development of a SMART Low Energy Electronic Systems (LEES) integration scheme. At its heart is a production process that begins and ends with standard processing at a silicon foundry, and also involves a series of growth steps associated with the growth of III-Vs on silicon.

Later on in this piece, we will describe our process in greater detail. But before we do this, let us first make the point that the advantages of our technique are not limited to smaller interconnects. Benefits also include the seamless integration of digital logic with III-V devices, which are best suited for photonic, opto-electronic and wireless electronic functions. Products that could result from this complementary marriage of materials include: intelligent LED lighting systems, which could feature integrating adaptive controls; high-speed wireless optical systems (Li-Fi); networks of self-powered drones for logistics and



The approach developed at SMART for monolithic integration begins with a designer using the LEES heterogeneous design kit to create novel circuits with interconnected III-V and silicon CMOS devices. Silicon CMOS devices are then fabricated using standard front-end-of-line processes at a foundry partner (up to the first dielectric layer deposition step). The addition of III-V layers and devices follows at the LEES facility, before wafers are reconstituted, so that they are indistinguishable from regular CMOS wafers. Finally, the foundry partner performs standard back-end-of-line processes on these wafers, such as metallisation, to connect the III-V and the silicon CMOS devices within the die.

monitoring; and self-powered wearable electronics. There is also the possibility of using our hybrid technology in the mobile communications sector, to create an intelligent traffic system. This might help to overcome blind spots and avoid accidents; and it could include other applications, ranging from safety to navigation and law enforcement.

Looking further ahead, our heterogeneous technology could help to make the world a greener place. For example, it could improve the performance of electric vehicles, by providing efficient sensors, and delivering persistent monitoring in harsh environments, to refine combustion processes.

The perfect size

Our LEES facility has been built for 200 mm wafer processing. With this wafer size, CMOS technology nodes are compatible with analogue mixed-signal applications. The 0.18 μm node continues to be heavily used in these markets, and the combination of CMOS and III-V devices allows the design of novel structures using inexpensive trailing-edge silicon manufacturing infrastructure. On top of this advantage, research and development costs are lower with 200 mm wafers than those of a larger size.

Circuit designers that use our facility work with a foundry design kit that has been augmented by LEES. This kit, which includes III-V circuit elements that we are developing, allows engineers to create ICs in design environments that are familiar to them.

Following the design of the IC, silicon CMOS devices are fabricated using standard front-end-of-line processes. CMOS processing is then interrupted, with wafers taken out of the line at the silicon foundry, and sent to our LEES facility, where our team of engineers carry out wafer-bonding and III-V processing steps that are necessary for integration. The hybrid wafers that result, which feature a CMOS device layer and a III-V device layer separated by just one micron or so, are then returned to the foundry. Back there, conventional CMOS back-end-of-line processing realises interconnections between CMOS and III-V devices and also amongst CMOS devices.

One of the great strengths of this approach is that it makes best use of the prior investment into CMOS processing infrastructure. Thanks to this, additional investment is directed at the development of the essential innovative steps that provide seamless integration of new materials into the traditional CMOS process flow.

Growth on silicon

Currently, our research focuses on two families of III-V materials: the nitride family, which is targeting high-power applications and blue and green LEDs; and the arsenide-phosphide family, targeting applications such as ultra-high-frequency power amplifiers, low-noise amplifiers, and yellow and red LEDs.

Epitaxy of the former family, the nitrides, is performed on silicon (111) substrates. AlN is deposited at the beginning of the buffer layer to prevent melt-back etching, which occurs when gallium and silicon atoms interact at high temperatures. A combination of AlN and AlGaN step-graded buffer layers is then used to provide a bridge between the silicon and the GaN lattice constant. Careful selection of the step-graded AlGaN layers results in a compressive stress, which compensates for the tensile stress that originates from the thermal mismatch, and can be an issue during the post-growth cooling.

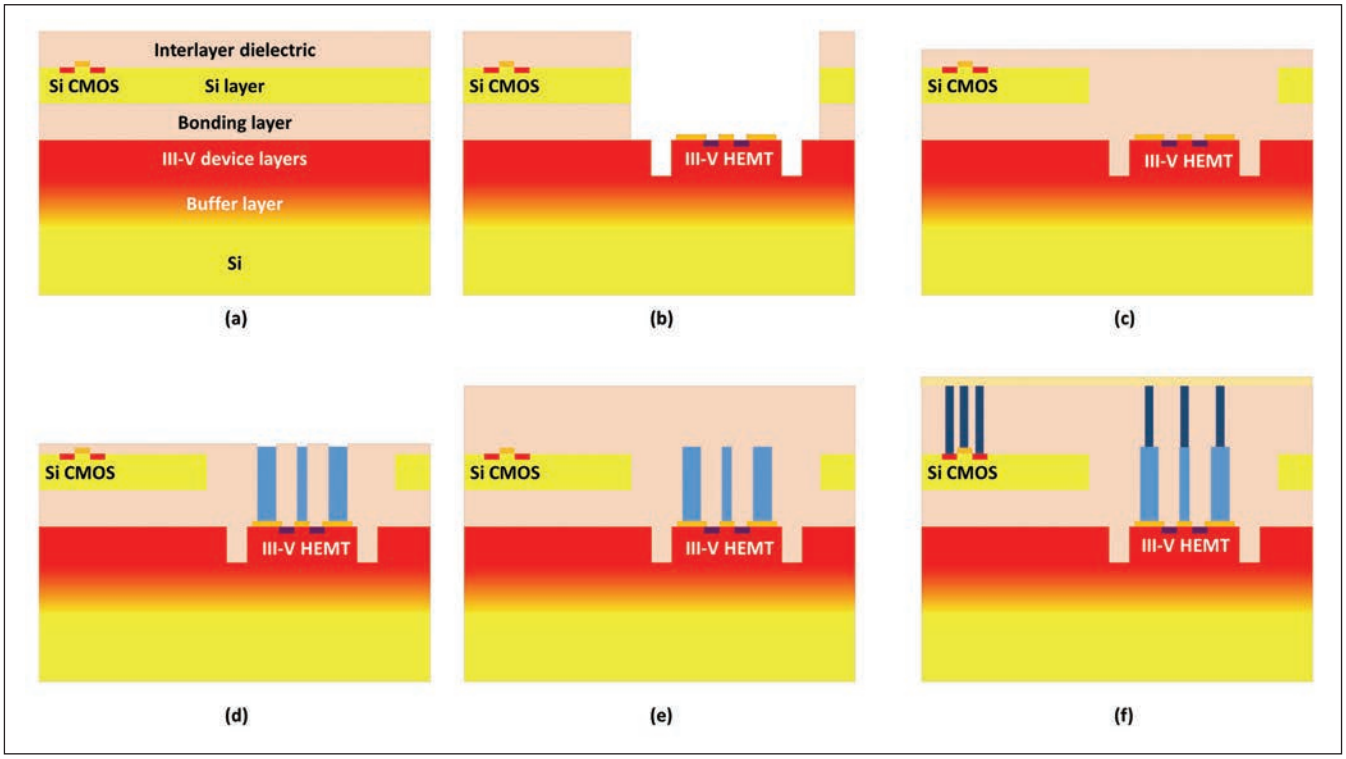
Our development of a GaN-on-silicon growth process draws on research in this area that goes back three decades. Progress has led to processes that have reached industrial acceptance, but success tends to rely on the use of relatively thick silicon (111) substrates. They are typically 1 mm or more, making them incompatible with standard CMOS foundry equipment. For compatibility with silicon foundries, it is necessary to use 725 μm-thick substrates – but they introduce a larger wafer bow, and are more fragile than their thicker cousins.

We have tackled this issue head-on. By developing a detailed understanding of the strain mechanism and by learning how to carefully control the growth process, we are able to grow high-quality GaN HEMTs on 200 mm silicon substrates with a thickness of 725 μm. These epiwafers exhibit excellent crystal quality, and their bow is typically less than 20 μm, well below the value required for processing in silicon lines.

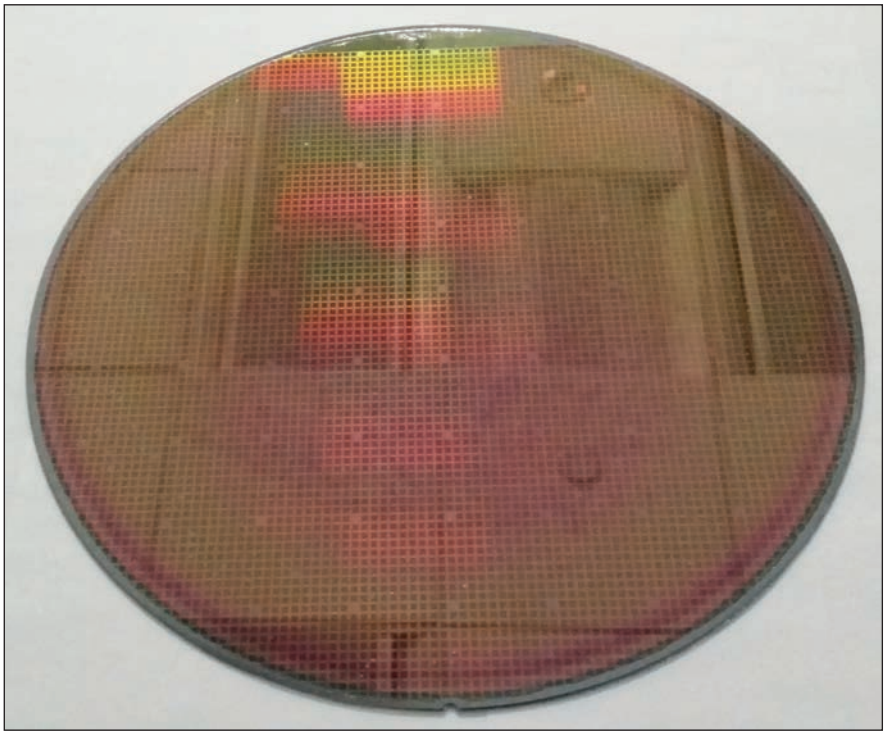
According to high-resolution X-ray diffraction, the full-width-at-half maximum of the diffraction peak for the (002) reflection is just 430 arcsec, and it is only 520 arcsec for the (102) reflection. The electrical properties of our epiwafers are very promising, with a Hall mobility of 1200 $cm^2 V^{-1} s^{-1}$ and a sheet density of $2 \times 10^{13} cm^{-2}$.

For the growth of arsenides on silicon, we start with 725 μm-thick silicon (100) wafers with a 6° offcut. On these substrates, which have an orientation that prevents the formation of anti-phase boundaries, we form InGaAs HEMTs by first depositing a metamorphic buffer comprising a pure germanium layer, a GaAs layer and a compositionally graded InAlAs buffer, all grown *in situ*. To realise this with our MOCVD system, we installed a GeH_4 gas line. This is not common in conventional MOCVD systems.

Using this tool we first deposit a composite buffer, which has an interface



An overview of the LEES processing scheme. (a) A 1 μm-thick silicon CMOS layer is bonded to a III-V-on-silicon wafer, fabricated using epitaxy. (b) Windows are opened in the CMOS-free areas to expose the underlying III-V layers, and III-V devices are then fabricated. (c) The dielectric layer is deposited, before chemical-mechanical polishing yields a flat surface. (d) W-plugs are created to contact III-V devices. (e) The dielectric is deposited and flattened using chemical-mechanical polishing. The wafer is thoroughly cleaned, so that it can re-enter the silicon foundry. (f) The silicon foundry connects the silicon CMOS and III-V devices together, using their typical interconnection scheme, to complete the integration process.



A 200 mm wafer with a silicon dummy CMOS layer integrated with III-V device layers.

between GaAs and germanium that is critical for obtaining high-quality III-V layers. Recently, we have shown that a high arsine partial pressure – in our reactor, it must be between 5 mbar and 10 mbar – must be applied during GaAs growth to prevent anti-phase boundaries from forming. With this approach, our interface between GaAs and germanium is free from anti-phase boundaries, and misfit dislocations are confined at the silicon-germanium interface, according to transmission electron microscopy.

Before transistors are formed on this GaAs layer, we add a 1.5 μm-thick InAlAs buffer. This is formed by linearly grading the indium content up to a composition of $In_{0.30}Al_{0.70}As$ – higher values are not used, because this would lead to phase separation under typical growth conditions. Once we have added this buffer, we deposit our InGaAs HEMTs.

Scrutinising these transistors suggests that they have very promising characteristics. There is strain relaxation in the graded buffer, according to X-ray diffraction measurements and the presence of a regular crosshatched surface; and plan-view transmission electron microscopy reveals a dislocation density in the low 10^7 cm^{-2} range. Electrical characterisation of a typical HEMT with a 10 nm thick $In_{0.30}Ga_{0.70}As$ channel suggests a room-temperature Hall mobility reaching 6000 cm^2 V^{-1} s^{-1} for a carrier density of 3 x 10^{12} cm^{-2}.

Creating a hybrid platform

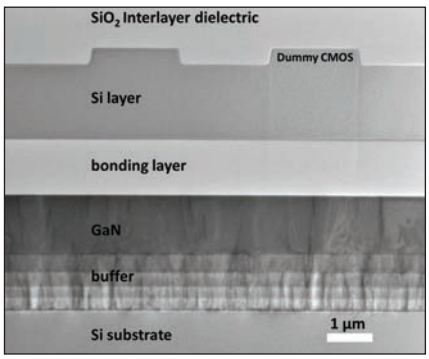
Another challenge we have overcome is how to bring the silicon CMOS and III-V device layers close together. Our success results from fabricating silicon CMOS devices first, up to the point just before the backend interconnection, so that silicon CMOS transistors are covered by an interlayer dielectric. Note that these wafers have CMOS-free areas, which designers have reserved for III-V devices.

At this point, wafers are transferred to our LEES facility for III-V integration and processing. Transfer of the silicon CMOS layers on each wafer to our III-V wafers involves a series of wafer bonding, oxide deposition and chemical-mechanical polishing steps. Bonding is accomplished with a direct fusion bonding process, and its strength is enhanced via a subsequent anneal. Windows opened in the CMOS-free areas expose the underlying III-V layers.

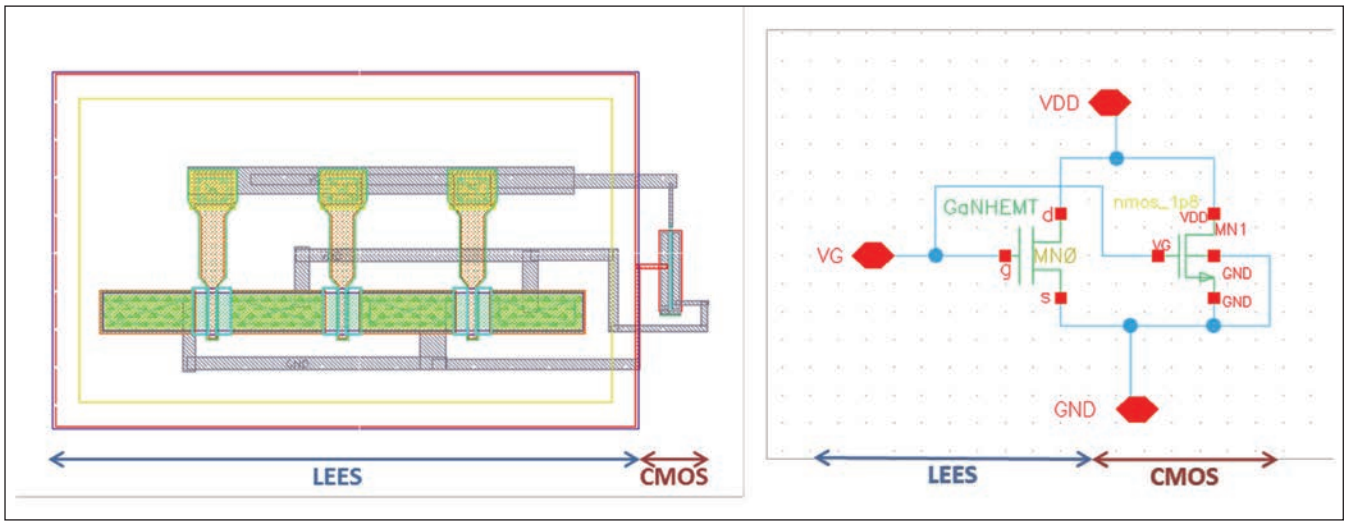
We are constrained with our device fabrication processes, because the integrated wafer must remain CMOS compatible, and we must avoid any modification to the already-fabricated silicon CMOS devices. Working within these restrictions, we have developed and optimised several novel processes. They include the development of: low-temperature ohmic contacts using CMOS compatible metals; etching steps that can replace lift-off steps; and a reduction in thermal budget, so that it is low enough that it avoids impacting the performance of the silicon devices. After carrying out all these processes, we thoroughly clean the wafers before they are returned to the silicon foundry. Careful cleaning ensures that the wafers are free from non-CMOS compatible materials, which may be present on the exposed surfaces.

Once these wafers are back in the silicon line, back-end-of-line processes complete IC fabrication. With this approach, there are no significant changes to the foundry's conventional silicon CMOS flow.

If our approach is to be widely used,



A cross-sectional transmission electron microscopy image of a GaN-on-silicon (111) wafer bonded to a silicon (100) layer containing a dummy CMOS area.



LEES augments silicon CMOS design kits with additional components to allow inclusion and integration of III-V devices into hybrid III-V and CMOS circuits. The heterogeneous LEES and silicon CMOS design kits offer circuit designers a familiar design environment to work within.

designers must have access to a suitable design kit. We have addressed this need, and this has lead to the seamless integration of III-V design components into the existing CMOS design kit. Thanks to this approach, designers have an environment that is familiar, and they can make use of the CMOS digital and analogue IP libraries that are currently available.

To ensure that circuit designers make the best decisions, we have designed physics-based compact models with Verilog-A cores for a range of III-V devices, including those based on GaN and on InGaAs. These models have been qualified and validated with DC and RF data, and implemented in Cadence Spectre for seamless integration with our design kit. This approach also allows our circuit designers to give feedback to device and material researchers as they develop the novel platforms.

When circuits are complex, automated rule-checking is critical, because it can uncover layout and interconnect violations. We have developed a set of design rules for our own processes, and we package them with the standard rules from a given CMOS process. This allows designers to use commercial CAD tools to perform rule-checks on hybrid III-V and CMOS designs, and detect interconnect errors between these two classes of device.

The challenges ahead

We have developed an innovative method to seamlessly integrate III-V devices with silicon CMOS, and thus create novel circuits with new functionalities. However, before applying this technology to mass production, we must overcome several challenges.

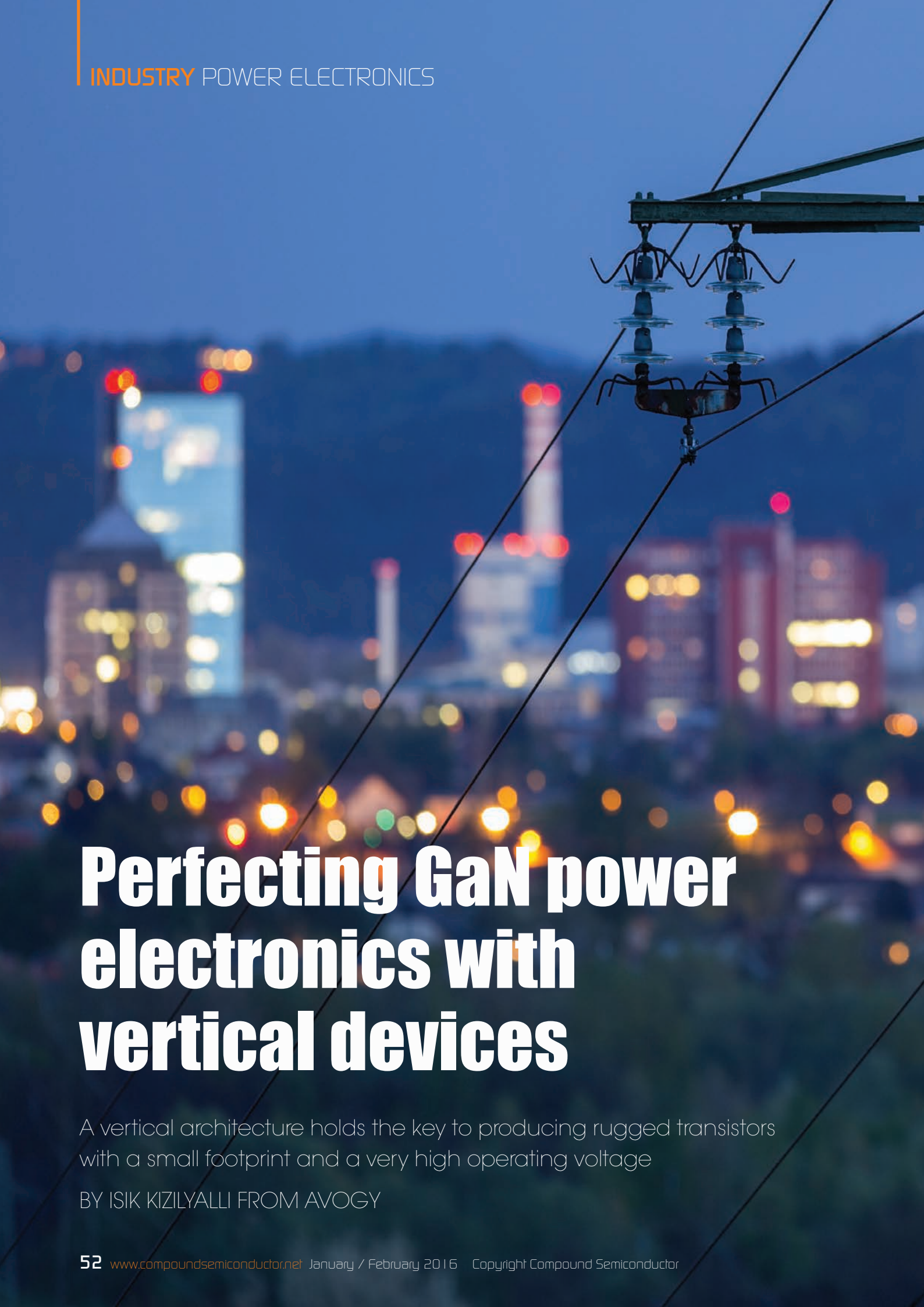
One of the most significant of these stems from the designers of silicon CMOS operating in a very different world from those that design III-Vs. That is not surprising: silicon CMOS design involves the integration of millions, if not billions, of devices with mature EDA tools; in contrast, III-V designers are the architects of circuits with a handful of devices, designed using customised models and processes. It is tough to bring the technology of these two very different worlds together, and it will require us to strengthen our design kit, so that it generates a greater level of acceptance by industry players. We can achieve this through greater collaboration with silicon CMOS designers, EDA tool companies and III-V circuit designers.

Another goal of ours is to improve our process so that it is compatible with high-volume manufacturing. Advances must be made in the areas of process robustness, reliability, and device performance homogeneity. Further gains could result from reducing the process complexity through a trimming of the number of steps needed to integrate III-Vs with silicon CMOS.

One additional avenue that we will explore is the integration of silicon CMOS with other types of materials. We are already investigating materials for memory and energy storage, because this promises the creation of circuits with even greater functionality. Armed with more technologies, what can be achieved in future is set to overshadow the accomplishments to date.

Further reading

[1] smart.mit.edu/research/lees/lees.html
[2] www.circuit-innovation.org
[3] K.H. Lee *et. al.* Jap. J. of Appl. Phys. **54** 030209 (2015)
[4] E.A. Fitzgerald *et al. Monolithic 3D integration in a CMOS process flow* 2014 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Milbrae, CA, Oct 2014



Perfecting GaN power electronics with vertical devices

A vertical architecture holds the key to producing rugged transistors with a small footprint and a very high operating voltage

BY ISIK KIZILYALLI FROM AVOGY

IT IS HARD TO IMAGINE a world without electricity. It is this form of energy that powers so much of what we own and use, from PCs and TVs to clocks, light bulbs and the internet.

In different situations, we require different forms of electricity. Consequently, there is a need for an interface, based on power electronics that manipulates the frequency, amplitude and the phase of the electrical source. Conversion of electricity in this manner takes place in: laptop chargers, which convert AC power coming from the socket at between 110 V and 260 V, depending on the country, to 19 V DC power; in solar inverters that must transform 48 V DC power to 220 V AC power; and in an electrical vehicle, where a 200 V DC battery is used to drive a 650 V a three-phase AC motor.

At the heart of all these power systems are semiconductor devices, gate drivers and controller circuits. All these elements currently employ silicon devices – a combination of Schottky diodes and *p-i-n* diodes, and classes of transistor such as the MOSFET and IGBT.

Thanks to advances in the performance and the reliability of silicon-based power devices, voltage-manipulating electrical systems are more efficient, lighter and smaller than their predecessors. But this trend cannot continue throughout this decade and beyond, because the performances of silicon devices are encroaching their fundamental limits.

By far the best way to overcome this limitation is to turn to a new breed of semiconductor device, made from wide bandgap materials. Armed with SiC and GaN devices, electrical systems can be far lighter, smaller and more efficient than they are today.

Many firms are already working with wide bandgap materials, with the aim of either breaking into or expanding their share of the multi-billion dollar power semiconductor device market. This includes our team at Avogy of San Jose, California. Founded five years ago, we are pioneering the production

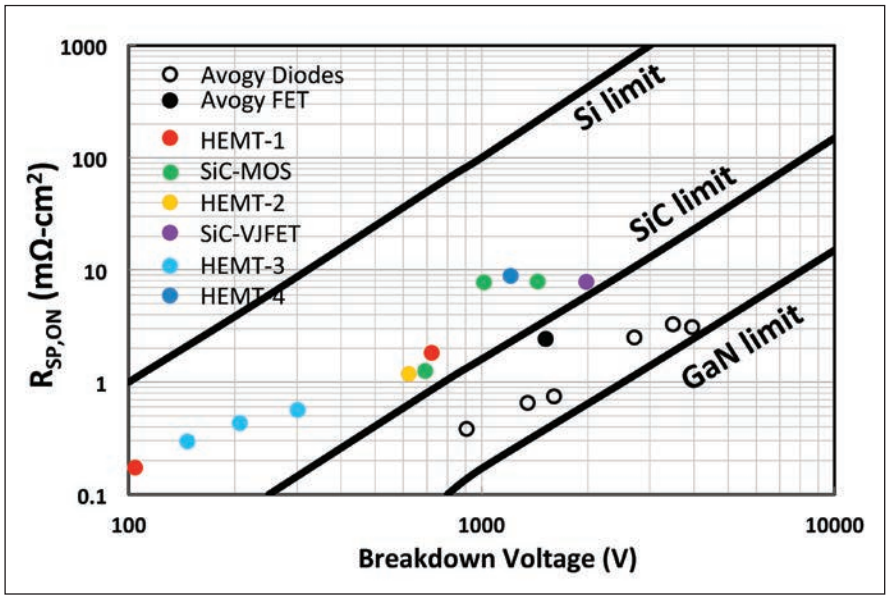


Figure 1. Power device figure-of-merit comparison of wide bandgap semiconductors.

of vertical GaN devices that are made on native substrates. Attributes of these novel, MOCVD-grown devices – which features current flow perpendicular to the wafer surface, and a drain contact on the backside of the substrate – include an incredibly low reverse-leakage current and a tremendous reliability at high temperatures.

By controlling doping in the drift layers, we can realise vertical architectures with drift layer thicknesses of 6 μm to 40 μm and a net carrier electron concentration as low as 1 x 10^{15} cm^{-3}. These characteristics enable the production of devices spanning a wide range of breakdown voltages.

Why GaN?

We make our devices from GaN because this material's properties are better than those of SiC, and are vastly superior to those of silicon. Strengths of GaN and its related alloys include: high bandgap energies, which are responsible for low intrinsic carrier concentrations that aid high-temperature operation; attractive transport properties, such as a high electron mobility and a high saturation velocity; a high critical breakdown electric field; and a high thermal conductivity.

A meaningful benchmarking of power devices must combine an assessment of the performance of blocking and conducting modes. A highly capable device must marry a low resistance, described by its specific resistance (R_{sp}), with a high blocking voltage that will enable it to sport a high breakdown voltage. These conflicting requirements for a unipolar power device have been captured by a figure of merit that is governed by the square of the blocking voltage, divided by the specific on resistance – this is roughly equal to the product of electron mobility and the cube of the critical electric field at which breakdown occurs (see Figure 1).

It is the cubic dependence on the critical electric field that enables wide bandgap devices to be vastly superior to those made from silicon. The critical electric field for silicon is 0.3 MV/cm, while it is at least 3.5 MV/cm for bulk GaN, and it could be as high as 3.75 MV/cm. Due to this order-of-magnitude supremacy in the critical electric field, if we ignore thermal and self-heating effects, we can expect a vertical GaN device to exhibit the same breakdown voltage and on-state resistance as a silicon equivalent, while having a footprint that is a thousandth of the size.

In practice, the shrinking of the footprint may not be quite as substantial as this – but it still delivers massive benefits. Smaller devices have lower capacitances, and they can switch at far higher frequencies, which allows a trimming of the size of the energy storage elements, a combination of inductors and capacitors.

The flaw in lateral thinking

For power applications, it is common knowledge that lateral devices are inferior to their vertical cousins. The vertical architecture –a HEMT in the case of GaN – is better suited to realizing higher breakdown voltages, thanks to the opportunity to deposit an arbitrarily thick

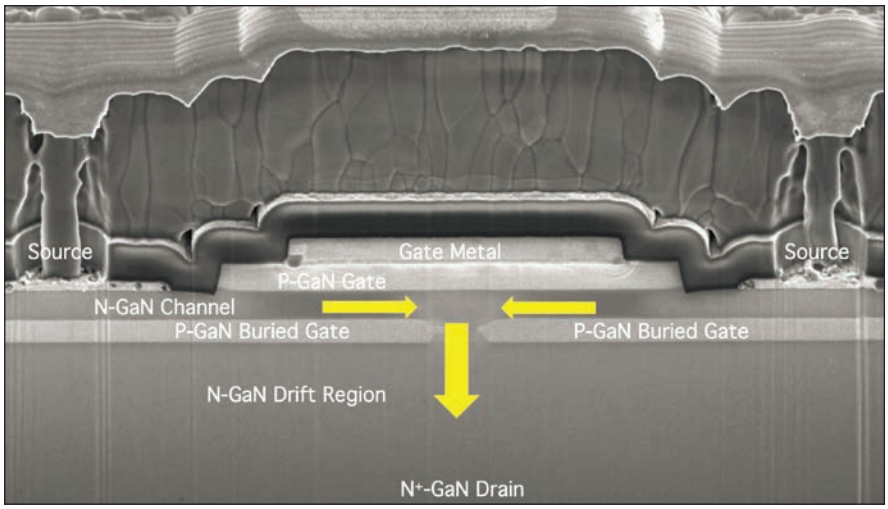


Figure 2. Cross-sectional, scanning-electron microscopy image of Avogy's vertical transistor. In this device architecture current flow (yellow arrows) is from source through the channel and down the aperture to the drift region. Current flow is controlled by both the top and buried *p*-GaN gates.

2016 IEEE Compound Semiconductor IC Symposium

INTEGRATED CIRCUITS and DEVICES in
GaAs, InP, GaN, SiGe, and other compound semiconductor and CMOS technologies

October 23–26, 2016
Doubletree by Hilton, Austin, TX, USA

Sponsored by the IEEE Electron Devices Society
Technically co-sponsored by the Solid State Circuits Society
and the Microwave Theory & Techniques Society

FIRST CALL FOR PAPERS

2016 CSIC Symposium

From its beginning in 1978 as the GaAs IC symposium, the IEEE Compound Semiconductor IC Symposium (CSICS) has evolved to become the preeminent international forum for developments in compound semiconductor integrated circuits and devices, embracing GaAs, InP, GaN, SiGe, and CMOS technology. Coverage includes all aspects of the technology, from materials, device fabrication, IC design, testing, and system applications. CSICS provides the ideal forum to present the latest results in high-speed digital, analog, microwave, millimeter wave, THz, mixed-mode, and optoelectronic integrated circuits. First-time papers addressing the utilization and application of InP, GaAs, GaN, Silicon, Germanium, SiGe, and other compound semiconductors in military and commercial products are invited. Specific technical areas of interest include:

- High performance devices such as GaN power conversion devices, 700 GHz SiGe HBTs & InP HEMTs
- Novel devices such as tunnel FETs (TFETs), carbon nanotubes, MEMS, graphene & diamond transistors
- Integration of III-V devices on Si
- Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics
- Device and circuit modeling concepts and implementation / EM and EDA tools
- Thermal management technologies, thermal simulation, and advanced packaging of high-power devices and ICs
- Device and IC manufacturing processes, testing methodologies, & reliability
- Analog, RF, mixed-signal, mm-wave, THz, power conversion and optoelectronic circuit blocks and ICs in III-V, CMOS, SiGe BiCMOS

Symposium Highlights

High quality technical papers will be selected from worldwide submissions for oral presentation and publication in the Symposium Digest. Invited papers and panel sessions on topics of current importance to the Compound Semiconductor IC community will complete the program. Extended versions of selected papers from the Symposium will be published in a special issue of the *IEEE Journal of Solid State Circuits*.

Primer Course

The Symposium will offer a primer course which is an introductory-level class intended for those wishing to obtain a broad and fundamental understanding of RFIC and High-Speed Analog-Mixed Signal technology. The Sunday evening course is designed to provide insight into the design of the principal RF building blocks, namely PAs, LNAs, Mixers and Oscillators, emphasizing the specific background needed for participants to understand and appreciate the papers presented in the Symposium Technical Program.

Short Courses

Two short courses will be held on Sunday, October 23, 2016. The courses are currently under development and will cover current topics in the industry. Organizer: Brian Moser, Qorvo. Ph: +1-336-678-8573, E-mail: Brian.Moser@qorvo.com.

Deadline for Electronic Receipt of Papers is Close of Business, April 22, 2016

Authors must submit a paper (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the content and measured results.

The abstract must concisely and clearly state:

a) **The purpose of the work**
b) **What specific new results have been obtained**
c) **How it advances the state-of-the-art or the industry**
d) **References to prior work**
e) **Sub-committee preference:**
   - **Advanced Devices and modeling**
   - **Analog, RF, and Microwave ICs**
   - **mm-Wave and THz ICs**
   - **High-Speed digital, Mixed-Signal & Optoelectronic ICs**

The paper must include: the title, name(s) of the authors(s), organization(s) represented, corresponding authors' postal and electronic addresses, and telephone number. A paper template is available from www.csics.org. Please indicate your preference for subcommittee review. The program committee will honor the authors' preference where possible, but reserves the right to place the paper in other review categories.

All company and governmental clearances must be obtained prior to submission of the abstract.

Authors must submit their papers in PDF format electronically using the www.csics.org web page. They will be informed regarding the results of their submissions by June 3, 2016. Authors of accepted papers will be required to submit to the IEEE their final camera-ready paper by July 22, 2016 for publication in the Symposium Technical Digest. The accepted papers may be used for publicity purposes. Portions of these papers may be quoted in magazine articles pubilcizing the Symposium. **Please note on the paper if this is not acceptable.**

Further questions on paper submission may be addressed to the Symposium Technical Program Chair:

Jim Carroll
NI-AWR Group
Ph: +1-469-248-5472
E-mail: jim.carroll@ni.com

All Symposium information, including paper submission instructions and a link to our paper submission address is available on the CSICS website at:

www.csics.org

Figure 3. Zolt Plus: Just one device is needed to charge laptops, tablets and phones simultaneously.

electron drift layer. What's more, vertical devices can deliver higher currents, such as 50 A or more, without the need for a parallel architecture; they are less prone to thermal management issues, thanks to power dissipation in the bulk volume; and the die-yield-per-wafer is higher, because electron drift regions extend into the device, rather than spread out laterally.

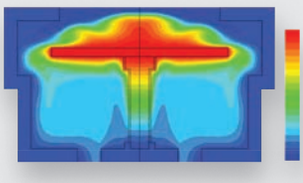
An additional strength of the vertical architecture is that it simplifies incorporation of *p*-type GaN. This, combined with *n*-type drift regions of high quality and low defect density, allows the fabrication of devices with avalanche capability. Armed with this particular attribute, vertical GaN devices can go into avalanche breakdown safely without suffering from either catastrophic failure or parametric degradation. In power switching and rectifying applications, a premium is placed on the ruggedness in breakdown, because it eliminates the need for supplementary snubber circuits, which impose system-level performance and efficiency penalties.

It is worth noting that vertical devices are actually the norm in power applications – this is the architecture of silicon and SiC devices that are operating above 600 V. Taking this route with GaN raises a question regarding the choice of substrate. It is possible to grow GaN layers on foreign substrates, such as silicon and SiC, but thermal and lattice mismatches with GaN make it very challenging to realise electron-drift regions with a thickness of 10 μm and a high material quality. If these layers are too thin, the breakdown voltage is compromised; and if the epilayers have a defect density in excess of 10^8 cm^{-2}, this impairs both yield and critical characteristics, such as breakdown voltage, off-state leakage current and reliability. The latter includes the operating life of the device, its high-temperature reverse-bias behaviour and avalanche ruggedness.

Despite the many compelling reasons for using native substrates for fabricating vertical GaN power devices, there are very few reports by teams pursuing this approach, due to the lack of availability of low-defect-density (less than 10^6 cm^{-3}) bulk GaN substrates. Compounding this, it is often assumed that bulk GaN substrates are too expensive to be commercially viable. That's not actually the case, however. Today there are many suppliers of bulk GaN substrates, and due to research and development efforts, material quality is improving rapidly. High prices, meanwhile, are becoming less of an issue, as they fall through economies of scale, thanks to increasing use in the optoelectronic industry. It is also important to note that vertical devices that are fabricated on native substrates have a far smaller die area than lateral structures, and they can expand the breakdown-voltage-limited, safe-operating-area to well beyond 600 V.

We are highlighting the high voltage capability of these devices by producing GaN diodes with breakdown voltages of 4000 V. Reduce this to 1200 V, and we are able to routinely reach pulsed current levels of 400 A. We are investigating the capability of devices operating with this breakdown voltage within the ARPA-E funded SWITCHES programme, where we are targeting cost parity with silicon equivalents. If we fulfil this goal, our GaN devices will be very competitive, thanks to a switching speed that is superior to that of the incumbent device by a factor of 10 to 50.

Optimize the Thermal Performance of your Process Equipment.



Extensive computational tools enable product designs to be highly refined for ultimate performance.

Multi-zone circuit layouts in a polyimide construction are highly customized to deliver exacting performance up to 250°C.

EZ-ZONE® RM Multi-loop controllers are fully scalable with up to 152 PID Loops and 256 monitor points per system.

Watlow provides innovative solutions to help process tool manufacturers meet the needs of the semiconductor technology roadmap. Our approach is to work collaboratively to help solve complex thermal challenges associated with state-of-the-art manufacturing processes; helping to improve yield, throughput and cost of ownership. This includes innovative heaters, controllers and sensors for use in front-end and back-end applications such as CVD, PECVD, Etch, Diffusion, Bonding, IC test and more.

ASSURANT™ gas and pump line heaters feature high temperature capabilities with low outgassing.

Contact Watlow® today for the latest thermal solutions for semiconductor applications.

European Technical Sales Offices

Germany +49 (0) 7253-9400-0
info@watlow.de

France +33 1 41 32 79 70
info@watlow.fr

Italy +39 02 4588841
italyinfo@watlow.com

Spain +34 91 675 1292
info@watlow.es

UK +44 (0) 115-964-0777
info@watlow.co.uk

WATLOW®

One necessity for vertical devices – but not for their lateral peers – is that the device is properly terminated around the edges, while electric field gradients are accommodated within the structure. We have succeeded in this endeavour by modifying junction termination extension strategies originally developed for vertical silicon and SiC devices. Efforts were also directed at the development of robust ohmic contacts for *p*-type GaN, as well as a bottom *n*-type contact that is formed on nitrogen-rich GaN.

We have evaluated our wide portfolio of vertical field-effect transistors, extracting values for various material characteristics, including electron mobility, minority carrier lifetime and thermal conductivity. We have plugged these values into sophisticated device models, and by accounting for thermal (Joule) heating effects, we have been able to develop scaling rules for our vertical devices. This has given us a toolkit for determining the size of devices and generating cost models. Additional support for developing vertical-junction, field-effect transistors has come from the knowledge acquired from studying *p-n* devices.

Today, we are in pre-production with a structure that is flexible enough to accommodate normally-on and normally-off implementations (see Figure 2). We are pursuing the normally-on variant, because it is a more manufacturable device. Due to the lack of a mature, viable *p*-type ion implantation and activation scheme for GaN, we have developed planar, selective epitaxial MOCVD growth techniques for defining the *n*-GaN channel regions and the top *p*-GaN gate regions. These are added after etching an aperture in the buried *p*-GaN layer.

With our devices, the buried *p*-GaN region must be connected to the source (in the case of normally-off devices) or to the gate (in normally-on devices), rather than left floating. We have also developed a plug process, so that we can form an ohmic contact on an etched *p*-GaN surface.

This approach, which is protected by more than 60 patents, has enabled us to demonstrate field-effect transistors with breakdown voltages exceeding 1500 V and forward currents of more than 5 A. As expected, the vertical architecture of these transistors enables them to be free from threshold voltage shifts, on-resistance degradation or collapse, and reductions in drain current collapse during operation or under high temperatures stress. With breakdown voltages of up to 4 kV, and drive current capabilities of up to 400 A, our devices can target myriad markets (see Table 1 for a listing of regular market segments, and the incumbent semiconductor technologies serving these applications).

Out of all these opportunities, we have started by targeting the power supply market. This is being pursued through our Zolt brand, a range of the world's lightest, smallest and most efficient laptop chargers (see Figure 3). At the heart of these products is our proprietary and patented core systems (resonant switching topology) and component technologies.

Our company's next steps include working with bulk GaN substrate vendors to: further improve substrate quality; cut the cost of bulk GaN wafers; and quickly see the launch of 4-inch substrates. Device-related efforts will include developing higher current capability, designing higher-power electronic systems for data centres and solar applications, and conducting further reliability studies that should prove that vertical transistors formed on native substrates fulfil standards required by automotive markets.

	Power Supplies*	Solar	EV	Wind	Motor Drive	UPS/Grid/ Rail/Ship
Voltage (V)	600-1200	600 - 1200	600 - 1200	1200 - 3300	600 - 1200	1200 - 3300
Current (A)	0.5 – 20A	1 – 75A	50 – 200A	100 – 200A	2 – 100A	100 – 400A
Devices in Systems Today	Si MOSFET Si PN SiC SBD	Si MOSFET Si IGBT Si PN SiC SBD	Si IGBT Si PN	Si IGBT Si PN	Si IGBT Si PN	Si IGBT Si Thyristor Si PIN

Table I. Power electronics market segments and semiconductor technologies.

EVG®

invent
innovate
implement

www.EVGroup.com

Solutions for

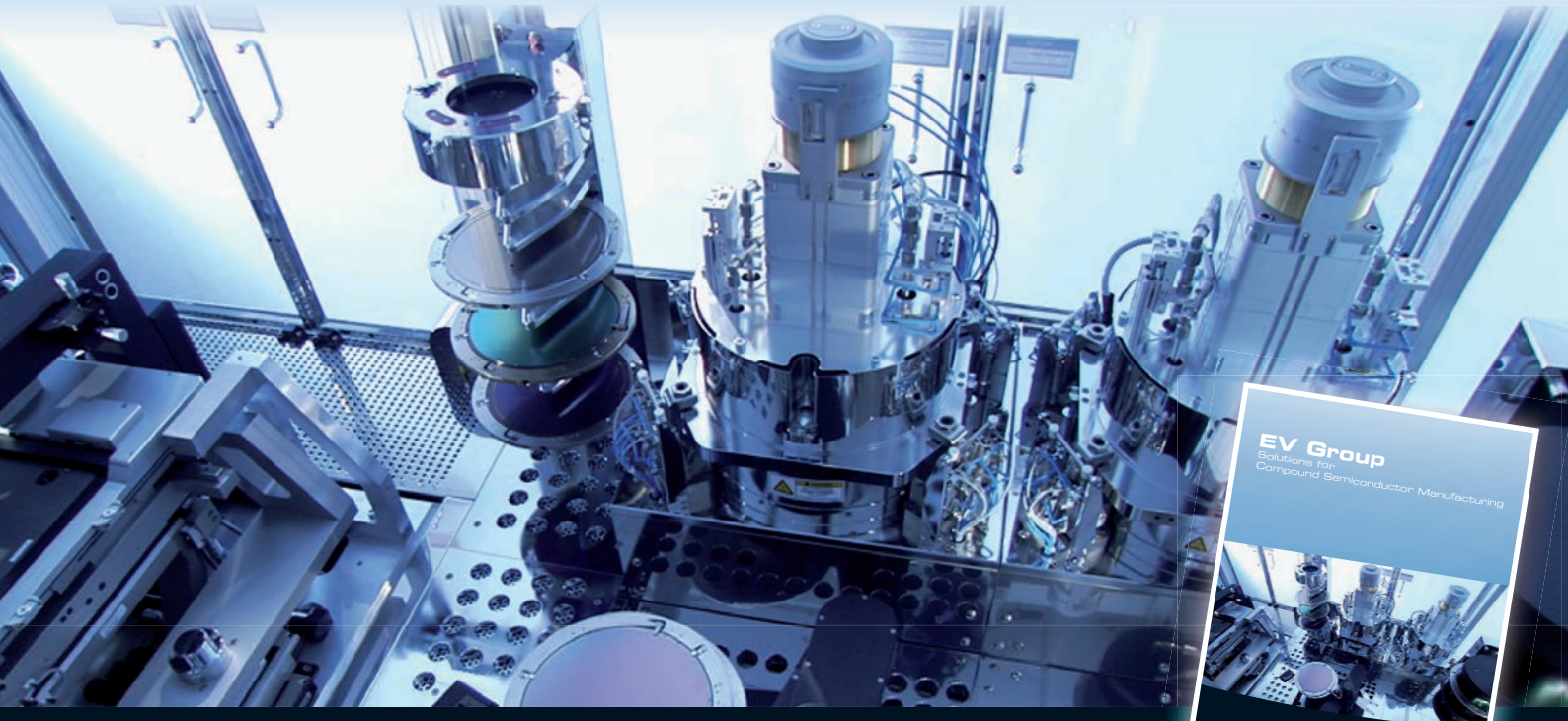
COMPOUND SEMICONDUCTOR MANUFACTURING

Wafer Bonding
for Heterogeneous Integration, Layer Transfer and Advanced Packaging

Optical and NanoImprint Lithography
for Device Patterning and Advanced Packaging

Advanced Resist Processing
for Dielectrics, Thick / Thin Resist Layers, Through Vias and High Topography

Temporary Bonding and Debonding
of Thinned and Fragile Compound Semiconductor Substrates



For more information visit **www.evgroup.com/compoundsemi**

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

PIC International Conference
SPEAKERS ANNOUNCED!

PIC International 2016 will provide timely, comprehensive coverage of every important sector within the photonics integrated circuits industry.

PIC International Conference is being launched to strengthen the relationships between the makers and the users of photonics integrated circuits.

PIC International will be held and co-located with the highly successful 6th CS International conference at the Sheraton Brussels Airport Hotel, Belgium on Tuesday 1 & Wednesday 2 March.

Attendees at PIC International will hear industry-leading insiders delivering more than 30 presentations spanning six key themes which collectively provide complete coverage of the photonic integrated circuits industry and offer many opportunities to meet many other key players within this community.

Book your place now at:
www.picinternational.net/register

This two day event covers six themes

Conference Chair: Michael Lebby (left)– Chair in Optoelectronics - Glyndŵr University Board Director, Lightwave Logic
Theme Chair: Jose Pozo - Director of Technology and Innovation at EPIC

Where Should the Laser Go?

Is heterogeneous integration the best option for lighting up the IC? Or is it better to couple the laser's emission onto the chip?

William Ring – BB Photonics | High speed photonic integrated receivers for 100G and above

Gregory Fish - Aurrion | Heterogeneous integration: creating photonic circuits for advanced systems-in-package

Shinji Matsuo – NTT Photonics Lab | Excelling in the efficiency of lasers formed on silicon

Fang Wu – ArtIC Photonics | How far does monolithic integration go?

Hamid Arabzadeh – Ranovus Turning to quantum dot lasers for terabit communication?

Driving Deployment of PICs in Datacentres

PICs are a solution to the rocketing demands facing datacentres. But what do they need to deliver, and how can they be put to best use?

Brad Booth – Microsoft | Lighting up the Cloud

Arlon Martin – Mellanox Technologies | Using silicon photonics to support next-generation cloud computing, datacentre and high performance computing connectivity

Di Liang – Hewlett Packard Enterprise | Constructing very large scale PICs for datacentres

Jason Orcutt – IBM | Towards cost-effective 100 Gb/s optical transceivers

Craig Thompson – Finisar | Creating the building blocks for better datacentres

Increasing the Capability of Optical Networks

Are PICs about to dominate the landscape of optical networks? Is there room for different forms of device?

Silvio Abrate - ISMB | How can silicon photonics benefit optical access deployment? An example from the FABULOUS EU Project

Mohamed Osman – McGill University | Photonic circuits enabling multi-dimensional IM/DD systems for short reach optical interconnects

Harald Bock – Coriant | Silicon photonics in optical networking – yesterday's hype, today's reality, tomorrow's vision

What is the Role of the Foundry?

Can companies afford to make PICs in-house? And if they do outsource, what should they look for from a foundry?

René Heideman – LioniX | LioniX: Aid the growth of photonics with the TriPleX integrated optics platform

Katarzyna Ławniczuk - JePPIX | Accelerating photonic ASICs development

Samuel Wang – Global Communication Semiconductors | Can foundries underpin the success of the PIC?

Luc Augustin – Smart Photonics | Enabling a broad range of applications with a generic integration platform on InP

Philippe Absil – IMEC | Imec's flexible, state-of-the-art silicon photonics platform overview

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

Do we Have the Tools for Designing, Making, Packaging and Testing PICs?

The silicon CMOS industry sets a benchmark for chipmaking. How can the PICs industry catch up?

Sean Anderson – CISCO | Bringing first-time-right design to silicon photonics

Stefano Grillanda – Politecnico di Milano | Taking a close, damage-free look at the light in PICs

Niek Nijenhuis – PhoeniX Software | Current status of photonic and electronic design tools and flows

Pieter Dumon – Luceda Photonics | Make photonic IC designers re-use 40 years of electronic IC design experience: challenges and opportunities

André Richter – VPI Photonics | From circuit-level to mask layout and back – design, analysis and optimisation of large-scale PICs

Iñigo Artundo – VLC Photonics | Outsourcing options and trends for the fabless development of PICs

Ignazio Piacentini – FiconTEC | Lowering the cost of PICs assembly and testing via advanced automation

Jonas Flueckiger – Lumerical | Towards an EPDA Design flow

Christopher Bower – X-Celeprint | Heterogeneous integration of optoelectronic devices by micro transfer printing

Giovan Battista Preve – INPHOTEC | Advanced silicon photonics packaging: challenges, trends, automation and the role of the INPHOTEC Photonics Technology Center

A Question of Material: InP, Silicon or Something

InP is fragile and expensive, but a great material for integrating all the components on one chip. Silicon can't do this, but is a larger, more mature platform. So is it the case of selecting the right material for the particular application, or can there be a universal, long-term winner?

Lê Nguyên Bình & Thomas Wang Tao – Huawei | A system-and-networking view on PIC technologies

Meint Smit – TU Eindhoven | InP and silicon: A strong combination for integration of photonics and electronics

Ronald Broeke – Bright Photonics | Selecting materials for PIC production

Vincent Reboud – CEA-Leti | A bright future for germanium-on-insulator wafers?

Martijn Heck – Aarhus University | Hybrid and heterogeneous PICs for high performance applications

Martin Guy – TeraXion | InP or silicon photonics or both? Choosing the right material platform for applications

Martin Eibelhuber – EV Group | Advanced wafer bonding techniques for photonic integration

Michael Lebby – Lightwave Logic | Presentation TBC




Book your place NOW !

Visit www.picinternational.net/register to secure your place

PLATINUM SPONSORS

EAG Evans Analytical Group

EVG

ficonTEC micro assembly machines

INPHOTEC Integrated Photonic Technologies Center

LUCEDA PHOTONICS

VLC PHOTONICS

VPIphotonics DESIGN AUTOMATION

YOLE Développement

GOLD SPONSORS

IQE

SMART Photonics III-V foundry services

Yenista OPTICS

ADDITIONAL SPONSORS

Lanyard Sponsor

IQE

USB Sponsor

JSR Micro JSR MATERIALS INNOVATION

Delegate Bag Sponsor

LIGHTWAVELOGIC™

Supported by

EUROPRACTICE IC SERVICE

imec

Mastering the marriage of III-Vs and silicon

Defect-trapping pockets enable the growth of high-quality films of GaAs on large-area, conventional silicon substrates

BY QIANG LI AND KEI MAY LAU FROM HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

IN 1965, GORDON MOORE, at the time director of research and development at Fairchild Semiconductor, published a now-famous article in *Electronics*. In his four-page piece he outlined the benefits wrought from shrinking the dimensions of silicon transistors, and how fast this level of miniaturization might occur. Hindsight highlights the greatness of Moore's insight, which has been captured by a law named after him.

It is now just over fifty years since the publishing of Moore's seminal paper. And for most of that time, by simply scaling device dimensions, engineers have delivered gains in speed and cost while trimming the power required to operate each transistor. But recently, shrinking device size has not been enough – introducing new materials has held the key to maintaining improvements in performance while trimming dimensions. In this regard, the biggest modification so far has been the shift from SiO_2 to high-κ HfO_2 as gate dielectric, to prevent leakage currents from escalating to unacceptable levels when the thickness was scaled to a few angstroms.

This revolution in the range of materials employed within the transistor is driving a new era for digital and memory devices. The age of 'more-than-Moore' has arrived. This is a time when both new materials and three-dimensional non-planar architectures are

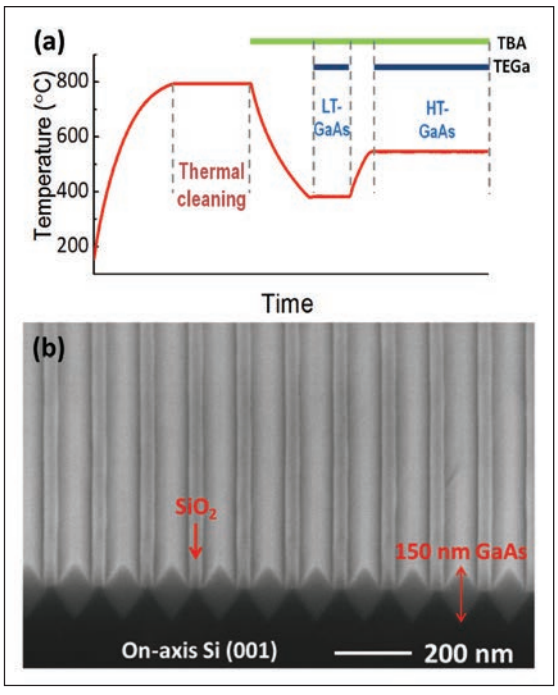


Figure 1: (a) Gas flow and temperature sequence for planar GaAs nanowire growth on silicon using a two-step procedure. The precursors that are used are triethylgallium (TEGa) and tertiarybutylarsine (TBA) (b) tilted-view scanning electron microscopy image of planar GaAs nanowires on silicon.

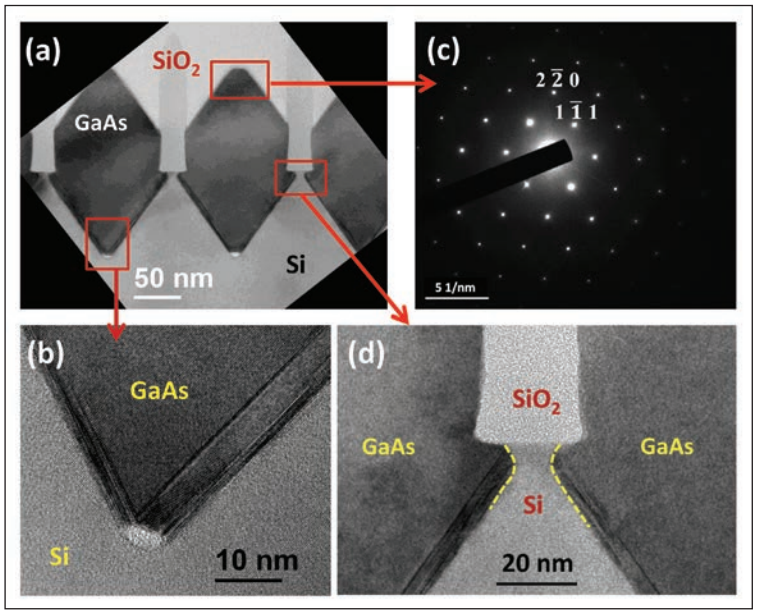


Figure 2: (a) Cross-sectional transmission electron microscopy image of GaAs nanowires; (b) high-resolution transmission electron microscopy image of the GaAs-silicon interface; (c) selective diffraction pattern taken at the apex of the nanowires; (d) transmission electron microscopy image of the stacking faults trapped by a 'tiara'-like structure made of silicon.

viewed as the way forward. There is also the promise of system-on-chip solutions that dramatically improve capability, while trimming size, cost and power dissipation.

Advances in 'more-than-Moore' will require the heterogeneous integration of broad classes of materials that are traditionally not present in silicon fabs. Silicon is great for electronic switching and memory, but its indirect bandgap precludes its use in efficient light emission and photon interaction. This weakness is a major flaw in the 'big data' era, where there is explosive growth in demand for data transmission. But hopefully silicon's deficiency can be addressed by integrating it with photonic semiconductors, such as III-Vs. Such a marriage could revolutionize future on-chip and chip-to-chip communication technologies with optical interconnects.

The most attractive option for bringing these two classes of material together is to grow an epitaxial III-V film on a silicon substrate. There are challenges associated with this, primarily arising from differences in the lattice and thermal mismatch and crystal polarity. Attempts to succeed in this endeavour date back to the 1980s, but despite a great deal of effort by researchers from all around the globe, progress has been slow, and breakthroughs few and far between.

One group that has made significant strides in this direction is our team from Hong Kong University of Science and Technology (HKUST). We are exploring

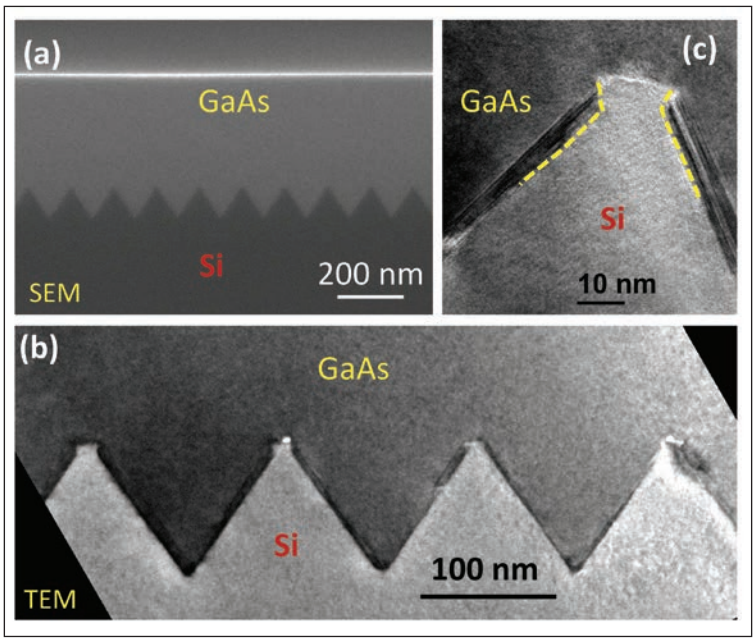


Figure 3: (a) Cross-sectional scanning electron microscopy of a 300 nm coalesced GaAs film using the nanowires as a special buffer; (b) transmission electron microscopy image showing that stacking faults at the hetero-interface are localized and trapped by silicon pockets; (c) transmission electron microscopy image highlighting the defect trapping effect by patterned silicon after coalesced thin-film growth.

technologies for growing III-V nanostructures and thin films on CMOS-compatible silicon substrates by MOCVD. We are by no means alone in pursuing this approach. However, while most groups are using catalysts and focusing on vertically orientated nano-structured materials, we are working on compliant substrates, which are highly compatible with the well-established silicon planar processing technology. Our great strength is that we can close the gap between the material growth schemes and the ultimate device implementation.

Our efforts can be traced back to the 2000s, when we first took the lead in the metamorphic growth of InP on planar (001) silicon substrates. Instead of using conventional techniques such as compositional grading of III-V alloys or a germanium buffer, we developed a two-temperature growth process and optimized intermediate GaAs buffers. We overcame the problems associated with an 8 percent lattice mismatch, and achieved device-quality InP featuring a smooth surface. This led to the demonstration of InAlAs/InGaAs based HEMTs and MOSHEMTs on planar silicon. Both of these types of device exhibit state-of-the-art characteristics.

A two-pronged attack

To further improve the material crystal quality, we have adopted a hybrid approach to forming III-Vs on silicon. We combine selective-area heteroepitaxy with epitaxial lateral overgrowth, which is undertaken on nanometre-scale, patterned silicon substrates. One of the strengths of using this particular form of substrate is that it allows the use of recessed pockets – designed correctly, they offer a unique, defect-trapping capability that is not possible with conventional blanket heteroepitaxy.

Taking this approach, we produced ultra-low-defect antiphase-domain-free GaAs thin films on silicon. These were formed via deposition on highly ordered in-plane GaAs nanowires on V-grooved silicon. To produce these GaAs films, we began by taking planar silicon (001) wafers, and patterning them with [110]-orientated SiO_2 stripes with a line-opening width of 90 nm and a line pitch of 130 nm. This created regions in the silicon substrate with a shallow recess, which defines the defect-containing silicon pockets. This approach is notably different from traditional blanket heteroepitaxy, which does not employ the exactly orientated substrates that we use, but rather off-cut silicon, which minimises the formation of anti-phase domains.

We avoid anti-phase domains by etching V-shaped grooves at the bottom of the trenches. This technique, which has been demonstrated by a team of researchers from imec, Belgium, enables the deposition of III-V materials on exposed {111} silicon facets. On these side walls, the films that form tend to be free from anti-phase domains.

By adopting a two-step growth method for the epitaxy of planar GaAs nanowires on V-grooved silicon, we are able to realise a superior crystalline quality (see Figure 1 (a)). After thermal cleaning at 800°C in an MOCVD chamber, we begin by depositing a GaAs nucleation layer at 385˚C. This is followed by the growth of a GaAs main layer at typically 550˚C.

Strengths of our highly-ordered, site-controlled GaAs nanowires, which are separated by SiO_2, include smooth facets and uniform morphology (see Figure 1(b)). Analysis of X-ray diffraction ω-rocking curves indicates that nanowires with a thickness of 150 nm yield a full-width-at-half-maximum that is comparable to that of 1 μm-thick GaAs thin films on planar off-cut silicon. In other words, switching from planar growth to our novel defect reduction approach slashes buffer thickness by more than a factor of six for the same crystalline quality.

Scrutinising our structures with cross-sectional transmission electron microscopy uncovers some peculiar defect-trapping phenomena (see Figure 2 (a)). Close examination of the GaAs-silicon hetero-interface reveals that the 4.1 percent lattice mismatch is not accommodated by propagation of threading dislocations, but by formation of stacking-disordered layers just a few nanometers thick (see Figure 2 (b)). Thanks to this novel strain-relief mechanism, the GaAs bulk layer has a high crystalline quality, as evidenced by the selective diffraction pattern taken at the apex region (see Figure 2(c)).

A tremendous tiara

Looking more closely at the glide of the few-layer stacking faults at the GaAs-silicon hetero-interface reveals that the disordered layers are stopped by a 'tiara'-like structure (see Figure 2(d)). This is made of silicon beneath the SiO_2 walls, and it originates from silicon recessing by combined dry etching and potassium hydroxide wet etching.

Blocking of defects by this type of hetero-epitaxial approach is often referred to as aspect ratio trapping (ART), or the epitaxial necking effect. Although research on ART is not new, it has traditionally focussed on the growth of high-quality crystals in small cavities, which are defined by a patterned dielectric. There have also been a handful of attempts to produce large area planar films by combining ART with epitaxial layer over-growth. However, the dielectric patterns have spawned hard-to-control asymmetries and irregularities in faceted growth regions. The upshot is a high density of coalescence defects, a rough surface morphology and even more defects originating from the dielectrics.

Our films do not suffer from the same fate, because our tiara-like structure enables the diamond-shaped silicon pocket to localise and confine most of the hetero-interface defects. Another way to look at this is that by removing SiO_2, our nano-sized wires coalesced into planar thin films with a smooth surface, while retaining the defect trapping capability associated with the epitaxial necking effect.

Removing SiO_2 between the merging nanowires improves the surface morphology of the resulting planar thin films. According to images obtained by scanning electron microscopy, just 300 nm of GaAs overgrowth is needed to realise a flat surface (see Figure 3 (a)). Further inspection of the structure by transmission electron microscopy reveals that the silicon pockets can prevent interfacial defects from extending into the upper layers (see Figure 3(b) and (c)). Meanwhile, atomic force microscopy uncovers a surface roughness of 1.9 nm across a 5 μm by 5 μm scan area, and shows that the surface is free of antiphase-domain boundaries (see Figure 4).

"Blocking of defects by this type of hetero-epitaxial approach is often referred to as aspect ratio trapping (ART), or the epitaxial necking effect. Although research on ART is not new, it has traditionally focussed on the growth of high-quality crystals in small cavities, which are defined by a patterned dielectric"

We have assessed the crystalline quality of the coalesced GaAs films with X-ray diffraction. Peaks from ω-rocking curves have a full-width at half-maximum that decreases from 230 arcsec to 154 arcsec as the thickness of GaAs increases from 1 μm to 2 μm. The ω-2θ linewidth is 72 arcsec. These values indicate good material.

One way to look at the success that we have had is that compared to GaAs films grown on non-patterned, off-cut silicon, the X-ray linewidth is cut by more

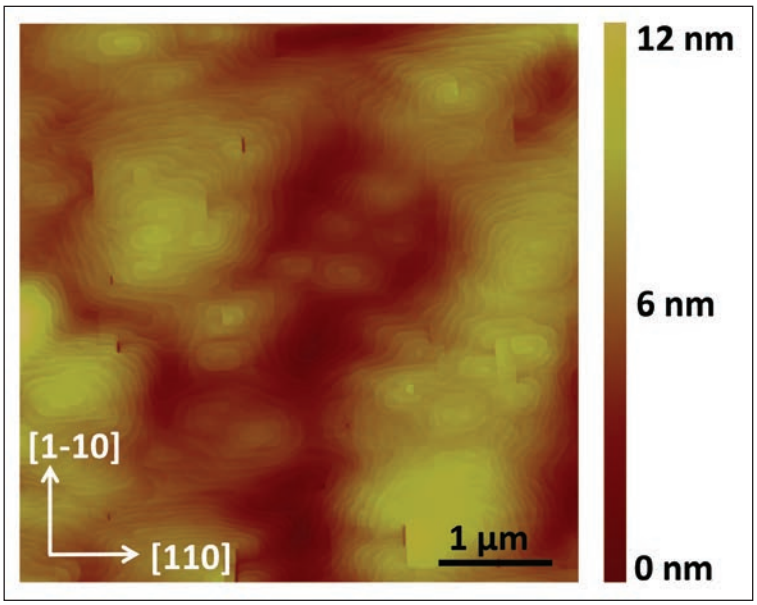


Figure 4: Atomic force microscopy image of a 300 nm-thick coalesced GaAs film grown out of high-ordered nanowires.

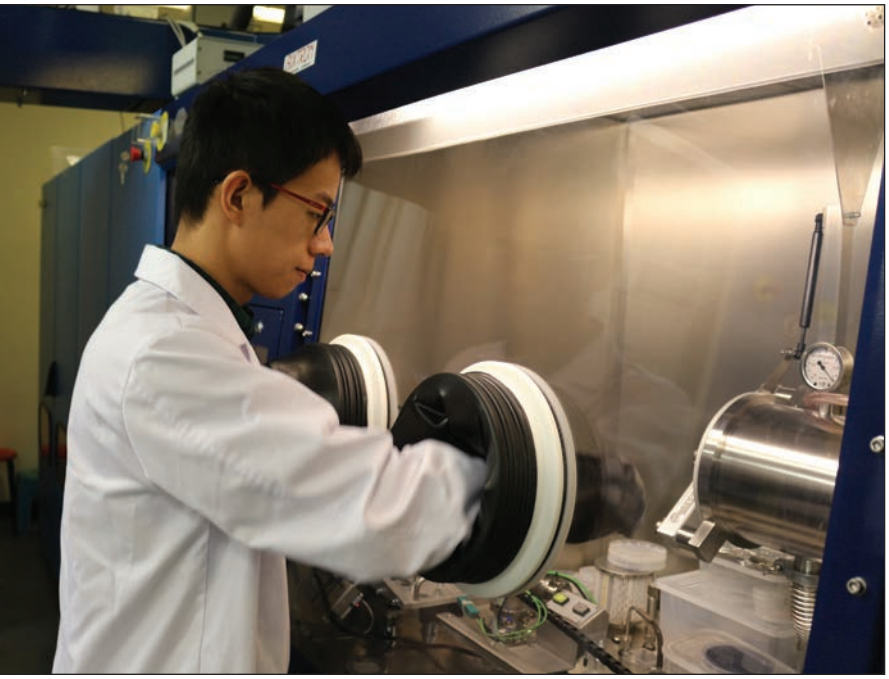
than 50 percent with the same buffer thickness. Alternatively, a comparable X-ray linewidth is possible with a three-fold reduction of buffer thickness (see Figure 5).

Characterising our structures demonstrates that the benefits of our growth scheme are not limited to removing the need to use off-cut silicon to suppress anti-phase domains – they also include a superiority over traditional blanket hetero-epitaxy, when it comes to trapping and reducing defects. What's more, our efforts show that low-defect-density GaAs can be deposited on silicon without the need for other intermediate buffers, such as those based on germanium or graded SiGe.

Additional improvements in the crystalline quality of our as-grown GaAs films are possible by introducing other defect reduction techniques. For example, undertaking three-cycle thermal annealing on 1 μm GaAs on V-grooved silicon cuts the full-width at half-maximum of the ω-rocking curve from 230 arcsec to 180 arcsec.

Another lever for increasing material quality is the nanowire pitch size. Get this right and the overall defect density in the coalesced films can be further reduced in the epitaxial layer overgrowth process. Note that if the lateral overgrowth distance is too long, it introduces coalescence defects and increases surface roughness.

For each material one would expect that the optimal growth conditions and the shape of the silicon pockets could be different. We are now looking at materials with an even larger lattice mismatch with silicon, such as InP, because this combination would enable the fabrication of long-wavelength lasers and HEMTs on silicon. These efforts have already led to some success – we have produced some InP-on-silicon compliant substrates.



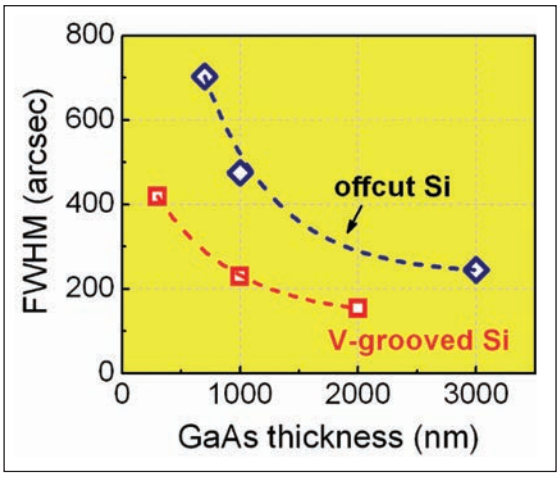


Figure 5: Comparison of the full-width at half-maximum of X-ray diffraction ω-rocking curves for GaAs thin films grown on non-patterned, off-cut silicon and V-groove patterned silicon substrates.

Further opportunities for our technology are associated with using our epitaxial planar nanowires to construct a wide variety of heterostructures on industrial-standard (001) silicon substrates. Combining these nanostructured materials with a nanofabrication process should provide opportunities to develop novel devices and improve and refine conventional devices in three-dimensional geometries.

Using the nanowire as a starting point for forming micro-scale crystals and large-area thin films should unlock the door to the fabrication of a range of devices on large-area, inexpensive and abundant silicon substrates. They include those requiring thick hetero-epitaxial layers, such as monolithically integrated quantum dot lasers, detectors and multi-junction solar cells. If our work kicks-starts a global effort in this direction, it may also light a path towards the long-dreamed-of convergence of electronics and photonics on a common platform.

Further reading

Q. Li *et. al.* Appl. Phys. Lett. **106** 072105 (2015)
Q. Li *et. al.* J.of Crystal Growth **405** 81 (2014)

Slashing power consumption with tunnel FETs

Tunnel FETs are the post-CMOS solution, thanks to their ability to deliver great performance while consuming very little power

BY RAHUL PANDEY AND SUMAN DATTA FROM PENNSYLVANIA STATE UNIVERSITY AND THE UNIVERSITY OF NOTRE DAME

THE SILICON MOSFET is the workhorse of today's semiconductor industry. Through relentless shrinking of its dimensions and steady reductions to its operating voltage, this transistor has driven phenomenal gains in IC performance and device efficiency over several decades.

This state of affairs can't last, however. The benefits wrought by reducing the size of the transistor, which are detailed in Moore's law, are now under threat. If the operating voltage of today's transistors is trimmed a little more, this would lead to an unacceptable drop in transistor performance. Or to look at it a different way, if the threshold voltage of the silicon MOSFET were reduced to enable a scaling of the operating voltage, there would be an exponential increase in the off-state current, and a corresponding explosion in energy loss. This is a big deal for circuit designers, because the sub-threshold leakage power is as significant as the active power in microprocessors.

The high sub-threshold leakage power stems from the inability of the MOSFET to provide steep switching from the on-state to off-state (see Figure 1(a)). Consequently, even when the MOSFET is turned off, there is a significant leakage current.

One way to assess the switching ability of the

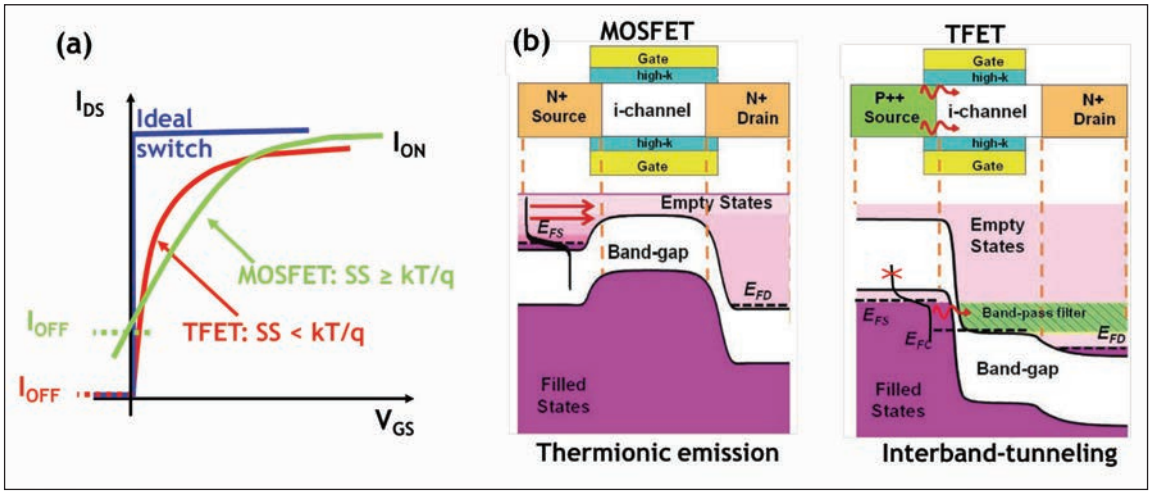


Figure 1. A comparison of the incumbent technology, the MOSFET, and a possible successor, the tunnel FET: (a) switching characteristics, and (b) the source-channel carrier-injection mechanism. Filtering of high-energy carriers in the tunnel FET produces sub-KT/q switching slope, which holds the key to reducing the power consumption of the device.

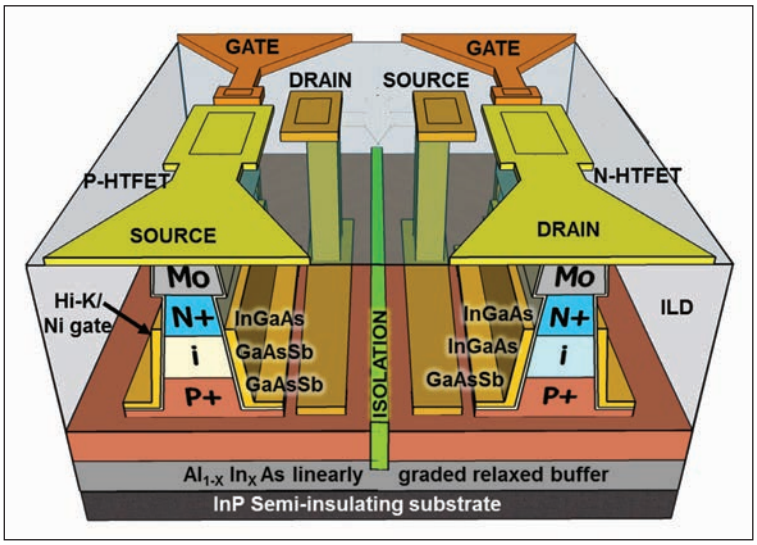


Figure 2. An attractive candidate for enabling a reduction in operating voltage of future logic circuits is complementary *p*-type and *n*-type hetero-junction tunnel FETs formed with a common metamorphic buffer technology.

MOSFET is to determine its switching slope, which is defined as the change in gate voltage needed to produce a decade change in drain current. To achieve a limited improvement in the switching slope and improve electrostatistics, there has recently been a change in the transistor architecture from a planar design to a three-dimensional finFET. These newer devices, which feature a fin protruding out of the plane of the wafer, made their commercial debut in 2012 at the 22 nm node, with those at the 14 nm node following in 2014.

Although the new three-dimensional architecture has bought the silicon industry more time, there is no escaping the fundamental limitations on the switching slope for the MOSFET – it is related to a Boltzmann distribution describing the energy of carriers in the source region that are emitted thermionically over the barrier. This Boltzmann tyranny in the MOSFET, which restricts the switching slope to 60 mV/decade at room temperature, has driven efforts to look at alternative devices delivering steeper switching. These potential successors could extend supply voltage scaling without compromising leakage power and performance.

Researchers pursuing this goal are not solely focused on a quest for lower voltage, but are also concerned with transport enhancement. To succeed on both fronts, they are investigating the likes of novel materials, strain and bandgap engineering. Within this effort, one device that is piquing the interest of many is the tunnel FET. It promises to deliver switching that is steeper than an optimised MOSFET.

Our team at Pennsylvania State University and the University of Notre Dame is developing a tunnel FET for maintaining the march of Moore's law. We have already had tremendous success, with highlights including the first demonstration of an all III-V system based on complimentary hetero-junction tunnel FETs that can operate at a low voltage and deliver a record-breaking current and switching performance. Our *n*-type tunnel FETs feature an InGaAs channel and a low density of interface traps, and our *p*-type tunnel FETs combine a significantly improved interface with a GaAsSb channel.

We have devoted a great deal of effort to developing and refining tunnel FETs, because they have the potential to deliver superior switching to MOSFETs, due to an improvement in the manner in which carriers are injected into the channel (see Figure 1(b)). In a MOSFET, modulation of the gate adjusts the source-to-channel energy barrier, and this controls the thermionic emission of carriers into the channel region. In contrast, with a tunnel FET, carrier injection into the channel comes from inter-band tunnelling from the source to channel region. The great merit of interband tunnelling is that it filters out the high-energy carriers in the Boltzmann distribution that are present in the valence band of the source region. Thanks to this carrier 'cooling', switching in the tunnel

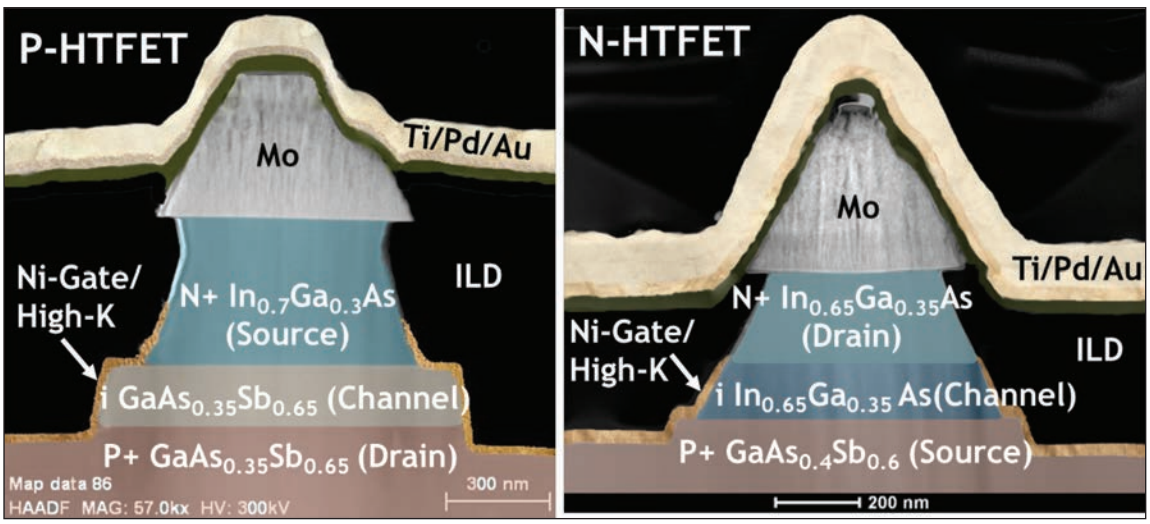


Figure 3. Cross-sectional transmission electron microscopy of *p*-type and *n*-type hetero-junction tunnel FETs.

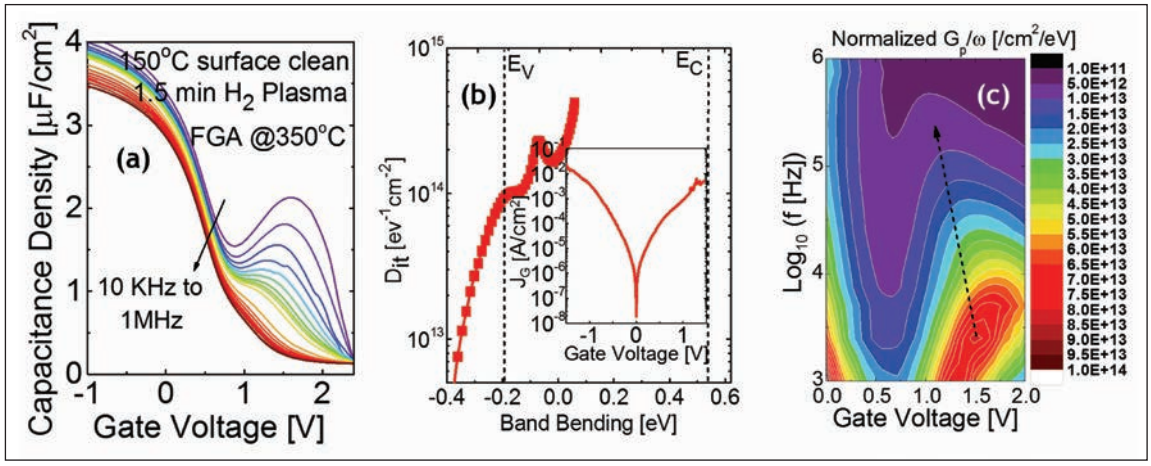


Figure 4. (a) Optimized capacitance-voltage characteristics of *p*-type $GaAs_{0.35}Sb_{0.65}$ MOSCAPs with a 3.5 nm HfO_2 gate dielectric using a H_2 plasma surface clean; (b) interface trap density extraction using Terman method. Gate leakage is shown in the inset; (c) Normalized parallel conductance plot with dotted line trace showing movement of the conductance peak maximum. Efficient Fermi level movement is obtained till mid-bandgap. Mid-gap interface trap density pins the Fermi level movement at low frequency.

FET is very steep, enabling this device to get far closer to the behaviour of an ideal switch than a MOSFET can.

With a tunnel FET, careful selection of the material system is needed to ensure that when this device is operated at a very low voltage, it outperforms a MOSFET. The natural choice of material for making a tunnel FET is silicon, due to its high-quality native oxide, and the opportunity to produce the device in a state-of-the-art foundry. Silicon's native oxide enables a high-quality interface with a low density of interface states – it is 10^{11} cm^{-2} eV^{-1} or less – and due to this, many groups have been able to report a device with very steep switching. However, these transistors suffer from a very low on-current, due to the large effective height of the tunnel barrier seen by carriers tunnelling from the source to the channel. This current is so low that it rules out the use of silicon tunnel FETs for logic applications.

Turning to other semiconductor materials is no guarantee of success, either. With all homo-junction tunnel FETs there is a uniform bandgap in the source, channel and drain regions. This means that the effective height of the barrier equals that of the bandgap. The on-current can be increased by reducing the bandgap, but the price to pay for this

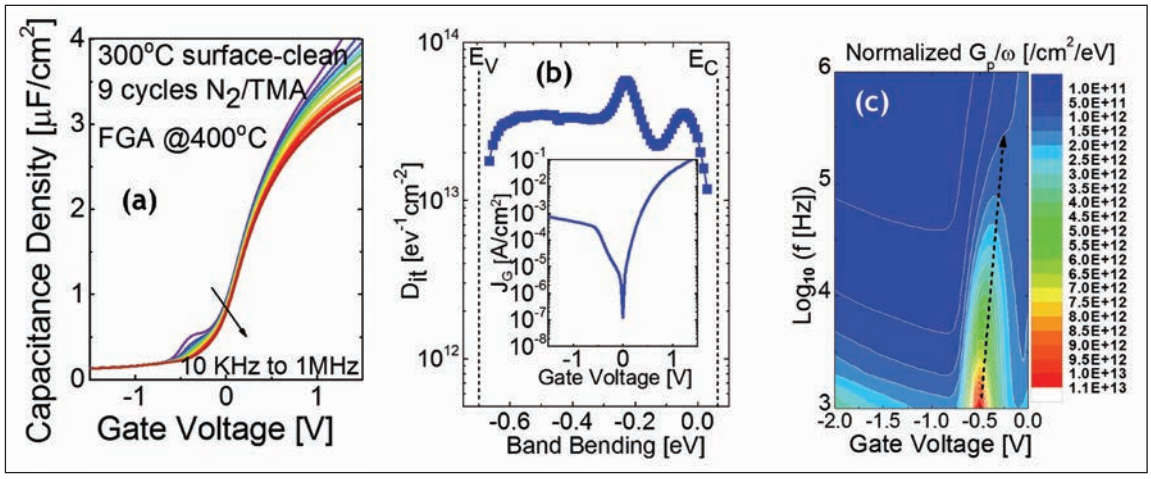


Figure 5. (a) Optimized capacitance-voltage characteristics of n-type $In_{0.53}Ga_{0.47}As$ MOSCAPs with 4nm ZrO_2 gate dielectric using N_2 plasma/TMA clean; (b) interface trap density extraction using the Terman method. Gate leakage for both the 3 nm and 4 nm ZrO_2 dielectrics is shown in the inset; (c) Normalized parallel conductance plots for 4 nm ZrO_2. Dotted line trace shows efficient Fermi level movement throughout the band gap.

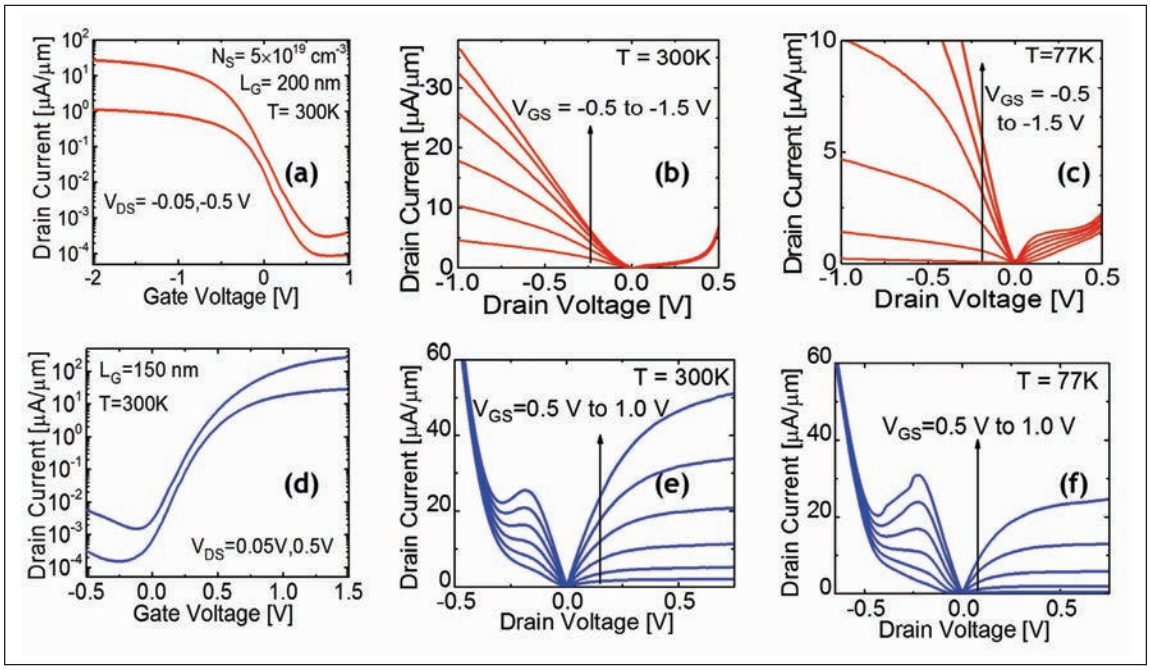


Figure 6. DC transfer and output characteristics of (a-c) a *p*-type hetero-junction tunnel FET and (d-f) an *n*-type hetero-junction tunnel FET. All measurements are at T=300K, except the additional T=77K data in (c) and (f). Negative differential resistance is visible in the *p*-type transistor's output characteristics at T=77K, due to the suppression of trap response. N_S denotes the source doping concentration in the device.

is the aggravation of parasitic leakage mechanisms – they include Shockley-Read-Hall generation-recombination within the reverse biased *p-i-n* diode, and band-to-band-tunnelling leakage on the drain side. Off-state leakage rockets as a result, degrading the current on-to-off ratio and leading to a highly diluted switching slope.

The solution is to switch from a homo-junction to a hetero-junction. With the latter form of FET it is possible to reduce the height of the tunnel barrier beside the source channel junction, while maintaining large bandgaps in every other region. Armed with this architecture, tunnel FETs can realise a high on-current and a steep switching slope.

Several material systems have been explored in the pursuit of a tunnel FET for next-generation logic. Success has not been easy. Devices made with the combination of silicon and SiGe, and germanium and GeSn, suffer from a significant trade-off between on-current and the switching slope. To implement energy-efficient complementary logic, this trade-off must be addressed while using a material system that is ideally capable of producing high-performance *p*-type and *n*-type devices. It is for that reason that we work with arsenide-antimonide hetero-junctions, because they offer a wide range of lattice-matched, compositionally tuneable effective tunnelling barrier heights that are suitable for making *n*- and *p*-type tunnel FETs.

One of the biggest challenges associated with making any class of III-V transistor for logic applications is that it is tricky to engineer a high-quality interface between the compound semiconductor channel and the gate dielectric. Native oxides of III-Vs are vastly inferior to those associated with silicon, and this prevents the creation of a pristine interface with the channel.

The problem stems from a III-V surface that is very reactive, with dangling bonds giving rise to a high density of interface states (they can hit 10^{14} cm^{-2} eV^{-1}). These imperfections severely limit the ability of the gate field to effectively modulate the source-channel tunnel barrier. In turn, this degrades the performance of the tunnel FET.

In the last year or so, however, research related to the gate stack has borne much fruit, with interface quality improving, thanks to high-quality surface treatments. These surface treatments consist of a combination of *ex-situ* wet-etch clean and *in-situ* pre-ALD H_2 or N_2 plasma based clean. They provide efficient removal of native oxide along with achieving high-quality surface passivation. Drawing on this success, we have formed InGaAs channel *n*FETs with excellent interfaces and a low density of interface traps, and *p*-type GaAsSb siblings with significantly improved interfaces.
Our three-dimensional vertical hetero-junction tunnel FET, which is grown by MBE at IQE's facility in Bethlehem, PA, features a metamorphic buffer. This

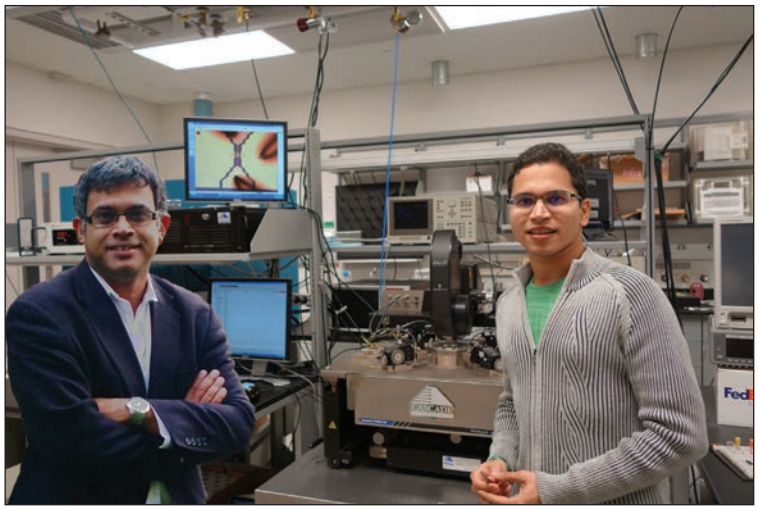
growth technology is used to form our epiwafers because it is capable of forming high-quality, abrupt hetero-junctions. This means that the design of the tunnel, which has been carefully chosen, can be accurately reproduced in the device, with MBE growth forming a defect-free tunnel-interface that maximizes the junction electric field without the need for abrupt doping profiles.

Fabrication of our hetero-junction tunnel FET begins with the creation of nano-pillars. They are formed with an electron-beam lithography patterning process, followed by plasma dry etching. Any damage to the sidewalls caused by dry etching is removed by wet etching to create a structure suitable for self-aligned gate metal deposition at the tunnelling junction.

Gate dielectrics are added by atomic layer deposition. Due to differences in the composition of the channels, *n*-type devices have ZrO_2 gate dielectrics, while *p*-type FETs have a HfO_2 gate. Gate-metal deposition follows, before the source contact for the *n*-type transistor is defined by electron-beam lithography. Benzo chlorobutane is used as an inter-layer dielectric, which is etched back before a drain contact is deposited on top. For the *p*-type device, the roles of the source and drain are exchanged.

After these steps, the entire structure is planarized by selective etching of benzo cholorobutane to create vias that enable the addition of contact pads on the top of the inter-layer dielectric. This structure, which has been scrutinised by transmission electron microscopy (see Figure 3), helps to reduce parasitic capacitance.

Forming a good interface between a high-κ dielectric and a III-V is particularly tricky for the antimonide-based FET, because movement of the surface Fermi level is restricted by the high density of interface traps near the middle of the bandgap. To overcome this challenge, we undertook a rigorous optimisation of the gate stack. The interface between a $GaAs_{0.35}Sb_{0.65}$ channel and a HfO_2 high-κ dielectric is highly reactive, due to dangling bonds, Sb-Sb bonds, antimonide oxides and anti-site defects. To remove the antimonide-oxides and passivate defect states we combine an *ex-situ* HCl clean with an *in-situ* H_2 plasma treatment.



Electrical engineers Suman Datta and Rahul Pandey in the Device Characterization Laboratory at the Millenium Science Complex, Penn State University.

The highest accumulation-capacitance density results from a 250°C plasma clean. The high temperature enables efficient desorption of native oxide, but at the expense of forming elemental antimony, which increases the interface trap density. By optimising the H_2 plasma surface clean temperature for a 3.5 nm-thick HfO_2 gate dielectric, we realise the thinnest capacitance equivalent thickness, of around 1.2 nm, with the lowest mid-gap density of interface traps (see Figure 4 (a) and (b)). This enables efficient movement of the Fermi level between the valence band and the mid-gap, but sluggish movement away from mid-gap (see Figure 4 (c), which illustrates this behaviour with normalized conductance maps).

The *n*-type FET faces similar challenges to its *p*-type

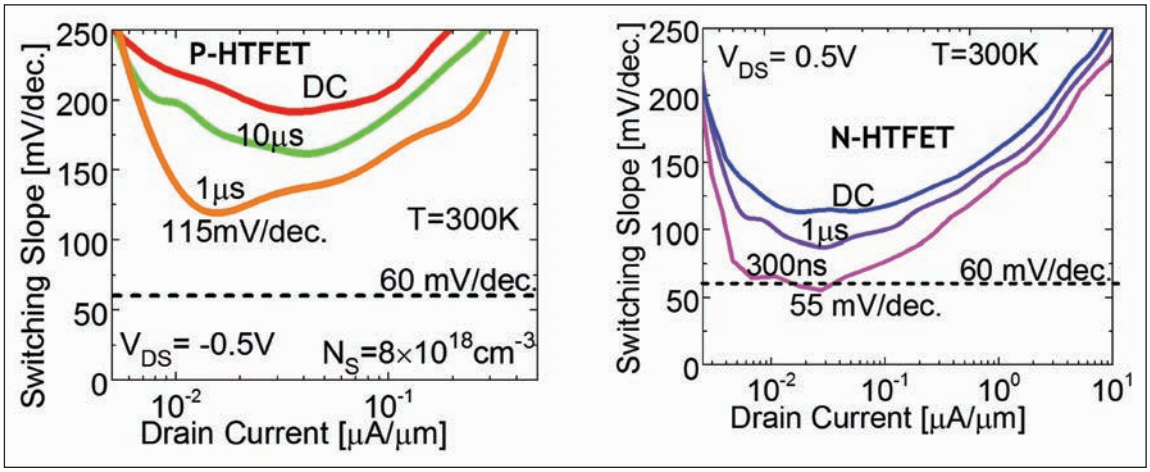


Figure 7. Fast I_{DS}-V_{GS} measurements reveal improved switching characteristics in *p*- and *n*-hetero-junction tunnel FETs. All measurements at 300K.

	PTFET				NTFET			
	R. Gandhi et al., EDL, Nov. 2011	L. Knoll et al., EDL, June 2013	This work, R. Pandey et al., VLSI 2015		G. Dewey et al., IEDM 2011	M. Noguchi et al., IEDM 2013	This work, R. Pandey et al., VLSI 2015	
Structure	SiNW GAA	SiNW	III-V N_s=5X10^{19}cm^{-3}	III-V [Fast I-V] N_s=8X10^{18}cm^{-3}	III-V	III-V	III-V	III-V [Fast IV]
V_{DS} [V]	-0.6	-0.5	-0.5	-0.5	0.3	0.3	0.5	0.5
I_{ON} [μA/μm]	1.8	10	14	10	12	6	245	275
I_{MIN} [μA/μm]	1.2X10^{-6}	2.0X10^{-6}	3.0X10^{-4}	2X10^{-3}	1.0X10^{-4}	2.0X10^{-6}	1.4X10^{-3}	1.4X10^{-3}
I_{ON}/I_{MIN}	1.4X10^{6}	5.0X10^{6}	4.7X10^{4}	5X10^{3}	1.2X10^{5}	3.0X10^{6}	1.8X10^{5}	2.0X10^{5}
SS_{Min} [mV/dec.]	30	90	171	115	58	64	102	55
EOT [nm]	4.5	0.7	0.8	0.8	1.1	1.4	0.7	0.7
Lg [nm]	140	200	200	200	100	-	150	150

Figure 8. Benchmark of silicon and III-V TFET. V_{ON} (V_{MIN}) corresponds to the gate voltage at I_{ON} (I_{MIN}). $|V_{ON}|$ is limited to 1.5 V from $|V_{MIN}|$.

sibling, with the interface between a ZrO_2 gate dielectric and an $In_{0.65}Ga_{0.35}As$ channel marked by the presence of dangling bonds, As-As bonds, arsenide-oxides and anti-site defects. To eradicate arsenide-oxides and passivate the interface, we combine an *ex-situ* buffered oxide etch clean with an *in-situ* N_2 plasma/TMA [trimethylaluminum] cyclic treatment.

Surfaces can be damaged with over exposure to the plasma, so we limited the number of cycles to nine. Taking this approach and using a 4 nm-thick ZrO_2 high-κ dielectric, we produce devices with a capacitance equivalent thickness of 1.1 nm and a low mid-gap density of interface traps (see Figures 5 (a) and (b)). Measurements of the conductance peak indicate efficient Fermi-level movement with gate voltage (see Figure 5 (c)).

We have measured the room-temperature transfer and output characteristics of our *n*-type and *p*-type hetero-junction tunnel FETs (see Figure 6). The *p*-type devices deliver an on-current of 30 μA/μm and produce an on-off current ratio of 10^5. When these transistors are cooled by liquid nitrogen, they exhibit negative differential resistance and saturation, due to the suppression of a response from the mid-gap interface traps. With *n*-type devices, the on-current is 275 μA/ μm and the ratio of on-to-off current is 3 x 10^5.

One major downside of the slow response time associated with the mid-gap interface traps is that it causes the DC switching slope for both types of FET to exceed 60 mV/decade at room temperature. However, it is possible to suppress the impact of mid-gap interface traps on the sub-threshold slope by sweeping the gate voltage at a rate that is faster than the trap response time.

We took this approach, evaluating the switching slope with an input gate voltage ramp rise time that varied from 10 μs to 300 ns. Using these conditions, switching characteristics improved, with room-temperature values for the *n*-type and *p*-type FETs of 55 mV/decade and 115 mV/decade, respectively. These switching slopes and high currents highlight the importance of employing high-quality, scaled gate dielectrics and tunnel barriers in the arsenide-antimonide system.

To put our results in context, we have benchmarked our devices against published results (see Figure 8). This comparison includes hetero-junction tunnel FETs made with silicon/SOI/SiGe materials that deliver steep switching, but not in conjunction with a high current. Our antimonide-based *n*-type transistors deliver superior performance, and when partnered with our *p*-type arsenide-channel devices, demonstrate the potential of III-V complimentary tunnel FET logic.

We will now build on our work. We have already accomplished the first demonstration of an all III-V material system based on complimentary hetero-junction FETs that combines a low operating voltage with a record on-current and switching performance. Our goals for the future include an expansion of the steep switching range over multiple decades of drain current without compromising the on-current. We know that cutting contributions to parasitic leakage and engineering high-quality interfaces hold the key to realising high-performance hetero-junction tunnel FETs with a steep switching slope that can serve energy-efficient logic.

Further reading

R. Pandey *et. al.* "Demonstration of *p*-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and *n*-type $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic", in 2015 Symposium on VLSI Technology, T206-T207, 16-18 June 2015.
D. Mohata *et. al.* IEEE Electron Device Letters **33** 1568 (2012)
V. Chobpattana *et. al.* Applied Physics Letters **104** 182912 (2014)
M. Barth *et. al.* Applied Physics Letters **105** 222103 (2014)
R. Bijesh *et. al.* IEDM 28.2.1-28.2.4 (2013)

Making multi-junction cells with room temperature bonding

Researchers unite a pair of double-junction cells with a commercial wafer-bonding tool

ROOM-TEMPERATURE wafer bonding has been used to fabricate, for the first time, a four-junction cell with an efficiency in excess of 40 percent, according to a team from China.

The researchers believe that wafer bonding is an attractive option for making solar cells with four or more junctions because it provides an easy route to accommodate differences in the lattice constants of the materials used in each of the cells.

To ensure a high mechanical strength and a low electrical resistance, traditional wafer bonding techniques employ elevated temperatures and lengthy adhesion times – both of which degrade device performance. Differences between the thermal expansion coefficients of the wafers cause them to bend and give rise to voids; and high-temperature annealing can drive diffusion of dopants from the heavily doped tunnel junctions that are inserted between the sub-cells.

The Chinese team, which is led by researchers from Suzhou Institute of Nano-tech and Nano-Bionics, eliminates these issues with a room-temperature wafer-bonding technique. InP-based wafers featuring InGaAs and InGaAsP cells are united to GaAs and GaInP cells on GaAs-based wafers with a Mitsubishi Heavy Industries wafer-bonding machine. It is equipped with an argon ion gun and a high-vacuum chamber.

Low-energy argon ions are directed at both wafers, activating surfaces and creating dangling bonds. Bringing the two surfaces together with a force of 5000 N creates a four-junction structure.

The researchers avoid contaminating the bonding surface by carrying out the process in a high-vacuum chamber. This precaution is said to be very important, because particles can cause large voids and defects that impair cell performance.

MBE is used to make both double-junction epiwafers. Corresponding author Shulong Lu explains that this growth technique is well suited to making tunnel junctions with high doping – but MOCVD has the upper hand for the growth of quaternary InGaAsP material.

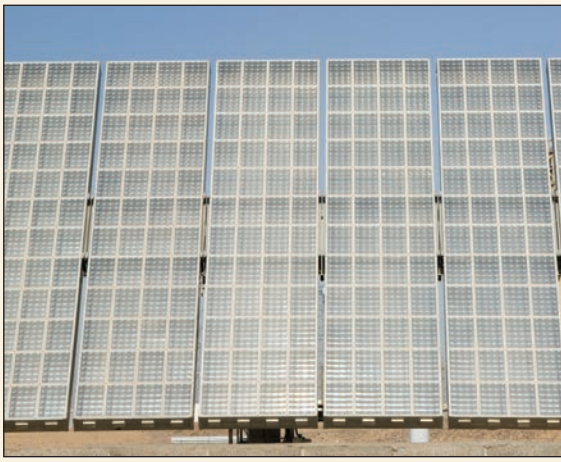
Efforts by the Chinese team included a simulation of solar cell efficiency that considered three loss mechanisms: radiative loss, thermal loss and transmission loss. Calculations suggest that if the bandgap of the two highest-energy cells were fixed to 1.91 eV for the InGaP cell and 1.42 eV for the GaAs cell, it should be possible to hit an overall efficiency of 45.4 percent at one sun, if the other two cells had bandgaps of 1.01 eV and 0.56 eV.

However, the team reasoned that it is unrealistic to form lattice-matched materials with these bandgaps. Instead, they have used an InP substrate as the basis for combining two lattice-matched cells: an InGaAsP cell with an energy of 1.07 eV, and an InGaAs cell with an energy of 0.74 eV. At one sun concentration, the highest possible efficiency with this combination is 39.0 percent.

After the epiwafers were united, researchers scrutinised the quality of the bonded interface with cross-sectional transmission electron microscopy. They didn't find any voids, or any threading dislocations or planar defects, which are typically seen in material formed during lattice-mismatched epitaxial growth.

Devices were made using a AuGe/Ni/Au front contact, a Au/Zn/Au/Cr/Au back contact, and a Ta_2O_5/TiO_2 anti-reflection coating. Measurements of short-circuit-current as a function of voltage revealed an energy conversion efficiency of 31.6 percent at 1 sun. Increasing the concentration to 230 suns enabled a hike in conversion efficiency to 42 percent.

The team is hopeful that they can break the record for multi-junction solar cell conversion efficiency, which stands at 46 percent, by optimising the structure. This might involve fine-tuning the thickness of some layers – the record-breaking device from Soitec, CEA-Leti, and Fraunhofer ISE, had thickness for the InGaP and GaAs cells of 650 nm and 1400nm, while values of just 480 mn and 800 nm were employed in the solar cell made by the Chinese team.



Room-temperature wafer bonding could aid the production of higher efficiency cells that increase the competitiveness of concentrating photovoltaic technology.

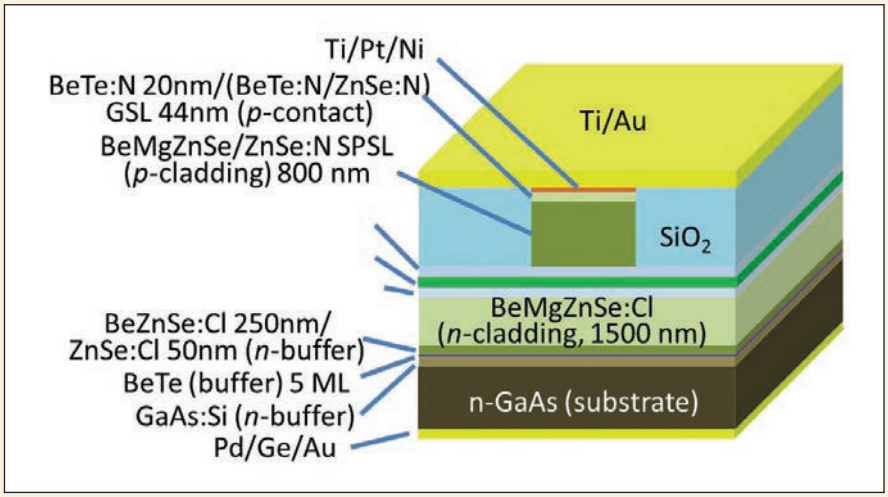
Improving the quality of the bottom cell could also help to increase overall solar cell efficiency. The open circuit voltage of the team's bottom cell is just 0.54 eV, 0.13 eV below that in the record-breaking device. It is speculated that the lower growth temperature of MBE, compared with MOCVD, mighty lead to defect states and deep centres.

Lu says that the team is now optimising the device through efforts associated with material growth and photocurrent matching.

P. Dai *et. al.* Appl. Phys. Express **9** 016501 (2016)

Trimming threshold currents of yellow lasers

A ridge waveguide reduces the threshold current of BeZnCdSe-based yellow lasers



A ridge-waveguide enables fabrication milliWatt, continuous-wave yellow lasers.

A PAIR OF Japanese researchers has reduced the threshold current in yellow-emitting, BeZnCdSe-based lasers by introducing a ridge waveguide structure. This refinement will aid commercialisation of these lasers, which can be used for medical cures.

"For retina treatment, yellow lasers such as argon-krypton gas lasers, and lasers based on nonlinear wavelength conversion, have been used," explains corresponding author Ryoichi Akimoto from the National Institute of Advanced Industrial Science and Technology (AIST). "Advantageous features of laser diodes – low cost, low power consumption and easy operation – are also applicable to these emerging application fields."

However, to target these applications, output powers must increase. The lasers made by Akimoto and his co-worker Jijun Feng, who is affiliated to AIST and the University of Shanghai for Science and Technology, emit a few milliwatts. Meanwhile, applications demand powers ranging from 100 mW to 1 W. Fabricating yellow laser diodes emitting in the 560 nm to 590 nm range is very challenging. This region is tough to reach with nitride lasers; inaccessible with those based on InGaP; and the most promising material system is based on ZnSe, which can be mixed with beryllium to increase laser lifetime.

Adding cadmium propels emission to longer wavelengths, but growth of ZnCdSe quantum wells on GaAs substrates leads to significant strain in the material.

Switching to alternative substrates, such as ZnTe or InP, has enabled lasing at longer wavelengths. However, photopumping has been needed to realise room-temperature lasing, with electrically pumped lasing restricted to low temperatures.

In 2012, a team that included Akimoto announced that a related, promising material for making yellow lasers is BeZnCdSe, which has a small lattice mismatch with GaAs. During the last few years, gain-guided green lasers with a quantum well made from this quaternary have produced outputs in excess of 50 mW, and variants with a ridge-waveguide have operated with a threshold current below 10 mA.

The ridge-waveguide holds the key to the low threshold current of the recently reported yellow lasers of Feng and Akimoto. One of these emits at 567 nm and has a threshold current density of 0.51 kA cm^{-2}, and its 563 nm sibling has a threshold current density of 0.82 kA cm^{-2}.

The researchers made their lasers using MBE, with a 500 nm-thick *n*-type buffer layer deposited in a chamber designed for III-V growth, prior to transfer to a second chamber designed for II-VI growth. There, a BeZnCdSe single-quantum well was sandwiched between BeZnSe optical guiding layers, which were surrounded by a BeMgZnSe *n*-type cladding layer and a *p*-type cladding region made from a short-period superlattice, formed from the pairing of BeMgZnSe and ZnSe:N.

Electron-beam lithography defined the mesa width of the ridge waveguide lasers formed from the epiwafers. A metal deposition and lift-off process added a Ti/Pt/Ni stack, which act a mask to subsequent dry etching and enables an ohmic contact to the *p*-type layer. Inductively coupled plasma etching to a depth of 900 nm created waveguides that were subsequently buried with 2 μm of SiO_2, deposited by plasma-enhanced CVD. Following chemical-mechanical polishing to form a flat surface, etching removed the remaining SiO_2 to expose a metal mask. Electrodes were added to this using photolithography.

Cleaving created a range of ridge waveguide lasers with various cavity lengths. A facet reflectivity of 90 percent resulted from the addition of a dielectric coating made from four pairs of SiO_2 and ZrO_2.

From the wafer producing 567 nm lasers, the best results were obtained with a device with a 7 μm-wide, 300 μm-long cavity that had a threshold current of 10.8 mA and a threshold voltage of 8.4 V. For the 563 nm laser, the best performance came from a chip with a 7 μm-wide, 300 μm-long cavity. In this case, threshold current and voltage were 7.4 mA and 8.48 V.

Goals for the duo are to improve output power and reliability. According to Akimoto, commercial devices require an output of 100 mW or more and a reliability in excess of 5000 hours.

J. Feng *et. al.* Appl. Phys. Express **9** 012101 (2016)

Carrier lifetimes uncover multiple causes of droop

Analysis of carrier lifetimes indicates that carrier delocalisation is behind the onset of droop, with leakage dominating at higher current densities

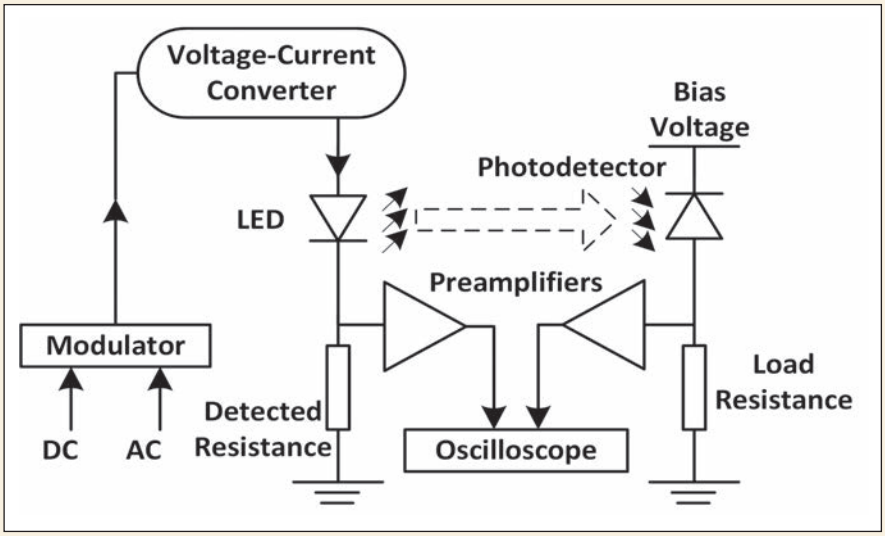
BACKERS of alternatives to Auger as the primary cause of LED droop will be buoyed by recent work from a team from Tsinghua University, China. Using differential carrier lifetime analysis, these researchers concluded that carrier delocalisation is behind the onset of droop, with carrier leakage taking over at higher current densities.

It is possible to differentiate between Auger recombination and carrier leakage with the team's approach, because these two processes have different impacts on carrier lifetime. Auger recombination enhances the recombination rate, leading to a reduction in carrier lifetime, while electron leakage has no impact on carrier lifetime – it just reduces the carrier density in the active area.

One of the most important aspects of this work is the optimisation of the experimental set-up, which allows carrier lifetime to be determined with great accuracy. Armed with this information, the team fitted curves, as a function of current, of both external quantum efficiency and carrier lifetime. Then, through the application of the well-known *ABC* model, they obtained insights into contributions to droop.

Using differential carrier lifetime analysis to try and fathom the origin of droop is not a new idea. In 2013, a group at Aalto University, Finland, led by Markku Sopanen, adopted this approach and obtained lifetimes of the order of microseconds. This is an order of magnitude or so higher than that determined by the Chinese team, who believe the discrepancy might be due to the parasitic capacitance of the high-speed detector used by the Finish group.

A pair of researchers from Philips Lumileds has also turned to differential carrier lifetime analysis to study droop, determining carrier concentrations from carrier lifetimes, and assuming 100 percent injecting efficiency.



To eliminate a shift in phase caused by capacitances and resistances, a load resistance is connected in series with the optical detector. The resulting signal is too low for an adequate signal-to-noise ratio for the oscilloscope, so a pre-amplifier is inserted in this path – and also in that of the electrical signal, to eliminate any phase delay associated with the use of a pre-amplifier.

Contributing author Lia Wang from Tsinghua University argues that this approach is flawed, because it gives values for the *A*, *B* and *C* coefficients that are wide of the mark. "According to these coefficients, one cannot calculate the efficiency and carrier lifetimes correctly."

Wang and co-workers carried out their measurements on commercialised blue and green LEDs. Modulating an AC signal on a DC injection current and comparing the phase difference between the electrical and optical output of the LED gave carrier lifetimes for the blue and green LEDs at 2 mA of 103.2 ns and 198.7 ns, respectively. Cranked up to 50 mA, carrier lifetimes fell to 37.2 ns and 50.8 ns, respectively.

To rule out Auger as the major cause of droop, the team made the assumption that *only* Auger recombination contributes to droop, and then they tried to fit curves of the reciprocal of the carrier lifetime as a function of carrier density. It proved impossible to fit this curve well, and also that of the external quantum efficiency as a function of injection current. Accounting for droop with just carrier leakage also failed to produce good curve fitting, and a combination of this and Auger recombination fared even worse. So the team introduced another loss mechanism – carrier delocalisation – that attributes droop to an increase in carriers reaching non-radiative centres at higher drive currents. Combining terms for carrier leakage and carrier delocalisation led to good curve fitting.

"What we plan to do next is to design a novel active region to decrease carrier concentration," says Wang, "and to design a superlattice electron-blocking layer to not only enhance electron blocking, but also improve hole tunnelling injection."

X. Meng et. al. Appl. Phys. Lett. **108** 013501 (2016)

CORPORATE PARTNERS DIRECTORY

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

Non Contact Measurements
Resistance, Resistivity
Wafer Thickness
KITEC microelectronic technologie
Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

Temescal
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

EPIGAN
Email: info@epigan.com
www.epigan.com

LAYTEC Knowledge is key
Tel. No.: +49 (0) 30 89 00 55 0
Fax No: +49 (0) 30 89 00 55 180
e-mail: info@laytec.de
website: www.laytec.de

Lake Shore CRYOTRONICS ADVANCING SCIENCE
Tel: +1 614 891 2244
Fax: +1 614 818 1600
Email: info@lakeshore.com
www.lakeshore.com

HIDEN ANALYTICAL
Tel: +44 [0] 1925 445225
Fax: +44 [0] 1925 416518
Email: info@hiden.co.uk
www.hidenanalytical.com

OXFORD INSTRUMENTS The Business of Science®
Tel: +44 (0)1934 837000
Fax: +44 (0)1934 837001
Email: plasma.technology@oxinst.com
www.oxford-instruments.com

WATLOW®
www.watlow.com

Meister Abrasives abrasives
Tel: +41 52 304 22 00
Fax:+41 52 304 22 12
Email: info@meister-abrasives.ch
www.meister-abrasives.ch

化合物半导体 COMPOUND SEMICONDUCTOR · CHINA
Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

TYSiC 1st SiC-epi Foundry in China
Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

III/V-Reclaim GaAs InP
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.de

GATAN
Tel: +1 925 224 7355
Email: info@gatan.com
www.gatan.com

UMC UNITED MINERAL & CHEMICAL CORP.
MBE Specialists
Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

kSA k-Space Associates, Inc. Thin-Film Characterization
Tel: +1 734-426-7977
e-mail: requestinfo@k-space.com
www.k-space.com

BACH·RC
Tel: +49 33398 696592
Fax: +49 33398 696594
Email: jp@bachrc.de
www.bachrc.de

NANO-MASTER
Cleaning • Deposition • Etching
Tel: +1 512-385-4552
Fax: +1 512-385-4900
Email: r.andrade@nanomaster.com
www.nanomaster.com

evatec process systems
Tel: + 41 81 720 1080
Fax: 41 81 720 1161
www.evatecnet.com

Vistec Electron Beam
Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

Fil-Tech, Inc.
Savings on Quality Vacuum and Coating Supplies
Tel: +1 617-227-1133
Fax: +1 617-742-0686
Email: paula@filtech.com
www.filtech.com

BRUKER
Tel: +49 721 50997-0
Fax: +49 721 50997-5654
www.bruker.com

Instrument Systems light measurement
Tel: +49 (089) 45 49 43 - 0
Fax: +49 (089) 45 49 43 - 11
Email: info@instrumentsystems.com
www.instrumentsystems.com

Veeco
Tel: 516-677-0200-1222
Fax: 516-714-1231
Email: jpina@veeco.com
www.veeco.com

Pick your size.

The Temescal UEFC-4900—ultimate lift-off metallization performance like the UEFC-5700, but optimized for smaller wafers and smaller production volumes.

Temescal
UEFC–4900

It's the elephant in the room. With our Auratus™ deposition enhancement methodology and the UEFC-5700, we brought you huge metallization process improvements including near perfect uniformity; but UEFC-5700 is a high-volume production tool. Now we've packed this performance into a mid-sized system, the UEFC-4900, because sometimes the elephant is just too big.

Harmonize your process to the vapor cloud and experience the huge performance benefits, even if you run smaller wafers and smaller production volumes.

A Temescal system can bring near perfect uniformity to your lift-off metallization coating process. To find out more, visit **www.temescal.net/auratus-elephant** or call **+1-925-371-4170**.

FerroTec