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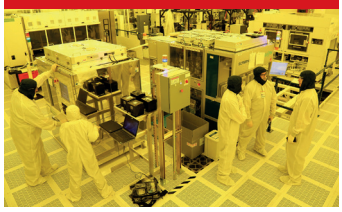
Global sales of GaAs devices start to plateau

Shining in space by vertical integration

The third dimension: The logical step for III-Vs

CS shares enjoy a tremendous 12 months

Processing SiC in a dedicated 150 mm line



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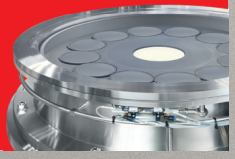

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Viewpoint

By Dr Richard Stevenson, Editor

Going vertical

WHEN I THINK OF vertical integration I tend to think of Infinera, the maker of InP photonic integrated circuits that are incorporated into its systems that are deployed in optical networks. It would appear that this in-house strategy has served the company well: it has formed a highly successful multi-million dollar business with devices that are notoriously difficult to make with high yields.

Obviously, Infinera isn't the only vertically integrated III-V chipmaker. Another example is Cree, a pioneer of LEDs that is now a leading force in solid-state lighting; and SolAero, a company that has been carved out of Emcore and makes solar cells and satellite panels.

The latter entity has been pursuing a vertically integrated strategy for many years. Emcore's cells for satellites first hit the market in 1997, and four years later it acquired TecStar, a maker of solar panels.

For more than a decade, Emcore continued in this vein. However, the break up of the business units in late 2014, with ownership of the solar arm taken over by Veritas Capital, has spawned a flurry of activity.

The strengthening of solar capabilities has come through a combination of acquisitions and investment. In 2015 SolAero bought Alliance Spacesystems, equipping the company with lightweight frame technology for satellites; and in 2016, it acquired Vanguard Space Technologies, a move that strengthened expertise in engineering in space (see the interview of p.32 of this issue for details).

In May 2016 SolAero won a contract to supply solar panels to One Web, a company with ambitious plans that aims to bring the opportunity for connectivity to everyone across the globe via a vast array of satellites. To fulfil this mission, it plans to launch three satellites per day.

To keep pace, SolAero is investing $10 million to replicate its know-how from its other two sites to its headquarters. By taking this step, it will streamline operations by avoiding having to ship parts around the country while completing its orders.

This move gives the company a unique capability, which should enable it to improve margins in an industry that is experiencing very tough conditions.

Rivals that just produce cells these days will be envious of SolAero's position. With the collapse of the fledgling CPV market, it's now precarious to just be making devices – and far better to be enjoying the benefits of vertical integration.

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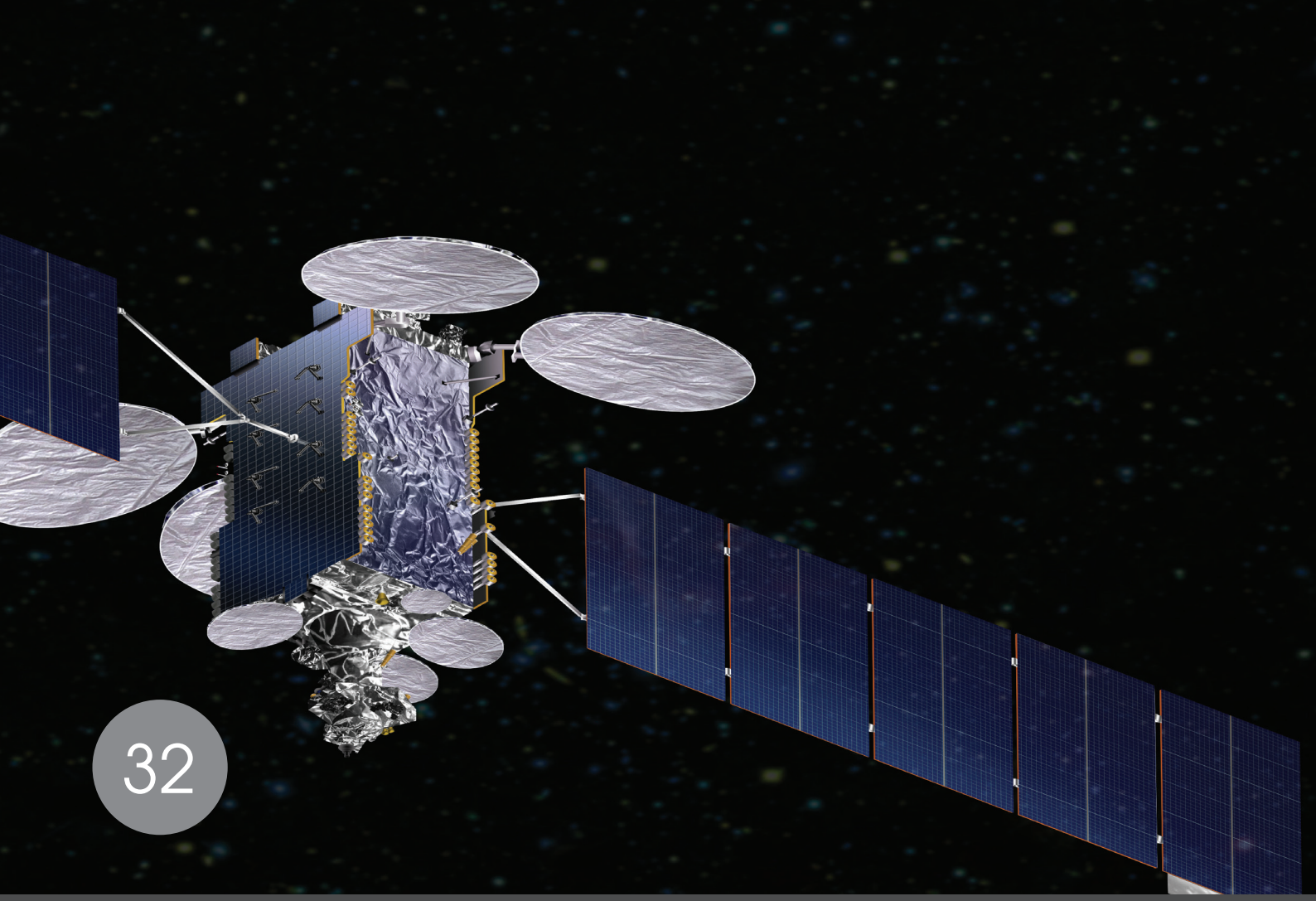
COVER STORY

Perfecting 200 mm processing tools

As the demand for MEMS, sensors and mobility expands, heterogeneous devices on 200mm substrates will become more common to address that increased demand.



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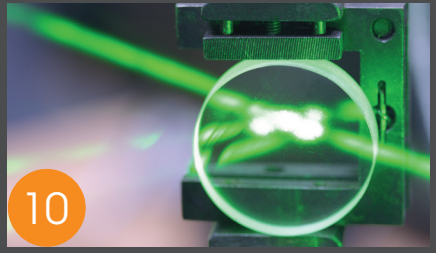

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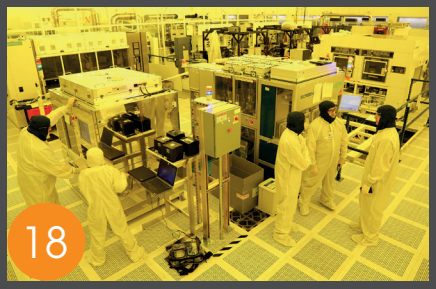

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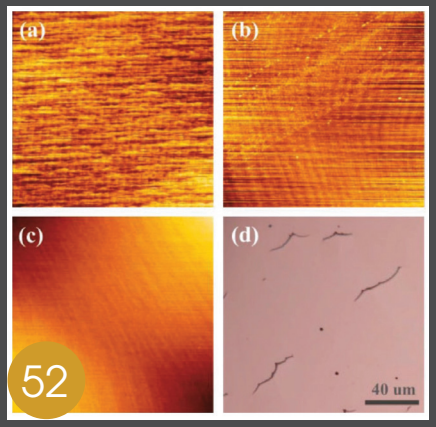


X-Fab and Exagan make first 200 mm GaN-on-silicon devices

X-FAB SILICON FOUNDRIES and Exagan, a GaN start-up, have demonstrated mass-production capability to make highly efficient high-voltage power devices on 200 mm GaN-on-silicon wafers using X-Fab's standard CMOS production facility in Dresden, Germany.

This accomplishment is the result of a joint development agreement launched in 2015, enabling cost/performance advantages that could not be achieved with smaller wafers.

Exagan and X-Fab have successfully resolved many of the challenges related to material stress, defectivity and process integration while using standard fabrication equipment and process recipes.

Combined with the use of 200 mm wafers, this will significantly lower the cost of mass producing GaN-on-silicon devices. By enabling greater power integration than silicon ICs, GaN devices can improve the efficiency and reduce the cost of electrical converters, which will accelerate their adoption in applications including electrical vehicle charging stations, servers, automobiles and industrial systems.

The new GaN-on-silicon devices have been built using substrates fabricated at Exagan's 200 mm epi-manufacturing facility in Grenoble, France. These epi-wafers meet the physical and electrical specifications to produce Exagan's 650 V G-FET devices as well as the tight requirements for compatibility with CMOS manufacturing lines.

The industry's previous work with GaN had been limited to 100 mm and 15-mm wafers due to the challenges of layering GaN films on silicon substrates. Exagan's G-Stack technology enables GaN-on-silicon devices to be manufactured more cost effectively on 200 mm substrates by depositing a unique stack of GaN and strain-management layers that relieves the stress between GaN and silicon layers. The resulting devices have been shown to exhibit high breakdown voltage, low vertical leakage and high-temperature operation.

"This is a major milestone in our company's development as we accelerate product development and qualification," said Frédéric Dupont, president and CEO of Exagan. "It demonstrates the combined strengths of our epi material, X-Fab's wafer fab process and our device design capabilities. It also confirms the success of our vertically integrated fab-lite model, with expertise from materials to devices and applications. It's perfect timing to establish GaN technology and products on the most competitive 200 mm platform just as GaN power products are getting broad traction in IT server, consumer electronics and automotive markets."

WIN Semiconductors completes second phase of fab expansion

WIN SEMICONDUCTORS has completed the second phase of expansion of its newest wafer fab, Fab C. It says this will boost its GaAs wafer manufacturing capacity by over 20 percent. According to the company, this operation is now fitted with state-of-the-art clean rooms, efficient process lines and advanced equipment for GaAs MMIC production, epitaxial growth of compound semiconductors, as well as fabrication and test of optical devices. Serving customers in mobile PA, WiFi, wireless infrastructure and optical markets, WINSemiconductors provides a broad portfolio of HBT, pHEMT, integrated BiHEMT technology solutions and optical devices. WIN Semiconductors' manufacturing services can support applications from 50 MHz to 150 GHz and through light-wave.

"In response to increasing demand across all market segments, we continue to add manufacturing capacity at our third wafer fab located in Guishan,Toayuan City, Taiwan. Known as Fab C, the facility now supports mass production of a wide range of compound semiconductor technologies. When fully built out, the 706,000ft^2 facility will more than double our capacity", said Kyle Chen, senior VP and COO of WIN Semiconductors.

Advantech releases second generation GaN Ka-band BUCs

Advantech Wireless has released its second generation of 100 W to 125 W K_a-Band Block Upconverter (BUC), based on GaN technology.

The new GaN-based BUCs are designed for K_a-Band LEO and GEO satellite up-link applications. The GaN-based SSPB-3010Ka series are integrated units, complete with power supply, phase-locked oscillator, mixer, filter and proprietary cooling mechanism.

Intended for outdoor operation, the second generation GaN-based systems are the most advanced GaN based Ka-Band units in the market providing higher power and linearity, higher reliability and very low spectrum regrowth.

"GaN technology allows us to reach power levels that were not possible before, and to serve customers that are looking for solutions in fast growing market segments," said Cristi Damian, VP business development at Advantech Wireless.

"Advantech Wireless is a pioneer in Ka-Band solid state technology, with products in the field since 2005. The new 100/125W K_a-band SSPAs take advantage of advanced GaN technology to deliver unmatched performance and reliability."

Mitsubishi, Nokia Bell Labs and UC San Diego develop ultra-fast GaN envelope-tracking amplifier

MITSUBISHI ELECTRIC, Nokia Bell Labs and the Center for Wireless Communications at UC San Diego have developed an ultra-fast GaN envelope-tracking power amplifier (PA) for next next-generation wireless base stations.

Believed to be a world first, the PA supports a modulation bandwidth up to 80MHz, which is four times wider than the signals reportedly used in other envelope-tracking power amplifiers. Technical details will be presented during the IEEE MTT International Microwave Symposium (IMS) 2017, which will be held in Honolulu, Hawaii, USA from June 4 to 9.

To help meet the demand for increasing wireless capacity, mobile technologies are shifting to next-generation systems that use complex modulated signals with large peak-to-average power ratio (PAPR) and extra-wide modulation bandwidth. This will require power amplifiers to operate most of the time at backed-off power levels that are well below their saturation levels.

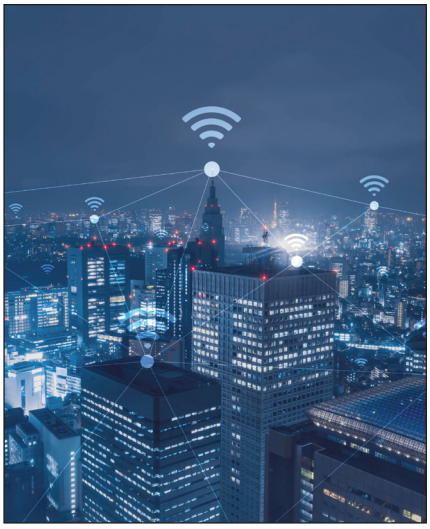
Generally, power amplifiers achieve high efficiency near their saturation power levels, but significantly degraded efficiency at backed off levels, as in the case of 4G LTE* signals (>6dB PAPR).

Envelope-tracking power amplifiers have been studied extensively as a means to enhance power-amplifier efficiency, but so far the supply-modulator circuit has been the bottleneck limiting modulation bandwidth for advanced wireless communications, such as LTE-Advanced.

The newly developed ultra-fast GaN envelope-tracking power amplifier achieves state-of-art performance thanks in part to Mitsubishi Electric's high-frequency GaN transistor technology and design innovation for the GaN supply-modulator circuit.

Using Nokia Bell Labs' real-time digital pre-distortion (DPD) system, the power amplifier has demonstrated efficient operation even with 80MHz modulated LTE signals, the world's widest modulation bandwidth for this purpose as of May 19, 2017. The new GaN envelope-tracking power amplifier uses Mitsubishi Electric high frequency GaN in supply-modulation circuits, which enable high-speed operation. The result is highly efficient amplification of complex signals with modulation bandwidth up to 80MHz.

The technology achieves a world-class drain efficiency of 41.6 percent in such wide-bandwidth operation, thereby reducing base-station energy



consumption while increasing wireless communication speed and capacity. Further, the real-time DPD system enables pre-distortion for wideband signals to correct the output signal from the power amplifier, resulting in an adjacent channel leakage ratio (ACLR) of -45dBc for LTE 80MHz signals, which satisfies the wireless communication standards.

In view of its leading system-level performance, the new envelope-tracking power amplifier is believed to be a highly promising candidate for next-generation wireless base stations.

IEEE awards George Craford for contributions to LED lighting

LUMILEDS has announced that George Craford, Lumileds Solid State Lighting Fellow, was selected for the IEEE Edison Medal for 'a lifetime of pioneering contributions to the development and commercialisation of visible LED materials and devices'.

Craford will be presented with the medal at the IEEE Honours Ceremony in San Francisco on May 25, 2017, during the IEEE Vision, Innovations, and Challenges (IEEE VIC) Summit.

Craford's career spans from the early days when LEDs were first developed to delivery of high brightness LEDs suitable for commercial use in a variety of applications, including LED bulbs. He is best known for his invention of the yellow LED in 1972. Craford then led the development of increasingly brighter red, orange and amber LEDs.

In 1979, Craford began work at Hewlett-Packard, where his team pioneered the development of AlInGaP LEDs using metalorganic chemical vapor deposition (MOCVD). MOCVD was then a relatively expensive lower volume process and had not been used for the high volume commercial production of LEDs. AlInGaP LEDs increased the performance of red and yellow LEDs by more than ten times. Craford's team continued to achieve technology breakthroughs in AlInGaP LEDs, eventually reaching 100 lm/W. "Not only was George responsible for substantial breakthroughs in technology, but with his team, ensured that the technology could be reliably and cost effectively manufactured," said Mark Karol, 2017 IEEE Awards Board Chair.

One can see the impact of Craford's early work in the colour LEDs now ubiquitous in traffic signals, emergency and automotive lighting. Craford's later work focused on making white LED light cost effective for retail, office, architectural, outdoor and industrial lighting markets. In the early 2000s, his team's work enabled commercialisation of the first high power LEDs in the 10-20 lumen range. Such LEDs contributed to the creation of the

first LED bulbs to meet the high efficiency and long lifecycle requirements to win the US Department of Energy's 'L Prize' for a 60W-equivalent LED bulb.

"George has terrific instinct for what will work, but at the same time he's got that practical engineering side that drives a solution until it produces the best results," said Jy Bhardwaj,CTO of Lumileds.

Today, Craford is Lumileds Solid State Lighting Fellow at Lumileds. He is an IEEE Life Fellow and a member of the National Academy of Engineering. He has received numerous awards including the 2002 National Medal of Technology and the 2015 US National Academy of Engineering Charles Stark Draper Prize. He has also been awarded the International SSL Alliance Global Solid State Lighting Development Award, the Strategies in Light LED Pioneer Award, the University of Illinois Alumni Distinguished Service Award, the IEEE Morris N. Liebmann Award, the IEEE Third Millennium Medal, the Optical Society of America Nick Holonyak Jr. Award, the International Symposium on Compound Semiconductors Welker Award, the Materials Research Society MRS medal, the Electrochemical Society Electronic Division Award and the Economist Innovation Award.

Osram shows third generation plant growing LED

AT this year's Lightfair in Philadelphia (USA), Osram Opto Semiconductors showed a new high power LED prototype designed to promote plant growth.

The Oslon Square Hyper Red is a third-generation 2 W LED designed to cut the cost of plant lighting systems by featuring improved emission characteristics, higher optical output, and better corrosion resistance.

Plants need water and light to grow. By using LEDs with different wavelengths, commercial growers are now able to control each individual stage of plant growth. With a wavelength of 660 nm the prototype of the Oslon Square Hyper Red, for example, can control the growth of blossom. Together with the deep blue (450 nm) and far red (730 nm) versions, the Oslon family covers the entire spectrum of plant growth.

The prototype of the LED has an integrated 2 mm x 2 mm chip which provides improved performance. By using the latest technologies, developers have been able to achieve a typical radiant power of 905 mW with radiant efficacy of 60 percent, at a current of 700 mA and an operating temperature of 25°C. This represents an improvement of 13 percent in terms of radiant power and 25 percent better radiant efficacy compared with the current Oslon SSL. The beam angle of the Oslon Square Hyper Red is 120°.

"Thanks to its high corrosion resistance and long life, the new Oslon Square Hyper Red is extremely reliable. Our new flagship product therefore also meets the usual high quality standards of the entire Oslon family", said Kok Peng Lim, product manager SSL at Osram Opto Semiconductors.

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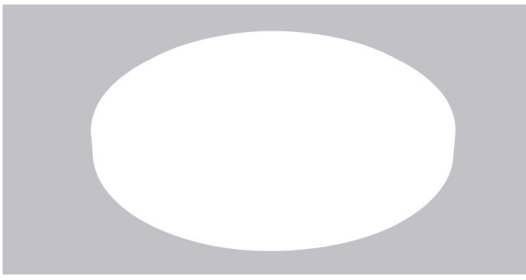

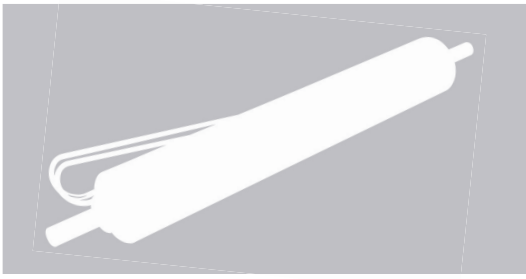

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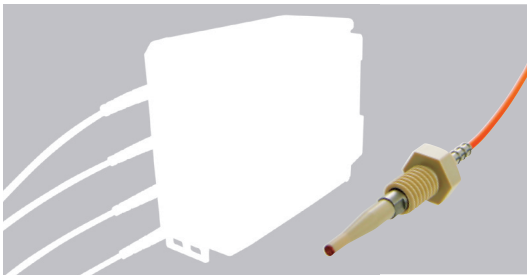

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Cambridge Nanotherm addresses UV-LED thermal management challenges

THERMAL management company Cambridge Nanotherm has launched Nanotherm DMS, a direct-metallised single-sided thermal management solution for UV-LED modules.

UVA LEDs are rapidly displacing traditional UV lamps in the industrial printing industry, speeding up print times and reducing cost. UVC LEDs are also opening up applications like portable sterilisation units that can provide millions with clean drinking water, or let you sterilise your toothbrush when you're camping.

However, UV LEDs present a significant thermal challenge. UVC LEDs often only convert 5 percent of power into photons. The remainder must be conducted away as heat via the base of the LED to a thermally conductive PCB to avoid the LED die overheating.

As shorter wavelengths of UV light degrade organic material the choice of PCB is often limited to inorganic materials, discounting cost-effective metal-clad PCBs (MCPCBs) that rely on an organic epoxy based dielectric layer. Ceramics such as Al_2O_3 or AlN are used, but they present a conundrum to LED designers - low-performance but cost-effective Al_2O_3 (25W/mK), or high-performance but expensive AlN (140-170W/mK). Ceramic is also brittle and prone to cracking, far from ideal for new of portable applications and equally an issue for industrial applications overtighten a screw and the module PCB will fracture.

Cambridge Nanotherm has developed Nanotherm DMS to address these issues. It combines the robustness and manufacturability of aluminium with the high thermal performance of AlN and as it undergoes thin-film processing, it's entirely inorganic. Nanotherm's direct metallised single-sided PCB (Nanotherm DMS) uses an extensively patented electro-chemical oxidation (ECO) process to convert the surface of aluminium into an alumina dielectric layer. This nanoceramic alumina has a thermal conductivity of 7.2W/mK which, coupled with being just tens of microns thick and using a direct metallisation process, gives a composite thermal performance of 152W/mK.

While this is slightly inferior to the very best and most expensive AlN substrates, the mechanical robustness of the Nanotherm metal board permits better approaches to mounting so measured system performance exceeds that of AlN. Cambridge Nanotherm sales and marketing director Mike Edwards said: "UV LEDs are opening up incredible new opportunities for applications ranging from the life changing to lifestyle changing. The challenge for module manufacturers remains how to balance thermal requirements with cost and practicality. With Nanotherm DMS there is now an option that brings together the performance of ceramics with the robustness and manufacturability of MCPCBs and being fully inorganic it won't degrade with use."

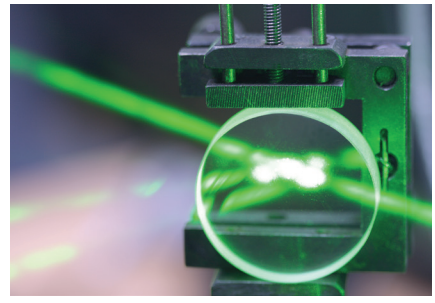
CST Global to increase laser test throughput

CST Global, the UK-based III-V opto-electronics foundry, has introduced an automatic visual inspection machine, increasing laser throughput and test accuracy. According to Colin Jackson, production project engineer at CST Global, the new inspection machine takes throughput from 10,000 lasers per shift to 30,000. CST Global worked with the visual inspection machine manufacturer, Keyence, and software developer, Wolf, to commission, develop and optimise the new machine.

"The Visual Inspection machine brings other key benefits to CST Global. We now only need one inspector per shift, allowing us to re-deploy valuable resources elsewhere. We can track wafer batch quality, working with our key suppliers to help increase yield. Finally, we are streamlining the visual inspection process to handle yet more gel packs per shift. We expect throughputs to near 40,000 lasers per shift, shortly," adds Jackson.

Osram Opto Semiconductors is leading a project called UNIQUE to develop high-power AlGaN-based UV LEDs (with wavelengths in the 260 to 280nm range) for disinfection applications. By developing a small, cost-effective, energy-efficient, mercury-free, long-life UV diode the project partners are looking to gain a strong position on the growing market for UV LEDs and use the results of the project to strengthen Bavaria as a location for business. UNIQUE is funded by the Bavarian Ministry for Economic Affairs, Media, Energy and Technology, and involves five Bavarian companies and research institutions.

Aprotec GmbH is responsible for the design of a special installation for producing AlN volume crystals by evaporating AlN powder at over 2000°C.



The Fraunhofer Institute for Integrated Systems and Device Technology (IISB) is in charge of developing a process chain for producing AlN substrates. Osram Opto Semiconductors is developing the UVC LED chip with the associated component epitaxy and processing on the basis of the AlN substrate. UV LED chips need the protection of a gas-tight package that offers a constant vacuum and therefore a stable atmosphere for the chip. Developing a permanently vacuum-tight package from inorganic UV-stable materials and evaluating the structure and connections are the tasks of SCHOTT AG in Landshut.

Infineon starts volume production of first full-SiC-module

INFINEON is starting volume production for the EASY 1B, the first full-SiC module that was announced at last year's PCIM 2016. At PCIM in Nuremberg, the company is showing additional module platforms and topologies for the 1200 V CoolSiC MOSFET family. Infineon says it is now able to bring the potential of SiC technology to a new level.

"SiC has reached a tipping point: Taking cost-benefit analysis into account, it is ready for use in a variety of applications," said Peter Wawer, division president Industrial Power Control from Infineon. "In order to make the new semiconductor technology a revolution to rely on, however, it needs a partner like Infineon. Products tailored to the application, our own production capacities, comprehensive technology portfolio and system understanding: these four building blocks have made us the market leader for power semiconductors. We want and will also achieve this with our SiC product portfolio." The new 1200 V SiC MOSFETs have been optimised to combine high reliability with performance. They show dynamic losses which are an order of magnitude lower than 1200 V silicon IGBTs. First products will initially support upcoming system challenges in applications such as photovoltaic inverters, uninterruptible power supplies (UPS) and charging/storage systems. The new configurations will also enable new solutions in industrial drives, medical technology or auxiliary power supplies in the railway sector in the near future, according to Infineon.

One major advantage of the trench technology with the 1200 V SiC MOSEFT lies in an extended robustness. This is due to the lower failure in time (FIT) rate and the short-circuit capability, which can be adapted to the respective application. Thanks to a threshold voltage (V th) of 4 V and the recommended switch-on threshold (V_{GS}) of +15 V, the transistors can be controlled like an IGBT and safely switched off in the event of a fault. The SiC MOSFETs enable very fast switching transients. In addition, Infineon's technology offers an easy adjustability of the transients via gate series resistors. The EMC behavior can thus be easily optimised. Last year, Infineon announced the lead products EASY 1B (Half-Bridge / Booster) as well as the discrete TO-247-3pin and -4pin solutions. The EASY 1B platform is well established and an ideal module platform for fast switching devices. At this year's PCIM fair, Infineon will be exhibiting additional module platforms and topologies based on the 1200 V SiC MOSFET technology. This extends the performance spectrum of the CoolSiC MOSFETs step by step.

Among others, Infineon is showcasing the following SiC modules:
EASY 1B with B6 (Six-Pack) topology module has an on-resistance of only 45 mΩ. An integrated body diode ensures a low-loss freewheeling function. The EASY 1B is suitable for applications in the fields of drives, solar or welding technology. EASY 2B with Half-Bridge topology offers an enhanced performance with an on-resistance of 8 mΩ per switch. The low-inductance module concept is suitable for applications with more than 50 kW and fast switching operations. These include solar inverters, quick-charging systems or solutions for uninterruptible power supplies.

62 mm with Half-Bridge topology features even higher power with on-resistance of 6 mΩ per switching function. This module platform offers the possibility of low-inductance connection of systems in the medium power range. A great variety of applications make use of this, including medical technology or auxiliary power supplies in the railway sector, to name a few. Because of the large number of possible applications, Infineon anticipates a rapid spread of this module. The lead products introduced at PCIM 2016, EASY 1B and the two discrete devices TO-247-3pin and -4pin, are gradually entering volume production during this year. The Half-Bridge configuration for the EASY 1B is now available. Its market launch is supported by various driver modules and demo boards, which are also available from now on. The new product configurations are available as samples, and the serial start is planned for 2018.

StratEdge packages to include high-power GaN transistors and MMICs

STRATEDGE CORPORATION, a company that makes high performance semiconductor packages for microwave, millimeter-wave, and high speed digital devices, has expanded its LL family of high-power laminate copper-moly-copper (CMC) base packages to include both GaN transistor and MMIC device packages and package assembly services.

The packages can now accommodate large MMICs, with die attach areas as high as 5.92 x 12.14 mm. They operate at frequencies from DC to as high as 63GHz for applications in communications, radar, automotive, aerospace, defense, and those requiring high power millimeter-wave signals.

In addition to the packages, which are manufactured in StratEdge's San Diego, California facility, StratEdge offers complete automated assembly and test services for these packages, including gold-tin solder die attach.These assembly processes are said to routinely generate >96 percent void-free attachment with bond line thicknesses of <6 microns when used with the new LL series of packages. This is particularly important for GaN power amplifiers where efficient thermal transfer is critical for improved operation and reliability of the device.

The LL family of CMC-base packages dissipate heat from high-power compound semiconductor devices, such as GaN, GaAs, and SiC. These laminate power packages are built with a base material ratio of 1:3:1 CMC, which provides a good thermal match for alumina-based materials and a GaN chip.

"StratEdge was one of the first to market with laminate power packages for GaN devices," said Tim Going, StratEdge president. "StratEdge has continued to develop packages to handle the requirements of new materials and devices. Our LL family additions can handle frequencies up to 63 GHz and large MMIC devices, and our precision automated assembly and test services enable the chips to operate with the efficiency and electrical integrity they were designed to achieve."

StratEdge will be exhibiting at the 2017 International Microwave Symposium (IMS2017), to be held 6-8 June 2017, at the Hawaii Convention Centre in Honolulu, Hawaii.

Raytheon GaN radar surpasses 1000 operational hours

RAYTHEON has announced that its GaN-powered Active Electronically Scanned Array (AESA) proposed upgrade to the Patriot Air and Missile Defense has surpassed more than 1,000 hours of operation in just over a year - half the time of a typical testing program.

"We achieved this milestone so quickly because of our successful experience developing and maturing GaN for programs like the US Navy's Air and Missile Defense Radar," said Doug Burgess, director of AESA programs at Raytheon's Integrated Defense Systems business. "We're ready to take the next step and get this radar into the hands of our customers."

During the course of the 1,000 hours, Raytheon's GaN-based AESA prototype radar routinely demonstrated 360° capability by working together with a second GaN-based AESA antenna that was pointed in a different direction. As targets flew out of one array's field of view and into another, the two arrays seamlessly passed information back and forth, tracking the target continuously. The main array also detected and tracked tactically maneuvering fighter jets and thousands of other aircraft, according to the company.

"Raytheon's GaN technology is backed by 19 years of research and $300 million in investment, while our competitors are either new to the market or primarily build GaN for commercial applications," said Ralph Acaba vice president of Integrated Air and Missile Defense at Raytheon's Integrated Defense Systems business.

Raytheon's GaN-based AESA radar will work with the Integrated Air and Missile Defense Battle Command System and other open architectures. It maintains compatibility with the current Patriot Engagement Control Station and full interoperability with NATO systems. A number of current and expected future Patriot Air and Missile Defense System partner nations in Europe and Asia have expressed interest in acquiring GaN-based AESA.

Poland submitted a Letter of Request for GaN-based AESA Patriot, March 31. Raytheon's GaN-based AESA technology also meets Germany's requirements for the German Taktisches Luftverteidigungssystem, or TLVS, tactical air and missile defence system.

Cree President and CEO Chuck Swoboda steps down

CREE'S CHAIRMAN, president and CEO Chuck Swoboda will step down from his executive positions and as a member of the board of directors following a transition period. Swoboda stated: "I have had the privilege of leading Cree for 16 years, which has been extremely rewarding both professionally and personally. My decision to change my work-life balance follows a recent medical issue, which was resolved, and which caused me to revaluate my priorities."

He added: "I believe that this is a good transition time for Cree as we have three core businesses poised to enter another phase of accelerated growth. I know that under its next CEO, Cree will continue to disrupt markets with new technologies and superior-performing products that deliver great value to our customers while consuming less energy. I look forward to working with the Cree board to find the right leader and to ensure a smooth handoff to my successor."

Swoboda intends to stay on until a successor is appointed, and thereafter

will remain available as a consultant to the company to ensure a seamless transition of leadership responsibilities. Since joining Cree in 1993, Swoboda has held numerous executive positions with the company, leading Cree from a near start-up to today's technology market leader, with approximately 6,400 employees worldwide. Swoboda has served as a member of the Cree board rs since 2000, as chief executive officer since 2001, and chairman since 2005.

In 2010, Mr. Swoboda was named Ernst & Young's Entrepreneur of the Year for the Carolinas, and in 2013 he was named The Edison Report's Lighting Industry Person of the Year. Cree was recognised as one of MIT Technology Review's 50 Smartest Companies for 2014, and as one of Fast Company's World's 50 Most Innovative Companies in 2015. Robert A. Ingram, lead independent director of the Cree board said"

"The board extends its deep appreciation to Chuck for his outstanding leadership over the past 16 years as CEO, and for his 24 years of service to Cree. During that time, his passion for the business and focus on innovation has helped transform industries and has enabled the company to achieve an eight-fold increase in revenue."

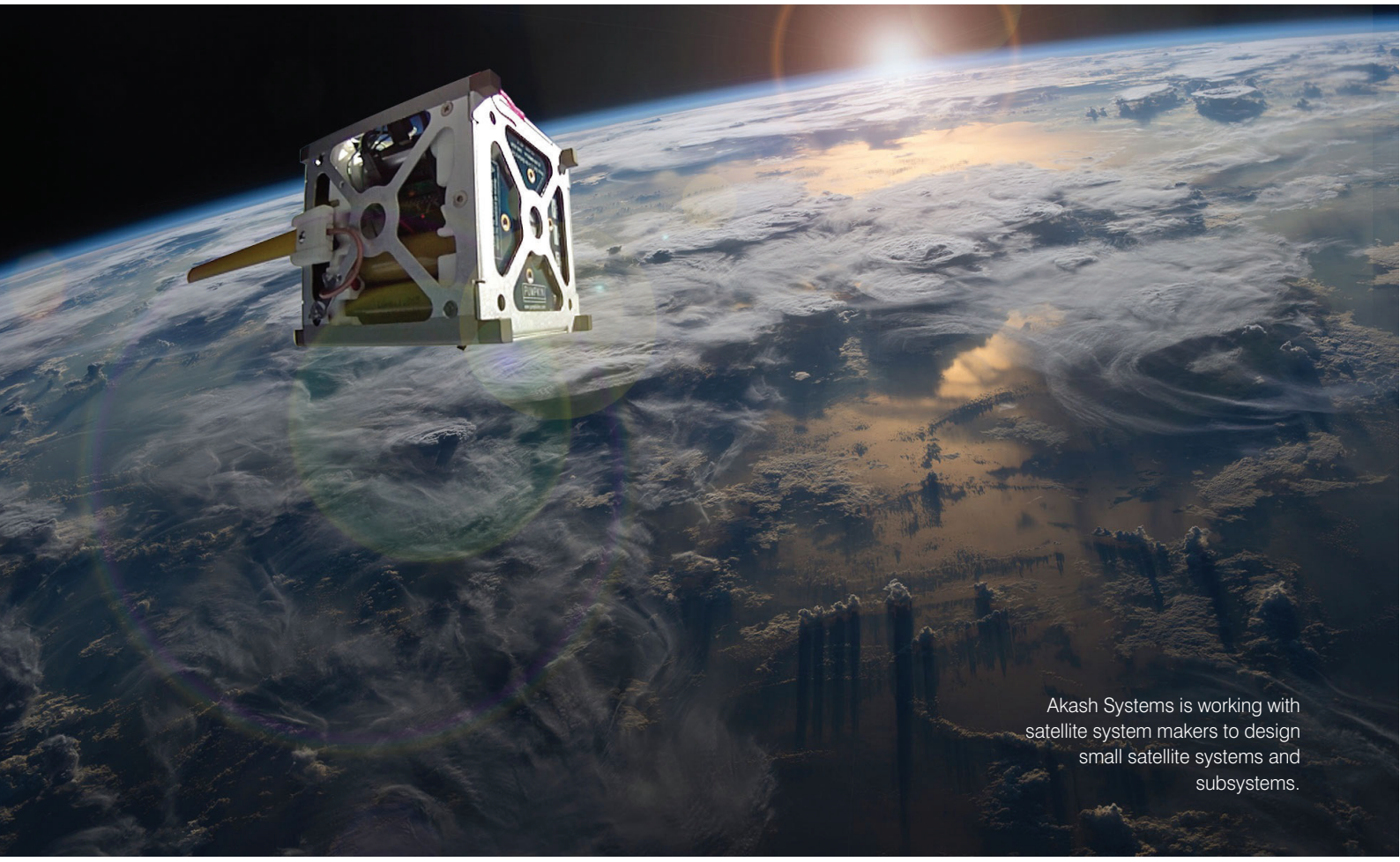
Ingram concluded: "Given Chuck's decision, he and the rest of the board agree that now is the right time to accelerate the process to identify a new CEO to lead Cree and further grow our three businesses. We look forward to Chuck's continued leadership as we conduct our CEO search and transition."

Soraa expands into directional luminaires

GaN on GaN LED specialist Soraa has announced its expansion into the directional luminaire market. The new Arc range is built around a very low profile die-cast heat sink, and optimised for superior thermal management.

"Soraa's core GaN on GaN technology is what makes us different than every other LED company in the world," says Susan Larson, VP at Soraa responsible for the Fixture business and the design lead for Soraa Arc. "It's the science behind our technology that gave my team the ability to design shallow fixtures, small apertures and narrow clean beams, unmatched by anyone else." Soraa Arc will initially be offered in track, pendant, downlight, and surface mounted designs as well as with fixture SNAP accessories, including trims, Snoot and wall washes in a variety of colour light engines with full spectrum 95CRI, R9>95 and Rw 100 typical. Black and white finishes are standard; custom colours are available on request. Arc luminaires with 9°, 10° and 15° beam spreads are also compatible with the existing Soraa SNAP System to further customise beam and light colour.

"Having recently previewed the Arc directional fixtures, our customers are thrilled to now have an end-to-end solution from Soraa they can rely on for a wide range of applications," says George Stringer, senior VP of sales at Soraa.



Akash Systems is working with satellite system makers to design small satellite systems and subsystems.

Akash: flying high ahead

With its GaN-on-diamond power amplifiers entering satellite markets, Akash Systems is reaching for the sky, reports Rebecca Pool.

AS GLOBAL DEMAND for data soars and today's communications infrastructure struggles to suffice, GaN industry veterans have joined forces to tackle the problem head on.

Akash Systems was founded in January 2016 by GaN pioneer and former Group4Labs chief executive, Felix Ejeckam, with Cree executive, Ty Mitchell, to drive GaN-on-diamond technology firmly into the satellite communications space.

As Mitchell tells *Compound Semiconductor*: "We wanted to solve the biggest problem in satellite communications today – data access and cost – and are focused on providing fast, cost-effective and high-bandwidth communications across Earth and in deep space."

To this end, the company is developing and supplying next-generation small, powerful and cost-effective CubeSats, with, of course, the RF power amplifiers that power these systems. But as always, speed and power come at a price, and it's heat.

While today's GaN-based HEMTs can ideally reach an incredible 40 W/mm RF power at 10 GHz frequencies or more, thermal heating limits power densities to around 10 W/mm. Mitchell is certain GaN-on-diamond will make the difference.

"Look at any communications application and the power amplifier is the most power hungry and hottest element in the system, but GaN-on-diamond could change this," he says. "High thermal conductivity diamond can remove the heat in an amplifier by up to four times faster than any other substrate in use today."

"Using GaN-on-diamond RF amplifiers we intend to create small, powerful and cost-effective satellites that provide much higher data rates for services that depend on information density and quality, like high definition video streaming," he adds.

And with ex-Qorvo heavyweights, Kris Kong and Paul Saunier, also in tow, the company is moving forward fast. GaN-on-diamond hybrid power amplifiers and MMIC power amplifiers are already entering the market. Meanwhile plans to work with satellite system makers and design CubeSat systems and subsystems are well underway.

By 2019, Akash aims to deliver various sized CubeSats, and 300 W K_a-band transmitters, with blisteringly fast downlink data-rates of 100 Gbps to 1 Terabit, as well as extremely high-resolution earth imaging and terapixel video capabilities. Then by 2021, the company intends to have satellites in low Earth orbit offering communications bandwidth for cheap, high-speed global broadband access, live streaming imaging and more.

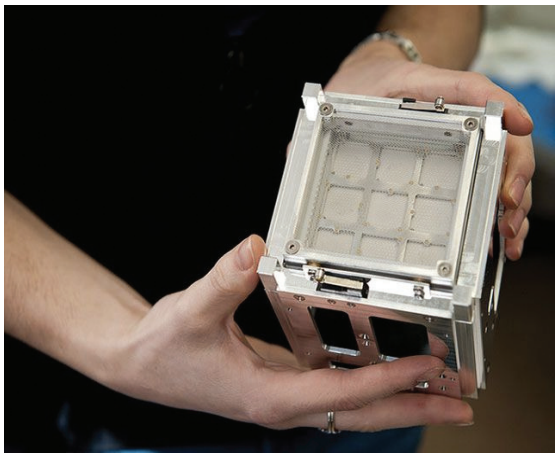
"We'll have our product line of amplifiers filled out during 2018 and at the same time will complete our initial CubeSat design," highlights Mitchell. "In 2019 we will continue to iterate on the CubeSat designs and then get a window for launch."

"Timing is aggressive – it has to be – but it is absolutely do-able, and we have a firm plan to get there," he asserts.

Potent IP

Akash Systems' satellite ambitions have been years in the making, starting in 2003 when Ejeckam launched Group4 Labs to develop methods for fabricating the first ever GaN-on-diamond wafers. By lifting GaN epitaxy from its original growth substrate – silicon – and transferring it to a synthetic CVD diamond substrate, Ejeckam and colleagues could enable customers to manufacture high performance RF and power semiconductors.

Crucially, Group4's GaN-on-diamond technology was the first of its kind to become commercially available. By 2013, the company had concluded its DARPA Near Junction Thermal Transport (NJTT) program, and partners at Raytheon and Triquint Semiconductor had separately announced that their GaN-on-diamond devices had outperformed GaN-on-SiC. In HEMTs, for example, Raytheon achieved a three times improvement in GaN-on-diamond's RF areal power density, compared to GaN-on-SiC devices.



Akash Systems is developing and supplying next generation CubeSats.

Still, come mid- 2013, the company's intellectual property and assets were acquired by technology partner Element Six. And by the start of 2016, Ejeckam left Element Six, and he and Mitchell began negotiations to buy back the IP from Element Six.

"We had been talking about how powerful this technology could be at a systems level as it would solve the heat problem in electronics systems," says Mitchell. "Also at Cree, I had seen first-hand how a fundamental technology could have a huge impact at the systems level, and expand, even create, new industries."

"So we figured that if we could use this GaN-on-diamond IP we would have something very exciting," he adds.

Given this, the pair worked with global RF and microwave component manufacturer, RFHIC, to jointly buy back the all-important IP from Element Six. And by mid-2016 Akash Systems had agreed to acquire Element Six's patents and IP rights relating to the technology for use in satellite communications with RFHIC acquiring technology rights for several applications including wireless communications.

So as RFHIC gets ready to deliver RF power transistors and systems for wireless infrastructure markets, Akash has its sights firmly set on satellites. Right now fabrication takes place on 100 mm GaN-on-diamond wafers, although scaling up to 150 mm in the future is a clear option. Price-wise, Mitchell is adamant that the overall cost-per-Watt for amplifiers based on the GaN-on-diamond is competitive with GaN-on-SiC devices and is confident satellite pundits can see the benefits of his company's technology.

Still, as he highlights, Akash is not setting out to compete with GaN-on-SiC devices. "The purpose of GaN-on-diamond is not to supplant GaN-on-SiC and I believe the technologies are actually complementary."

"However, GaN-on-diamond will enable satellite systems to reach new levels of performance," he adds. "We want to redefine what people believe are the limitations in satellite communications."

Setting the SiC standard

With a state-of-the-art SiC line up and running, and packaging facilities soon to come online, the New York Power Electronics Manufacturing Consortium is poised to deliver next generation power devices, discovers Rebecca Pool.

In a breakthrough for power MOSFET qualification, the New York Power Electronics Manufacturing Consortium (NY-PEMC), led by the State University of New York Polytechnic Institute (SUNY Poly), recently produced patterned wafers in its SiC process line at SUNY Poly's Albany, NY, campus.

As Jeffrey Hedrick, Vice President of SUNY Poly, tells *Compound Semiconductor:* "This means we are up and running, our tools are up and running, and our engineers and scientists are now working hard to fabricate these advanced devices."

It all started in 2014 when the General Electric Company (GE) partnered with SUNY Poly to build a state-of-the-art 150 mm process line for silicon carbide MOSFETs and diodes.

Forming the New York Power Electronics Manufacturing Consortium – NY-PEMC – with SUNY Poly, GE provided more than $100 million in intellectual property, while overall investment in the consortium, including support from New York State, reached $500 million.

Then, come 2015 and another $100 million in New York State funds, GE and SUNY Poly revealed plans to establish a power electronics packaging facility at the Computer Chip Commercialization Center (Quad-C) located on SUNY Poly's Utica campus.

And with Danish power module manufacturer, Danfoss Silicon Power, recently joining GE and SUNY Poly to set up SiC power module packaging operations here, NY-PEMC looks set to become the 'silicon carbide corridor' of North America.

Hedrick certainly thinks so. Heading up both the wafer fabrication and packaging arms of NY-PEMC, he highlights how the manufacturing consortium will help provide much needed jobs and revitalise the economy of Upstate New York.

GE will fabricate cutting-edge SiC chips that will then be assembled and packaged by Danfoss for integration into systems. Fabrication capabilities will top 15,000 wafers a year, and with Danfoss earmarked to operate the only domestic high-volume packaging centre in a burgeoning US market, the future for NY-PEMC looks bright.

"GE and Danfoss are our core members, and we expect to add other key partnerships in the near future," says Hedrick.

"We're equipped to easily run 15,000 wafers a year, which is more than sufficient for the next three years, and we have the expansion capabilities to increase this figure to 50,000 when the market ramps up to higher volumes."

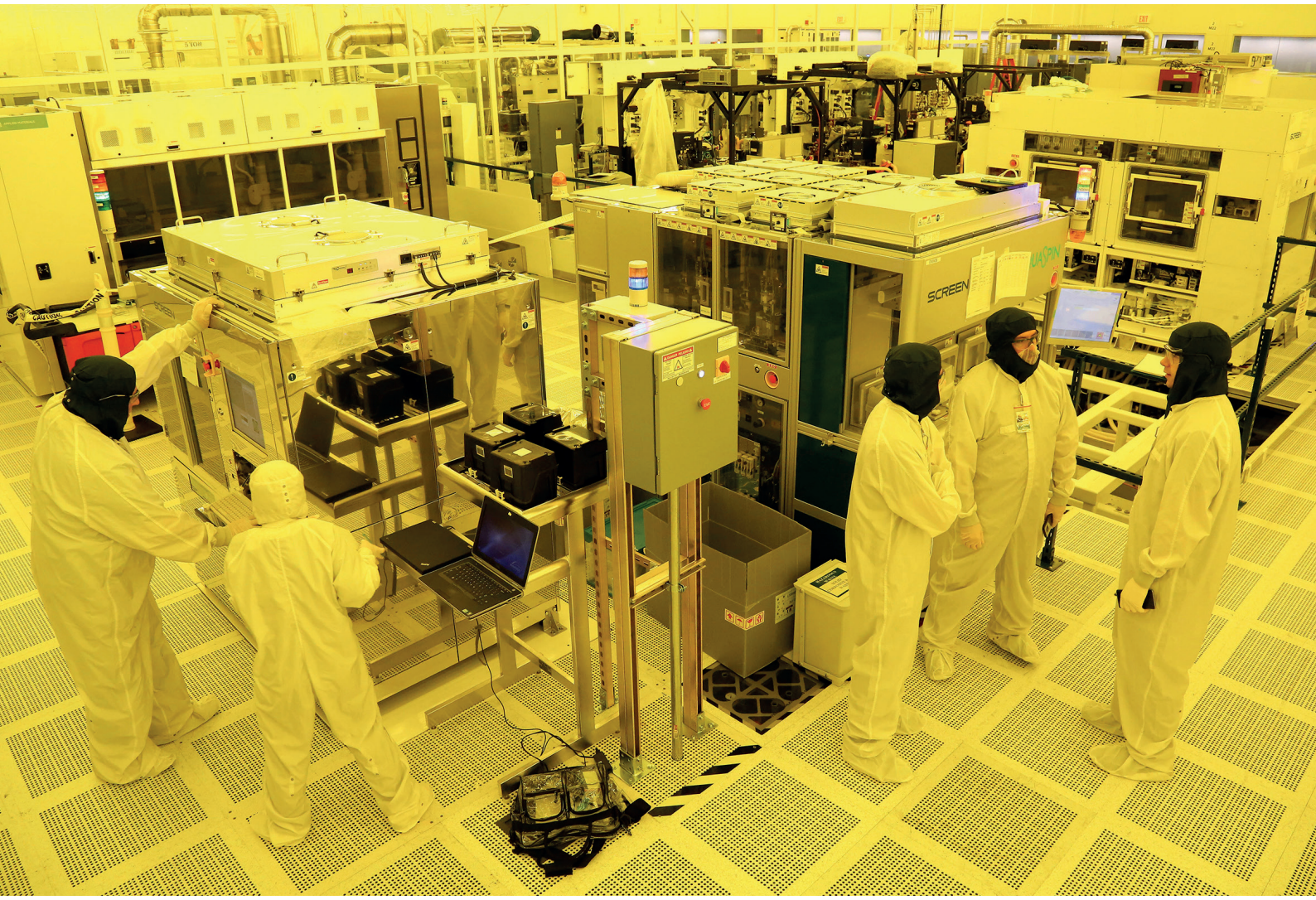
Latest developments

In recent months, activities at NY-PEMC's wafer fabrication arm have focused on scaling up its baseline process flow to manufacturing readiness. The process flow includes technology developed at the GE Global Research Center in Niskayuna, New York. And as Hedrick points out: "GE has been continually working with us to transfer technology from its research centre to our line in Albany."

Right now, the wafer fabrication facility is in its final stages of ISO 9001 certification in a SiC-dedicated Class-1 capable cleanroom. All tools, including photolithography, reactive ion etching, metallization, metrology, measurement, in-line electrical test and more, are nearing full installation. And the consortium's team of engineers intends to have the process flow verified and qualified – to automotive AEC-Q101 reliability specifications – by the end of this year.

"We're focusing on process setup and verification right now," explains Hedrick. "But very soon we will be able to fabricate qualified MOSFET devices with unmatched reliability."

Indeed, come 2018, 1.2 kV MOSFET fabrication will be well underway, and this is just the beginning. Hedrick



and colleagues intend to offer 1.7 kV MOSFETs shortly thereafter, and then higher voltage devices and integrated circuits by 2020.

What's more, the tools installed in the SiC process line are 200 mm-capable equipment from top-tier manufacturers, and as Hedrick points out, have been 'chucked down' to support 150 mm wafers.

"The industry is currently transitioning to 150 mm substrates and will eventually transition to 200 mm substrates," highlights Hedrick. "In a few years from now when the 200 mm substrates are technically and economically viable, we will be able to chuck our tools up at a low cost. "As the market ramps up, we're going to be ready," he adds.

Meanwhile, activities are also well underway at the packaging centre at Quad-C in Utica. The site will house manufacturing lines for industrial, transportation, and automotive applications, while additional lines will be devoted to research and development, and prototyping of new modules and power blocks.

"We have a very aggressive schedule to get the packaging facility set up for Danfoss and we are ordering many of the custom tools right now," says Hedrick. "These have a lead time of up to eight months and we'll get many of them by the end of this year. We'll start installing these tools as soon as we can, and have the first three lines qualified in 2018," he adds.

So with all systems go for the next few years, what does the longer-term hold for NY-PEMC?

Hedrick, for one, hopes to continue extending what he describes as the power electronics ecosystem within NY-PEMC.

"I'm currently seeking additional funding to create a design centre for power electronics devices and systems," he says. "We're also very open to working with businesses that may want to bring SiC substrate and epi wafer production capability to New York. We'll continue to develop this high-tech corridor across New York, and I expect that many consumable and equipment suppliers will soon be joining us."

Perfecting 200 mm processing tools

As the demand for MEMS, sensors and mobility expands, heterogeneous devices on 200 mm substrates will become more common to address that increased demand.

Devices such as GaN-on-Si for RF (Radio Frequency)and power, and BAW/FBAR and MEMS on various substrates, will require a new generation of 200 mm process tools to satisfy the needs for high-throughput and high yield lift-off compatibility. Batch sizes will also be enlarged to match that of other process steps. High collection efficiency of precious metals will continue to a driver for reduced device cost and excellent wafer and batch film uniformity will continue to be required for new device performance across all materials of interest.

Ferrotec announces a new lift-off metal deposition system to meet these needs for 200 mm substrates, the Temescal UEFC-6100 ultra-efficient electron beam evaporator.

A key factor to achieve high yield lift-off is the near normal incidence of the deposition across the entire wafer surface. This is best achieved with the line of sight material travel of e-beam deposition at long source-to–substrate distances. The UEFC-6100 is designed for source-to-substrate (SR) distances of 43" (1092 mm) or 46" (1168 mm) to achieve ≤ 5 degree incident angles at all locations on a wafer's surface.

Dual-axis and patented no-contact, magnetically driven HULA (high uniformity lift-off assembly) wafer motion ensures excellent uniformity across multiple process conditions. HULA motion also delivers the highest material collection efficiency for precious metals by minimizing the need for large area uniformity masks while maintaining a high wafer packing fraction. Throughputs are further aided by the intelligent conic chamber designs; which minimize and optimize both volume and total non-substrate coated surface areas within these systems.

These factors improve pump down times by minimizing outgassing surfaces and their coating based degradation in pump times due to condensate build-up over multiple operating cycles.

A large 25x (200 mm) wafer batch also improves throughput while limiting the need for tracking split lots that may be required in smaller tools. As the size and value of the wafers increases, automated wafer handling becomes more preferred. This new system design is matched with the Ferrotec Wafer Valet automatic wafer handling system to eliminate the need for operators to handle individual wafers, which speeds tool load and unload times and reduces the risk of handling errors.

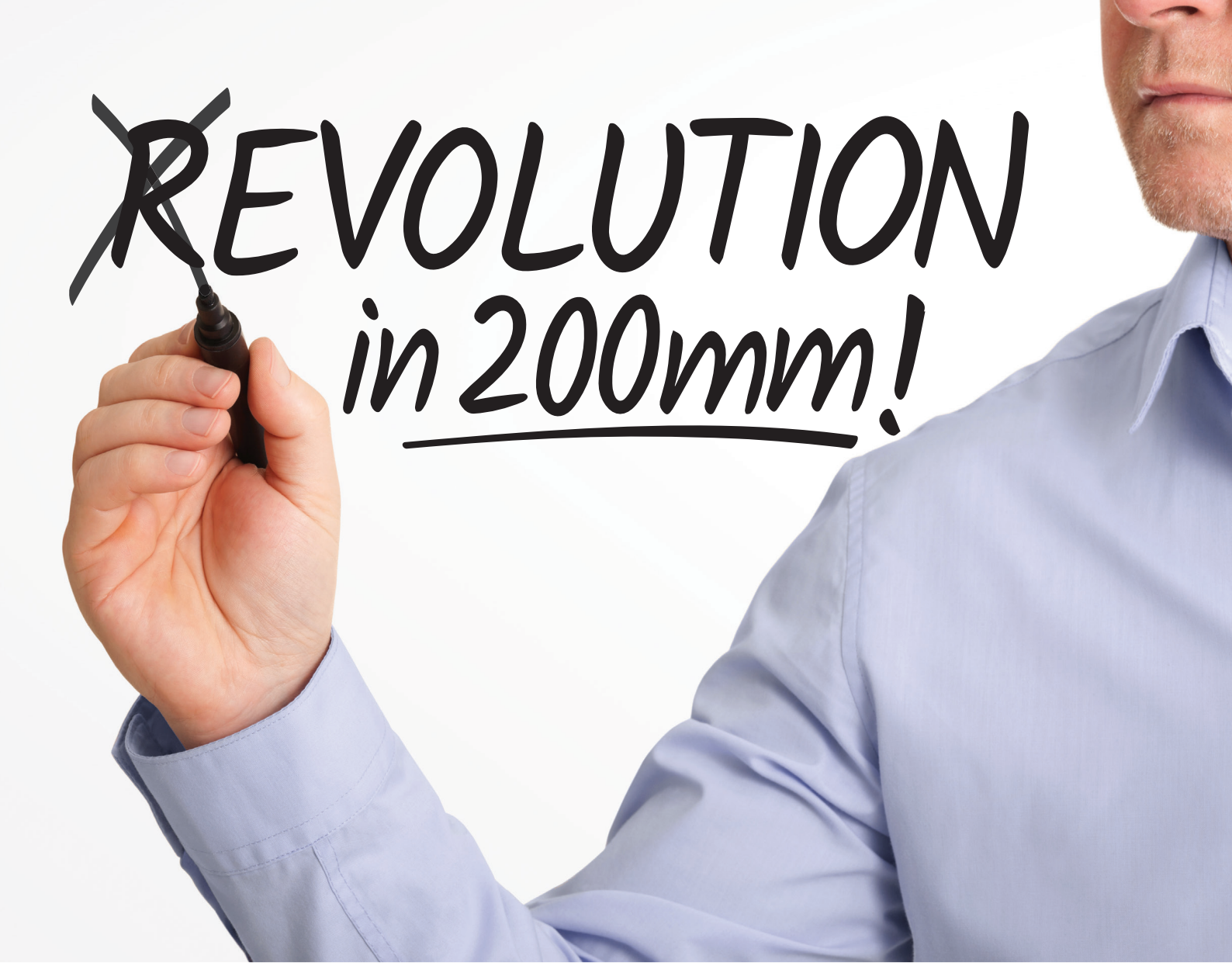
The combined effect of all these design factors is pointed out in the table below. The table compares performance for deposition of a 1 micron thick gold layer of the UEFC-6100, with two other tool designs; an existing tool originally designed for 150 mm wafers at 43" throw distance that could hold up to 18 x 200 mm wafers, and a theoretical "best design" for a traditional box style system with a single axis of rotation carrier that could handle 25 x 200 mm wafers.

With the assumption that masking to achieve uniform films is required, it is clear the UEFC-6100 outperforms the traditional designs in all areas listed.

	FC-4400, 43"SR	UEFC-6100, 43"SR	UEFC-6100, 46"SR	Single Axis "Best Design", 46"SR
Max Angle of incidence, degrees	5.1	5.1	4.8	4.8
Number of wafers per run	18	25	25	25
Net Cycle time, minutes	70.1	68.0	68.0	78.0
Wafers produced per hour	15.4	22.0	22.0	19.2
Collection Efficiency	17.9%	23.3%	21.7%	19.2%
Cost of Au per wafer (at $50/gram), $	$162.14	$124.94	$133.85	$151.26

All samples modeled for 5/a sec Dep rate

Table 1. Performance comparison for deposition of 1 micron gold layer.



Meet the Next Generation in Compound Semi

Introducing Ferrotec's Temescal UEFC-6100 evaporator, the first electron beam system optimized for metallization on 200mm substrates. Wafer sizes are evolving and this new system is ideally suited to meet expanding demands for RF filter and other emerging compound semi heterogeneous integrated substrates.

The UEFC-6100 is engineered for production, with a 25 wafer batch size, the unique Temescal conic chamber, the HULA–High Uniformity Lift-off Assembly, and the Auratus™ deposition process enhancement methodology.

Don't let evolution pass you by, find out more. Contact Ferrotec at 1-925-371-4170.

FerroTec

Price erosion and a slowing of smartphone growth will lead to a very modest increase in the GaAs market, argues Eric Higham from Strategy Analytics in an interview with Richard Stevenson

GaAs sales set to **plateau**

Eric Higham

Q Will the introduction of 5G deliver a hike in GaAs sales? And how long might it be before sales of phones with 5G technology take off?

A I think the answer to that question is being defined as we speak. We have done a number of 5G projects this year. We have talked to a lot of equipment guys, and a lot of operators, to get a sense of what they're looking for.

I'm kind of envisioning it as a multi-variable equation that is getting solved. The solution is going to determine the technology.

One of the things that is going to be fundamental is the definition of massive MIMO. How many of these beams do you have? The equipment guys tend to talk about transmit power in terms if EIRP – effective isotropically radiated power. Those numbers are going to be fixed, and they'll be a number for a macro-cell, or a micro-cell. But the more antenna beams that you are going to have in your massive MIMO network, the lower each transmitter needs to be for a fixed EIRP.

So, if you say my definition of massive MIMO is going to be 16 antenna beams, that implies a different level of power than if it's going to be 128. Depending on what the number of antenna beams you are going to have, you can run from GaN all the way to RF CMOS to meet the power requirements.

There are lots of other factors in this multi-functional, multi-variable equation that I'm talking about. What is going to percolate to the surface sooner or later is power consumption. I heard a company talking about having done a CMOS PA at millimetre-wave frequencies – it might have been E-band – but it has 8 or 10 percent power-added efficiency out of that PA.

If you think that you are going to be doing a massive number of additional base-stations, and each one has a very low power-added-efficiency, how do you find all that power?

The other interesting thing is that as we start to talk about these massive MIMO antennas at 28 GHz or the true millimetre-wave frequency range, antenna physical spacing starts to become an issue.

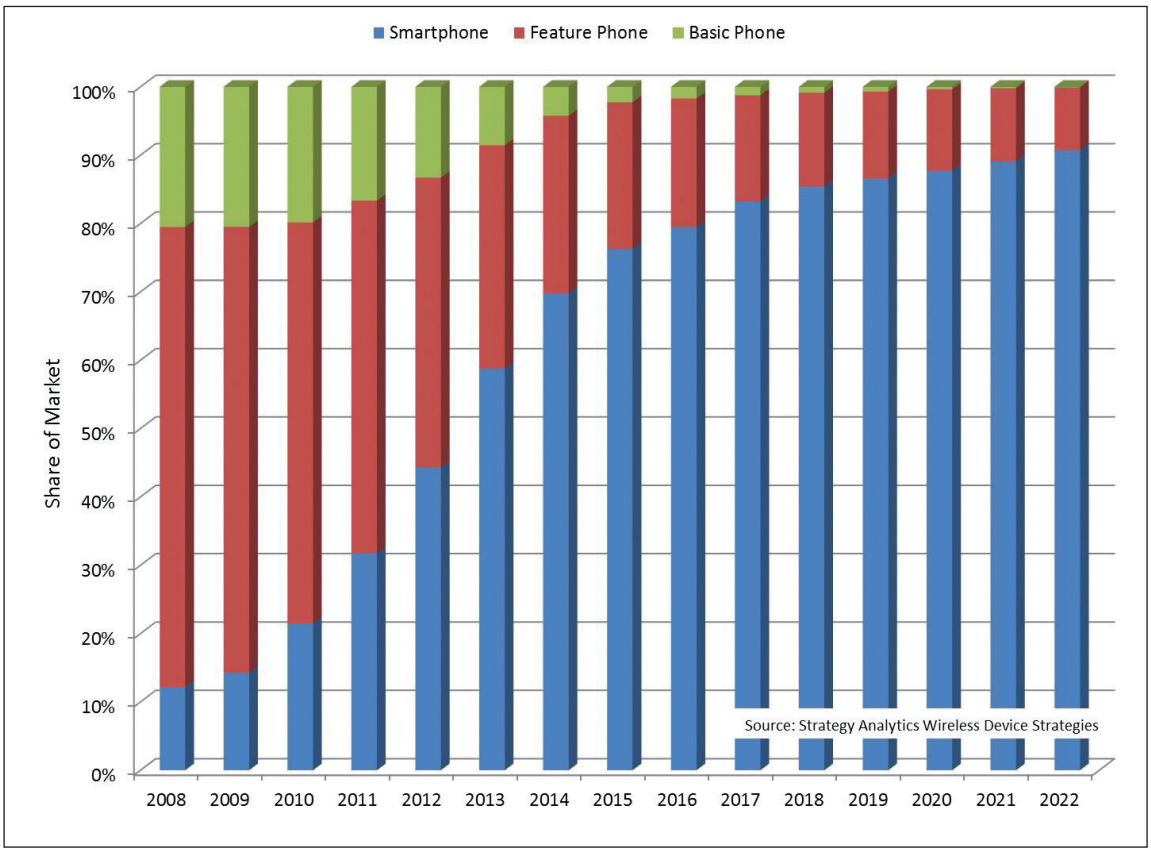
As you go higher in frequency, the wavelength spacing between radiators gets to be a very small physical distance. How do you handle that? Is that running lines along different dimensions? That adds loss and denigrates performance.

With GaN, because for a given power output you can make the chip smaller than other technologies, that might give that technology a leg up, particularly on the packaging standpoint. As these antennas that are half-wavelength spaced tend to be cross-polarised, you tend to have two antennae at that location – and you can put two GaN amplifiers in a package, and maintain that spacing at 28 GHz right up to the antenna radiating element. That might not be the case with other amplifiers, because the amplifiers physically have to be bigger.

The GaAs community is very excited about what is going to happen. For the middle of the range, the number of antennae result in a power level that would be pretty easy for GaAs to handle.

So that's positive, but until we get more consensus on what that architecture is going to look like, I definitely wouldn't rule out GaN, even for the lower power. Nor would I would rule out silicon for some versions, but that's probably RF CMOS.

Smartphones penetration continues to rise, but the rate of growth is in decline.



Q Will there much growth in the global GaAs microelectronics market over the next five years?

A It looks like a little bit of a kick up if you look at the five-year forecast. We will have a little dip in the next couple of years, followed by an upward trending line to get to that little kick-up. But these downs and ups are a percent, or less than a percent, from year to year, so relatively flat.

The cellular market is the largest single driver by far. If you expand that a little bit and call it the wireless market, which will pull in base stations, WiFi and VSAT, then that's 80 percent of the GaAs market. So the trend for cellular, and broader scale wireless, is driving the overall market. Right now, the cellular trend is price erosion, with other technologies capturing share. Smartphones
are driving the cellular market, and the big negative is that we are starting to reach a time in history where smart phone penetration is starting to definitely slow down.

On the flipside, handset quantity goes up every year, and you've still got more complexity. The US just finished its 600 MHz auction, and now handset manufacturers are going to have to figure out how to squeeze that frequency band in amongst all the others.

Q So is the GaAs content in mobile devices still on the up?

A The complexity is increasing, definitely. I'm sure you'll have seen the announcements about speed trials and speed results as we trend towards 5G. Operators are doing that with bigger chunks of spectrum, but also with carrier aggregation.

What does that mean for the handset? More linearity in the power amplifier, and definitely more complexity and more sophistication in that front-end.

What makes answering your question a little bit more challenging is that device manufacturers have done a great job at being able to do multi-mode, multi-band – and the number involved in the multi portion of that is increasing. If you are covering five bands or eight bands, that not five or eight PAs. It hasn't been that way for a long time, but I think that the number of distinct PAs is decreasing.

When you started to aggregate, and two bands became one band, it was never twice the price or twice the die area. It was always a little bit less than that. The phone manufacturers are not going to say we like you guys, so we're going to give you more money. So it's conflicting forces. If you look at the bill-of-materials. I think that's going up, but perhaps slowly. That's a positive – one of the only positives in the cellular market.

Q Several years ago, the leading players in GaAs HBT technologies were championing their BiFET and BiHEMT technologies. Are these now in production?

A I think they are. There were being championed as a difference maker, but the reasons for the BiFET have gotten less compelling. However, the more hybrid approach has gotten to be less expensive. If you are going to have to make a couple more wire bonds, or a couple more part placements, I don't think that's significant any more.

Q Is there much investment in GaAs technology. For example, are features sizes shrinking?

A In the silicon industry, everybody is so interested in Moore's Law. That node size is decreasing pretty quickly. The claim is that the GaAs industry isn't doing anything similar. I certainly would say that the GaAs industry is not changing feature sizes as quickly as the silicon industry. But we are seeing a trend towards smaller gate sizes. I know that Qorvo announced a 90 nanometre process in the last year or so, geared towards at the time optical applications. But I'm sure they ported that over to millimetre wave, so point-to-point radio and emerging 5G. I think it's not unusual to see foundries that are in the hundreds – 120, 130 – or down below 100.

Q Is most of the world's production now on 6-inch lines?

A Yes, but I don't think it makes sense to obsolete 4-inch lines. The premise that the mobile handset market drives the GaAs market, and price erosion there is strict, means that it makes sense to go to 6-inch to get to that cost reduction. One of the foundries told me, probably a couple of years ago, that they were seeing somewhere in the 10-15 percent per quarter die shrink, so that's cost saving. If it gets smaller, it gets cheaper. I think companies that have 4-inch are selectively using that 4-inch for some of the other 50 percent of the market that is not handset. This may not have that same negative slope on the price erosion.

Q The number of makers of GaAs parts seems to be declining. Anadigics is no more, and TriQuint and RFMD have merged to form Qorvo. Does this entity and Skyworks have a stranglehold on the market?

A Qorvo and Skyworks account for almost 60 percent of the market. And if you throw in Broadcom and WIN Semiconductor, you are almost up to 75 percent. The GaAs market is bifurcating into the top two heavyweights that are mobile device driven, and everybody else. Everybody else has a pretty wide range of customers – there are 50, or 60 or 70 companies that do something in the GaAs market. Not everyone has their own foundries – a lot of those guys are buying chips and building higher level assemblies. But it's a big universe of companies that will produce devices that have GaAs devices in them.

Q The capabilities of Qorvo and Skyworks seems to have increased, with products that contain several different technologies. The days of thinking of them as simply GaAs HBT makers are long gone, aren't they?

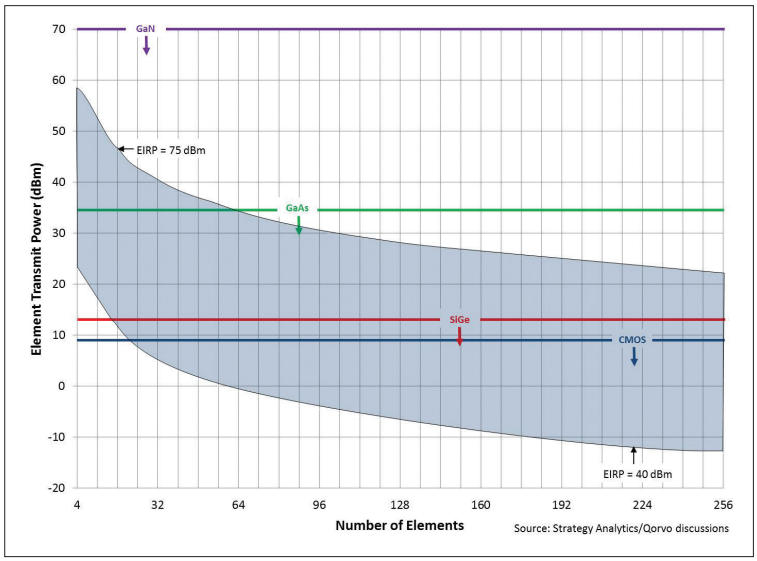
A Very true. Just look at the top-line revenues that both of them report, a smaller and smaller portion of that is GaAs these days.

If you look back in history, Skyworks got left out when Nokia was the biggest handset manufacturer, and Nokia was tied in tightly with RFMD. So Skyworks looked for other manufacturers, other markets and other technologies to remain in that position they had. History has moved forward, and throwing your rod in with Nokia for smartphones turned out not to be the best decision in the world. Some of the other guys that Skyworks looked at, such as Samsung, got to be much more important.

Skyworks has also done a great job of diversifying technology and end markets. They have got involved with the internet-of-things, smart metering – what you might not think of as mainstream markets if you think of Skyworks as strictly a GaAs company. That's in their DNA to find other markets for their technology. Pretty early on they acquired SiGe Microsystems, and had SiGe technology for a while. With Qorvo, with Green Peak, their IoT acquisition, those guys can now do everything on silicon. Now Qorvo can go to shows where you might not think a GaAs company would be. With both of those guys, they have really done a good job in having a technology portfolio. Part of the challenge has been getting comfortable with that outsource model, where they don't have the RF CMOS and the SiGe foundry under their roof.

Q Has the merger of RFMD and TriQuint led to the cost savings that were hoped for?

In the silicon industry, everybody is so interested in Moore's Law. That node size is decreasing pretty quickly. The claim is that the GaAs industry isn't doing anything similar. I certainly would say that the GaAs industry is not changing feature sizes as quickly as the silicon industry



For 5G, the number of antenna employed for the MIMO architecture will determine the power requirements, and thus the suitable technologies.

A Yes, but I don't think it has materialised quite the way they thought it was going to. We all know that synergy is another word for layoffs, and I think that when that $150 million synergy was first announced, most people looked it and thought that's got to be foundry. They would have thought that they've got duplication of foundry, too much capacity, and something is going to happen with that – but it hasn't.

The reason for that is that they have done a really good job in repositioning the foundry, and they have been helped by a big uptick in the filter market. I think that Qorvo, definitely more than Skyworks – but Skyworks to a little extent – have branched off into filters, and things that aren't active parts anymore. For five or six years, growth of Skyworks' GaAs revenue has outpaced the overall market. That allowed them to increase their lead over Triquint and RFMD and then Qorvo. This last year, Skyworks, for the first time in my memory, underperformed the GaAs market growth, which wasn't much. Qorvo seems to have got things squared away and closed the gap on Skyworks a little. They are coming out with new products that are addressing new product segments, and the financial results seem to be forming in a positive direction. So we can assume that they are ready to move forward, and are not spinning their wheels.

Q In general, are profit margins tight for suppliers of components for handsets?

A Yes. However, even though price erosion has been pretty constant in that market, I think they've gotten better by using technology. They've been able to make the multi-mode, multi-band PAs incorporate more bands. So they retain a large portion of that overall revenue by creating a better mouse trap, if you will, to address the problem. They don't just have to compete on whether everything will be cheaper than the guys down the street. I think Qorvo has benefited from a strong filter capability, from the module standpoint. Perhaps they can capture more revenue by supplying a fully integrated module with a number of filters and PAs, rather than just selling them individually.

Q The GaAs HBT is under threat from silicon technologies, such as SOI. How strong is this challenge?

A I think that there have been some interesting developments. About three-to-four years ago Qualcomm announced the RF360 platform that had CMOS PAs and was going to target the latest release of LTE. Shares for WIN, TriQuint, RFMD and Skyworks from before the Qualcomm announcement to the Qualcomm announcement underwent a step function. But as we see now, Qualcomm has just entered into an agreement with one of the Japanese companies to do PAs in GaAs for their higher-frequency, higher-performance offerings.

At the time, we were saying if anyone can get their foot in the door with CMOS PAs, it will be Qualcomm. They have a tremendous amount of expertise to throw at the problem, they've got the name. Having said that, for the lower feature phones, entry-level 3G and the 2.5G that still exists, there is a lot of CMOS PA content. It's just that the drive until recently was to have the latest and greatest smartphone. I don't believe CMOS has gotten much traction in those next-generation, higher-frequency 4G, 4.5G phones, but it is definitely taking market share away from GaAs in the lower side of the market. The good news there is a lot of people are being transitioned, and people are turning off 2 G networks and going to higher data-rate capability.

Q In non-mobile GaAs technologies, is there a place for the little guy?

A If you exclude WiFi, markets are all fairly small. Here you can get some better gross margins than the high volume markets. They end up being the targets of the ecosystem of 50 or 60 companies who aren't Qorvo or WIN or MACOM or Skyworks. None of these guys are big, or have a portfolio that addresses every single market, but they have all found niches. I think what keeps the little guy going is finding those niches where they can do a value added, performance-driven solution, and not have to worry about squeezing that last fraction of a penny out of the cost of the price.

For point-to-point radio, test-and-measurement, and other markets, you can almost count volumes on your hand, and you can get good gross margins. Hittite is the classic example. Those guys minted that 70 percent gross margin quarter after quarter. They would not set foot in the high-volume market, because there is nowhere to get the margins there. I think that's what keeps the second tier, in terms of revenue, going. They find that niche, and they do a good job of that niche.

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CS shares enjoy a tremendous twelve months

Topping this year's shareprice leaderboard are the suppliers of epiwafers, substrates and MOCVD tools

BY RICHARD STEVENSON

IF YOU OWN a portfolio of shares in compound semiconductor companies, you'll be pleased by performance over the last 12 months. While it's not been as stellar as it was seven years ago, when shares in every firm listed on the *Compound Semiconductor Shareprice Leaderboard* delivered double-digit growth, the majority of companies have outperformed the technology-rich NASDAQ – and even that has shot up by nearly 27 percent in the last year.

Example of success include the two industry heavyweights Qorvo and Skyworks, which have delivered gains in share price of 51 percent and 49 percent, respectively, during the twelve months up to the end of this April. Last year, those performances would have been good enough to secure the second and third spots on the table, but this year it's placed them eighth and ninth.

Topping the table this year is epiwafer supplier IQE, which has seen its share price rocket by more than 200 percent; next on the list is substrate maker AXT, with an appreciation of just over 160 percent; and third is MOCVD manufacturer Veeco, which has seen its share price climb by nearly 80 percent.

Possible drivers behind the growth in IQE's valuation can be found in the company's results for the year ending 31 December 2016. These figures, which were reported on 21 March, reveal a 16.4 percent hike in year-over-year annual revenue from £114.0 million to $132.7 million. The increase in sales is attributed to success in multiple markets, plus an 11 percent post-Brexit strengthening of the US dollar against sterling. Adjusted operating profit also climbed, increasing by nearly 17 percent to £22.1 million.

Commenting on the 2016 annual results, IQE CEO Drew Nelson picked out the photonics division as the "star of the show", thanks to its year-on-year growth in sales of more than 43 percent. "This is being driven by VCSEL and InP technologies, which enable a broad range of applications, from fibre optic communication

to advanced sensors and industrial processes." Margins from this sector are high, with an operating profit of £6.9 million on sales of just $22.8 million.

Sales of IQE's photonic products are expected to increase, with the depth and breadth of photonics development programmes and customer qualifications providing a solid platform for strong growth. The company is now shipping 6-inch VCSEL epiwafers, which are claimed to slash the unit cost of chips, and thereby accelerate the adoption of this technology. Devices can be used in 3D sensing, data communications, data centres, gesture recognition, health and cosmetics.

The lion's share of IQE's sales comes from the wireless sector. Here it claims to have 55 percent of the global market. The company "performed well" in this sector, according to Nelson, with sales up 15 percent. However, margins are far tighter than they are in photonics, with annual sales of £91.2 million producing an adjusted operating profit of £7.9 million. Infra-red and CMOS++ are the two other divisions of IQE's business. The former, which produces InSb and GaSb wafers, generated an annual revenue of £10.6 million and an adjusted operating profit of £2.2 million; and CMOS++, which involves the growth of III-Vs on silicon substrates, brought in yearly sales of £1.4 million, and made an adjusted operating loss of £1.6 million.

The hike in IQE's share price may have been spurred on by its increase in capital investment. This shot up between 2015 and 2016 from £10 million to £19.1 million. Investment in equipment increased by £7.1 million to address growth opportunities, principally in photonics, GaN and its rare-earth oxide technology.

Another possible factor behind the surge in IQE's valuation is the tremendous level of activity associated with establishing a compound semiconductor cluster in Cardiff, where IQE has its headquarters. One of the company's visions is to be at the epicentre of the world's first compound semiconductor cluster, and recent progress towards that goal includes: a £75 million investment by Cardiff University to form the Institute of Compound Semiconductors; a £24 million joint investment by IQE and Cardiff University in the formation of the Compound Semiconductor Centre; a commitment by the UK government to £50 million of funding for a Compound Semiconductor Catapult in Cardiff, which will receive a further £100 million in funding from Innovate UK and Industry; and a £10 million investment by the EPSRC's to create a Compound Semiconductor Manufacturing Hub.

AXT's achievements

Glancing at the financial results from AXT leads one to wonder whether it's just the improvement in the earnings figures that has propelled the company's share price from $2.57 in late 2016 to $6.75 a year on. Sales are up, but not much, with revenue for the first fiscal quarter 2017, ending 31 March, worth $20.6 million, compared to $18.7 million for the equivalent quarter of last year. However, it can be argued that the company's bottom line is getting much better: profit hit $0.7 million in first quarter 2017, compared to $42,000 in the equivalent quarter of 2016.

One can argue that the share price is being spurred on by the ambitious plan for the company and the strength of its management. The firm has recently raised $32.3 million through a public offering of 5.3 million shares. Speaking during the first fiscal quarter earnings call, Chief Financial Officer Gary Fischer remarked: "We expect to use the proceeds for general purposes, which will of course include a relocation of the gallium arsenide product line as well as capital for the expansion of our operations to meet the requirements of exciting business opportunities across our portfolio and other things."

According IHS, the average TV panel size exceeded 40 inches for the first time ever in 2016. This is good news for LED makers, and also MOCVD equipment makers, such as Veeco.

When unexpected difficulties arise at AXT, the company acts quickly and effectively. On 15 March, an electrical short-circuit fire broke out at the Beijing manufacturing facility, impacting the electrical power supply supporting 2-inch, 3-inch and 4-inch GaAs and germanium crystal growth. Making matters worse, the fire department accidentally damaged the critical wastewater pipe that services wafer processing. Initially, AXT revised down its forecast for the first quarter 2017 to reflect the halt in production of certain products. However, it didn't take long for the company to address this delay.

"We were able to repair the wastewater pipe much faster than we anticipated, which allowed us to resume wafer processing and orders shipments after four days," explained Fischer in the recent earnings call. What's more, thanks to the use of custom-designed furnaces, engineers were able to rotate key hardware between crystal growth diameters, allowing some 6-inch furnace capacity to be used for producing 2-inch, 3-inch and 4-inch diameter GaAs and germanium crystals.

The upshot of all of this, in combination with exploiting some redundancy in the furnaces, is that sales for first quarter 2017 did not just exceed the revised forecast – they topped the original guidance. This has helped the share price to recover from its pre-fire value, which dropped by about 20 percent in the days after the emergency.

For the second fiscal quarter of 2017 sales are expected to be in the range $22 million to $23 million, a sequential increase of 9 percent. Profit for the quarter should be in the range $1.5 million to $2.3 million, indicating a promising future for AXT.

Veeco rebounds

Last-but-one on last year's leaderboard is Veeco, which has rebounded to third place this year. Between the end of April 2015 and April 2016 its share price fell from just over $30 to below $17, but since then it's climbed from that nadir to hit $33. A driver behind the recovery and soaring share price is a growth in sales and bookings of MOCVD tools, which currently account for the majority of the company's revenue.

Speaking to investors on 4 May, 2017, to discuss the results for the first fiscal quarter, Veeco CFO Sam Maheshwari explained that sales to makers of lighting, display and power electronics products increased by 39 percent quarter-over-quarter, and accounted for 58 percent of the $94 million quarterly sales. "[The]

Compound Semiconductor share price leaderboard

Rank	Company	Ticker	Share value, April 29, 2016 ($)	Share value, April 28, 2017 ($)	% appreciation	Change in Rank
1	IQE (London)	IQE	0.26	0.81	212.5	+6
2	AXT	AXTI	2.57	6.75	162.6	+1
3	Veeco	VECO	18.41	33.00	79.3	+12
4	Riber (Paris)	RIB	1.00*	1.90*	74.0	+5
5	Lumentum	LITE	25.30	42.75	69.0	-2
6	Oclaro	OCLR	5.05	8.01	58.6	-5
7	Emcore	EMKR	5.70	9.00	57.9	-3
8	Qorvo	QRVO	45.03	68.03	51.1	+5
9	Skyworks	SWKS	66.82	99.74	49.3	+5
10	IPG Photonics	IPGP	86.67	126.32	45.7	-5
11	Finisar	FNSR	16.46	22.84	38.8	+4
12	NASDAQ composite	IXIC	4,775.36	6047.61	26.6	-6
13	Aixtron (Frankfurt)	AIX	4.74*	5.48*	15.6	-2
14	Rubicon	RBCN	0.68	0.75	10.3	+2
15	Cree	CREE	24.51	21.99	-10.3	-5
16	Infinera	INFN	11.89	9.92	-16.6	-2
	* Converted to dollars using the exchange rates on 28 April of 1 EURO = 1.0895 USD and 1 GBP = 1.2937 USD					

IQE's share price has rocketed since autumn 2016.

vast majority of this business was derived from EPIK MOCVD reactors to support ongoing demand for blue LED applications. Demand for red, orange, and yellow LEDs drove incremental K475i product sales."

During the call, Veeco's chairman and CEO John Peeler spoke in more detail about the recovery of the LED industry. "Demand for LCD panels has remained healthy, particularly for larger size TVs, which require more LEDs to backlight them. According to IHS, the average TV panel size exceeded 40 inches for the first time ever in 2016, and the firm predicts another 7 percent increase in panel size this year."

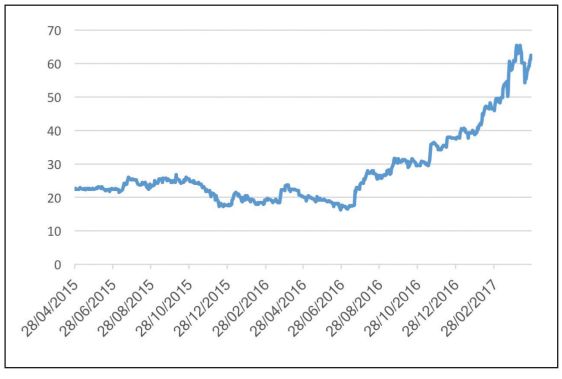
Peeler also discussed the growing market for fine-pitch digital signage, which is also known as direct view displays. In these products, an LED forms each pixel, with its size dictating the minimum viewing distance for an optimal image. "For the past few years, the recommended viewing distance was something greater than 40 feet; however, with the advent of fine-pitch LEDs, that distance is now only about 8 feet."

This reduction in viewing distance has driven a dramatic increase in the deployment of these screens. "We're seeing increased use in stadiums, lobbies, and retail stores," said Peeler. To meet increased demand, customers need to produce more devices, and this has led Veeco to witness increased MOCVD demand for its tools.

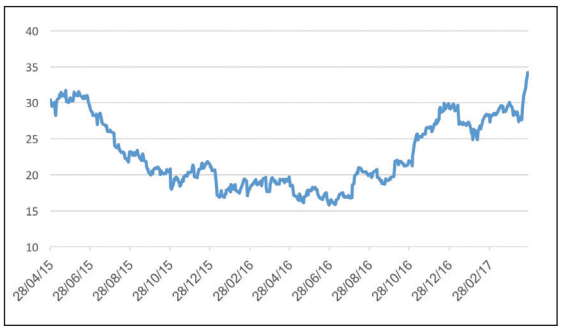
For quarter one sales, the company made a loss of $1.1 million, but gross margins are expected to improve once the company has completed renovating its New Jersey facility to combine manufacturing operations for ion beam, optical, and other components. Veeco expects revenue for the next quarter to be in the range $85 million to $100 million, and for the full year it expects the bottom line to lie between a profit of $3.6 million and loss of $2 million.

Infinera's issues

Footing this year's table is Infinera, the maker of InP photonic integrated circuits that are used in its systems for optical and data communication. In the twelve months up to 28 April 2017, its share price fell by almost 17 percent, a reflection of its declining



IQE's share price has rocketed since autumn 2016.



Veeco's share price has more than recovered from the fall it took during 2015 and early 2016.

sales. Revenue for the first fiscal quarter of 2017 was $176 million, down $5.5 million sequentially, and a fall of $69.3 million compared to the equivalent quarter of 2016. In conjunction with the falling revenue, there has been a reduction in gross margin: for the latest quarter it is 40.3 percent, compared to 41.8 percent for the previous quarter, and 50.2 percent for the equivalent quarter of 2016.

Speaking to investors on 4 May, 2017, in an earnings call for the first fiscal quarter of this year, Infinera CFO Brad Feller spoke about the tough market conditions for this sector, and explained that the relatively low gross margin was due to ongoing pricing conditions. He argued that there is a need to invest, in order to preserve existing business ahead of the delivery of new products. "In addition, we continue to be negatively impacted by the reduced volumes within our manufacturing infrastructure."

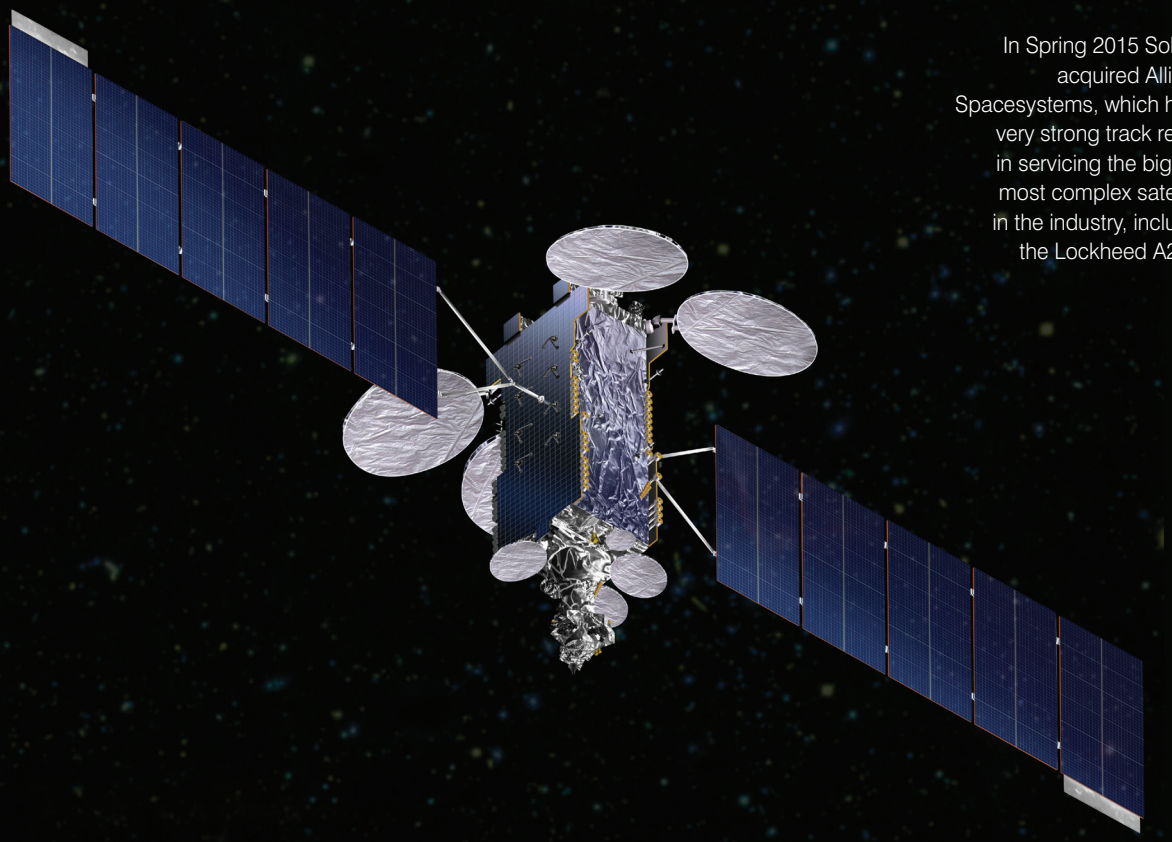
In the next few quarters Infinera will launch many products. "Pent-up customer demand suggests that our new products are well suited to address evolving architectures that require the most scalable and cost-efficient networks," commented CEO Thomas Fallon during the call.

Products coming out in the third quarter include the XT-3300 for long-haul and metro, the XTM Series with a 400-gig module for metro, and the XTS-3300 for the subsea market.

Although Infinera's management are upbeat about the future, they know that a return to profitability will take some time. "We won't start to see margin recovery until our new products gain traction in the market, which should enable us to realize cost structure benefits and to re-establish fixed cost leverage from our vertical integration model," explained Feller.

If Infinera starts to turn the corner, its share price will climb, and it could go up the leaderboard next year. Currently the top three spots are occupied by firms that support the production of chips, but are not device makers. Will that be the case in 12 months' time?

Disclaimer: Richard Stevenson own a small number of shares in IQE.



In Spring 2015 SolAero acquired Alliance Spacesystems, which had a very strong track record in servicing the biggest, most complex satellites in the industry, including the Lockheed A2100.

SolAero:

Mastering Vertical Integration

Acquisitions and investment enhance SolAero's capabilities in solar power technologies for satellites.

BY RICHARD STEVENSON

WITHIN OUR INDUSTRY, several firms are vertically integrated. They include: Sony, a maker of GaN lasers that are used in its BluRay players; Samsung, a producer of LEDs that are incorporated into its TVs; and Infinera, a leading player within the optical communications market that produces systems based on photonic integrated circuits.

These three outfits were always vertically integrated. But that's not the only path that can be taken – there are some companies that started off as chipmakers, and have now diversified. They include Cree, a pioneer of the LED that now manufacturers light bulbs; and SolAero, a firm formed in late 2014 through the sale of Emcore's solar power business, that has recently expanded its capabilities through acquisitions and investment.

It is easy to label any firm operating within the compound semiconductor industry as either vertically integrated or not – and even judge them on this basis. But that's folly. What matters is how successful a company is. If it is vertically integrated, its performance will hinge on how well its parts fit together, and how the resultant entity can support the market it serves.

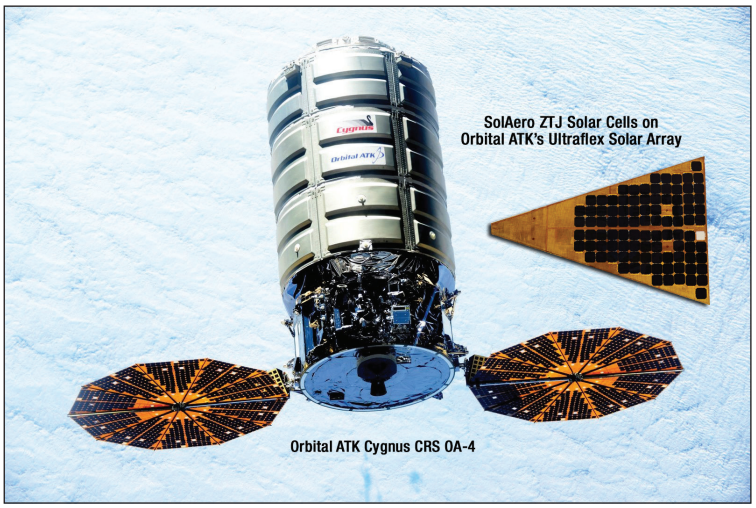
In today's satellite and aerospace market, there is a good case to be made for vertical integration. "With a change in focus from the traditional, large GEO telecom satellites to lower orbit constellations manufactured in high volume, vertical integration gives us an opportunity to realize economies of scale that will benefit our customers," explains SolAero President and CEO, Brad Clevenger.

Through three acquisitions, capability has extended from the production of solar cells that sport state-of-the-art efficiencies to initially the manufacture of solar panels and finally satellite structures. "That's been important for us to go out and attack some of the opportunities in the industry," claims Clevenger, arguing that winning business can be harder when capabilities are narrower, as collaboration with other firms is then needed, possibly including coordination with prime contractors.

Acquisitions, acquisitions

SolAero's vertical integration originated in 2001 with the acquisition of the assets of TecStar, the US' first supplier of space solar cells. Back then, Emcore had been making space solar cells for just four years. Following that acquisition, Emcore's space solar power business grew to be one of the largest in the world, providing more than 300 kW of space solar power annually to satellite manufacturers around the globe.

The next big step came in the Spring of 2015 with the acquisition of Alliance Spacesystems, a maker of composite structures – these are the lightweight, carbon fibre-based frames used to build solar systems. According to Clevenger, that acquisition gave SolAero an edge over its peers that still exists today: "We are the only supplier in the world that can deliver, to customers, a satellite solar panel 100 percent integrated in house."



SolAero Technologies provided panel technology for OATK's Cygnus OA-7 mission, which launched on 18 April 2017. For the OA-7 mission, Orbital ATK used the Enhanced Cygnus Pressurized Cargo Module (PCM) to deliver cargo to the International Space Station.

The acquisition of Alliance enabled SolAero to enter new markets. Since then, it has been able to draw on Alliance's very strong track record in servicing the biggest, most complex satellites in the industry, such as Lockheed A2100s and Boeing high-power and medium-power 702 satellites. But that's not all. At the time of the acquisition, about 20 percent of Alliance's business came from sales of solar panel substrates, some of which were sent to SolAero, where the cells were integrated. Now all of this can be carried out by one company, in one location.

SolAero strengthened its business again in May 2016 via the acquisition of Vanguard Space Technologies. Although this firm also had experience building over 70 large satellite structures, the majority of its business came from its engineering expertise. This had been used to provide the likes of an instrument deck for a Mars Rover, stable optical structures, and over 100 satellite antennae reflectors. Armed with these capabilities, SolAero has enhanced the end-to-end design and manufacturing services that it can offer to its customers.

The most recent move at SolAero has been a $10 million investment at its headquarters in Albuquerque, NM. This is being used to construct

a 40,000 ft² manufacturing facility, primarily to supply solar panels for OneWeb, which has the ambitious goal of producing two-to-three satellites per day. To avoid moving parts around the country for the OneWeb contract, the technologies and knowhow at sites formerly owned by Alliance and Vanguard are being adopted in the new facility. "We can streamline the manufacturing of solar panels in a way that I don't know any other company in the world has the capability to do today," says Clevenger.

Investment in the headquarters, while retaining expertise at its sites in California, will help SolAero compete in both the traditional GEO telecom and emerging satellite markets. It is a challenging environment, so companies in this sector must evolve their business models, including considering acquisitions. "We have our eyes to the horizon, but we have a lot of work on our plates."

It's not easy to know if the owners of SolAero, Veritas Capital, are enjoying a good return on their investment because financial information is not disclosed. But, the signs are good, with major contracts being won and headcount increasing. "We were 250," says Clevenger. "We're now 375, and with OneWeb we expect that to climb – certainly over 400, but perhaps to 450 when we're in full production."

Cell advances

While SolAero's shift toward greater levels of integration has increased its technology portfolio, the most complex part remains that with which it first began – the multi-junction solar cell. Over the years, production volumes have mushroomed, which risks driving the cell toward commodity status. "It may be a fancy component, but it's a component," says Clevenger. "What customer's need, especially at the satellite level, is solutions which is why we have made the strategic moves that we have."

Despite this shift of emphasis, SolAero still prides itself on the quality and the performance of the multi-junction device. "The solar cell is still the biggest knob to manage and improve the performance of the solar array," explains Clevenger.

To improve performance, the company has commercialized an inverted metamorphic (IMM) device architecture. This trims weight by 30 percent and delivers a substantial increase in efficiency. "Production-scale sales that we are making right now – first generation IMM – are 32 percent efficient, which is about 10 percent higher relative efficiency than what state of the practice is in satellite power today." There are many benefits associated with this gain in efficiency. For a given power requirement, a panel

Test launch of the Silent Falcon. It has SolAero UAV-tunnel-junction solar cells integrated onto its wings.

can be smaller, making it lighter, more compact and cheaper to launch. What's more, its reduction in size and weight can benefit the dynamics of the satellite.

The IMM cell is relatively mature, with more than 30,000 produced, and adoption for multiple flights. However, SolAero is only half-way through qualification by the American Institute of Aeronautics and Astronautics (AIAA) standards. It could take up to another 9 months or so to win approval.

Clevenger points out that the lengthy qualification period has applied the brakes to the pace of advancement in solar cell technology, in an industry that has beome more conservative over the last 20 years. Back in the late 1990s, when Emcore broke new-ground with the launch of the first dual junction cell, the company released a new technology every 18 months and now it takes that long for qualification.

"You should only develop at no more than about half that pace – about every 3 years – or you'll never realise any return on your R&D investment, because you'll be parasitic towards you own last product," explains Clevenger. This means that it could be many years before the six-junction cell demonstrated by SolAero enters production.

Taking flight

An emerging, promising market for the company is that of providing solar power for unmanned aerial vehicles (UAVs). For this application cells need to bend to the shape of the wing, but that's not a problem. "Frankly, we have products that can bend around a pencil," says Clevenger, adding that devices developed for space can provide efficiencies of above 30 percent in high-altitude conditions.

Clevenger is willing to accept that the company's multi-junction cells might not be the best devices for some forms of UAV: "Some UAVs have a tremendous wing area, which means that high efficiency solar cells are not necessarily the right solution." But he points out that with smaller UVAs, typically requiring 100 W or less, SolAero's cells are ideal for excelling in two key areas: watts-per-kilogram and watt-per-square-metre. "We have some great partnerships on-going, and in just the past three months we have done two outstanding demonstrations of electric power of UAVs with our products.

The solar cell market for UAVs could be huge, but it presents challenges, including the supply of materials and products. "We saw that in concentrating photovoltaics, where a lot of people were worried by germanium wafer supply," says Clevenger, who is now witnessing similar concerns in the UAV sector. In his view, if sales are to take off, the whole supply chain must work hard to reduce costs, as this will hold the key to enabling the technology to flourish competitive

SolAero's headquarters are in Albuquerque, New Mexico.

market. An unanticipated benefit of SolAero's steps to greater vertical integration is that its capabilities in carbon composites are an asset in the UAV industry. "We are making aircraft parts, whether it be a fuselage or a wing," says Clevenger. "We are able to integrate the solar process, which we believe will set us apart in our capability to service the UAV industry."

Given this state of affairs, it is clear that there are many benefits associated with the mastering of vertical integration. Some of these are clear at the outset, while others emerge as new opportunities arise.

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GaN HEMTs:

The substrate conundrum

With GaN HEMTs, is the additional cost of a native substrate a price worth paying?

BY MOHAMMED ALOMARI FROM THE INSTITUTE FOR MICROELECTRONICS STUTTGART (IMS CHIPS)

SILICON, the incumbent technology for power electronics, has its limitations. They includes its failure to provide DC power conversion with near ideal efficiency in systems that combine operating at voltages in excess of 500 V with frequencies higher than 1 MHz. This is a major impediment, as such conditions are desired in many applications, including: motor drives for automotive and industrial power supplies; power units in electric vehicles (they are inserted between either the charging unit and the battery, or the battery and the motor); photovoltaic inverters; data centres; and telecom power supplies.

Fortunately, there is a compelling alternative to silicon: the GaN HEMT. It's ideal for power switching, thanks to its capability to handle high voltages and high current densities, and its fast switching speeds.Thanks to these merits, analysts are tipping this device to generate billion-dollar sales by the middle of the next decade.

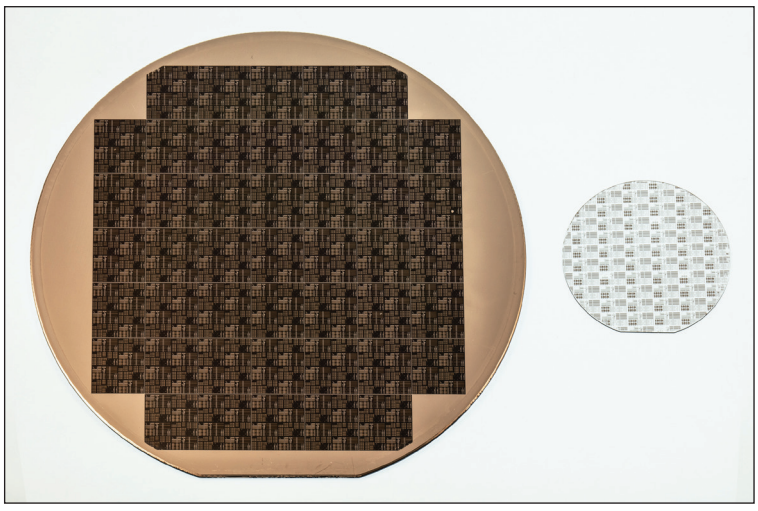

Figure 1. The 6-inch GaN-silicon wafer (left) can make GaN power devices cost effective, but reliability is attained only by using GaN-on-bulk-GaN wafers, such as the 2-inch wafer shown (right).

However, that's not to say that this device is faultless. It has downsides that are delaying its entry to market year after year. While no one doubts its attractive properties, it is not gettimg traction in markets with wide consumer bases, such as the automotive industry, even though these sectors have an urgent need for the performance it offers.

There are, in fact, two obstacles in the way of the commercial success of the GaN HEMT: its cost and its reliability.

Our team at the IMS CHIPS, has taken a close look at these issues by undertaking a very thorough investigation of the capabilities and weaknesses of the GaN HEMT. One of the key questions that we have investigated is whether this device can have more commercial success when it is formed on silicon, or on a native substrate. Read on to discover our conclusions.

Issues of cost…

If GaN HEMTs have a reputation for their high-cost, this can be traced to their production on small diameter, expensive substrates, such as SiC. Addressing this concern are large diameter silicon substrates, which are now commercially available through epiwafer suppliers. This material is of sufficient quality to enable high-voltage operation, and it can be processed in already established silicon lines in a CMOS-compatible fashion (see Figure 1 for an image of a 6-inch GaN-on-silicon wafer, similar to what is now routinely processed in our CMOS-line).

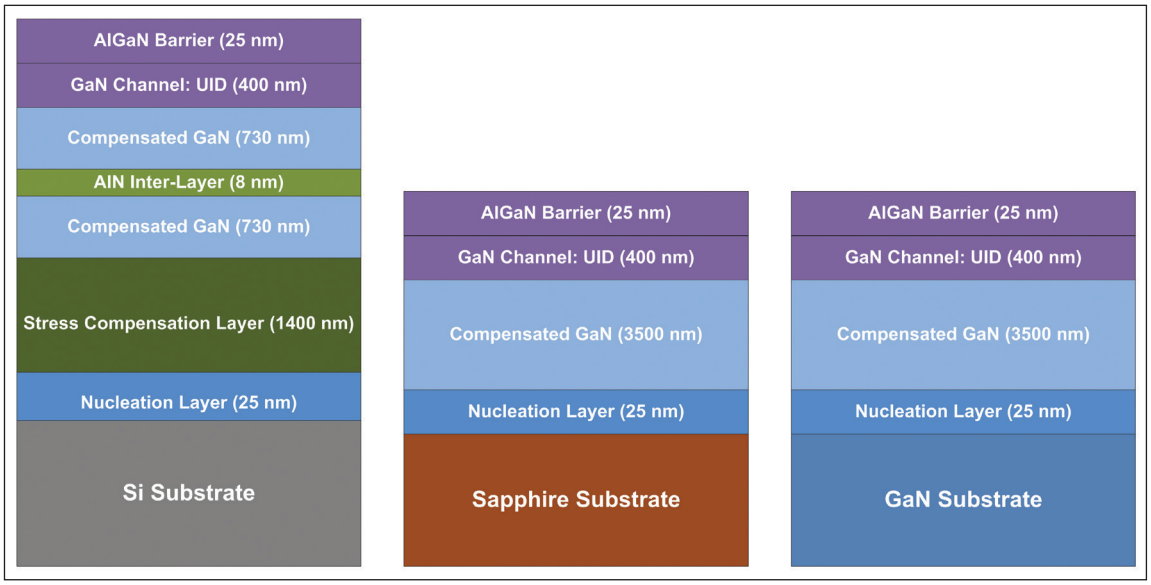

Figure 2. Many stress and compensation layers are needed to enable the production of high-voltage GaN HEMTs on silicon substrates. The epitaxial complexity is much reduced with sapphire and bulk GaN substrates.

Anyone using this approach slashes the cost of single die, because GaN can be processed side-by-side with CMOS silicon. No major investment in a separate GaN line is needed.

However, even with these advances, GaN HEMTs are pricey. The cost of the bare wafer ranges from € 2000 to € 5000, due primarily to the cost of GaN epitaxy. Growing GaN on silicon is not easy, with a multi-layer stack needed to mitigate the thermal and lattice mismatch between cubic silicon and hexagonal GaN (as depicted in Figure 2). What's more, a relatively thick compensated isolation buffer layer is needed to shield the high voltage from the conductive silicon substrate.

Even with a carefully chosen epistructure, a GaN-on-silicon wafer suffers from high residual stress and large wafer bow. This impacts yield, because it increases the probability of wafer cracking during processing. Devices are also impaired by charge trapping and inefficient thermal dissipation. This stems from the existence of so many different layers and interfaces, and the high defect density, which is of the order of $2x10^9$ cm^{-2}.

… and reliability

Operation of the GaN HEMT hinges on a difference in the polarisation between the top layer, which is typically an AlGaN barrier, and the bottom buffer layer, typically GaN. If charges are trapped, this produces an uncontrolled and dynamic imbalance, and ultimately degrades device reliability. Operation of the device leads to a decrease in the channel density – often described as an increase in the dynamic on-resistance – and an accumulated increase in leakage current, which causes unpredictable device behaviour. There are implications of this decline in performance for the surrounding control electronics. The worst case scenario is a sudden, catastrophic device or circuit failure.

So, in short, GaN-on-silicon has the potential to be highly cost-effective – but it also has some serious flaws, in terms of reliability and thermal management.

For our investigation, we could have taken into account the limitations of the GaN-on-silicon wafers while estimating yield and final die cost. But this is far from easy, partly because there are no strict epiwafer standards. What happens in practice is that different suppliers take different approaches, depending on their choices for epitaxial equipment and silicon substrates, to produce epiwafers with the same design.

To enable standardization of the epitaxial process, there is a need for a statistical approach that correlates the general causes for defect generation to the growth technology. This is the track that we are pursuing in partnership with leading reliability and modelling partners. GaN-on-silicon wafers from different wafer suppliers are characterized structurally and electrically, with the statistical results correlated with the common epitaxial steps employed by each supplier.

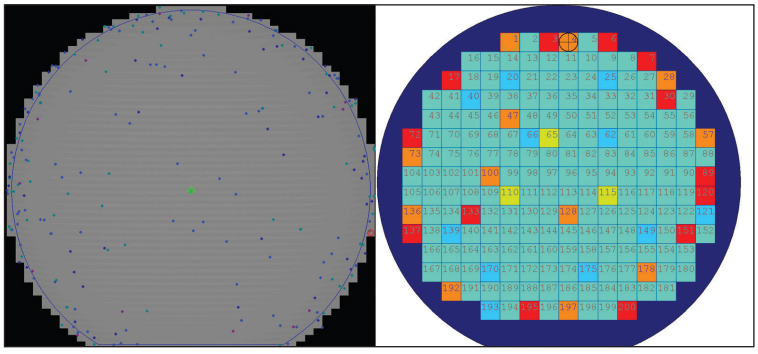

Figure 3. Defect mapping on a commercial GaN-on-silicon wafer (left), and the resulting device performance wafer map (right). Here the red marked dies totally failed, while some are below the designed specification. However, most of the die pass the test criteria (blue coloured die).

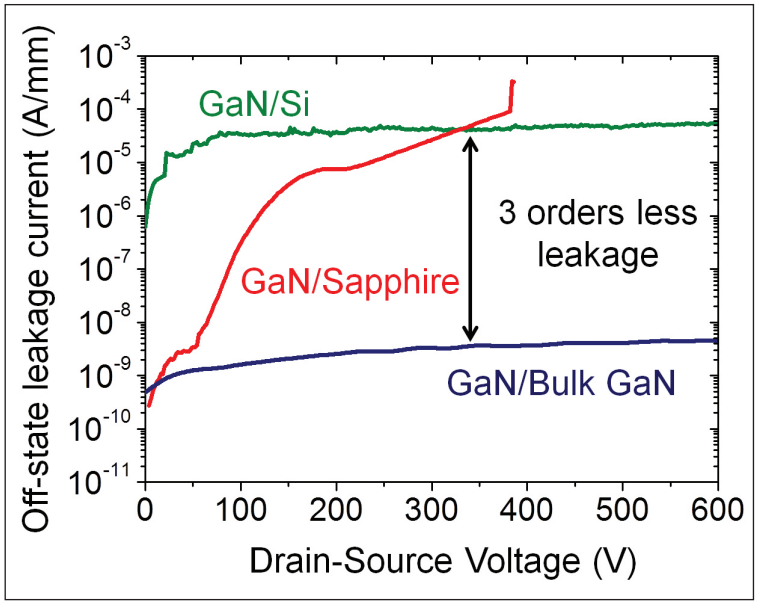

Figure 4. GaN-on-bulk-GaN HEMTs show inherently lower leakage than those based on GaN-on-silicon and GaN-on-sapphire.

We process our wafers with our 'fast loop GaN process'. It forms GaN devices using the fewest and least interfering fabrication steps – that is, without inducing any degradation to the material quality during device processing. Although this approach is not capable of producing as a complex structure as a CMOS-based process, it is the best choice for material characterization purposes. That's because it provides fast, comprehensive analysis of the wafer's quality to the wafer supplier. The turnaround time is between two and four weeks, depending on the extensiveness of characterization and reporting.

The characterization that we can provide ranges from DC measurements to reliability analysis. This can be undertaken on full or partial wafers.

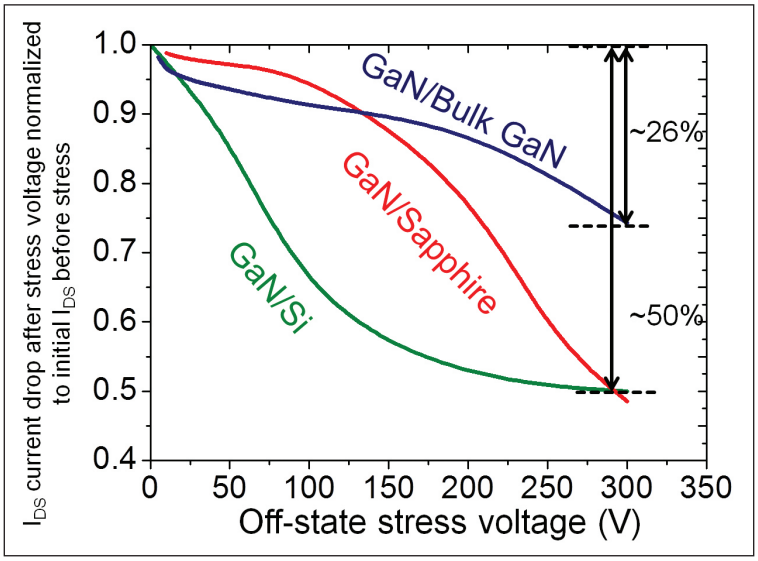

Figure 5. GaN-on-silicon HEMTs suffer from stronger charge trapping effects than those formed on bulk GaN.

An example of our work is obtaining a defect map on an unprocessed, 6-inch, GaN-on-silicon wafer (see Figure 3). Using our fast-loop process, we can quickly correlate the electrical results to the physical state of the wafer. Adopting this approach in a wider and statistical manner should enable a common consensus on the most suitable way forward for epitaxy.

It is clear that exploitation of the lower costs associated with GaN-on-silicon hinges on greater standardisation of these epiwafers, and a more thorough investigation of approaches that can mitigate the reliability issues arising from epitaxy. However, if the reliability issue is to be fundamentally solved, defects and trapping centres will have to be eliminated – and this appears to only be possible by switching to homo-epitaxy of GaN HEMTs, using insulating bulk GaN substrates.

There are many merits associated with the use of native substrates: there is no need for stress relief and compensation layers; and the defect density plummets, falling from either 2 x 10^9 cm^{-2} for a commercially available GaN-on-silicon wafer, or 9 x 10^8 cm^{-2} for GaN grown on sapphire, to less than 1 x 10^6 cm^{-2}.

To highlight the improvements in reliability that stem from a switch from a foreign substrate to a native one, we have characterised GaN-on-GaN, GaN-on-silicon and GaN-on-sapphire wafers using our fast loop process. Note that although compensation layers are not needed for GaN-on-sapphire and GaN-on-GaN, they were added to enable direct correlation of reliability and defect density. The benefits of a lower defect density on reliability are abundantly clear, with leakage current falling by three orders of magnitude when a foreign substrate is replaced with a native one (see Figure 4 that shows plots of the evolution of the leakage current with voltage, when the device is in the off-state.).

By monitoring the device current immediately after the off-state, it is possible to infer trapping effects due to defects. We have investigated this, conducting measurements after different off-state voltages (see Figure 5). This shows that regardless of substrate, trapping increases with the off-state voltage. However, the extent of this trapping varies, with GaN-on-GaN devices the least affected, and those with silicon and sapphire foundations loosing almost half their on-state current. For GaN-on-GaN devices, most of the trapping is in the compensation layer. As stated already, this is not needed, and without it trapping should be greatly reduced.

When the device is on, it is conducting current. This causes it to self-heat, and the longer it is on, the greater the reduction in current (see Figure 6).

Armed with a native substrate, the GaN HEMT is relatively immune from self-heating effects. Thermal effects are far worse when this transistor is grown

on sapphire, because this substrate has a poor thermal conductivity, hampering thermal dissipation. At first glance, silicon should be a good choice, due to a thermal conductivity that exceeds that of GaN. However, with this pairing, thermal power dissipation is held back by highly defective nucleation and compensation multi-layers.

So, judged in terms of reliability, the best foundation for the GaN HEMT is a bulk GaN substrate. But when this is viewed from a commercial perspective, it has some major drawbacks: it is pricey, small in size, and there is limited availability of the insulating form that is needed for high-voltage devices.

Two options for manufacturing bulk GaN are ammonothermal growth and HVPE. The former yields the best quality material, which is semi-insulating. However, crystal growth conditions are difficult to control, leading to substrates that are too expensive, too variable in quality from vendor to vendor, and limited to a diameter of up to 2-inch. What's more, it appears that high-volume production is not yet possible.

Many of these issues are addressed with the HVPE approach. It involves the growth of GaN on sapphire until it is thick enough to yield a high-quality, defect-free layer. At that point, the layer is removed from sapphire. Substrates are then formed, with processing producing high-quality surfaces.

Thanks to growth rates as high as 200 μm/hour – this is seven times that of the ammonothermal approach – several substrate manufacturers are using this approach. Their products are offered in various grades, in terms of crystalline quality and insulation, and although this method requires separation and finishing steps, the size of the substrate is limited only by the size of the carrier sapphire wafer. This form of substrate, which we have used in our investigation, is employed for the manufacture of blue lasers and ultra-high-power LEDs. If this optoelectronics sector continues to grow, availability of such wafers should increase, leading to a reduction in their cost.

Today, the manufacturers of GaN HEMTs have to choose between a lower-cost substrate that compromises reliability, and one that yields a better, but more expensive device. One implication of this is that for the next few years, GaN-on-silicon HEMTs may only enjoy commercial success in applications where the operating voltage is far below the capability of GaN, because this reduces reliability issues. Meanwhile, HEMTs produced on a native substrate can demonstrate the full capability of this device in power applications, where they will enable highly efficient, compact size power electronics. However, due to the high cost of these transistors, they will only serve in niche applications.

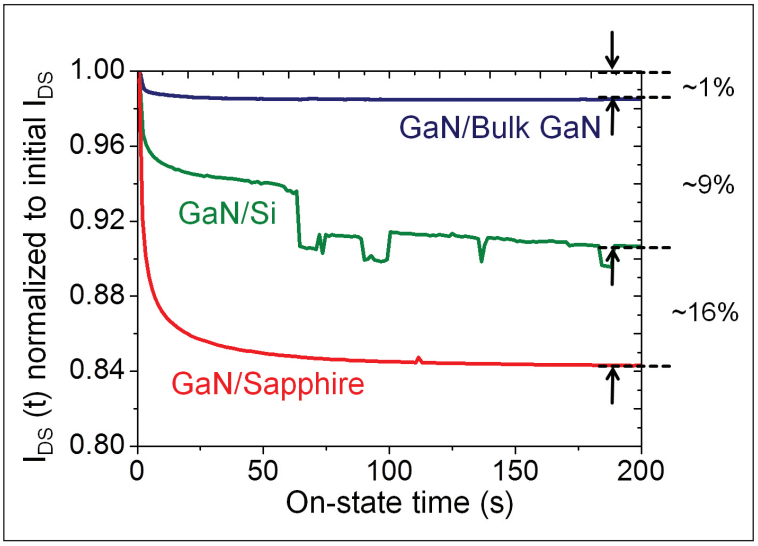

Figure 6. The thermal dissipation capability of the bulk GaN substrate allows much reduced self-heating. Although silicon has a higher thermal conductivity than GaN, the multi-layers needed for stress compensation act as a thermal bottle neck.

Ideally, this state-of-affairs will change when larger, lower-cost bulk GaN substrates are available. This will not happen overnight, but while we wait, we hope for a gradual reduction in cost. This may occur through the introduction of substrate transfer methods, where the active layer of several 2-inch bulk GaN wafers is transferred to a carrier substrate, such as 8-inch silicon, and the remaining template is reconditioned and reused. We are active in this, working with a leading epitaxy partner. Together, we plan to produce material by this approach within two years, with the aim of increasing the commercial appeal of the GaN-on-GaN HEMT.

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siconnex
customized solutions

Wet BATCHSPRAY power device manufacturing

As history tells us, before a solution can be found, a problem must first arise that needs to be solved. The history of Siconnex began when a power device manufacturer was faced with this challenge and since then many new applications and solutions have been enabled throughout the semiconductor industry, including power, LED, analog/mixed signal, MEMS, and many more.

Optimization of a Standard Power Process: Al(Si) – Freckle or Ti/TiN Etch and Resist Strip

One of the most common processes within the power industry is Al etch followed by barrier or freckle etch and resist strip. This process sequence opened up the door to success for Siconnex at a European customer's site 12 years ago. The main issue faced by the customer was that this process sequence requires a large number of different wet benches full of chemicals, which at that time were mainly manually operated. This procedure involved wasting huge amounts of cleanroom space, exhaust gas, chemicals, and operator time. In addition, the result was barely sufficient in terms of particles and uniformity.

In standard production conditions, nobody wants to change an existing process or system. It's good to maintain a healthy skepticism when it comes to amending processes, but the possibility for improvement will eventually be exhausted. In this case, it was the sheer number of factors which were far from the optimum level that led to the decision being made to change the process.

At this stage, Siconnex introduced the Siconnex BATCHSPRAY technology. The system used was equipped with three chemical tanks and the option of using ozone in the process. With the Siconnex BATCHSPRAY solution, all the chemicals, water, ozone, and other gases are channeled to a process chamber, where they are sprayed onto a rotating batch or batches of wafers.
This principle enhances chemical exchange significantly. Furthermore, drying can also be performed inline in the process chamber. With this solution, the customer combined the whole process sequence into one system with a 2.2 m^2 footprint and on a dry in–dry out basis.

As a further benefit, uniformity dropped to below 2% as a result of the high chemical exchange. This was achieved for "within wafer," "wafer to wafer," and even "batch to batch" uniformity thanks to the in-situ, automated end point detection system.

Throughput saw a significant improvement too once the whole sequence was processed without interruption and intermediate drying. With operators not having to carry the wafers from one wet bench to another, the throughput was more than doubled.

One of the most important benefits was the use of ozone, which made it possible to replace the solvent chemical entirely. This is a huge benefit in terms of cost, since only O_2 is needed to generate O_3. Additionally, this is an advantage for the operators. Since most solvents are hazardous chemicals and replacing them with what is basically air leads to a much better working environment.

When all the benefits of this optimized process technology are summarized together, the real cost-saving potential is revealed:
Combination of four processes:

- Al etch
- Freckle etch
- Ti/TiN etch
- Resist strip (up to five processes are possible in total)
- Simultaneous processing of 50 wafers
- Average process: 45 min
- Average throughput: 67 wph

Siconnex Batchspray® Acid

- Uniformity: <2%
- No solvent required
- Dry-to-dry process

Taking all of this into account, the typical time for return on investment (ROI) is close to one year, depending on the existing process.

This process with the Siconnex BATCHSPRAY technology has been implemented at 16 plants around the world and continues to be in high demand among existing and new customers alike even after 12 years.

State-of-the-Art Technology, Processing of SiC, and GaN for High-End Technology

One of the changing factors within the power device industry is the wafer material used. For high frequency, high power, high temperature, or low leakage current, compound semiconductor substrates are used to ensure that the increasing requirements are met. The two materials most commonly in use at the moment are SiC and GaN.

For these materials, Siconnex has developed, and is still developing, processes so as to put itself in a position to provide state-of-the-art equipment. The focus of these investigations is to provide cleaning technologies for new materials, as well as the possibility to perform uniform etching.

300 mm Semiconductor Manufacturing

Although the current power market is focused predominantly on 200 mm or below, Siconnex is already one step ahead, providing its BATCHSPRAY platform–fully automated and ready for full integration in state-of-the-art 300 mm fabrication plants–for all semiconductor sectors.

In this case, two BATCHSPRAY process chambers share one robot. Each chamber is able to process 25 wafers with a diameter of 300 mm simultaneously.

Siconnex Batchspray® Acid

The results for 300 mm wafers are the same as or even better than the results achieved for 200 mm, meaning that uniformity values below 2% are standard. The Siconnex BATCHSPRAY system is the method of choice for high-volume, low-cost production.

Future Challenges

Siconnex is looking forward as technology progresses, seeing every challenge as a possibility to provide the ideal solution. A future step within the power sector is going to be keeping an eye on the evolution of emerging materials like AlN, diamond or Ga_2O_3 and developing the solutions the industry needs. Besides the power sector, Siconnex also provides solutions for markets such as LED, MEMS, analog/mixed signal, and many more.

Our goal is to replace wet benches with the Siconnex BATCHSPRAY technology to help our customers save resources and money, while also achieving better process results. For this reason, Siconnex is constantly looking into new applications within existing and new markets. In the Siconnex laboratory, new processes are developed and existing processes continually optimized.

The Siconnex equipment development team works closely with the process team to guarantee that the rising demands placed on Siconnex systems are fulfilled and that our systems are at the cutting edge of technology.

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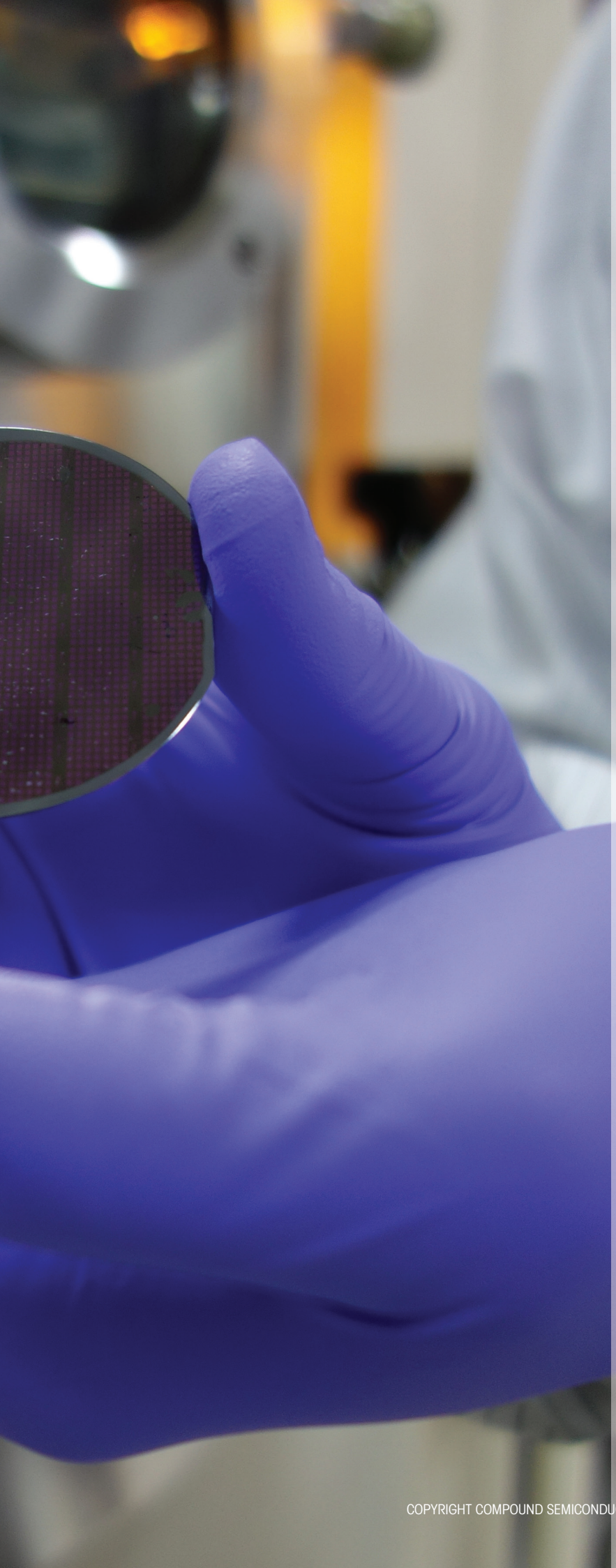
"The use of ozone made it possible to replace the solvent chemical entirely."

The third dimension:

The logical step for III-Vs

Wafer bonding and substrate re-use offer a route to making a InGaAs-on-insulator MOSFET architecture that could slash power consumption while increasing transistor density via vertical stacking

BY SANGHYEON KIM, SEONGKWANG KIM AND HYUNG-JUN KIM FROM KOREA INSTITUTE OF SCIENCE AND TECHNOLOGY



TRADITIONALLY, one of the benefits of trimming the size of the silicon transistor has been a cut in the power it consumes. But that's no longer the case, and due to this, there is a great deal of concern over how to handle the power consumed by the transistor, and also the interconnects.

To try and address these issues, researchers in industry and academia have been developing transistors with high mobility channels made from III-Vs, such as InGaAs, GaSb; and also germanium. Turning to these materials allows electrons and holes to zip along at far faster speeds than they would do in silicon, increasing the drive current. Thanks to this, is possible to reduce the voltage supplied to the transistor and ultimately its power consumption.

However, that's not the only lever to pull to cut power consumption. In addition, transistors can be stacked vertically and monolithically, an approach called monolithic 3D (M3D). Switching to this architecture shortens the length of interconnects, cutting delay and power loss; and it increases transistor density, allowing ultimate power scaling. What's more, the M3D architecture enables functional scaling, because it allows the integration of non-digital components, such as RF devices and sensors.

One of the biggest challenges currently facing silicon-based M3D technology is associated with the incompatible process temperatures (see Figure 1). A low-temperature process is essential for fabricating the top transistors, but current CMOS technology requires a high process temperature, typically 1000-1100 °C. This is hot enough to melt the interconnect metal above the bottom transistor and severely degrade the performance of the bottom transistor – it is formerly fabricated prior to the production of the top transistor. Due to this severe thermal budget constraint, undertaking M3D integration with conventional silicon technology is very difficult.

Keeping cool with III-Vs

With III-Vs this problem is avoided. Transistors with these channel materials have a process temperature that is typically below 400 °C, which is low enough to prevent damage to bottom transistors and interconnect metallization.

Recently, there have been many reports of high-performance InGaAs-on-insulator MOSFETs. These devices are highly scalable, and they have a very straightforward device structure, which makes them promising candidates for M3Ds. However, there is a stumbling block: an exorbitant increase in cost compared with that for silicon processing. From a

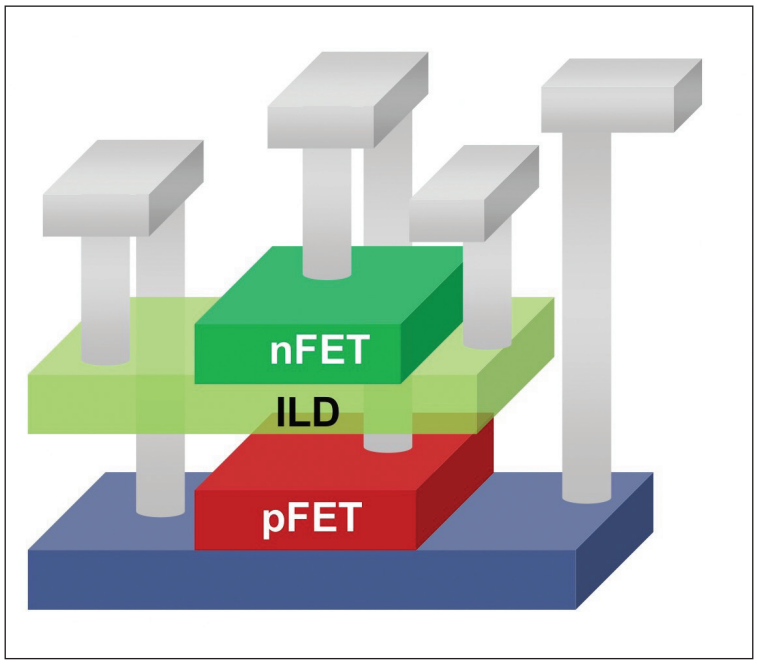


Figure. 1 Monolithic 3D integration in silicon is challenging, due to incompatible process temperatures. This issue can be overcome by turning to III-V semiconductors.

manufacturing perspective, this outweighs all the benefits associated with using InGaAs.

To address this shortcoming, our team at the Korea Institute of Science and Technology (KIST) in Seoul has recently developed cost-effective processes for fabricating InGaAs-on-insulator substrates, and using them to make high-performance MOSFETs. At the heart of our technology are the direct wafer bonding and epitaxial lift-off techniques used to form InGaAs layers on silicon substrates (see Figure 2). A key advantage of this process is non-destructive wafer splitting, which enables donor wafer re-use.

Device formation begins with the epitaxial growth of InGaAs active layers on InP substrates. Sandwiched between the active layers and the substrate is an AlAs sacrificial layer. Controlling its thickness is crucial: it impacts layer quality, due to the lattice mismatch between InP and AlAs, and it also governs the speed of the epitaxial lift-off process. Experiments on structures with various AlAs thicknesses allowed us to determine the optimum thickness for this layer.

Our next step is to deposit a Y_2O_3 layer on the III-V epi-wafer and the silicon wafer. The former has been prepared for a speedy epitaxial lift-off with a pre-patterning process that includes enlargement of the exposed etching area. One of the keys to enhancing the speed of the epitaxial lift-off is to use a hydrophilic surface, such as InP, rather than GaAs or InGaAs. This type of surface ensures a smooth solution flow and prevents large reaction products.

Once a Y_2O_3/InGaAs/AlAs/InP and a Y_2O_3/silicon substrate have been bonded together, the resultant structure is etched in HF solution to remove the AlAs layer and yield an InGaAs-on-insulator/silicon substrate and an InP donor wafer. This process typically takes an hour, making it the fastest epitaxial lift-off technique reported so far. Following this step, the InGaAs-on-insulator wafers are used to fabricate the MOSFET, while donor substrates are re-used for further epitaxial growth, enabling significant cost reductions.

Characterising these wafers reveals the good crystal quality of our material, and its clear bonding behaviour. These attributes are seen in our transmission electron microscopy images (see Figure 3), and demonstrate the capability of our process for providing high-quality InGaAs films on insulator that are essential for M3D technology.

Forming FETs

We are the first team to ever fabricate InGaAs-on-insulator MOSFETs on a silicon substrate using direct

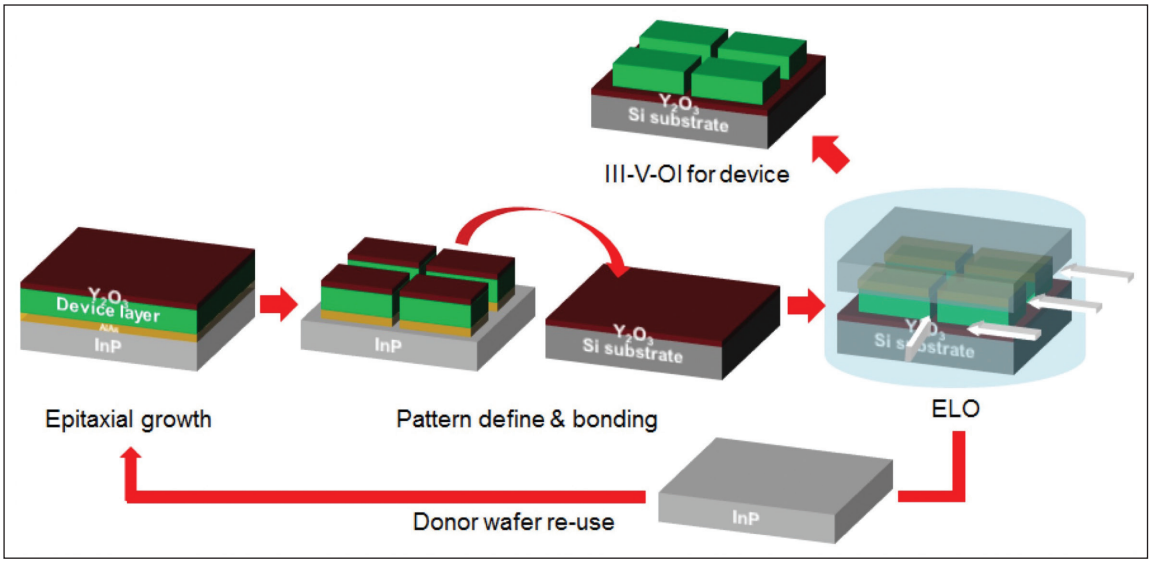


Figure 2. Researchers at KIST are processing InGaAs-on-insulator wafers by wafer bonding. This multi-chip/-wafer bonding process is applicable to wafers with diameters of 300 mm or more.

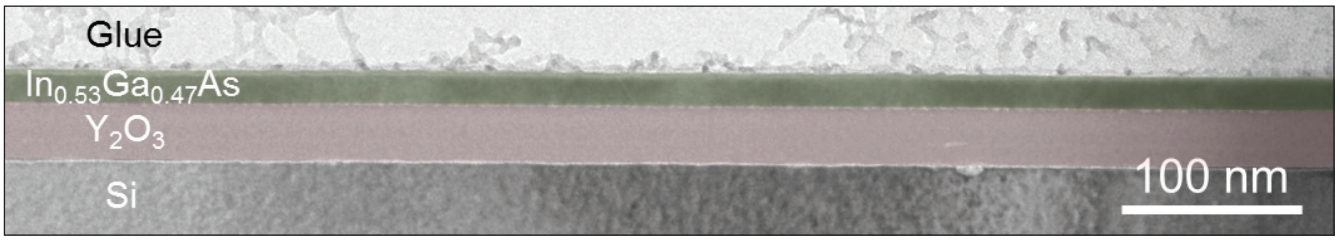


Figure 3. Cross-sectional transmission electron microscopy of InGaAs/Y_2O_3/silicon, and high-resolution images of the sample. Clear bonding behaviour is observed, with no evidence of distinguishable bonding interfaces.

wafer bonding and epitaxial lift-off. Our transistors were formed using a recessed gate structure and a Y_2O_3/InGaAs MOS interface. Ensuring the high mobility in the device is the combination of direct wafer bonding and epitaxial lift-off processes. They lead to good layer quality, and a dedicated thermal annealing that improves the MOS interface of Y_2O_3/InGaAs.

Our results are encouraging. The trap density at the MOS interface is about 5 x 10^{11} cm^{-2} eV^{-1}, which is nearly a record, and is an order of magnitude below the typical figure for a high-κ/InGaAs interface. Devices have good electrical properties, such as an on/off ratio of 10^6, a sub-threshold swing of just 120 mV/dec, and a peak mobility of approximately 2800 cm^2 V^{-1} s^{-1}, which is a record for surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs (see Figure 4).

Note that the mobility of our InGaAs-on-insulator MOSFET exceeds that of InGaAs MOSFETs on InP substrates. We believe that this superiority may stem from the high layer quality, and also the more favourable charge distribution in the channel layer. Even better results may follow, through further oxide thickness scaling, interface improvement, and the optimisation of the entire process.

Re-using the subs

The low cost of our process results from the fast epitaxial lift-off and the re-use of the donor wafers. Note that for many III-V devices, their high cost comes from the high price for the native substrate, which is much more than that for silicon.

To investigate the extent of re-usability of our InP donor wafers, we mimicked the epitaxial lift-off process by growing InGaAs and AlAs layers on InP, etching these structures in H_3PO_4-based solutions, and then undertaking re-growth. According to atomic force microscopy, the smooth surface found on a fresh InGaAs MOSFET epistructure is also present on a re-used wafer (see Figure 5 (a)). This indicates that an epi-ready InGaAs surface may be maintained after wafer re-use.

Since surface morphology is no guarantee of

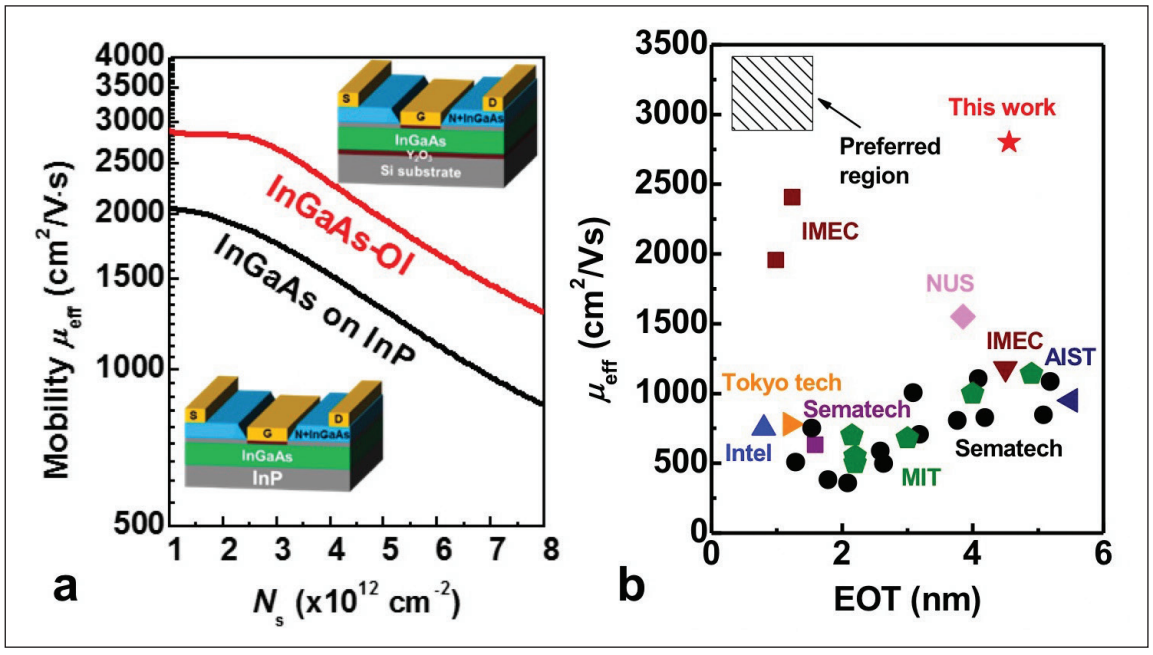


Figure 4. (a) The mobility characteristics of MOSFETs produced from InGaAs-on-insulator are very similar to those from bulk InGaAs. (b) Benchmarks of mobility as a function of equivalent oxide thickness (EOT)/ capacitance effective thickness (CET) for surface-channel, $In_{0.53}Ga_{0.47}As$ MOSFETs.

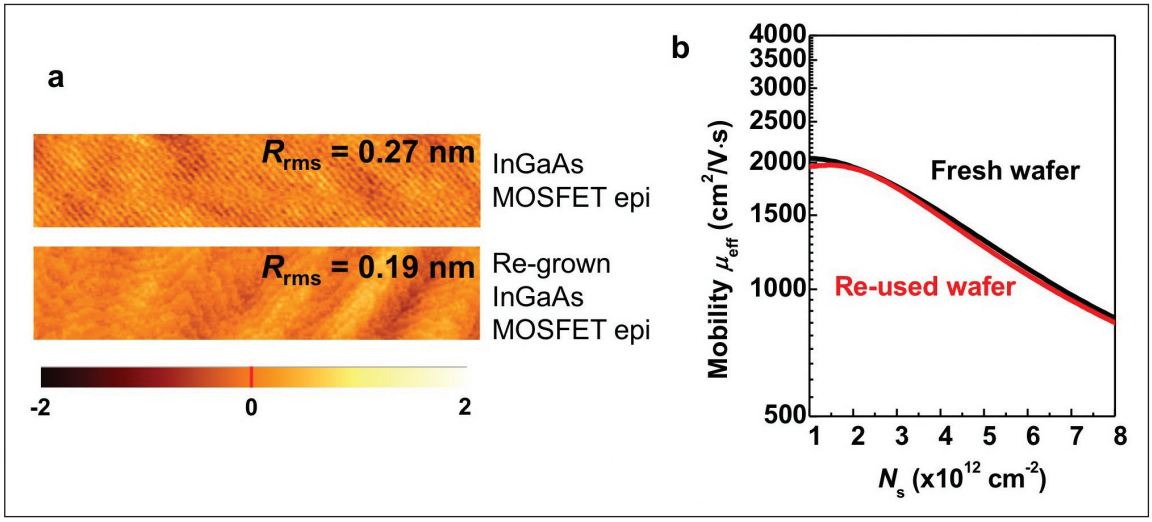


Figure. 5 (a) Atomic force microscopy of InGaAs surfaces grown on fresh and re-used InP wafers. Both surfaces have a low root-mean-square roughness. (b) The mobility characteristics of InGaAs MOSFETs on fresh and re-used substrates are very similar.

re-usability, we also compared the electrical characteristics of InGaAs MOSFETs from fresh and re-used wafers. Encouragingly, the mobility characteristics of the two types of device were almost identical, indicating that the donor wafer can be re-used after the epitaxial lift-off process (see Figure 5 (b)). This verifies our approach to slashing the cost of producing InGaAs-on-insulator transistors. The upshot is a route to: cost-effective M3D architectures that benefit from an insulation layer, which eases integration; and the production of next-generation logic circuits featuring high-quality InGaAs layers.

Our approach is one of several that can unite III-Vs with silicon. Its rivals include a wafer bonding process that involves the etch-out of donor substrates, aspect ratio trapping, and confined epitaxial layer overgrowth. Comparing all these, we believe that our technology has much to offer from a viewpoint of device engineering and cost reduction (see Table 1), while offering the opportunity to develop stacking technology that allows the integration of other classes of device, such as sensors, lasers and energy harvesters.

Further reading

S. Kim *et. al.* "Cost-effective Fabrication of $In_{0.53}Ga_{0.47}As$-on-Insulator on Si for Monolithic 3D via Novel Epitaxial Lift-Off (ELO) and Donor Wafer Re-use", IEDM, p. 616 (2016)
S. Kim *et. al.* Appl. Phys. Lett. **110** 043501 (2017)

	Wafer bonding (grown on III-V sub.)	Wafer bonding (grown on Si sub.)	Aspect ratio trapping	Confined epitaxial layer overgrowth	Wafer bonding and ELO
Wafer size > 300mm	X	●	●	●	●
Cost	High	Medium	Low	Low	Low
Growing method	III-V/ III-V sub.	III-V/thick buffer/ Si sub.	III-V/ buffer/ Si sub.	Lateral growth	III-V/ III-V sub.
Channel layer quality	●	▲	▲	●	●
Back interface control	●	●	X	X	●
SCEs control	UTB or Fin	UTB or Fin	Fin	UTB or Fin	UTB or Fin

Table 1. Benchmarking methods for integrating III-Vs and silicon.

Making a debut:

The *p*-type SiC MOSFET

Breaking new ground with SiC MOSFETs that are *p*-type, rather than *n*-type, swells the promise for the future of complementary inverters

BY JUNJIE AN, MASAKI NAMAI, MIKIKO TANABE, DAI OKAMOTO, HIROSHI YANO AND NORIYUKI IWAMURO FROM THE UNIVERSITY OF TSUKUBA

SiC is renowned for its wide band gap and large dielectric constant. These assets help SiC power devices to have the upper hand over silicon in many regards, including: a lower on-state resistance; a higher maximum operating temperature; a lower conduction loss; and a smaller increase in chip temperature during operation, thanks to the high thermal conductivity.

The weaknesses of silicon devices limit the efficiency of some circuits, and hold back the capability of others. When they are deployed in conventional inverters, they are highly problematic. In these circuits, where *p*-type and *n*-type transistors are paired together, there is the potential for a short circuit to arise from the on-state of both devices. To prevent this, engineers must ensure that the dead time, corresponding to the delay time of the gate driver circuit, is at least 1.0 μs. However, addressing that problem introduces another: a relatively high total harmonic distortion in the output AC waveforms. This is highly undesirable, because it makes it very challenging to increase switching frequency – and this is wanted, because it holds the key to smaller, lighter, more efficient inverters.

Our team at the University of Tsukuba is pioneering a new inverter architecture that reduces the dead time while addressing issues associated with a high total harmonic distortion. Our approach is a complementary inverter topology that involves SiC devices.

Initially, we considered the combination of *n*-channel SiC transistors and *p*-channel silicon transistors. However, this is far from ideal: compared to its *n*-channel counterpart, the *p*-channel silicon IGBT is not a great performer, due to its poor operating tolerances, such as its small safe-operating area. Switching to a silicon MOSFET is not a good solution, because it is held back by its low breakdown voltage and inferior thermal characteristics.

So, due to these drawbacks in *p*-type silicon, we decided to pioneer the development of a *p*-type SiC MOSFET. This device, which has a large safe-operating area, is only commercially available in the form of an *n*-type transistor. Aside from our work, there are no reports of a *p*-type variant.

Our device is a descendent of an implantation and epitaxial MOSFET developed by the National Institution of Advanced Industrial Science and Technology. It has a vertical structure (see Figure 1), and its fabrication involves *n*-channel implantation.

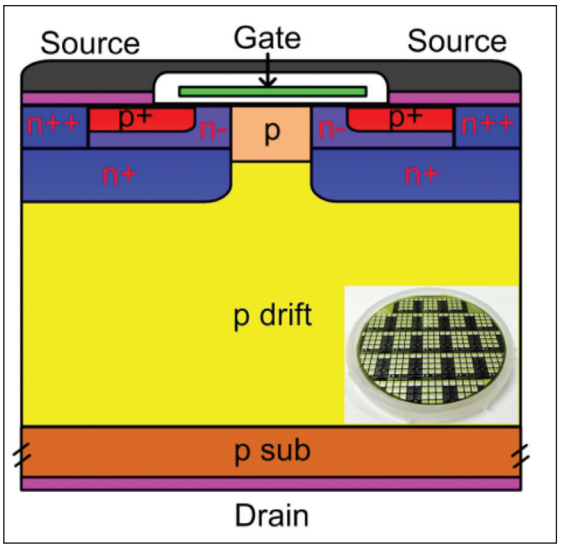


Figure 1. The cross-section of the SiC *p*-MOSFET fabricated at Tsukuba University. The inset shows the wafer of the fabricated SiC *p*-MOSFET.

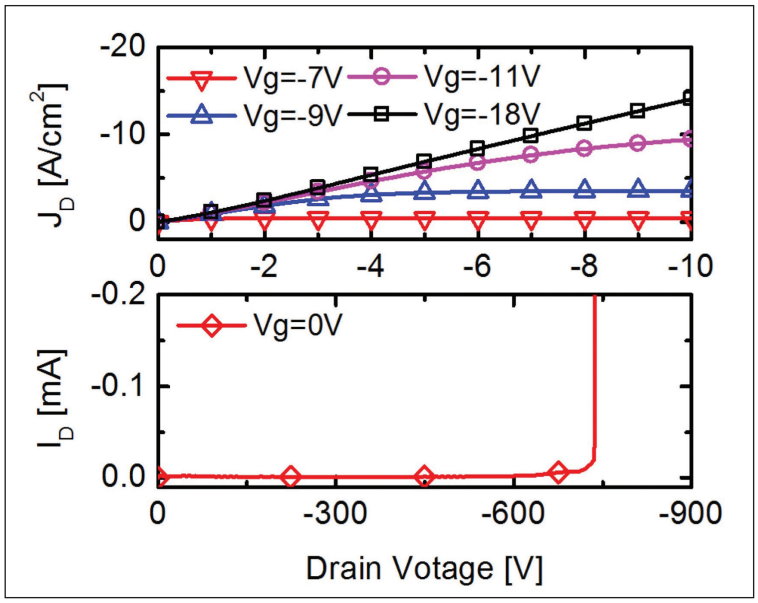


Figure 2. The typical on-state, blocking characteristics for the fabricated SiC *p*-MOSFET.

The foundation for our *p*-MOSFET is a silicon-face, *p*-type 4H-SiC substrate with the thickness of 350 μm and resistivity of 2 Ωcm. On this we deposit a 5 μm-thick drift layer with a doping concentration of 1.6×10^{16} cm^{-3}. The bottom of the *n*-channel region is formed with selective implantation of nitrogen ions at a concentration of 4×10^{18} cm^{-3}. On this surface we grow a 0.5 μm-thick *n*-channel region with doping concentration of 5×10^{15} cm^{-3}.

Our *p*-MOSFET features a JFET region, formed by selective aluminum ion implantation that reduces resistance. After adding this, the steps to complete device fabrication are: the addition of a 50 nm-thick gate oxidation layer on the surface; formation of the gate electrode, via the deposition and annealing of highly-doped polycrystalline silicon; and the creation of source and drain electrodes with a metal process. With this process we form 3 mm by 3 mm *p*-MOSFET die.

Electrical measurements on our *p*-MOSFETs reveal a typical threshold voltage of -5.32 V and a breakdown voltage in excess of -730 V (see Figure 2). A weakness of this transistor is its on-resistance, which is more than ten times that of the *n*-channel equivalent, due to the combination of a low hole mobility in the bulk and channel, the thick p^+ substrate and the conventional gate oxidation process. We are not too concerned with this high on-resistance, however, because we believe it could plummet by: adopting an advanced cell design, such as super-junction; and turning to a trench gate structure and state-of-the-art fabrication technologies.

Short-circuit strengths

We have focused on evaluating the short circuit capability of the SiC *p*-MOSFET via measurements of drain current and gate voltage as a function of short circuit withstand time. These experiments, which involved using a -300 V DC bus, show that the gate voltage can be as high as -27 V, with a short-circuit withstand time ranging from 75 μs to 90 μs (see Figure 3 (a) and (b)). Destructive failure with this testing methodology takes place at 90 μs, and the associated short circuit energy is 16.1 J cm^{-2}. Note

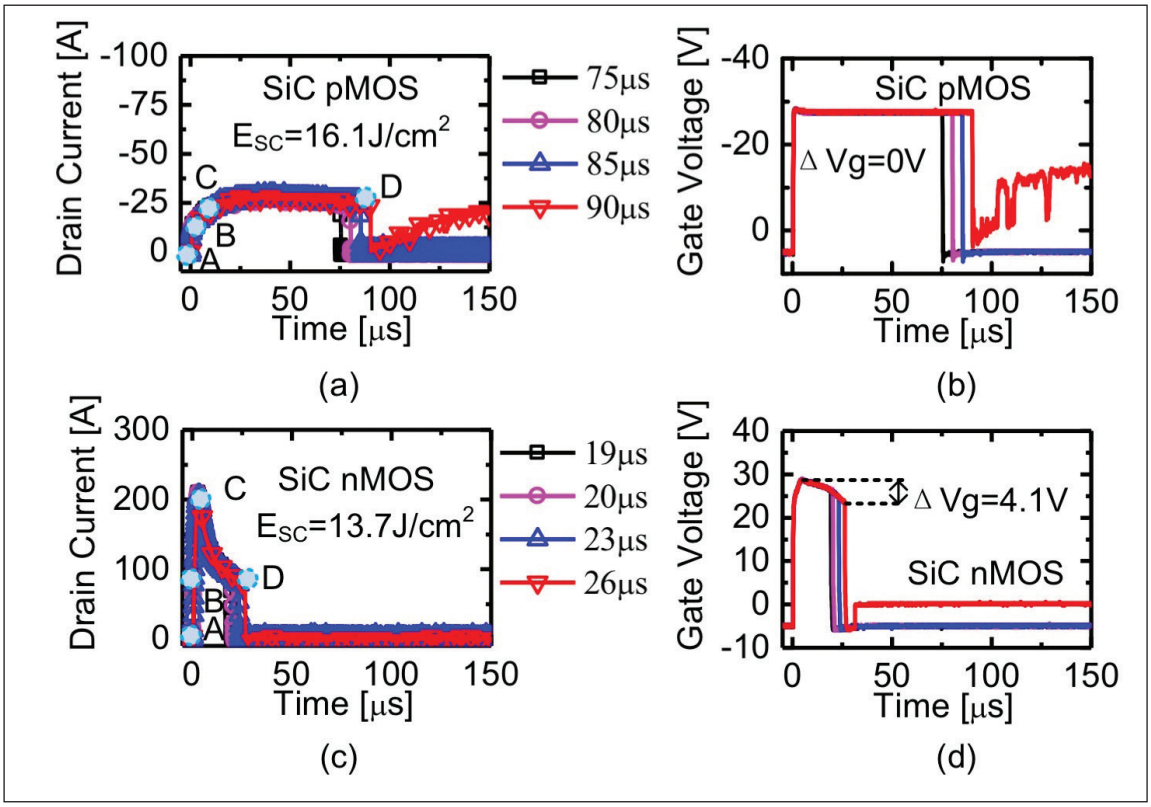


Figure 3. Experimental results of the time dependence of the drain current waveforms, and gate voltage for SiC *p*-MOSFET and SiC *n*-MOSFET, respectively.

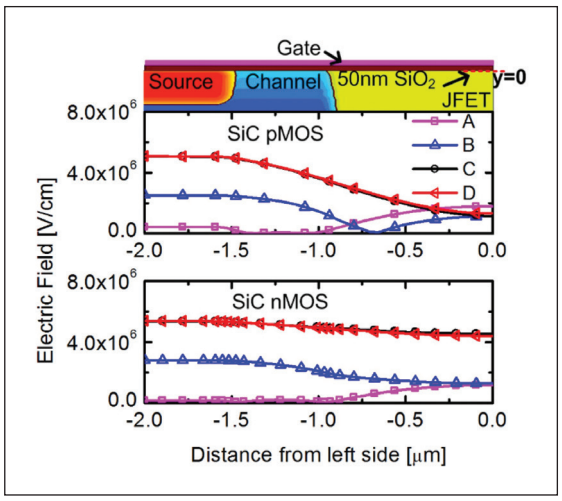


Figure 4. Simulation results of electric field profiles in the gate oxide at four points of short circuit transient in Figure 3(a) and (c) for SiC MOSFETs with gate oxidation layer of 50 nm.

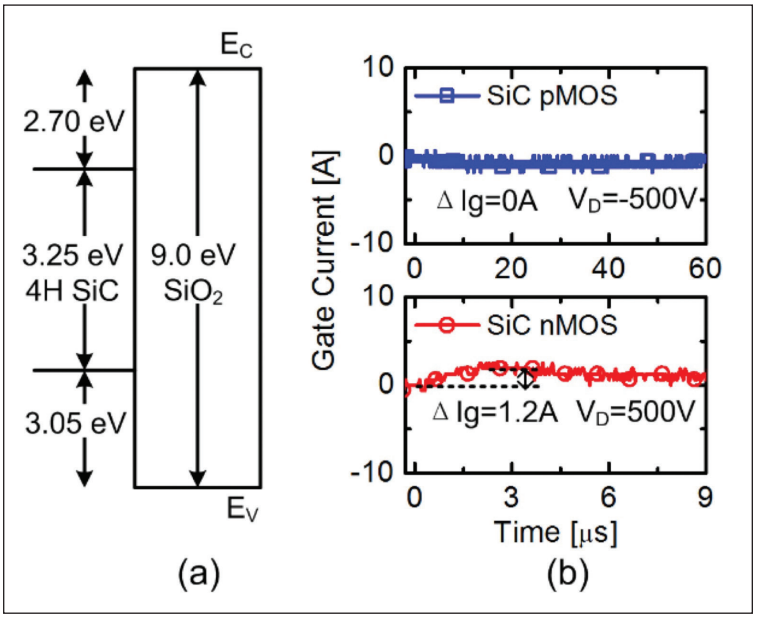


Figure 5. (a) Energy band diagrams of 4H-SiC and SiO_2 illustrating barrier heights. (b) Experimental results of gate leakage current with 500 DC bus for the fabricated SiC *p*-MOSFET and the SiC *n*-MOSFET.

that there are no signs of degradation of the gate voltage, despite an electric field as high as 5.4 MV/cm being applied to the gate oxide.

To evaluate our *p*-MOSFET, we have compared it to a SiC *n*-MOSFET with a 2.8 mm by 2.8 mm die size, a drift thickness of 8 μm, and a rated voltage of 650 V. Again, we evaluated short circuit capability with measurements of drain current and gate voltage, but this time we used a maximum short-circuit withstand time of just 26 μs (see Figure 3 (c) and (d)). With this device, the short circuit energy is just 13.7 J cm^{-2}, so approximately 85 percent of the energy for the SiC *p*-MOSFET. Our *p*-MOSFET also has the upper hand over the SiC *n*-MOSFET in gate voltage stability, with the later gradually decreasing by 4.1 V.

We have shorted the gate and source terminals in these *p*-type and *n*-type MOSFETs by applying a high electric field to the gate oxide and using an elevated junction temperature. In both devices, almost no damage or degradation is observed in the *p-n* junction, thanks to an infinite impedance between the two terminals. Even when the gate-source terminals are completely shorted, devices retain their blocking characteristic.

Simulations have enabled us to investigate the reliability of the *p-n* junction and the gate oxide during short circuit transients. Results show that when using a 300 V DC bus, the electric field in the gate oxide gradually increases until meeting its maximum value, at which point the device gradually switches from its off to its on-state (see Figure 4).

This existence of a high electric field, which will occur at a high surface temperature, highlights the need for ruggedness between the gate and source terminals. This field is to blame for the degradation in the gate voltage from 27 V to 22.9 V in the SiC *n*-MOSFET (see Figure 3 (d)). Thanks to the larger effective barrier height between SiC and SiO_2 for *p*MOS than *n*MOS devices – it is 3.05 eV, rather than 2.70 eV – our SiC *p*-MOSFET can effectively avoid degradation until it reaches the critical failure condition.

Our device also outperforms the SiC *n*-MOSFET in terms of gate leakage. Using a -500 V DC bus and considering a short-circuit transient, our device shows no gate current, while it is 1.2 A for the *n*-type device (see Figure 5). We have also investigated impactionization. Armed with data from the short circuit test results, simulations show that in both

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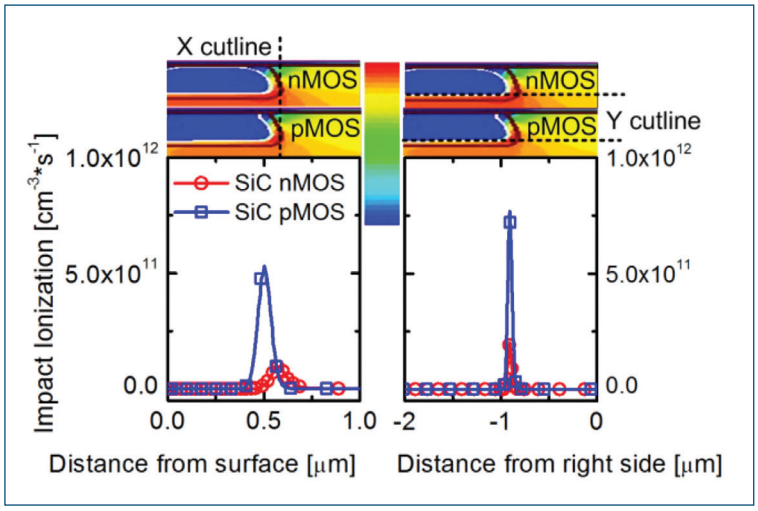


Figure 6. Simulated results of impact ionization for the SiC MOSFETs in the X and Y cutline.

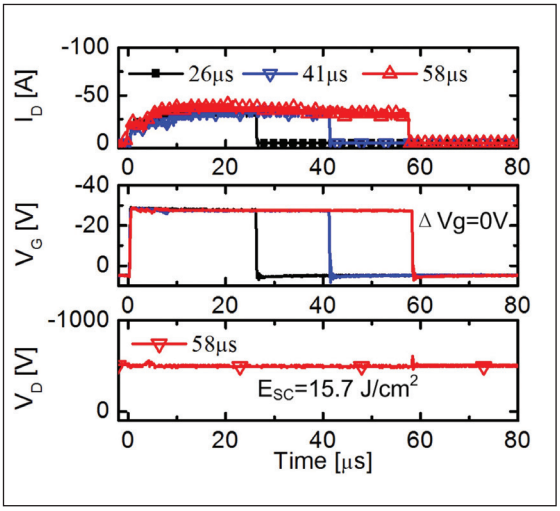


Figure 7. Experimental results of the time dependence of drain current, gate and drain voltage waveforms for a SiC *p*-MOSFET with maximum short circuit withstand time of 58 μs and -500 V DC bus.

devices impact ionization peaks at the junction corner (see Figure 6). The hole impact ionization in the SiC *p*-MOSFET is higher than the electron impact ionization in the SiC *n*-MOSFET, but its value of less than 1×10^{12} cm^{-3} s^{-1} indicates that it is too small to induce avalanche breakdown.

To confirm the avalanche immunity of our *p*-MOSFET, we have measured its short-circuit capability, using a drain voltage of -500 V (see Figure 7). This experiment shows that the device can successfully survive high avalanche conditions – the short circuit energy is 15.7 J cm^{-2}, and short circuit withstand time is 58 μs. Our measurements and simulations demonstrate that our *p*-MOSFET is capable of withstanding severe shorts circuits, thanks to the ruggedness of its *p-n* junction and gate oxide. Compared to the *n*-MOSFET, our *p*-type device delivers a 15 percent higher tolerance for the short-circuit energy, and a higher gate oxide reliability and avalanche immunity during the short-circuit test. What's more, our *p*-MOSFET promises to have a higher safe-operating area than its *n*-type sibling.

These results are very encouraging for the future of complementary inverter circuits based on pairs of SiC *p*-type and *n*-type MOSFETs.

Part of this work has been implemented under a joint research project of Tsukuba Power Electronics Constellations (TPEC).

Further reading

K. Okuda *et al*. "A dead-time minimized inverter by using complementary topology and its experimental evaluation of harmonics reduction," EPE2016-ECCE Europe, Karlsruhe, Germany, 2016.

S. Harada *et. al*. "1.8 mΩ cm^{-2}, 10 A Power MOSFET in 4H-SiC," in 2006 International Electron Devices Meeting, 2006, pp. 1-4.

Carrier lifetimes offer insight into LED droop

When droop kicks in, differential carrier lifetime decreases slowly, due to carrier leakage into the *p*-type region

SCIENTISTS at Hanyang University, Korea, have strengthened their case that phase-space filling is the origin of LED droop, the decline in device efficiency with increasing current.

For several years, this team has been arguing that phase-space filling saturates the LED's active region – and once this occurs, electrons are not consumed as efficiently, leading to an increase in non-radiative recombination, via the overflow of electrons into the *p*-type cladding.

"The significance of the current work is that we use the measurement of differential carrier lifetime to examine the saturation of the radiative recombination rate in more detail," explains Dong-Soo Shin.

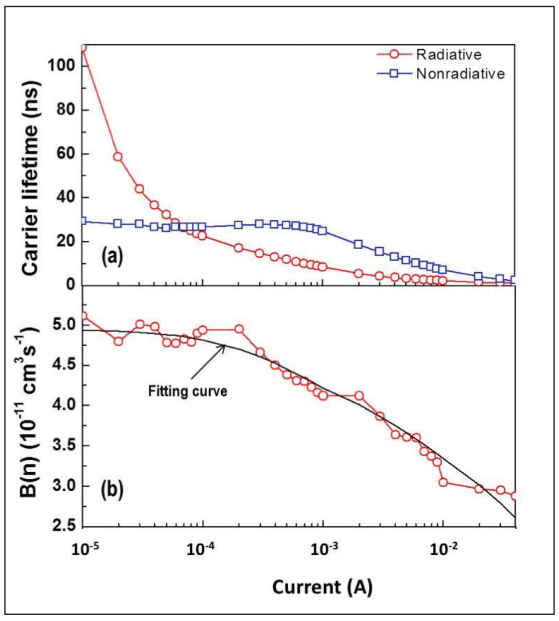
He and his co-workers measured the internal quantum efficiency of 200 μm by 800 μm LEDs at 25K and 300K, and extracted a differential carrier lifetime from an electrical measurement. The LEDs, which contain an AlGaN electron-blocking layer, have a peak internal quantum efficiency of almost 80 percent.

There are three different regimes for the LED, according to the team's semilog plot of the differential carrier lifetime as a function of current. There is the low current regime, where the internal quantum efficiency is below 50 percent, and differential carrier lifetime decreases slowly as current increases: there is the mid-current regime, where as current increases and internal quantum efficiency rapidly approaches its maximum, the differential carrier lifetime decreases rapidly; and there is the high-current regime, where differential carrier lifetime decreases slowly, and droop is observed in the internal quantum efficiency measurements.

To determine the carrier density in the active region – and gain greater insight into saturation's role in droop – the researchers undertake calculations that includes a 'B-term' that caters for the effects of phase-space filling. This approach contrasts with that of many researchers studying droop, which use a simpler term in their *ABC* rate equations.

Wang and colleagues believe that this simplification is to blame for the widespread lack of understanding of phase-space filling on LED droop. "Many theoretical works, including ones performing numerical simulations, use the constant *ABC* model," says Shin. "This has precluded many researchers from seeing the real nature of the efficiency droop."

Carrier density calculations by Shin and co-workers show that carriers cannot be consumed beyond a certain carrier density, so they leak out into the *p*-type cladding. Here, an additional radiative path is established, shortening the non-radiative carrier lifetime.



(a) Differential carrier lifetime measurements can determine radiative and non-radiative carrier lifetimes. (b) *B*(n), which is expressed as a function of carrier density in the active region to include the effects of phase-space filling, is determined from carrier lifetime analysis.

The view of Shin and colleagues differs from that of most researchers investigating droop, who argue that Auger recombination is the primary cause. Shin and co-workers question this, with an argument based on the relationship between the extent of droop and the forward voltage.

According to Shin, if Auger were the primary cause of droop, LEDs with more droop should have a higher total recombination rate in the active region – and, by implication, a decrease in forward voltage. "What we observe, on the contrary, is increased forward voltage with a higher amount of efficiency droop."

The team will continue with its work on droop, trying to understand issues such as: the role of defects in the active region; and why InGaN-based LEDs behave so differently from those made from other material systems."We believe that an efficiency droop model should explain all the observed experimental results comprehensively, not just some results only," argues Shin. "We think we are on the right track in this regard."

Reference

D. Han *et. al*. Appl. Phys. Express **10** 052101 (2017)

Perfecting the GaN Schottky barrier diode

Using a low growth rate for the drift layer produces a vertical GaN Schottky barrier diode with very high switching efficiencies

A PARTNERSHIP between researchers in Japan and China is claiming that it has produced vertical GaN Schottky barrier diodes with a very low on-resistance and a record-breaking turn-on voltage.

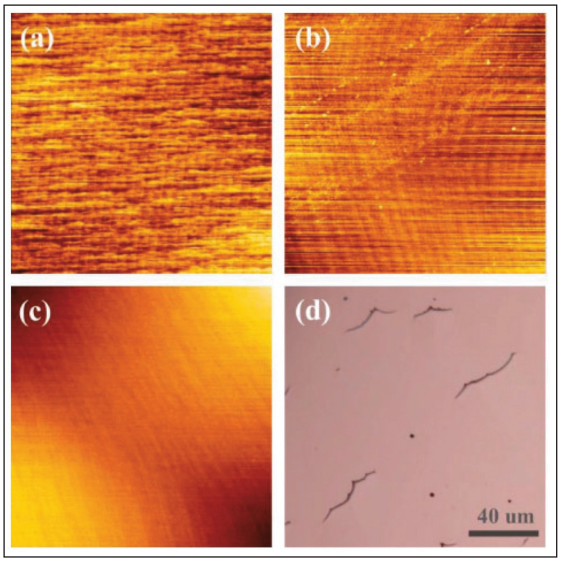
Spokesperson for the team, Linjun Wang from Shanghai University, says that the lowest on-resistance ever reported is 0.71 mΩ cm^2. "Ours is 0.72".

The combination of an incredibly small on-resistance and a turn-on voltage that is lower than ever before makes the diode produced by this team from Shanghai University and the National Institute for Materials Science in Tsukuba, Japan, a very attractive candidate for increasing efficiency in electrical circuits.

The architecture of the team's transistor is markedly different from that of many GaN HEMTs developed over the last decade. More common is a lateral geometry, which delivers a promising performance, due to a high frequency capability and a high breakdown field. However, conversion efficiency and current drive are impaired by lattice-mismatch induced dislocations and surface and interface states, which can lead to current collapse.

Vertically structures, such as the device produced by Wang and colleagues, are now receiving a great deal of attention. They can operate at high voltages and high currents; they have a very low on-resistance; and they are less impaired by surface and interface states.

Two leading options for the vertical device are the Schottky barrier diode and the *p-n* junction diode. Wang and colleagues are developing the former, because they believe it is better suited to high-power, high-frequency switching applications. That's because it's not plagued by a minority carrier issue and has a higher electron mobility. Together, these attributes have the potential for low on-resistances and low turn-on voltages.



Atomic force microscopy shows aligned atomic steps in GaN drift layers at growth rates of (a) 2.61 um/hr, (b) 4.72 um/hr, and (c) 7.78 um/hr. An optical image of the film formed at a growth rate of 8.08 um/hr reveals valley-like defects.

Wang and co-workers are claiming to break new ground by being the first to develop a device that actually delivers on this promise of combining a low on-resistance and a low turn-on voltage. Crucial to this is the realisation of a high-mobility drift layer.

To develop high-performance devices, Wang and co-workers compared the characteristics of drift layers produced with different growth conditions.

GaN substrates with a dislocation density of 4 x 10^6 cm^{-2} were used for MOCVD growth of GaN drift layers at a temperature of 950 °C. Four growth rates were used: 2.61 μm/hr, 4.72 μm/hr, 7.78 μm/hr and 8.08 μm/hr.

Formation of the Schottky barrier diode involved sputtering of a Ti/Al/Au ohmic contact on the back side of the substrate, and using electron-beam evaporation and a conventional lift-off technique to add the Ni/Au layers that create the Schottky contact.

Atomic force microscopy revealed aligned atomic steps in GaN drift layers formed with all but the very highest growth rate. That particular sample was plagued by valley-like defects.

Using current density measurements, the team extracted mobility values. The lowest growth rate produced a mobility of 1370 cm^2 V^{-1} s^{-1}, a high value that is claimed to result from reduced ionisation scattering, due to low levels of carbon incorporation.

Current-voltage measurements confirmed that lower growth rates lead to better performance. Although the use of a low growth rate for chip manufacture is not ideal, because it increases production costs, Wang believes that in their case this is not a big issue. "Our lowest growth rate, actually, is still higher than usual."

The team are now focusing on increasing the breakdown voltage of their diodes, and understanding the breakdown mechanism for this device.

Reference

B. Ren *et. al*. Appl. Phys. Express **10** 051001 (2017)

A hike in UV LED power

AlN nanophotonic structures increase LED extraction efficiency, propelling power output to more than 150 mW

A COLLABORATION between researchers at Japan's National Institute of Information and Communications (NICT) in Kobe and Tsukuba Research Laboratories has raised the bar for the output of deep UV LEDs.

The team's 265 nm device, which delivers a CW output of more than 150 mW at 850 mA, breaks the record for LEDs emitting below 280 nm. The output from this large chip with a novel architecture is 20 times that of a conventional, flat-surface LED.

Corresponding author Shin-ichiro Inoue from NICT says that the record-breaking LED, featuring an AlN nanophotonic structure that aids light extraction, can be used for air and water purification, surface disinfection, chemical and biological agent detection, lithographic microfabrication and medical diagnostics.

The two primary causes for the low output power and low external quantum efficiency of the majority of deep UV LEDs are the high dislocation densities in the AlGaN-based active layers and the extremely low light extraction efficiency from the chip.

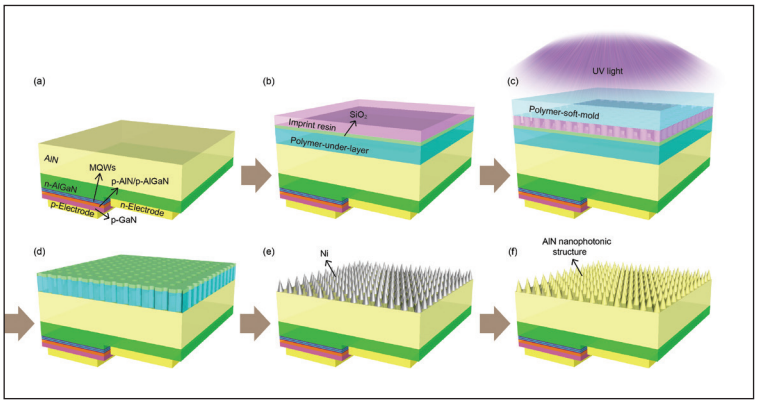
Several years ago, the team from Japan addressed the first of these concerns by switching the substrate from sapphire to AlN. Turning to this foundation led to dislocation densities of less than 10^6 cm^{-2}.

Unfortunately, AlN substrates are not a panacea. They have a much higher refractive index, which leads to a far narrower escape cone for the light and a lower extraction efficiency. What's more, there is intrinsic absorption in bulk AlN, caused by impurities.

The extent of this absorption depends on the technique used to make AlN. If it is grown by HVPE, the absorption coefficient is more than three times smaller than if it is formed by physical vapour transport.

To combine a low dislocation density with a high degree of light extraction, the researcher's deep UV LEDs contain AlN nanophotonic structures, formed on 100 μm-thick, HVPE grown AlN substrates.

A key part of the fabrication process is the use of nanoimprint lithography – it allows the team to produce large-area light extraction structures with a high-volume, high-throughput technique. Material is processed into large devices that provide uniform current spreading and allow high-current injection. Device fabrication begins with the growth, by MOCVD, of a multi-quantum well structure with an AlN electron-blocking layer. Formation of the nanophotonic structure starts with the addition of three layers to the epiwafer: a UV-curable imprint resin; a SiO_2 layer, which acts as the hard mask; and a polymer sacrificial layer. UV exposure occurs after a flexible, low cost mould is applied to the surface. Dry etching then transfers the imprinted pattern to the SiO_2 hard mask. After this, electron-beam evaporation and lift-off form a nickel hard-mask pattern, before two etching steps yield the sub-wavelength AlN nanostructures.



Formation of UV LEDs with AlN nanophotonic structures involves: (a) mesa etching and the addition on *n*- and *p*-type electrodes; (b) deposition of the polymer underlayer, a SiO_2 hard mask and an imprint resin coating; (c) application of soft UV nanoimprint lithography; (d) plasma etching of the SiO_2 and polymer; (e) nickel deposition and lift-off; and (f) AlN dry and wet etching.

The 0.35 mm^2 LEDs formed with this process feature a triangular lattice of circular AlN cones with an aspect ratio of 1.0 and a lattice constant of 600 nm. The fill factor at the base of the cones is 0.9.

When operating the device in CW mode at room temperature, the maximum output of the device is 151 mW at a maximum operating injection current of 850 mA. In comparison, a conventional, flat-surface LED produces a peak output of 38 mW at 450 mA. Driven at 850 mA, the output from this device is below 20 mW.

Inoue says that the team will now focus on packaging their chip, which should lead to even more powerful, more efficient emission.

Reference

S. Inoue *et. al*. Appl. Phys. Lett. **110** 141106 (2017)

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VENDOR VIEW Proton Site

On-site hydrogen generation: smart choice to improve process results

Hydrogen is widely used to support a variety of industrial applications worldwide, due to its ability to meet the specific needs of high purity industrial applications, ranging from semiconductor manufacturing and epitaxy to heat treating and materials processing.

Relying heavily on hydrogen to maintain process results, many operations personnel are responsible for evaluating which gas supply method will best suit their operation. Over time, this task can become daunting, because as businesses grow, increasing amounts of hydrogen are needed to satisfy elevated levels of production demand. This spike in hydrogen usage has translated into a collection of issues for facility operation.

Hassles such as inefficient production practices, fire permit restrictions, space limitations, increased costs, dangerous hydrogen storage and handling can make gas sourcing especially problematic.

Offering clear advantages over older, conventional methods of hydrogen supply such as delivered gas, dissociated ammonia and exo or endo gas, hydrogen generated on-site is a drier and safer alternative.

A high performance solution to suit businesses small and large, on-site gas generators satisfy demand by producing hydrogen at its point of use with no inventory of flammable or poisonous gas. Hydrogen generation systems are easy to permit, easy to install, and operate automatically.

Market data shows more and more stakeholders are making the switch to gas generators, eliminating the need for delivery and storage of hazardous gases within the industry.

With more than 2,500 systems installed in over 75 countries, Proton OnSite hydrogen generators are consistently creating value around the world. Utilizing advanced Proton Exchange Membrane (PEM) electrolysis, with a high differential pressure design, our on-site hydrogen generators produce very pure hydrogen in a safe, reliable, and cost effective package.

Our industrial customers are particularly impressed with the fact that they are able to realize rapid paybacks while dramatically improving facility safety. The on-site generators eliminate the need for stored hydrogen, while meeting the daily requirements of various industrial processes. Thus, providing an attractive return on investment for customers and improving site security, safety and personnel productivity.

Want to learn more about the ways hydrogen generation enables reducing, non-carburizing atmospheres without hydrogen or ammonia inventory? Interested in 99.9995%+ purity, -65°C dewpoint, 200+ psig hydrogen for use pure or blended? Our compact, packaged systems can do that, and then some. Improve your facility safety, minimize storage and handling, and improve your process results!

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