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China's maturing LED production



LEDs for light and communication



Advancing the GaN-on-silicon LED



Increasing SiC MOSFET voltages



Better GaN HEMTs for UHF radar



CS Clean Solutions
Improving waste gas abatement

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editorial view

by Dr Richard Stevenson, Editor

What's the best foundation for the LED?

MANY MAKING THE CASE for silicon as the finest foundation for the GaN-based LED focus on cost savings. It is not just that silicon is significantly cheaper than sapphire; growth on 200 mm silicon substrates enables low-cost processing in mature silicon fabs.

Against these strengths there are downsides stemming from the significant lattice and thermal mismatches between silicon and the nitrides. Chipmakers require sophisticated growth processes to prevent excessive strain building up in the epilayers that could cause wafers to warp, possibly to such an extent that they can't be processed in a silicon line.

Judged in the terms outlined above, many might argue that the benefits of switching to silicon are insufficient to warrant the effort required to overcome the challenges.

However, a decision based on just these factors is flawed. That's because the strengths of silicon extend far beyond those already outlined to include those that many may overlook.

For starters, considerations over the cost of the LED should not be limited to the cost of the chip, but extend to that of the package. Using silicon rather than sapphire pays dividends,



because it is compatible with wafer-level chip packaging. LEDs on sapphire cannot boast the same claim, as light leaks out from these devices. In that case, the production process is more cumbersome, involving chip dicing, transfer and binning, as well as the application of a phosphor at the chip level, rather than over an entire wafer.

Another strength of a silicon foundation is that it can lead to a very high degree of wavelength uniformity. Deviations in wavelength across the wafer can be limited to just 4 nm, removing the need for chip binning.

Advantages also exist at the device level. The strain that is inevitably present in GaN-on-silicon LEDs cuts the strength of the electric field within the device, leading to superior radiative efficiency; and at the elevated temperatures, where real devices tend to operate, droop is less severe than it is in the GaN-on-sapphire LED.

I hope that all these merits of the GaN-on-silicon LED are encouraging you to discover more about its virtues. If that's the case, turn to page 24 of this issue and read the feature by Samsung Electronics on their development of these devices.

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Cree breaks LED lumens per watt record

CREE has demonstrated a single high-power LED delivering nearly 1,600 lumens at 134 lumens-per-watt (LPW) which it says has similar colour quality as an incandescent light bulb. The R&D LED performance was measured at 1587 lumens at 350mA and junction temperature of 85°C, delivering 134 LPW with a CRI $R_a > 90$ and $R_g > 90$ at 2700K CCT.

With this result, the company says it has achieved a breakthrough 25 percent increase in lumens per watt (LPW) over production LEDs of similar colour quality under operating conditions found in real-world LED lighting applications.

“Today, advancing LED technology goes beyond just increasing LPW,” said John Edmond, Cree co-founder and director of advanced optoelectronics. “Cree is also focused on improving spectral content and the efficacy of warmer colour temperatures while pursuing tremendous opportunities to increase LPW at real-world operating conditions. This R&D result continues Cree’s high power LED technology innovation and provides a path to better lighting



experiences at the lowest overall system cost.”

As an example of what Cree’s technology could achieve, a current 60W LED replacement lamp with average light quality (3000K CCT and 80 CRI) could be upgraded to incandescent-like light quality (2700K CCT, 90+ CRI & 90+ R_g) with the same light output and power consumption levels at no additional cost.

Corial unveils platform for 6-inch patterned sapphire substrates

Corial, a manufacturer of plasma etch and deposition equipment, has announced the general availability of a process for sapphire patterning (PSS) on 6-inch wafers, to be used in high-volume LED production with the fully automated Corial PS200 single-module platform. Patterned Sapphire Substrate is the standard in the LED industry to get brighter LEDs. Going back to 2009, Corial has been among the first companies to supply a stand-alone ICP system with etching processes dedicated to PSS application.

Based on a production-proven plasma technology, the new Corial PS200 is a fully automated single module platform combining the highest productivity on sapphire substrates with excellent etching performances for

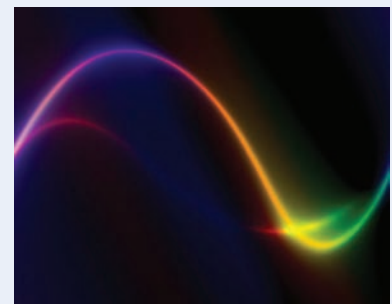
PSS application. According to Corial, key advantages of the PS200 platform include; a high density plasma source providing best in class uniformity and process repeatability; dingle wafer processing with Brooks elevator for front end cassette in vacuum load-lock and Brooks robot in vacuum transfer chamber for fully automated wafer handling; and production flexibility with extendable platform configuration (up to three process modules). Corial patterning process on 6-inch wafers has been tested and qualified by a major LED manufacturer in Asia. Typical results for PSS on 6-inch wafers are: average STD within wafer < 0.5 ; PSS height of $1800\text{nm} \pm 40\text{nm}$ and PSS width of $2800\text{nm} \pm 40\text{nm}$; $\leq \pm 1.5$ percent etching uniformity (conical shape); and a throughput ≥ 2.5 wafers/hours.

SoraaLaser presents laser diodes for lighting

SORAA LASER, a spin-off from the LED company Soraa, presented its visible laser light source technology at the Strategies in Light conference in Santa Clara, California.

“Laser diodes are droop-free, and can be combined with phosphors to safely produce highly directional output with superior delivered lumens per watt compared to other light sources,” said company co-founder the Nobel Laureate Shuji Nakamura. “Laser diodes are lighting’s future.”

SoraaLaser’s visible laser light sources are based on its proprietary and patented semi-polar GaN laser diodes, combined with advanced phosphor technology. The source is focused to a small spot on the phosphor and converted to white light, to provide highly collimated white light output.



Optical control uses miniature optics and reflectors, along with fibre optic transport and glare-free waveguide delivery, according to the company. These laser light sources are said to provide novel properties compared with other light sources by combining the benefits of solid-state illumination such as minimal power consumption and long lifetime, with the highly directional output that has been possible only with legacy technology.

These features are said to be ideal for specialty lighting applications including architectural, hospitality, retail, security, entertainment, and automotive.

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New Chair of Compound Semiconductor Centre

THE COMPOUND SEMICONDUCTOR CENTRE, a joint venture between IQE and Cardiff University has appointed Colin Whitehouse as Chair.

A world-renowned expert in advanced compound semiconductor materials, nano-devices and nanotechnology, Whitehouse brings a wealth of experience in both managing and directing research as well as the commercial exploitation of research.

Colin was, until recently, deputy chief executive of The Science and Technology Facilities Council (STFC), which is one of the UK's Research Councils. He was also Director of the STFC Daresbury Laboratory in Cheshire and was also responsible for initiating the formation of the National Science and Innovation Campuses at Daresbury and Harwell.

Whitehouse's previous roles include Board membership of Sheffield Innovations Ltd (the commercialisation arm of the University of Sheffield), STFC Innovations (STFC's very successful commercial exploitation company), the Oxfordshire Local Enterprise Partnership (LEP), STEMNET, and chair of the UK's R&D Society. He is also an elected

Fellow of the Royal Academy of Engineering, the Institute of Physics and the Institute of Materials, Mining and Mineralogy.

On his appointment, Whitehouse said: "The rapidly growing dependence on compound semiconductors that enable all key technology markets will create exciting opportunities for the recently formed Compound Semiconductor Centre (CSC), IQE and Cardiff University.

"I have been a very long-standing strong supporter of the UK building such genuinely international-class critical-mass R&D activities via high-quality collaboration. The CSC is uniquely positioned to perform the extremely important intermediate role between university-based research, particularly through Cardiff University's Institute of Compound Semiconductors (ICS), and the very recently announced CS Applications Catapult Centre, also to be based in South Wales.

"I am truly delighted therefore to become the Chair of the CSC, and am really looking forward to working closely with all of the CSC team."

Plessey boosts LED production with AIX G5+C

AIXTRON, a provider of deposition equipment, has announced that Plessey Semiconductors has ordered an AIX G5+ C cluster system for the production capacity expansion of GaN LEDs manufactured on silicon wafers (GaN-on-Silicon). The tool is scheduled for delivery in the third quarter 2016.

The AIX G5+ C cluster for Plessey consists of two multi-wafer AIX G5+ reactors which are supplemented by Aixtron's next generation cassette-to-cassette handler for large-scale, fully automated epitaxy production. Plessey purchased the Aixtron planetary system mainly for the expansion of its 150 mm GaN-on-Silicon wafer production but also works towards 200 mm production qualification mid-term as Aixtron's G5+ system enables the processing of eight 150 mm wafers or five 200 mm wafers at the same time.

Mike Snaith, operations director at Plessey, said: "We are now moving from proof of capability for our GaN-on-Silicon LED products into a capacity expansion phase. In the meantime, we have built significant demand for a range of our LED products. We have decided to purchase Aixtron's latest planetary system as the AIX G5+ C combines outstanding on-wafer uniformity and run-to-run performance at lowest cost of ownership - aspects that are crucial for efficient high-volume GaN-on-Si production."

Frank Schulte, VP Aixtron Europe, comments: "We have a longstanding and trustful relationship with Plessey and therefore, we are delighted by the renewed order. Our AIX G5+ C planetary system resolves the common challenges of high-yield, high-quality and high-throughput production of GaN-based materials on large-area silicon wafers through its fully automated cassette-to-cassette loader and a thermally activated gas etch of the MOCVD chamber."

US lab makes GaN CMOS FETs

HRL LABORATORIES, a US R&D lab owned by Boeing and General Motors, has announced what it believes is the first demonstration of GaN complementary metal-oxide-semiconductor (CMOS) FET technology.

The findings were published January 6, 2016, in *IEEE Electron Device Letters*. In doing so, it says it has established that the semiconductor's superior transistor performance can be harnessed in an integrated circuit.

This breakthrough paves the way for GaN to become the technology of choice for power conversion circuits that are made in silicon today.

GaN transistors have excelled in both power switching and microwave/

millimeter wave applications, but their potential for integrated power conversion has been unrealised. "Unless the fast-switching GaN power transistor is intentionally slowed down in power circuits, chip-to-chip parasitic inductance causes voltage instabilities," said Rongming Chu HRL senior staff research engineer and principal investigator.

Chu and his colleagues in HRL's Microelectronics Laboratory have overcome that limitation, developing a GaN CMOS technology that integrates enhancement-mode GaN NMOS and PMOS on the same wafer.

"Integration of power switches and their driving circuitry on the same chip is the ultimate approach to minimising the parasitic inductance," Chu said.

CS International shines in new location

A SWITCH of venue proved a great success for the CS International Conference, with over 420 delegates and nearly 50 sponsors descending on Brussels for this annual event.

Held in the Sheraton Airport Hotel on Tuesday 1 and Wednesday 2 March, CS International took on a new dimension, thanks to its twinning with the inaugural and highly successful PIC International. Now in its sixth year, CS International continues to go from strength to strength, with a diverse line-up of speakers delivering key insights into the various sectors within the compound semiconductor industry.

Highlights of the latest conference included: compelling arguments over the need for 5G, and the lack of standards for it; the tremendous advances in III-V MOSFET technologies that could maintain the march of Moore's Law; advances in wide bandgap devices for power electronics, and breakthroughs in the characterisation of these classes of materials and related devices; and a frank discussion of the market for III-V cells, which is dominated by deployments in space. During the lunch and coffee breaks in a packed exhibition hall, delegates learnt of the latest developments by toolmakers and material suppliers, while mingling with attendees and exhibitors from



the PIC International Conference. This parallel-running conference on photonic integrated circuits got off to a great start, with speakers talking to a large, enthusiastic audience. Topics covered included the role of the foundry, strategies for success in the datacomms and optical network markets, and a discussion surrounding the best approach for uniting the laser with the rest of the chip.

More in-depth coverage of both conferences will be provided in the April&May issue of *Compound Semiconductor* magazine, and the launch edition of *PIC magazine*. The April&May issue of *Compound Semiconductor magazine* will also contain details of the winners of the coveted CS Industry Awards.

For more information about CS International Conference and the PIC International Conference, and opportunities available for the 2017 events, contact Stephen Whitehurst: stephen.whitehurst@angelbc.com Tel +44 (0)2476 718 970.

Toyoda Gosei develops new LED package

TOYODA GOSEI has developed a new surface mount LED package for lighting that produces up to 200 lumens per watt (lm/W), while maintaining colour fidelity.

The LED package is designed for general lighting applications, such as bulbs, tubes, downlights, and ceiling lights.

According to the company, the new package provides a cost-effective alternative to fluorescent and lower CRI (Colour Rendering Index) LED products and can help reduce overall energy consumption.

The new surface mount component combines blue LED die with phosphors.

Toyoda Gosei achieved this increase in efficiency, as compared to its prior LED package, through improvements to both die and package materials.

The package combines high efficiency, low thermal resistance to enhance the performance of the LED, and uses thermosetting plastics to provide high reliability while maintaining a superior gas barrier.



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Macom aims to make GaN-based PAs mainstream

MACOM has launched its anticipated MAGb series of GaN power transistors for use in wireless macro basestations.

Based on the company's Gen4 GaN technology, the new series is claimed to be the first commercial basestation-optimised family of GaN transistors to achieve a linearity and cost structure like LDMOS, and a path to better than LDMOS cost at scaled volume production levels.

"We believe that Gen4 GaN positions Macom at the vanguard of a transformative evolution in basestation power amplifiers, enabling a price/performance breakthrough that can't be achieved with alternative semiconductor technologies," said Preet Virk, senior VP and general manager, Carrier Networks, Macom.

"We anticipate that the wireless application expertise and commercial manufacturing scalability that Macom brings to this domain via the MAGb product platform will vault GaN-based PAs into the mainstream, unlocking a host of benefits for the next generation of

wireless basestations," he added. The MAGb series of power transistors target all cellular bands within the 1.8 GHz to 3.8 GHz frequency range. Initial entries in the product series include single-ended transistors providing up to 400 W peak power in small packages, dual-transistors and single-package Doherty configuration providing up to 700 W peak power in both symmetric and asymmetric power options.

This product series is said to deliver power efficiency improvement of up to 10 percent and package size reduction greater than 15 percent over legacy LDMOS offerings. The MAGb is easy to linearise and correct with digital-pre-distortion (DPD) schemes compared to other GaN technologies, says Macom.

The power transistors in the MAGb family cover much wider bandwidth than LDMOS, reducing the number of parts needed to cover the major cellular bands. The new product family delivers these advantages while simplifying the Doherty implementation over LDMOS-based transistors and maintaining over 200 MHz of video bandwidth.

AXT continues to realign business

AXT, a manufacturer of compound semiconductor substrates, has reported financial results for Q4 ended December 31, 2015.

Revenue was \$18.1 million compared with \$18.4 million in Q3 2015. Gross margin was 17.1 percent of revenue compared with 25.1 percent of revenue in Q3 2015. Operating expenses were \$4.8 million, compared with \$5.3 million in the Q3 of 2015. Operating loss for Q4 was \$1.7 million compared with \$0.7 million in the third quarter of 2015.

Net interest and other income for the fourth quarter of 2015 was \$0.1 million, compared with \$0.8 million in the third quarter of 2015. Net loss in Q4 2015 was \$1.2 million compared with a net profit of \$42,000 in Q3.

"2015 was a year of transformation for

AXT as we continued to realign our business with the trends that are driving growth in compound semiconductor substrates," said Morris Young, chief executive officer.

He added: "We focused on strategic investments in our technology and manufacturing capabilities that would improve our competitive positioning, and enable us to drive better consistency and efficiency across our substrate portfolio.

"We are pleased with these investments, and in the early results of our efforts. Although raw material pricing is providing a near-term headwind, we expect to continue to see a positive shift in our revenue mix in 2016 driven by InP, providing the potential for both revenue and margin expansion."

POET to deliver prototypes in 2016

POET TECHNOLOGIES, a developer of opto-electronics fabrication processes, has announced that it is on-plan with its lab-to-fab initiative to deliver first prototypes this year.

The company says that it is sticking closely to its commercialisation timetable to introduce a monolithic opto-electronics process platform for the production of smart optical components. Built to deliver the power of light at near the competitive price points of copper, POET's platform is designed to be capable of significant improvements in energy efficiency, component cost and size, according to the company.

Since its previous corporate update in September last year, POET has reached a number of milestones. It has transferred its proprietary technology to multiple foundry partners; received promising initial results of wafers processed at its newest foundry supplier Wavetek; initiated a process to produce integrated VCSEL prototypes; and has also consolidated its Toronto-Connecticut-San Jose operations in Silicon Valley.

The company also reports being in advanced discussions with a leading institution to enter into a joint development agreement to evaluate the adaptation of the POET platform for applications in micro-displays for the augmented reality market.

POET CEO Suresh Venkatesan commented: "Photonics is experiencing a post-telecom second wave of growth - this one, fuelled by consumers engaged in always-on social networking, cloud computing, Software as a Service (SaaS) and the ubiquitous devices that are central to our lives. "Social Networking, Cloud Computing, the Internet of Things and the growth of mega-datacentres are galvanising a renewed growth spurt in photonics. We believe, POET is at confluence of these megatrends. And we believe we are in the position not just to ride them, but to drive them."

Munich team deposits nanolasers on silicon

PHYSICISTS at the Technical University of Munich (TUM) have developed a process to deposit nanolasers directly onto silicon chips. A patent for the technology is pending.

Growing a III-V semiconductor on silicon is challenging. "The two materials have different lattice parameters and different coefficients of thermal expansion. This leads to strain. For example, conventional planar growth of GaAs onto a silicon surface results in a large number of defects," explains Gregor Koblmüller at the Department of Semiconductor Quantum-Nanosystems who led the project with Jonathan Finley, director of the Walter Schottky Institute at TUM.

The TUM team solved this problem in an ingenious way: By depositing nanowires that are freestanding on silicon their footprints are merely a few square nanometers. The scientists could thus preclude the emerging of defects in the GaAs material.

But how do you turn a nanowire into a vertical-cavity laser? To generate coherent light, photons must be reflected at the top and bottom ends of the wire, thereby amplifying the light until it reaches the desired threshold for lasing. "The interface between GaAs and silicon does not reflect light sufficiently.

We thus built in an additional mirror - a 200 nm thick silicon oxide layer that we evaporated onto the silicon," explains Benedikt Mayer, doctoral candidate in the team led by Koblmüller and Finley. "Tiny holes can then be etched into the mirror layer. Using epitaxy, the semiconductor nanowires can then be grown atom for atom out of these holes."

Only once the wires protrude beyond the mirror surface they may grow laterally – until the semiconductor is thick enough to allow photons to jet back and forth to allow stimulated emission and lasing.

"This process is very elegant because it allows us to position the nanowire lasers directly also onto waveguides in the silicon chip," says Koblmüller.

Currently, the new GaAs nanowire lasers produce infrared light at a predefined wavelength and under pulsed excitation. "In the future we want to modify the emission wavelength and other laser parameters to better control temperature stability and light propagation under continuous excitation within the silicon chips," adds Finley.

The team has just published its first successes. And they have set their sights on their next goal: "We want to create an

electric interface so that we can operate the nanowires under electrical injection instead of relying on external lasers," explains Koblmüller.

"The work is an important prerequisite for the development of high-performance optical components in future computers," sums up Finley. "We were able to demonstrate that manufacturing silicon chips with integrated nanowire lasers is possible."

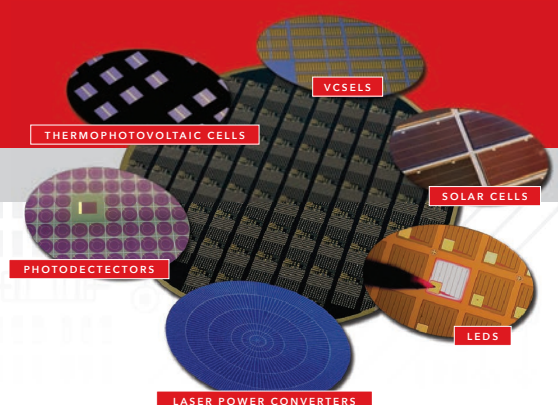
The research was funded by the German Research Foundation (DFG) through the TUM Institute for Advanced Study, the Excellence Cluster Nanosystems Initiative Munich (NIM) and the International Graduate School of Science and Engineering (IGSSE) of the TUM, as well as by IBM through an international postgraduate program.

'Monolithically Integrated High-beta Nanowire Lasers on Silicon' by B. Mayer et al; *Nano Letters*, 2016, 16 (1)
'Coaxial GaAs-AlGaAs core-multishell nanowire lasers with epitaxial Gain control' by T. Stettner et al; *Applied Physics Letters*, **108**, 011108 (2016)
'Continuous wave lasing from individual GaAs-AlGaAs core-shell nanowires' by B. Mayer et al; *Applied Physics Letters*, **108**, Vol. 8, to appear on Feb. 22nd (2016)


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imec breaks down 3D memory barriers

InGaAs channel to 3D NAND Flash memory is set to solve the read speed issues plaguing Samsung, Toshiba and more. Rebecca Pool reports.

IN A WORLD FIRST, Belgium-based nanoelectronics research institute, imec, has integrated a high-mobility InGaAs channel to a 3D vertical NAND memory structure in a bid to banish the drive current issues surrounding today's 3D NAND Flash devices that use a poly-silicon channel.

Right now, key NAND Flash manufacturers are replacing conventional planar NAND with 3D NAND to overcome problems such as cell-to-cell interferences and read noise associated with aggressive scaling.

The basic premise of these 3D memory devices is to stack storage cells vertically to dramatically boost the bit density relative to planar NAND flash.

Alternating layers of conductive polysilicon and silicon dioxide dielectric are deposited as a vertical stack, with channels then etched through the layers.

Hollow poly-silicon tubes, known as 'macaroni channels', are then deposited within the etched channel.

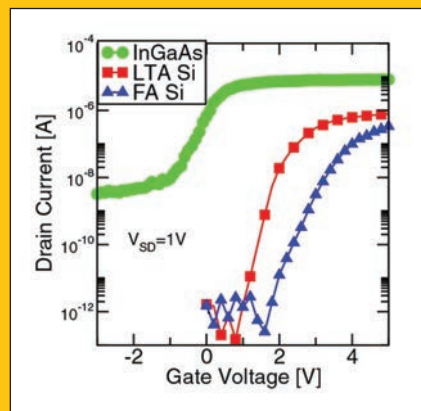
Since Samsung delivered the first mass-produced, 24-layer memory device in 2013, progress has been rapid.

The South Korean conglomerate unveiled

its latest 'vertical' NAND 48-layer chip in August last year while Toshiba and SanDisk also recently introduced a 48-layer flash memory device.

At the same time, Intel and Micron have released a 32-layer chip, and ultimately, industry players intend to create 100-layer stacks to achieve 1 Tbit memory devices.

But like the planar predecessors, these 3D NAND device's days are also numbered, and it's all down to the poly-silicon macaroni channel.



Typical I_D - V_G : $\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$ delivers an improved I_D - V_G characteristic. The $I_{\text{on}}/I_{\text{off}}$ ratio of three orders of magnitude is sufficient for typical NAND operation.

As Arnaud Furnemont, memory department director at imec, points out, the drive current of these 3D devices – with poly-silicon macaroni channels – decreases linearly with the number of memory layers.

“The resistance in poly-silicon is more or less proportional to the length of this channel, so if [industry players] keep stacking up the layers, at some point device read speed will just become too slow,” he says.

As Furnemont concedes, it is difficult to predict at what point this will happen but as he says: “Companies have announced 48 layers, and 64 layer devices are in sight on the roadmap.”

“I think this number of layers will be fine, but above 64 layers and by 100 layers it will be interesting to have an alternative channel,” he adds.

Given this, imec has been looking to swap the poly-silicon channel with a III-V alternative with a higher electron mobility. SiGe, with its high hole mobility, didn't fit the bill, so the researchers turned to InGaAs.

“InGaAs provided the right trade-off between electron mobility and bandgap,” says Furnemont. “And by changing the

ratio of indium and gallium we can play on this trade-off.”

In this latest work, the researchers have fabricated a three-layer memory stack into which 45 nm channel openings are etched and an InGaAs channel then formed, using MOCVD.

According to Furnemont, the resulting devices out-performed the poly-silicon equivalent by an order of magnitude, and critically, memory characteristics, including programming, erase and retention were maintained.

But clearly a three-stack device is a far cry from industry’s latest 48-layer versions. And what’s more, the InGaAs channel was actually solid, rather than the required macaroni conformity.

As Furnemont puts it: “Our InGaAs channel fills the entire hole, so to make the device relevant we need to convert the process from a full channel to macaroni channel.”

Given this, he and fellow researchers now hope to develop an atomic layer deposition process, so they can create a five-layer structure with the required macaroni channel.

“Apart from a few exceptions, ALD hasn’t really been developed for III-V materials, and there isn’t a full solution here yet,” he says. “But we are working with a supplier to develop III-V ALD. So far we have structural data but no electrical data.”

Furnemont also expects researchers to experiment with epitaxial growth, ALD and annealing to achieve progressive crystallisation of InGaAs macaroni channels in 3D NAND structures.

Beyond channel resistance issues, the researchers may also look at the problem of stresses in the memory stack. Defects form at the interface of the channel and

silicon dioxide layers but adding a thin high-k layer here could resolve this problem.

Given a full solution to 3D NAND’s integration issues has yet to come, is Furnemont still hopeful that the likes of Samsung and Toshiba will adopt imec’s processes? Indeed, these and other memory developers have massive research and development teams working on the very same problems.

“We still believe that channel mobility is not the worst part of these next-generation [3D NAND] devices, and maybe a cheaper [memory] solution will be discovered and implemented at some point in time,” says Furnemont.

“But if we can deliver a full integral solution for this approach then [industry players] will definitely look into this more deeply, and who knows, may apply it to their products,” he adds.



EARLIER THIS YEAR, UK Chancellor of the Exchequer, George Osborne, revealed that the government has set aside £50 million for a Compound Semiconductor Applications Catapult centre at a yet-to-be-confirmed location in Wales.

With annual funds of £10 million flowing from now until 2020-21, the government commitment spells good news for British businesses that would benefit from a fifth semiconductor cluster in the UK, centred around compound semiconductors.

"Because of the importance of compound semiconductors, we've been working hard to persuade government to put this in place," Chris Meadows, corporate systems manager at IQE. "This endorses our vision to grow a cluster in South Wales based on compound semiconductors with supply chains coming from Wales, the UK and the rest of Europe."

device processing. "A big part of the Catapult will be an open access facility so anyone that is designing a new product can use its services to do this, and IQE or CSC could act as a source for the epitaxy," points out Meadows.

"For device manufacturers, this is a very costly business with many barriers to entry and very expensive equipment," he adds. "So the Catapult will broker access to the necessary epitaxy tools, growth expertise and fabrication to enable custom device development."

What's more, Meadows is also hopeful that the Catapult will connect device manufacturers to end users in the aerospace industry, such as Airbus, as well as automotive manufacturers and more.

"These end users tend to just buy off-the-shelf [products]," says Meadows. "So we're trying to engage with them

is already starting to form here, and the catapult will encourage this."

"Start-ups, SMEs, spin-offs from universities, existing companies, investors as well as end users tend to want to be close to where products are being developed, so we would expect this to happen," he adds. "Look at imec and the Fraunhofer research institutes; these organisations act as magnets and once a region is known for a technology, more and more organisations are attracted."

So what can the compound semiconductor industry expect now? Right now only two facts are clear; £50 million funds are in place, and the centre will be based in Wales.

Specific location and founding members are yet to be confirmed. But as Meadows highlights, Innovate UK, the government body set up to support fledgling

Processing promise

As UK government dedicates £50 million to compound semiconductor device development, what can industry expect next, asks Rebecca Pool.

Indeed, Cardiff, South Wales, has been a hive of activity for compound semiconductor development. The launch of the multimillion pound Institute of Compound Semiconductors in late 2014 was followed by the Compound Semiconductor Centre (CSC), late last year.

The former venture, set up by Cardiff University, is exploring novel growth methods and material combinations. Meanwhile, the CSC, backed by the university, IQE and the Welsh government is intent on pushing compound semiconductor related research towards commercial production.

And now, the latest catapult centre is set to bring even more to the UK compound semiconductor industry. Focusing on the application of compound semiconductors, the new catapult will provide the facilities and expertise necessary for compound semiconductor

to understand future demands and the Catapult will be important here."

Welcome boost

In a bid to fuel economic growth across the UK, so-called Catapult centres were launched by government in 2011 to unite business and researchers and, importantly, to help start-ups market products that would otherwise prove difficult due to a lack of facilities and funding.

Indeed, up and coming short wavelength quantum cascade laser start-up, Stratium, has publicly announced its relocation from Sheffield to Cardiff, to take advantage of the new £50 million centre. And the South-West can expect more of the same.

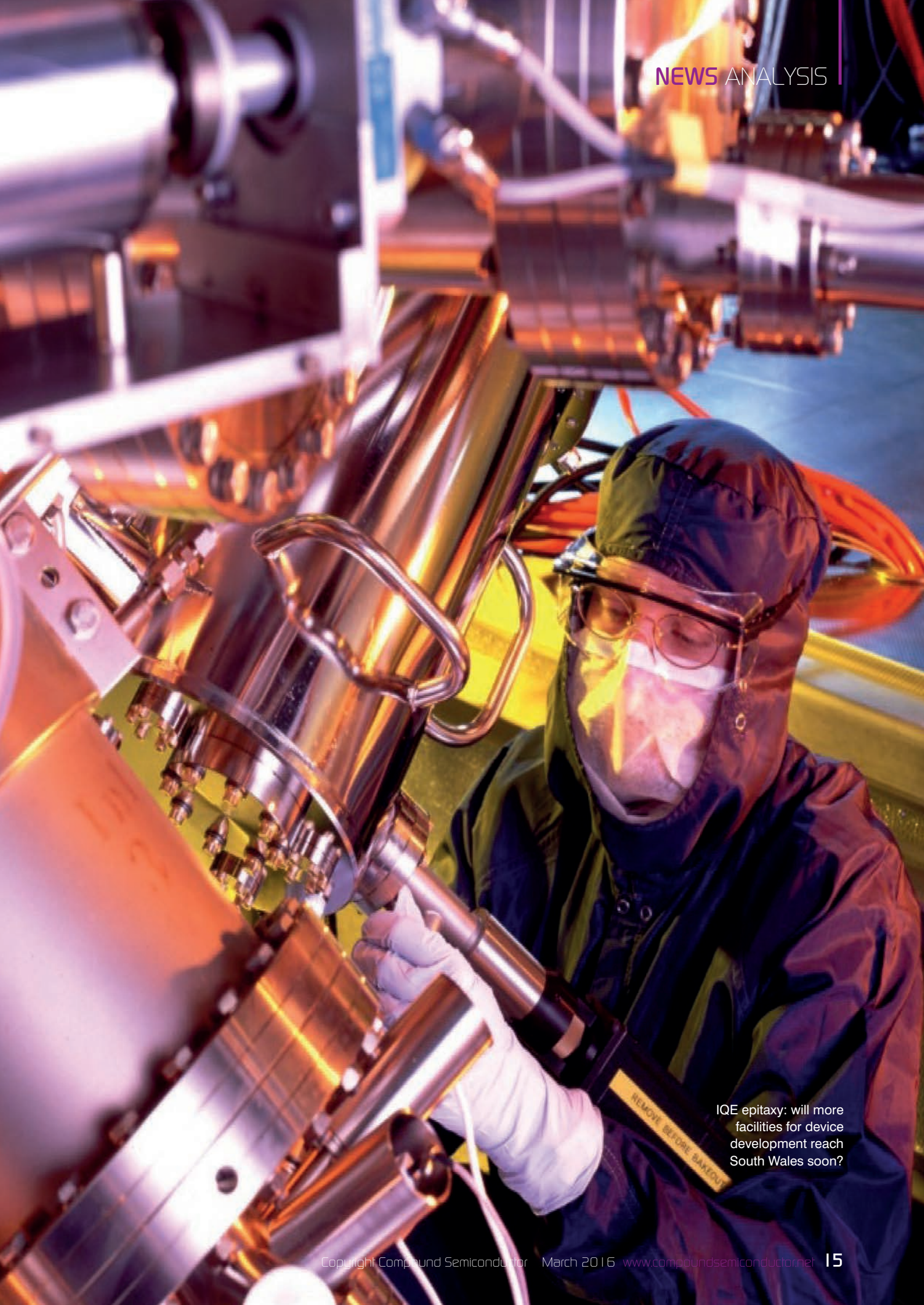
As Meadows highlights: "George Osborne made a commitment to a compound semiconductor catapult in South Wales largely because a cluster

businesses, is currently collaborating with industry to establish the best location and required facilities.

"We're seeing a lot of encouraging signs and Innovate UK has already been approached by quite a few interested representatives from the compound semiconductor industry," he says. "We've been told this catapult has generated a lot of early stage interest, which seems encouraging and unprecedented."

And Meadows is confident that the next few years will bring growth to the region.

"Cardiff University carried an impact study which reported that over the next five years, and certainly now with the catapult and semiconductor cluster, around 5000 jobs could be created [from this industry]," he says. "This is small compared to the semiconductor clusters in Europe, and of course Silicon Valley, but is still pretty significant."



IQE epitaxy: will more facilities for device development reach South Wales soon?



Stratium launches first laser and chases investments

As UK start-up, Stratium, releases gas-sensing lasers and relocates to South Wales to tap local expertise, Rebecca Pool asks director, Phil Cornish, about future plans.



Left: Stratum is one of the first start-ups to re-locate to Cardiff, UK, to take advantage of £50m in government funds, recently announced by Chancellor George Osborne.

government launched the Compound Semiconductor Centre, on the back of the multi-million pound, Cardiff University-led Institute of Compound Semiconductors.

“We’re taking advantage of a good situation in terms of these recent announcements,” highlights Stratum commercial director, Phil Cornish. “We have every intention of growing our company in Cardiff, so the Catapult is particularly important.”

“This centre could open up MOCVD and provide expertise here, and I expect we may be one of many compound semiconductor companies that could use these resources as well as those at the Compound Semiconductor Centre and Cardiff,” he adds.

Right now, Stratum manufactures short-wavelength QCLs, by depositing antimonides, such as InGaAs/AlAsSb, on 2-inch InP wafers.

Wafer manufacture and epitaxy – both MBE and MOCVD – are carried out in-house with the company also manufacturing 50 mW, pulsed, chip-on-sub-mount QCLs that emit at 2.8 μm , 3.3 μm and 10 μm to detect ethanol, methane and ammonia.

Operating above room temperature, the QCLs are said to enable detection and analysis of CH₄, HCL, CH₂O, CO, CO₂, NO and more, in the parts-per-trillion range. And according to Cornish, these products follow several years of research, including careful feedback between design and growth processes, as well fabrication and testing.

“Various growth parameters have had to be controlled to achieve the extremely tight tolerances required for material composition and layer thickness,” he says. “Additionally, the layer interface quality has to remain very high.”

The launch of the company’s first QCLs follows seed capital funds of more than £300,000 from UK-based intellectual property business, IP Group and Finance Wales. “This initial investment is helping us to optimise Stratum’s existing QCL

materials growth, fabrication, test and characterisation capabilities,” says Cornish. “And following our next funding round, we may make a strategic decision to acquire our own MBE tool.”

Funds are also helping to deliver Stratum’s second product, the ‘Eira’ Fabry-Perot QCL. This 4–10 μm CW laser emits more than 20 mW will come in a high-heat-load package, and is scheduled to launch towards the end of Q2, this year. Cornish believes key commercial opportunities will include industrial process monitoring and facilities gas monitoring.

“We can see great potential in gas sensing and monitoring markets so our core business right now is going to be developing these QCL [devices] so we can establish Stratum as a supplier of fully-tested QCL reliable products,” asserts Cornish.

Future applications for the start-up’s QCLs could include vehicle collision avoidance, breath diagnostics and more. And as Cornish adds: “We will grow and expand the company for sure, and as we move closer to new applications, such as environmental monitoring, we’ll also need to collaborate with people from around these fields.”

In the meantime, however, Stratum is expanding and hoping to recruit an electronics hardware design engineer. And Cornish has no doubts that the rapidly growing compound semiconductor expertise, in the South Wales region, can only fuel his company’s future success.

“Within Stratum we have QCL design capability and growth experience and we may acquire an MBE system,” says Cornish. “But the Catapult centre, for example, could present us with an opportunity to part-share such a system, removing this capital outlay.”

“The costs of an MBE or MOCVD system is of the order of a million pounds and this doesn’t include maintenance, clean room and running costs,” he adds. “These are all considerable and act as barriers to entry for any company wanting to develop technologies here.”

As the pace of compound semiconductor device development gathers momentum in South Wales, University of Sheffield spin-out, Stratum, is one of the first, of no doubt many, to re-locate to the region.

Having just launched its first quantum cascade laser for gas sensing and environmental monitoring applications, the company intends to take advantage of the local compound semiconductor expertise and investment in this region.

Early this year, the UK government revealed plans for a £50 million Compound Semiconductor Applications Catapult centre. Meanwhile late last year, Cardiff University, IQE and Welsh

AN INCREASED PORTFOLIO FOR WASTE GAS ABATEMENT

The planned merger of CS Clean Systems and Centrotherm Clean Solutions creates a single-source vendor offering a full suite of exhaust gas abatement products

BY JOE GUERIN FROM CS CLEAN SOLUTIONS

WORK in the compound semiconductor industry and you will face far greater challenges than colleagues working with silicon. It's not just that you have to strive far harder to minimize defects, and are unable to access design tools and measurements systems that are as sophisticated as those in the silicon sector – safety is more difficult to realise, due to the use of a wider range of gases that require careful handling. And on top of this, the abatement of the waste process gas requires more thought, partly because it can contain a greater variety of by-products.

CS Clean Solutions will offer a very broad portfolio of approaches to help with the safe treatment of exhaust gases resulting from the production of compound semiconductor chips. The new company will combine the expertise of CS Clean Systems, which has a pedigree in dry bed removal of hazardous gases that dates back to the 1980s, with the capabilities of Centrotherm Clean Solutions, a leading manufacturer of burner-wet and related thermal scrubbers.

All these companies, whether high-volume chipmakers or small start-ups, can soon draw on our full suite of trusted abatement products and our enlarged team of waste gas management experts. We are best prepared to support our customers and meet the challenges of the future.

At the heart of the manufacture of compound semiconductor devices is the growth of thin films, either by MBE or MOCVD. The former finds its greatest use in the deposition of films for high-frequency power amplifiers, HEMTs and HBTs. As MBE tends to involve solid-source precursors, the need to handle waste

gases downstream is often avoided, with the focus on the safe entrapment and disposal of solid by-products, which often include pyrophoric white phosphorous and arsenic.

The situation is very different when films are grown by MOCVD, the most common method for making LEDs. This growth technology involves group III metal-organics and group V hydrides that are either pyrophoric, highly toxic, or fit into both of these categories. The safety challenges associated with these materials surpasses that in the silicon industry by some margin, due to litre-per-minute flows of toxic hydrides, matched with simultaneous usage of pyrophoric metal-organics, and the predominance of hydrogen carrier gas in the exhaust.

Adding to the challenge is the length of the growth process. It can last for several hours, which is significantly longer than that associated with plasma etching or PECVD. And complicating matters even further, throughout the process cycle the concentrations of the individual exhaust species fluctuate strongly as growth steps stop and start.

Heading the list of concerns are two highly toxic, widely used gases: arsine and phosphine. In silicon foundries, these gases provide a source for *n*-type doping, with typical flow rates of 5 sccm to 20 sccm. That is about two orders of magnitude less than that used for the growth of III-V films, where arsine flow rates typically range from 300 sccm to 3000 sccm, and that for phosphine can hit 5000 sccm. Consumption rates for metal-organic precursors are rarely disclosed by chipmakers, but can be of the order of a gram or so per minute.



Dry bed scrubbing

Dry bed scrubbing is the most common technology for handling waste products generated during growth of GaAs and related material systems. This approach is favoured, because it requires very little maintenance, so operators rarely have to intervene to replace or service contaminated components. Unlike wet-scrubbing methods, the surplus III-V reactants and their MOCVD by-products end up as solids within the absorber column, so there is no liquid or sludge waste that must be handled and disposed by on-site service personnel. For our customers, there is also the benefit of a network of local service centres for emptying and refilling absorber columns.

There are two different classes of dry bed scrubbing. One option is based on physisorption, which is short for physical adsorption. What we advocate, however, is to use chemisorption – in other words, chemical absorption.

The physical adsorption approach for treating MOCVD exhaust products involves bonding of arsine and phosphine gases to a high-surface-area medium, such as charcoal. To enhance the retention performance of these materials, commercially available charcoal or

‘activated carbon’ media are often impregnated with metal oxides. However, despite this modification to the material, most of the adsorbed arsine and phosphine adheres to the carbon surface in its original – highly reactive – gaseous state.

One of the steps taken with physical adsorption is to periodically treat the bound hydride gases with a dilute mixture of air. This converts them into solid arsenic and phosphorous oxides. During this step, when the expended cartridge is air-treated, incoming exhaust gas is routed through a second cartridge. This cycle is reversed and repeated, typically every few days.

Rewind the clock and there was a time when impregnated charcoal was widely used for the abatement of MOCVD exhaust gases. However, recently there has been a sharp decline in the use of this approach, due to the transition of MOCVD from research and development to mass production, and a heightened awareness of worker safety.

Our preference for dry scrubbing is to use chemisorption, which converts by-products to solid at an ambient temperature. Chemisorption can work

The recently released Cleansorb Primeline PD model is designed for zero-downtime manufacturing. It incorporates two main absorber columns plus a back-up column. This allows one column to remain active absorbing exhaust gas with full SEMI S2-compliant safety protection, while the second column is removed for refilling.

with a range of hydrides, including arsine, phosphine, germane, stibine and disilane; and also commonly used metal-organics. Our product line, known as Cleansorb, involves the reaction of gases with a chemisorber granulate in an absorber column. The reaction is immediate, with no reliance on other media or heating.

When we install our Cleansorb systems at customer sites, we specify the retention efficiency of our dry bed columns in terms of the absolute concentration at the column outlet, rather than as a percentage of inlet concentration. The gas concentration at the column's outlet lies below the detection level of commonly used gas detectors – right up until the end of absorber capacity lifetime.

Selectivity is essential in the dry bed chemisorption process used during epiwafer growth by MOCVD. It is critical that the chosen absorber granulate must be reactive enough to enable effective, safe removal of waste gases and precursors, but it must not undergo any reaction with the bulk carrier gas, hydrogen. Of all the common hydride species, phosphine is the most reactive, followed by arsine, silane, germane and then hydrogen.

The challenge of removing group IV and V gases to below detection level, while allowing hydrogen to pass unabated, is even tougher at higher hydride flowrates. That's because the exothermic scrubbing reaction generates heat, which promotes the reaction between hydrogen and the absorber bed. If non-dedicated absorber media are deployed, reactions with hydrogen can take place at arsine and phosphine flow rates as low as around 1 slm. If this occurs, the temperature can rapidly ramp up, due to 'thermal

runaway'. Chipmakers then lose time and money, because the scrubber must be shut down due to overheating.

Preventing scrubber overheating is not the only challenge. It is also a necessity to tailor chemisorber chemistry to ensure controlled conversion of process by-products, while avoiding vigorous chemical reactions – especially with highly pyrophoric species such as hydrazine and metal alkyls.

To address all of these concerns, we have developed a range of Cleansorb granulates that are specifically tailored to the needs of individual MOCVD applications. Examples include selective removal of the highly poisonous, but relatively unreactive germane from hydrogen carrier gas; safe scrubbing of arsine and phosphine at combined flows of 5 slm and well beyond, while maintaining a safe energy barrier to reaction with hydrogen; selective removal of Group III metals from GaN and other MOCVD exhausts; and non-charcoal based removal of chlorine gas, which is increasingly used for *in-situ* cleaning of MOCVD chambers.

Handling hydrogen

Hydrogen is employed as the carrier gas in most MOCVD recipes for depositing arsenides, phosphides and nitrides. Though sometimes matched in flow rate by the nitrogen dilution added to the pump, hydrogen is often the major component of the exhaust gas. It is not relevant in terms of its toxicity, and it doesn't contribute to global warming – but it can form explosive mixtures with air over a wide concentration range, so its safe handling is obviously the primary concern.

One step MOCVD engineers must take to prevent any explosions associated with hydrogen gas is to ensure

that exhaust lines are free of leaks and other sources of air incursion. On top of this, measures must be taken to deal with hydrogen that are tailored to the particular materials being deposited. These measures may differ from those employed in silicon semiconductor facilities, which have traditionally used thermal and burner-wet scrubbers to incinerate hydrogen at the point of exhaust. If toxic metals are a concern for regulatory compliance, chipmakers may use dry-bed/ burner-wet scrubber combinations to prevent the contamination of scrubber waste water. This approach is particularly common when arsenic is used.

For the production of optoelectronic devices, LEDs and photovoltaics, and for the growth of wafers in III-V foundries, hydrogen tends to be diluted with air. With this approach, known as safe dilution, engineers aim for a maximum hydrogen-in-air concentration of 2 percent or even 1 percent. This corresponds to about 50 percent to 25 percent of the lower explosion limit. In some facilities, there are purpose-built dilution stations that feature a side-channel blower, which extracts the hydrogen stream into an auxiliary high flow of air via a series of non-return flaps. Once safely diluted, hydrogen can be released to atmosphere without any negative impact on the environment.

Gases for GaN

Ammonia is nearly always used for the growth of GaN. This precursor is used regardless of whether the substrate is sapphire, SiC or silicon, and whether the device will be an LED, laser or power transistor. In the growth chamber, ammonia reacts with a metal-organic precursor to produce GaN and a hydrocarbon gas.

At first glance, it appears that one of the advantages of the nitride MOCVD process is that it is less toxic

“ It is clear that the waste gas abatement of III-V processes covers an ever-widening spectrum of applications, each with its own challenges requiring individual, optimized solutions ”

than its phosphide and arsenide counterparts. For example, according to the American Conference of Governmental Industrial Hygienists, for ammonia the eight-hour threshold-limit (time-weighted average) is 25 ppm, compared with just 0.005 ppm for arsine and 0.3 ppm for phosphine.

However, this far higher ceiling is offset by the incredibly high consumption of ammonia gas for the growth of some devices. For LEDs, ammonia flow rates can hit 150 slm or more, exceeding that for arsine and phosphine by more than an order of magnitude. Due to these very high flow rates, dry bed scrubbing does not offer a viable solution for the abatement of GaN processes. Even when GaN devices are produced in research and development facilities, ammonia flow rates can be 30 slm. A weekly change-out of the absorber filling is required at this flow rate, rendering dry scrubbing commercially unfeasible.

Treatment of GaN exhaust gas is an important issue, due to the incredibly high volumes of GaN chips that

Figure 1 Left: Typical flow ranges used in the MOCVD production of arsenide and phosphide based III-V devices. Right: Typical flow ranges used in the MOCVD production of GaN-based LEDs and power amplifiers.

Material Regime:	GaAs, InP, AlGaAs, etc.	Typical Flow Ranges
Group III Precursors	TMAI, TMGa, TEGa, TMIIn, TEIn,	0.1 – 2 g/ min. (from bubbler)
Group V Precursors	AsH ₃ , PH ₃	0.3 – 5 slm
Dopants	DEZn, Mg(Cp) ₂ , Si ₂ H ₆ , CBr ₄	0-10 mg/ min.
Carrier Gas	H ₂	20 – 150 slm
Inert Gas Dilution	N ₂	10 -70 slm

Material Regime:	GaN, InGaN, etc.	Typical Flow Ranges
Group III Precursors	TMAI, TMGa, TEGa, TMIIn, TEIn,	0 – 30 g/ min. (from bubbler)
Group V Precursors	NH ₃	20 - 200 slm
Dopants	DEZn, Mg(Cp) ₂ , Si ₂ H ₆ , CBr ₄	0-100 mg/ min.
Carrier Gas	H ₂	20 – 250 slm
Inert Gas Dilution	N ₂	10 -100 slm

are produced every year. The approaches that are taken appear to vary by region, and in Asia, large, sometimes self-built, wet scrubbers are prevalent. However, even in aqueous solution, ammonia can exert a high vapour pressure, so effective removal requires an acidic scrubbing media, such as sulphuric acid. With this approach, the scrubbing by-product is an ammonium sulphate sludge. Freed of metallic and other contaminants, this has the potential to be reclaimed and recycled to fertilizer.

In other parts of the world, a popular approach for abatement is to use heated scrubbers. This is energy-intensive, rather than maintenance-intensive, and can involve catalytic bed designs, which decompose ammonia into its constituent nitrogen and hydrogen elements. Here again, MOCVD facilities with a policy of at-source hydrogen removal tend to use burner/wet scrubbers. With this approach, a key challenge is to balance the combustion of hydrogen with the formation of secondary nitrogen oxide pollutants.

III-Vs on silicon

Clear divisions between the compound semiconductor and silicon industries are blurring, with III-Vs seen as a potential saviour to maintain the march of Moore's law. Within the silicon industry, the design of equipment and facilities to support next-generation 450 mm wafers is already well underway. One of the most important objectives for the Facilities 450 mm Consortium is to ensure that energy savings, conservation of resources and emissions reduction are factored into facility design, right from the early planning stages.

InGaAs is tipped to enter the manufacturing roadmap for silicon devices at around the 7 nm node. The introduction of this III-V will bring with it environmental, health and safety challenges that have not escaped the attention of the larger silicon device makers

and foundries. They are currently evaluating the implications of introducing these high mobility materials, and considering how to accommodate the growth of these films into their facilities.

Due to the delicate circuitry and the associated limited thermal budget of the silicon IC, the group V precursor that is most likely to be used in production is either tertiarybutylphosphine or tertiarybutylarsine. The good news, from a safety perspective, is that both of these precursors are far less toxic than their phosphine and arsine analogues. What's more, thanks to the nanometre dimensions of the transistor gates, flowrates will probably be far lower than those used for the growth of other devices by MOCVD.

Despite these comforts, MOCVD processing is still uncharted terrain for most silicon wafer fabs. Some working in that sector have anxieties related to the prevention of emissions to air and waterways. In particular, there are concerns about the safe containment of arsenic, both from a deposition processes perspective and as a by-product of III-V etching.

It is clear that the waste gas abatement of III-V processes covers an ever-widening spectrum of applications, each with its own challenges requiring individual, optimized solutions. Companies entering this industry should not be alarmed, though, but take reassurance from the well established III-V community: it already spans several industries, and has a remarkably high track record of safety and environmental compliance.

All these companies, whether high-volume chipmakers or small start-ups, can now draw on our full suite of trusted abatement products and our enlarged team of waste gas management experts. We are best prepared to support our customers and meet the challenges of the future.

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 GaSb InSb InP InGaP
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Increasing the competitiveness of the GaN-on-silicon LED

Wafer-level, chip scale packaging using 200 mm silicon substrates improves wavelength uniformity, reduces thermal droop, aids radiative efficiency and slashes LED production costs

BY HYUN KUM, JOOSUNG KIM, YONGJO TAK, JONGSUN MAENG, JUN-YOUNG KIM AND YOUNGSOO PARK FROM SAMSUNG ELECTRONICS

Aixtron's G5+ is well-suited to the growth of high-quality GaN-on-silicon epiwafers.

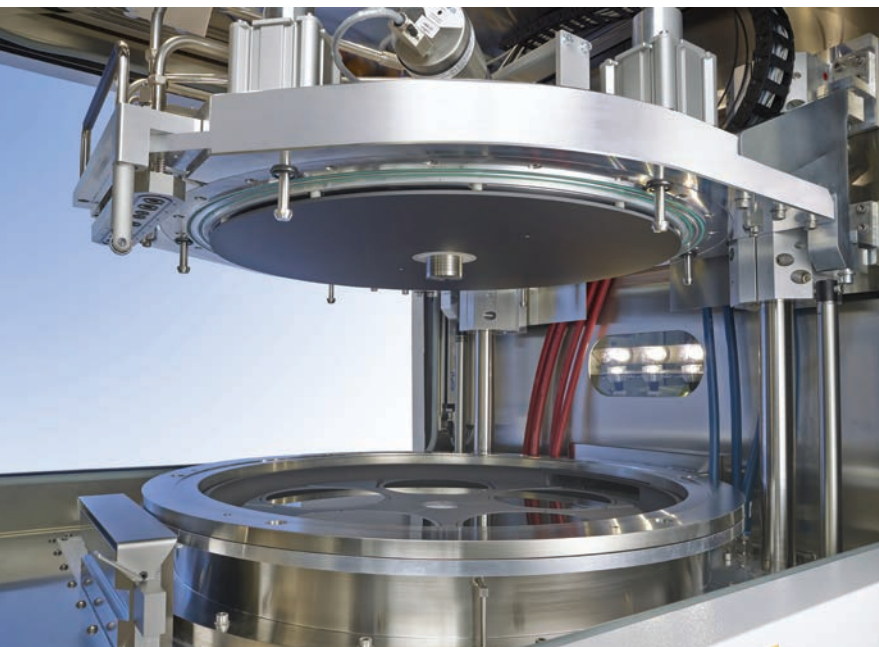
THE ERA of solid-state lighting has begun. LED light bulbs must now get better and cheaper, so that it is not just the early adopters that are investing in this technology, but the majority of the public parting with their cash, so that they can bring home efficient, reliable sources that will trim their electricity bills.

To drive down the price of the LED bulb so that more consumers will see it as a viable alternative to fluorescent, the cost of manufacture for the light-

emitting chips must fall. One way to do this is to manufacture devices on cheaper, larger substrates, such as 200 mm silicon. And another option, which many LED makers are considering, is to turn to wafer-level, chip-scale packaging (WLCSP). Taking this approach eliminates the multiple sorting and processing steps employed for the manufacture of a conventional LED package. Instead, these packages are directly created from the epitaxial wafer.

At Samsung Electronics of Gyeonggi-do, Korea, we view both of these approaches as complimentary, and are developing processes to make LEDs from 200 mm GaN-on-silicon wafers using WLCSP (see Figure 1 for potential cost savings). This approach makes a lot of sense, given that true WLCSP technology has not been demonstrated successfully on conventional sapphire substrates. There are several reasons for this, including a 'blue leak' issue, where blue photons escape from the sidewalls of the device (see Figure 2). A true wafer-level process cannot address this issue, so instead the GaN-on-sapphire epiwafer has to be diced, binned, and transferred individually onto a thermal tape for phosphor dispensing, before another dicing step is undertaken.

With our WLCSP approach, which is based on thin-film flip-chip technology, we combine thinner GaN layers (they are less than 3 μm -thick) with the removal of the silicon substrate. This essentially eliminates the blue leak, and enables a simpler process for phosphor coating and dicing. No binning and transferring is needed. Consequently, wavelength uniformity





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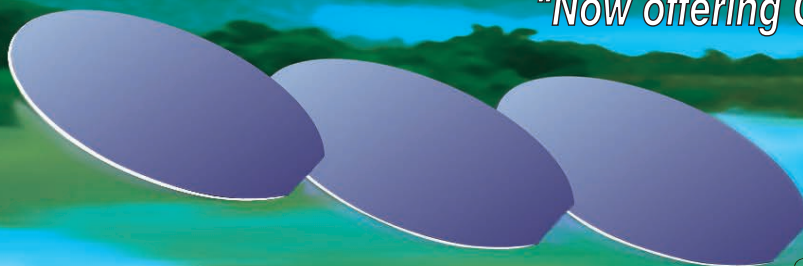
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- Single wafer processing possible
- We buy used wafer and sell recycled wafer



Figure 1. Switching to wafer-level, chip-scale packaging and 200 mm silicon substrates can slash the cost of the LED by 60 percent.

becomes critical, because the phosphor is coated as a film over the entire wafer. Obtaining the desired colour temperature and colour-rendering index hinges on matching the wafer wavelength and the phosphor characteristics.

To realise a sufficiently high yield with our WLCSP technique, we need to produce high-performance, reliable LEDs from 200 mm GaN-on-silicon epiwafers exhibiting excellent wavelength uniformity. Specifically, we target 95 percent or more of the epiwafer's area to have a wavelength range of 4.0 nm or less. This is a demanding target, as a typical, state-of-

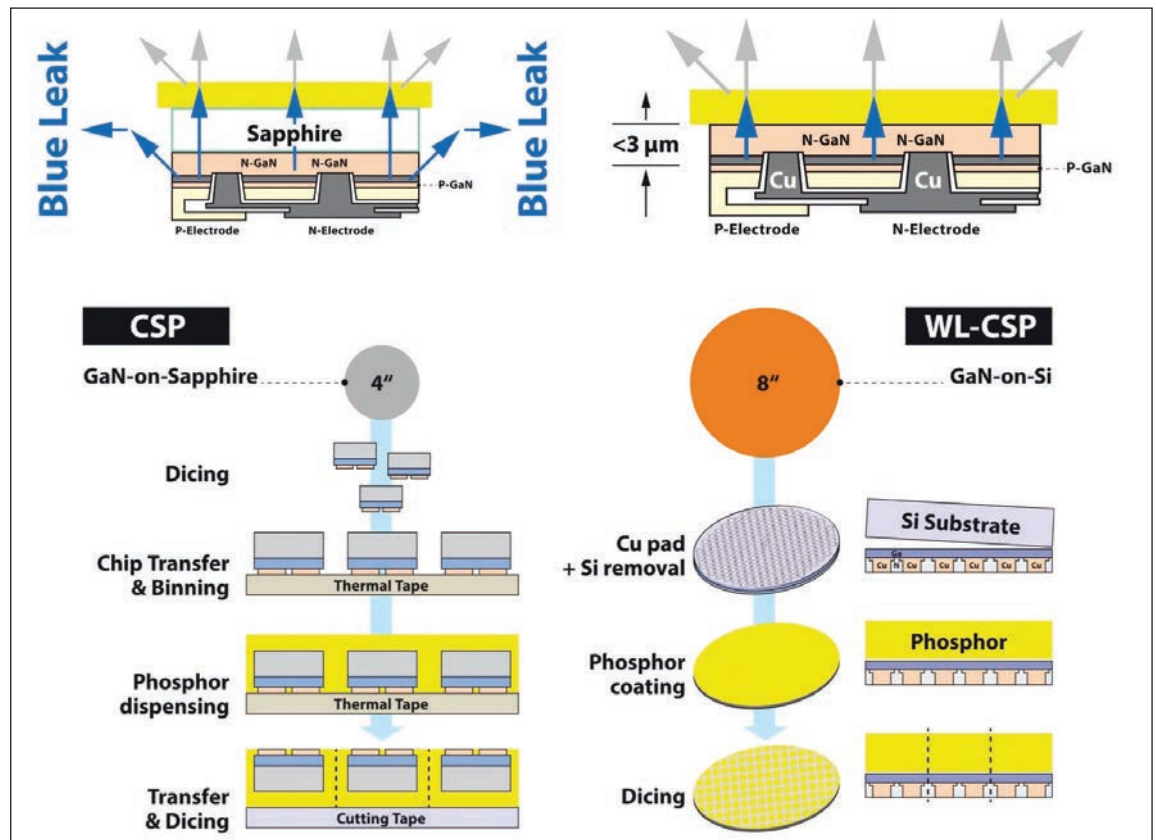
the-art 100 mm sapphire substrate has an in-wafer wavelength uniformity of about 8 nm.

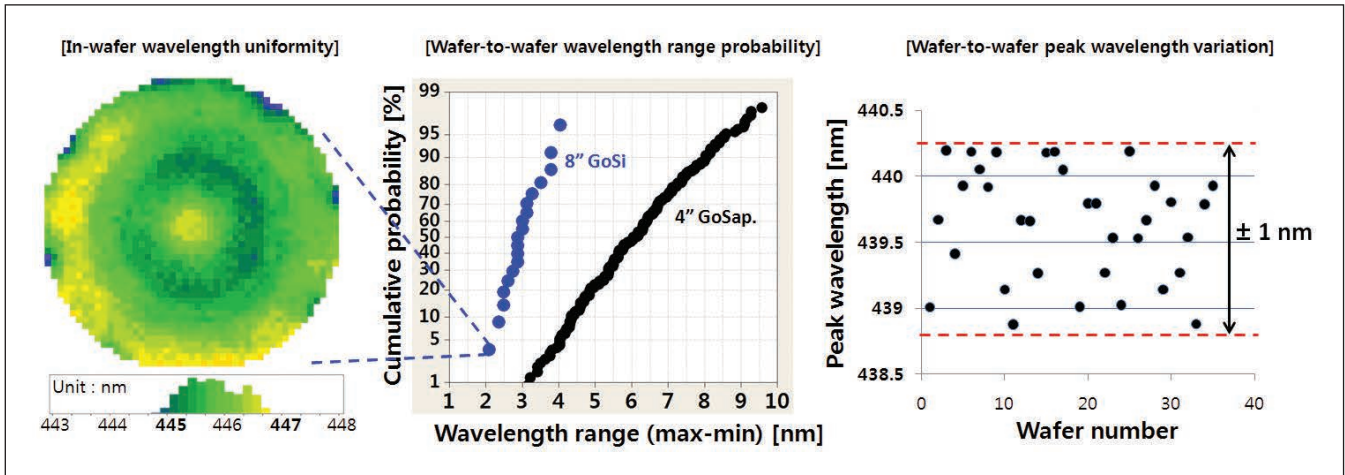
MOCVD of GaN on silicon

Perfectly meeting this need for a tight wavelength distribution, while excelling in productivity and minimising production costs, is the Aixtron AIX G5+ system in a multi-wafer, 5x200 mm batch configuration.

Several key technologies contribute to the high yields realised with this reactor. On-wafer yield benefits from: the inherent rotational symmetry of deposition; an

Figure 2. Sapphire substrates are incompatible with true wafer-level, chip scale packaging, because blue light leaks out of the chips (top left). This is not an issue with GaN-on-silicon LEDs (top right). With sapphire substrates there is a need for dicing, followed by chip transfer and binning, phosphor dispensing and transfer and binning, and transfer and dicing (bottom).





optimized RF heater design; and excellent tunability of the distribution of growth species in the gas phase.

Using silicon rather than sapphire is another virtue, because its higher thermal conductivity reduces wafer bow, which in turn decreases the temperature gradient through the wafer and the deposited epitaxial structure. As each wafer's temperature can be controlled to the target set-point, it is possible to realise the overall uniformity requirements for WLCSP (see Figure 3).

Another strength of the AIX G5+ is its thermally activated chemical reactor reset. This guarantees the same growth conditions from one run to the next, and prevents silicon wafer edge damage resulting from gallium meltback, and minimizes yield loss through particles and defects (see Figure 4).

Although the benefits of low-cost LEDs produced on large-diameter silicon wafers are compelling, these devices are yet to have an impact in the lighting market. That's because the quality of the GaN films that are grown on silicon is below what is ideal, hampering the device's efficiency and reliability.

Growing high-quality GaN epilayers on silicon is not easy because there is a significant lattice mismatch between the two materials, and a difference in thermal expansion coefficient of nearly 50 percent. These differences can cause crystalline defects, such as dislocations and cracks, that impair efficiency and reliability and ultimately lead to low yield and increased cost.

Cracks, which occur in the GaN epilayer above a certain stress threshold, tend to originate at the wafer edge, where the stress during and after growth is greatest. However, these cracks can propagate further into the centre of the wafer, significantly lowering yield.

Threading dislocations, the other common imperfection associated with GaN-on-silicon

epiwafers, appear during the growth, due to the 17 percent lattice mismatch between the two materials. Dislocations can be reduced with strain compensation layers, also known as buffer layers. However, even with this approach, the typical dislocation density of a GaN layer that is grown on silicon is two-to-three times that grown on sapphire. The dislocations hamper sales of GaN-on-silicon LEDs, because they drive down device efficiency, introduce reliability issues and may be the origin of catastrophic failures, due to electrostatic discharge.

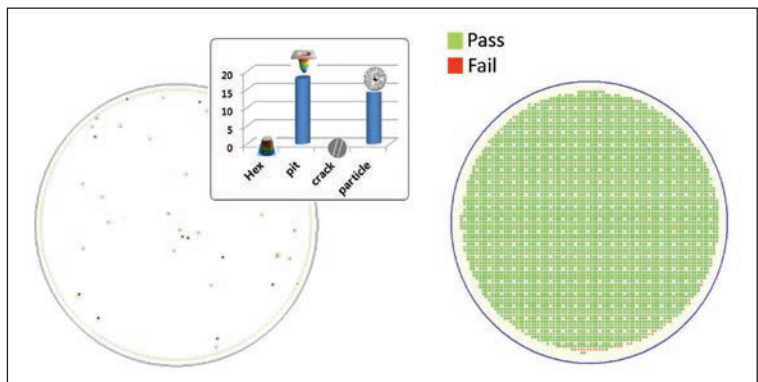
By optimising the buffer layers of our LED structures that are grown on 200 mm silicon, we can produce crack-free material with a dislocation density of typically just $3 \times 10^8 \text{ cm}^{-2}$. The proportion of the wafer that is good enough for chip production is very high (see Figure 4).

One of the biggest advantages of solid-state lighting, compared to incandescent and fluorescent lighting, is the longer lifetime of the source. Although those buying LED bulbs have to pay more than they would do for the alternatives, they have to fork out for them less often, and they are rewarded with lower electricity bills.

Given the longer lifetime of solid-state lighting, it is not surprising that the designers of light bulbs

Figure 3. The wavelength uniformity for GaN-on-silicon (GoSi) is significantly superior to that of GaN-on-sapphire (GoSap), despite the doubling of wafer diameter to 200 mm.

Figure 4. The wafer defect and LED pass/fail map shows the very high quality of epiwafers that may be produced by the Aixtron AIX G5+.



“

The higher levels of strain that are present in GaN layers grown on silicon, rather than sapphire, are viewed as undesirable, because they can impair crystal quality. But that’s not a balanced view, as this silicon foundation increases radiative recombination

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are concerned with the defect density in GaN-on-silicon epilayers. In general, researchers studying catastrophic failure and degradation mechanisms in solid-state lighting have found that failure of the module is more likely than that of the device.

The good news is that our studies with GaN-on-silicon LEDs confirm this view, with thousands of hours of reliability testing revealing that with our strain-managed process, silicon substrates have little to no impact on device reliability compared to sapphire substrates. The degradation characteristics of both types of LED are very similar (see Figure 5 for the device test results).

Diminished droop

The performance of all forms of GaN LED is held back by droop, a decline in device efficiency at higher drive currents. However, the reduction in performance caused by thermal droop in our LEDs is only about half of that for devices grown on sapphire (see Figure 6). A lower thermal droop is a very valuable attribute, because most mid- to high-power devices operate way beyond room temperature, and it is the lumen-per-dollar that they produce at an elevated temperature that is the best measure of their bang-per-buck. Note that the exact physical mechanism for thermal droop is still under investigation, but it is known that some processes, such as carrier overflow, are stronger at elevated temperatures.

To determine a device’s performance in a particular application, it is helpful to measure the junction

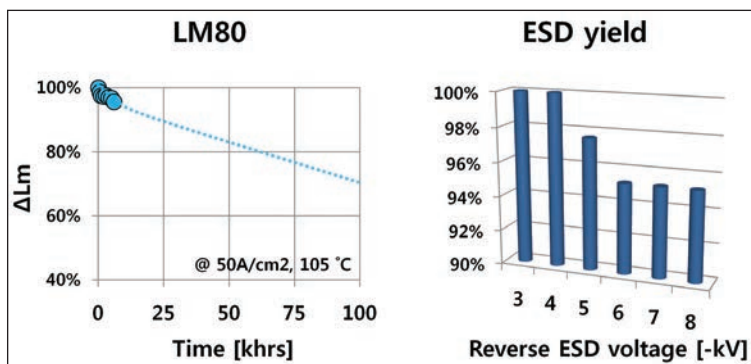
temperature directly. By making these measurements, we have found that devices grown on silicon run about 20 °C cooler than equivalents on sapphire. (We determined this by first extracting the thermal coefficient, which can be measured by applying a low amplitude pulse current as a function of precisely controlled ambient temperature, and then considering the change in forward voltage with temperature – in our case the shift in forward voltage at a 350 mA drive current for temperatures from 25 °C to 85 °C). The lower junction temperature is beneficial, because it trims costs. If the junction temperature is higher, then better and more expensive heat sinks and cooling systems are needed to prevent chip and package degradation.

The higher levels of strain that are present in GaN layers grown on silicon, rather than sapphire, are viewed as undesirable, because they can impair crystal quality. But that’s not a balanced view, as this silicon foundation increases radiative recombination. When GaN is grown on sapphire, there is a compressive strain in the GaN epilayers that results in an in-built piezoelectric field within the quantum wells – this occurs through the rearrangement of electronic states in the crystalline structure at the GaN/InGaN interface. This field pulls apart electrons and holes in the quantum wells, reducing the overlap of these wavefunctions and ultimately the radiative efficiency.

When GaN epilayers are grown on silicon, the situation is markedly different. A relatively tensile strain is forced upon the active region, due to the difference in thermal expansion coefficients, and this offsets the piezoelectric field. A reduction in the electric field results, which increases electron-hole wave-function overlap and radiative efficiency.

In addition to the increase in radiative efficiency, the reduction in the electric field strength propels emission to longer wavelengths. Consequently, if the thickness of the wells is maintained, less indium is needed to reach the same wavelength. This is great news, because a reduction in indium content allows growth at higher temperatures, improving crystal quality.

Figure 5. Samsung’s GaN-on-silicon LEDs have a high degree of robustness to electrostatic damage, and their output shows a modest decline over many hours of operation. Note that 25,000 hours corresponds to about 3 years of continual use.



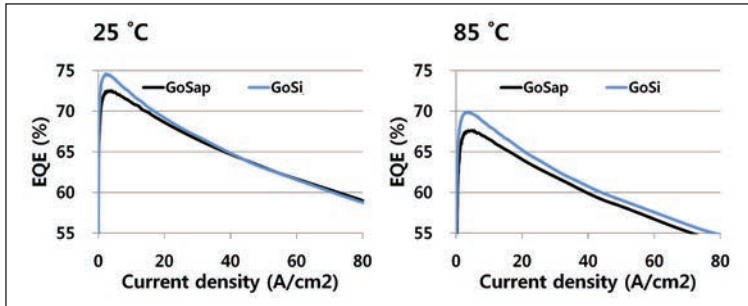


Figure 6. The external quantum efficiency (EQE) of the GaN-on-silicon (GoSi) LED is very similar to that of GaN-on-Sapphire (GoSap) at 25°C, but better at 85°C, a typical operating temperature.

Another encouraging characteristic of our devices is their low thermal droop – it is 73 percent lower than that of equivalent WLCSP LEDs grown on sapphire. This superiority underlines the superb crystalline quality of our GaN-on-silicon epilayers. In these devices, thermal degradation in the active region will be less than that for sapphire-based variants, correlating to a more gradual performance degradation and a longer lifetime. As solid-state lighting products are expected to exceed 50,000 hours of operation, this could be a tremendous benefit over time.

In future, it may be possible for LEDs grown on silicon to outperform their more conventional cousins. Such devices would be very promising, given that silicon

is well suited to WLCSP. For example, it is easy to remove silicon substrates from GaN epilayers, and it is relatively straightforward to trim the thickness of GaN, which cuts efficiency losses due to absorption of photons within the LED chip. What's more, it is not that challenging to texture the GaN or phosphor surface at the wafer level, to maximize photon extraction efficiency. And efficiencies can be driven up even higher by implementing novel package-level designs, such as multi-layer, multi-colour phosphor coatings.

Based on our work so far, we have an optimistic outlook for the future of the GaN-on-silicon LED. Combining our WLCSP technology with the growth of GaN-on-silicon epiwafers in an AIX G5+ system, we have been able to produce highly efficient LEDs that are on a par with those based on sapphire. We are now commercialising these devices, and we expect them to take a significant share of the LED market. This share could grow if optimisation of these devices allows them to outperform their conventional counterparts, or they are adapted to target other markets. By shrinking their dimensions, micro-LEDs could be produced for next-generation display technology. While sapphire may be the substrate of today, the future surely lies with silicon.

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China's maturing LED industry

The Chinese LED industry is changing. A multitude of rivals is giving way to a smaller number of larger and ever-expanding LED chipmakers that are targeting growth of domestic and overseas sales, says IHS analyst Alice Tao during a wide-ranging interview with Richard Stevenson.

Q How would you describe the state of the LED industry in China today?

A I don't think I can describe it in one sentence, but I can choose some words. The first is expansion, and then price erosion and bankruptcy. There are still companies – major, public and large companies – that are expanding their capacity.

For price erosion, it is mostly due to the competition among Chinese companies. Sometimes they have exactly the same products, so they can only compete with each other on price. Bankruptcy is mostly related to smaller companies without enough funds or a technical advantage. It becomes difficult to survive, due to the bigger players.

Q How is the Chinese government supporting LED manufacturing right now?

A It actually depends on the local government. If an LED company decides to invest a lot in the city, maybe the local government will have some subsidies, mostly on the technical and innovation side, like R&D. There may also be tax abatement or the providing of free land.

Q Does the Chinese government, or local government, still offer subsidies on MOCVD reactor purchases?

A I think that there are still some cities that are offering MOCVD subsidies. But it is not recent subsidies. Companies that signed a co-operation agreement with the government three or so years ago are still keeping adding tools, based on their contracts.

Q A few years ago there was a massive ramp in the number of LED chipmakers in China. Has this led to a significant number of mergers and acquisitions?

A Most smaller companies went bankrupt. However, there were mergers amongst smaller companies – for example, NationStar acquired Invenlux. These two companies are very small chipmakers. They have around ten-to-twenty MOCVD tools. For larger companies, which have more than 50 MOCVD tools, I don't think there will be any acquisitions. The larger ones are all expanding their own capacity, and they don't want to acquire the smaller ones.

Q Is LED chip manufacture centred around a few cities, or a particular region?

A It is spread around the country. The locations of LED chipmakers depend on the local government, and whether it provides subsidies. If the local government provides subsidies, the manufacturer will choose to have a factory there.

Q How good is the quality of most of the LEDs made in China today?

A It depends on the application. LEDs are good enough for most applications, like LED video walls or signage. Chinese LEDs are also good enough for general lighting, because there are a lot of different lamps and luminaires.

For some high-end applications that need a very high CRI, or for other applications like automotive headlamps, maybe they are not good enough.





Q How would you describe the LEDs made in China, in terms of their output power? Are most mid-power devices?

A Chinese manufacturers can produce both, but most are mid-power.

Q Are most of the LED sales associated with backlighting, or general illumination?

A General lighting. Backlighting, compared to general lighting, is a very small market.

Q Are LED bulb manufacturers in China buying their LEDs domestically, or importing them?

A Both, because there are too many lamp and luminaire manufacturers – maybe tens of thousands. It depends on the company’s target market. If the target market is the US or Europe, maybe the bulb maker will choose an LED chip from Korea or a Taiwanese company.

For most lighting companies, their main market is domestic, so they just use Chinese LED chips.

Q Is LED lighting big in China? Or are most homes and offices using fluorescent sources?

A I think in most homes and offices it is not LEDs.

Q Who are the leading LED makers, in terms of quantity and quality?

A Definitely San’an.

Q Are most companies making chips and packaging them? Or is the packaging outsourced?

A For chipmakers in China, they usually don’t do packaging themselves. I don’t think it’s easy to do vertical integration in China. There is always too much competition, so companies focus on one area. If you want to do integration, you need a lot of funding.

Q Is manufacture in China predominantly on 2-inch sapphire?

A Most companies have moved to 4-inch. Essentially these are the big players.

Q Are many companies developing GaN-on-silicon LEDs?

A Some companies might be doing R&D on this topic. But for companies that really have a production line, in China it is probably just Lattice Power.

Q How seriously are Chinese LED makers taking IP issues?

A It depends. I think smaller companies are not that concerned, because they only sell their products in China. For larger companies, because they need to expand their business overseas, they have to work on this issue. Maybe most of them use the easy strategy of acquiring a company with lots of patents.

Q Is there a strong relationship between universities and LED makers to support the development and manufacture of high-performance LEDs?

A I have heard that Lattice Power – it is the only company doing GaN-on-silicon LEDs in China – have cooperated with Nanchang University. For other companies, I believe that there must be some partnership, but I don’t know this for sure.



According to Alice Tao from IHS, San'an is China's leading LED maker, in terms of both quality and quantity.

Q MOCVD reactors are a significant expense for LED chip manufacture. Are LED makers in China still buying from Aixtron and Veeco, or are Chinese MOCVD firms starting to compete?

A They are still buying from Aixtron and Veeco. Previously in China, the sale price was relatively high, but because Aixtron and Veeco have been competing with each other, the tool price has dropped a lot compared to what it was three or four years ago. However, this tool is still very expensive. Maybe reliability is very important, and LED makers don't believe the quality of the Chinese-made MOCVD tools.

Q Due to high levels of bankruptcy, are there lots of second-hand MOCVD tools being bought and sold?

A Not many. Currently, only large LED chipmakers can survive. These large companies are all expanding their

own capacity. They don't want to purchase old tools.

Some of the small companies that started in the LED business were motivated by getting the subsidy from the government. The MOCVD tools actually belong to the government, rather than the small companies. I think there are some second-hand tools, but not many. Also, Veeco and Aixtron announced their next-generation tool about a year ago, and some companies don't want the earlier reactors.

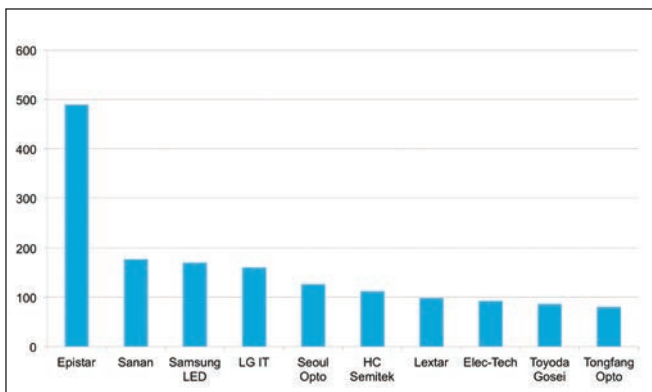
Q What about Taiyo Nippon Sanso?

A I don't think that they have supplied MOCVD tools to China. Maybe five or six years ago I heard of some sales with China, but recently no.

Q What about the supply of substrates, ammonia and metal-organics? Is that domestic, or imported?

A For substrates, they are mostly sapphire. There are lots of sapphire manufacturers in China, so most of the substrates come from domestic suppliers. But sometimes, for 4-inch, companies want patterned sapphire, so sometimes they purchase from Taiwanese or Korean companies. But that's not a large amount.

For others materials, especially speciality gases, I think it is still dominated by Western companies.



Chinese LED chipmaker San'an is second on the list for the top 10 merchant MOCVD customers by the end of third quarter of 2015.

• Alice Tao holds the role of Senior Analyst, LEDs & Lighting, at IHS. She joined IHS as a market analyst in February 2011 and works on the China LED market and MOCVD and LED supply. She was previously a manager at ENF, a PV consulting firm. She has a BA from Anhui Normal University.

Optimising LEDs for wireless communication

The attributes of white LEDs are not limited to high efficiencies and long lifetimes. Scale them down, arrange them in arrays and equip them with fast-responding colour converters, and these devices are very promising broadband sources for high speed, light-based wireless communication

BY JONATHAN MCKENDRY FROM THE UNIVERSITY OF STRATHCLYDE

Various patterns displayed on a micro-LED array. Each pixel is 100 μm by 100 μm and is individually addressable. The red scale bar is 300 μm .



WE ARE CONTINUING to refine the way we use light to transmit information. Back in the ninth century, during the Arab-Byzantine wars, communities would relay very simple messages by the lighting of bonfires on a particular hour of the day. Fast-forward to the 1860s, and communication at a rate of several words per minute could be transferred between sailors on-board ships of the British Royal Navy using a form of Morse code. And a decade or so after that, the well-known scientist, engineer and inventor Alexander Graham Bell demonstrated a 'photophone', a device that used an intensity-modulated beam of sunlight to transmit speech from one location to another.

Today, there is interest in transmitting data at far higher rates, using light bulbs as the source. If these bulbs are incandescents or fluorescents, high data rates are out of reach. But with the introduction of LED lighting, transmission at hundreds of Mb/s, or even several Gb/s, is now feasible. As the uptake of solid-state lighting is booming, there is good reason to believe that an era of using white LED sources for simultaneous illumination and wireless communication, often dubbed 'Li-Fi', is on the horizon.

Li-Fi, which is a form of visible-light communication (VLC), involves using LEDs to simultaneously illuminate an environment and transmit data via modulating the intensity of the source. Modulation is performed in a manner than is imperceptible to the

human eye and compatible with dimming schemes. One of the great strengths of Li-Fi is that it makes use of a wide, licence-free visible spectrum. It could help to maintain the rapid growth in wireless data traffic, which rocketed from 2.5 Exabytes (Eb) in 2014 to 4.2 Eb in 2015 and is projected to outstrip improvements in existing radio-frequency wireless technology (see Figure 1).

Taking standard 'off-the-shelf' white-emitting GaN LEDs, a team from the TeCIP Institute in Italy has already demonstrated data transmission rates in free space in excess of 1 Gb/s, and realised 3.4 Gb/s through the simultaneous use of red, green and blue LEDs. However, while the LEDs used for these studies offer high modulation bandwidths in comparison to incandescent and fluorescent sources, they are still relatively modest, typically 10-20 MHz. These low modulation bandwidths limit the maximum data rates, although it is possible to increase this with more complex modulation schemes.

A narrow bandwidth is not, in general, a concern for the designers of LEDs for lighting, as their focus is optimising characteristics such as the luminous flux and wall-plug efficiency. But it does matter to our team from the Institute of Photonics at the University of Strathclyde, which is participating in a four-year project, entitled Ultra-parallel visible-light communications, that kicked off in October



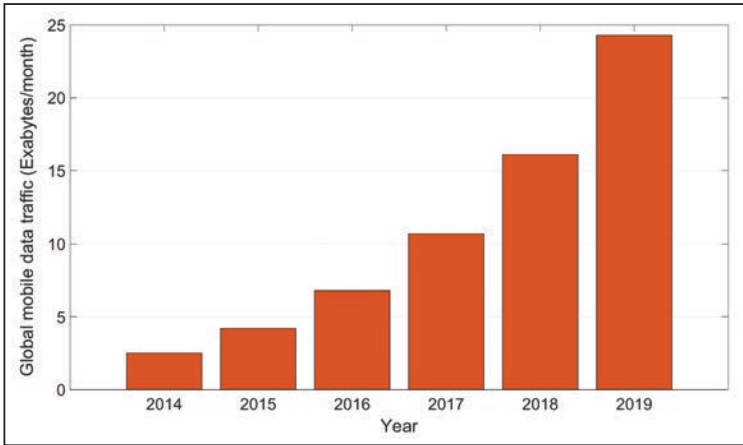


Figure 1. Global wireless data traffic is growing rapidly with an estimated compound annual growth rate (CAGR) of 57 percent. Note that this data is taken from the Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2014–2019.

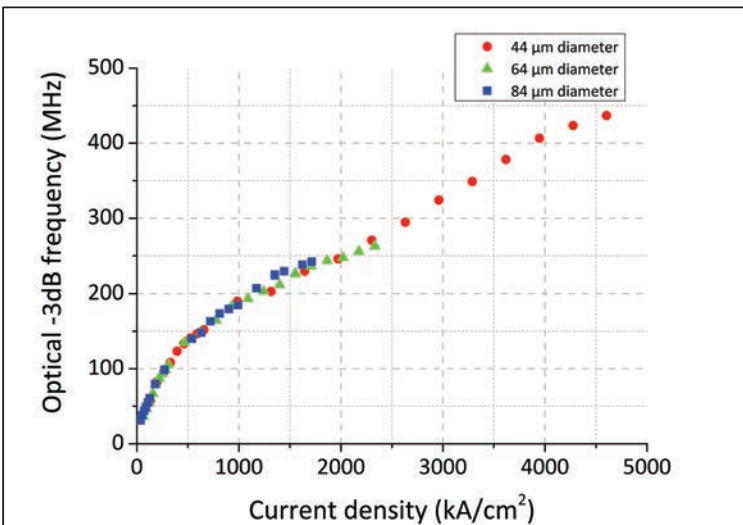


Figure 2. The modulation bandwidth of three micro-LEDs, each with a peak emission wavelength of 450 nm, at differing operating current densities. Each micro-LED has a different diameter, but are from the same array. This plot highlights that: micro-LED bandwidth is dependent on current density (with the different-sized micro-LEDs showing the same bandwidth when operated at the same current density); and smaller micro-LEDs are able to be operated at higher current densities than their larger counterparts, because they are able to reach higher modulation bandwidths.

2012. Backed by £4.6 million of funding from the Engineering and physical Sciences Research Council, we are working with colleagues from the Universities of Cambridge, Edinburgh, St. Andrews and Oxford towards the goal of determining how data rates are influenced by novel modulation schemes, receivers, colour-converting materials and LED-based transmitters.

Our particular focus lies on the transmitter side. We are able to leverage our expertise in micro-LED arrays, which contain many individually-addressable LEDs with typical dimensions of less than 100 µm. Thanks to their small size, hundreds of these devices – which can be produced by conventional processing of commercially-available GaN LED wafer material – can fill an area that would usually be occupied by a single LED.

Shrinking device dimensions is highly beneficial for data transmission, because the modulation bandwidth is no longer limited by the device’s resistance and capacitance – instead, it is governed by carrier lifetime. This depends on the carrier density, which can much higher in our LEDs. They operate at typically 15,000 A cm⁻², compared to just 10-100 A cm⁻² for most standard LEDs. Due to this ability to handle higher current densities, modulation bandwidths are an order of magnitude higher than those for conventional LEDs (see Figure 2)

We have used our devices to break the record for the highest reported data rate from a single GaN LED. Using a single micro-LED pixel with a peak wavelength of 450 nm and a pixel diameter of 50 µm, we realised a data rate of 3 Gb/s using orthogonal frequency-division multiplexing (see Figure 3).

The signal-to-noise ratio available at the receiver limited the separation of the transmitter and receiver to 5 cm. However, by adding transmitter and receiver optics, this data link can be extended to 10 m. This result highlights the capability of micro-LED optical transmitters for multi-Gb/s data transmission rates over useful link lengths.

Multiple pixels

Following our demonstration of the potential of individual micro-LED emitters, our focus shifted to exploring the possibilities of utilising multiple pixels within an array. With micro-LED sources, their multi-emitter, pattern-programmable format has the potential for individual addressing of hundreds of emitters. By turning from a single emitter to a multiple variant, data communication can be enhanced in different ways. For example, multiple data streams can be transmitted in parallel to increase the overall data rate – a technique known as multiple-input, multiple-output,

or MIMO. Alternatively, data can be encoded into the spatial position of the pixels. With this approach, which is a form of spatial modulation, transmission of data is via the switching on of the appropriate LED(s) during designated times.

To investigate increases in data rates via the use of several pixels in an array, we built a scalable, integrated VLC system consisting of a: micro-LED array; CMOS LED drivers; and a 3 by 3 avalanche photodiode array, fabricated with a 0.18 μm CMOS process. With this approach, every micro-LED can transmit identical data (a so-called ‘ganging’ mode), in order to increase the power of the transmitted signal. Alternatively, the system can operate in MIMO mode, with each pixel transmitting a separate data stream. Another degree of flexibility is associated with the handling of the output of the detectors in the receiver array, which can be summed together or read out separately. When operating transmitters and receivers in the MIMO mode, we have realised a data rate of 1 Gb/s over a distance of 1 m (see Figure 4)

Another area of our research concerns ‘colour-converters’. These are materials that can be used in combination with LEDs to generate white light – and can also enable devices to generate signals at multiple wavelengths, as this provides an opportunity for wavelength-division multiplexing. The vast majority of commercial white-emitting LEDs generate their broad emission by using a blue LED to pump yellow-emitting cerium-doped YAG phosphor. White light results from the colour mixing of blue and yellow. This approach is an efficient way to generate white light, but the device that results is far from ideal for communication. That’s because the phosphor has a very long excited state lifetime – it is of the order of microseconds – so it is slow to respond to modulation signals.

Due to this issue, the majority of researchers that

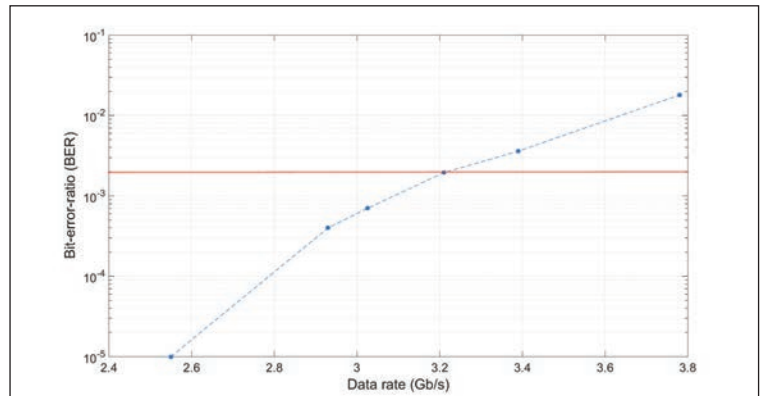


Figure 3. The measured bit-error-ratio (BER) – that is, the ratio of the total transmitted bits to the total incorrectly-transmitted bits – as a function of data rate for single micro-LED orthogonal frequency-division multiplexing. The red line indicates a BER of 2×10^{-3} , below which a technique called ‘Forward error correction’ can be used to correct any errors in the bit stream. This comes with a 7 percent overhead penalty, so the ≈ 3.2 Gb/s point on the figure corresponds to the error-free 3 Gb/s.

are developing VLC systems completely filter out the phosphor emission at the receiver, to leave just the comparatively fast signal from the blue-emitting LED die. Two major downsides result from this approach: A substantial proportion of the optical output of the LED is not used to transmit data, and the yellow component of the emission is not used to realise parallel data transmission at multiple wavelengths.

To address these weaknesses, we are investigating alternative colour-converters. Like conventional phosphors, they can be paired with an LED to create white light, but the critical difference is that they have a much faster response – typically, it is in the regime of nanoseconds to tens of nanoseconds. With this approach, the colour-converted emission can be used as a high-speed optical data channel, rather

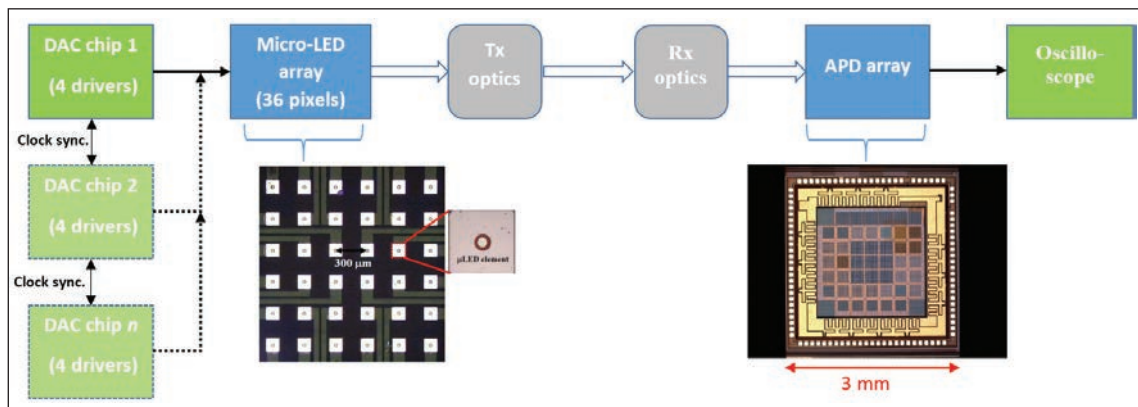
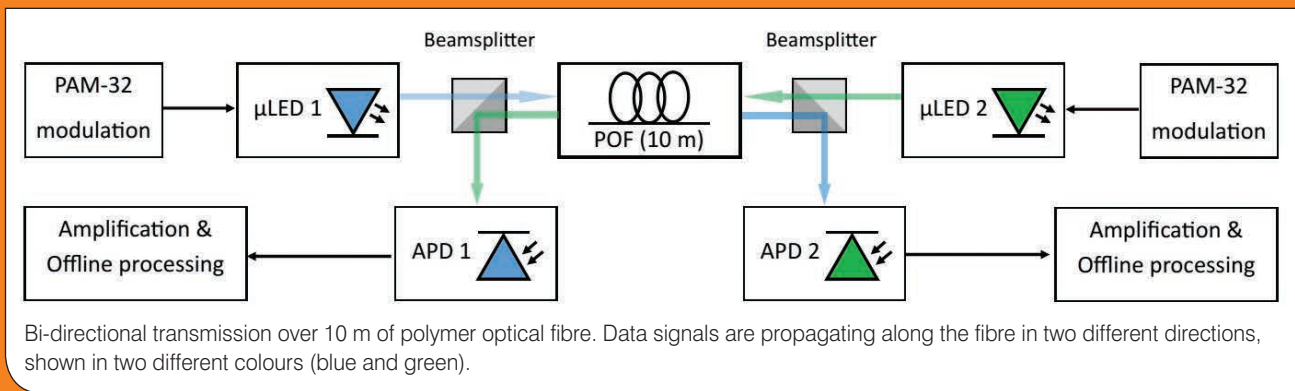


Figure 4. A custom scalable, integrated VLC system can be constructed from a micro-LED array and an avalanche photodiode array are also shown.

LEDs and plastic optical fibre

POLYMER OPTICAL FIBRE (POF), being far cheaper and more robust than its silica-based counterpart, is often used in short-haul networks, such as in-home or automotive data links. Meanwhile, its cousin, the polymer optical waveguide, is a promising technology for realising next-generation, high-speed rack-to-rack, board-to-board or chip-to-chip interconnects in scenarios where traditional copper-based electrical interconnects are challenging to realise, due to issues including electromagnetic interference. In all these forms of polymer waveguide, the lowest absorption losses are found in the blue-green region of the visible spectrum, making GaN LEDs a very attractive candidate for the transmission source.

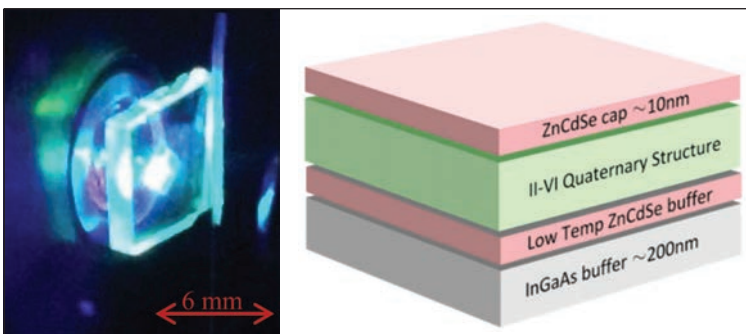
Researchers at the Universities of Strathclyde and Cambridge have recently demonstrated simultaneous, bi-directional transmission over 10 m of POF at 5 Gb/s. This involved the use of beam-splitters at each end of the POF to separate the transmitted and received signals. This is the highest reported data rate for an LED-based POF link. The downside of using beam-splitters is a 6 dB power loss. To address this, the researchers are currently investigating alternative, lower loss approaches for implementing bi-directional transmission. Another goal is to demonstrate wavelength-division multiplexing.



than being discarded, which is the case for LEDs incorporating yellow YAG-based phosphors. Our trials with a blue micro-LED and a yellow-emitting polymer colour-converter have enabled data transfer at 1.68 Gb/s, which is the highest value for VLC for a single white-emitting source.

A second option that we are exploring is to unite a GaN device with a membrane of II-VI material with a very fast response time. By capillary-bonding a green-emitting II-VI platelet to an LED, we have created a source with a modulation bandwidth of 145 MHz (see Figure 5). As well as generating white light, these materials could potentially be patterned, enabling the construction of multi-colour, micro-LED arrays. These multi-colour sources could transmit multiple data streams simultaneously over free-space or routed through a waveguide.

Figure 5. One option for colour conversion using materials with very fast lifetimes is to use a blue-emitting (450 nm) micro-LED to optically excite a green-emitting II-VI membrane.



While the development of LED lighting will continue to be driven by demand for high-quality, highly-efficient solid-state lighting, the results emerging from our UPVLC project highlight the capability of these devices to deliver very high data rates, once they have been adapted and optimised for communication.

With society's ever-increasing reliance on wireless data communication, one promising solution to the ever increasing demand for data is high-speed VLC based on GaN LEDs.

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Heat sinking GaN-on-silicon: the substrate removal challenge

Removing thermal boundaries and adding thermal pathways help devices to keep their cool

BY MARKO TADJER, TRAVIS ANDERSON, JENNIFER HITE, JORDAN GREENLEE, KARL HOBART AND FRITZ KUB FROM THE UNITED STATES NAVAL RESEARCH LABORATORY

IF AN ELECTRONIC DEVICE is to be a major commercial success, it has to deliver great performance at an affordable price.

Judged in these terms, GaN-on-silicon technology is very promising. HEMTs formed with this material system have many great attributes – including a high mobility, a high critical field and a high current density – and they can be produced at relatively low cost, thanks to manufacture in mature silicon processing lines.

One perceived weakness with this class of device is that its performance is held back by the large mismatches in the lattice constant and the coefficient of thermal expansion between GaN and silicon (111). However, tremendous

progress in epitaxial technology over the past few years has addressed these concerns, and today AlGaIn/GaN-on-silicon HEMTs compete in performance with cousins made on SiC. Thanks to their performance parity with GaN-on-SiC, there is a good chance that HEMTs made on silicon could see insertion into high-fidelity applications, such as airborne radar in the L-band to X-band regime.

GaN-on-silicon devices that can be used for power and RF switching are thermally limited. This restriction actually affects all semiconductor devices, but with GaN-on-silicon the impact is particularly significant because of their aforementioned electrical performance advantages. Consequently, the downsides of a higher device operating

temperature are not limited to a lower gain and efficiency, but also include reliability concerns.

These reliability-related issues stem from the structure of the device. Although advances in GaN-on-silicon technology have enabled the production of very high quality, low-dislocation density GaN buffer layers, realising a high-quality heterostructure requires thick, highly defective AlGaIn and/or AlN nucleation layers on the substrate side (see Figure 1).

These layers, combined with a relatively thick SiN passivation on the device side, create a GaN-on-silicon HEMT that is optimized for electrical performance, but has an electrothermal performance that is impaired by a low thermal conductivity





for the nucleation and passivation layers (see Table I). For the nucleation layers, the thermal conductivity diminishes near the silicon substrate, due to the increase in defect density. Another issue is the use of ternary nucleation layers, such as AlGaN – this has a lower thermal conductivity than its binary constituents, AlN and GaN.

To improve the electrical performance of the GaN-on-silicon HEMT several groups have pioneered approaches associated with substrate-side engineering. This includes Farid Medjdoub's group at IEMN that has increased the breakdown voltage of the device through localized removal of the silicon substrate beneath the transistor (see, for example, *Compound Semiconductor* Nov&Dec p. 58 (2015)), and the team led by Prof.

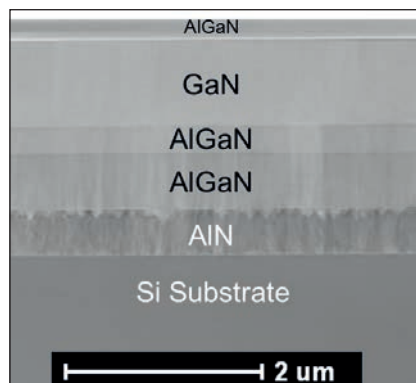


Figure 1. Transmission-electron microscope image of a GaN-on-silicon wafer cross section.

Tomás Palacios at the Massachusetts Institute of Technology that have delivered a hike in breakdown voltage by switching from a silicon substrate to one made with quartz.

At the Naval Research Laboratory in Washington DC we are taking a holistic approach to improving the performance of the HEMT. We are not limiting our efforts to optimising electrical performance, but also aiming to build a device that delivers its best, in terms of its thermal and mechanical characteristics. We believe that the silicon substrate is an essential ingredient for the ultimate success of the GaN-based HEMT, and we are investigating whether improvements can be wrought from removing the substrate and accessing the nucleation layers, which might ultimately be

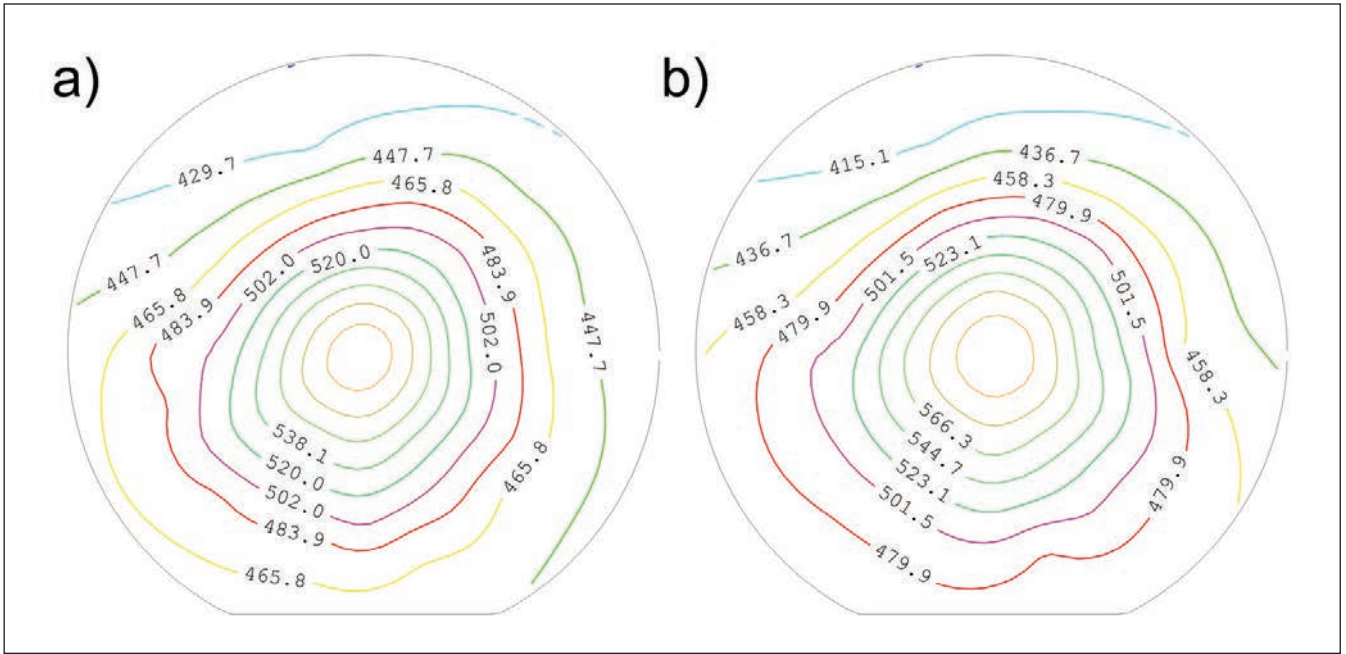


Figure 2. Thinning the silicon substrate from 575 μm to 200 μm (a) and 150 μm (b) did not produce any significant change in the sheet resistance profile.

replaced with effective, substrate-side, electrothermal passivation.

We are not alone in exploring the possible benefits of substrate removal. Palacios' team at MIT have carried out dry plasma etching of silicon beneath the AlGaIn/GaN heterostructure, and they found an increase in the carrier density of the two-dimensional electron gas following substrate thinning from 500 μm to 350 μm. Further etching

was detrimental, however, with cracks in the GaN epilayer and reduced electrical performance occurring for devices with silicon substrates thinned to 150 μm.

The origin of the epiwafer cracks is not clear to us. High-power plasma etching causes wafers to heat up, and cracks might stem from the additional stress induced by heating, or by etching – or even by a combination of the two. As

we are keen to know if our device process is limited by the lattice or thermal mismatch of GaN and silicon, we have investigated the impact of substrate thinning processes on device performance.

Efforts began by studying the consequences of substrate thinning on the characteristics of AlGaIn/GaN-on-silicon HEMTs. MOCVD-grown 4-inch epiwafers with 575 μm-thick (111) silicon substrates were thinned to 200 μm and 150 μm at room temperature by backgrinding and chemical mechanical polishing.

We evaluated the strain in these epiwafers with wafer curvature interferometry and Raman spectroscopy. Strain increased with processing, being inversely proportional to final substrate thickness. However, sheet resistance was nearly unchanged, prompting us to fabricate devices from our thinned epiwafers (see Figure 2 for maps of sheet resistance).

The characteristics of the material degraded after ohmic contact annealing. Sheet resistance shot up by more than 150 percent, according to transfer

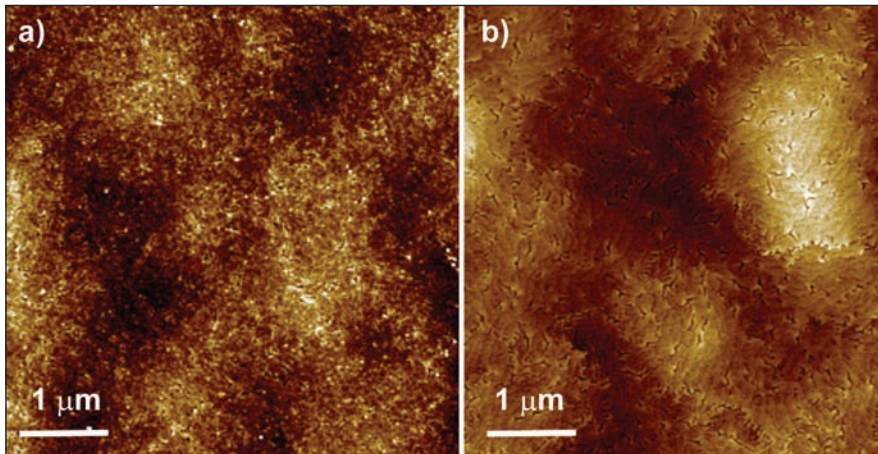


Figure 3. Atomic force microscope images of the AlGaIn surface of a sample from wafer B (a) before and (b) after an 850 °C, 30 s anneal in N₂ atmosphere. Each image covers a 5 μm x 5 μm surface area.

Material	Thermal Conductivity W/cm·K	Specific Heat J/g·K	Bulk Density g/cm ³	Thermal Diffusivity cm ² /s
Si	$1.48 \cdot (300/T)^{1.4}$	0.7	2.33	0.91
SiN	0.1	0.67-1.1	2.37-3.25	0.04
GaN	$1.6 \cdot (300/T)^{1.3}$	0.49	6.15	0.53
AlN	2.85	0.6	3.255	1.46
4H-SiC	$4.0 \cdot (300/T)$	0.69	3.1	1.87
Diamond	33	0.52	3.52	18.02

k – thermal conductivity, ρ – bulk density, C_p – specific heat, a – thermal diffusivity, $a=k/(\rho \cdot C_p)$.

Table 1. Thermal Properties of Relevant Device Materials

Wafer/ Sample	Thickness μm	R_{SH} Ω/sq.	ΔR_{SH} %	$E_{2,GaN}$ cm ⁻¹	$\Delta\sigma_{XX}$ GPa	Bow μm
A	575	480.6	-	567.03	-	41
B	200	501.7	4.3	567.31	0.81	220
B+RTA	200	1289	168	567.49	1.33	-
C	150	504.2	4.9	567.52	1.42	314

Table 2. Comparison of AlGaIn/GaN HEMTs as a function of substrate thickness and high temperature annealing.

length measurements (see Table II), and shallow cracks appeared on the surface of the AlGaIn barrier (Figure 3). The cause of all of this degradation is the high-temperature contact anneal, which relaxed the stress that built-up in the heterostructure by partial substrate removal. Transistors formed from these thinned epiwafers suffered from a low drain current density and a fall in channel electron density – it is about a third of its original value, based on Hall measurements. This particular investigation highlights the thermal fragility of AlGaIn/GaN heterostructures, which can be compromised by the large difference between the coefficient of thermal expansion of GaN and that of silicon.

Two options for avoiding the hike in sheet resistance caused by rapid-thermal annealing are to carry out ohmic contact deposition prior to substrate thinning, and to employ a non-alloyed ohmic metallization process. We would like to

go one better, however, and do away with the silicon substrate altogether.

Success will hinge on developing a process that can remove all of the silicon without damaging the heterostructure, and without introducing additional thermal boundaries in the device. Our plan is that after removing the silicon substrate, having temporarily attached our epistructure to a thermally-matched carrier wafer, we will deposit on our III-Ns, at a high temperature, a thick, high-thermal-conductivity layer of diamond.

We believe that replacing the silicon substrate with a high thermal conductivity material, such as diamond, will aid the production of GaN transistors delivering optimal electrothermal performance. The ultimate improvement in electrothermal performance, however, will not result from just removing the silicon substrate – it will require a stripping away of all the low thermal conductivity layers in the heterostructure. This is a challenge

for us and other developers of GaN HEMTs, with success requiring new device processes and novel HEMT architectures.

- The authors are grateful for the STEM imaging by Prof. Petra Specht (UC Berkeley), as well as the NRL Nanoscience Institute Staff for processing equipment support.

Further reading

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Designing power conversion systems with fewer, higher-voltage MOSFETs cuts component count, increases reliability and has little impact on the total area of the chips

BY VIPINDAS PALA, EDWARD VAN BRUNT AND JEFFREY CASADY FROM WOLFSPEED



Simplifying power conversion with medium voltage SiC MOSFETs

THE START of this decade heralded a new era for power electronics. Back then, commercial SiC power MOSFETs hit the market with operating voltages spanning 900 V to 1700 V. These rivals to the silicon incumbents attracted a great deal of interest from the outset, because they enable material and operating cost savings at the systems level, and improved efficiencies. These advantages have driven interest in the use of SiC MOSFETs for solar inverters, automotive charging systems, induction heating, welding power supplies, and a variety of additional power conversion applications.

Benefits of replacing silicon IGBTs with SiC MOSFETs result from the superior properties of the wide bandgap device. It slashes switching losses by a factor of 5 to 40; it does not suffer from a knee voltage, so conduction losses can be far lower; and it has a high performance body diode, so there is no need to pair it with an external antiparallel diode in applications requiring bi-directional conduction.

To increase the number of applications that SiC MOSFETs can serve, manufacturers of these devices

have extended their capability to higher voltages. These efforts have included the development and evaluation of medium-voltage SiC switch devices, which span the 2.5 kV to 15 kV range, in traction applications.

Examples of this are Mitsubishi Electric's development of a 3.3kV SiC MOSFET power module for electric trains that yielded operating savings of 40 percent when power operation and regeneration modes were considered; and efforts by researchers at Fraunhofer ISE that explored the use of 10 kV SiC MOSFET switches for flexible photovoltaic power transmission from a 400 V panel to the grid. In the latter application, the switch from traditional transformers to SiC-based power conversion architectures increases the voltage for power transmission – and this has led to less copper cabling, higher efficiency, and greater flexibility in accommodating photovoltaic arrays with differing levels of power generation.

At Wolfspeed, a Cree Company, we have a rich history in the development and production of SiC MOSFETs. We were the first to bring these transistors to market,



Medium voltage (2.5 kV – 15 kV) SiC transistors are being explored for use in rail and in photovoltaic panel to grid power transmission. SiC transistors have demonstrated up to 40 percent operating savings in the rail market, and allow new approaches in photovoltaic panel to grid power distribution.

and during the intervening years we have improved device performance and expanded the range of blocking voltages. The 3.3 kV, 6.5 kV, and 10 kV SiC MOSFETs that we have developed are currently being evaluated by strategic leaders in rail, HVDC, grid-tied power distribution, and renewable energy grid storage applications. Their investigations offer important insights for engineers working with medium voltage applications above 100 kW and considering SiC devices for maximizing power density and driving down system complexity.

When engineers are designing these medium voltage power converters, one key decision that they face is whether to use higher voltage, lower current SiC MOSFETs connected in parallel, or lower voltage, higher current MOSFETs connected in series. Both approaches can deliver the desired voltage and power levels, and selecting the right way forward is more than just a matter of totting up the cost of the SiC die.

One of the merits of using medium-voltage SiC MOSFETs, rather than lower voltage variants, is that it enables simpler topologies with fewer levels

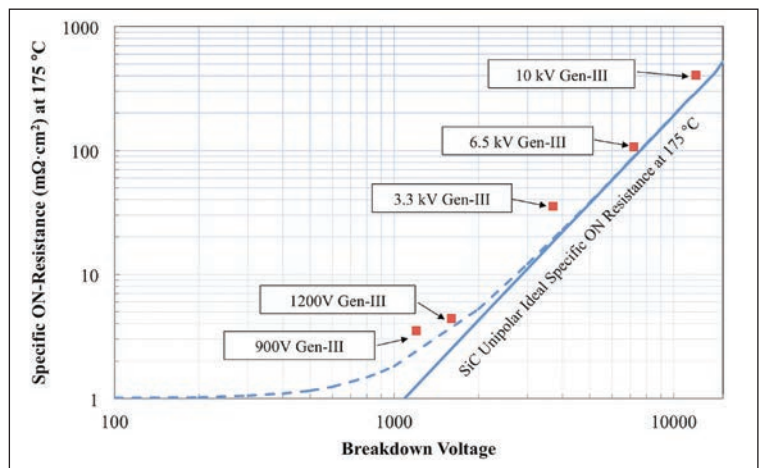


Figure 1: Examining the specific on-resistance at 175°C, the SiC unipolar ideal value is contrasted with the measured results of Wolfspeed’s new Gen III SiC MOSFETs. Close agreement can be seen at higher voltages where the drift region resistance is dominant. The dashed line represents parasitic resistance of 1mΩ·cm² from ohmic contacts, channel resistance, etc. The data points represent the actual breakdown voltage of the device, while the labels represent the device voltage rating.

“

For the body diode characteristics, which occur when a reverse bias gives rise to reverse current, the 10 kV SiC body diode produces the lowest forward drop. This advantage, which results from minority injected conductivity modulation in the drift region, highlights one of the benefits of selecting a single MOSFET operating at a higher voltage, rather than a string of lower voltage devices

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and components. Cutting component count is very attractive, because it leads to higher reliability as there are fewer components that can fail. It is not just the number of MOSFETs that falls with this approach. The reliability of power converters also increases via fewer wirebonds inside a module, and a cut in the module, gate driver, and passive component count. Working with fewer components also simplifies design.

Generation III

We are now developing our third-generation MOSFETs, which have voltages spanning 900 V to 15 kV. The merits of these transistors include a high reliability planar device structure and simple gate drive requirements. Another feature is the robust, low-reverse-recovery body diode, which enables significant system-level circuit design enhancements

with regard to power density, cost, and reliability.

When engineers are faced with the task of selecting the most suitable SiC MOSFETs from our portfolio for a medium-voltage, high-power application, they must compare the measured performance, in terms of on-resistance as a function of breakdown voltage (see Figure 1). The downsides of a higher-voltage MOSFET are an overshoot of voltage during switching, and the additional voltage de-rating required to avoid device failure induced by terrestrial cosmic rays. In future, we will examine both of these limits in detail; for the purposes of this analysis, we will assume that SiC power MOSFETs, when properly designed and implemented in low-inductance modules, can operate at up to 80 percent of the rated voltage.

For lower voltage parts, parasitic resistances prevent the device from delivering its theoretical performance. These resistances come from the ohmic contacts, the channel, and the substrate. Together they contribute at least $1\text{m}\Omega\cdot\text{cm}^2$, which is a fairly significant portion of total device resistance in MOSFETs rated below 1.7 kV.

To obtain a clearer picture of the expected MOSFET chip performance, the rated current density of our Gen III SiC MOSFET chips in a typical module thermal environment must be compared with the rated breakdown voltage at 175°C. We have undertaken this, measuring the SiC current density of each chip in a module environment (see Figure 2).

Armed with these figures for the rated current for the SiC MOSFET in a module environment we can obtain a figure of merit that is representative of the power density of each SiC MOSFET at 175°C (see Figure 3). Using this figure of merit – the product of rated current and rated voltage – we have, for the first time, been able to identify the amount of SiC needed, based on the selected MOSFET voltage rating.

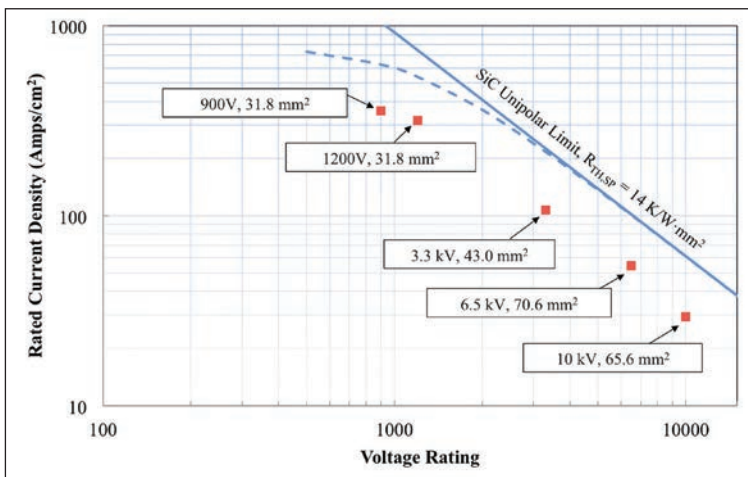


Figure 2: Rated current density of Wolfspeed Gen III SiC MOSFET chips in a typical module thermal environment, compared to rated breakdown voltage at 175°C, assuming a SiC unipolar limit of 14KW/mm², with an AlSiC baseplate and 750 μm-thick AlN substrate. The dashed line represents the additional thermal limit from parasitic channel and contact resistance.

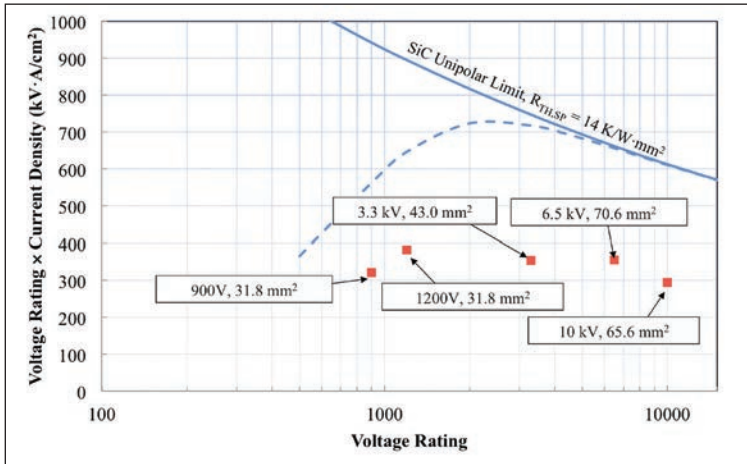


Figure 3: The measured power-density figure-of-merit of Wolfspeed Gen III SiC MOSFET chips in a typical module thermal environment compared to rated breakdown voltage at 175°C, assuming a SiC unipolar limit of 14 K/Wmm² with an AlSiC baseplate and 750 μm-thick AlN substrate. To implement a 10 kV switch, the amount of SiC used is relatively independent of the voltage rating of the chip between 1.2 kV and 6.5 kV. The dashed line represents the additional thermal limit from parasitic channel and contact resistance.

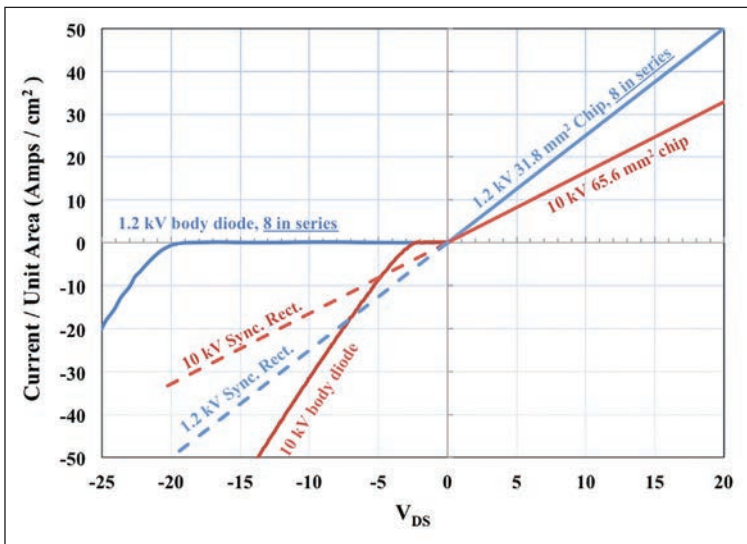


Figure 4: A comparison of the forward and reverse characteristics of eight series-connected 1.2 kV SiC MOSFETs and one single 10 kV SiC MOSFET chip at 175 °C. For the body diode characteristics (reverse bias, negative current flow), the 10 kV SiC body diode has the lowest forward drop due to minority injected conductivity modulation in the drift region.

This analysis is illuminating. One important insight is that for SiC MOSFETs spanning 900 V to 10 kV, the power density figure of merit remains very close to 350 kVA cm⁻² and varies by only 24 percent. And if we just consider the 1.2 kV, 3.3 kV, and 6.5 kV SiC MOSFETs, the achievable system power density per unit device area only varies by 7 percent. This is by no means an ideal limit, though. It should be possible to go beyond 400 kVA/cm² by building bigger die with a higher channel mobility, a reduced edge termination area and fewer defects.

So far, our analysis of SiC MOSFETs with different voltage ratings has been limited to considering only forward conduction. A rigorous assessment must go further, including anti-parallel current flow through the body diode and the channel of the MOSFET.

A key difference between the silicon IGBT and the SiC MOSFET is that the voltage range of the wide band gap device can utilize both the internal body diode and the channel of the MOSFET for anti-parallel current flow.

We have considered the impact of reverse characteristics when evaluating two options for a 10 kV switch: a single 10 kV SiC MOSFET; and eight, 1.2 kV SiC MOSFETs connected in series (see Figure 4). For the body diode characteristics, which occur when a reverse bias gives rise to reverse current, the 10 kV SiC body diode produces the lowest forward drop. This advantage, which results from minority injected conductivity modulation in the drift region, highlights one of the benefits of selecting a single MOSFET operating at a higher voltage, rather than a string of lower-voltage devices.

Our comparison of using SiC MOSFETs with different voltage ratings in medium-voltage power applications reveals that the total area of SiC material used is largely independent of voltage rating, giving designers the flexibility to choose the topology, part count, and system size that best suits their needs.

This makes higher rated SiC MOSFETs, such as 3.3 kV, 6.5 kV and 10 kV transistors, an attractive option, as they enable systems with simpler topologies, smaller part counts, and smaller physical sizes. On top of this, higher-voltage MOSFETs are favoured for their lower drop at reverse bias.

Further reading

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Targeting radar with 150 V RF GaN HEMTs

Drain engineering increases the operating voltage of GaN HEMTs, enabling them to combine unprecedented power, gain and efficiency with great reliability

BY GABRIELE FORMICONE, FOUAD BOUERI, JEFF BURGER, JAMES CUSTER
AND JOHN WALKER FROM INTEGRA TECHNOLOGIES

There is plenty of room for improvement in the high-power radar systems operating in the UHF band. Lying at the heart of the majority of these systems are travelling-wave tubes, which are bulky, fragile and have an efficiency that is limited to about 65 percent. Replacing these tubes with solid-state devices could increase efficiency and robustness, and also enable a number of other improvements, including: the introduction of lower voltage power supplies, a move to a more flexible, modular design that is easier to maintain, and a reduction in long-term system costs.

Although there are several solid-state technologies capable of delivering an output in the microwave region, most are not that attractive for deployment in high-power radar. Silicon devices, such as the bipolar junction transistor and the vertical and lateral diffused MOSFET, are used in several radars from VHF to S-band and have an output power capability that is somewhat limited. Meanwhile, attempts to take significant market share with the SiC static induction transistor have failed, due to a gain of less than 10 dB and an efficiency of barely 50 percent at 450 MHz.

A far more promising technology is the GaN-based HEMT. In general, its transmit power is held back by its operating voltage, which is typically 50 V or below up to S-band. However, thanks to sophisticated drain engineering technology developed by our team at Integra Technologies of El Segundo, California, operating voltages can reach 150 V. This leads to a dramatic improvement in output characteristics. Pulsed power densities can reach 30 W/mm, equipping radar manufacturers with a solid-state device for producing an output power of several

tens of kilowatts. What's more, our HEMTs provide unprecedented gain and efficiency, combined with good reliability.

These devices are a part of our portfolio that includes more common products operating at power supply voltages of 28 V and 50 V. By supplementing these more standard offerings with variants operating at higher voltages, we are setting ourselves apart from our peers and expanding the markets that we serve – although we are highlighting radar, high-power RF amplifiers operating at high voltages can also be used for applications in particle accelerators, microwave sintering, as vacuum tubes replacement in general, and other applications involving industrial, scientific and medical radio bands.

Device development and production takes place at our 6-inch all-gold metallization silicon wafer fab, which includes equipment re-tooled to process

4-inch GaN-on-SiC wafers. By adopting this approach, as our GaN sales grow, we can meet the need for increased production by switching production to 6-inch wafers. This transition will double capacity, while trimming production costs.

At our headquarters, we have a fully owned 22,000 square-foot facility with a clean room. To further support design, we have another 4,000 square-foot of space in research centres in other locations.

To eliminate the risk of failing to fulfil customer orders, we employ a dual source strategy, working with domestic foundries and partners. We avoid outsourcing all production, however, because we believe that by owning a fab, we are better positioned to support customers for the expected operational

lifetime of the devices, which is in excess of 30 years. During this time, supplies can be disrupted through mergers, acquisitions, natural disasters and unforeseen eventualities.

Increasing the power

At our facility we have demonstrated the virtues of our high-voltage HEMTs by measuring the increase in output power with bias voltage. Using an operating frequency of 430 MHz, a pulse width of 100 μ s and a 10 percent duty cycle, we have found that operation at 75 V, 100 V, 125 V and 150 V produces a saturated output power of 150 W, 250 W, 350 W and 450 W, respectively (see Figure 1).

What is particularly pleasing is that the benefits of an additional 25 V of bias are not limited to a 100 W hike in the saturated output power. Instead,



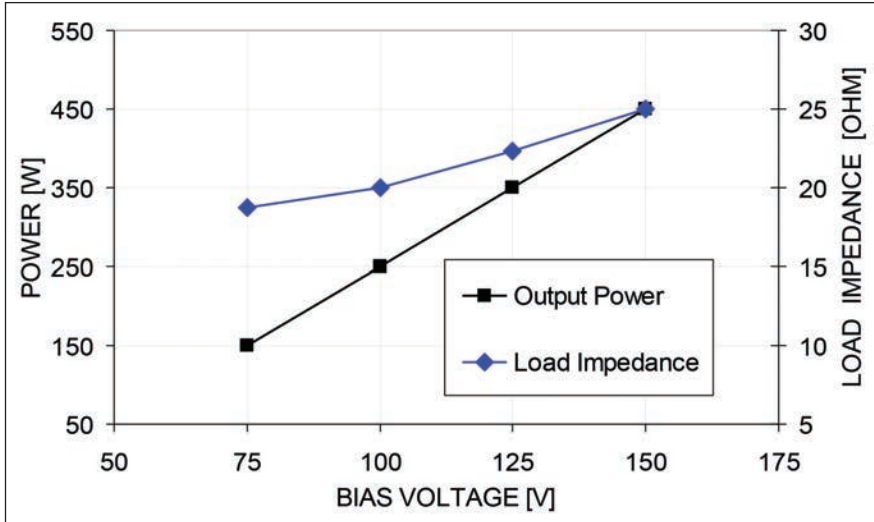
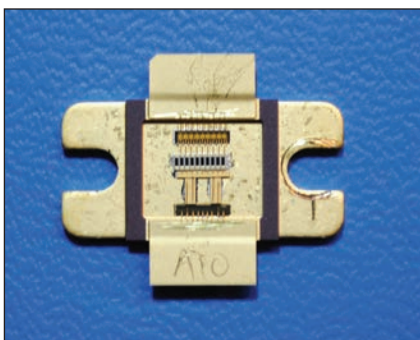


Figure 1: Saturated output power and terminal load impedance of a 15 mm, high-voltage GaN transistor. On the right hand side is the corresponding load impedance the transistor requires for optimum match. At 150 V, the 450 W device has a load impedance of 25 ohms, which is straightforward to match to 50 ohms. This medium-size transistor has an array of 60 gate fingers, each with a length of 250 mm. This die, which has dimensions of 3.9 mm by 1.0 mm, has been optimized to provide stable and reliable operation.

they extend to an increase in the load impedance, so that it is closer to that needed to deliver maximum output power to a 50 ohm load, such as an antenna. Note that the load impedance of all RF power transistors, regardless of the materials they are made from, is relatively low, with efforts to increase the output power via an increase in gate periphery paying the expense of a lower load impedance. The smaller it is, the larger the impedance transformation required to match it to 50 ohms – and the greater the output loss and reduction in efficiency.

The substantial success that we have had begs the question: given that a



15 mm 150 V GaN transistor, with no internal output match and a LCL input match. The internal output match is not used so that optimum fundamental and harmonic impedances can be adjusted outside the device package.

higher operating voltage produces the dual benefit of a higher output power and a higher load impedance, why is this approach not standard within industry?

The answer is that to operate at a higher voltage, the transistor must withstand a higher breakdown voltage. And to realise this and avoid catastrophic failure, the drift region of the device must be extended. Since this is the most critical region of a high-voltage RF transistor, this modification, which is known within the industry as drain engineering, is challenging and must be carried out with great care.

Even optimal drain engineering produces an increase in the transistor's on-resistance, which translates to a higher loss and diminished radar efficiency. However, this loss in efficiency is minimised with our state-of-the-art drain engineering and field plate techniques. Combining these two results in a high breakdown voltage, while minimizing impact on the on-resistance.

With AlGaIn/GaN HEMTs there are more options than there are with silicon technologies, such as LDMOS, for increasing the breakdown voltage while making minimal impact on the on-resistance. One avenue, which we have taken, is to increase the breakdown voltage by adding iron into the buffer layer – a similar response results from a small incorporation of aluminium.

When adopting either of these approaches the key is to not be too aggressive and impair reliability. If aluminium or iron is added improperly, although on-resistance will appear to be low under DC operating tests, it will increase dynamically under RF operation; this process in GaN devices is called DC-RF dispersion, and it is very detrimental to RF device performance.

To avoid these issues, comprehensive optimisation must take place that considers the drift region length, locations of field plates, and the iron and aluminium content in the device buffer layer. Get this just right and it is possible to minimize the transistor on-resistance, realise acceptable RF performance and enable operation at a targeted voltage.

Excelling in efficiency

As well as producing very high output powers, our devices excel in efficiency. This exceeds 70 percent at voltages ranging from 75 V to 150 V, and peaks at 78 percent at 100 V (see Figure 2 for details). The reason why the efficiency is highest at this voltage is that the test fixture had been used for a previous project, where harmonic tuning techniques were used to optimize power at 100 V bias. Retuning the test fixture harmonic impedances will enable the efficiency at 150 V to get close to 80 percent. This adjustment is guaranteed to pay dividends, as it has already succeeded with devices operating at 75 V.

Turning to gate pulsing, a mode of operation often used for radar, can deliver a further efficiency gain of 5 percentage points on average. This can propel the efficiency of our 450 W devices, which have a gate periphery of just 15 mm, to over 80 percent at 150 V. Operating in this manner, gain is well above 22 dB, indicating that our 150 V GaN technology promises to perform well at higher UHF frequencies, as well as in the L-band, where it could serve pulse radar.

In comparison, a SiC static induction transistor operating at the same frequency produces just 10 dB of gain, and struggles to realise 50 percent drain efficiency. The lower gain has unwanted consequences: an additional transistor is needed to drive the output stage, leading to a circuit with a larger footprint and an even lower efficiency at the system level.

The route to realising even higher powers, which might be needed for applications such as pulsed radar, is to increase the size of the gate periphery.

Given the high initial impedance, lowering this is not expected to have any major drawbacks. (Note that we already have experience of devices with a larger gate periphery, as we have used more traditional 50 V GaN transistors with a 36 mm gate periphery in a multi-chip package that produces a S-band output power of 1 kW. In the L-band, we also use larger chips, which have a 50 mm gate periphery.)

If we increase the gate periphery of our 150 V device from 15 mm to around 40 mm, this will create a single chip delivering a saturated output power in excess of 1 kW. Although load impedance will fall from scaling, it would still be just over 11 ohms, which is very manageable from an impedance matching perspective. There is also the opportunity to form a four-chip, 4 kW device in a single-ended ceramic package with an output load impedance of around 3 ohms, and a six-chip, 6 kW variant in a dual lead package with a load impedance of around 2 ohms.

As well as considering the impedance of these devices, which at these power levels are in a very comfortable region from an impedance matching perspective, we must consider issues related to thermal management. For our 15 mm device driven with 100 μ s pulses and a 10 percent duty cycle, according to our model, thermal resistance is 0.5°C/W at a case temperature of 26 °C (it is 2°C/W in CW operation, which is not recommended). When operating at

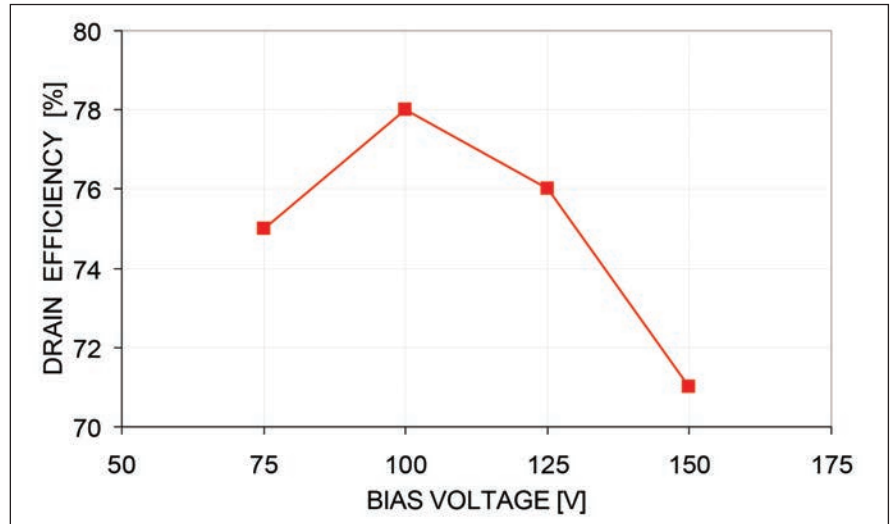


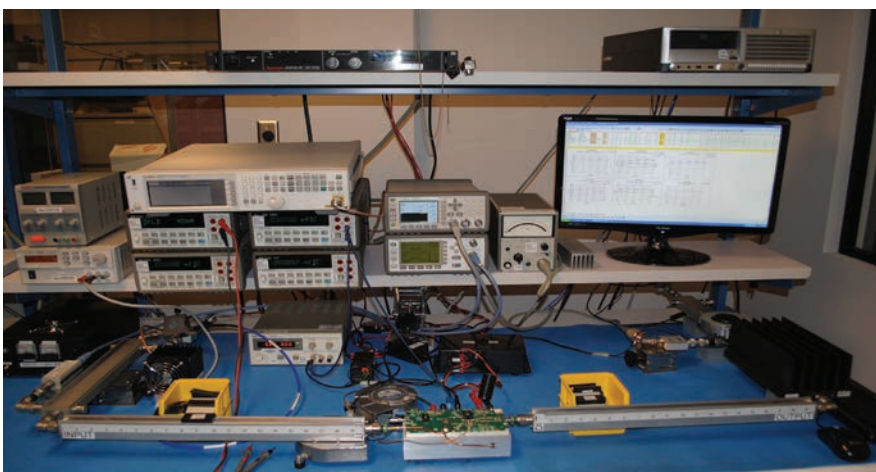
Figure 2: Drain efficiency at saturated output power for a 15 mm, high-voltage GaN transistor. The efficiency is calculated based on average current during the 100 μ s pulse with a 1 ms period (or 10 percent duty cycle); in radar operation it is common to shut-off the device when the pulse is off through a gating circuit. This procedure has the effect of increasing the efficiency values reported above by an average of 5 percentage points.

80 percent efficiency and producing an output of 1 kW, the DC power supplied to the die is 1.25 kW, so it dissipates 250 W. This would lead to a peak junction temperature during the 100 μ s pulse of 150°C, which is well within the regime of reliable operation. In fact, the temperature will be below this, because the length of the fingers must be extended for a 1kW die design, and this modification drives down thermal resistance.

To ensure high reliability, our chips are housed in a nickel- and gold-plated package that is hermetically sealed with a gold-tin solder. Gold bond wires, formed with a highly precise, automated machine, enable the highest levels of repeatability and consistency in RF performance. We

have no doubt that our 150 V transistors set a new benchmark for the performance of solid-state devices for ultra-high power pulse radars in the UHF band. Preliminary data suggests that a single device with an output power in excess of 5 kW can provide 20 dB of gain and a drain efficiency of more than 70 percent.

The load impedance for this device, which would contain six larger chips and be housed in a dual lead industry-standard package, is higher than 2 ohms, making it easy to match to 50 ohms. Customers can obtain customised variants of this technology to meet their particular requirements, and a greater range of options should be available in future, as we expand our products to a wider range of frequency bands.



Test station used to develop the high efficiency impedance matching for the 150 V GaN HEMT

Further reading

G. Formicone *et. al.* "Analysis of a GaN/SiC UHF Radar Amplifier for Operation at 125V Bias", 2015 European Microwave Week, France.

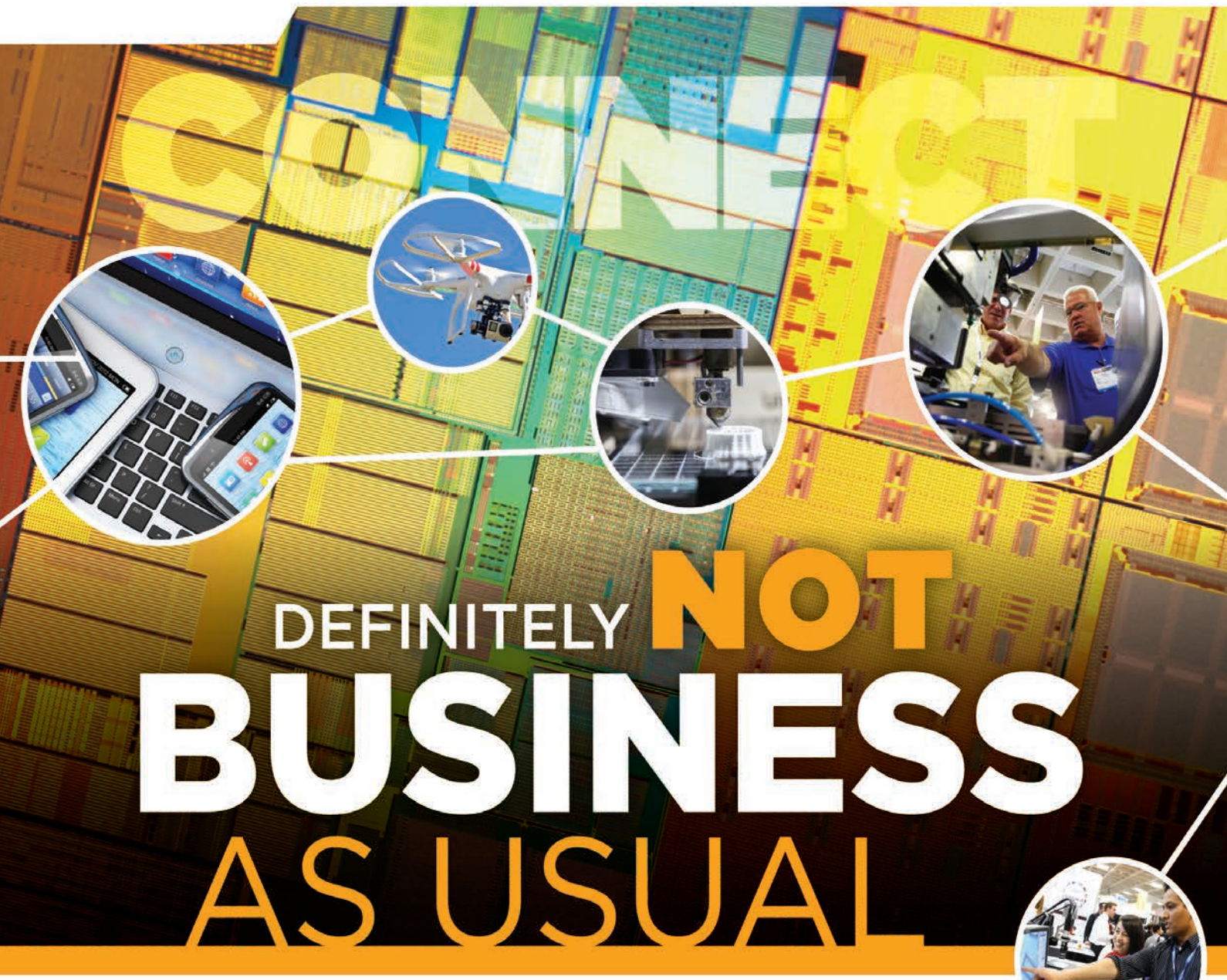
G. Formicone *et. al.* "Mixed Mode Class EF-1 High Efficiency GaN Power Amplifier for P-Band Space Applications," IEEE International Microwave Symposium, 2015.

J. Walker *et. al.* "A 1kW S-Band GaN Radar Transistor", IEEE COMCAS-2013, Israel

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The promise of truly two-dimensional transistors

Combining molybdenum disulphide channels with graphene electrodes creates high-performance transistors that consume very little power.

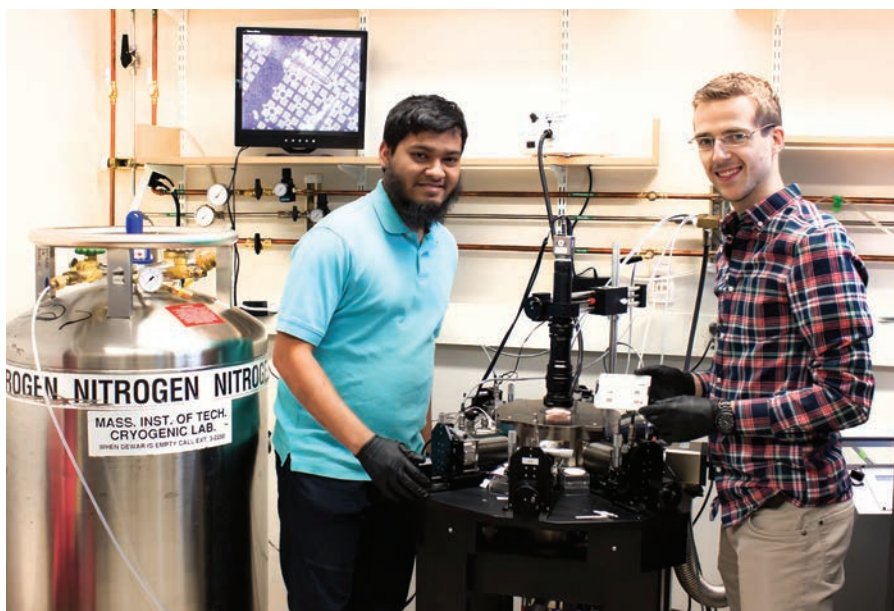
BY AMIRHASAN NOURBAKHSI, LILI YU, AHMAD ZUBAIR AND TOMÁS PALACIOS FROM MASSACHUSETTS INSTITUTE OF TECHNOLOGY

THE DAYS OF the silicon transistor are numbered. Increasing the transistor count on an IC through a reduction in the size of the device, and the power required to operate it, may continue throughout this decade. But if the march of Moore's law is to continue in the 2020s, it will require the introduction of alternative materials with superior characteristics to silicon, allied to the development of new device architectures.

Much of the effort associated with the development of devices sporting new materials has focused on high electron mobility III-Vs, such as InGaAs, that can be paired with germanium, a material that can transport holes at high speeds. Transporting carriers at higher mobilities than silicon is a tremendous asset, as it can enable a cut in the transistor's operating voltage while maintaining the current flowing through this device. Lowering the voltage is highly beneficial on two fronts: it reduces chip heating; and it cuts the power consumption per transistor, enabling mobile technologies to introduce more powerful ICs while maintaining battery life.

Device fabrication typically involves the deposition of films of either germanium or III-V heterostructures onto silicon substrates, which may have modified surfaces. The high mobility materials may be thought of as two-dimensional, given that the layer can be just a few nanometres in thickness and extend over areas of many microns. However, the reality is that these materials are quasi-low-dimensional semiconductors that are riddled with numerous dangling bonds (see Figure 1).

It is possible to produce transistors with truly two-dimensional materials by turning to a different class of semiconductors. Options for atomically thin films of



semiconductors include transition metal dichalcogenides such as MoS_2 . Merits of these materials are not limited to an absence of dangling bonds, and include a high degree of mechanical stability.

At the Massachusetts Institute of Technology (MIT), our team is developing technologies based on MoS_2 that will enable a shrinking of the size of these transistors, so that their channel length is less than 10 nm. Another aim of ours is to demonstrate the use of these two-dimensional transistors in circuits and systems for large-scale flexible electronics applications.

We have selected monolayer and few-layer MoS_2 for device development. This material has a large band gap of 1.85 eV that equips the FET with an extremely

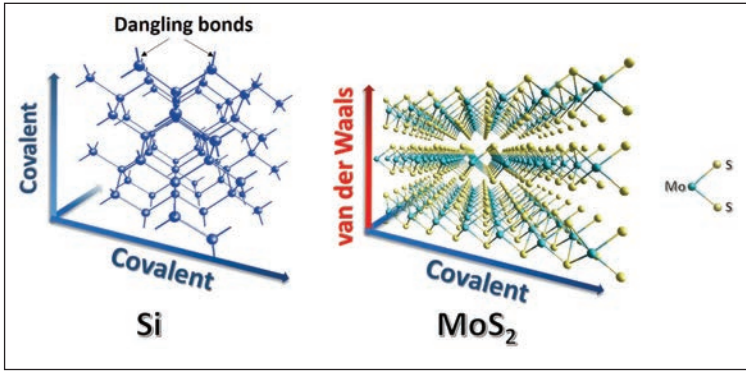


Figure 1. The crystal structure of layered MoS₂ is significantly different from that of bulk semiconductors, such as silicon and the III-Vs. Unlike these more traditional semiconductors, dangling bonds do not occur in the layered crystals because of van der Waals interlayer interactions.

low off-current. What's more, when this class of transistor is built from a monolayer or a few layers of MoS₂, it is effectively an ultra-thin body FET, and thus immune to short channel effects. On top of this, thanks to its atomically thin body, this two-dimensional semiconductor is promising for applications requiring the integration of electronic and optoelectronic circuits on flexible substrates, such as polyethylene terephthalate (PET).

Another strength of the MoS₂ device – and wide-bandgap, two-dimensional semiconductors in general – is the opportunity to combine high-performance with an ultra-low power consumption, which is attractive for Internet-of-things technologies. Incredibly low levels of power consumption are possible by optimising the transistor for sub-threshold operation. When running in this regime, the on-current near the threshold voltage is governed by the sub-threshold swing, rather than carrier mobility. A very low off-current results from

the use of wide bandgap, two-dimensional materials.

Recently, we have demonstrated a double-gate MoS₂ FET with a 15 nm channel length. The MoS₂ layer is formed by CVD, via sulphurization of MoO₃, using perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) as seed.

A role for graphene

With this particular architecture, the electrodes for the source and drain are in immediate contact with the channel, and must be as thin as it to avoid disrupting the electric field lines. To fulfil this requirement, we construct these electrodes from monolayer graphene. This allotrope of carbon is ideal – it forms the thinnest conductive membrane in nature, and it can sustain very high current densities of around 10⁹ A cm⁻².

The most important step in the fabrication of our double-gate MoS₂ FET is the high-resolution patterning of graphene, which defines the transistor's source-drain length (see Figure 2 (a) for a diagram of the structure). To perform this step, we stack a graphene monolayer on the MoS₂ film, before patterning it by electron-beam lithography, using a poly(methyl methacrylate) resist. High-resolution patterning results from developing this PMMA at a low temperature. By employing a cold development process, we are able to open well-controlled trenches with widths as low as 10 nm.

Selective etching of the graphene monolayer follows. This step is critical, because it must avoid imparting any damage to the underlying monolayer or few-layer MoS₂ surface. We have fulfilled this requirement by developing a mild etching process that uses oxygen plasma pulses, rather than a continuous plasma exposure. Facing the samples away from the plasma flux avoids direct exposure to the energetic plasma particles.

Adopting this approach allows us to precisely etch the graphene layer while making minimal impact on the MoS₂ channel (see Figure 2 (b) for an AFM image of the resulting surface). The method is actually well suited to forming contacts on any ultra-thin body transistor; it is comparable to the metal dry-etching process used to fabricate source, drain and gate electrodes in a conventional device technology, and it is CMOS compatible.

Employing graphene for the channel has an additional benefit, as it allows doping to vary the work function of this material over a wide range. This means that the process can potentially be used for both *n*- and *p*-FET technology.

Comparing the transfer characteristics of our 15 nm, 30 nm and 60 nm single-gate MoS₂ FETs reveals that devices with the two shorter channel lengths suffer from short-channel effects, which lead to a hike in the off-current and large values for sub-threshold swing (see Figure 2(c)). This can be lowered, however, by adding a top gate structure to form a double-gate

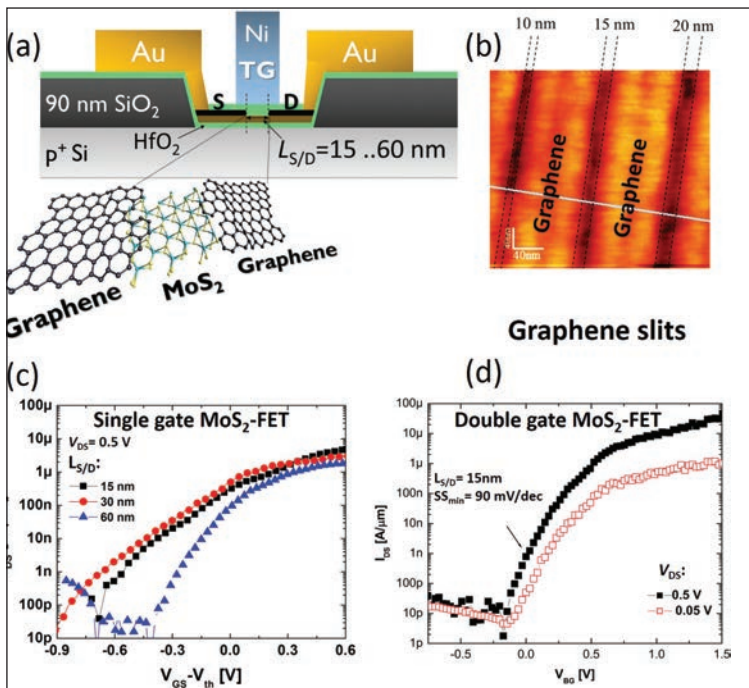
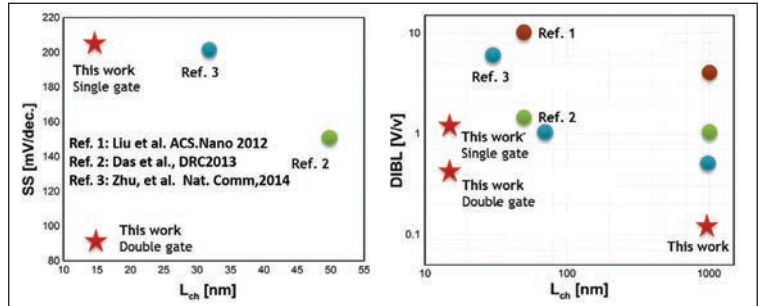


Figure 2. (a) The cross-section of short-channel, graphene-contacted MoS₂-FET. (b) Atomic force microscopy images showing 10 nm, 15 nm and 20 nm graphene slits. (c) Transfer characteristics of 15 nm, 30 nm and 60 nm single-gate MoS₂-FETs with graphene source and drain contacts. (d) The double-gate MoS₂-FET produces record performance values, including a sub-threshold swing of 90 mV/dec and an off-current of about 10 pA/μm.

configuration. Measurements show that a 15 nm MoS₂ FET with a double-gate configuration has an on-off current ratio of about 10⁶, an on-current of typically 50 μA/μm, and a minimum sub-threshold slope of 90 mV/dec at a drain-source voltage of 0.5 V. Benchmarking the performance of MoS₂ channel FETs, and considering long-channel and short-channel regimes, indicates that our transistor has the shortest operating channel length. Another of our transistor's attributes is that it produces a record minimum sub-threshold swing (see Figure 3 (a)).

Our MoS₂ FET also has excellent immunity to short-channel effects, even when it is formed with a single gate. This strength is highlighted by the benchmarking of the drain-induced barrier lowering (DIBL), which is an indication of change in threshold voltage with respect to drain-to-source voltage. In a long channel FET, the energy barrier, as well as threshold voltage between the drain and channel, remains constant irrespective of drain bias – this is not true for the short channel case. Adding a second gate increases robustness against short-channel effects, and results in a device that performs, in many aspects, as well as much larger state-of-the-art silicon-on-insulator transistors, despite the lack of systematic optimization. Thanks to the high on/off ratio and excellent sub-



threshold characteristics, further device scaling should be possible.

The Achilles' heel of the MoS₂ transistor is its high contact resistance, which stems from the Schottky barriers used for electron injection. To mitigate this, low-work-function metals are often used for the source and drain ohmic contacts on n-type MoS₂. This helps to lower the Schottky barrier significantly, but the contact resistance remains relatively large – it is in the kΩ.m range – and this limits device performance.

The solution is to heavily and locally dope MoS₂ in the contact region, because this reduces the energy barrier and eases carrier injection into the channel.

Figure 3. The MoS₂ channel transistors produced at MIT set a new performance benchmark, according to values for sub-threshold swing and drain-induced barrier lowering.

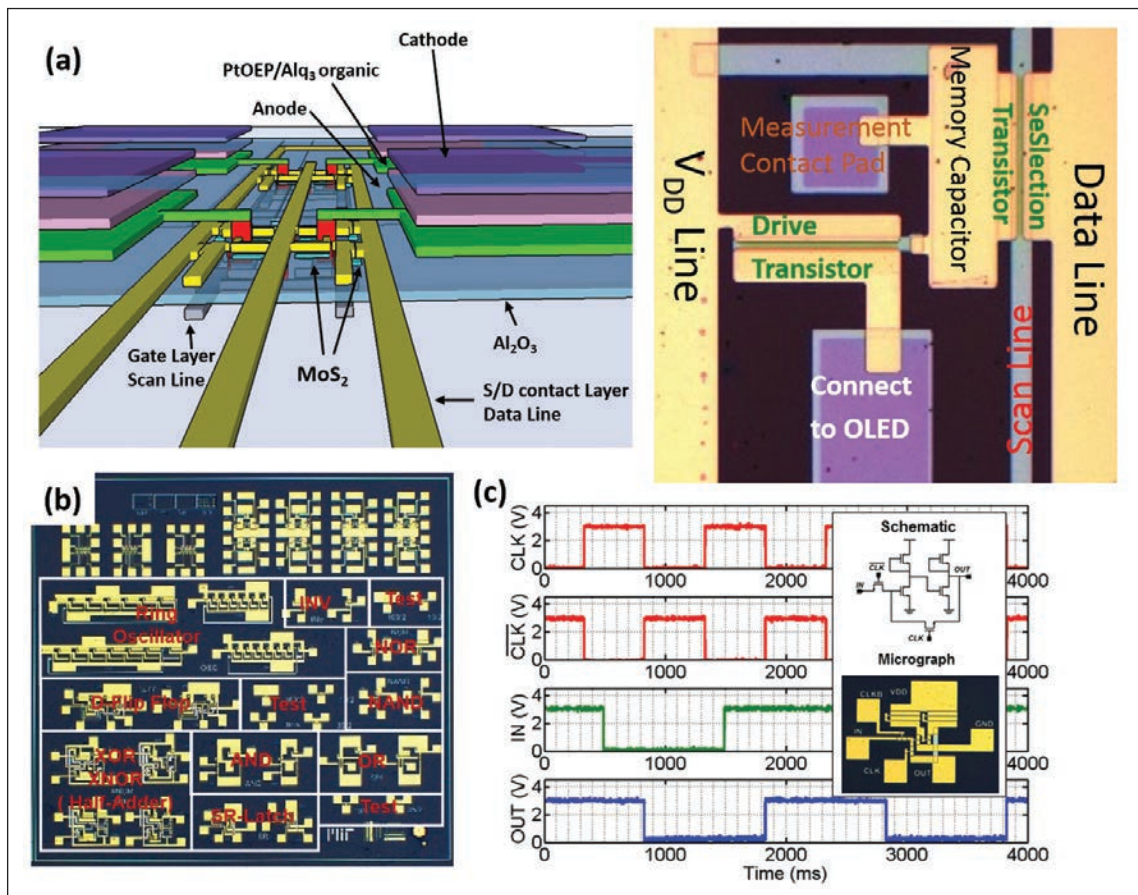


Figure 4. (a) One opportunity for the MoS₂ thin film transistor is as part of a backplane circuit for an organic LED display (left). (b) Optical image of a logic circuit chip. (c) Transient performance of a latch with a memory effect. The latch, which was designed as part of this work, uses two cross-coupled inverters and pass transistors. When the clock signal is low, the latch output follows the input, but when the clock is high, the feedback loop is enabled and the latch operates in the hold mode.

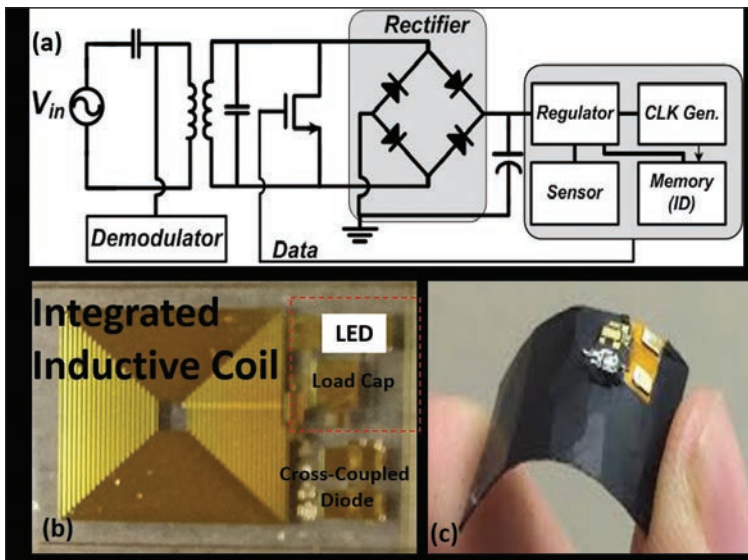


Figure 5. (a) Design of a self-powered RF sensor system. (b) Optical image of an RF-powered LED node. (c) Integration of the RF LED node with a flexible coil.

Doping allows a tuning of the work function of graphene from 4 eV to 5 eV, a range wide enough to cover the work functions of several metals that are commonly used in CMOS technologies.

Increasing complexity

Our recent development in the modelling and design automation of MoS₂-based devices and circuits has allowed us to move up to another level of circuit complexity. We can make various device components and circuits (see Figure 4), including a single-stage inverter, and multi-stage combinational and sequential logic circuits (NAND, NOR, AND, OR, XOR, XNOR, and latch).

One of the many system-level applications being pursued for large-scale MoS₂ electronics is the backplane circuit for flexible organic electronics. Our group is working in this area, developing a technology involving the use of large-area synthetic MoS₂ as the active semiconductor to fabricate a thin-film transistor (TFT) backplane for flexible, transparent, organic LED displays.

These backplane circuits use two TFTs and a storage capacitor to control each pixel and trigger the luminescence (see Figure 4 (a)). One TFT starts and stops the charging of the storage capacitor, while the second acts as a voltage source in the saturation region, delivering a constant current to the pixel. Organic materials with multi-layered heterostructures are deposited for OLED integration,

before a transparent electrode is added on top of the organic materials. Another system-level application that we are currently working on is a self-powered RF sensor node, which includes an energy harvester, rectifier network, a sensor node and logic units (see Figure 5(a)). A key component in the energy power management and energy harvesting circuits is the diode, which is used for RF energy harvesting and rectification.

For this work we use a gated diode. This device, which is formed by connecting the gate and the drain of an E-mode MoS₂ FET, exhibits an excellent rectifying, and can operate over a wide range of frequencies, spanning 1 Hz to 13.6 MHz. The low-frequency response can be very helpful when interfacing the system with a piezoelectric energy harvester device, where 13.56 MHz is the base carrier frequency used in short-range communications for near-field, communication-type, radio-frequency identification (RFID) applications.

In this particular application, a near-field communication-type reader supplies AC power, via inductive coupling, to the inductor-capacitor tank circuit integrated in the RF sensor chip. The rectified and regulated voltages serve as supply voltages for the sensor nodes. Environment information acquired by the sensor is processed by the digital circuit and then stored as data in the memory. This data is transmitted via changes in the output frequency of the demodulator.

High performance levels are possible with our test chip, which contains some of the most important components, including half-wave rectifiers and switched-capacitor DC-DC converters (see Figure 5(b)). We have also designed and fabricated a wireless link and driver circuit on a flexible substrate (Figure 5(c)), and used an LED load to demonstrate milliwatt-scale inductive power transmission and MoS₂ rectifiers.

Having combined all these functions on a single chip, our next goal is to move to a flexible substrate – and on this eventually form ultra-short-channel transistors that will enable a high-performance, multifunctional platform for emerging technologies. This will not be easy, however. To succeed, we first need to develop CMOS-compatible doping methods for efficient, high precision local doping and contact engineering of MoS₂ transistors, so that we can take the performance of this class of electronics to a new level. This will be the first step on a long road to the acceptance and implementation of MoS₂ transistors by the mainstream electronics industry, which must draw on new materials to continue to ensure progress.

Further reading

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L. Yu *et al.* "MoS₂ FET fabrication and modeling for large-scale flexible electronics", 2015 Symposium on VLSI Technology, Kyoto, Japan.

X. Ling *et al.* Nano Lett. **14** 464 (2014)

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Improving the quality of AlN-on-sapphire films

A high-quality buffer could increase deep UV LED efficiency

A PARTNERSHIP between researchers in Japan and Malaysia claims to have set a new benchmark for the quality of annealed AlN films grown on sapphire.

“The optimum annealing temperature and AlN thickness are 1650-1700 °C and around 300 nm, respectively,” says corresponding author Hideto Miyake from Mie University, Japan.

One of the strengths of the buffer layer is its low threading dislocation density of $4.7 \times 10^8 \text{ cm}^{-2}$.

This dislocation density, which is more than an order of magnitude below that of a typical AlN-on-sapphire film, will appeal to the developers of deep UV LEDs, because the greater the imperfections, the lower the device efficiency.

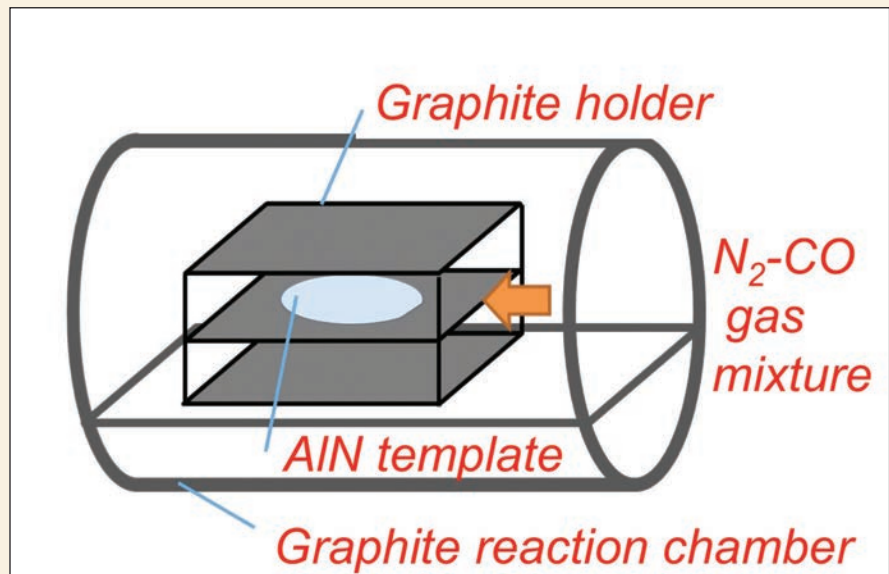
Another virtue of the team’s AlN buffer is its very high crystal quality. X-ray rocking curve measurements produce a full-width at half-maximum of 16 arcsec in the (0002) plane and 154 arcsec in the (10 $\bar{1}$ 2) plane. In comparison, a typical AlN-on-sapphire film will have a full-width at half-maximum in the (10 $\bar{1}$ 2) plane of 1000-2000 arcsec.

The idea of using annealing to improve AlN-on-sapphire film quality is not new. However, it is more common to anneal either the AlN or GaN nucleation layers than the buffer layer, which is the approach of the Japanese team.

These researchers determined the best conditions for buffer annealing by considering a range of temperatures and film thicknesses.

Prior to annealing, sapphire substrates were loaded in an MOCVD chamber, cleaned in hydrogen gas at 1100 °C for 10 minutes, and buffer layers with thicknesses ranging from 100 nm to 1000 nm were deposited at 1150-1200 °C.

The AlN-on-sapphire samples were then annealed under a carbon-saturated mixture of carbon monoxide and nitrogen for 2 hours at temperatures ranging from 1500 °C to 1750 °C.



Annealing enables a slashing of defect density and a dramatic improvement in the crystal quality of AlN-on-sapphire films.

Although this lengthy annealing time at elevated temperatures is not ideal for high-volume manufacturing, but it is acceptable, insists Miyake: “AlN growth of 100 wafers at temperature of 1500 °C will be difficult, and the cost expensive. However, annealing 100 wafers is very easy – you just put 100 wafers in annealing furnaces.”

AlN films with a thickness of 2 μm were grown on a range of AlN buffer layers using a growth rate of 1 $\mu\text{m}/\text{hour}$ at 1450 °C.

The team used atomic force microscopy to scrutinise the surface of several samples, along with cousins that had not been annealed. They found that thicker buffers led to rougher surfaces, while annealing led to a dramatic improvement in surface quality.

For example, the root-mean-square surface roughness of a film with a 300 nm buffer plummeted from 3.1 nm to 0.49 nm after annealing at 1650°C.

Analysing the values of the full-width-at-half-maximum of X-ray diffraction peaks for samples annealed at a range of temperatures uncovered an annealing

sweet-spot at 1650-1700 °C. At higher temperatures, surface roughness increased, due to thermal decomposition of the AlN buffer.

To uncover the mechanism behind the annealing-driven improvement in film quality, the team turned to cross-sectional transmission electron microscopy.

This technique revealed that as-grown films feature inverted cone-shaped domains, which are replaced with a two-layer structure after annealing.

The researchers have also studied the imperfections in a film formed by annealing a 300 nm-thick AlN buffer at 1700 °C for one hour, and then growing on this a 2 μm -thick AlN film at 1450 °C.

Using transmission electron microscopy, they estimated an edge-type threading dislocation density of $5 \times 10^8 \text{ cm}^{-2}$; screw type and mixed type threading dislocation densities were below $1 \times 10^8 \text{ cm}^{-2}$.

H. Miyake *et. al.* Appl. Phys. Express **9** 025501 (2016)

Better tunnel junctions for better LEDs

Hybrid growth creates transparent, low resistance contact for nitride LEDs

MORE EFFICIENT, more powerful GaN-based LEDs and lasers could result from the superior tunnel junctions developed by researchers at the University of California, Santa Barbara (UCSB).

This team's tunnel-junctions – an attractive alternative to the light-absorbing, current-spreading layer of indium tin oxide (ITO) – combine low-resistivity with transparency and a low device operating voltage.

What's more, these junctions, formed by a combination of MOCVD and MBE growth, enable top-side *n*-type contacts, considerably opening up the design space for III-Nitride LEDs and lasers.

The UCSB team are by no means alone in developing tunnel-junctions as a replacement for ITO. Success is not easy, however, as it is more challenging to fabricate tunnel junctions with the GaN-based material system than it is with lower bandgap materials.

Some groups increase tunnelling currents by adding AlN and InGaN interlayers. However, this success comes at the expense of a higher voltage, in the case of adding AlN; or greater optical absorption, following the insertion of InGaN.

Alternative approaches are to add GdN nanoparticles, but this increases resistance; and to form an Esaki-type diode, but that requires doping levels for the *p*-type and *n*-type regions of around 10^{20} cm^{-3} .

The UCSB group is an adopter of the latter approach, and has broken new

ground with its growth technology. "The hybrid approach allows us to make use of the unique advantages of each growth method – the high efficiency active regions by MOCVD, and the MBE capability of regrowing on *p*-type GaN without repassivation," explains corresponding author Erin Young.

Additional advantages of MBE, which lead to superior transport through the tunnel junction, are a higher level of silicon incorporation than is possible by MOCVD, and a higher quality *n*-type GaN at that concentration.

"Regrowing only the *n*-side by MBE also means the impurities associated with the regrowth interface – which are typically *n*-type – are not buried in the *p*-GaN."

Young and co-workers used MBE to deposit a thin, highly doped *n*-type layer on an MOCVD device to form a tunnel-junction, before adding a thicker *n*-type layer that enabled uniform current spreading and carrier injection into the device.

Although the team focused on reporting the results of tunnel junctions on semi-polar structures, success is also realised with polar and non-polar architectures.

"We are interested in LEDs on semi-polar orientations of GaN for low droop, high power device operation," explains Young.

After deposition of the *n*-type layers, the researchers used standard lithography techniques to fabricate LEDs with an area of 0.1 mm^2 . Ti/Al/Ni/Au contacts were used for the *n*-type top and bottom contacts.

Electrical measurements revealed that a carrier concentration of around $1.5 \times 10^{20} \text{ cm}^{-3}$ produced the lowest resistivity. The downsides of even higher carrier concentrations are not just a higher resistivity – they include diminished optical transparency. These findings led the researchers to select a carrier concentration of $1 \times 10^{20} \text{ cm}^{-3}$ for all their devices.

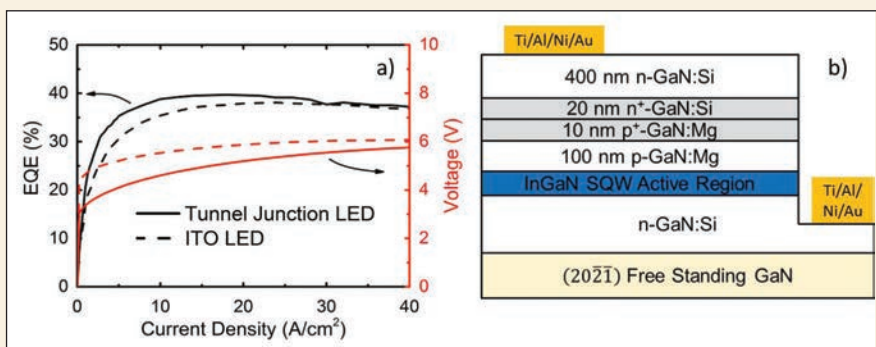
The first LEDs that were made had an increase in turn-on voltage of 1 V, associated with the tunnel junction. To reduce this, the team tried various cleaning procedures, which had no impact, and annealing steps. They found that tunnel junctions with a low resistivity and a low voltage were formed via a combination of a low ammonia flow for regrowth, and minimal exposure of the sample surface to this gas.

Atom probe tomography uncovered oxygen in this tunnel junction, with a concentration broadly mirroring that of the magnesium dopant. The team speculates that the oxygen binds to active magnesium, with residual oxygen enhancing tunnelling by contributing carriers.

External quantum efficiency measurements showed that at low current densities, an LED with a tunnel-junction outperforms that of an equivalent device with an indium tin oxide contact. At 40 A cm^{-2} both devices have a similar efficiency.

Equality at the high current density is thought to result from optimisation of the packaged devices for ITO current spreading.

"The *n*-contacts in these devices were not ideal – we have since optimized them," explains Young. "We would expect that for a more optimal packaged device design, the tunnel-junction LED performance would be better over the full current density range."



LEDs with tunnel-junctions outperform those with ITO at low current densities.

E. Young *et al.* Appl. Phys. Express 9 022102 (2016)

Trumping SiC devices with Ga₂O₃

Ga₂O₃ diodes deliver great thermal management, and have the edge over SiC equivalents in a key figure-of-merit for power devices

RESEARCHERS at Flosfia of Kyoto, Japan, have fabricated Ga₂O₃ Schottky barrier diodes with a lower on-resistance than the best Schottky barrier diodes made with SiC.

This work highlights the potential of devices made from Ga₂O₃ for increasing efficiency in the power electronics industry.

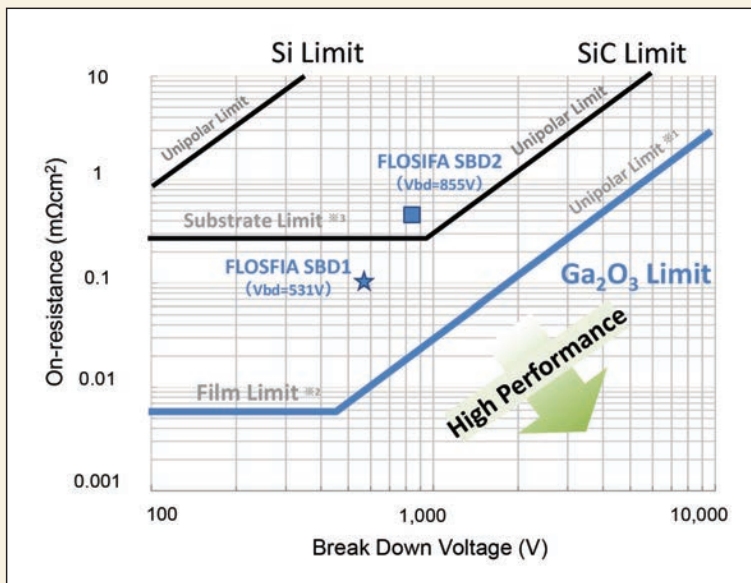
Corresponding author of the paper describing the work, Masaya Oda, believes that the most important aspect of Flosfia's work is the creation of a device that combines a very low on-resistance with good thermal management.

"Gallium oxide has low thermal conductivity. Therefore, we use a very thin α -Ga₂O₃ film to reduce the heat diffusion length, so this device can realize effective heat diffusion from the device to the heat sink."

This form of Ga₂O₃, which has a bandgap of 4.7 eV-5.3 eV, can be grown on various substrates, such as α -Ga₂O₃ and SiC. However, sapphire is preferred, as it is much cheaper, allowing a trimming of the manufacturing cost of the device.

Engineers at Flosfia deposit the α -Ga₂O₃ films on sapphire using a growth technology described as 'mist epitaxy'. This is based on the 'mist CVD' technology developed by Shizuo Fujita's team at Kyoto University, but features improved material quality, partly via a reduction in the density of impurities.

Flosfia's growth process begins with the generation of small mist particles. They have a diameter of several microns, and are formed by the ultrasonic atomisation of water and/or alcohol solutions containing metal compounds. A carrier gas transfers the small mist particles to a reaction chamber where a heated substrate drives a reaction that leads to film deposition. To reduce impurities,



Flosfia's Schottky barrier diodes can deliver a performance beyond what is possible with SiC. In the plot on the left: (1), the unipolar limit has determined from a electron mobility of 300 cm² V⁻¹ s⁻¹, a breakdown voltage of 8 MV cm⁻¹, and a relative permittivity of 10; (2), a film thickness of 20 μm has been used, with a resistivity assumed from measurements of mobility and carrier concentration; and (3), the resistivity of the SiC wafer is assumed to halve when it is thinned.

a carbon-free gallium halide source is used.

Impurity levels in the α -Ga₂O₃ films grown by mist epitaxy have been measured by secondary ion mass spectroscopy. The concentration of hydrogen was 2 x 10¹⁷ cm⁻³, while levels for the likes of carbon, fluorine, chlorine, bromine, sodium and magnesium were below the detection limit.

Engineers formed devices by growing an n⁺ and an n layer of α -Ga₂O₃ on sapphire. Tin halide provided a doping source of tin, which could span concentrations from 1 x 10¹⁷ cm⁻³ to 3 x 10¹⁹ cm⁻³. The epilayers are removed from the substrate, a step that may be aided by the presence of misfit dislocations and strain at the α -Ga₂O₃-sapphire interface. Two significant advantages resulted from substrate removal: a reduction in the series resistance of the diode; and improved thermal management, due to the opportunity to mount the device directly on a heat sink.

A pair of diodes were fabricated by the team. The first, designed to produce a low on-resistance, had a 430 nm-thick n⁻ layer; and the second, targeting a higher breakdown voltage, had a

2580 nm-thick n⁻ layer. Both also had an n⁺ layer with a thickness of 3-4 μm, a Schottky electrode of Pt/Ti/Au with a 30 μm diameter, and an ohmic electrode with a 60 μm diameter.

The thinner device had an on-resistance of 0.1 mΩ cm² and a breakdown voltage of 531 V, and the thicker sibling had an on-resistance of 0.4 mΩ cm² and a 855 V breakdown voltage. Both diodes had a relatively high leakage current. This might be due to surface leakage that results from the lack of a passivation layer and defects formed during heteroepitaxy.

Graphing on-resistance as a function of breakdown voltage showed that both devices were close to or below the theoretical limit for SiC, underlining the promise of Ga₂O₃ diodes (see figure).

Oda believes that higher-voltage, lower-leakage devices could be formed by improving the sapphire substrate removal process and cutting carrier concentration. He and his colleagues are planning to increase the size of their Schottky barrier diodes, so that they are capable of handling up to 20 A.

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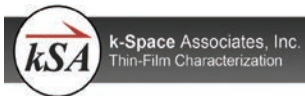
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