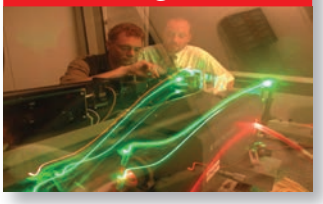
COMPOUND SEMICONDUCTOR

Connecting the Compound Semiconductor Community

Volume 21 Issue VIII November / December 2015 @compoundsemi www.compoundsemiconductor.net

LED droop: More evidence for Auger

Exposing flaws in modelling LEDs



Positive vibes for silicon carbide

Antimonides aid infrared sources

Uniting III-Vs with silicon CMOS

AIXTRON

Our technology. Your future.

YOU THINK,

AIXTRON SYSTEMS SHOULD OFFER YOU THE BEST COST OF OWNERSHIP.

WE THINK THAT TOO.

THE NEW AIX R6.

DISCOVER THE NEW AIX R6.

Revolutionizing an industry is not about changing everything. It's about making the good even better. Introducing: The new AIX R6. It has everything you expect from the industry's technology leader plus **better usability, better throughput and better cost of ownership.**

AIXTRON SE · info@aixtron.com · www.aixtron.com

editorial view

by Dr Richard Stevenson, Editor

Where is the boundary?

ONE POPULAR APPROACH for driving technology forward involves identify weaknesses in incumbent products, and devising ways to address them. If the weaknesses are significant, and the rewards for addressing them lucrative, then you can bet that many will be chasing the prize.

On some occasions, one technology is an obvious successor – think of the LED head torch, and its forerunner based on the filament bulb. In these cases, the battle will be fought over factors such as the speed to market, bang-per-buck, and the strength of the marketing campaign.

In others instances, firms pursue different technologies to break into an established market with a supposedly superior product. When this happens, it might be a case of winner-takes-all – and it may also be a matter of horses for courses, which is the case in the power transistor arena.

In this sector, silicon devices currently rule the roost, but they have several weaknesses, including a limited range of operating temperatures and an efficiency that is not that high. To exploit these drawbacks, many companies, from start-ups to multi-nationals, are developing chips based on two wide band-gap materials: GaN and SiC.

Analysts that are following this market, such as Yole Développement, are arguing that both materials can enjoy success. That's because they believe that a boundary exists at 600 V, with higher voltages reserved for SiC, and the lower realm awaiting occupation by GaN-on-silicon.

The thinking behind this is that GaN-on-silicon is better suited to lower voltages, thanks to its lower chip costs. But at higher voltages, leakage currents hit unacceptable values – so it is the SiC devices, grown on native substrates, that are likely to emerge as the successors to silicon.

But this vision is not a forgone conclusion. There are some research teams that would question this outlook, because they are developing technologies to propel GaN-on-silicon transistors to higher voltages. This includes the group led by Farid Medjaboub, from IEMN in France, that has developed a technique to slash leakage currents through selective substrate removal. Taking this approach has already increased the blocking voltage of the GaN HEMT to 3 kV and beyond.

Over the next few years, it will be interesting to see whether this technique is used to extend the blocking voltage of commercial GaN HEMTs. If this happens, there should be a shifting of the boundary between both of the wide bandgap technologies. SiC would still be a winner, but GaN would grab the bigger prize.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718109
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Amy Rogers arogers@brunmedia.com +001 678-714-6775
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

Volume 21 Issue VIII 2015

features

32 GaN transistors: Breaking barriers adoption
Grow GaN transistors on silicon and their bang-per-buck increases

36 A positive outlook for the SiC substrate
Sales of SiC substrates will rise significantly as shipments shift to the 6-inch format and established suppliers face increased competition from Chinese start-ups

40 LED droop: Physics beyond the common model
Optical spectroscopy exposes fundamental flaws in the well-known model for LED droop

48 Multiple materials enhance front-ends
The front-ends of smartphones should not be served by a single material

58 Extending the capabilities of GaN-on-silicon HEMTs
Removing the substrate allows GaN-on-silicon transistors to combine high operating temperatures with blocking voltages beyond 3 kV

64 Targeting spectroscopy with antimonide sources
By delivering great performance at low cost, GaSb-based devices are the ideal sources for gas sensing

70 Can Auger recombination be good for LEDs?
The benefits of Auger: A reduction in turn on voltage and higher wall-plug efficiency

news

06 Osram announces €3 billion investment programme

07 Soraa moves ahead with manufacturing plans

08 Imec and Ghent University show InP laser arrays on silicon

10 Qorvo delivers solid Q2

11 AXT acquires GaAs line from Hitachi Metals

news analysis

12 POET Technologies: From Lab To Fab

14 GaN: beyond the basestation

16 Plessey: bright and bold

22 MACOM set to mass market GaN

24 Delivering the future

26 Oclaro hits 2016 on a high

28 InP: great expectations

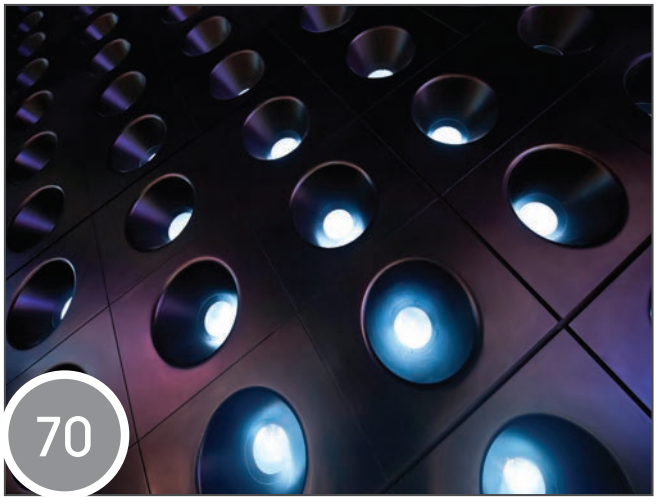
30 Beyond radar

research review

74 Optimising LEDs with tunnel junctions

75 A better laser for lighting

76 HEMTs: Oxygen plasma treatment eliminates the need for a GaN cap



Osram announces €3 billion investment program

OSRAM has announced that it will invest around €3 billion in new technologies and applications by 2020. Of this, around €2 billion will be spent on R&D to expand into new markets. Another €1 billion will be for the construction of a new LED chip plant in Malaysia.

"With a focus on profitability, flexibility, and entrepreneurship, following a phase of strategic realignment, we are now launching the 'Diamond' innovation and growth initiative. This means we are switching the focus to sustainable growth, benefitting even stronger from the potential offered by semiconductor-based technologies," said Olaf Berlien, CEO of Osram Licht AG.

'Diamond' comprises several strategic measures. In a first step, Osram will invest around €370 million in its Opto Semiconductors (OS) segment for a new LED chip plant in Kulim, Malaysia. Since further expansion measures are already being planned, the company expects to invest a total of around €1 billion there by 2020. The new plant will represent the largest and latest 6-inch LED chip production site worldwide, according to the company.

Osram says that the additional production capacity and its technological leadership will enable it to significantly increase its market share in the fast growing general lighting markets. This market segment is the largest in the area of opto semiconductors, with a current volume of around €5.7 billion. Given average annual growth rates of 7.5 percent, it offers the company the greatest potential until 2020.

Through economies of scale, Osram says it can also reduce its cost position in other market activities such as automotive lighting as well as applications for mobile devices, in which Osram already has a strong presence.

Osram is also planning additional investments in the Specialty Lighting (SP) segment to enable a broad-based rollout of new technologies in the market and to realise further growth potential in areas such as automotive lighting. For example, Osram is currently the only company in the world offering laser modules for headlamps ready for series production. Another new technology in the field of automotive lighting is organic light-emitting diodes (OLEDs), which is also about to be rolled out for use in rear lights of vehicles. Osram expects the market for laser and OLED applications in the automotive sector to amount to around €1.1 billion in 2025.

In the recently created Lighting Solutions & Systems (LSS) segment, Osram will be focusing on intelligent, more technologically demanding lighting solutions. Given the increasing importance of complex lighting solutions, Osram is also shifting the focus on expanding the electronics and software expertise. Over the next two years, new capacities for electronic ballasts and light management systems will be created for this purpose.

In line with the announced innovation and growth initiative, Osram will increase its R&D budget significantly. By doing so, the company intends to promote in particular the development of smart city applications, wireless lighting control as well as laser and OLED technology.

Osram has kept its research quota at just over six percent of revenue over the past years. After the initiated carve-out of the general lighting lamps business, the increased research expenditure will account for approximately 9 percent of revenue by FY 2016.

"Investments in research and development have paid off for the company in the past by taking it to a clear number one position in the automotive sector and leading to groundbreaking applications with opto semiconductors. Through the intended increase in research intensity, Osram wants to further strengthen its technical expertise for semiconductor-based technology and extend its market position," said CEO Olaf Berlien. According to the company, the 'Diamond' innovation and growth initiative will focus the company on balanced growth and add value for employees, customers, and shareholders. In addition to high-revenue areas that hold large growth potential for the company, lucrative niche areas, where Osram is already in a good position, will continue to make a valuable contribution to overall returns. The company has set itself several targets to complete in the final year 2020.

One of these goals is to achieve revenue of between €5 billion and €5.5 billion. After the carve-out of the lamps business, this would correspond to an average annual growth rate of 8 percent.

Another asim is earnings before interest, tax, depreciation, and amortisation (EBITDA) of between €0.9 billion and €1 billion. This would correspond to an average annual growth rate of around 9 percent.

In addition, the company aims to generate earnings per share of around €5, which would be equivalent to an average annual increase rate of around 25 percent compared with fiscal 2015. The announced share buyback program is included in this target.

Soraa moves ahead with New York manufacturing plans

SORAA, a developer of advanced lighting products and GaN-on-GaN LED technology, will open a new semiconductor fabrication plant in Syracuse, New York.

In partnership with the State of New York, the company will construct a new state-of-the-art GaN-on-GaN LED fabrication facility that will employ hundreds of workers.

Working in coordination with SUNY College of Nanoscale Science and Engineering (SUNY Poly CNSE), the new facility is on pace for shell completion by the end of this year with production beginning in the second half of 2016.

Soraa currently operates an LED fabrication plant in Fremont, California, one of only a few in the United States. "Central New York's economic growth is due in large part to high-tech companies like Soraa that recognise the region's wealth of assets and resources," Governor Cuomo said.

"Today's announcement not only means economic stability for the region, but it also strengthens Central New York as leader in the development of the clean technology that will help light and power the future."

"Syracuse is an optimal location for the new fabrication facility for a number of reasons including the innovative high-tech vision and strategy of Governor Cuomo; the ability to attract some of the best and brightest scientists and engineers in the world; and the capacity to tightly control the product quality and intellectual property around our lighting products through our partnership with SUNY Poly CNSE," commented Jeff Parker, CEO of Soraa.

"Since we launched our first product in 2012, global market reception for our high quality of light LED products has been phenomenal and sales have soared. The new facility will significantly increase our manufacturing capacity to meet this growing demand."

Infinera demos 100G on-demand at Supercomputing conference

INFINERA, a maker of InP photonic integrated circuits (PICs) and network equipment, and Corsa Technology, a software-defined networking (SDN) company, have announced a new demonstration of SDN-enabled on-demand 100 gigabits per second (100G) packet services.

The demo, which took place at the International Conference for High Performance Computing, Networking, Storage and Analysis (SC15) in Austin, Texas, show the feasibility of delivering the scalable, high-bandwidth services required by high-performance computing (HPC) and advanced research & education (R&E) applications.

Features include dynamic multilayer provisioning, precision switching and terabit traffic management, over a converged packet-optical transport network.

Infinera and Corsa collaborated to create the proof-of-concept demo using Corsa's 100G DP6400 switching platform, Infinera's Cloud Xpress metro

optical transport platform and Infinera-developed SDN control capabilities. Also at the SC15 conference, Infinera has announced it would deliver 1.5 terabits per second (Tb/s) of transmission capacity with network firm CenturyLink to support SCinet at the SC15 conference. SCinet is a powerful network created each year to support the research applications and experiments taking place at the conference, connecting the Austin Convention Center to networks around the world.

The 1.5 Tb/s of line-side capacity connects the Austin Convention Center to CenturyLink's global fibre optic network, using the Infinera DTN-X platform.

The terabit deployment demonstrated CenturyLink's rapid provisioning of 100 Gigabit Ethernet (GbE) services from the conference to CenturyLink's point of presence in Austin and to six major US cities across the country.

CenturyLink operates a 250,000-route-mile US fibre network and a 300,000-route-mile international transport network. Through a dedicated network connection, the company delivers 100 GbE Optical Wavelength Service to enterprise customers; research, financial and educational institutions; and Internet content providers across the US and in select international cities.

The DTN-X Family is a key part of the Infinera Intelligent Transport Network, and includes the chassis-based XTC series and the new XT series. The DTN-X Family was recently extended with the addition of Infinera's DTN-X XTC-2 and XTC-2E for metro applications as well as with the DTN-X XT-500, a new compact platform to address long-haul high-capacity point-to-point interconnect applications.

Imec and Ghent University show InP laser arrays on silicon

IMEC AND GHENT UNIVERSITY have presented, for the first time, arrays of InP lasers monolithically integrated on 300 mm silicon substrates in a CMOS pilot line.

This breakthrough, published in *Nature Photonics*, provides a path toward high-volume manufacturing of cost-effective photonic integrated circuits (PICs) with monolithically integrated laser sources. Such laser-powered PICs could change the way data is transferred between future logic and memory chips.

Over the past few years, demand for data communication between servers in cloud datacentres has been growing exponentially, following strong growth in social networking, cloud computing and big data applications.

Silicon photonics technology enables cost-effective manufacturing of fibre-optic transceivers, which in turn provides continued scaling of server and datacentre capacity with improved power efficiencies. However, wide-spread adoption of this technology has been hampered in part by the lack of monolithically integrated laser sources.

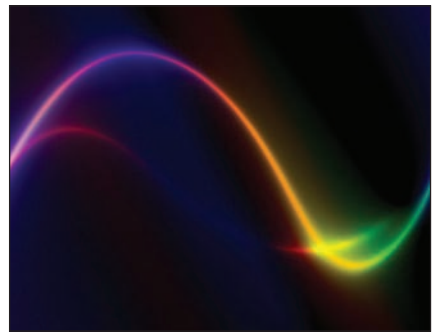
The integration on silicon of efficient INP based light sources, currently driving long-range telecommunication networks, is known to be very challenging, owing to the large mismatch in crystal lattice constants between both materials.

Imec and Ghent University overcame these structural differences and largely suppressed the detrimental crystal defects that typically form at the interface between silicon and InP.

Using a production grade MOVPE growth reactor, InP semiconductor was selectively grown on silicon in a pre-patterned oxide template, realising InP waveguide arrays across the entire 300 mm substrate.

Subsequently, periodic grating structures were etched in the top layer of these waveguides, providing the optical feedback required for laser operation. Lasing operation was demonstrated for all tested devices consisting of an array of ten InP lasers. Typical lasing threshold powers of around 20 mW were observed at room temperature under optical pumping.

Lasing performance showed small variability along the array, illustrating the high material quality of the heteroepitaxial grown InP. In addition, accurate control on the distribution of lasing wavelengths in the array was demonstrated by modifying the grating parameters.



The newly demonstrated approach for integrating lasers with silicon has been carried out in Imec's 300 mm CMOS pilot line facility, therefore providing a path to large volume manufacturing.

Ongoing research efforts focus on growing more complex layer stacks to enable electrical injection of the lasers and emission in the 1300 nm wavelength range, along with integration with silicon based waveguide devices.

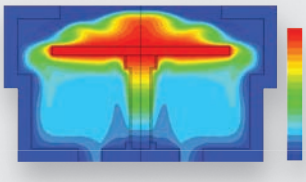
This work has been carried out as part of imec's industry affiliation program on Optical I/O, which targets the development of a scalable, silicon-based optical interconnect technology for high-bandwidth chip-level I/O.

The work was also partly supported by the European Commission through an ERC starting grant awarded to Dries Van Thourhout of Ghent University for research on Ultra Low Power Photonic ICs (ULPPIC).

This five year project aims to develop novel active photonic devices with lower power consumption, for integration on next generation electronic and photonic ICs.

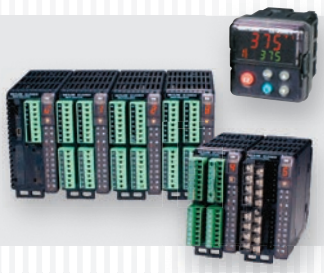
Imec's research and development work on Optical I/O is performed in cooperation with key partners in its core CMOS programs including Huawei, GlobalFoundries, Intel, Micron, Panasonic, Qualcomm, Samsung, SK Hynix, Sony and TSMC.

Optimize the Thermal Performance of your Process Equipment.



Extensive computational tools enable product designs to be highly refined for ultimate performance.

Multi-zone circuit layouts in a polyimide construction are highly customized to deliver exacting performance up to 250°C.



EZ-ZONE® RM Multi-loop controllers are fully scalable with up to 152 PID Loops and 256 monitor points per system.

Watlow provides innovative solutions to help process tool manufacturers meet the needs of the semiconductor technology roadmap. Our approach is to work collaboratively to help solve complex thermal challenges associated with state-of-the-art manufacturing processes; helping to improve yield, throughput and cost of ownership. This includes innovative heaters, controllers and sensors for use in front-end and back-end applications such as CVD, PECVD, Etch, Diffusion, Bonding, IC test and more.

ASSURANT™ gas and pump line heaters feature high temperature capabilities with low outgassing.

Contact Watlow® today for the latest thermal solutions for semiconductor applications.

European Technical Sales Offices

Germany +49 (0) 7253-9400-0
info@watlow.de

France +33 1 41 32 79 70
info@watlow.fr

Italy +39 02 4588841
italyinfo@watlow.com

Spain +34 91 675 1292
info@watlow.es

UK +44 (0) 115-964-0777
info@watlow.co.uk

WATLOW®

Qorvo delivers solid Q2

QORVO, a provider of RF and other technologies for mobile, infrastructure and aerospace/defence applications, has announced financial results for its fiscal 2016 second quarter, ended October 3, 2015. Qorvo also announced a new one-year $1 billion share repurchase program which expired on November 4, 2016. Share prices rose nearly 15 percent in response.

"The Qorvo team delivered a solid September quarter, with quarterly revenue increasing 12 percent year-over-year, led by strong 19 percent year-over-year growth in Mobile Products, " said Bob Bruggeworth, president and CEO of Qorvo.

"Design activity during the quarter was particularly robust, as we secured multiple opportunities to expand content in the marquee smartphones launching in calendar 2016 and 2017 and positioned IDP to accelerate growth across its target markets."

Steve Buhaly, chief financial officer of Qorvo, said: "In the nine months since Qorvo's formation, revenue has grown 25 percent from the same period in the prior year while non-GAAP operating income has nearly doubled. We're proud of this performance and are excited about our opportunities in the coming year."

On a GAAP basis, September quarterly revenue was $708.3 million, gross margin was down slightly at 40.2 percent (41.5 percent previous quarter), operating income was greatly increased at $18.0 million (compared to a $1.3 million loss in Q1) and net income was up to $4.4 million (compared to $2.0 in Q1), or $0.03 per diluted share based on 150.8 million shares outstanding.

On a non-GAAP basis, September quarterly revenue increased sequentially to $707.4 million and gross margin was 49.7 percent (down from 51.5 percent in Q1). Operating expenses declined sequentially, yielding operating income up at $194.8 million (compared to $187.8 million in Q1), or 27.5 percent of sales. Net income was $183.3 million, or $1.22 per diluted share based on 150.8 million shares outstanding.

Strategic highlights include capturing multiple LTE reference design wins for multimode PAs, multimode transmit modules, switches, duplexers, and multiplexers; capturing BAW (bulk acoustic wave) filter and amplifier wins at Tier 1 automotive suppliers; solidifying long-term defence and aerospace market position by establishing multiple multi-year supply agreements; participating in pre-5G and 5G demos at major basestation OEMs; sampling high performance GaN-based macro cell PAs to the five leading base station OEMs; capturing an increasing percentage of DOCSIS 3.1 sockets with hybrid GaAs and GaN products.

IQE appoints director for Compound Semiconductor Centre

IQE PLC, a supplier of advanced semiconductor wafer products and services, has appointed Wyn Meredith as director of the Compound Semiconductor Centre (CSC), the new joint venture, between IQE and Cardiff University was formally launched later this month.

IQE has a long standing relationship with Wyn who has been working on its behalf in a variety of roles, most recently developing links to education and funding bodies.

In his new role Wyn will be responsible for developing funding opportunities in external programs and will report to the CSC board of directors.

Wyn, who holds a PhD in Optoelectronics from Heriot Watt University, joins IQE from his current role as Commercial Director at Compound Semiconductor Technologies Global Ltd (CST).

Lumileds accelerates outdoor LED fixture design

Lumileds has introduced the Luxeon XR-M line of Matrix Platform solutions, designed as a turnkey solution for outdoor LED fixtures.

These building blocks integrate three, four or five Luxeon M LEDs on a metal core PCB, providing a platform that enables fixture manufacturers to accelerate their design of streetlights, high bay and low bay luminaires. For instance, the 2 x 2 LED square version, in combination with industry standard optics and driver, yields a complete IP66 solution, according to the company.

"Luxeon XR-M incorporates Luxeon M, one of our most efficient and top selling, high power LEDs. The boards can be connected in parallel or series for driver design flexibility, and the wide variety of lens options means designers have multiple turnkey options to release a full range of luminaires much faster to market," said Andrew Cohen, product manager of the Matrix Platform at Lumileds.

The Luxeon XR-M achieves 140 lm/W at 4000K, 70 CRI, T_c=85degC and 700 mA drive current. Using constant pitch between the LEDs and PCBs, combining multiple Luxeon XR-M modules achieves the most uniform, distributed light patterns. Each Luxeon XR-M module provides 3,300 to 5,500 lm and is available in colour temperatures of 4000K, 5000K and 5700K with a minimum CRI of 70.

This new product is part of the Lumileds Matrix Platform of infinitely configurable LED boards, linear flex and modules featuring Luxeon LEDs. The Matrix Platform comes in both off-the-shelf and built-to-spec options, offering a virtually limitless range of solutions for any application.

AXT acquires GaAs line from Hitachi Metals

AXT, a manufacturer of compound semiconductor substrates, has acquired highly automated processing and cleaning equipment for GaAs substrates from Hitachi Metals.

The production line includes automated equipment for wax mounting/demounting, edge grinding, wafer sawing, polishing and cleaning. In addition, AXT has licensed from Hitachi Metals associated technical information and applicable patents intended to enable AXT to use the equipment in full production.

The equipment has been uninstalled in Japan and shipped to AXT's production facility in Beijing, China where it is currently being installed. SCIOCS, the related spin-off from Hitachi Metals, will assist in the installation and optimisation process. This production line is ideally suited for 4in and 6in GaAs and InP manufacturing processes and AXT intends to supply such GaAs substrates to SCIOCS and other customers.

"This acquisition comes at a time when AXT is making a concerted effort to invest in automated manufacturing equipment to increase sales of its InP substrates and 6in semi-insulating GaAs substrates," said Morris Young, AXT's chief executive officer. "We plan to leverage the automation and manufacturing technology acquired to further enhance our product quality and consistency. We are highly appreciative of the multi-faceted partnership between the two companies."

The terms of the acquisition are not being disclosed. However, it is not expected to have a meaningful impact on the cost of operations going forward.

MACOM announces datacentre chipset

MACOM TECHNOLOGY has announced a chipset for CWDM (coarse WDM) and PSM4 (parallel single mode) applications in the datacentre. The chipset includes the complete lineup of electronic and optical chips to achieve the lowest power consumption in a QSFP28 form factor.

As new mega-datacentres continue to expand to service the demand for high-speed data communications, the volume of 100G transceivers is expected to grow exponentially with the parallel need for lower power, smaller size and lower cost components. Macom has consolidated the high-speed semiconductor content in 100G transceivers and now offers a complete solution including lasers, drivers, clock data recovery (CDR), and transimpedance amplifiers (TIAs) – optimised to provide differentiated performance, power, size and cost benefits.

Macom's M37046 and M37049 are said to be the lowest power and smallest quad channel receive and transmit CDRs with market leading performance. The MAOM-002301 and MAOM-002304 are single and quad-channel direct modulated laser (DML) drivers that offer

the lowest power solution in the market. In addition, Macom's 127/129/131/133D-25C-LCG11 family of distributed feedback (DFB) lasers covers CWDM and PSM4 wavelengths, offering high-performance over broad operating temperature range. The M03002 and M03102 are single and quad-channel TIAs offering the industry's lowest noise and power consumption for 28G applications.

"This chipset demonstrates the value which Macom brings to our end customers and the industry as a whole," said Vivek Rajgarhia, VP of Strategy, Networks. "By providing the complete solution in a neat bundle, we can provide cost and power efficiency benefits which solve our customers' high speed networking challenges."

POET Technologies: From Lab To Fab

Can POET Technologies deliver commercial optoelectronic IC production? Rebecca Pool talks to CEO, Suresh Venkatesan, to find out.

TO SAY THE LAST FEW MONTHS have been action-packed for GaAs-based optoelectronic IC pioneer, POET Technologies, would be an understatement.

First, semiconductor industry trailblazers from Global Foundries and Applied Materials were hired. Second, the company hitched up with Anadigics to transfer its laboratory-proven VCSEL manufacturing to a commercial 6-inch process.

And now, investor relations advisor, Robert Ferri Partners, an organisation renowned for coaching up-and-coming tech-related businesses, has been brought in.

As Suresh Venkatesan, ex-Global Foundries senior vice president of technology development and now POET chief executive tells *Compound Semiconductor*: "To be taken seriously, the technology has to be transfered out of the lab and into something that can be manufactured on a wholesale basis."

"We're in the process of accelerating this transition today and will have detectors and VCSELs built using our proprietary process and Anadigics' commercial manufacturing process by the first quarter of 2016."

Talent grab

Venkatesan jumped aboard POET Technologies in June this year, joining former Global Foundries chief executive, Ajit Manocha, and ex-vice president of emerging technologies and products at Applied Materials, Subhash Deshmukh. Manocha is now co-executive vice chairman at the company while Deshmukh is chief operating officer.

The sudden swell of talent at POET has not gone unnoticed by industry pundits. One investor at US stock market analysis firm, Seeking Alpha, wrote at the time: "Professionals of this caliber simply do not leave leadership roles at multi-billion corporations for a tiny tech firm on a whim".

And as Venkatesan highlights, the move is exciting. "I've already taken many technologies from early concept to commercialisation but it's always been under the umbrella of large-scale companies such as Motorola and Global Foundries."

"With POET I get another chance to grow something from its concept phase that also has the potential to be substantially disruptive to the semiconductor industry," he adds.

The crux of POET's technology hinges on a patented materials system, pioneered by the company's chief scientist, Geoffrey Taylor. This supports monolithic fabrication of ICs comprising active and passive optical, and high-performance analog and digital electronics, components.

Right now, the company has its sights firmly set on manufacturing a 10 GHz VCSEL-based transceiver by early 2016, with the first step in its 'lab to fab' being to port its 3-inch fabrication process from the University of Connecticut's facilities to Anadigics' foundry in New Jersey.

The transfer is well underway and Venkatesan is confident that Anadigics is the place to be.

"There are multiple foundries out there, but Anadigics has a state-of-the-art six-inch facility," he says. "We're targeting high-volume, low-cost markets and having the cost advantage of larger wafers is so important. And to be frank, I didn't want to go through multiple wafer transitions."

Also critically for POET, the New Jersey-based foundry has 6-inch VCSEL processing capabilities.

"There aren't too many companies out there today that have this. Most foundries are still at three or four inch, while many six inch foundries in the Far East don't yet process optical components," points out Venkatesan.

"In terms of long-term high-volume manufacturing we're still evaluating who this will be, but it is this mix of six-inch

facility and VCSEL capability that has engaged us initially with Anadigics," he adds.

With foundry in tow, POET is also about to pin down its epitaxy wafer supplier. According to the chief executive, the company is currently working with several external epi-vendors with a single source to be announced soon.

"We're still in the process of scaling up here, but over the course of this year, as epi-wafers are built and qualified, we will finalise our exact source," he says.

High volume, low cost

POET's first target market is short-range data communications. Power-hungry server farms, for example, are already looking for alternatives to the direct attach copper (DAC) cable assemblies for short-reach interconnects.

According to Venkatesan, POET's VCSEL-based transceiver will provide the answer and be ready by 2017.

As Venkatesan highlights, thanks to its CMOS-based integrated process manufacturing, POET's components will be competitive with DAC.

"The main customer pain point in the DAC market is cost, and we are in parity with copper," he says. "But then the next important consideration is power and here, we can blow the socks off anything you get with DAC."

"We make what's on the wafer ten times more energy efficient, ten times cheaper and more than ten times smaller," he adds.

If successful at high volume manufacture, POET's monolithic opto-electronic process platform will extend the end of Moore's law, and even change the face of monolithic optical integrated circuit fabrication. But given the company's ambitious and aggressive commercialisation plans, how realistic is this goal?

Clearly cash could be a sticking point. Still at the end of September, the company unveiled a very healthy balance sheet of $20.5 million in cash, expected to carry development for the next eight quarters, well beyond prototype demonstrations.

And Venkatesan is confident that with the process proven on a large-scale, licensees will follow.

"You don't attract good licensees until you demonstrate the value of your technology as a real product," he says. "Our strategy is to now focus on products and tie up licensees in the transceiver space and adjacent market segments. Yes, our roadmap is aggressive, but a lot of development has been going on for a fair amount of time," he adds. "We are creating disruption; it's exciting and risky, but no innovation comes without risk."

GaN: beyond the basestation

As the GaN RF power amplifier penetrates wireless base stations, industry developments hint handsets could be next. Rebecca Pool talks to Qorvo to find out more.

IN A LITTLE over a decade, the mighty GaN transistor is transforming from novelty device into a must-have in a growing number of applications. Thanks to US government initiatives, GaN – with its staggeringly high power density – is the star technology in radar, electronic warfare and satellite, and is infiltrating more routine spaces, most notably wireless basestations.

Sumit Tomar, general manager of wireless infrastructure at Qorvo, is confident this passage to the more ordinary will continue. He believes GaN has already uprooted LDMOS, as the technology of choice for RF power amplifers in the high capacity base stations of 4G LTE network providers. And the endless need for greater network capacity and faster services, driven by rising mobile data demand, will only fuel this move.

"Next-generation base station platforms will go into production by the end of 2016, and we believe these will be based on high-power GaN RF amplification," he says. "LDMOS is limited beyond 2.4 GHz, so GaN comes into play here. At 4.5G and 5G we expect significant GaN adoption in base stations, particularly at frequencies greater than 1.8 GHz."

Tomar is also certain that network operators will opt for GaN-on-SiC power amplifiers, over GaN-on-silicon versions. GaN's impressive power density means devices can be housed in relatively small packages and still dissipate heat, but factor in silicon and this can change.

"Silicon has a poor thermal conductivity, compared to silicon carbide, and our customers are worried that GaN-on-silicon power amplifiers cannot dissipate heat as efficiently," he asserts. "This could reduce overall life cycle, raise the risk of field failure, which is a major issue for the basestation OEM customer."

"For power levels over 100 watts, all major players in the basestation market are not looking at anything on silicon for precisely this reason," he claims.

Right now, major GaN RF device providers, Cree, Sumitomo, Freescale, and of course Qorvo, are pursuing GaN-on-SiC processes. In contrast, MACOM prides itself on being the world's only provider of GaN-on-silicon technology for RF applications, with its devices being used in military and communications applications.

However, earlier this month, MACOM started sampling a GaN-on-silicon wideband RF transistor for operation up to 200 W, and reckons the device delivers a performance to rival GaN-on-SiC.

As Michael Ziehl, vice president of marketing RF and microwave at MACOM said at the time: "We expect to see ramping commerical adoption of our GaN technology in other RF applications in the future, including 4G/LTE base stations."

Still, Tomar is confident leading systems providers, Freescale, NXP Semiconductor and Infineon are all looking to adopt GaN-on-SiC over GaN-on-silicon.

"These players dominate the power market and are all pursuing GaN-on-SiC. GaN-on-silicon has a play at power levels less than 100 W, but at more than 300 W, the technology just isn't there," he says.

A different device

But basestations aside, industry players are beginning to explore the opportunities for high power density GaN power amplifiers in wireless handsets. Earlier this year, a group of researchers from Intel, led by co-director of Components Research in Technology and Manufacturing, Robert Chau, revealed an enhancement-mode GaN MOS-HEMT.

Designed for RF power amplifiers, as well as voltage regulators, in low power mobile silicon-on-chips, the researchers claim the transistor out-performs industry-standard GaAs RF power amplifier transistors in the power output and efficiency stakes.

Chau declined to comment on the latest development, but stated in his paper: "This work shows for the first time that the application space of GaN electronics can be expanded beyond the existing high-voltage power and RF electronics to include low power mobile SoCs."

Intel is the first company to publicly share such results, but doesn't appear to be alone in its development of GaN RF power amplifiers for next-generation handsets.

Tomar is quick to highlight Qorvo's GaAs process development, saying: "It gets tricky to put a higher supply voltage amplifier inside a handset but we have a unique pHEMT GaAs process that we can scale to serve the need of 5G handsets."

But at the same time, GaN HEMT development for power amplifiers in future handsets is clearly underway. "We are also working on GaN processes that I believe can go as low as 10V and in the future will go lower," says Tomar.

"I do not want to discuss this publicly," he adds. "But we will keep looking at different flavours of GaN, as well as other processes, and will see where the market goes."

Plessey: bright and bold

With a hefty £30m bank loan and massive expansion underway, where next for GaN-on-silicon LED pioneer, Plessey, asks Rebecca Pool.

IN SEPTEMBER, UK-based Plessey revealed plans for a massive £60 million expansion at its Plymouth LED facility, after securing a £30 million loan from Deutsch Bank and having won £6.7 million in local government funds.

"To actually get a tier one bank on board at this stage [of our company development] is quite an achievement and very exciting for us," remarks Plessey's chief financial officer, Iain Silvester.

"Using the Deutsch Bank Loan, Regional Growth Funds and our own cash generation, we will now add capacity as sales ramp," he adds.

Expansion plans are aggressive. Over the next two and a half to three years, the company intends to increase production capabilities by a factor of thirty – adding at least ten new reactors to the facility – while more than tripling the workforce to around 535 employees.

According to Silvester, come the end of next year around 150 new employees will already be on board, doubling today's headcount. The lion-share of new jobs will fall within the facility itself, with Plessey hiring more MOCVD operators, process engineers and skilled workers to manage the facility.

"We will see fairly modest growth on the commercial side of the business, but we operate all day and night, so really, this is going to be about scaling up production," says Silvester.

Since 2010, Plessey has been developing GaN-on-silicon LEDs using two Aixtron Crius II MOCVD reactors in a 7 by 6-inch wafer configuration. But this is set to change.

As Mike Snaith, Plessey's operations director points out, the company has all the necessary tools to support current MOCVD throughput, with some redundancy.

However, to scale production, Plessey will now buy two additional reactors and expand bulk gas capability ready for at least another ten MOCVD reactor chambers, capable of 6-inch and 8-inch LED manufacture. The company has yet to confirm whether or not the new reactors will be sourced from Aixtron, Germany, or Veeco, US.

"Our Plymouth site has three clean room areas and our intention is to have all in-house capability for high-volume MOCVD GaN-on-silicon growth, high precision and large die alignment, deep trench etch, wafer bond and lift-off as well as a full back-end toolset," says Snaith. "One of the clean rooms will retain CMOS tooling to add additional passive components and allow for the manufacture of monolithic LEDs."

And production will, at least for now, remain at Plymouth. "A typical competitor will have between fifty and one hundred reactors, and we are now looking to have about fifteen in our facility over the next three to four years," says Silvester.

"Whether or not we continue to manufacture in the UK, beyond this point, we will have to see, but growth over the next four years will certainly be driven by our Plymouth facility," he adds.

More integration

In addition to rapid expansion, silicon-based chip-scale packaging is well underway at Plessey, and the company intends to develop a range of integrated LED devices, that have, for example, power management and sensors, integrated into the silicon platform. At the same time, the company has recently patented technology relating to chip-scale optics, in which the LED lens is integrated on-chip.

According to Silvester, development will now continue apace, with the first integrated LED products reaching market as early as the second quarter of next year.

"Everyone understands the cost advantage that using silicon wafers will bring but this is actually secondary to some of the integration that we can provide within the device," says Silvester.

"Silicon substrates offer opportunities that just aren't available to sapphire, so using our existing CMOS skills and our engineering base, we will now develop these integrated LED devices."

But integration aside, a key goal for Plessey has been to move from 6-inch to 8-inch wafer fabrication. The LED manufacturer has been working closely with Aixtron to address the MOCVD reactor re-tooling issues that accompany scaling, and Silvester asserts the latest Deutsche Bank backing will now accelerate this transition.

"We have an ongoing programme devoted to our eight inch process and most certainly we'll be moving towards eight inch production within four years," he says.

"Next year the new reactors will be six inch and beyond that we'll be re-tooling to eight inch," he adds. "Clearly a key goal is to set up eight inch production as fast as we can."




6th CS International Conference

2016 Brussels Belgium

CS International 2016 will provide timely, comprehensive coverage of every important sector within the compound semiconductor industry.

The 6th CS International conference will be held at the Sheraton Brussels Airport Hotel, in Belgium on Tuesday 1st & Wednesday 2 March 2016. The sixth CS International conference will build on the success of its predecessors, with industry-leading insiders delivering more than 30 presentations spanning sectors.

Visit **www.cs-international.net** for further information on this event

Book your place NOW !

Visit www.cs-international.net/register.php to secure your place

TWO DAYS, FIVE THEMES

OVER 30 INSPIRING PRESENTATIONS

Five key themes lie at the heart of CS International 2016:

- The quest for 5G,
- Driving deployment of wide bandgap power devices
- Exploiting opportunities for LEDs and lasers
- Making heterogenous integration a hit
- Capturing light, generating cash

Within each topic there is a key-note presentation from one of the most influential companies within this sector; one talk by a leading market analyst who will discuss trends within the industry and presentations by the leaders of firms developing cutting-edge technology in this field.

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry.

Conference Chair:
Drew Nelson President, CEO, IQE

This two day event covers five themes

The Quest for 5G

What challenges will GaAs and CMOS power amplifiers face in making the transition from 4G to 5G? And will faster data links play into the hands of GaN-based amplifiers for base stations?

KEYNOTE **James Klein: Qorvo** | Compound semiconductors: At the core of 5G

ANALYST **Eric Higham: Strategy Analytics** | Will chipmakers and foundries benefit from 5G?

SPEAKERS

Duncan Pilgrim: Peregrine Semiconductor | CMOS: Game on!

Peter Gammel: Skyworks Inc | Technology requirements and initiatives for 5G smartphones

Takahisa Kawai: SEDI | GaN for 5G base stations

Driving deployment of wide bandgap power devices

Is SiC set to displace silicon in electric cars? And how will this material help to revolutionise the efficiency and operation of electrical grids?

KEYNOTE **Daniel Fernandez: EU Project SPEED** | Silicon carbide wide band-gap devices for energy applications

ANALYST **Pallavi Madakasira: Lux Research** | Hype versus reality: driving adoption of wide band gap power electronics

SPEAKERS

Peter Ward: Anvil Semiconductors | Driving down the cost of SiC devices for consumer applications

Markus Behet: EpiGan | GaN on silicon – a truly revolutionary semiconductor technology matures

Hans-Joachim Würfl: FBH Berlin | GaN normally-off devices for highly efficient power switching

Marta Borasio: Laytec | Reliability and yield limiting variances in power-electronic manufacturing - early detection by advanced in-situ monitoring

Mark Dineen: Oxford Instruments Plasma Technology | Latest developments in plasma etch processing for power and RF devices

Yumin Gao: Evans Analytical Group | Advanced material characterization for Compound Semiconductor R&D and Manufacturing

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry.

Exploiting opportunities for LEDs and lasers

Can LED bulbs meet the most demanding lighting applications, such as those found in the retail sector? And what are the opportunities for infrared and ultra-violet LEDs?

KEYNOTE Abdelmalek Hanafi: BMW I Doubling driver visibility with laser-based headlights

ANALYST Pars Mukish: Yole Développement I Opportunities for IR LEDs

SPEAKERS

David Cheskis: Anadigics I 6-inch VCSEL wafer fabrication manufacturing advances

Augustinas Vizbaras: Brolis Semiconductors I Mid-infrared light sources: manufacturability and applications

Paul Crump: Ferdinand-Braun-Institut I High-power, high-efficiency lasers for fibre lasers and other markets

Reinhard Windemuth: Panasonic I Solutions for LED manufacturing

Bedwyr Humphreys: Seren Photonics I Semi-polar Gallium Nitride enabling super high power automotive LEDs

Making Heterogenous Integration a Hit

III-V channels are poised to make an introduction in next-generation logic circuits. But how will they be introduced, and what impact will they have?

KEYNOTE Yanning Sun: IBM I III-V/Si integration: Moore and more

ANALYST Nadine Collaert: IMEC I Heterogeneous integration of high mobility materials on a 300mm Si platform

SPEAKERS

Suresh Venkatesan: POET Technologies I A comprehensive technology platform for opto-electronic Integration

Lukas Czornomaz: IBM I Hybrid IIIV/SiGe technology for CMOS and beyond, opportunities for 3D monolithic integration

Thomas Uhrmann: EVG I Heterogeneous Integration enabled by Advanced Wafer Bonding

Capturing Light, Generating Cash

What is needed to kick-start significant deployment of concentrating photovoltaic technology? And what are the opportunities for III-V detectors operating in the infrared?

KEYNOTE Carlos Algora: Technical University of Madrid I Perspectives of concentrator photovoltaic technology

ANALYST Frank Dimroth: Fraunhofer ISE I Terrestrial III-V solar cells - challenges and opportunities

SPEAKERS

Paul Sharps: Solaerotech I High efficiency multi-junction solar cells - what's next?

Andreas Umbach: Finisar I Propelling detectors to 100 Gb/s and beyond




Book your place NOW !

Visit www.cs-international.net/register.php to secure your place

PLATINUM SPONSORS

AIXTRON

EAG Evans Analytical Group

EPIGAN

evatec process systems

EVG

LAYTEC Knowledge is key

OXFORD INSTRUMENTS The Business of Science®

seren photonics

Temescal

Veeco

YOLE Développement

GOLD SPONSORS

CS CLEAN SYSTEMS® Exhaust Gas Abatement

IQE

Lasertec

NORSTEL

united monolithic semiconductors

ums

KLA-Tencor

ADDITIONAL SPONSORS

Delegate Bag sponsor: qorvo

Lanyard sponsor: PFL

Portfolio sponsors: Plasma-Therm

Exhibitor sponsor: KITEC, Panasonic

Wi-Fi sponsor: BROLIS SEMICONDUCTORS

Supported by: EPIC European Photonics Industry Consortium

MACOM set to mass market GaN

Will MACOM's latest GaN-on-silicon transistor nudge GaN from niche to norm, asks Rebeeca Pool.

WITH A SPOTLIGHT ON GaN, September was quite a month for MACOM. Celebrations of shipping more than one million GaN-on-silicon RF power devices were swiftly followed by the news that the company was sampling 100 W GaN-on-silicon HEMTs.

The latest continuous-wave wideband transistor, designed for DC to 2.7 GHz operation, boasts a 70 percent drain efficiency, which appears to have got many RF industry players excited.

As MACOM highlights, the latest 100 W transistor can now deliver a performance to rival more expensive GaN-on-SiC, with a cheaper volume production cost structure than LDMOS.

"We've made a breakthrough in drain efficiency which is now 10 percent better than the best of the LDMOS parts, targeted at similar applications in ISM frequency band applications," highlights Mike Ziehl, vice president of RF and Microwave. "So for the same given CW power, you have less heat dissipation and can reduce the costs of cooling and power supplies."

"These 100 W devices have caused some excitement, particularly in the RF Energy community," he adds.

MACOM manufactures both GaN-on-silicon and GaN-on-SiC HEMTs, and from word go has firmly outlined where it believes each technology belongs. Due to the high cost of growing SiC boules, this flavour of transistor will service low-volume, niche applications such as broadband electronic warfare jammers and radar systems, where the emphasis is also on performance.

In contrast, GaN-on-silicon has already been proven in military communications applications and MACOM is certain that cost-sensitive, high-volume applications will embrace the technology on 8-inch wafers. Indeed, the company is in the process of scaling manufacture to larger wafer sizes.

"We have long been a leader in L-band and S-band pulsed power radar and customers looking for the ultimate in performance still prefer GaN-on-SiC," says Ziehl.

"But for higher volume, commercial applications, we think GaN-on-silicon has to be the solution."

Right now, MACOM has its eyes on RF energy applications, such as the magnetron-powered microwave oven. In late December 2014, Freescale caused a furore when it delivered the first silicon LDMOS FETs to replace the mighty magnetron in the microwave oven. But the excitement could be short-lived.

"Solid state devices can be used to control cooking much more accurately than a magnetron, but the LDMOS transistor is only 60 percent efficient so you are giving away efficiency in today's systems," points out Ziehl. "Our Gen4 GaN-on-silicon transistor is much closer in efficiency to the magnetrons used in existing systems, which will make a big difference to manufacturers of the end product."

Thermal concerns

Other new markets for the 100 W GaN-on-silicon HEMTs include automotive ignition and plasma lighting, but what about base stations? GaN-on-SiC power amplifiers are beginning to uproot LDMOS devices in high capacity base stations of 4G LTE networks.

However, concerns over silicon's poor thermal conductivity, relative to SiC, could slow demand for GaN-on-silicon versions. As Qorvo wireless infrastructure general manager, Sumit Tomar, told *Compound Semiconductor,* in late September: "Our customers are worried that GaN-on-silicon power amplifiers cannot dissipate heat as efficiently."

Ziehl disagrees. While the vice president did not want to detail customer discussions, he highlighted: "This is not a materials discussion on whether its silicon or silicon carbide, this is a product discussion."

Indeed, as Ziehl highlights, during GaN-on-silicon HEMT manufacture, MACOM thins its wafers, optimises the die attach and die attachment methods, die layout and more.

Will the latest 100W GaN-on-silicon transistor open new markets for the GaN technology?

"We pay attention to every step of transistor assembly, and even at 100 W, I can show you our GaN-on-silicon parts that have a better thermal rating than other manufacturer's 100 W GaN-on-SiC parts," he asserts.

"We have customers that come to us and say, 'well I need a SiC transistor as its thermally superior', and then we educate them as to what our GaN-on-silicon product does compared to other products in the market at similar power level," he adds.

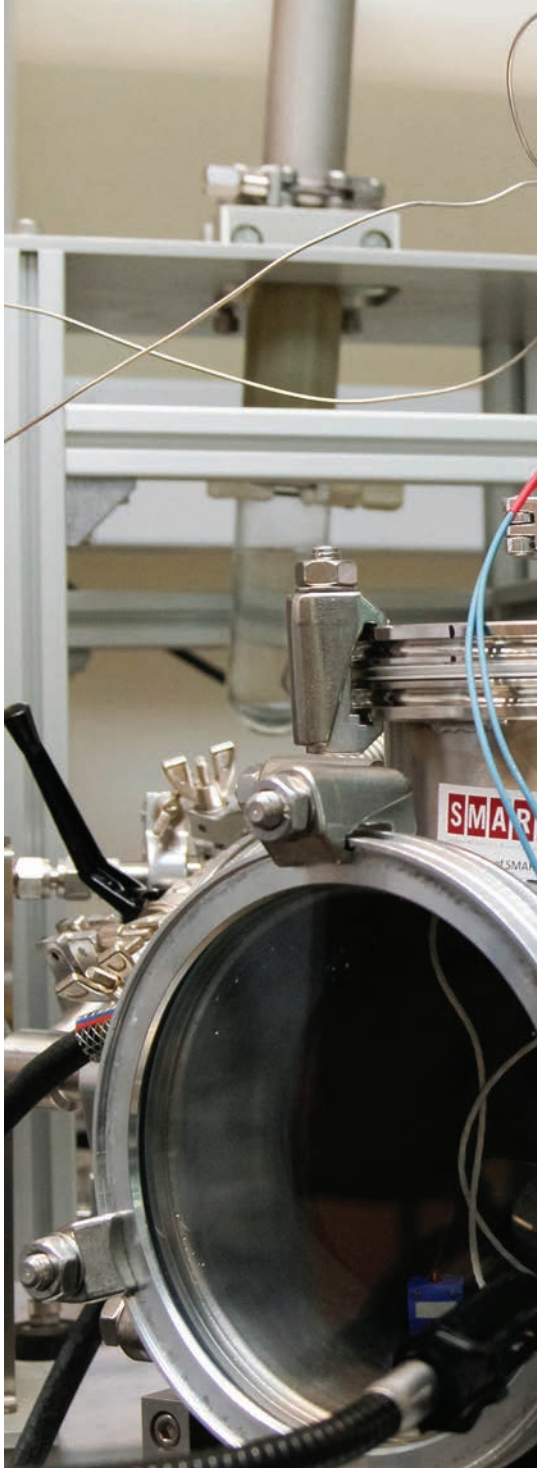
So where next for MACOM's GaN-on-silicon technology? According to Ziehl, the 100 W HEMTs are only the first in a family of 200 W and 300 W transistors; these are expected to sample late this calendar year.

What's more, the company also expects its first GaN-on-silicon devices to enter high-volume production in 2016, which will surely mark a watershed for commercial GaN. Still, the vice president remains balanced.

"This is all about offering the right choice of GaN to the application. If you look at RF energy, it's higher volume so GaN-on-silicon is the solution, but for electronic radar, its GaN-on-SiC," he says. "We offer what meets our customers' challenges, and sometimes they buy both."

Delivering the future

With III-V and CMOS integration well underway, novel ICs from Singapore-MIT program, SMART-LEES, could reach market soon. Rebecca Pool reports.



FROM THE OUTSET, researchers from the Singapore-MIT Alliance for Research and Technology, working on low-energy electronics systems, decided not to reinvent the wheel.

Brought together by the Singapore government and MIT in January 2012, the SMART-LEES team intends to create fundamentally new integrated circuits based on III-V materials and silicon as Moore's Law collapses. And according to academic Eugene Fitzgerald from MIT, working with silicon has always been the priority.

"Silicon foundries already have CMOS manufacturing in place and these organisations can't be expected to change processes just to carry out crazy stuff for universities," he says. "Yet, whenever someone comes up with a new device it is difficult to insert that into the manufacturing infrastructure."

"We know from a capital point of view it doesn't make sense to build new infrastructure end-to-end for this," he adds. "So from the very beginning we have said that III-V materials have to fit into a silicon design kit."

With this in mind, researchers from the SMART-LEES programme, based at MIT, National University of Singapore and Nanyang Technological University, have been working with myriad industrial partners on this very issue.

Silicon CMOS powerhouses, Global Foundries, Singapore, and Japan-based Tower Semiconductor-Panasonic joint venture, TPSCo, are key manufacturing partners. Meanwhile Aixtron, Germany, IQE, UK, Austria-based EVG, and Samco of Japan, all join forces with the project later on along the IC supply chain.

And with weighty board members from IQE, Netherlands-based Lumileds and Analog Devices, US, also backing the project, SMART-LEES clearly has clout.

"We set up the board to have stakeholders that would be interested in seeing this succeed," highlights Fitzgerald.

"But we also put together a research team from materials, device and circuit design that can simultaneously influence each other," he adds. "And because we can't re-work the entire CMOS process, we developed 'modular processing'."

Here, the researchers take 200 mm silicon wafers from the front-end of their partner's CMOS manufacturing processes and then use existing CMOS design tools to develop novel ICs at the SMART-LEES 200 mm facility in Singapore.

This fab houses two Alixtron CRIUS reactors and *in-situ* optical monitoring tools, so here, III-V layers are added and devices are fabricated. The wafer is then returned to the foundry for the back-end processes that connect the III-V and silicon CMOS devices within the die.

"We've set up LEES so we can add any kind of III-V material, but it has to be done so that the wafer looks like it never left the foundry," says Fitzgerald. "The wafer will return with dielectric and contact areas so that you start the back-end of the foundry process, it looks like it never left."

LEES has a cleanroom equipped with epitaxy and microfabrication tools capable of handling 200 mm wafers, and a characterization facility providing inspection and characterization of wafers and devices. Credit: SMART LEES

And as he adds: "What this actually does is to induce innovation that is exactly aligned to future manufacturing requirements. We innovate around, say, particular temperatures and processes so [our results] are ready for commercialisation."

Indeed, in 2012, the LEES team started work on GaN, GaAs and InP deposition on silicon substrates, but as Fitzgerald points out, 'things have moved on'. The researchers are now focusing on InGaAs and GaN, integrating an InGaAs HEMT, GaN HEMT and GaN LED into silicon design platforms.

"We now have an entire process and design toolkit which can include lattice-mismatch engineering such as aspect ratio trapping and metamorphic buffers," explains the MIT Professor. "We do a lot of epi- and wafer-bonding, and have basically created an engineered substrate that can support whatever device we want."

"We transfer the CMOS processes to the top of this, process the III-V devices... and send them back to the foundry," he adds. "So we can design, for the first time, circuits as part of a very real foundry process, and that's not easy to do. There's no special research process and this is unique."

Clearly, the main thrust of the LEES manufacturing model is to get novel integrated circuits into the marketplace faster and more easily, but when will industry see real devices? It could be sooner rather than later.

According to Fitzgerald, test chips will be delivered next year and he expects to see prototypes in very real applications some two to three years later.

"We pretty much know how to put III-Vs onto silicon wafers, but when we started, the complete unknown was how to then transfer the CMOS onto this engineered substrate," he says. "But we're now moving wafers back and forth between the foundry and thanks to sizable enough funding, our companies and researchers can collaborate in ways that wouldn't normally be possible."

"Soon, we're going to have the one thing that everyone wants," he concludes. "And that's to have a design kit for both III-V devices and CMOS."

Suppliers of optical components are benefiting from the growth in cloud computing and internet traffic. One company in this position is Oclaro, which is sampling its QSFP28 transceiver to data centres upgrading to 100G infrastructures.

Oclaro hits 2016 on a high

Following a hefty restructure, Oclaro posts impressive financials. Can industry expect more of the same, asks Rebecca Pool.

EARLIER THIS AUTUMN, optical component and module supplier, US-based Oclaro, revealed a key milestone in its first quarter 2016 financial results that set investors buzzing.

By generating its first positive adjusted EBITDA of $4.2 million, it had spectacularly increased what is essentially net income by $25 million in just two years.

At the same time, $87.5 million revenues came in at the high end of guidance, up by more than $5 million from the fourth quarter. And gross margin reached 2 percent, marking an increase of 6 percent from last quarter.

Clearly the results spell good news for a company that has recently taken severe measures to reach profitability.

In 2014, chief executive, Greg Dougherty, announced a major re-structuring programme, culling staff numbers by some 50 percent to 1500.

Meanwhile, operating sites were reduced and the company's GaAs laser diode business sold to II-VI for $115 million, bringing in some $88 million in cash.

Following the results, shares stood at $3.38. They have edged upwards throughout the past year as rival Finisar shares drift down. And as Dougherty said in his recent earnings call: "We have firmly put the turnaround challenges behind us."

Alex Henderson, senior analyst at US-based investment banking and asset management firm, Needham, was somewhat surprised by Oclaro's latest results.

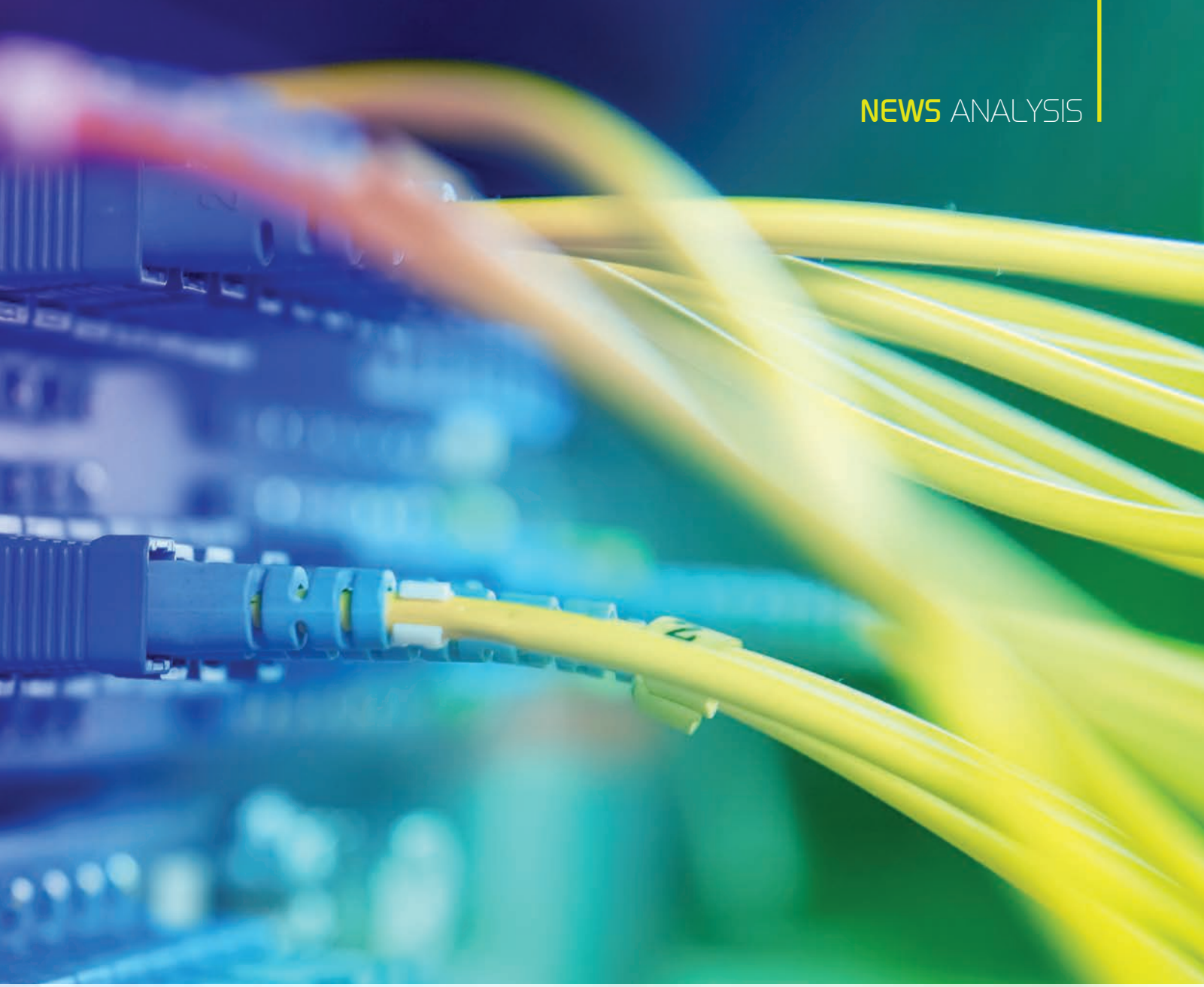
As he tells *Compound Semiconductor*: "Revenues were ahead, but within the range of expectations for improving growth. [But] we were surprised at the sharply better than expected gross margins."

The Needham analyst attributes the company's results to three key factors: first, production is streamlined; second, money-losing legacy products have been ditched; and third, manufacturing takes place in regions that have benefited from a strong US dollar; namely Japan and Europe. And now, Oclaro looks set to achieve profitability.

"The company is on the cusp of profitability," says Henderson. "It's already cash-flow positive, and while annual price reductions in the March quarter are likely to slow improvement, it will likely hit the mark in the June quarter."

Potent products

According to Oclaro's Dougherty, latest quarterly revenues were primarily



driven by its 100G product lines. 100G product revenue grew by $7 million, or 20 percent, compared to the previous quarter, and now represents some 47 percent of total sales.

This isn't an enormous surprise. While 100 Gigabit Ethernet has been a long time coming, industry pundits predict 2016 is set to be a breakthrough year.

IHS Infonetics, for one, has predicted next year will be 'huge' for 100G as products reach market and internet content providers, for example, shift from 40G to 100G optics, driving sales.

Anticipating rising demand for 100G transceivers, Oclaro increased capacity for its 100G client-side transceivers in early 2015 and has been sampling its QSFP28 transceiver to data centres upgrading to 100G infrastructures. It has also started shipping its DWDM lineside analog-coherent transceiver – deemed to be the company's 'biggest deal' by Henderson – for deployment in this quarter.

And pleasingly for Oclaro, demand from China, for client and lineside 100G products, is rising.

According to Dougherty: "It appears our customers are preparing for awards for 100G systems from China Mobile and China Telecom... and we expect to see continued 100G sales growth in China."

Henderson concurs, and points out that other industry players including MACOM, Inphi, Oclaro and Lumentum are also reporting ramping China orders.

"This demand is likely to cause abnormal demand in the first half of 2016," he says. "If stronger China demand picks up enough, it could cause [Oclaro's] March quarter to buck seasonal patterns, resulting in even earlier [profitability]."

So the future looks bright for Oclaro. With shrewd product development beginning to pay off, it has nearly clawed its way back to profitability.

But competition is fierce, and size-wise, the company is small compared to the likes of Finisar and even NeoPhotonics. Could scale be an issue?

Henderson thinks not. "Competition is stiff in VCSEL short-range optics but less so in [Oclaro's] high-end integrated segment," he says,

"Also, we do not see China-based players moving up in scale with the fab and integrated optics capabilities. Oclaro has a very good technology and strong management with a clear roadmap," he adds. "This and its strong offerings could vault them over the next few years."

InP: Great expectations

As AXT buys Crystacomm, Morris Young, AXT CEO, tells Rebecca Pool about plans for 6-inch InP substrate growth, mobile markets and more.

EARLIER THIS YEAR, compound semiconductor substrate maker, AXT, acquired California-based InP substrate developer, Crystacomm in an all-cash deal.

While AXT is perhaps best known for supplying wireless device markets worldwide with GaAs substrates, the California-based business also grows InP substrates, which begs the question; why buy Crystacomm? The answer lies in markets and quick, cost-effective crystal growth.

Ten years ago, AXT's GaAs substrate sales were rising rapidly, largely thanks to increasing GaAs content in mobile products and a resurgent LED industry.

Smartphones, netbooks and more, were supporting new features that demanded an increasing number of power amplifiers and switches, reliant on GaAs substrates.

Meanwhile, automotive and display lighting was driving LED sales with 2-, 3- and 4-inch GaAs substrates scooping the lion's share of the market.

Fast-forward a decade and the semiconductor market is a different place. "The cellphone switch business, which we supplied with GaAs pHEMTs, has been beaten back by SOI taking market share," points out AXT chief executive Morris Young. ""The GaAs landscape has taken this on the chin; for example, Hitachi Cable went out of business."

"Also, business opportunities do exist for LEDs, but pricing pressures have been very severe, so we don't have a lot to report here," he adds.

But amid the struggle, InP has become, in Young's words, 'AXT's bright spot'. As the chief executive highlights: "In 2010, InP substrates were a small portion of our revenue contribution, but this business segment has since grown very nicely and InP now claims the largest proportion of our revenue."

New applications

Right now AXT's InP substrates are largely supplied to manufacturers of lasers and photodetectors for fibre-optics network applications, including fibre-to-the-home as well as data centre communications.

However, device manufacturers are increasingly keen to harness the material's high electron mobility in the fabrication of HBTs and HEMTs. Indeed, looking to the future, 5G mobile networks could hold tremendous promise for this flavour of substrate.

According to Young, next-generation wireless communications networks will demand frequencies as high as 25 GHz, which devices fabricated on silicon substrates, and even GaAs wafers, will struggle to support.

"InP is the natural choice as it has the properties to enable the increasing requirements of 5G, and is also lower in cost and power consumption than GaN," he says. "We know a very large wireless device maker has been looking at InP very seriously."

And this is where AXT's latest acquisition is important. Crystacomm was the first to deliver 2-, 3- and 4-inch commercial InP substrates and is also leading the development of 6-inch InP technology, which could prove vital to the development of cost-effective, InP-based transistors for 5G wireless devices.

What's more, while AXT has pioneered Vertical Gradient Freeze (VGF) growth for InP, and other substrates, Crystacomm has focused on Liquid Encapsulated Czochralski (LEC) growth.

Compared to LEC growth, VGF growth can produce substrates with relatively low defect densities and higher mechanical strengths, leading to better epi-layer quality and higher circuit yields during device production, as well as superior device performances. But when it comes to 6-inch InP wafers, VGF growth is simply too expensive.

As Young asserts: "If you want a substrate with a very low etch pit density and low stress then VGF is the way forward, in fact VGF has won the race in producing materials for GaAs-based devices."

"But in HEMT and HBT applications, LEC has hung on to the market for quite a while, and has this unique opportunity to bring the larger diameter of 6-inch InP

into play at potentially higher yields," he adds. Young won't yet confirm that, for example, the etch pit densities, in 6-inch, LEC-grown, InP substrates will be sufficiently low enough for next-generation wireless devices.

6-inch InP substrate growth is in its infancy, and as he highlights: "6-inch GaAs took a US Defense Production Act Title III program and millions of dollars in funding to achieve. This is a fairly major task and we still need partners."

But the prospect is clearly there and in the meantime, he is keen to offer AXT customers a choice of VGF- or LEC-grown substrates.

"Internally we will allow the technologies to compete," he says. "If, for example, you can tolerate a slightly higher etch pit density, then we could provide you with an LEC material at, perhaps, a discounted price."

Work in progress

Right now, Crystacomm's crystal-growth equipment and processes are being installed at AXT's Fremont facility. Crystacomm founder and chief executive, George Antypas, is leading activities and will stay on as a consultant to AXT.

Equipment includes a 6-inch crystal growth prototype system but as Young emphasises, the prime focus will be to repeat what Crystacomm can do with its 2-, 3- and 4-inch crystal growth equipment at the Fremont facility. The team intends to turn to the 6-inch system in a year, to a year and a half. Looking to the longer term, Young is excited about the potential market opportunities for InP substrate providers. As he highlights, right now, only a few InP providers exist including, AXT, Sumitomo Electric, WaferTech and InPACT.

"During the nascent stage of GaAs, there were around twenty substrate makers worldwide although many have now dropped out," he says. "In comparison, in InP, we only have a few. The material is very challenging but I believe we can develop it."

Beyond

As solid-state GaN power amplifiers permeate radar applications, UK developer, Diamond Microwave, is eyeing new markets. Rebecca Pool reports.

EARLIER THIS AUTUMN, UK-based Diamond Microwave launched its latest in a rapidly growing line of GaN-on-SiC pulsed solid-state power amplifiers that can also operate in continuous wave mode.

The latest 1 kW X-band device operates over a 1200 MHz bandwidth, at 9.5 GHz, is described as ultra-compact and primarily targets the radar applications that traditionally would have relied on travelling wave tube amplifiers.

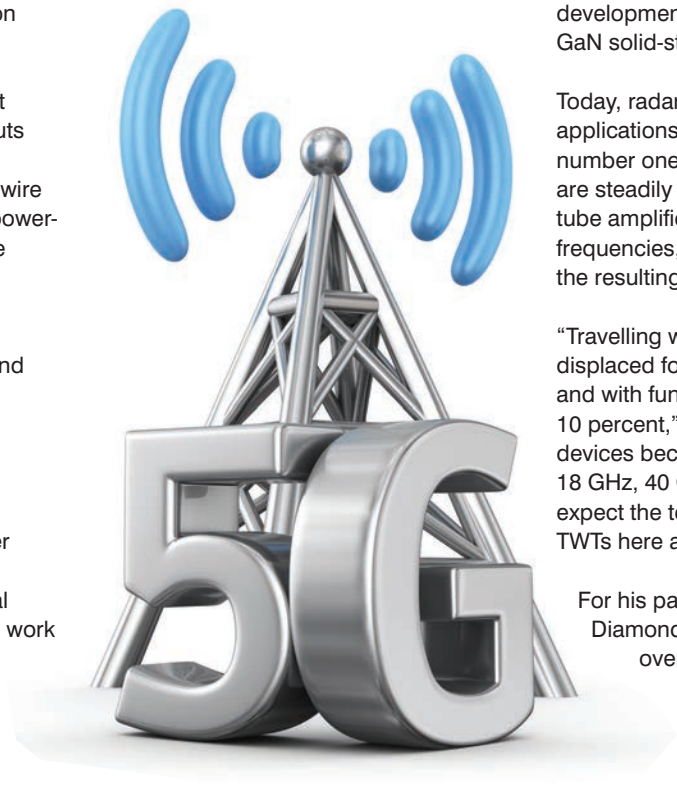
As Ian Davis, business development manager at Diamond Microwave, puts it: "Like all our GaN solid state PAs, these amplifiers employ a chip-and-wire microwave design.... and [have] a power-to-volume ratio that we believe to be among the highest in the industry."

Since it span out from the diamond electronics team of synthetic diamond materials developer, Element Six, in 2006, Diamond Microwave has witnessed much change.

Setting out to develop a diamond MESFET for future microwave power modules, chief executive, Richard Lang said at the time: "The technical challenges are high... there is much work to be done to realise a practical device."

And he was right. Five years later, diamond transistor development had dwindled, and as Davis now says: "We successfully demonstrated that the approach most researchers were using to produce a diamond transistor was flawed."

Still, the time wasn't wasted. According to the business development manager, Diamond Microwave had built a GaN power amplifier with the intention of replacing its GaN transistors with a diamond-based version.



Clearly, this was never meant to be, but as Davis highlights: "GaN was now emerging as a practical semiconductor material and we had developed a very good GaN amplifier here."

"We won a major contract with a prime defence manufacturer for further development and are now producing GaN solid-state power amplifiers."

Today, radar – both civil and defence – applications are Diamond Microwave's number one market. GaN power devices are steadily displacing travelling wave tube amplifiers at higher and higher frequencies, and the company is chasing the resulting market share.

"Travelling wave tubes have already been displaced for applications under 18 GHz and with functional bandwidths up to 10 percent," says Davis. "And as GaN devices become available to operate at 18 GHz, 40 GHz and beyond, we can expect the technology to displace the TWTs here as well."

For his part, Davis is convinced Diamond Microwave has an edge over other manufacturers of GaN power amplifiers, such as Korea-based RFHIC and Communications & Power Industries, US. As

radar

he highlights, competitors tend to source packaged transistors and amplifiers and integrate these into a power amplifier, but Diamond Microwave works with bare die and incorporates additional circuitry for, say, biasing and matching.

"[Competitors] are taking standard products but these aren't matched with the operating bandwidth or maximum power at a particular frequency," he says.

"Our hybrid manufacturing technique using chip and wire has an advantage," he asserts. "We operate with the bare die, and match these to get wider operating bands and higher power levels, and we also make a more compact, light-weight amplifier."

And while the company integrates GaN-on-SiC devices into its amplifiers, it is, as Davis says, 'technology agnostic'.

"We use GaN as it is the best semiconductor when we are looking to reduce size and weight," he says. "But if, say, a packaged LDMOS or GaAs device were more appropriate to solve a problem, then we would use this technology."

Looking ahead, Davis reckons Diamond Microwave's future won't be all about radar. The compact lightweight attributes of its devices, combined with the fact that these can operate on continuous wave mode, could open up a whole new market to the company; wireless communications.

GaN power amplifiers are already replacing silicon LDMOS devices in today's basestations. And as Davis points out: "GaN has also been recognised as a key enabler for the hardware that is going to support 5G networks, and certainly with respect to 5G, we have already witnessed a keen interest in GaN."

"The opportunities for us are at the higher power levels of wireless infrastructure and I think GaN could find a place in, say, the local nodes of wireless backhaul networks," he adds. "We have been talking to communications companies and hope to team up and develop [systems] where size, weight and power are important; this is a market we would like to develop."

GaN transistors

Breaking barriers to widespread adoption with silicon substrates

Grow GaN transistors on silicon and their bang-per-buck increases, widening deployment from defence markets to mainstream commercial applications

BY TOM KOLE FROM MACOM

DESIGNERS of power amplifiers have several challenges they face when designing high-power, broad-bandwidth amplifiers: low load impedances and the presence of performance-impairing parasitics.

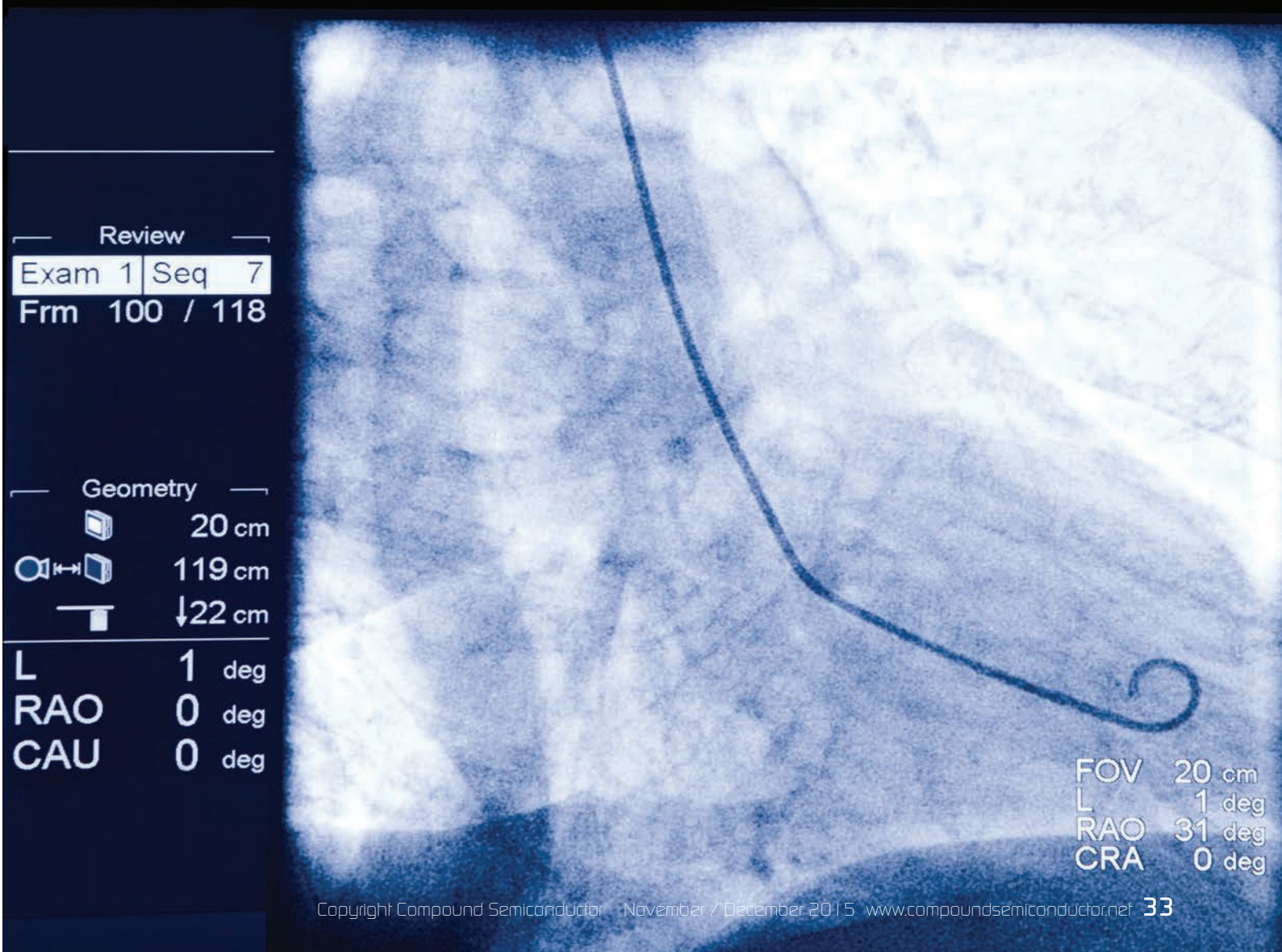
The former challenge stems from an output load line impedance that is naturally low, and falls off with increasing power. To address this, designers craft matching circuits that interface to 50 Ω. The bandwidth, efficiency, and complexity of the design are then governed by the ratio of the impedance of the 50 Ω interface to that of the transistor. One solution to this challenge is to use the smallest device with intrinsically higher impedance such as a transistor that operates at higher operating voltage. For example, at 100 W increasing the voltage from 12 V to 48 V results in a significant increase in load impedance, in this case from less than 1 Ω up to 12 Ω. It is a squared relationship, so quadrupling the operating voltage raises the load impedance 16 fold. This higher impedance allows for much simpler matching networks but also allows the potential for much wider bandwidth designs.

The second challenge – parasitics – is particularly problematic when designing wideband power amplifiers. At lower frequencies, resistive elements of the FET-equivalent circuit tend to dominate; but at higher frequencies they are overtaken by the effect of input shunt capacitance between the gate and source and the output shunt capacitance between the drain and source, which together drive down impedance and raise the quality factor, Q. Put another way, the impedance becomes more reactive and rotates around the Smithchart, i.e it varies with frequency.

A very attractive option for addressing both of these challenges is to turn to GaN transistors for power amplifier designs. Compared to the incumbent technologies of GaAs at high frequencies and silicon LDMOS in the lower bands, GaN naturally supports operation at higher voltages, allowing more power at higher frequencies. Additionally, GaN's higher power density allows for physically smaller devices than their legacy counterparts, which results in both lower intrinsic high-frequency effects, and lower input and output capacitances. The resulting lower Q characteristics of GaN allow for previously unobtainable wideband amplifier designs capable of covering multiple octaves at very high power levels.

Virtues of GaN power amplifiers are not limited to a wider bandwidth. They include an efficiency exceeding 70 percent; a ground breaking power density; and a capability to operate reliably at higher temperatures than other semiconductor technologies, which again allows for physically smaller devices. Combining these assets with an electron mobility that is similar

Right: Solid-state RF energy offers numerous benefits unavailable via alternate solutions, powering applications like Medical Ablation


Review
Exam 1
Seq 7
Frm 100 / 118
Geometry
20 cm
119 cm
22 cm
L 1 deg
RAO 0 deg
CAU 0 deg
FOV 20 cm
L 1 deg
RAO 31 deg
CRA 0 deg

GaN enables a constant output power, zone-controllable heating and a ten-fold hike in oven lifetime.

to GaAs enables the construction of transistors delivering high power at high frequencies, while sporting far smaller parasitics than their rivals.

Due to these strengths, it is of no surprise that GaN is steadily becoming recognized as the optimal solution for mainstream applications in many different markets. Amplifiers made from this wide bandgap semiconductor material are expected to proliferate into every aspect of commercial and consumer RF power markets.

Expanding horizons

In defence communication and electronic warfare, where the emphasis is on performance, GaN has rapidly displaced LDMOS. This explains why this sector led the way in embracing GaN over the last decade in applications needing semiconductor devices with a high efficiency and a broad bandwidth. Here, one of the appeals is replacing multiple narrowband LDMOS channels with a single wideband one made from GaN that offers comparable or better gain, power, and efficiency. Armed with these attributes, designers can build systems that are smaller and more efficient. In handheld radios this lower battery demand reduces weight, which is everything to a dismounted warfighter.

But the next market that GaN will conquer is much closer to home. Commercial telecommunication systems require highly linear PAs and power efficiency is becoming critical for a host of practical reasons. Infrastructure waveforms use complex OFDM schemes to shoehorn as many bits as possible into a given bandwidth, and the energy has to remain in-channel to prevent interference. Power amplifier designers have employed several linearity enhancing techniques over the last couple of decades, moving from single carrier with simple back-off, to feedforward multi-carrier in GSM networks. Today, the optimal solution is a combination of Doherty combining and digital pre-distortion (DPD). Doherty gives high power efficiency with high peak-to-average ratio (PAR) waveforms, and DPD reduces the vector errors and adjacent channel interference.

So how does GaN perform in this contemporary architecture? The answer starts with an understanding of a key fundamental behavioural difference between GaN and LDMOS. LDMOS has a so-called hard compression characteristic, that is, it is very linear to near P1 dB, but compresses, or limits, just above that level. In other words, PSAT is a hard limit, encountered abruptly and the transition between linear and non-linear regions is almost a point. GaN has a soft compression point. P1 dB and PSAT may be separated by several dB, and if you continue to increase drive, the device will continue to deliver marginally more power.

This is ideal for use in DPD linearized power amplifiers as the P_{in} versus P_{out} relationship is relatively continuous. The resulting linearity near compression is better than LDMOS and less sensitive to factors like temperature, voltage, or load that tend to move P1dB. The compression point of GaN is continuous, rounded, and in mathematical terms, it is comparatively well behaved across the upper operating region, where power and efficiency are highest. What this means in practical terms is that if the amplifier is properly matched, instantaneous power can well exceed the stated CW capability of the device, which is ideal for reproducing high PAR waveforms.

When digital correction is in place, GaN sets a new benchmark at the system level. Compared to LDMOS, the efficiency associated with a GaN lineup is between 5 percent and 7 percent higher, all other things equal. Comparisons of raw efficiency are very favourable: providing gain at 2.5 GHz, 100 W class GaN devices configured in Class AB can exceed 70 percent, while today's best LDMOS devices struggle to reach 60 percent. When properly utilized in commercial applications, the superiority in efficiency can deliver a significant impact at the system level.

At MACOM of Lowell, MA, we are enabling commercial adoption with our GaN-on-silicon technology. Now

in its fourth generation, it will enable commercial applications and markets to benefit from GaN's exceptional performance, efficiency and bandwidth at cost structures in line with LDMOS. To deliver cost savings that will accelerate the adoption of GaN in commercial applications, we are scaling the manufacture of our devices to larger wafers.

Microwave ovens ...

Another great opportunity for GaN is in providing the source of radiation for the microwave oven. There are emerging magnetron replacement prototypes that utilize LDMOS, but their efficiency falls short of what would be needed for them to be a viable alternative technology. With GaN it is a different story, because devices made from this material can bridge the 10 percent efficiency gap between the desired value and that associated with LDMOS-based modules.

Our technology is ideal for providing a replacement for the magnetron, because it combines the efficiency of GaN – at 2.45 GHz, efficiency is 70 percent – with a cost that is comparable to that of silicon. It is an attractive alternative to the tube based technology that can be traced back to the 1940s, because it enables a constant output power, zone-controllable heating and a ten-fold hike in the oven lifetime.

...and lighting

Plasma lighting offers yet another opportunity for GaN. This form of illumination involves RF power excitation, which is largely serviced with LDMOS technology. Relatively low frequencies are used, such as hundreds of megahertz. Although plasma lighting has been slow to make inroads in the overall lighting market, it has found its best niche in lighting for crop growth. When used for this, it is an ideal lighting source, thanks to a colour temperature that very closely matches that of natural sunlight.

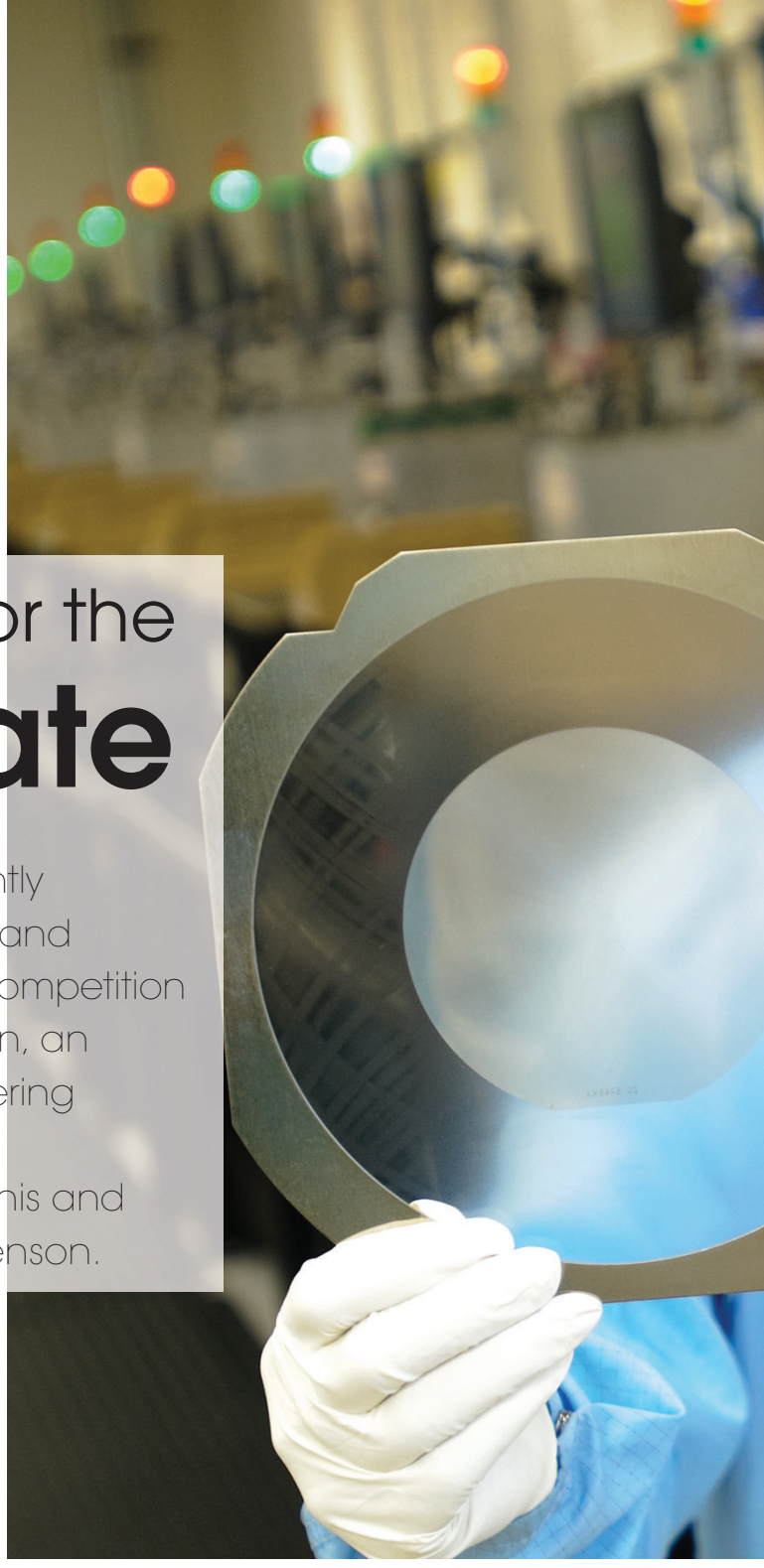
Developments in plasma lighting are now underway that will increase frequencies toward 6 GHz and efficiencies beyond 70 percent; these are specifications that are incredibly challenging for LDMOS, but a natural fit for GaN. With its higher power densities, transistor dimensions can be trimmed, making these devices a very attractive option for vendors that are driving plasma lighting as an alternative to the LED in the indoor light bulb replacement market.

GaN can also aid wireless power transmission technology. Low power, consumer grade wireless power transmission for handsets already exists, while larger scale wireless power generation and harvesting is in the prototype stage of development. With power measured in kilowatts of radiated power efficiency and stringent constraints on the dimensions of the unit – the higher the frequency of transmitted power, the smaller the physical antenna – GaN is the obvious choice for RF energy transfer applications. With devices made from this wide bandgap semiconductor, efficiency can be 10 percent higher than that for LDMOS at 2.45 GHz, an optimal frequency for antenna size.

With opportunities in plasma lighting, microwave ovens, and medical to name but a few, it is clear that GaN can serve many mainstream markets. It is an appealing option, due to the performance it delivers at high levels of efficiency. This enables an overall reduction in costs, allowing it to serve price-sensitive, high-volume applications in the commercial market.

We are firm believers in the great potential of GaN, and we are prepared to support the entire supply chain, in order to drive the adoption of this class of device. Through investments, acquisitions, and manufacturing agreements, we have positioned ourselves to scale and leverage the capabilities of GaN for widespread commercial applications at low cost for our customers.

Developments in plasma lighting are now underway that will require increased frequencies toward 6 GHz and efficiencies beyond 70 percent



A positive outlook for the SiC substrate

Sales of SiC substrates will rise significantly as shipments shift to the 6-inch format and established suppliers face increased competition from Chinese start-ups. Pierric Gueguen, an analyst from Yole Développement covering the power electronics and compound semiconductor markets, discusses all this and more in an interview with Richard Stevenson.

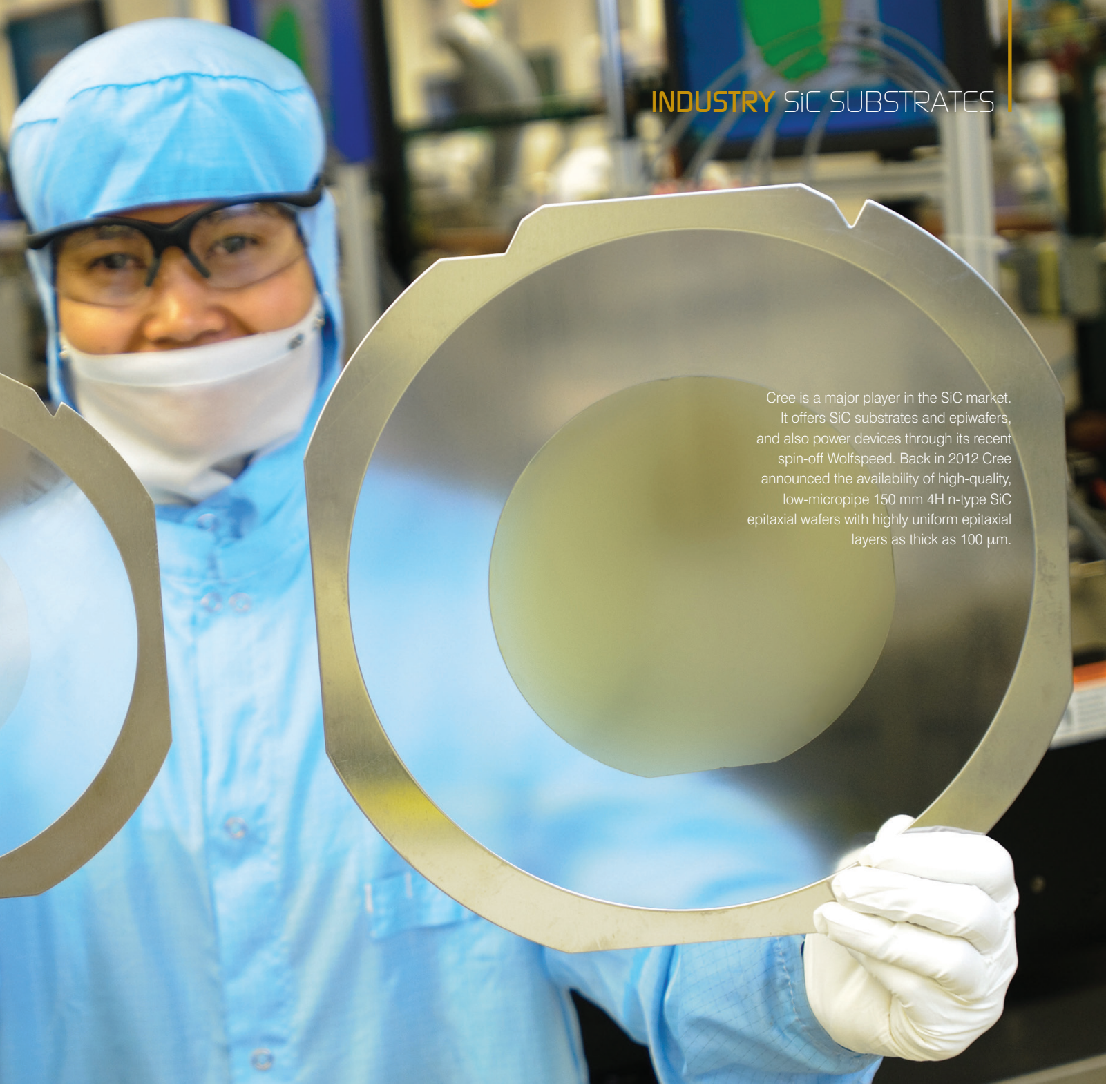
Q Over the years, there have many firms that have developed manufacturing processes for SiC substrate production. They include big names, such as Cree; starts-up that have been acquired, such as SiCrystal that is now owned by Rohm; and firms such as Caracal, which has vanished without a trace. Where does the SiC substrate industry stand today?

A In general terms, you are yet to have a strong application that drives the market. In the past we expected this market to grow at a higher growth rate [than it did], but that didn't happen. What happened is that in some cases we had some consolidation. That is the case with SiCrystal. We have some major companies today that take all the market. And these companies are supplying integrators and device makers. Some device makers want several sources, which is why if you are one of the two or three main companies, you get almost all the market.

Q Do some of the SiC substrate makers distinguish themselves from their rivals by employing a different, and arguably superior, growth technology?

A There is not that much difference in the main process today – it's sublimation. If you look at the options for crystal growth of SiC, you will see several solutions, but the mainstream is sublimation.

When you target the semi-insulating SiC substrate for RF applications, you will see some more technical aspects. Today, we have seen patents that block and lock the market for only three main players that manufacture semi-insulating substrates.



Cree is a major player in the SiC market. It offers SiC substrates and epiwafers, and also power devices through its recent spin-off Wolfspeed. Back in 2012 Cree announced the availability of high-quality, low-micropipe 150 mm 4H n-type SiC epitaxial wafers with highly uniform epitaxial layers as thick as 100 μm.

Q When it comes to price, is there much different between vendors?

A Yes, definitely. What we try to do is establish an average selling price. But today the pricing depends on two things: The volume and the business model.

In a similar situation to what happens at the device level, you have only a few big companies that have almost all the market, and they are pulling huge volumes compared to the overall market. These ones are able to negotiate, and they have access to lower costs for SiC wafers compared to other companies. And then you have really different business models, depending on whether or not the company is doing the epitaxy, and whether or not it is making its own SiC wafers. This has a huge impact on the wafer price.

Q Are the vast majority of substrates now the 4H polytype?

A Yes, definitely. SiC substrates started with the 6H polytype, but the 4H polytype is now mainstream and it will stay that way for many years.

Q Do customers still have concerns related to the quality of SiC substrates?

A Yes, mostly in power applications. Today we discuss [the issue of quality] a lot with integrators and OEMs that are willing to implement SiC wafers, and devices that are made on top of them. What happens is that they fear long-term reliability, and due to crystal quality issues, they are not able to manufacture large-current capability devices. The power devices that you have with SiC today do not have that high a current rating.

> "In the past, it was more power. But at the moment we see a strong interest in SiC in RF applications. I would say that today we are more 50-50"

Q Are the concerns over material quality related to defects, such as carrots and basal plane dislocations?

A Yes. Today the main focus is on this. There are fewer and fewer micropipes. When you are manufacturing the SiC MOSFET, you have other reliability issues, like the gate oxide.

Q What is the most popular size of substrate today, and how might this change going forward?

A The most popular today is the 4-inch wafer. We are moving slowly towards the 6-inch wafer, and this move will last two or three years. At Yole, we have seen the first prototypes of the 8-inch wafer for SiC by II-VI, earlier this year. But to us, that will remain a prototype.

Q Today, how do 4-inch and 6-inch substrates compare in quality and cost?

A In terms of cost, we have a ratio today of about 2.25. The ratio we estimate for 2020 will be around 2. When you have to pay twice the price for a 6-inch wafer, even if you have a larger area, we don't think that will really be a breakthrough technology for price reduction in the SiC market. We see this trend that 6-inch will come, mainly because [it is favoured] in terms of productivity. But we are not convinced that in terms of direct costs, it will have an important impact.

In spring 2013 Cree released its second generation of SiC MOSFET, manufactured using its SiC substrates. These devices, now made and sold by Wolfspeed, deliver half the cost-per-amp of their predecessors.

Q In terms of quality, is 6-inch inferior?

A Today it's quite inferior. Devices that are manufactured on 6-inch wafers are diodes, because it is easier to make diodes than MOSFETs on top of wafers with a lower crystal quality.

Q Cree consumes many SiC substrates for its own LED production. What is your estimate of the value of this captive market, and how does it compare to the merchant market?

A Cree has a vertically integrated LED business. We have some estimation from their LED revenue, compared to other business units. I cannot disclose that, but I can say that more than 70 percent of their markets are for LEDs. Then after, they are using their SiC wafers for power and RF, plus the merchant market, because they are also selling their SiC wafers.

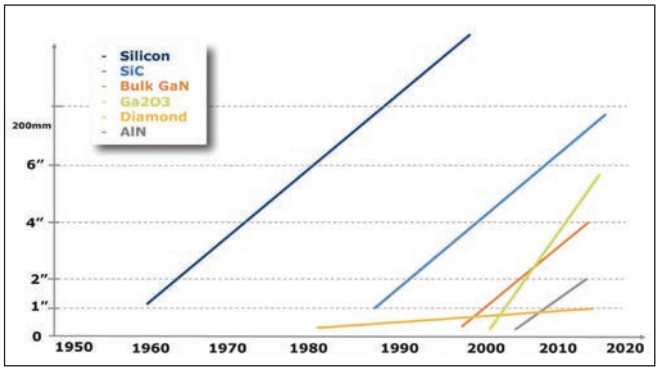
What is interesting is that even though Cree sells fewer wafers than it uses for its LED production, in the merchant market Cree is an important player. Their market share, roughly, is one-third of the market.

Q Outside of LED production, how do sales break down between substrates for power electronics and for RF electronics?

A In the past, it was more power. But at the moment we see a strong interest in SiC in RF applications. I would say that today we are more 50-50.

Q When it comes to power electronics, historically the vast majority of substrates have been used to make Schottky barrier diodes. Is that still the case, or are there now significant sales of substrates for making SiC MOSFETs?

A 80 percent of the market for SiC devices is for diodes. This share of 80 percent will roughly remain in the coming years, because the diode is really easy to implement, there are not major reliability issues, and in some applications it has already been identified as providing strong added value.



Of all the forms of wide bandgap substrate, that made from SiC is by far the most mature. (Source: SiC, GaN and other WBG materials for power electronics applications report, Yole Développement, October 2015)

Q Are sales of SiC substrates under threat from GaN-on-silicon devices?

A I don't think so. What we have done this year is that for each application we have compared the added value of SiC and GaN-on-silicon. We ended up with a pretty clear picture of where SiC will find its market and where GaN-on-silicon will find its home.

We have identified only a very few applications where you will have strong competition between SiC and GaN. We have a huge share of the GaN market that is linked to a low voltage range, while SiC has the pole position in higher voltage ranges. The boundary is around 600 V.

Q How fast will the SiC substrate market grow over the next few years?

A We have estimated an annual growth rate of 21 percent year-to-year, from now to 2020.

Q Is there much profit to be made in SiC substrate production? Or do firms need to be more vertically integrated in order to enjoy healthy margins?

A This is a tricky question. What we think is that there is added value in having internal manufacture of SiC substrates, in order to have the right process in terms of quality, and being able to monitor this.

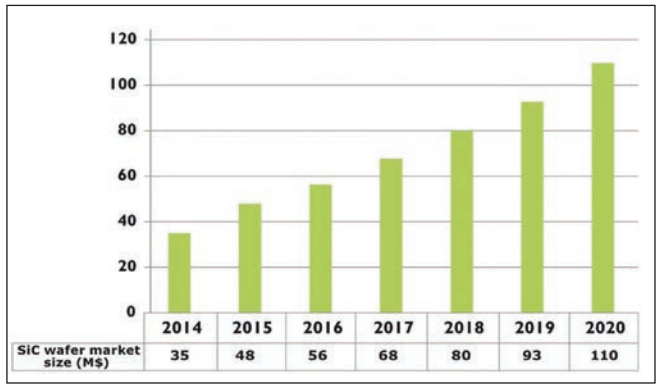
But we see Chinese SiC wafers coming on the market, and that could have an important impact on the pricing of wafers. At the moment, the status is that we have overcapacity of SiC wafers, so you have pressure on the price.

Q Given your market outlook, do you expect consolidation, expansion, or little change in the number of SiC substrate suppliers over the remainder of this decade?

A We think that you will have both. You will have small companies that will have to consolidate in order to compete with the existing big players. And the ones that are already big will continue to expand. They will be the first to benefit from market growth.

At the same time, you will have more and more Chinese companies that pop up in the market. We don't think that every single Chinese company will remain, so you will have consolidation in this area. But overall, you will have more SiC suppliers.

Also, you may have other semi-insulating SiC wafer manufacturers in the future. Today it is a closed market, because only a few suppliers can supply this type of SiC wafer.



According to Yole, the SiC wafer market will grow at a compound annual growth rate of more than 20 percent through the remainder of this decade. (Source: SiC, GaN and other WBG materials for power electronics applications report, Yole Développement, October 2015).

Pierric Gueguen is Business Unit Manager for Power Electronics and Compound Semiconductor activities at Yole Développement. He has a PhD in Micro and Nano Electronics and a master degree in Micro and Nanotechnologies for Integrated Circuits.

He worked as PhD student at CEA-Leti in the field of 3D Integration for Integrated Circuits and Advanced Packaging. He then joined Renault SAS, and worked for 4 years as technical project manager in the R&D division. During this time, he oversaw power electronic converters and integration of Wide Band Gap devices in Electric Vehicles. He is author and co-author of more than 20 technical papers and 15 patents.

LED DROOP

Physics beyond the common model

Optical spectroscopy exposes fundamental flaws in the well-known model for LED droop

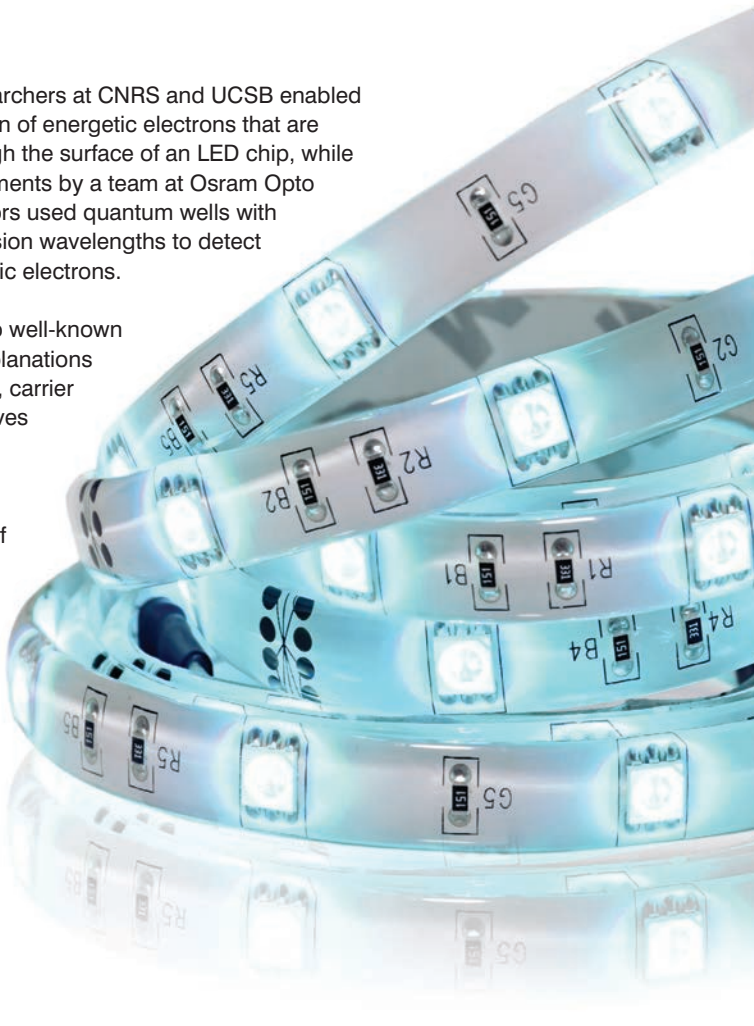
BY ANDREAS HANGLEITER AND TORSTEN LANGER FROM THE TECHNISCHE UNIVERSITÄT BRAUNSCHWEIG, GERMANY

THE LED is a flawed gem. On the plus side, it has a very long lifetime, an ability to reach full power in an instant and an efficiency exceeding that of conventional lighting sources. But on the downside its weaknesses include: a price that, while falling, is still too high for widespread adoption of solid-state lighting; and an output, in the case of the III-nitride devices that emit in the blue, green and white, that is severely limited by efficiency droop.

This malady, which is associated with a decline in efficiency at higher current densities, has been at the centre of a sometimes-fierce debate concerning the origin of droop, and possible remedies for it. Leading explanations for its cause include Auger recombination, carrier leakage, and density-activated defect-recombination.

Of these three, the mechanism receiving the greatest support is Auger recombination. This is a three-particle non-radiative process, where an electron and a hole recombine, transferring their energy to a third particle (an electron or a hole) as kinetic energy. It is established that Auger recombination takes place in III-nitride LEDs, because highly energetic particles have been observed in these devices. Collaboration between researchers at CNRS and UCSB enabled the observation of energetic electrons that are emitted through the surface of an LED chip, while optical experiments by a team at Osram Opto Semiconductors used quantum wells with different emission wavelengths to detect highly energetic electrons.

One of the two well-known alternative explanations for LED droop, carrier leakage, involves an increasing proportion of electrons lost to the *p*-side of the device at higher current densities. Despite the presence of an electron-blocking layer, it is argued that some of the electrons



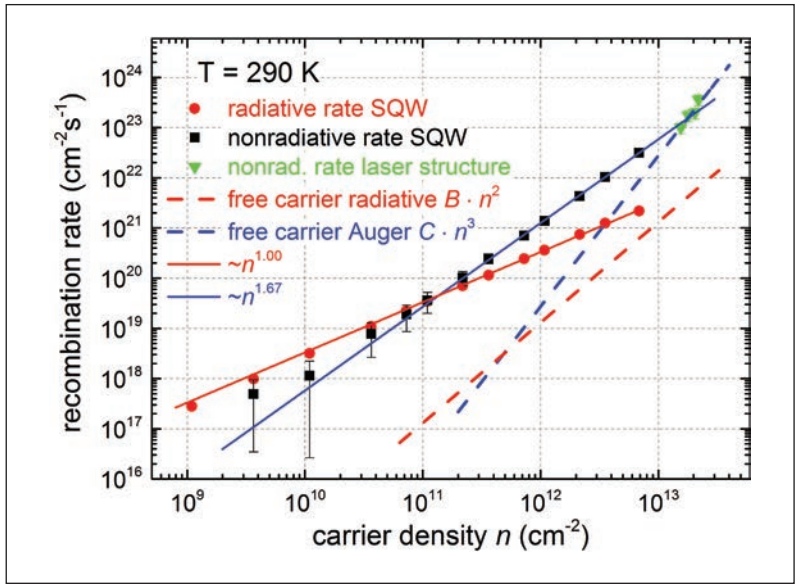


Figure 1: Comparison of experimental values (full symbols) for the radiative (red) and non-radiative (blue) recombination rates versus carrier density in GaInN/GaN quantum wells with the *ABC* model (dashed lines). At the highest densities, an Auger-like behaviour of the non-radiative rate is observed. At lower carrier densities, both radiative and non-radiative lifetimes behave non-classically, i.e. exhibit slopes of 1.0 and 1.67, contradicting the *ABC* model.

injected from the *n*-side of the *p*-*n* junction will spill over the active region and recombine with holes in the *p*-region, or even reach the *p*-contact. Several groups have reported evidence suggesting that carrier leakage may play a role in LED droop.

The third common conjecture for droop, density-activated defect recombination, is based on the idea that there is an energy barrier preventing carriers from reaching non-radiative defects. According to the model, this barrier decreases at higher carrier densities – and this enables the rate of defect recombination to increase superlinearly with carrier density.

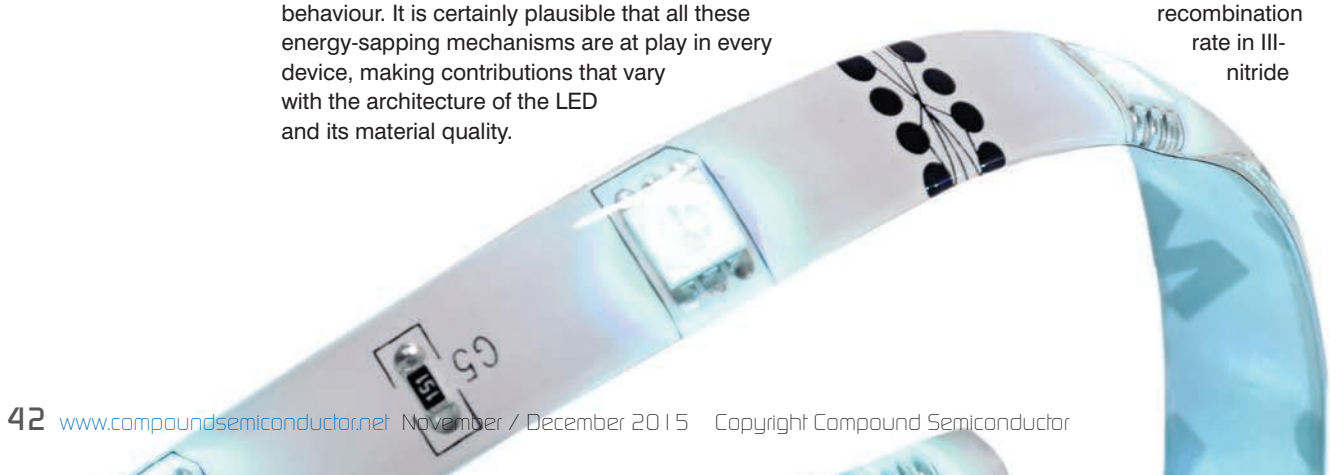
There is no reason to believe that droop must be a result of just one of these mechanisms, and the other theories have no role to play in device behaviour. It is certainly plausible that all these energy-sapping mechanisms are at play in every device, making contributions that vary with the architecture of the LED and its material quality.

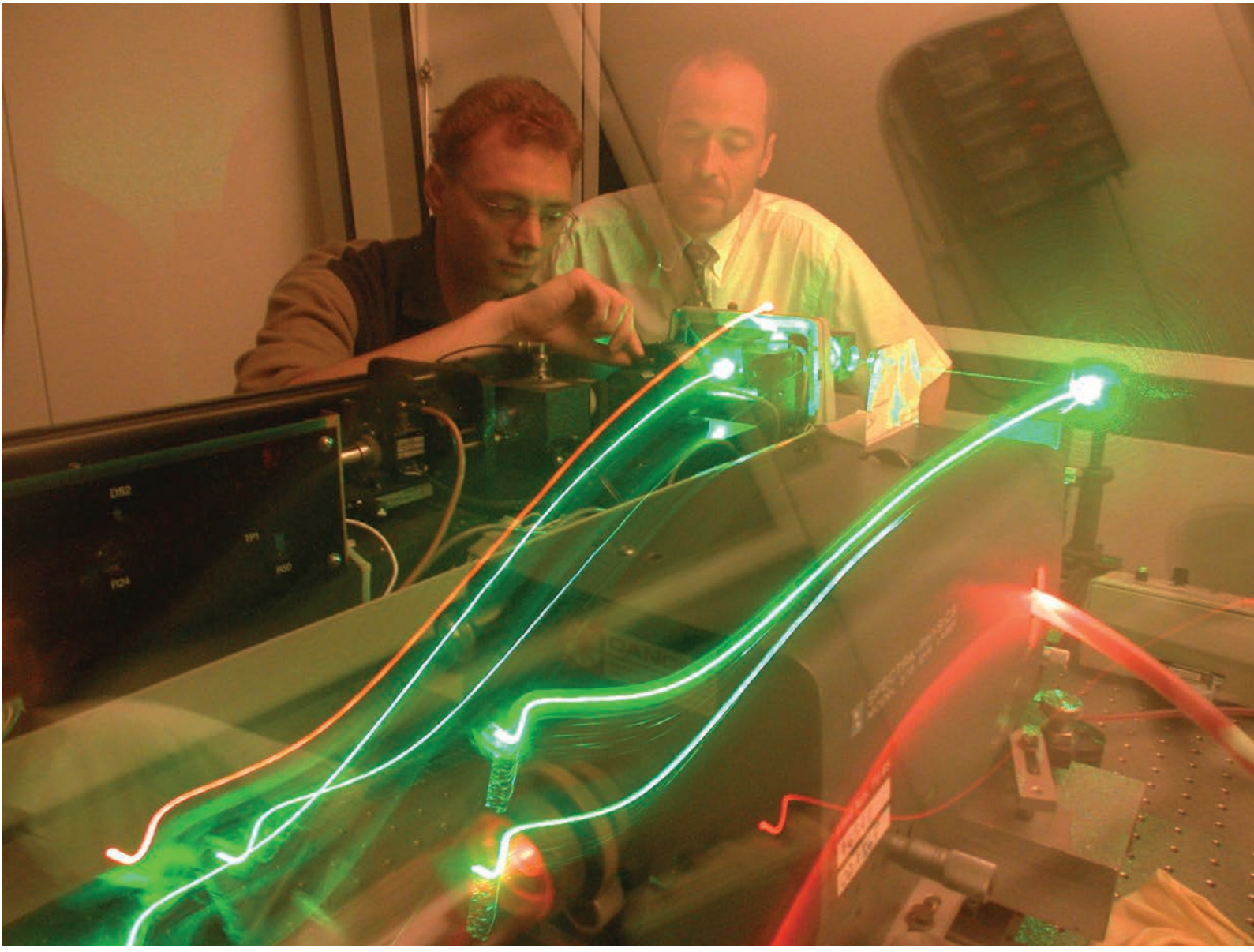
To analyse the dependence of efficiency on current density, many researchers investigating droop are using the so-called *ABC* model. This describes the recombination rate in a semiconductor with a combination of: a linear term in carrier density for Shockley-Read-Hall (defect) recombination, a quadratic term in carrier density for the radiative band-to-band recombination, and a cubic term in carrier density for band-to-band Auger recombination. The linear, quadratic and cubic terms have *A*, *B* and *C* coefficients, respectively, accounting for the name *The ABC Model*. It is based on a single-particle picture applied to a non-degenerate semiconductor, and it has been verified for a range of semiconductors with narrow to moderate bandgaps.

One of the downsides associated with using the *ABC* model to evaluate the LED is that it is not possible to directly measure the carrier density from either the quantum efficiency or the current density. Both of these quantities are functions of the recombination rates, such as of the sum of the *A*, *B* and *C* terms. This is a major drawback, because it means that measurements of LED efficiency as a function of current – the plots that are needed to gauge the extent of droop – are unable to determine the validity of applying the *ABC* model to the device.

The good news, however, is that it is possible to determine the relationships between carrier density and radiative and non-radiative recombination rates independently of each other with optical techniques. This is the approach that our team has pursued at Braunschweig University of Technology, where we have employed time-resolved optical spectroscopy to analyse recombination mechanisms [1]. This effort has involved using ultrashort laser pulses with variable pulse energy to resonantly excite InGaN quantum wells. The carrier density created by these pulses is directly proportional to the pulse energy, with the decay of the luminescence directly revealing the carrier lifetime at that given carrier density.

These experiments expose two fundamental flaws in the *ABC* model. One is that the radiative recombination rate in III-nitride





quantum wells is not proportional to the square of the carrier density, as assumed in the *ABC* model: Instead, it depends linearly on carrier density. The second flaw is related to the non-radiative recombination rates at high carrier densities. They vary approximately quadratically with carrier density, rather than showing the cubic dependence that is expected for non-radiative Auger recombination rates in the classical picture.

Although these findings will surprise some of those investigating droop, they should not be that shocking. That's because as far back as the 1990s, deviations from the *ABC* model were observed in 'good old' silicon. There, the Auger recombination rate at moderate carrier densities varies in a quadratic rather than cubic fashion [2,3]. Note that despite its indirect bandgap, Auger recombination is an important phenomenon in silicon – it is a major limiting factor on the quantum efficiency of solar cells made from this material [3].

The reason why the *ABC* model fails to capture the relationships between both radiative and non-radiative recombination and carrier density is that it does not consider the attractive Coulomb interaction between electrons and holes in the semiconductor.

This interaction leads to the formation of a mobile bound state, like a hydrogen atom, that is known as a free exciton. When an electron and a hole are confined within an exciton, their spatial overlap increases significantly, and this leads to an enhanced radiative (and non-radiative)

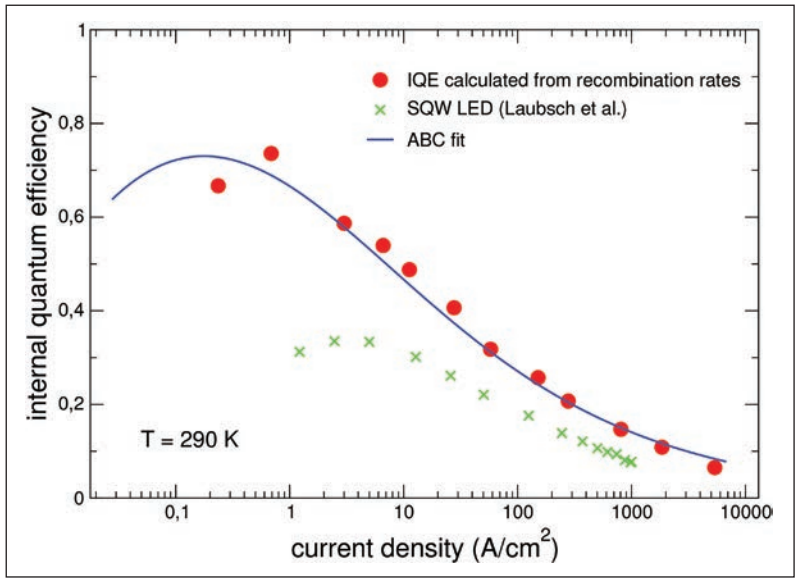


Figure 2: Calculated values of internal quantum efficiency as a function of current density, based on measured radiative and non-radiative recombination rates (full circles). The data are well fitted by the *ABC* model (full lines), even though the original dependence of the recombination rates contradicts the *ABC* model. For comparison, a typical LED droop curve (Laubsch *et al.* IEEE ED-57 79 (2010)) is shown (crosses), demonstrating very similar behaviour.

recombination probability. Due to this mechanism, the recombination rate depends on the density of excitons, which is governed by the carrier density. A quantitative description of the radiative and non-radiative processes in semiconductor materials can be realised by modifying the *ABC* model with so-called excitonic enhancement factors that represent the density-dependent increase of the recombination probabilities [2,4]. In this more realistic model, excitonic enhancement factors are calculated from a many-particle theory that accounts for free-carrier screening of the Coulomb interaction and phase-space blocking.

The effect of excitonic enhancement on Auger recombination is even highly significant in silicon, a material with a bandgap below that of LEDs. In this material, the exciton binding energy is around 15 meV, about one half of the thermal energy at room temperature. In wide-gap III-nitride-based quantum wells, as used in blue LEDs, excitonic enhancement is far stronger, due to an exciton binding energy that can be as large as 50 meV, which is about twice the thermal energy. In this III-N, one would expect the effect of excitonic enhancement to be far greater – and it is, according to the strong deviations from the *ABC* model.

Do these considerations reveal anything about the cause of the droop? Absolutely. By taking data for the radiative and non-radiative recombination rates obtained from our optical experiments, we can calculate the efficiency of an LED at different current densities, generating a plot that shows a typical droop curve for this device (see Figure 2).

Note that even though our carrier-density-dependence of the recombination rates is quite different from that prescribed in the *ABC* model, our efficiency curve at differing current densities is indistinguishable from a real LED, demonstrating the ambiguity of typical droop analysis [5].

A further important conclusion from our studies is that an efficiency droop can be observed even under selective optical excitation, where carrier leakage does not occur. Consequently, this observed droop is merely related to recombination processes. Our measured non-radiative recombination lifetimes at high carrier densities are sample-independent and depend only weakly on temperature, but decrease towards high densities. This implies that an intrinsic (i.e. not related to crystal defects) non-radiative recombination process like Auger recombination must be dominant.

When we take into account the excitonic enhancement of Auger recombination, it follows that the recombination rate for this process varies like the square of the carrier density, rather than showing a cubic dependence. Consequently, Auger recombination constitutes at least the intrinsic limit of the droop phenomenon.

Our studies reveal that the widely used *ABC* model has major flaws that hamper studies of efficiency droop in III-nitride LEDs. To really understand the physics of droop, it is essential to account for the excitonic enhancement of both radiative and non-radiative recombination processes. Take this approach, and the dominant culprit for droop is unveiled as an intrinsic one: excitonic Auger recombination.

Further reading

Cited references

1. T. Langer *et. al.* Appl. Phys. Lett. **103** 202106 (2013)
2. A. Hangleiter *et. al.* Phys. Rev. Lett. **65** 215 (1990)
3. A. Richter *et. al.* Phys. Rev. B **86** 165202 (2012)
4. A. Hangleiter Phys. Rev. B. **48** 9146 (1993)
5. A. Hangleiter *et. al.* Proc. SPIE **9363** Gallium Nitride Materials and Devices X, 93631R (2015)

Optional references

J. Iveland *et. al.* Phys. Rev. Lett. **110** 177406 (2013)
M. Binder *et. al.* Appl. Phys. Lett. **103** 071108 (2013)

Book your place at the

CS International Conference

Tuesday 1st & Wednesday 2nd March 2016

Limited availability

The compound semiconductor industry is developing and manufacturing new devices that will help to shape the world of tomorrow.

This industry is currently debating a handful of key questions: -

- What challenges will GaAs and CMOS power amplifiers face in making the transition from 4G to 5G? And will faster data links play into the hands of GaN-based amplifiers for base stations?
- Is SiC set to displace silicon in electric cars? And how will this material help to revolutionise the efficiency and operation of electrical grids?
- Can LED bulbs meet the most demanding lighting applications, such as those found in the retail sector? And what are the opportunities for infrared and ultra-violet LEDs?
- III-V channels are poised to make an introduction in next-generation logic circuits. But how will they be introduced, and what impact will they have?
- What is needed to kick-start significant deployment of concentrating photovoltaic technology? And what are the opportunities for III-V detectors operating in the infrared?

To know what the leading industry insiders are thinking about these important issues, make sure you attend CS International.

Book your place NOW!

Sheraton Brussels Airport Hotel, Belgium

Register: www.cs-international.net

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

PIC International Conference
SPEAKERS ANNOUNCED!

PIC International 2016 will provide timely, comprehensive coverage of every important sector within the Photonics Integrated Circuits industry.

PIC International Conference is being launched to strengthen the relationships between the makers and the users of Photonics Integrated Circuits.

PIC International will be held and co-located with the highly successful 6th CS International conference at the Sheraton Brussels Airport Hotel, Belgium on Tuesday 1 & Wednesday 2 March 2016.

Attendees at PIC International will hear industry-leading insiders delivering more than 30 presentations spanning six key themes which collectively provide complete coverage of the Photonic Integrated Circuits industry and offer many opportunities to meet many other key players within this community.

Book your place now at: www.picinternational.net/register

Platinum Sponsors

EAG Evans Analytical Group · EVG · LUCEDA PHOTONICS · VLC PHOTONICS · VPIphotonics DESIGN AUTOMATION · YOLE Développement

Supported by

EPIC European Photonics Industry Consortium

Gold Sponsor

IQE · Yenista OPTICS

Lanyard Sponsor

IQE

This two day event covers six themes

Conference Chair:
Michael Lebby – Chair in Optoelectronics - Glyndŵr University
Board Director, Lightwave Logic

Where Should the Laser go?

Is heterogeneous integration the best option for lighting up the IC? Or is it better to couple the laser's emission onto the chip?

- **William Ring – BB Photonics**
  High speed photonic integrated receivers for 100G and above
- **Gregory Fish - Aurrion**
  Heterogeneous integration: creating photonic circuits for advanced systems-in-package
- **Shinji Matsuo – NTT Photonics Lab**
  Excelling in the efficiency of lasers formed on silicon
- **Fang Wu – ArtIC Photonics**
  How far does monolithic integration go?
- **Hamid Arabzadeh – Ranovus**
  Turning to quantum dot lasers for terabit communication?

Driving deployment of PICs in datacentres

PICs are a solution to the rocketing demands facing datacentres. But what do they need to deliver, and how can they be put to best use?

- **Brad Booth – Microsoft**
  Lighting up the Cloud
- **Arlon Martin – Mellanox Technologies**
  Using Silicon Photonics to support next-generation cloud computing, data centre and high performance computing connectivity
- **Di Liang – HP**
  Constructing very large scale PICs for data centres
- **Jason Orcutt – IBM**
  Towards cost-effective 100 Gb/s optical transceivers
- **Craig Thompson – Finisar**
  Creating the building blocks for better datacentres
- **Katharine Schmidtke – Facebook**
  What components do we need to build the datacentres of tomorrow?

Increasing the capability of optical networks

Are PICs about to dominate the landscape of optical networks? And is there room for different forms of device?

- **Silvio Abrate - ISMB**
  How can silicon photonics benefit optical access deployment? An example from the FABULOUS EU Project
- **David Plant – McGill University**
  Photonic circuits enabling multi-dimensional IM/DD systems for short reach optical interconnects
- **Harald Bock – Coriant**
  Silicon photonics in optical networking – yesterday's hype, today's reality, tomorrow's vision.

What's the role of the foundry?

Can companies afford to make PICs in-house? And if they do outsource, what should they look for from a foundry?

- **René Heideman – LioniX**
  LioniX: Aid the growth of photonics with the TriPleX integrated optics platform
- **Katarzyna Ławniczuk - JePPIX**
  Accelerating photonic ASICs development
- **Samuel Wang – Global Communication Semiconductors**
  Can foundries underpin the success of the PIC?
- **Luc Augustin – Smart Photonics**
  Enabling a broad range of applications with a generic integration platform on InP
- **Philippe Absil – IMEC**
  Imec's flexible, state-of-the-art silicon photonics platform overview

Do we have the tools for designing, making, packaging and testing PICs?

The silicon CMOS industry sets a benchmark for chipmaking. How can the PICs industry catch up?

- **Sean Anderson – CISCO**
  Bringing first-time-right design to silicon photonics
- **Stefano Grillanda – Politecnico di Milano**
  Taking a close, damage-free look at the light in photonic integrated circuits
- **Twan Korthorst – PhoeniX Software**
  Overview of the current status of photonic and electronic design tools and flows
- **Pieter Dumon – Luceda Photonics**
  Make photonic IC designers re-use 40 years of electronic IC design experience: challenges and opportunities
- **André Richter – VPI Photonics**
  From circuit-level to mask layout and back – design, analysis and optimization of large-scale PICs
- **Iñigo Artundo – VLC Photonics**
  Outsourcing options and trends for the fabless development of PICs

A question of material: InP, silicon or something else?

InP is fragile and expensive, but a great material for integrating all the components on one chip. Silicon can't do this, but is a larger, more mature platform. So is it the case of selecting the right material for the particular application, or can there be a universal, long-term winner?

- **Thomas Collins – Huawei**
  Surveying silicon photonics technologies: Identifying strengths and weaknesses and likely future trends
- **Meint Smit – TU Eindhoven**
  InP and silicon: a strong combination for integration of photonics and electronics
- **Ronald Broeke – Bright Photonics**
  Selecting materials for PIC production
- **Vincent Reboud – CEA-Leti**
  A bright future for germanium-on-insulator wafers?
- **Martijn Heck – Aarhus University**
  Hybrid and heterogeneous PICs for high performance applications
- **Martin Guy – TeraXion**
  InP or silicon photonics or both? Choosing the right material platform for the target application
- **Martin Eibelhuber – EVG**
  Advanced wafer bonding techniques for photonic integration

Multiple materials enhance front-ends

The front-ends of smartphones should not be served by a single material. Instead, to ensure sufficient performance, they should combine a GaAs-based power amplifier with a silicon-on-insulator switch and filters made from piezolelectrics

BY JAMES YOUNG FROM SKYWORKS

MANY OF US feel lost without our mobile phone. In one form or another, we have been taking them with us on a daily basis for many years, and as time has gone on, we are probably using them more than ever. In the past, we made calls and sent texts, but now these portable devices are also used for listening to music, surfing the web, and watching videos.

To improve the experience of the user, every generation of mobile phone operates at a higher data rate than its predecessor. Due to this advancement, network data is growing at an exponential rate. What's more, there is an every-increasing complexity in the handset's RF front-end. It is packed with filters, switches and power amplifiers that are meeting more demanding specifications than ever before.

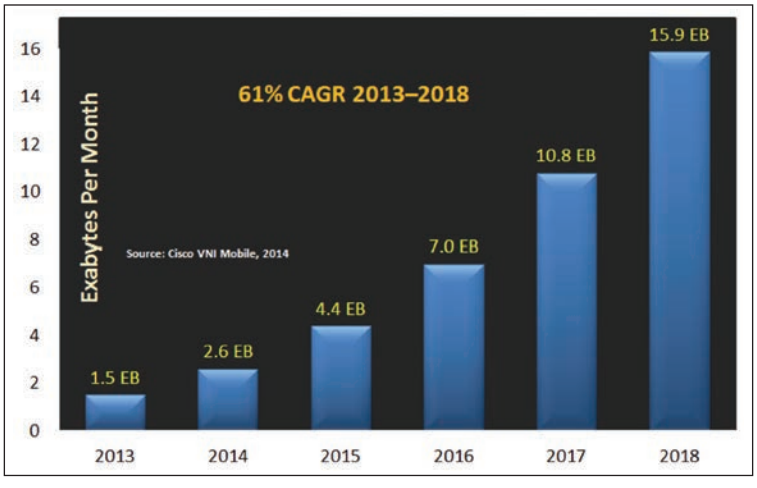


Figure 1. Throughout this decade, mobile data traffic is increasing at an exponential rate.

Another major change in the design of the RF front-end is the shift from discrete components to highly integrated products. This evolution has made life easier for the makers of handsets, but more challenging for their suppliers that are faced with designing more complex products. Two distinct approaches have been adopted – the system-on-chip and the system-in-package – and both can feature compound semiconductor and silicon content. In the remainder of this article we will evaluate all these technologies, before considering the make-up of a state-of-the-art front-end module that combines affordability with great performance and a small footprint.

One of the essential requirements for an RF front-end is that it can cope with the exponential growth in data that has underpinned the expansion of new standards and bands (see Figures 1 and 2). The introduction of 4G has provided a ten-fold increase in the mobile handset data rate, but if no new bands were added to the network, this additional capacity would be consumed in just three-to-five years. To address this, high-end smartphones are now being packed with

Figure 2. Introducing new mobile standards and bands enablesan increase in data rates.

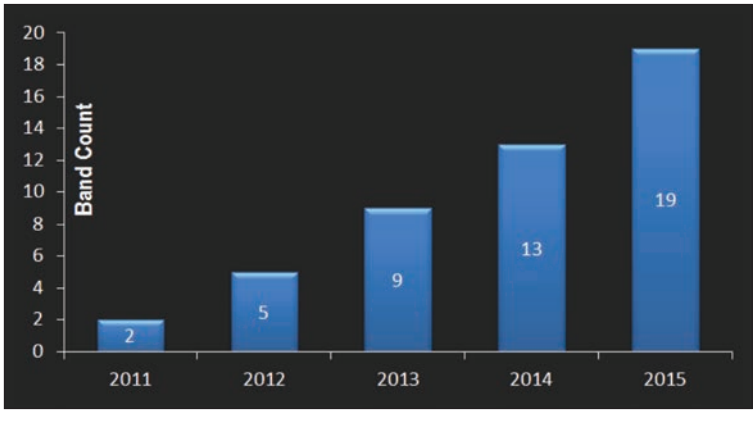
	2012	2014	2016E	2020E
LTE Rel	LTE Rel-11	LTE Rel-12	LTE Rel-X	5G
# CA Bands	2	3	3	5
MIMO	8x8	8x8	8x8	64X8
Proposed New Bands		5+	24	50
CA Band Combos	25	75+	172	300
Peak/Max DL	1.2Gbps	3Gbps	6Gbps	18Gbps

more and more bands (see Figure 3). Changes such as this increase the complexity of the RF front-end, and products with high levels of integration, are needed to overcome issues related to efficiency, size, cost and time-to-market.

Examples of the complexity of the modern RF front-end include the need to support 13 to 24 4G bands and be capable of handling carrier aggregation (see Figure 4 for a front end block diagram). These requirements must be met with a product offering high efficiency, to ensure a long battery life for the smartphone.

To extend the battery life the phone must be efficient at converting the battery energy to RF energy transmitted out of the antenna. Any loss of energy in the PA and after the PA will reduce the battery life. Dominating losses are those occurring at: the duplexer/filter; the PA transistor; and the passive components, including the matching networks and the carrier aggregation functions (see Figure 5). We will now assess all of these areas in turn, in an effort to highlight the best technologies for delivering great performance from a small, low-cost product.

Figure 3. To improve the rate of data transfer to a smartphone, the number of 3G/4G bands that it incorporates is increasing.



Superior switches

Key characteristics for judging the quality of the switch are its insertion loss, level of isolation, linearity, cost and size. When designing this component, it is essential to consider the standing-wave RF voltage across the switch when it is delivering its maximum output power. In extreme cases, which can occur when there is a high mismatch-impedance at the antenna, the voltage across the switch can peak at just over 70 V. This is enough to damage a single transistor. High levels of voltage across a transistor can also generate harmonic levels that lead to unacceptable performance.

To overcome these limitations, multiple devices are stacked in series. This approach splits the voltage across multiple transistors. For example, when transistors are made with a 0.18 μm MOSFET SOI process, between 8 and 12 devices typically form a switch. This can be reduced to roughly three devices by using a dual-gate PHEMT, thanks to its higher breakdown voltage.

Once the transistor technology and stack has been chosen, an engineer must select the width of each FET, a decision that determines the off capacitance and the off RF isolation. The isolation must be between 25 dB and 30 dB to ensure that the off arms do not disturb the performance of the on arm.

The width of the FET also dictates the on-resistance of the switch, and this in turn governs the RF insertion loss. A comparison of different technologies for a nine-throw antenna switch shows that MEMS provides the lowest insertion loss (see Figure 6). However, the silicon-on-insulator devices with a slightly higher insertion loss (they are still superior to those based on GaAs PHEMTs) are used because they provide the highest level of integration at a low cost.

Fantastic filters

An ideal filter would reject all frequencies outside a particular band, while passing those within it with minimal loss. In practice, this is not possible – a typical passband response for a duplexer is shown in

Figure 7. Note that decreasing the spacing between the transmit passband and the receive passband enables more efficient use of the frequency spectrum, but requires more resonators to achieve the out-of-band attenuation. Doing this has a downside, as it leads to a rise in insertion loss. Note that the typical requirements for a high-performance duplexer are a transmitter isolation in the receive passband in excess of 55 dB, and an insertion loss in the transmitter and receive passbands of less than 2 dB.

Comparing the different approaches to making filters shows that devices based on surface acoustic wave (SAW) technologies are needed to meet the requirement for an insertion loss of less than 2 dB (see Figure 8). Although this is by no means the lowest cost approach, it is implemented, because filters are a significant contributor to the overall front-end energy loss between the power amplifier output and the antenna.

Filters configured as a diplexer, triplexer or quadplexer are also used to connect multiple bands at one time to the antenna. This is done to support carrier aggregation, which allows two or three bands to simultaneously operate over a common antenna.

This approach is illustrated in Figure 4, which shows mid- and low frequencies combined through a diplexer, and high-band frequencies operating via a separate antenna. It is a design that allows three bands to be active at one time, and when the diplexer is formed with a printed circuit board or a low-temperature, co-fired ceramic technology, insertion loss is around 0.4 dB.

The downside of using two antenna is that it consumes more space – so designers may prefer to triplex the three bands and reduce the number of antennas to one. But with a single antenna, the mid- and high bands are very close together, causing a high loss at the diplexer or triplexer. If this were made with a low-cost, printed circuit board, lumped element or low-temperature co-fired ceramic technology, the typical insertion loss would be 1.5 dB. That's considerable, as offsetting this loss would require an increase in the output of the power amplifier by 1.5 dB – and that equates to a 40 percent hike in the current consumed by this amplifier. That is a high price to pay for a single antenna design, and explain why many handsets incorporate multiple antenna.

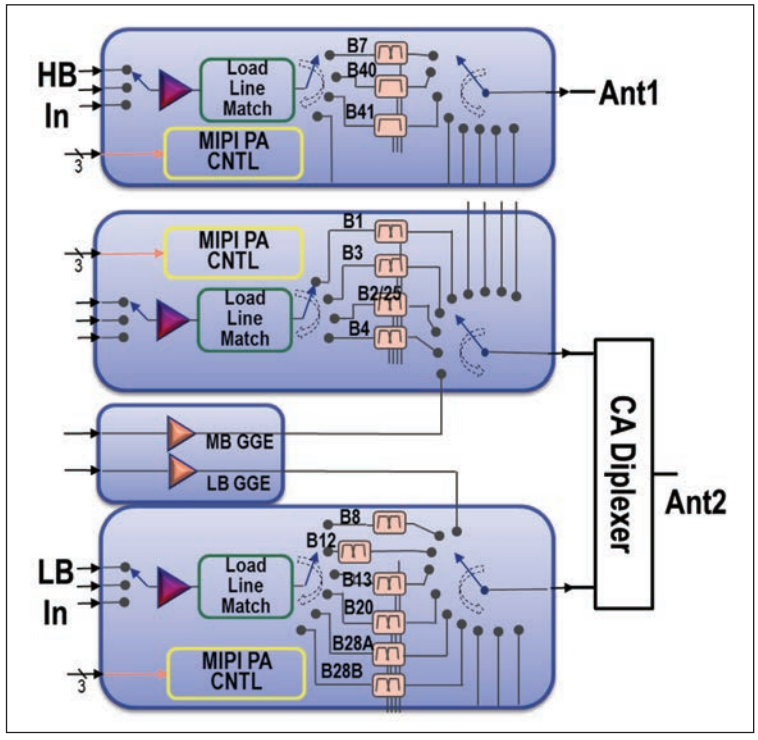
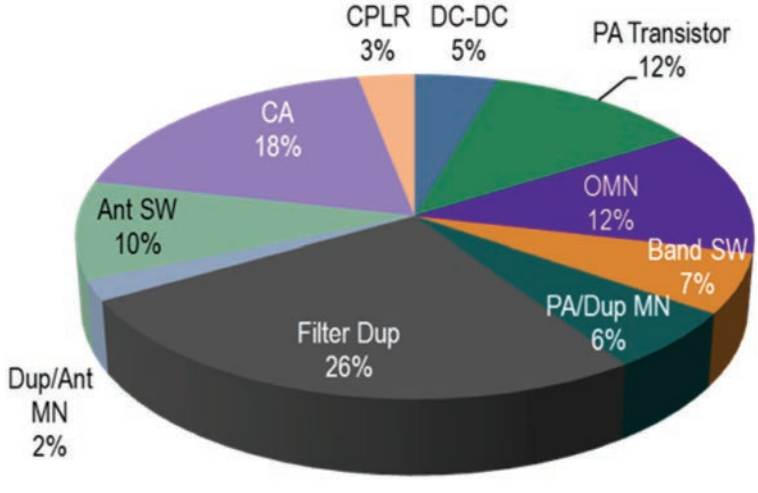


Figure 4. A typical mobile front-end block diagram, which has been taken from Skyworks 'SkyOne' products. Note that this particular configuration allows the user to combine the high, mid- and low bands external to the package as the user desires.

Attractive amplifiers

The key attributes for a successful power amplifier are a high power-added efficiency, small size and low cost – and excellence in these areas must be accomplished while maintaining other system specifications. To optimise amplifier efficiency, engineers must carefully select the class of operation, load line impedance, transistor size, and bias. Another decision for engineers of front-end systems is to choose between one of two control systems for



Right: Figure 5. A breakdown of the causes of efficiency lost during converting DC to antenna RF. Note that the passive components include the matching networks (MN) and the carrier aggregation (CA) function.

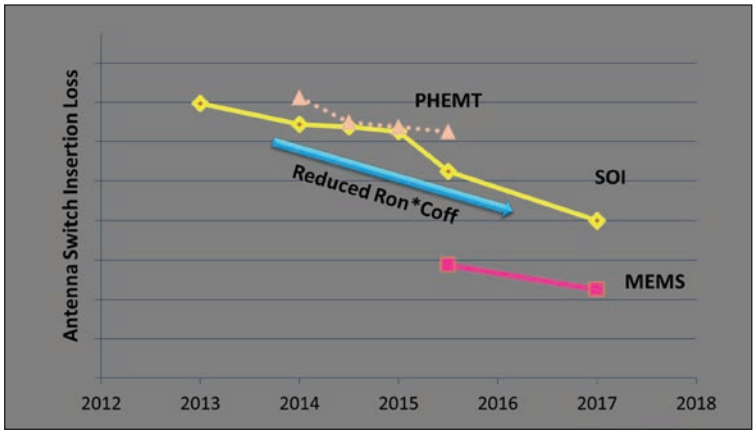


Figure 6. For a nine-throw antenna switch, MEMS technology offers the lowest insertion loss. However, silicon-on-insulator (SOI) technology has an acceptable insertion loss and is significantly cheaper, so this dominates the market today.

improving the efficiency of the amplifier: average-power tracking, which operates the amplifier in its linear region; and envelope tracking, which operates the amplifier in gain compression or in saturation.

With the former approach, where the amplifier is run in a linear regime, the saturated output power is set high enough to pass the peaks of the waveform with minimal distortion. As the peak-to-average power increases, the average power is set further below the maximum saturated output power of the amplifier. The difference between the average power and the saturated power is referred to as the 'back-off' power. At higher data rates, the peak-to-average waveform is higher, so the back-off power is higher, reducing the efficiency of the amplifier.

The common alternative to this, envelope tracking, is centred on two fundamental concepts: that the amplifier's maximum saturated output power is proportional to the supply voltage; and that the power-added efficiency of the amplifier is highest when it is saturated. So, for an amplifier operated with envelope tracking, the load line is calculated and fixed, based on the maximum peak output power to be transmitted at the maximum rated supply voltage. Once the value for the load line has been set, the saturated output power is varied by changing the supply voltage, so that it tracks the envelope of the signal.

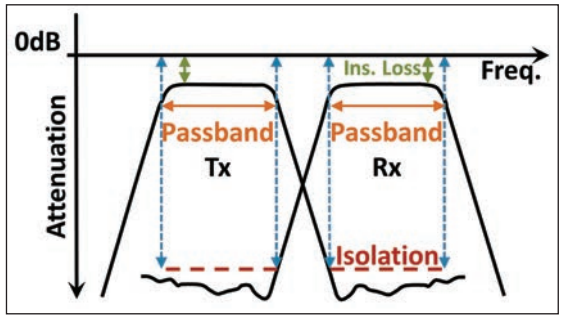


Figure 7. A typical passband response for a duplexer.

It should be noted that with an envelope tracking system, the minimum voltage that can be applied to the drain or collector of the transistor limits the range of power that can be tracked. The minimum voltage is typically around 1 V, and below this the gain of the transistor drops to unacceptable levels. Due to this, the range of the RF envelope output power that the envelope tracking system can track tends to be around 12 dB, and this limits the average output power tracking to the top 6 dB to 10 dB of output power. Fall below this range and the efficiency of the envelope tracking system drops, shifting the amplifier's mode of operation to average-power tracking in a linear regime.

Another decision that an engineer must consider is the class of operation for the amplifier. Amongst the many options, a class F load is popular, because it produces a higher efficiency at a given linearity.

To realise class F operation, the collector voltage and current waveforms are shaped with harmonic traps or resonators in the output network. This modifies the voltage waveform to approximately a square wave, and the current waveform to approximately a half-sine wave. Realising this involves presenting a short to the collector at even harmonics, and an open at odd harmonics.

The efficiency of an ideal class-F power amplifier increases with the number of harmonic terminations. Producing a high-efficiency output network might appear taxing, but in practice only the first few harmonics need to be correct. When size and cost considerations are taken into account, optimal termination of just the second and third harmonics tends to suffice.

Envelope-tracking amplifiers have been operated in both Class F and Class E. Higher efficiencies are possible with Class E, because with a simple output network, the collector waveforms are properly shaped. However, when the system drops back to average-power tracking, class F provides superior linearity.

GaAs or silicon?

One debate that is going on within the amplifier sector is whether the incumbent technology, the GaAs HBT that holds over 95 percent of the market, will lose market share to devices based on CMOS and silicon-on-insulator technologies.

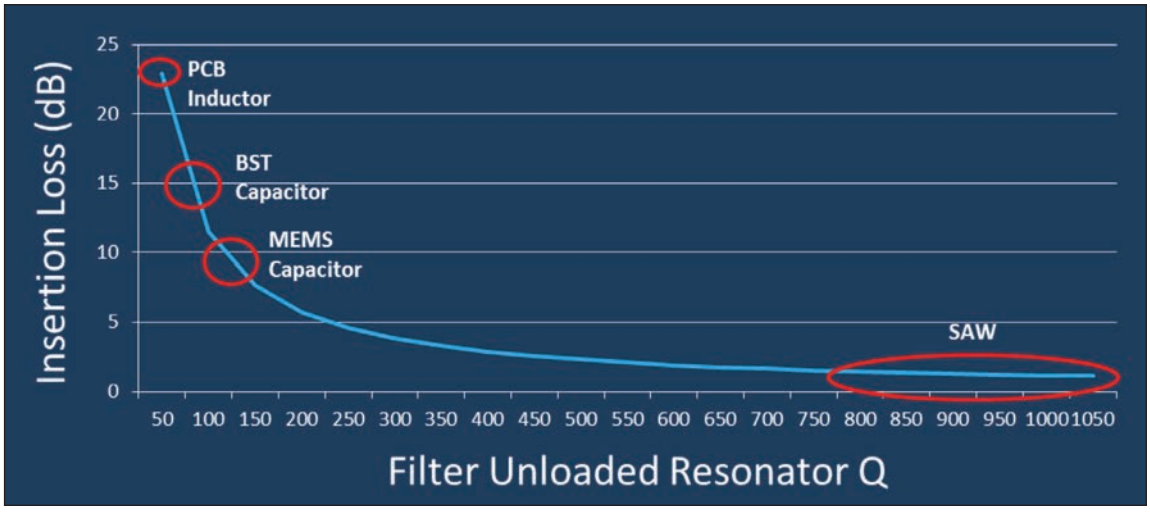


Figure 8. The higher the quality factor (Q), the lower the insertion loss for a band 2 transmitter filter designed to maintaining the specified receiver band isolation. It is clear that discrete filter implementations with inductors implemented in printed circuit board, low-temperature co-fired ceramic or chip form with quality factors around 40-50 would have far too high an insertion loss. Also noted are tunable technologies. But their quality factor is also too low. In order to have an insertion loss of less than 2 dB, a high quality factor realised with a SAW or FBAR process is required.

Comparing the strengths of these competing technologies is straightforward once we have established the power-added efficiency operating points for average-power tracking and envelope tracking. Plots of power-added efficiency as a function of output power can highlight the differences in efficiency between the different material technologies and the different modes of operation.

One such plot is shown in Figure 9, which is for a two-stage power amplifier operating with a range of supply voltages. The collector voltage, which is essentially the same as the drain voltage for a FET, is modulated to vary the saturated output power. Different supply voltages produce different curves. For comparison, the maximum drain or collector voltage used in this example is 3.5 V which is the mobile phone battery voltage. This implies that the saturated output power at 3.5 V will be equal to the amplifier's maximum peak output power.

Based on these assumptions and findings, it is possible to consider the operating conditions for different forms of data transmission. For a WCDMA voice waveform with a 3.5 dB peak-to-average power ratio, the average operating point will be around 3.5 dB below Point A (this is labelled in Figure 9 as the 'Voice Mode ET' operating point). It can be seen from the graph that the average envelope-tracking voice operating point at the maximum output power would have about a 4 percent power-added efficiency below point A, and have an average modulated collector voltage of about 2.3 V.

When the mode of operation is average-power tracking, the collector voltage must remain at 3.5 V to support the WCDMA voice waveform peaks. However, the average operating point of the amplifier will follow the black dotted line in Figure 9, which is labelled 'Linear PA' and is 21 percent below point A. This highlights the inferiority of average-power tracking – for voice mode, the power-added efficiency is 17 percent lower than that for envelope tracking. The data shown in Figure 9 is based on

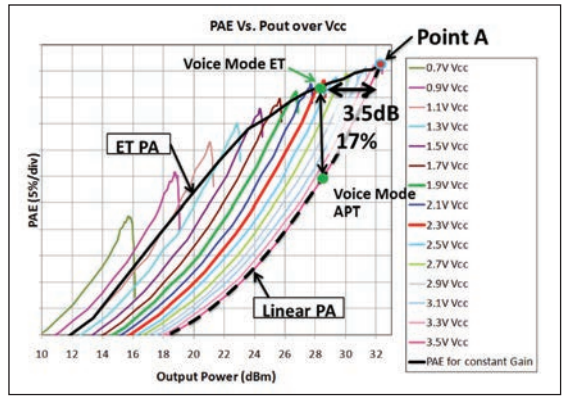


Figure 9. Envelope tracking (ET) enables a far higher efficiency than average-power tracking for Voice Mode OP. Note that one can estimate the efficiency for various waveforms by moving down the ET or Linear PA operating curve from point A by the peak-to-average power of the new waveform.

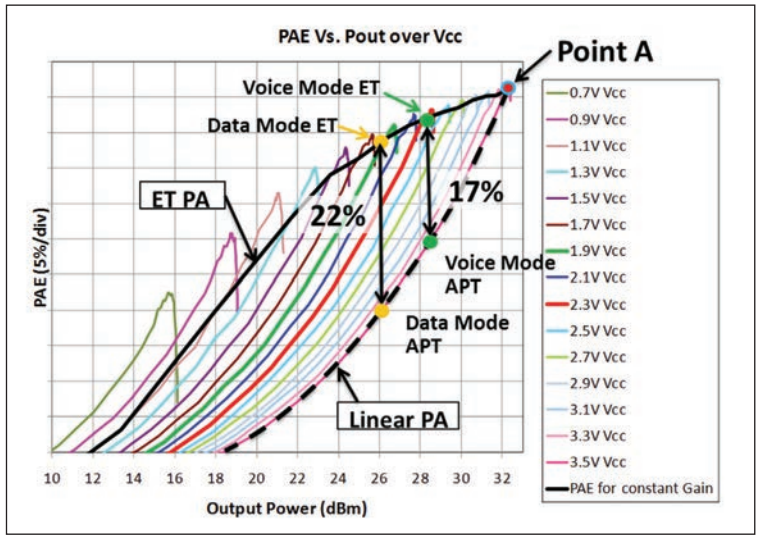


Figure 10. For Data Mode OP, envelope tracking (ET) provides a 22 percent higher power-added efficiency than average-power tracking (APT).

measurements on a specific power-amplifier, and a different design may change the absolute value of point A. While the absolute efficiency, or starting Point A, will vary from one amplifier design to another, or from one technology to another, the relative difference in efficiency from Point A will change very little. So the absolute efficiency, or starting Point A, will vary from PA design to PA design, and from technology to technology, but the relative difference in efficiency from Point A will remain close to the same.

Another comparison that can be made is to consider efficiencies associated with data, rather than voice. Assuming an LTE data operating point with a peak-to-average waveform of about 6.25 dB, the power added efficiency for average-power tracking is 22 percent less than that for envelope tracking (see Figure 10).

Armed with knowledge of the relative changes in power-added efficiency to point A simplifies a comparison of the various technologies. Point A has been calculated for a two-stage power amplifier, a form of design found in many handsets (see Figure 11 for details).

Relatively simple calculations based on this approach allow a comparison of HBT, silicon-on-insulator and CMOS technologies (see Table 1). While the power-added efficiency of amplifiers based on silicon-on-insulator technology have shown incremental improvement over time, with ST setting a new benchmark with an 80 percent drain efficiency, amplifiers based on the GaAs HBT are ahead by a considerable margin, and are getting even better with time. At first glance, the primary appeal of the silicon amplifier would thus be its apparently lower cost. But that's not the case: System-on-chip silicon amplifiers have die sizes that are three to five times bigger than those of GaAs HBT die, which means that the latter combines higher performance with lower cost.

A marriage of materials

This survey highlights the need to pick the best technology for each of the elements within the front-end of a mobile device. Take this approach, and silicon-on-insulator switches are combined with SAW filters and power amplifiers made from GaAs HBTs. The alternative, system-on-chip approach cannot exploit a material that excels in all areas. The leading

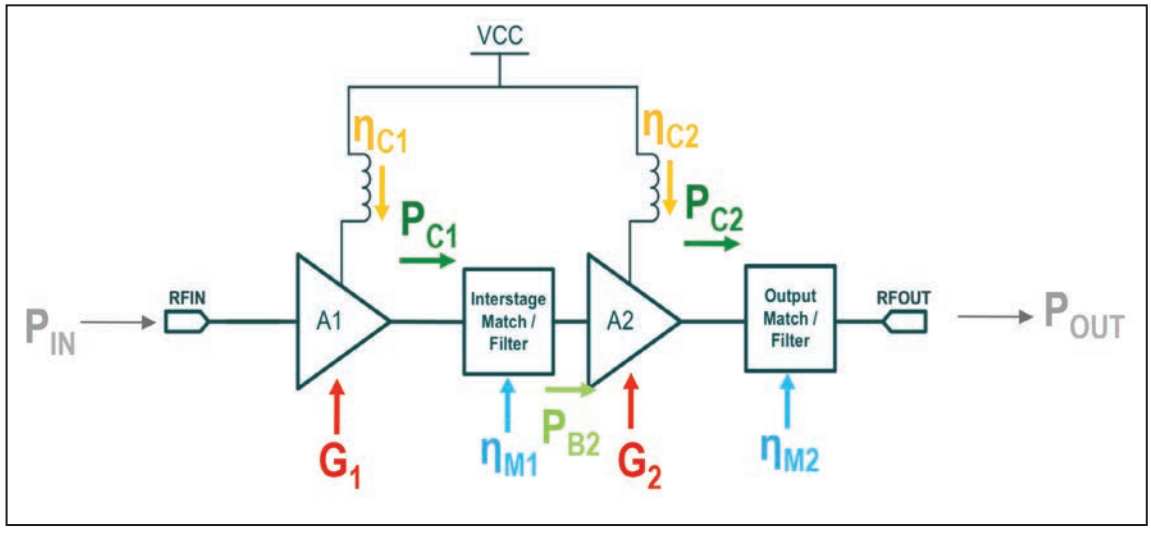


Figure 11. A typical multi-stage power amplifier. In this diagram, P_{IN} is the RF input power, η_M is the match efficiency, η_C is the collector or drain efficiency, P_C is the RF collector or drain power, P_{OUT} is the RF output power, and P_B is the RF base of gate power. Values for all these can be fed into relatively simple equations to calculate the power added efficiency. See Table 1 for results obtained in this manner.

your

EPITAXIAL GROWTH

partner

Enabling advanced technologies

- World leading technology
- Complete materials range
- MOCVD, MBE, CVD
- Advanced semiconductor wafer products
- Advanced R&D capabilities
- Multiple, manufacturing sites (Europe, Asia, USA)

IQE

www.iqep.com

Table 1. Amplifiers made with GaAs HBTs deliver by far the highest power-added efficiency. The comparison is using Point A of figure 10.

Technology	Drain or Col. Eff. η_{C2}	Output Match Loss η_{M2} (dB)	G_2	Inter-stage Loss η_{M2} (dB)	Driver Eff. η_{C1}	PA PAE Point A
GaAs HBT	89%	-0.65	14	-0.5	50%	71%
Measured HBT 2013						66%
Measured HBT 2015 Product						78%
SOI	75%	-0.65	14	-0.5	40%	60%
Measured CMOS Amalfi[7]						50%
Reported CMOS Nujira [8]	57%		14	-0.5	40%	54%
SOI Carrara, Presti, et al.[9]	72%	-0.65	14	-0.5	40%	57%
CMOS 65nm [10]	70%	-0.65	14	-0.5	40%	56%
Peregrine SOI PA [11]	72%	-0.65	14	-0.5	40%	57%
ST H9SOI [12]	80%	-0.65	14	-0.5	45%	64%

candidate is silicon-on-insulator, but it cannot integrate the filter on die. What's more, the assumption that a system-on-chip approach leads the way in terms of cost and a small footprint does not hold true for the RF front-end.

With the system-in-package architecture, the amplifier output match can be moved into the low cost laminate, and the power amplifier bias into a low-cost CMOS process. This creates a cheaper product that is also smaller, thanks to the reduced dimensions of the amplifier die. An additional strength of this design is the opportunity to stack CMOS and HBT die with three-dimensional packaging, a step that saves more space.

The system-in-package front-end will continue to improve, as new features are added with each generation of product. Receive carrier aggregation is now being incorporated, and soon this will be twinned with transmit carrier aggregation. Other refinements that are anticipated are an increase in receiver sensitivity and a reduction in the transceiver pin count, achieved by moving the low-noise amplifier next to the duplexers and into the front-end package.

The front-end design will continue to evolve, and system-in-package flexibility will allow it to quickly respond to market changes, enabling potential customers to quickly sample new products.

The author would like to acknowledge the work and effort of Greg Blum, Ed Lawrence, Phil Lehtola, and Dave Ripley without which this feature would not be possible, along with many other colleagues at Skyworks.

Further reading

1. J. Young, "Carrier Aggregation (CA) Quantifying Front End Loss," IWPC Workshop, Chicago, Sept. 16, 2014.
2. F. Raab *et. al.* IEEE Transactions on Microwave Theory and Techniques **50** No. 3, March 2002
3. F. Raab *et. al.* IEEE Transactions on Microwave Theory and Techniques **49** No. 6, June 20014.
4. M. Lapedus, "CMOS And SOI Invade RF Front End," Semiconductor Engineering, April 18, 2013
5. H. Jones, "Market Overview and Opportunities With Emphasis On RF," 2014 International RF SOI Workshop, Shanghai, China, Sept. 23, 2014
6. J. Young, "Mobile Handset PA Performance, ET vs. APT & GaAs HBT vs. SOI/CMOS," 2014 International RF SOI Workshop, Shanghai, China, Sept. 23, 2014
7. H-S Lee *et. al.* "RF Power Amplifier Design Series Part 4: RF Module Design using Amalfi CMOS PA," 2012 Agilent Technologies, Inc., Webcast
8. "Envelope Tracking: Unlocking The Potential Of CMOS PAs In 4G Smart Phones," Nujira White Paper, Feb. 2013
9. F. Carrara *et. al.* "Power Transistor Design Guidelines and RF Load-Pull Characterization of a 0.13-um SOI CMOS Technology"
10. S. Leuschner *et. al.* "A 31dBm, High Ruggedness Power Amplifier in 65nm Standard CMOS with High-Efficiency Stacked-Cascode Stages," 2010 IEEE Radio Frequency Integrated Circuit Symposium, RTU1C-3
11. N. Comfoltey *et. al.* "State-of-the-Art of RF Front-End Integration in SOI CMOS," 2013 IEEE S3S Conference
12. L. Formenti, "ST H9SOI_FEM: 0.13 RFSOI Technology for Front End Module Monolithic Integration," 2014 International RF SOI Workshop, Shanghai, China, Sept. 23, 2014

Book your place at the

PIC International Conference

Tuesday 1st & Wednesday 2nd March 2016

Limited availability

PIC International will provide comprehensive coverage of all aspects of the integrated photonics industry

This industry is currently debating a handful of key questions: -

- Is heterogeneous integration the best option for lighting up the IC? Or is it better to couple the laser's emission onto the chip?
- PICs are a solution to the rocketing demands facing datacentres. But what do they need to deliver, and how can they be put to best use?
- Are PICs about to dominate the landscape of optical networks? And is there room for different forms of device?
- Can companies afford to make PICs in-house? And if they do outsource, what should they look for from a foundry?
- The silicon CMOS industry sets a benchmark for chipmaking. How can the PICs industry catch up?
- Is it the case of selecting the right material such as InP and silicon for a particular application? Or can there be a universal, long-term winner for integrating all the components on one chip?

This inaugural event brings together the best in class of the integrated photonics industry, so make sure you attend PIC International.

Book your place NOW!

Sheraton Brussels Airport Hotel, Belgium

Register: www.picinternational.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

Extending the capabilities of **GaN-on-silicon HEMTs**

Removing the substrate allows GaN-on-silicon transistors to combine high operating temperatures with blocking voltages beyond 3 kV

BY FARID MEDJDOUB FROM IEMN

JUDGED IN TERMS OF SALES, silicon devices reign supreme within the power industry. But they are not without fault – while they are competitively priced, their performance is not that strong. For example, transistors that provide blocking voltages of 1 kV or more are limited to operating temperatures of 150 °C or less, and have switching speeds topping out at hundreds of hertz.

These weaknesses are a major impediment when these devices, in the form of IGBTs and IGOs, are used in medium-voltage applications such as: static reactive power compensators, which are used to stabilise power grids; and DC-to-DC converters in renewable power plants, which will undergo greater deployment with the uptake of 'smart' grids. The low switching frequencies associated with silicon devices, and the need to keep these chips operating at relatively low temperatures, means that the power switching systems are not as efficient as they could be, and the electronics requires cooling systems.

Improvements in efficiency at the system level could result from replacing silicon devices with alternatives that combine operating temperatures of more than 250 °C with switching speeds in excess of 20 kHz – the latter gain would limit auxiliary filtering requirements. The benefits of using superior devices would not be limited to greater efficiency, but would extend to smaller and lighter units, thanks to reductions in the sizes of accompanying capacitors and inductors.

The front-runners for replacing silicon in power-switching units are a pair of wide bandgap semiconductors: SiC and GaN. With an order of magnitude better conduction than silicon, and better switching properties, these wide bandgap materials are a natural fit for power electronics – they enable the production of smaller, faster, and more efficient devices that can withstand higher voltages and higher temperatures.

Of the two, devices made from SiC are the more mature. Today these are commercially available from various manufacturers. Some products, in the form of Schottky barrier diodes, have been on the market for more than a decade, but widespread adoption is hampered by the high cost of the devices.

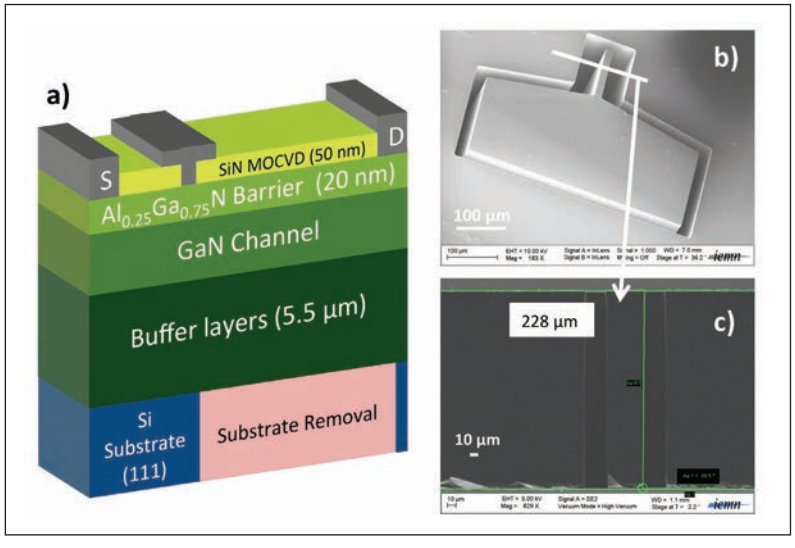


Figure 1: (a) A cross-section of the AlGaN/GaN HEMT with local substrate removal. (b) A scanning electron microscope image of a backside ring around the drain. (c) A scanning electron microscope cross-section of etched silicon trenches.

GaN has the potential to address this issue, while retaining the performance advantage over silicon. When this wide bandgap material is grown on silicon, chip costs are relatively low, while performance is very encouraging. Thanks to heterostructures that combine high mobility with a low specific on-resistance at high bias, devices can be manufactured that sport a low power loss and a high switching frequency.

The silicon substrate is actually a doubled-edged sword: It leads to low costs for the epiwafer, but limits the blocking voltage to typically below 2 kV, especially when the substrate is grounded. This limitation stems from a high electric field, which creates parasitic conduction at the interface between the buffer and the substrate. Leakage current increases, resulting in premature transistor breakdown.

To break through this barrier to higher blocking voltages, our team from The Institute of Electronics, Microelectronics and Nanotechnology in Lille, France, has developed a new device architecture that involves removing parts of the substrate that are in the vicinity of the high-electric-field region. This modification has led to a record-breaking lateral breakdown voltage of 3 kV, double that for conventionals device, for a transistor with a 40 μm gate-drain distance. What's more, at an operating temperature of 325 °C, our devices set another new benchmark, being the first GaN transistors to deliver a blocking voltage of more than 3 kV.

Devices are formed by carrying out full transistor fabrication on the front side, before using a 'Bosch' process to etch the substrate from the back side up to the buffer layer all around the drain (see Figure 1 (a) for the epitaxial structure and Figure 1 (b) for the post-etching architecture). Strengths of our deep etching process include highly reproducible vertical etching with a high aspect ratio (Figure 1 (c)), and full scalability for larger devices – gate widths of several tenths of millimetres are needed for high-power operation.

To ensure a rigorous evaluation of this process, local substrate etching has been performed on part of the cells across the wafer. This approach avoids growth and process induced variations.

We have compared devices with and without lateral substrate removal. For the more conventional transistors, off-state characterisation reveals bumps in the gate and drain currents at 500 V and 1000 V (see Figure 2). We attribute the first bump to issues related to the buffer-silicon interface. As the voltage increases, there is an exponential increase in leakage current to around 1.3 kV. In this regime the current, which is most likely the result of parasitic substrate conduction, reaches the 1 mA/mm limit at 1.5 kV.

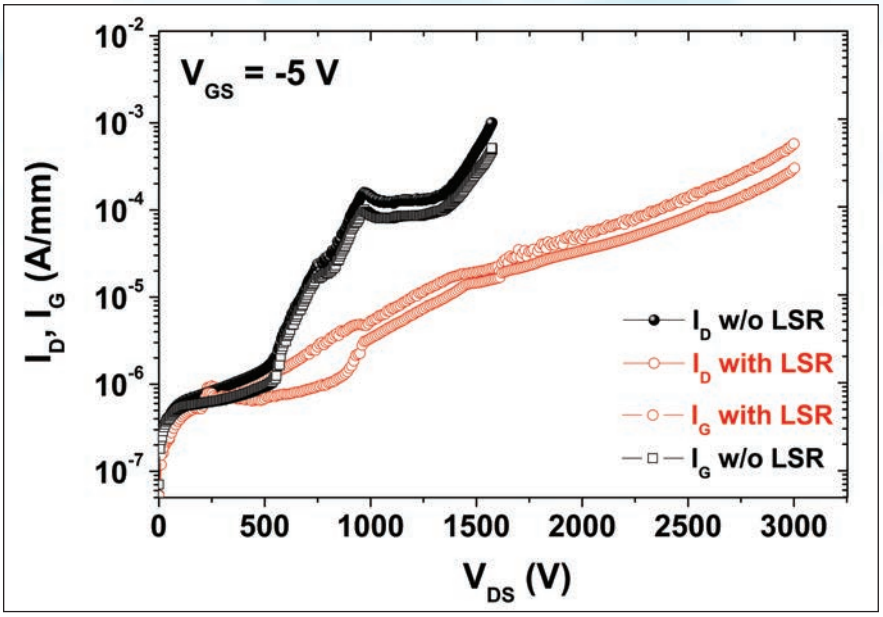


Figure 2: Off-state characteristics of a 1.5 x 50 μm² AlGaN/GaN HEMT with a gate-drain separation of 40 μm, with and without local substrate removal, at a gate-source voltage of -5 V.

Removing parts of the substrate eliminates the bumps in the off-state characterisation plots, and quashes leakage current in the 500 V to 1.5 kV range by an order of magnitude. These improvements result from the absence of current leakage at the buffer-silicon interface. The other noteworthy feature of the modified devices is the increase in breakdown voltage to the limit of what we can measure, 3 kV. This electrical characterisation confirms that our novel transistor architecture suppresses the conductive path of the substrate. It is worth noting that the gate and drain leakage currents are nearly identical in the devices we measure. This identifies the primary origin of the off-state leakage current as the Schottky gate leakage current, which could be suppressed significantly by adding a gate dielectric.

We have also studied the impact of the gate-drain distance on the specific on-resistance and the

The combination of the high blocking voltage and high operating temperature make our devices very attractive candidates for deployment in harsh environments. And these transistors should get even better, given that our work is still in its infancy

breakdown voltage, for both conventional devices and those that feature local substrate removal. For non-etched devices, specific on-resistance linearly increases as the gate-to-drain distance is extended from 5 μm to 40 μm (see Figure 3). The behaviour of the breakdown voltage was more complex, increasing linearly to 1.5 kV as the gate-to-drain distance is lengthened from 5 μm to 20 μm, before levelling off at higher voltages. This value is high for this class of device, reflecting the high quality of the thick buffer layers.

These results highlight that local etching of the substrate suppresses current leakage. Thanks to this, there is a continual increase in the blocking voltage as the distance between the gate and drain increases, while a low specific on-resistance is maintained.

We have benchmarked the performance of our devices by considering the specific on-resistance at breakdown voltages of 1 kV and above (see Figure 4). This evaluation, which includes unipolar SiC-based devices, indicates that the performance of our devices – a combination of on-resistances of 6.5 mΩ cm² and 10.1 m Ω cm² and blocking voltages of 2.4 kV and 3 kV, for devices with gate-drain distances of 30 μm and 40 μm, respectively – compares favourably with the state-of-the-art.

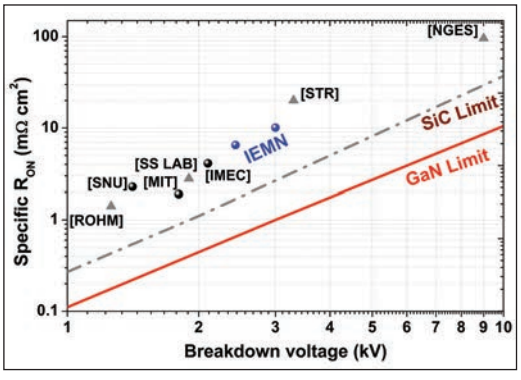


Figure 4: Benchmarking of specific on-resistance versus blocking voltage for GaN-on-silicon transistors and unipolar SiC-based devices rated beyond 1 kV.

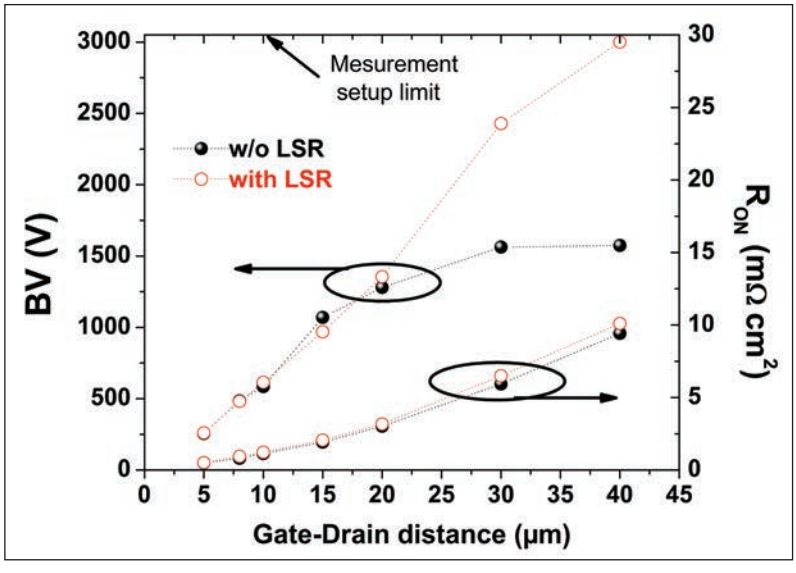


Figure 3: The blocking-voltage and specific on-resistance of AlGaN/GaN HEMTs, with and without local substrate removal, as a function of the gate-drain spacing.

One of the attributes of our wide bandgap devices is that they can operate at far higher temperatures than their silicon-based peers. To assess this level of superiority, we investigated device performances at temperatures of up to 600K. Measurements were conducted in vacuum, with a pressure of 10^{-6} bar, to prevent surface flashover under high bias. A more common approach, using a Fluorinert solution, is unsuitable, due to the fast evaporation of this liquid at elevated temperatures.

Measurements at a drain-source voltage of 10 V on 1.5 μm by 50 μm HEMTs are essentially identical for devices with and without substrate removal (see Figure 5). Changes in threshold with temperatures are rather small, exhibiting a positive shift of less than 200 mV up to 600 K. This shift is attributed to activation of the carrier trap density at high temperatures. The change in carrier density with increasing temperature is negligibly small.

Reasons to sponsor CS International Conference 2016

- ✓ Senior management networking opportunities
- ✓ Increased company and brand awareness
- ✓ Access to the top strategists within the compound semiconductor industry
- ✓ Create, develop and support customer relationships
- ✓ Engage in debate, share insight and expertise on industry challenges
- ✓ Gain visibility and recognition as an industry leader
- ✓ Leverage exposure in multiple industry media
- ✓ Demonstrate market innovation and leadership by launching new services, products and systems



www.cs-international.net

CALL NOW +44 (0)24 76718970
email **event@cs-international.net** or view the online sponsorship pack at **mediapack.cs-international.net**

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

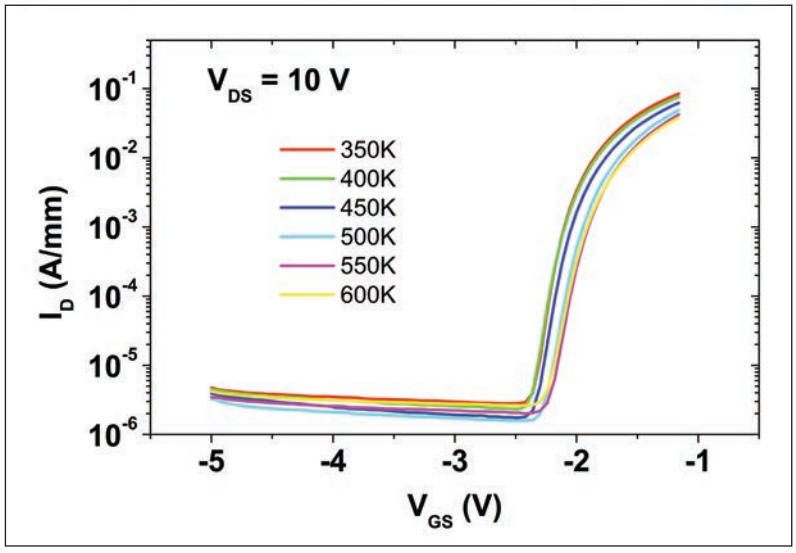


Figure 5: Temperature dependence of transfer characteristics at a drain-source voltage 10 V for 1.5 x 50 μm² AlGaN/GaN HEMTs with a gate-drain separation 40 μm. Similar evolution is observed with and without local substrate removal.

A characteristic that changes significantly with temperature is the drain current. At higher temperatures, the drain leakage is higher, even in devices subjected to local substrate removal (see Figure 6), due to an increase in buffer leakage. That is to be expected, because as the temperature increases, more residual donors are activated in the bulk (Al)GaN layers and interfaces (nitrogen implantation is fully stable up to 600 °C). It is worth noting that the transistors recover their original characteristics when cooled to room temperature, confirming the absence of permanent degradation.

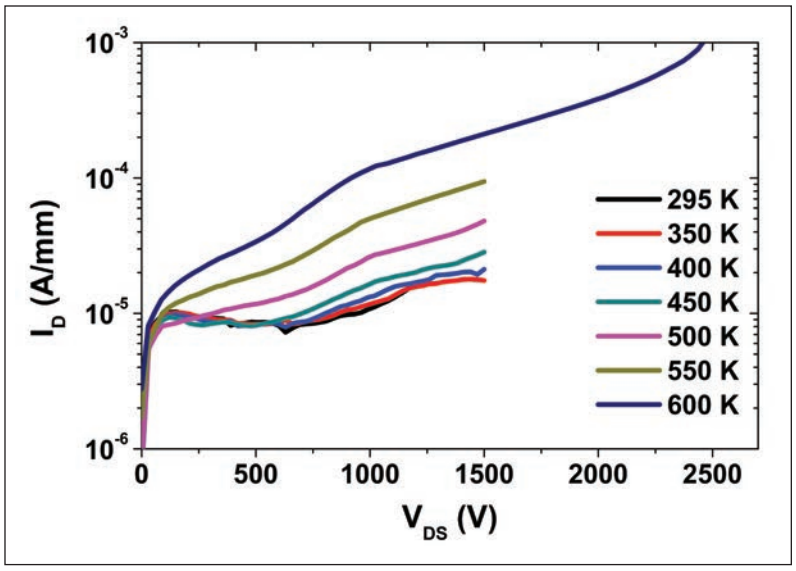


Figure 6: Temperature dependence of the drain leakage current from 295K to 600K for 1.5 x 50 μm² AlGaN/GaN HEMTs with a gate-drain separation of 40 μm and local substrate removal.

In etched devices, the breakdown voltage, evaluated as the voltage where leakage exceeds 1 mA/mm, decreases with temperature. However, this deterioration is not that severe, and a breakdown voltage close to 2500 V can be obtained at 600K.

This high blocking voltage at 600K is due to a remarkably small increase in leakage current with increasing temperature. To explain this, one must note that it is the conduction across the AlN seed layer and the silicon substrate interface that plays an important role in the degradation of the breakdown voltage at high temperature. With our novel devices, this conduction is hampered by the removal of silicon, a feature that holds the key to high-voltage operation at high temperatures.

The combination of the high blocking voltage and high operating temperature make our devices very attractive candidates for deployment in harsh environments. And these transistors should get even better, given that our work is still in its infancy.

A reduction in the specific on-resistance is promised by moving to a higher-polarization, aluminium-rich barrier heterostructure, and a slashing of the off-state leakage current could result from the introduction of a gate dielectric. There is also the possibility of making a major improvement to thermal dissipation, without degrading the outstanding breakdown voltage, by depositing materials inside the trench.

One option is the pairing of a high breakdown field (> 4 MV/cm), thick dielectric, such as AlN, followed by a thick copper metallization. With all these routes to be explored to improving the performance of our novel form of GaN HEMT, its future looks very bright.

The work reported here has been sponsored by the French Defense Ministry (DGA) as well as the French RENATECH network. The authors would like to acknowledge the company EpiGaN for high quality material delivery.

Further reading

N. Herbecq *et. al.* Appl. Phys. Express **7** 034103 (2014)
N. Herbecq *et. al.* " Above 2000 V breakdown voltage on ultrathin barrier AlN/GaN-on-Silicon transistors ", Proc. of CS MANTECH (2015).

SEMICON® KOREA

January 27 - 29, 2016
Hall A·B·C·D COEX, Seoul
Organized by SEMI
www.semiconkorea.org

Pre-register Now

for complimentary admission
November 16 to January 20

Co-located with

LEDKOREA

semi

Targeting spectroscopy with antimonide sources

By delivering great performance at low cost, GaSb-based devices are the ideal sources for gas sensing

BY AUGUSTINAS VIZBARAS FROM BROLIS SEMICONDUCTORS

LASERS are incredibly well suited to targeting the specific absorption features of gas molecules. These inherently narrow-linewidth, high-brightness sources enable rapid, sensitive gas detection, making them suitable for a vast range of applications. They can be used for: industrial process monitoring in petrochemical, plastic, automotive and space industries; environmental and trace gas monitoring; and biomedical and security applications, agriculture, semiconductor fabrication and metrology.

Of all the possible classes of laser that can be used for gas sensing, by far the best is that based on a semiconductor diode. This solid-state source combines ease of high-volume manufacture with some great attributes, including low cost, small size, a continuous-wave output, a high level of efficiency, and the opportunity to modulate the output. What's more, diode lasers are simple to use, and by making small changes to the drive current, the wavelength changes in a linear fashion. This makes for a simple, predictable sensor system design.

At Brolis Semiconductors of Vilnius, Lithuania, we are trailblazing the high-volume manufacture of a class of diode laser that is ideally suited to gas sensing in a spectral range spanning the near-infrared to the mid-infrared. We believe that our devices, which are conventional laser diodes operating at far longer wavelengths than usual, offer a higher level of performance than common solid-state alternatives: interband cascade lasers and quantum cascade lasers.

Their superiority stems from the manner in which light is generated within the device. In laser diodes, radiation results from an optical transition in so-called type-I quantum wells, while in interband cascade lasers emission occurs through a type-II transition in a cascaded superlattice structure, and in quantum

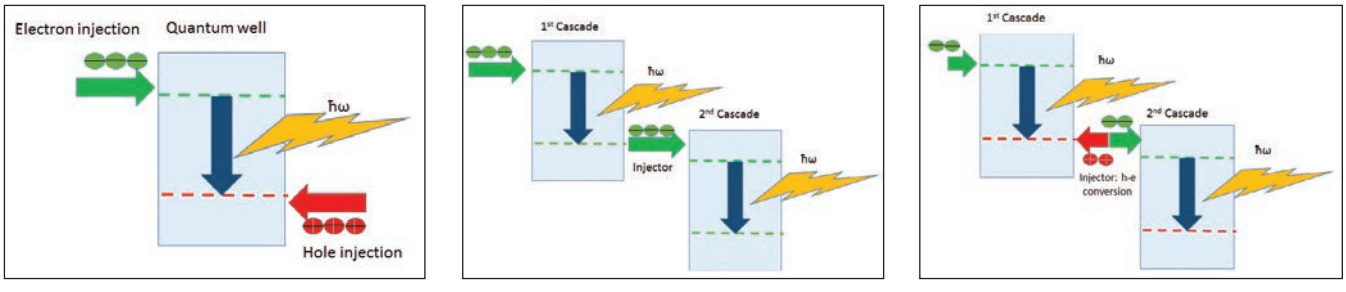
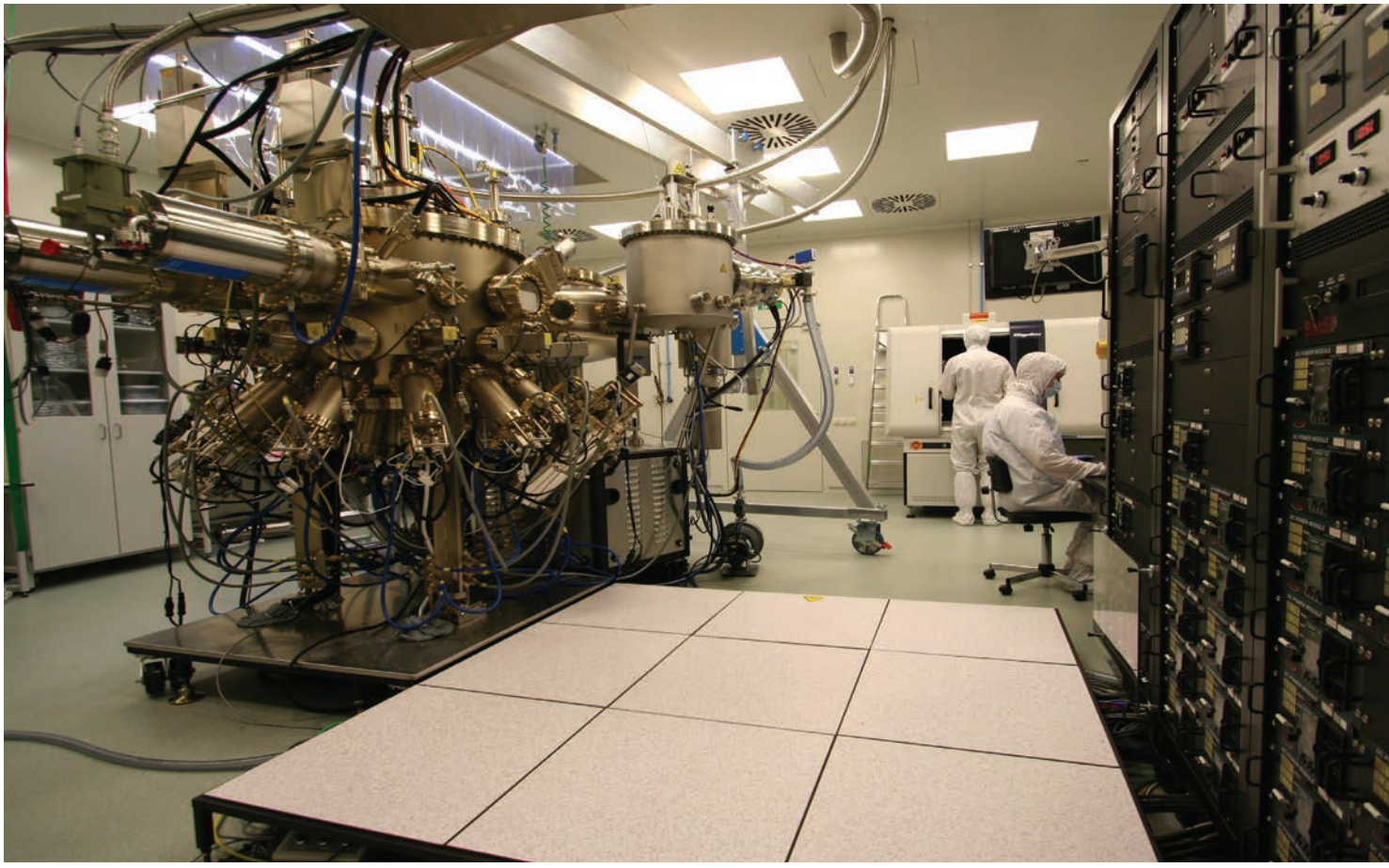


Figure 1. Schematic representation of light generation principles in three discussed technology platforms: a) type-I quantum well; b) quantum cascade laser and c) interband cascade laser. Green arrows depict electron injection into conduction band quantized state (green dashes); red arrows depict hole injection into valence band quantized state (red dashed line); and blue arrows depict optical transition.



Industrial multi-wafer MBE tools such as the Veeco Gen200Edge are used to produce long-wavelength, antimonide-based sources.

cascade lasers the output comes from cascaded intersubband transitions that take place in the conduction band of many coupled quantum wells (see Figure 1).

Of all these three mechanisms for generating light, the most efficient and effective is the type-I optical transition. With this process, the electron and hole wave-functions have the largest overlap, resulting in gain that is sufficiently high to ensure lasing without the need of cascading – and this means the lowest possible voltage drop. Gain in interband cascade lasers and quantum cascade lasers is far lower, so to realize a sufficient output, the region where light is generated must be formed from multiple zones. Repeating the active region several times in the interband cascade laser and several tens of time in a quantum cascade laser addresses the issue of sufficient gain, but comes with the penalties of a higher drive voltage and increased power consumption.

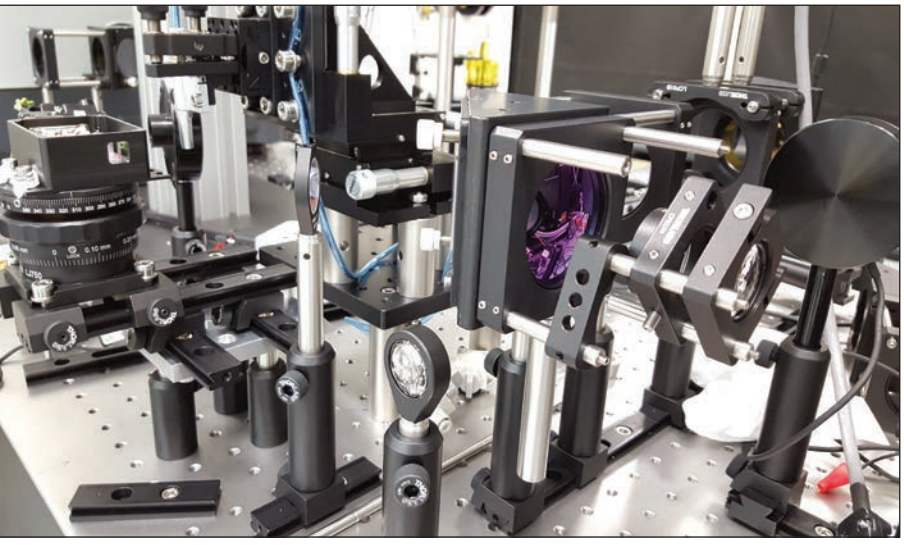
Drawing more power is a major drawback, because it hampers deployment of battery-operated gas sensing. A good figure of merit for evaluating the power consumption of the laser is the input threshold power – a product of drive current and drive voltage required to achieve lasing – and this tends to increase as the emission wavelength stretches further into the infrared (see Figure 2).

Antimonide attributes

Our lasers are based on the GaSb-based material system, which is the preferred III-V for the 2.0 μm – 2.6 μm spectral range. Emitters made from this III-V are capable of wavelengths as short as 1.5 μm, and can stretch as far as 3.7 μm with type-I quantum well technology – and right out to 6 μm with interband cascade laser technology. As well as making lasers from GaSb, we produce other types of emitter, including broad-spectra superluminescent diodes and structures that can provide a gain medium for ultra-widely tunable spectroscopy.

This choice allows the use of the most appropriate device for a particular application. For example, there are situations where detection sensitivity is not paramount – this can occur when the concentration of the detectable agent is high, or the absorption band is broad, as is the case in liquid solutions. In these instances it is possible to employ a broadband source, with the superluminescent diode being the perfect choice.

Distinct from a laser, the superluminescent diode has an output mirror loss that is sufficiently high to prevent lasing. Due to this, the device operates in the superluminescent regime, where it combines a broad emission spectrum with a relatively high output power. With our devices, the spectral density can hit 1 mW/nm (see Figure 3), while the output power can be an order of magnitude higher than that of mid-infrared LEDs produced elsewhere. Another product that we make, which is suitable for widely tunable spectroscopy, is an external cavity laser. This



Moving to wavelengths beyond 2 μm requires custom optics components as glass becomes absorptive. Special types of glass, chalcogenides, silicon and germanium need to be used.

features a diffraction grating that rotates, allowing a tuning of the wavelength where feedback is delivered to the gain-chip and amplification occurs. With this approach, wavelength tuning can occur over the entire gain curve, which can be 100 nm wide.

One problem to avoid with the external cavity laser is undesired mode-hoping, which results from instantaneous switching between neighbouring modes. This can be prevented by lowering the facet reflectivity to 10^{-5}. Realising such a low figure with straight waveguides is very challenging, so we introduce additional device design elements, such as a bending of the laser ridge at a certain radius, to minimize feedback into the cavity.

Performance is maximised with a single-angled-facet design (see Figure 4). Such a chip features an output facet with a waveguide bent at a certain angle and coated with a low anti-reflection coating delivering minimal reflectivity; and a back facet coated with a high-reflectivity mirror to maximise output power. A strictly single-spatial mode output is produced by our single-angled-facet gain-chips, which can provide over 100 nm of tuning per chip, while maintaining high continuous-wave output across the entire tuning range. The side-mode suppression ratio from these lasers is over 30 dB, enabling them to deliver excellent performance, even for the most demanding of sensing applications (see Figure 5).

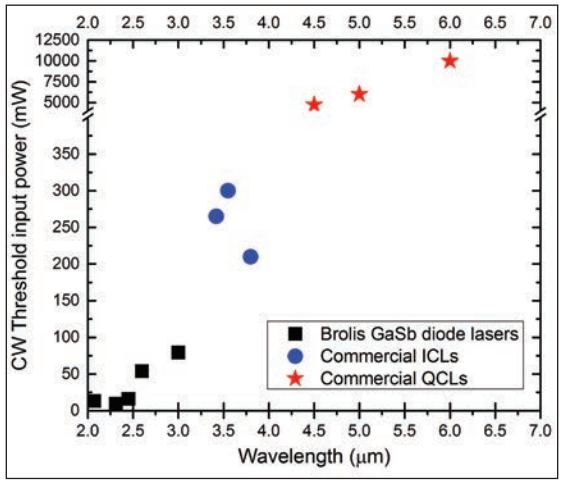
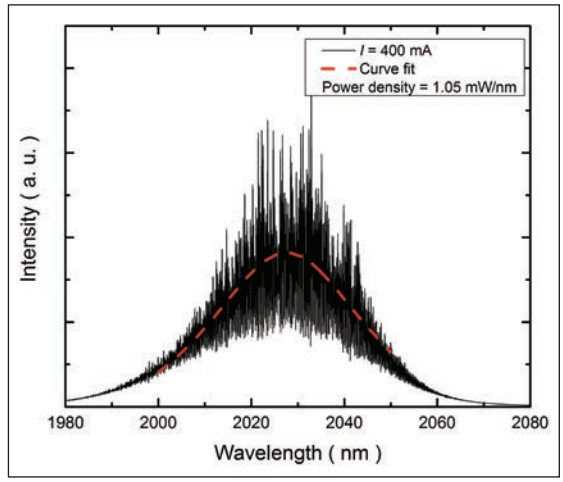


Figure 2. Input threshold power versus emission wavelength for three technology platforms.



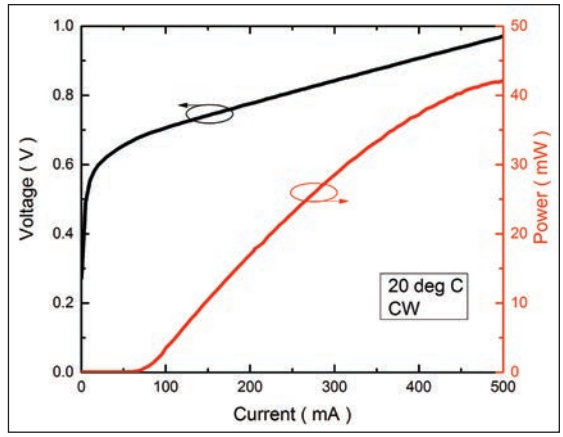


Figure 3. Typical performance of Brolis high-power superluminescent diode: a) spectrum with power density exceeding 1 mW/nm and b) typical L-I-V data.

If gas sensing requires the detection of a single, known gas molecule, then thanks to its inherently narrow absorption line, tuning over a narrow range is sufficient. Single-frequency lasers are suitable for this task, allowing the use of a VCSEL, a distributed feedback laser, or a single-frequency laser employing a single-angled-facet gain-chip and a fixed position grating. One of the merits of the latter is that it produces a very narrow linewidth – it is typically less than 100 kHz, a figure low enough to enable ultimate sensitivity for the most demanding of applications. In comparison, VCSELs and DFBs have an inherently wider linewidth of typically 10 MHz or more, and a low output power.

Our single-frequency laser employing a single-angled-facet gain-chip can be housed in a commercial HHL

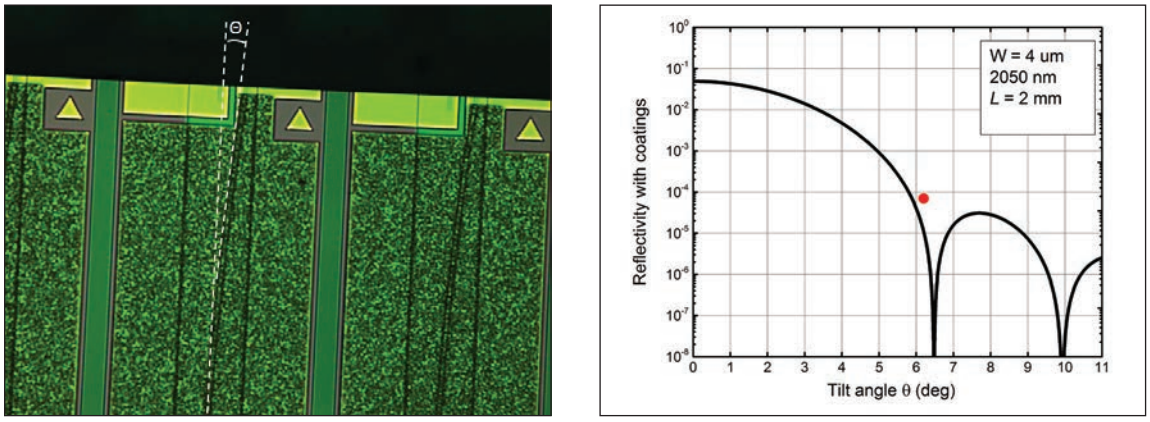


Figure 4. a) Microscope picture of Brolis single-angled facet gain-chip featuring angled output facet; b) Simulated power reflectivity as function of output facet angle. Red dot indicates experimentally determined reflectivity of 2 μm gain chip.

package, comparable to those used for commercial QCLs. Placed in this package, our lasers have a tuning range of 30 GHz – 40 GHz, which is sufficient for sensing a gas molecule.

This design is well suited to serving a small-sized market requiring relatively low quantities of different wavelengths. The single-angled-facet gain-chip can be used to make a single-frequency laser at any wavelength within the gain curve, thus avoiding the need to grow multiple epi-wafers that satisfy ten wavelengths and are spaced 10 nm apart.

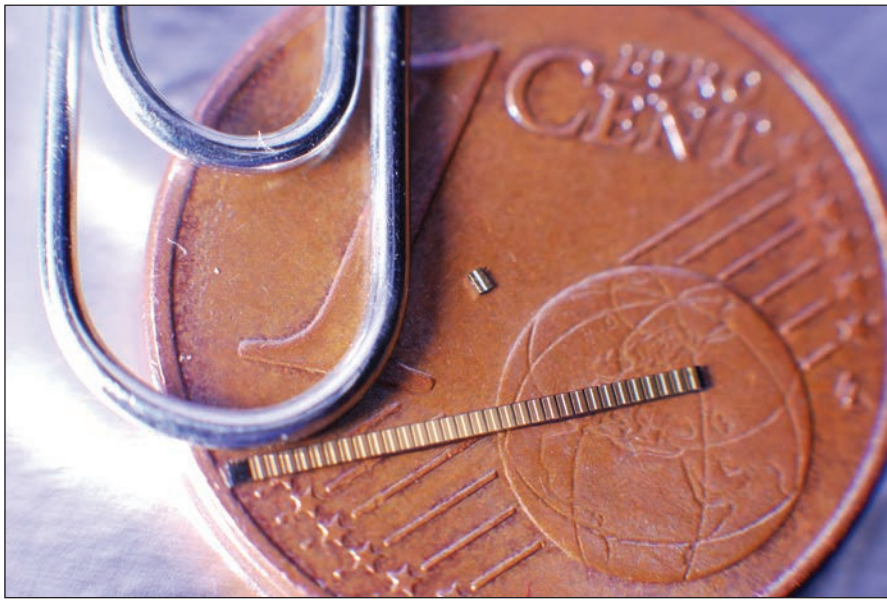
Ease of manufacture

To target a mass market, the design of the light source must enable high-volume, high-yield manufacture of a reliable, affordable product delivering at least satisfactory levels of performance. Judged in these terms, our design that is based on a type-I quantum well trumps the interband cascade laser and the quantum cascade laser (see table 1 for details of this evaluation).

This superiority partly stems from the far lower number of interfaces in our class of laser. In a type I quantum well laser diode, the majority of the structure is formed from a few bulk layers, and there are only a few quantum wells in the active region. Such a structure has a relatively small number of interfaces, which reduces machine wear. However, it is only fair to note that for the growth of a GaSb type-I quantum well, deposition of the bulk layers is typically quite complex. There is a need to form ternary and even quinary compounds, making growth far more complex than it is for shorter-wavelength laser diode structures made from the GaAs and InP material families.

With lasers with a cascade structure, the number of interfaces is far higher than it is for a laser diode, due to the huge number of quantum wells that form the active regions and carrier injection parts. Growing these structures by MBE requires the opening and closing of thousands of shutters, and a comparable number of valve movements are required for deposition via MOCVD. Whichever growth technology is adopted, those mechanical adjustments accelerate machine wear within the tool and significantly shorten the length of the growth campaign. This can be 30 percent shorter, with an MBE growth campaign for a type-I quantum well laser diode structure lasting for 10-11 months before being interrupted for 45 days for maintenance, while the campaign for the laser with cascade structures is limited to 7-8 months. The increased maintenance of the machine and the reduced 'up-time' lead to a hike in production costs.

Another virtue of making a long-wavelength infrared laser with type-I quantum wells is that it is compatible with straightforward approaches to qualification of wafers prior to processing. Savings are not only in the form of money, which would be wasted on fabrication costs, but also time: Typical foundry lead times before the dies can be put under test are 3-7 weeks. With type-I quantum well structures, the strong optical transitions in the active region enable epiwafers to be



The small sizes of long-wavelength light sources allows many devices to be formed from a single wafer.

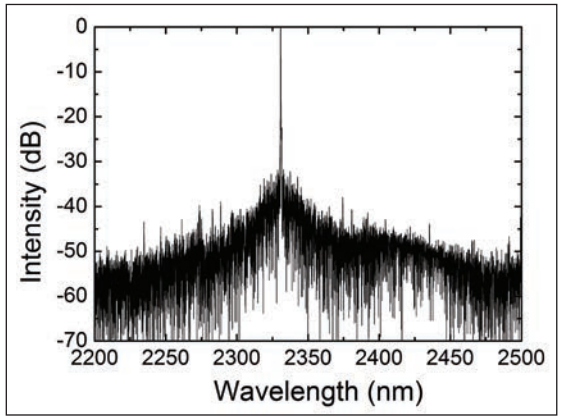


Figure 5. Widely tunable single-angled facet gain-chip performance: a) CW tuning curve of the Brolis SAF gain-chip family with more than 100 nm of tuning/chip; b) typical single-frequency emission spectrum with a side-mode suppresion ratio in excess of 30 dB for the gain-chip in external cavity setup.

probed by standard photoluminescence techniques. This approach uncovers direct information on emission wavelength, and the optical quality and homogeneity of the wafer (see Figure 6 (a)). To evaluate the electrical properties of the wafer, on-wafer current-voltage measurements can be performed (see Figure 6 (b)).

Evaluating the wafer before processing is more challenging with interband cascade lasers, and very tough with quantum cascade lasers. For both types of device, a reliable quality assessment can only be performed after the wafer goes through the entire fabrication process and initial bar testing is carried out.

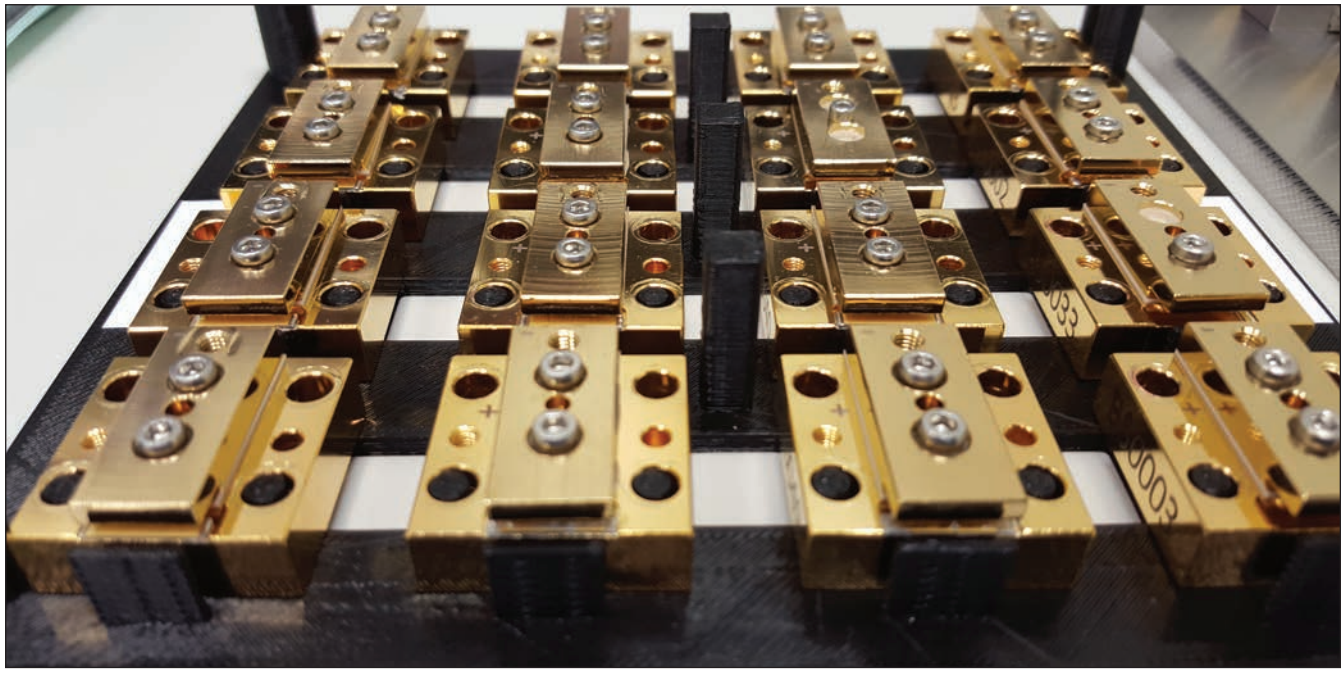
Photoluminescence, a very informative technique for scrutinising structures with type-I quantum wells, can only reveal the approximate emission wavelength in interband cascade structures, and it is not able to offer a worthwhile insight into epiwafers with quantum cascade lasers. In both cascaded structures, the electrical field has to equal a particular value to ensure a desired quantized energy alignment that is required for lasing – and this situation can only be evaluated after production of the laser.

An additional, common technique for assessing epiwafer quality is high-resolution X-ray diffraction. This, in combination with photoluminescence spectra and current-voltage measurements, enables excellent evaluation of whether an epiwafer featuring a type-I quantum well should be scrapped or sent on to the fab for processing. With the cascade-based lasers, however, high-resolution X-ray diffraction is the only tool offering considerable insight into the structure, and this is not sufficient to determine whether to process a wafer or scrap it.

Our claims relating to the inferiority of quantum cascade laser technology may raise eyebrows, given the volume of scientific papers that back this class of laser, due to its inherent advantage of being compatible with standard telecom foundry processes. But it should be noted that this argument is only relevant to wafer processing technology, which is actually quite similar for both GaSb type-I and interband cascade technology (in fact, all these wafers can be perfectly processed in any InP foundry, making compatibility a general feature rather than an advantage). The most important point is that the very limited number of reliable, non-destructive methods that are available for testing quantum cascade lasers makes manufacture more challenging and lengthens product development times. Higher chip costs result, hampering sales in mass markets.

Why is this weakness associated with cascaded designs often overlooked? Well, today the markets for long-wavelength infrared sources are small, and customers are accepting costs of a few thousand

For defence applications where output power is paramount, GaSb emitters are combined into bars to provide CW output power of several tens of Watts.



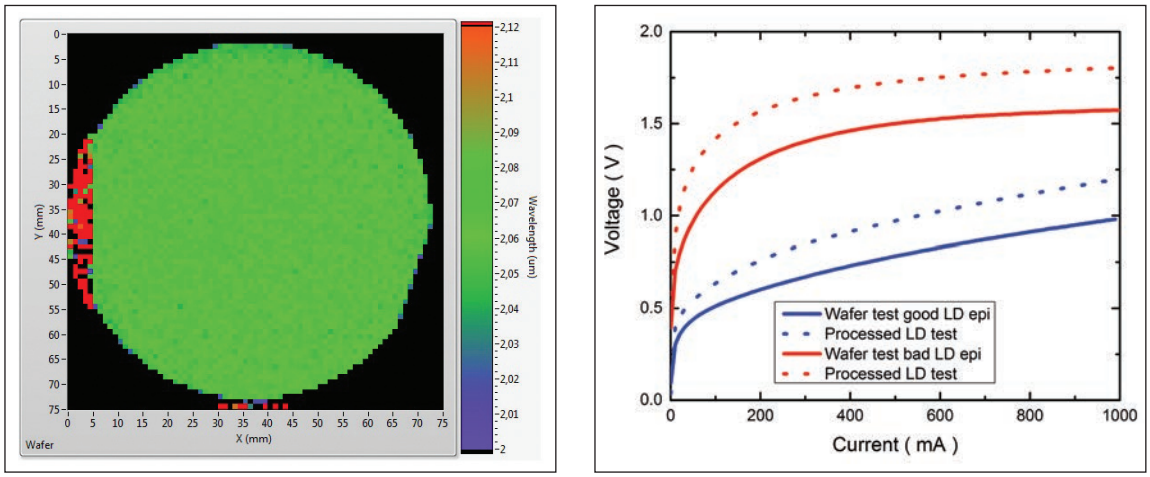


Figure 6. Type-I quantum well technology benefits from the availability of early-stage on-wafer testing for the decision on the fab process: a) typical photoluminescence peak wavelength distribution across the 3-inch laser diode epi-wafer; b) electrical on-wafer qualification compared with device electrical performance after fab processing.

dollars per chip. But this must come down if an application – be it gas sensing, for example – is to be served with a solid-state laser.

Another factor governing the cost-per-chip is the size of the substrate. Lasers with a cascade structure tend to be grown in small, research-grade reactors. This limits the substrate size to 2-inch in a multi-wafer configuration and 3-inch in a single wafer tool. Transferring the production process to larger substrates in a multi-wafer tool is challenging, due to complexities of growth. There are a vast number of interfaces, and forming these well demands extremely precise temperature control across the platen. It is a very different story for the growth of type-I quantum well lasers. Substrate sizes are larger – GaAs has reached 4-inch as standard; InP is typically 3-inch; and GaSb is 3-inch, but it could move to 4-inch if warranted by market demand – and structures with sufficient quality can be formed in large multi-wafer tools operating with high up-times.

Advantages such as this highlight that when it comes to large-scale applications involving tuneable laser diode absorption spectroscopy, type-I quantum well devices are the leading technology in terms of manufacturability and mass market readiness, regardless of device type. Whether it be distributed feedback lasers, VCSELs, superluminescent diodes or LEDs, it is devices with this form of active region that are best-positioned to serve as the light sources in the final system.

	Preprocess qualification	Growth complexity	Growth machine wear down	Device reliability	Commercial substrate size	Manufacturability
Type-I QW	Very good	Medium	Low	> 10 000 h	3-inch	Good / Very good
ICL	Medium	Very high	High	Limited data	2-inch & 3-inch*	Low / Medium
QCL	Poor	Very high	High	> 10 000 h	2-inch	Low

Table 1. Judgement on manufacturability focuses on three main aspects: ease of production, potential for low cost, and reliability. Ease of production takes into account machine wear down, growth complexity and pre-process qualification, all of which affect the final cost per chip, together with the commercially available substrate size. Reliability is related to final device lifetime, which should be compatible with standard industrial lifetimes. Typically, 10 000 hours is sufficient for most applications. *data is limited to single 3-inch wafer growths by US Navy Labs. The commercial growth of interband cascade lasers (ICLs) is performed with small, research-grade MBE reactors.

Can Auger recombination be good for LEDs?

Many view Auger recombination as an incurable illness that saps the efficiency of the LED. But that affliction goes hand-in-hand with two little-known but important benefits: A reduction in turn on voltage and higher wall-plug efficiency

BY SIMON LI FROM CROSSLIGHT

THE LED is a simple device with a few layers, an active region that is fairly easy to understand, and just two doped regions in the entire structure. However, despite all this simplicity, the LED is not that well understood. When it is made from GaN-based material, its quantum efficiency falls off at high current densities for reasons that are far from obvious. This has led those working in this field to debate the origin of this energy-sapping malady, which goes by the name of droop.

A popular explanation for the cause of droop is that it is some form of Auger process. This reduces the quantum efficiency, because when an electron and a hole come together, instead of recombining radiatively, they are involved in a non-radiative process that transfers energy to a third carrier.

The leading alternative explanation for droop is electron leakage. The thrust of this argument is that instead of recombining in the quantum wells, electrons hop over the electron-blocking layer and enter the *p*-type region, where they either recombine with holes or reach the metal contact.

Those in the Auger camp will take heart from the recent work presented by a partnership from the University of California, Santa Barbara, and the École Polytechnique, France. This team reported experimental detection of energetic Auger-induced hot carriers in 2013 [1].

Work of this nature is rare, however: There are very few direct measurements of either an Auger-based process or electron leakage, and this state of affairs is hampering closure over the leading cause of droop. To try and fathom the cause of this malady, many theorists are offering simulations – but this is adding to the confusion, because various theories all lead to more or less the same efficiency droop. This

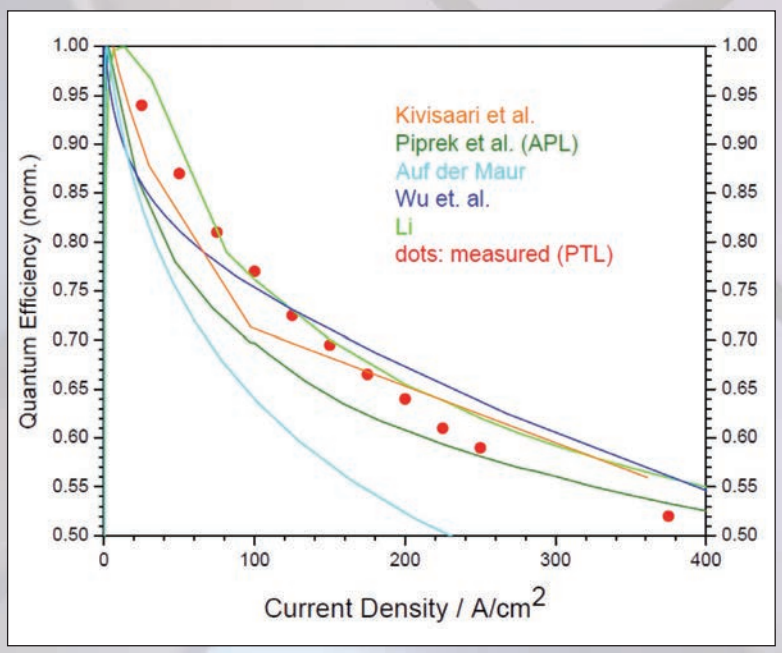


Figure 1. Normalized internal quantum efficiency from various theoretical calculations. Data first presented in a special issue of Journal of Computational Electronics (JCEL **14** 2015).

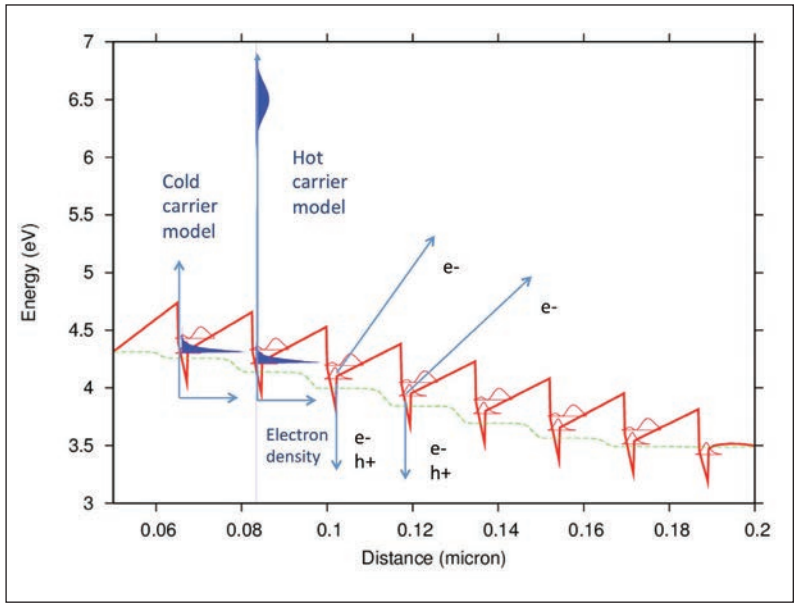


Figure 2. Band diagram of conduction band from conventional drift-diffusion calculation. Quantum states are indicated by fine red lines and Fermi level by dashed green line. Overlaid on the first well is the electron density distribution plot for cold carriers. The hot carrier model is indicated at the second well with Auger generated hot carriers at 2.3 eV above the Fermi level.

situation is not helped by researchers applying their simulations to different LEDs, which may sport different architectures or have substantial differences in material quality.

To address the latter limitation, several different groups have modelled exactly the same experimental data. It came from measurements on a conventional, multi-quantum-well, blue-emitting LED that had been made and scrutinised by researchers from National Cheng Kung University, Taiwan.

The results of this multi-group theoretical effort were unveiled in the June 2015 issue of the *Journal of Computational Electronics*. The main difference between the approaches of various groups was the model used for carrier transport. Researchers based at Aalto University, Finland, employed a Monte-Carlo method; Matthias Auf der Maur from the University of Rome 'Tor Vergata' adopted an approach based on the non-equilibrium Green's function; a team from National Taiwan University based their approach on percolation transport, while considering random alloy fluctuations; and I, head of the software company Crosslight, pursued a simulation based on non-local transport. Yet despite these major differences, the simulated plots of efficiency as a function of current were similar (see Figure 1).

What about I-V curves?

One option for distinguishing between the right and wrong way to model droop is to consider another piece in this puzzle: The turn-on voltage. This characteristic is important, because it influences the wall-plug efficiency. What's more, if a model is credible, it should be able to explain both the efficiency curve and the current-voltage plots.

The turn-on voltage offers an insight into the internal band alignment. In a blue LED that emits at 430 nm, the energy of the photons is nearly 2.9 eV. Since the Fermi level split is expected to be about 90 percent of this figure, it should be about 2.6 eV.

This value for the Fermi level split for a blue LED should be similar to that found in the LED made by the team from National Cheng Kung University, which features barriers in the active region that are wider than most – they have a thickness of 15 nm. One of the consequences of this is that the polarization charge at the interface with the multiple quantum well lifts up the height of the barriers to such an extent that a highly resistant material layer results (see Figure 2).

According to most theories, this resistance, which is compounded by the electron-blocking layer, should result in a voltage drop of around 0.7 V. But this is not seen in the current-voltage measurements on real devices.

The large voltage drop is also absent in the results of my calculations, which are based on a non-local carrier transport mechanism that mimics

"One option for distinguishing between the right and wrong way to model droop is to consider another piece in this puzzle: The turn-on voltage. This characteristic is important, because it influences the wall-plug efficiency. What's more, if a model is credible, it should be able to explain both the efficiency curve and the current-voltage plots"

the effects of hot carriers near the active region. Due to the presence of these hot carriers, which are generated by an Auger process involving two electrons and a hole, there is no need for an extra 0.7 V to kick–start conduction through multiple barriers (see Figure 3). Thanks to this, the resistance of the device is lower than it would be otherwise, and the wall-plug efficiency is higher.

Other theories fail to reproduce a small voltage drop because they are based on cold carriers. In these models, carrier transport through the heterojunction and quantum wells is evaluated assuming quasi-equilibrium – that is, carriers in the quantum well, or at the lower part of the barrier, share the same Fermi distribution as those in the barrier or near its top.

It is possible to visualise this by thinking about a carrier distribution that decays exponentially as energy is increased (see Figure 2). In this case, described by the thermionic emission model, only a tiny fraction of carriers have sufficient thermal energy to overcome the high barriers.

With the hot carrier model, the situation is very different. In this scenario, the non-radiative recombination of electron-hole pairs excites hot Auger carriers to an energy state 2.3 eV above the Fermi level [1]. How far the hot Auger carriers can travel without losing energy is a contentious issue, but it is reasonable to assume that they will overcome the barriers.

To carry out these simulations, I have incorporated a rather special simulation technique called non-local multi-quantum-well transport into my company's drift-diffusion-based simulation software APSYS. With this approach, the simulation mesh from within each well is connected to beyond the active region. This special mesh connection – that goes both forwards and backwards (see Figure 4) to reflect the fact that Auger hot carriers have random momentum after generation – allows one to mimic the escape of the hot carriers.

One of the features of my model is that it allows the adjustment of the fraction of hot carriers that can make the long jump over the barriers, rather than being locally thermalized. Even when the proportion that makes this leap is set very low, the multi-quantum-well region is modified to a flat-band condition, which eliminates the 0.7 V drop that is predicted by other theories, but not observed in measurements on real devices.

Clearly, the strength of my model is that, unlike its rivals, it is not limited to replicating the experimental data for the efficiency curves – it can also account for the current-voltage plots. What's more, it shows the impact of Auger in a different light. Yes, in terms of a loss of carriers out of the quantum well, Auger is a villain. But it also has its good side, driving down the operating voltage and driving up efficiency.

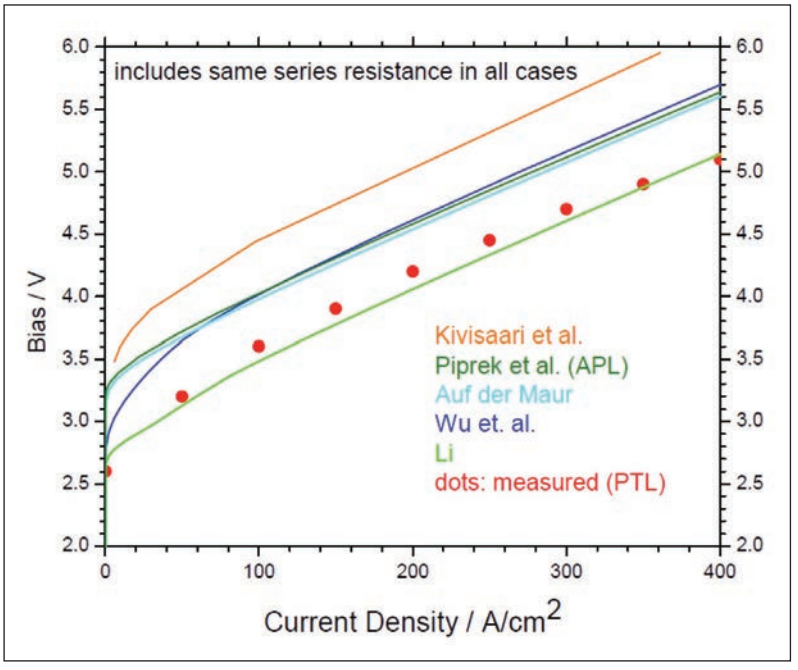


Figure 3. A current-voltage curve from various theoretical calculations. This data first appeared in the special issue of JCEL **14** 2015. More details can be found at: https://nusod.wordpress.com/2015/06/03/how-to-explain-the-low-turn-on-bias-of-blue-light-emitting-diodes/

The author thanks Joachim Piprek for insightful discussion and for providing the data comparison appearing in this feature.

Further reading

[1] J. Iveland, et.al., Phys. Rev. Lett. **110** 177406 (2013)
[2] Z. M. Simon Li, Journal of Computational Electronics **14** 409 (2015)

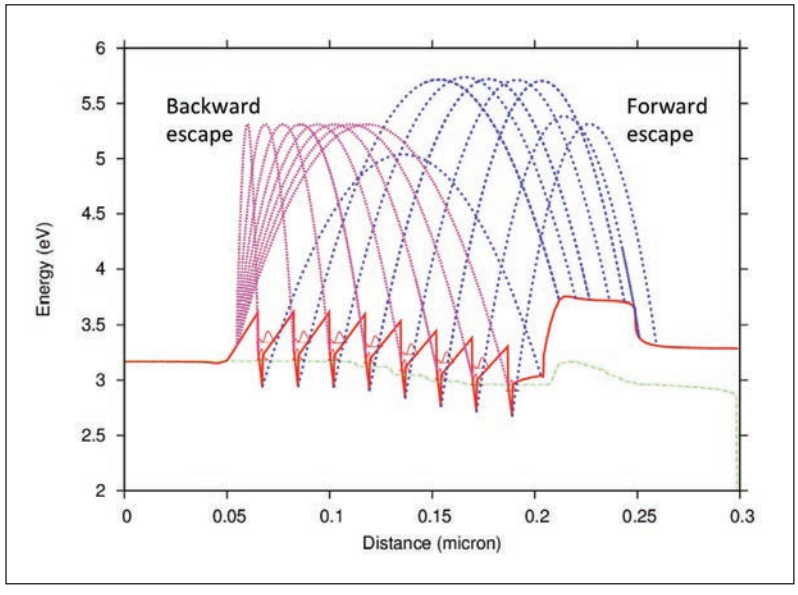


Figure 4. Mesh connections indicating non-local carrier transport paths to mimic the behaviour of Auger generated hot carriers.

Optimising LEDs with tunnel junctions

Nanowires and tunnel junctions enable phosphor-free white light under AC power

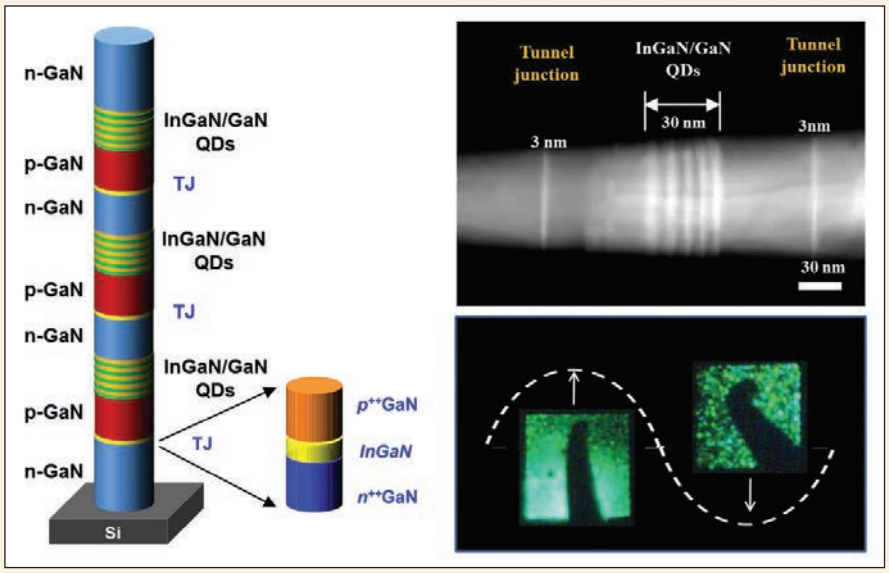
LEDs are a great source of lighting, combining high-efficiencies with long lifetimes and the ability to hit full brightness in an instant. But they also have their weaknesses: it is not possible to plug conventional devices directly into the mains; there are an internal losses associated with producing white emission via phosphor conversion; and there is droop, the decline in device efficiency at higher drive currents.

It is possible to address all these issues, however, with a novel LED architecture pioneered by Zetian Mi and co-workers from McGill University. This team has developed nanowire LEDs that, thanks to the incorporation of GaN-based tunnel junctions, can be driven by an AC source. These devices can feature red, green, and blue emitting sections, so avoid losses associated with pumping phosphors.

Mi believes that one of the most important aspects of this team's work is that it provides the first demonstration of InGaN/GaN nanowire LEDs that are free from a *p*-type contact. By inserting a tunnel junction, a *p*-type contact can be replaced by one that is *n*-type, leading to significant cuts in device resistance, voltage loss, and heating.

"Moreover, with the use of a polarization-engineered tunnel-junction interconnect, we have shown that multi-junction, phosphor-free nanowire LEDs can exhibit improved light intensity and reduced efficiency droop," adds Mi.

Although tunnel junctions are not new, it is challenging to incorporate them into nanowire LEDs with multiple active regions. To succeed in this endeavour, Mi and his co-workers produce a type of LED that would be incredibly challenging to realise with a planar structure. That's because the stacking of multiple quantum wells or dots in a planer structure leads to high densities of defects and dislocations, which together hamper low-current, high-voltage-operation. With the nanowire structures pursued by Mi and his team, defect densities are far lower.



Combining *p*-GaN up and *p*-GaN down tunnel-junction, dot-in-a-wire devices on the same silicon substrate enables the fabrication of LEDs that can be driven by an AC source

The researchers make devices by MBE, using their patented dot-in-a-wire LED technology. Commercial LEDs, meanwhile, are manufactured by MOCVD. "However, the growth of nanowire LEDs by MOCVD has been extensively studied by other universities and industrial labs," says Mi. "We believe these devices can be readily grown by MOCVD for production."

The researchers began by evaluating a range of devices: conventional InGaN/GaN dot-in-a-wire *p*-type GaN up LEDs; single-active region, tunnel junction dot-in-a-wire *p*-type GaN down LEDs; and two types of multiple-active region, tunnel junction dot-in-a-wire *p*-type GaN LEDs. One type of the latter emits at a single wavelength, and the other produces peaks in the red, the green and the blue.

Electroluminescence measurements show that the switch from a conventional dot-in-a-wire LED to that incorporating a tunnel junction results in a higher light intensity. The team attributes this to superior current-spreading through the low-resistance *n*-type contact, and improved hole injection inside the dots.

The tunnel-junction LEDs with a multiple active region that emits a single electroluminescence peak produce significantly more intense emission than those with a single active region. This is believed to result from repeated carrier regeneration at each tunnel junction, which results in an increase in the number of opportunities for radiative recombination.

The tunnel-junction LED that has different active regions produces peaks at 445 nm, 570 nm and 625 nm. An increase in injection current did not lead to a noticeable shift in wavelength.

AC LEDs were formed by turning to selective area growth. The researchers formed *p*-GaN up and *p*-GaN down tunnel junction, dot-in-a-wire devices on the same silicon substrate. The array of nanowires that resulted emitted green light for both positive and negative AC voltages. It is claimed that this is the first demonstration of LEDs that are formed on silicon and can be driven by an AC source.

Earlier this year, the team reported a 30 mW output from a single, non-packaged LED on silicon. They are now aiming for far higher values with structures incorporating tunnel-junctions.

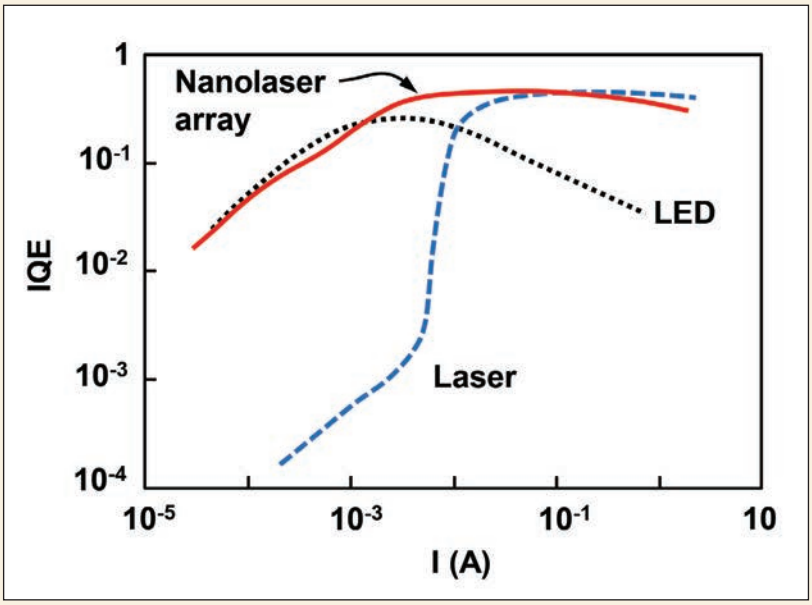
S. Sadaf *et. al.*
Nanoletters **15** 6696 (2015)

A better laser for lighting

A novel nanolaser delivers high optical efficiencies over a very broad range of currents

A VERSATILE, high-performance solid-state light source must deliver high wall-plug efficiency over a vast range of operating currents. Judged in these terms, LEDs are compromised by droop, the reduction in efficiency as the current through the device is cranked up; and lasers are thwarted by their poor performance below threshold.

But there is a device that can deliver a strong performance over a very wide range of operating currents, according to recent work by Weng Chow and Mary Crawford from Sandia National Laboratories. According to calculations by this duo, a nanolaser array can be almost as efficient as an LED at low current densities, and nearly match the efficiency of a laser at far higher current densities.



Unlike LEDs and VCSELs, a novel form of nanolaser produces high internal quantum efficiency over a vast range of drive currents

Chow and Crawford arrived at this conclusion after developing a single theory that is applicable to LEDs and lasers operating above and below threshold. This theory has been used to study three types of device: an LED without an optical cavity; a VCSEL with an optical cavity defined by distributed Bragg reflectors; and a nanolaser, which features a smaller optical cavity that provides further control of spontaneous emission.

Calculations for the efficiency of the LED are based on a device with a single, 2 nm-thick $In_{0.37}Ga_{0.63}N$ quantum well sandwiched between GaN barriers. By selecting such a simple structure, the duo from Sandia avoid complications arising from non-uniform carrier populations and the screening of the quantum-confined Stark effect. In their calculations, theorists incorporate a term that gives an onset of droop at around 10 A cm^{-2}. They argue that this value is reasonable, because it is consistent with the figure given in the work of Chris van de Walle's team from the University of California, Santa Barbara – they undertook first-principles calculations for phonon-assisted Auger scattering.

Simulations by the Sandia team were carried out for a 100 μm by 100 μm LED at 300 K. The performance limit of this device was determined by assuming 100 percent light-extraction efficiency and unity carrier injection, with the exception of Fermi blocking at high excitation.

Meanwhile, modelling of VCSELs considered a 3 by 3 array of devices with a 5.6 μm by 5.6 μm emitting cross section. This configuration, which has a 3 percent fill factor, was chosen because it produces a 1 W output at 1A.

The plot of VCSEL efficiency as a function of current supports the view that lasers are superior to LEDs once they have reached threshold (see figure). However, while the VCSEL may be ideal for high-power lighting, it is not necessarily suitable in general lighting applications, where dimmable lights enable energy savings.

Addressing this weakness is a novel class of nanolaser. It may be formed with photonic lattices or plasmonic cavities, and its key feature is the efficient channeling of spontaneous emission into the lasing mode. When there is a high degree of spontaneous emission (the spontaneous emission factor β is set to 1), the output power increases almost constantly with increasing current.

This level of linearity is highly valued, but it should be noted that the failure of the nanolaser to lase leads to a degradation of device performance, associated with the high level of absoption in the InGaN/GaN material system.

An alternative approach to using lasers for lighting would be to use an array of VCSELs, with just a fraction turned on at low powers.

"We now have LED lights with high and low intensity modes, depending on the number of LEDs that are switched on," says Chow, who points out that using nanolasers allows lower powers than a single VCSEL and simpler electronics, because there is no requirement for addressable current injection.

Chow is now working on extending his calculations to multi-mode operation of nanolasers.

W. Chow *et. al.*
Appl. Phys. Lett. **107** 141107 (2015)

HEMTs Oxygen plasma treatment eliminates the need for a GaN cap

If oxygen plasma treatment is used to address current collapse, the benefits of adding a GaN cap are negligible

ONE OPTION for improving the electrical performance of a GaN HEMT is to add a GaN capping layer. But this step has almost no benefit if devices are subjected to an oxygen plasma treatment, according to recent work by a Japanese team from the University of Fukui and Hokkaido University.

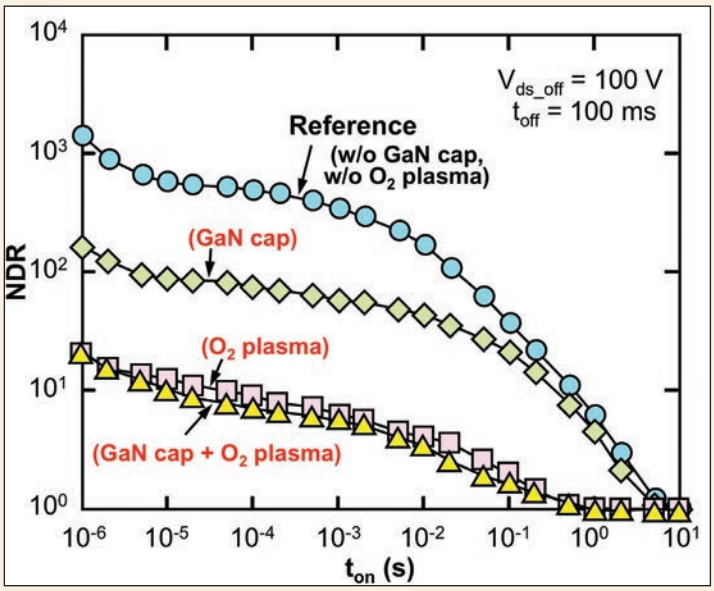
"Using oxygen plasma treatment of the surface alone, we can avoid problems associated with GaN cap layers, such as obtaining good ohmic contacts when using undoped GaN; and increased leakage, and the associated decrease in breakdown voltage, when using an *n*-type GaN cap," says corresponding author Joel Asubar from the University of Fukui.

There are also other drawbacks of an *n*-type GaN cap, says Asubar, such as inferior gate control of the current, which stems from an increase in the gate-to-channel distance.

To highlight the futility of incorporating a GaN cap in a GaN HEMT that has been subjected to plasma treatment, the team from Japan fabricated a range of devices and carried out a series of electrical measurements on them.

All devices were grown on SiC, and featured a 500 nm-thick layer of GaN, followed by a 25 nm-thick layer of $Al_{0.2}Ga_{0.8}N$. After source, drain and gate contacts were formed, sputtering added a 150 nm-thick SiN passivation layer.

Four types of device were formed, distinguished by whether or not they had been treated with an oxygen plasma for 60 s at a power of 100 W prior to SiN passivation, and whether or not they featured a GaN cap.



Oxygen plasma treatment is a very effective way to reduce current-collapse, which has been evaluated by considering the ratio of dynamic on-resistance to static on-resistance.

Cap-free devices with and without plasma treatment produced very similar values for maximum drain current density, threshold voltage, leakage current and breakdown voltage. This indicates that plasma treatment does not have a negative impact on the DC characteristics of the device.

The researchers also investigated current collapse in a range of devices, evaluating the ratio of the dynamic on-resistance to static on-resistance – the higher this value, known as the normalised dynamic on-resistance (NDR), the greater the current collapse.

Measurements on the uncapped structures revealed that oxygen plasma treatment mitigates current collapse (see figure).

These experiments also show that a GaN cap can combat current collapse, but this is not as effective as oxygen plasma treatment – and combining a GaN cap with oxygen plasma treatment produces only a very marginal improvement over just plasma treatment.

Further insight into the benefits of plasma treatment came from numerical modelling of the dependence of the NDR on the on-time of the device.

Simulations show that oxygen plasma treatment completely eliminates the two deepest trap levels, occurring at 0.62 eV and 0.67 eV, while the GaN cap only eliminates the deepest trap at 0.67 eV.

To understand the impact of plasma treatment, the researchers employed X-ray photoelectron spectroscopy to investigate the nature of the AlGaN surfaces.

They found that oxygen plasma treatment creates a surface oxide layer that is about 2 nm-thick, and probably contains a combination of Al_2O_3 and Ga_2O_3.

This finding led the team to conclude that the reduction in current collapse produced by oxygen plasma treatment results from the termination of near-surface gallium and aluminium atoms, and the probable occupation of nitrogen vacancies by oxygen atoms.

Asubar and co-workers are now aiming to realise true collapse-free operation with their GaN HEMTs. "We are planning to combine the oxygen plasma-treatment approach with other approaches against current collapse, such as the use of field plates."

J. Asubar *et. al.*
Appl. Phys. Express **8** 111001 (2015)

Optimising LEDs with tunnel junctions

Nanowires and tunnel junctions enable phosphor-free white light under AC power

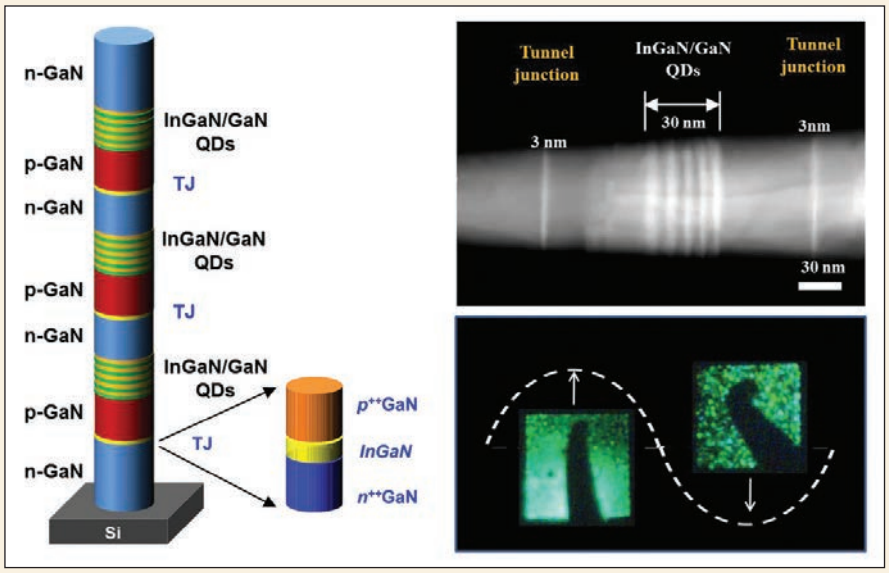
LEDs are a great source of lighting, combining high-efficiencies with long lifetimes and the ability to hit full brightness in an instant. But they also have their weaknesses: it is not possible to plug conventional devices directly into the mains; there are an internal losses associated with producing white emission via phosphor conversion; and there is droop, the decline in device efficiency at higher drive currents.

It is possible to address all these issues, however, with a novel LED architecture pioneered by Zetian Mi and co-workers from McGill University. This team has developed nanowire LEDs that, thanks to the incorporation of GaN-based tunnel junctions, can be driven by an AC source. These devices can feature red, green, and blue emitting sections, so avoid losses associated with pumping phosphors.

Mi believes that one of the most important aspects of this team's work is that it provides the first demonstration of InGaN/GaN nanowire LEDs that are free from a *p*-type contact. By inserting a tunnel junction, a *p*-type contact can be replaced by one that is *n*-type, leading to significant cuts in device resistance, voltage loss, and heating.

"Moreover, with the use of a polarization-engineered tunnel-junction interconnect, we have shown that multi-junction, phosphor-free nanowire LEDs can exhibit improved light intensity and reduced efficiency droop," adds Mi.

Although tunnel junctions are not new, it is challenging to incorporate them into nanowire LEDs with multiple active regions. To succeed in this endeavour, Mi and his co-workers produce a type of LED that would be incredibly challenging to realise with a planar structure. That's because the stacking of multiple quantum wells or dots in a planer structure leads to high densities of defects and dislocations, which together hamper low-current, high-voltage-operation. With the nanowire structures pursued by Mi and his team, defect densities are far lower.



Combining *p*-GaN up and *p*-GaN down tunnel-junction, dot-in-a-wire devices on the same silicon substrate enables the fabrication of LEDs that can be driven by an AC source

The researchers make devices by MBE, using their patented dot-in-a-wire LED technology. Commercial LEDs, meanwhile, are manufactured by MOCVD. "However, the growth of nanowire LEDs by MOCVD has been extensively studied by other universities and industrial labs," says Mi. "We believe these devices can be readily grown by MOCVD for production."

The researchers began by evaluating a range of devices: conventional InGaN/GaN dot-in-a-wire *p*-type GaN up LEDs; single-active region, tunnel junction dot-in-a-wire *p*-type GaN down LEDs; and two types of multiple-active region, tunnel junction dot-in-a-wire *p*-type GaN LEDs. One type of the latter emits at a single wavelength, and the other produces peaks in the red, the green and the blue.

Electroluminescence measurements show that the switch from a conventional dot-in-a-wire LED to that incorporating a tunnel junction results in a higher light intensity. The team attributes this to superior current-spreading through the low-resistance *n*-type contact, and improved hole injection inside the dots.

The tunnel-junction LEDs with a multiple active region that emits a single electroluminescence peak produce significantly more intense emission than those with a single active region. This is believed to result from repeated carrier regeneration at each tunnel junction, which results in an increase in the number of opportunities for radiative recombination.

The tunnel-junction LED that has different active regions produces peaks at 445 nm, 570 nm and 625 nm. An increase in injection current did not lead to a noticeable shift in wavelength.

AC LEDs were formed by turning to selective area growth. The researchers formed *p*-GaN up and *p*-GaN down tunnel junction, dot-in-a-wire devices on the same silicon substrate. The array of nanowires that resulted emitted green light for both positive and negative AC voltages. It is claimed that this is the first demonstration of LEDs that are formed on silicon and can be driven by an AC source.

Earlier this year, the team reported a 30 mW output from a single, non-packaged LED on silicon. They are now aiming for far higher values with structures incorporating tunnel-junctions.

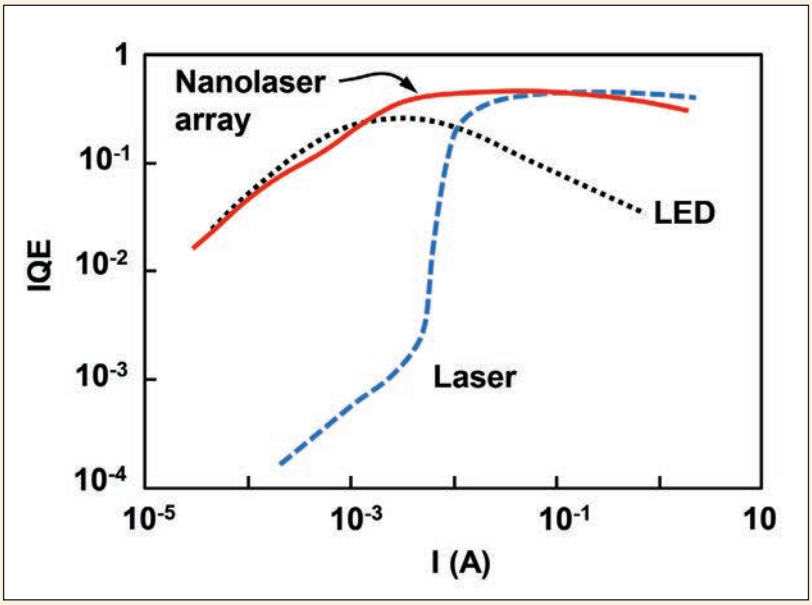
S. Sadaf *et. al.*
Nanoletters **15** 6696 (2015)

A better laser for lighting

A novel nanolaser delivers high optical efficiencies over a very broad range of currents

A VERSATILE, high-performance solid-state light source must deliver high wall-plug efficiency over a vast range of operating currents. Judged in these terms, LEDs are compromised by droop, the reduction in efficiency as the current through the device is cranked up; and lasers are thwarted by their poor performance below threshold.

But there is a device that can deliver a strong performance over a very wide range of operating currents, according to recent work by Weng Chow and Mary Crawford from Sandia National Laboratories. According to calculations by this duo, a nanolaser array can be almost as efficient as an LED at low current densities, and nearly match the efficiency of a laser at far higher current densities.



Unlike LEDs and VCSELs, a novel form of nanolaser produces high internal quantum efficiency over a vast range of drive currents

Chow and Crawford arrived at this conclusion after developing a single theory that is applicable to LEDs and lasers operating above and below threshold. This theory has been used to study three types of device: an LED without an optical cavity; a VCSEL with an optical cavity defined by distributed Bragg reflectors; and a nanolaser, which features a smaller optical cavity that provides further control of spontaneous emission.

Calculations for the efficiency of the LED are based on a device with a single, 2 nm-thick $In_{0.37}Ga_{0.63}N$ quantum well sandwiched between GaN barriers. By selecting such a simple structure, the duo from Sandia avoid complications arising from non-uniform carrier populations and the screening of the quantum-confined Stark effect. In their calculations, theorists incorporate a term that gives an onset of droop at around 10 A cm^{-2}. They argue that this value is reasonable, because it is consistent with the figure given in the work of Chris van de Walle's team from the University of California, Santa Barbara – they undertook first-principles calculations for phonon-assisted Auger scattering.

Simulations by the Sandia team were carried out for a 100 μm by 100 μm LED at 300 K. The performance limit of this device was determined by assuming 100 percent light-extraction efficiency and unity carrier injection, with the exception of Fermi blocking at high excitation.

Meanwhile, modelling of VCSELs considered a 3 by 3 array of devices with a 5.6 μm by 5.6 μm emitting cross section. This configuration, which has a 3 percent fill factor, was chosen because it produces a 1 W output at 1A.

The plot of VCSEL efficiency as a function of current supports the view that lasers are superior to LEDs once they have reached threshold (see figure). However, while the VCSEL may be ideal for high-power lighting, it is not necessarily suitable in general lighting applications, where dimmable lights enable energy savings.

Addressing this weakness is a novel class of nanolaser. It may be formed with photonic lattices or plasmonic cavities, and its key feature is the efficient channeling of spontaneous emission into the lasing mode. When there is a high degree of spontaneous emission (the spontaneous emission factor β is set to 1), the output power increases almost constantly with increasing current.

This level of linearity is highly valued, but it should be noted that the failure of the nanolaser to lase leads to a degradation of device performance, associated with the high level of absoption in the InGaN/GaN material system.

An alternative approach to using lasers for lighting would be to use an array of VCSELs, with just a fraction turned on at low powers.

"We now have LED lights with high and low intensity modes, depending on the number of LEDs that are switched on," says Chow, who points out that using nanolasers allows lower powers than a single VCSEL and simpler electronics, because there is no requirement for addressable current injection.

Chow is now working on extending his calculations to multi-mode operation of nanolasers.

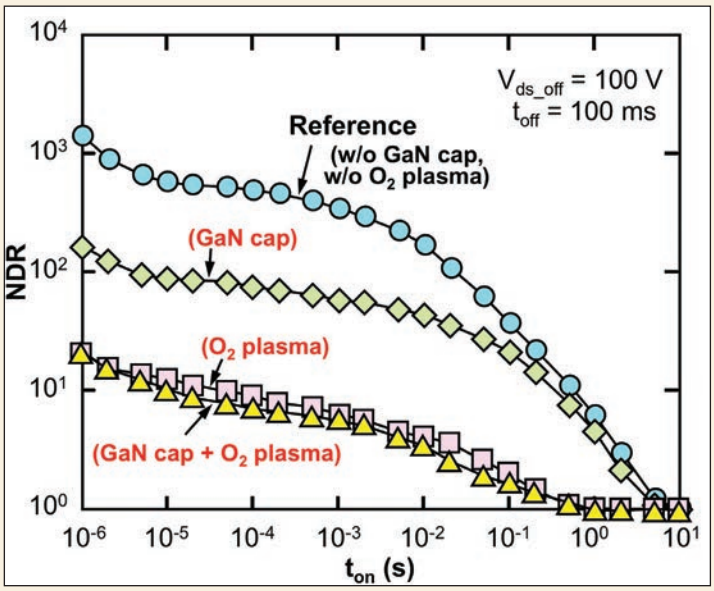
W. Chow *et. al.*
Appl. Phys. Lett. **107** 141107 (2015)

Oxygen plasma treatment eliminates the need for a GaN cap

If oxygen plasma treatment is used to address current collapse, the benefits of adding a GaN cap are negligible

ONE OPTION for improving the electrical performance of a GaN HEMT is to add a GaN capping layer. But this step has almost no benefit if devices are subjected to an oxygen plasma treatment, according to recent work by a Japanese team from the University of Fukui and Hokkaido University.

"Using oxygen plasma treatment of the surface alone, we can avoid problems associated with GaN cap layers, such as obtaining good ohmic contacts when using undoped GaN; and increased leakage, and the associated decrease in breakdown voltage, when using an *n*-type GaN cap," says corresponding author Joel Asubar from the University of Fukui.



Oxygen plasma treatment is a very effective way to reduce current-collapse, which has been evaluated by considering the ratio of dynamic on-resistance to static on-resistance.

There are also other drawbacks of an *n*-type GaN cap, says Asubar, such as inferior gate control of the current, which stems from an increase in the gate-to-channel distance.

To highlight the futility of incorporating a GaN cap in a GaN HEMT that has been subjected to plasma treatment, the team from Japan fabricated a range of devices and carried out a series of electrical measurements on them.

All devices were grown on SiC, and featured a 500 nm-thick layer of GaN, followed by a 25 nm-thick layer of $Al_{0.2}Ga_{0.8}N$. After source, drain and gate contacts were formed, sputtering added a 150 nm-thick SiN passivation layer.

Four types of device were formed, distinguished by whether or not they had been treated with an oxygen plasma for 60 s at a power of 100 W prior to SiN passivation, and whether or not they featured a GaN cap.

Cap-free devices with and without plasma treatment produced very similar values for maximum drain current density, threshold voltage, leakage current and breakdown voltage. This indicates that plasma treatment does not have a negative impact on the DC characteristics of the device.

The researchers also investigated current collapse in a range of devices, evaluating the ratio of the dynamic on-resistance to static on-resistance – the higher this value, known as the normalised dynamic on-resistance (NDR), the greater the current collapse.

Measurements on the uncapped structures revealed that oxygen plasma treatment mitigates current collapse (see figure).

These experiments also show that a GaN cap can combat current collapse, but this is not as effective as oxygen plasma treatment – and combining a GaN cap with oxygen plasma treatment produces only a very marginal improvement over just plasma treatment.

Further insight into the benefits of plasma treatment came from numerical modelling of the dependence of the NDR on the on-time of the device.

Simulations show that oxygen plasma treatment completely eliminates the two deepest trap levels, occurring at 0.62 eV and 0.67 eV, while the GaN cap only eliminates the deepest trap at 0.67 eV.

To understand the impact of plasma treatment, the researchers employed X-ray photoelectron spectroscopy to investigate the nature of the AlGaN surfaces.

They found that oxygen plasma treatment creates a surface oxide layer that is about 2 nm-thick, and probably contains a combination of Al_2O_3 and Ga_2O_3.

This finding led the team to conclude that the reduction in current collapse produced by oxygen plasma treatment results from the termination of near-surface gallium and aluminium atoms, and the probable occupation of nitrogen vacancies by oxygen atoms.

Asubar and co-workers are now aiming to realise true collapse-free operation with their GaN HEMTs. "We are planning to combine the oxygen plasma-treatment approach with other approaches against current collapse, such as the use of field plates."

J. Asubar *et. al.*
Appl. Phys. Express **8** 111001 (2015)

EVG®

invent
innovate
implement

www.EVGroup.com

Solutions for

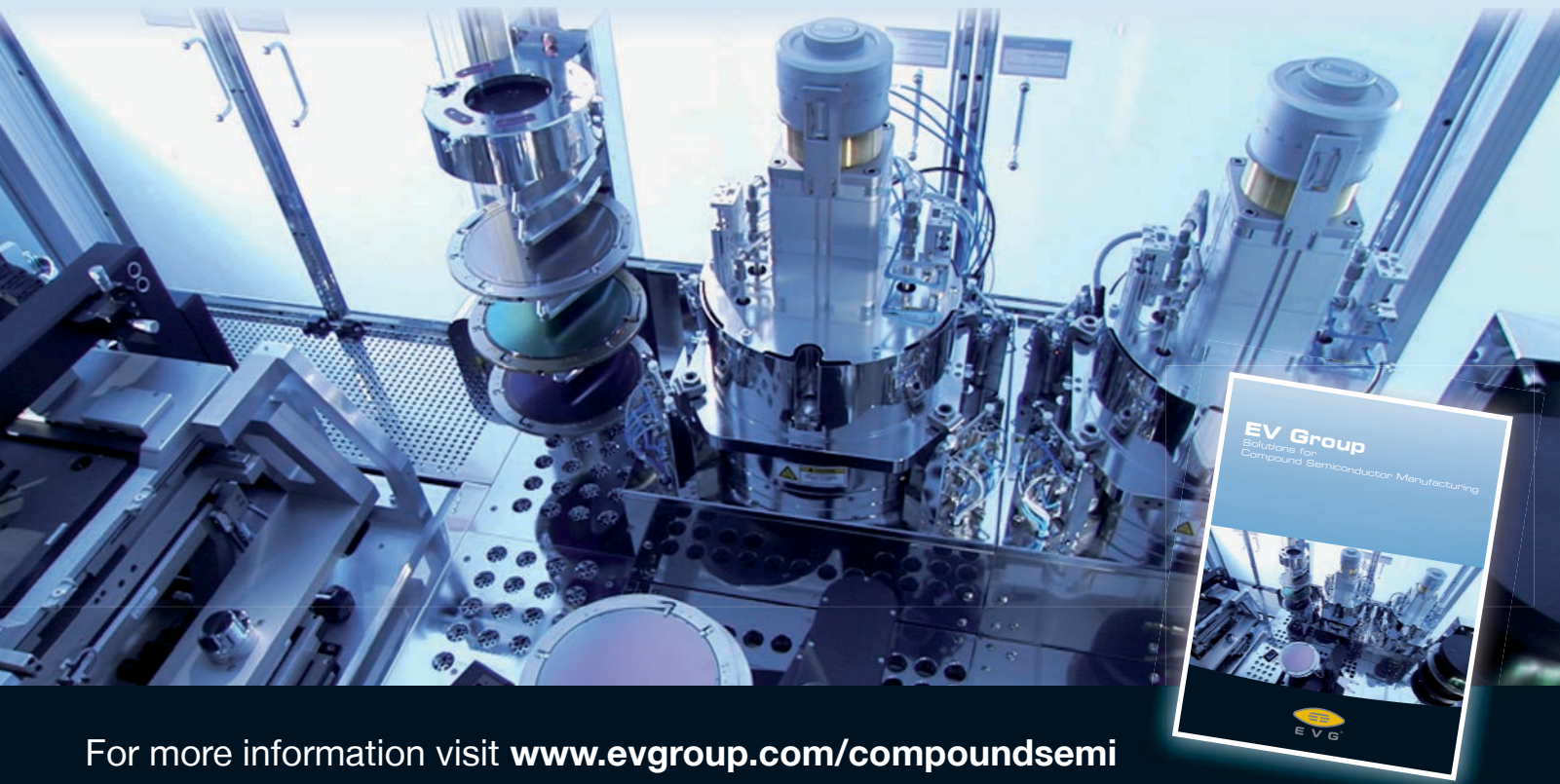
COMPOUND SEMICONDUCTOR MANUFACTURING

Wafer Bonding
for Heterogeneous Integration, Layer Transfer and Advanced Packaging

Optical and NanoImprint Lithography
for Device Patterning and Advanced Packaging

Advanced Resist Processing
for Dielectrics, Thick / Thin Resist Layers, Through Vias and High Topography

Temporary Bonding and Debonding
of Thinned and Fragile Compound Semiconductor Substrates



For more information visit **www.evgroup.com/compoundsemi**

CORPORATE PARTNERS DIRECTORY

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

KITEC
Non Contact Measurements
Resistance, Resistivity
Wafer Thickness
Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

Temescal
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

EPIGAN
Email: info@epigan.com
www.epigan.com

LAYTEC
Knowledge is key
Tel. No.: +49 (0) 30 89 00 55 0
Fax No: +49 (0) 30 89 00 55 180
e-mail: info@laytec.de
website: www.laytec.de

Lake Shore CRYOTRONICS
ADVANCING SCIENCE
Tel: +1 614 891 2244
Fax: +1 614 818 1600
Email: info@lakeshore.com
www.lakeshore.com

HIDEN ANALYTICAL
Tel: +44 [0] 1925 445225
Fax: +44 [0] 1925 416518
Email: info@hiden.co.uk
www.hidenanalytical.com

OXFORD INSTRUMENTS
The Business of Science®
Tel: +44 (0)1934 837000
Fax: +44 (0)1934 837001
Email: plasma.technology@oxinst.com
www.oxford-instruments.com

WATLOW®
www.watlow.com

Meister Abrasives
Tel: +41 52 304 22 00
Fax:+41 52 304 22 12
Email: info@meister-abrasives.ch
www.meister-abrasives.ch

化合物半导体 CHINA
Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

TYSiC
1st SiC-epi Foundry in China
Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

III/V-Reclaim
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.de

GATAN
Tel: +1 925 224 7355
Email: pmartineau@gatan.com
www.gatan.com

UMC UNITED MINERAL & CHEMICAL CORP.
MBE Specialists
Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

kSA k-Space Associates, Inc.
Thin-Film Characterization
Tel: +1 734-426-7977
e-mail: requestinfo@k-space.com
www.k-space.com

BACH·RC
Tel: +49 33398 696592
Fax: +49 33398 696594
Email: jp@bachrc.de
www.bachrc.de

NANO-MASTER
Cleaning • Deposition • Etching
Tel: +1 512-385-4552
Fax: +1 512-385-4900
Email: r.andrade@nanomaster.com
www.nanomaster.com

evatec
process systems
Tel: + 41 81 720 1080
Fax: 41 81 720 1161
www.evatecnet.com

Vistec
Electron Beam
Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

Fil-Tech, Inc.
Savings on Quality Vacuum and Coating Supplies
Tel: +1 617-227-1133
Fax: +1 617-742-0686
Email: paula@filtech.com
www.filtech.com

BRUKER
Tel: +49 721 50997-0
Fax: +49 721 50997-5654
www.bruker.com

Instrument Systems
light measurement
Tel: +49 (089) 45 49 43 - 0
Fax: +49 (089) 45 49 43 - 11
Email: info@instrumentsystems.com
www.instrumentsystems.com

Veeco
Tel: 516-677-0200-1222
Fax: 516-714-1231
Email: jpina@veeco.com
www.veeco.com

Submit your **Lab & Fab** article

Research is the foundation for the growth of the compound semiconductor industry.

If you want to highlight the important breakthroughs that you make, submit your latest research stories to **RichardStevenson@angelbc.com**

It is imperative that Compound Semiconductor remains a timely resource for this industry, so we are only interested in highlighting very recent work reported in academic papers.

Therefore, please only consider writing a short piece highlighting your work if you have a journal paper that has been accepted and about to appear in press, or a paper that has been published within the last month.

COMPOUND SEMICONDUCTOR
Connecting the Compound Semiconductor Community

www.compoundsemiconductor.net

Shattering the Barriers to Mainstream GaN Adoption

Only MACOM offers the portfolio, partnerships & people to fully leverage GaN technology in a wide range of commercial applications such as medical ablation, microwave oven magnetron replacement, plasma lighting and RF energy transfer.

We're shattering the final barriers to mainstream GaN adoption with an industry-leading portfolio of cost-effective RF power devices available in Si and SiC. Our GaN transistors and amplifiers improve upon the high-power handling and voltage operation of LDMOS with the high-frequency performance of GaAs.

Our growing product family delivers the cost, bandwidth, density and efficiency advantages of GaN in a variety of form factors—5W-90W Pk transistors in DFN and SOT-89 plastic packaging, up to 1000W ceramic packages and L-, S-band fully matched modules. We also offer ceramic GaN on silicon transistors up to 200W, DFN packages from 5W to 25W and TO-272 plastic packages from 50W to 200W CW.

For over 40 years, MACOM engineers have been redefining RF power and are now applying their GaN expertise to an array of commercial, industrial, scientific, medical and wireless backhaul applications. Only MACOM delivers GaN performance at silicon cost structures to drive adoption.

MACOM™

Partners from RF to Light

Learn more and get samples:
www.macom.com/gan