COMPOUND SEMICONDUCTOR

November 2007 Volume 13 Number 10

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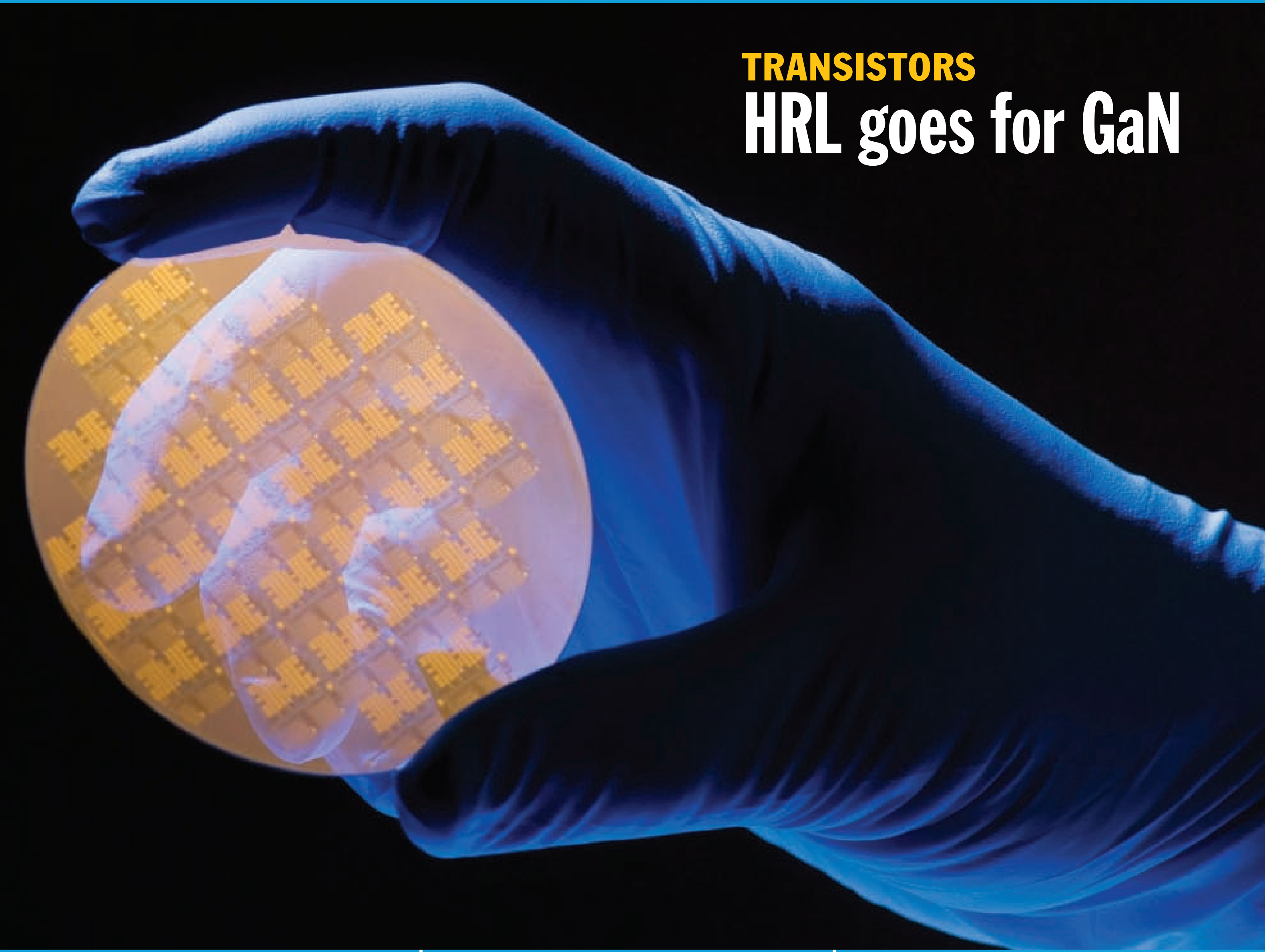

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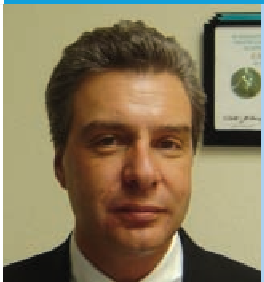

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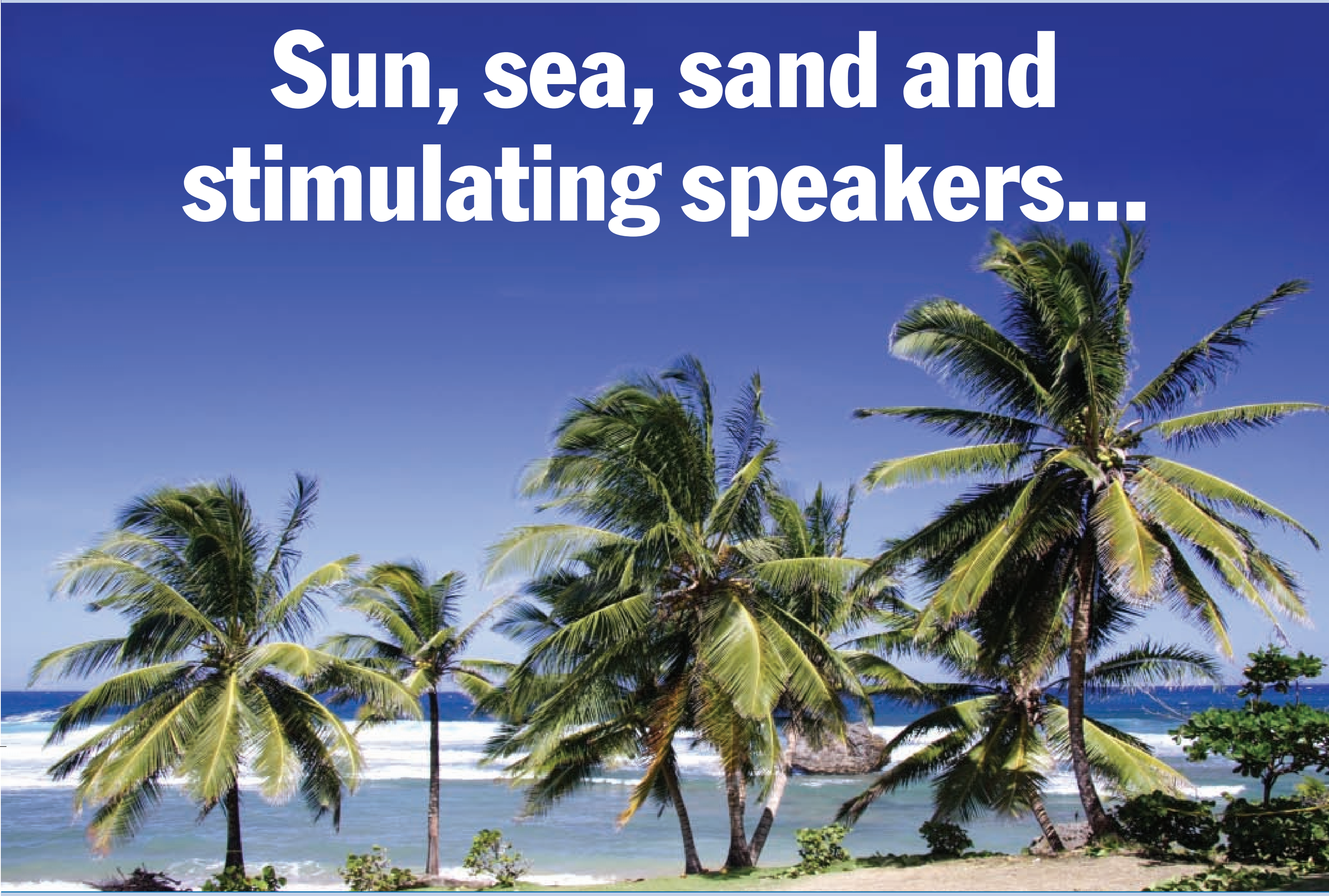
Sun, sea, sand and stimulating speakers...



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- **Craig Cornelius** (Solar America Initiative)
- **Alexei Erchak** (Luminus Devices)

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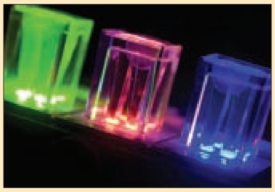
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Nitrides were on the agenda in September at the massive MGM Grand Hotel in Las Vegas. **p17**

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Main cover image: *GaN-based RF transistors on a wafer produced by HRL in Malibu, California. The company believes that the chips would open up a niche in wireless communications. See p21. Credit: HRL.*

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EDITORIAL

Economies of scale

The economies of China and India have been revolutionized over the past couple of decades – China's largely through manufactured goods and India's through information technology and telecommunications.

That transformation has, of course, included the silicon semiconductor industry. First China and latterly India have become important chip-manufacturing locations. But Taiwan apart, their impact on compound semiconductor fabrication has been more muted.

China's role in the compounds industry is somewhat complex. On the one hand, it might be widely regarded as a vast packaging center, with a sprinkling of commodity chip and epiwafer manufacturing. But on the other hand, you could argue that the Chinese government is leading the world towards a solid-state lighting revolution, among the first to recognize the huge role that semiconductor technology can play in reducing energy consumption and increasing energy security.

Thanks to its central government's energy strategy, some key LED manufacturing locations have sprung up in China over the past few years. But now things are really starting to happen and last month's official opening of Century Epitech in Shenzhen marked a key moment in the evolution of mainland China's III-V story.

"China's role in the compounds industry is more complicated."

The scale of this "compound semiconductor base" is nothing short of enormous. With the first stage completed, the site is focused on epiwafer fabrication right now. But, over the next five years, it will grow into an entire supply chain – ranging from materials research right through to packaged devices – ready to serve the needs of its host country.

That five-year plan is not just about LEDs. Century aims to make microwave components, laser diodes, solar cells and more. Nor is it solely to serve China's needs, with a senior figure involved in the project saying that there is a strong desire to work with companies from the West.

While China marches forward, India has barely begun any kind of compound semiconductor effort. Happily, that is now changing, although not because of any government-led strategy. Dhrubes Biswas, a technologist who helped to establish Anadigics' groundbreaking 6 inch GaAs wafer facility, is now setting up a III-V development center at the Indian Institute of Technology in Kharagpur. We wish him every success.

Michael Hatcher *Editor*

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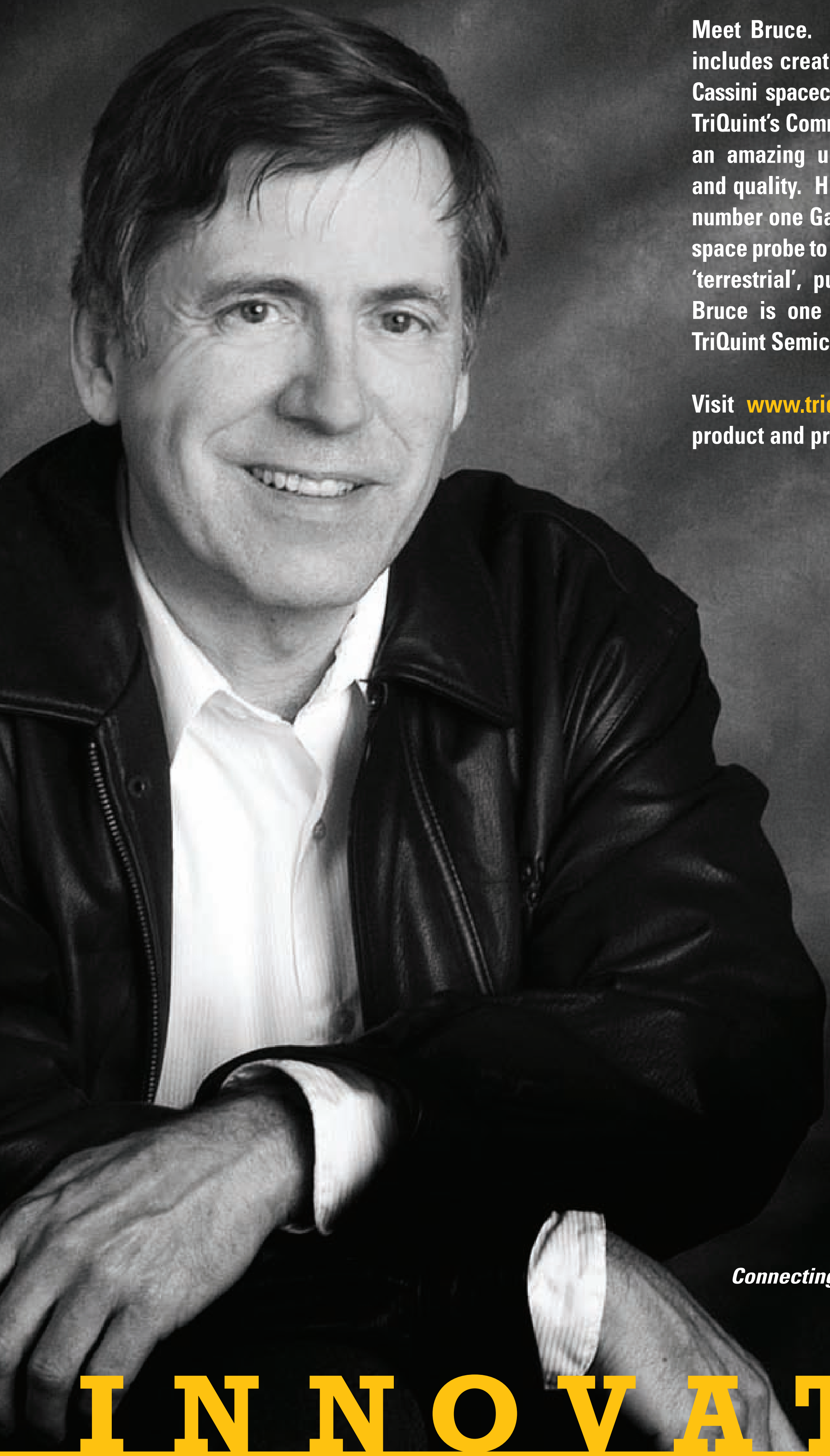


CHINA

Giant Shenzhen facility is inaugurated

By Michael Hatcher

Government officials in China have celebrated completion of the first stage of a massive compound semiconductor epiwafer and chip-production base in Shenzhen.

The base is called Century Epitech Company Ltd and development of the sprawling site has the twin backing of the central Chinese government and the Hong Kong financial group Sunbase.

Gao Jingde, the Century Epitech chairman, describes the site at the Guangming Hi-tech Industrial Park as China's "only all-round compound semiconductor industrial base". Spreading over an enormous 3 km^2, this site will eventually incorporate five individual zones, of which the epiwafer fab, now said to be up and running, is the first.

Target technologies include major compound semiconductor applications, from research and development of core materials, through to chip and module production.

One of the base's five zones is focused on optoelectronics, including white LEDs for solid-state lighting, as well as laser diodes for optical data storage and communications. Another zone will be dedicated to microwave communications, while the remaining site areas are reserved for administration, and a conference and exhibition center.

Complete with bunting and fireworks, the completion of the first stage of the development was celebrated on October 11. According to Jacob Tarn, the general manager of fiber-optic component company Optical Communication Products' Asian unit, and also a senior figure in the Shenzhen development, solar cells and high-power laser diodes for industrial machining applications are other key applications.

Driven by China's demand for energy-efficient lighting, III-V production at Century Epitech looks set for a huge expansion. Tarn told *Compound Semiconductor* that, within five years, the base will rival key LED manufacturer Epistar in terms of its sheer epiwafer production scale. "There is a huge market in China for LEDs and energy production," Tarn said. "[This development] is strongly supported by the central government and is very important to China."

According to the official Century Epitech website, the total investment planned for the Shenzhen base will be a remarkable ¥32 billion yuan ($4.3 billion). The epiwafer-focused initial phase that has just been completed is itself the result of a ¥3 billion yuan investment and signals China's enormous commitment to compound semiconductor technologies.

RFICs

RFMD expands again with 6 inch GaAs fab

RF Micro Devices is building a $103 million fab to produce highly integrated GaAs power amplifier (PA) chips for miniaturization-motivated cellphone makers.

The expansion will provide the PA maker with the capacity to produce wafer-level packaged surface acoustic wave filters and the ability to develop next-generation process technologies.

"Our next-generation technologies will include those that afford single-chip integration of power amplifier, switch, low-noise amplifier and control necessary for integrated front-end products in cellular and WiMAX applications," the company told *Compound Semiconductor.*

The facility is intended to be production capable by summer 2008 and will be sited in Greensboro, NC, separated from RFMD's existing campus. Initially it will employ 100–150 additional employees, but this will ultimately increase to more than 300.

The new fab will be the company's second 6 inch post-epitaxial wafer processing line, on top of existing 4 and 6 inch GaAs fabs and its separately housed MBE facility. RFMD will be spending more money on processing equipment for photolithography, metallization, wafer dicing and other fabrication steps.

"The fab will accommodate rolling capacity expansion, which will track market demand," the company said. "The initial equipment investment will be below $100 million but could exceed twice that amount prior to reaching the facility floor space capacity maximum."

DEVELOPMENT

Indian institute gets $12 m for epitaxy kit

By Andy Extance

The Indian Institute of Technology (IIT) in Kharagpur is setting up a semiconductor nanogrowth facility featuring MBE and MOCVD equipment for III-V device development.

A $12 million government fund was awarded specifically to Dhrubes Biswas, an RF compound semiconductor expert, whose lengthy resumé includes establishing the first 6 inch GaAs HBT process at US-based Anadigics.

Now CTO and professor of electronics and electrical communication engineering at Kharagpur, Biswas told *Compound Semiconductor* that this money was primarily for RF front-end development.

"In India, we have about 100 design companies in Bangalore, but none of them work in III-V," Biswas observed. "My role as IIT's CTO is to motivate them into getting into front end, where compound semiconductors can have an impact, using our lab to give them prototypes."

Awarded the money earlier this year, Biswas is buying MBE and MOCVD equipment to install at IIT Kharagpur's existing very-large-scale integration electronics lab.

In the two years since he joined IIT Kharagpur, Biswas has already introduced III-As, III-P and SiGe processing to its highly reputed electronics facility. This has been achieved in conjunction with a consortium of 14 companies, including Intel, Texas Instruments, National Semiconductor, Agilent and Analog Devices.

"I am on a quest to get a research innovation lab in IIT as well," Biswas said. "I got the first $12 million for the epi part; now I am trying to get $50 million for the remainder of the process. We will end up with a complete innovation fab out of IIT Kharagpur that can make products using our design expertise for the local globalized business industry out of Bangalore, Hyderabad or Delhi."

He continued: "I've been dealing with compound semiconductors all through my life and what I really want now is for people in India to understand III-Vs more, use them, build them locally and create a global business out of it."

POWER AMPLIFIERS

Jazz plays up RF silicon process

Jazz Semiconductor looks set to challenge the dominance of compound semiconductors in integrated single-chip power amplifiers (PAs) with a low-cost radio platform provided on a single piece of silicon.

The Californian foundry has moved its RF process up a notch by shrinking gate lengths from 0.35 to 0.18 µm and developing silicon-on-insulator (SOI) capabilities. SOI allows the inclusion of an antenna switch for the first time, alongside a SiGe or CMOS PA, a SiGe-based low-noise amplifier and a passive module.

"We have put all four elements of a radio into a single piece of CMOS silicon and now we can be more effective at attacking GaAs PAs and switches," said Chuck Fox, Jazz's director of sales and marketing.

Eight-inch RF wafers made this way are already available from Jazz. The company says that its process can reduce die cost by 50% over GaAs. The company used European Microwave Week, held in Munich in early October, to put forward its claims.

Despite the aggressive bid to gain share in the RF market, Fox admits that Jazz still has work to do. "I would say that the integrated silicon radio isn't going to meet all of the requirements for power and linearity today, but it will meet some," he conceded. "We can meet the 802.11n, WiMAX and just about all of the wireless LAN standards. The cellular standards, we expect to be able to meet in the first quarter of 2008. We understand that the GaAs market for PAs isn't going to suddenly go away and let silicon take over in six months. It will take several years for that to happen."

The principal fronts on which Jazz is fighting the PA war involve convincing designers that a silicon technology can do the job and helping them to understand how to use it.

"Single-chip silicon is a scary road to go down because there's not a lot of evidence that it can be done and the design gets more complex," Fox explained. "We help the RF designer, hold his hand, give him a lot of information so that it's not so scary and show him how you really can do an integrated CMOS-silicon solution."

To provide some of that missing evidence, Jazz is currently measuring linearity and noise performance on its own wafers, and it recognizes that these figures will hold the key to the ultimate success of its silicon PAs in handsets.

"We are very bullish on the cellular standards, but the bar is very high," Fox said. "Just walking in with a PowerPoint presentation doesn't cut it for the cellular guys. They want to see data from real silicon and those measurements are in process now."

● SiGe Semiconductor has released a highly integrated front end for 802.11n Wi-Fi.

WIDE-BANDGAP TRANSISTORS

Toshiba set to ramp GaN HEMT

Toshiba has produced a GaN HEMT with an output power of 65.4 W at 14.5 GHz, which it hopes will replace competing electron-tube technologies in satellite communications.

According to the Japanese company, this is the highest power-output FET to operate in the 12–18 GHz K$_u$-band of the microwave spectrum. Revealed at European Microwave Week in Munich, in early October, the device will be sampled at the end of 2007 and should enter mass production in March 2008.

The GaN HEMTs will be marketed for high-capacity, high-definition satellite broadcasting base-stations and high-power radar systems, which both require high-power amplifiers. "Demand is particularly strong for GaN devices, which offer advantages over GaAs devices in heat dissipation and high-power performance characteristics at high frequency," Toshiba said.

The HEMT's designers ensured high rates of heat conduction by growing AlGaN and GaN layers on a thermally conductive SiC substrate. The circuit design was also configured to be highly heat dissipative.

Via holes from the surface source electrodes to the backside ground electrode are used to reduce parasitic inductance in the device. Making vias through SiC is a challenging process, so forming them in these HEMTs was a breakthrough for Toshiba.

The 3.4 × 0.53 mm GaN chip measures 21.0 × 12.9 mm in its packaged form and offers a linear gain of 8.2 dB. Such modest proportions offer the GaN device an advantage over its bulkier electron-tube competitors.

However, klystron and traveling-wave electron-tube microwave amplifiers can offer kilowatt power outputs that remain beyond the reach of these individual FETs.

RF DESIGN

WIN, Plextek form bespoke team

WIN Semiconductor has chosen UK-based Plextek as its approved design partner and says that the collaboration can provide customized RF circuits more cheaply than rival integrated device manufacturers (IDMs).

The formal partnership was conceived at June's Microwave Theory and Techniques Society show, better known as MTT-S, as an extension of an existing collaboration.

Plextek had already designed MMICs for clients using WIN's process and the companies are now working on custom GaAs circuits for an unnamed maker of versatile cross-market subsystems.

The combined approach sees the circuits designed at Plextek's Great Chesterford, UK, site and realized at WIN's Taiwan fab. Liam Devlin, Plextek's director of RF integration, told *Compound Semiconductor* that the collaboration offers customers two main benefits. "One is that they can have an IC that meets their functional requirements exactly, they don't just have to buy a part off the shelf that is the closest to what they need. The second benefit is cost. If you take the price of a wafer and divide that by the number of ICs you have, that's quite a lot cheaper than you can buy from an IDM."

Plextek works with a number of compound semiconductor foundries, including TriQuint and GCS, and says that the number of ICs that a customer wants will drive the decision about which foundry to use.

WIN's four-in-one multiproject technology allows four customers to share a mask set. Each customer is allocated one-quarter of the reticle that contains the photomask design data. This keeps costs low for prototype IC fabrication.

"When WIN makes the wafers, they step-and-repeat your quarter of the reticle across one wafer, somebody else's quarter of the reticle across another wafer, so each wafer in the batch will have a unique set of circuits for one client," Devlin explained. "In this way, they can deliver one complete wafer with just your circuits on, but still give you the multiproject wafer cost savings."

The two companies are currently seeing most enquiries from companies wanting high-data-rate GaAs circuits with WIN's capabilities also well suited to millimeter-wave communications.

To date, all of the companies joining the WIN-Plextek collaboration have come from outside the US, although Devlin made it clear that this was not intentional.

Instead it seems that a collaboration of non-US companies avoids US-specific laws collectively called International Traffic in Arms Regulations (ITAR). These control the export and import of items deemed to be defense related.

"There are certain functions that are on the ITAR list of controlled components," Devlin commented. "Which functions and components fall into ITAR regulations is becoming broader as time goes on, and some people are a little wary of using US foundries because of these export restrictions."

SUBSTRATES

Cellular surplus hits sales at Hitachi Cable

Hitachi Cable's GaAs epiwafer sales in the first fiscal quarter of 2008 have slumped below the previous year's, as weak demand filters down from the handset market.

"Sales of compound semiconductors fell from the first quarter of the previous fiscal year, as sales for use in high-frequency devices were sluggish," the company said in its quarterly report. A spokesperson for the wafer manufacturer said that this fall was caused by excess inventory in the cellular business and that demand should rebound in the second half of the year.

GaAs power-amplifier makers TriQuint and RF Micro Devices have also suffered from excess inventory as a result of a downturn in business at Motorola. TriQuint had to write off $3 million of stock.

In total, Hitachi Cable's sales of compound semiconductor products in the quarter that ended June 30 came to ¥3.5 billion ($30.3 million), deriving primarily from GaAs wafers.

Sales of GaN wafers are yet to make a significant contribution and the company is not yet producing its ground-breaking 3 inch GaN substrates in production quantities.

Its sales are divided roughly between LED-making customers, laser firms and companies producing other devices, including high-frequency electronics.

The Japanese firm's revenues are dominated by sales to its domestic market. However, local power-amplifier manufacturers have dropped out of the current industry top-10 list, which could put more pressure on Hitachi Cable's revenues.

SOLID-STATE LIGHTING

Craford bags an innovation prize

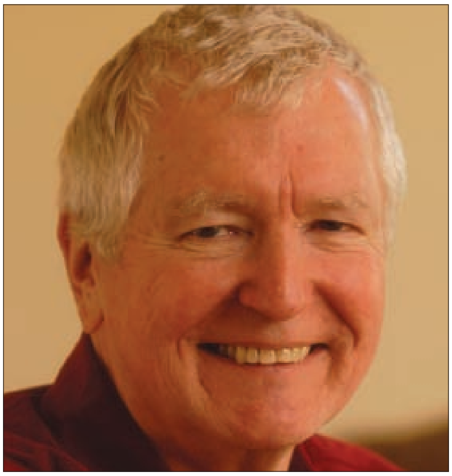
Veteran LED technologist George Craford has stressed the importance of improving the internal quantum efficiency (IQE) of InGaN-based LEDs to ensure that solid-state lighting fulfills its commercial potential.

The Philips Lumileds CTO visited London in mid-October to pick up an award for innovation in energy and the environment from *The Economist* magazine. He told *Compound Semiconductor* that although the solid-state lighting revolution is "beginning to happen", there is still a critical need to develop emitters that maintain a very high IQE at high current densities.

"There's no longer any question that LEDs will take over," Craford said, although it is only within the past 12 months that he has become convinced of this.

The big question that remains, however, is exactly how technologists will crack the problem of reduced IQE at high current densities, although Craford believes that a team from Philips Lumileds has now identified the key to that particular problem.

According to the team's photoluminescence study of InGaN material, it is the phenomenon of Auger recombination that causes the drop-off in IQE at high current densities. Previously, the problem – sometimes referred to as droop – has been attributed to other mechanisms, such as high plasma temperatures, a high density of threading dislocations or pockets of InGaN material with a high InN composition.


PHILIPS LUMILEDS

Winning vision: Lumileds' CTO George Craford was honored for innovations in LED development.

If Craford's colleagues are right and Auger recombination is the root cause of this droop, it may help to solve a long-standing problem in the development of very-high-brightness blue, green and white LEDs.

Craford's hunch is that evolutionary developments in LED design that increase the carrier recombination volume, such as thicker structures, could now lead to devices suitable for general lighting applications and perhaps to a conventional 1 mm scale chip capable of emitting 500 lm.

"I hope that we don't have to do something radically different," said the CTO.

RESEARCH

Picogiga receives European funds

Compound semiconductor epiwafer maker Picogiga and its silicon-on-insulator (SOI) focused owner Soitec have gained €62 m ($88.6 m) to develop substrates.

The funds are part of the European Union's Nanosmart strategic research program, under which Picogiga will develop substrates for GaN-based high-brightness white LEDs.

"Advanced substrates for III-V applications will involve GaN, either to improve the quality of active layers of devices or to simplify device integration," Picogiga said.

The second major theme of Nanosmart focuses on high-mobility substrates, which will enhance carrier mobility by integrating germanium into CMOS and optimizing crystal orientation.

In its third theme the program will develop SOI substrates for specific applications, particularly for CMOS and power devices.

All three themes will take advantage of Soitec's Smart Cut technology, in which ultra-thin single crystal layers of wafer substrate are transferred onto another surface.

The Nanosmart program is worth €200 m in total, which Bernin-based Soitec will split with the French CEA/Leti government electronic research institute in Grenoble.

The program will proceed over five years. The funds are made up of €80 m from the European Union and €120 m from the French government.

Soitec and Picogiga's €62 m is made up of a €34 m direct subsidy and a €28 m advance, which may need to be paid back, depending on the success of the project.

DISPUTE

Epistar imports are banned again

The US ban on imports of Epistar's omnidirectional mirror adhesion, metal- and glue-bonded LEDs has been restored.

California-based LED manufacturer Philips Lumileds has gained the upper hand in its long-running court battle with its rival, thanks to a ruling that prevents the Taiwanese company's imports to the US.

The US Court of Appeals for the Federal Circuit (CAFC) has removed its temporary freeze on the US International Trade Commission's (ITC) decision to prohibit the import of Epistar's omnidirectional mirror adhesion (OMA), metal-bonded (MB) and glue-bonded (GB) products.

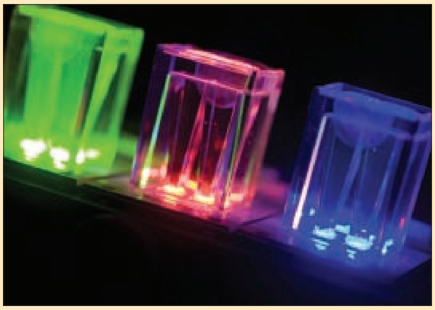
However, Epistar says that US Customs and Border protection has ruled that its Phoenix and Aquarius AlGaInP LEDs are not subject to the import ban.

Lumileds does not agree with this claim and said in a statement: "Discussions with US Customs have confirmed that the agency has issued no such order and has neither cleared the Phoenix or Aquarius LEDs for importation nor found that they do not infringe Philips Lumileds' 718 patent."

According to Lumileds, the exclusion order prohibits the import of Epistar's OMA I, OMA II, MB I, MB II, GB I and GB II LEDs; any products infringing its US patent 5,000,718; packaged LEDs containing Epistar's infringing LEDs; and boards consisting primarily of packaged LEDs.

"Companies that use, import or sell these unlicensed infringing products, even unknowingly, are direct infringers of Philips Lumileds' patent and are subject to the exclusion order," continued the US company in its statement.

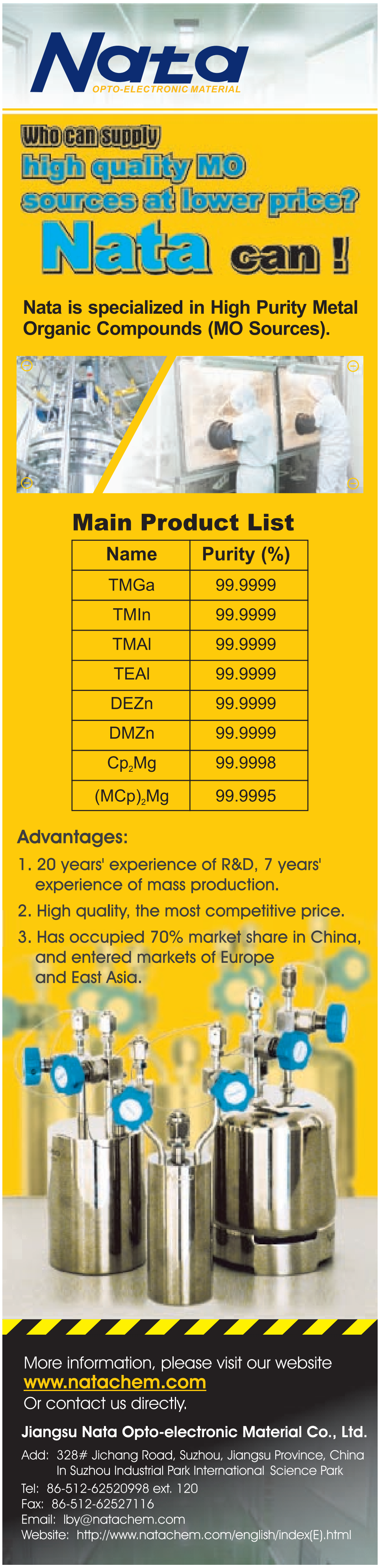
Epistar is attempting to overturn the decision and has lodged an appeal with the CAFC. "Epistar has always maintained that the ITC decision was incorrect, both factually and legally," said Epistar president BJ Lee. "We look forward to the opportunity to present our case to the US appeals court."



OSRAM OS

A team from Osram Opto Semiconductors in Germany has been nominated for the German Future Prize. Now in its 11th year, the prize is conferred by the German federal president for outstanding scientific and technical achievement. The award will be presented by President Horst Köhler on December 6. Three of Osram's high-brightness O-Star LEDs are shown here.

The team nominated includes Stefan Illek and Klaus Streubel from Osram, and Andreas Bräuer from the Fraunhofer Institute for Applied Optics and Precision Engineering. They were key players in the development of thin-film LED structures in which the original substrate material is removed, to increase the total light emitted from the top of the device.



FIBER-OPTICS

CyOptics looks to hybrid chips

InP optoelectronics specialist CyOptics and silicon photonics pioneer Kotura are to collaborate on a $12.7 million, three-year project to develop photonic circuits known as TeraPICs, for terabit-scale optical communications.

The two chip firms are working under an advanced technology program (ATP) award from the US National Institute for Standards and Technology, which has supplied funding of $6 million to support the effort.

Stefan Rochus, TeraPICs' principal investigator and also vice-president of marketing and business development at CyOptics, says that the ultimate aim of the project is to deliver 1 Tb/s connection speeds over one singlemode optical fiber.

CyOptics has already made some progress with photonic integrated circuits (PICs), thanks to a previous project supported by the supercomputer builder Cray and the US Defense Advanced Research Projects Agency (DARPA).

Under DARPA's high-productivity computing systems program, CyOptics began developing 80 Gb/s transmit and receive optical subassemblies, and it has also done some experiments on integrating InP optoelectronics into a silicon platform – a key element of the latest project.

"Without ATP funding, TeraPICs would probably be delayed by about 2–3 years," Rochus told *Compound Semiconductor.*

A fundamental aim of the TeraPICs effort is to cut down the number of individual components required for terabit-per-second communication, reducing the cost of such a platform. Key to this will be CyOptics' highly automated assembly and packaging capability, which should provide high manufacturing yields and low overall costs.

In terms of the key technical challenges presented by the aims of the project, Rochus says that some innovation in InP epitaxy will be required to grow monolithic arrays of uncooled electroabsorption modulated lasers. These emitters must operate over a wavelength span of 80 nm, with high output-power maintained across all wavelengths.

Integrating these InP components into silicon waveguides without losing too much power through coupling and insertion losses also presents a serious technical challenge.

While PICs are not a new concept (Infinera and recently JDSU both have commercial products based on the technology), the approach taken by CyOptics and Kotura is fundamentally different, Rochus says. "Infinera has developed monolithically integrated transmitter and receiver PICs in InP for dense-wavelength division multiplexing applications. These designs are targeted at optical transport applications and longer reach, and they require thermo-electric coolers (TECs)." TeraPICs, on the other hand, will be for shorter-reach applications of up to 2 km, with the potential for 10 km. They will use coarse-wavelength division multiplexing and don't need TECs," he added.

If successful, the TeraPICs will be smaller, lower in power consumption and lower in cost, Rochus says. He does not envisage that PIC production will lead to any major changes to InP wafer processing in the future, but does suggest that when TeraPICs become a volume driver, there will be a need to move to 3 or even 4 inch wafer diameters.

PHOTOVOLTAICS

Cyrium start-up adds quantum-dot junction

Early-stage III-V solar cell company Cyrium Technologies is using InAs/GaAs quantum-dot layers to convert light into electricity more efficiently than existing multi-junction devices can.

Within the quantum-dot layer of Cyrium's cells, the effective bandgap can be tuned to absorb light from 885 to about 1350 nm. This coincides with the region of the spectrum in which light is least effectively absorbed by current triple-junction devices.

Despite having applied for a patent for its quantum-dot cells in 2005, Cyrium has yet to fully exploit its technology commercially.

However, it has been working with the epiwafer foundry IQE and has put forward a number of modes of application for the quantum-dot layer in multi-junction solar cells. It could replace the GaAs layer in a triple-junction cell to provide better current balance between the layers, for example, or it could become the fourth layer in a quadruple-junction cell.

The start-up was established in 2003 at the Canadian National Research Council's Industrial Partnership facility in Ottawa by quantum-dot expert Simon Fafard. It secured $2.6 million in venture funding in 2005, in a round led by Pangaea Ventures.

UV LEDs

Funding round boosts AlN firms

AlN material specialists Hexatech and Crystal IS have each won $2 million awards to help to develop ultraviolet (UV) LEDs for water purification applications.

North Carolina State University spin-out Hexatech is focused on perfecting the production of its single-crystal AlN substrates and will investigate both polar and non-polar materials. “It’s a three-year program,” commented Hexatech’s CEO Jim LeMunyon. “During that we would plan to have substrates for sale as well as UV-LED devices that can be demonstrated.”

“The Advanced Technology Program (ATP) grant does two things,” the CEO added. “It validates that what we’re working on is the real deal and it’s going to let us do things sooner than we otherwise would.”

Founded in 2001, Hexatech makes its substrates using a sublimation process that LeMunyon says is kept under “exceptional control” to assure maximum crystal quality.

These high-quality AlN substrates will provide a close lattice match for high-aluminum-content AlGaN. Increasing aluminum content results in shorter-wavelength LEDs but it also generates a wider lattice mismatch with conventional substrates like sapphire, lowering the output power.

The ATP project – managed by the US National Institute of Standards and Technology – will see Hexatech using external epitaxy suppliers to make the UV-LEDs.

Hexatech’s substrates can be used either for UV optoelectronics or for high-power RF devices. Beyond the ATP project, a number of partners are interested in using Hexatech’s high-quality AlN.

“We’ve seen others roll out with any old 2 inch wafer and the crystal quality just isn’t there,” LeMunyon commented. “A lot of device-type customers feel burned by that, with good reason.”

LeMunyon explained that the US Environmental Protection Agency is putting its weight behind UV-based water treatment, giving UV-LEDs a major opportunity. For example, new UV treatment facilities in New York are set to treat 2.2 billion gallons of water per day.

“They have to use what are effectively UV fluorescent tubes,” LeMunyon said. “The tubes have lifetimes of the order of one year and, by their nature, have small amounts of mercury in them, so they create a disposal problem. The opportunity in this industry is to basically remove the tube and replace it with solid-state [lighting].”

Meanwhile, Crystal IS has received a near-identical grant in the same area. “The money will be spent on a development program to use AlN substrates to develop high-efficiency, high-power UV-LEDs with long lifetimes,” said Tim Bettles, Crystal IS’ vice-president of business development, sales and marketing.

Running from this month, the three-year project aims to produce 280 nm LEDs with a performance that is “significantly higher” than the current industry best.

“Current state-of-the-art UV-LEDs operate at 2% wall-plug efficiency and have a lifetime of less than 1000 hours,” Bettles said. “While this is OK for some research and analytical applications, the bigger markets, such as germicidal disinfection, require considerably better performance.”

Under a previous ATP award, Crystal IS had developed the world’s first 2 inch AlN substrates cut from boules at its Green Island, NY, laboratories. It now plans to develop non-polar and semi-polar AlN material.

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...40 G partnership
InP chip maker JDSU is partnering with communication systems company Mintera on a new 40 Gb/s technology. A new transponder module based on the concept should be released in the first half of 2008.

...Bandwidth bags a million
The US Missile Defense Agency has funded a $1 million effort at Bandwidth Semiconductor to develop high-reliability, high-power red lasers based on GaAs. The technology required is similar to that already used in photovoltaic concentrator cells.

...QPC doubles sales
Now shipping its third-generation lasers for applications in medicine, QPC Lasers expects to post total revenue of about $5 million in the first nine months of 2007.

SOLAR CELLS

Emcore's Danzilio basks in the sunshine

Emcore has been winning multimillion dollar contracts for its terrestrial solar cells, modules and systems. Photovoltaics vice-president **David Danzilio** tells **Richard Stevenson** about the reasons behind this success and the advances that the company is making in its products for space applications.

David Danzilio: a career in compounds

1984: graduates with a chemistry degree from the University of Lowell, MA, and joins M/A COM as a process engineer.
1987: joins Adams-Russell Electronics as a staff engineer.
1988: takes a senior engineering role at Raytheon.
1995: returns to M/A COM and directs all GaAs MESFET and PHEMT development.
1999: wins promotion at M/A COM and manages a 24/7 GaAs wafer fab.
2004: moves to Emcore and takes the role of vice-president and general manager of the photovoltaics division.

You have recently netted some very large terrestrial concentrator photovoltaic (CPV) contracts. Was 2007 the year that CPV took off?

I'd characterize 2007 as the leading edge of CPV being a viable, commercial technology. [This technology has] had a couple of few-hundred kilowatt deployments and a 2.1 MW deployment in Spain by the Institute for Photovoltaic Concentration Systems (ISFOC), but we haven't seen the 10 MW projects getting deployed. It's going to be 2008 that CPV really begins to deploy.

Which are Emcore's key contracts?

Our largest customer on the terrestrial side is Green and Gold Energy of Australia. We currently have more than 100 MW in backlog. We are producing today and shipping against that order, which is scheduled to be fulfilled in 2008.

We have other activities on the system side. Our investment in World Water and Solar has resulted in a supply agreement for up to 100 MW of system design and system-level products over the next few years. They are bidding for projects using the Emcore CPV system, but that's not the only thing that they are using. Depending on the geographical location of a particular installation, flat-plate silicon may actually be a better solution. Where CPV is preferable, World Water and Solar is bidding [with our technology].

We have put in a bid for 400 kW of CPV installation at the Castilla la Mancha location in Spain. That's the ISFOC project, which is a test-bed for CPV. It provides the first reasonable-sized installations for many new designs to get on-sun heritage. It was a wonderful concept by ISFOC and the Spanish government to fund this activity, because one of the biggest barriers to the development of CPV is acceptance of the technology.

What has driven your recent terrestrial success?

We have actually won significant contracts in our space business as well. It's the result of a lot of investment over the last couple of years in technology, manufacturing and the business.

On top of that, the market is increasing in both space and terrestrial, and Emcore has positioned itself very well to be the preferred supplier. When somebody looks at placing a 100 MW product order for terrestrial, they have to make the assessment: can we fulfill that order? When they come, our terrestrial customers see that we do have the capacity. Look at our investment roadmap, look at our technology roadmap and it becomes clear that we are positioning ourselves to be the dominant supplier.

On the space side we've made a lot of investment in manufacturing. In space, the most important factors are reliability, reliability and reliability. Our solar cells perform and we have pushed the technology forward, but ultimately what our customers buy is a low-risk, highly reliable product, whether it be a solar cell or a solar panel. We've also made a lot of investment in advanced process control techniques for all of our manufacturing processes. These sorts of investment resonate very well with our space customers, because the key to high-reliability products is highly controlled, well characterized manufacturing.

Emcore also makes fiber-optic components. How much of the company's business is solar?

In 2007, solar is going to be more than 35% of Emcore's revenue. Right now, 90% of this is derived from space activities. The balance is terrestrial and it's hard to say what the split is between cells and modules. We don't have any system revenues so far.

In 2008, I expect that the revenue split will be equal for space versus terrestrial, but in five years time – pure speculation – I see a growing market in space plus terrestrial. Clearly terrestrial is the bigger market by a factor of 300 to 500, so in five years we could be 75% terrestrial, 25% space. But it all depends on how successful CPV is and how successful we are in winning that CPV business.

Applied Materials says that CPV will only find a handful of niche locations where it can be economical, but others, such as SolFocus, say that CPV could ultimately produce one-third of all PV energy. What is Emcore's estimate?

I tend to be more on the SolFocus side. I believe that the majority of electricity that is generated by renewable means is going to be generated in large utility-scale installations. That's the market segment that Emcore is addressing. Maybe 30% of the market is aggressive, but I estimate CPVs to be 15–20% of the total market. That is more than a niche.

Applied Materials' products provide turn-key manufacturing lines for silicon. This is silicon for rooftops. Although that's a big market, it's not going to be generating electricity on the scale of a multiple number of 10–100 MW utility-scale installations.

Applied Materials is focusing on silicon cells and is obviously a very influential company within the semiconductor business. Is it a complementary or a competitive technology?

I see it as complementary. I look at Applied Materials as enabling the flat-plate silicon market, which to a major degree is complementary, but to a minor degree competitive. So I don't see them as a threat and they are bringing a lot of good discipline and manufacturing expertise to the silicon PV market.

Skeptics say that CPV is unproven. Are there any potential show-stoppers?

I don't see any potential show-stoppers. The component that's going to be seeing the most stress and strain is the solar cell, followed by the optical components. On the solar cell side, we've designed these parts to operate well in excess of 1000× – that's the design of the tunnel junctions and the current-carrying components. There is enough design margin in there based on our experience with space and our understanding of the degradation mechanisms and we feel very confident that our solar cells will provide a useful life in excess of 20 years.

In fact, for a number of our systems customers where we are providing components, we have already agreed to a performance warranty on par with that of silicon. I feel quite confident and comfortable that the solar cell will be reliable for the life of the system. Once you get beyond that there is still the stability of the lenses and plastics and then the motors and structures. There is still a lot to be learned about the long-term stability of the optical components, the lenses and the secondary optics, but I don't see any reliability issues with electric motors – they just need to be maintained.

What is your view of copper indium gallium diselenide (CIGS) technology?

CIGS is interesting. It has the potential to have a very low manufacturing cost and it is going to find application in areas where available land is plentiful and has a moderate solar resource. The low efficiency requires you to have fairly large-area installations, which drives up installation costs, but it has the potential to see broad deployment.

You've invested quite a bit in equipment recently. What is your capacity?

That depends on what type of capacity you are talking about. The way I do my calculations is to work out how much capital asset is applied to terrestrial and apply an appropriate concentration factor.

Using a 1000× concentration factor, in 2008 we will have in excess of 200 MW of terrestrial production capacity, while simultaneously supporting about 200 kW of production capacity for space. But depending on the business levels for space, I can choose to allocate some of that capacity to terrestrial.

Another way to look at it is wafer throughput. We currently have the capacity to produce 300,000 [4 inch] wafers per year and we're running at about 70% capacity. We are expanding and I expect to be at around 400,000 wafers per year by late 2008.

Do III-V chip costs dominate the $/W equation?

No. That's the unique characteristic of CPV – the solar cell is a very small proportion of the overall system cost. For a typical silicon flat-plate module, 75% of the cost is the solar cells. But for CPV, because you use concentration, you're using much less of what is a more expensive solar cell. In the order from Green and Gold Energy the solar cell costs $0.23/W.

Many of the systems developers are targeting an overall installed system cost in the $3/W range, which gets you under the threshold of $0.1/kWhr. If you use $3/W as a target – and no-one has got there – $0.23/W is less than 10% of the cost of the system. I've been telling my customers that I've got there and I've got there very, very fast, because I have a unique design that uses a high concentration and takes very good advantage of the power available on the wafer.

Is your triple-junction solar-cell technology completely optimized?

No, there's room for improvement. For space, our flagship technology is a 28.5% efficient solar cell. We have a 30% cell that is going to be released in late 2007 or early 2008 that will probably be the last embodiment of the typical Ge/GaAs/InGaP triple junction.

The next architecture is going to be the inverted metamorphic (IMM), which has demonstrated 31.9% efficiency under space conditions. The target is 33% and the cell should be available in the 2009/2010 timeframe in commercial quantities. In parallel we are working on four-junction IMM, targeting an efficiency of 35% under space conditions.

One of the highly desirable, unique aspects of multijunction technology is that you have many more degrees of freedom in terms of materials, bandgap engineering and all aspects of materials science. That is a tremendous advantage over silicon, which has hit its limit. There are a couple of tricks that you can do to get the efficiency higher by putting the contacts on the back, but there is a fundamental limit.

How long will the standard triple-junction cell be the leading product?

Well into the next decade. In space, demonstrated reliability is much more important than technical innovation, and our space products have a fairly long life cycle, such as 5–6 years. I believe that our 28.5% cell deployed last year will be selling well into the next decade. The 30% cell that will be deployed late this year, or early next year, will be shipped through 2012/2013 and the IMM being deployed in 2010 will probably enjoy a 5–7 year product life cycle.

In the terrestrial area, the adoption of technology is more rapid. The driver is efficiency, because efficiency drops directly to the bottom line in terms of the number of kilowatt hours that a system can generate. The market is driving towards the low 40s by 2010 and I believe that we can get there with our next-generation triple-junction cell.

> "I estimate the market for CPVs to be 15–20% of the total market. That is more than a niche."
> **David Danzilio**
> Emcore


EMCORE

Emcore's solar cell business is currently dominated by space applications, but in five years it is expected that most sales from the photovoltaic division will be to the terrestrial segment.

WIN joins the BiFET brigade

WIN has joined a select band of chip makers with its own BiFET technology. The H^{2}W foundry process optimizes HBTs and PHEMTs independently, and it integrates power amplifiers, low-noise amplifiers, logic control and a power switch on a single chip, says **Cheng-Kuo Lin**.

WIN Semiconductors makes its H^{2}W chips at its 150 mm GaAs foundry in Ta

Ruthless component price erosion is prevalent in the highly competitive market of front-end modules (FEMs) for cellular phones. To stay competitive, chip makers have to reduce their manufacturing costs by reducing die size and count, and increasing functionality, which ultimately lowers overall component costs. At the same time, the FEM's performance has to undergo continual improvement to satisfy the desires of handset system designers.

GaAs still offers an RF performance advantage over silicon technologies, such as SiGe and BiCMOS, but it is falling behind in terms of cost and the level of integration. To address this weakness, most component manufacturers in the RF industry integrate several technologies into a multichip module (MCM) package, such as the HBT-based power amplifier (PA), PHEMT switch, CMOS controller and surface-mount passives. However, this approach suffers from high packaging costs that typically account for half of the overall bill of materials.

Recently, GaAs chip makers – including the US manufacturers Anadigics, Skyworks and TriQuint – have addressed this weakness by monolithic integration of the HBT and E/D-PHEMT. These sophisticated chips, which are often referred to as BiFETs, can eliminate the cost associated with MCM packaging. Now foundry customers can get access to this technology and receive an additional benefit – simplification of supply-chain management.

At WIN Semiconductors, a GaAs foundry based in Taoyuan, Taiwan, we are now offering our version of BiFET technology that we call H^{2}W. This 150 mm GaAs process, which we released earlier this year, integrates the InGaP HBT, E/D-mode PHEMTs and various passive components, including backside through via holes (see box "WIN Semiconductors' H^{2}W process").

Our H^{2}W process enables a HBT-based PA, a D-mode PHEMT switch, an E-mode PHEMT low-noise amplifier and an E/D-mode PHEMT logic control circuit to be combined on a single GaAs chip, free from external passive elements. Circuit designers can access the HBT and PHEMT technologies simultaneously and take the best advantages of each device type without any compromise in performance.

Our H^{2}W technology provides great design flexibility and novel circuit opportunities. For example, a PHEMT switch can be configured to produce a bypass circuit that boosts the efficiency at low power in a multiple-stage HBT (figure 1). Alternatively, the HBT's base-collector diode can act as the electrostatic damage (ESD) protection diode for PHEMT switches. This can address the issue of an unacceptably large real estate occupied by the Schottky ESD protection diode, which is a key drawback of the stand-alone PHEMT process. Other possible PA circuit designs that can benefit from the H^{2}W process include a bias control switch, a power control circuit and a current limiter. These opportunities are just a few examples. We believe that many other high-performance circuit designs are possible once engineers gain more experience with our mixed device technology.

with H^2W foundry process

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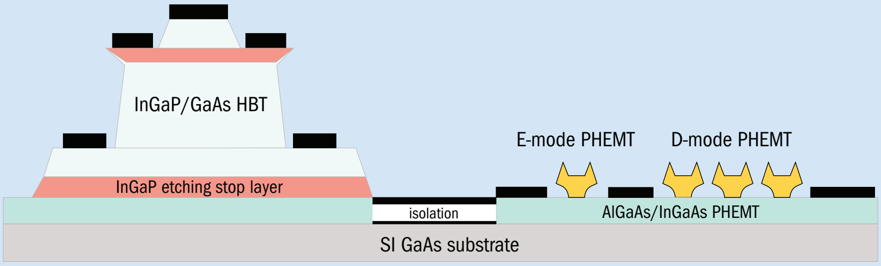
WIN Semiconductors' H^2W process



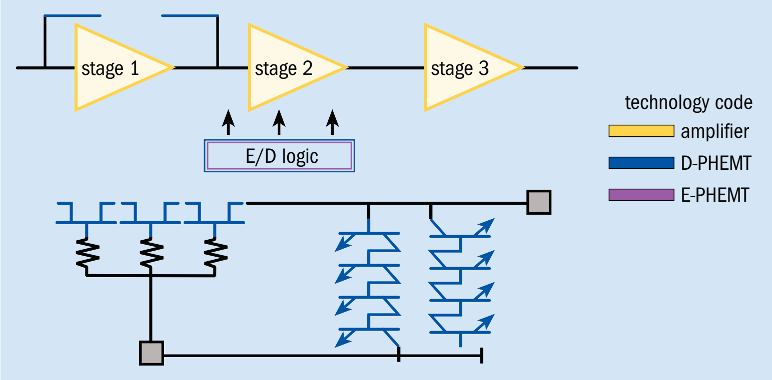
The H^2W fabrication process begins with a HBT mesa etch, followed by base metal formation and etching of the base and collector mesas. Electron beam evaporation adds ohmic contacts to the HBT collector and the PHEMT's source and drain, before ion implantation and a selective first recess etch isolate the two types of transistor.

These etching processes create HBT structures that protrude from the rest of the wafer. Fabricating high-quality 0.5 μm single- and multiple-gate PHEMT devices across this rugged landscape proved to be our greatest challenge during process development. However, we achieved success by carefully carrying out our gate recess process prior to metallization, which ensured fast gate switching by minimizing the impact from surface states.

Our 0.5 μm gate D- and E-mode PHEMTs feature the gate metals Ti/Pt/Au and Pt/Ti/Pt/Au, respectively. Multiple-gate D-mode PHEMT transistor cells are produced during the process, which can be used to make high-power switches for GSM applications.

After gate metallization, the HBT and PHEMT are fully passivated by depositing a SiN layer, before a TaN resistor is added with a sheet resistance of 50 Ω. Two interconnection metal levels and a 100 nm thick SiN layer are used to form 600 pF/mm^2 MIM capacitors, before polymide bridges and nitride protection layers are added to ensure the chip's reliability.

This completes the front-side processing. The substrate is then thinned down to 75 μm and through-via holes are added using an inductively coupled plasma etch. Finally, the backside of the wafer is plated with a 4 μm thick gold film.



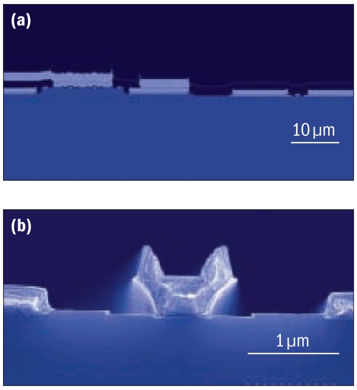


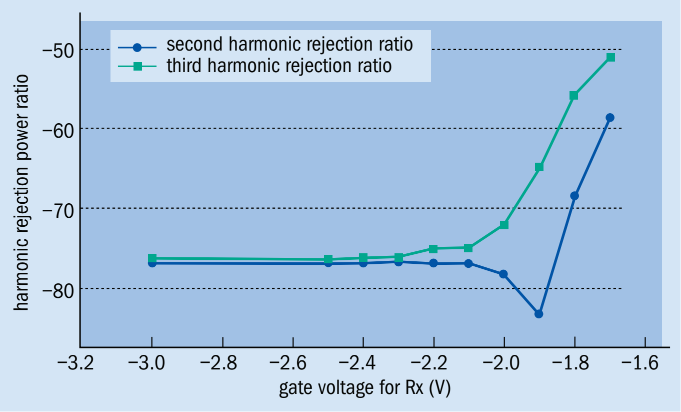
Fig. 1. (far left) The H^2W process can produce circuits that use the base-collector p-n junction diode of HBT to provide an electrostatic damage-protection diode for the PHEMT switches. **Fig. 2.** (left) Scanning electron microscopy images of **(a)** a cross-section with a HBT, E-mode PHEMT and two D-mode PHEMTs (right to left), and **(b)** the gate of a PHEMT.

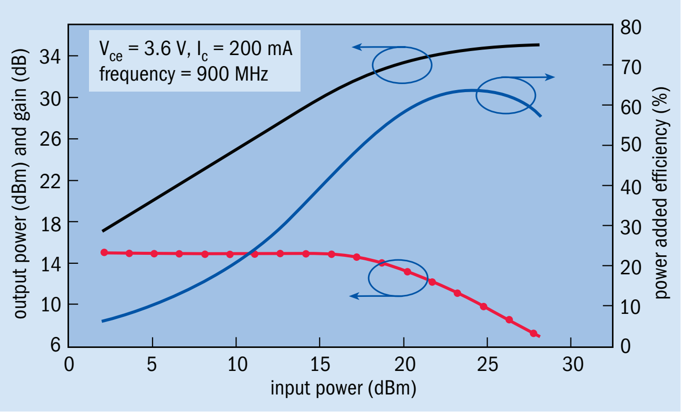
The epiwafers for our H^2W process are grown by MOCVD on semi-insulating GaAs and feature a stacked layer structure with the InGaP HBT on top of the PHEMT. Such a design is suitable for high-volume, low-cost manufacturing because it uses the single growth approach and avoids the selective regrowth technique pioneered by TRW in the 1990s.

The H^2W process eliminates additional parasitic capacitance in the PHEMT by placing the HBT on top of this device. With this geometry the undoped InGaP etch-stop layer isolates any influence that the PHEMT has on HBT performance. Skyworks, in comparison, adopts a different approach. The emitter layer is used as the channel layer for FET fabrication. In this case, parasitic capacitance could affect the FET's RF performance, but that is not a major concern because this transistor's function is primarily to improve the bias circuit.

The other strength of our technology is the use of an InGaP etch-stop layer that fully separates the HBT and PHEMT. With our H^2W process, the HBT and PHEMT do not share any epitaxial layers, which means that it is possible to optimize the HBT and the E/D-mode PHEMT separately. This is different from Skyworks' and Anadigics' designs. Skyworks uses the HBT's emitter layer as the channel for its FET, while Anadigics shares its thick, highly doped collector layer between both transistors.

Our HBT's structure is ideal for cellular handset applications because it combines a high-power output with a rugged design. The PHEMT benefits from an epitaxial structure that is compatible with a double selective gate recess etch process, which means that the AlGaAs and InGaAs layers can be used for





PHEMT and HBT characteristics

D-mode PHEMT		*E-mode PHEMT*		*InGaP HBT*	
V_{to} (V)	−0.9	V_{to} (V)	0.35	B_{vcbo} (V)	30
I_{dds} (mA/mm)	210	I_{dds} (mA/mm)	0.01	B_{vebo} (V)	7
V_{dg} (V)	20	V_{dg} (V)	20	BV (eco)	22
g_m (mS/mm)	320	g_m (mS/mm)	500	β	78
R_{on} (Ω/mm)	2	R_{on} (Ω/mm)	3.3	$V_{turn-on}$ (V)	1.26
f_t (GHz)	27	f_t (GHz)	28	f_t (GHz)	31
f_{max} (GHz)	63	f_{max} (GHz)	69	f_{max} (GHz)	115

Fig. 3. (above left) Single-pole-double-throw switches produced by the H^{2}W process and designed to operate at 900 MHz offer low insertion losses, excellent isolation and high second- and third-harmonic rejection ratios. **Fig. 4.** (above right) The H^{2}W process was used to produce an amplifier operating at 900 MHz that had been maximized for gain by tuning the input- and output-matching networks. This device, which has a total emitter area of 11,520 µm^2, produces a maximum output power of 34.5 dBm and was operated under the conditions of a collector-emitter voltage of 3.6 V, a quiescent current of 200 mA and a base voltage of 1.3 V. The power-added efficiency peaks at over 60%.

the Schottky barrier and the channel, respectively. We have also selected the layer thicknesses, doping concentration and composition of the III-V alloys to optimize the trade-off between characteristics such as breakdown voltage, on-resistance, pinch-off voltage, transconductance and gate lag.

These H^{2}W processing steps form HBTs and PHEMTs separated by 25 µm that are clearly visible in cross-sectional scanning electron microscopy images (figure 2, p15). The wide recesses of the devices illustrate that it is possible to develop a process that can reliably control the gate's dimensions.

Our H^{2}W process can reliably yield high-quality PHEMTs and HBTs on the same chip (table 1). Both D and E-mode PHEMTs, for example, deliver a drain current from a 100 ns pulse that is greater than 90% of the value from continuous operation. This indicates that they are suitable for serving applications requiring high frequencies and power densities combined with a fast switching time for PAs and switches.

Tests on our 2 × 75 µm E-mode PHEMT operating at 3.5 GHz, which is biased at a source-drain voltage of 5 V and produces a source-drain current of 130 mA/mm, reveal a maximum power-added efficiency (PAE) of 64.3% and an output power of 392 mW/mm. Meanwhile, our 8 × 25 µm E-mode PHEMT produced a minimum noise figure of 0.44 dB at 3 GHz and 16.7 dB of gain, under the conditions of 3 V and 75 mA/mm.

We have also investigated the performance of single-pole, double-throw switches fabricated with our H^{2}W multigate process technology (figure 3). At 900 MHz, they produce a 0.45 dB insertion loss (the difference between the signal at the transmitter and the antennae) and more than 25 dB of isolation (the ratio of the signal at the transmitter and receiver).

Harmonic testing has been carried out to assess this switch's linearity and has proved that our H^{2}W optical gate lithography process is suitable for multiple-gate high-power and high-linearity applications using low control voltages.

We have also assessed our InGaP HBT's performance. These transistors have a typical turn-on voltage of 1.26 V and feature a base layer designed to deliver a DC current gain of 78. PAs built with these devices and operating at 900 MHz produced 34.5 dBm at 63% PAE (figure 4). Tests to assess the ruggedness of this amplifier, which revealed a voltage-standing-wave ratio of 12 for all input phases under the conditions of a collector-emitter voltage of 3.6 V and an input power of 27 dBm, demonstrate that this device is robust without sacrificing power.

Reliability tests have been performed on both types of transistor. The D- and E-mode PHEMTs pass our internal 500 h test at 165 °C, using source-drain voltages and currents of 8 V and 80 mA/mm, respectively. Meanwhile, the HBTs show no decline in current gain after operating for 1000 h at an ambient temperature of 125 °C.

This series of tests demonstrates the reliability and performance of HBTs and PHEMTs united by the H^{2}W process. In addition, it shows that fabless designers of PAs now have access to a foundry process that can produce highly integrated RF transceivers and novel RFIC circuits. The H^{2}W approach may still be in its infancy in terms of circuit design but it will now have an increasingly important role to play in the evolution of handset FEMs. ●

About the author

Cheng-Kuo Lin is the project manager of WIN's HEMT product technology development division. He joined the company in 2004 after completing a PhD at National Central University, Taiwan.

R STEVENSON

LED chip makers lock horns in Vegas

The “city of sin” saw leading chip makers go on the offensive with claims of class-leading devices, and GaN-substrate developers championing breakthroughs in large-diameter free-standing material. **Richard Stevenson** reports from the 7th International Conference on Nitride Semiconductors.

Las Vegas oozes a party atmosphere and the beat wasn’t lost on the delegates at ICNS. Great talks inspired a feel-good factor among the attendees and this positive outlook was only reinforced by registration figures that exceeded all expectations.

Klaus Ploog, the legendary MBE crystal grower and former academic of the Paul Drude Institute, Germany, kicked off the meeting by extolling the versatility of nitrides, although he did temper this by pointing out that many applications demand more development. While GaN LEDs are obviously a great commercial success, Ploog reminded everybody that work is needed to improve the efficiency of green emitters, as is the case for a whole host of other uses of the semiconductor.

Ploog believes that edge-emitting lasers are being held back by the lack of affordable GaN substrates, but says that recent progress in this area has been tremendous. The absence of a GaN VCSEL is also a blot on the nitride copybook, and the key issues to address here are improvements to the mirror’s reflectivity and conductivity.

On the RF side, problems such as high HFET drain currents have been solved. However, low production yields are a concern, along with high chip costs that result from the use of expensive SiC substrates.

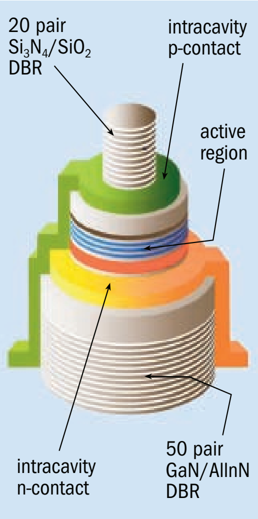
Ploog’s themes were picked up by many speakers during the conference. As expected, the representatives from several of the leading LED makers – including those from Nichia, Cree and Lumileds – did not hold back in stressing the strength of their research and commercial devices, particularly in the context of white devices for general illumination.

If the key battleground is efficacy at 350 mA, then Nichia came out on top with a 134 lm/W white LED. This 1 × 1 mm chip can produce 361 lm at 97 lm/W and 1 A, and it features a blue (λ~450 nm) LED.

Nichia’s Yukio Narukawa explained that the latest LED also beats the company’s previous record at 20 mA, which was announced last fall, and raises this efficacy benchmark from 138 to 169 lm/W. The previous record-holding chip was the result of efforts to boost extraction efficiency and featured an ITO contact in place of translucent metal and a hexagonally patterned substrate. The latest gains have come from research focused on lowering the forward voltage and increasing current spreading through improvements to the device’s epitaxial quality and design. The new record-breaking chip is better at maintaining efficiency with increasing drive current and has a wall-plug efficiency of almost 40% at 350 mA.

Although these performance figures are impressive, Narukawa believes that there is plenty of room for improvement. According to Nichia’s calculations, phosphor-pumped LEDs made with blue emitters have a theoretical limit of 263 lm/W. This is significantly higher than the maximum for a violet

The 7th International Conference on Nitride Semiconductors (ICNS) was held in Las Vegas on 16–21 September and attracted 940 delegates. The venue was the massive MGM Grand Hotel, a facility that boasts more than 5000 rooms, 3000 slot machines, 19 places to eat and a 6.6 acre swimming pool complex.



GaN VCSELs produced by École Polytechnique Fédérale de Lausanne, Switzerland, and the University of Southampton, UK, can produce electroluminescence with a linewidth of 0.3 nm. The laser that produced this emission features a Si_3N_4/SiO_2 top mirror, an AlGaAs/GaAs bottom mirror and current injection beneath the top mirror.

405 nm pumped equivalent, which is predicted to top out at 203 lm/W.

Cree also revealed its latest efficacy figures, which are just a whisker behind those of Nichia. Company co-founder John Edmond announced that Cree's best result now stands at 133 lm/W for an LED with undisclosed dimensions. This is a slight improvement on the 129 lm/W announced in September. Edmond also said that it should be possible to make light bulbs from a single GaN chip, although thermal issues must be overcome, and he took the opportunity to slam mercury-containing fluorescents, which he described as "vile and poisonous".

The influence of chip size on performance was discussed in a talk by Lumileds' Frank Steranka. He explained that the company's LED design produces 115 lm/W at 350 mA from a 1 × 1 mm chip and also delivers 142 lm/W from a 4 × 4 mm chip. His underlying message was clear: claims of record efficacy need to include details of the chip's size.

Steranka also discussed the progress required to hit the US Department of Energy's stiff future targets, which include the goal of 150 lm/W at 2 A by 2012. According to him, hitting this milestone will require a hike in internal efficiency to 90%. Phosphor technology must also improve, as one-fifth of the emission can be lost in conversion.

Although the 2012 target is demanding, Steranka believes that reaching it holds the key to LED adoption in solid-state lighting. At present, incandescent and fluorescent lamps have a cost-per-lumen ratio of \$0.03–0.05 and \$0.06, respectively. To compete, the figure for LEDs needs to drop by a factor of 20. But increasing drive current to 2 A and efficacy to 150 lm/W will deliver a nine-fold improvement, which means that chip makers can get into the right ballpark if they halve the cost of making LEDs.

Better substrates

Significant recent progress has been made in the field of GaN substrates, including the first 2 inch material produced by the ammonothermal method. Fumio Kawamura from Osaka University, Japan, explained that he and his co-workers produced this material by adding about 1 mol% of carbon to the standard mixture of materials in the reactor, which substantially reduced the proportion of polycrystalline material. The 2 inch GaN, which is 4 mm thick and has a dislocation density of $2.3 \times 10^5\,cm^{-2}$, was produced with a new reactor design that features mechanical stirring and thermal convection to ensure a homogenous solution.

In the same session, Hitachi Cable detailed its growth of 3 inch GaN using void-assisted-separation technology. Yuichi Oshima explained that the process used to make a substrate begins by depositing a 300 nm thick GaN layer on sapphire at 1000 °C. A thin TiN layer is then added, which forms a nanoscale mask when the wafer is annealed in a nitrogen and ammonia atmosphere.

A 600 µm thick GaN layer is grown on this mask by HVPE at 1050 °C. Once growth is complete, this film self-separates from the sapphire during cooling to form a free-standing substrate. In trials, each of the four attempts at producing 3 inch material has been successful and all of the substrates have been free from cracks and a specular surface.

Non-polar substrates were also covered at ICNS, with Mitsubishi revealing its process for making 10 × 10 mm *m*-plane material. Company representative Kenji Fujito says that manufacture begins with HVPE-growth of *c*-plane GaN at 270 µm/h, typically for 40 h. The resulting GaN crystal boule is vertically sliced to form pieces of *m*-plane GaN. These substrates have a dislocation density as low as $4.4 \times 10^5\,cm^{-2}$ and a thermal conductivity of 1.9 to $2.5\,Wcm^{-1}K^{-1}$. "Our activity is focused toward 2 inch diameter *m*-plane GaN," said Fujito, but it is clear that a different approach is needed to scale to that size.

For several years, GaN VCSELs have just been a distant dream, but this could soon change. Eric Feltin from École Polytechnique Fédérale de Lausanne, Switzerland, revealed that his groups' collaboration with the University of Southampton has produced electroluminescence from a VCSEL with an external quantum efficiency of 0.7%. The emission had a peak wavelength of 445 nm and a linewidth of 0.3 nm. The laser's cavity had a Q-factor of 1500, which is the highest Q-factor reported under electrical injection, says Feltin. According to him, if this figure can be doubled, there is a very good chance of producing a VCSEL that lases.

Although much of the focus in Vegas was on optoelectronics, RF devices were also covered. Masahito Kanamura from Fujitsu detailed the company's development of alternative high-k dielectrics to SiN for improving transconductance and power gain in HEMTs. He revealed that Ta_2O_5 can suppress leakage current and has led to the first MIS-HEMT with a 100 W output power. Fujitsu's 38.4 mm device produced 143 W at 2.14 GHz, and it showed excellent RF power stability during a 150 h lifetime test.

Despite improvements in GaN RF performance, pessimism permeated through the rump session discussing the commercial future of these types of device. Replacing silicon LDMOS in cell-phone base-stations has been identified as the target market for many years, but this rival's continual performance improvements have thwarted sales wins for GaN. However, other potential markets for the technology, such as in the electronics circuit for light bulbs and cable TV amplifiers, were highlighted in this session. Philippe Roussel from Yole Developpement predicts that the total market could be worth \$101 million in 2010, but this equates to only 10,000 4 inch wafers per year – nowhere near enough to support the growing number of SiC suppliers. Lack of progress in scaling GaN to higher frequencies was also noted, with one wise-cracker claiming that the best root to progress was to replace nitrogen with arsine. This session aside, the mood at ICNS was unquestionably upbeat.

PHOTOVOLTAICS

Room for improvement in solar cells

Despite photovoltaic conversion efficiencies recently reaching record highs, there is no shortage of ideas for further refinements, finds **Michael Hatcher**.

With conversion efficiency records claimed on a regular basis over recent months, the growing potential for energy production using III-V solar cells has rarely been out of the headlines. But, as the recent European Photovoltaics and Solar Energy Conference in Milan showed, there are still plenty of new ideas for further refinement of the technology.

Dwarfed by the existing market for silicon photovoltaics, III-V cells are only just becoming a commercial product for terrestrial applications. However, III-V research themes enjoyed a high profile at the Milan event's technical conference, right from the opening plenary session.

Spectrolab's Richard King kicked things off with a look at the recent breakthroughs leading to 40.7% efficiency in traditional triple-junction concentrator designs, before highlighting the potential offered by adding further junctions to deliver efficiencies heading towards the theoretical limit of 72%.

The problem with adding more junctions based on InGaN or GaAsN is not just the lattice mismatch with the existing epitaxial structure. The current generated by these subcells needs to be matched to the three junctions, while the changeable nature of the terrestrial solar spectrum (particularly in the early and late periods of the day) offers further complications.

King says that a four-junction cell could produce a maximum external quantum efficiency of 59%. Spectrolab's researchers have already made preliminary designs reaching 35%. These, and futuristic five or six-junction converters, are some way from commercial release, however, and King was keen to stress what could be produced in the III-V fab today. In 2008, Spectrolab will produce triple-junction cells with an average lot efficiency of 37%, rising to 40% in 2010.

While US-based Spectrolab and its compatriot Emcore are the current technological leaders in the sector, Matthias Meusel highlighted how the top European cell-maker, Azur Space Solar Power, is also pushing forward with designs for terrestrial applications.

Much of Azur's work is focused on custom designs for its commercial partners, but the German company is also working on extra-thin, flexible cells (just 20 µm thick compared with the standard 145 µm).

Using a 12 × 4 inch Aixtron reactor for the wafer production of 35% efficiency cells, Azur is working on additional junctions, admitting that GaInNAs layer quality must be improved for this concept to be feasible. Lattice-mismatched structures are also in the pipeline, with Meusel acknowledging that bypass diodes are an indispensable element of the cell design.

Allen Barnett, University of Delaware, described the newly expanded DARPA program to reach 50%, showing how the combination of a GaInP/GaAs 31.7% tandem cell with a 6.2% GaInAsP and 5% silicon cell could be combined in a 42.9% module. Barnett predicts 50% efficient modules in around three years.

Of course, satellite power is still the workhorse application of the triple-junction cell, and, in a session dedicated to space technologies, Emcore's Paul Sharps discussed the firm's ZTJ cell, so-called because it represents the end of the line for improvements in GaInP/GaAs/Ge triple-junction designs. The ZTJ began space qualification tests in August.

Just three years ago, Sharps believed that 28.5% would be the ultimate limit for the average lot efficiency of these cells under a one-sun illumination. But, by tuning the aluminum composition of the InGaAlP layer of the ZTJ to improve current matching, Sharps and colleagues were able to push to 29.5%. He expects the benchmark efficiency of these cells in mass-production to reach 30% in 2008.

Getting beyond this figure will require a completely new design, however, with Sharps convinced that 30% really is the limit for lattice-matched triple-junctions in space. Emcore's new inverted metamorphic (IMM) cells, which the company also showed off at its industry exhibition booth, look like the key to future space applications. So thin that, upon first glance, one resembles a piece of discarded aluminum foil, the IMM offers the potential for super-light, rollable solar panels that could be unfurled by a satellite or spacecraft after launch.

Another US group looking at potential fourth-junction materials is Alex Freundlich's at the University of Houston. Freundlich described one candidate, GaAsN, as a "pathetic semiconductor". Problems with doping and a poor minority carrier lifetime are the key difficulties with this material, although multi-quantum-well (MQW) devices based on the dilute nitride could be possible. Using the rarely seen technique of chemical beam epitaxy, the Houston research team made a 15-period MQW stack of alternating GaAsN and GaAs layers and, although only a low current was generated, a 0.6 V photovoltage suggests that the approach may have some merit.

Alongside a plethora of research into novel cell materials, such as InGaN, polycrystalline germanium, quantum dots and ZnS nanoparticles, important work is now being directed towards proving the reliability of III-V cells in real-world conditions. David Faiman from the Ben Gurion University of the Negev in Israel appears to have put an array of GaAs cells through the toughest conditions yet. He used the world's largest solar dish, known as PETAL, to focus intense beams of sunlight onto the module over the course of a few months.

Encouragingly, Faiman found no signs of degradation, much to his surprise, despite exposing the unencapsulated array to 1000× sunlight and, inadvertently, to condensation. Here's hoping that the rigorous testing regimes required for long-term cell deployment in space have made the technology sufficiently robust and reliable for applications on Earth.

The 22nd European Photovoltaic Solar Energy Conference and Exhibition was held at the Fiera Milano-Rho exhibition center in Milan, Italy, on 3–7 September. The conference attracted 3000 delegates and 12,000 exhibition visitors.

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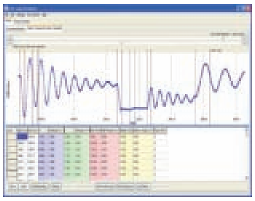

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HRL pushes high-frequency envelope

Successfully shrinking a GaN HFET's dimensions can ramp up its operating frequency and open the door to applications such as 94 GHz radar, last-mile wireless communication and non-lethal weapons that disable opponents by heating their skin, says HRL's **Brian Hughes** and **Michael J Keesling**.

Although there is strong demand for high powers and fast data rates, today's RF engineers are restricted by a lack of devices with operational frequencies beyond the low-gigahertz range at useful power levels. Fortunately, however, the situation is set to change, thanks to the significant amount of research that is focusing on a very promising class of device, GaN transistors.

Probably the most publicized and well funded effort developing this device is the US Defense Advanced Research Projects Agency program, entitled Wide Bandgap Semiconductors for RF Applications, which has focused on frequencies up to 45 GHz. But GaN can also serve far higher frequencies than this. Our development of this technology at HRL Laboratories of Malibu, California, has demonstrated that GaN devices can deliver a power density of 2 W/mm at 80 GHz. In fact, we have fabricated a range of GaN transistors operating in the 50–100 GHz range with similar power densities, which we detailed at last December's International Electron Devices meeting in San Francisco.

The key breakthrough resulting from our GaN development is an eight-fold hike in output power density compared with GaAs and InP technologies. This tremendous increase in output power will have far-reaching effects in the satellite and high-data-rate communications industries. It will also have effects in other applications, such as non-lethal weaponry, a technique that uses electromagnetic radiation at particular frequencies to disable opponents by increasing their skin temperature.

To produce these improvements in GaN HFET's frequency performance required aggressive scaling of the device's dimensions. This included scaling of the gate with electron beam lithography, which led to the production of a 100 nm T-shaped structure with a very low resistance. Another key feature of our transistors is the use of a patented double heterostructure that is formed during the MBE growth of GaN on SiC. This heterostructure is critical for reducing short-channel effects that can degrade transconductance. A heavily doped cap layer is also used in our design to reduce parasitic contact resistance to 0.2 Ω/mm, which required the development of a recess gate process.

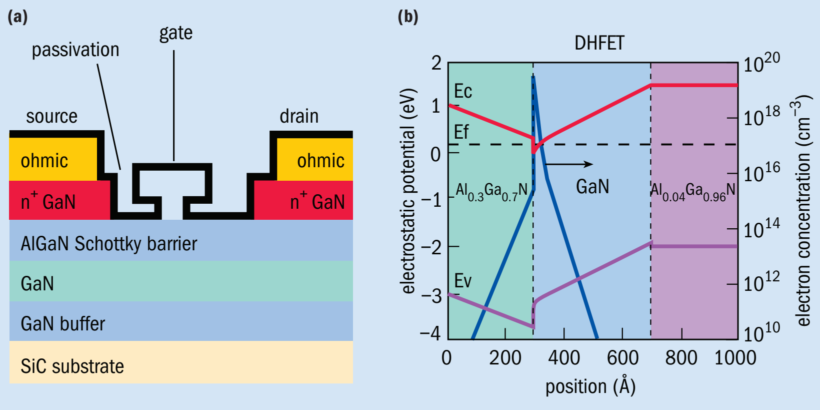
Scaling is not restricted to the device. It also includes the substrate's thickness and the ground interconnect dimensions. SiC substrates are thinned to 50 µm to avoid unwanted modes in the microstrip transmission line of the MMICs. Vertical vias measuring 30 µm are also cut through the substrate to reduce the ground interconnect inductance to less than 10 pH, which is a suitably low value for high-power devices operating at millimeter-wave frequencies.

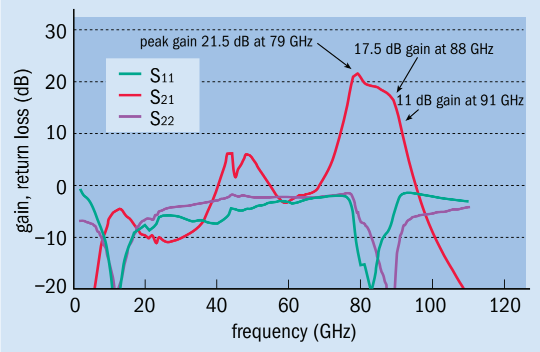
GIGABEAM

GigaBeam and its competitors, which build local high-speed wireless data links operating at 71–76 and 81–86 GHz, could benefit from HRL's powerful GaN MMICs. These devices can deliver an eight-fold improvement in power density over the equivalents built from InP and GaAs.

These modifications were used to produce all of our HFETs with high cut-off frequencies, including devices with an f_T of 90 GHz, 6 dB of power gain at 90 GHz and 2 W/mm power. Such devices operated with a high drain voltage of 15 V.

One factor that hampers the output power density of every III-V high-frequency FET is an inherent restriction on the gate width. If the gate is too large, propagation delays prevent the signals from combining in phase so the gate width must be less than a certain value, which decreases as the operating frequency increases. NGST holds the current output-power record for W-band MMICs and its InP HEMTs can produce 0.42 W at a gate width of





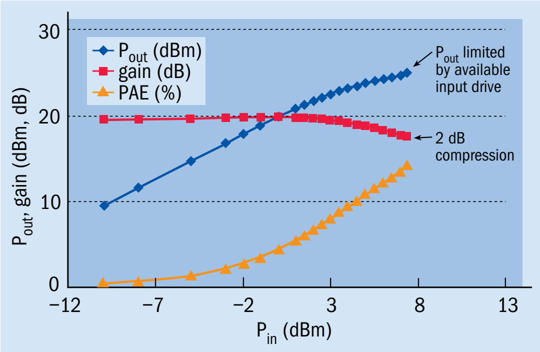


Fig. 1. (above left) HRL increased the operating frequency of its HFETs by scaling the device dimensions. The n^+ GaN layer provides an ohmic contact **(a)**. The company's proprietary double-heterojunction structure improves electron confinement and alleviates short-channel effects. The conduction band, Fermi level and valence band are denoted by E_c, E_f and E_v, respectively **(b)**. **Fig. 2.** (above right) HRL's three-stage GaN MMIC can produce 21.5 dB of gain at 79 GHz, 17.5 dB at 88 GHz and 11 dB at 91 GHz. S_{11}, S_{21} and S_{22} are the input port voltage reflection coefficient, the forward voltage gain and the output port voltage reflection coefficient, respectively. **Fig. 3.** (right) HRL's GaN MMIC can produce 316 mW in continuous-wave mode, which is an order of magnitude higher than that delivered by a GaAs PHEMT of a similar size. The device, which has an output stage of 4 × 37.5 μm, had a drain efficiency of 26%, a saturated power output of 25 dB, a gain of 17.5 dB, a power added efficiency of 14% and a power density of 2.1 W/mm.

1.6 mm. However, we estimate that a switch to our T-gate GaN HFETs with a similar gate width could ramp MMIC output to 3 W.

This eight-fold hike in power density could cause thermal issues. However, the channel temperature in the GaN devices is actually similar to that of their InP or GaAs counterparts, thanks to SiC's far higher thermal conductivity. In addition, GaN is capable of operating at far higher temperatures, which makes the thermal management for this class of device relatively simple.

Our GaN HFETs are also highly reliable. At this year's CS Mantech conference in Austin, Texas, we showed results that demonstrated the robustness of these transistors under tough power compression. Testing under compression generates valuable data because it replicates the typical operating conditions encountered by commercial devices.

The 2000 h test at 2 dB power compression and temperatures of 285, 315 and 345 °C produced a value for the activation energy of 1.8 eV, which implies a mean time to failure of more than 100 years at a baseplate temperature of 80 °C. This impressive reliability results from careful encapsulation of the transistor by SiN passivation and demonstrates that this technology is ready for product development.

High-frequency applications

Our GaN HFETs could be used to improve the performance of many different types of product. This includes millimeter-wave solid-state power amplifiers (SSPAs) for military and civilian communications. These amplifiers currently couple several InP MMICs to produce less than 1 W units typically costing $15,000. But the introduction of GaN could slash the component count and overall cost. The high price of the GaAs SSPA is not just caused by the cost of the InP MMICs themselves but also results from addressing combiner losses, the high assembly costs and other manufacturing issues. These include the need to hand-tune the SSPA to ensure that the phases and amplitudes of all of the arms of the waveguide combiner are perfectly matched over a broad range of temperatures, a requirement that ensures an efficient overall output.

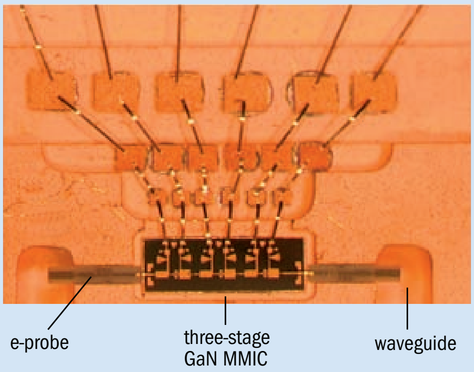
Using GaAs and InP MMICs also limits the output power to 1 W. It is impractical to build a 3 W SSPA because this would require a 16-way waveguide and a discrete component count of nearly 200, including almost 50 MMICs. Switching to GaN can cut the number of components to five (a single GaN chip, two electronic probes and two bias capacitors), thanks to the hike in power density. Although there is no getting away from the fact that the price of GaN devices is more expensive, partly because of the higher substrate costs, this dramatic reduction could cut the price for an SSPA to a few thousand dollars, even if the cost of a GaN chip is 10 times that of a state-of-the-art GaAs PHEMT. In addition, the GaN SSPA could deliver a further advantage – greater temperature tolerance – because there would be no temperature-induced phase mismatch between the power-combining arms.

GaN SSPAs could also provide an alternative to traveling-wave tube amplifiers (TWTAs). These devices provide amplification in the W-band (75–110 GHz) but are only available at power levels of 100 W or more. TWTAs have several other weaknesses: they are fragile, very power hungry, take a long time to warm up and can cost over $100,000.

High-frequency GaN for radar

Millimeter-wave phased-array radar benefits from a compact antenna that is fast, light and rugged, and if this technology is used in the Ka and W-band it is very suitable for target detection. Unfortunately, a lack of millimeter-wave power amplifiers offering high power density and efficiency has pegged back development, but the US government is now showing strong interest in GaN millimeter-wave power amplifiers.

One weakness of phased array radar is its vulnerability. The receiver can easily be damaged by powerful jamming signals and strong accidental signals from adjacent radars. Protection circuits can address this but they degrade the receiver's noise figure and add expense. However, protection is needed for technologies like GaAs PHEMTs because low breakdown voltages go hand in hand with the high-gain and low-noise characteristics required for low-noise amplification. Millimeter-wave GaN, however, is a different story because it can combine low-noise figures with a high breakdown voltage. This advantage has already been seen in one of our GaN MMIC amplifiers, which survived an input power greater than 5 W and has less than 2 dB of noise between 4.5 and 16 GHz.



A three-stage GaN MMIC (left) can produce several watts and offers a potentially affordable technology for producing active denial systems for troops that could incapacitate opponents.

GaAs MMICs are not likely to offer an alternative to this technology because of the lack of power associated with these chips. However, GaN HFETs could be combined into an SSPA to offer an alternative type of amplifier delivering 10 W or more in a relatively small package. The potential for miniaturization also creates new opportunities for millimeter-wave radar, such as miniature satellite transponders.

GaN MMICs are attracting significant interest in the commercial E-band communication market for providing high-speed wireless data links. These links operate at 71–76 and 81–86 GHz, two 5 GHz bands that have been opened up by the Federal Communications Commission. Communications providers, such as Bridgewave, GigaBeam, Loea, E-band Communications and Sophia Wireless, are all seeking business in this market and could benefit from deploying 0.5–2.0 W MMICs in their point-to-point data links. Although relatively low transmission powers are needed for these local links during good weather, heavy rain is highly absorbing at these frequencies and can break up the data link. This is obviously a major downside for businesses using this service, as well as a potential barrier to increasing the number of customers using this wireless connection, but the high transmission powers of GaN could lead to more reliable connections.

GaN could also become the technology of choice in satellite communication, missile systems and fighter jets. These applications demand low weight and high power, which equates to very high efficiencies and minimal heat sinks. GaN MMICs are competitive in terms of efficiency and have relatively small heat-sinking requirements, so we plan to get our devices space-qualified.

There has also been interest in GaN MMICs for active denial systems – non-lethal weapons that transmit electromagnetic waves at 95 GHz. This radiation excites water molecules in the outer layer of the skin and causes a burning sensation. The radiation can be directed at targets up to 0.5 km away and is viewed as a technology that can stop potential terrorists without injuring innocent civilians.

Raytheon has already built a TWTA-based Silent Guardian protection system that has been mounted on a humvee. But the military has been increasingly asking for portable, cheaper and lower-power versions, which could be used as an alternative to electric shock weapons. The potential market for police and prisons is very large, but the current cost for millimeter-wave power is too high. GaN brings this cost down and can even make active denial systems the "killer application" for millimeter-wave devices.

The various applications that we have highlighted illustrate that there are many sectors within the millimeter-wave market that could benefit from the introduction of amplifiers based on GaN HFETs. However, this is not the only potential role for this device, as it could also be used in RF switches. These are an essential component of many systems, such as filters and transmitter–receiver modules.

All types of solid-state switch are cheaper, faster and more reliable than their mechanical equivalents. However, they are limited by their voltage swing before they distort signals or are damaged, and by the RF parasitics that attenuate the signals. GaAs PHEMTs currently have a significant market in switches because they have low-RF parasitics, but their power is limited by their breakdown voltage. A 0.1 µm gate GaAs PHEMT typically has a breakdown voltage of less than 8 V, which is less than one-fifth of an equivalent GaN FET.

Today, GaAs MMICs enjoy tremendous production volumes in commercial devices, such as cellular phones, while their GaN counterparts that can offer greater performance are still in their infancy. Fortunately, specialized foundries, such as ours and Northrop Grumman's, can supply GaN MMICs to the nascent market, which will, we hope, lay the foundations to widespread deployment of this high-performance technology. ●

About the authors

Brian Hughes is a business development manager at HRL Laboratories, focusing on the commercialization of advanced III-V IC products. He has more than 25 years of experience in III-Vs, from design and characterization to management and business development. **Mike Keesling** is an independent technical writer.

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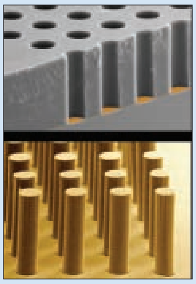

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Lake Shore’s new Model CRTTP6-4K micro-manipulated probe station provides efficient temperature operation and control with a 4 K cryogen-free closed cycle refrigerator, eliminating expensive liquid cryogens. It has a standard temperature range of 4.5 K–350 K, with 10 mK temperature stability. An optional high-temperature sample holder provides a temperature range of 50 K–475 K. Control heaters at each stage facilitate fast thermal response and rapid warm up for sample exchange – cycle time is <3.5 hours. Integrated vibration isolation and damping limit vibration to <1 µm throughout the full temperature range.

Contact Lake Shore Cryotronics
Tel +1 614 891 2244
E-mail info@lakeshore.com
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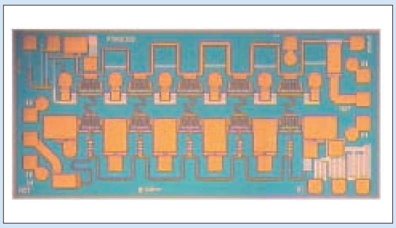
New BB MMIC Amplifiers from Filtronic

Filtronic Compound Semiconductors Ltd

Filtronic Compound Semiconductors has released a new family of Broadband MMIC amplifiers – the **FMA3007**, **FMA3008**, **FMA3009** and **FMA3058**. Filtronic’s Broadband MMIC products are high-performance 2–20 GHz gallium arsenide monolithic travelling wave amplifiers suitable for use in broadband communications, instrumentation and EW applications. The die is fabricated using high-reliability GaAs pHEMT technology.

Samples are available now via e-mail, or visit our website to download datasheets and supporting technical information.



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Diamond cools high-power transistors

Synthetic CVD-grown polycrystalline diamond has fantastic heat-conducting properties. Inserting a thin layer underneath a GaN HEMT can halve this transistor's operating temperature and substantially increase its maximum output power, says a team of researchers at California's **Group4 Labs**.

The vacuum tube amplifier is a technology threatened with extinction. Silicon LDMOS is already preferred for low-frequency, low-power applications and the hold that the vacuum tube has on the higher-frequency, higher-power applications could soon slip away. Although these tubes are still employed in amplifiers used in radar systems and satellite communications, there is an ever increasing threat from wide-bandgap technologies that are delivering impressive, improved performance characteristics.

Next-generation SiC and GaN amplifiers are expected to deliver output powers of hundreds of watts at frequencies beyond 10 GHz. This will make these devices an attractive option in various markets, including amplification for mobile-phone base-stations, satellite communications and high-power phased array radar systems. The primary advantages of these solid-state devices, much like their silicon brethren, are smaller sizes, cooler operation and suitability for integration into complex systems.

Transistors are already being deployed in increasing numbers in smaller areas and ever more complex systems. Radar systems, for example, can now employ more than 50,000 distinct amplifiers. This miniaturization requires modules that combine high performance with compactness and creates significant heat-management issues at the transistor and system level.

Smaller devices, such as FETs, present the greatest challenge for heat removal. These transistors, which are the primary workhorse of the microwave power industry, contain sub-micron heat sources that produce large temperature drops in the immediate proximity of the heat source – the regions around the gates and contacts. Traditional approaches for removing heat from these devices are based on external heat sinks. However, these only have a marginal impact on the temperature drops within 1 μm of the heat source, so there is a lot of room for improvement in thermal management.

The only practical way to improve heat flow from a sub-micron source is to spread it into the material surrounding the source. Placing materials with very high thermal conductivities close to the active region can achieve just this, and it occurs when SiC, a good heat conductor, is used as the substrate for GaN device growth. However, GaN-on-SiC devices are very expensive, while even better thermal management is possible by turning to a more powerful thermal conductor – synthetic diamond.

US NAVY

GaN-on-diamond wafers lower the operating temperature of GaN HEMTs and make these devices a more attractive option for deployment in radar systems that can employ thousands of amplifiers.

CVD-grown synthetic polycrystalline diamond has the best thermal conductivity of any naturally occurring substance known, with the exception of prohibitively expensive single-crystal diamond. Although the value for thermal conductivity depends on the quality of the diamond, it is in the range 12–15 $\mathrm{Wcm^{-1}K^{-1}}$, which is up to four times as high as that of SiC. This means that synthetic diamond can act as an exceptionally efficient heat spreader, by itself or in combination with other materials.

In many applications, a thin diamond layer can produce an adequate improvement in transistor thermal management. For example, calculations show that a 100 μm thick diamond layer can cut a SiC device's peak temperature by up to 50% (see results in figure 1a, p26), or commensurately produce 50% more power than a SiC substrate device. Measurements on real devices back up this claim of improved thermal management, and those made by Lester Eastman's group at Cornell University show a substantial reduction in device operating temperature for a given power output.

Substrates with a CVD diamond layer are also competitive from a cost perspective – the price of a

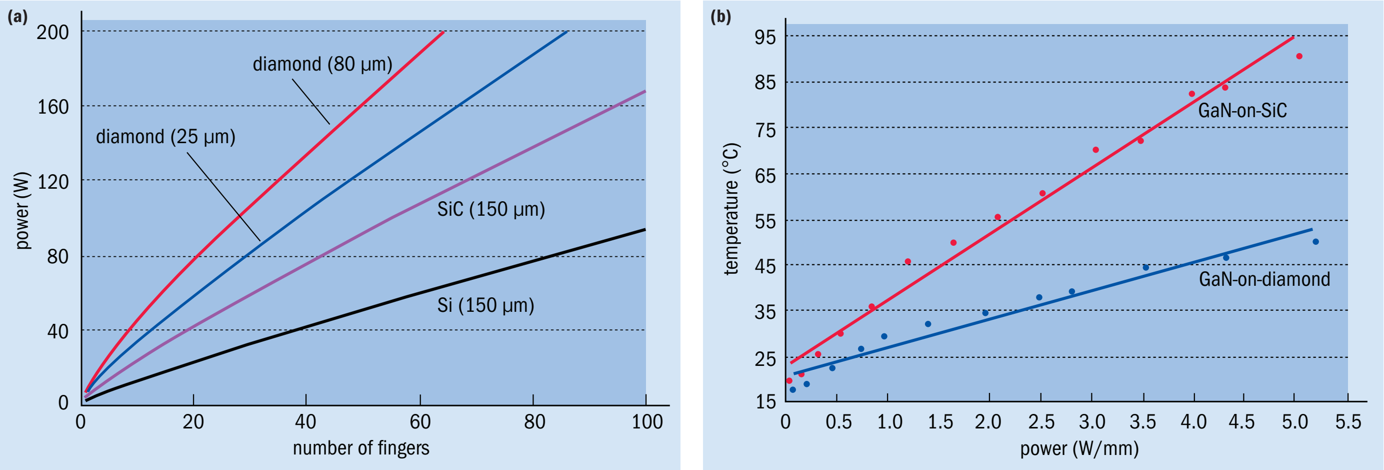


Fig. 1. (a) Calculations predict that layers of polycrystalline diamond can dramatically improve the output power of an AlGaN/GaN HEMT restricted to operating at a maximum temperature of 250 °C. The calculations compare the performance of 2 µm thick AlGaN/GaN epilayers on two different thicknesses of CVD diamond, and SiC and silicon, which are all attached to a 150 mm thick copper substrate with 10 µm of AuSn solder. The gate finger width is 124 µm. **(b)** Lester Eastman's team at Cornell University has built GaN-on-diamond HEMTs that have a gate temperature that is half of that of their GaN-on-SiC equivalents.

GaN-on-diamond FET epiwafer is very similar to a GaN-on-SiC equivalent. This cost, coupled with excellent conductivity, makes this substrate a very attractive platform for wide-bandgap transistors.

Diamond platforms

CVD diamond is polycrystalline, so it is unsuitable for epitaxial growth and GaN epilayers must be transferred onto this material from another wafer. At Group4 Labs, which is based in Menlo Park, California, we have a proprietary process that can do just this. Our process removes GaN epilayers from their original substrates and atomically attaches them to smooth CVD diamond wafers (see box "How to make GaN-on-diamond wafers", p27). The most important and innovative feature of this process is that the heat-conductive substrate ends up just hundreds of nanometers below the transistor's active area. This results in exceptional heat spreading and conduction away from the heat source, while maintaining the substrate's electrical isolation and low microwave losses.

We use three key metrics to assess the quality of our composite GaN-on-diamond wafers: bonding yield; wafer bow; and the mobility of the HEMT's 2D electron gas (2DEG).

The bonding yield is defined as the proportion of the wafer's surface that contains GaN joined to synthetic diamond free from voids. This is currently evaluated by visual inspection under a microscope. The quality of the materials' surface preparation governs the bonding yield, which is typically 95%.

Minimal wafer bow is essential for the high-volume manufacture of GaN-on-diamond devices. We determined this bow by measuring the total-thickness variation (TTV) across our wafers with a surface profilometer. If optical lithography is used for device processing, then the TTV should be less than 50 µm over a 4 inch wafer, or less than 20 µm across a 2 inch wafer. Our state-of-the-art wafers currently exhibit TTV greater than 300 and 50 µm for 4 and 2 inch wafers, respectively, but these values can be driven down by optimizing our growth conditions.

Reductions in the HEMT's 2DEG mobility could be caused by dopant or dislocation diffusion. However, no changes in mobility have been observed from the transfer of the transistor to the diamond platform, according to Hall and photoluminescence measurements at various temperatures and resistivity maps. Photoluminescence mapping revealed that the aluminum composition remains unchanged to within the resolution of the measurement (<0.75% in composition), while Lehighton measurements of the 2DEG's electrical conductivity showed a change of less than 0.3% relative to the as-grown sample.

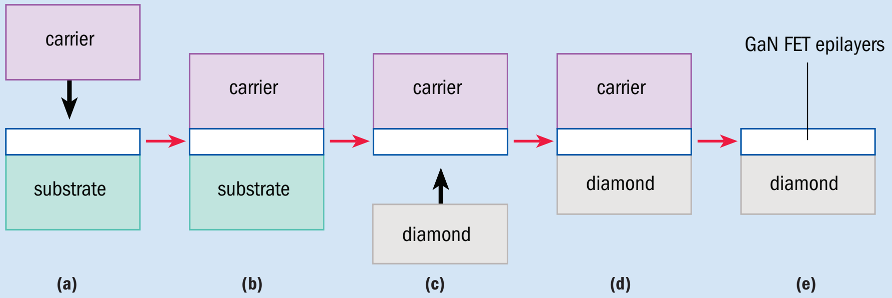
This evaluation is very promising, but challenges still remain. In particular, we need to establish the optimal process for managing the intrinsic diamond stress and the large difference in thermal expansion coefficients between various materials, which will lead to lower wafer bow. We have already found that free-standing wafers with thicknesses of 25–35 µm can be fragile and have produced GaN-on-diamond wafers with diamond thicknesses greater than 90 µm that have a lower bow. GaN epilayers that are either grown on silicon or attached to diamond are under tension at any temperature below that used for the processing, because GaN's thermal expansion coefficient perpendicular to the *c*-axis ($3.3\times10^{-6}\,K^{-1}$) is larger than that of silicon ($2.8\times10^{-6}\,K^{-1}$) or diamond ($0.8\times10^{-6}\,K^{-1}$). We attempt to balance this tension with a flexible silicon or quartz carrier wafer that has a counter-bowing action and can absorb the thermal expansion mismatches.

Early device results

GaN HEMTs incorporating our GaN-on-diamond wafers have already been built by researchers at the Air Force Research Labs (AFRL), Cornell University and TriQuint. AFRL announced the first-ever

Group4 Labs is producing 2 inch GaN-on-diamond wafers that are sampled to customers and partners fabricating various forms of devices that generate heat.

How to make GaN-on-diamond wafers



GaN HEMTs are usually grown on the (0001) surface of hexagonal GaN – the gallium face – because the intrinsic polarization associated with this surface aids the formation of an electron-accumulation layer. The preference for this face means that composite wafers comprising GaN-HEMT epilayers on diamond must also have this surface exposed.

Exposing the gallium face requires two epilayer transfer steps. But before this can occur, epilayers must be grown on a suitable substrate, such as silicon, sapphire, SiC or AlN **(a)**. After growth, thin dielectric layers are added to protect the GaN surface and enable bonding to a sacrificial substrate, such as silicon. The sacrificial substrate is attached with a bonding fixture that provides ample uniform force. An elevated temperature ensures that there is a strong bond **(b)**.

The original substrate, which in our case is silicon, is removed by polishing and a chemical etch that stops on the underlying AlN and GaN layers **(c)**. The GaN epiwafer's back surface is then chemically prepared for CVD diamond attachment. Once the bonding has occurred, the GaN HEMT's active junction is located within hundreds of nanometers of the highly conductive CVD diamond layer. The sacrificial carrier and the underlying glue layer are chemically etched away **(e)** and the composite wafer is then ready for processing into electronic devices.

results using this approach late last year, which were produced on unoptimized GaN-on-diamond materials. The researchers observed clear transistor behavior and demonstrated that 2DEG characteristics persisted during the transfer from silicon to free-standing diamond.

Cornell has carried out a side-by-side comparison of GaN-on-diamond and GaN-on-SiC devices. The GaN-on-diamond devices benefit from a two-fold reduction in junction temperature, thanks to the superior thermal conductivity of CVD diamond (figure 1b, p26), based on DC measurements that monitor the device gate temperature with a thermal probe directly over its center. More localized measurements have also been made with a ThermoMicroscopes' AFM-based scanning thermal microscopy system that can reveal the channel temperature as a function of dissipated power density. The SiC-based device produced a temperature rise of 12 °C/(W/mm), while the diamond-based equivalent increased by only 6 °C/(W/mm).

Further characterization of the GaN-on-diamond HEMTs by Cornell revealed a unity-current-gain frequency (f_T) of 53.4 GHz, a power-added-efficiency of 47% and an output-power density of 2.79 W/mm at 10 GHz. These transistors, which have a gate periphery of 250 µm, deliver a full-channel current of 1.03 A/mm at a gate-source voltage of 0 V, produce a peak transconductance of 376 mS/mm and have a contact and sheet resistance of 0.87 Ω/mm and 401 Ω.

TriQuint's GaN-on-diamond HEMTs have a 50 µm gate width, excellent pinch-off performance, a high current density of 800 mA/mm and peak transconductance of 180 mS/mm. At a drain voltage of 10 V, these transistors produce an f_T of 12.3 GHz and a maximum oscillation frequency of 21.8 GHz.

Although GaN-on-diamond HEMT development is still in its infancy, the addition of diamond is already having a positive impact on transistor performance. It should come as little surprise that many engineers are starting to consider using this technology for new applications previously hindered by heat. These include compact low-cost terahertz sources for X-ray category airport security systems and high-power ultraviolet, blue and green laser diode sources for storage and lithography systems.

GaN-based terahertz sources currently have extremely low efficiencies, which limits their output powers. Ramping up the output power is not necessarily the solution, because this drives up the power densities on the chip and ultimately destroys the device, unless it has superior heat-management capabilities. GaN laser diodes are needed in very heat-intensive applications, such as optical data storage, biomedical laser treatments, deep sub-micron lithography, spectroscopic analysis and high-brightness optical displays. These diodes are temperature-sensitive devices with highly concentrated heat sources, but an exceptionally heat-conductive substrate can improve lasing operation through direct heat extraction from the heat-generating active junction. This means that the active region of the diode can be maintained at a cool, steady temperature.

In the short term, we will strengthen our GaN-on-diamond wafer products by reducing the bow in our 2 and 3 inch wafers. We will also continue to sample these wafers to our customers and partners who fabricate various electronic devices. As the quality of GaN-on-diamond wafers improves in the months to come, the devices that use this platform will improve and emphasize the benefit of this highly conductive composite.

Further reading

G H Jessen *et al.* 2006 *CSICS* 271.
J G Felbinger *et al.* (in press) *Electron. Device Lett.*
D Dumka *et al.* 2007 *Devices Research Conference.*

About the authors

Group4 Labs' **John Wasserbauer** (top left), **Firooz Faili** (top middle), **Dubravko Babic** (top right), **Daniel Francis** (bottom left) and **Felix Ejeckam** (Felix_Ejeckam@Group4Labs.com, bottom right) have all contributed to the development of GaN-on-diamond wafers. They are grateful to John Blevins (program manager at AFRL), the AFRL, the Missile Defense Agency and Mark Rosker (program manager at DARPA) for their generous support of the development of GaN-on-diamond technologies in recent years.

MBE RESEARCH

Nanostructures enhance IR detectors

The desire for detectors that are fast, efficient and free from cooling has fuelled the development of several new classes of infrared (IR) device. Three alternatives capable of two-color operation were highlighted at this year's North American Molecular Beam Epitaxy Conference, which was held on 23–26 September in Albuquerque, NM.

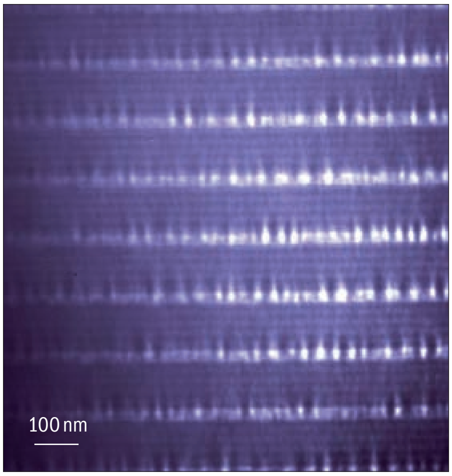
These devices can be employed for various civilian and military applications, including night vision, medical diagnostics and gas detection for environmental monitoring and astronomical observations. For many tasks there is a choice of detector, but each type has its own weaknesses. Microbolometric detectors have a slow response time but can operate at room temperature, while HgCdTe, bulk InSb and quantum-well IR photodetectors are faster but need cryogenic cooling.

Quantum-dot IR detectors are one promising type of device, according to Keh-Yung "Norman" Cheng from the University of Illinois at Urbana Champaign (UIUC). He believes that these low-dimensional structures have the potential to combine speed with freedom from cooling, while offering the advantage over their quantum-well-based equivalents of a strong photoresponse to normal-incident radiation. However, individual quantum-dot layers have low detection efficiency, and addressing this weakness simply by growing more of them is not easy because it tends to produce strain dislocations in the epitaxial layers.

Cheng has been able to avoid these strain issues by fabricating quantum-wire IR photodetectors through a process called strain-induced lateral-layer ordering (SILO). Wires are formed by growing short-period superlattices, which contain alternating layers of InAs and GaAs, with sufficient strain to drive an *in situ* lateral compositional modulation. These wires are typically 12.5 nm high, 10 nm wide and have a density of $10^6\,\mathrm{cm}^{-1}$.

Cheng's research team at UIUC has produced several different devices based on the SILO technology, including a detector that consisted of 20 regions of short-period superlattices, which each contain 10 pairs of InAs/GaAs. Devices with a 150 µm × 150 µm detecting area were formed from epiwafers using standard photolithography and wet chemical etching.

This device produced spectral responses at 6.3 and 4.1 µm, which were the results of a bound-to-bound transition and a bound-to-continuum transition, respectively. The strength of the response at each wavelength depended on the device's bias and peaked at 3 mA/W. "This device offers the possibility for integrating two or three detector wavelengths in one structure," remarked Cheng.



UIUC

Cross-sectional transmission electron microscopy images reveal the quantum wires fabricated by Cheng and co-workers at the UIUC. The wires were formed by strain-induced lateral-layer ordering.

Another class of IR photodetector is the quantum-dot-in-a-well (DWELL) design, which contains quantum dots embedded in a quantum well. Such a device also delivers a two-color response, which can be tuned by biasing. However, this detector suffers from low quantum efficiency, according to Rajeev Shenoi, a member of Sanjay Krishna's group at the University of New Mexico.

Shenoi explained that he and his co-workers had managed to boost efficiency by increasing the number of active periods within the device. This required a new DWELL design that minimizes epilayer strain through a reduction in indium content and involved optimization of the dot, well width and capping layers. At the heart of the improved structure are layers of InAs quantum dots, which were grown with 2.4 monolayer coverage, embedded in a quantum well made from 1 nm of InGaAs and 6.85 nm of GaAs. These layers are surrounded by 50 nm thick AlGaAs barriers.

The researchers produced photodetectors with 410 µm × 410 µm mesa structures containing circular apertures ranging from 25 to 300 µm in diameter and an active region consisting of 30 stacks of the optimized DWELL structure. These devices featured a range of InGaAs cap thicknesses and were grown on GaAs substrates in a VG Semicon V80H MBE reactor.

As expected, these detectors produced a two-color response, with sensitivities at 8.9 and 10.5 µm, associated with the electron transition from the dot to the AlGaAs barrier and from the dot to the GaAs shoulder, respectively. The addition of a 1 nm thick InGaAs cap boosted the shorter wavelength response, says Shenoi, but did not influence the longer wavelength. With this design, the detector delivered a response at 8.9 µm of 7.54 A/W under 4 V bias when it was cooled to 77 K.

Shenoi says that his future plans include incorporating the device into focal plane arrays and optimizing the barrier width.

Another promising class of IR detector is based on the InAs/GaSb superlattice. These devices could offer high-temperature operation, thanks to the large electron-effective mass in the superlattice, which cuts tunneling currents and Auger recombination rates.

According to Elena Plis, who is a member of Krishna's group, the standard superlattice detector is based on a photodiode design that is hampered by Shockey–Read–Hall centers and surface states – both significant sources of noise. Plis says that these problems can be avoided by turning to an nBn structure, which features a thin n-type narrow-bandgap contact layer, a 50–100 nm thick wide-bandgap electron barrier and a thick n-type narrow-bandgap absorbing layer.

The inventors of the nBn structure – Shimon Maimon and Gary Wicks from the University of Rochester, NY – had significantly improved the operating temperature of their InAs detector. Plis and co-workers have attempted to transfer this benefit to InAs/GaSb superlattice structures.

The researchers from New Mexico University initially fabricated nBn structures on tellurium-doped GaSb substrates, which comprised a 500 nm n-type superlattice, a 100 nm undoped $\mathrm{Al}_{0.4}\mathrm{Ga}_{0.6}\mathrm{Sb}$ barrier, a 2.5 µm undoped superlattice and an n-type superlattice cap. "The room temperature performance of our nBn detector is comparable to state-of-the-art pin detectors," remarked Plis.

Plis and colleagues went on to build dual-color detectors with similar structures, which feature InAs/GaSb and InAs/InGaSb superlattices and had cut-off wavelengths of 4.5 and 8 µm, respectively. When a bias is applied, the relative response from each of the two superlattices is altered significantly and a dual-color response can be produced at 77 K by adjusting the bias from 0 to 100 mV.