COMPOUND SEMICONDUCTOR

July 2007 Volume 13 Number 6

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

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ZnO nanowires generate power for biosensors

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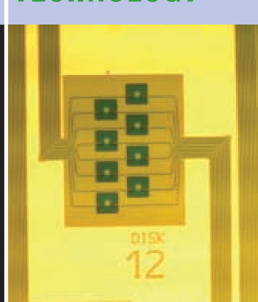

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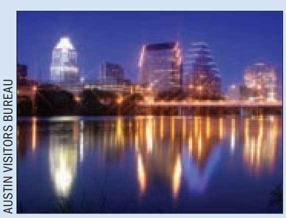

AUSTIN VISITORS BUREAU

Downtown Austin
This year’s CS Mantech took place in Austin, Texas. p19

Main cover image: *Wireless sensors embedded in the human body could provide a fantastic diagnostic tool, but powering them is a problem. A team from Georgia Tech believes that ZnO nanowires may hold the solution. This false-colored micrograph shows flower-like nanostructures produced with a tin catalyst. The nanowires produce a tiny electrical signal when exposed to ultrasound. See p16. Credit: Georgia Tech.*

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EDITORIAL

UK sees the light

Much has been said about the demise of the manufacturing industry in the UK. France, Germany, Japan and the US all remain major players in automobile industry, for example, whereas cars made by genuinely "British" companies are now a very rare thing.

Surprisingly, the UK is still a major force in the European semiconductor industry. According to SEMI Europe president Heinz Kundert, with 50 currently operational fabs, the UK's semiconductor manufacturing footprint is second only to Germany's (88) in the region.

But one area where the UK has lagged behind the rest of the world is in light-emitting diodes. Despite undoubted expertise at its universities, and plenty of innovative lighting companies to exploit the technology, there is no LED chip manufacturer in the country at present.

The fault lies partly with the UK government and is perhaps a legacy of the almost entire lack of any UK politicians with a scientific background. For all its fervent politicization of the climate change issue, the government has appeared oblivious to the possibilities that LED-based lighting offers. Unlike Japan, Korea, the US and China, there has been no national drive to develop the technology.

"The UK has lagged behind in developing LED technology."

This is a strange state of affairs, given that lighting accounts for fully one-fifth of global electricity consumption (International Energy Agency figures) and presents one of the biggest opportunities to cut carbon dioxide emissions without applying the brakes to economic growth. No, the UK's political elite is, for some reason, much keener on telling its subjects to do things like recycle their potato peelings into garden compost than to spend their taxes wisely and help develop technological solutions.

Things may at last be changing. Prompted by Cambridge professor Colin Humphreys, questions have been raised in both Houses of Parliament: why is there no national program? Why haven't simple calculations been performed to show how LED-based traffic lights would cut emissions?

Answers to those questions are not particularly encouraging, but recent moves by the Department of Trade and Industry suggests some progress. The decision to fund the development of GaN-on-silicon LEDs, with an eye on future volume production within the UK, is a high-risk, but potentially very high reward, strategy. Let's hope it is a sign of things to come.

Michael Hatcher *Editor*

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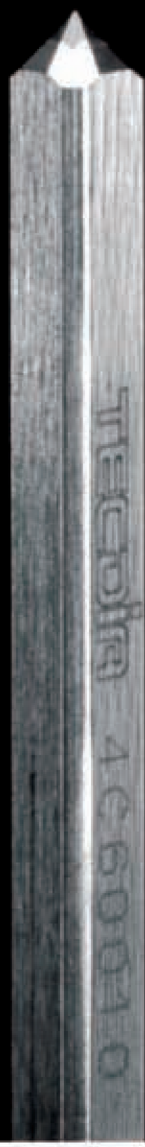
Japanese Quality Standard In Diamond Scribing



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US LIGHTING POLICY

$20 m prize challenge for LED makers

By Andy Extance

The US government is debating legislation including proposals to set minimum lighting efficiency limits and introduce prizes for solid-state lighting worth $20 million.

The CLEAN Energy Act of 2007 estimates that more efficient lighting technology could reduce annual electricity costs in the US by $18 billion, equivalent to energy produced by 80 coal-fired power stations each year. The Act has been passed by the Senate, although it may change significantly before becoming law.

Eric Richman, a senior research engineer at Pacific Northwest National Labs and an expert in lighting technology, commented: "The performance limits for lighting technologies are aimed at eliminating the least efficient versions in order to save US energy."

The Act also specifies that three "bright tomorrow" prizes for solid-state lighting should be established. They include a replacement for 60 W light bulbs, a halogen lamp replacement and a 21st century lamp prize for fixtures attaining efficacies of 90, 123 and 150 lm/W respectively, amongst other performance conditions. The prize for replacing luminescent bulbs is the largest, at $10 million, with the other two challenges worth $5 million each.

While some expected the Senate to limit and eventually to eliminate the use of incandescent bulbs, Richman was less certain: "In spite of the current legislation, I do not believe we will see complete bans of incandescent lighting in the near future."

High-profile policies intended to phase out incandescent sources in California, Ottawa and Australia have received much attention, but the real scenario is more complex, as Richman points out: "Most of the legislation offers some sort of exemption list. In this case, manufacturers could simply switch production and continue incandescent lamp production until different legislation emerges."

"The efficiency performance limits of the new Act will restrict production of certain lower efficiency lighting products, but there is no real push to replace them with another technology such as LEDs."

Despite being passed by the US Senate, a raft of amendments are still expected. Whatever final form it takes, the inclusion of lighting and LEDs in the debate must represent an important milestone for solid-state lighting.

ACQUISITION

Philips to grab Color Kinetics for $0.8 billion

Dutch giant Philips is set to purchase LED lighting specialist Color Kinetics (CK) for $34 per share, or $791 million, assuming the deal clears all regulatory hurdles.

CK will operate under the name "Philips Solid-State Lighting Solutions" and the new set-up will retain CK's current management. "Color Kinetics has a very strong position in the US, but integrating with Philips will help open up other markets," said Philips.

CK's headquarters will move from the prestigious location in the center of Boston, behind the meeting house from which emerged the Boston Tea Party uprising, to Burlington, Massachusetts.

"This acquisition uniquely positions Philips as a major player in the fast-growing SSL business with technology, expertise and intellectual property in all parts of the value chain of integrated LED-based lighting solutions," said Theo van Deursen, CEO of Philips' lighting division.

Philips has now acquired some of the most prestigious companies in LED lighting. Having bought Lumileds in August 2005, it completed the acquisition of TIR Systems just a week before announcing the CK deal.

A spokesman for Philips confirmed the predictable threat posed to existing suppliers to CK: "It makes all the sense in the world to use Lumileds LEDs now and exploit the synergies there."

"Lumileds is very strong in producing dice, TIR Systems is particularly strong in the middle part of the value chain, making modules which fit into lamps or luminaires," said the Dutch firm. "Now Philips owns Color Kinetics, our LED lighting line is further integrated still."

COLOR KINETICS

Color Kinetics' products include this versatile strand of 50 individually controlled white LED nodes. The durable, flexible design allows for dynamic points of white light to be installed across nearly any interior or exterior surface – walls, ceilings, floors, and three-dimensional sculptures and set pieces.

CELL PHONES

Qualcomm ban may hit Anadigics and TriQuint

An impending ban on US imports of new 3G cellphone handsets based on Qualcomm chipsets could spell bad news for GaAs specialists TriQuint Semiconductor and Anadigics. That's according to Aaron Husock, an analyst at Morgan Stanley who covers many of the companies involved in the US cellular business.

The ban is set to result from a ruling by the US International Trade Commission (ITC) in response to a complaint against Qualcomm that was filed by its rival Broadcom back in June 2005.

The ITC has issued an exclusion order, barring imports of the infringing chips and chipsets, as well as new models of 3G cellphones that contain them. The original Broadcom patent at the center of the case relates to power conservation in the advanced handsets, although Qualcomm maintains that Broadcom barely uses the technology.

Analyzing the likely effect of the ruling, Husock believes that, if implemented and sustained, the ban would have a threefold impact on the US handset market. Although the situation is complicated, his view is that the net effect on GaAs chip makers will be beneficial for RF Micro Devices and Skyworks Solutions; but that there will be a "modest" negative impact on Anadigics and TriQuint.

BROADBAND WIRELESS

WiMAX prospers as Anadigics and Nitronex build technology

Anadigics' InGaP power amplifiers (PAs) have been specified for use in reference designs of chipsets used in the development of WiMAX-enabled mobile phones.

The agreement sees the Warren, New Jersey, company's 2.5 and 3.5 GHz PAs included in WiMAX specialist Beceem Communications' BCS200 baseband and RF chipsets.

Sanyo is using the BCS200 chipset to develop a dual-mode CDMA/WiMAX phone, and Beceem says that its chipsets are also being used in "various Samsung WiMAX-enabled devices."

David Patterson, vice-president of marketing at Beceem, explained: "The operating efficiencies of Anadigics' WiMAX PAs, in conjunction with the reduced power consumption of the BCS200 chipset, provide compelling solutions for mobile WiMAX terminals."

The move builds on Anadigics' expertise in producing PAs for wireless access, the basis of a close relationship with Intel, which is responsible for 18% of the company's total sales.

Meanwhile, Nitronex has exploited its qualified GaN-on-Si process to boost the power output of its high-performance RF power transistors for broadband wireless base stations.

Two new devices operate at 190 and 240 W, and are designed for WiMAX and 3G/3G long-term evolution (LTE) in the 2.3–2.7 GHz range.

Nitronex's CTO Kevin Linthicum said of these products: "The 802.16e and LTE systems want to pack more power into ever smaller footprints, while increasing channel bandwidth and peak-to-average ratio. Nitronex devices, based on our SIGANTIC process, are ready to meet these challenges."

Having also recently entered the WiMAX base station business in its joint venture with Toshiba, Nortel demonstrated its take on the "mobile broadband" experience at June's NXTcomm show in Chicago.

Talking to *Compound Semiconductor* about the networking company's base station project, Gerry Collins, wireless business director for Europe, the Middle East and Africa, said: "Nortel and Toshiba will jointly develop WiMAX base stations offering low power consumption, high reliability and miniaturized equipment."

COMPANY FINANCE

Disciplined Skyworks is "undervalued"

By Andy Extance

The future is looking bright for Skyworks Solutions, with a new analyst report predicting that its sales will grow 8–10% each year, along with rocketing profits.

Aaron Husock, of Morgan Stanley Research, adds that Skyworks has been undervalued in comparison with the number one power amplifier (PA) maker, RFMD.

Speaking in late May, Husock said: "Skyworks is trading at a 27% discount to RFMD – despite 2007 operating margins expected to be more than twice those of RFMD."

Although Husock admits his analysis has a more optimistic outlook towards the Woburn, Massachusetts, company than many of his peers', his report cites the differing mixes of wideband CDMA (W-CDMA), transceiver and non-linear products as favoring Skyworks, which he perceives as leading RFMD over the development of W-CDMA PAs.

He expects the firm to benefit from Nokia and Qualcomm's efforts to make W-CDMA more widely available in the handset market, despite "minimal sales to Nokia".

Both RFMD and Skyworks are likely to gain from the move towards integrated front-ends for handsets, which incorporate switches, filters, duplexers and passives into one unit and can sell for up to three times as much as a standard PA.

By contrast, Husock presents a negative view of the transceiver market, which constitutes 33% of RFMD's sales but only 10% of Skyworks'.

Skyworks' "linear products", the collection of non-handset devices for base stations and GaAs-based wireless LAN front-ends, should also provide a welcome bonus, with Husock predicting 20% annual sales growth for several years in this business.

But his report also sounds a note of caution over the price erosion of front-end modules and W-CDMA, which is likely to accompany the increase in numbers of handsets containing these components.

MTT-S SHOW

Toshiba launches first GaN HEMT

Toshiba is adding the first GaN HEMT product to its commercially available microwave amplifier range. Supplied by the Toshiba America Electronic Components (TAEC) arm of the Japanese business, the TGI8596-50 operates in the X-band of the electromagnetic spectrum.

TAEC, based in Irvine, California, is targeting radar systems and medical tools, including devices for the treatment of cancer, as the main-end applications for its new amplifier. The firm also hopes to extend its GaN HEMT offering to the C- and Ku-bands for satellite-communication applications.

"GaN HEMT amplifiers have the potential to achieve significantly higher gain and output power than GaAs FETs at comparable frequency and input power," explained Homayoun Ghani, business development manager for microwave, logic and small signal devices at TAEC.

The TGI8596-50's output signal falls in the 8.5–9.6 GHz range of the X-band, offering a power output of 50 W and a typical gain of 9.0 dB. The device was showcased at the recent MTT-S International Microwave Symposium in Hawaii, alongside Toshiba's conventional GaAs microwave amplifiers.

Also showcasing their latest GaN-based components in Hawaii were RF Micro Devices (RFMD) and Cree. Cree says that its new CGH40025 general-purpose device is the smallest 25 W transistor available in the industry, delivering 14 dB of gain and a drain efficiency of 55% when used in a 3.6 GHz amplifier.

At its booth, the Durham, NC, company also demonstrated a broadband power amplifier (PA) based on its existing CGH40045F transistor. The PA produces 15 dB gain, a saturated output power of 50 W and 45% drain efficiency over the 0.5–2 GHz bandwidth.

Meanwhile, RFMD presented its latest GaN transistors. Eyeing a total addressable market that it believes to be worth $1 billion, RFMD introduced five 48 V GaN power transistors. Volume production should begin in the second half of this year.

The five unmatched power transistors in the RF393X product family range in output power from 10 W to 120 W, offer a wide tunable bandwidth, gain of 14–16 dB and a peak drain efficiency of 65% at 2.1 GHz. With customers in the pipeline, RFMD estimates that these types of power transistors will account for $150 million of the emerging market.

CEO Bob Bruggeworth said: "The company is engaged with top-tier companies in multiple markets and expects to commence production in the second half of 2007."

RFMD is hopeful of applying its existing customer relationships and expertise in GaAs device production to the emerging GaN market in applications like high-power radar and cellular infrastructure.

But, whereas its GaAs operation is based on in-house epiwafer production using MBE, RFMD's GaN-based products are fabricated on SiC substrates using MOCVD.

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...Sirenza beats noise record

Sirenza claims that it has produced the first GaN power amplifier (PA) with an output power above 2 W and a noise factor below 1 dB, encompassing the 0.2–8 GHz range.

"What is exceptional about this amplifier is the fact that it exploits both the low-noise and high-power capability of the GaN HEMT device technology," explained Kevin Kobayashi, executive engineering fellow at the company.

"We describe fully monolithic solutions which suggest reproducibility and scalability for MMIC applications," he added. "Until now MMIC-matched low-noise amplifiers have been limited to linear output of 1 W or less and noise figures above 1 dB over a multi-octave bandwidth in the S- and C-band frequency range."

...Samsung funds SiGe

Samsung has led a round of venture funding in SiGe Semiconductor. The Korean firm's first investment in SiGe forms the largest part of a $20 million injection that features additional funding from previous investors Venture Capital and TD Capital Ventures. SiGe will use the cash to expand its customer base and develop its Wi-Fi, WiMAX and GPS product lines.

Bill Burke, CFO of SiGe, said: "There's a lot of money being put around out there towards developing WiMAX products."

RESEARCH

US invests a further $13.3 m in solid-state lighting

The US Department of Energy (DoE) has selected eight more solid-state lighting (SSL) research and product development projects that will receive total funding of $13.3 million. Cree, Sandia National Labs and the University of California, Santa Barbara spin-out Inlustra Corporation are among the recipients.

Two of the projects from the initiative share $5.5 million and will be focused on developing or improving commercially viable materials, devices or systems. The other six projects, which share a $7.8 million pot, will aim to close key technology gaps and significantly advance the SSL technology base.

Cree is running one of the product-focused projects to develop a platform for high-efficiency commercial luminaires. The ultimate goal is to produce a 110 lm/W lamp module emitting at a color temperature of 4100 K that can be integrated into a 1400 lm luminaire.

While organic LEDs also feature heavily in the DoE program, another III-V project is headed by Inlustra Technologies. Inlustra is aiming to improve the internal quantum efficiency of blue and particularly green InGaN LEDs by using non-polar GaN planes.

Sandia National Laboratories is targeting improvements in growth efficiency and control of indium incorporation, which should lead to an increase in InGaN internal quantum efficiency.

Other projects involve a collaboration led by Yale University and involving Brown University, which aims to enhance LED device efficiency through nanotexturing, while Carnegie Mellon University, which is supported by the University of Michigan, hopes to improve LED efficiency by solving fundamental issues of semiconductor physics.

Success in these eight projects will push the DoE towards its 2025 goal of developing advanced SSL technologies that have a product system efficiency of 50%, with lighting that accurately reproduces a sunlight spectrum.

EPIWAFER PRODUCTION

Ambitious EpiLEDs speeds epitaxy ramp

Recently formed Taiwanese LED producer EpiLEDs has ordered two Thomas Swan "Close Coupled Showerhead" reactors from the German MOCVD equipment maker Aixtron for large scale production of GaN chips.

EpiLEDs confirmed that the existing MOCVD tools from Aixtron at its facility in Tainan were already operating at full capacity. President Steve Ku said: "Aixtron provides us with speedy qualification and comprehensive support, so installation and ramp-up will be on schedule to meet the market's needs."

EpiLEDs' vice-president Mingsen Hsu told *Compound Semiconductor* that the new reactors, which support 30 × 2 inch wafer production, would be used to make chips for mainstream lighting and backlighting.

Set up as a joint-venture between ProMOS, a DRAM maker, and chip processing equipment vendor Hermes-Epitek in August 2006, EpiLEDs has already brought a number of blue and green high-brightness LEDs to market.

Its existing products are all based on InGaN/GaN technology grown on sapphire substrates, spanning the full range of backlighting, general illumination and outdoor display applications. Aixtron describes the Taiwanese firm as "very ambitious".

Cree's XR-E high-brightness LEDs feature in this new line of high-performance outdoor lighting systems launched by Beta LED, a division of US lighting company Beta Lighting.

The North Carolina chip company has also won a contract to supply the camping gear specialist Coleman with XLamp lights featuring XR-E and XR-C chips for its lighting products. On top of that, Cree has seen its XR-E chips light up a walkway on the Croatian riviera, a popular tourist haunt in Europe.

Cree has also now released a new version of its blue XLamp XR-E that is capable of producing a maximum output of 42 lm at a drive current of 350 mA.

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...UCSD spin-off bags $3 million

US start-up company Quanlight says that its novel dilute nitride technology will improve the brightness, cost and wavelength-stability of red LEDs. The firm, a spin-off from the University of California, San Diego, has won $3 million in venture capital, which it says will be enough to make the transition from the research and development stage to initial wafer production.

CTO Vladimir Odnoblyudov said: "The system is InGaNP, with a few percent of nitrogen [content]. It is pseudomorphically grown on a transparent GaP substrate, which eliminates the need for wafer bonding."

The company has been working with conventional liquid encapsulated Czochralski produced GaP material, although it is hoped that a collaboration with substrate specialist PVA Tepla will result in a vertical gradient freeze process that can produce crystals with lower defect densities.

...Tools selling fast at BOC Edwards

Vacuum specialist BOC Edwards has expanded its range of "gas abatement solutions" to include new Helios 6 and Spectra G systems, many of which are being deployed in new top-tier LED fabs in Europe and Asia.

Designed specifically for nitride MOCVD applications, the Spectra G tools are capable of handling volumes of gas that equate to the exhaust of up to five of the best-selling epitaxy reactors. The new, six-inlet Helios 6 is primarily aimed at customers using higher hydrogen flow processes, such as SiGe epitaxy and MOCVD.

...Lumileds expands capacity

Philips Lumileds has ordered an Aixtron AIX 2600G3 IC planetary reactor to further expand its LED production. The multi-wafer tool features automatic wafer handling and will be used to produce AlGaInP red-emitting devices.


The face of innovation
is changing

RESEARCH

UK funds disruptive GaN-on-silicon play

In a sign that the UK government is warming to the potential for LEDs to cut energy consumption, the country's Department of Trade and Industry (DTI) has backed two projects that are based on novel chip structures.

One is a £3 million ($5.96 million) effort that aims to drastically cut the cost of solid-state lighting by developing GaN emitters based on large-area silicon substrates. The second project, worth £1.2 million, will develop photonic crystal GaN LEDs for backlighting LCD displays.

GaAs chip manufacturer Filtronic, Qinetiq, LED-distributor Forge Europa, MOCVD equipment vendor Thomas Swan and Colin Humphreys' research team at Cambridge University are the five partners in the GaN-on-silicon project, which will run for three years. The DTI is supplying half of the funds, with the commercial partners contributing the remainder.

Humphreys told *Compound Semiconductor* that the critical motivation behind the project was to reduce the cost of high-brightness LED chips. The presence of Filtronic, which makes GaAs-based RFICs primarily for cellphone handsets and defense applications at its 6 inch fab, suggests that, for the first time, the UK may become a location for volume LED chip production – if the project is a success.

While virtually all commercially available GaN LEDs are based on either sapphire or SiC substrates today, both of these base materials have their drawbacks. Sapphire production has proved difficult to scale to large wafer diameters, while SiC remains relatively expensive. Cree has recently begun to switch its GaN-on-SiC LED production to a 4 inch platform, however.

According to Filtronic's optical business manager Steve Clements, the GaN-on-silicon technology must work on a 6 inch platform to be compatible with the company's high-volume MBE-wafer fab, which currently produces PHEMT structures for the likes of RF Micro Devices.

As Nitronex has shown, the GaN-on-silicon approach has proved practical for RFIC manufacturing; but for light emitters, the material combination remains extremely underdeveloped. Humphreys' research team at Cambridge has already demonstrated multiple-quantum-well LED structures on 2 inch silicon, although the light emission is not yet as good as from GaN-on-sapphire. "On 2 inch silicon, we have measured an internal quantum efficiency of 20%, which compares with something like 70% for sapphire," Humphreys said.

JOHN CARTWRIGHT

Question time: Cambridge GaN specialist Colin Humphreys has prompted Parliamentary discussion of LED technology, the energy-saving potential of which the UK government is finally starting to recognize.

The key challenge for the Cambridge team will be to show that the technology can scale to a 6 inch silicon platform and overcome the inevitable problems associated with strain that will arise at the larger wafer size. They have adapted their 6 × 2 inch MOCVD reactor for single 6 inch wafer growth and are now looking at how to cut dislocation densities, currently an order of magnitude worse than seen with sapphire. To do that, they are developing proprietary intermediate layers, which Humphreys says are the key to making the novel material system work.

If the Cambridge team is successful, Qinetiq, which is receiving a Thomas Swan MOCVD system under the DTI funding, will aim to reproduce the technology on a multi-wafer manufacturing platform and supply epiwafers to Filtronic for further processing into LED structures.

Compared with its counterparts in Japan, China, Korea and the US, the UK government has been relatively slow to pick up on the potential for LED-based solid-state lighting. Humphreys himself has tried to address this issue with the country's political establishment, prompting discussion of the technology in both Houses of Parliament. It now appears that this may be having some effect.

Aside from the Filtronic-led project, a team lead by Sharp Laboratories Europe has embarked on a two year effort to develop quasi-photonic crystal (QPC) structures to make 405 nm LEDs that could be used alongside red and green LEDs in dynamic backlights.

Sharp's role in the project, which has also received half of its funding from UK's Department of Trade and Industry, is to provide GaN material and expertise in system-level integration. The University of Glasgow and the Institute of Photonics, which is located in the same city, will carry out all the device fabrication. Mesophotonics, a spin-out of the University of Southampton, will provide design and modeling of the QPC structures.

According to the research team, the mass-fabrication technology developed in the project could also extend beyond the production of ultra-high-brightness LEDs and assist commercialization of next-generation nano-photonic and nano-electronic devices.

● There was a further financial boost for European LED chip development when Finland-based OptoGaN closed a $6.8 million venture-funding round led by the Nordic Venture Fund and Denmark's Via Venture Partners.

OptoGaN's CEO Bernd Meyer, previously at the quantum-dot specialist NL Nanosemiconductor (now Innolume), says that the Finnish start-up has access to manufacturing facilities in Dortmund, Germany.

GAN LASERS

BinOptics hoping to slash blue laser production cost

BinOptics, the Cornell University spin-out company that specializes in etched-facet lasers, has developed a continuous-wave 405 nm emitter that has a much shorter cavity than current commercial designs.

If the technology can be fully developed and scaled to volume production, it could allow three times more lasers to be fabricated on a given wafer and slash the cost of producing individual devices.

BinOptics CEO Alex Behfar told *Compound Semiconductor* that a new etched-facet process technology designed specifically for GaN lasers was the key to the latest development. As well as enabling the production of smaller laser chips the method allows on-wafer device testing, which could reduce processing costs.

Using a standard, chemically assisted ion-beam etching tool, specially adapted by the BinOptics team for GaN material, Behfar and colleagues were able to make continuously emitting blue lasers with cavity lengths as short as 100 µm and threshold currents as low as 10 mA.

Emitting 5–10 mW (the power is dependent on the cavity size), the lasers should be powerful enough for high-definition DVD playback and, with on-wafer lifetimes of several hours already demonstrated, their initial reliability looks promising.

Conventional processing relies on cleaving the wafer to define the individual laser facets, or mirrors, and results in a typical die size of 400 µm × 600 µm.

At that die size, a 2 inch wafer yields a maximum of 5000 chips. But using the etched-facet approach and producing lasers with a cavity length of only 200 µm would triple that potential yield to 15,000 lasers.

If the etching process can be applied on a large scale, it could help to cut the cost of individual blue diodes dramatically.

Like major manufacturers such as Sony, BinOptics is fabricating the lasers on expensive free-standing GaN substrates, of which Japan-based Sumitomo Electric Industries is the dominant supplier. However, the relatively small wafer diameters available and the number of defects in the GaN material system is hindering the drive to reduce the cost of the lasers through volume production.

"We need to complete the development [of the GaN lasers] and get our supply chain organized," Behfar said. "I would be very disappointed if we couldn't begin to sample a small number of blue lasers later this year."

The CEO added that he remains open to a variety of business strategies with which to move forward, including potential licensing deals with major chip manufacturers.

BinOptics obtains some of its epitaxial material from a partner in Japan, but hasn't ruled out the possibility of ramping up GaN wafer manufacturing at its own facility.

"We are planning not to need another round of [venture] funding," Behfar said. "But if we decide to adopt a more aggressive approach, for example doing MOCVD in-house, we might need to raise more capital."

FIBER-OPTIC COMPONENTS

Oplink finally seals OCP acquisition

Optical Communication Products (OCP) is set to come under the wing of Oplink Communications, thanks to an improved cash offer for outstanding OCP stock.

Despite an agreement between major OCP shareholder Furukawa Electric and Oplink, the acquisition had looked to be in serious jeopardy when OCP's remaining shareholders issued a so-called "poison pill" rights plan to protect their interests.

Oplink paid Furukawa $1.50 per share for 58% of OCP, but to win over the minor shareholders it was forced to increase its offer to $1.65 for the remaining 42% of the company.

The final value of the deal will be around $179 million and is expected to close by the end of the third calendar quarter of 2007.

Just one final hurdle remains – the merger agreement requires the affirmative vote of two-thirds of the outstanding OCP shareholding not yet acquired by Oplink.

OCP, which specializes in compound semiconductor-based products for applications in optical communications, acquired the Taiwanese chip-maker Gigacomm in July last year.

PHOTOVOLTAICS

Emcore's solar cell beats record

A record-breaking multi-junction cell from Emcore promises to usher in a new class of lightweight, high-efficiency solar arrays to power next-generation spacecraft and satellites, says the company.

Emcore's Albuquerque-based photovoltaics operation has come up with the so-called "inverted metamorphic" (IMM) cell design, which operates at a record conversion efficiency for space applications of 30.9% and is more than an order of magnitude thinner than conventional cells. The record for terrestrial concentrator cells is currently 40.7% and is held by Spectrolab.

Describing the latest developments, Emcore's VP and general manager of photovoltaics David Danzilio said that the new IMM architecture would cut down on the number of lattice defects seen in metamorphic structures.

In metamorphic solar-cell designs, junctions based on different materials are fabricated within the same structure. A composition-graded buffer layer is deposited between the different layers so that the lattice mismatch can be overcome.

However, the mismatch between germanium – the material used in the bottom layer of the metamorphic structure – and the other compounds means that lattice defects still mount up, restricting the cell's efficiency.

In Emcore's IMM design, the junctions are deposited in a different order, with InGaAs sitting on top of InGaAlP and germanium junctions in the final structure. "It's like growing the 'top' cell first," said Danzilio.

Because the inverted design absorbs sunlight more effectively, cells based on the structure are less than one-tenth the thickness of conventional structures, thereby saving on materials costs. Arrays based on the thinner cells would also be lighter and more flexible than current designs.

"The successful demonstration of this IMM cell represents the most significant improvement, in terms of watts per kilogram and dollars per watt, in the past decade," added Danzilio. "[It] will enable never-before-envisioned space-power applications."

The cells could also be used in terrestrial applications, where Emcore's current production devices already have a peak conversion efficiency of 37% under concentration.

Emcore is busy scaling up production of terrestrial cells to meet an expected boom in demand over the next several years. Speaking to *Compound Semiconductor*, Danzilio said that he expected the global market for solar-power systems to be worth between $7 billion and $8 billion by 2010.

Around 20% of that market could be served by systems based on multi-junction cells, equating to some $1.5 billion, he added. The photovoltaic element comprises anywhere between 10 and 20% of the system cost for multi-junction systems, suggesting that the market for terrestrial applications of III-V solar cells could be worth up to $200 million by 2010.

"We are at the leading edge of this at the moment, and have an [order] backlog of 20–30 MW," said Danzilio.

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...Finisar completes record year

Finisar posted record revenues of $419.2 million in the year ended April 30, 15% up on the previous year. Quarterly revenue was down 9.5% on the previous three months to $97.3 million.

The relocation of Finisar's VCSEL fab across Texas, from Richardson to Allen, had a detrimental effect on sales as customers used inventory reserves built up to protect against supply risks posed by this move.

"We've had some rocky waters that we've had to go through in the last quarter, but we're coming out of it," observed Finisar CEO Jerry Rawls.

...Bookham challenges YAGs

A new AlGaAs/InGaAs laser diode bar from Bookham, producing light at 1060 nm, will enter the market to compete with Nd:YAG lasers before the end of the year.

"We'll be looking at volume shipments in the third quarter of 2007, as there are key customers demanding an aggressive ramp on these products," said senior product-line manager Christian Naumer.

Bookham hopes that the modules will be readily able to break into medical applications, partly because the US Food and Drug Administration is already very familiar with systems operating at this wavelength.

LED APPLICATIONS

Hunter fires missive at 'toxic' rivals

Cree founder and former CEO **Neal Hunter** left the chip company two years ago and headed up the supply chain with the launch of LED Lighting Fixtures. **Richard Stevenson** hears his vision for a market dominated by LED-based lighting.

LLF

Why did you decide to leave Cree and start LED Lighting Fixtures (LLF)?
I left Cree for personal reasons. I had been there for 18 years and my role was in transition. I didn't think I was getting back in technology, but then Gerry Negley [former Cree employee] and Tony van de Ven [CEO of Lighthouse Technologies] approached me with an idea to try to push LEDs into the lighting industry.

All the lighting guys kept saying: "It's going to be 3–5 years, or 5–10 years before LEDs enter the lighting industry." We got tired of hearing that and thought that there was an opportunity for someone who knew the technology of the chips and those sorts of things. But we started out looking at a totally different application – not general illumination, but billboard lighting. However, through that process we discovered our core technology, which led us to very high efficacy, very high color rendering light.

I was not going to go back into a technology start-up without a very good team. Gerry and Tony are extremely brilliant inventors and scientists, and they have also been involved in start-up companies before, so it was an opportunity to get together with a really good core of people. And to add Mike Rogers, who was an executive vice-president at Cree, and Cynthia Merrell, who had been Cree's CFO, was incredible.

How difficult was it to get funding for this venture?
Very easy, because of our track record. We personally put some money in during our initial round with strategic partners, and we're right in the middle of what we call our "series b" round. We've only conducted one or two days of work on that and it looks like it will be totally oversubscribed. The industry is very exciting to a lot of investors right now and we've just got to make sure that they are excited for the right reasons.

We are an industry that gets very obsessed with what chips are used or whose product is in this, but we have to remember what the customer experiences. They don't care about chips, they care about the quality of light. They want to say that's warm light, I'm used to that, and it doesn't look like an LED. In our minds they don't want to see an LED, they just want to see light. If they know that it is very efficient, that's going to make them feel better. And if they know that they don't have to change it for years and years, that's going to make them feel good too.

That's where people miss the boat – even I did when I was at Cree. I would always think about chips and the packages, but it's really about the experience. You're trying to translate all that technology into a lighting experience for the customer.

Did you ever think of starting a fixture division within Cree?
It definitely could be done, but we never considered going upstream. We tried that in the 1990s with Real Color Displays, but we got our fingers burnt a little because we were a little bit early in the technology cycle. The general feeling among the board, or anyone at Cree, would probably be that it would not be of interest to the shareholders to go that far up the food chain.

What is your vision for LLF?
To become the next big lighting player. That's what you have to do to be successful. You have to drive a finished product to the end market, because anything in-between is not going to work.

We've got a lot of different products that we need to get into rapidly. We've invented a lighting platform and we need to distribute that platform across many different product lines.

How would you describe progress so far?
We've kick-started the entire industry. We've demonstrated 80 lm/W out of a fixture and our initial product will be 60 lm/W. That's a huge boost to the industry. Other fixture and bulb companies thought that they were going to be able to sit on this for a while, but now they are going to have to step up.

On the tactical side, we've got representation in 49 US states. That is something about which people said: "You can't do that, it will not be possible."

We have also had two of the of the largest fixtures houses in the US send letters to their entire field-sales

LED Lighting Fixtures launched the LR6 this spring. The fixture, which can simply be screwed into many existing lighting sockets, delivers 650 lm from 12 W and has a color-rendering index of 92.

force, telling them that if they carry our product line, then they are at risk of losing their license. That's flattery. We're a pre-revenue company and they have named us specifically. They are trying to – and this is typical old-style tactics – protect their turf by putting a wall up. That means that they are not innovating. But believe me, they are going to have to fill their line with an LED product at some point. We are creating movement across the industry.

Do you have many customers?
We have still not released our product finally, and I'd put our customer list in the 20–50 range. Initially we thought we were developing our products for the residential market, but there are many, many opportunities on the commercial side.

We are in with Friendly Ice-Cream Corporation, a 500-store chain in the US. We're starting a demonstration there and if it goes well, we will roll-out. We're getting a lot of that type of retail customer coming to us for demonstrations, but we're also getting into commercial buildings in the Midwest.

How does pricing and profit look?
We've got a defensible IP position on our core platform, so we think that that's going to provide for a good margin long-term. You've got to go in realistically and not overprice your products. We're trying to deliver a product, at around $75 to the consumer, that has maybe twice the output and performance of the other competing products, which are generally priced higher. No-one is going to win in this business unless you get the prices where they need to be.

Do you only source LEDs from Cree?
We're sourcing from Cree, but we have sourced from other suppliers as well. However, right now we are using Cree XR-E technology.

We want higher efficiencies, higher brightness, lower cost, like any other customer. That's been the LED mantra for years. But we also want to see better power-conversion products.

What about reliability?
It's obviously extremely important. The reason we picked the Cree XR-E is because of reliability. We're looking for testing data that's consistent within the industry, where we can depend on the numbers that are put out there. Many guys throw around this 50,000 hour number. How do you know that? What are your testing criteria?

There is a lot of responsibility on behalf of the fixture manufacturer to make sure you are getting good devices. But the higher the efficacy, the easier it is to make a good, robust fixture, because you are not dealing with as much heat.

Our fixture runs at 650 lm at roughly 12 W so you're dealing with a lot less heat than traditional LED fixtures, but you've still got to take care of it.

Do you see compact fluorescents (CFLs) as a threat to your future business?
Certainly. Everyone thinks that CFLs are going to go by the wayside. But even though they are more expensive, they put out a lot of light and for a lot of people they are okay. CFL adoptions are going up at alarming rates.

But that's good because it raises people's awareness for energy-efficient lighting. Our industry needs to make sure that we are not fighting with ourselves so much as trying to grow the industry. There is a tendency in the LED business to be hitting each other all the time and I think that gets some of the larger integrators less excited about going after some of these areas.

How is LLF different to other fixture companies working with LEDs?
We've got a different platform. Tony and Gerry have laid down some color properties that are totally different from anyone else's.

We also have IP that doesn't just deal with our color space and they way we put light together, but also deals with basic chip technology. So we've got knowledge all the way across the board.

Plus we have a team that's extremely experienced on all fronts, whether its finance or general management. Tony's run Lighthouse, Gerry's been involved in many start-ups, and Cindy's raised over $350 million in her career at Cree.

How can you compete with the big lighting manufacturers, such as Osram and Philips?
We'll have to see them on the battlefield I guess. The question is: how quickly do they want to cannibalize their fluorescent or incandescent businesses?

Right now you can also make one argument that they are knowingly putting devices that contain a toxin into the houses of all Americans and people worldwide with fluorescents. That's not a small issue, I think, with the legal system in the US. Eventually someone is going to figure that out.

We're going to be the non-toxic alternative. We already have a performance that's better than fluorescents, both in color quality and efficacy, and so I think that they are going to have to react to platforms like ours. We like our chances.

"We are going to be the non-toxic alternative."
Neal Hunter
LLF

Nanowires promise battery-fr

The battery has been a great servant for powering devices in situations where mains electricity is inappropriate, but it has its downsides, which include a relatively short life and a toxic composition. ZnO nanowire power generators are free from these weaknesses, and have the potential to drive small devices such as implanted biosensors, says **Zhong Lin Wang** from Georgia Institute of Technology.

About the author
Zhong Lin Wang is a Regents' Professor and College of Engineering Distinguished Professor at Georgia Tech. He was one of the world's 25 most cited authors in nanotechnology from 1992 to 2002 according to *Science Watch*, and has published more than 460 journal articles. He is also a fellow of the American Physical Society and the Amercian Academy for the Advancement of Science, and the winner of several prizes, including the 2001 ST Li prize for Outstanding Contribution in Nanoscience and Nanotechnology, a Sigma Xi 2005 Sustained Research Award, and the 1999 Burton Medal from the Microscopy Society of America. For more details see www.nanoscience.gatech.edu/zlwang. Wang thanks NSF, DARPA, NASA and NIH for their support, and Xudong Wang, Jinhui Song, Puxian Gao, Rusen Yang, Jin Liu, Jun Zhou, Sheng Xu and Ben Weintraub for their research contributions.

Researchers are developing wireless nanodevices and nanosystems for a variety of applications, such as monitoring changes in cancer cells, providing gas sensing in remote areas, and delivering *in vivo* measurements of blood pressure and blood sugar levels. All of these applications need a power source. In the case of an implanted wireless biosensor, this power can come directly or indirectly by charging a battery. But the toxic chemicals inside a battery are a potential health hazard, and so a better solution would be to create "self powering" sensors.

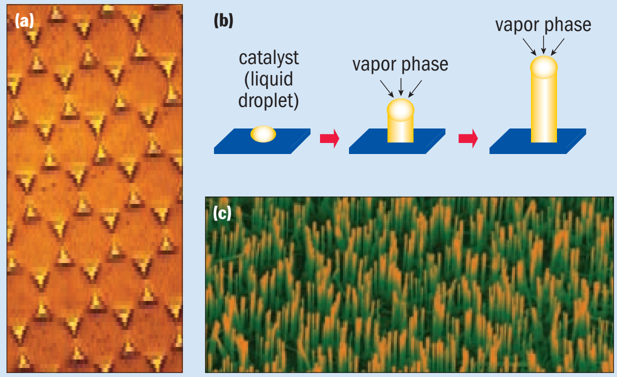
Unfortunately, alternative nanoscale power sources are almost non-existent, despite the great need for a non-battery alternative for many miniature sensing devices for biological sensing and defense applications. However, there are many other forms of energy that could drive nanodevices, such as mechanical energy that can come from body movement and muscle stretching, vibration energy from acoustic and ultrasonic waves, and hydraulic energy from the flow of blood and fluids in the body, and the contraction of blood vessels.

At the Georgia Institute of Technology in Atlanta we have invented a technology based on ZnO nanowire (NW) arrays that can harvest energy from its local environment. By combining the coupled semiconducting and piezoelectric properties of ZnO, and the huge elastic deformation that can be produced in NW structures, we can convert mechanical energy into electricity.

We have produced our aligned ZnO NWs, which are the essential building blocks for our nanoscale power generators, by physical techniques and chemical synthesis. The physical vapor–liquid–solid process produces the best quality material, but the chemical synthesis approach is better suited to volume production (see "ZnO nanowire growth and generator design" for details).

Now we have shown that prototypes containing these aligned ZnO NW arrays can convert mechanical energy into electrical power. The power generator couples ZnO's piezoelectric and semiconducting properties, and forms a Schottky barrier between the metal and ZnO contact.

ZnO nanowire growth and generator design



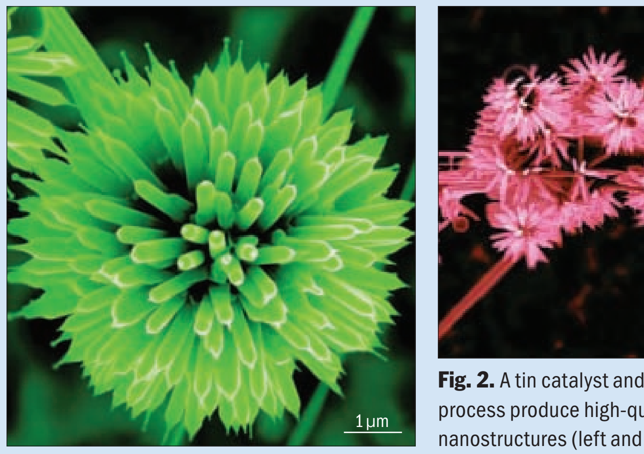


Fig. 2. A tin catalyst and ... process produce high-qu... nanostructures (left and ...

ZnO nanowires (NWs) can be produced by a vapor–liquid–solid technique (VLS) and a chemical synthesis process. The VLS process begins by taking a platform, such as a GaN thin film, and patterning it with gold particles that act as a catalyst to initiate and guide the growth. The patterned sample is placed in a tube furnace at 500 °C, and subjected to a vapor formed by heating ZnO powder and

graphite to 900 °C. By ... the growth temperatur... rates, ZnO NWs can be ... wafer that all point in t... due to the epitaxial ori... between them and the ...

Switching source ma... of ZnO, SnO_2 and grap... creates a selection of ... NWs morphologies, wh...

Harnessing the energy

We have evaluated our array's potential performance by using an atomic-force microscope (AFM) tip to deflect individual wires (figure 4a). When the tip comes into contact with a wire, it stretches one side of it and compresses the other. This produces a charge separation within the NW, with positive

ree powering of small devices

ig. 1. (Left) Growth of
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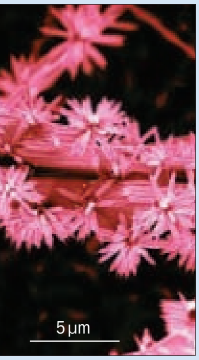

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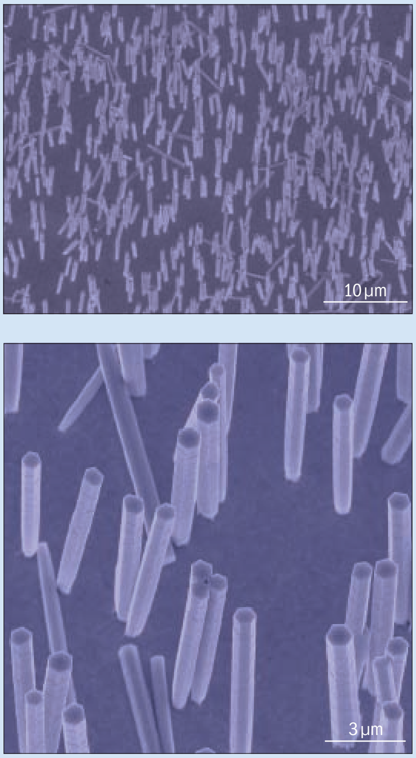

Fig. 3. ZnO nanowire arrays (above and top) for nanogenerators can also be built on polymer substrates that provide a flexible platform.

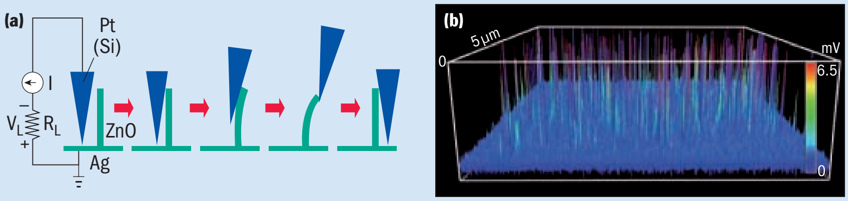

Fig. 4. The conductive tip on an atomic force microscope (AFM) can generate electricity through piezolelectric nanowire (NW) deformation **(a)**. The nanowire's root is grounded, and researchers apply an external 500 MΩ load that is much larger than the inner resistance of the NW. The AFM scans across the NW arrays in contact mode. An output voltage can be recorded as the AFM tip scans across the NW arrays **(b)**. Discharging is so quick that each event is only characterized by a couple of data points (see Z L Wang *et al.* 2006 for further information).

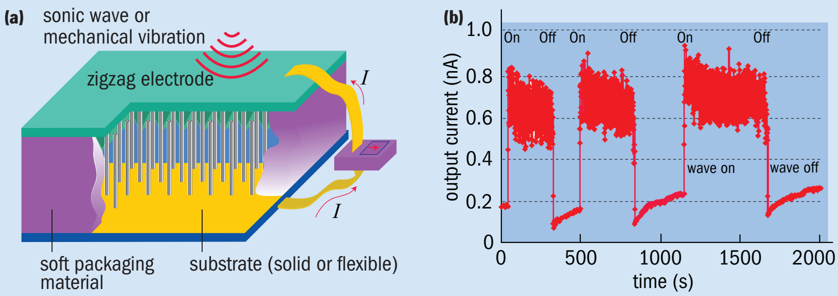

Fig. 5. A zigzag top electrode **(a)** can take over the role of the AFM tip for providing the bending and stretching required for electrical generation. A continuous output current is produced by driving the nanogenerator with an external ultrasonic wave or mechanical vibration. The plot **(b)** shows the output from a nanogenerator when the ultrasonic wave was on and off. Approximately 500 nanowires simultaneously contributed to the DC current (for more details see X D Wang *et al.* 2007).

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flowers (figure 2). This time a tin (Sn) droplet that dissociates from SnO_2 serves as the catalyst, on which many different configurations of ZnO nanostructures can be grown. The large tin droplet acts as a base for the growth of many NWs, and the far smaller tin nanoparticles govern NW growth. The tin nanoparticles are visible at the tips of the NWs.

We have also developed a chemical synthesis route for producing ZnO NWs, which is better suited to fabricating larger volumes of material. The technique uses a much lower growth temperature of 70 °C, and allows the substrate to be replaced with many other types of material, including polymers that are ideal for applications requiring flexibility and foldability, such as flexible electronics. Growth proceeds by suspending a gold-coated plastic substrate in a Pyrex glass bottle containing an equal molar aqueous solution of zinc nitrate hydrate ($Zn(NO_3)_2 6H_2O$) and hexamethylenetetramine ($C_6H_{12}N_4$), which is held at 60–80 °C. By optimizing the temperature, solution concentration, reaction time and substrate surface, ZnO NW arrays can be produced with controlled dimensions and orientation (figure 3).

and negative charges forming on the stretched and compressed sides, respectively. The Schottky barrier that is formed between the AFM tip and the NW preserves these charges. We have measured the electrical voltage produced by each of the NWs in an array just before they are disconnected from the scanning AFM tip (figure 4b).

The charging and discharging process produced by scanning the AFM tip illustrates how the NW array could generate electricity. We have subsequently converted this principal of operation into working nanogenerators built on a polymer substrate that can serve practical applications by overcoming three initial obstacles. The first of these involved no longer using an AFM to produce NW mechanical deformation, and refining our power generator so that it is adaptable, mobile and able to provide a cost-effective approach over a larger scale. In addition, we adapted our system so that all of the NWs generated electricity simultaneously and continuously, and all of that power was collected and used. Finally, we had to start to use a primary energy source that enabled the nanogenerator to operate "independently" and wirelessly.

A vertically aligned ZnO NW nanogenerator that produces electrical energy from ultrasonic waves has recently fulfilled all of these goals. The core of our new and innovative design is a saw-tooth-shaped electrode array that replicates the bending cycle created by the AFM tip. An external ultrasonic wave oscillates this electrode vertically or horizontally and causes the NWs to bend and stretch, leading to simultaneous generation of an electrical signal (figure 5a, p17).

Promising potential

Our array with approximately 500 NWs actively generating electricity has delivered an output of nearly 1 nA (figure 5b). As expected, this current ceases when the ultrasonic wave source is off. The current generated by the design is at the lower limit of the nanoamp to microamp range required to drive a nanodevice, and the power output is insufficient for this task. However, this result proves that our innovative nanogenerator design could be a promising solution to the problem of building a cost-effective, mobile and adaptable power source.

In practice, the energy that is fed into the nanogenerators is likely to be mechanical energy from the local environment. This is potentially compatible with our nanogenerator technology, which should produce electrical power by converting mechanical movement or hydraulic energy.

The way forward

We plan to continue to refine and improve the performance of our nanogenerator so that it can produce more power and harvest/recycle energy from its local environment. This further development will initially come from in-house research. However, we are also building a start-up company to commercialize some of our concept and prototype technology that the DC nanogenerators have established. These self-powering nanosystems will target a variety of important applications in implantable biosensing, wireless and remote sensing, nanorobotics, MEMS, and sonic-wave detection.

Further reading

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AUSTIN CONVENTION AND VISITORS BUREAU

Armadillos and BiFETs light up Austin

With the GaAs industry finally back in some kind of healthy balance, the mood at CS Mantech was as warm as the Texan sunshine. **Michael Hatcher** and **Andy Extance** soaked up the atmosphere.

CS Mantech has a reputation as something of a party conference, and with "racing" armadillos, cigar-rolling Fidel Castro lookalikes and the delights of Austin's 6th Street featuring heavily this year, it's not difficult to see why.

As well as the armadillos (whose races looked more like harassment than anything else), there was plenty for delegates to enjoy at the conference itself. In the customary "state of the nation" plenary, delivered this year by TriQuint Semiconductor CEO Ralph Quinsey, the upbeat but watchful tone of the week was set. "Business is good," he said. "Long term, it looks like it will be even better."

Quinsey's central message was that the GaAs IC portion of the compound semiconductor business reached a watershed in 2006, with the overcapacity of recent years finally being shaken off and supply matching demand. This is a healthy situation that should help to reduce the pricing pressure from powerful chip customers like Nokia and Motorola, something Quinsey would be very happy to see.

The key to the new-found equilibrium between GaAs device makers and their customers is largely the widespread acceptance of 3G cell phones. "3G is finally here in a material way [in the form of wide-band-CDMA]," said Quinsey. "Between 150 million and 170 million 3G phones will be sold in 2007."

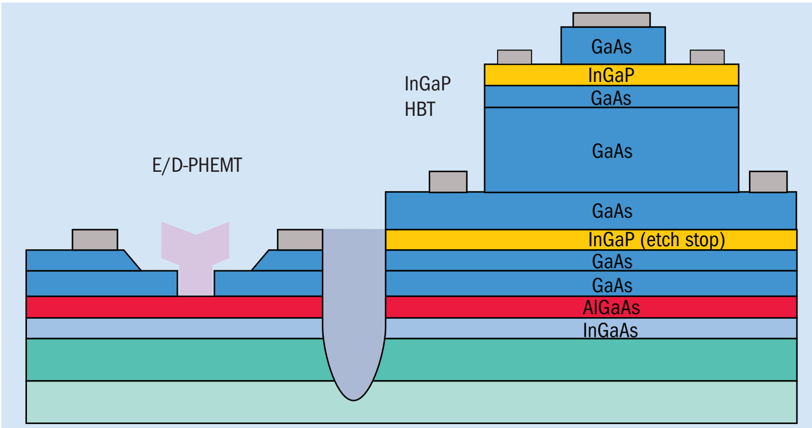
What with W-CDMA, WiMAX and LTE (long-term cellular evolution) already in the wireless lexicon, you would think that there were already enough acronyms to go around, but Quinsey introduced yet another – UMB, also known as "ultra-mobile broadband". It's a term that the CDMA development group is using to sum up the latest "next generation" in wireless communications. Scheduled for commercial roll-out in early 2009, one of its key features – as far as the GaAs community is concerned – is the use of multiple radios (multiple input, multiple output, or "MIMO") to support mobile broadband in the home, car, office, street and everywhere else you can think of.

With GaAs having seen off the threat of silicon-based radio power components thus far, it's reasonable to think that UMB, along with LTE, WiMAX and the rest of the wireless future will be dominated by the compound semiconductor at the power-amplifier stage. The bottom line is that more radios and amplifiers will be needed to support all those frequencies and MIMO designs, which is good for GaAs chip manufacturing companies.

"Value is moving back into the compound semiconductor space," Quinsey elaborated, comparing the current period of stability with the miserable five years from 2000 onwards, where commoditization and over-supply drained any value from the industry and limited investment opportunities. That said, he still doesn't expect to see major expansion in global chip capacity from the current level of just over 800,000 6 inch wafer equivalents, which should be enough to support requirements through 2011.

The future will not necessarily be plain sailing for everybody involved in GaAs production, however, with Quinsey predicting that mid-tier players could be forced to consolidate as the major volume

The 2007 International Conference on Compound Semiconductor Manufacturing Technology was held in Austin, Texas, on May 14–17, with 282 delegates and 56 exhibitors. Next year, the conference takes place April 14–17 in Chicago, at the Westin Chicago North Shore hotel.



WIN SEMICONDUCTORS

Integrated approaches to GaAs transistor manufacturing was a key theme in Austin, with WIN Semiconductors and TriQuint detailing new processes that are currently being qualified prior to volume production. Both are based on MOCVD and feature an InGaP HBT on top of a PHEMT structure. In WIN's device, shown here, an InGaP etch-stop layer is used to separate the devices.

suppliers, such as his own company and Skyworks and RF Micro Devices (RFMD), take increasing control of volume GaAs applications. Many of the lower-tier contenders have lost market share and become increasingly sidelined (one exception being a fast-improving Anadigics). As a result, the TriQuint CEO now envisages a scenario in which the industry increasingly splits into two distinct supplier bases that require different business models.

One of these will be for relatively low-end components used in the highest-volume market of personal voice and data transmission, mostly cell phones and laptop computers. The other, which will serve a much smaller niche in terms of chip and wafer volumes, will support unique applications and strategic needs, and perhaps be embedded within much larger organizations as part of a vertically integrated business.

When Quinsey said he saw no pressing need for major capacity expansion in the coming years, it's possible that he was taking into account the effect of BiFET innovations at GaAs manufacturers, who are shrinking more complex chip functions into smaller die sizes. Anadigics and Skyworks have pioneered this technology but as the Mantech session on the subject confirmed, it is spreading fast.

After Bill Peatman had shown the extent to which Anadigics has implemented its InGaP-plus approach to BiFET fabrication, launched in 2003 and now featuring in most of its circuit designs, the Taiwanese foundry WIN Semiconductors revealed details of its own new HBT-PHEMT process.

Called H2W, short for HBT and HEMT at WIN, this approach involves an InGaP HBT grown on top of an E/D-mode PHEMT, separated by 25 μm in the device design. Using MOCVD on 6 inch GaAs, the H2W process has now passed internal qualification, said WIN's C K Lin, and has shown good early reliability data and pulse I-V characteristics.

TriQuint is also taking integration one step further. Tim Henderson from the company's Hillsboro, Oregon operation stressed that using less GaAs and a smaller die size ultimately translates to a lower total system cost for the customer. His team's approach is to combine an HBT with a D-mode PHEMT and an E-mode PHEMT that sit side by side. The difficulty with this so-called BiHEMT is that, with the HBT structure on top of the PHEMT, the PHEMT mobility is affected. TriQuint engineers have adjusted the PHEMT epi-structure accordingly (see diagram).

Although still in the development phase, with plenty of qualification to be carried out, the approach could lead to an HBT-power-amplifier circuit combined directly with E/D-mode logic and control circuitry, RF switches and low-noise amplifiers. TriQuint is now working on improving performance with the development of a 0.5 μm gate process and ramping the overall scheme to volume production.

Skyworks' Ravi Ramanathan echoed the main reason behind BiFET development, however, "Everyone wants better efficiency," he said. "But the bottom line is cost, cost, cost."

One firm not yet pursuing the BiFET or BiHEMT route is RFMD. While there does not seem to be any likelihood of that changing in the near future, the firm is rumored to be looking at acquiring an additional fab – possibly Avago Technologies' Fort Collins site, currently used for E-PHEMT production.

DAVID IDDON

Texas hold'em: Armadillo racing provided entertainment at the conference's international reception.

GaN reliability proves popular

One new technology that RFMD is actively pursuing is GaN. The wide-bandgap material featured heavily in Austin, with three entire sessions and several other scattered talks reflecting widespread efforts to further develop and commercialize it for both RFIC applications and power microelectronics.

Reliability has proved to be the critical theme in recent years and judging by the number of delegates interrogating Nitronex's Samir Singhal after his talk, it still is. Singhal discussed the qualification of the company's NRF1 process, which is gathering steam for volume production of amplifiers used in WiFi and WiMAX infrastructure.

Toshihide Kikkawa, voted author of the best paper at last year's Mantech, updated delegates on Fujitsu's GaN HEMTs, focusing on the high efficiency that will be required to achieve the 100 Mb/s transfer rates expected for 4G wireless technologies at reasonable power consumption. At high power levels, gate leakage currents rapidly reduce this efficiency. Fujitsu has addressed this by placing a SiN layer over the top of the GaN layers in its device, but this led to an unwanted drop in threshold voltage. Kikkawa suggested that this was because the SiN layer traps electrons and showed that the effect on the threshold voltage was minimized by optimizing the quality of the SiN cap material.

Fumikazu Yamaki of Eudyna Devices also talked about cutting GaN HEMT leakage currents, this time by eliminating imperfections in the substrate material. He showed a strong correlation between devices with the highest leakage and areas of high defect density in the SiC substrate.

Optoelectronic Device Yield

By Frank Burkeen

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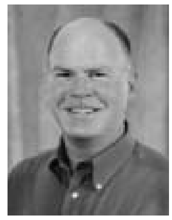

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The last decade has seen the evolution of many new optoelectronic devices which affect our daily lives. Automobiles, cell phones and PDAs, digital cameras, and computers contain an increasing number of microdisplays, high-brightness light-emitting diodes (HB-LEDs) and power devices based on compound semiconductor manufacturing techniques. With our ever-increasing consumption of these devices, this market growth and rapidly emerging technologies place tremendous pressure on manufacturers to get product to market.

Automated defect inspection has been a critical part of the semiconductor manufacturing process for detecting manufacturing problems early to reduce costs and increase product yield and performance. In the optoelectronics world, these defect inspection techniques translate as semiconductor wafer materials, in addition to silicon, are often used. The use of automated defect inspection has much less pervasive in optoelectronics wafer processing than in silicon wafer processing, but that is changing with the ever-present need to reduce costs and increase yield. A number of global manufacturing facilities are employing an Optical Surface Analysis (OSA) inspection technique that combines the elemental principles of scatterometry, ellipsometry, reflectometry, and topographical analysis to detect and classify defects in optoelectronic substrates and films.

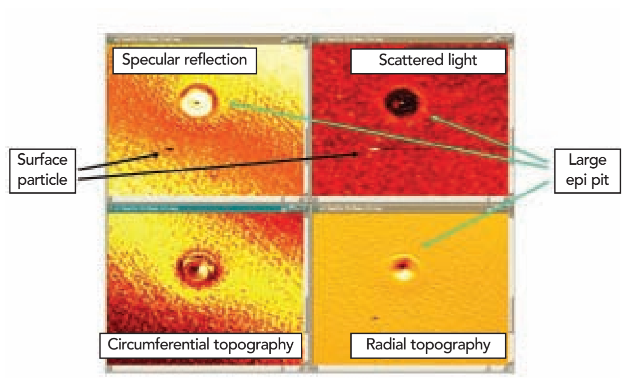


Figure 1: Defect images from four OSA signal types from a sapphire wafer with GaN epitaxial layers.

HB-LEDs

HB-LEDs are composed of multiple epitaxially grown layers of GaN and AlGaN, and are usually grown on one of two types of substrates: silicon carbide or sapphire. These have different advantages and disadvantages, but share one major downside. Due to the fact that the epitaxial layers are not latticed matched to the substrate, the defect density in the epitaxial layers is much higher than in homoepitaxial processes (such as in GaAs or Si epi layers). Fig. 1 shows the same portion of a wafer (about 2 mm by 2 mm in size), with two types of defects visible. The optical signatures for these two defects are clearly different and can be recognized separately by the OSA software.

POWER DEVICES

Some SiC-based power device manufacturers rely on manual microscope inspection with the process being very time consuming and not capable of finding all critical defects. OSA can be used to detect and classify defects in SiC substrates and epi layers automatically. As an example, the surface of GaN HEMT wafer contains an AlN buffer layer, a GaN layer, and an AlNGaN surface layer grown on a SiC substrate. Inspection can be performed in various stages of the manufacturing process of these devices. Fig. 2 shows a micropipe defect and a crystal defect commonly called a triangle defect, which only appears in topography signals. Micropipes appear as elongated defects in OSA images, making them easy to detect and classify.

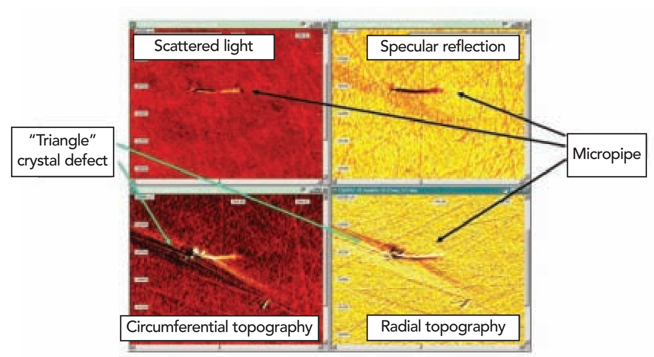


Figure 2: Defect images from four OSA signal types from a SiC wafer.

MICRODISPLAY

A new generation of CMOS imagers, LCoS displays, and digital light processing devices have been widely adopted into many consumer products. Many manufacturers have relied for years on manual microscope inspection making the process time consuming for 100% inspection. Inspection of the glass substrate and coated layers is challenging because defects such as stains from washing processes remain transparent and difficult to identify visually. Defects as small as 1 micron in size in advanced imagers have the potential to create blurry images where the manufacturer has to scrap the devices, thus lowering yields and profitability. The OSA system for glass wafer inspection is very sensitive to residues and other thin films

Manufacturers must find new ways to optimize their new product processes and decrease defect rates to stay profitable and competitive. Relying on manual optical microscope inspection is no longer an alternative at high volume rates and when every new device generation is more complex. Manufacturing processes require sufficient data about each and every process in order to create a defect yield management strategy that is effective and competitive. OSA technology can help manufacturers to automate the defect inspection process for optoelectronic devices, and this technology can be employed in incoming substrate inspection, post-clean wafer inspection, and after epi and film deposition processes.

Miro Micovic of HRL rounded off the reliability session with a look at typical failure mechanisms of GaN HEMTs. Two accelerated experiments and one real-time test identified oxidation at the AlGaN layer when the tests were performed in air, and under nitrogen an increased number of surface states between the gate and drain. Micovic suggested that hermetic packaging would significantly improve device reliability.

The GaN theme continued through a session focused on the development of electrical power devices. Wataru Saito of Toshiba began by estimating the size of the market for power electronics at \$8.4 billion, of which power MOSFETs constitute about half. The trend towards higher power density is now pushing the performance limits of silicon. GaN HEMTs have great potential as an alternative, but current collapse at high voltages is a big drawback. Saito identified the cause of the collapse in Toshiba's HEMT as trapping of electrons by imperfections in its GaN layer.

Eudyna's Eizo Mitani reported a record-breaking AlGaN/GaN HEMT grown on a SiC substrate. Presenting impressive figures such as 50% efficiency and 800 W output, Mitani claimed the highest power ever reported for an S-band transistor.

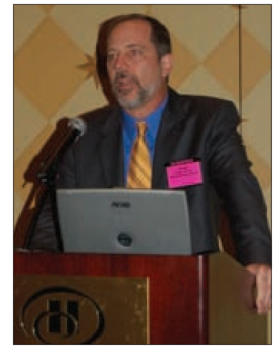
Switching to SiC-based power devices, SiCED's Peter Friedrichs said that the applicability of some manufacturing processes already established for silicon gave SiC technology a head start in attaining the power equivalent to "Moore's Law" – doubling power performance every two years.

The session on novel substrates was almost entirely focused on finding better material for GaN devices. Aixtron's Bernd Schineller demonstrated the company's early-stage development of vertical HVPE equipment for GaN boule growth. He suggested that a practical off-the-shelf solution for high-quality GaN substrate growth wasn't too far away.

Diamond protagonists arrived in force, and Patrick Doering of Apollo Diamond anticipated that Apollo's 2 inch wafers would be available at the end of 2007. He predicted, perhaps boldly, that 4 inch material would be available by 2009 at a similar cost to SiC.

Silicon-on-diamond substrates offer an unparalleled level of thermal control, added Jerry Zimmer of sp3 Diamond Technologies, while Dan Francis of Group 4 Labs showed a flip-chip method of making GaN HEMTs on diamond after first growing the transistor on sapphire or SiC.

The substrate debate continued into a "rump" session. Perhaps the composition of the audience distorted the outcome of that discussion, but the overriding impression was that SiC still had a strong lead as the GaN substrate of choice – much to the chagrin of Doering and the diamond followers.



MARGARET DOYLE

TriQuint CEO Ralph Quinsey tells Mantech delegates that "value is moving back into the semiconductor space".

InP promises to turbo-charge ICs

If we stick to using copper interconnects in silicon ICs, then it's only a matter of time before we arrive at a performance-limiting data-transfer bottleneck. The solution: additional optical interconnects built from silicon waveguides and InP lasers and detectors, says **Dries Van Thourhout**.

Severe data-transfer bottlenecks between the different sections of a silicon IC are threatening to limit the performance of future generations of electronic circuits. This is because the continuing reductions in device dimensions are making it increasingly difficult to keep propagation delays at an acceptable level. Even if we take the most optimistic estimates for conductor resistivity and dielectric permittivity, it seems likely that ICs performance will not keep pace with that set out in the International Technology Roadmap for Semiconductors. So it is clear that a radically different approach is needed for linking together the different parts of a silicon IC.

One promising option could be the addition of a high-speed optical interconnect layer that sits on top of, or in between, the classical copper interconnect layers of future microprocessor chips (see figure 1). Aside from the bandwidth advantage, the benefits of such an optical interconnect layer would be a reduced temperature sensitivity for the link, an immunity to electromagnetic noise, lower power consumption and the possibility for synchronous operation, both within the circuit and with other circuits.

In Europe we have been pursuing exactly this type of technology through a European Union funded project entitled "Photonic Integration layer on CMOS by wafer-scale integration (PICMOS)". This recently completed €4.5 million ($6 million) project, which ran for just over three years, focused on building an optical interconnect layer by combining a silicon nanophotonic optical waveguide circuit and microscale III-V lasers and detectors. The effort was led by researchers at the Photonics Research Group that is affiliated to Ghent University and the Interuniversity Micro Electronics Center (IMEC), which are both in Belgium. It involved six other partners: the French companies ST Microelectronics and Soitec-owned TRACIT Technologies; France's INL (Institut des Nanotechnologies de Lyon) and CEA-LETI; the National Center of Scientific Research "Demokritos" in Greece; and the Technical University Eindhoven, in the Netherlands.

Optical interconnect layers for on-chip communications require very compact waveguide circuits, due to the lack of available space. Fortunately, silicon "wire" optical waveguides allow just that, and can be fabricated by classical lithography and etching on silicon-on-insulator (SOI) substrates with a 200–400 nm silicon top layer. Restricting the wire width to around 500 nm produces single-

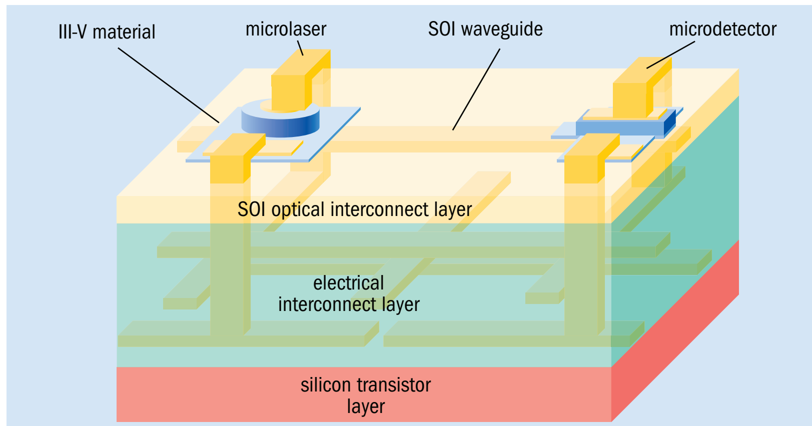


Fig. 1. On-chip optical interconnects could speed up data transfer between parts of a silicon IC.

mode waveguides that are ideal for data-transfer applications, and have virtually lossless bend radii as small as 2 μm thanks to a high refractive index contrast. Spacing these waveguides close together is also possible, as they can be brought to within a micron of one another without inducing serious losses – a level of miniaturization comparable to the pitch of copper lines on the upper interconnect layers in today's CMOS chips.

Laser sources

Devices that have recently been built for these silicon-wire waveguides by groups in the US at Intel, Luxtera and Cornell, in Japan by MTT and NEC, and in Europe by LETI and IMEC, feature very powerful filtering, wavelength selectivity and high-speed modulation. However, this approach suffers from a significant drawback: getting light out of silicon. Despite extensive research employing schemes using nanoscale features or silicon's nonlinear properties, it is unlikely that purely silicon-based lasers will reach an efficiency comparable to that of their III-V cousins for the foreseeable future. Consequently, we believe that it is imperative that the light-emitting function of III-V materials complements the strengths of the silicon-wire waveguide.

There has already been a large effort over the past few years to try and reach this goal by using advanced epitaxial growth techniques to form monolithically integrated structures. Our PICMOS project, however, has followed a radically different approach. This method, which is free from the lattice-matching constraints associated with producing III-V devices

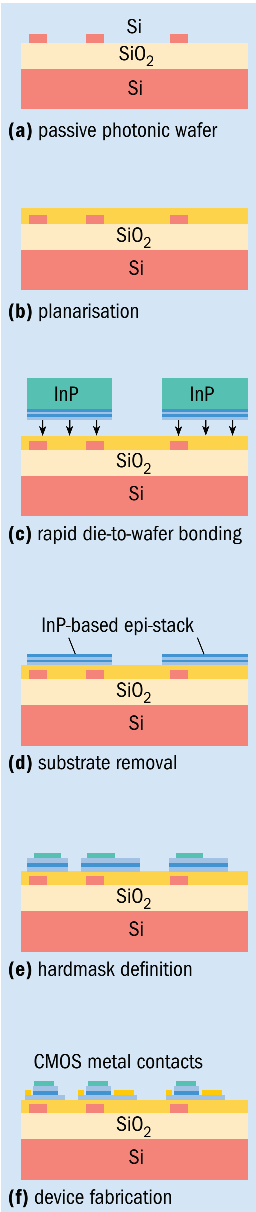
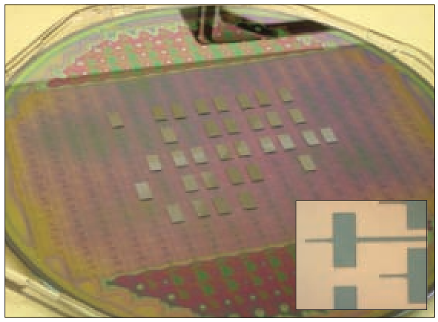
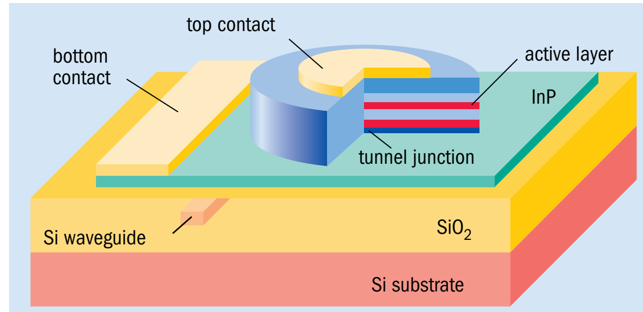


Fig. 2. The PICMOS approach to building an InP microlaser coupled to a silicon-wire waveguide involves the fabrication of a passive photonic silicon wafer **(a)**, its planarization **(b)** and the addition of InP die **(c)**. The substrate is then removed from these InP structures **(d)**, before a mask defines the laser **(e)** and CMOS metal contacts are added **(f)**.





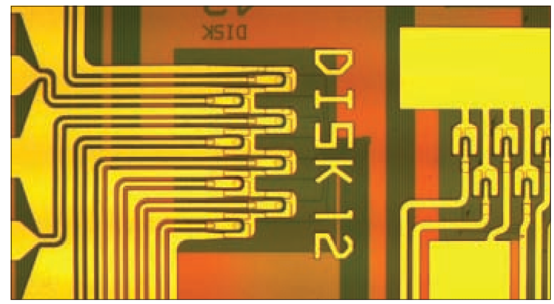


Fig. 3. (above) A wafer bonding process unites a 200 mm CMOS silicon-on-insulator wafer with InP dies using 15 nm thick silica layers. The inset gives a magnified view of the MOCVD-grown InP dies. **Fig. 4.** (above right) Microdisk lasers have been used to provide the optical sources for the PICMOS project. These devices support whispering gallery modes and a central top contact can be added without introducing significant optical loss. **Fig. 5.** (right) An array of eight microdisk lasers, with a diameter of 7.5 µm, on top of nanophotonic silicon-wire waveguides after metallization.

on silicon, employs an efficient die-to-wafer bonding process to transfer small III-V-based epitaxial dies onto SOI wafers. Following substrate removal, the III-V epilayers are then processed using classical wafer-scale processes (see figure 2 for details).

Our starting point for the process is the SOI wafer. A combination of deep-ultraviolet lithography and inductively coupled plasma (ICP) etching form the nanophotonic waveguiding circuits in the wafer, before SiO_2 deposition and chemical-mechanical polishing (CMP) provide planarization. We then bond InP dies containing suitable epitaxial layers epi-side down onto this SOI wafer. The sizes of these dies are application-dependent and vary from 1 mm^2 to over 1 cm^2. Since the InP dies have not been processed, their alignment tolerance is relatively large (>50 µm). This allows for a fast pick-and-place process that would be unsuitable for the transfer of preprocessed optoelectronic components. Mechanical grinding and selective wet etching then removes the InP substrate material to leave a thin layer of III-V epitaxial material on the SOI wafer. Finally, lithography, etching and metal deposition defines the lasers and detectors.

The key advantage of this approach is the wafer-scale lithography process used to align the III-V devices and the underlying silicon-wire waveguides. This approach is low-cost, but delivers an alignment accuracy of better than 0.1 µm.

Our bonding process for the transfer of InP layers to silicon is similar to wafer-to-wafer bonding processes that have already been used by many other research groups. However, in our case a full wafer-bonding process is not the most economical solution because of the high cost of InP epitaxial wafers and the significant size mismatch between commercially available InP wafers and SOI wafers, which are available in 200 mm diameters.

These drawbacks drove us to develop an alternative, efficient die-to-wafer SiO_2–SiO_2 molecular bonding process. MBE-grown wafers containing the laser structures were coated with a 15 nm silica layer using an electron cyclotron resonance deposition process and the MOCVD-grown wafers for the detectors, which had a rougher top surface, were covered with a thicker SiO_2 layer, before planarization by CMP. After both these III-V wafers were diced, the individual chips were bonded to a SOI wafer by our colleagues at CEA-LETI. The thickness and uniformity of the remaining SiO_2 layers strongly influences the operating characteristics of the final device, so TRACIT Technologies developed a specific process to optimize chip performance. Finally, the wafer-bonded dies were annealed at a low temperature to complete the transfer process (see figure 3).

Microdisk emitters

The upshot is that our process is broadly similar to that recently employed by Intel and the University of California, Santa Barbara. This US research partnership built hybrid III-V silicon lasers using a plasma-activated direct wafer-to-wafer bonding process that did not require an intermediate silica layer. However, the SiO_2–SiO_2 bonding process that we have used has the advantage of being generic: the same process and surface activation procedure can be used, independent of the wafer source.

The lasers for our optical link need to be ultra-compact, capable of high modulation speeds, produce very low threshold currents and require a power-consumption budget that is ideally lower than that needed for classical electrical paths. We have tried to address all these requirements with a microdisk that we described in a post-deadline paper at the recent Optical Fiber Communication

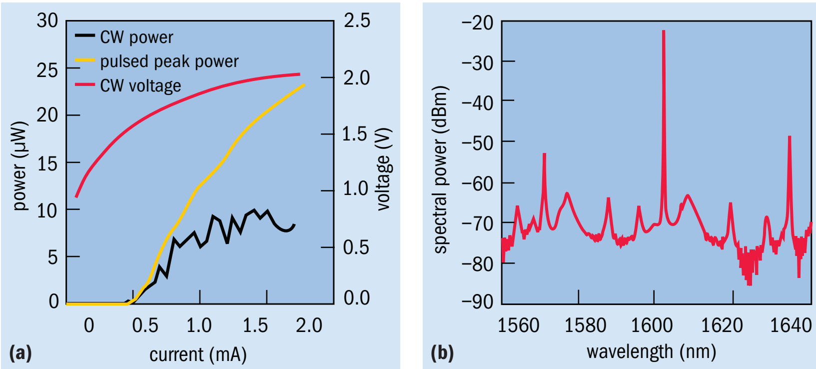


Fig. 6. (above) Performance characteristics at 20 °C for a 7.5 μm disk laser **(a)**. The continuous-wave lasing spectrum at 1.4 mA drive current, which has been normalized for the fiber-coupler efficiency and on-chip propagation loss, reveals the dominant lasing wavelength at 1.6 μm **(b)**.

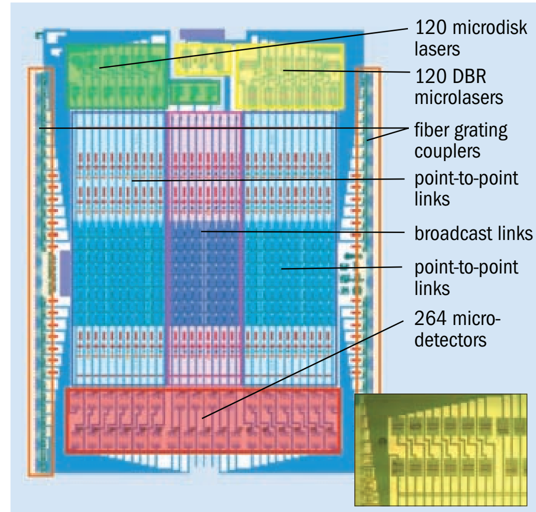


Fig. 7. (right) Combining the InP lasers and detectors with silicon-wire waveguides has produced the first demonstration of a full optical link on a nanophotonic waveguide platform.

conference, which was held this March in Anaheim, CA. This optical source was formed by etching the microdisk structure in a thin InP-based layer bonded on top of the silicon waveguides (see figures 4 and 5, p26). The disk supports whispering gallery modes confined to the microdisk's edges, and a top contact can be added in the device's center without introducing additional optical losses.

Classical lasers use a heavily doped InGaAs layer as the p-side contact, but this approach would introduce unacceptable internal losses for our thin-film laser. So our partner INL developed and optimized a less-absorbing alternative structure, which contains an InGaAsP tunnel junction with a bandgap of almost 1 eV and a second n-type contact (see figure 4 for an image of the disk lasers and interconnects). Using this design our 7.5 μm diameter disk lasers produced 1.6 μm single-mode continuous wave emission at room temperature and had a threshold current of 600 μA (figure 6). Output powers up to 100 μW were produced in pulsed mode.

A comparable process has also been used to fabricate similar-sized detectors with an InGaAs-absorbing layer, which were grown by MOCVD at the Technical University Eindhoven. These devices have a 0.45 A/W efficiency, a 1.6 nA dark current, and form the final part of a full optical link.

Putting it all together

The processes for fabricating all the individual components of our photonic ICs are now established, which has put us in a position to build our first demonstrator chip, a structure containing 250 microlasers connected to a similar number of detectors with a silicon-wire waveguide array (see figure 7). Due to a processing error, the power coupled from the microsource into the waveguide was very low. However, a preliminary measurement that is still to be verified revealed that up to 60% of this coupled power was picked up by the detector. This result has provided us with the first ever demonstration of a full optical link on a nanophotonic waveguide platform, and clearly shows the potential of this technology.

Our next goals, which follow on from the recent PICMOS project, will include the integration of the completed optical layer within an actual CMOS circuit, which could be carried out using a wafer-to-wafer bonding process that is similar to those currently being developed by CMOS chip makers for three-dimensional IC stacking. In addition, we also need to perform complete fabrication of the optical layer in a CMOS fab.

We are already part way towards this goal. A CMOS pilot line and a 200 mm SOI substrate were used for both the silicon waveguide fabrication at IMEC and the die-to-wafer bonding and masking process used for the III-V mesas, which were both carried out at LETI. But the other processing steps, such as etching and metallization, were carried out in the III-V cleanrooms of IMEC, INL and Technical University Eindhoven. To refine the entire process so that it is compatible with a CMOS fab requires a better understanding of potential contamination issues and the development of a CMOS-compatible metallization process – tasks that are currently under development.

Although the PICMOS project specifically addressed on-chip optical interconnects, our electro-photonic integration platform could also serve other applications. For example, the technology could be used to unite 40 miniature disk lasers, emitting at slightly different wavelengths, with silicon-wire waveguides, and provide a very compact transmitter with capacity of up to 400 Gbit/s for on-chip and off-chip data links. These laser sources could also combine with compact wavelength-division-multiplexing circuits to form complex reconfigurable networks, or be used to build incredibly cheap, but very powerful optical biosensors. So the benefits of the PICMOS platform are potentially both significant and wide-ranging, and only time will tell how far this approach to building optical interconnects will permeate into tomorrow's chip technology.

About the author

Dries Van Thourhout (**dries.vanthourhout@intec.ugent.be**) was the co-ordinator of the PICMOS project. He is a permanent staff member of the Photonics Research Group at IMEC/Ghent University and his research interests include silicon nanophotonics, III-V/silicon heterogeneous integration and integrated photonics in general.

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Sophisticated models replicate the effects of tunnel junctions

LEDs, lasers and multi-junction solar cells can all employ tunnel junctions to improve performance. Calculating the effects of this junction is tricky, but there are ways to accurately simulate chip characteristics and cost-effectively optimize the structure's design, say **ZQ (Leo) Li** and **Simon Li**.

Leo Esaki's discovery of electron tunneling in p–n junctions in the late 1950s has left a legacy for our industry. Although major scientific recognition for his work came in the form of a shared Nobel Prize for Physics in 1973, an arguably even greater accolade has followed – the widespread use of the tunnel-junction structure based on his discovery in a wide variety of commercial devices.

Today tunnel junctions (see box "How a tunnel junction works", p30, for an explanation of the operating principle) appear in electronic and optoelectronic compound semiconductor devices to perform functions such as reducing resistance, preventing current crowding, linking devices together and providing electrical and optical confinement. In multi-junction solar cells they "glue" individual cells together and in LEDs they cut resistance and reduce current-crowding in p-type layers, leading to substantial increases in light extraction and uniformity. Tunnel junctions can also be used to stack bipolar cascade laser diodes together to form high-power bars that recycle electrons at each stage and produce an output proportional to the number of stages. In VCSELs, the junctions can provide electrical and optical confinement within the device.

It is important to cost-effectively optimize the design and processing methodology of the tunnel junction within each of these devices, which is possible with a technology computer-aided design (TCAD) approach. This has already been employed in the silicon industry for manufacturing CMOS chips, power devices and image sensors, but it is much more challenging to apply this technique to compound semiconductor optoelectronics.

For one thing, simulating optoelectronic devices is far more complicated. In addition to the Poisson equation (which calculates the electric-field gradients) and the carrier-transport equation that describe silicon devices, more equations are needed to calculate light generation (an optical-gain equation) and propagation (an optical-wave equation), alongside an approach that takes into account the coupling between these effects. Optoelectronic devices can also contain quantum wells and dot structures to confine the carriers, which means that the traditional drift-diffusion equation must be modified for these nanostructures. In addition, many of the material parameters for compound semiconductors that are needed for simulations are not well calibrated. Despite these immense challenges, the popularity of TCAD for the design of laser diodes, LEDs and photodetectors has grown in recent years.

At Crosslight, which is headquartered in Vancouver, Canada, we have developed a software package for modeling optoelectronic devices incorporating tunnel-junctions. We believe that this tool, which is called "advanced physical models of semiconductor devices" (APSYS), is the only piece of commercial software available for simulating this type of structure. Carrier transport of the tunnel-junction-based devices is modeled by drift-diffusion theory using a

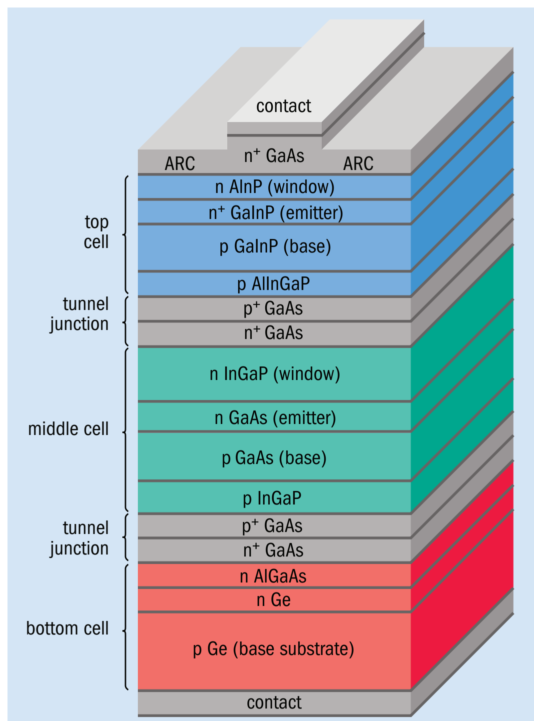
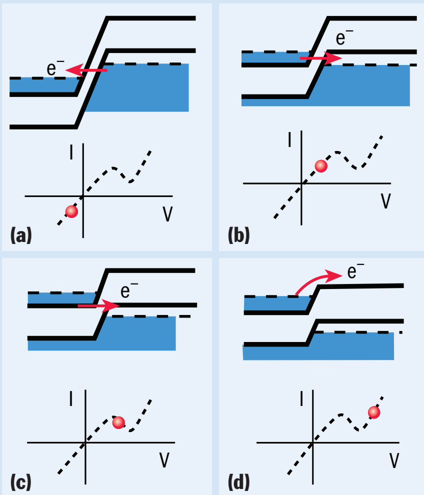


Fig. 1. Crosslight's software can model the band structure of devices containing tunnel junctions, such as triple-junction solar cells comprising sub-cells of germanium, GaAs and InGaP.

IBM

Leo Esaki discovered the tunneling effect that holds the key to tunnel-junction operation in 1957 when he was leading a small group of researchers studying the properties of germanium p–n junctions at Sony Corporation, Tokyo. Three years later he left Japan, joined IBM and started to pioneer the development of semiconductor quantum structures such as superlattices. In 1993 he retired from IBM and returned to Japan to become president of the University of Tsukuba.

What is a tunnel junction?



A tunnel junction is a heavily doped, thin p–n junction that has a negative resistance at certain forward bias values due to electrons tunneling from the n-side to the p-side.

The structure is formed from p-type and n-type layers with a typical thickness of 10 nm and a doping level of around 10^{20} cm^{-3}. Heavy doping creates a "broken" bandgap, (denoted by the dotted lines in the figure), which leads to electron states in the conduction band on the n-side of the junction that are similar in energy to the valence-band-hole states on the p-side.

Under reverse bias (figure (a)) electrons tunnel in the opposite direction (from the p-side to the n-side). This results in different electron and hole states on each side of the junction that are increasingly aligned. Electrons can then tunnel through this junction from valence band to conduction band (a process called interband tunneling).

Under forward bias, voltage increases (see figure (b)) cause electrons to tunnel through the p–n junction due to the electron states on the n-side aligning with hole states on the p-side. When the voltage is further increased (figure (c)), these states become more misaligned and the current drops. This scenario is called negative resistance, because current decreases with increasing voltage.

As the voltage bias increases even further (figure (d)) the device begins to operate as a conventional diode. Electrons then travel by conduction across the junction, rather than tunneling through this barrier.

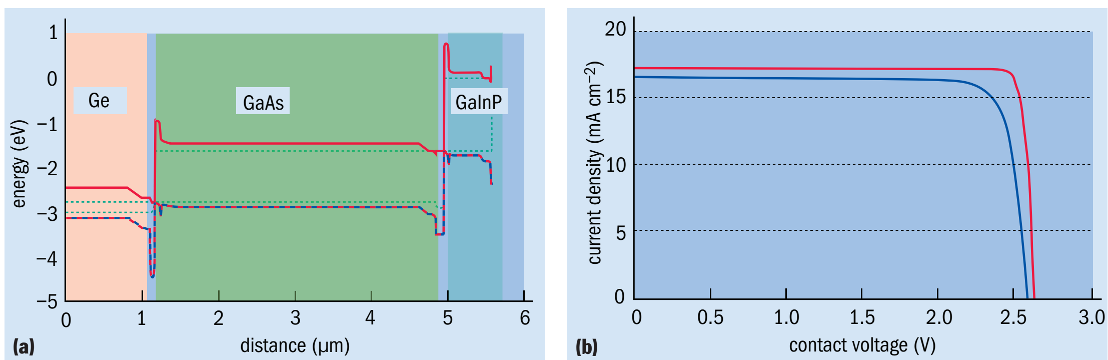


Fig. 2. (a) Crosslight's tool can calculate the band structure in a germanium, GaAs and InGaP solar cell under a bias of 3 V. The green dashed lines show the quasi-Fermi levels for the conduction and valence bands. The red line shows the conduction band throughout the structure. The dashed red and blue lines show the heavy-hole and light-hole valence bands. **(b)** Predictions of the short circuit current density for this triple-junction solar cell (red line) are in good agreement with the experimental results (blue line). The actual cell had a surface area of 21.65 cm^{-2}, a fill-factor of 85.15% and produced 0.783 W at an operating temperature of 28 °C and an efficiency of 26.7% under AM0 illumination.

finite-element approach. The electron density, hole density and electric potential at each mesh point form the basic variables; the other physical properties are calculated from these three quantities.

With a tunnel-junction structure, the current in the device depends on electron transport on one side of the junction and hole transport on the other. This means that the non-local nature of the inter-band tunneling current cannot be simply added into the drift-diffusion model, so a carrier generation term has been introduced into the layers to circumvent this issue. Tunneling is then modeled as another carrier generation mechanism, which depends on the local electric field and electron bandgap.

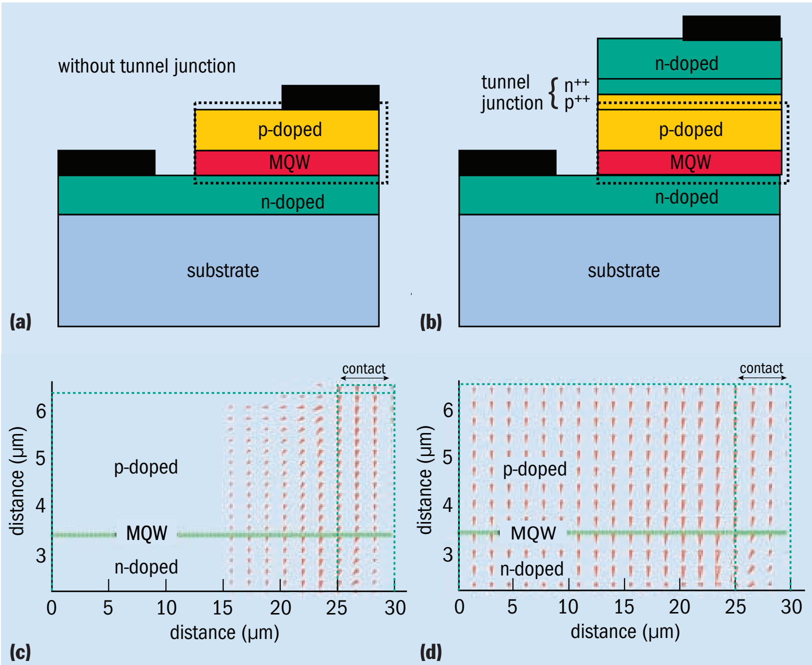
Our model shows that the tunnel junction's thickness is critical to device performance. If it is too thin it prevents depletion in the layer, but if it is thicker than strictly necessary it increases free-carrier optical absorption. Doping of the junction must also be sufficiently high to reduce electrical resistance, but not so high that it affects material quality. Compounding this delicate balancing act is the influence of the overall device structure on a particular optimization of the junction's thickness and doping level. This means that tunnel-junction optimization must be carried out in conjunction with all the other layers of the device.

Multi-junction solar cells

Our model can simulate the performance of multi-junction solar cells. It has been used to study a common structure that features three sub-cells: germanium, GaAs and InGaP junctions stacked in series (see figure 1, p29). The GaAs and InGaP sub-cells each have a bottom back surface field layer and a top window layer, and two tunnel junctions connect each pair of sub-cells. Solar-cell operation involves a complicated interaction between photons and electrons, the transport of carriers and the propagation of light through the tunnel junctions.

Our simulation has maximized this triple-junction cell's efficiency by optimizing every layer's thickness and doping density. This approach can calculate the positions of the valence and conduction bands throughout the entire structure (see figure 2a) and the device's current-voltage characteristics (see figure 2b). Predictions for short-circuit current, open-circuit voltage and efficiency are in very good agreement with experimental results.

Carrying out simulations is a cost-effective way to investigate the effects of new materials and different solar-cell structures on the efficiency of multi-junction structures. We have begun to study the performance of quadruple-junction solar cells employing an additional nitride layer. Initial results



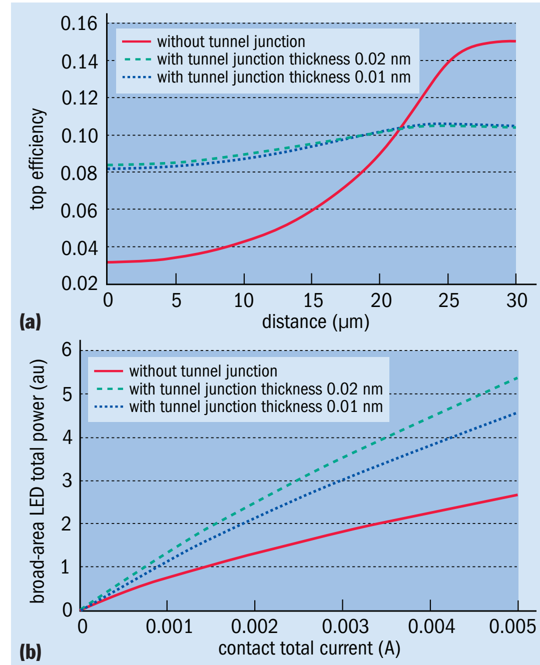


Fig. 3. (above) The addition of a tunnel junction to a conventional design (see **(a)** and **(b)**) improves current spreading beneath the contact and ultimately increases output power and emission uniformity. The vector plot **(c)** shows a current-flow simulation for the rectangular area outlined in **(a)**, which has a far less uniform current flow than that calculated for the tunnel-junction-based device **(d)**. **Fig. 4.** (right) Crosslight's simulations reveal the benefits of a tunnel junction on LED efficiency. The LED's "top efficiency", which is defined as the external efficiency across the top of the device, is much lower in the center of the conventional LED (distance = 0) due to current crowding. With a tunnel junction, the top efficiency and emission power (measured in arbitrary units) are substantially improved **(b)**.

suggest that this combination could boost overall conversion efficiencies to 43%.

Nitrides already feature in billions of blue and white LEDs. The commercial success of these chips is undeniable but their performance remains limited by poor current spreading, which results from a low hole concentration and high resistivity in the heavily doped p-type layers.

This problem can be overcome by either turning to a semi-transparent p-type electrode that improves current spreading and light extraction in top-emitting LEDs, or by switching the design to a flip-chip structure. However, both these approaches pay the penalty of more complex fabrication.

This pitfall can be avoided by adding a buried tunnel junction on the LED's p-side. It removes the need for lateral hole injection and can double the top-emitting power of blue LEDs, according to research from Seong-Ran Jeon and co-workers from Chonbuk National University, Korea. The US Air Force Research Laboratory (AFRL) has produced similar results with tunnel-junction structures that eliminate the hole-injection layer and provide a link between a stack of GaAs-based LEDs. The tunnel junctions improve the uniformity of the output power from this multi-LED emitter.

Typical LEDs employing a tunnel junction require three more epilayers than their conventional equivalents (see figure 3). With these additions, significant increases in output power are possible at the expense of only a small increase in operating voltage, if the thickness and doping profile of the tunnel junction has been optimized. Self-heating effects also need to be considered. To simulate all relevant effects in a coupled and self-consistent manner we have developed sophisticated models, which produce very good results.

Researchers William Siskaninetz and Thomas Nelson from AFRL have used our tool and commented: "The APSYS software by Crosslight gave us extremely accurate electrical predictions of our bipolar cascade LED structures as verified experimentally. We also received tremendous qualitative agreement in the light-output predictions."

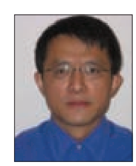
The guidance provided by our simulations is illustrated in a comparison of LEDs with and without tunnel junctions. Calculations of the current flow reveal that the switch from a hole conduction layer to a tunnel junction dramatically improves current spreading beneath the p-contact (see figure 3). The greater current spreading also improves the uniformity of the LED's external emission (figure 4a), and the output power (figure 4b). All of these results are in very good agreement with experimental observations and demonstrate the benefits of accurate modeling for cost-effective device design and optimization.

Further reading

N H Karam *et al.* 1999 *IEEE Trans Elec. Dev.* **46** 2116

S R Jeon *et al.* 2002 *IEEE J. Sel. Topics Quan. Elec.* **8** 739

W J Siskaninetz *et al.* 2002 *Elec. Letts* **38** 1259




About the authors

Z Q Li (left) is vice president of engineering of Crosslight Software Inc. He has more than 50 research journal publications on modeling of semiconductor devices and materials, and previously worked for the National Research Council of Canada. **Simon Li** (right) is president and chief software designer of Crosslight Software Inc. He has more than 20 years of experience in modeling semiconductor devices, and also worked for the NRC before founding the company.

DEVICE DESIGN

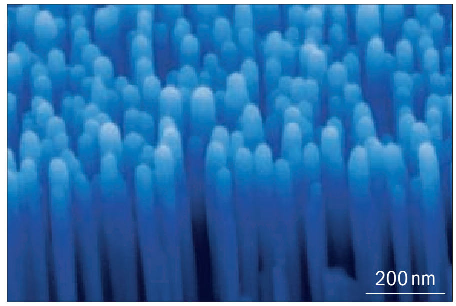
Nanotip top boosts LED output by 70%

A US team led by researchers at Rutgers University has delivered a 70% increase in the brightness of a conventional blue LED by adding ZnO nanotips to the top of the device.

"Our approach does not require complicated processing technologies, such as laser lift-off, flip-chip bonding, or electron-beam lithography," remarked Yicheng Lu.

However, according to him, the nanotip approach still produces an enhancement factor that is similar to that associated with other common technologies used to boost extraction , such as flip-chip bonding and using photonic crystals. "And with an optimized gallium-doped ZnO layer on p-GaN, significantly higher light emission is expected," said Lu.

The GaN and ZnO growth used to produce this type of LED is carried out in two separate reactors. "After making GaN LEDs without the top electrodes, gallium-doped ZnO is deposited on the top of GaN as the top transparent and conductive electrode," explained Lu. ZnO nanotips are added on top of this layer to boost light extraction.



RUTGERS

Adjusting the MOCVD process conditions can switch growth from a ZnO film to a nanotip structure that increases LED extraction efficiency.

Adjustments to the MOCVD growth conditions for ZnO, such as the gas-flow rate and substrate temperature, are used to switch between thin film and nanotip growth.

Room-temperature measurements of the nanotip LED built from the epiwafer, and a conventional LED used as a reference, revealed that the nanotip device had a notably higher output power and delivered a 70% improvement at a drive current of 20 mA.

The researchers have also modeled nanotip LED performance. The nanotips themselves only increase light extraction by 20%, but they also cause a roughening of the surface that accounts for the remainder of the boost in output power.

Journal reference
J Zhong *et al.* 2007 *Appl. Phys. Lett.* **90** 203515.

PROCESSING

Batch fabrication scales LED production

By James Tyrrell, nanotechweb.org

Nanowire LEDs could soon shed their status as a research curiosity thanks to a batch production breakthrough. Until now these LEDs, which offer highly directional emission and waveguiding properties on a miniature scale, could only be produced one at time.

"Most likely the nanowire LEDs will be used for biological-sensor applications," said Abhishek Motayed and Albert Davydov of the National Institute of Standards and Technology (NIST).

"Nanowire LEDs offer highly localized illumination with a defined peak wavelength that would allow a decrease in the size of the sensor, as well as reducing the volume of sample required for detection."

Researchers from NIST, Howard University and the University of Maryland claim that their fabrication scheme, which involves photolithography, wet etching and metal deposition, is well suited to commercial production and already has a yield of 60%.

The group uses an electric field to self-align its n-type GaN nanowires on a commercial p-doped GaN/sapphire substrate, which simplifies the often tedious task of manipulating each nanowire into position.

Operating in the 350–370 nm range, the team's GaN emitter is a good match for detecting airborne pathogens. What's more, by working with group III nitride alloys, and with other material systems, the group thinks that it can come up with a multi-spectral array for analyzing an even wider range of compounds.

Journal reference
A Motayed *et al.* 2007 *Appl. Phys. Lett.* **90** 183120.

Research in brief...

...QCLs get the horn

The drawbacks of metal waveguides used in quantum cascade lasers (QCLs) can be overcome by adding a miniature horn to one facet, according to researchers at University of Neuchâtel, Switzerland.

They say that the novel approach improves the beam quality and can deliver a tenfold increase in output power. These improvements should make QCLs a more attractive option for various applications, such as providing the source for heterodyne receivers that are used to carry out space-based spectroscopy.

The horn waveguide attached to the QCL is made from semi-insulating GaAs and has a simple geometry, with an initial section running parallel to the wafer and a second section flaring with an angle of 45°.

Maria Amanti from Neuchâtel says that different horn geometries could lead to additional improvements in performance.

Journal reference
M I Amanti *et al.* 2007 *Electron. Lett.* **10** 573.

...AlN cap cuts current collapse

Researchers from Nagoya Institute of Technology in Japan have reduced the current collapse in GaN-based transistors by incorporating AlN layers into the devices.

The team's AlN/AlGaN/GaN metal-insulator-semiconductor HEMTs, which were grown on 4 inch silicon substrates, featured AlN passivation to reduce the surface states that are responsible for current collapse under large signal radio-frequency modulation.

Addition of the 2 nm thick AlN cap layer reduced gate-leakage current by two orders of magnitude, and created a device with a maximum drain-current density of 361 mA/mm and a maximum extrinsic transconductance of 152 mS/mm.

"We plan to improve the quality of AlN growth on silicon and make a normally off-type MIS-HEMT," explained Nagoya's Takashi Egawa. Producing a normally-off transistor on silicon is an important step towards making a CMOS-compatible transistor.

Journal reference
S L Selvaraj 2007 *Appl. Phys. Lett.* **90** 173506.

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