COMPOUND SEMICONDUCTOR

September 2007 Volume 13 Number 8

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

PHEMTs

GaAs radar adds grunt to Growler

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RF Micro and Sirenza set for merger deal p5

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Cubic GaN

Nottingham team grows alternative crystal structure using MBE. p17

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Medal winner

Al Cho rewarded for epitaxy work with US National Medal. p5

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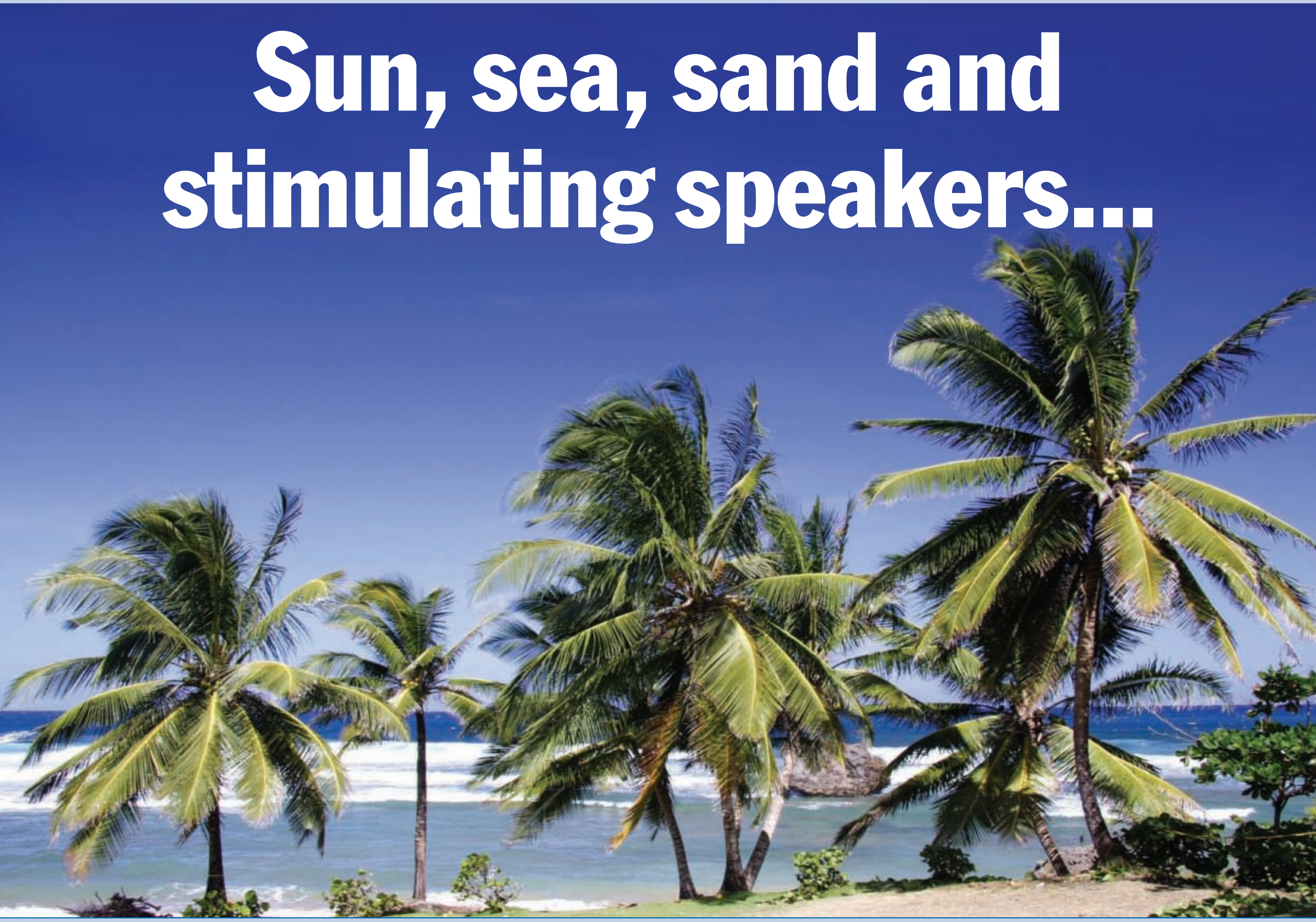

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- **Craig Cornelius** (Solar America Initiative)
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SEPTEMBER 2007
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COMMUNITY

INDUSTRY

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12 **Portfolio: Winds of change blow through GaAs** Major fluctuations in the market shares of the leading handset vendors pose the immediate challenge for power amplifier suppliers, while increased 3G network build-out boosts RFIC sales and suggests that RF Micro Devices' acquisition of Sirenza could be a timely one.

TECHNOLOGY

14 **Nitride LEDs get brighter with transparent ZnO contacts** LED manufacturers can boost chip performance by up to 30% if they replace ITO contacts with those based on ZnO, says Structured Materials Industries' Gary Tompa.

17 **Materials Update: Cubic crystal offers GaN solution** Perpendicular cleaving planes and an absence of polarization fields mark out thick layers of little-known free-standing cubic GaN as the ideal platform for optoelectronic devices, say Nottingham University's Sergei Novikov, Anthony Kent, Richard Campion and Tom Foxon.

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TRIQUINT

TriQuint's fab
TriQuint's 100 mm GaAs fab features tools for gate-metal deposition that are a key part of the process of PHEMT manufacture. **p25**

28 **Research Review** Atomic deposition promises InP logic…Layer transfer cuts InP substrate cost…Narrow trenches unite GaAs with silicon.

Main cover image: *The US Navy's latest Super Hornet aircraft, such as this Boeing EA-18G Growler, are kitted out with the latest in electronic warfare technology. The radar unit features hundreds of modules based on GaAs PHEMT devices made by Raytheon. See p6 and 25. Credit: US Navy.*

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IOP Publishing

Into the broadband era

I've lost count of the number of times I've written about "third generation" cellular services in the pages of this magazine. Ever since 1999, it's been the next big thing, next year's killer application – everybody's great white hope. But next year inevitably turned into the year after, and then the year after that.

Until 2007. 3G is right here, right now – broadband wireless is a reality and the sales figures for companies like Anadigics, Skyworks, TriQuint and the rest are finally reflecting that change. David Aldrich, the Skyworks CEO, summed it up pretty neatly, saying that the transformation of the wireless communications industry from voice-centered business to multimedia was "finally a reality".

That's key for the GaAs industry, because much more of the compound is required in advanced handsets and notebook chipsets, in order to handle broadband services without wasting masses of battery power. The result is already becoming clear on the bottom line – improved profitability for all of the key suppliers.

> "The wait for 3G to turn into a genuine market for GaAs chip suppliers became a tortuous one."

It's a trend that TriQuint chief Ralph Quinsey highlighted earlier this year and one that he expected to be accompanied by further industry consolidation. That's happening too – RF Micro Devices has decided that now is the time to become a more diverse company, servicing much more than just the mobile handset sector. Its acquisition of the fabless outfit Sirenza Microdevices is a direct acknowledgement of not only RFMD's need to broaden its wings, but also the size of the RFIC business now becoming available in markets like cellular infrastructure and upgrades to cable TV networks.

It indicates that RFMD sees potential in WiMAX, also known as (whisper it quietly) "4G". This technology has received a major shot in the arm too, with Sprint Nextel, its most active supporter, saying that its partners are committed to embedding 50 million WiMAX chipsets in consumer equipment to support its 2008 network build-out.

The wait for 3G to turn into a genuine market for GaAs chip suppliers became a tortuous one. But with those suppliers now in rude financial health, the opportunities are there.

Michael Hatcher *Editor*

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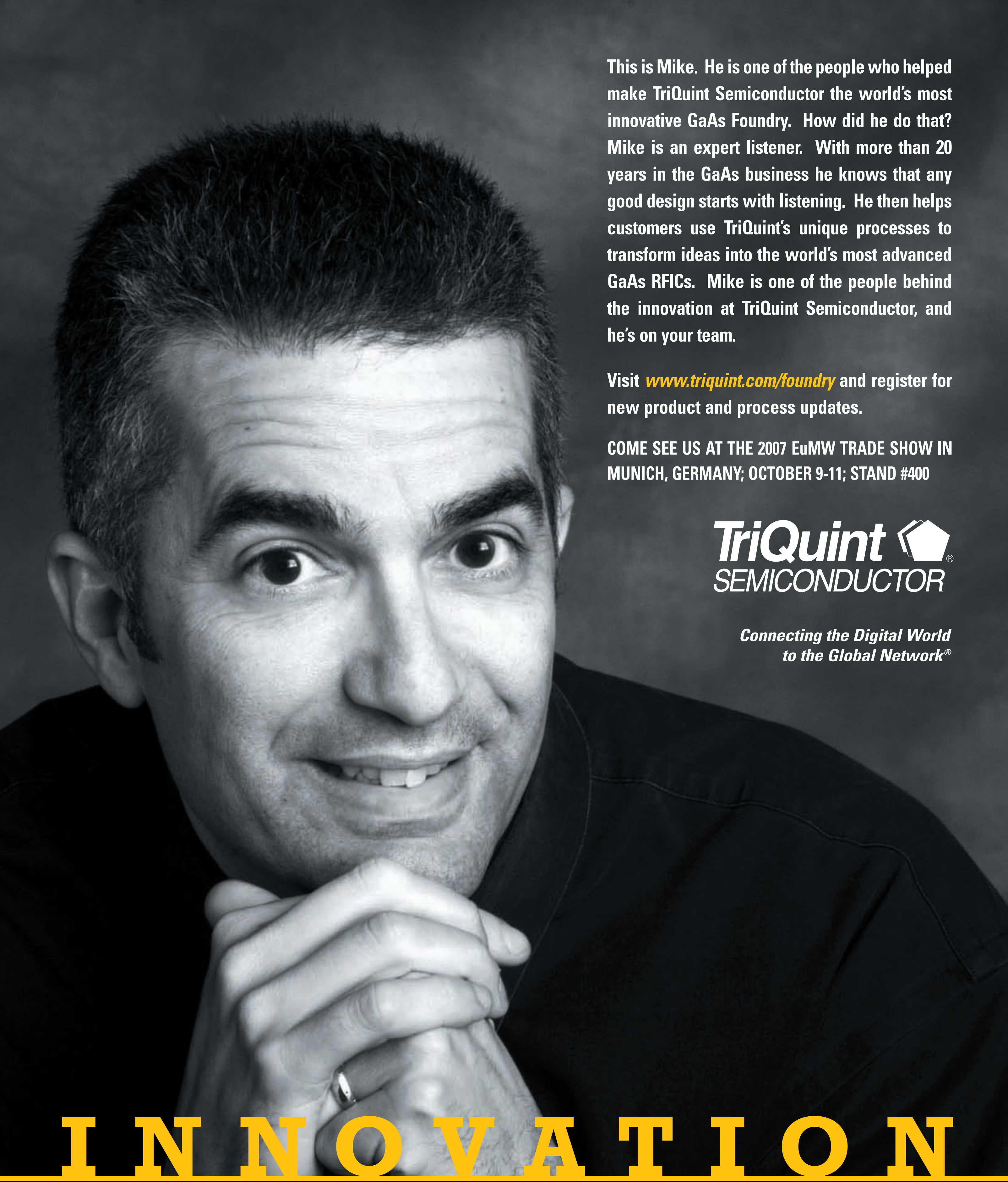
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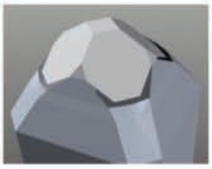
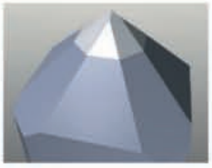
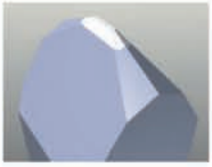






CONSOLIDATION

RF Micro splashes $900 m on Sirenza

Top-ranked GaAs chip maker RF Micro Devices (RFMD) is to consolidate its leading position and significantly diversify its portfolio of semiconductor products with the acquisition of fellow RFIC specialist Sirenza Microdevices.

Already approved by the two companies' directors, the deal will cost RFMD around $900 million, including $300 million cash.

Whereas RFMD is acknowledged as the market leader in power amplifiers for cellphone handsets (market research firm Gartner cites a 41% market share in 2006), the North Carolina company is reliant on this market, which makes up 94% of its sales.

Sirenza's revenues, on the other hand, are generated by a somewhat more diverse range of applications, including broadband and cable TV, wireless connectivity, wireless network infrastructure and defense.

RFMD's Bob Bruggeworth, who will remain as CEO of the combined companies following the completion of the deal, said: "Our two businesses are highly complementary in terms of customers, markets, products and manufacturing expertise."

The two firms have very different approaches to chip manufacturing. RFMD runs the world's largest MBE facility for GaAs wafer fabrication, whereas Sirenza has followed a fabless strategy.

Bruggeworth and Sirenza CEO Bob Van Buskirk were both keen to state how GaN technology would benefit from the move. GaN is crucial to RFMD's strategy, because the firm's management expects to be able to sell products based on the wide-bandgap material at a much higher profit margin compared with those based on GaAs.

Although RFMD has pioneered GaN chip development and Bruggeworth says that a "tremendous number of customers" are keenly evaluating the technology already, the company has not been a major supplier for wireless infrastructure applications, the most obvious end-market for GaN.

On the other hand, Sirenza's expertise in high-end components for wireless infrastructure has seen it establish strong relationships with the likes of Huawei and ZTE, the leading Chinese network systems companies. They are keen to source GaN components for their high-speed networks.

Now, the combination of Sirenza's customer relationships and RFMD's manufacturing power should provide a boost for GaN commercialization, with Van Buskirk anticipating that the technology will have a significant role to play in all of Sirenza's existing market sectors.

Although the acquisition still requires approval from the shareholders of both companies, as well as the relevant regulatory bodies, it is expected to be completed by the end of the year. The Sirenza business will then become the major part of RFMD's new "multi-market products group". Van Buskirk will move to North Carolina to lead that business division in the future.

LEGISLATION

Norway's arsenic purge could impact GaAs

On December 15, Norway is planning to adopt legislation that will ban consumer products containing arsenic compounds in amounts of more than 0.01% by weight of the product's "homogenous component parts".

The Norwegian Pollution Control Authority lodged documentation on the proposed restrictions with the World Trade Organization on June 8 this year, commencing a review process including a consultation period that closed on September 1.

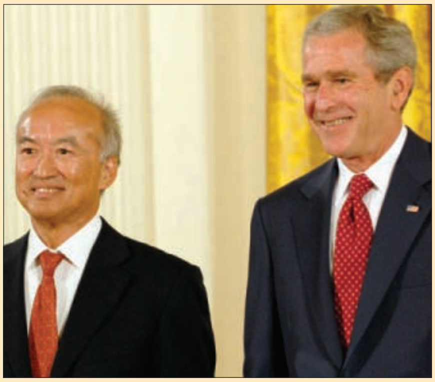
"One of the aims of the consultation will be to determine what additional exemptions are necessary to make the regulation workable," commented Roland Sommer, managing director of the RoHS International consultancy, prior to the deadlines.

RoHS International has already submitted comments into the review process on GaAs in semiconductor devices and Sommer expects to see an exemption from the ban for these materials.

A draft of the legislation, entitled "Prohibition on certain hazardous substances in consumer products" (PoHS), is hosted on the consultancy's website.

While it seems unlikely that Norway would allow the legislation to affect massively popular GaAs-dependent consumer products such as mobile handsets and DVD players, some believe that GaAs chip makers need to address any potential threat. Michael Kirschner, the president of consulting firm Design Chain Associates, says that the legislation could have a "devastating" impact on GaAs-based devices. He believes that GaAs device manufacturers need to comment to the Norwegian government on the proposed directive.

The "homogenous component" referred to in the legislation relates to the GaAs die. According to the Norwegians' documentation with the World Trade Organization, there are certain exceptions to the ruling, including food products and tobacco. In addition, the document states that there are proposed exceptions when a real alternative is lacking, or when a prohibition would "involve significant costs".



NATIONAL SCIENCE AND TECHNOLOGY MEDALS FOUNDATION

Al Cho, the co-inventor of the MBE technique that is now widely used to manufacture compound semiconductor epiwafers, received the US National Medal of Technology from President Bush on July 27.

The award recognized his pioneering work at Bell Laboratories from the late 1960s. Speaking with *Compound Semiconductor* after the White House awards ceremony, Cho said: "I feel I am so lucky to represent the MBE community to receive this award." See *compoundsemiconductor.net* for more details.

GAAS DEVICES

Japanese drop out of top-10 GaAs list

US-based chip companies have strengthened their grip on the GaAs device market, with Mitsubishi Electric now the only firm to represent Japan in the top 10. That's according to Strategy Analytics' assessment of the 2006 market for merchant and captive GaAs device sales.

In 2006 the top three suppliers – RF Micro Devices, Skyworks Solutions and TriQuint Semiconductor – held 55% of the $3 billion market, up from a 47% share in 2005.

These chip manufacturers have dominated the GaAs scene for the past few years, although TriQuint was the star performer in 2006, with its GaAs device revenues estimated to have grown 37% year on year.

Anadigics also had a very good year, meaning that US companies now dominate the top-10 list more than ever, with no European manufacturers featuring and only Mitsubishi Electric flying the flag for Japan.

While Europe's leading producers – Filtronic, United Monolithic Semiconductors and Ommic – are unlikely to make much of a dent in the US domination, there is at least an opportunity for Mitsubishi's compatriots to mount a challenge, says report author Asif Anwar.

"Switch complexities are increasing, which could potentially provide Japanese companies with an opportunity to regain lost ground in the cellular handset market," suggested the analyst. "We believe that Japanese market requirements may be particularly demanding, which will play to the strengths of companies like NEC, Sony and Eudyna Devices."

Power amplifiers (PAs) still represent the biggest market opportunity and Strategy Analytics believes that this sector could be ripe for consolidation, even as the GaAs device market expands to a predicted $5 billion by 2011 on the back of increased demand for broadband wireless connectivity.

Chris Taylor, another analyst at the market research and consultancy firm, reckons that the supplier base for handset PAs and front-end modules could follow the consolidation already seen in the market for similar products used in cellular base stations.

Only two major producers of base-station PAs remain, says Taylor: Andrew and Powerwave. He speculates that the dominance of just a handful of handset makers, led by Nokia, Samsung and Motorola, could force a similar situation, leaving perhaps as few as six suppliers by 2012.

MILITARY APPLICATIONS

GaAs radar adds grunt to Growler warplanes

US NAVY

Due to enter operations in 2009, the Growler is an updated version of the F/A-18 Super Hornet and comes equipped with the latest electronic warfare equipment, which includes radar based on GaAs PHEMTs.

Raytheon has been signed up to provide more than 400 APG-79 radars for the US Navy's F/A-18 Super Hornet and EA-18G Growler aircraft.

"We expect deliveries to continue over the next five to ten years and possibly longer, depending on international interest," said a spokesperson for the military contractor.

The APG-79 radars rely on transmit/receive (TR) modules populated with GaAs MMICs, many of which are made at Raytheon's Andover, Massachusetts, foundry. GaAs PHEMTs form the basis for power generation, power amplification and amplification of the radar's received X-band signals.

The TR modules integrate GaAs high-power amplifier, driver amplifier, low-noise amplifier and common leg circuit MMICs into a high-density package to be incorporated into the radar.

Active electronically scanned array (AESA) systems, such as the APG-79, are characterized by the large number of TR modules that perform transmitter and receiver functions. This gives AESA radar an advantage in its reliability, because it can continue to operate despite individual TR failures.

For the APG-79 in particular, operating in the X-band also allows the long-range tracking of multiple targets day or night, including in adverse weather conditions. "The AESA is a game changer that not only improves the Super Hornet's sting but also makes the F/A-18E/F Super Hornet Block II more reliable, more survivable and more formidable against all known threats," said Bob Gower, vice-president for the F/A-18 programs at Boeing.

Although Raytheon will only be producing between four and six APG-79 radars per month, the need for large numbers of TR modules in each unit demands a low-cost GaAs manufacturing approach. Consequently, high yields and volume-production techniques are needed – challenges that Raytheon has met, it says.

The need for production ramp-up may get even greater, as APG-79's popularity with the US military grows. "Super Hornet Block II and EA-18G aircraft equipped with AESA's revolutionary war-fighting capability make naval aviation more relevant than ever," said Donald Gaddis, F/A-18 and EA-18G program manager for the US Navy.

Raytheon will be banking on the enthusiasm of Gaddis and his colleagues as it bids for a program that would expand its production of AESA radar systems – seeing them fly in the prestigious F-15 Eagle, which has reportedly never been shot down by an enemy.

WIDE-BANDGAP DEVICES

Europeans eye GaN production

European collaborators have begun the second phase of a project that should lead to the continent's first volume production of GaN-based chips for RF applications.

Coordinated by the Fraunhofer Institute for Applied Solid-State Physics (IAF) in Freiburg, Germany, the project collaborators include United Monolithic Semiconductors (UMS) and NXP Semiconductors.

The three parties have been collaborating on GaN since September 2006, but the focus will now switch to refining the technology for future volume production at UMS's facility in Ulm, Germany.

A spokesman for Fraunhofer IAF says that improvements in the reliability and linearity of the GaN-based devices is still required before volume production can start.

Former Philips division NXP is largely focused on silicon technologies and maintains that it is committed to silicon LDMOS as the key semiconductor process for cellular base-station amplifier applications. It sees GaN as a technology for the future.

"Today's base-station power amplifiers (PAs) are limited to specific applications. With GaN technology, operators will be able to use a 'universal transmitter' switch between systems and frequencies to meet instantaneous demands in areas covered by the base-station," stated NXP.

While NXP believes that using GaN will deliver significant cost reductions in system manufacturing, the high cost of the III-V material has always been a problem area.

Nevertheless, NXP expects to bring out a GaN-based PA product within the next three years, with so-called switch-mode PAs set to follow. The UMS technology roadmap already includes GaN, with qualification of a 0.5 µm process expected in 2008 and volume production slated to start in 2009.

RIVAL TECHNOLOGIES

VCs stake $10 m on silicon PAs

By Andy Extance

Semiconductor chip designer Acco has attracted $10 million in a first round of funding intended to develop what it claims is a "major breakthrough in power amplifier (PA) design". The French company says that it has made enhancements to conventional silicon CMOS, specifically for use in PAs, claiming improved breakdown voltage, gain and linearity performance.

Acco gained $5 million for the concept behind its so-called "MASMOS" technology, of which little is known, but which derives its name from the company's founder and CTO, Denis Masliah, and $5 million when it produced working prototypes.

The company plans to sample PAs at the beginning of 2008 and have products in handsets by 2009. Its present devices have breakdown voltages of more than 14 V at 0.5 GHz, in comparison with 2–3 V typical of conventional CMOS. "One of the issues with CMOS was being limited by breakdown voltage," explained Masliah.

The higher breakdown voltage provides Acco with the ability to design its PAs to match and eventually better the linearity of GaAs, Masliah believes.

Acco is focused squarely on pitching MASMOS up against GaAs in the 3G handset market, hoping to eventually exploit the opportunities for integration unavailable to III-V technologies and to grab a 3–5% share of the available market.

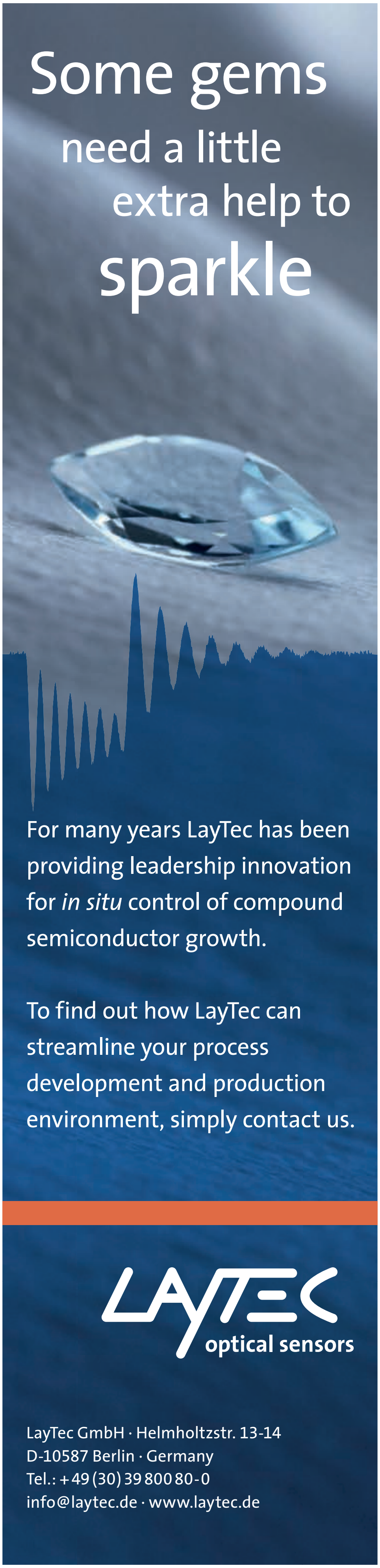
SUBSTRATES

SiC firm has big ideas

C9 Corporation has won $1.75 million funding for facilities to ramp up its 6 inch SiC growth technology and reach for even larger wafer sizes. The power semiconductor company will establish its proprietary equipment in a new fab in Malta, New York, to enter production for its military contract activities and pursue solar cell applications.

This expansion, which could cost up to $20 million, will also allow C9 to up its headcount from 10 to 35, with occupancy targeted in late 2008.

C9 has invested $11 million in its SiC program since starting an MBE approach in 2005, which it has progressively modified, allowing rapid progress from 2 inch to 6 inch SiC wafers in less than 12 months. CEO Kevin Donegan believes that he will have an 8 inch batch SiC reactor in action by March 2008. "We were micropipe-free from day one," said Donegan.



CHIP MANUFACTURING

Asia's LED build gathers pace

By Andy Extance

Showa Denko will expand its capacity to make GaN-based blue LEDs to 200 million units per month, after receiving orders "far exceeding original expectations" in 2007.

With monthly production at the Japanese company's Chiba site currently at 60 million, work is already in progress to raise this to 100 million a month by the end of the year.

The expansion will double this figure by the end of 2008, requiring an additional investment of ¥5 billion ($41 million). A source at Showa Denko says a similar expansion of its AlGaInP red/orange/yellow LED facilities, previously growing at the same rate as the GaN line, may not be far behind.

This acceleration of LED manufacture is part of the diversified chemical group's Passion Project business strategy, for which a ¥20 billion annual sales target for ultrabright LEDs in 2008 was reiterated.

Display backlights are driving the expansion, Showa Denko says, with a projected annual growth rate of 20% over the next five years dependent on the development of the technology beyond mobile phones into larger LCD displays, such as televisions and PC monitors.

Meanwhile, in Penang, Malaysia, Osram Opto Semiconductors has broken ground on its 30,000 m^2 LED chip fab, which the company says will be the world's most advanced. The ceremony was performed by Osram Opto CEO Rüdiger Müller and chief minister of Penang, Koh Tsu Koon.

Highlighting the relationship behind Osram's creation of another 800 jobs in Malaysia, Müller said: "This is only possible because our many years of co-operation have meant that we have the utmost trust in the quality, motivation and skills of the local workforce and community."

● Wuhan, China-based start-up HC Semi-Tek has received and commissioned its first Thomas Swan close-coupled shower-head (CCS) MOCVD reactor from Aixtron. "It is our strategic plan to quickly gain the ability to develop and manufacture GaN HB-LEDs," said HC SemiTek's co-founder, Chen Changqing. HC Semitek's technical team is pooled from local institutes and is said to have experience with CCS MOCVD tools.

WAFER DICING

Deep UV laser "boosts die count"

By Marie Freebody

Front-side wafer scribing using a laser emitting at 266 nm rather than conventional 355 nm could allow manufacturers to produce up to one-fifth more LEDs per wafer.

According to laser system vendor JPSA Laser, its deep-UV laser, which is based on a frequency-quadrupled source, achieves an industry-leading kerf width of 2.5 µm at a cut speed of 100 mm/s.

"Typically you can design a wafer to get up to 20% more LEDs by front scribing using a 266 nm laser, compared with scribing from the back using a 355 nm laser," said Adrian Baughan, international sales manager at JPSA.

"The shorter wavelength couples well into a larger variety of materials and can be focused to a smaller spot to get very high-quality ablation with a minimal heat-effected zone," added Baughan, who detailed the technology at the recent Association of Laser Users meeting in Cardiff, UK.

Until now, using a 266 nm laser in industrial applications has been limited by the source's relatively low power. "The laser operates at around 2 W, which is limiting in overall material removal rates for many applications," explained Baughan. "We have not increased the power; it is advanced optical design and the higher absorption of a shorter wavelength in sapphire that has resulted in faster scribing."

According to Baughan, careful design and choice of application means that high-speed scribing in LED die singulation is feasible. "We can now achieve high quality and very narrow kerf scribing of exotic materials," he said.

"In difficult materials such as sapphire or GaN, the improved coupling of the radiation to the substrate can result in faster scribing speed at lower power compared to using a 355 nm laser."

The front scribing method is key to achieving yields of more than 99%, reckons Baughan: "Front scribing means you can position the laser very accurately to the street that appears on the wafer and using a narrow kerf of 2.5 µm enables utilization of more of the wafer."

Marie Freebody is a reporter for optics.org.

CHIP DEVELOPMENT

UK alliance nets £1.7 m funding

A project looking to "promote the UK to the forefront of leading research" into GaN LED light sources has earned £1.7 million ($3.4 million) in funding from the UK government.

The partnership, which began in March, is worth £3.3 million in total and is called NoveLELS. It will run for three years and involves nine participating institutions.

According to Gareth Jones, NoveLELS' project manager and CTO of solid-state lighting company Enfis, the ultimate aim is to develop LED products that could enter commercial production – although no volume manufacturing is planned in this initial part of the collaboration.

"There are two real strands to the project," Jones said. "One is to take existing commercial technology for the GaN chip and build that into lighting modules. That will also act as a benchmark for some of the technology development that's going on at the chip and epitaxy level within the other side of the project."

The LED technology development will rely on two academic partners, using Brunel University's expertise in phosphors, and HVPE and MOCVD techniques developed by Wang Nang Wang, University of Bath.

The collaboration hopes to use Wang's processes to increase yields and make GaN LEDs on 4 inch wafers, combining it with the technology of the other partners to reduce cost-per-lumen in solid-state light sources. IQE will contribute epitaxial foundry services to help to achieve these targets.

MANUFACTURING

Nichia accelerates production schedule

Nichia says that its 150 lm/W high-brightness white LEDs will be available by the end of 2007, bringing its highest-efficacy products to market two years ahead of schedule.

The Japanese LED maker confirmed that it is planning a dramatic advance in its production timeline, with these devices originally slated for commercial release in 2009.

Nichia indicated that the products would be based on the low-current lab devices announced in December 2006, which deliver a 4600 K color temperature and a 9.4 lm luminous flux at a driving current of 20 mA.

Although efficacy is impressive, actual lumen output per chip is much lower than the 100 lm devices recently introduced by Cree and Philips Lumileds.

From our web pages...

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...Osram and Citizen cease fire
White-LED makers Citizen Electronics and Osram Opto Semiconductors have agreed an extensive licensing deal, putting an end to a dispute sparked in 2005 by Osram's claims that Citizen had violated intellectual property rights relating to white-light production via the use of a blue chip and a yellow phosphor. The licensing deal covers white LEDs in any size, suitable for cell phone keypads through to automobile headlamp applications.

...Demand drive for MOCVD kit
MOCVD equipment vendors Veeco Instruments and Aixtron are both seeing plenty of order activity as the installed capacity for LED epiwafer manufacturing continues to grow strongly. Aixtron says that sales of its high-capacity systems were particularly strong.

...Lumileds flashes past 100 million
Philips Lumileds has now sold 100 million Luxeon flash units for use in camera phones. The San Jose HB-LED specialist says that its flash products provide enough light to illuminate a two megapixel camera, without sapping battery life.

...Argos and Nichia agree terms
UK high-street retailer Argos and GaN chip maker Nichia have agreed a supply deal as part of a settlement regarding the Japanese company's patent litigation.

...BridgeLux in the money
High-performance LED chip designer BridgeLux has raised $23 million in its latest venture funding round, which was led by new investor Chrysalix Energy. The cash injection will go partly towards production and research.

PHOTOVOLTAICS

Ge-free cell seizes record

By Andy Extance

US researchers have produced a low-defect solar cell with a conversion efficiency of 33.8% under the standard terrestrial spectrum of sunlight, beating the previous efficiency record of 32%.

The work, which was performed at the National Renewable Energy Lab (NREL), Colorado, builds on the triple-junction inverted metamorphic approach that Emcore has used to attain the current record for space-based efficiency.

The NREL group, which includes solar pioneers Sarah Kurtz and Jerry Olson, made a cell that uses InGaAs for the 1.0 eV junction instead of germanium and grew the device on a GaAs substrate that can be removed after processing.

Talking to *Compound Semiconductor*, NREL's Mark Wanlass explained: "When you grow the structure it's inverted. Then we flip it and mount it to a silicon or glass handle and in this case we dissolved the GaAs layer – although you can keep and extract the materials."

The InGaAs layer is better than germanium for current matching with the 1.4 eV GaAs and 1.8 eV GaInP junctions used in the current leading commercial solar cells based on III-V materials.

InGaAs is lattice-mismatched with the GaAs junction it is adjacent to, but the inverted approach leaves its growth until last, allowing the 1.8 and 1.4 eV layers to be grown on top of the GaAs substrate with high crystal quality.

This metamorphic growth of graded GaInP, before InGaAs is finally deposited at the top of the epitaxial structure, minimizes the number of dislocations in this final layer, adding to the overall performance of the cell.

As well as improving current matching, eliminating germanium also lowers the weight and cost of the final device, yielding what Wanlass describes as "way higher" watt-per-kilogram performance.

Under concentrated sunlight, NREL's efficiency mark reached 38.9% – short of Spectrolab's record of 40.7%, although the respective degrees of concentration, 81 versus 240 suns, give NREL scope for improvement. "At high concentration under the terrestrial spectrum, we could be looking at 42–43% efficiency," Wanlass said.

If commercial cells can be pushed further, to 45 or even 50% efficiency, the crucial cost-per-watt metric falls dramatically and could lead to widespread deployment. Wanlass is hopeful that the germanium-free approach will attain this goal, although he admits that more junctions would be required.

"I think we can get there with four," Wanlass said. "Our technique looks to be the most promising thing on the table right now, in terms of getting to higher efficiencies."

● Emcore says that its production cells, which are based on the more conventional use of germanium substrates, now offer 39% efficiency at a concentrated illumination of 1000 suns. Emcore is already increasing its solar-cell production capacity to meet demand for alternative energy sources, while relative newcomers, such as Spain's Isofoton, Germany's Concentrix Solar and Taiwan's WIN Semiconductors, are all looking to exploit multi junction technology.

The University of Delaware has also claimed a new solar conversion record of 42.8%. Led by Allen Barnett, the team was due to reveal details of this technology, which is based on silicon and III-V converter materials, at the European Photovoltaic Solar Energy Conference in early September.

FINANCE

$26 m net loss fails to daunt ramping Infinera

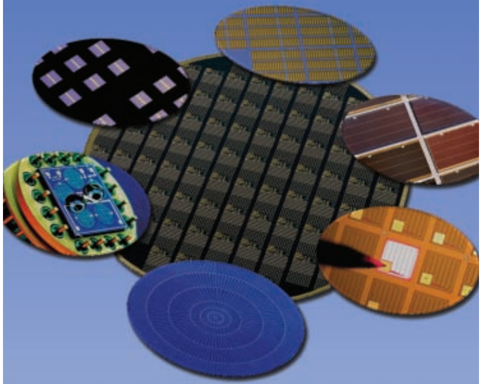
In its first quarter as a publicly listed company, Infinera recorded revenues of $58.4 million.

According to formal accounting rules, this delivered the Sunnyvale, California, system maker a net loss of $26.1 million for the three months until June 30, although by applying a different accounting method Infinera showed a profit of $2.7 million.

Whatever the differences in accounting approach, gross margins have improved dramatically over the past 18 months, because the company has ramped up the production of systems relying on its InP-based photonic integrated circuits.

Singh expects telecom customers to double their network capacity each year, allowing Infinera to grow 25% annually.

Cox Communications, the third largest cable provider in the US, has just selected Infinera to support a 12,000 mile network, while another new deal effectively trebles the capacity of XO Communications.



FINANCE

Tunable bounce helps Bookham

Laser chip maker Bookham posted sales of $45.1 million for the quarter that ended on June 30, up marginally on a sequential basis. But despite the flat revenue picture, the San Jose firm's bottom line is starting to look healthier, following major cost-cutting efforts over recent months.

According to standard accounting principles, the chip manufacturer made a net loss of $13.6 million in the quarter, an improvement on the $24.3 million loss in the previous three-month period. While that loss is still undeniably hefty, the combination of shrinking costs and an anticipated future increase in sales should help the company to move towards financial break-even.

Restructuring measures, including staff cuts at its compound semiconductor facility in Caswell, UK, cost Bookham $6.1 million in the June quarter, as the company used up $19 million of its slender cash reserves.

Alain Couder has now joined the company as its new CEO. The interim chief Peter Bordui, estimated in early August that Bookham is 70% through its restructuring, with further costs to come in the next two quarters.

However, the cost cuts have already impacted on financial results, with gross margins recovering well. Combined with sales to number-one customer Nortel more than doubling over the previous quarter and sales of tunable lasers jumping by 60%, the company's management is sounding hopeful for the future.

Declining orders for amplifiers from networking giant Cisco Systems put a drag on sales, but Bookham said that the adoption of 10 Gb/s components for both metropolitan and long-haul networks bounced back during the latest quarter.

Now, with no fewer than six "top-tier" customers buying its tunable laser products, Bookham sees this relatively new technology as one of its key growth drivers. It is also set to release a new, more compact version of the component in the second half of 2007.

With shipments of 980 nm pump lasers made at its Zurich facility now up and running, Bookham is predicting further improvement in manufacturing margins for the September quarter, as well as a hike in sales to around $52 million.

If the company can continue improving at this rate and ensure that its cash position does not become a problem, Couder may have taken over the reins at just the right time.

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...Arasor bags Alfalight

High-power diode laser supplier and InGaAs fab owner Alfalight is one of two companies being scooped up by Australian telecoms firm Arasor in a combined $63 million all-share deal. However, Alfalight's existing CEO, Mohan Warrior, will continue to manage the Madison, Wisconsin firm, as a wholly owned subsidiary. Alfalight will provide Arasor with optical chip, laser chip and optical coupler components for use in its fiber-optic products. Arasor already works with Novalux, another US chip maker, on the development of laser-based televisions.

...JDSU goes dental

JDSU has released a new 808 nm diode for pumping neodymium-doped crystals used in high-power laser equipment. The Milpitas, California, company says that the low-cost device provides the highest levels of brightness available on the market, delivering a reliable 4 W power output when fiber-coupled – twice that of its previous offerings.

"The 2495-L3 series not only provides a more elegant offering for high-precision laser applications, it also opens the door for JDSU to participate in new markets," said Alex Schoenfelder, vice-president and general manager of JDSU's Integrated Photonics business unit. According to the company, 808 nm lasers are increasingly being used in dental and medical fields, for example as a precision treatment for diseased gum tissue.

...Crystal IS invests

AlN expert Crystal IS has begun development of deep-UV LEDs, as part of a plan to expand beyond the manufacture of substrates. The Albany, New York, company has purchased two MOCVD reactors to develop and manufacture 280 nm devices, which it aims to sample later this year and bring to market in early 2008. Crystal IS says that its AlN substrates provide a lower dislocation density than sapphire, yielding better devices.

RFIC SUPPLIERS

Winds of change blow through fabs

Major fluctuations in the market shares of the leading handset vendors pose the immediate challenge for power amplifier suppliers, while increased 3G network build-out boosts RFIC sales and suggests that RF Micro Devices' acquisition of Sirenza could be a timely one. **Michael Hatcher** surveys the latest financial developments.

Table 1. Global mobile handset shipments (figures quoted in millions of units)

Vendor	*Q1 '06*	*Q2 '06*	*2006 total*	*Q1 '07*	*Q2 '07*
Nokia	75.1	78.4	347.5	91.1	100.8
Samsung	26.7	25.2	113.8	34.8	37.4
Motorola	46.1	51.9	217.4	45.4	35.5
Sony Ericsson	13.3	15.7	74.8	21.8	24.9
LG	15.6	15.3	64.4	15.8	19.1
Others	45.9	45.8	184.0	38.3	40.1
Total	222.7	232.3	1001.9	247.2	257.8

STRATEGY ANALYTICS

Motorola's dramatic reversal of fortune has seen all of the other top handset vendors gain market share at the US giant's expense and Samsung take its place in the number-two spot behind Nokia. Overall sales remain robust, with total handset shipments in 2007 expected to grow by around 10% on the 2006 figure. Apple's high-profile iPhone has barely made a dent in the market yet, with an estimated 0.1% market share.

Worries over risky loans to US homeowners and the threat of an ensuing "credit crunch" sent an ill wind through global equity markets in August, ensuring that pretty much every stock was buffeted down, up and then back down again.

Compound semiconductor stocks were no exception, so the effect of some strong trends in the broadband network and handset sectors may well have gone unnoticed in all of that volatility.

First of all there was the Motorola effect. Hit by well documented problems selling its low-cost handsets at any kind of profit and its failure to come up with a handset to match the phenomenal success of its RAZR, Motorola has ended up stockpiling millions of phones that nobody wants to buy.

The result, according to Neil Mawston from Strategy Analytics, is that Motorola's share of the global handset market has plunged from 22.3 to 13.8% over the past 12 months. With overall shipments still growing steadily, all of Motorola's rivals have benefited. Finland's Nokia has extended its lead as the number-one vendor and Korea-based Samsung has overtaken the US firm for the first time to take its number-two ranking (table 1).

What does all of this mean for makers of the GaAs-based HBTs and PHEMTs that feature in the vast majority of handsets in the form of power amplifiers (PAs) and switches? There are no clear-cut answers. As the leading PA and front-end module vendor, RF Micro Devices is perhaps more exposed than most to these fluctuations. In its latest quarter it saw sales slump by nearly 20% sequentially as Motorola made a drastic cut in orders.

This slump was partly offset by the market share swing to Nokia, RFMD's biggest customer, but was also felt by TriQuint Semiconductor, which is more exposed to fluctuations in consumer goods markets following its successful targeting of the handset space over the past couple of years. Thanks in no small way to its success in Samsung phones, TriQuint still managed to post a sequential increase in sales revenue in the latest quarter, but it felt the Motorola effect on its bottom line in the form of a $3 million excess inventory charge. Net profits were pegged back to just $1.4 million as a result (from $6.4 million in the previous quarter).

TriQuint CEO Ralph Quinsey remains cautiously optimistic about the remainder of 2007, as do all of the other players in the GaAs RFIC business, largely because of the fast-growing 3G sector. TriQuint has seen revenue from sales of high-speed WEDGE (combined wideband-CDMA/EDGE) chips more than double year on year and the deployment of 3G technology in all parts of the world now looks like boosting the coffers of all of the key suppliers.

Skyworks Solutions is one of those suppliers and CEO David Aldrich highlighted the key trend in the Woburn, Massachusetts, company's latest investor conference call. "The transformation from a voice-centered business to multimedia devices is finally a reality in our industry," he said.

Analyst Aaron Husock, of Morgan Stanley, agreed with Aldrich, saying: "Skyworks' design win activity highlights increasing traction in the move toward more integrated power amplifiers and in 3G, both of which offer meaningfully higher dollar content per handset."

The acceleration of 3G adoption has narrowed down the field of suppliers that can provide the technology, giving Skyworks – and of course its rivals – more opportunities with different handset manufacturers and perhaps even the hope of an upward trend in average selling prices.

"It is a very, very small, we think elite, group of folks, who can compete," explained Aldrich, "so therefore there should be much less long-term price pressure and more stability in this market."

Aside from 3G, Skyworks is continuing to diversify beyond handsets with its linear amplifier products.

Fabless Hittite, which is also based in Massachu-

Michael Hatcher does not own or intend to purchase any of the stocks in this article.

Table 2. Financial round-up – June quarter figures

Company	*NASDAQ ticker*	*June quarter total revenue ($m)*	*June quarter operating profit/loss ($m)*	*August 16 share price ($)*
Anadigics	ANAD	53.9	0.3	15.31
Hittite	HITT	37.6	17.3	40.21
RF Micro Devices	RFMD	212.0	−1.8	5.87
Sirenza Microdevices*	SMDI	46.7	4.0	14.83
Skyworks Solutions	SWKS	175.1	12.4	7.18
TriQuint Semiconductor	TQNT	113.8	−0.5	4.07

**On August 13, Sirenza agreed to be acquired by RFMD in a deal that valued Sirenza at $16.64 per share. The deal is expected to close by the end of 2007.*

setts, registered a pre-tax profit of $18.5 million on sales of $36.7 million in the latest quarter, demonstrating once again that lacking ownership of a fab is no hindrance to financial success. Hittite CEO Stephen Daly reiterated Aldrich's sentiment, saying that the build-out of cellular infrastructure to support broadband communications in Asia was one of the key revenue drivers in the last quarter, along with microwave and military applications.

Like TriQuint, New Jersey's Anadigics has been setting the pace in the development of handset PAs for 3G applications and high-end focus is continuing to improve the company's financial results. In its last quarter, Anadigics registered a record sales revenue of $53.9 million and posted its first net profit in years.

CEO Bami Bastani, the architect of Anadigics' 3G strategy, described the three specific "mega-trend" growth markets impacting his business at the moment – 3G cellular, broadband wireless LAN and the widespread upgrade of cable TV networks.

The Korean firms LG and Samsung, both major Anadigics customers, are winning market share (largely from Motorola) with their high-end handsets and smart phones, for example. The 3G market dominates Anadigics' wireless product sales, accounting for the vast majority of the business segment's quarterly sales of nearly $26 million – 48% of total revenue.

Another major sales driver is Intel. Its latest mobile computing chipset – codenamed "Santa Rosa" and sold under the Centrino Pro banner – is ramping much faster than initially expected, which Intel has said is one of its fastest chipset ramps ever.

Intel's Santa Rosa products support the 802.11n broadband wireless LAN standard, which offers a far better coverage, range, connection speed and battery life than previous generations of the technology. Crucially for Anadigics and its suppliers, it also requires multiple RF chains, which demands several power amplifiers (PAs) and a much higher GaAs content. The broadband Wi-Fi sector, which includes WiMAX applications, accounted for 22% of Anadigics' sales in the last quarter. With strong traction in the CATV sector (28% of sales), things are looking good for an even better performance in the rest of 2007 and into 2008.

Significantly, RFMD is now set to grab a piece of this action, with an eye on widening its product portfolio to make it less dependent on the handset PA sector (currently 94% of sales) and on improving its profit margins. The North Carolina company is all set to acquire its Colorado-based namesake Sirenza at a cost of nearly $1 billion.

Sirenza Microdevices looks like a hybrid of Hittite and Anadigics. Fabless, it focuses on high-end applications of RFICs – including silicon CMOS, SiGe and III-V designs – and is witnessing great demand driven by the build-out of broadband cellular and cable TV networks, wireless connectivity protocols like 802.11n and WiMAX, as well as lucrative, high-margin contracts in the aerospace and defense sectors.

With quarterly sales in the $45–50 million range, Sirenza has not come cheap, and RFMD will use a major chunk of its war chest in the proposed deal, spending $300 million in cash as part of the $900 million cash-and-stock transaction.

Once the deal is closed, which is expected by the end of the year, Sirenza's existing business will add quickly to RFMD's bottom line, and with little or no overlap in products or sales revenue, the combined company operations should fit together smoothly.

On the share price front, Anadigics continues to be the star performer of the GaAs companies, pushing up to the $16 mark before the credit crunch worries of mid-August. After such a remarkable turnaround in fortunes, it is easy to forget that Anadigics' stock was trading at only just above $1 as recently as May 2005. A 1000% gain over that time is a huge credit to Bastani and his management team.

Not surprisingly, given that RFMD's offer represented a 17% premium on its August 10 closing price, Sirenza's value also shot up in the last quarter, while all but one of the major GaAs companies in the US trod water. The exception was TriQuint, which shed around a quarter of its stock value between mid-July and mid-August as the market digested the impact of Motorola's stale inventory on TriQuint's profit margins.

But aside from that, things are looking good. Strategy Analytics maintains that the combined impact of the continued 3G build-out, WiMAX deployment, cable TV infrastructure upgrade and rapid growth in wireless connectivity will see the market for GaAs devices balloon from $3 billion in 2006 to $5 billion in 2011. RFMD and Sirenza expect to see the market for GaN-based RF components take off over that timeframe, adding further to the market opportunity.

With so many of the key companies looking well positioned to exploit that expected growth, it looks like we are now truly in the midst of the broadband era for RFICs – and the leading positions are still up for grabs in what should become a much more valuable market for GaAs and GaN ICs.

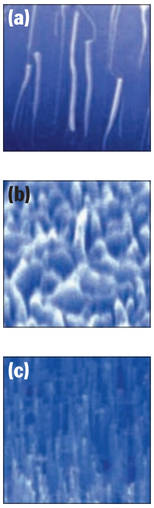
> "It is a very, very small, we think elite, group of folks, who can compete"
> **David Aldrich**
> Skyworks Solutions

Nitride LEDs get brighter wi

LED manufacturers can boost chip performance by up to 30% if they replace ITO contacts with those based on ZnO, says Structured Materials Industries' **Gary Tompa**.

GaN LEDs are a great success. They have created a multibillion dollar market and are now used in many applications, including mobile phone displays and keypads, small screens and architectural lighting systems. However, if LED sales are to continue to grow at a rapid rate, then traction is needed in the next lucrative application, the $60 billion solid-state lighting market. But success in this sector will require cheaper, even more efficient LEDs, that can only be achieved through refinements in high-volume manufacturing technologies.

At Structured Materials Industries (SMI) – an MOCVD equipment manufacturer based in Piscataway, New Jersey – we have developed one such technology, a production-compatible method for depositing ZnO contacts. These contacts are transparent, and when they replace those based on light-blocking metallic films they can increase LED light output by 80%.



ZnO films with various different morphologies can be produced by MOCVD, including **(a)** highly crystalline continuous films, **(b)** close-packed crystalline columns and **(c)** arrays of nanowires.

LED designs

The drawbacks of any form of metallic contact can be seen in many of today's LEDs, which are generally built on a sapphire substrate that is transparent but electrically insulating. The LEDs are produced by growing a buffer layer on the sapphire, followed by n-type GaN, a multiple quantum-well active region and a p-type layer that is difficult to dope highly. Contacts are then added before the LED chip is packaged. Such designs have the potential to be very efficient and can even deliver 200 lm/W. However, today's LEDs deliver just half of this value or less, partly because a significant proportion of the light emitted from the active region remains trapped in the structure.

The first generation of LED devices, for example, featured metallic patterned contacts to the p-layer and n-layers that block or attenuate light and reduce the device's emitting area (figure 1a and 1b). Such devices also produce weaker emission farther from the contact, due to the low conductivity of the p-type contact layer. Both of these weaknesses can be addressed by switching to a thin metal layer across the surface to improve current spreading within the structure, but the benefit of more uniform light emission comes with the penalty of attenuated emission caused by the new contact.

Moving to a thin-film contact also increases the chances of catastrophic burn-out at stronger currents. Thickening the contact's layer can reduce this risk, but it also cuts the extraction efficiency. Although techniques such as the introduction of photonic crystal structures or surface roughening can reduce light trapping in the device and boost extraction, LEDs with this design will never operate at their theoretical maximum.

The only way to address the inherent weaknesses of the metallic contacts directly is to replace them with transparent conductors (figure 1c). Indium tin oxide (ITO) is the obvious choice because it is already widely used in flat-panel displays and photovoltaics. With this material, LED output power increases by 30–50%, but the deposition technique used for the contact, electron-beam evaporation or sputtering, cannot routinely deliver high-quality films, which is a major drawback to volume production. As we will see later, however, ZnO can overcome this problem and offers several other advantages besides.

There are also manufacturers employing designs that are essentially free from conventional metallic

Structured Materials Industries' ZnO MOCVD reactor

Structured Materials Industries produces ZnO reactors featuring high-speed rotating discs with a variety of capacities: 1 × 1, 1 × 2, 3 × 2, 6 × 2, 8 × 2, 19 × 2 and 38 × 2 inch. These SpinCVD tools use a uniformly heated deposition plane to grow uniform films over large areas at a deposition rate of 10–20 nm/min.

The uniform deposition results from a four-zone heating system that is compatible with the high temperatures, thermal expansion and oxidizing environment associated with ZnO growth. With this design, the largest reactor delivers a temperature uniformity across the wafer carrier that varies by less than 1%, and can produce doped and undoped films with

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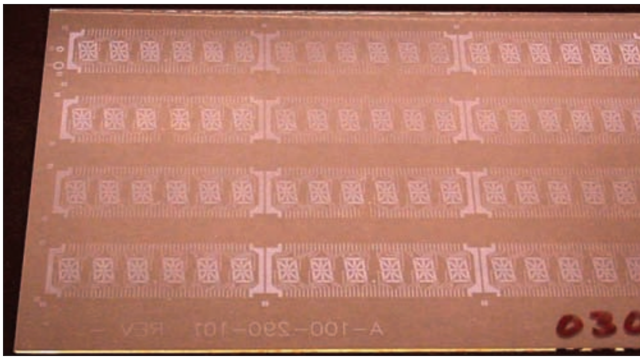

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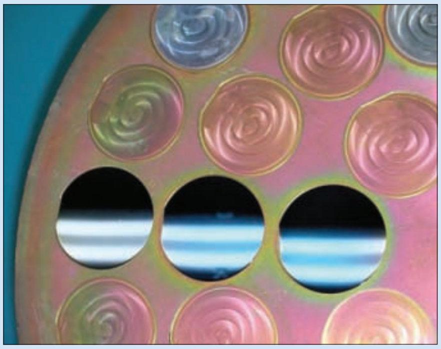
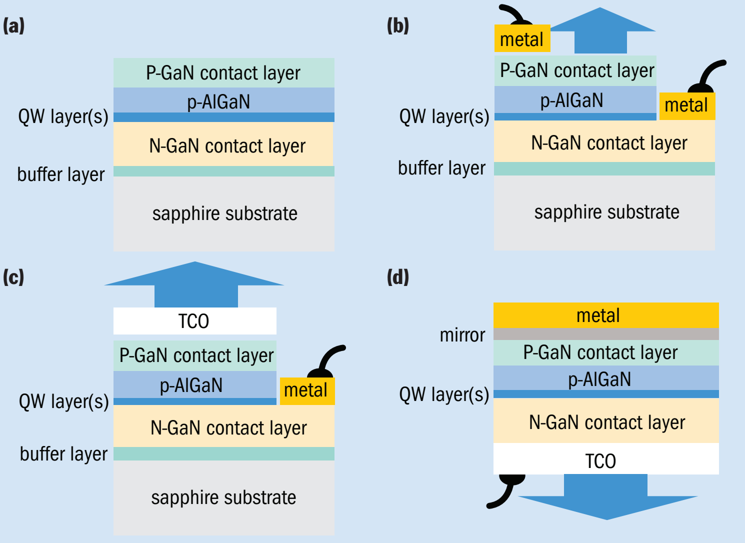


Filament heating is used in the reactor, alongside rotation speeds of hundreds of revolutions per minute. The multiwafer reactors can deposit ZnO on silicon, quartz and GaN.



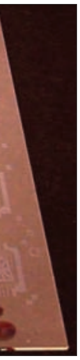
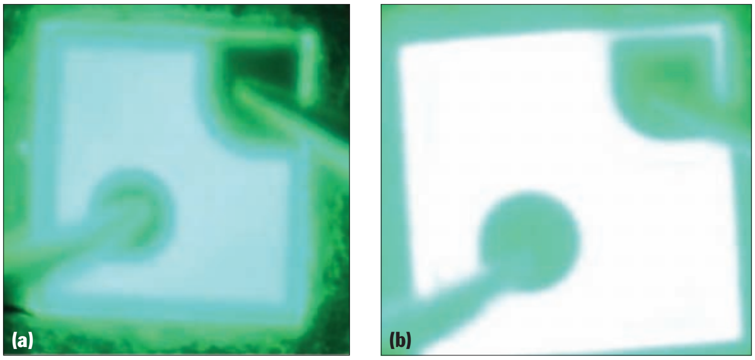


Fig. 1. (above right) LED design has evolved to increase extraction efficiency, but all forms have the same basic epilayer structure **(a)**. Metallic contacts can be added to this structure, but they block the light generated by the active region and reduce the effective emission area **(b)**. Transparent ITO can overcome this drawback and form the top contact of a conventional design **(c)** and a flip-chip structure **(d)**. **Fig. 2.** (left) MOCVD-grown ZnO films have a transparency of 85–90% and can easily be etched. **Fig. 3.** (right) LEDs with ZnO contacts showed higher light extraction efficiency than equivalents with metallic and ITO contacts. At 40 mA, the Ni/Au-contacted GaN LED **(a)** produced 191 mcd and the ZnO contacted equivalent **(b)** produced 355 mcd, which saturated the camera. The ITO variant, which is not shown, produced 271 mcd.



contacts and instead feature a highly reflective mirror. These include LEDs that feature light extraction through the sapphire substrate (figure 1d). This approach certainly mitigates the current spreading limitation of the p-layer and enhances uniform light-level emission across the LED. However, light extraction is still far from perfect and, as the chip size increases, current spreading in the n-type layer starts to limit performance. Some LED developers have even resorted to "drilling" multiple n-type contact holes, but every new contact hole is a black spot, in terms of light emission, that detracts from the overall light output.

Mirrors also feature in commercial designs that incorporate a flip-chip structure. Again, the p-side layer is contacted uniformly but this time a thicker metallic layer provides mechanical support for the chip. The sapphire is then removed, allowing direct contact with the n-type layer. This exposed film has the high-defect-density buffer layer at its surface, which produces optical losses, but this can be overcome by polishing. A top contact is still needed and again a transparent version should be used for maximum extraction efficiency. Surface roughening and photonic crystal structures can also be added to boost light extraction.

The various LED designs that we have just described highlight the effort that has been applied to overcome the problems associated with metallic contacts. But turning to a high-quality, conductive and transparent contact remains the best way to overcome this problem and we believe that this approach – in conjunction with the use of photonic crystal structures or surface roughening – will play a major role in the brightest and highest-efficiency LEDs for some time to come.

ZnO vs ITO

ZnO is an ideal contact material because it is transparent throughout the entire visible spectrum and at ultraviolet wavelengths that are often used to pump light-emitting phosphors in white LEDs. ITO can

Table 1. The choice for an LED contact

	Ni/Au	ITO	ZnO
Optical transparency	poor	good	good
Lattice match to GaN	poor	moderate	good
Thermal stability	poor	moderate	good
Refractive index and bandgap grading	no	minimal	excellent
Columnar microstucture	no	no	yes
Overall economic benefit	poor	moderate	good

Table 2. Different ZnO deposition technologies

	Electron-beam evaporation	Sputtering	MBE	CVD or MOCVD
Step coverage	poor	poor	poor	good
Scalable to high volume	no	yes	no	yes
Post-deposition annealing required	yes	yes	no	no
Composition grading	no	no	yes	yes

also fulfil this criterion but ZnO has several advantages, including better thermal conductivity, a much smaller lattice mismatch to GaN and a superior high-temperature stability (table 1). In addition, ZnO can be wet and dry etched, and doped with aluminum, indium and gallium to improve conductivity.

ZnO also has one other key advantage over ITO for LED manufacturing – a better, more reproducible growth process. ITO is deposited by either PVD processes, such as MBE and electron-beam evaporation, or by sputtering. All of these techniques tend to produce poor-quality films on surfaces of varying topography, such as those found on an LED's top surface. This weakness, referred to as poor step coverage, produces poor contact reliability and limits device yield. MBE and electron-beam evaporation of ITO are also difficult to scale to large-volume production, while sputtering processes actually damage the devices.

MOCVD, the process we use to deposit ZnO at SMI, is immune from all of these issues (table 2). It is also suitable for volume production and is highly compatible with the GaN device fabrication process thanks to the shared growth method. LEDs produced by this method are also free from post-growth annealing used to activate the p-type dopant, because MOCVD is a thermally driven process.

ZnO films grown by MOCVD can also be produced with a range of morphologies, including highly crystalline continuous films, close-packed crystalline columns and arrayed nanowires. This allows surface texturing of the LED's contacts, which can further boost extraction. We have already developed the MOCVD processes to produce three different types of ZnO surface morphology and we plan to investigate the influence of contact morphology on LED performance.

We have demonstrated the benefit of ZnO contacts by depositing them on GaN epiwafers using our own high-speed rotating disc reactor, which has 38 × 2 inch wafer capacity (see box, "Structured Materials Industries' ZnO MOCVD reactor", p14 for details). These aluminum-doped ZnO contacts, which have a thickness uniformity of a few percent, were deposited with a growth rate of 10–20 nm/min and form a good ohmic contact with a resistance of less than 10^{-3} Ω/cm.

We compared these ZnO-contacted LEDs with two different control devices made from a conventional NiAu thin film and ITO. At drive currents of 10–80 mA, the LEDs with a ZnO contact delivered 80 and 30% more light than the devices with metal and ITO contacts, respectively (figure 3). The ZnO-based LEDs also produced a five-fold or more gain in lifetime during a conventional burn-out test. These significant improvements in LED power and lifetime produced by the addition of ZnO contacts have led us to file a patent to protect our technology.

Routes to higher outputs

This initial result illustrates the potential of ZnO contacts, but we believe that many further improvements in LED performance are possible through engineering the bandgap of ZnO alloys, the incorporation of photonic crystal structures and the direct deposition of phosphor structures. CdZnO and MgZnO alloys can also be grown by MOCVD and would allow tuning of the contact's bandgap and optical properties to optimize a particular LED design. Rare-earth elements, such as thulium, manganese and europium, could also be added during ZnO growth to produce luminescent contacts using either a single or dual deposition system. Growing and passivating a light emitter without breaking vacuum is clearly an appealing option and we have already fabricated a simple structure containing a green phosphor, ZnSiO:Mn, which produces cathodoluminescence, electroluminescence and photoluminescence.

Our results demonstrate that ZnO contacts can improve GaN LED performance. We are now sampling ZnO contact materials with several companies and research groups, including those in Taiwan, China, Japan, Korea and the US. We are working with these organizations to develop processes that can deliver the benefits of ZnO contacts on their particular device structures, which all differ in some way. We hope that this will drive sales of our multi-wafer ZnO MOCVD reactors and ultimately fuel improvements in the performance of commercial LEDs employing phosphor-containing transparent contacts and photonic crystal structures. ●

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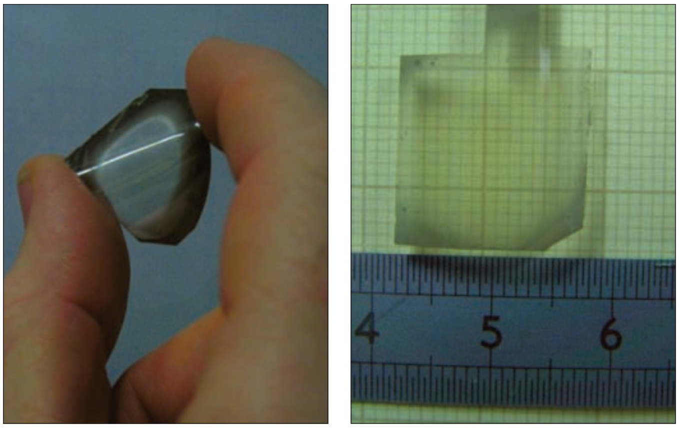
About the author

Gary Tompa (gstompa@structuredmaterials.com) is the president of SMI and founded the company in 1994. He thanks S Sun, G Provost, D Mentel, B Willner and N Sbrockey from SMI and Philip Chan, Keny Tong, Raymond Wong and A Lee from Podium Photonics for their efforts on ZnO development.

GAN

Cubic crystal offers GaN solution

Perpendicular cleaving planes and an absence of polarization fields mark out thick layers of little-known free-standing cubic GaN as the ideal platform for optoelectronic devices, say Nottingham University's **Sergei Novikov**, **Anthony Kent**, **Richard Campion** and **Tom Foxon**.



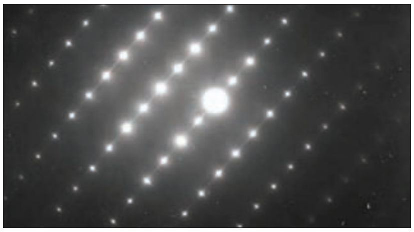


Fig. 1. (left) Nottingham's plasma-assisted MBE process can produce cubic GaN substrates of up to 50 µm in thickness with a surface area of more than 1 cm^2. **Fig. 2.** (above) Reflection high-energy electron diffraction images of 30 µm thick free-standing GaN reveal the high quality of the cubic single-crystal structure.

III-nitride (III-N) devices are being held back by a shortage of bulk GaN for lattice-matched epitaxial growth. Meanwhile, those few that are available command a high price, along with a hexagonal wurtzite structure that is not ideal for all types of device. Although the high-polarity fields that exist in the substrate and the subsequent epilayers – due to a mix of piezoelectric and spontaneous polarizations – aid HEMT design, they cut recombination efficiency and therefore the light output in optoelectronic devices.

This weakness has fuelled interest in the growth of non-polar light-emitting III-N structures. In these devices, polarization effects are eliminated due to growth on the non-polar orientations of the crystal, such as the *m*-plane. However, these non-polar hexagonal bulk crystals and templates are difficult to produce, they are even more expensive than their polar equivalents and their quality, while satisfactory, is far from perfect.

An alternative, more promising method for eliminating the polarization effects in GaN-based devices involves the use of non-polar (100) oriented zinc-blende III-N layers. Although these thermodynamically metastable cubic GaN layers have received relatively little attention, they also have two major advantages over both polar and non-polar wurtzite GaN: they can easily be cleaved on {110} crystal planes for device fabrication, thanks to the geometry of the crystal structure; and they offer a carrier mobility that is an order of magnitude higher, due to the increased crystal symmetry.

Cubic GaN epilayers have already been produced on cubic platforms, such as GaAs and SiC, using specialized growth conditions and MBE, HVPE and MOCVD techniques. The MBE approach is the most promising because it produces the lowest content of hexagonal GaN inclusions. In comparison, the higher process temperature required for HVPE, and especially MOCVD, produces rapidly increasing hexagonal content with further GaN growth.

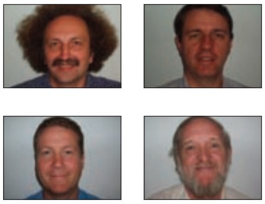
Up until now the thickness of cubic GaN has been limited to 1 µm or so, but research by our team at the University of Nottingham, UK, has shown that MBE can produce far thicker material. This has enabled us to form free-standing GaN, which is a promising forerunner to making cubic substrates.

We grew our undoped, thick cubic GaN films on semi-insulating GaAs (001) substrates by plasma-assisted MBE (PAMBE), using arsenic as a surfactant to initiate the growth of the cubic phase. The growth rate for these films is 0.3 µm/h, which is not particularly fast but is comparable to that used for forming bulk hexagonal GaN crystals from liquid gallium at high pressures.

Examples of our free-standing cubic GaN layers produced by PAMBE include an 8 µm thick piece that has a surface area greater than 1 cm^2 (figure 1). This film is transparent with a shape that reveals its cubic microstructure. It is also strong – it can be easily handled when its thickness is increased to 30 µm or more, enabling it to be used as a substrate for cubic GaN-based structures and devices.

We have investigated the properties of our material using a range of ex situ techniques, such as X-ray diffraction, reflection high-energy electron diffraction (RHEED), transmission electron microscopy, photoluminescence (PL) and nuclear magnetic resonance spectroscopy. All of these techniques, including RHEED (figure 2), were unable to identify any hexagonal inclusions within the first 10 µm of this material. PL measurements determined that the film's bandgap is 3.25 eV at room temperature and 3.30 eV at 4 K.

When we increased this thickness towards 50 µm, hexagonal inclusions formed in the film with a concentration of up to 10%. We plan further investigation into the nature and density of this and other types of defects in cubic GaN and to work in partnership with Sharp Laboratories of Europe in a program funded by the UK's Department for Business, Enterprise and Regulatory Reform that is aimed at refining our technology for commercialization. This effort will focus on increasing the material's size and growth rate.



About the authors

Sergei Novikov (top left) is a senior research fellow in the School of Physics and Astronomy, University of Nottingham. He is responsible for the MBE growth of III-nitride semiconductors. **Anthony Kent** (top right) is a professor at the University of Nottingham. His research focuses on fundamental physical properties of III-V semiconductor nanostructures and devices, including those based on GaAs and GaN. **Richard Campion** (bottom left) is chief experimental officer in the school. He is responsible for the MBE growth of III-V semiconductors. **Tom Foxon FRS** (bottom right) is a research professor at the University of Nottingham.

Optoelectronic Device Yield

By Frank Burkeen

Senior Product Marketing Director at KLA-Tencor
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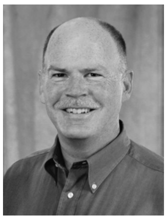

The last decade has seen the evolution of many new optoelectronic devices which affect our daily lives. Automobiles, cell phones and PDAs, digital cameras, and computers contain an increasing number of microdisplays, high-brightness light-emitting diodes (HB-LEDs) and power devices based on compound semiconductor manufacturing techniques. With our ever-increasing consumption of these devices, this market growth and rapidly emerging technologies place tremendous pressure on manufacturers to get product to market.

Automated defect inspection has been a critical part of the semiconductor manufacturing process for detecting manufacturing problems early to reduce costs and increase product yield and performance. In the optoelectronics world, these defect inspection techniques translate as semiconductor wafer materials, in addition to silicon, are often used. The use of automated defect inspection has much less pervasive in optoelectronics wafer processing than in silicon wafer processing, but that is changing with the ever-present need to reduce costs and increase yield. A number of global manufacturing facilities are employing an Optical Surface Analysis (OSA) inspection technique that combines the elemental principles of scatterometry, ellipsometry, reflectometry, and topographical analysis to detect and classify defects in optoelectronic substrates and films.

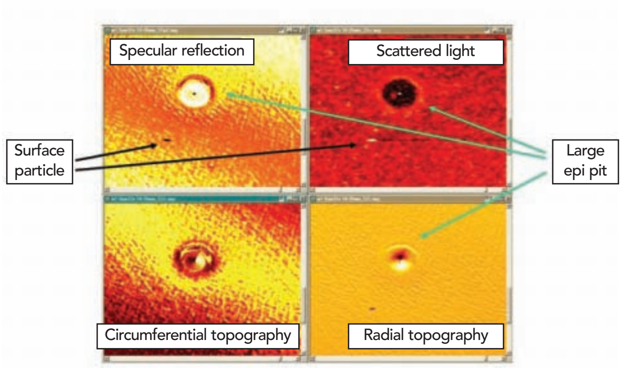

Figure 1: Defect images from four OSA signal types from a sapphire wafer with GaN epitaxial layers.

HB-LEDs

HB-LEDs are composed of multiple epitaxially grown layers of GaN and AlGaN, and are usually grown on one of two types of substrates: silicon carbide or sapphire. These have different advantages and disadvantages, but share one major downside. Due to the fact that the epitaxial layers are not latticed matched to the substrate, the defect density in the epitaxial layers is much higher than in homoepitaxial processes (such as in GaAs or Si epi layers). Fig. 1 shows the same portion of a wafer (about 2 mm by 2 mm in size), with two types of defects visible. The optical signatures for these two defects are clearly different and can be recognized separately by the OSA software.

POWER DEVICES

Some SiC-based power device manufacturers rely on manual microscope inspection with the process being very time consuming and not capable of finding all critical defects. OSA can be used to detect and classify defects in SiC substrates and epi layers automatically. As an example, the surface of GaN HEMT wafer contains an AlN buffer layer, a GaN layer, and an AlNGaN surface layer grown on a SiC substrate. Inspection can be performed in various stages of the manufacturing process of these devices. Fig. 2 shows a micropipe defect and a crystal defect commonly called a triangle defect, which only appears in topography signals. Micropipes appear as elongated defects in OSA images, making them easy to detect and classify.

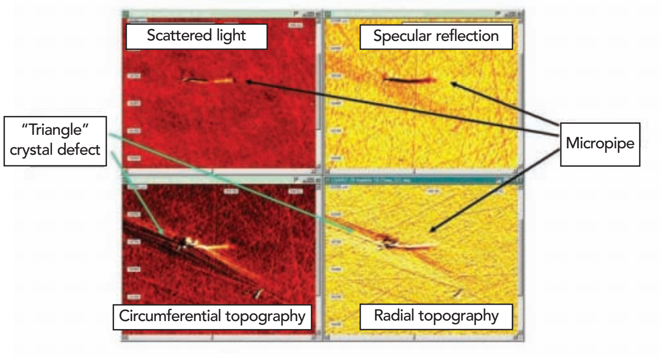

Figure 2: Defect images from four OSA signal types from a SiC wafer.

MICRODISPLAY

A new generation of CMOS imagers, LCoS displays, and digital light processing devices have been widely adopted into many consumer products. Many manufacturers have relied for years on manual microscope inspection making the process time consuming for 100% inspection. Inspection of the glass substrate and coated layers is challenging because defects such as stains from washing processes remain transparent and difficult to identify visually. Defects as small as 1 micron in size in advanced imagers have the potential to create blurry images where the manufacturer has to scrap the devices, thus lowering yields and profitability. The OSA system for glass wafer inspection is very sensitive to residues and other thin films

Manufacturers must find new ways to optimize their new product processes and decrease defect rates to stay profitable and competitive. Relying on manual optical microscope inspection is no longer an alternative at high volume rates and when every new device generation is more complex. Manufacturing processes require sufficient data about each and every process in order to create a defect yield management strategy that is effective and competitive. OSA technology can help manufacturers to automate the defect inspection process for optoelectronic devices, and this technology can be employed in incoming substrate inspection, post-clean wafer inspection, and after epi and film deposition processes.

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Palladium barrier cuts materials bill

If you develop the right process, a switch from a platinum to a palladium barrier can cut your PHEMT production costs without compromising leakage currents, says Skyworks' **Kezia Cheng**.

One of silicon's primary strengths is a stable complementary oxide that can form the gates of electronic devices such as MOSFETs. Unfortunately, III-Vs are not blessed with a high-quality equivalent of SiO_2. Although there has been recent success with esoteric alternatives such as HfO_2, the gates used for manufacturing numerous MESFETs, PHEMTs and so on are metallic structures that form a Schottky barrier contact.

This metallic gate usually consists of three different layers, such as a titanium/platinum/gold sandwich structure. Titanium is the popular choice for the base layer that contacts the semiconductor because it forms a high-quality Schottky junction due to its work function and barrier height characteristics. It also adheres well to the semiconductor, but is let down by its poor electrical conductivity – its bulk resistivity is $4\times10^{-5}\,\Omega$/cm – so a gold layer is added to address this weakness. However, gold tends to migrate and diffuse through titanium into the device, which degrades performance. So to combat this, a barrier layer is sandwiched between the titanium and gold to prevent diffusion.

Platinum is the common choice for this barrier, but as everybody who's bought a platinum ring would know, it is expensive. What's more, the price for refined material has quadrupled in recent years towards $50/g. So at Skyworks Solutions we have been developing a gate using palladium. This alternative is only about one-sixth of the cost of platinum and can significantly reduce our transistor's bill of materials, although the process is little different.

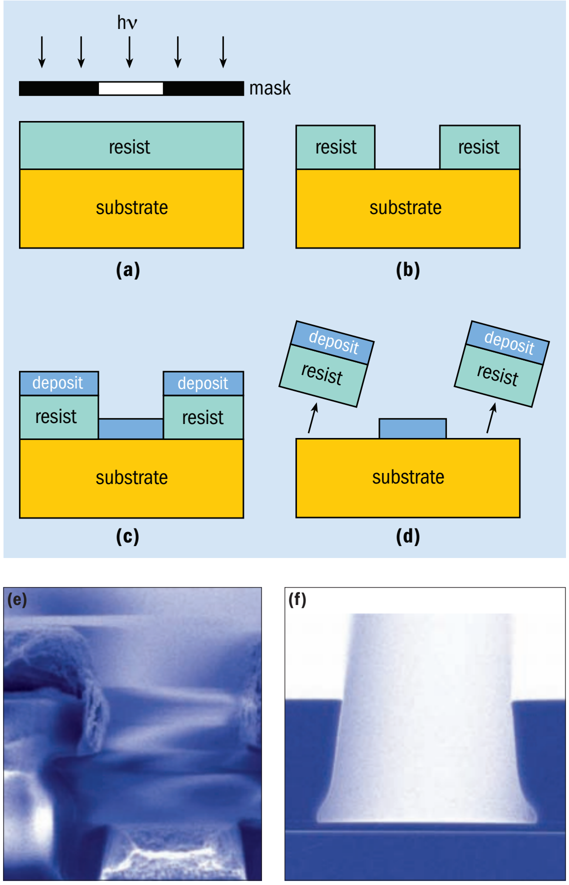
Our gates are fabricated with a lift-off approach that is widely used throughout the industry (see figure 1, p20). A photoresist is applied to the wafer, before it is patterned using a mask and photolithography. The exposed film is then developed and a metal film is evaporated onto the patterned wafer, before the remaining photoresist is removed to leave metallic contacts.

The particular process that we use involves a negative-acting chemically-amplified resist. This is activated by a post-exposure bake and then developed. The nature of the exposure and the acid diffusion kinetics creates a re-entrant profile (figure 1f, p20) and the gates formed by evaporation into this structure have cross-sections that are narrower at the top than the bottom (figure 2, p20).

Many of these gates also feature a "foot" at the base of the metal (figure 3a, p20), which contains gold and palladium material overlapping the titanium layer – as shown by transmission electron microscopy and energy-dispersive X-ray analysis (figure 3b, p20). This overlap is highly undesirable because it allows palladium and gold to contact the semiconductor surface, before diffusing into the epilayer when sufficient activation energy is available.

Skyworks Solutions has cut its PHEMT production costs by developing a new high-yield evaporation process that produces palladium barriers with a low gate-leakage current.

Researchers from Taiwan's Chung-Cheng Institute of Technology and Chang-Gung University have determined that the diffusion mechanism into GaAs is mainly interstitial (the foreign atom is much smaller than those in the lattice, so it can move freely between them), and that palladium transport can occur at low temperatures. This means that the thermal energy associated with the plasma-enhanced chemical-vapor nitride deposition used for passivation and the creation of the capacitor's dielectric layer, which takes place at 250 °C, is suf-



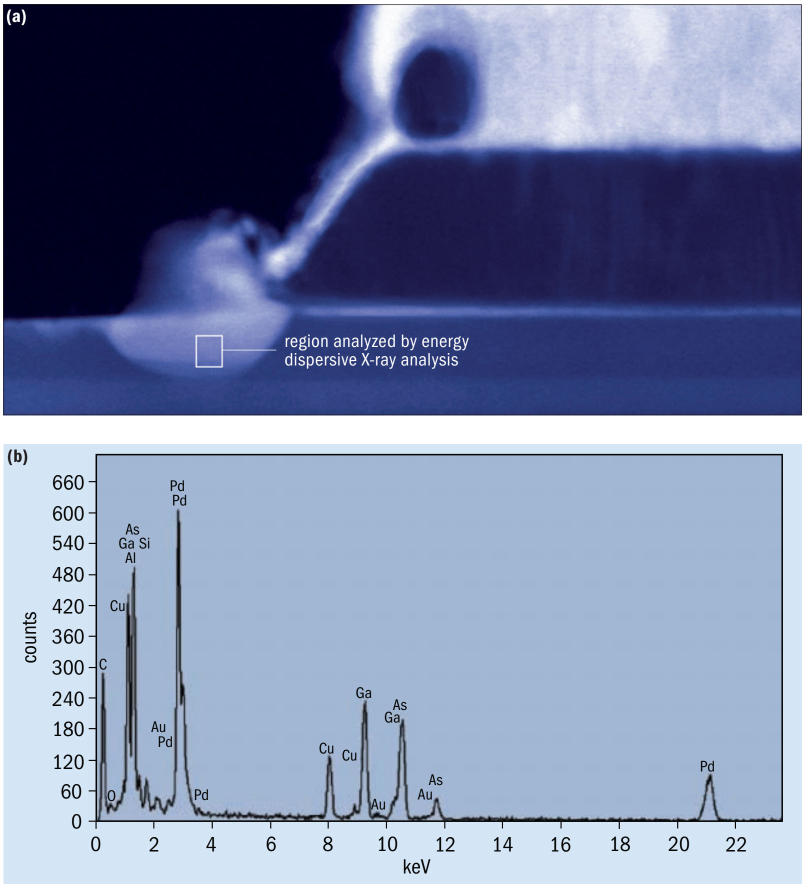


Fig. 1. (top and bottom left) Skyworks uses a conventional lift-off process to produce metal gates for its PHEMTs. After the photoresist has coated the wafer, a mask is aligned before light exposes part of the film **(a)**. Part of the resist is then removed **(b)**, a metal is deposited **(c)** and the metal-on-photoresist regions are selectively dissolved **(d)**. Bilayer structures can also be used for the photoresist **(e)**, but they fail to prevent a foot from forming at the base of the gate. The resist profile used by Skyworks Solutions does not have vertical sides, but instead forms a re-entrant profile that leads to gates that are wider at the bottom than the top **(f)**. **Fig. 3.** (top and bottom right) Focused ion beam/transmission electron microscopy image of the gate **(a)** clearly shows the unwanted foot structure. **(b)** Energy-dispersive X-ray analysis of the outlined area in **(a)** that is associated with this foot, reveals palladium diffusion into the device's epitaxial structure.

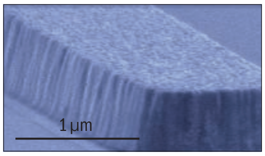


Fig. 2. The gates formed by metal deposition onto wafers with a re-entrant resist profile are narrower at the top than at the bottom. A foot formed at the bottom of the gate leads to the diffusion of palladium and gold into the epilayers, which degrades device performance.

ficient to drive palladium into the semiconductor. Once diffusion is started, palladium and gold can form ohmic contacts with the semiconductor and create a leakage path (see figure 3 for an example). With our normal process conditions, platinum-based barriers rarely suffer from diffusion-related problems and have a lower leakage current than their palladium equivalents.

The unsuitability of our standard process for forming satisfactory palladium-based barriers has driven us to develop an alternative process based on our production Temescal FCE2700 evaporators. These tools feature a metallic source and target separated by 107 cm and are driven by Simba II 15 kW power supplies.

Due to the diffusion issue, our new process must prevent any gold or palladium from coming into contact with GaAs. This is possible by making the titanium layer larger than the palladium and gold layers through the use of a beam sweep for titanium growth. For this layer, the electron beam is swept across the source and titanium is evaporated from an area instead of a point, which increases the area of the deposited layer.

We have also investigated whether lower deposition rates that cut the metallic atom's arrival energy can improve gate quality. When an atom hits the wafer surface it condenses and loses a fixed amount of energy, known as latent energy, and the remainder governs the atom's mobility. By reducing this deposition rate for gold and palladium and using a beam sweep for just the titanium layer, we minimized the gold and palladium overlap with titanium at the base of the gate metal.

We also looked at the effects of film thickness on gate leakage. Barriers were grown with 20% thicker titanium layers and thinner palladium layers, but this variation produced no measurable reduction in the leakage current.

The improvements produced by our new process are clearly illustrated in the before and after images. Focused ion beam/scanning electron microscope images reveal that the existing process produces palladium and gold at the foot of the metal stack and suggest that there is some palladium diffusion (figure 4a, p21). After optimization both of these blemishes are absent (figure 4b, p21). More important, the subsequent thermal treatment applied to the

Comparing processes

	Standard Pd gate	*Optimized Pd gate*
Control leakage at standard growth rate (μA)	14.0	8.3
Control leakage at low growth rate (μA)	9.7	4.3
Second harmonics (dBc)	74.7	73.8
Third harmonics (dBc)	77.2	75.5
Insertion loss (dB)	−0.26	−0.27
Source-drain current (mA)	33.7	33.5

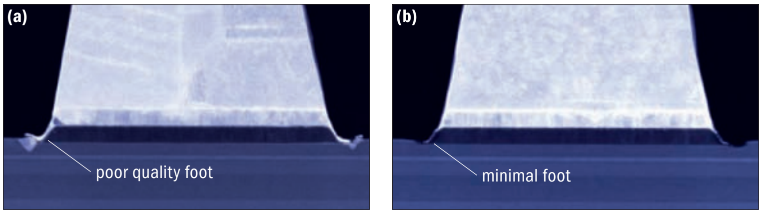


Fig. 4. Optimizing the gate's growth process can substantially reduce the foot's size through the use of beam sweeps and different deposition rates. Focused ion beam/transmission electron microscopy images of the standard process, but with a palladium barrier, show the presence of a substantial foot **(a)**, which is far smaller with the new process **(b)**.

wafer does not drive any diffusion of palladium or gold into the GaAs surface.

The higher quality of our new gates is confirmed by DC process control monitoring tests that compare the performance of our palladium-based gates produced with both processes, using the same mask (see table). At a standard deposition rate the average (mean) gate leakage was cut from 14.3 to 8.2 μA and the standard deviation narrowed from 8.2 to 3.9 μA. Slowing the growth rate also brought significant dividends for both processes and reduced the gate leakage for the optimized process to 4.3 μA. The other key parameters for the device, such as the source-drain current and insertion loss, were unaffected by the new process that delivered a 15% increase in yield compared to the standard process with a palladium-based barrier.

We are now using the palladium-based barrier in production, which has cut our bill of materials. We are also working to improve our understanding of the process and aim to investigate how the sticking coefficients of the metals play a role in the foot formation. Gold and palladium have sticking coefficients of less than unity, so these atoms can reflect off chamber walls and nearby structures to cause a more pronounced foot, particularly at higher deposition rates. Learning how to reduce this foot should ultimately lead to higher yields and make an even stronger case for the palladium-based barrier. ●

Further reading

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About the author

Kezia Cheng (kezia.cheng@skyworksinc.com) is a senior process engineer, responsible for metallization processes. He thanks Larry Hanes and Skyworks Woburn's process engineering and development teams for their technical contributions and Marietta Balandan for assistance in running the experiments.

GAN SUBSTRATES

Vertical HVPE tool produces 2 inch GaN

Aixtron is helping to accelerate the commercialization of free-standing GaN through the launch of a vertical HVPE tool that features a hanging seed holder and is capable of producing 2 inch diameter boules, says **Bernd Schineller**.

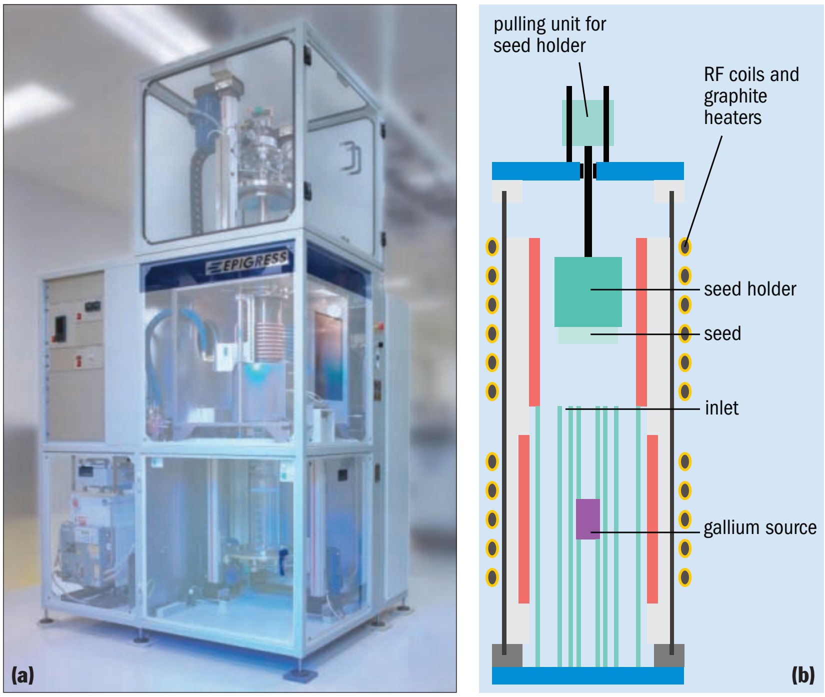


Fig. 1. Aixtron launched its first vertical HVPE system this year, based on its prototype tool **(a)**. The design contains a seed holder that hangs from the top of the growth chamber and gas inlets at the bottom of the chamber **(b)**. The gases fed into the growth chamber (gallium chloride and ammonia) are separated by sheath flows until they reach the growth zone, and an additional wall-purge flow prevents deposition on the reactor walls. Two independent radio-frequency heaters provide chamber heating. Coils on the outside of the reactor chamber induce currents in the graphite heater elements, which effectively delivers heat to the gallium source and the growth zone. Refilling of the source, planting the GaN seed and harvesting the boule can be carried out through reactor gates at the top and the bottom of the tool. The by-product gases, which include hydrogen, hydrogen chloride and ammonium chloride, are swiftly removed from the reaction chamber through a specially designed exhaust manifold kept above 340 °C. This delays the inevitable formation of ammonium chloride dust until the gas reaches a designated high-capacity filter located far downstream of the reaction chamber. With this design several days of continuous growth are possible without interruptions for maintenance, to service the exhaust or refill the source.

Defects in GaN optoelectronic devices, such as 405 nm high-power laser diodes, and ultraviolet and blue LEDs, cut light output and lead to failure at high current densities. To combat this, manufacturers employ elaborate buffer schemes for growth on foreign substrates that minimize the defect densities in the epilayers. However, even the most effective technique – epitaxial lateral overgrowth – pays significant penalties for the reduced defect density. Process steps are more expensive and complex, and produce a smaller usable wafer area, which impairs production yield.

These weaknesses highlight the need for a free-standing, affordable, low-dislocation-density GaN substrate. A great deal of research is being carried out in this area, using techniques such as HVPE, high-pressure solution growth, ammonothermal growth, physical vapor transport and sublimation growth.

Today, HVPE is the most popular technique for manufacturing free-standing substrates, thanks to its process maturity, controllability and reasonably high growth rate. Several companies around the world are currently marketing GaN substrates made with this technique, which are often grown on single or multi-wafer tools on foreign templates, such as sapphire.

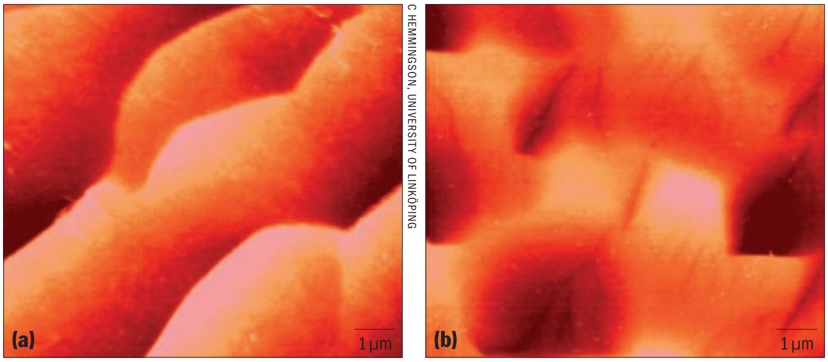
It is logical to try to extend this growth and to produce a boule that is several centimeters thick, which is an approach that is already being pursued by various companies in the US and Asia. Wire saws can then cut several substrates from this boule before they are polished. In addition, one of these substrates can also be used as a seed for the subsequent growth, leading to a steady fall in the dislocations in the material, and allowing growth on lattice-matched material.

Growth by HVPE is clearly an attractive option, but it poses several challenges, including a by-product of GaN growth – ammonium chloride – which forms a caustic dust below 340 °C. This dust must be kept away from the growth area, where it could contaminate the GaN boule, and the exhaust system, which it can clog up, therefore delaying what are already lengthy growth processes.

At Aixtron, in Aachen, Germany, we have developed a vertical HVPE chamber that addresses this issue. The new tool is capable of producing 2 inch diameter boules up to 7 cm thick using growth rates of several hundreds of microns per hour (figure 1). This reactor, which we launched commercially this year, features a boule hanging face-down from the top of the reactor. This set-up prevents any ammonium chloride from falling onto the growth surface. The rotated boule can also be retracted at a rate that maintains a constant distance between the gas inlet and the growth surface.

Before launching this mass-production system, we built two similar prototype systems with comparable reactor geometry. These tools have been installed at the University of Linköping, Sweden, and the Ferdinand Braun Institute for High-Frequency Technology (FBH) in Berlin, Germany.

Researchers at the University of Linköping have assessed the quality of the material grown by HVPE. They used atomic force microscopy to investigate the surface of 250 µm thick and 2 mm thick layers of GaN that are grown on GaN-on-sapphire templates under identical growth conditions (figure 2, p23). Increasing the layer thickness produces a change in



C HEMMINGSON, UNIVERSITY OF LINKÖPING

Fig. 2. Atomic force microscopy measurements of 250 µm thick **(a)** and 2 mm thick **(b)** GaN epilayers reveal that the growth of additional GaN alters the material's morphology but does not degrade the surface. These films were grown on GaN-on-sapphire templates. The z-scale for these images is 25 nm.

growth morphology but does not affect the film's roughness. This maintains a root-mean-square value of 3 nm for a 10 µm × 10 µm scan size and a peak-to-valley height of 10–15 nm. This lack of variation in the surface's roughness indicates that its quality is unaffected by growth. As expected, additional GaN growth cuts the epilayer's defect density, with the etch pit density decreasing from $2 \times 10^6\,\mathrm{cm}^{-2}$ for the 250 µm thick layer, to $5 \times 10^5\,\mathrm{cm}^{-2}$ for the 2 mm thick layer. This implies that thicker boules will not only yield more wafers but also produce material with lower defect densities.

We are continuing to work with various research and development labs to improve the GaN HVPE tool and the growth process. This effort, which should ultimately improve the performance of GaN devices, includes the installation of a next-generation mass-production system later this year at FBH. This tool, which is similar to our commercial HVPE reactor but features a modified gas inlet configuration and substrate holder, will be used to improve boule crystalline quality. Once that has been done, efforts will turn to the growth of larger-diameter material, followed by the growth of ternary bulk AlGaN.

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About the author

Bernd Schineller is manager of Aixtron's R&D projects department. He is responsible for the management and coordination of national and European-funded R&D projects inside Aixtron, and the project management of new developments and prototypes. The work referred to in this article was partly funded by BMBF under the contract numbers 01BU404 and 01BU0623. We thank the University of Linköping, Sweden, and the FBH Berlin, Germany, for their contribution to the experimental work.

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PHEMTs rise to wide-gap challenge

New geometries and field plates have extended the operating voltage, power output and efficiency of GaAs PHEMTs to a level where they can compete with SiC and GaN-on-silicon devices, claim **David Fanning**, **Edward Beam**, **Paul Saunier** and **Hua-Quen Tserng** from TriQuint Semiconductor.

Process enhancements can extend the lifetime of cost-effective incumbent technologies and enable them to fight off the threat from new alternatives. Silicon LDMOS amplifiers, for example, have improved in performance, thanks to process advances to fend off rivalling compound semiconductor products. Similarly, GaAs amplifiers are now raising their voltage and power as wider-bandgap technologies come on the scene.

Since GaAs was developed, its operating voltage has generally been restricted to less than 10 V. However, military and commercial base-station applications have driven demand for higher power-output densities, which has led to higher-voltage GaAs processes. At the same time, GaN technology has raised the bar in terms of operating voltage and power-output density. This material has inherent advantages over GaAs, but our results have revealed that it is possible to extend the operating voltages and power-output densities of GaAs further.

Even with these improvements, GaN-on-SiC holds advantages over GaAs in some areas, such as power density and higher-frequency operation. However, GaAs can offer process maturity and proven reliability at a reasonable cost. These benefits are very important in risk-averse markets, such as defense, where RF transistors are used for radar and communications, as well as the cellular-base-station sector. So for systems requiring near-term deployment, decision makers must weigh the maturity, performance and cost of GaAs versus GaN.

Our recent improvements to GaAs performance began with our 0.35 µm power PHEMT process (PWRPHEMT), which we reported in 2002 and released two years later. This extended the operating voltage of GaAs PHEMT amplifiers to 12 V for frequencies of up to 18 GHz. More recently, a modified version of this process, HV3X, has been optimized for power output in the X-band (8–12 GHz). This design delivers 2.0 W/mm – twice the power-output density of conventional GaAs – at a power-added efficiency (PAE) of 55% at 10 GHz.

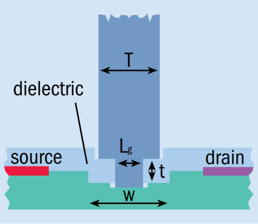
We have also developed an HV3S production process that delivers an operating voltage of up to 28 V, alongside high PAE and high power-output density at S-band frequencies (2–4 GHz). High voltages can be combined with low current operation to produce system efficiency improvements. A high PAE is required at these powers to combat the relatively poor thermal conductivity of the underlying GaAs substrate. By maintaining a suitable PAE, channel temperature and power dissipation are kept to acceptable levels. This process and the HV3X and PWRPHEMT processes are being used for both internal and foundry designs that can serve military applications and cellular infrastructure. Meanwhile, process development currently under-way has demonstrated operation up to 48 V.

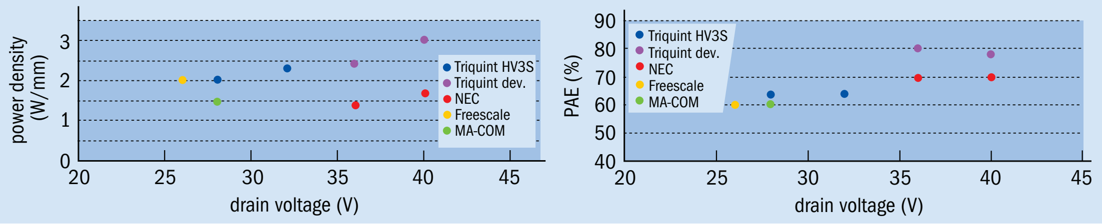
TRIQUINT

TriQuint's 100 mm GaAs fab in Richardson, TX, features tools for gate-metal deposition that are a key part of the process of PHEMT manufacture. The company, which has a history of GaAs development stretching back over 20 years, also has a 150 mm GaAs fab at its headquarters in Hillsboro, OR. The company is also leading a multi-year, multi-company R&D effort into GaN high-power wide-amplifier technology, which began in 2005.

Adding field plates

The first target for our HV3S process was an increase in the operating voltage from 15 to 28 V. Unfortunately the higher operating voltage comes at the expense of current handling and cut-off frequency. Taking HV3X as the starting point, we modified a T-shaped field plate (figure 1, p26), and increased and optimized the channel geometry. The overlapping gate serves as an integrated field





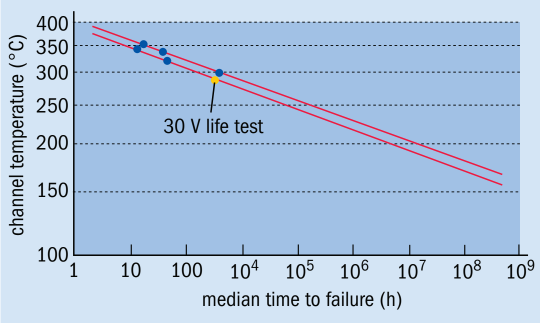


Fig. 1. (above) Adjustments to the channel geometry, such as gate length (L_g), recess width (w), dielectric film thickness (t) and field-plate width (T), have increased the amplifier's operating voltage from 15 to 28 V. **Fig. 2.** (above right) Two of TriQuint's processes, HV3S and one in development (dev), compare favorably with devices made by NEC, MA-COM and Freescale. **Fig. 3.** (right) Lifetime tests reveal that the HVS3 process can produce 24 V devices with a lifetime of 5 million hours at 200 °C. The activation energy is 1.9 eV. The single test at 30 V appears to indicate a similar lifetime.

plate and holds the key to reducing the peak electric field in the channel. By cutting the electric-field strength here, the operating voltage is greatly increased at the expected penalty of diminished frequency response.

Our HV3S process uses identical techniques for metallization and capacitor fabrication to those employed for our established three-metal interconnect (3MI) technology. The epitaxial structure is also similar to our conventional PHEMTs, but it is modified to reduce leakage current at high voltages. At 15 V or more, conventional devices suffer from leakage through the substrate, which degrades the PAE, but the new structure maintains a high PAE up to 40 V. As expected, our HV3S process leads to lower current and transconductance due to a larger gate length and wide recess. Typical values for maximum transconductance and maximum drain current are 250 mS/mm and 450 mA/mm, respectively, compared with values of 400 mS/mm and 600 mA/mm for our 12 V process.

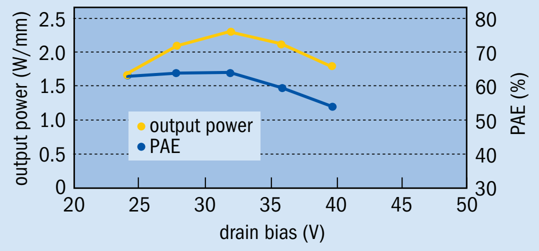
RF load-pull performance measurements at 3.5 GHz on a 4 × 250 µm device reveal a power density of 2.1 W/mm, 14 dB gain, a cut-off frequency of 7 GHz and 64% PAE at 28 V. These figures, which are tuned for maximum efficiency and quote power at the peak PAE, compare favorably with other GaAs PHEMT manufacturers that have developed high-voltage PHEMTs (figure 2).

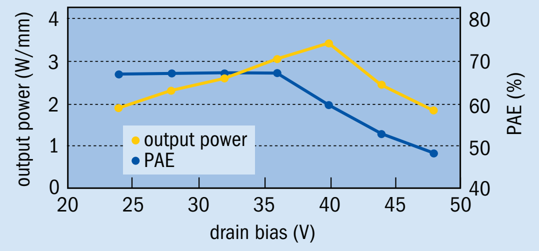
Several MMICs have been designed using the HV3S process. Most are customer owned or competition sensitive, but there is an exception: a single-stage "reliability MMIC" with 4.8 mm of gate periphery, which is suitable for performance monitoring and reliability testing. This MMIC was not designed for high PAE, but it does demonstrate the power capability of this type of chip. At 24 V it delivers 7–8 W between 2.6 and 3.4 GHz at a PAE of 45–51%. The power-output density varies from 1.7 W/mm at 24 V to more than 2 W/mm at 32 V, which is similar to the 1 mm discrete load-pull results. The power and PAE values are also nearly identical to those reported in 2004 for a 4.8 mm SiC MESFET built by George Henry and co-workers from Northrop Grumman, while the gain is about 2 dB higher.

It's imperative to verify that the hike in operating voltage produced by the HV3S process does not come at the expense of any new failure mechanisms. Encouragingly, reliability tests that accelerate temperature and operating voltage reveal that HV3S' temperature performance is superior to that of our conventional GaAs, thanks to the enlarged channel parameters and lower current sensitivity. Predicted lifetimes of a million hours at a channel temperature of more than 200 °C were drawn from an Arrhenius plot that shows a thermal activation energy of 1.9 eV (figure 3). Even at an operating voltage of 30 V, no voltage-accelerated degradation is seen in the data. The lower temperature tests lasted more than 3000 h to expose any lower-activation-energy failures. Using a single-stage reliability MMIC, RF life tests were performed at 24, 27 and 30 V at a reduced channel temperature to focus only on electrical effects. None of the devices degraded during the 2000 RF life hour test and no differences due to operating voltage were observed.

Our high-voltage PHEMTs also deliver robustness, according to qualification tests that involve the load pulling of every wafer at 28 V to verify voltage-handling capability and performance. Measurements showed very consistent results, with standard deviations of 5% and 2% for the power and PAE measurements, respectively. Load-pull tests were also taken at higher voltages until the device failed. These revealed that a 4 × 250 µm device typically delivers 2.3 W/mm and 65% PAE at 32 V, and survives all the way to 40 V. Similarly, we have conducted on-wafer and in-fixture tests of MMICs at over-voltage conditions, which survived to 36 V – the upper limit of our testing apparatus.

We are currently developing a new process for even higher voltage, power-output density and PAE. Further modifications to the channel and epitaxial structure have led to 48 V operation and an





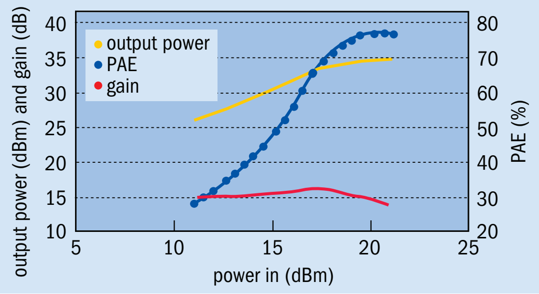


Fig. 4. (above left) TriQuint's PHEMT S-band amplifiers, which are built using the HV3S process, are designed to operate at 28 V but can actually work all the way up to 40 V. **Fig. 5.** (above right) A variant on the HV3S process that's still in development can extend the amplifiers power and voltage capability. At 40 V, this device delivers 3.4 W/mm at 60% PAE. **Fig. 6.** (left) Harmonic tuning can improve efficiency at the expense of power. At 40 V, this 4 × 250 µm device delivered 3.0 W/mm at a 78% PAE. The harmonic impedance used resembles class F operation with a quasi-square wave of voltage for the input and output.

increase in the PAE by typically 5%. With these adjustments, power-output densities of 3.4 W/mm at a PAE of 60% have been delivered at 40 V bias on a 4 × 250 µm device (figure 5).

These gains in output-power densities have demanded comparable improvements in PAE to maintain reliable channel temperatures and can be met by tuning the second and third harmonics. Effects of harmonic impedance on efficiency are well known and amplifiers configured in the class B, over-driven class B, class C, class E and class F mode can all deliver efficiency enhancements. In each case, reactive terminations functioning at harmonic frequencies shape the current and voltage waveforms at the device terminals. For greatest success, overlap between the current and voltage must be minimized to avoid power dissipation that hampers DC to RF conversion efficiency. The load must also be optimally matched at the fundamental frequency for high-efficiency operation. Efficiency improvements with this technique are significant – predictions show drain efficiencies in excess of 80% using optimum terminations for only the second and third harmonics.

Accounting for harmonics

By short-circuiting the second harmonic and using an open circuit at the third harmonic for both the input and output, we have produced a 4 × 250 µm device biased at 40 V that delivers 78% PAE, 14 dB gain and 3.0 W/mm output at 3.5 GHz (figure 6). At a reduced drain voltage of 36 V, the PAE of this class F device increases to 80% with 13 dB gain at 2.42 W/mm. The drain efficiency is 84%, which is very close to the theoretical efficiency of a type of transistor operating in this mode. Harmonic terminations can also be performed on an MMIC, typically at the expense of bandwidth. In the production HV3S process, harmonic tuning enabled 2.1 W/mm and 72% PAE at 32 V.

The performances delivered with our latest process, such as 3.4 W/mm and 60% PAE at 3.5 GHz using 40 V operation, are comparable to SiC and GaN-on-silicon devices. For example, Cree's 1 mm SiC devices operating at 50 V produce 3.4 W/mm and 60% PAE at 3.5 GHz, while Nitronex's GaN-on-silicon FETs deliver 3.9 W/mm and a 62.5% drain efficiency, at 28 V and 3.5 GHz. GaN-on-SiC technology can deliver even better power performance. Published results of S-band frequencies include 5.4 W/mm at 28 V and 10 W/mm at 48 V, and the technology has the potential to go to even higher voltages. More important, GaN-on-SiC delivers high power and PAE at much higher frequencies than any high-voltage GaAs technology. However, for SiC and GaN-on-silicon, frequency performance is more limited. For SiC, the low cut-off frequency limits its upper range to the S-band, while GaN-on-silicon technology has focused on lower frequencies for commercial markets. We have demonstrated X-band operation in GaN-on-silicon devices, but found that RF losses in the substrate will restrict performance at higher frequencies. Since both of these types of device offer a comparable performance to our advanced HV3S results, it is difficult to make a convincing case for deploying these emerging and expensive technologies over GaAs for power applications below 6 GHz. ●

Further reading

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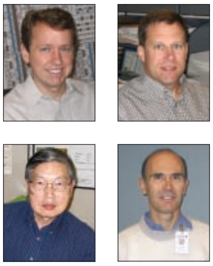


About the authors

David Fanning (top left) is a senior research scientist and program manager in TriQuint's research and development group. He has focused on developing and transferring high-voltage PHEMT processes to production. **Edward Beam** (top right) is a TriQuint fellow responsible for III-V material growth and characterization. Prior to joining TriQuint, he oversaw III-V material development at Texas Instruments' central research laboratory. **Paul Saunier** (bottom right) is a fellow at TriQuint Semiconductor responsible for the development of advanced GaN and GaAs devices. He is the principal investigator for the DARPA contract for wide-bandgap semiconductors for RF applications. **Hua-Quen Tserng** (bottom left) is a TriQuint fellow involved with the characterization and design of high-voltage PHEMTs, AlGaN/GaN HEMTs and MMICs. He has over 30 years experience in the design and characterization of solid-state microwave devices and circuits.

INTEGRATION

Atomic deposition promises InP logic

A collaboration headed by Peide Ye's team at Purdue University has produced the first InP MOSFETs that feature a high-k dielectric layer grown by atomic layer deposition (ALD).

The Al_2O_3 dielectric MOSFETs, which were produced in partnership with US firm Amberwave Systems, address the weaknesses of their equivalents built with SiO_2, such as low channel-mobility and a high interface trap density.

If these devices can be fully optimized, then the InP MOSFET's channel is calculated to deliver a high-field transconductance 60% greater than that associated with silicon, germanium or GaAs, which would produce a very promising candidate for high-speed logic applications.

The team built its transistors on a pre-treated semi-insulating InP substrate. ALD added a 30 nm layer of Al_2O_3, before source and drain regions were defined by implantation and an electron-beam and lift-off process formed AuGe/Pt/Au gates.

The transistors produced a mobility of $600\,cm^2V^{-1}s^{-1}$. This value is higher than that for InP MOSFETs with a SiO_2 dielectric and standard silicon devices, says Ye, which have typical mobilities of $400\,cm^2V^{-1}s^{-1}$. However, a switch to InP epilayers should bring further substantial improvements in the mobility.

A move away from using the InP substrate for the device should also boost the maximum drain current, which was 70 mA/mm at a gate and drain bias of 8 and 3V, respectively.

The researchers are now developing MBE-grown devices and targeting the 22 nm node, which requires an equivalent oxide thickness of 1 nm. "However, our ultimate goal is to make an ALD high-k InP MOSFET on a silicon substrate," explained Ye. "The work presented in our paper is the first step towards that goal."

Journal reference
Y Q Wu *et al.* 2007 *Appl. Phys. Lett.* **91** 022108.

SOLAR CELLS

Layer transfer cuts InP substrate cost

Researchers at Aonex Technologies, the California Institute of Technology and Emcore have developed a technique that promises to cut the cost of four-junction solar cells.

The potential savings would be driven by a switch from a bulk InP substrate to the team's recently fabricated InP-on-silicon composite, which features far less InP material.

"We are now ready to fabricate ultra-high efficiency InGaP/GaAs/InGaAsP/InGaAs four-junction cells on silicon, because we have also developed a technique to make tandems between cells based on InP and GaAs," explained Caltech's Katsuaki Tanabe.

The researchers use a layer-transfer technique that involves bonding InP and silicon, then exfoliating a thin film of InP through ion implantation. Only a few microns of the InP film are consumed in this transfer step, leading to a low materials bill because the donor can be reclaimed and used repeatedly.

The team formed its InP-on-silicon composite by implanting the InP donor with a dose of at least $1 \times 10^{17}\,cm^{-2}$ of He^+ ions. Applying a pressure of at least 1 MPa at 150 °C bonded the two materials together, before they were separated to leave a 900 nm thick InP film on the silicon handle. This composite suffered from a high density of lattice defects near the exfoliated surface, so the top part of the InP film was removed to leave 400 nm of higher-quality material.

MOCVD produced single-junction InGaAs solar cells on this composite and a commercial InP substrate. These were compared using illumination from a source mimicking the spectrum that these cells would receive in a multijunction device.

The InP-on-silicon cell produced an energy conversion efficiency of 13.6% at a current density of $24.9\,mA/cm^2$. This is sufficiently high to current-match to InGaP/GaAs double-junction cells. In comparison, the control device delivered 12.9% efficiency at $21.5\,mA/cm^2$.

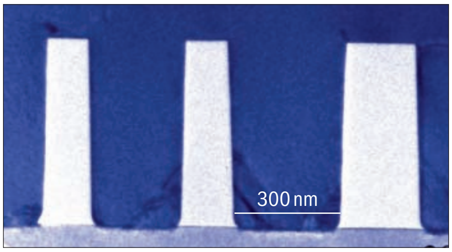
Journal reference
J M Zahler *et al.* 2007 *Appl. Phys. Lett.* **91** 012108.

EPITAXY

Narrow trenches unite GaAs with silicon

Engineers from Amberwave Systems and Sarnoff have developed a dislocation trapping technique capable of producing high-quality GaAs-on-silicon epilayers that are compatible with silicon CMOS and GaAs optoelectronic technologies.

"Crucially, this is achieved with only a few hundred nanometers of epitaxial growth, which minimizes the stress arising from the large difference in the thermal expansion coefficients of the materials," explained Jizhong Li from Amberwave.



Trenches in the SiO_2-on-silicon wafer, with a high trench height-to-width ratio, hold the key to low-defect GaAs epilayers grown by MOCVD.

Li believes that this approach will also work for materials with a larger mismatch, such as InP, and he says that the III-V islands produced by this technique are sufficiently large to accommodate devices such as semiconductor lasers.

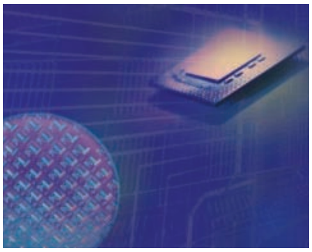
The researchers produced their GaAs-on-silicon layers using a standard 200 mm silicon CMOS line and commercially available production equipment. Photolithography and reactive ion etching formed trenches in a SiO_2-on-silicon wafer with widths of 0.3–2.5 µm, before a GaAs layer was added using growth temperatures and rates of 430 °C and 7 nm/min for the buffer, and 720 °C and 50 nm/min for the top layer.

The trench height-to-width ratio governs GaAs layer quality. At a ratio of 1.8, cross-sectional and plan-view transmission electron microscopy images reveal that the dislocations formed at the hetero-interface are terminated within 200 nm of GaAs growth.

The team is now characterizing its material with techniques such as etch pit density measurements and starting to investigate the growth of electronic and optoelectronic devices on this platform.

Journal reference
J Z Li *et al.* 2007 *Appl. Phys. Lett.* **91** 021114.

the right fit



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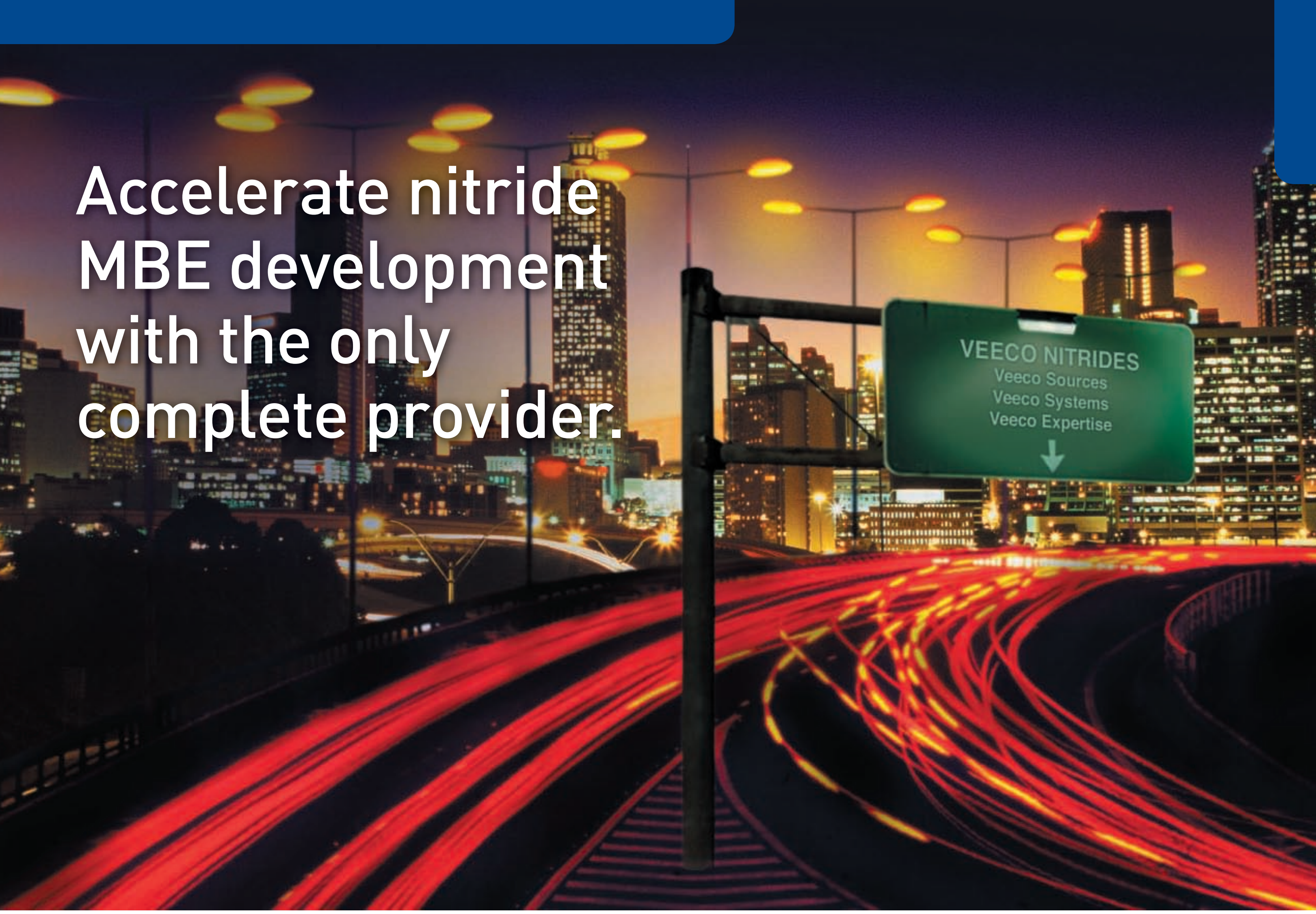
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