

COMPOUND SEMICONDUCTOR

November 2008 Volume 14 Number 10

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

NOVEL MATERIALS

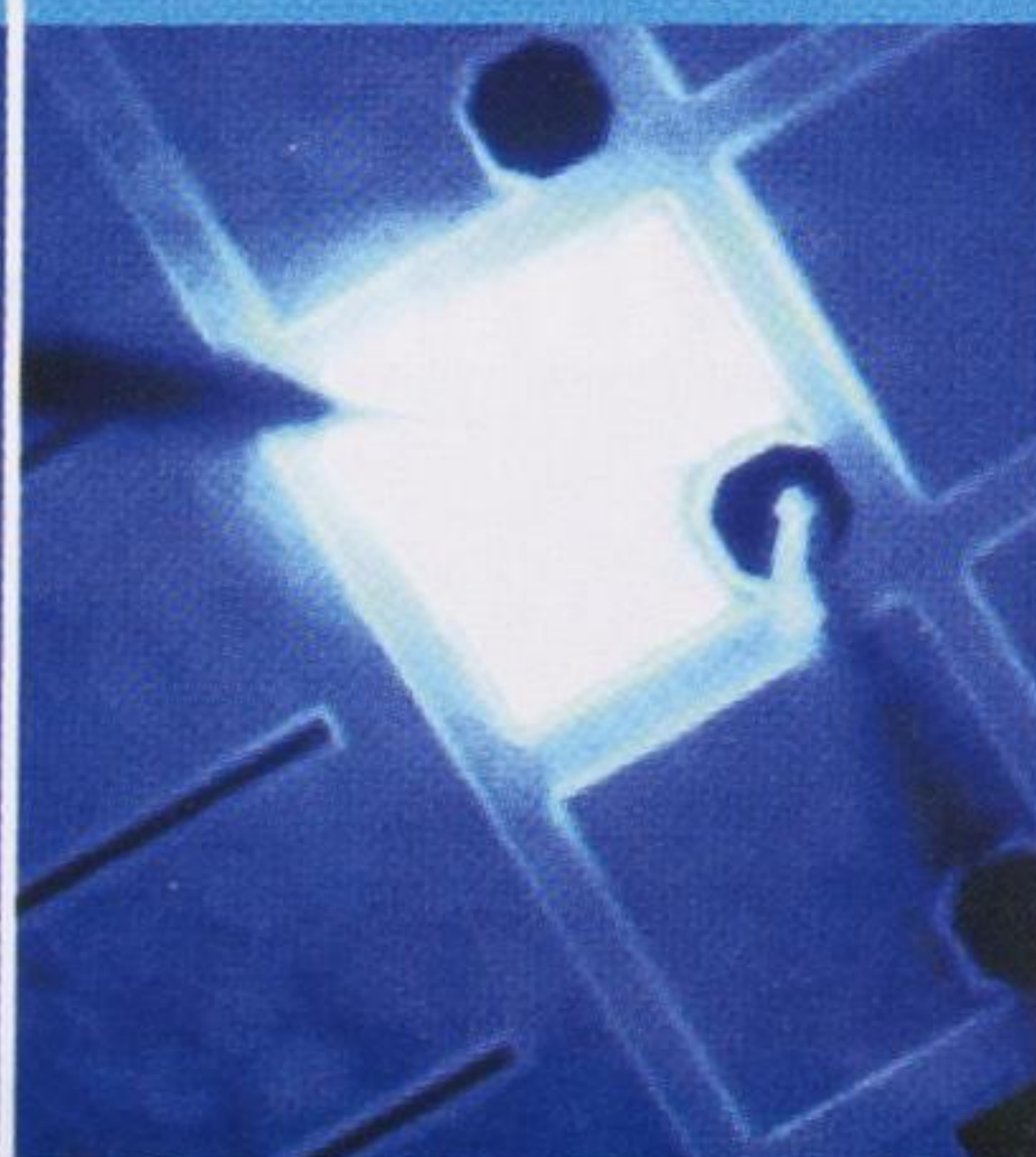
Graphene makes a big splash in Barcelona



OPINION

Aviza sees great opportunities in III-Vs p14

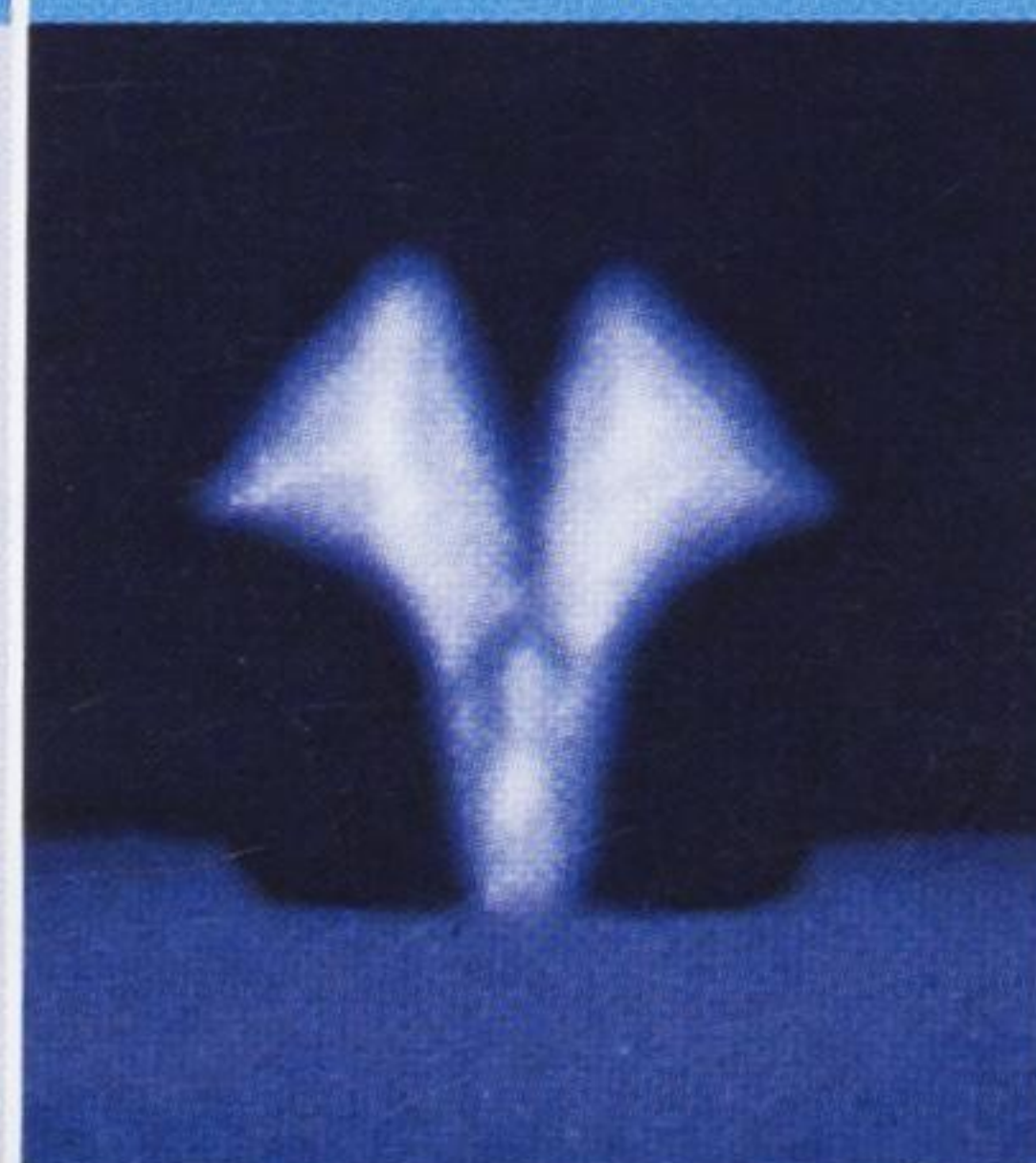
FUNDING



Cash is king

RPI secures \$18.5 m for a new LED lighting center. [p5](#)

RF ELECTRONICS



Ultra-fast wireless

Y-shaped HEMTs form the building blocks for Fujitsu's 10 Gbit/s transmitters. [p29](#)



Meet Lisa. She is a process engineer, working first-hand to improve quality and reduce costs in TriQuint's manufacturing line. She knows that quality is not a separate function or a box to check, it is a culture she helps create. Lisa worked with a diverse team to breakdown traditional barriers between functional areas and implement an advanced system for tracking materials through the manufacturing process. During her ten years at TriQuint, her commitment to increasing yield and reducing cycle times through such projects is part of what makes TriQuint's Commercial Foundry the premier GaAs foundry industry-wide. Lisa is one of the people behind the innovation at TriQuint Semiconductor, and she's on your team.

Learn more about our newest GaAs processes by visiting www.triquint.com/prodserv/foundry/process_info.cfm

TriQuint 
SEMICONDUCTOR

*Connecting the Digital World
to the Global Network®*

INNOVATION
BEGINS WITH PEOPLE

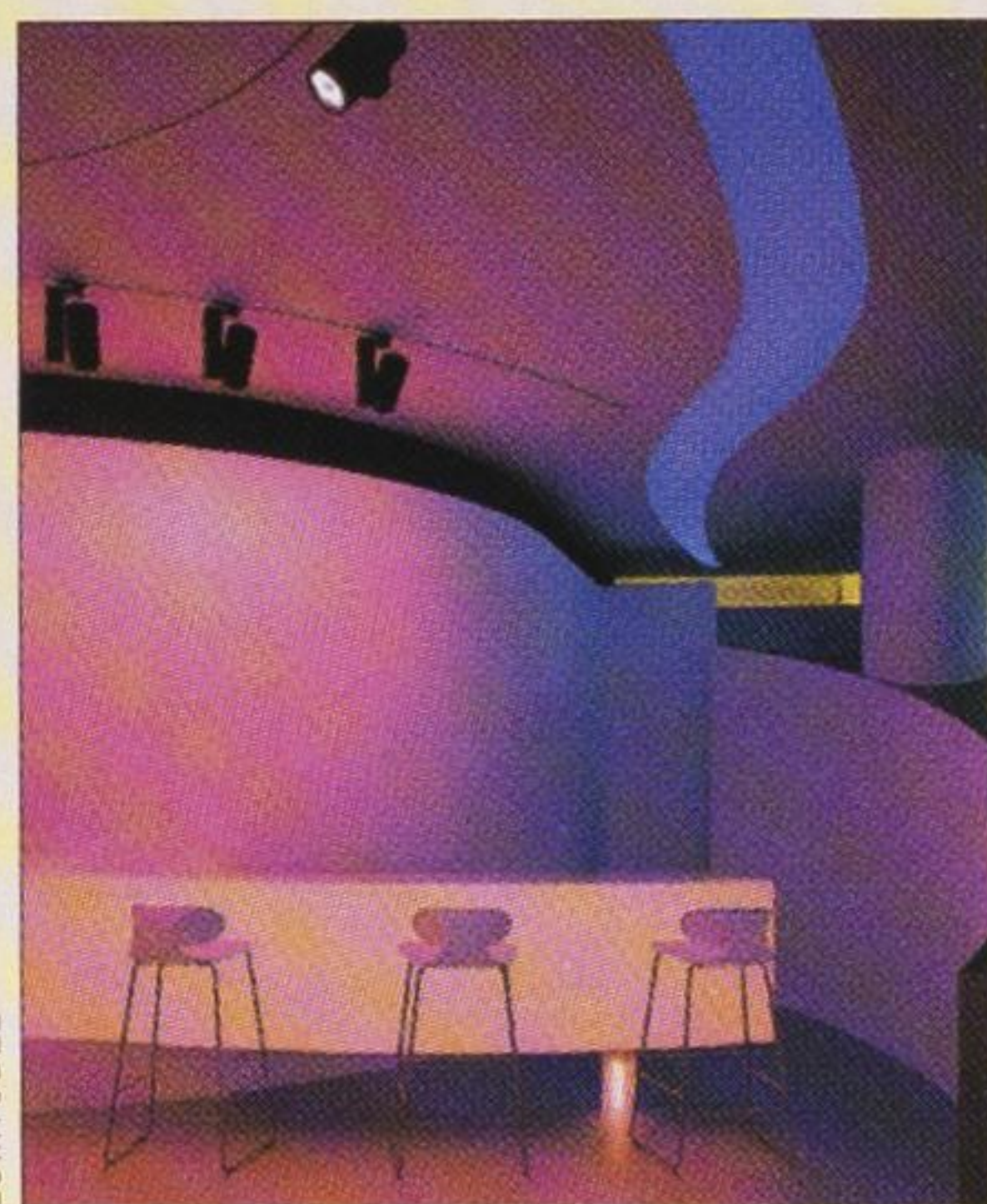
Phone: +1-503-615-9000 • Fax: +1-503-615-8900 • E-mail: foundryinfo@tqs.com • Website: www.triquint.com

INDUSTRY

5 **Headline News:** SEMI urges reformed European vision... RPI gets \$18.5m for smart LED lighting... SolFocus calls for more solar-cell producers.

6 **The Month in RFICs:** Fujitsu makes first 100 W normally off GaN HEMT... Mystery buyer saves SiC-maker Caracal... Record-power SiC devices enhance radar... Riber buys OIPT's MBE group.

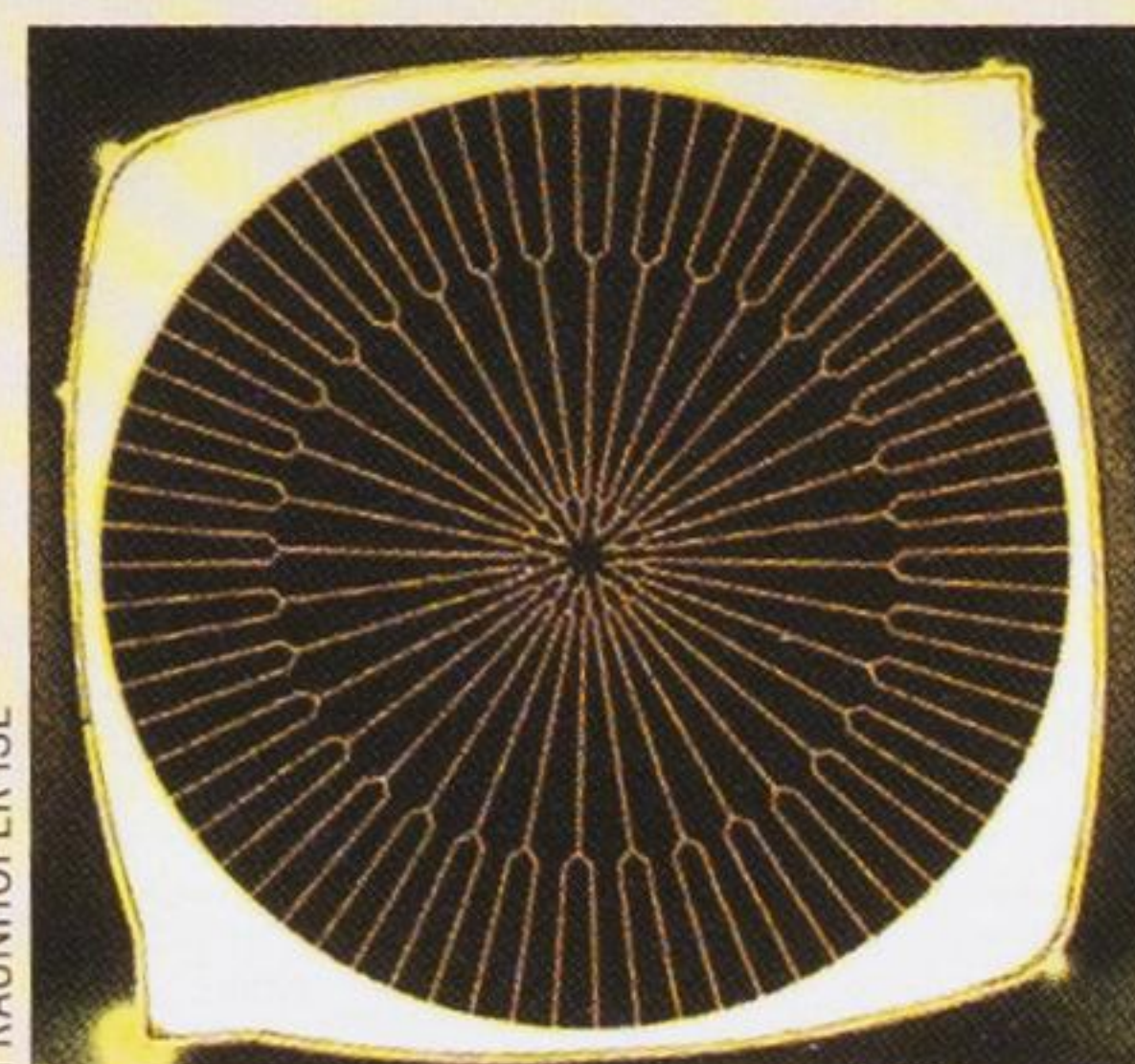
8 **The Month in HB-LEDs:** Cree lands milestone European deal... Mitsubishi expands non-polar substrates... Toshiba hones UV die for improved RGB LEDs.



Deal makers

Leading lighting firm Zumtobel has raised the prestige of Cree's fixtures by signing a long-term deal as their European distributor. **p8**

10 **The Month in Optoelectronics:** European record cell targets CPV... BN doping heralds transparent solar cells... Sanyo diode raises Blu-ray stakes... 3S Photonics unfazed by Avanex tunable woes... PICs lift the economic gloom in Brussels.



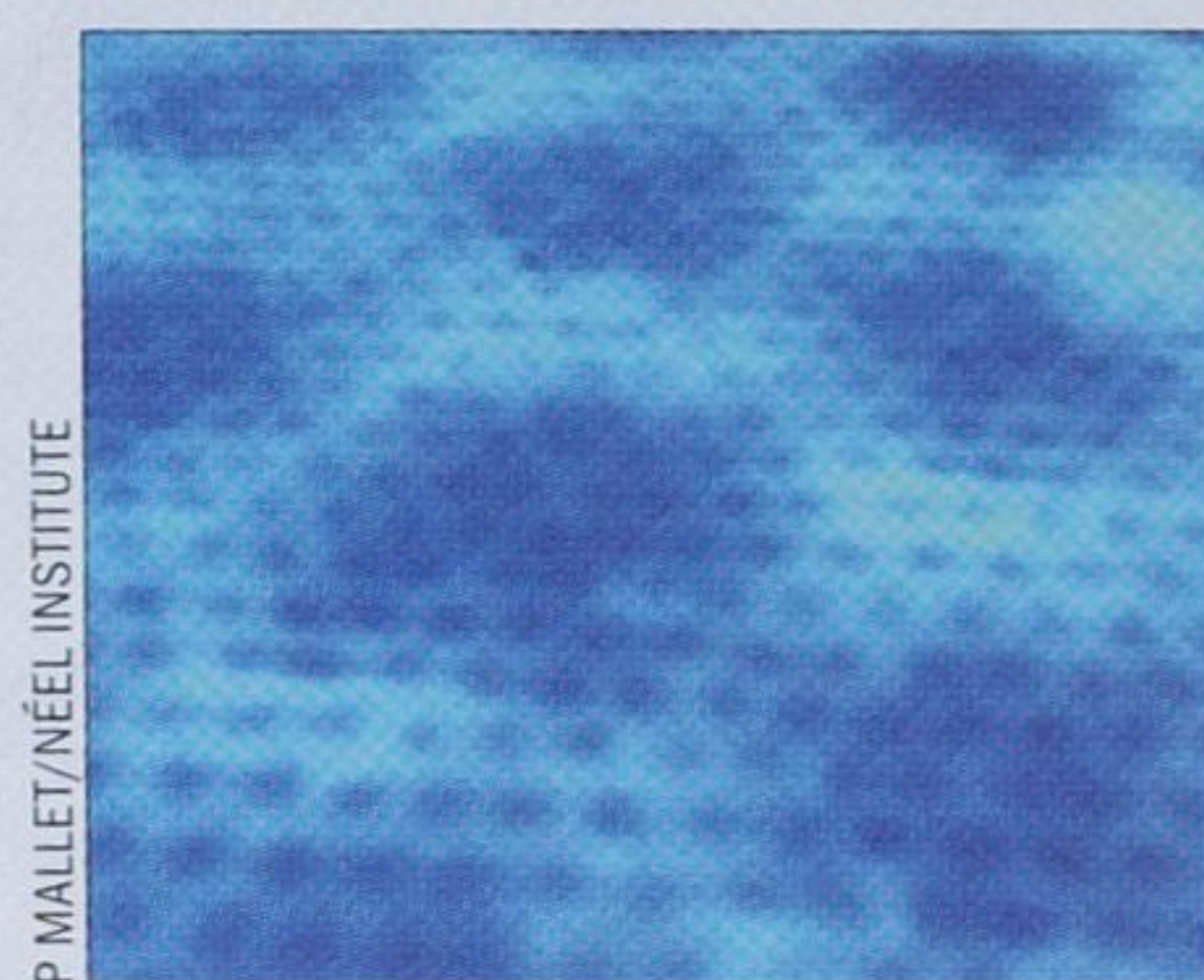
Record breaker

By redesigning its metamorphic III-V cell's gold contacts, Fraunhofer ISE has added more than 2% to its European energy-conversion record. **p10**

14 **Opinion: Aviza sees a bright spot in compounds**
It isn't just Wall Street that's down in the dumps – spending on semiconductor equipment has slumped over the past six months. Fortunately, compound semiconductor markets are bucking the trend, writes Aviza's Kevin Crofton.

TECHNOLOGY

16 **SiC material developments power progress in Barcelona:** Andy Extance saw graphene emerge as a great new hope at ECSCRM 2008, while Japanese car makers help to fuel steady progress towards more-reliable SiC electronics.



Graphene advances

The hexagonal honeycomb structure of monolayer graphene is revealed under low-bias scanning tunneling microscopy at the Néel Institute. **p17**

19 **Uncovering the LED's darkest secret:** Droop stops GaN-based LEDs performing in the critical regime for emerging applications – high-current densities. However, this weakness can be overcome with polarization-matched epitaxial structures, say RPI's Martin Schubert, Min Ho Kim, Jong Kyu Kim and E Fred Schubert.

24 Product Showcase

25 **RFMD gives the BiFET a new twist:** RF Micro Devices' BiFET technology offers a cost-effective route to extending HBT capabilities. JFETs can be created through the growth of two extra layers, an additional mask and just one more etch, say Brian Moser, William Clausen, David Vines and Walt Wohlmuth from the company.

29 **Pulse generator slashes the size and cost of 10 Gbit/s transmitters:** Oscillators, mixers and RF switches add to the cost and complexity of 10 Gbit/s transmitters for last-mile networks. However, all of these components can be discarded by switching to a radical design that just features a pulse generator and an amplifier, says a team of researchers at Fujitsu.

32 **Research Review:** Larger JFET cranks current beyond 50 A... Dashes deliver broad spectral bandwidth... TEM exposes cracks.

Main cover image: Graphene emerged as a leading theme of this year's European Conference on Silicon Carbide and Related Materials, held in Barcelona, Spain. See p16. Credit: Turisme de Barcelona i Espai D'Imatjes.

Editor Michael Hatcher
michael.hatcher@iop.org
Tel +44 117 930 1013. Fax +44 117 925 1942

Features editor Richard Stevenson
richard.stevenson@iop.org
Tel +44 117 930 1192

Reporter Andy Exance
andy.exance@iop.org
Tel +44 117 930 1007

Senior sales executive David Iddon
david.iddon@iop.org
Tel +44 117 930 1032. Fax +44 117 920 0977

Business development manager Rosemarie Guardino
Guardino@ioppubusa.com
Tel +1 215 627 0880. Fax +1 215 627 0879

Sales executive Jeffrey Spratley
spratley@ioppubusa.com
Tel +1 215 627 0880

Circulation manager Claire Webber
claire.webber@iop.org
Tel +44 117 930 1165. Fax +44 117 920 0984

Publisher Michael Hatcher
Production Louise Unwin
Ad production Mark Trimmell
Art director Andrew Giaquinto
Technical illustrator Alison Tovey

Subscriptions
Available free of charge to qualifying individuals working at compound semiconductor fabs and foundries. For further information visit compoundsemiconductor.net/subscribe. Subscriptions for individuals not meeting qualifying criteria: individual £95/\$174 US/€142; library £209/\$378 US/€305. Orders to: Compound Semiconductor, WDIS, Units 12 & 13, Cranleigh Gardens Industrial Estate, Southall, Middlesex UB1 2DB, UK. Tel +44 208 606 7518; Fax +44 208 606 7303. Subscription enquiries: iop@optimabiz.co.uk

8976 average total qualified circulation*
*Updated June 2008 BPA audit statement

Editorial board
Mayank Bulsara Atlas Technology (USA);
Andrew Carter Bookham (UK); **Jacob Tarn** Century Epitech (China); **Ian Ferguson** Georgia Institute of Technology (USA); **Toby Strite** JDSU (USA);
Mark Wilson Freescale (USA); **Dwight Streit** Northrop Grumman (USA); **Joseph Smart** Crystal IS (USA);
Colombo Bolognesi Swiss Federal Institute of Technology (Switzerland); **Shuji Nakamura** University of California at Santa Barbara (USA)

©2008 IOP Publishing Ltd. All rights reserved.

US mailing information: *Compound Semiconductor* (ISSN 1096-598X) is published 11 times a year for \$174 by IOP Publishing, Dirac House, Temple Back, Bristol BS1 6BE, UK. Periodicals postage paid at Middlesex, NJ 08846. POSTMASTER: send address corrections to Compound Semiconductor, c/o PO Box 177, Middlesex, NJ 08846. US agent: Pronto Mailers Association Inc, 200 Wood Avenue, PO Box 177, Middlesex, NJ 08846.

IOP Publishing

Apocalypse when?



To paraphrase Mark Twain: the reports of capitalism's death have been greatly exaggerated. But it would be fair to say that the world's prevailing economic system has suffered a pretty nasty scare, and that many have taken understandable fright.

What does it all mean for the semiconductor industry? Well, a rapid slow down in consumer spending looks inevitable, and that will of course have an impact on chip manufacturing. On the other hand, silicon and III-V devices have become such ubiquitous elements of modern life that it is difficult to imagine any real implosion of demand.

Take cellphones. Nokia measured industry unit volumes of 310 million in the third quarter of this year – up 8% from the same period in 2007.

Look at Intel's latest sales figures, which at \$10.2 billion represented a best-ever third-quarter performance. The silicon leader may not be a compound semiconductor company, but its fortunes are a clear indicator of the PC market and therefore allied to wireless LAN chipsets.

One area of genuine concern is semiconductor equipment bookings.

“It is difficult to imagine any real implosion of demand”.

At \$754 million (according to SEMI), September bookings were down nearly 40% on the previous year – painting a very gloomy picture indeed. However, the vast majority of these bookings are for silicon fabs, and the compound sphere is increasingly being eyed by

some equipment makers as an oasis in the silicon desert.

LED, GaAs and wide-bandgap technologies are seen as growth areas for traditional equipment vendors. Lithography giant ASML is shipping increasing numbers of deep-UV stepper systems to GaAs companies upgrading their processes and Ultratech expects to sell many more projection alignment steppers to LED manufacturers. EV Group has just sold its one-hundredth nanoimprint system.

There will no doubt be more doom, more gloom and unprecedented hand-wringing in the short term. Many capacity expansions and upgrades will be delayed until financial conditions improve. But innovation tends to follow on the heels of such turmoil, and, although solid-state lighting, solar cells and high-efficiency transistors are nothing new to us, they are seen as innovative in the wider world. They are also looking increasingly attractive to equipment companies seeking refuge from traditional markets.

Michael Hatcher *Editor*

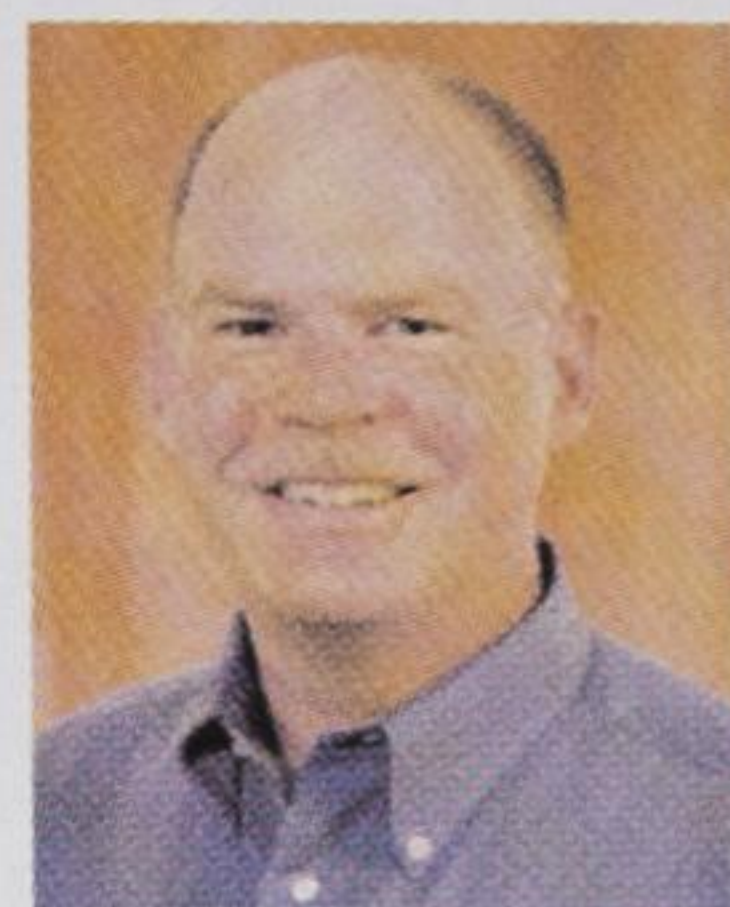
Advertisers' Index

Aixtron AG	13	PANalytical BV	OBC
AXT	4	Riber	9
Beta Squared Lithography, Inc	7	SAFC Hitech	IBC
IQE (Europe) Ltd	24	Smithers Rapra Technology Ltd	15
KLA Tencor Instruments	3	Solid State Equipment Corporation	22–23
Lake Shore Cryotronics Inc	24	Spire Semiconductor LLC	10
LayTec GmbH	24	Swiss Federal Institute of Technology	24
Oxford Instruments	11, 28	TriQuint Semiconductor	IFC
Proton Energy Systems	24		

Emerging Standardization for Sapphire Substrate Inspection

By Frank Burkeen

Senior Product Marketing Director at KLA-Tencor
Frank.Burkeen@kla-tencor.com



A growing demand for GaAs substrates and epitaxial wafers is being driven by two major device industries: (1) LED devices used in automobiles, signs, and flat-panel displays, and (2) MMIC devices for mobile electronics and Wi-Fi stations. As a result, industry experts are forecasting 16% CAGR for GaAs material by volume over the next 5 years. While volume demand for GaAs materials will continue at a healthy pace, overall demand will be counterbalanced by decreasing die sizes as GaAs device manufacturers improve fabrication processes. To date the use of automated defect inspection has been much less pervasive in compound semiconductor processing than in silicon wafer processing, however this is changing with the increasing need to increase yield and reduce costs.

With tighter design limits, substrate and epi defectivity is more critical than ever. A number of global manufacturing facilities are employing an Optical Surface Analysis (OSA) inspection technique that combines the power of scatterometry, ellipsometry, reflectometry, and topographical analysis to detect and classify defects in substrates, epi-layers, and process films. OSA technology is being used by industry leaders to monitor production lines, identify mission critical defects of interest, and create process-specific recipes to detect and classify yield killing defects while ignoring nuisance defects.

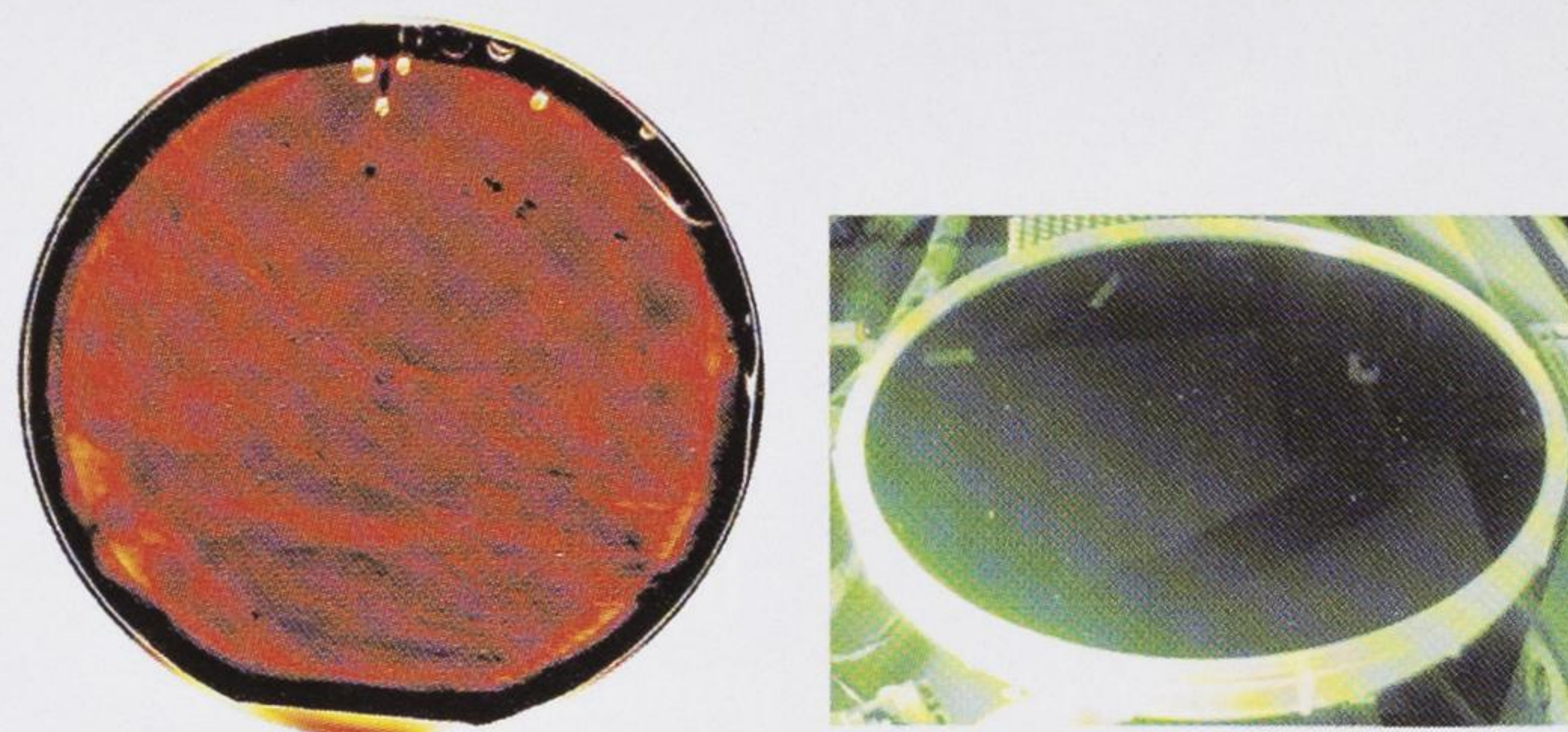


Figure 1: Candela Qphase™ image of GaAs substrate stains showing various water stains, wipe stains, edge defects and dark spots. Stains have been identified as killer defects resulting in rough epi morphology and poor epi-layer adhesion. Substrate stains cannot be seen under microscope or bright light inspection

Substrate stains on bare GaAs wafers are one such killer defect and frequently result in full wafers scraps after epi deposition. Historically GaAs substrates have been monitored with optical microscope or bright light inspection. However these inspection techniques are ineffective at detecting these killer stains and other thin film defects like some CMP residues. Many of these stains are only tens of angstroms thick and are not detectable with microscope or bright light inspection.

Figure 1 shows the OSA Qphase™ (digital image analysis application) image of GaAs substrate stains highlighting various water stains, wipe stains, edge defects and dark spots. Certain stains have been identified as killer defects resulting in rough epi morphology and poor epi-layer adhesion. Failed epi is causing full-wafer scraps throughout the supply chain creating turmoil between substrate suppliers, epi OEMs and device manufacturers as incumbents investigate whether the resultant wafer scraps are due to growth conditions or substrate quality. The Candela OSA has proven effective at root cause analysis of GaAs substrate stains and real-time defect detection and classification.

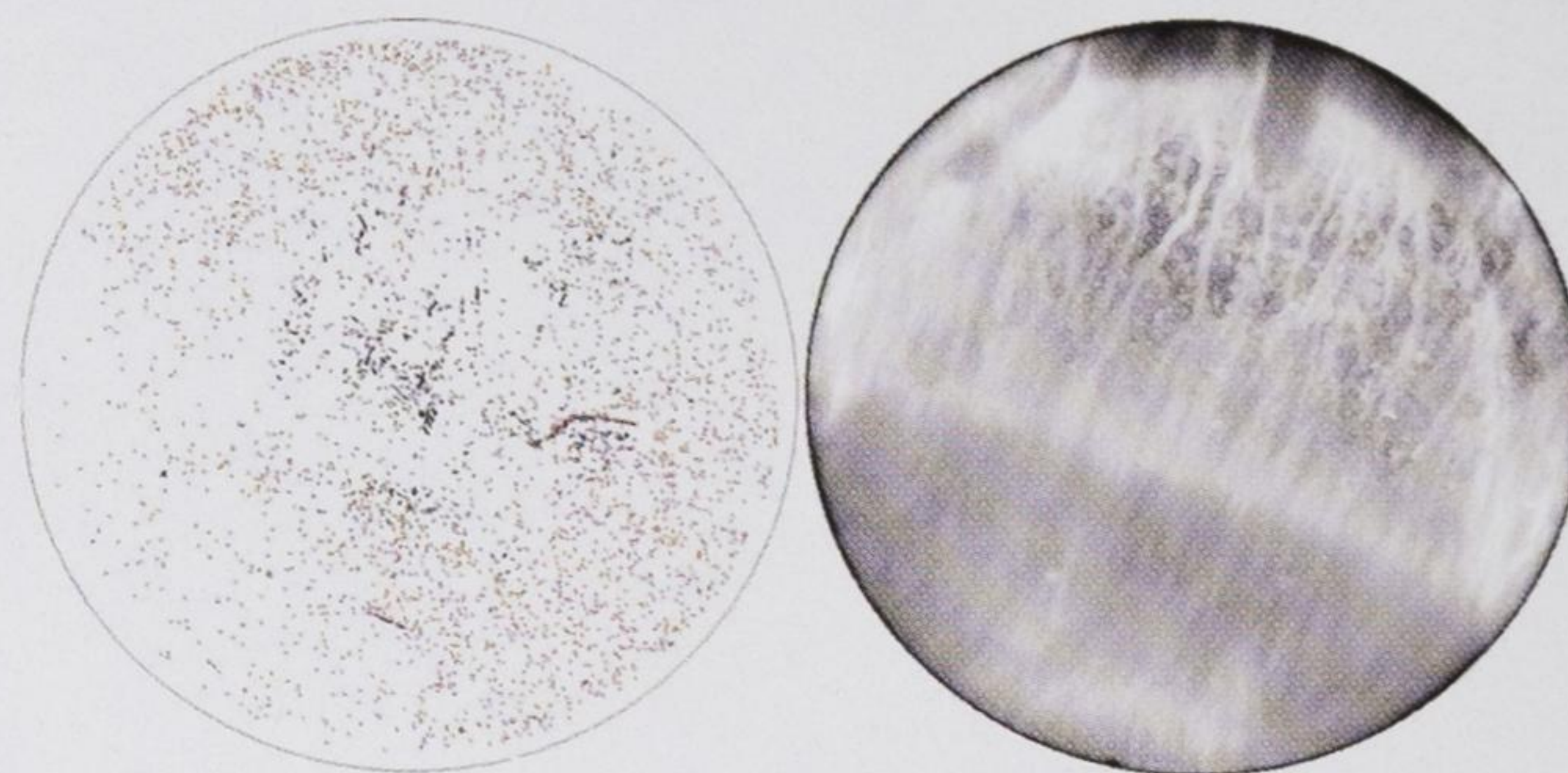


Figure 2: OSA Defect Map and Qphase™ image of same bare silicon wafer

The long-standing industry standard in the semiconductor industry has been the report of Light Point Defects (LPDs) and surface haze. LPD defect maps are commonly used for process control and tool monitoring but a growing number of manufacturers are recognizing that some killer defects do not necessarily scatter light and scatterometry alone is not enough to meet their quality control needs. Figure 2 shows an LPD defect map and OSA Qphase image of the same bare silicon wafer. The substrate stains seen in the Qphase image are not detected using scatterometry.

Optical surface analysis technology enables manufacturers and suppliers to automate defect inspection and define well-controlled process control limits. OSA technology, as found in KLA-Tencor's Candela™ CS20, can be employed at incoming substrate inspection, post-clean inspection, and after epitaxial growth and process film deposition to improve yield.

To learn more, read about the Candela CS20 at:
www.kla-tencor.com/CS20

Your premier choice for III-V and Ge substrates and related strategic raw materials.



axt

VGF

STRENGTH.

PERFORMANCE.

INNOVATION.

OUR VISION

To be the number one advanced semiconductor materials supplier of choice through superior quality, effective cost of ownership, and a customer focused philosophy.

OUR MISSION

To identify and develop growth opportunities that will ultimately result in exceeding customer's expectations, market share enhancement, sustainable profitability, and provide shareholder value.

USA Headquarters
4281 Technology Drive
Fremont, CA, USA 94538

T: 510-438-4700
F: 510-353-0668

E: sales@axt.com
W: axt.com

INDUSTRIAL STRATEGY

SEMI urges reformed European vision

The competitiveness of the European semiconductor industry has diminished in recent years and the region is running out of time to remedy the situation. That's the key conclusion of a white paper published by global industry group Semiconductor Equipment and Materials International (SEMI).

Released to coincide with October's Semicon Europa event in Stuttgart, Germany, the white paper makes six recommendations to the European Union and its individual member states; steps that SEMI believes can restore lost European prominence in the semiconductor industry.

Heinz Kundert, the president of SEMI Europe, said: "It is vital [to] take immediate action to reinforce and revitalize our local industry, to ensure future competitiveness and viability. [We] need a concerted vision from the industry, the EU and national governments to keep state-of-the-art manufacturing in Europe going."

Although SEMI's paper is primarily concerned with the silicon industry, that vision would also encompass key compound semiconductor technologies, such as LEDs, high-efficiency solar cells and low-loss switches based on materials such as GaN and SiC, all of which could play important roles in tackling problems like energy shortages and climate change.

The white paper states that, with the semiconductor industry on the cusp of a new growth era, Europe is in a position to become a global leader – if the right decisions are made. Keeping a strong supply base of semiconductor manufacturing, as well as equipment and materials, is essential, says SEMI.

The trouble is that Europe has been losing ground on its global competitors. Behind Japan and the US for decades, Europe's semiconductor production capacity was estimated at just 12% of the world's total in 2005.

A couple of years later and that proportion is believed to have dipped below 10%.

Other global regions have launched local semiconductor expertise by creating federal or state-funded science parks and industry clusters. Europe has lagged behind though and SEMI says that the EU's "political vision, policy and economic instruments" in place to support the semiconductor industry have been lacking.

As well as calling for additional research funding, the development of public-private R&D partnerships and tax breaks for semiconductor companies, SEMI wants to see faster decisions over research funding and more intercontinental collaboration between Europe, the US and Asia.

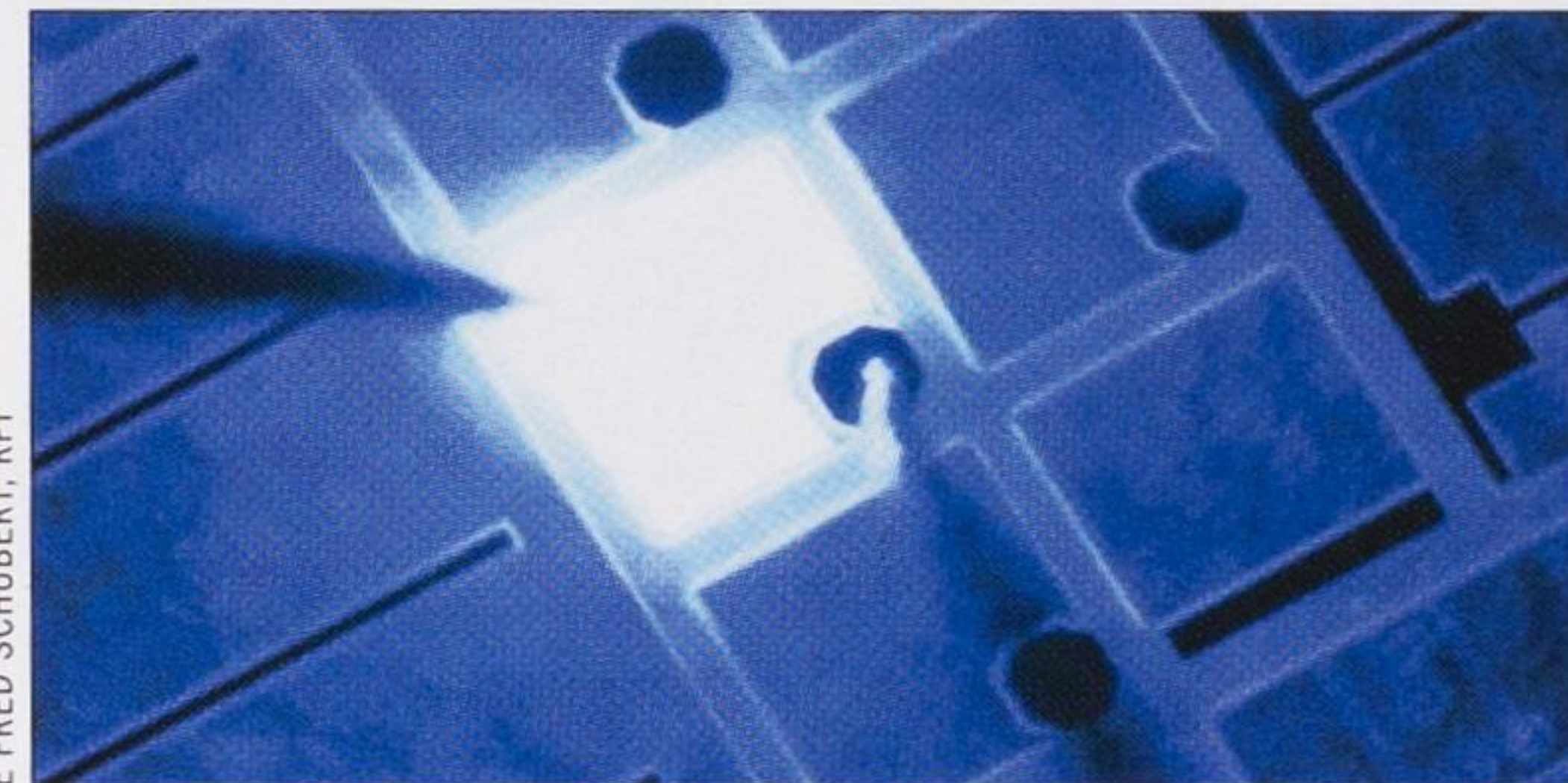
Rather more drastic, and perhaps beyond the powers of even the EU, is SEMI's request that the dollar/euro exchange rate be tipped in favor of the dollar, to help European exporters to become more competitive.

LIGHT-EMITTING DIODES

RPI gets \$18.5 m for smart LED lighting

The US National Science Foundation (NSF) has granted Rensselaer Polytechnic Institute (RPI) \$18.5 million to lead a center intended to revolutionize LED use. The money will establish the NSF's Smart Lighting engineering research center, which RPI expects to receive up to \$50 million over 10 years.

Of NSF's five-year grant, \$3.25 million is committed to the first 12 months at the center, which started in September and is headed by E Fred Schubert. Other contributions to the first year include \$1 million



The Smart Lighting engineering research center will investigate materials, devices and systems, led by solid-state lighting expert E Fred Schubert.

from the 18 industrial partners, \$700,000 from New York and \$500,000 from RPI.

The industrial partnership agreements are still being finalized and therefore the

individual companies have not been named. However, Schubert told *Compound Semiconductor* that they include LED chip makers, material providers, lighting companies and device manufacturers.

The center will boast around 5000 m² of laboratory space, half of which is currently equipped, with apparatus yet to be installed in the other half. Beyond this, the funding will mainly be spent on research students.

Schubert says that research will be split between materials, device technology and systems applications. "With Smart Lighting we have absolute control over every aspect of the light," he added. "We can custom tailor a light source for nearly any imaginable scientific or commercial application."

PHOTOVOLTAICS

SolFocus calls for more solar-cell producers

SolFocus has invited more of the compound semiconductor community to join it in the solar market, saying that it's open to approaches from additional cell makers.

The Californian photovoltaic system producer has recently achieved recognition as a serious solar technology, in qualifying for incentives in its home state. "A lot of projects are depending on the rebates for their

return on investment," marketing vice-president Nancy Hartsoch said.

Hartsoch says that the California Solar Initiative accreditation has now opened doors across the US and Europe. "California's important because it leads the US in standards and metrics," she explained. "It's a credibility validation." She believes that this is an important step in SolFocus' plan to lower the cost of electricity produced by its systems to grid parity by 2012–2015.

However, the company is concerned that current industry players will not provide a sufficiently large supply chain to meet the

demand that this will create. Here is where companies that make the GaAs-based cells at the heart of the CPV systems, like Emcore, Spectrolab and their newer competitors, come in.

"The real key concern is having enough successful companies to build an industry," Hartsoch said. "Having one or two suppliers who are just dynamite, that's not as good for the industry as having five or 10. We work closely with a lot of the start-up compound semiconductor guys because we want to help them to be successful if they've got advanced technology ideas."

WIDE-BANDGAP TRANSISTORS

Fujitsu makes first 100 W normally off GaN HEMT

Japanese wide-bandgap pioneer Fujitsu has opened the way for the first 100 W-plus III-V enhancement-mode transistor in the market, targeting microwave and millimeter-wave base stations.

Fujitsu unveiled the HEMT, slated for use in high-capacity wireless communication by 2010, at the International Symposium on Compound Semiconductors in Rust, Germany, on September 23. Toshihiro Ohki of Fujitsu Laboratories introduced the normally off device, which boasts 126 W power output and a 336 V breakdown voltage.

“Our new technology enables us to use the GaN HEMT in enhancement-mode without using special growth and process techniques,” said Toshihide Kikkawa, research fellow in Fujitsu’s advanced device laboratory. “Reliability can easily be obtained,” he

told *Compound Semiconductor*.

With the conglomerate’s first GaN HEMTs finding their way into base stations this year, Ohki and Kikkawa’s team was able to boost these devices’ power to target millimeter-wave operation. To do this, they introduced an AlN layer into their MOCVD-grown transistor’s cap structure and modified its gate design.

The piezoelectric properties of AlN mean that it induces positive charge at the interface with an n-type GaN layer beneath it, helping to boost power output. “This positive charge produces additional carriers in the channel layer,” Kikkawa said. “As a result, two-dimensional electron gas density is increased.”

AlN can’t be left as the top layer in the cap structure, because its rough surface

lowers the transistor’s breakdown voltage. The final cap structure is therefore a single n-type AlN layer between two n-type GaN layers. The results presented in Rust show that this three-layer cap boosts the volume of electrons transmitted through the device by 60%. The final HEMT also avoids the negative voltage that is needed to turn off other devices, instead boasting a 0.25 V positive threshold voltage.

High power and normally off characteristics make the transistor ideal for energy efficient and economical high-data-rate communications in gigahertz frequencies and even beyond, Fujitsu says. It sees great potential in millimeter-wave communications thanks to good directionality, fast data transfer and the extensive bandwidth that is currently unused in this range.

MATERIALS

Mystery buyer saves SiC-maker Caracal

An unidentified multinational consortium has rescued SiC epiwafer and substrate supplier Caracal Inc from bankruptcy proceedings.

On August 8, the consortium bought out the Ford City, PA, company, which claims to have remained intact since filing for bankruptcy protection in April. Caracal says that the consortium “traditionally has a long-term perspective on all of its investments.”

In response, a spokesman for the consortium commented: “We are very excited about the acquisition of the Caracal assets. We have kept an eye on the wide-bandgap



Caracal's prize-winning on-axis epitaxial 4H-SiC.
The lines demarcate coalescing SiC islands.

semiconductor market and see potential for strong growth year on year.”

Meanwhile, Caracal continues to garner acclaim, having most recently won a prize for research presented at the European

Conference on Silicon Carbide and Related Materials in Barcelona in September.

The company’s chlorosilane-based SiC growth method allows rapid production of thick, high-quality material. “We continue to develop this process,” said Stefano Leone, Caracal’s chief epitaxial-growth scientist. “Today we can also grow very high quality films on on-axis wafers, which eliminates the problem of basal-plane dislocations that harm SiC bipolar devices.”

Leone earned the accolade by producing 100 μm thick epilayers grown on on-axis 4H-SiC at 25 $\mu\text{m}/\text{h}$, in conjunction with Linköping University. His work showed that the addition of chlorine to standard precursors is a key parameter for growing thick homoepitaxial layers on 4H-SiC silicon-face on-axis substrates.

DEFENSE

Record-power SiC devices enhance radar

Microsemi has used SiC to produce what it claims are the most powerful radio-frequency transistors yet made for VHF and UHF radar applications.

The two kilowatt-scale static-induction transistors (SITs) launched on October 6 are already in pilot production.

“The critical electric field of SiC is an order of magnitude higher than silicon,” pointed out Mike Mallinger, Microsemi’s director of business development for wide-

bandgap products. “That means I can operate the transistor at much higher bias voltages. We can create a transistor approximately the same size with a much higher power level that then adds to the capability of the overall system,” he said.

The company’s Bend, OR, fab makes millimeter-dimension chips based on outsourced 3 inch SiC epiwafers prior to back-end processing at its Santa Clara, CA, site. Connecting the transistors in parallel, rather than producing larger chips that are more likely to contain device-killing SiC material defects, enables high-power operation.

The device that targets VHF radio wavelengths at 150–160 MHz typically produces

1400 W signals, while the 406–450 MHz UHF transistor can reach 1100 W. They provide 9 and 8 dB of gain, respectively.

Demands for increased radar range and identification capability increase performance needed from the radar semiconductor components. Increased signal pulse length means that the transistors heat up more, while shorter periods between pulses give them less opportunity to cool.

Here, the high-temperature operating capability and three-fold thermal conductivity improvement that SiC offers over silicon come into play. Microsemi has shown that its components can operate at 300°C, compared with 150°C for its silicon transistors.

GROWTH EQUIPMENT

Riber buys OIPT's MBE group

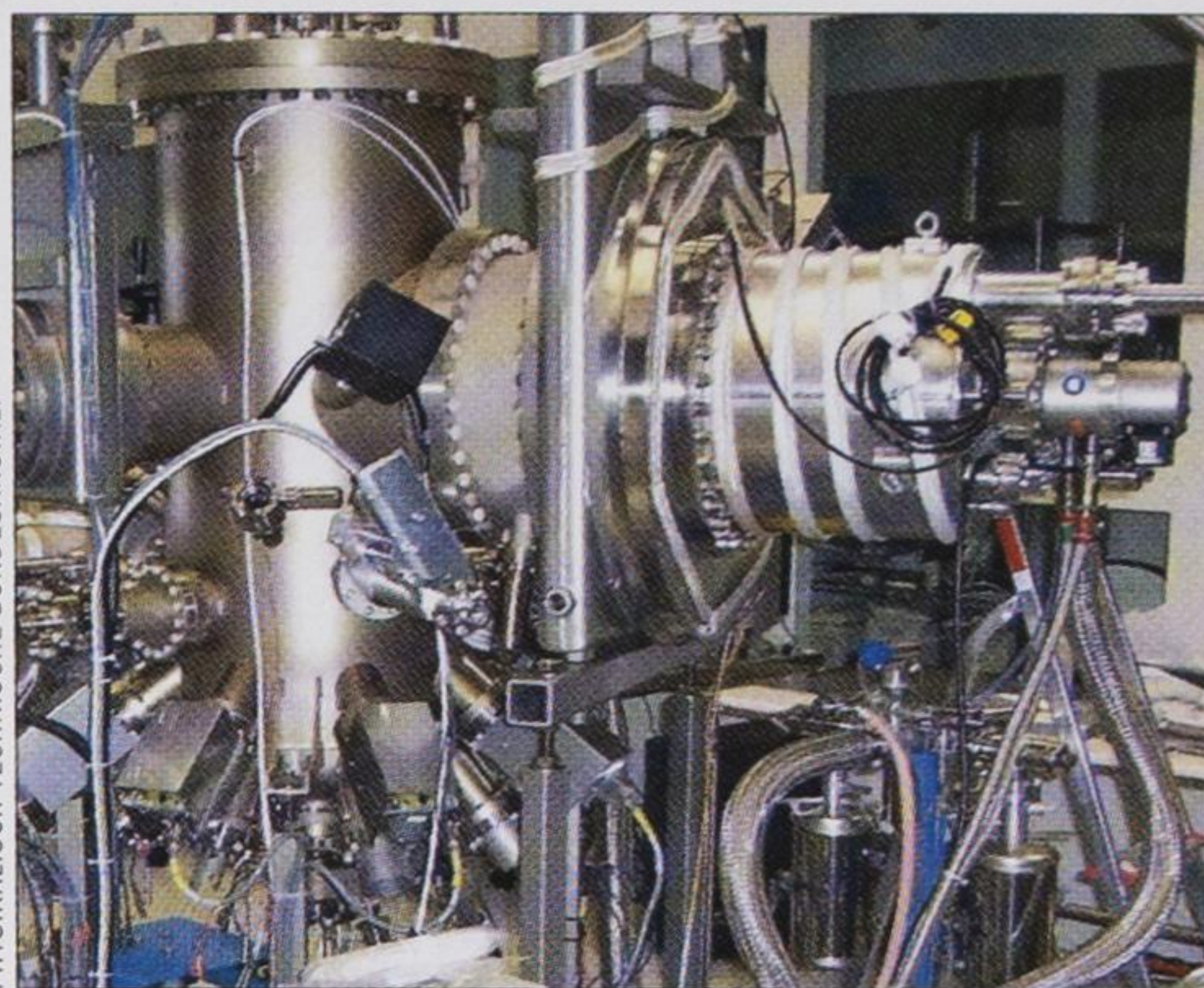
French molecular-beam epitaxy equipment supplier Riber has strengthened its market position by purchasing Oxford Instruments Plasma Technology's (OIPT's) competing tool business.

The deal immediately transferred the rights to OIPT's technology and after-sales business when it was signed on September 22. No employees will be exchanged, nor will OIPT make any redundancies following the deal, although some hardware will move between the companies.

Riber has paid an initial €450,000 (\$665,000) and follow-on payments of €400,000 are due to the UK company based on future spares sales. Riber principally intends to use the deal to develop its equipment support revenues. "This will strengthen Riber's after-sales business, which has increased by 35% in 2008," the company said in a statement.

There are currently in the region of 300 OIPT reactors in use around the world, and these will now grow Riber's total installed base to 800. OIPT says that in recent years the turnover of the MBE division has averaged €1.2 million. Jean-Pierre Regner, president of Riber's executive board, told *Compound Semiconductor* that this revenue now comes exclusively from spares and support. "There have been no sales of this equipment over the last year."

The MBE reactors that Riber offers are sufficiently advanced to mean that it doesn't need the designs that are sold by OIPT to broaden its offering, Regner says.



Riber is looking to increase the revenues that it earns from supporting MBE machines, like this Riber Compact 21 in use at the German national metrology institute, Physikalisch-Technische Bundesanstalt.

"We will not promote this equipment, but we will be open if people want to make a special deal," he explained.

Riber's system-support business has recently benefited from organic growth and its acquisition of component supplier Addon. In contrast, an MBE business relying on supporting already-installed reactors had looked increasingly out of place as Oxford Instruments focused on faster-growing sectors like LED manufacturing.

OIPT's MBE technology stemmed from its buy-out of Thermo VG Semicon in 2003. Prior to the Riber deal, OIPT still offered the V100 system, which VG Semicon then claimed was the most widely used MBE system for GaAs mass production.



From our newsfeed...

visit compoundsemiconductor.net for daily news updates

...Nitronex turns up power on HEMTs

Nitronex – the Durham, NC, GaN-on-silicon manufacturer – has shown that its technology can deliver 28 dBm output in the 5.8 GHz Wimax band and 27 dBm output in the 5.2 GHz Wimax band.

...Handsets galore for GaAs firms

The key US cellphone power-amplifier makers have been busy trailing what their peak December quarters will have in store this year. South Korea is a big focus, with Greensboro, NC's, RFMD claiming "more than 10" design wins with Samsung, while Warren, NJ's, Anadigics will be appearing in LG Electronics'

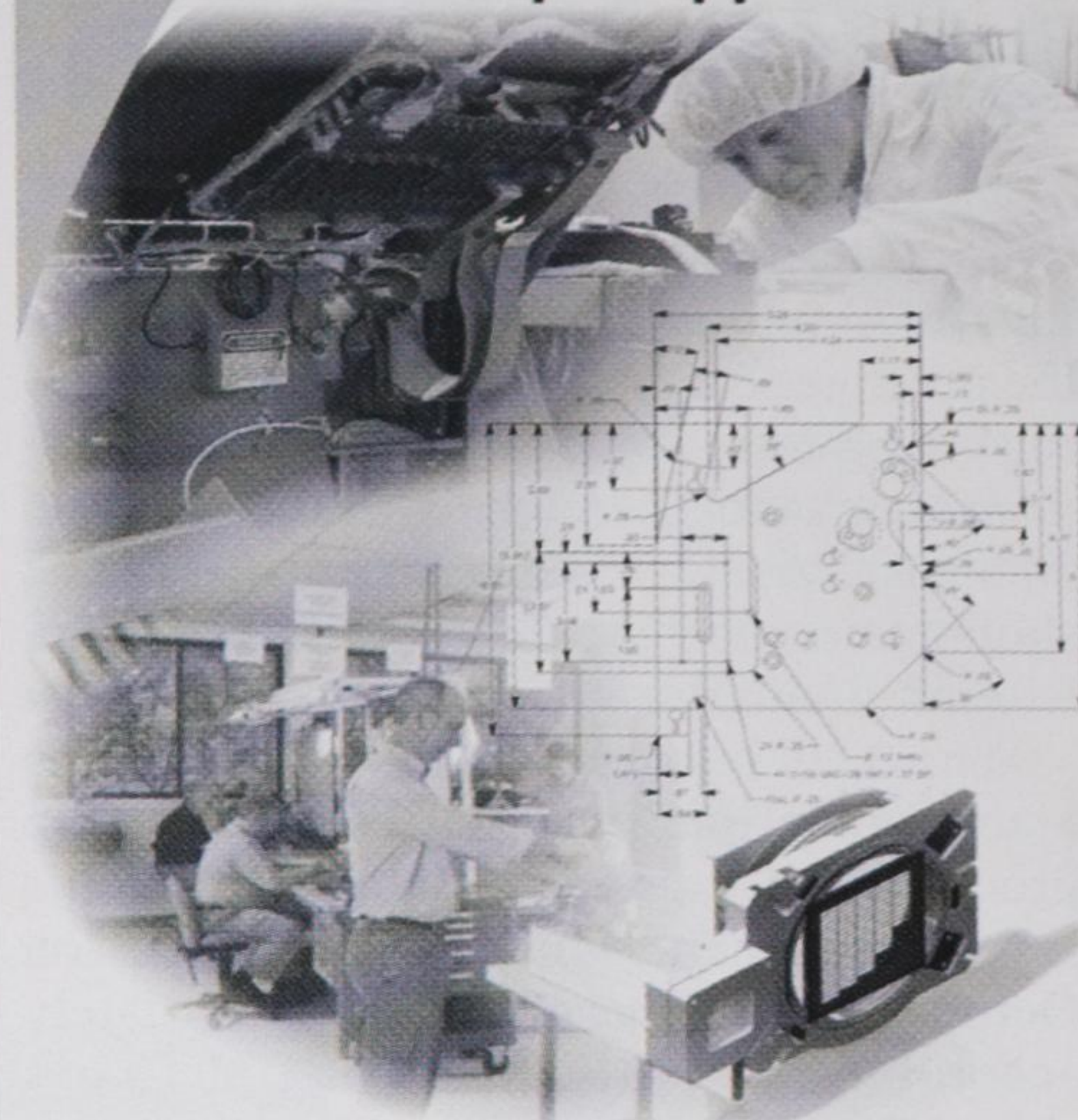
latest touch-screen handset – the Vu. Meanwhile, Woburn, MA, based Skyworks Solutions says that it has sold 40 million power amplifiers into smartphones in 2008, which is double its 2007 volume.

...TriQuint wins \$4.5 m US Navy contract

The US Office of Naval Research has awarded TriQuint a 21-month, \$4.5 million contract to advance manufacturing methods used to produce high-power, high-frequency GaAs amplifiers. The program aims to extend the Hillsboro, OR, company's high-voltage PHEMT technology to higher frequencies than its previous X- and S-band processes.

Your Lithography Solution

For Your Unique Application



Beta Squared Lithography Inc. has redesigned the Micralign™ today for tomorrow's compound semiconductor requirements, incorporating BSL's trademark reliability and performance upgrades. We currently have systems throughout the world that are processing these substrates/applications:

- Gallium Arsenide (GaAs)
- Silicon Carbide (SiC)
- Sapphire (Al₂O₃)
- Cadmium Zinc Tellurium (CdZnTe)
- Cadmium Mercury Tellurium (CdHgTe)
- Germanium (Ge)
- Quartz (SiO₂)
- Pyrex
- Solar/HD Heads/Ink Jets
- Gyros/Accelerometers

To find out more information or to purchase a refurbished Micralign™ for your compound semiconductor requirements, email us at: sales@beta2L.com



**Beta Squared
Lithography Inc.**

940 Federal Road, Brookfield, CT 06804
Phone: 203.775.4242 Fax: 203.775.1337
www.betaSquaredLithography.com

ILLUMINATION

Cree lands milestone European deal

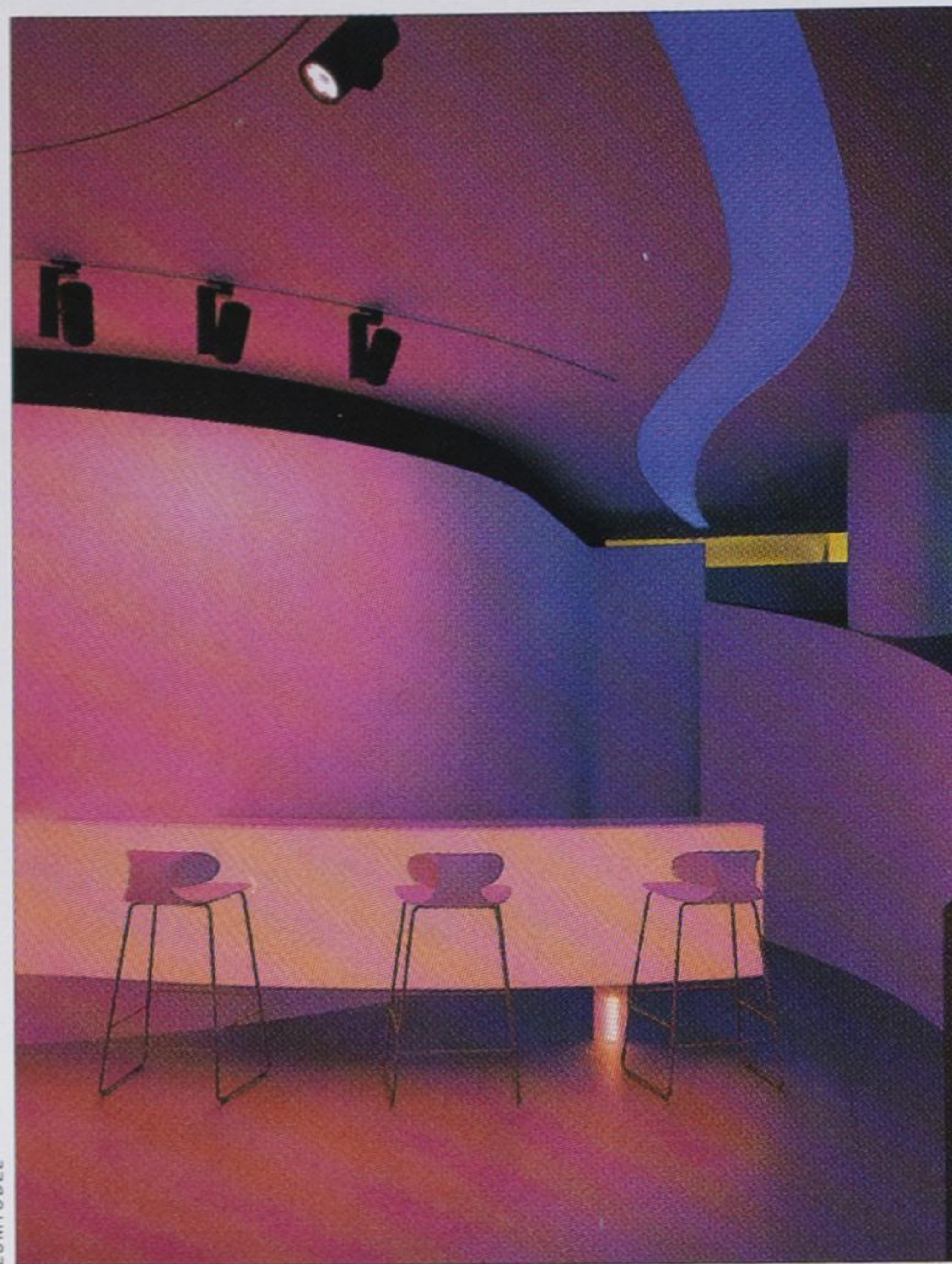
Leading lighting firm Zumtobel has raised the prestige of Cree's LR6 fixtures, by signing a long-term strategic deal as their European distributor. Zumtobel, which was voted Austria's most valuable brand for 2007, should account for sales of at least 50,000 LR6 luminaires in the deal's first year.

With 12 XLamp LEDs in each LR6, this marks an early acceleration of Cree's chip production for general illumination. The supply agreement, which was announced on October 8, become effective immediately according to Ty Mitchell, head of Cree's chips and materials division, meaning that the production ramp is now in motion.

"Although it has a relatively small impact given our overall chip volume, this deal demonstrates the growing adoption of solid-state lighting," Mitchell told *Compound Semiconductor*. Cree expects the exclusive agreement to distribute its recessed downlights in more than 40 countries to expand into 2009.

Architects around Europe collaborate with Zumtobel on lighting installations and concepts, including a prestigious collaboration on a new terminal at Vienna airport. A spokesperson for Zumtobel said that it is in the process of introducing a fixture design that combines an LED downlight with a more conventional uplight. He could not yet confirm whether the LR6 is the downlight in this product.

This is one illustration of advances in



Zumtobel's Tempura fixtures have been made with LED modules from Philips Solid State Lighting. Now Cree is supplying the Austrian firm with luminaires, plus LEDs for it to develop its own products with.

LED illumination that investment analyst Oppenheimer and Co says will help Cree to strengthen its sales growth in an economically difficult 2009. Yair Reiner's rating upgrade anticipates that the Durham, NC, chip maker's share price will grow faster

than the S&P 500 index over the next 12–18 months. Reiner says that the use of LED lighting in general illumination is "not just a PowerPoint slide anymore".

"On the demand side, higher energy costs and increased concern about greenhouse gases are driving countries, businesses and consumers to search for alternatives to traditional lighting solutions," he wrote. "On the supply side, an LED ecosystem of luminaire makers, contractors and distributors has begun to coalesce and offer products that look and work better, and cost less."

Cree's LR4 fixture won the US Lighting for Tomorrow prize for downlighting, announced on September 16. The 72 lm/W efficacy of its LR24 architectural light also gained the company an additional honorable mention, combining with the LR4 and LR6 to underline Cree's status in this sector.

Over the last year, Reiner says that Cree's declining sales of LEDs for handset backlighting has masked success in other areas. "With Cree now largely weaned off its exposure to handsets, the underlying growth momentum should become more apparent."

Backlighting for TVs and notebook computers, credited with driving growth for other LED makers, is not currently an important application for Cree, Reiner says. "Though a purported joint venture with LG Display leaves a significant window of opportunity open, our positive thesis on Cree does not hinge on backlighting."

M-PLANE GaN

Mitsubishi expands non-polar substrates

Mitsubishi Chemical Corporation is aiming to extend its lead in the non-polar GaN field with 2 inch substrates by 2010, according to the company's Toshinari Fujimori.

Fujimori, speaking in Montreux, Switzerland, on October 6, revealed that Mitsubishi has already produced 12×20 mm non-polar GaN substrates in the lab. He told the audience gathered at the International Workshop for Nitride Semiconductors meeting that 18×18 mm pieces are set to follow in the near future.

Non-polar substrates enable the growth of high-quality lasers and LEDs that are free from strong internal electric fields.

These fields are an obstacle to the develop-

ment of conventional green lasers. Fujimori is optimistic that growth on non-polar GaN will lead to the fabrication of the first GaN-based green laser diodes.

Mitsubishi constructed the HVPE reactor from which it produces bulk GaN itself, and makes non-polar substrates by vertically slicing the boules made by the tool.

Fujimori says that clogging of the reactor's exhaust line is one of the problems that the researchers have had to overcome, alongside the need to eliminate pits and a rough surface through optimization of the growth conditions. He presented studies on a 52 mm diameter, 5.8 mm thick free-standing boule to demonstrate the present status of Mitsubishi's technique.

Cathodoluminescence measurements on horizontal slices from this boule revealed that the dislocation density is highest next to the interface with the HVPE growth sub-

strate. The slice nearest to this interface had a dislocation density of $5 \times 10^6 \text{ cm}^{-2}$, compared with $1 \times 10^6 \text{ cm}^{-2}$ for the slice nearest to the boule's top surface.

Secondary ion mass spectrometry measurements showed very low levels of impurities other than silicon, which was present at a concentration of $1.5 \times 10^{17} \text{ cm}^{-3}$.

Fujimori revealed that Mitsubishi has also been developing a "chemical equilibrium reaction" for GaN boule growth, which promises to slash the cost of non-polar GaN substrates.

While Kyma Technologies and Mitsubishi Chemical are still the leading vendors of m-plane GaN, as of May 1 a European project called PolarCoN has been seeking to join them. This €2 million (\$3.16 million) academic effort is also targeting 2 inch substrates and is being guided by Osram Opto Semiconductors.

CHIP DEVELOPMENT

Toshiba hones UV die for improved RGB LEDs

Toshiba claims to have produced the most efficient sapphire-substrate UV-LED chips, in support of an unconventional approach to replacing incandescent lamps.

In an *Applied Physics Express* paper published online on September 26, the Japanese conglomerate described flip-chip 383 nm LEDs with an external quantum efficiency of 36%. The output power under 20 mA, 3.5 V operation was 23 mW, and the Toshiba team estimated that internal quantum efficiency (IQE) could be as high as 72%.

"To the best of our knowledge this is the highest [IQE] reported for UV LEDs formed on sapphire substrates," wrote Yasuo Ohba and his colleagues. "These values are thought to be comparable to those for visible LEDs, considering no special techniques such as surface patterning are used to enhance light extraction."

The team used a high-temperature MOCVD-grown AlN buffer on the sapphire substrate to lay the foundations for high-quality GaN growth. AlN-buffer test wafers were made using conditions similar to those that Toshiba used for blue-violet laser diodes, but changing the growth temperature for depositing the active layer.

Photoluminescence studies on wafers produced using Ohba's technique suggested that LEDs with peak emission wavelengths above 380 nm would be free from significant non-radiative recombination caused by threading dislocations. As a result, the team expected high quantum efficiencies for those chips in comparison with standard LED structures, where efficiency decreases drastically below 400 nm.

Ohba showed this to be the case by producing final $400 \times 400 \mu\text{m}$ LED devices using a flip-chip approach and testing their electroluminescent performance. The measured output power of the 383 nm LEDs increased linearly with current, reaching 68 mW at 60 mA.

UV LEDs are important to Toshiba for exploiting europium-based phosphors that convert UV light to a red emission for red-green-blue illumination. Ohba says that this phosphor is "a key material for realizing high luminous efficacy and color rendering."

However, the europium phosphor is not well matched to visible-wavelength LEDs. To enable its use, according to the Toshiba team: "development of UV LEDs is very important for realizing white LEDs of low color-temperature warm light to replace conventional incandescent lamps."



From our newsfeed...

visit compoundsemiconductor.net for daily news updates

...Nichia suffers patent invalidation

LED company Seoul Semiconductor is celebrating after the Korean Intellectual Property Tribunal ruled that a patent that its Japanese rival Nichia was trying to enforce was invalid. Nichia had claimed that Seoul Semiconductor's Z-Power P9 white-LED products infringed its Korean patent no. 491482. Nichia told *Compound Semiconductor* that it is appealing the decision because it "regrets the outcome and

firmly believes that the validity of the patent will be recognized by the Patent Court."

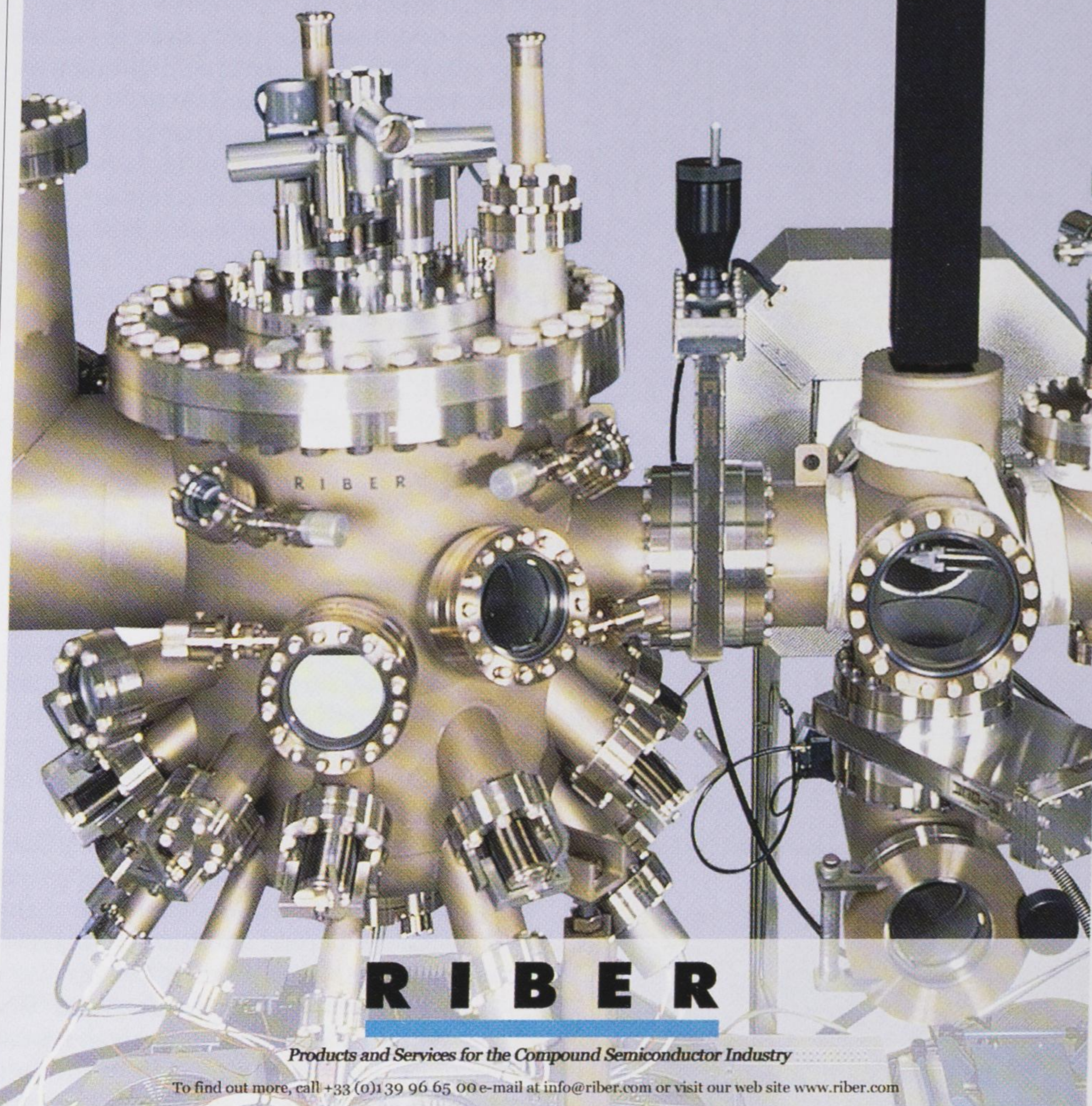
...Dell commits to LED backlights

The US-based PC maker says that two-thirds of its Latitude E-Family laptops will use LED backlighting as of December 15. By the end of 2009 80% of all laptops will be LED backlit, with 100% conversion slated for 2010. This will yield an estimated energy saving of 22 million kWh in 2010 and 2011 combined.

Compact 21 System

Versatile MBE

Twelve source ports / Modular and expandable
Suitable for III-V's, II-VT's, MCT, oxides, spintronics, etc.
Very high performance
Small footprint / Low cost of operation



RIBER

Products and Services for the Compound Semiconductor Industry

To find out more, call +33 (0)139 96 65 00 e-mail at info@riber.com or visit our web site www.riber.com

8 Reasons to Work with Spire Semiconductor to Develop Your Next Optoelectronics Product...



- 1** Spire Semiconductor is a **complete compound semiconductor fabrication facility** dedicated to supporting its customers.
- 2** Spire Semiconductor has its own **MOCVD III-V and II-VI multi-wafer, multi-reactor** capabilities for high volume production requirements.
- 3** Spire Semiconductor has a **first-class compound semiconductor device fabrication facility** with class 100 cleanrooms.
- 4** Spire Semiconductor's engineering staff has **extensive experience** in material and device design, process development and testing.
- 5** **You can work directly** with Spire Semiconductor's engineers.
- 6** Spire Semiconductor can **manufacture your products** in volume exclusively for you.
- 7** As a pure play foundry, we do not compete with our customers.
- 8** Working with Spire Semiconductor will **keep you ahead of your competition.**

Edward D. Gagnon
General Manager,
Spire Semiconductor



Spire Semiconductor, LLC
25 Sagamore Park Road, Hudson, NH 03051
T 603.595.8900 F 603.595.0975
sales@spiresemi.com

III-V CELLS

European record cell targets CPV

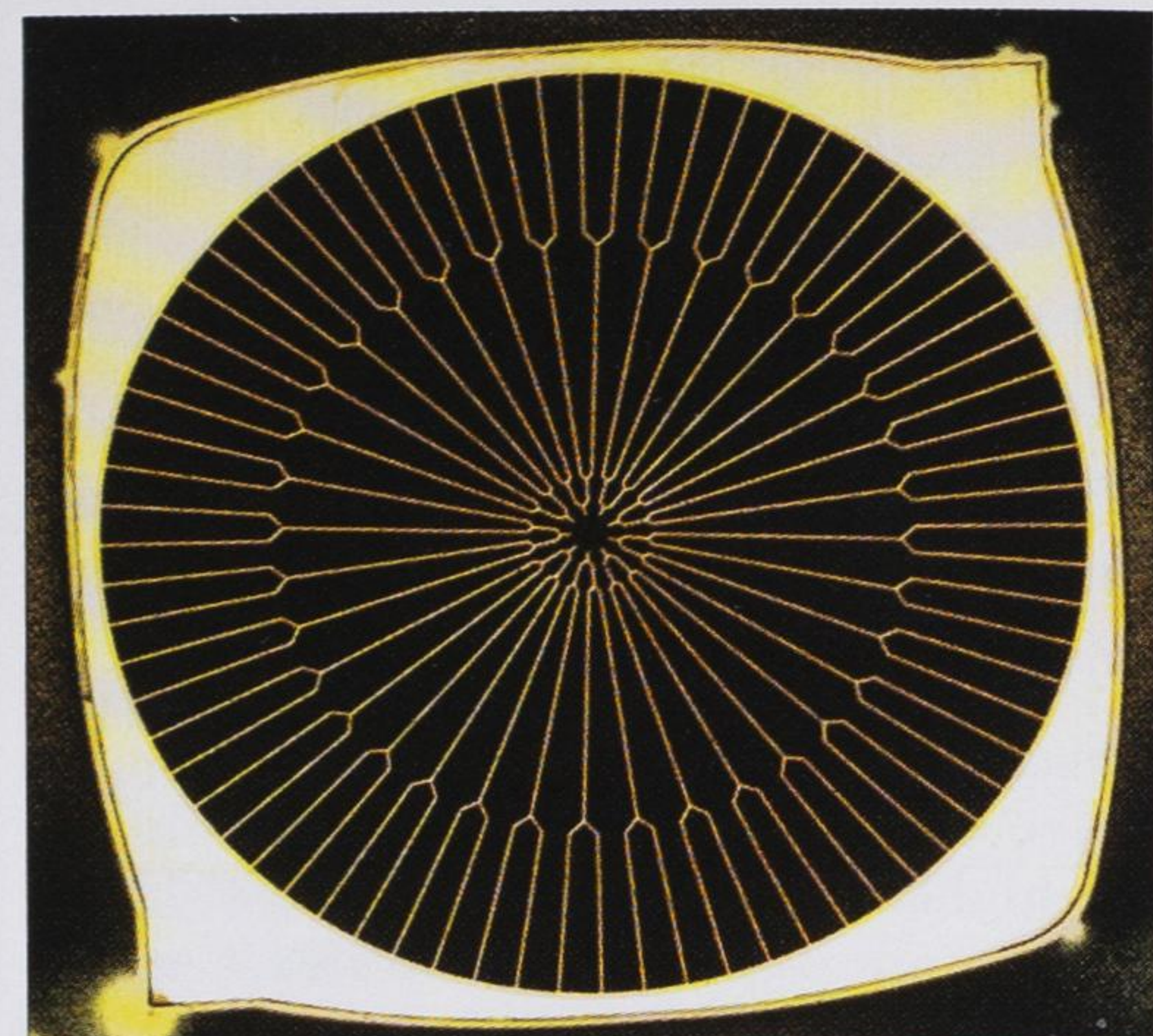
A German group has set the European benchmark for solar-cell conversion efficiency for the second time this year, and is rapidly closing on the world photovoltaic record held by the US National Renewable Energy Laboratory (NREL).

Fraunhofer Institute for Solar Energy Systems (ISE) has delivered 39.7% efficiency, using the same metamorphic $\text{Ga}_{0.35}\text{In}_{0.65}\text{P}/\text{Ga}_{0.83}\text{In}_{0.17}\text{As}/\text{Ge}$ epitaxial cell structure that it announced had reached 37.6% in July.

"We changed the layout of the metal contact," Frank Dimroth, head of Fraunhofer ISE's III-V epitaxy and solar-cell group, told *Compound Semiconductor*. "If you have less metallization area on the surface you get more light into your solar cell. You can convert more of that light to current and that gives you high efficiency in the end."

Fraunhofer ISE's designers couldn't just narrow the gold contacts down to ever-finer filaments though. They must remain large enough to carry the current produced with low resistance.

The redesigned cell now performs optimally when lenses concentrate light on it at 300 times the sun's standard intensity, compared with 1700 suns for Fraunhofer ISE's previous record. Higher concentrations mean a greater total area of incoming sun-



By redesigning its metamorphic III-V cell's gold contacts, Fraunhofer ISE has added more than 2% to its European energy-conversion efficiency record.

light is redirected by lenses onto each cell, and the resulting modules can use fewer expensive compound semiconductor cells.

However, existing commercial concentrator photovoltaic systems use 300–600 sun concentrations, and Dimroth says that theoretical maximum efficiencies lay around the 300 sun mark. The NREL overall 40.8% solar-conversion efficiency record was set at 326 suns.

WIDE-BANDGAP OPTOELECTRONICS

BN doping heralds transparent solar cells

Japanese researchers have invented a doping technique that could bring BN into use as a III-V wide-bandgap semiconductor, and have used it to make a solar cell.

The National Institute for Materials Science (NIMS) team used plasma-enhanced CVD to produce high-density polycrystalline BN and simultaneously performed laser-induced silicon doping. Previously, few doping techniques have been successful, meaning that BN remains neglected as a semiconductor.

Shojiro Komatsu, leader of the NIMS wide-bandgap semiconductor group, told *Compound Semiconductor* about the technique shortly before submitting a paper detailing it to *Applied Physics Letters*.

"The semiconducting dense-phase BN prepared here is now one of the most robust semiconductors in the world – a unique refractory and visibly transparent semicon-

ductor," Komatsu said.

To demonstrate its capability as a semiconductor, Komatsu's team made a BN/silicon heterodiode solar cell by depositing BN on a silicon substrate. This prototype operated with 2% conversion efficiency, with an effective bandgap of 5.5 eV.

The combined laser mixing/PECVD method yields the cell in just one step, producing a diamond-like p-type BN layer containing silicon atoms, which come from the substrate. In the process, the plasma supplies precursor radicals to the growing film, where a UV laser catalyses photochemical reactions that trigger deposition.

NIMS is now commercializing this technology with unnamed partners, and also plans to make n-type BN in order to produce homodiode, transparent solar cells. It hopes that these could turn anything from sunglasses to windows into opportunities for generating power.

"The physics behind the laser mixing/PECVD method is important," said Komatsu. "The wider use of BN will be in our hands soon."

BLUE LASERS

Sanyo diode raises Blu-ray stakes

Sanyo has sent a warning to Blu-ray recorder producers by developing the world's highest-output 405 nm blue-violet laser diode. The pulsed-operation 450 mW GaN laser unveiled on October 3 could allow the Japanese technology corporation to make a big impact on the Blu-ray recorder market.

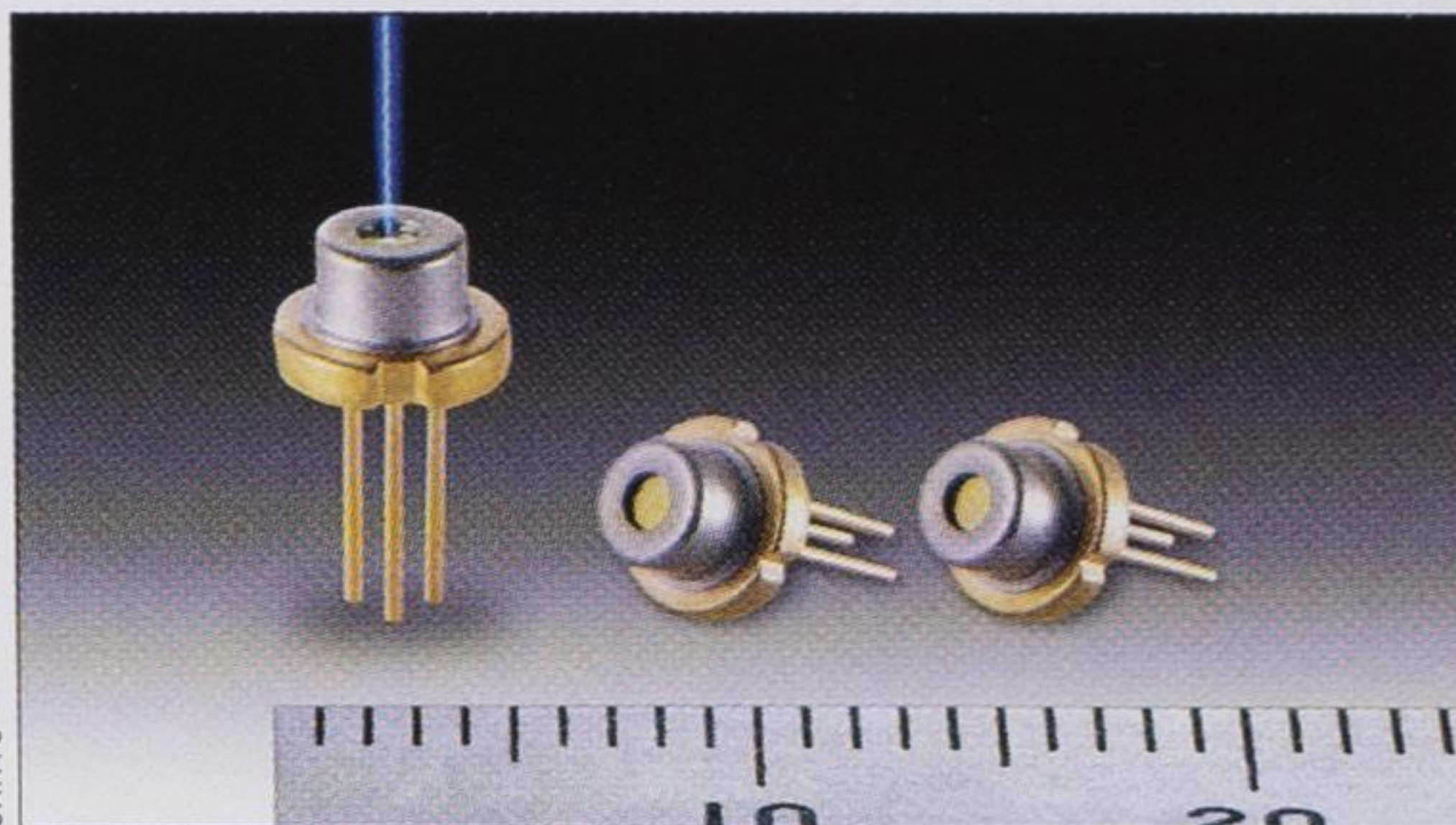
The device's current threshold is 50 mA and at 200 mW the operating current is 200 mA. When used with four-layer Blu-ray discs the 450 mW device enables 12x recording. However, the diode's record power output falls to 200 mW under continuous operation.

Sanyo has boosted power in part by using simulations to help ensure the laser-beam position is stable in the diode's optical waveguide. High-precision dry etching helps to accurately produce the simulated design, providing a more stable optical output.

It also says that it has grown high crystal quality optical cladding layers, reducing the extent of optical loss. A protective membrane also coats the edges of the laser and helps to boost long-term reliability.

According to the market report *World-wide DVD and Blu-ray Market* from analyst firm In-Stat, consumers in Japan have particularly bought into Blu-ray recorders, where higher-power diodes are crucial. Recorders already represent one-third of the 5 million unit Blu-ray player market that In-Stat predicts for 2008.

In-Stat's principal analyst Michelle



With 450 mW pulsed-operation GaN diodes, Sanyo has staked a surprising claim on the Blu-ray recording-speed benchmark with 12x standard rates.

Abraham says that this overall figure will represent year-on-year unit growth of 150%. She says that the industry will ship 12 million players and recorders in 2009, with sales led by the likes of Sony and Samsung. Sony expects to sell a staggering ¥1 trillion (\$9.6 billion) worth of Blu-ray-related products in total during that time. Manufacturers in Taiwan and China are also expected to launch Blu-ray products soon.

Sharp reportedly now dominates the recorder market, thanks to a diode that it announced in April. At 250 mW the GaN diode is currently the highest-power offering on the market.

Together with Sony and Nichia, Sharp is now a dominant player in the supply of the laser chips. For these companies, it appears that initially poor manufacturing yields are no longer restricting diode supply.

FIBER-OPTIC COMPONENTS

3S Photonics unfazed by Avanex tunable woes

3S Photonics, the GaAs- and InP-based component maker formerly owned by Avanex and Alcatel Optonics, has posted an 87% increase in sales for fiscal year 2008.

This comes despite Avanex deciding to shed 47 employees before the end of October as it rationalizes its tunable transponder and transceiver operations.

In the 12 months that ended on June 30, the now-privately owned company recorded revenue of €27.9 million (\$39.6 million) and tripled its net profit to €2.1 million as the fiber-optic recovery gathered momentum.

According to 3S Photonics, the optoelectronics market itself grew 15% over the past year. It was able to exploit this with new products like its 980 nm GaAs-based pump lasers that are used in submarine amplifier

components to boost fiber-optic signals.

This focus limits the Nozay, France, fab's exposure to Avanex's current problems. Yannick Bailly, 3S Photonics' vice-president of marketing, told *Compound Semiconductor* that Avanex now contributes less than 8% of his company's sales. "Our main customers are based in Asia and thus we are much less affected by the US market turn-down," he said.

3S Photonics has chosen not to produce tunable laser diodes like those used in transceivers and transponders made at Avanex's soon-to-be-closed Melbourne operation, Bailly says. "Santur and JDSU made good business in the past, but now the market is overcrowded," he said. "Margins are very low when compared with the high level of investment that is needed."

Instead of tunable products, 3S is currently developing photonic integrated circuit technology and higher-power linear transmission lasers.

Templates for Blue and UV LEDs

GaN, AlN, AlGaIn, InN, InGaIn



World leaders in development of Hydride Vapour Phase Epitaxy (HVPE) processes and techniques for the production of novel compound semiconductors

- Templates
- Wafer size: 50mm-150mm
- Research grade InGaIn wafers
- Custom design epitaxy
- Contract development
- Small and large batch quantities available

Wide range of materials (GaN, AlN, AlGaIn, InN and InGaIn) on different sizes and types of substrates (sapphire or SiC)

Contact us now!

welcome@tdii.com

Technologies & Devices International

Tel: +1 301 572 7834



An Oxford Instruments Company



The Business of Science®

www.oxford-instruments.com/tdi1

OPTICAL COMMUNICATIONS

PICs lift the economic gloom in Brussels

The fiber-optic component industry is back in a growth phase and September's European Conference on Optical Communications (ECOC) saw photonic integrated circuits (PICs) take center stage.

With manufacturers of fiber-optic components like 3S Photonics and Bookham also getting back onto a firmer financial footing, this year's ECOC ought to have been positive for III-V specialists.

Unfortunately, because it took place during the apparent unravelling of the global financial system, the mood at the event took on a gloomier air, compounded by news of cuts in carriers' capital spending.

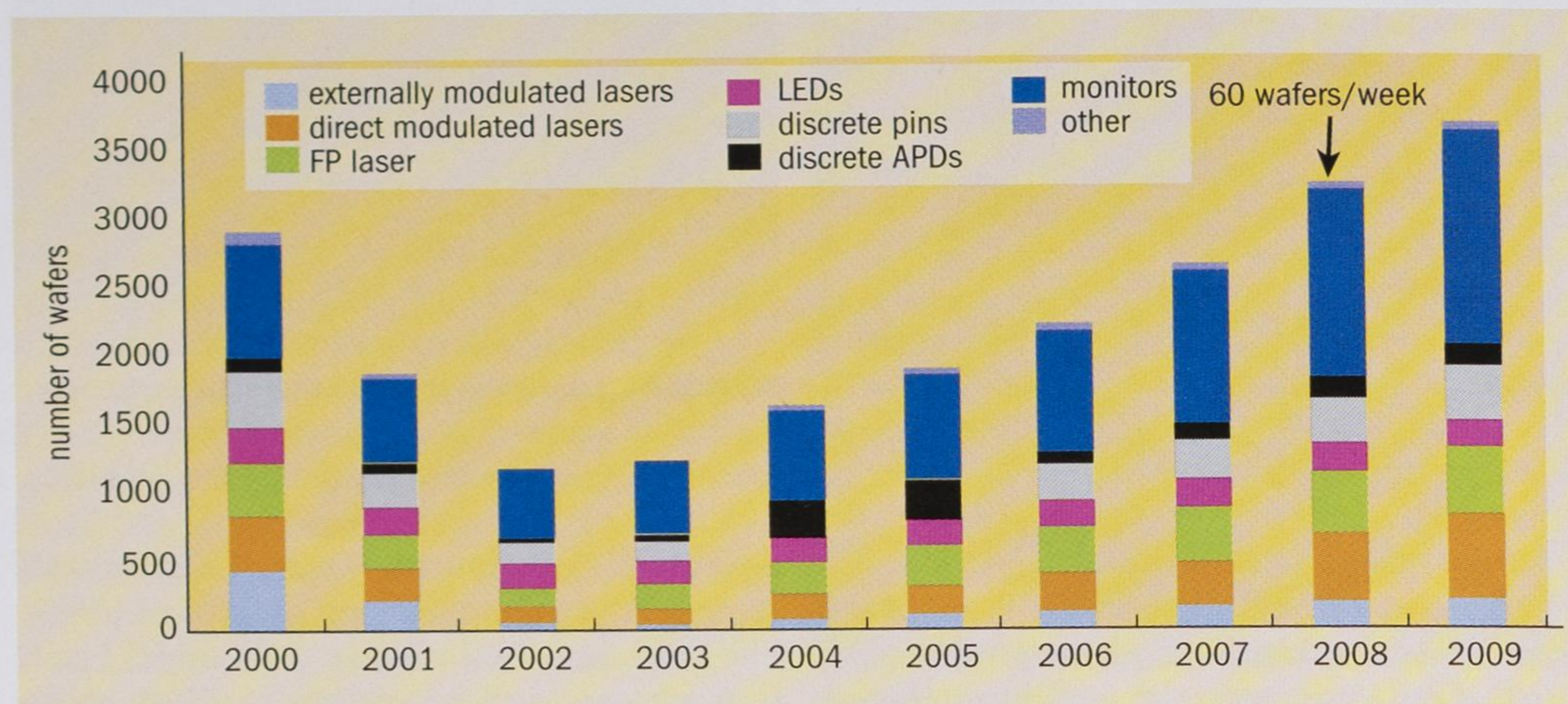
However, one concept that helped to elevate the spirits was the PIC. No longer the exclusive preserve of Californian firm Infinera and a handful of photonics research groups, this technology has clearly caught the eye of other companies.

Even before the event started, it became clear that Infinera might be facing more competition in the PIC realm. Close neighbor Santur said that it would demonstrate live PIC-enabled 100 Gbit/s transmission and another Valley company, JDSU, unveiled what it described as the world's first photonic integrated amplifier – effectively a new generation of the erbium-doped fiber amplifier.

The UK's aptly named Centre for Integrated Photonics (CIP) also demonstrated its own new integrated photonics platform, dubbed "HyBoard". Graeme Maxwell, CIP's vice-president of hybrid integration, said that the approach can deliver "bespoke, truly scalable and cost-effective PICs, optimized to the end-user's requirements at realistic yields".

On top of these demonstrations, PICs were heavily referenced in a workshop discussion on the future of photonics foundry companies. Mike Lebby, president of the Optoelectronics Industry Development Association (OIDA) described PICs as being the "in" fiber-optic technology, explaining that most of the newer proponents are targeting the network edge, as opposed to Infinera's focus on the network core. This means fiber-to-the-premises applications and suggests that volume demand for PICs ought to become significant in the long run.

The photonics foundry workshop encompassed silicon and III-V optoelectronics. Lebby highlighted that, despite a recent recovery in the telecommunications market



With only around 60 fiber-optic-related InP wafer starts per week worldwide, the Optoelectronics Industry Development Association says that a collaborative foundry approach could be the best way forward.

for laser diodes, the number of InP wafer starts needed to meet fiber-optic industry demand (around 60 per week) is still only sufficient to support one or two foundries.

The OIDA president believes that there is a better approach than that used by the industry today. He advocates the creation of a virtual photonics foundry, along the lines of MOSIS (metal oxide semiconductor implementation system). The MOSIS service began in 1972 to support industrial, university research and government institutions in the US, allowing both start-ups and established companies access to much cheaper research facilities.

Such a foundry could also accelerate PIC development, believes Lebby, who has been attempting to size up the US market potential for new classes of highly integrated PICs. He says that the current practice is not ideally suited to the PIC approach. This is partly because the foundry customer needs significant experience in design, epitaxy, processing and test procedures before it can approach foundries or epi suppliers.

In what he describes as a "III-V foundry concept for tomorrow", Lebby suggests that an additional step in the chain – an interface between the customer and the foundry companies – could be the answer, allowing the development of common platforms for different applications.

The large physical size of PICs means that wafer diameter will be a key issue, he adds, suggesting that III-V on silicon might ultimately provide the common platform for a successful foundry model.

CIP will argue that it has come up with

a foundry solution, although it is not a full monolithic integration process. Aimed at network-edge applications like metropolitan wavelength division multiplexing, CIP's multichannel laser module features individual InP sources aligned to silica waveguides and other passive optical elements, including an arrayed waveguide grating.

Because CIP's photonic integration relies on board-level integration of InP chips, planar silica waveguides and micro-machined silica sub-mounts, it isn't directly comparable to chip-level photonic integration like Infinera's. But its ECOC demonstration showed that the concept can deliver impressive 32-channel transmission, in which each channel can be switched individually.

Tunable laser specialist Santur's live 100 Gbit/s demonstration at ECOC did involve a much higher degree of integration than CIP's, however. The US firm's approach is a variation on its existing tunable laser technology, which contains an array of 10 lasers tuned using a micro-electro-mechanical system (MEMS) device. But in the new PIC, the MEMS device has been replaced by a passive multiplexer, which combines the light from all of the 10 Gbit/s lasers (running at the same time) onto a single fiber.

The company claims that its device offers a simple solution for distances up to 10 km in access networks and short-reach interconnects. It could be cheaper than the 4 × 25 Gbit/s or parallel optics schemes that are being considered for 100 Gbit/s applications.

● Additional reporting by Pauline Rigby and Jeff Ferry.

*Do you want to be ahead
of the industry's roadmap?*

AIXTRON



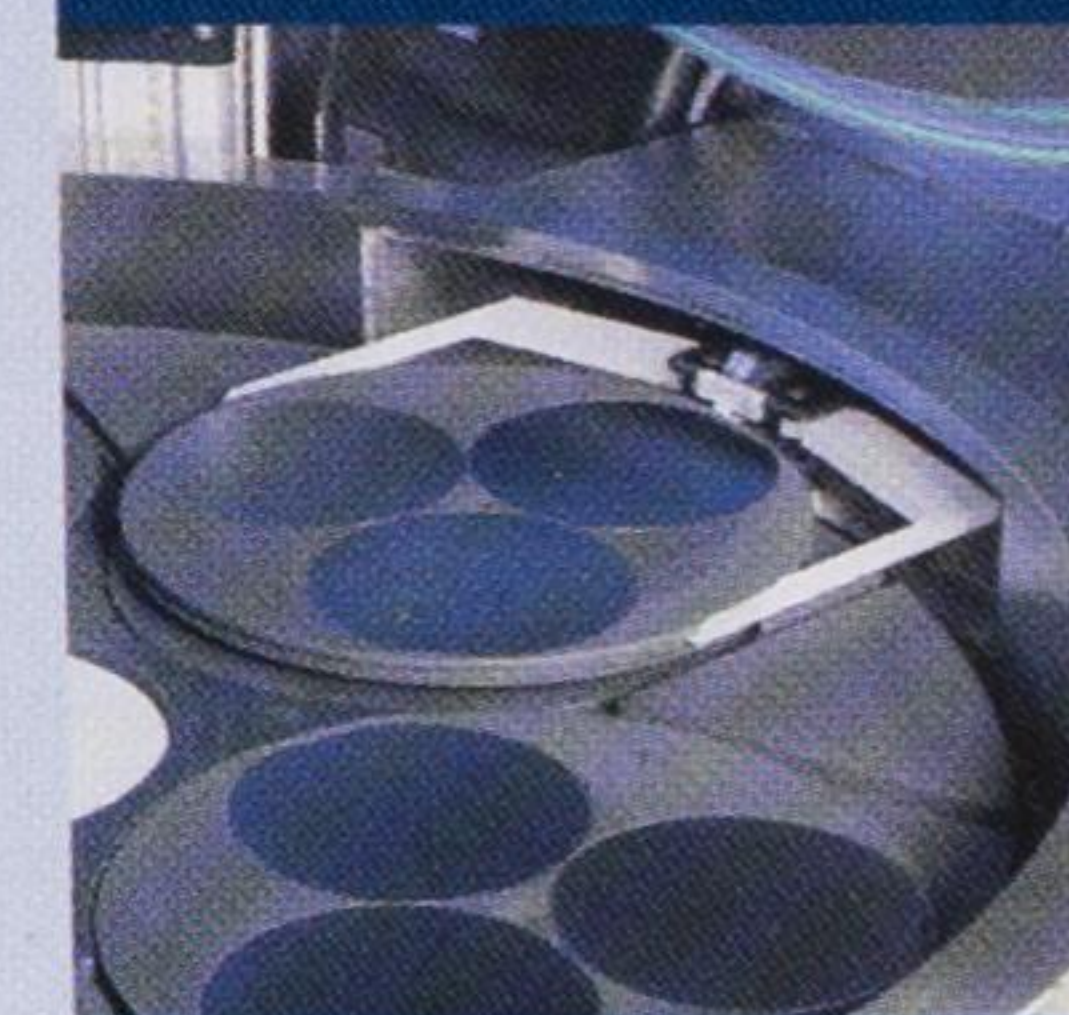
Marathon production for the manufacture of As/P LEDs and Solar Cells on 2 inch to 8 inch Substrates

AIXTRON supplies MOCVD systems equipped with automated wafer handling up to 8 inch enabling high throughput production at low cost of ownership.

Be ahead of the industry's roadmap and increase your throughput, device yield and quality with AIXTRON's deposition equipment.

The AIXTRON product range comprises R&D and production tools for compound, organic, or SiC materials and nanostructures.

ALD ■ AVD® ■ CVD ■ MOCVD ■ OVPD® ■ PECVD ■ PVPD ■ SiC CVD



AIXTRON

AIXTRON AG · Kackertstraße 15-17 · 52072 Aachen, Germany
info@aixtron.com · www.aixtron.com

push your  **PERFORMANCE**



CAPITAL EQUIPMENT

Aviza sees a bright spot in compounds

It isn't just Wall Street that's down in the dumps – spending on semiconductor equipment has slumped over the past six months. Fortunately, compound semiconductor markets are bucking the trend, writes Aviza's **Kevin Crofton**.

Table 1. Semiconductor equipment billings (\$bn)

Region	Q2 2008	Q1 2008	Q2 2007	Quarterly change	Year-on-year change
Europe	0.52	0.73	0.62	-29%	-15%
China	0.47	0.81	1.22	-42%	-61%
Japan	1.93	2.39	2.06	-19%	-6%
North America	1.25	1.84	1.51	-32%	-17%
Korea	1.41	1.74	1.77	-19%	-20%
Taiwan	1.45	2.37	3.20	-39%	-55%
Rest of the world	0.80	0.67	0.63	19%	26%
Total	7.83	10.56	11.01	-26%	-29%

SOURCE: SEMI

Second-quarter semiconductor equipment billings, according to these figures from SEMI, showed a steep decline on both the prior quarter and one year ago. Total bookings of \$7 billion during the same period were down 30% year on year, but SEMI still expects a recovery in 2009.

The global economy is slowing, and the west is already in a recessionary state – that much is obvious. Rising fuel and food prices, lower consumer confidence and job-security concerns have suppressed discretionary spending, and these same trends are putting pressure on the end markets served by our customers.

In the IC sector, the story is a mixed one. Total unit sales and average IC selling prices grew at double-digit percentages between the first halves of 2007 and 2008. However, in stark contrast, spending on equipment has felt the squeeze. SEMI's latest figures showed equipment bookings at a five-year low, following five straight months of rapid decline.

That IC units have continued to grow while capital equipment spending is in a slump suggests that equipment utilization is rising, and at some point new investments will need to be made. Industry analysts at Gartner and SEMI anticipate this turnaround in the second half of 2009, while cautioning that their data are heavily dependent on the impact of the current economic slowdown, and rely on access to finance through the battered capital markets.

From a distance then, an observer could be forgiven for concluding that the semiconductor equipment market is a bad place to be. But there are opportunities, both in silicon and III-Vs, and ultimately IC producers must invest if they are to remain competitive for the next growth cycle.

In the silicon world, one bright spot is advanced packaging: specifically three-dimensional chip stacking (3D-IC), where two or more die are stacked vertically and connected by through-silicon vias (TSVs).

The approach not only delivers a more compact package, it also improves performance because the vertical interconnects are shorter than horizontal global wires, cutting resistance-capacitance delays. And there is more to come – 3D-IC has the potential to stack dissimilar die, creating heterogenous “super-

packages” containing memory, microprocessors, power devices, analog chips and more.

The first generation of 3D-IC is in volume production, and uses traditional wire bonding. However, research programs are developing a second-generation design where peripheral wire bonds are replaced with TSVs – channels that are made by etching through the middle of the die using plasma processes and then filled with conductors such as copper.

This technology is a classic example of an IC maker leveraging its core expertise in a new field, delivering growth despite the softness of capacity investment. But we see a different story in compound semiconductors – a market that is bucking the more widespread trend of cautious capital spending.

Five or six quiet years followed the heavy capacity additions of the communications technology bubble of 2000 and 2001, but now we see that capital spending by compound semiconductor makers is on the rise – and not just in the blooming high-brightness LED (HB-LED) sector.

Currently accounting for just 6% of total global semiconductor revenues, the compound market is nevertheless growing 50% faster than the overall semiconductor market, and its total revenues are expected to exceed \$30 billion by 2012, according to BCC Research. If correct, this growth would represent a doubled market share of the total semiconductor industry in just five years.

What will drive this upsurge? The demand for GaAs-based RF integrated circuits will increase, thanks to growing shipments of mobile wireless devices, plus new, long-range wireless access architectures such as WiMAX. Wireless industry experts at ABI Research expect more than 1.3 billion mobile devices to ship in 2008. And despite the uncertainties of global economics, they say that growth will continue, largely driven by developing markets in Asia, South America and Africa.

Optoelectronic devices will also contribute strongly. BCC's report predicts double-digit growth of fiber-optic communications between now and 2012 to serve demand for broadband communications, while high-definition video applications like Blu-ray will fuel similar growth in optical data storage.

HB-LEDs provide perhaps the brightest application spot of all. Continued improvements in the luminous efficiency and color rendering of GaN-based white HB-LEDs, combined with lower manufacturing costs, will start to open up the general illumination market over the next 2–3 years, building on a sector already valued at more than \$4 billion per year.



Copper-filled through-silicon vias, seen here, is a growing application area.

While technology is doubtless advancing, innovation in compound semiconductor IC processing has typically proceeded more slowly than its silicon affiliate – partly because substrate sizes have been limited to less than 200 mm, but also because performance benefits relate primarily to III-V material properties rather than raw device scaling. That said, the scaling of compound semiconductor devices does still enhance performance, and the need to reduce costs is now forcing device manufacturers to adopt some of the processing technologies that are more usually associated with silicon ICs.

Shrinking device-critical dimensions provides more than an increase in die per wafer: it improves device performance, increases fab yields and delivers a higher return on capital investment. The flip side is an added complexity in device interconnection, which requires an accompanying increase in the number of metal layers in wafer processing. This brings further challenges, with planarization processes needed to provide the surface flatness demanded by lithography depth of focus.

Aside from increasing the number of processing steps, the use of multi-level metal will also significantly increase material costs associated with the gold that is typically used as the interconnect metal in compound semiconductor ICs. To partially offset this cost increase, chip makers are beginning to incorporate the copper interconnect architectures that have

long been favored by silicon IC fabs.

Device shrinkage also puts strain on the passive capacitor, a key part of most GaAs-based RFICs. More-aggressive design rules necessitate an increase in capacitance per unit area. While there is hope of addressing this by using thinner conventional materials such as PECVD SiN, reliability concerns will eventually force the introduction of higher “k” dielectric materials and, perhaps, the use of MOCVD or even ALD processes for dielectric deposition.

Device scaling also places greater demands on etch processes. Recessed gate technology is widely used as a method to reduce noise in GaAs-based transistors. This has traditionally been done using a wet-etching process. But because of the relative lack of critical dimension (CD) control, gate CD shrinkage eventually makes the use of wet etch impractical, and high-selectivity dry-etch processes must be developed.

So while the dark economic clouds have moved in and become a full-blown storm, in the semiconductor equipment world there is room for optimism, and this is particularly true within the compound semiconductor niche. Aviza is committed to supporting the smaller wafer platforms required by manufacturers, while for future needs we have considerable production experience with copper interconnects and high-k dielectrics – the technologies that compound semiconductor makers will soon need and which conventional tool suppliers to the niche may not be able to provide.



About the author

Kevin Crofton is senior vice-president of product business units at Aviza Technology. He previously worked at Lam Research, Newport Corporation and NEXX Systems.

POLYMER ELECTRONICS 2009

A unique opportunity to ensure that you are at the forefront of polymer electronic developments

Barcelona, Spain, 4 - 5 February 2009

Register before
4 December 2008
and save €200!

For more information and to register online, please visit:

www.polymerconferences.com

or telephone the Smithers Rapra Conference Department

tel +44 (0)1939 250383, fax +44 (0)1939 252416 or e-mail conferences@rapra.net

Organised by...  **rapra**

SiC material developments p

Andy Extance saw graphene emerge as a great new hope at ECSCRM 2008, while Japanese car makers help to fuel steady progress towards more-reliable SiC electronics.

For the past few years, the SiC community has waited tensely for chips made from the material to move confidently on from their tentative early steps in the high-power commercial electronics market. But other than LED-maker Cree, which produces and consumes SiC substrates in its light emitters, developers of the semiconductor material are still waiting for the big pay-off.

As SiC technology creeps forward, development funding ebbs and flows. At this year's European Conference for Silicon Carbide and Related Materials (ECSCRM) in Barcelona, Spain, some SiC groups admitted that their contingents had shrunk from previous years. Murmurs of difficulties in obtaining money to support ongoing SiC studies emerged from university professors gathered in darker corners, and were echoed by researchers with links to the US military. However, notable advances ranging from fundamental material research to commercial applications were on hand to provide any apathetic paymasters with food for thought.

The collective relief from such concerns provided by the conference's first-ever dedicated session on graphene was palpable. The University of Manchester's Andre Geim and Kostya Novoselov gained the Europhysics prize for the isolation of graphene in 2004 just a week before ECSCRM. With the pair subsequently touted as an outside shot at the Nobel Prize for Physics, the excitement surrounding SiC's potential impact in this area could be the perfect wake-up call to funding bodies.

Graphene is a continuous sheet of hexagonal carbon rings that when stacked with other sheets is well known as graphite. It was first characterized by removing monolayers from graphite with adhesive tape, shortly followed by production from SiC – a potentially more high-throughput approach. The SiC-based method heats conventional substrates so that silicon evaporates and leaves graphene behind.

The graphene research presented at ECSCRM ranged from the fundamental – for example microscopy analysis of graphene formed on SiC – to more practical concerns like improved preparation methods. Pierre Mallet of the multidisciplinary Néel Institute in Grenoble, France, bridged both areas. To date, much material made from SiC has been few layer graphene (FLG), which is essentially a graphene monolayer above graphite layers. Mallet and his colleagues made graphene by repeated anneal-

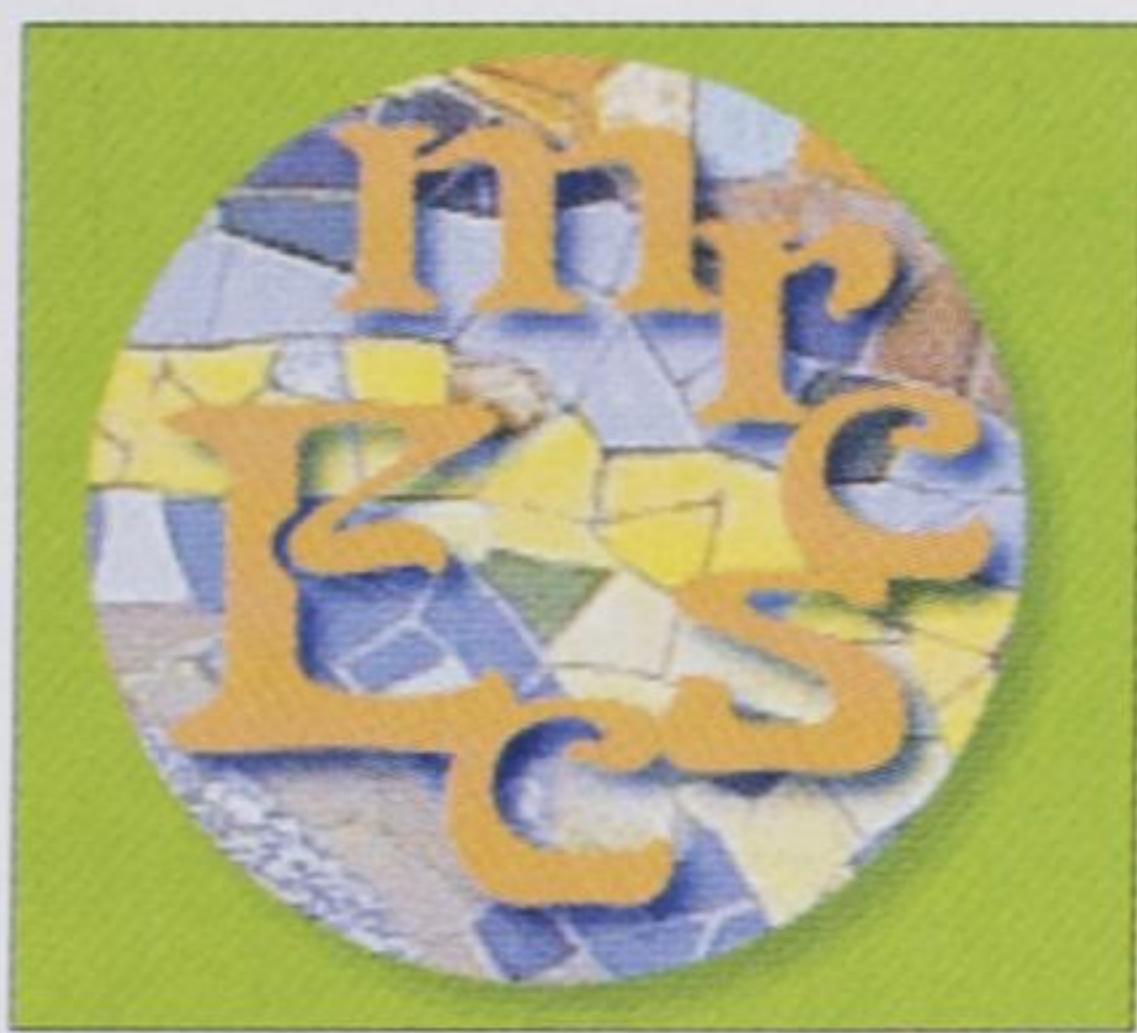


SiC makers are rapidly approaching their power-electronics goals, unlike attem

ing of 6H-SiC at temperatures of up to 1100°C under ultra-high vacuum. Using scanning-tunneling microscopy the team showed that it had made 10–40 nm islands of true monolayer graphene.

Linköping University drew notable crowds during the poster sessions with its researchers' attention-grabbing graphene developments. They showed characterization details and images of 2 inch diameter graphene monolayers produced in a specially modified furnace. Annealing at 2000°C yields a single domain of graphene above most of the underlying 6H-SiC wafer, but also surprisingly generates some regions with a different structure according to low-energy electron microscopy.

Graphene boasts many exceptional qualities, but the interest at ECSCRM largely revolved around its promise as a basis for nanoelectronics. At the beginning of the year a team including Geim found that the intrinsic electron mobility of graphene was around 200,000 cm²/Vs. This remarkable figure compares with 1500 cm²/Vs for silicon and 8500 cm²/Vs for

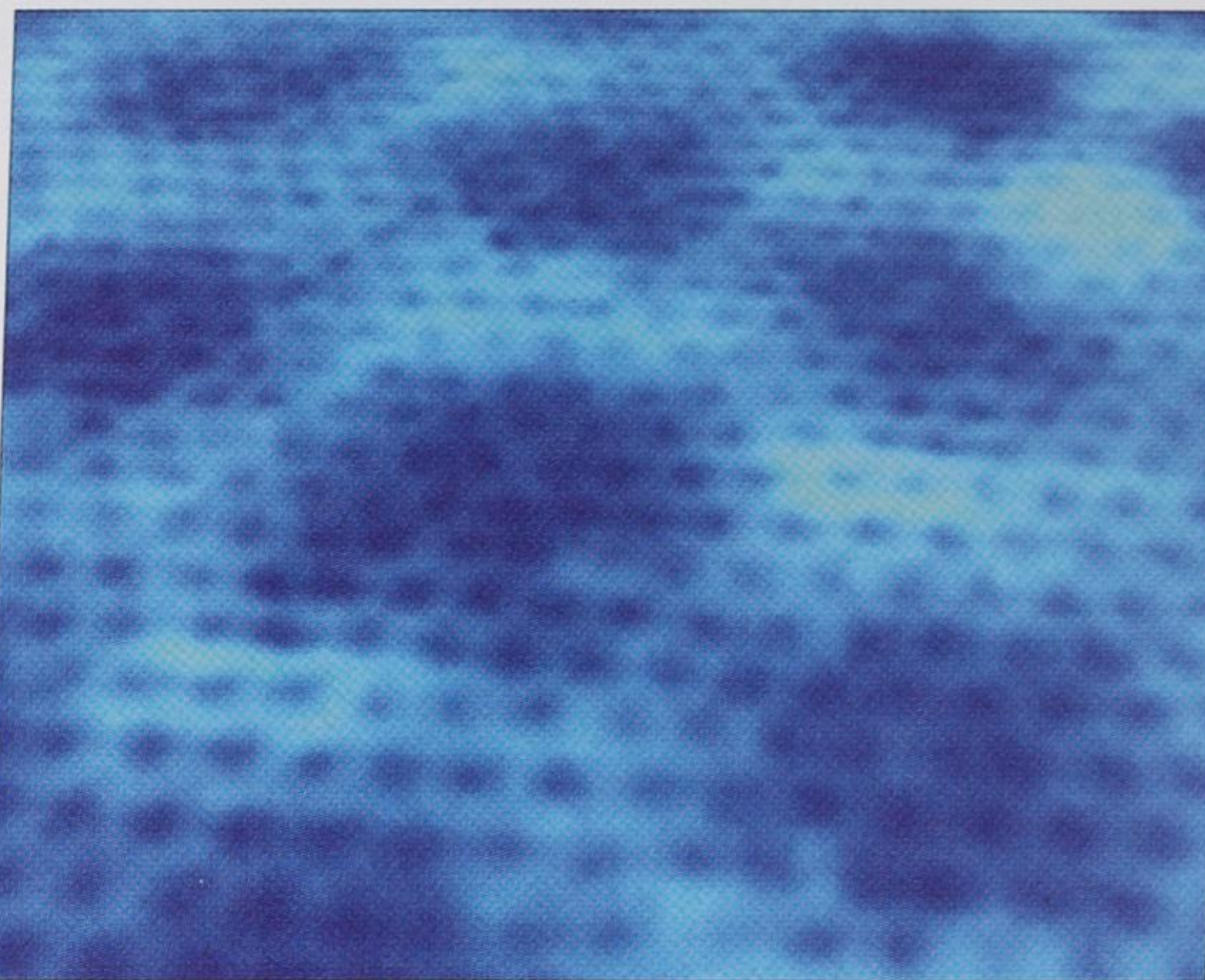


The biennial European Conference on Silicon Carbide and Related Materials (ECSCRM) was held this year at the Axa Winterthur Auditorium in Barcelona, Spain, on 7–11 September. 443 delegates and 20 exhibitors gathered from 27 countries to attend, with a 65:35 ratio of academic to industrial attendees.

power progress in Barcelona



ke attempts to complete Gaudi's Sagrada Família church in Barcelona, Spain.



The hexagonal honeycomb structure of monolayer graphene (left) is revealed under low-bias scanning tunneling microscopy by Pierre Mallet and colleagues at the Néel Institute.

GaAs. The problem for this fledgling field is how to use these properties in devices that are compatible with graphene's single-atomic-layer thickness. "If you look at where processor speeds are now, and look at Intel's roadmap, we've got 15 years to figure it out," joked one attendee. However, Shriram Shivaraman of Cornell University produced some of the first basic Schottky devices by evaporating metal dots on graphene formed from n-doped epitaxial SiC substrates. The graphene devices operated at higher currents than Shivaraman's SiC controls for the same forward voltage.

Advances in producing the cubic 3C-polytype of SiC represent a more immediately significant, and under appreciated, development than graphene. The flat surface and high elastic modulus of 3C-SiC makes it a strong candidate for the development of harsh-environment micro-electro-mechanical systems. 3C-SiC's properties may also help in metal-oxide-semiconductor (MOS) device applications, because reduced defect density at the SiC MOS

gate interface may help to improve carrier mobility.

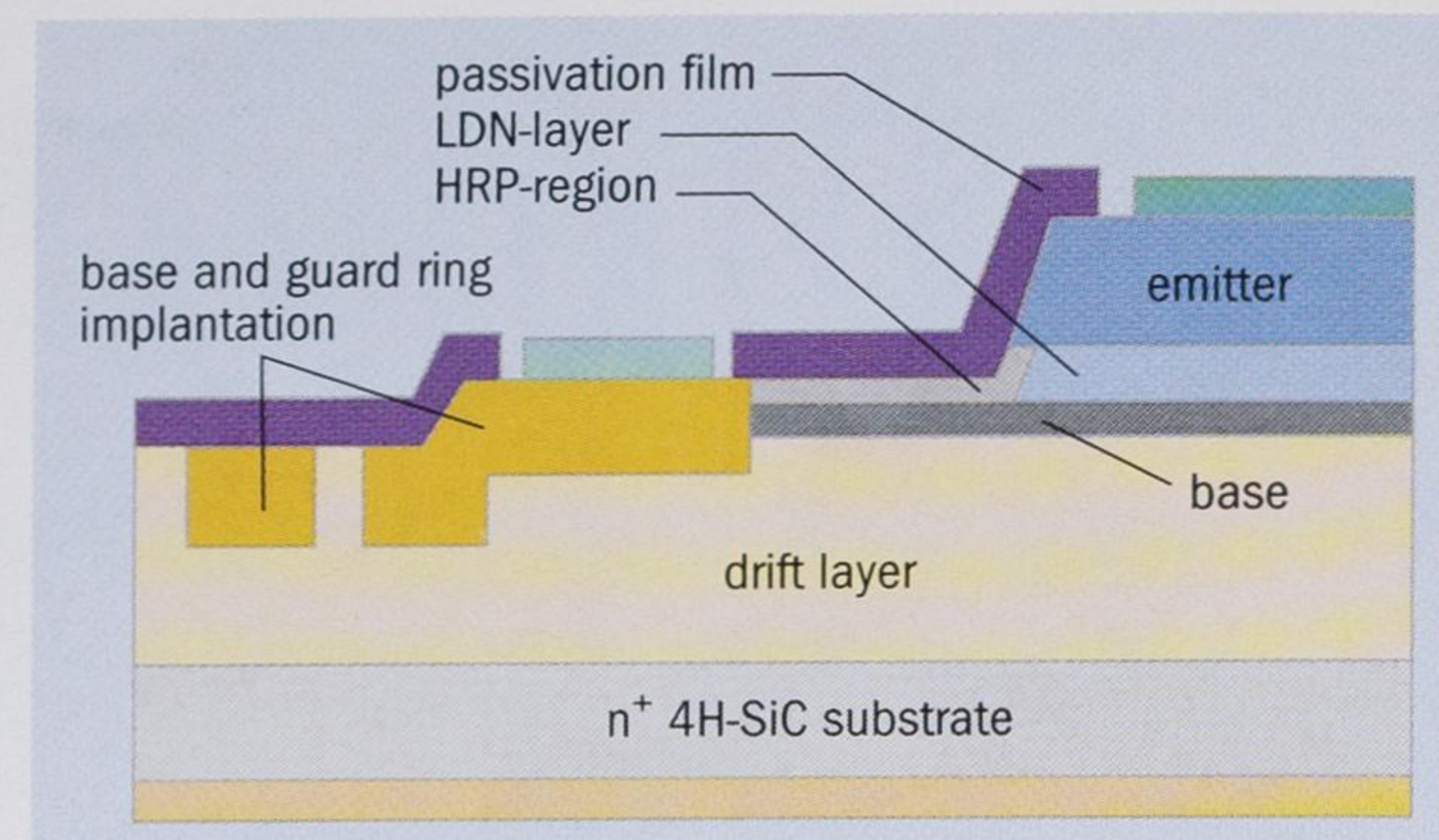
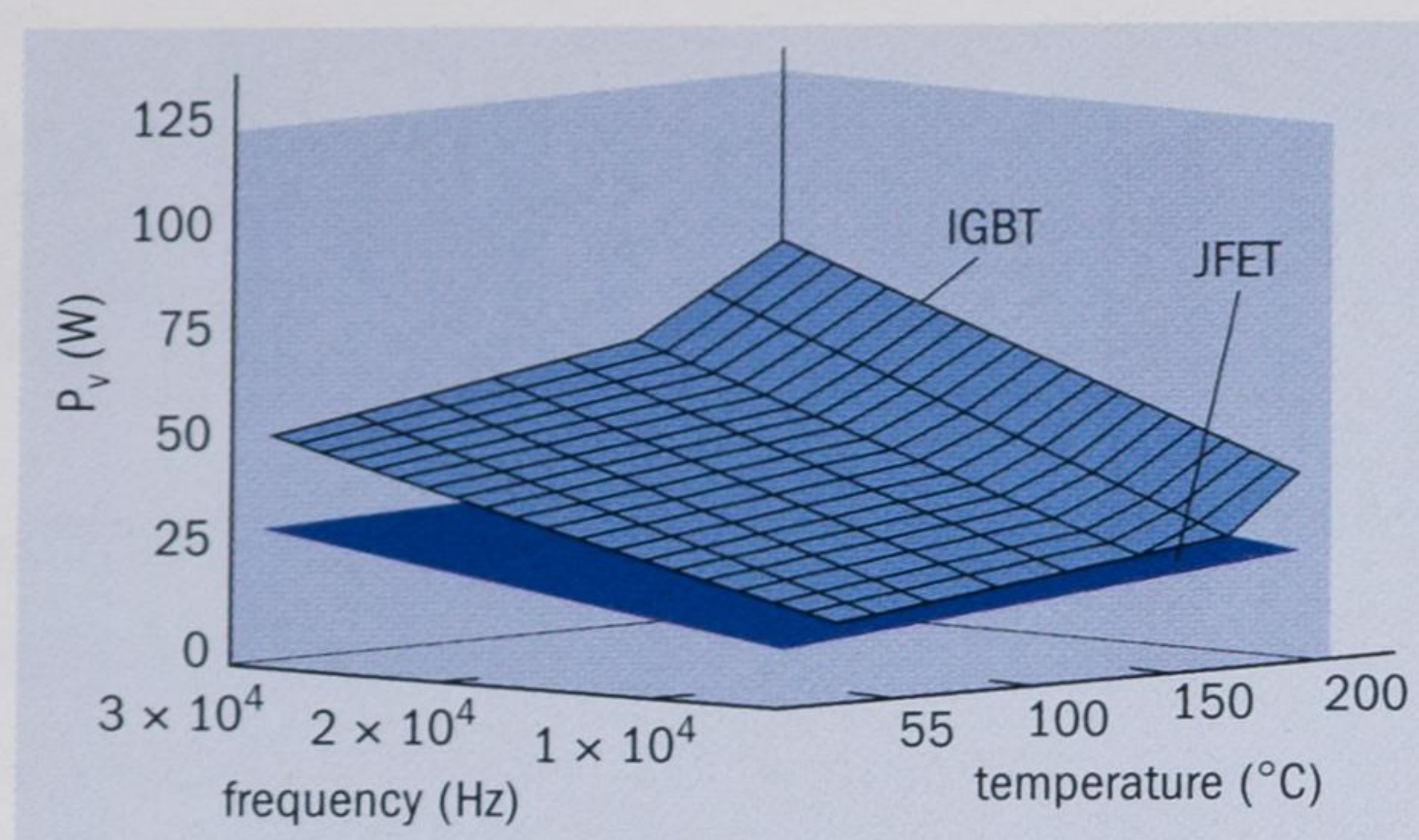
Ever since the first international conference on SiC in 1959, bulk single-crystal 3C-SiC growth has been held back by a lack of good-quality seed crystals. Now the European MANSiC project, set up specifically to advance 3C-SiC, is changing this. The institutions involved in the project, which is funding 19 young researchers, were represented in all of the oral presentations given on 3C-SiC at ECSCRM. In terms of bulk growth, 1.7 mm/h millimeter-size ingot production by sublimation was the key breakthrough, presented by Didier Chaussende of the Grenoble Institute of Technology.

A host of posters demonstrated the wider interest in both 3C-epitaxy and bulk growth, with the volume of work from Japan rivaling that coming from the European collaboration. The status of 3C-SiC epitaxy on non-native substrates has recently advanced rapidly and MANSiC member NovaSiC is formally selling 3C epiwafers. The company's presentation detailed epilayer thicknesses up to 12 μm grown on 2 inch silicon substrates, which hold the potential for expanding to larger diameters in the future.

4H-SiC remains the workhorse for SiC electronics, which typically use substrates sliced at an 8° angle from the primary 4H axis. This provides a saw-tooth-like surface for epitaxy that helps epilayers retain the 4H polytype. Unfortunately, each tooth can be the source of defects known as basal-plane dislocations (BPDs), which have been shown to evolve into other faults under bias and limit the lifespan of SiC devices. Unsurprisingly, given its pre-eminence in the SiC arena, Cree's pioneering method for eliminating BPDs is strongly defended by patents.

However, at ICSCRM 2007 – the international version of ECSCRM – in Otsu, Japan, much interest surrounded a new anti-BPD approach developed by the US Naval Research Laboratory (NRL). In

Fig. 1. (right) SiCED's JFETs operate in the Technical University of Braunschweig's test inverters with lower power losses than its parent company Infineon's silicon IGBTs at 1 A/mm² current density. **Fig. 2.** (far right) Honda's record-gain BJT, in which the interface between the lightly doped n-type (LDN) layer and a highly resistive p-type (HRP) region reduces recombination and improves gain to a record 114.



Barcelona, Brenda VanMil explained how the NRL approach interrupts SiC chemical vapor deposition by cutting silane gas and reducing propane gas flows. Initially at each interrupt the team was able to convert 34% of BPDs to threading etch dislocations that do not limit device performance. Optimizing the temperature of the interrupt formation step to 1580°C brings the conversion rate to more than 50%. Performing two interrupts with at least 2.5 µm of epitaxial material in between increases the proportion of BPDs converted to 84%.

Another star turn from ICSCRM was the Japanese Central Research Institute of the Electrical Power Industry, which this year showed that more techniques for BPD reduction are possible. The team detailed how it was able to perform virtually BPD-free SiC growth by turning down the growth rate in its high-speed epitaxy reactor from 250 to 20 µm/h.

Although the potential device lifetime benefits of these improvements are hopefully in the pipeline, SiC component manufacturers can already claim important performance achievements. At ECSCRM, Muhammad Nawaz from Swedish SiC transistor producer TranSiC detailed how his company's BJTs could be operated from -86 to 500°C. The breakdown voltage remained unchanged, although gain diminished with increasing temperature.

Driving SiC advances

Before the automotive industry displaces silicon with SiC in its electric vehicles, it wants further performance improvements. However, according to the Institute for Electrical Machines, Traction and Drives at the Technical University of Braunschweig, there are some circumstances where SiC already wins out. Immo Koch compared the power losses seen with a SiCED SiC JFET with those from an Infineon silicon IGBT in inverters for switching frequencies between 5 and 30 kHz. At high temperatures and current densities the extensive conducting losses from the JFET inverter limit its benefit to higher frequencies. However, at reduced current density SiCED's JFET is also superior for lower switching frequencies.

Infineon, which part-owns SiCED with joint venture partner Siemens, previewed some of the technology that will be used in its third-generation SiC Schottky diodes, from which it is currently releasing pilot products. The German giant claims to have

boosted reliability with a more thermodynamically and mechanically stable soldering process, an otherwise little-discussed topic in SiC device production. Semisouth, based in Starkville, MS, is also looking to add to the range of commercial SiC devices available with an official move from epiwafer supplier to vertical JFET manufacturer in 2009.

However, it was arguably Japanese automotive manufacturers who made the largest impact in Barcelona. Progress in SiC devices, especially in conjunction with their semiconductor industry compatriot Rohm, appears to be at a critical point. Development projects involving Honda and Nissan featured in the chip maker's status update, and represent some of the most successful work to date on power modules for electric vehicles.

Like Infineon, Nissan has successfully resolved reliability issues surrounding the packaging of SiC. Using a tantalum/TaN barrier, Satoshi Tanimoto was able to suppress a destructive reaction between Ni₂Si contacts and the aluminum interconnect that Nissan uses with SiC devices. Kenichi Nonaka described Honda's suppressed surface recombination structure BJTs (SSR-BJTs). These BJTs possess a lightly doped n-type layer and a highly resistive p-type region that reduces concentrations of electrons and holes at the device's SiC surface (figure 2). This improves current gain of the SSR-BJT even if there is a high density of recombination centers on the SiC surface. In this way, Honda delivered a BJT with a record gain of 114, 2.8 mΩ cm⁻² on-resistance and 1150 V blocking voltage.

ECSCRM's welcome reception brought a reminder of how tough the economic environment beyond SiC research has become, clashing with the lavish surroundings of the Liceu opera house in which it was held. Carles Gómara, director of innovation in the Catalan government's ministry of industry, lauded the environmental and industrial benefits that are promised by SiC. He emphasized the importance of technological development in driving economic growth at a time when recessions are taking root around the world. With its slow but steady progress towards end markets, the SiC community is already cautious about the future. However, as Gómara suggests, its impact on areas of rapidly growing interest like graphene and electric vehicles should provide a strong bolster to its confidence. ●

Uncovering the LED's darkest secret

Droop stops GaN-based LEDs performing in the critical regime for emerging applications – high-current densities. However, this weakness can be overcome with polarization-matched epitaxial structures, say RPI's **Martin Schubert**, **Min Ho Kim**, **Jong Kyu Kim** and **E Fred Schubert**.

LED makers are eyeing up new markets – automotive headlights, large-area displays and general illumination. To some degree, declining prices will help LEDs to penetrate these areas, but this in itself cannot guarantee success. Chips will also have to deliver very high efficiencies at high drive currents. And this means addressing a highly publicized problem that goes by the name of droop.

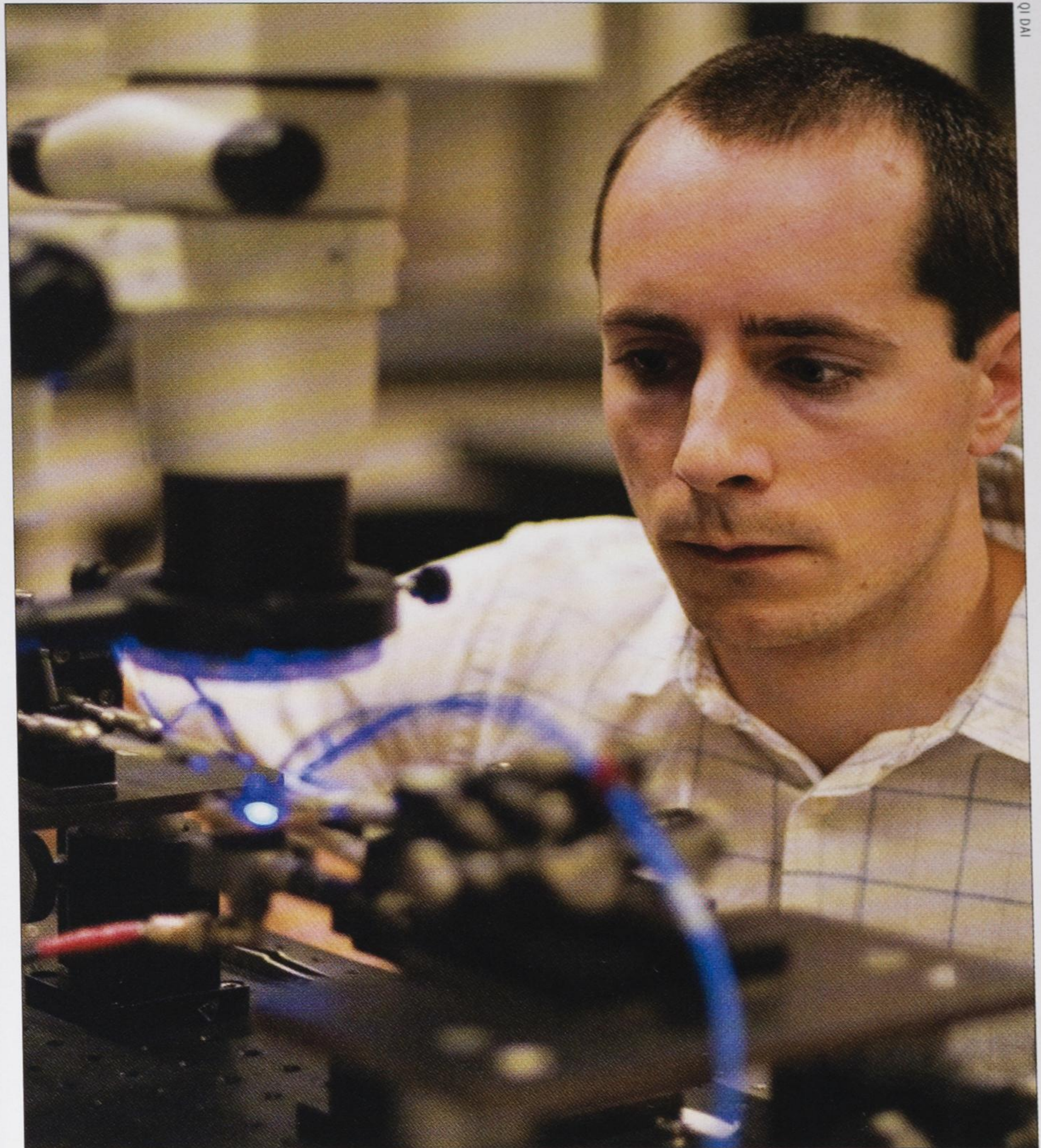
This term describes the lower efficiencies of blue, green and white LEDs at higher currents. GaN-based LEDs typically hit peak efficiencies at just 10 A cm^{-2} , and can fall to half that value by 100 A cm^{-2} . This is a major concern because today's high-brightness chips already need to operate efficiently at current densities well beyond 10 A cm^{-2} , and further progress is absolutely critical if the community is to stick to LED roadmaps.

Tackling this issue is clearly important, and it is attracting a great deal of interest from researchers in industry and academia across the globe. This includes our team at Rensselaer Polytechnic Institute in Troy, NY, which has been studying the origin of droop for the last few years. We believe that we now understand the cause and how to combat the problem with a radically different LED design.

Some of our work on understanding the cause of droop was carried out in collaboration with Mary Crawford's group at Sandia National Labs, NM. We focused on the influence of dislocation density on LED efficiency, discovering that while dislocations reduce low-current efficiency, they do not impact the droop-causing mechanism at high currents. At low currents, carriers are often lost to a trap-assisted process – Shockley-Reed-Hall recombination, which becomes more severe as the dislocation density increases. Cranking up the current initially improves efficiency through an increase in spontaneous emission. However, efficiency then falls due to increased competition from an additional carrier-loss mechanism that causes droop (figure 1, p20).

Leaky LEDs

We have also teamed up with Samsung Electro-Mechanics Company South Korea. This effort exposed the origin of droop – electron leakage from the active region, which is driven by the polarization mismatch between the quantum well, quantum barrier and electron-blocking layers (EBLs). Our



Comparing the output of electrically and optically pumped LEDs has helped the researchers at Rensselaer Polytechnic Institute to investigate the origins of droop in GaN-based devices.

explanation can account for droop's bigger impact at higher currents: the increase in drive voltage causes a greater fraction of the injected electrons to escape from the active region and reach the LED's p-side, where they recombine non-radiatively with holes at the p-contact (figure 2, p21).

This theory has been verified with experiments that compare the light output from LED structures under electrical bias and optical excitation (see box "Probing LED structures", p20). We showed that

Probing LED structures

Rensselaer Polytechnic Institute's (RPI's) researchers investigated droop in GaInN blue LEDs by studying light output under optical excitation and electrical bias. These comparisons have considered equal generation rates for electrons and holes, and the results revealed that droop is governed by carrier transport.

The optical experiments used 405 nm laser excitation. This ensures that absorption is limited to the quantum wells, where the pairs of electrons and holes that are generated will recombine.

Under steady-state optical excitation conditions there shouldn't be exclusive escape of either electrons or holes. If this happens, then the loss of one type of carrier would produce a charged quantum well that reigns in additional carrier leakage. The simultaneous escape of electrons and holes is also unlikely because the holes are strongly confined in the wells.

Nevertheless, some carriers do escape from the wells. Hit this structure with

a 405 nm laser and the consequences include a non-zero open circuit voltage. This results from forward biasing of the device, which is needed to compensate for the reverse current. The net current is zero, which is a requirement for any device that is not connected to an external circuit.

Forward biasing alters the LED's carrier transport. Hole and electron injection and escape rates into and out of the quantum wells are shifted, and it is likely that some of the electrons leak out of the wells. This should manifest itself in a difference between the light output efficiency of LEDs under optical excitation and electrical bias.

Measurements by RPI exposed this difference. Droop was seen in an electrically pumped device, but was absent when the LED was optically excited. This means that a form of recombination mechanism that takes place outside the quantum well is the cause of the droop.

there is a recombination mechanism taking place outside the quantum well, before making the connection between carrier leakage and polarization mismatch with numerical simulations.

Interfacial issues

Our efforts have been restricted to LEDs grown on the conventional plane of GaN – the *c*-plane. These devices feature strong internal electric fields that create large sheet charges at interfaces (see box “Feeling the inner forces”).

The interfacial sheet charges hamper LED performance on two fronts. They increase the barrier to electron injection into the quantum wells, while simultaneously reducing the barrier to electron leakage from the quantum well and over the EBL.

Our simulations back up the hypothesis that sheet charges degrade LED performance via electron leakage and suggest that carrier loss can be combated by cutting interface charges. The calculations also indicate that the lack of heavy p-type doping – particularly of the EBL – can add to efficiency droop. It is well known that the heavy doping of the emitter compared with the base in bipolar junction transistors impedes minority carrier injections into

“The trick is to slightly reduce the bandgap of the barriers, which leads to additional carrier confinement in the active region.”

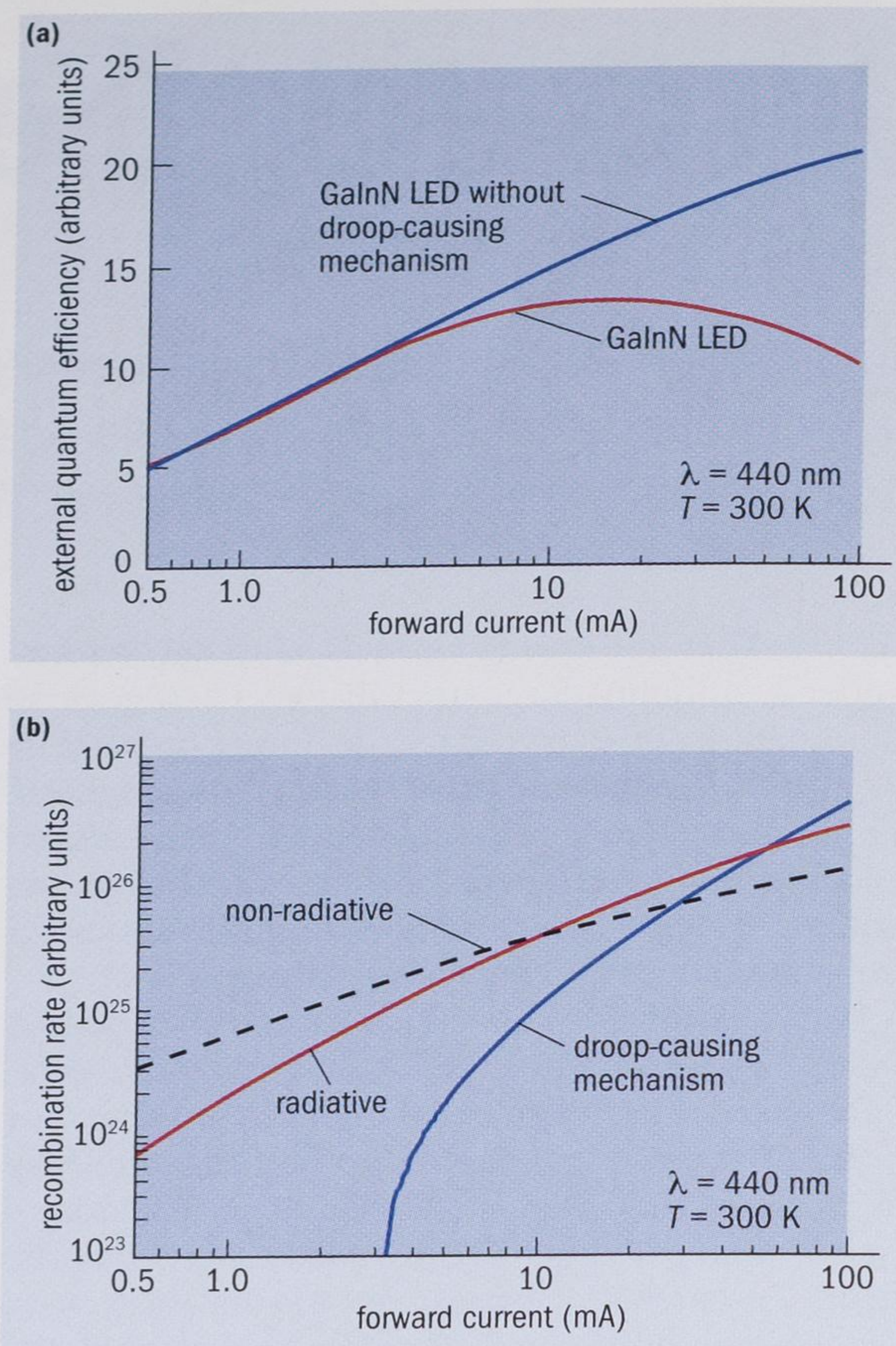


Fig. 1. Measurements on a conventional GaInN LED with a chip size of 1 mm × 1 mm reveal a reduction in output efficiency at drive currents above 10 mA (a). If it were possible to completely remove the droop-causing mechanism, LED efficiency would continuously improve as the current is ramped up. Non-radiative mechanisms dominate at low drive currents, but give way to radiative processes and then droop as the current increases.

the emitter. Similarly, in LEDs, hole injection into the active region can be hampered by low p-type doping levels in GaN and AlGaIn layers. This in turn leads to greater electron leakage.

Our belief that electron leakage explains the LED-droop phenomenon is not universally accepted; in fact, several different mechanisms have been suggested. Prominent among these is Auger recombination, which was proposed by researchers at Philips Lumileds (Shen *et al.* 2007).

Lumileds carried out photoluminescence experiments on *c*-plane GaInN/GaN double heterostructures and observed droop at high optical excitation densities. Analysis with rate equation models led them to assign Auger recombination to the cause of this droop in MQW LEDs.

To reach this conclusion they introduced an effective recombination thickness, which was chosen to be smaller than the physical thickness of the double heterostructure due to reduced electron and hole overlap in the quantum wells.

Feeding this recombination thickness into the rate equations leads to a prediction for a higher spontaneous emission rate in quantum wells with an elec-

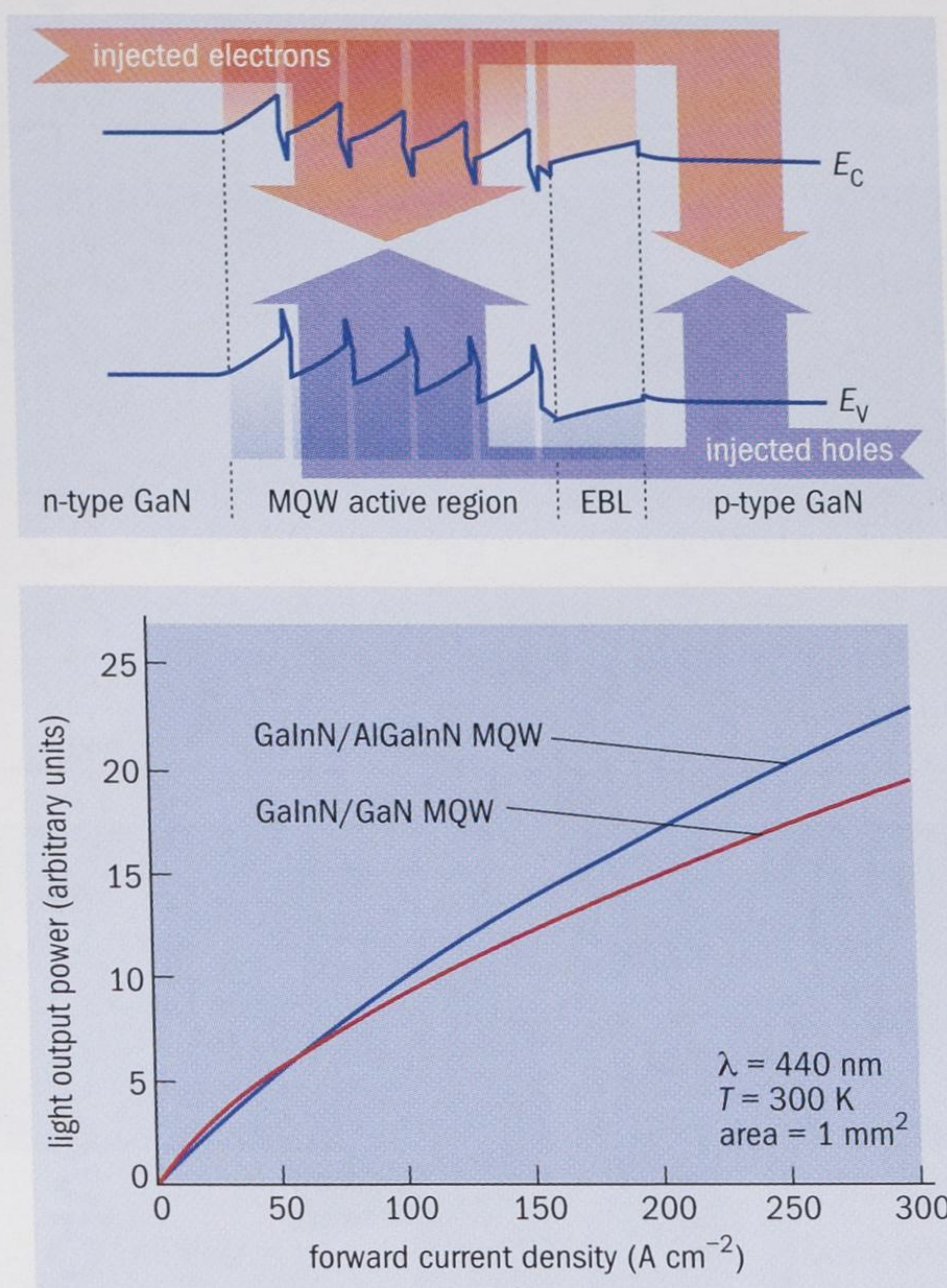


Fig. 2. (top) The researchers at Rensselaer Polytechnic Institute believe that electron escape is the main cause of LED droop. These carriers non-radiatively recombine with holes in the p-type GaN or at the p-contacts. **Fig. 3.** (bottom) LEDs with polarization-matched quantum wells and barriers deliver superior high-current performance by reducing electron leakage.

tric field than those without. This contradicts the fact that electric fields in GaN-based quantum wells actually reduce spontaneous emission. Consequently, we feel that Lumileds over-estimates the importance of Auger recombination in quantum-well LEDs at current densities close to the onset of droop.

The proof of the pudding is of course in the eating. To this end, we are now putting the results of our simulations into practice and building LEDs with AlGaInN barriers. Replacing the conventional GaN barrier with AlGaInN, and the conventional AlGaIn EBL with AlGaInN, gives us the freedom to tune bandgap and polarization, and ultimately cut the polarization mismatch and sheet charges at the active region's interfaces.

For the quantum barriers, we would grow a quaternary that has the same bandgap as GaN and matches the polarization of a typical quantum well. This is a tall order, however, because it's very difficult to grow AlGaInN layers that are rich in both indium and aluminum. However, significant improvements in device performance can be realized by cutting the polarization imbalance. Similar arguments can also be used for the EBL.

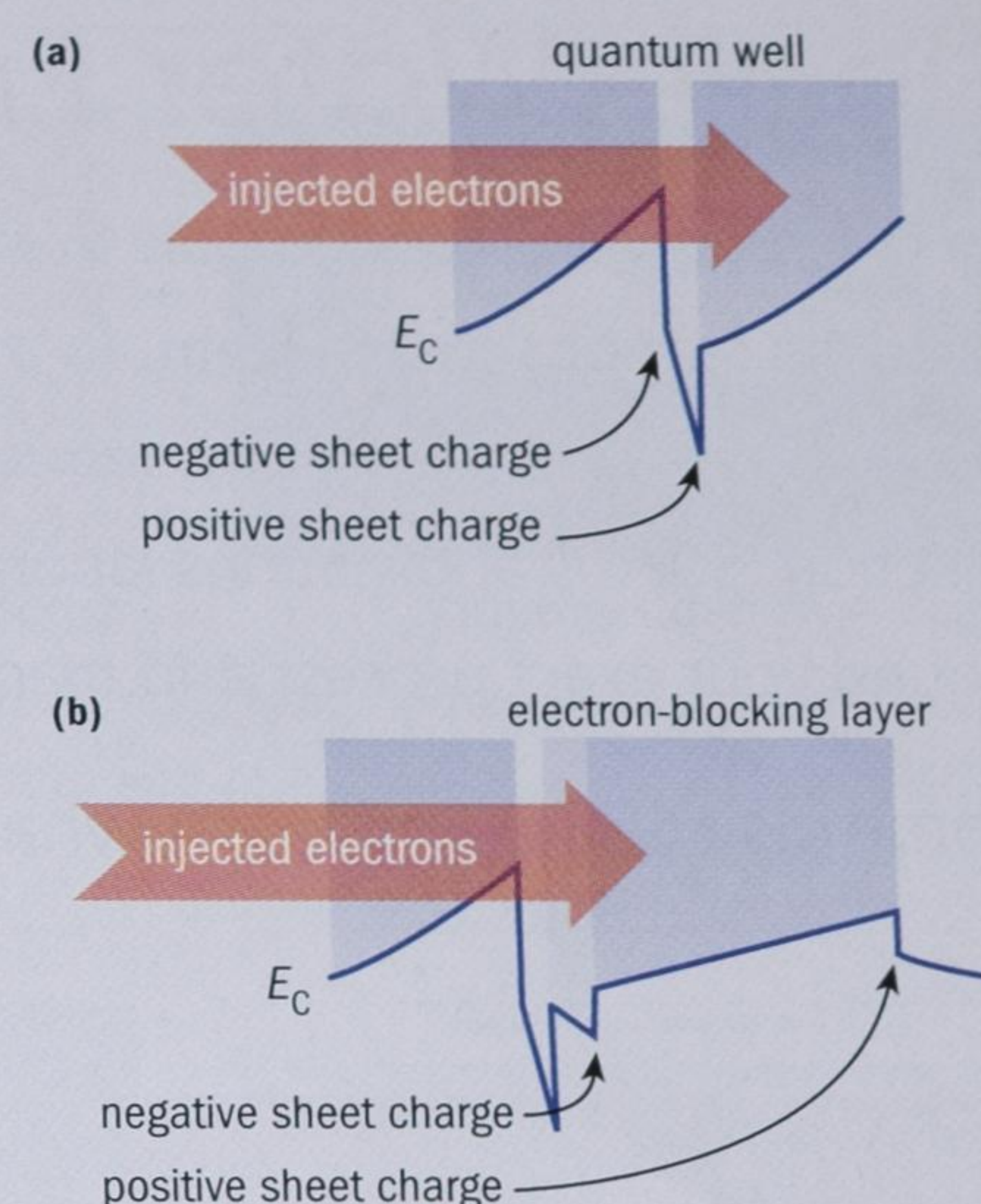
Our simulations reveal a tweak that can deliver almost all of the benefit of complete polarization matching, while using barriers and wells that only

Feeling the inner forces

GaN has a wurtzite crystal structure with polarization fields oriented along the c-direction. When LEDs are grown in this direction, large sheet charges at the interfaces are created due to differences in spontaneous polarization and strain-induced piezoelectric polarization between adjacent layers. These charges cut LED efficiency by reducing electron confinement and promoting electron leakage from the active region.

In a conventional blue LED, GaN barriers surround the GaInN quantum wells and the sheet charge is negative on the n-type side of the well. This charge repels electrons and hampers electron injection. On the p-side of the well there is a positive charge that attracts electrons and increases the probability of electron escape **(a)**.

AlGaIn electron blocking layers (EBLs) have the opposite effect. They create positive charges on the n-type side that make it easier for electrons to penetrate



this barrier **(b)**. Increasing the EBL bandgap by adding more aluminum to this layer isn't a great cure because this also increases the sheet charge.

cut the mismatch by half. The trick is to slightly reduce the bandgap of the barriers, which leads to additional carrier confinement in the active region.

Boosting wall-plug efficiency

These modifications have produced some encouraging results. Light output increased by 20% at high currents, thanks to the suppression of droop (figure 3). Forward voltage is also cut, due to a shortening of the height of the barrier to carrier injection into the quantum wells. This benefit – which is another consequence of the reduction in sheet charges surrounding the quantum well – helps to bolster wall-plug efficiency by 25%. Other benefits include a cut in wavelength shift with drive current, thanks to a lower electric-field strength in the quantum wells.

What is clear is that the growing focus on the causes of droop is paying dividends. Our understanding has improved and designs now exist that look capable of solving the problem. Commercial devices with this feature should be in the pipeline, opening up new markets including the ultimate prize – a worthy replacement for the lightbulb. ●

Further reading

- NF Gardner *et al.* 2007 *Appl. Phys. Lett.* **91** 243506.
- MH Kim *et al.* 2007 *Appl. Phys. Lett.* **91** 183507.
- MF Schubert *et al.* 2007 *Appl. Phys. Lett.* **91** 231114.
- MF Schubert *et al.* 2008 *Appl. Phys. Lett.* **93** 041102.
- YC Shen *et al.* 2007 *Appl. Phys. Lett.* **91** 141101.



About the authors

Martin Schubert (top left) is a graduate research fellow at Rensselaer Polytechnic Institute (RPI) and CTO of Troy Research Corporation.

Min Ho Kim (top right) is an employee of Samsung Electro-Mechanics Company, South Korea, and a visiting research scientist at RPI.

Jong Kyu Kim (bottom left) is research assistant professor at RPI. **E Fred Schubert** (bottom right) is Wellfleet senior constellation professor at RPI.

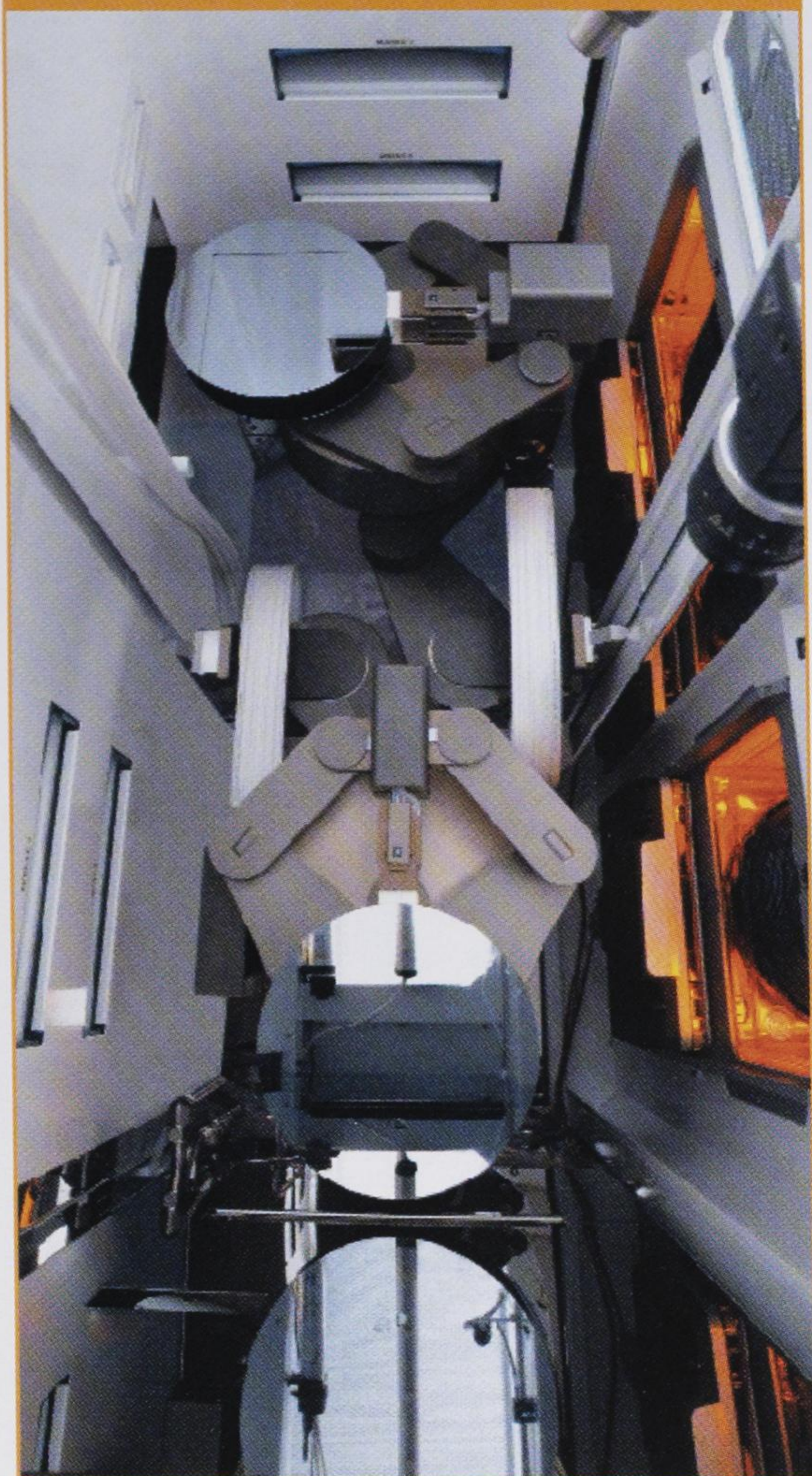
SSEC Single Wafer | wet processing

Single Wafer Processing

SSEC Systems are configurable in strip, etch and clean process stations with up to 12 stations in a system. In a Class 1 mini-environment, dual SCARA robotics can operate in any sequence to any station according to recipe selection. SSEC's applications laboratory will assist you in configuring a tool around your exact process and manufacturing requirements.

Come visit SSEC and learn what is new in single wafer processing.

Dual SCARA robotics can address all stations in any sequence.



SSEC 3301
1 Processing Station



SSEC 3303/4
3-4 Processing Stations



SSEC 3307
7 Processing Stations



SSEC 3310
10 Processing Stations

SSEC Compliance

SEMI S2-0706E Safety
SEMI S8-0705E Ergonomics
FM 4910 Materials
SECS GEM CCS 200 & 300
CE Marked
ETL Listed

Clean

99% Particle Removal Efficiency at the 88 nm, 65 nm, and 45 nm Nodes

Solvent Strip

Immersion and Single Wafer Processing

Etch

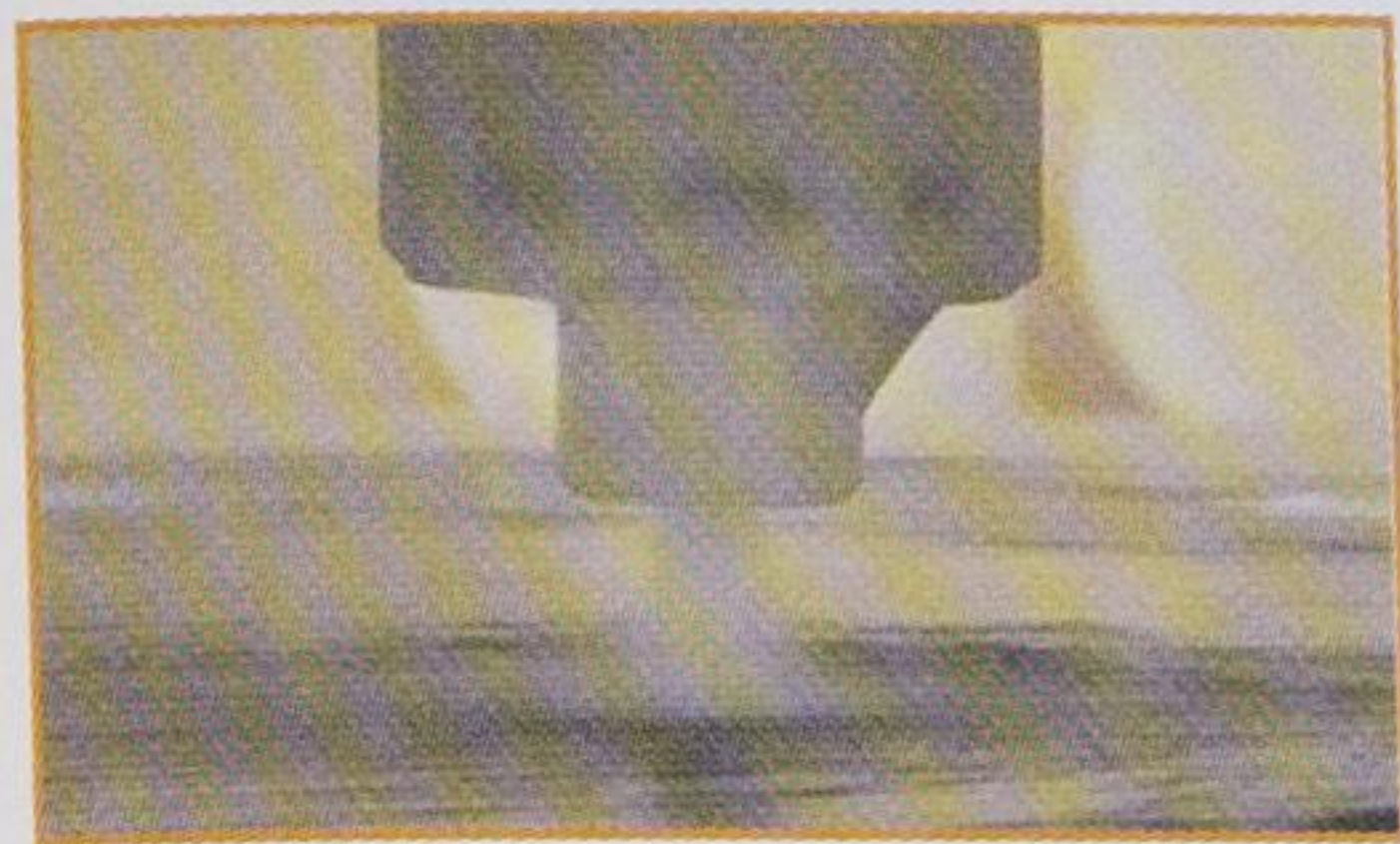
Uniform, Selective Etching on Multiple Process Levels

Coat/Develop

Photolithography Clusters

www.ssecusa.com

Solid State Equipment Corporation • Phone: 215-328-0700 • Email: info@ssecusa.com



High Velocity Scrub



Single Wafer Megasonic Scrub

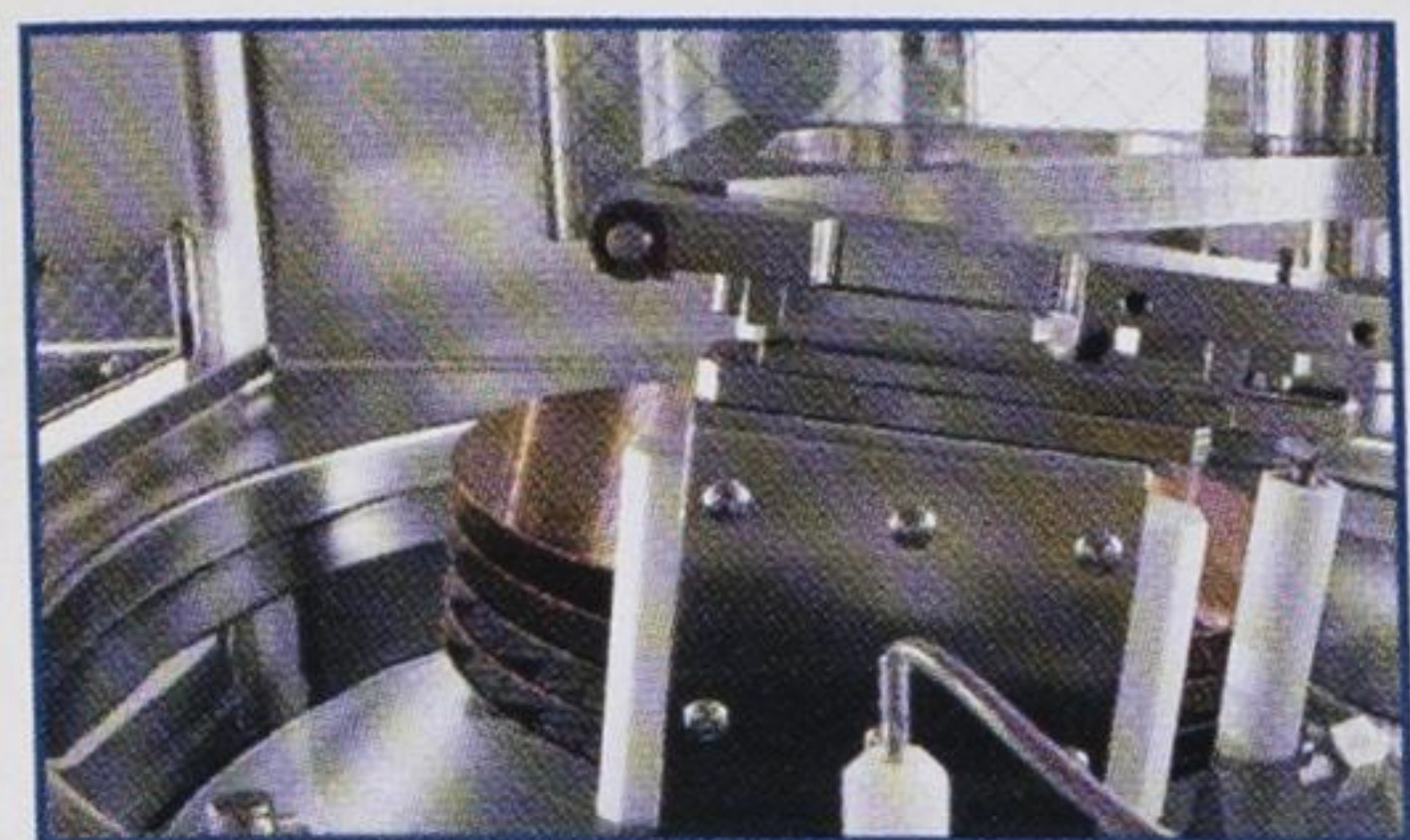


Rotary PVA Brush Scrub



Double-sided PVA Brush Scrub

For single-or double-sided particle clean, SSEC systems can be configured exactly to your cleaning requirements. Using dilute chemistries, such as SC-1 1:1:300, SSEC cleaning processors have 99% particle removal efficiency at the 88 nm, 65nm, and 45 nm nodes.



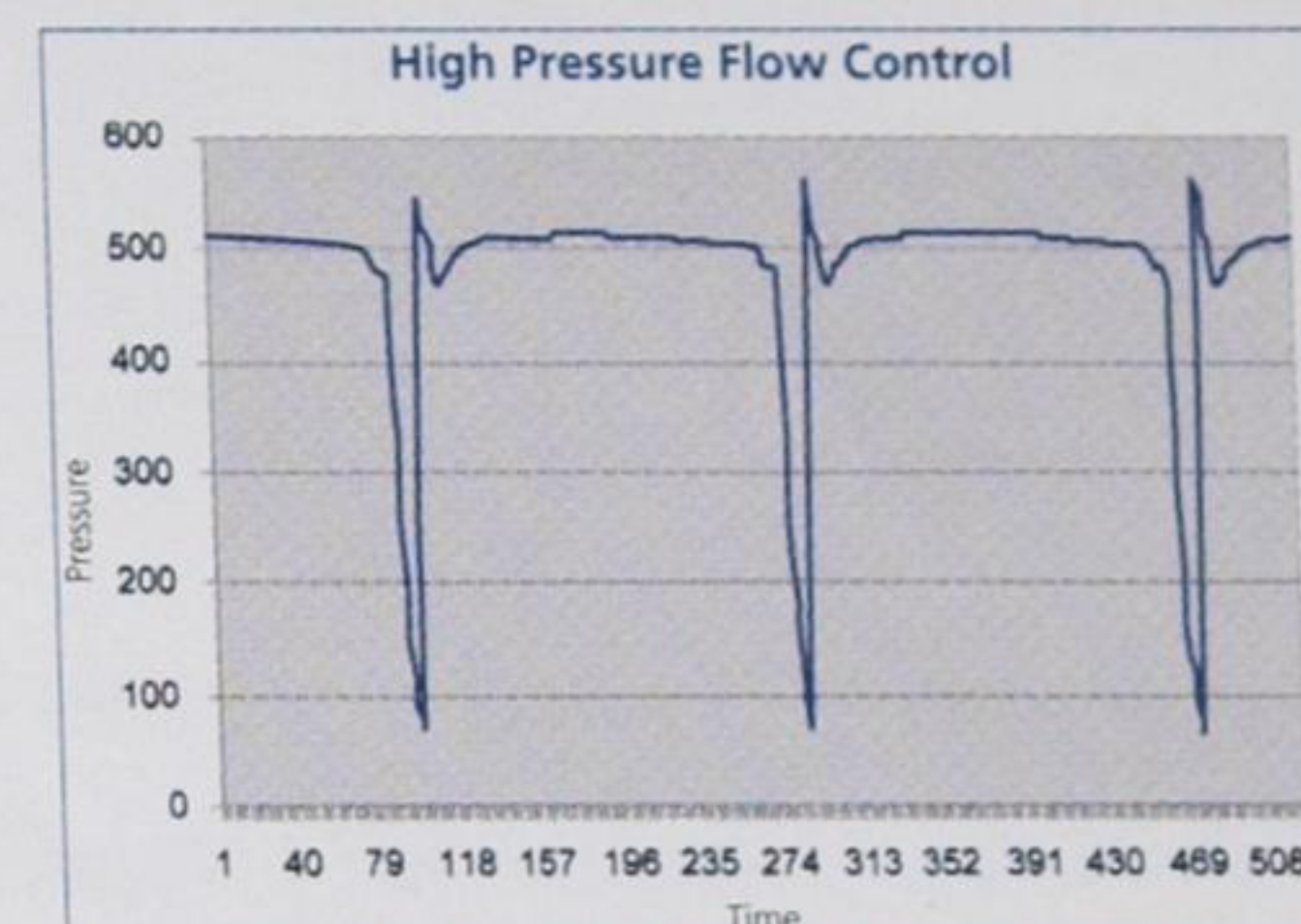
Solvent Immersion



High Pressure Spray



High Pressure Needle Dispense



Using only milliliters of solvent per wafer, SSEC solvent processors combine batch immersion and single wafer spray technology in one SEMI® safety compliant, dry-in/dry-out system. High pressure sprays are entirely under closed-loop control for flow, temperature, and dispense arm motions.



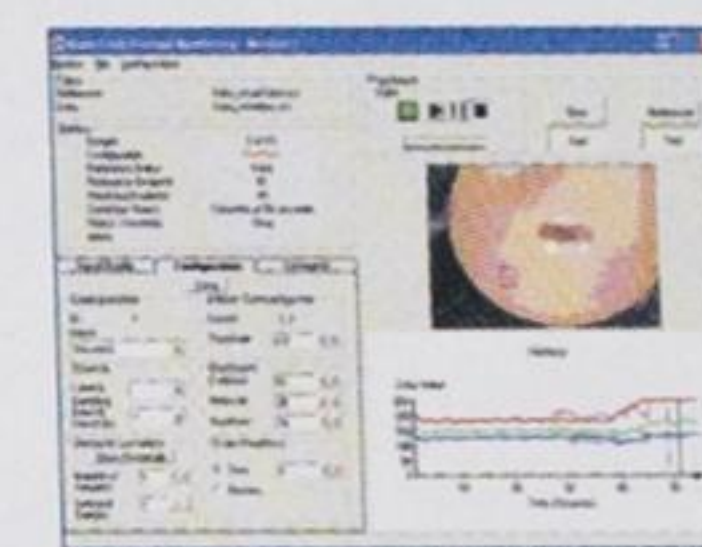
Backside/Bevel Cleaning



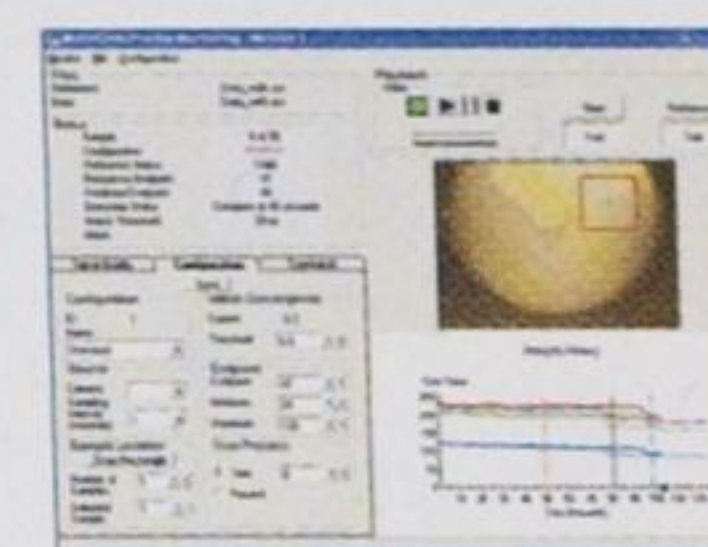
Stream Flow Etch



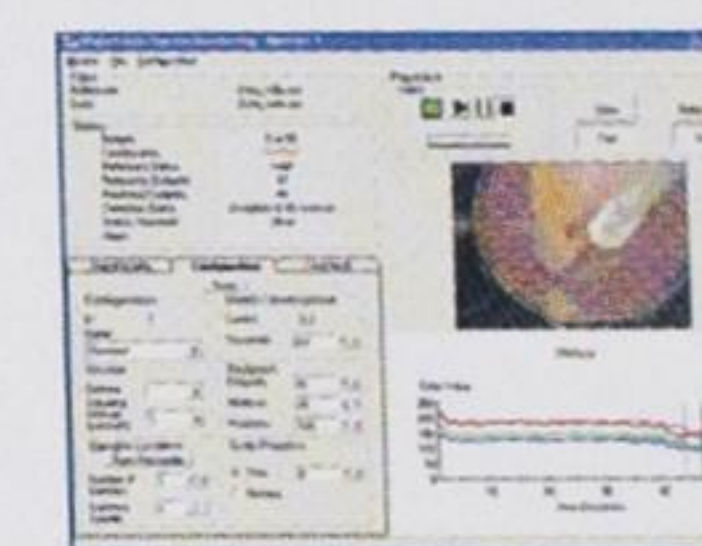
Spray Etch



Ti Etch

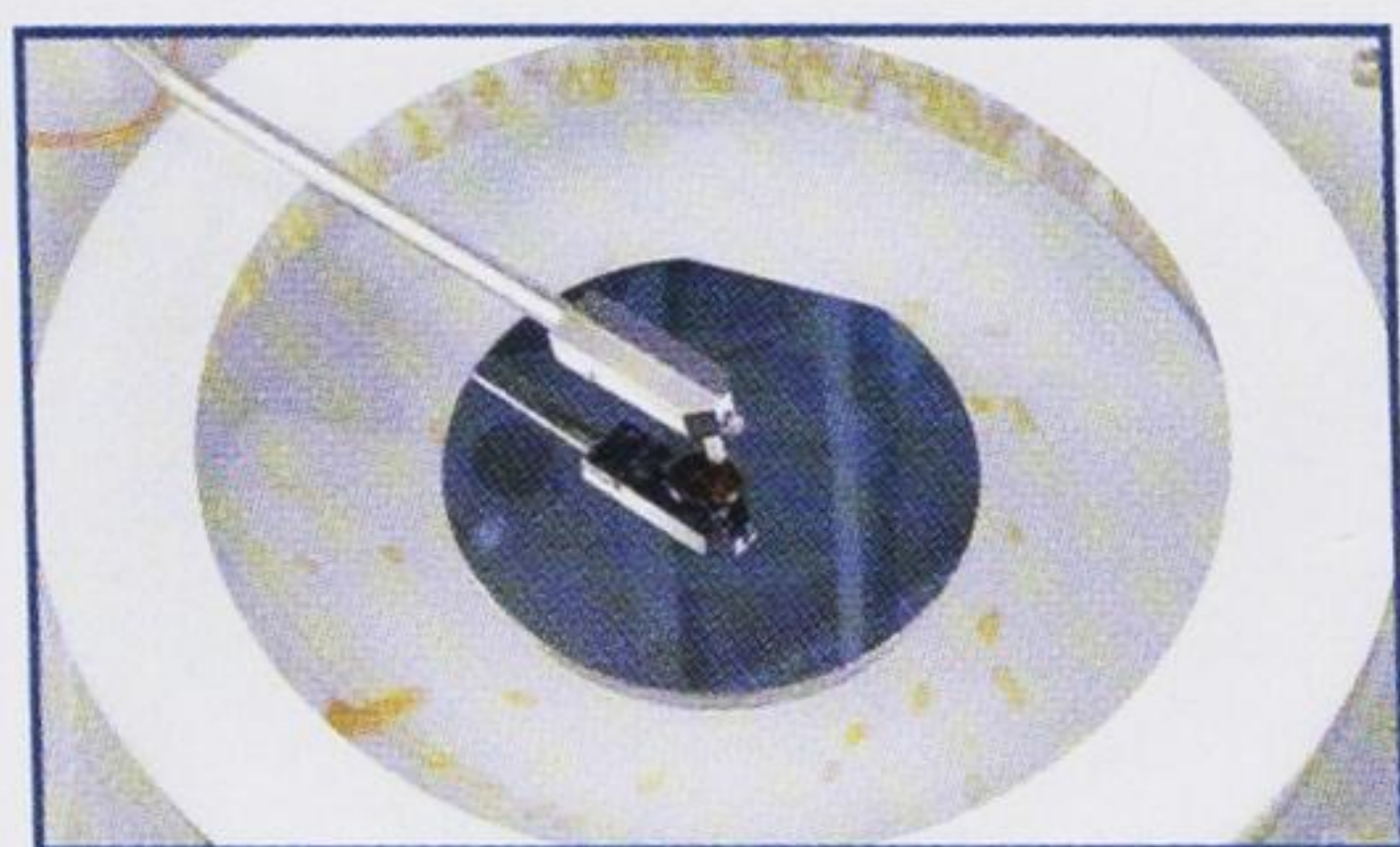


Al Etch

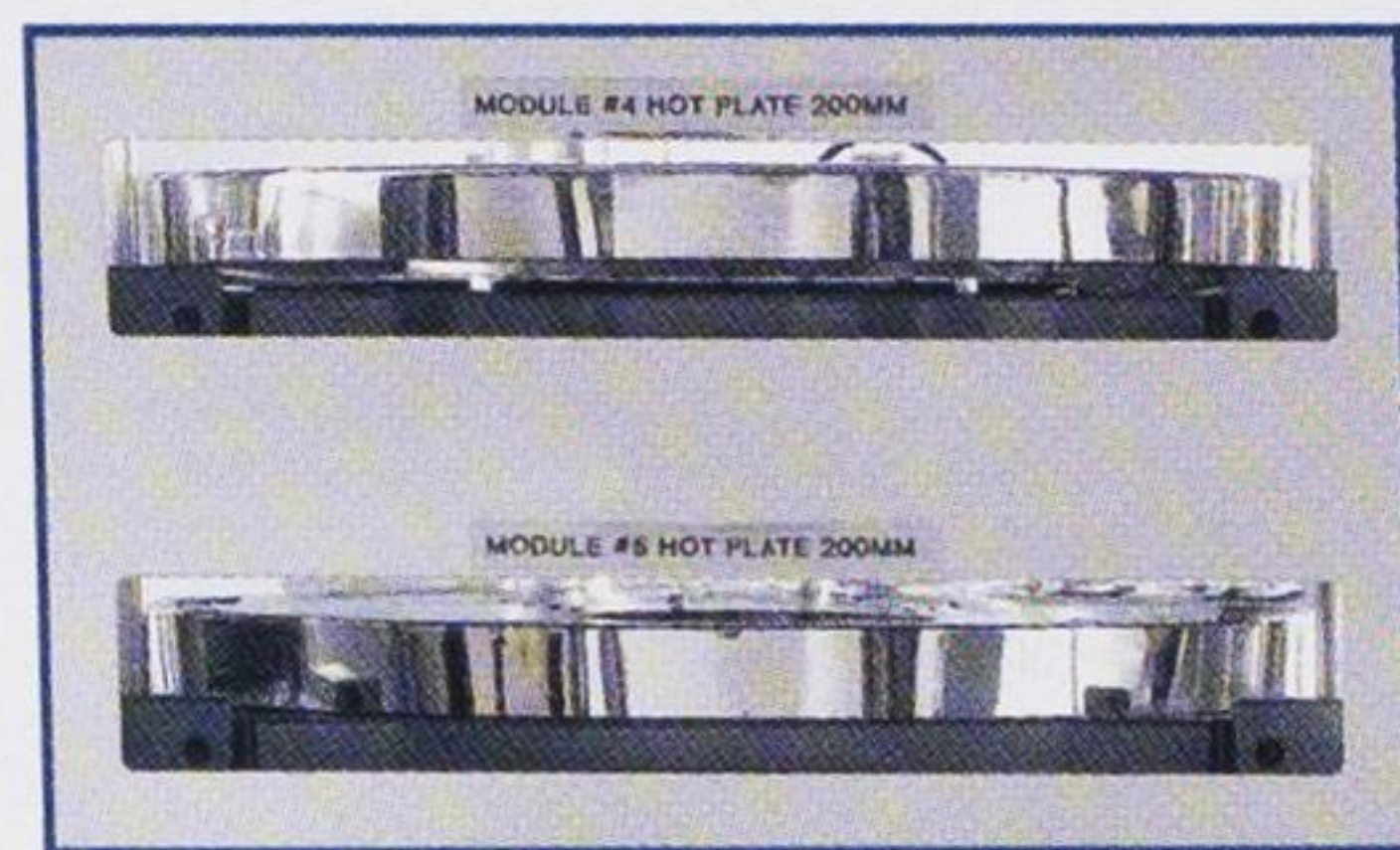


Cu Etch

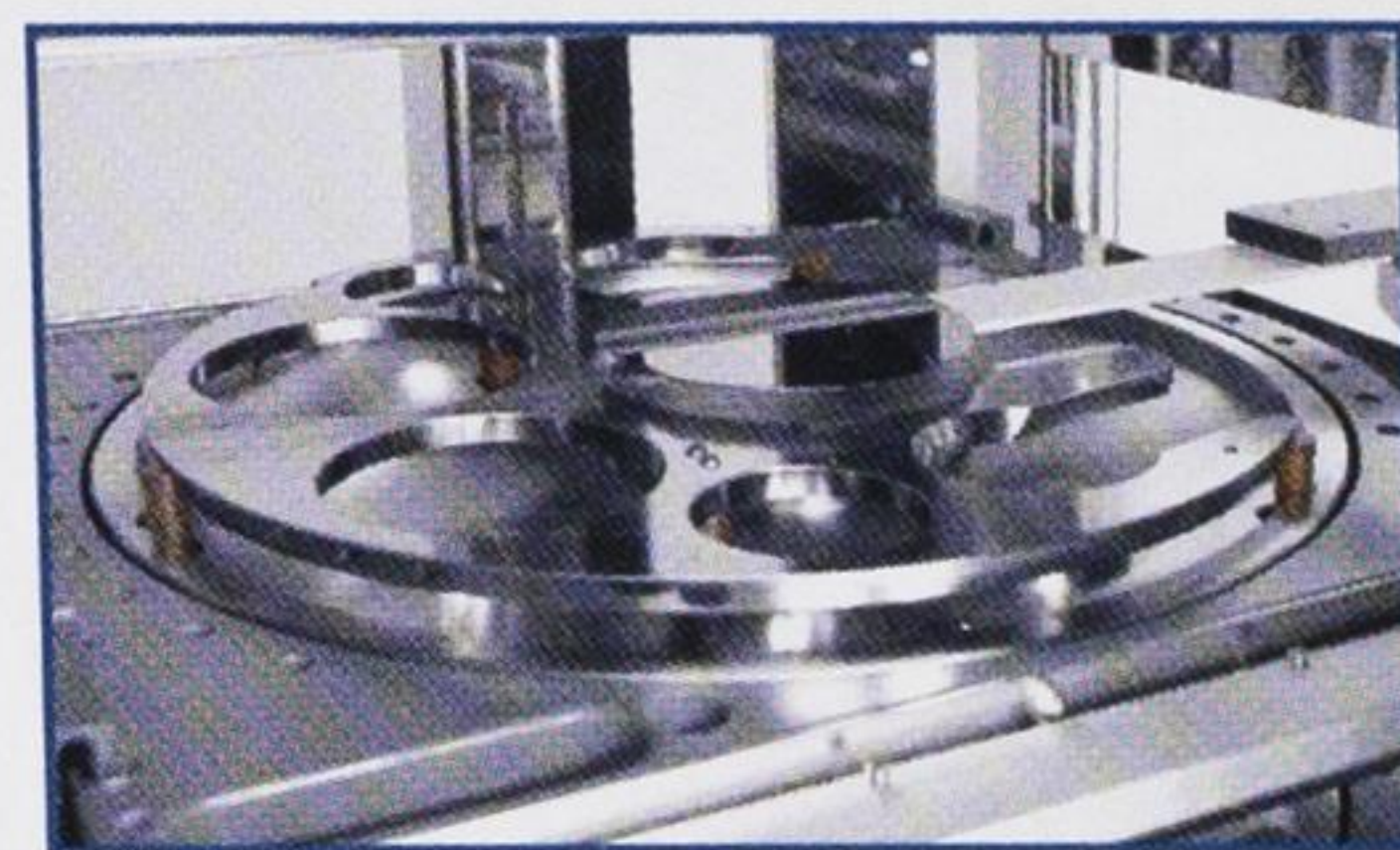
Single Wafer Wet Etch with PC Program Control over Flow Rate, Temperature and Chemical Blending by recipe with per wafer selectivity. SSEC's patent pending Chemical Collection System is over 90% effective for both single side and double sided processing. Each Wafer is processed under the careful watch of a color CCD camera for adaptive process control with SSEC's WaferChek System.



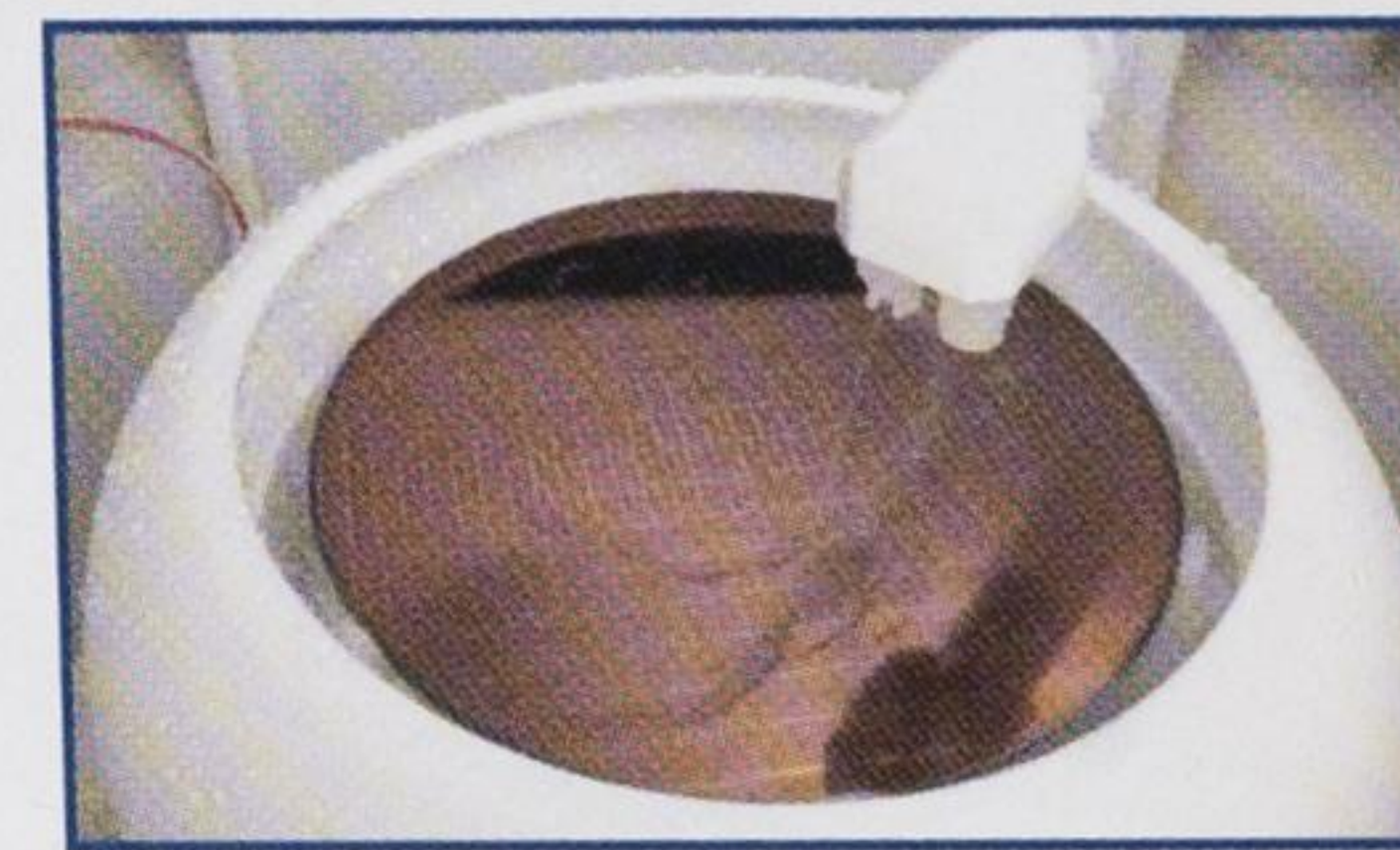
Spin Coating



Hot Plate Bake Processing



Multi Size Hot Plate



Spray Develop

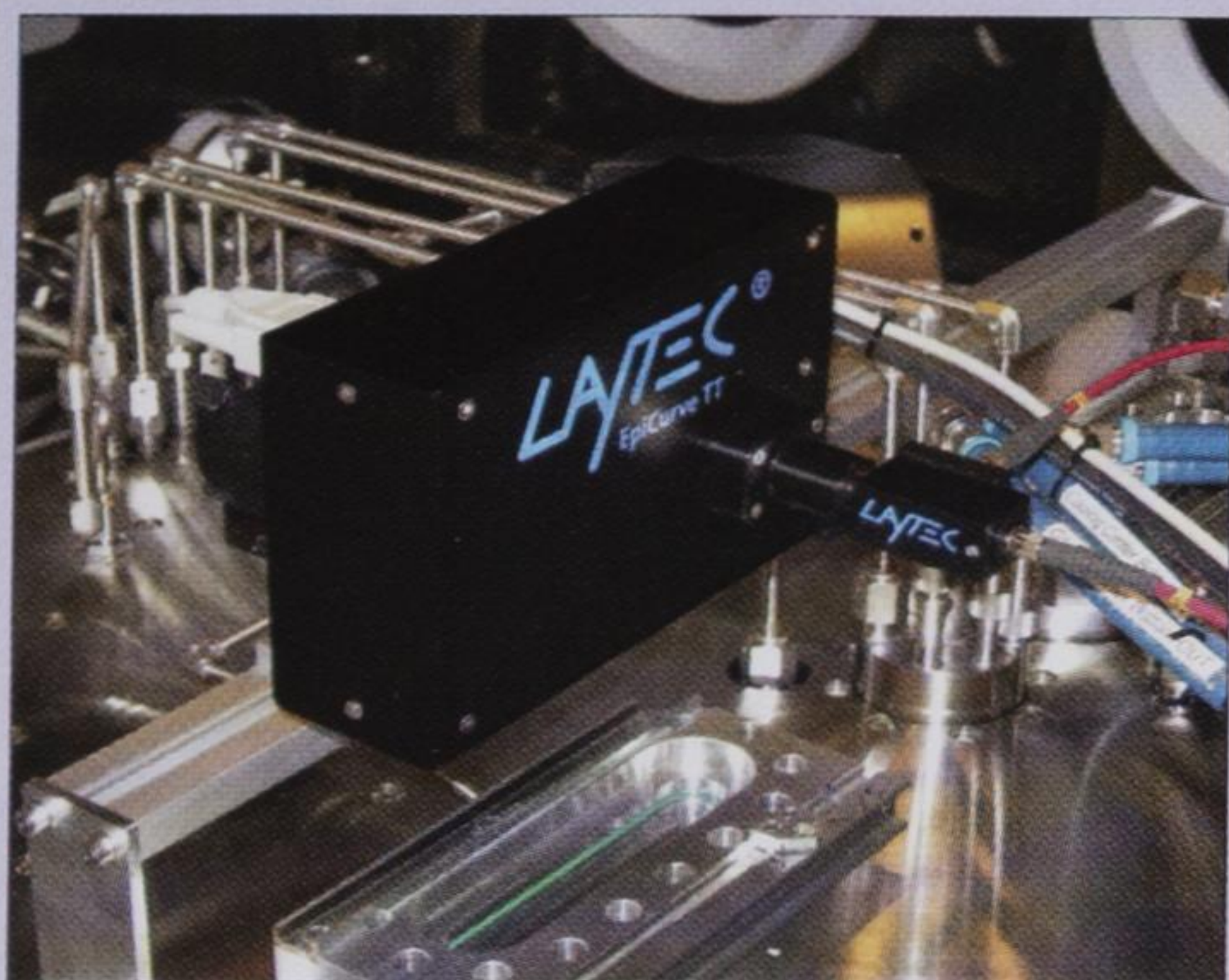
Coat and Develop processors are configured to your exact production requirements, whether for double sided MEMs Coating or Thick Resist Processing. With SSEC's Vision Driven Wafer Alignment, Coat/Develop processors can change wafer sizes with only a PC recipe change- no hardware tooling changes. All Systems are fully robotic enabling recipe driven sequencing operation.

CLASSIFIED/ PRODUCT SHOWCASE

EpiCurve[®]TT next generation

LayTec GmbH

LayTec has released a new generation of EpiCurve[®]TT sensor in a new compact design, which offers a further improved dynamic range. EpiCurve[®]TT sensors provide *in situ* measurements of wafer curvature,



temperature and growth rate for MOCVD, MBE and other thin-film applications.

Contact LayTec GmbH
Tel +49 30 39 800 800
E-mail info@laytec.de
Web www.laytec.de

NEW Versatile Cryogenic Probe Stations

Lake Shore Cryotronics, Inc

Lake Shore's redesigned line of cryogenic micro-manipulated probe stations includes table-top, field upgradeable, superconducting and electromagnet-based, full 4 inch wafer, and closed cycle refrigerator based probe stations. By providing in-field upgrade paths, these new designs are more flexible and expandable to keep up with demanding, ever-changing research requirements. A wide selection of options and accessories allow Lake Shore probe stations to meet your specific measurement applications while working within your budget.



Contact Lake Shore Cryotronics
Tel +1 614 891 2244
E-mail info@lakeshore.com
Web www.lakeshore.com

Ultra-High Purity Hydrogen Generator

Proton Energy Systems

HOGEN[®] hydrogen generators are a safe and cost-effective way to provide ultra-high purity hydrogen gas to compound semiconductor applications. HOGEN[®] hydrogen generation systems are designed to specifically meet the demanding requirements of the semiconductor manufacturing environment while providing an attractive economic payback, increased safety through lower onsite gas inventory and a smaller footprint by requiring a fraction of the floor space needed by cylinders. To learn more about our products:



Contact Proton Energy Systems
Tel +01 203 949 8697
E-mail customerservice@protonenergy.com
Web www.protonenergy.com

ETH

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory Engineer or Technician (Chemistry or Physics background)

with experience of semiconductor component manufacturing in a clean room environment.

We are looking for a Laboratory Engineer or Technician, ideally from the field of chemistry or physics, to contribute to the process technology for semiconductor components in both the Department's own clean room and in the ETH's Semiconductor Development Centre (FIRST Lab). Process and work experience in a clean room environment is desirable but training of suitably qualified applicants will also be considered.

Job Description:

The main activity involves the support, development and independent execution of technical processes for the manufacture of electronic or optoelectronic components in a clean room. Examples include Heterostructure Bipolar and Field Effect Transistors, Diode Lasers, Photonic Crystals, as well as the assembly of RF and microwave components and networks. Typical process technologies include Optical and Electron Beam Lithography, Dry and Wet Etching, Metal and Dielectric Deposition, Wafer Lapping and Chip Bonding. The work includes maintenance of the relevant technical equipment.

Profile:

Applicants (male or female) should have completed their formal training i.e. at a University of Applied Science, as a Laboratory Engineer or Technician with a background in Chemistry or Physics and have a minimum of two years experience of working in this environment. Practical experience for work in a clean room environment would be advantageous. Experience with operating and servicing of technical equipment (evaporation, dry etching, deposition, etc.) as well as with chemical processes is important. Applicants should be self-motivated and able to work reliably without constant supervision. You must be a team player with good communication skills. Good German and basic English is a prerequisite.

What we offer:

- Varied and challenging team work in an international research environment at the forefront of research;
- The opportunity to help develop diverse new technologies in state-of-the-art clean rooms;
- Interesting and stimulating team work in collaboration with young researchers;
- On-the-Job Training with opportunities to develop one's profile in advanced fields of application.

The D-ITET is one of the largest departments at the Swiss Federal Institute of Technology Zurich with more than 400 employees, an excellent research infrastructure and access to the ETH Zurich's world-class Semiconductor Development Centre FIRST (www.first.ethz.ch). The Department, its Professors and Students are internationally renowned for their pioneering discoveries in the areas of semiconductor technology, information theory, signal processing, control technology, electromagnetics and IT.

Your application:

Please send your complete application documents to Professor Colombo R. Bolognesi, Bolognesi@ifh.ee.ethz.ch, with cc. to Schuhbeck@ifh.ee.ethz.ch.

IQE

www.iqep.com

Senior MOCVD Process Engineer – Solar Cells Cardiff (UK), Bethlehem (PA) or Somerset (NJ)

IQE plc is this year celebrating its twentieth anniversary as the leading global supplier of advanced semiconductor offering the widest product range of any independent global wafer supplier.

The company is in the process of enhancing its product portfolio with a focus on GaAs based materials for Concentrator Photovoltaic (CPV) applications and is seeking a Senior MOCVD Process Engineer to play an active role in further establishing IQE's position as a key player in the rapidly growing solar markets.

IQE operates six manufacturing facilities; two in Cardiff and one in Milton Keynes in the UK; two more in Bethlehem, Pennsylvania and Somerset, New Jersey in the USA; and one in Singapore. The Group also has 11 sales offices located in major economic centres worldwide. The group's global headquarters is in Cardiff.

Key responsibilities

MOCVD growth optimisation: Your knowledge and experience of multi-junction solar cells based on Ge & GaAs substrates will allow you to make a major contribution to IQE's internal processes whilst adding value to our partners and customers.

Device Development: Working closely with IQE's existing technical and engineering resources you will play a key role in helping our partners and customers develop high efficiency, low cost CPV solutions

Process Engineering: Your technical expertise coupled with a strong business sense will help IQE deliver solar products to the high standards of quality, reliability and service that customers have come to expect from IQE.

The candidate

Excellent first degree in a relevant area such as Physics, material science or Electrical/Electronic Engineering. A second degree (Masters or Ph.D) would be advantageous.

A minimum of three years experience in epitaxial growth of III-V materials, ideally by MOCVD, that has been gained in a fast moving commercial environment. A knowledge of device processing, particularly for multi-junction solar cells, would be an advantage.

IQE has manufacturing sites in Europe, Asia and the USA with MOCVD capabilities at two locations in North America (Pennsylvania and New Jersey) as well as its site in Cardiff, UK. This role could be located at any of these sites.

If you have the skills and experience to join a world leader and wish to be considered for this exciting position please forward your resume/CV to:

Human Resources, IQE plc, Pascal Close, Cardiff, United Kingdom, CF3 0LW
personnel@iqep.com

RFMD gives the BiFET a new twist

RF Micro Devices' BiFET technology offers a cost-effective route to extending HBT capabilities. JFETs can be created through the growth of two extra layers, an additional mask and just one more etch, say **Brian Moser, William Clausen, David Vines** and **Walt Wohlmuth** from the company.

Handset manufacturers operate in a very competitive environment. Success hinges on the release of new models with ever more features, which must be crammed into sleeker designs catering for the latest fashions. In this sector innovation is paramount, alongside the sourcing of smaller components that offer more bang for your buck.

At RF Micro Devices (RFMD) we are addressing the handset manufacturers' wish-list with a unique BiFET process technology that delivers a complex, yet highly integrated and compact front-end module (FEM). The mobile's component count can then be reduced without sacrificing the number of features, their quality or the battery life.

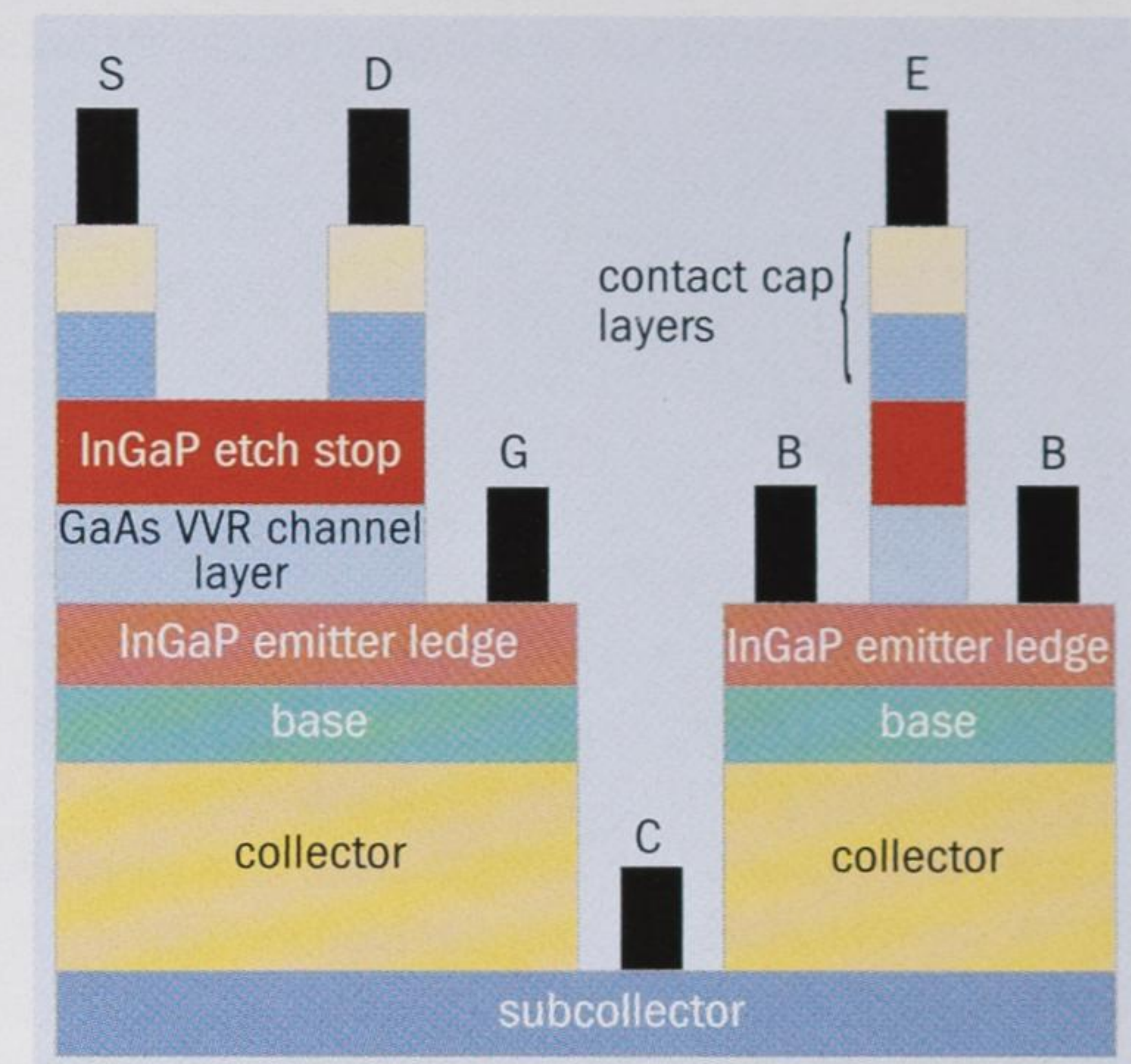
Handset designers prefer to use FEMs with control lines operating directly off the transceiver's lower voltages and currents. Our BiFET technology fulfills this and can integrate new DC circuits – including voltage regulators, analog bias control and low-leakage logic – directly into the FEM. This increases functionality, cuts the number of supporting external components on the phone's board and ultimately reduces this handset's bill of materials.

We are by no means the only BiFET developer. Approaches that integrate a PHEMT below the HBT have been pioneered by Anadigics, TriQuint and WIN Semiconductors, while Skyworks has merged a MESFET into the HBT emitter layers. But in every case, the addition of a second device to the existing HBT process makes manufacturing more expensive and complex.

We minimize this extra complexity in the most cost-effective way with our unique BiFET process. Our advantage stems from the way that we integrate a junction FET (JFET) into the emitter layers of the HBT's epitaxial structure. The JFET acts as a voltage variable resistor (VVR) and we often describe the device by this name because it reflects the application.

An overriding goal has dominated our BiFET development – reducing the additional process steps and changes required to add a FET to the existing InGaP/GaAs HBT epitaxial structure to ensure that our BiFETs manufacturing costs are only slightly higher than the traditional HBT-only process.

Our BiFET's epitaxial structure contains just two more layers than our HBT-only process – an InGaP etch stop and GaAs channel – and both are inserted between the cap and the InGaP emitter



Feature-rich mobile phones (left) could benefit from RF Micro Devices' BiFET process, which can increase the complexity of front-end modules without compromising compactness. **Fig. 1.** (above) RF Micro Devices' BiFET process unites a conventional HBT structure (right) with a JFET (left) that acts as a voltage variable resistor. This differs from the approaches used by Anadigics, TriQuint and WIN Semiconductors that integrate the PHEMT below the HBT, and Skyworks technology that merges a MESFET into the HBT emitter layers.

(figure 1). This epitaxial design has already been tried by researchers at the University of Illinois at Urbana-Champaign, but they restricted their studies to HBT devices. In that case the new design had no detrimental impact on transistor performance.

The VVR is notably different from other FETs that feature in BiFET technologies. There is no gate metal over the channel region, and a p-n heterojunction controls conduction between source and drain regions. The VVR's back-gate contact metal comes from the HBT base metal.

We isolate the source and drain with a wet recess etch to the InGaP etch-stop layer, and no gate metal deposition steps are needed for device fabrication. Identical metal layers provide contacts to the HBT emitter mesa and the source and drain contacts. The only additions to our InGaP HBT manufacturing process are another mask layer and one etch step.

Our tests show that no detrimental effects on BiFET HBT performance have resulted from the

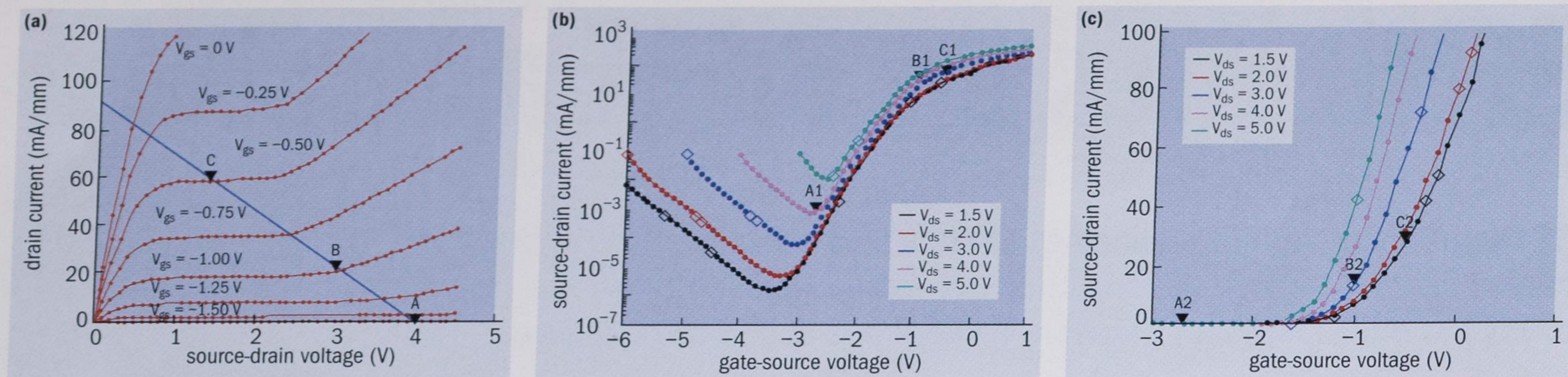


Fig. 2. The JFETs that form part of RF Micro Devices' BiFET technology are used as a voltage variable resistor (VVR). The load line (a) helps to illustrate how the VVR device might be used in a circuit application. Points A, A1 and A2 in the graphs (a) (b) and (c) show that this device has a drain current of $0.7 \mu\text{A}/\text{mm}$ in its off-state.

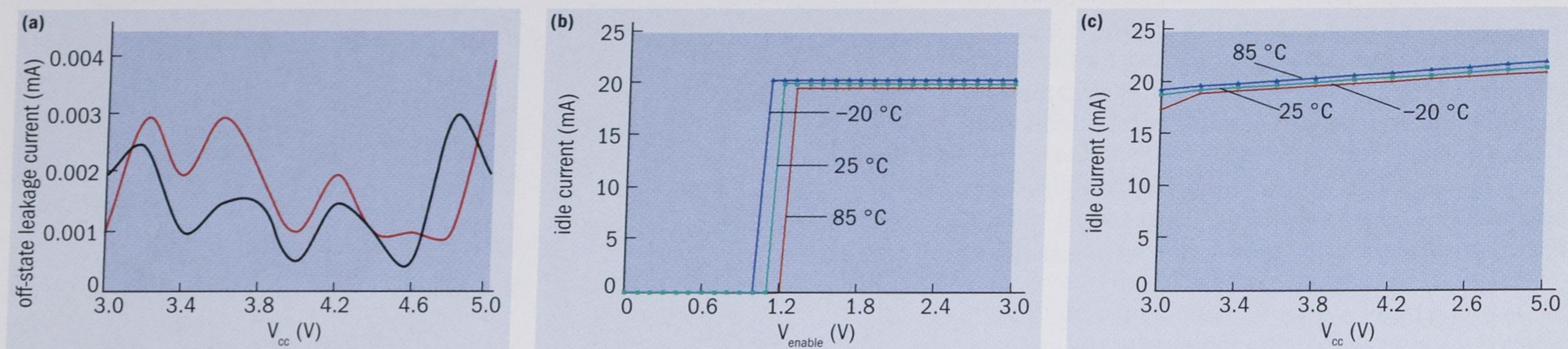


Fig. 3. An FEM with a digitally enabled internal regulator can be created from a regulator and logic. These data show the first-stage idle current of a two-stage WCDMA PA plus the current required for the bias and logic networks ($I_{cq1} + I_{cq2}$). The off-state ($V_{\text{enable}} = 0, 0.5 \text{ V}$) FEM leakage is less than $5 \mu\text{A}$ at room temperature (a). The PA is fully biased when the V_{enable} voltage exceeds 1.4 V , which makes it compatible with transceiver logic (b). Buffering the V_{enable} voltage with a double inverter creates a sharpened V_{enable} voltage, which switches at $\sim 1.2 \text{ V}$ (V_{be}). This means that the voltage output of the regulator is either on or off. The voltage output of the regulator is flat with V_{cc} as well, with most idle current change resulting from variability in the bias network used between the regulator output and the RF transistor (c).

incorporation of the VVR. Gummel plots reveal that the BiFETs current gain, β , matches that of the standalone device until the HBTs deliver a high collector current. Plots of the HBT collector current as a function of collector-emitter voltage are very similar for both processes, and small signal results show little difference between cut-off frequency and maximum oscillation frequency. However, the BiFET HBT has a lower emitter-base capacitance and the two additional epilayers produce an expected increase in emitter resistance, which is double that of the standalone HBT.

Of course, the ultimate test for any device is the performance that it delivers in its intended application. We've checked this out by comparing the performance of WCDMA power amplifiers incorporating HBTs from our standalone process and the new BiFET process. We intentionally avoided taking advantage of any of the new VVR devices and retained the original InGaP/GaAs HBT process layout to carry out this evaluation. Keeping with this philosophy, the parts from the new and original processes were built to be as consistent as possible.

Performance was unaffected, according to measurements taken over temperature, bias condition, power level and V_{cc} (the DC voltage applied to the collector of multiple HBTs in a circuit). Encouragingly, characteristics such as power-added efficiency, adjacent channel power and gain were all within the part-

to-part variation of the HBT-only process.

Our VVR's current-voltage characteristics are shown in figure 2. We have found that $0.7 \mu\text{A}/\text{mm}$ flows in the VVR when it is in its off state. When the drain-source voltage hits 4 V , leakage current must be kept low to avoid undesirable currents in the bias circuit. The current can be minimized by fine-tuning the manufacturing process and epitaxial structure.

High-yield manufacturing processes must account for and manage variation in VVR device performance and its effect on the circuit. Our BiFET design is notable for its absence of a gate metal above the channel, which creates a VVR device performance that strongly depends on epilayer thicknesses and doping concentrations. Our engineers are driving down these variations as the process matures and will monitor the changes in VVR that are caused by fluctuations in epilayer thickness and doping across the wafer and between runs.

We have also modeled device behavior (see box "Modeling the VVR transistor") to understand how our VVR behaves and how it can be integrated into more-complex circuits before production.

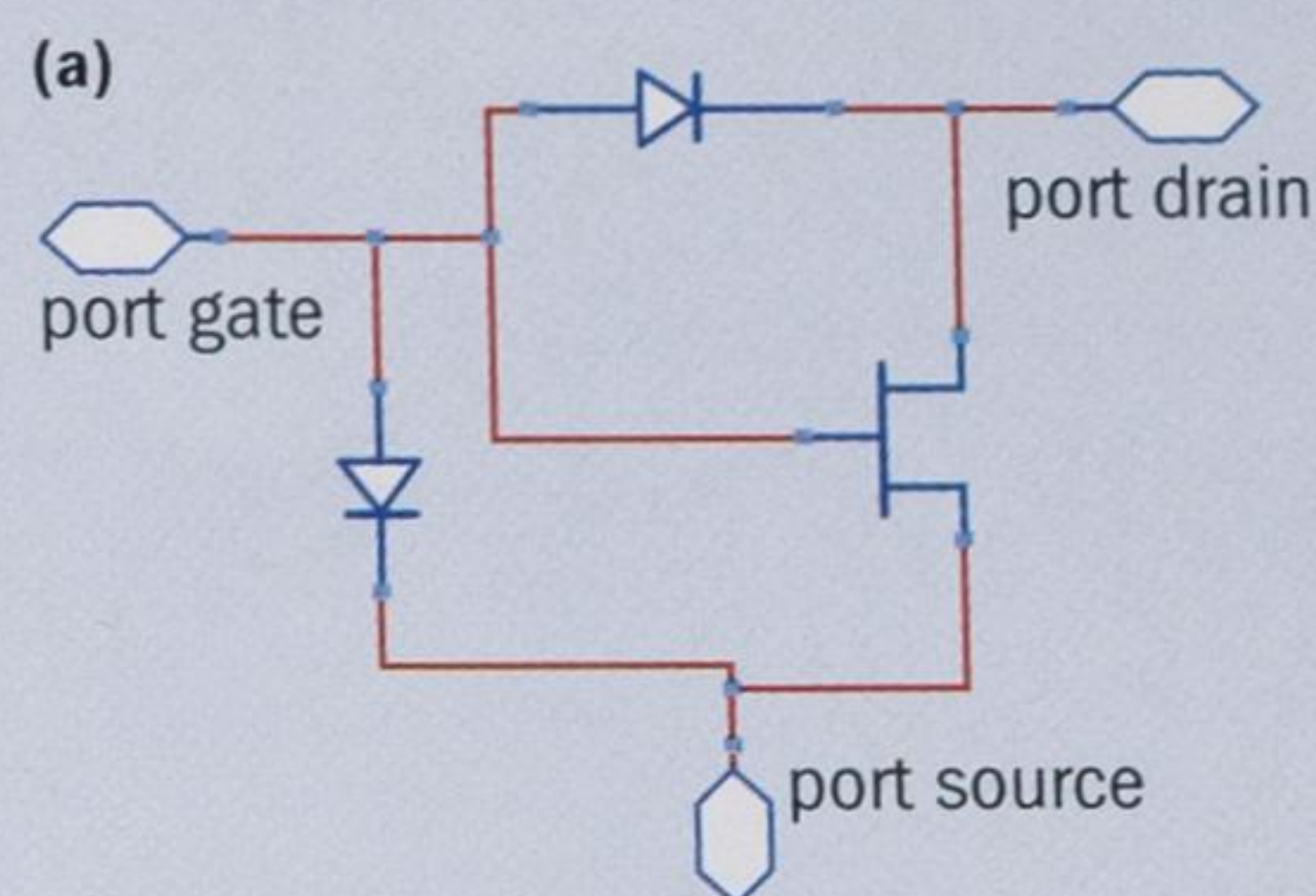
The WCDMA FEMs that we have developed will offer great value to our customers thanks to the incorporation of internal voltage regulators made from BiFETs. Ideally, internal voltage regulator circuits should deliver a constant voltage over all conditions, including variations in battery output,

Modeling the VVR transistor

The simulation that RF Micro Devices (RFMD) uses to predict the behavior of its VVR consists of two parts – one for DC operation and another for RF.

It's essential that the VVR model accurately predicts DC performance in all areas of operation: transient effects in bias switching applications, temperature variation, drain and source-width scaling, and threshold scalability. The modeling has been performed with a particular circuit topology **(a)** and in normal use its behavior is similar to a JFET **(b)**. This allows a modified PHEMT DC model structure to be employed that simulates current in the linear and active regions, which includes an accurate model for the sub-threshold region.

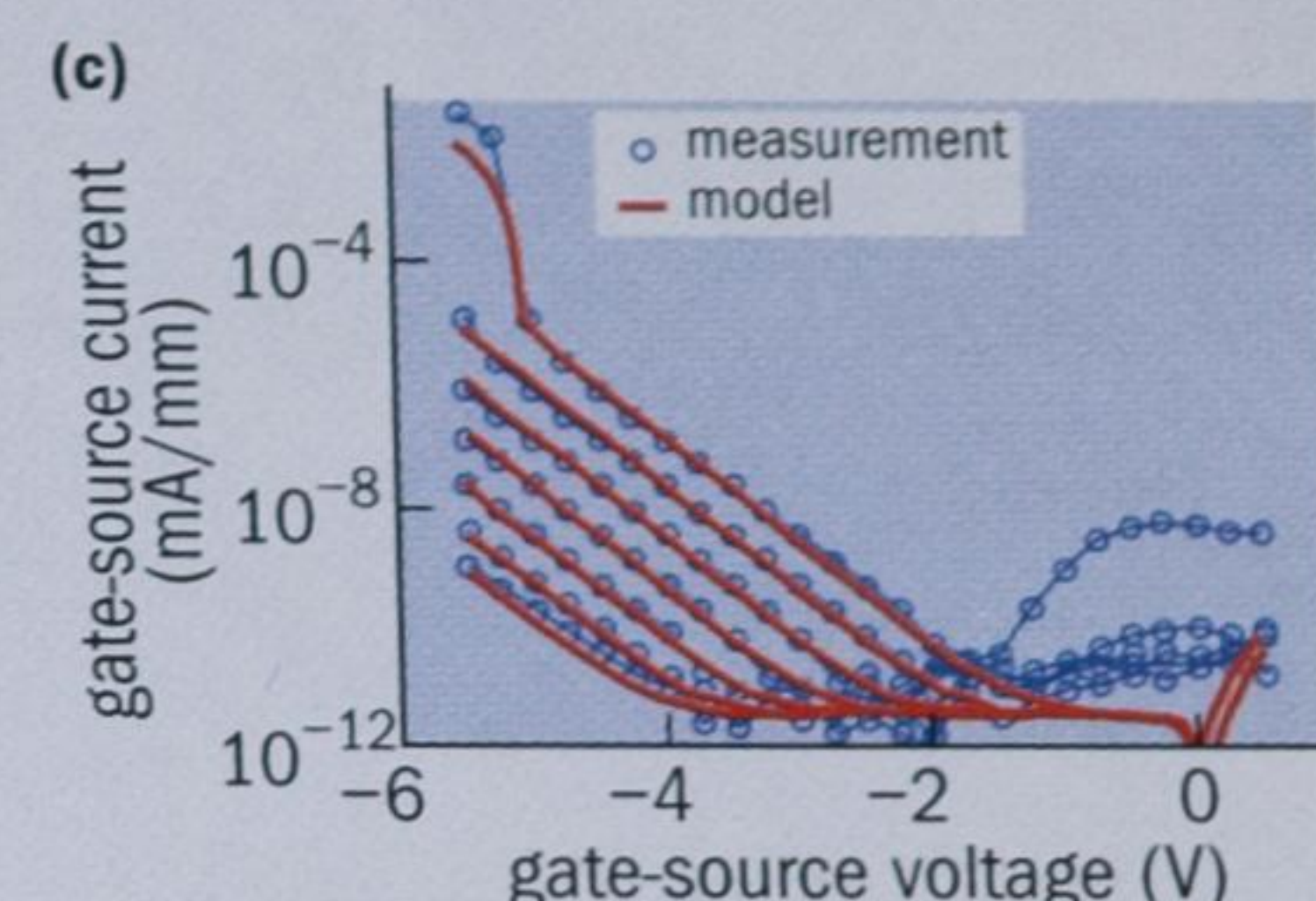
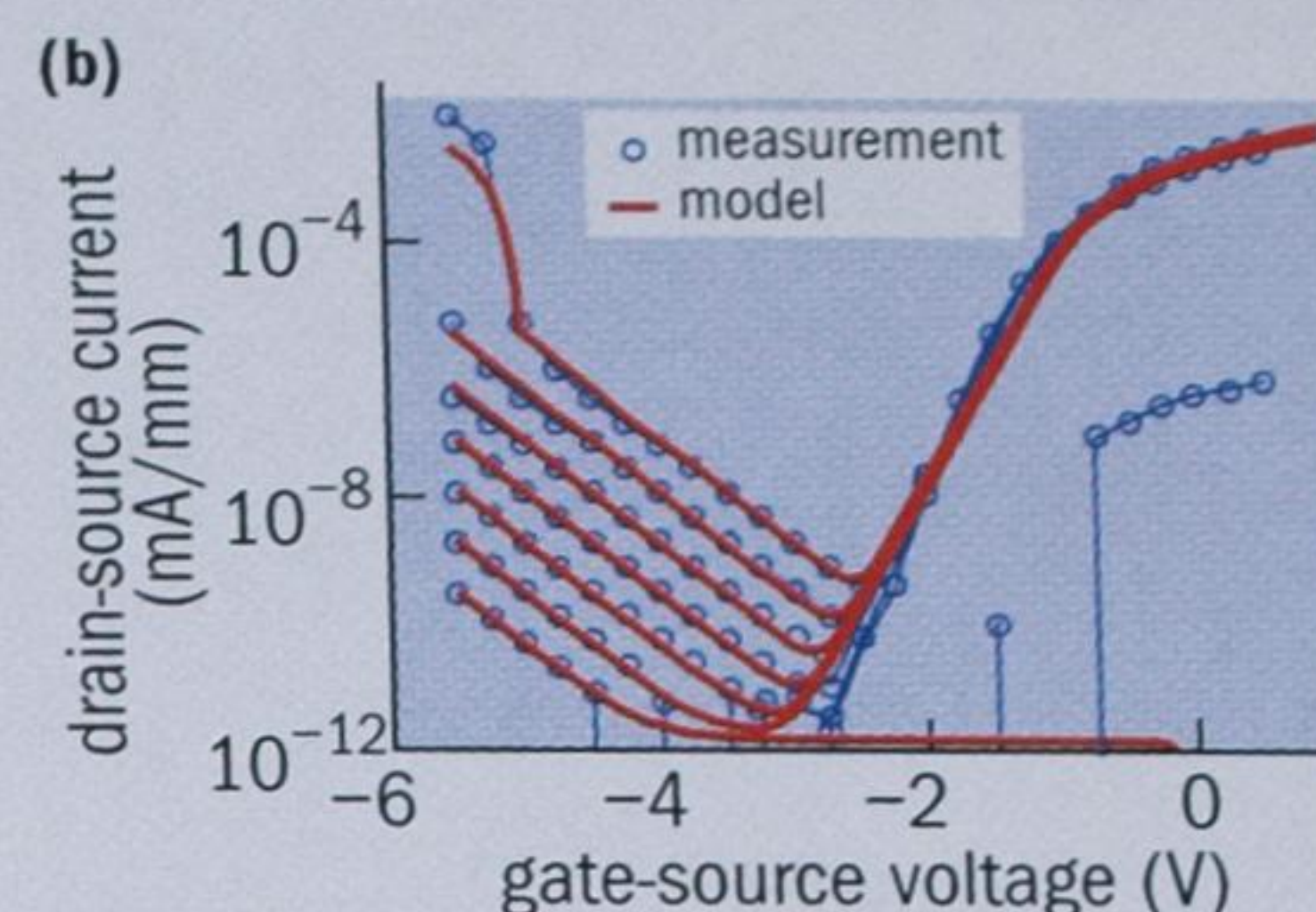
This model can do more than just predict the drain current when the transistor is turned on – it can also calculate the leakage current when the device is pinched off. The slope of the sub-threshold region is partly used to predict



the leakage current, which is also determined by the region where gate-to-drain leakage dominates.

The leakage is determined by the sub-threshold drain-to-source current and the reverse gate-to-drain current **(b)**.

If the model is to replicate reality, then increases in the potentials between the drain and gate must produce an increasing positive drain current, and a negative gate current that also increases. Both of these conditions are met **(b, c)** with a model that features an additional diode to cater for reverse leakage. This includes drain-to-source field dependence over temperature, which is modeled with a high reverse saturation current and an



ideality factor.

The forward-biased gate-to-source response employs separate diode models for the two ideality regions. Using two separate diode models for the gate to source and gate to drain has an important implication: accurate measurements are needed to differentiate the current from all three ports. It is important not to assume that all of the current is flowing through to the source node.

The model's RF portion is based on a model developed by Agilent Technologies called "EEHEMT", which forms part of the company's Advanced Design Systems' simulation software. RFMD has adapted this model for its VVR.

The customized software tool offers a greater degree of freedom in fitting capacitances, which are independent of the DC model.

Fitting a charge model to the VVR is particularly difficult, due to the depletion region's shape in the GaAs channel. The p-n heterojunction causes the depletion region in the VVR to be formed in the n-type InGaP emitter layer. Since the device's gate is the base-emitter p-n junction, the gate diode forward conducts at emitter-base voltages greater than 1 V. This prevents the transconductance in the VVR from saturating and stops an increase in gate-source capacitance that can result from base-emitter diffusion capacitance.

operating environment and load. BiFET-based internal regulators are configured in a different way, however, and must balance trade-offs to deliver a constant voltage over a limited range of conditions.

We are aware that some of our VVR device characteristics are not ideal. The VVR's low transconductance and drain cut-off current, and its "scalability" with gate width, mean that the easiest way to improve circuit performance is to place larger VVRs where more current is required. However, this goes against the trend of greater miniaturization.

Internal voltage regulator output is strongly influenced by the VVR's threshold voltage. Variations in this voltage can be minimized by summing two outputs: the regulated voltage and another output that is inversely proportional to the threshold voltage. A near constant regulated voltage results, which tracks the threshold voltage.

Internal voltage regulator circuits developed with our BiFET process exploit the VVR's ability to deliver a constant current at a fixed gate-source voltage across a wide range of drain-source voltages (figure 2a). Regulators can then be created to feed multiple circuits requiring a fixed voltage thanks to the HBT's ability to mirror currents.

Our BiFET process also enables logic with low-leakage currents – it is possible to create a low-

leakage inverter with a combination of HBT and VVR devices. Our inverter's load has to be large enough to ensure a sufficiently low leakage current for the FEM (typically less than 10 μ A), but high enough to drive the circuit.

It is possible to extend this concept and build AND, NAND, OR and NOR gates. In addition, FEMs with a digitally enabled internal regulator can be realized by uniting the building blocks of logic with a regulator (figure 3). Our BiFET can clearly deliver many desirable technologies while simplifying design, reducing the size of the circuits and cutting the total bill of materials.

Future goals include the exploration of new ways to exploit the inherent benefits of our unique BiFET technology and our approaches to drive the process to even higher yields. Ultimately, this should be good news for handset manufacturers.

Further reading

- M Fresina *et al.* 1996 *Electron Device Lett.* **17** 555.
- T Henderson *et al.* 2007 *CS MANTECH* 247.
- CK Lin *et al.* 2007 *CS MANTECH* 251.
- AG Metzgar *et al.* 2006 *CSIC* 175.
- B Moser *et al.* 2008 *CS MANTECH* 273.
- M Shokrani *et al.* 2006 *CS MANTECH* 153.
- P Zampardi *et al.* 2005 *CS-MAX* 32.



About the authors

Brian Moser (left; bmoser@rfmd.com) is a group leader in the Device Engineering Group at RF Micro Devices.

William Clausen (center; wclausen@rfmd.com) is a senior modeling engineer and

David Vines (right; dvines@rfmd.com) is a senior design engineer. The authors thank D Limanto, D Wernsing and J Fendrich for measurement data, and process engineers for their help – particularly R Vass, K Scott and C Duke. Staff at the Phoenix Design Center lab played a key role in the power-amplifier-level evaluation.

Oxford Instruments Etch, Deposition and Growth

For precise, controllable and repeatable etching, deposition and growth of micro and nano structures

Plasma Etch & Deposition

Atomic Layer Deposition

Ion Beam Etch & Deposition

Nanoscale Growth Systems

Hydride Vapour Phase Epitaxy



For more information email: plasma.technology@oxinst.com

Oxford Instruments Plasma Technology Tel: +44 (0)1934 837000

www.oxford-instruments.com/compsemi



2009
BUYER'S GUIDE

COMPOUND SEMICONDUCTOR

Your definitive
print directory
for the III-V and
II-VI industries

- Semiconductor materials
- Substrates
- Epitaxial growth reactors
- Materials characterization
- Process equipment
- Packaging
- Foundry services



Published by Compound Semiconductor magazine

ADVERTISE **FREE** IN OUR BUYERS GUIDE

The essential reference for
purchasers worldwide

To place your free listing, contact
the sales team today:

David Iddon (Europe/ROW)

Tel +44 (0)117 9301032 E-mail david.iddon@iop.org

Jeff Spratley (USA/Canada)

Tel +1 (215)6270880 E-mail spratley@ioppubusa.com

COMPOUND
SEMICONDUCTOR

Pulse generator slashes the size and cost of 10 Gbit/s transmitters

Oscillators, mixers and RF switches add to the cost and complexity of 10 Gbit/s transmitters for last-mile networks. However, all of these components can be discarded by switching to a radical design that just features a pulse generator and an amplifier, says a team of researchers at **Fujitsu**.

High-capacity wireless systems are a great option for data transfer over distances of up to a few kilometers. If they can operate at 10 Gbit/s or more, they can help to address the rocketing demand for capacity in mobile phone and internet networks, which is partly fueled by the growth of uncompressed high-definition video. On top of this, wireless promises to be a popular alternative in locations where it is particularly challenging to lay fiber-optic cables for trunk-line data network systems. Mountainous regions and areas with rivers, roads or rail tracks all exacerbate the difficulties that are associated with build-out of buried fiber-optic networks.

The best frequencies for delivering data transmission at speeds in excess of 10 Gbit/s are found in the millimeter band. This region within the electromagnetic spectrum is rarely used for commercial applications, which makes it relatively easy to secure wide swaths of bandwidth. A subset of this band, the “radio window” of 70–100 GHz, is also subjected to a relatively low level of attenuation by atmospheric gases. This increases the data transmission range and improves the link’s robustness.

W-band transmission

The short wavelengths that are associated with transmission in this radio window lead to equipment benefits. Millimeter-band radios can employ small hardware alongside high-gain antennas that produce a highly directional beam. This type of antenna reduces multi-path fading and interference with neighboring radios.

Despite these advantages, it is difficult to develop small, cost-effective equipment for transmitting in the 70–100 GHz range. This is because this type of unit currently requires the manufacture of several discrete single-purpose electronic components.

To address this weakness, our research team at Fujitsu and Fujitsu Laboratories, in Kanagawa, Japan, has embarked on the development of a radical form of impulse-radio technology. No oscillators or mixers are needed, and the transmitter can be built from just two active components: a pulse generator and an amplifier (figure 1, p30). The pulse gener-



Laying fiber-optic cable can be time consuming and expensive – in Japan the cost of laying just 1 km of fiber beneath the road is around \$1 million. Local wireless networks are an attractive alternative, particularly in mountainous regions, but they must deliver sufficiently high capacity.

ator’s emission corresponds to a data stream from a baseband block. RF signals, known as wavelets, are then created by passing this data stream through a band-pass filter. This filters a wide frequency spectrum of pulses to match the spectrum mask.

Our simple transmitter will only be a viable option for last-mile wireless if it can generate pulses with sufficient energy. Meeting this need

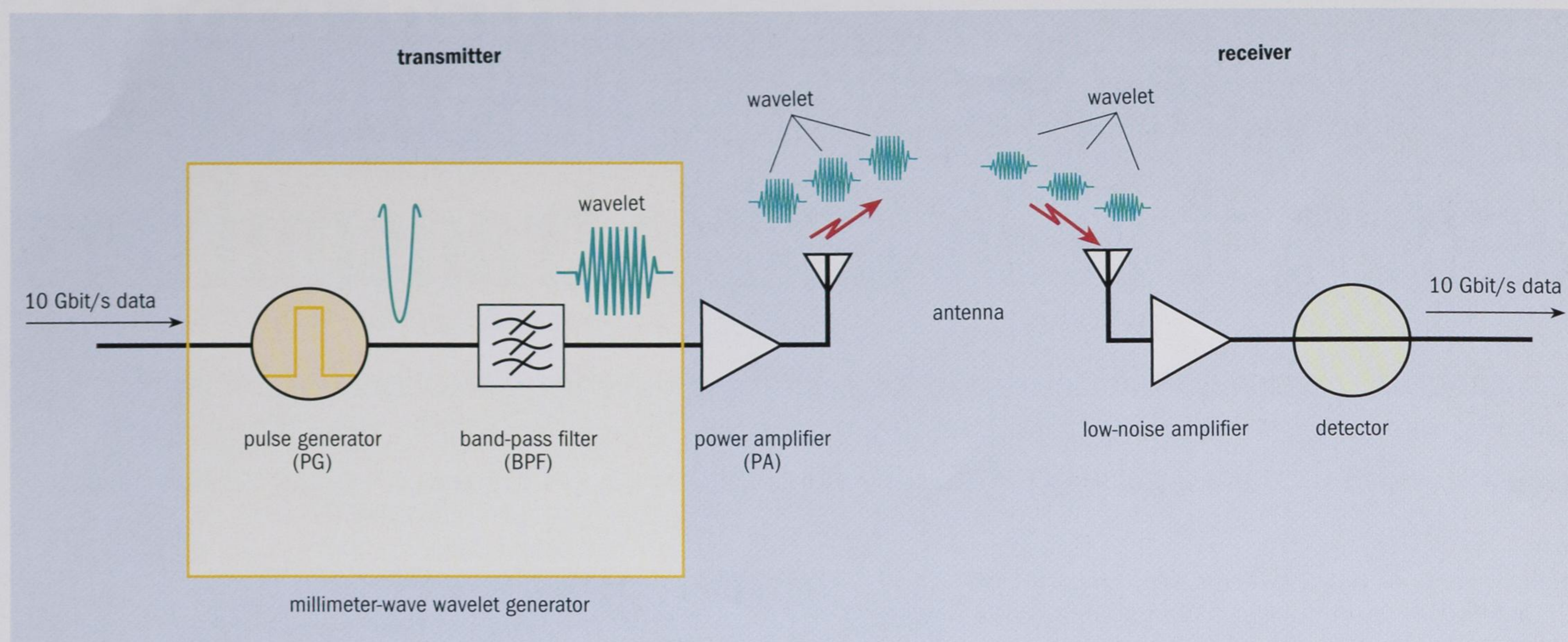


Fig. 1. Fujitsu's millimeter-wave wavelet generator takes a 10 Gbit/s signal and feeds it into a pulse generator that creates a series of pulses. These pulses correspond to a data stream from a baseband block. Passing this signal through a band-pass filter creates a series of wavelets spanning most of the 70–100 GHz range.

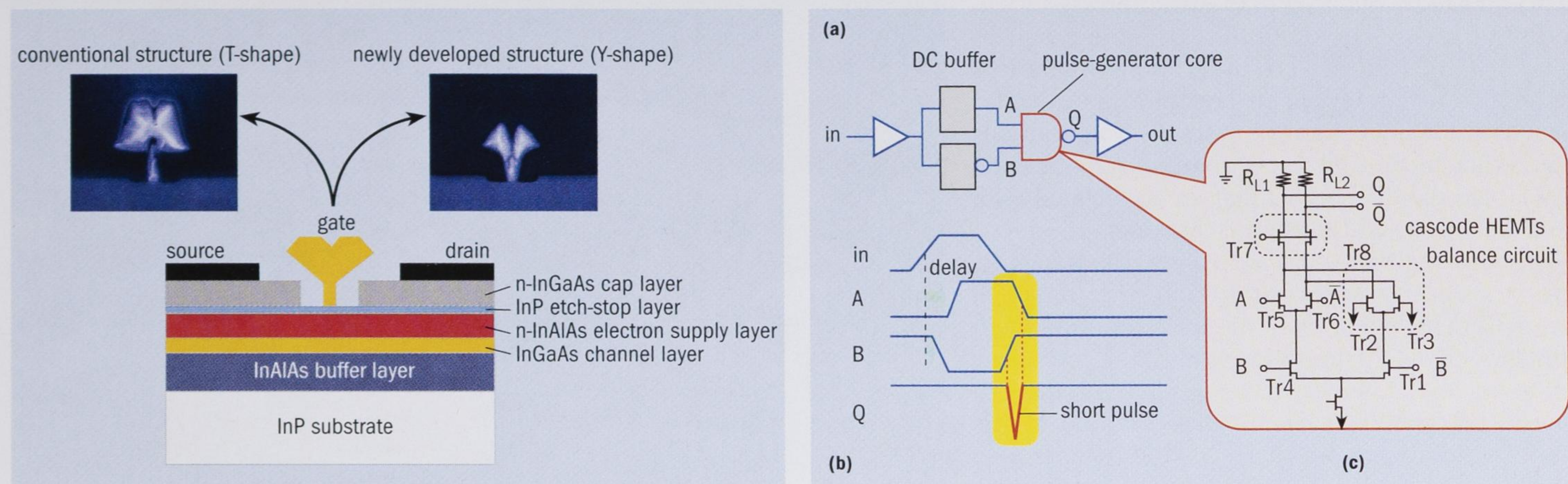


Fig. 2. (left) Fujitsu's 0.13 μm InP HEMT process features Y-shaped gates that are formed by a lift-off process. These are more robust than the traditional T-shaped gate architecture. **Fig. 3.** (right) The pulse generator splits the two signals, feeds each of them into a DC buffer and then brings them back together in the pulse-generator core (a). Ultrashort pulses can be produced by adjusting the time difference between the two pulses (b). The pulse-generator core is built from eight transistors, labeled Tr1 to Tr8. A balance circuit that contains the fixed-biased differential pair Tr2 and Tr3, decreases the Miller capacitance of Tr1 and improves the switching performance of the differential pair Tr1 and Tr4. In addition, cascode transistors (Tr7 and Tr8) reduce the Miller capacitances of Tr5 and Tr6, respectively, and boost switching of the differential pair Tr5 and Tr6. The former circuit shortens the falling time of the pulses, while the latter approach reduces the rising time.

requires very short pulses – the smaller the pulse's full-width at half-maximum (FWHM), the greater the power that is emitted at higher frequencies. Our application demands pulses with a FWHM of less than 10 ps, which we have realized with our InP HEMT technology. GaAs HEMT and sub-100 nm silicon MOS technologies were not employed because they have a weaker high-frequency performance and an inferior noise figure.

One distinguishing feature of our HEMT is its Y-shaped gate (figure 2). This architecture helps to prevent the top of the gate from peeling off and leads to a high gate-electrode fabrication yield. Conventional T-shaped gates are impaired by the low physical strength at the junction between a large top and a narrow stem. The Y-shaped gate is formed with

a lift-off process that includes electron-beam lithography and the evaporation of a Ti/Pt/Au contact. The typical gate length is 0.13 μm .

Y-shaped gates have the additional advantage of being able to improve the uniformity and stability in an InP wafer. This enables more than 1000 HEMTs to be integrated in a single chip. Thinning of the Schottky barrier layer in each of these transistors enhances performance, including an increase in maximum transconductance and cut-off frequency to 1.5 S/mm and 220 GHz.

We used triple-layer gold-plated interconnections and benzocyclobutene dielectric films with a low dielectric constant to integrate the HEMTs into circuits. Metal-insulator-metal capacitors and NiCr thin-film resistors are also formed on the InP substrate.

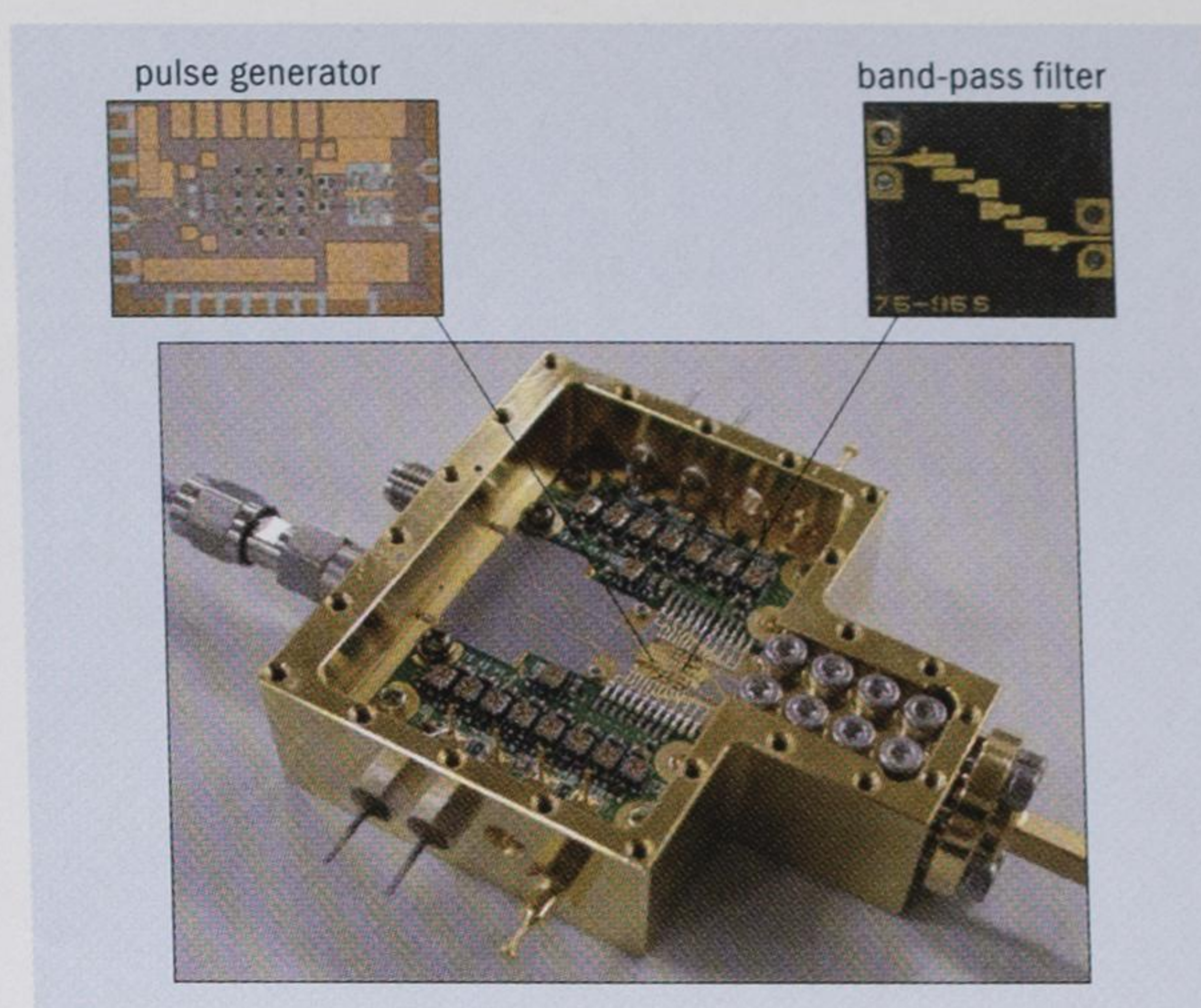
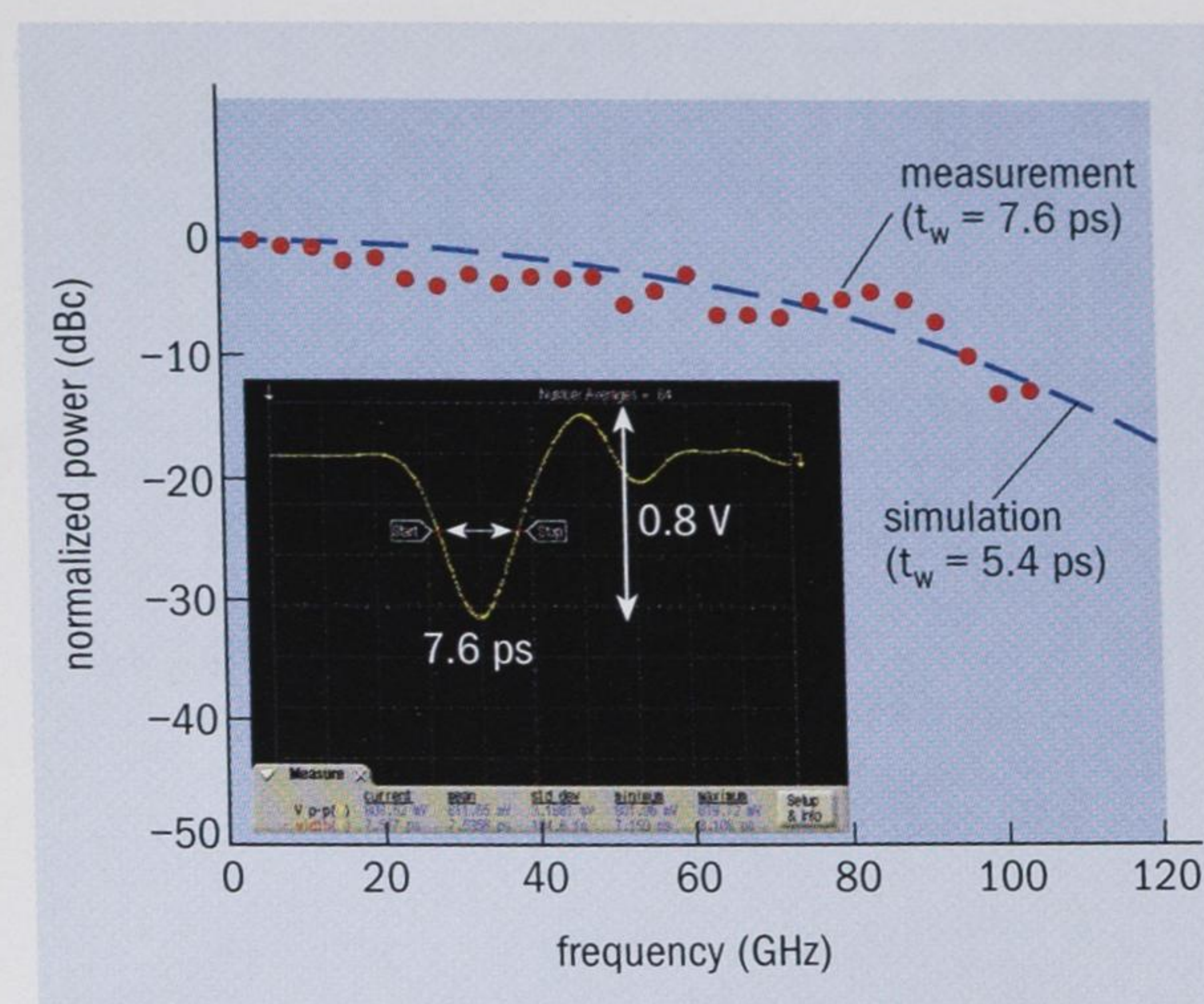


Fig. 4. (left) The pulse generator is capable of emitting pulses with a full-width at half-maximum of just 7.6 ps. The waveforms were analyzed with an oscilloscope that featured a 70 GHz sampling head. **Fig. 5.** (right) Fujitsu's millimeter-band pulse transmitter package is 70% smaller than its predecessors thanks to the simplicity of its design. It measures just 70 mm × 56 mm × 20 mm.

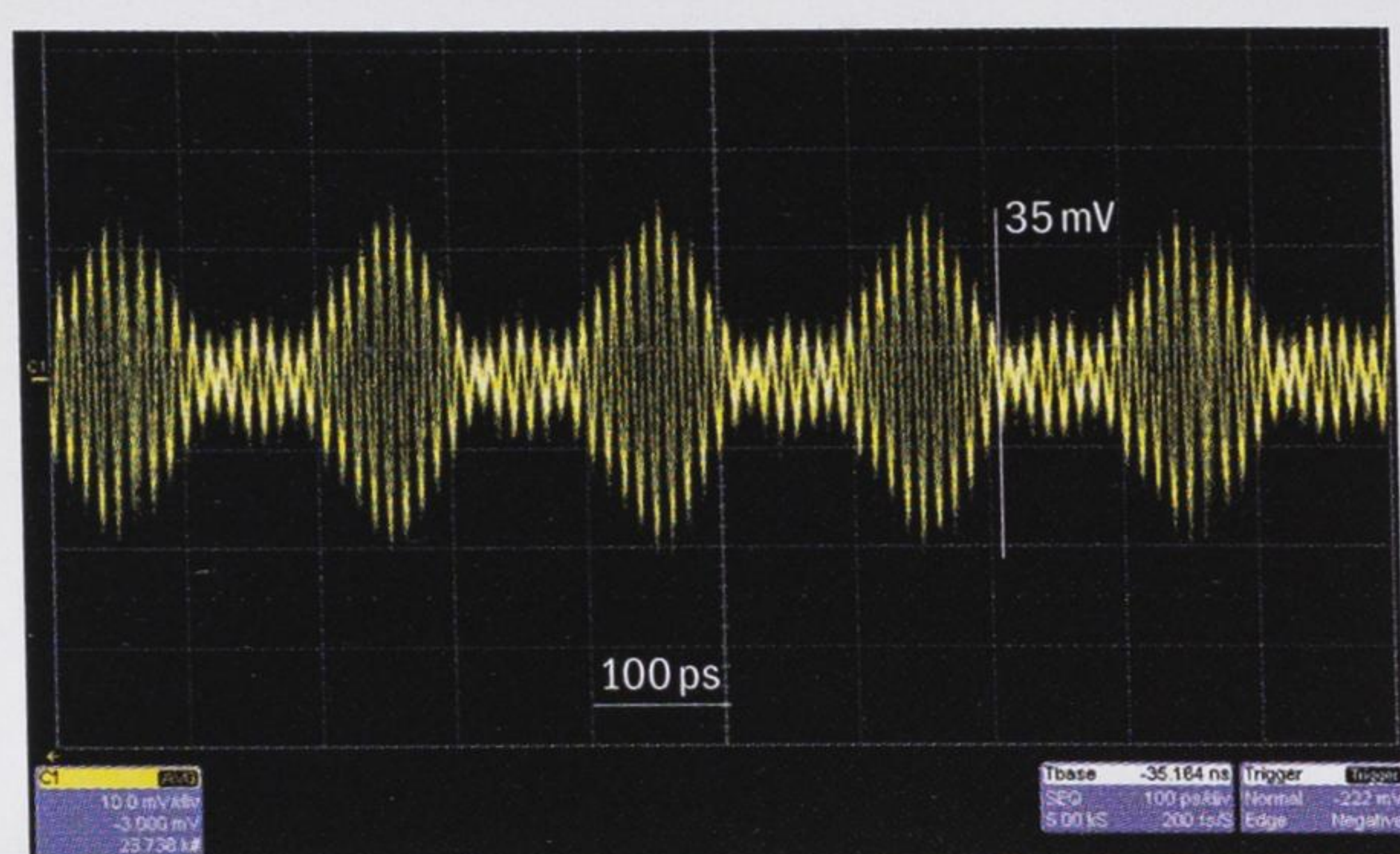


Fig. 6. Fujitsu's transmitter produces wavelets with a typical FWHM of 100 ps, which have frequencies spanning 78–93 GHz.

Very simple digital-based pulse generators can be created with this technology. These consist of input and output buffers, delay control (DC) buffers and a pulse-generator core (figure 3a).

Short pulses are created in the core by adjusting the DC buffer delay times, which in turn tunes the overlapping time between input signals A and B (figure 3b). The pulse-generator core behaves like a logical NAND circuit and creates a pulse width that is nearly equal to the overlap.

Shorter pulses can be created by increasing the response speed of the pulse-generator core or the NAND circuit. This led us to develop a new, bal-

anced NAND circuit (figure 3c) that can emit ultra-short pulses with a FWHM of just 7.6 ps (figure 4) and a peak-to-peak amplitude of 0.8 V.

We believe that these are the shortest pulses that have ever been generated from a semiconductor transistor. Spectral measurements reveal that the pulse generator can carry enough energy for frequencies above 100 GHz, which means that it's possible to build impulse-radio systems operating in the 70–100 GHz band.

Making a transmitter

We have followed this up by building a millimeter-band pulse transmitter (figure 5). This transmitter features a pulse generator, a 78–93 GHz band-pass filter and a W-band waveguide. Feeding 5 GHz clock signals into this module produced wavelets with a typical FWHM of 100 ps (figure 6). Spectral measurements confirmed that the wavelets had frequencies spanning the 78–93 GHz range, which almost corresponded to the transmission spectrum of the band-pass filter.

These results represent the world's first impulse radio transmitting at more than 10 Gbit/s in the millimeter band (in our case, 78–93 GHz). This new transmitter greatly simplifies the design of the millimeter-band emitters by eliminating the need for an oscillator, mixer and some other components. The upshot is a more compact package that is 70% smaller than its predecessors.

Our next aim will be to unite the transmitter with a receiver and conduct transmission testing with a fixed target. Field testing should follow.

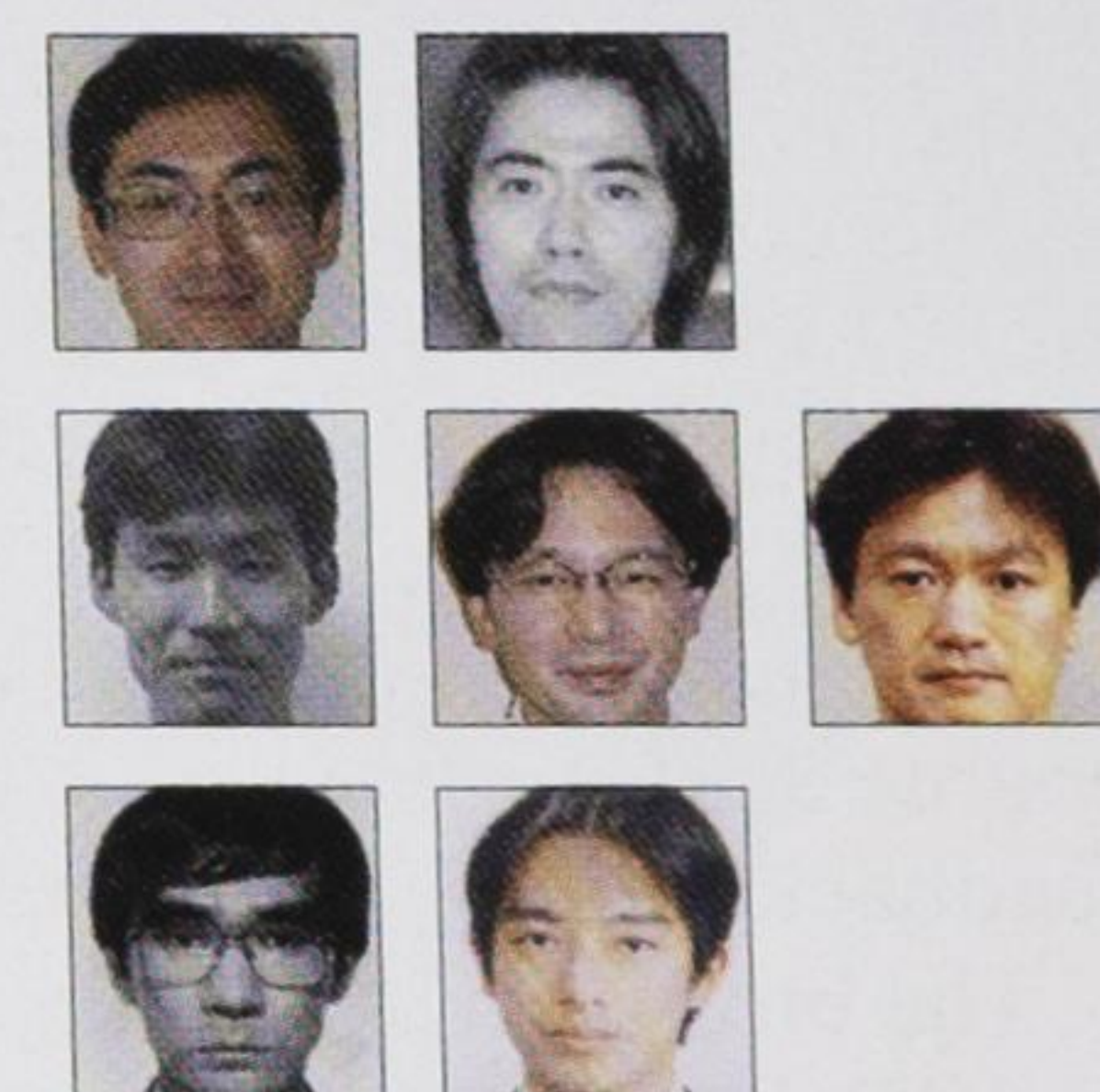
Further reading

Y Kawano *et al.* 2006 *IEEE Trans. Micro. Theory and Tech.* **54** 4489.

Y Nakasha *et al.* 2007 *Ext. Abstr. of the 2007 SSDM* 792.

Y Nakasha *et al.* 2008 *International Microwave Symposium Digest* 109.

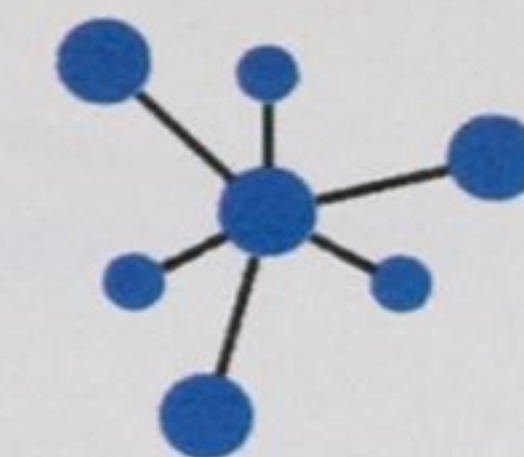
“We believe that these are the shortest pulses that have ever been generated from a semiconductor transistor.”



About the authors

Yasuhiro Nakasha (top left), **Yoichi Kawano** (top right), **Toshihide Suzuki** (center left), **Tsuyoshi Takahashi** (center), **Koza Makiyama** (center right) and **Naoki Hara** (bottom left) are researchers at Fujitsu.

Toshihiro Ohki (bottom right) is employed by Fujitsu Laboratories. All of the authors wish to acknowledge the valuable assistance and support of M Sato, T Hirose, K Joshin and E Yano. This work was also supported in part by Japan's Ministry of Internal Affairs and Communications.



SIC POWER ELECTRONICS

Larger JFET cranks current beyond 50 A

US researchers claim to have produced the largest active-area vertical-channel JFET based on SiC.

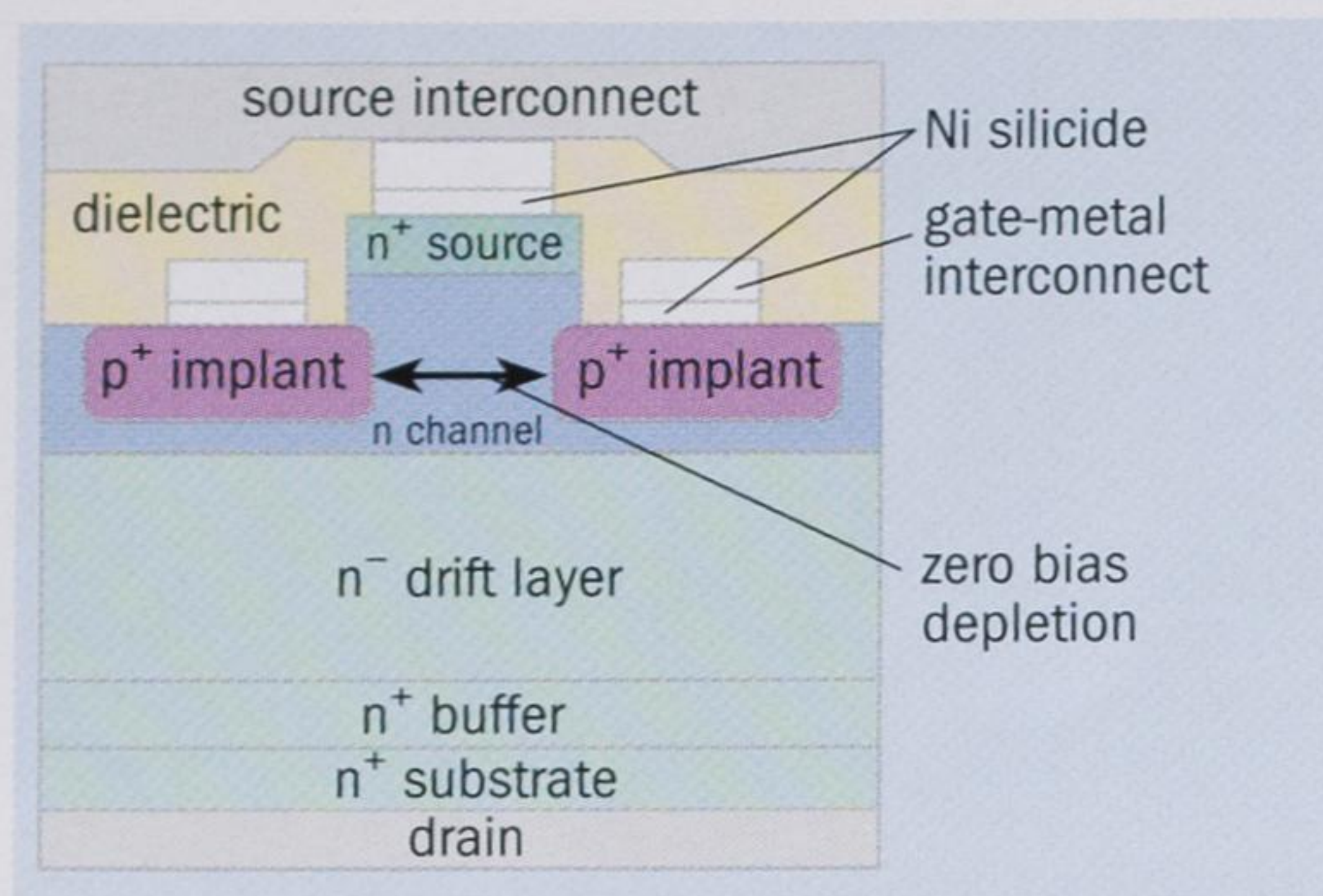
A team from Northrop Grumman Electronic Systems (NGES) and the US Army Research Laboratory has built a transistor with an active area of 0.143 cm^2 . It delivers a 53.6 A record drain current for this class of 1200 V device operating at 2.5 V.

The high current capabilities of these normally on SiC FETs make them candidates for deployment in hybrid electric vehicles and radar power-supply electronics.

FETs are grown on highly n-doped 3 inch 4H-SiC, and feature a $11.8 \mu\text{m}$ thick drift layer and a $2.1 \mu\text{m}$ thick channel (see figure).

The vertical-junction transistors can block voltages of up to 1680 V at a drain-current density of 1 mA/cm^2 and have an on-state resistance of $5.5 \text{ m}\Omega\text{cm}^2$.

The vertical-channel design has several advantages over the competing horizontal-channel technology, according



The p-type regions of the vertical channel, vertical-junction FET are created by ion implantation. Damage to the crystal structure occurs, but it can be repaired by a high-temperature annealing process.

to Victor Veliadis from NGES, including halving the on-resistance. The NGES FET uses seven photolithographic levels, but the horizontal-channel geometry requires epitaxial regrowth and two additional ion-implantation steps.

“Most circuit designers require normally off power switches due to the perceived safety that they provide in case of malfunction,” conceded Veliadis. However, a normally off high-current-gain switch can be built by connecting the team’s normally on FET with a low-voltage SiC equivalent in a cascode configuration.

The vertical-channel FET is not the only SiC option in the 1200 V market. However, Veliadis says that SiC MOSFETs suffer from low mobility and poor oxide reliability, and SiC BJTs are disadvantaged by forward voltage degradation and low current gain.

Veliadis and co-workers are planning to optimize the device yield and increase the current capability so that these devices can displace silicon in high-voltage power-switching applications.

Journal reference
V Veliadis 2008 *IEEE Electron Dev. Lett.* **29** 1132.

INP LASERS

Dashes deliver broad spectral bandwidth

An ultra-broadband infrared laser that covers an 85 nm spectral region has been developed by Boon Ooi’s group at Lehigh University in Bethlehem, PA.

Ooi says that the biggest potential market for his $1.54 \mu\text{m}$ -centered 1 W laser is optical telecommunications, where the single source could replace modules of distributed feedback transmitters for C- and L-bands.

The broadband laser structure was grown at IQE Inc and features a quantum dash active region. This contains four sheets of

5 monolayer-thick InAs dashes, each embedded within a 7.6 nm thick compressively strained $\text{In}_{0.64}\text{Ga}_{0.16}\text{Al}_{0.20}\text{As}$ quantum well. These are each sandwiched between 30 nm thick tensile-strained $\text{In}_{0.50}\text{Ga}_{0.32}\text{Al}_{0.18}\text{As}$ quantum barriers.

After depositing a 475 nm thick SiO_2 cap, Ooi’s team annealed the structure at 750°C in nitrogen gas for 1 min. This broadened the emission linewidth and shifted the lasing 100 nm into the blue.

Thinning of the dashes could cause the broadening, as could aluminum and indium atom diffusion from the wetting layer and barriers into the dashes, and out-diffusion of indium from the dashes.

Unpackaged, as-cleaved lasers with a

$500 \mu\text{m}$ long cavity have a threshold current density of 2.1 kA/cm^2 and produce 0.423 W/A. The maximum output is limited by thermal rollover.

Ooi says that the laser’s output power can be increased by optimizing the epitaxial structure and doping concentration, and placing it in a thermoelectric cooler package.

“Our immediate goal is to integrate multiple diodes along a single cavity using a spatial bandgap selective intermixing technique. This should produce a supercontinuum covering 1460–1620 nm from a single laser.”

Journal reference
CL Tamm et al. 2008 *Appl. Phys. Lett.* **93** 111101.

GaN HEMTs

TEM exposes cracks

GaN HEMTs can develop crack and pit-shaped defects close to the drain-side edge of the gate, according to US researchers who have studied transistors that have been stressed under DC bias.

TriQuint Semiconductor’s Uttiya Chowdhury says that the observation of these defects by transmission electron microscopy (TEM) confirms that the main source of electrical degradation is the inverse piezoelectric field effect. This theory was proposed by

MIT’s Jesus del Alamo, who is also involved in this US partnership alongside researchers from the University of Texas at Dallas.

The collaboration operated several conventional HEMT devices with a $400 \mu\text{m}$ total gate periphery for 6–1000 hours at 40 V drain bias, at 82, 112 and 142°C . Focused ion beam milling prepared thin slices from the middle of the gate width for TEM analysis.

This form of microscopy revealed pits up to 10 nm deep and cracks that usually extend down to the AlGaN/GaN interface, which is 20 nm from the surface.

“We have yet to observe cracks when the

device is stressed at room temperature,” explained Chowdhury. “However, we believe that micro-cracks form at room temperature and propagate at higher temperature.”

He thinks that crack formation can be combated by elastic strain reduction in the barrier. “Since cracks originate in the surface, we believe that surface preparation and engineering can delay and reduce cracking. We are working on both areas.”

Journal reference
U Chowdhury et al. 2008 *IEEE Electron Dev. Lett.* **29** 1098.

SAFC Hitech™

Changing the face of materials technology



SAFC Hitech is the new face that's set to transform the materials technology sector.

It sees Epichem, the proven market leader with a 25 year pedigree supplying the compound semiconductor industry, joining forces with the strength of SAFC®. Bringing you a reliable and responsive partner who is now even more prepared to deliver the innovative chemistry and extensive supply chain expertise you need, when and where you need it.

SAFC Hitech offers a global manufacturing and regional support infrastructure that is essential to enable technology and make your ideas happen.

The future of materials technology is revealed.
Look to SAFC Hitech today.

SAFC Hitech™
Enabling Technology

www.safchitech.com

SIGMA-ALDRICH™

Structural advantage for your process control



PANalytical offers a unique range of X-ray diffraction (XRD) tools, designed for characterizing and monitoring structural parameters of LED and compound semiconductors.

Our XRD solutions have such versatility and capability that they can be employed from R&D, through pilot lines, to full scale production. No other analytical partner provides this.

PANalytical delivers structural advantage to semiconductor companies around the world, through its:

- Top level expertise in materials characterization
- Unrivalled global customer support network
- Unique capability to fulfill analytical needs from R&D to full scale production

Let's meet at Semicon Japan
PANalytical booth number: 2A-203

PANalytical B.V.
Lelyweg 1, 7602 EA Almelo
P.O. Box 13, 7600 AA Almelo
The Netherlands
T +31 (0) 546 534 444
F +31 (0) 546 534 598
info@panalytical.com
www.panalytical.com/semi

The Analytical X-ray Company

 **PANalytical**