

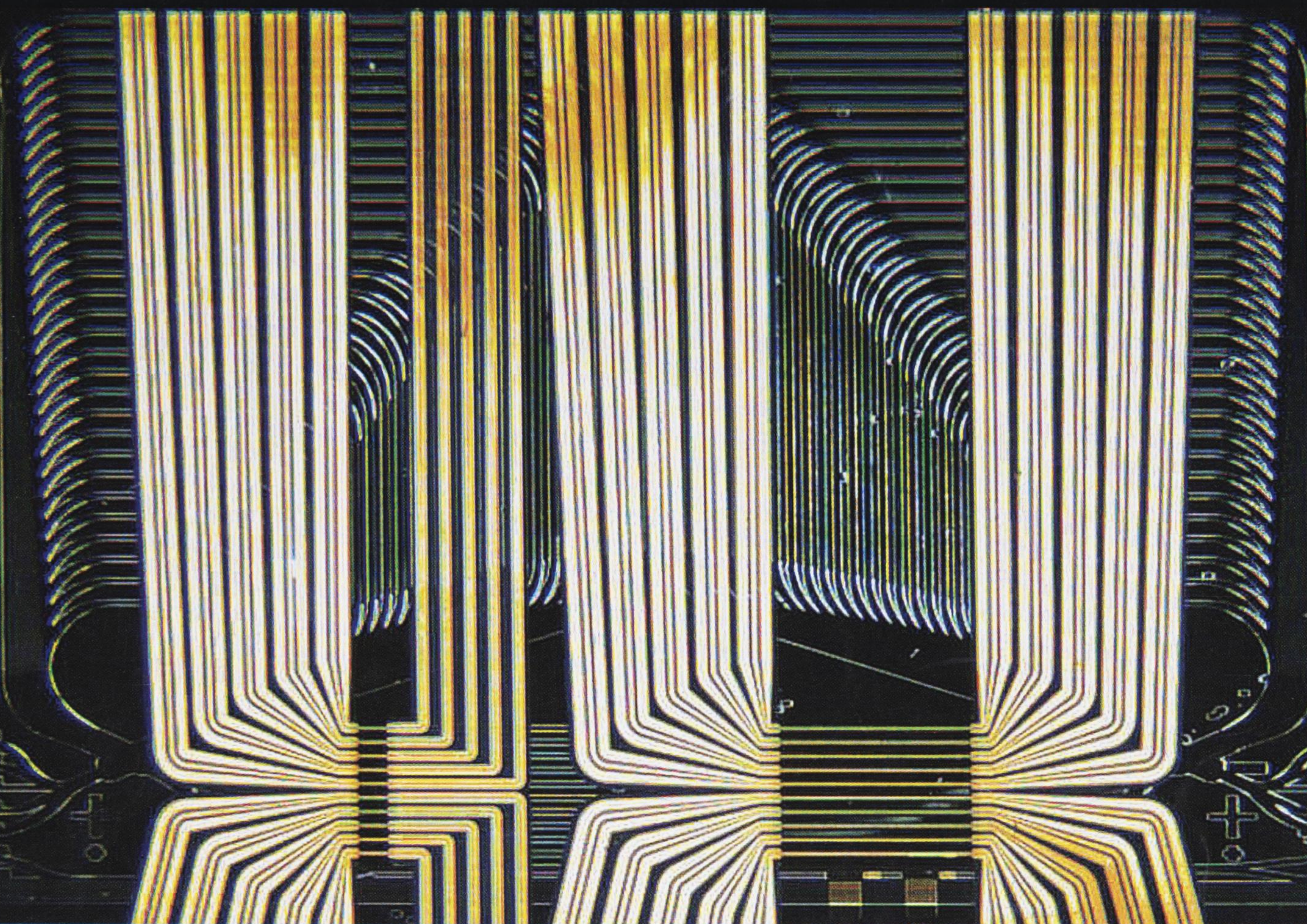
COMPOUND SEMICONDUCTOR

March 2009 Volume 15 Number 2

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INDIUM PHOSPHIDE

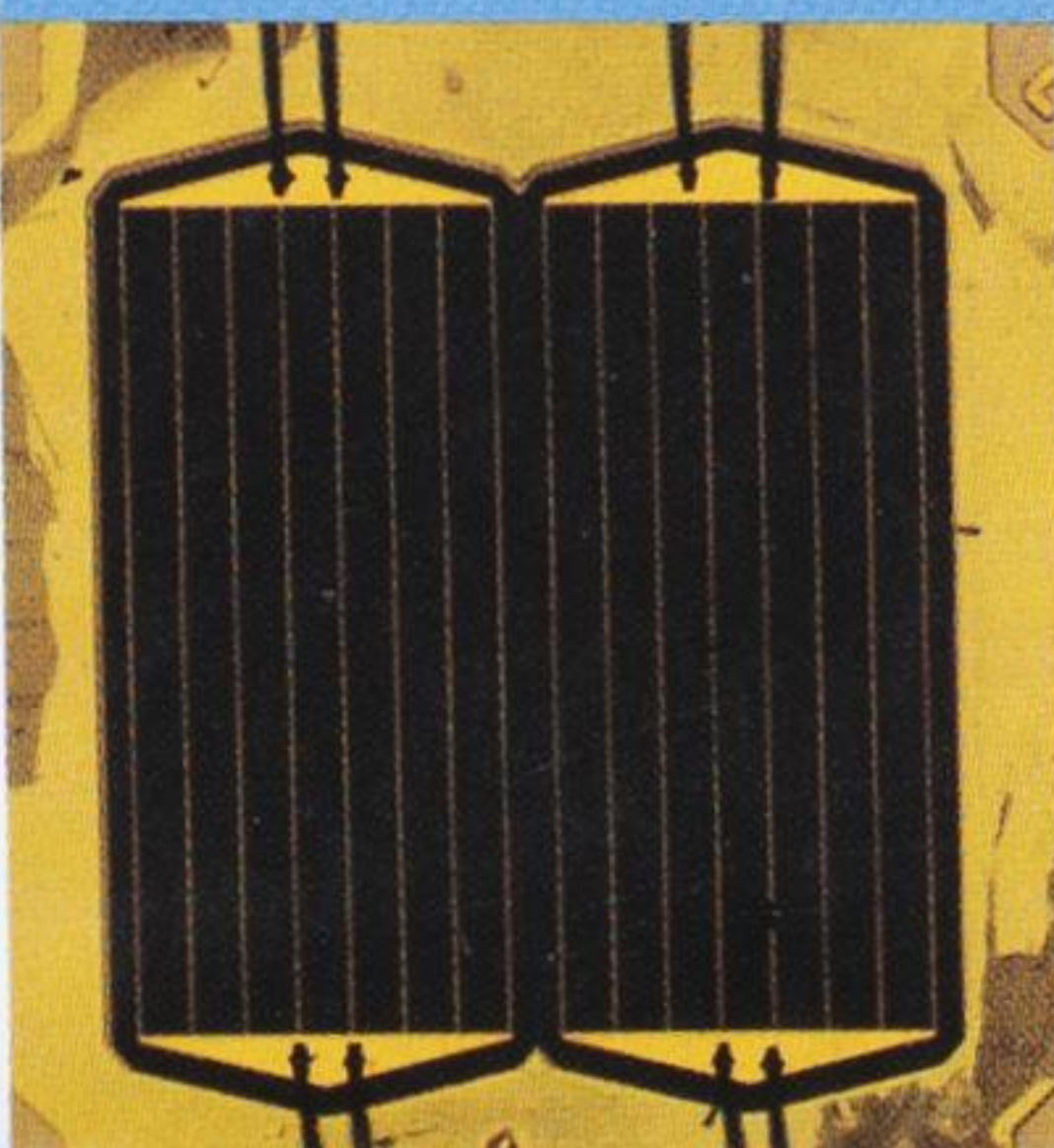
HVPE simplifies photonic integration



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**IR accuses former
CEO of stealing GaN
technology p5**

SOLAR CELLS



Record efficiencies

Germany trumps the
US with a metamorphic
design delivering
41.1%. [p9](#)

GAN LEDs



Novel platforms

Silicon-on-insulator
substrates provide an
affordable, reflective
base for green LEDs. [p25](#)

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INDUSTRY

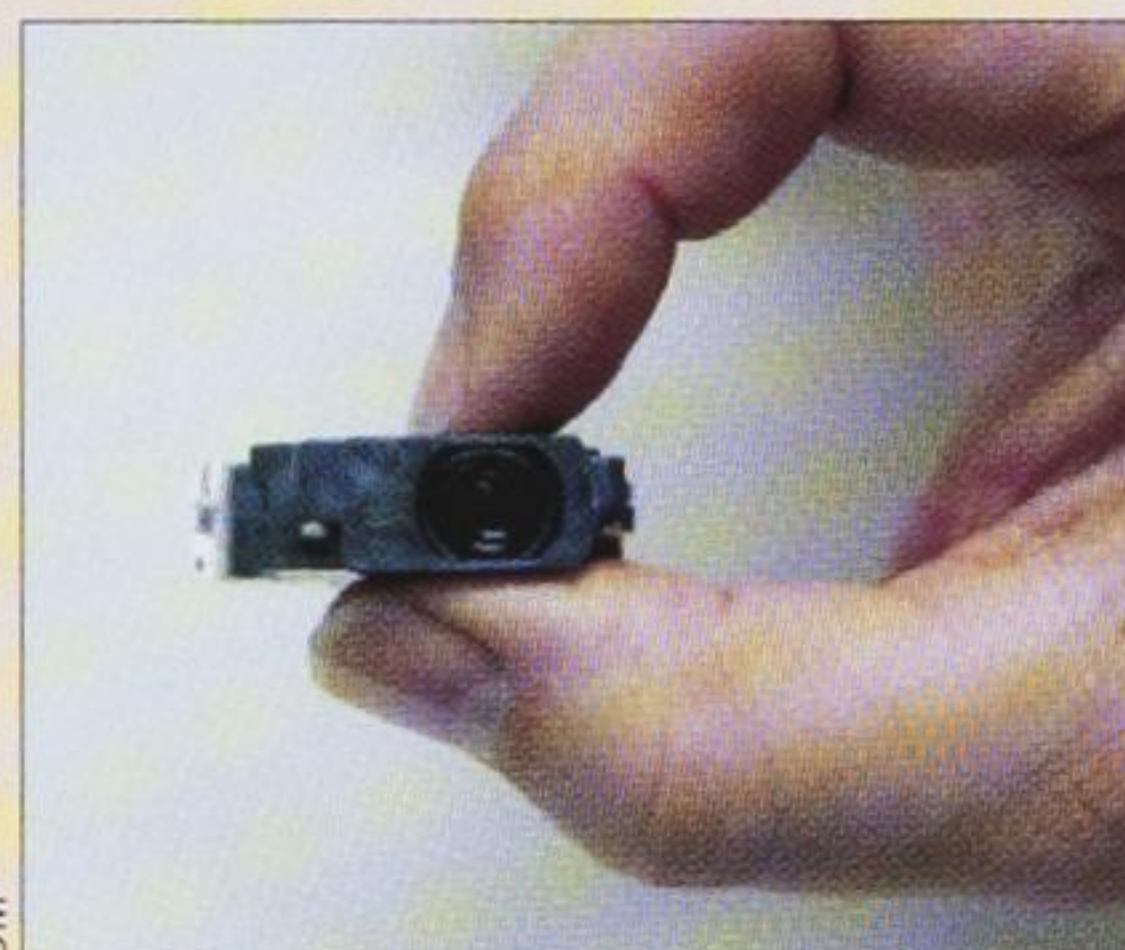
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Main cover image: Combining HVPE and MOCVD simplifies the fabrication of various types of photonic integrated circuit, including this arbitrary waveform generator. See p14. Credit: University of California, Davis.

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EDITORIAL

A little perspective



At the end of January, a very unusual thing happened in the UK media. For a couple of days, virtually every national newspaper ran stories about compound semiconductors. BBC television even ran a live interview with Colin Humphreys, the University of Cambridge professor who specializes in GaN. The reason was this: “magic” LEDs, grown on silicon by Humphreys’ team, would slash household electricity use.

At a time when efforts to cut consumption – both for environmental and financial reasons – is so prominent in the public consciousness, it is perhaps surprising that the potential for LEDs to save large amounts of energy is not highlighted more often.

But this level of publicity presents a dilemma. On the one hand it is great to see III-V technology covered so prominently and for some of the brightest minds in our community to be given the opportunity to show its great potential. On the other hand, this kind of coverage almost inevitably leads to a degree of unjustified hype, in which claims for the technology

“‘Magic’ LEDs
would slash
household
electricity use.”

are overdone and lead to disappointment.

No doubt the folks at the University of Cambridge press office will have given themselves a large pat on the back for attracting worldwide media interest in their research group. That, after all, is what they are there to do. But the devil is always in the detail and there are an awful lot of details to be ironed out before the potential energy-saving qualities of this approach to solid-state lighting technology can be fully realized.

What the Cambridge team has achieved so far with nitride growth on silicon is impressive. But theirs is a laboratory demonstration and any tangible impact on the lighting industry remains some years away. Exactly how many years is impossible to say at this stage, until the proof of principle shown in the lab is replicated in a true manufacturing environment. As many of you will appreciate from first-hand experience, that step can often be the toughest to take.

A few months ago, we invited the Cambridge team to write an article about the progress that they have made. It appears on p19 of this issue. We also feature an alternative approach to the problem, in which a Singapore-Germany collaboration has developed a technique using silicon-on-insulator substrates (p25) to make green emitters.

Can either of these technologies slash household electricity use? Only the progress made over the next three years will tell us the answer to that.

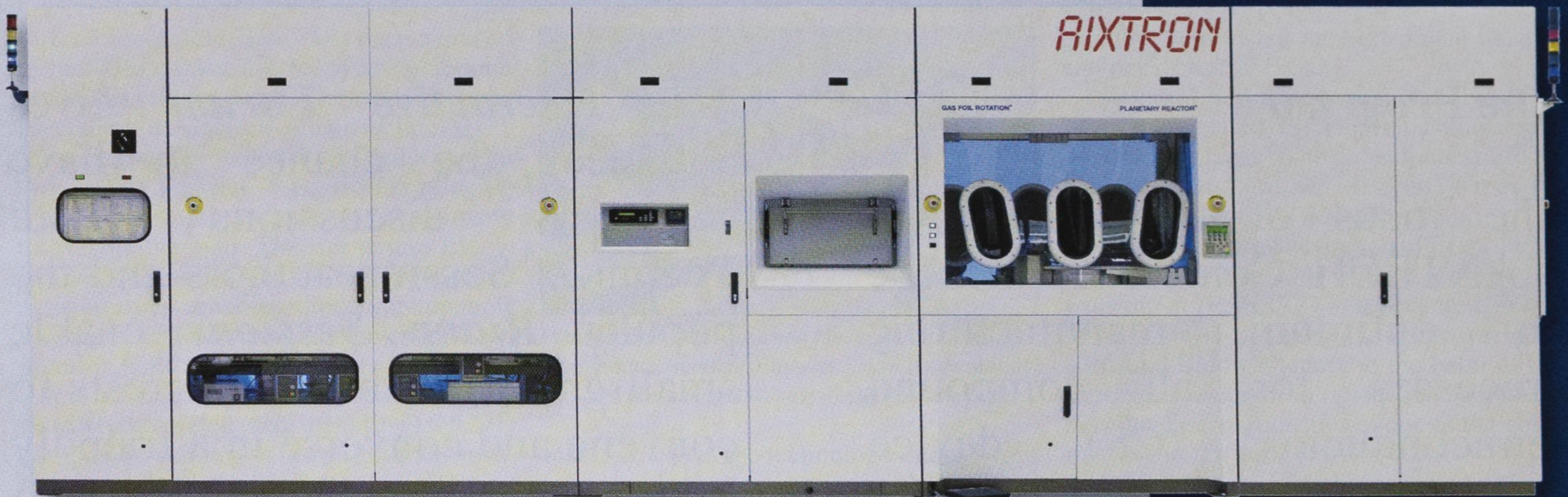
Michael Hatcher *Editor*

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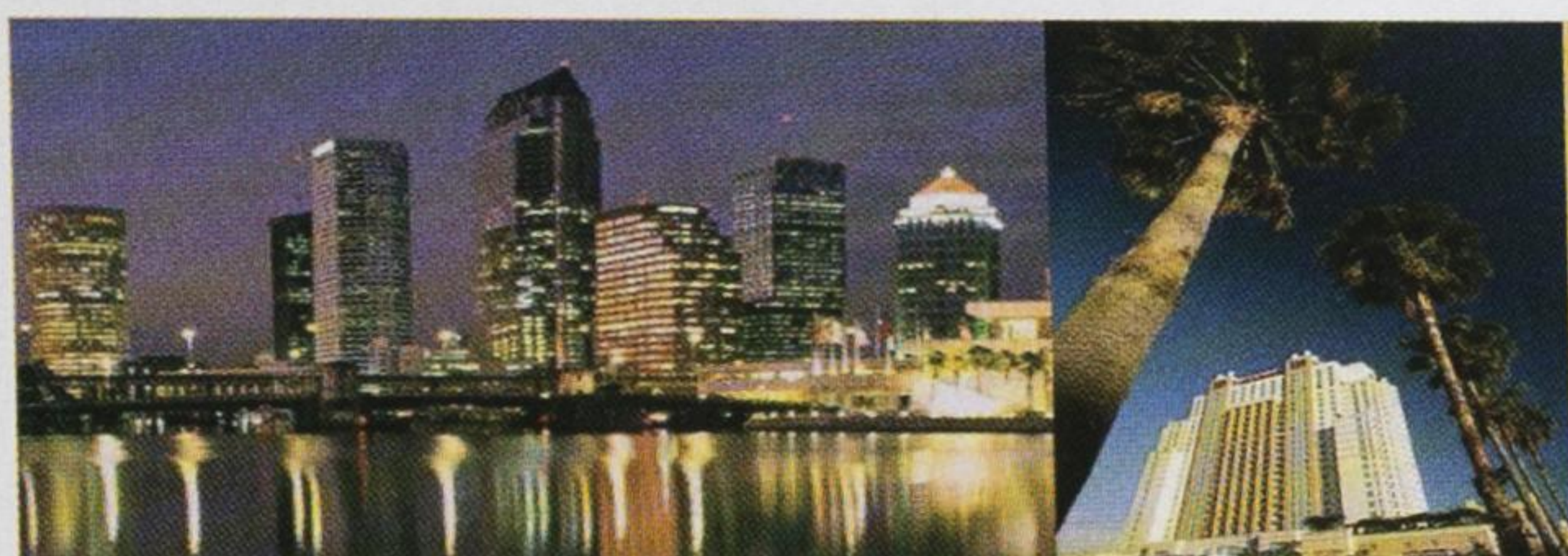
The program includes practical **Technical Sessions** including invited papers presented by technologists from around the world; an intensive **Workshop**; and an **Exhibit** featuring leading equipment, substrate, epitaxy, process chemical vendors and special service providers for CS device technologies (RF, Power, LEDs, Solar...).

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EXECUTIVE ETHICS

IR sues former CEO and Aixtron over GaN

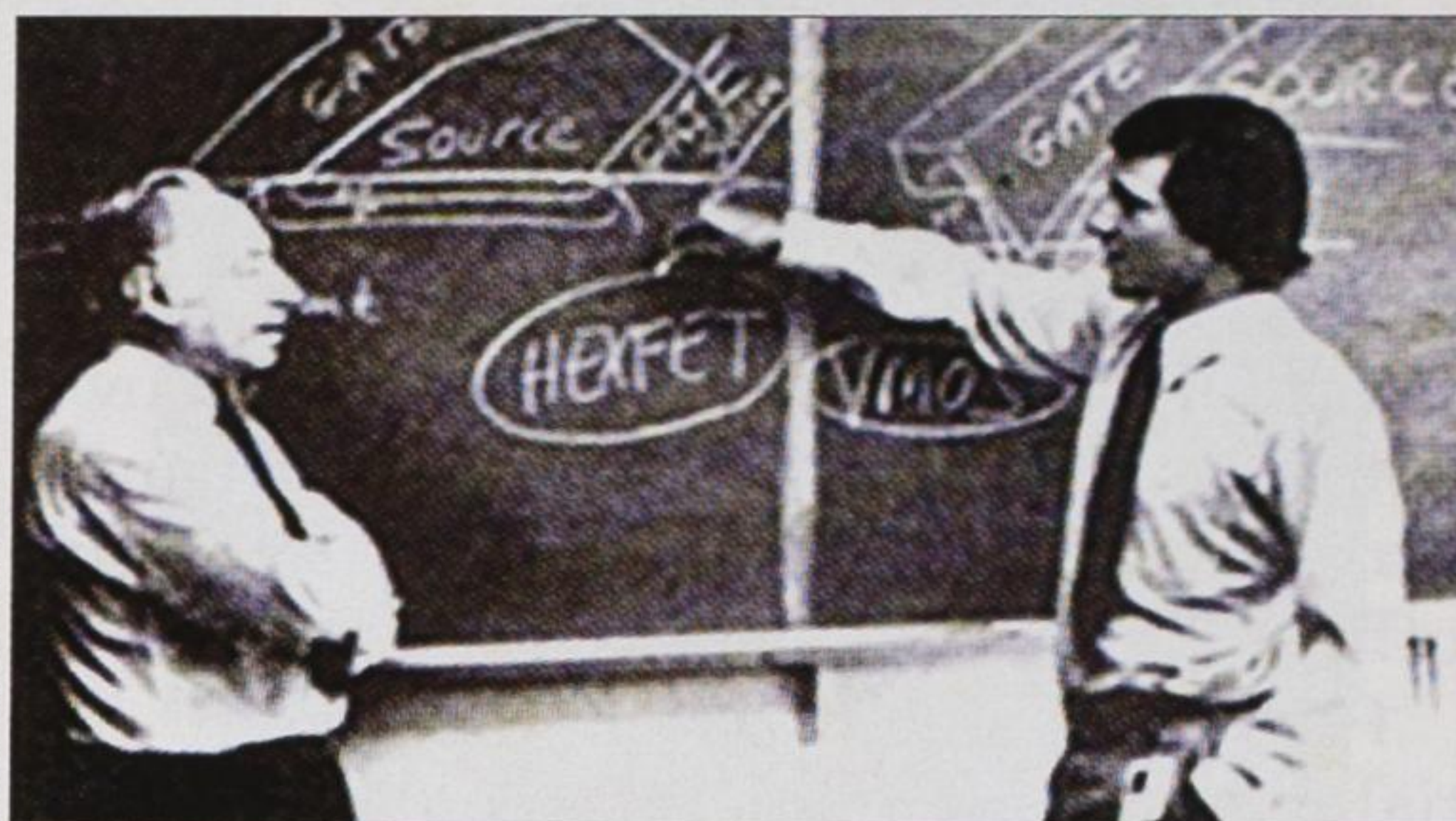
International Rectifier (IR) has accused former CEO, Alex Lidow, of an "elaborate fraudulent scheme to rob" the power electronics giant of its GaN-on-silicon technology.

On September 8, 2008, IR filed a case in the Central District of California alleging that Lidow set up an undercover company to execute the plan. The suit names Lidow and six fellow former IR employees that assisted in establishing that company, now known as Efficient Power Conversion Corporation (EPCC).

It also accuses companies that the EPCC team has interacted with, including MOCVD equipment vendors Aixtron and Hermes-Epitek plus silicon wafer supplier Episil Technologies. An interim hearing was held on February 2 where Aixtron and EPCC argued in favor of dismissing the case.

Lidow was CEO of IR from 1999 to October 2007, during which time he oversaw what IR claims to have been a \$60 million investment into GaN research. "By engaging in their unlawful conduct, defendants caused IR to lose much of the value of its multimillion dollar research expenditures on GaN-related projects and personnel," IR's court documents state.

IR had kept the disputed GaN-on-silicon research a closely guarded secret, and the company only revealed details of the work shortly before demonstrating prototype devices in November 2008. The suit says



Founder Eric Lidow and son Alexander both led International Rectifier. However, Lidow Jr now stands accused of stealing GaN technology from the firm.

that Lidow kept the technology under wraps to stop competitors knowing that IR was working on GaN, and prevented a public disclosure in summer 2007.

It claims that Lidow then started enrolling colleagues at IR, plus founder of Hermes-Epitek and Episil Archie Hwang, to his plan to form EPCC in early fall 2007. Beginning in late 2007, IR says EPCC tried to recruit its business collaborators, including etch tool supplier Lam Research Corporation. Lidow also allegedly made several trips to meet Episil and Hermes-Epitek in Taiwan.

Aixtron's involvement comes through a meeting that an EPCC representative is supposed to have held with its employee Yulmas Dimke at the company's Aachen premises in June 2008. Dimke had previously worked closely with IR's GaN epitaxy

group to help install an Aixtron G4 reactor and perform trial runs.

"[Dimke] had access to virtually all of IR's GaN-related information," the court documents claim. "The defendants at EPCC sought out and utilized Aixtron, just as IR does and did for its GaN effort."

Alexander Lidow is the son of Eric Lidow, who set up IR in 1947. Alex Lidow began working at IR in 1977 and became CEO in 1999. This is not the first controversy to surround Lidow's tenure at the helm of the firm – his resignation in late 2007 followed accounting irregularities at one of the company's foreign subsidiaries.

● IR's power semiconductor rival Microsemi Corporation has also taken up a grievance with its CEO, Jim Peterson, for saying he held degrees that he did not. Peterson will retain his post after falsely claiming to hold a Bachelor's degree and Master's in business administration from Brigham Young University (BYU).

On January 29 the silicon and SiC electronics company announced that an independent inquiry had found that he only held an Associate's degree, but had studied towards a Bachelor's at BYU. Consequently Peterson, who has been Microsemi CEO since December 2000, must immediately pay his employer \$100,000 and forego his annual bonus, which has averaged \$680,000 over the past three years.

LED DEVELOPMENT

Nichia's 249 lm/W LEDs mark tech shift

Researchers at Nichia have grabbed the attention of their LED industry peers by cranking up the efficacy of their white emitters to 249 lm/W at 20 mA.

However, the results reported at Photonics West on January 29 show that this falls to 145 lm/W at 350 mA, the drive current often used to compare the output of today's high-brightness LEDs. This decline in efficacy with current is incredibly steep, and Nichia's Takashi Mukai told delegates that it might be due to a mistake in the process.

Mukai initially introduced the result by stating that the theoretical efficacy limit for white LEDs is 263 lm/W. Yet when questioned by the audience he explained that Nichia has pushed this ceiling to more than

300 lm/W thanks to the introduction of a new phosphor technology.

Further questions revealed that the LED shared two features associated with the company's best devices from 2006 – a hexagonally patterned sapphire substrate and a transparent indium tin oxide contact. In comparison with Nichia's latest chips, Cree and Osram claimed 161 lm/W and 136 lm/W laboratory demonstration efficacies, respectively, at 350 mA in 2008.

Elsewhere, the Japanese LED innovator has continued expanding its array of licensing and supply deals in the first months of 2009. Most notably it has settled its protracted legal wranglings and signed cross licenses with former adversary Seoul Semiconductor. US LED manufacturer Luminus Devices has also signed up to a manufacturing, cross-licensing and co-development deal.

Furthermore, Taiwanese LED maker Opto Tech Corporation has halted construction of

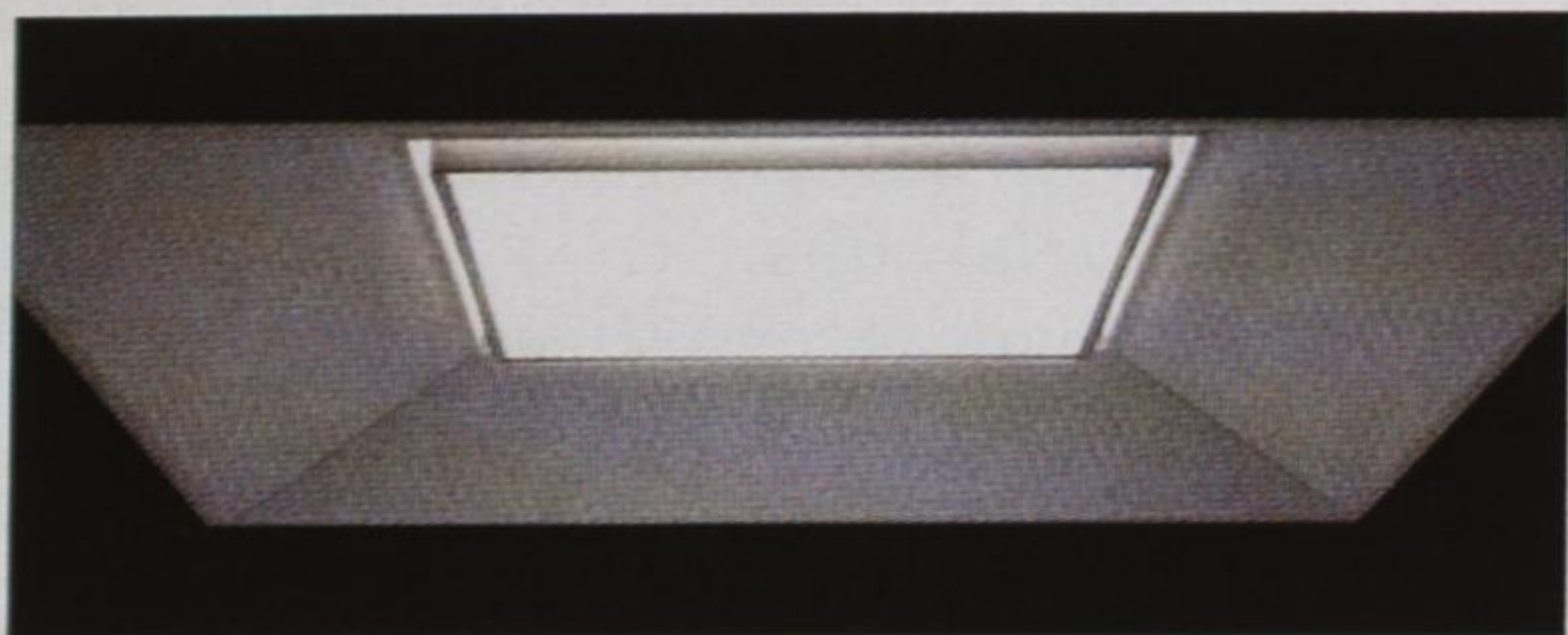
a factory in China and will instead collaborate more closely with Nichia. The Japanese giant invited die maker and packager Opto Tech to invest in it and strengthen the firms' mutually beneficial alliance in December.

Opto Tech began selling Nichia-branded products following a licensing agreement signed in 2004. That boosted Opto Tech's blue LED business, while the December deal represented a ¥1.06 billion (\$11.7 million) investment in its Japanese partner.

According to the *Chinese Economic News Service* and *Digitimes*, the enhanced collaboration comes as Nichia is attempting to increase its bare LED die sales. Opto Tech has helped Nichia to achieve this with recent qualifications from three companies operating in the notebook LED backlight supply chain. Under the alliance, Opto Tech will now produce more Nichia-branded die and Nichia will supply its own die to the Taiwanese firm to increase volumes.

LED MANUFACTURING

LG-Cree alliance fuels LED notebook push



There will be 4200 of Cree's LR24 fixtures installed in the Pentagon in 2009, after having proven their worth in the US Federal Reserve building.

The world's highest-volume LCD panel manufacturer, LG Display, has formed an alliance with LED maker Cree to help it to replace lower-efficiency fluorescent backlighting.

A spokesperson from the Korean thin-film transistor LCD producer told *Compound Semiconductor* that it intends to deploy LED backlighting in half of the notebook displays it will manufacture in 2009.

Under the strategic agreement, completed in early January, Cree will share its expertise in LED die packaging as LG Display brings backlight manufacturing in-house. The US chipmaker will also provide a stable supply of LEDs, although LG Display says that it will still source chips from Japanese producer Nichia and other rival companies.

LG Display produced 37% of the notebook TFT-LCD displays shipped globally in December 2008, according to figures released by industry analyst Displaybank on January 22. At 8.3 million, the month's total notebook display volume was down by 21% over the same time in 2007. In terms of overall volumes of TFT-LCD displays LG Display is also the leader, claiming 27% of the 27 million units shipped in December.

This marks a departure from the illumination-focused strategy that saw Cree increasing its sales and profits for the last quarter of 2008 in spite of the recession.

Although its \$147.6 million quarterly revenues were enhanced by \$5.6 million in one-off patent licensing fees, underlying product sales were still 1.3% higher than the previous quarter.

Lighting products propelled Cree's continued sales growth and helped the company boost its profits to \$10.7 million, up from \$5.9 million sequentially. \$4.4 million of that came directly from deals to license GaN substrate technology to Mitsubishi Chemical and LED chip patents to Bridgelux.

The patent windfall combined with higher utilization levels and product yields at the company's Durham, NC, and Hui-

zhou, China, facilities to drive the overall income leap.

Lighting fixture revenues are growing by more than 10% per quarter, although they are currently less than \$10 million overall and are dragging down profit margins.

However, Cree expects to enhance these product lines' financial performance as their manufacturing processes mature, while installations at the US Federal Reserve and Pentagon raise their profile.

"The Pentagon raised a lot of eyebrows, not just because it was 4200 fixtures and it was an entire wing," said chief executive officer Chuck Swoboda.

He emphasized that although the initial deployment might be seen by some as expensive, money saved in energy efficiency over current installed lighting would compensate. "They're talking about less than four-year payback," Swoboda expects a small amount of shipments for the Pentagon deal to begin in the current quarter.

For the three months to March this year, Cree is expecting revenues to fall below \$135 million, but is still targeting a profitable quarter.

INDUSTRY CONSOLIDATION

Bookham and Avanex finally agree merger

Avanex and Bookham announced on January 27 that they have reached a definitive agreement to merge, as they each strive for consistent profitability. The two companies will combine in an all-stock deal worth approximately \$35.4 million.

Avanex shareholders will receive 5.426 shares of Bookham common stock for every share of Avanex common stock that they own, and will end up owning 46.75% of the combined company. Based on the closing price of Bookham stock on 26 January, this arrangement values Avanex at \$2.17 per share – a considerable premium over its \$1.33 quoted price at the same time.

The companies expect the deal to close in three to five months, when they will combine under a new name that has yet to be decided. Bookham's president and chief executive officer Alain Couder will retain the same roles at the new company.

The first rumors of a tie-up between Avanex and Bookham emerged in late 2006, but the justification for the merger looks much better now, according to Couder.

"If we had done that [deal] several years ago it could have been quite expensive, but each company has done a great job to clean its own house and to end up very complementary," Couder told investors on a con-

ference call to discuss the deal.

Extrapolated from the September 2008 quarter, the Avanex/Bookham combination would make annual revenues of \$447 million, ranking it as the fourth largest optical communications earner behind Opnext at \$455 million, JDSU's telecoms division at \$532 million and Finisar at \$638 million.

With a GaAs fab in Switzerland and InP fab in the UK, Bookham primarily brings chip-level and components expertise for tunable products in particular. Fabless Avanex brings to the table strength in subsystems such as optical amplifiers, wavelength management and dispersion compensators. Since the divestment of its own III-V fab to form 3S Photonics, the company has purchased its laser diodes.

● The Opnext revenue figure quoted above includes figures from Stratalight, which it officially merged with on January 9. The two companies will now trade together under the Opnext name. "The marriage of [Opnext's] optical device and module technology with [Stratalight's] subsystems expertise will help our customers to optimize their future network designs for superior performance and cost," said the combined company's new CEO Gilles Bouchard.

WIRELESS BROADBAND

China's 3G triple play suits GaAs vendors

GaAs companies have welcomed the recent decision by China's Ministry of Industry and Information to roll out three broadband wireless protocols in the country, believing that the move offers up a major new commercial opportunity.

On January 7, the ministry approved licenses for China Mobile Communications, China Telecom and China Network Communications to build 3G networks. These networks will be based on TD-SCDMA, CDMA2000 and wideband-CDMA protocols, respectively.

US GaAs chip manufacturer Anadigics, which is focused on the broadband end of the wireless market, welcomed the development. Bruce Webber, the Warren, NJ, company's director of marketing for wireless products, told *Compound Semiconductor*: "[The decision] enlarges the market for all types of wireless components and systems," adding that Anadigics had developed products suited to each of the standards.

Asif Anwar, director of the compound semiconductor service at analyst firm Strategy Analytics, also believes that the development is good news for III-V specialists: "With three different licenses in play,

I think that all of the major GaAs suppliers will benefit," said Anwar. "It may take longer than the companies would like because the handset market will be slower this year.

"Infrastructure roll-out will be the early opportunity and companies like TriQuint, Avago, Skyworks and RF Micro Devices will be able to take advantage. Whether this will be an opportunity for high-voltage GaAs or GaN in base stations will be dependent on the approach adopted by base station manufacturers such as Huawei, Ericsson and Nokia Siemens Networks."

RFMD's management certainly views the development as a positive one for the Greensboro-based company. At the recent Needham Growth Stock Conference, CEO Bob Bruggeworth said: "We've been waiting a long time for this, but we are very pleased [with the decision]. We make components for all three of the standards issued."

While the W-CDMA and CDMA2000 standards are already well established, the 3G roll-out in China will represent the first outing for the People's Republic's home-grown TD-SCDMA protocol.

Anadigics, which believes that its long-standing business relationships with major handset companies in China gives it a unique insight into the country's 3G requirements, has TD-SCDMA products ready to ramp.

"[Our] AWT6241 power amplifier has been used in several TD-SCDMA designs that will ramp to production this year," Webber claimed. The AWT6241 is based on InGaP HBT technology and is suitable for both the home-grown Chinese standard and wideband-CDMA.

However, although the director of marketing believes that demand for 3G prod-



Verizon Wireless launched its Network Extender femtocell to improve signal coverage in the home in the US on January 26, for \$249.99. Manufactured by Samsung, which collaborates with GaAs chip maker Skyworks Solutions in this area, this is one of the first femtocell products released to consumers.

ucts will increase gradually as the Chinese networks expand, Anadigics' plans to build a GaAs chip fab in China remain on ice for now. "We have deferred investments in expanding our wafer capacity in China until such a time as customer demand requires it," said Webber.

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...Riber bucks trend with 2008 sales boom

The Paris-based MBE specialist's production epitaxy equipment sales jumped from 12 systems in 2007 to 15 in 2008, but the division's 2009 outlook remains uncertain. Its components and after-sales-service business has been buoyed by robust custom from the research community and rights to service MBE technology originating from VG Semicon – which Riber bought from Oxford Instruments in September 2008.

...Sumitomo Electric controls Eudyna

Sumitomo Electric will become the sole owner of Japanese compound semiconductor specialist Eudyna Devices when it buys Fujitsu's current 50% share on April 1. The

move will vertically integrate the company with the optical, transceiver and electronic device businesses of Sumitomo Electric, although Eudyna and Fujitsu will retain a close relationship.

...VPEC leaves LED epiwafer business

Taiwanese III-V foundry Visual Photonics Epitaxy Co. ceased operations in its LED business on January 15 and sold affected process equipment and LED patents to its compatriot Crystal Light Optotech. The company cited LED price erosion as the basis for its decision. Between 2006 and 2008, revenue from VPEC's ultra-bright red and yellow AlGaInP LED lines fell from 40% to just 18% of its overall revenue.

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DIODE LASERS

Quantum-dot VCSEL reaches 40 Gbit/s

German start-up VI Systems claims that it has produced the first single VCSEL to achieve error-free 40 Gbit/s data transmission through multimode fiber.

CEO Nikolay Ledentsov presented 20 Gbit/s performance data at the Photonics West event held in San Jose, CA, from January 24 to 29. However, he told *Compound Semiconductor* that since VI Systems' presentation topics were submitted the company has advanced its quantum-dot lasers to double that modulation speed.

"Now we have 40 Gbit/s serial transmission over multimode fiber using our VCSEL and our PIN photodetector module," Ledentsov said. The 850 nm-emitting record-breaking devices were produced using the same lithography masks as its 20 Gbit/s VCSELs, but with a modified epitaxial structure.

That design uses InAs quantum dots in a GaAs quantum well, embedded into an AlGaAs matrix to overcome the issues preventing conventional quantum-well VCSELs reaching such high speeds.

To double the data transmission rate in existing devices it would be necessary to increase current density four-fold, assuming other parameters of the laser cavity remain constant. Such increased current densities can reduce the lifetime of an 850 nm emitter by 400 times. Quantum-dot-based devices suppress lateral carrier diffusion, reducing defect formation and growth that leads to failure in quantum-well VCSELs.

Lasers that exploit quantum dots also benefit from low threshold currents and the 40 Gbit/s VCSEL is no exception, operating at just 10 kA/cm².

A number of emerging technological standards for data transmission call for the higher modulation rates offered by VI Systems' devices, Ledentsov points out. Technologies that currently achieve 40 Gbit/s use four transmitters and four receivers, but replacing this with fewer of each is preferable. "Serial transmission is the lowest cost, lowest power consumption solution," Ledentsov asserted.

VI Systems is currently taking orders for products based on the 20 Gbit/s technology that it presented at Photonics West. It operates on a fabless model, with its MBE-grown devices produced by foundries, and processing and characterization performed by Technical University, Berlin.

● QD Laser, Inc., the Japanese quantum-dot Fabry-Perot laser producer, has gained

¥700 million (\$7.8 million) to enhance its production capabilities and R&D activities.

The venture funding round was led by Mizuho Capital Co. Ltd with Tokyo Leasing Co. Ltd as an additional investor and founders Fujitsu and Mitsui also participating.

GaAs MANUFACTURING

Skyworks slows 6 inch wafer conversion



Landis and Gyr's wireless meters are helping drive Skyworks' expansion into energy management, using smart grid technology from start-up Eka Systems.

Skyworks Solutions' plan to begin manufacturing its GaAs products on 6 inch wafers has taken a knock as it reins in costs.

The wireless component maker held on to profitability in the last quarter of 2008, thanks in part to its control over expenses. Now it is executing a cost reduction plan that will delay the upgrade from 4 inch systems at its Woburn, MA, operation originally slated for completion this year.

"We have definitely slowed down that investment," Skyworks' chief financial officer Don Palette told financial analysts. "Right now our expectation is that we're going to go live with 6 inch early in 2010," he said in the conference call announcing the company's financial results.

The plan saw Skyworks lose 150 of its employees – 4% of its headcount – primarily from its transceiver development group in January. It expects that the resulting savings should amount to \$20 million annually.

Palette said that in the first three months of each calendar year he would normally expect Skyworks' revenues to fall 15% from the previous quarter. This year he expects that figure to be nearer to 20%, hence the need for further cost cuts.

This comes after the company's revenues at the end of 2008 – traditionally the strongest period of the year – fell nearly 10% from the previous quarter. Regardless of this, Skyworks still delivered \$22 million profit, down from \$35.3 million sequentially but

ahead of the \$19 million that it delivered in the same period in 2007.

It was able to offset the drop seen by other wireless semiconductor companies, thanks to demand from the latest smartphones and energy management systems. Sales of wireless metering products to vendors like Itron, Sensus, and Landis and Gyr increased by 30% in the quarter.

Production also ramped up for devices targeting smartphones, offsetting what management said was a consistent fall in revenues across the rest of its business.

PHOTOVOLTAICS

Metal-organics key to EU's III-V solar push

Novel metal-organic sources of germanium and silicon could hold the key to a new generation of multi-junction solar cells and ultimately to much cheaper solar-energy production in sunny climates.

Researchers leading the European drive towards commercialization of concentrating photovoltaics (CPV) systems believe that growing germanium epilayers in these cells will represent a crucial step in the development of the technology. The five-year, €11.7 million (\$15.3 million) project that they are working under – APOLLON – represents the biggest photovoltaics research effort funded through the EU's seventh Research Framework Programme (FP7) to date.

Gianluca Timò, who is coordinating APOLLON from the Italian research institute CESI Ricerca, hailed the initial meeting between the 16 project partners – held in Cyprus last October – as a great success.

The ambitious objective set for the APOLLON collaboration, which includes MOCVD reactor company Aixtron, is to develop CPV systems at a cost of €2 per watt of electricity produced.

The official cell supplier for APOLLON is Belgium-based Energies Nouvelles et Environnement who will grow new materials with a 1 eV bandgap. This may use epitaxial germanium alloys instead of InGaAs layers to improve quantum efficiencies.

"So far, InGaP/InGaAs/Ge structures have been realized with only the top and middle junctions epitaxially grown, while the third junction has been formed by atom diffusion into the germanium substrate," Timò explained.

According to the researcher, this process penalizes the third junction, because the dopant profile in the germanium lacks precision. This leads to a high surface recombination velocity at the interface between germanium and the first nucleation layer –

ultimately limiting cell performance.

Crucial to enabling this approach has been the relatively recent development of the metal-organic material isobutylgermanium, an innovation that may also lead to the first quadruple-junction InGaP/InGaAs/Ge-alloy/Ge solar cells.

Germanium epitaxy will also drive a bid to grow III-V cells on top of low-cost silicon substrates. Until now research teams have approached the lattice-mismatch problem by using plasma-enhanced CVD to create SiGe alloys on top of silicon, before loading these virtual substrates into an MOCVD reactor for subsequent III-V growth.

But under APOLLON, Timò and his collaborators will attempt to grow SiGe and III-V epilayers by MOCVD, exploiting new silicon precursors that decompose at lower temperatures than conventional sources.

• The APOLLON (multi-approach for high-efficiency integrated and intelligent concentrating PV modules) project officially started on July 1, 2008.

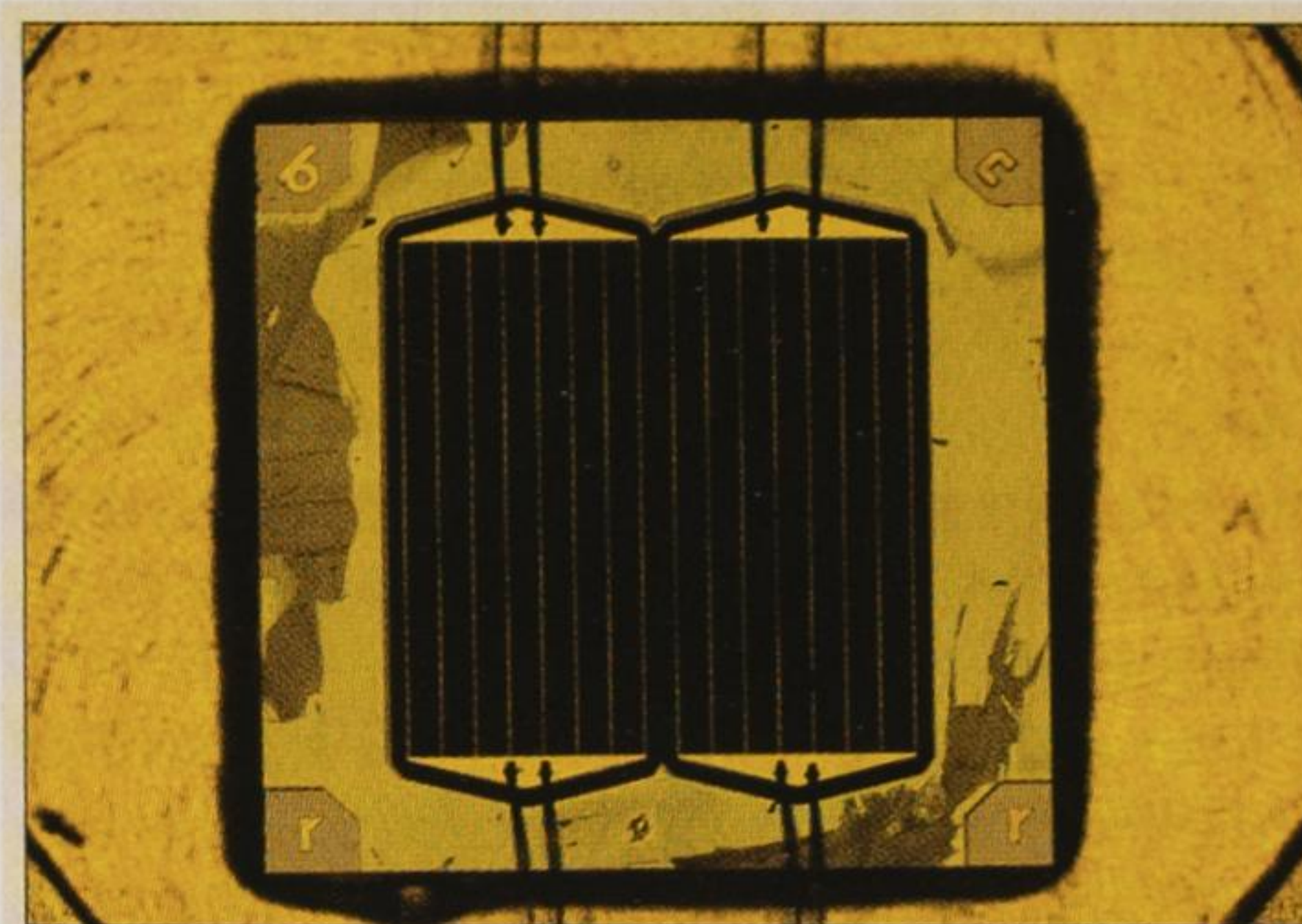
DEPOSITION EQUIPMENT

Veeco restructures despite LED strength

Veeco Instruments has embarked on a major restructuring effort, as the downturn takes its toll on the wider semiconductor industry.

"Our MOCVD systems business will go to a fully outsourced model by the end of the year," said CEO John Peeler in the company's Q4 earnings call. He also outlined a number of wider measures to cut costs, including a 26% reduction in workforce. Veeco will have less than 1000 employees by the end of 2009.

Demand for MOCVD and other epitaxy equipment remained strong through the closing months of 2008, however. Korean LED maker LG Innotek ordered four of Veeco's K465 MOCVD tools, while it



The title of most efficient individual photovoltaic cell has been wrested from the US National Renewable Energy Laboratory by Germany's Fraunhofer Institute for Solar Energy Systems. It has recorded 41.1% conversion efficiency in sunlight concentrated by a factor of 454, thanks to improved quality of compound semiconductor layers absorbing solar energy in the metamorphic triple-junction cells. The key innovation was optimizing a buffer layer that relieves strain between the $\text{Ga}_{0.35}\text{In}_{0.65}\text{P}$ top junction, $\text{Ga}_{0.83}\text{In}_{0.17}\text{P}$ middle junction and germanium bottom junction.

received another multisystem order from an unspecified maker of multi-junction solar cells. Of \$110 million sales in the final quarter of 2008, LED and solar applications accounted for \$37.6 million.

Total equipment sales for LED and solar applications, which includes thermal sources for CIGS deposition, reached \$166 million in 2008, representing 43% of overall Veeco sales and replacing data storage as Veeco's single biggest application market.

Orders for LED and solar-cell equipment also jumped 69% sequentially to \$44 million in the last three months of 2008. Although some LED manufacturers, particularly those in Taiwan, have delayed delivery of MOCVD equipment in recent weeks, Peeler does not believe that this will lead to substantial order cancellations.



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...Demand spurs II-VI's SiC output

Crystal growth specialist II-VI Incorporated says it has seen a marked increase in demand for 100 mm SiC substrates from Japanese manufacturers and US defense customers. Additionally, its Pine Brook, NJ, wide-bandgap group began shipping high-quality 3 inch diameter 4H conducting n-type wafers in the December quarter. II-VI also released 100 mm 6H semi-insulating substrates in January and

will complete 100 mm 4H n-type substrate development before the end of March.

...SolFocus raises another \$47.5 m

The Californian concentrator photovoltaic system developer has successfully closed its third venture-funding round, which it plans to use to firmly move into commercialization. Mark Crowley takes over as CEO from founder Gary Conley to oversee the transition.

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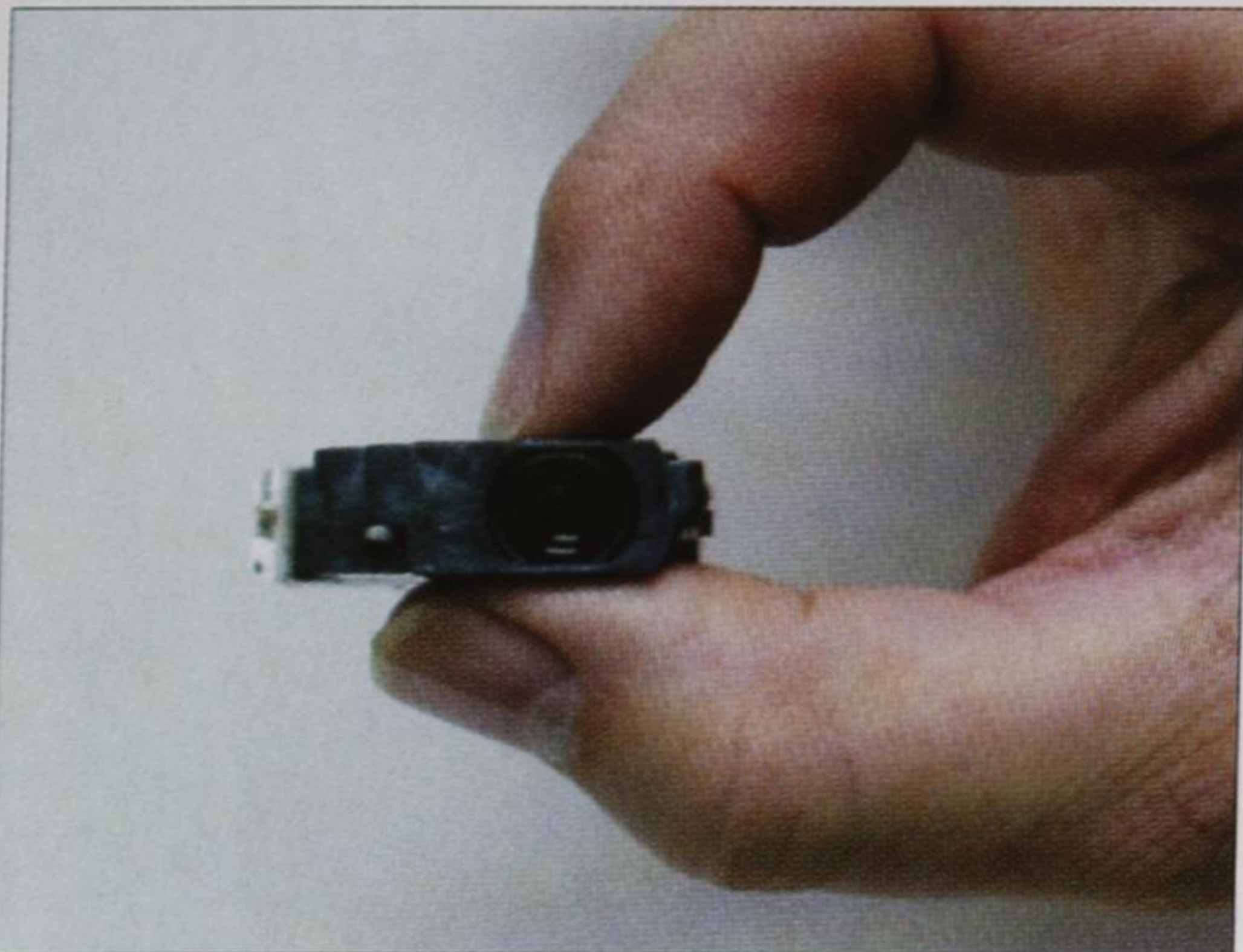
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LIGHT ENGINES

Display producers exhibit LED power



3M's MM200 pico-projection light engine is illuminated with multicolored LEDs and uses an advanced liquid crystal-on-silicon electronic imager.

LEDs provided the ammunition as the world's leading electronics manufacturers battled at the 2009 International Consumer Electronics Show (CES) for the position of thinnest TV and smallest projector.

A hitherto unseen level of high-profile display announcements at the January show revolved around the sleek profile, high-quality images and energy saving promise that LEDs bring. Samsung led the skinny LCD television pack at the Las Vegas, NV, event from Korean compatriot LG and Japanese brand JVC.

LED backlights feature in Samsung's high-profile Series 7 models that range in size from 40 to 55 inches and boast 240 Hz refresh rates. These combine enhanced image quality and efficiency with an internet TV service from Yahoo! in the narrowest TVs reported at CES, at just 6.5 mm.

A hair's breadth wider was JVC's 7 mm thick, 5 kg, 32 inch prototype, while LG emphasized the "astonishing" picture quality of its 55 inch, 23.8 mm thick LCDs. Cur-

rently none of these models has an official price. However, the 9.9 mm thick Sony ZX-1 LED-backlit TV – the thinnest currently available – has recently hit the market in Europe at around \$5000.

Dell, Toshiba, Acer and Samsung also unveiled battery-powered mobile display projectors that use LEDs to provide a combination of efficiency and image quality.

Acer and Dell's projectors are the size of a pocket dictionary, to be carried in a bag alongside a notebook computer. The K10 projector that Acer promoted at CES was revealed as using LEDs from US manufacturer Luminus Devices during the show. The K10 will soon be available for \$450, while Dell's M109S projector is \$499.

Toshiba and Samsung continue the theme with pocket-sized products intended to interface with computers and mobile devices.

CREDIT CRUNCH

Solar partner critical to Emcore's prospects

Compound semiconductor component and subsystem producer Emcore is looking to investment in its photovoltaic division to keep it afloat after another quarter of losses.

"Last month we signed a letter of intent with a major international investment group," explained CEO Hong Hou on February 10. In the conference call with analysts to discuss financial results for the last three months of 2008, Hou underscored the importance of the conglomerate's backing. He explained that the partner will provide funds for major concentrating photovoltaic (CPV) installation deals in a more flexible way than banks are currently able to.

After Emcore reported a \$52.5 million quarterly loss – impacted by a \$33.7 million devaluation of its recent acquisitions – such a partner appears a vital development. The company had just \$18.8 million in cash and

had used \$15.4 million of its \$25 million credit at the Bank of America at the end of 2008. Since then, however, Emcore has sold investments to provide it with another \$14 million. "We are still consuming cash," warned the CEO.

Hou says that the prospective collaborator would "organize equity investment" capital that will allow Emcore to produce, install and maintain CPV systems for major deployments. That could play a crucial role in the southwest US project for up to 80 MW of systems that Emcore has been shortlisted for after passing basic technology qualification. Emcore and its partner submitted a joint bid to the utility company assessing the systems, which will progress the project further in the second half of 2009.

Solar-cell manufacturing at Emcore has gained a boost after the signing of official supply agreements with two companies that have had their CPV systems qualified for the Spanish market. It also signed a \$70 million contract in December to provide cells for satellites, a business in which Hou says Emcore still has relatively good visibility.

GaAs-based cells contributed to year-on-year and quarter-over-quarter increases in revenue for Emcore's photovoltaic business. At \$14.9 million, this is a \$2 million increase over the same period in 2007 and \$400,000 better than the previous quarter.

Sales of fiber-optic components fell 15% sequentially to \$39.2 million but the businesses acquired from Intel actually pushed revenues up 15% from the same period in 2007. However, the adjustment to what it can now reasonably value that business at contributed to the \$33.7 million addition to its losses. The company now expects fiber-optic component sales to fall up to 15% in the current quarter.

Cost reductions – including 160 job losses – have been made and the firm will work to further improve its operating efficiency to try and offset the sales decline. "We're off to a rough start in fiscal 2009," Hou said.



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...JDSU hands packaging to Sanmina

The optical technology firm is transferring the Shenzhen, China, facility where it packages many of its communications modules to its Californian neighbor Sanmina. The site and the 2000 employees will be owned by the manufacturing services provider by April. The move was announced a day prior to JDSU recording a \$700 million quarterly loss, driven largely by revaluations of prior acquisitions.

...Finisar cuts 200 jobs

Finisar – the Sunnyvale, CA, fiber optic subsystem firm – is laying off 200 employees, 17% of the total workforce, excluding operations in Malaysia and Shanghai. It has also reduced most of its workers' salaries by 10%. These cuts come as Finisar warns that revenues for the quarter ended February 1 will be approximately \$137 million, down 14% sequentially.

...Correction: QPC Lasers

In our December 2008 issue, we stated incorrectly that QPC Lasers had filed for bankruptcy. In fact, the Californian company remains a going concern. As this issue went to press it was negotiating with creditors and investors to secure its future although the likelihood of some sort of bankruptcy filing remains, with some creditors demanding cash payments. We apologise for the error.

WIDE-BANDGAP SEMICONDUCTORS

Europeans aim to complete GaN chain

Engineers are eagerly awaiting the results of the first batch of GaN wafers fabricated under a new European research project that could kick-start the region's development of the wide-bandgap semiconductor.

The GREAT² project, which officially began in June 2008 with €8.6 million (\$11.4 million) backing from the European Space Agency (ESA), is scheduled to deliver its first results this spring.

According to the project co-ordinators, the lack of a reliable GaN device manufacturing process and space-compatible component supply chain has been a "missing link" in Europe's semiconductor expertise.

"If Europe's space industry is to maintain its competitiveness, then it needs guaranteed access to leading-edge GaN technology," said the ESA.

Talking to *Compound Semiconductor*, ESA's Andrew Barnes highlighted that the major challenge is providing sufficiently reliable devices. As a result, many of the key technical milestones in the first, three-

year, phase of the project relate to improvements in the mean-time-to-failure metric. This currently stands at approximately 1000 hours, but the project is aiming for a 1000-fold improvement.

"By 2011 we hope to have a preliminary space-compatible process, and to make the process available for defense and aerospace applications. The aim is to build a European supply chain for GaN," said Barnes.

Ultimately, GaN technology should result in major benefits for ESA. Among these is the increased RF output power capability for microwave signal transmission back to earth. Assuming that phase one of the project goes according to plan, phase two is expected to begin in 2011, with anticipated support of €4 million.

The full list of GREAT² project partners comprises: TESAT Spacecom (project management); IMEC (epitaxy optimization); the Ferdinand Braun Institute for High-Frequency Technology (reliability and transistor processing); the Fraunhofer Institute for Applied Solid-State Physics (epitaxy and MMIC processing); UMS (technology transfer and process development); the University of Bristol (thermal analysis); and the University of Rome Tor Vergata (device physics modeling).

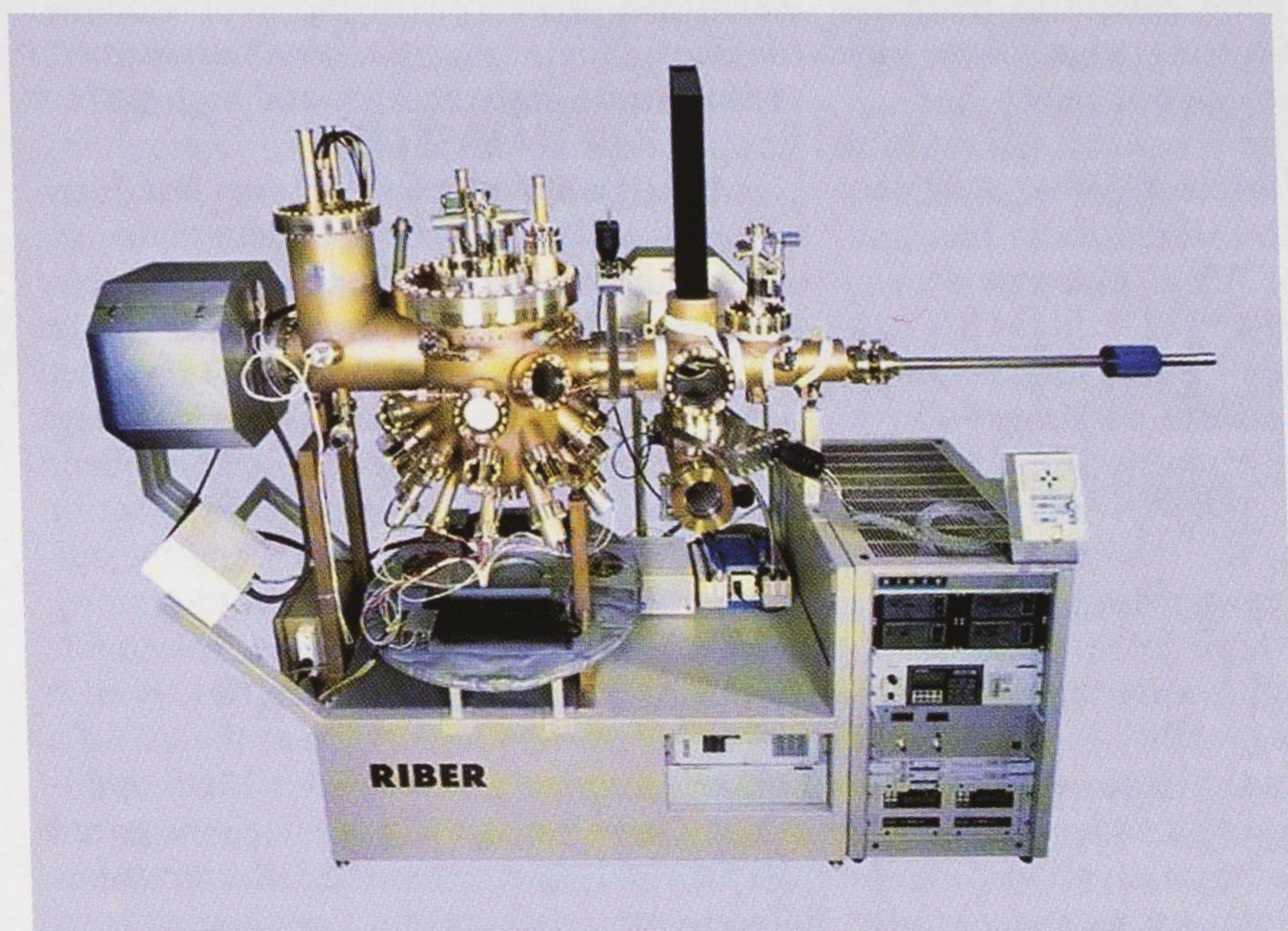


Mario Rivas became president and CEO of Anadigics on February 1. Before joining

the Warren, NJ, GaAs chip manufacturer Rivas served as CEO of Quartics, a fabless semiconductor and software company. Prior to that he was a senior executive at AMD and had managed Philips Semiconductor's wireless communications business. Rivas spent the bulk of his career at Motorola, with responsibilities in both semiconductor and wireless communications.

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RF ELECTRONICS

PA makers: demand plunge leveling out

RF Micro Devices (RFMD), the leading manufacturer of GaAs-based RF components, says that demand for its products is stabilizing, following a precipitous drop at the end of last year.

The company reported a 25% decline in sequential revenues to just over \$202 million and massive write-downs relating to acquisitions and the closure of its 4 inch wafer fab in Greensboro. CEO Bob Bruggeworth told investors: "Muted consumer activity in November was particularly challenging, with orders dropping week on week. This was compounded by excess inventories due to the [previously] expected December growth. In the first weeks of December, there were signs of improvement and, today, inventories are beginning to level off. However, visibility remains very limited and our customers are unable to pinpoint any return to normalized demand."

Taken at face value, RFMD's net loss for the December quarter – more than \$813 million – looks shocking. However, the vast majority of that loss relates to non-cash charges reflecting adjustments to the firm's balance sheet. And when those charges are stripped out, RFMD's net loss for the December quarter shrinks to just under \$13 million.

Of the non-cash charges, by far the most significant is the write-down of goodwill that relates to the company's 2007 acquisition of Sirenza Microdevices, which at the time cost RFMD \$300 million in cash and \$600 million worth of stock. With Sirenza's paper value dropping along with virtually everybody else's in the intervening months, this change had to be reflected on RFMD's balance sheet.

This accounted for \$673 million out of \$754 million in exceptional charges. An additional \$47 million related to the write-down of the 4 inch wafer fab and equipment, which RFMD has "no plans" to reopen at the moment.

● GaAs chipmaker TriQuint saw a similarly dramatic 20% sequential revenue decline to \$149 million in the final quarter of 2008. However, that did not prevent the company from recording its best-ever annual revenues of \$573.4 million.

Although it expects sales to again fall below \$120 million in the current quarter, TriQuint is still targeting another annual revenue record in 2009. Its focus on smartphones appears to be serving it well, after the company won its largest-ever number of

inclusions in handset designs in the December quarter last year.

"Underlying the slowdown, I remain excited about the expanding content of RF in smartphones, wireless broadband and military applications," said CEO Ralph Quinsey. "I have low visibility into 2009, but we will remain focused on innovation, efficiency and growth. This focus will allow us to take advantage of opportunities we have and emerge from these troubled times as a stronger company."

Some cost-cutting measures have been put in place, but as TriQuint is debt-free it plans to now invest modestly in making its operations more economical. While its fabs are operating some way from their capacity, the company is intending to reduce the time taken to manufacture products.

These efficiency drives will not have been helped by the call out of a hazardous material incident team to TriQuint's Hillsboro, OR, site after an employee spotted bubbling in a metal plating solution. A small team preparing the site for restart in the New Year unintentionally combined 15 gallons of gold plating solution containing 2% cyanide and six gallons of tin plating solution containing 5% sulphuric acid. Despite needing to call in authorities, there were no injuries or environmental impact.

POST-SILICON LOGIC

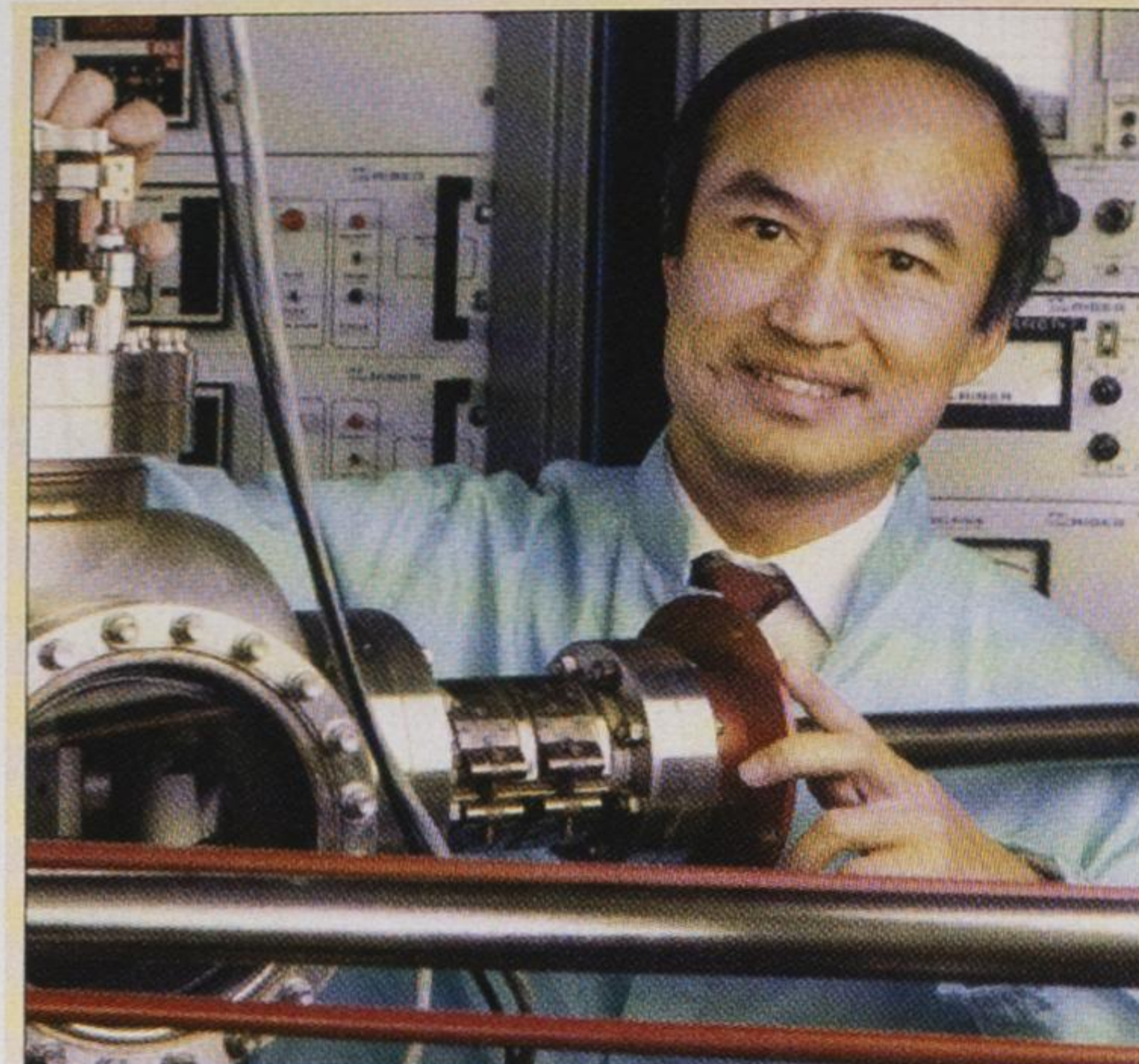
IBM shrinks III-V MOSFET gate lengths

Computing giant IBM has made InGaAs MOSFETs that come closest to matching the dimensions of cutting-edge silicon logic devices of any fabricated to date.

A team from the company's New York TJ Watson Research Center describes 160 nm gate length transistors in the January 2009 issue of *IEEE Electron Device Letters*. "To evaluate III-V logic it's critical to produce MOSFETs with gate length comparable to the state-of-the-art silicon devices," explained Yanning Sun, a member of the IBM team.

At the same time the researchers tackled surface states, a key performance-limiting issue for III-V MOSFETs, by passivating the devices with amorphous silicon. "Effective channel mobility in a MOSFET can be greatly degraded if the interface state density is high," Sun told *Compound Semiconductor*. "The α -Si passivation reduces the interface state density by successfully removing the III-V native oxides."

Without using its passivation technique the team's longer-channel 5 μ m gate length devices reached 1280 cm^2/Vs



Bell Labs luminary Al Cho will be inducted into the US National Inventor's Hall of Fame on May 2. MBE innovator Cho is a lone III-V industry figure among 14 semiconductor scientists – including Intel's Gordon Moore – being honored to celebrate the 50th anniversary of the integrated chip. He adds the accolade to the National Medal of Science and the National Medal of Technology that he already owns.

peak effective carrier mobility. When the approach was exploited it enhanced this to 3810 cm^2/Vs , determined at a carrier density of $1.8 \times 10^{12} \text{ cm}^{-2}$, a figure that Sun says is among the best.

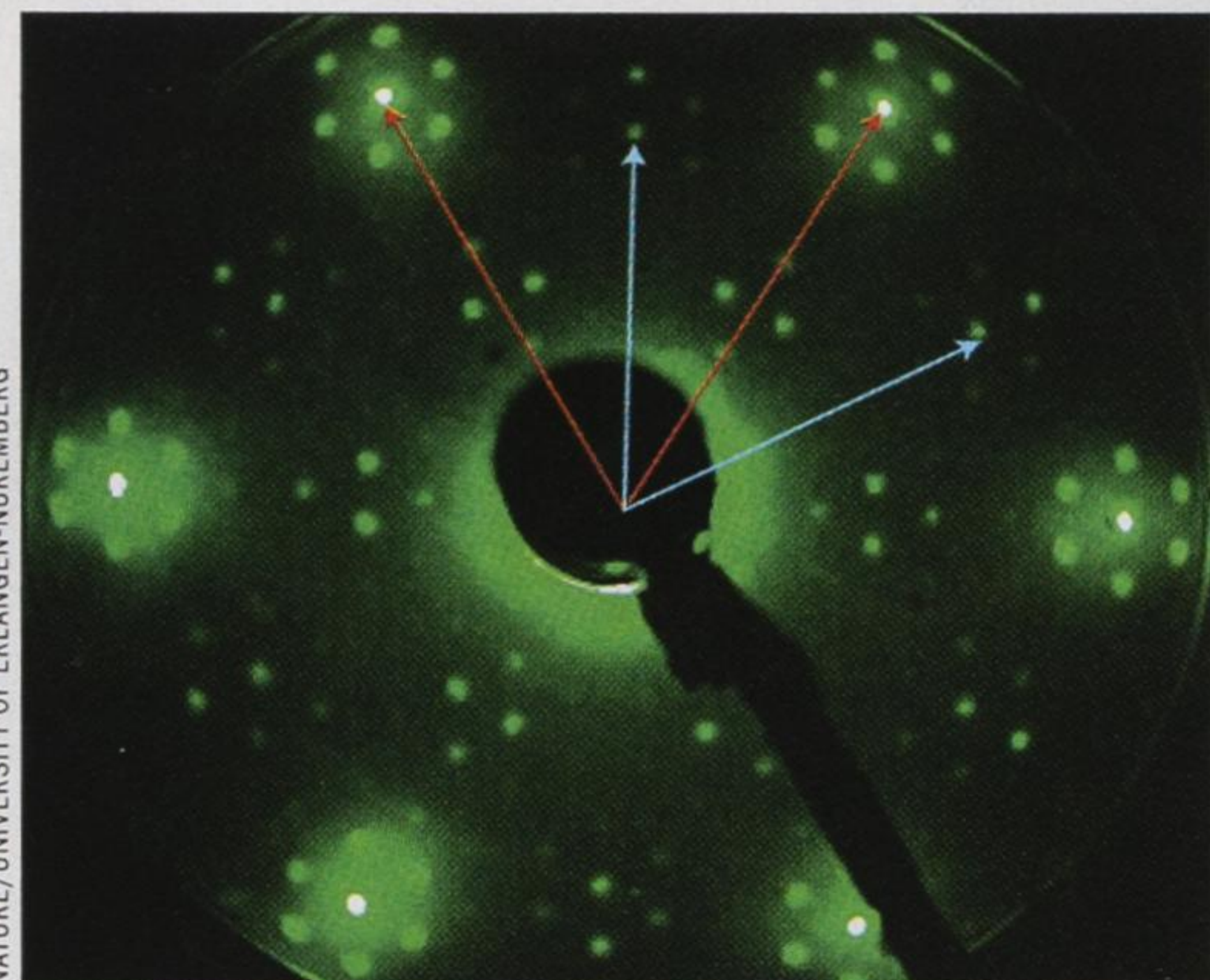
"III-V MOSFETs' effective channel mobility needs to be sufficiently higher than that in silicon devices to be considered for logic application," she explained. "However, the high mobility extracted from long-channel devices can not necessarily be preserved in the short-channel devices. Therefore, it's very important to demonstrate high mobility and high current in scaled III-V MOSFETs."

Although carrier mobility was not determined for IBM's 160 nm gate length device, a related property – virtual source velocity – was up to 1.7 times higher than silicon MOSFETs. The InGaAs transistor operated with a drain current of 825 $\mu\text{A}/\mu\text{m}$. Sun says that the short-channel devices had not been produced previously because fabrication processes are complicated and lengthy, currently requiring electron-beam lithography.

The MOSFETs' buried gate was made from a high-k dielectric material, with a large gate overlap region due to the use of a non-self-aligned process. For CMOS applications, a self-aligned process is required and Sun points out that the IBM team has already demonstrated such a scheme for its InGaAs MOSFETs. She also says that the team is now working on the high-k gate and α -Si deposition processes to further improve the interface with the III-V layers.

NEW MATERIALS

Argon enhances graphene-on-SiC



Diffraction spots from the well ordered graphene lattice (red arrows) and the SiC(0001) substrate (blue arrows) from LEED at 74 eV. The extra spots are due to a $(6\sqrt{3} \times 6\sqrt{3})$ interface layer.

German and US researchers have driven forward methods for producing graphene by annealing SiC substrates, producing the largest homogeneous epitaxial domains of the carbon material yet described.

The team, led by scientists from the University of Erlangen-Nuremberg, found that heating SiC in argon produces significantly better quality graphene than methods using ultra-high vacuum conditions. Analyses of the resulting samples at Erlangen and at the Fritz-Haber-Institute, Berlin, and Lawrence Berkeley National Laboratories, California, showed graphene terraces up to $3\mu\text{m}$ wide and $50\mu\text{m}$ long. This compares with 30–200 nm for the vacuum approach.

The group's progress towards effectively producing the single monolayer of graphite material was published online in *Nature Materials* on February 8. "We can unambiguously conclude that the large atomically flat macro-terraces are homogeneously covered with a graphene monolayer," wrote author Thomas Seyller in the paper.

"We were looking for practical ways to avoid the ultra-high vacuum environment for graphene growth, which is almost impossible to scale up to mass production," Seyller told *Compound Semiconductor*. Using a type of vertical cold-wall reactor that has performed post-growth annealing, it seems that the goal has been attained.

"It appears much simpler than the growth under ultra-high vacuum," said Pierre Mallet, a leading graphene researcher at Institut Néel in France. "I believe many labs and companies will try to synthesize their own epitaxial graphene-on-SiC using this method."

Graphene is formed as silicon evaporates

from the SiC substrate and the 900 mbar argon atmosphere that the researchers use reduces the rate at which this occurs. The argon deflects silicon atoms back towards the substrate, meaning that silicon desorption doesn't begin until 1500°C , compared with 1150°C for the vacuum method.

Erlangen's annealing method therefore occurs at 1680°C , enhancing diffusion of silicon and carbon atoms and improving surface morphology compared with the 1280°C vacuum method. A homogeneous layer is important because a single monolayer of graphene is a gapless semiconductor, but additional carbon monolayers change the film's electronic structure.

Previously, large epitaxial graphene films have been formed on the transition metal ruthenium, but for this to be useful electronically the fragile graphene layer must be transferred to an insulating substrate. By using the insulating, on-axis, Si-terminated, Si(0001) wafers produced by substrate vendor SiCrystal, Seyller and his colleagues had a clear advantage.

Electron mobility measurements showed a highest value of $2000\text{ cm}^2/\text{Vs}$ for graphene grown in argon, compared with $710\text{ cm}^2/\text{Vs}$ for vacuum-grown material. This is well short of the $200,000\text{ cm}^2/\text{Vs}$ reported by the discoverers of graphene at the University of Manchester, UK.

"Compared with exfoliated graphene, the mobility of our epitaxial graphene films is still below expectations," Seyller conceded. "We need to understand the reasons for this and develop strategies for improvement."

Mallet suggests that the price of SiC substrates and the vertical cold-wall reactor used could also be off-putting to some, but he is generally enthusiastic about the method. "The impact will be very high," Mallet said. "Not only the graphene-on-SiC community should be interested, but the entire condensed matter community."

SUBSTRATES AND EPIWAFERS

AXT: IQE wafer deal renewal key for 2009

AXT is emphasizing its contract wins, after revenues for the last quarter of 2008 slumped by more than 25% from its expectation.

Epiwafer manufacturer IQE has agreed a \$14.3 million deal to meet its 2009 requirements for 4 and 6 inch semi-insulating GaAs substrates, down from \$18.6 million in 2008.

With AXT's quarterly sales set to reach just \$15.9 million, compared with a prediction of \$21.9 million, chief financial officer Wilson Cheung underscored the agreement's significance. "The important news



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...Opto is lone bright spot in 2009

Market analyst iSuppli says that the market for laser diodes will grow by nearly 8% this year, with LEDs expanding by 2.9% and other optoelectronics growing 0.6%. The rest of the semiconductor market is expected to show an overall decline in value of 9.4% on 2008. The San Jose-based consultancy reckons that the markets for analog ICs and RF and microwave components will decline by 15% and 20%, respectively, this year.

...SMI expands MOCVD despite slowdown

Structured Materials Industries Inc. has signed a licensing deal with rival equipment manufacturer Veeco Instruments to broaden its SiC reactor offering and meet demand for induction heating. The Piscataway, NJ, firm has gained rights to US patent 6,368,404 from the larger MOCVD tool maker to expand its offered range of heating technologies.

is that we've renewed the IQE contract," he told analysts at the Needham Growth Stock Conference in New York on January 6. "This will help ensure that we have an extremely high level of capacity utilization."

Cheung also revealed a further potential revenue boost, as AXT has gained top LED manufacturer Philips Lumileds as a customer for semiconducting GaAs in 2009. His company will supply substrates for the firm's cutting-edge red-orange-yellow emitter manufacturing, although not in the 6 inch diameters that some substrate suppliers suggest blue LED manufacture is nearing.

AXT's financial health is bolstered by the low costs of its Beijing, China, based manufacturing and self-built crystal growth furnaces. The Beijing facility has large amounts of space to expand into, allowing the company to respond quickly to changing demand. Cheung predicts that this will help it take substrate market share as GaAs manufacturers move further towards 6 inch manufacturing into 2009 and 2010.

● IQE ended 2008 on a bullish note, after its revenues rose 20% from 2007 to £60 million (\$85 million). These results are in line with its prior expectations and are expected to generate a positive cash flow.

The UK company has implemented cost cuts – including a few job losses – in the face of the recession. However representatives of IQE told *Compound Semiconductor* that based on what they were seeing, they did not expect the wireless industry to fare as badly as it did in the recession of 2001.

Planar regrowth simplifies phot

Photonic integrated circuits are notoriously difficult to make, but the combination of HVPE and MOCVD can substantially simplify the fabrication of monolithic transceivers, routers and waveform generators on an InP platform, says a multinational research team.

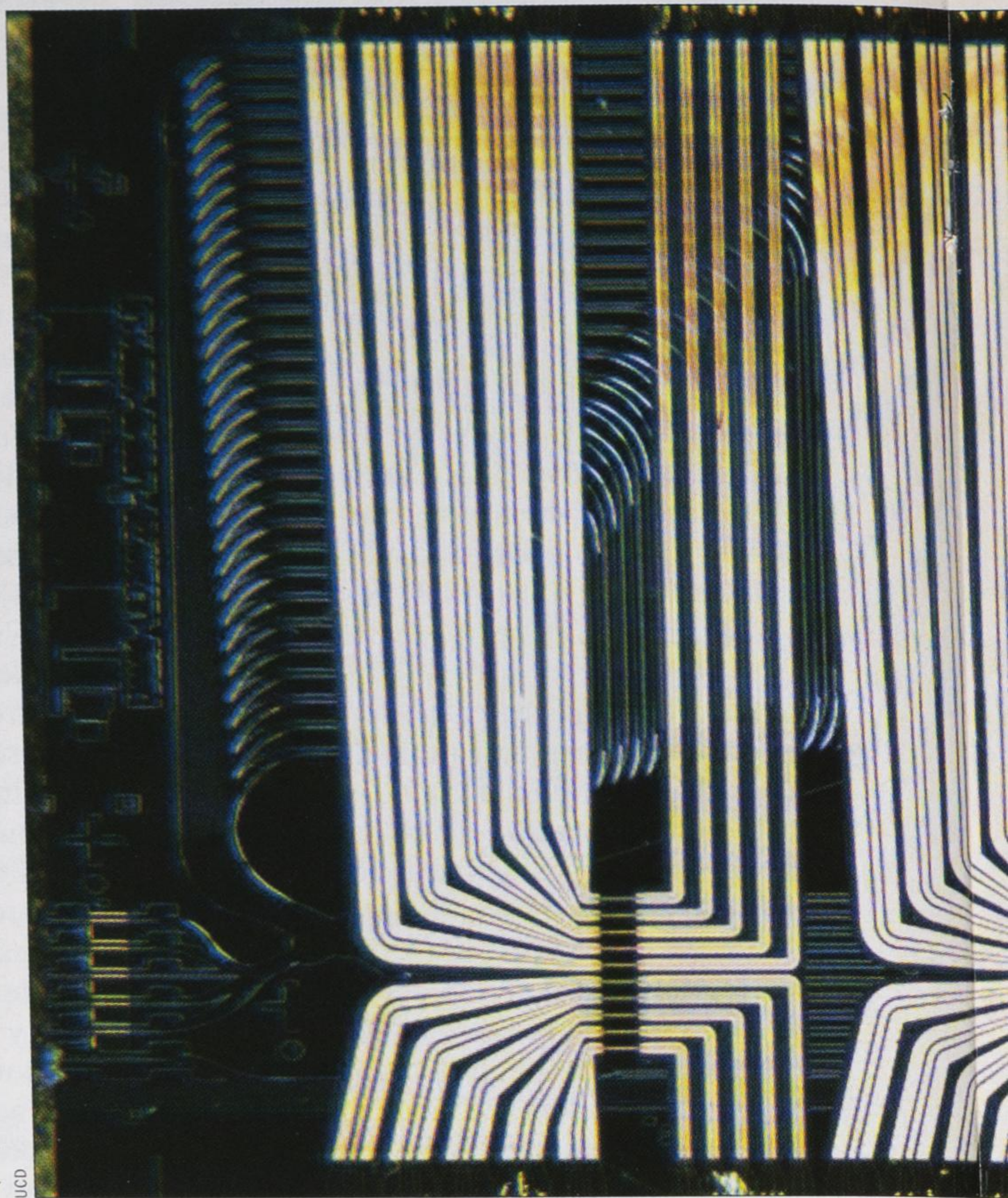
Rapid growth of multimedia communications, video streaming and file transfer activities are driving capacity increases in broadband connectivity to the internet. And internet traffic increases are set to continue, thanks to the introduction of new communication and entertainment services that include real-time interactive high-definition video with stereographic and even holographic images. Several companies are pioneering these systems and in 2011 the Japanese broadcasting corporation NHK plans to start experimental transmissions of its ultra-high-definition broadcast, which features a picture resolution that is 16 times greater than that of HDTV.

In terms of numbers, today's internet traffic in the US already exceeds 5 Tbit of data every second, according to AT&T, and by 2015 this figure will be 1000 times greater. This will place even more demand on network infrastructure, including the routers and switches in central offices.

Routers are already substantial pieces of equipment. For example, Cisco Systems' highest-capacity version for core networks, the CRS-1, weighs more than 50,000 kg and uses 1152 slots of line cards in 80 shelves to operate at 46 Tbit/s. Its energy consumption hits 0.85 MW, partly due to the very large cooling system required, and results in a staggering annual electricity bill of \$1.5 million. Clearly building larger routers is a highly undesirable approach to addressing the growth in internet traffic, both from an environmental and commercial standpoint.

Fortunately, photonic integration – the construction of optical circuits that unite various discrete components, including mode-locked lasers, optical switches (wavelength converters), arrayed waveguide gratings and modulators, on a single chip – can deliver tremendous miniaturization and lead to lower cost, more-efficient systems for the internet.

The inefficiencies in today's communication systems stem from excessive electronic processing, with each bit stored, processed and then sent forward by high-speed electronics. By switching to the photonics domain, data and signal processing can serve similar purposes while consuming very little energy. These benefits have already been realized in reconfigurable optical add-drop multiplexers with smaller IP routers, and carriers around



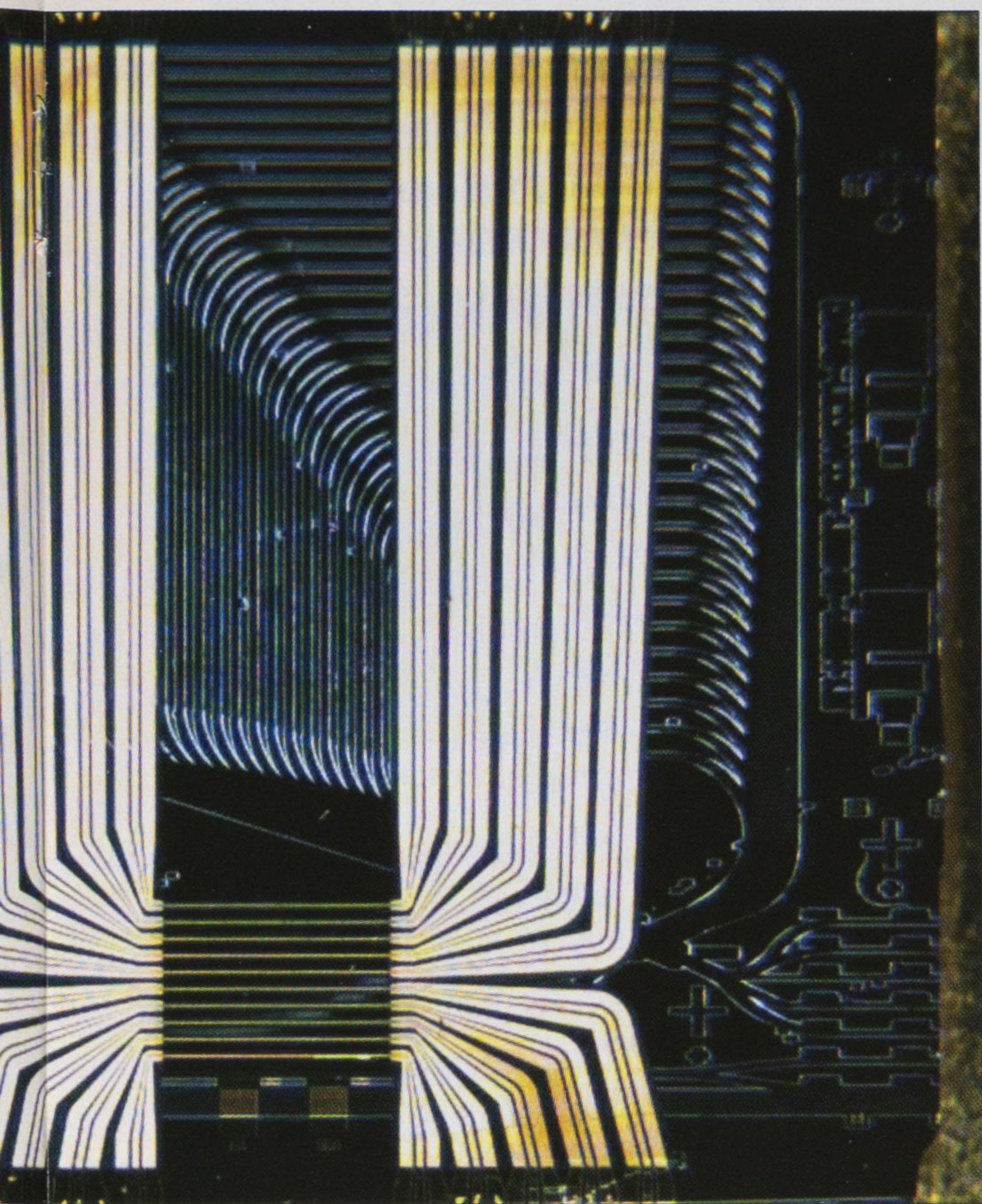
Various photonic integrated circuits have been built by researchers at the University of California, San Diego. These circuits include a monolithically integrated optical code-division multiple access (CDMA) generator, which is shown above, and an optical router on a chip that interfaces with

the globe are now using these components in preference to very large equivalents.

Several other benefits result from the replacement of hundreds or thousands of discrete modules with a single chip. Almost no optical power is lost at interfaces between components, and a single large chip is more affordable and easier to package than many small chips, which collectively consume more space and power. Replacing many chips with just one improves reliability by cutting the number of optical joints and a single thermoelectric cooler (TEC) can take the place of a handful of TEC units. A single photonic chip also has the potential to introduce new functionality and operate at faster speeds.

Although many benefits are associated with photonic integration, it is notoriously difficult to create these large, complex chips. The integrated fabrication process flow has to simultaneously produce all of the different types of device on a single chip and deliver a high manufacturing yield to realize the potential cost benefits.

Photonic integration of InP chips



the University of California, Davis, the Royal Institute of Technology, Sweden, and de-division-multiple-access (O-CDMA) transceiver system, an arbitrary waveform faces with electronics to create a very compact, low-power system.

Process optimization is crucial and the key challenge is to devise a series of fabrication steps that can maximize the performance of many different components. Any changes must deliver a universal benefit across the various active elements, including lasers, optical amplifiers, switches and passives such as waveguides, splitters and couplers.

The challenge of producing high-performance photonic integrated circuits has attracted several research teams around the globe. These include the vertically integrated communication-system company Infinera, the UK's Center for Integrated Photonics (CIP) and our team – a partnership between the University of California, Davis, the Royal Institute of Technology, Sweden, and Multiplex, Inc.

Infinera is the leading maker of photonic integrated circuits and its success at the systems level has catapulted the company to the number-one spot for deployment of long-haul fiber-optic backbone technology. The Californian company doesn't disclose the details of its InP monolithic chip technology, but

its integration process probably involves MOCVD-based material growth and regrowth, shallow etching of curved waveguides, iron-doped InP regrowths and p-type InP regrowth.

Ipswich-based CIP employs a form of hybrid technology that combines silica waveguides and InP semiconductor optical amplifiers. Mixing different materials has its downsides, however, such as greater manual handling, which leads to higher labor and production costs and less-robust chips.

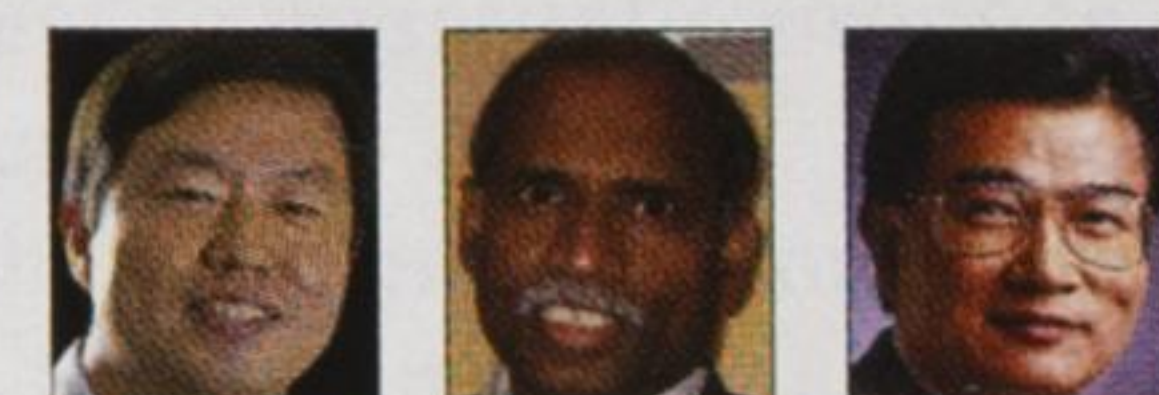
Like Infinera, our approach involves large-scale photonic integration, but we have the benefit of a more straightforward integration process that exploits judicious use of MOCVD and HVPE technologies. MOCVD growth produces the complex heterostructures, but it is not ideal for regrowth steps that fill in lower regions to produce the planar structures that are needed to complete the waveguides. This is because vertical growth takes place and forms "ears" that protrude in and outwards. HVPE does not suffer from this weakness thanks to lateral growth that is independent of crystal orientation.

Our efforts began by developing and refining a fabrication process for producing the building blocks for photonic chips, including mode-locked lasers, Mach-Zehnder interferometer (MZI) optical switches/wavelength converters, arrayed waveguide gratings (AWGs), amplitude modulators and phase modulators. Producing all of these devices involves a well defined process flow of selective etching of active quantum wells, MOCVD regrowth of p-type InP and a contact layer, waveguide definition and dry etching, HVPE iron-doped InP lateral regrowth, and metallization (figure 1, p16). Using this process flow, many building blocks can be put together into a larger system-on-a-chip.

One of HVPE's strengths is its ability to produce complete planarization, regardless of the mesa's orientation and height. Because of this, our complex devices can accommodate AWGs and MZIs that feature waveguides curving to all directions.

Other photonic integrated circuit developers, such as Infinera, don't enjoy the benefits of a highly effective lateral growth process. This hampers further integration and additional MOCVD regrowth steps are needed after shallow etching to produce planarization. The absence of HVPE also dictates the use of high-mesa waveguides (as pursued by NTT researchers), which are more difficult to define precisely and produce higher scattering losses.

Some researchers avoid issues associated with MOCVD regrowth by turning to quantum-well intermixing technology. Passive and active elements can be integrated by locally converting wells



About the authors

SJ Ben Yoo (left; yoo@ece.ucdavis.edu) is professor of electrical and computer engineering at the University of California, Davis, and director of CITRIS (center for information technology research in the interest of society). He develops photonic and electronic integrated systems for future communication and computing applications.

Sebastian Lourduoss (center) is professor and head of the Laboratory of Semiconductor Materials. His interests include monolithic photonic integration on InP for O-CDMA, and III-V-on-silicon technologies for nanophotonics and optical interconnects. **Won T Tsang** (right), president and CEO of Multiplex, Inc, pioneered the development of chemical beam epitaxy. He is also the inventor of the graded-index-separate-confinement heterostructure, which forms the heart of high-performance quantum-well lasers for optical fiber communication applications. The authors appreciate the support of DARPA and SPAWAR under agreement number N66001-01-1, and DARPA/DSO OAWG under agreement number HR0011-05-C-0155.

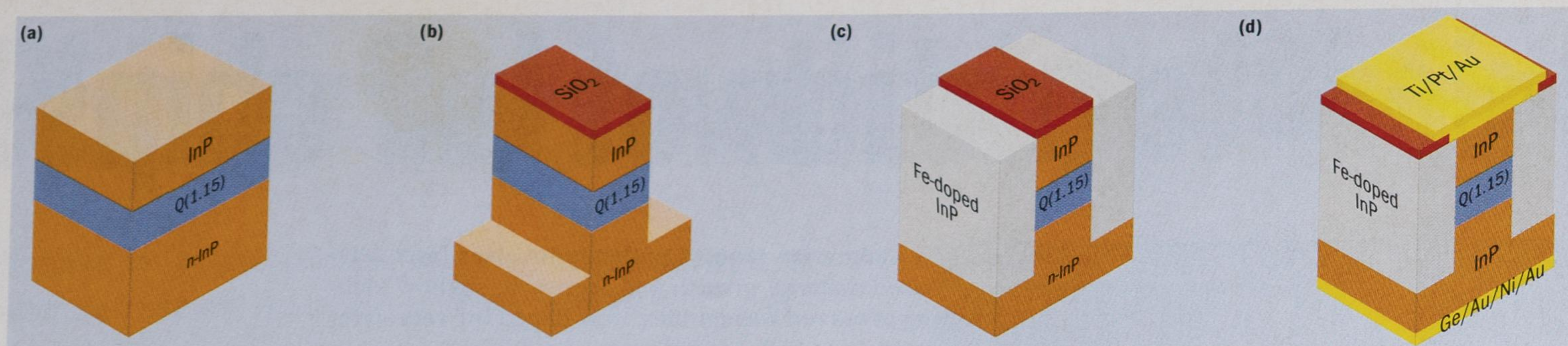


Fig. 1. Photonic integrated circuit fabrication begins with MOCVD growth of the epitaxial structure that involves quaternary (Q) material **(a)**. This is followed by the photolithographic definition of waveguides and dry etching **(b)**, HVPE lateral regrowth **(c)**, and lapping and metallization to complete the integrated device **(d)**.

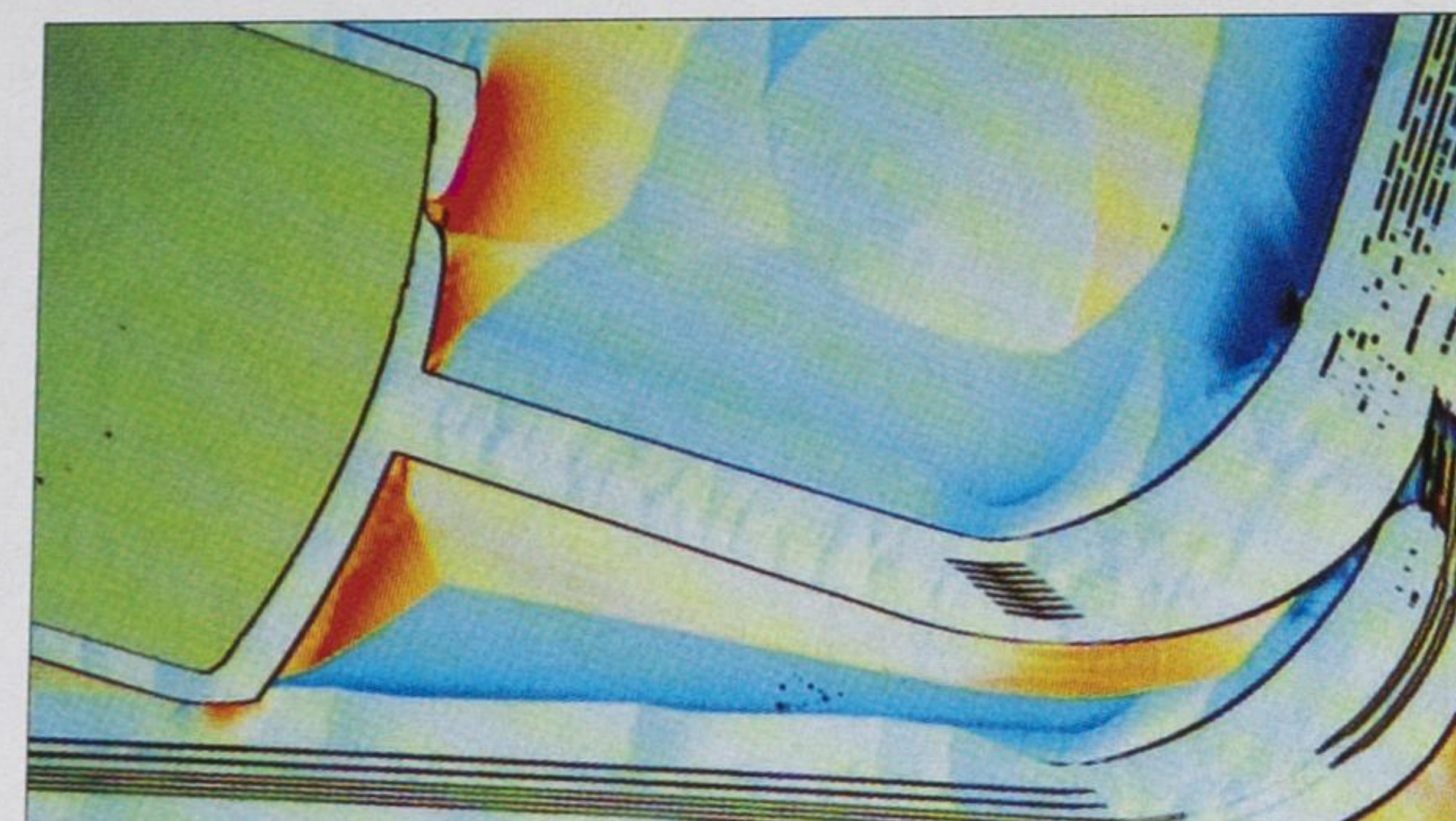
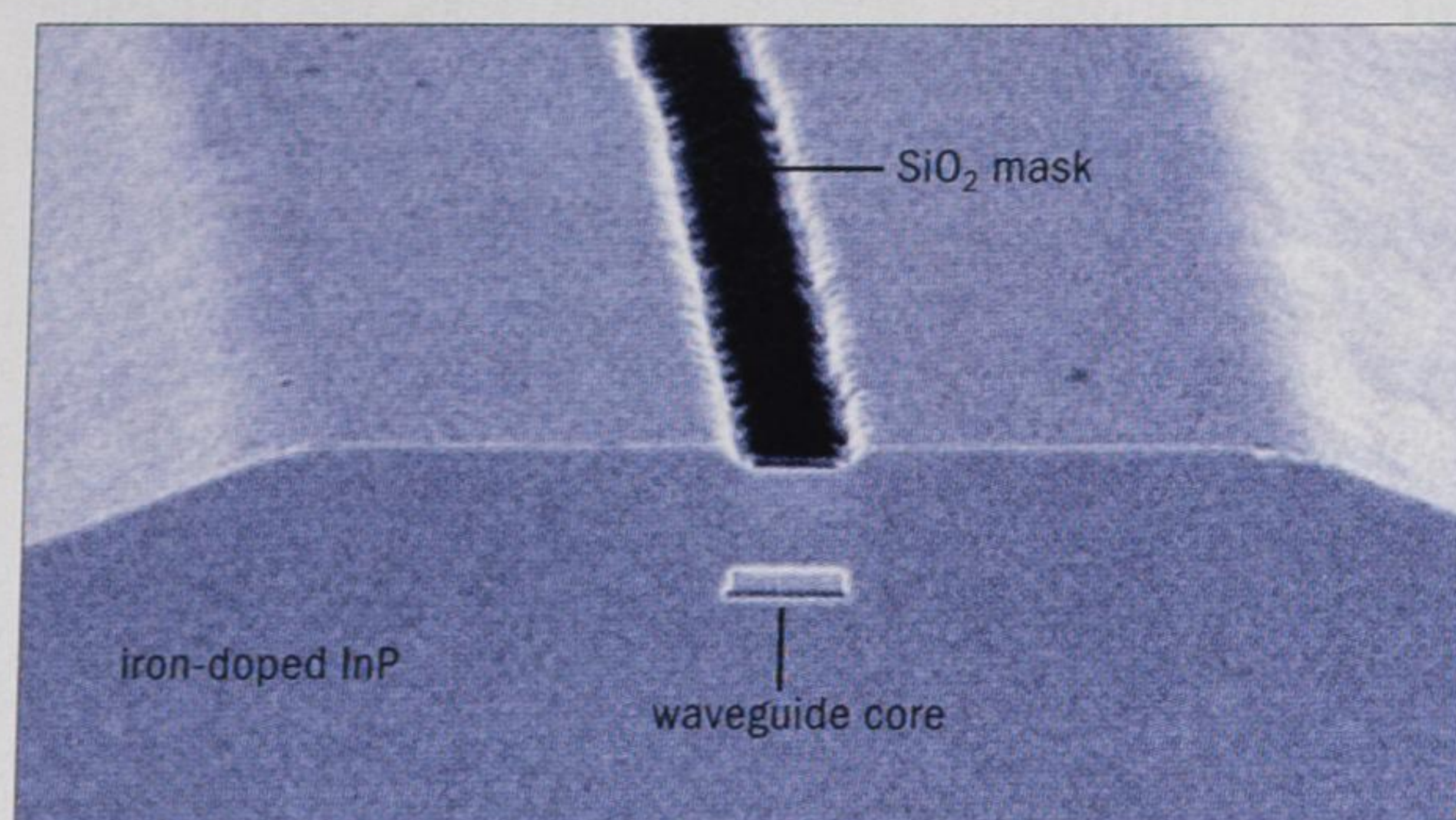


Fig. 2. HVPE's key strength is its suitability for lateral growth, leading to complete planarization regardless of crystal orientation.

into passive material through intermixing with the barrier. However, this tends to lead to high background losses typically beyond 10 dB/cm.

During the last few years we have built a variety of photonic integrated circuits with our relatively simple fabrication process, including 10 Gbit/s optical code-division-multiple-access (O-CDMA) transmitters and receivers, optical arbitrary waveform generators, and optical router systems.

Secure communications

O-CDMA transmitters and receivers have the potential to support optical local-area networks with a bandwidth of 10 Tbit/s, which is substantially broader than today's Ethernet or DSL networks. This technology provides secure links, just like its wireless equivalent, because every user has a specific code set and communication only takes place between users with matching codes. These are defined by applying phase shifts and amplitude changes on each spectral element of a broadband, coherent optical pulse.

Our transmitter features a mode-locked laser that produces ultrafast optical pulses, which are shaped with an integrated spectral encoder – an array of phase modulators sandwiched by AWGs. The receiver contains a spectral decoder with the same structure as the encoder and detection occurs when the mode-locked laser triggers the MZI switch.

Based on this technology we have demonstrated a 320 Gbit/s all-optical passive network testbed that uses spectral phase encoded time spreading O-CDMA and features up to 32 users operating at 10 Gbit/s (or equivalently 32,000 users at 10 Mbit/s).

This set-up delivers a bit error rate below 10^{-12} for a 320 Gbit/s O-CDMA network using Reed-Solomon forward-error correction.

The optical arbitrary waveform generator that we have developed operates at 1 THz bandwidths. It is suitable for rapid, secure communication of vast amounts of data and ultrahigh bandwidth LIDAR (light detection and ranging) – an optical technique used to determine the distance to a target. AWGs and high-speed (10 GHz) amplitude and phase modulators are combined in this monolithic chip.

We have also built an optical router that features photonic integrated chips and surrounding electronics. It has a routing capacity that can be scaled to 42 petabit/s, with switching speeds of 1 ns and routing latency of 50 ns. The chip's tiny footprint and power requirements make it an ideal replacement for today's power hungry, bulky electronic routers in telecom and enterprise networks and it could be suitable for deployment in the home and on military planes.

Our three types of photonic integrated circuits illustrate the potential of this technology, which has the capability to create supercomputers on a chip. The technology is still in its infancy, but we are fascinated to see how it develops. We will continue to play our part in this evolution by pushing photonic integrated circuit performance forward and investigating its commercial opportunities.

Further reading

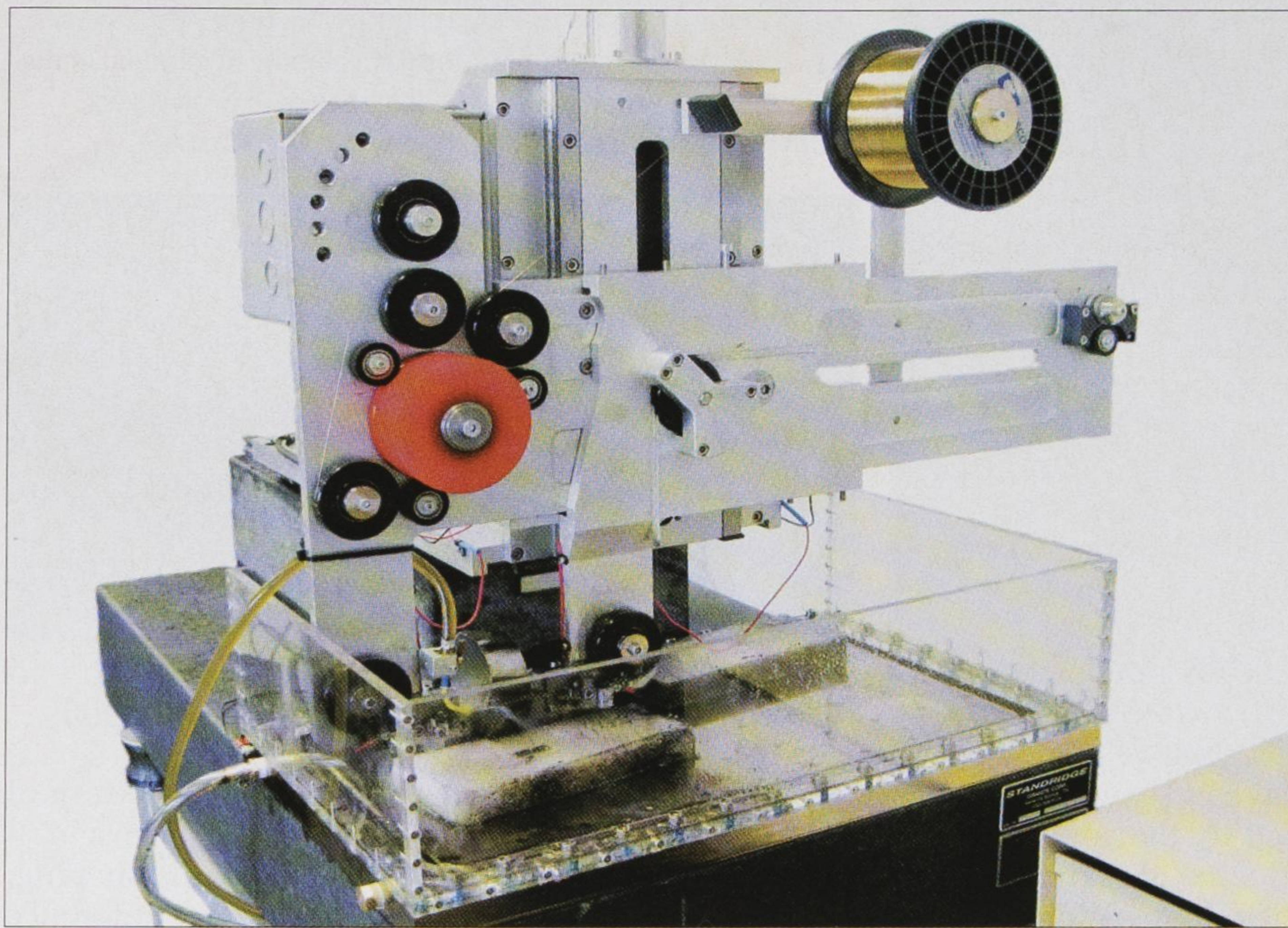
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WAFER SLICING

Electrical discharge machining promises high-quality, lower-cost substrates

Wire electrical discharge machining is a versatile, economic approach to boule processing. Its small kerf width means that it wastes substantially less material than the incumbent technology – the wire saw – and no microcracks are produced during processing, explain **Dinesh Rakwal** and **Eberhard Bamberg** from the University of Utah.



Wire electrical discharge machining uses electrical discharges from a high-tensile-strength metal wire, such as molybdenum, to remove material via local heating and evaporation.

Our community prides itself on its cutting-edge technologies. However, we are also dependent on a tool that has been refined and adapted over hundreds of years – the wire saw.

This piece of machinery is used by substrate manufacturers to cut thin slices of material from GaAs, InP and SiC boules, and offers a combination of simplicity, speed and effectiveness. However, sawing has some drawbacks: it wastes material and creates microcracks in these brittle semiconductors that can only be removed with additional processing.

Fortunately, these weaknesses can be addressed with wire electrical discharge machining (WEDM), a well established technique that has recently been applied to semiconductor machining through our efforts at the University of Utah.

This non-contact process begins by bringing a wire held at several hundred volts into close proximity with the boule. Arcing occurs when this gap falls to just a few microns. This transfers energy from

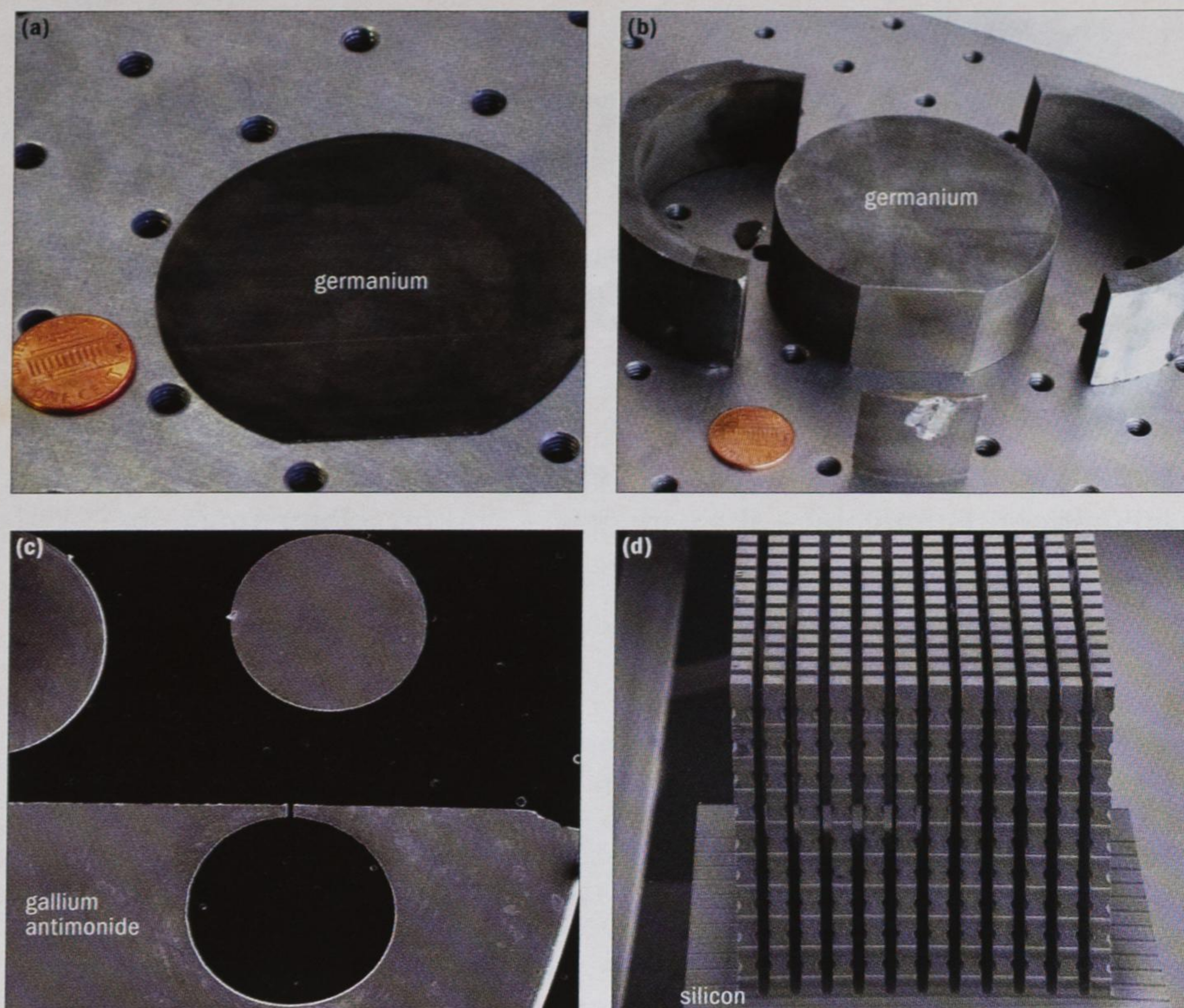
the wire to a small region of the boule, which then undergoes local heating and evaporation. A small cut is created in the boule, which can be deepened by repeating the arcing process to eventually produce a thin, circular slice of material.

The distance between the wire and the boule must be controlled precisely. Short circuits can occur when the boule and the wire get too close together, but if they are too far apart the processing speed plummets. Fortunately, the gap can be monitored by the WEDM's operating voltage. A fall in voltage reveals that the wire is too near to the boule and the cutting speed must be reduced to increase the separation distance. Similarly, a rising voltage indicates that the wire is too far from the boule and a faster cutting speed is needed.

Dielectrics, such as deionized water or oil, are directed into the gap between the wire and the boule. This increases the strength of the electric field that is produced by the wire, leading to improved focusing of the electrical discharge. The liquid also helps to carry away the molten material that is generated during the cutting process.

Any substrate manufacturer considering a switch from wire saws to WEDM will want to process material quickly, without compromising quality. The maximum cutting speed depends on the material that is being processed and it is possible to speed up the procedure by increasing the discharge energy – which is governed by the voltage across the gap, the discharge current and the timing of the electrical pulses. However, microcracks start to appear when the energy is too high, because material is removed by thermal shocks rather than by melting. With germanium we have concluded that electrical discharge energies of less than 0.111 mJ are needed to prevent microcracks from forming.

The boule's electrical conductivity profoundly affects the WEDM processing speeds. High resistances reduce current flow between the wire and the boule, decrease the energy of the pulses that are used to melt the semiconductor and ultimately slow down the procedure. Processing material with a resistivity of $0.01 \Omega \text{cm}$, such as germanium doped to $1 \times 10^{18} \text{cm}^{-3}$, is relatively easy. However, slow machining rates are inevitable at resistivities of $1 \Omega \text{cm}$. At $20 \Omega \text{cm}$,



WEDM is a very versatile technology for machining semiconductor materials. It can be used for wafer slicing (a), boule shaping (b) and free-form dicing (c). Researchers at the University of Utah are also using WEDM for three-dimensional microfabrication (d) and have created a 12×12 array of micro-needles with a $400 \mu\text{m}$ pitch in silicon. Each needle is 9 mm long and has a $120 \mu\text{m} \times 120 \mu\text{m}$ cross-section. The arrays produce electrical signals, which can act as a neural interface to simulate regions of the human brain for diagnostic and therapeutic purposes.

which is found in optical-grade undoped germanium that is used for infrared diffraction gratings, cutting speeds are incredibly slow, but we are aiming to address this with a high-voltage pulse generator.

Current flow is also limited by the contact resistance between the semiconductor and the metallic contacts that close the electrical loop. Adding metallic coatings on the semiconductor surface can cut contact resistance and lead to faster machining.

One of WEDM's strengths over wafer sawing is more-efficient material usage. This is seen in a reduction of the kerf – the width of material that is lost during a single cut. Wafer sawing produces $200\text{--}250 \mu\text{m}$ kerfs, which are more than twice as wide as the narrowest kerfs produced with our WEDM processes for germanium. With WEDM, the kerf width depends on the diameter of the wire and the discharge energy. We have produced 138 , 118 and $94 \mu\text{m}$ kerfs with 0.111 mJ pulses and 100 , 75 and $50 \mu\text{m}$ diameter wires, respectively (figure 1). This kerf width equates to $24\text{--}32\%$ material wastage for germanium substrate processing, compared with $40\text{--}45\%$ for wire sawing. Thinner wafers will benefit even more, allowing WEDM to lead to greater cost savings.

WEDM has a downside – it coats substrates with a thin “recast” layer that contains material from the boule, wire and dielectric (figure 2). This layer needs to be removed before subsequent wafer processing, and can be etched away with acids. We have found that the recast layer on germanium is $7\text{--}8 \mu\text{m}$ thick

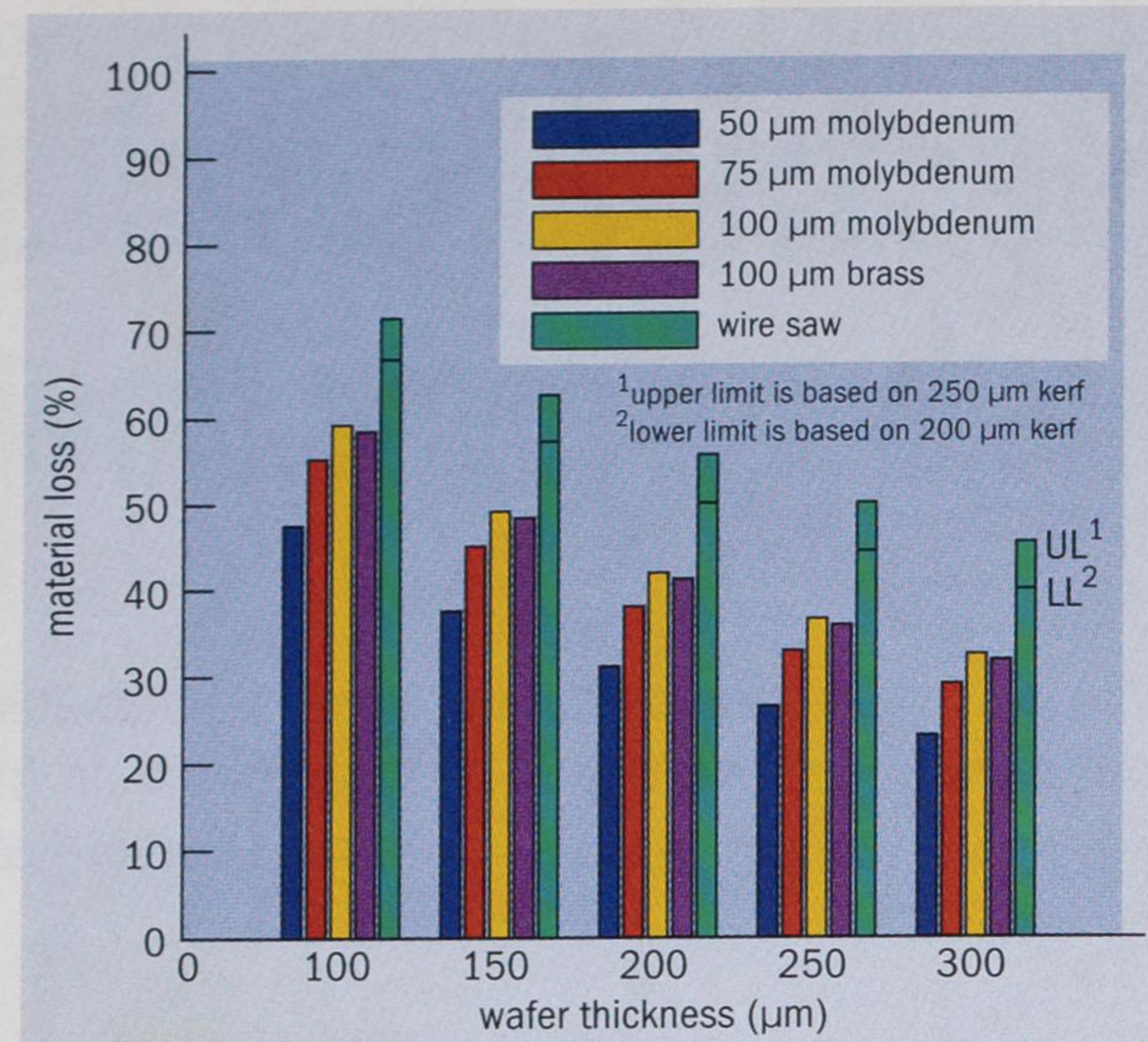


Fig. 1. WEDM can cut substrates from a boule of germanium far more efficiently than a wire saw can, thanks to a lower kerf width that leads to substantially less material wastage.

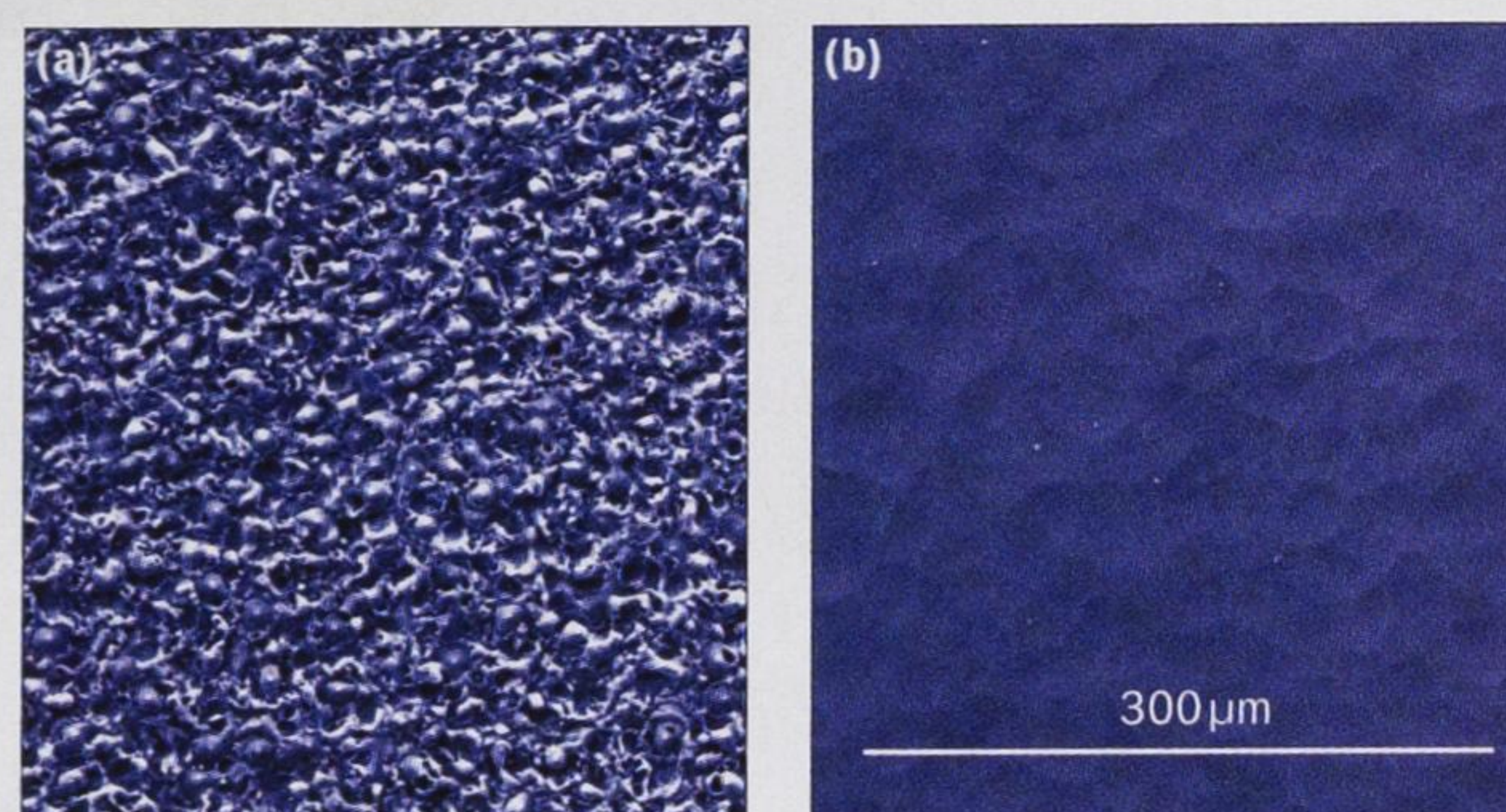


Fig. 2. WEDM creates a thin recast layer on any machined surface (a), but this can be removed by chemical etching (b).

and it can be etched away in 10s with a mixture of 60% acetic, 25% nitric and 15% hydrofluoric acid.

Another application for WEDM is boule shaping. This includes machining of the substrate reference flat, which involves the removal of extraneous material as large pieces. The surplus material, which is estimated to be $13\text{--}15\%$ of the boule, can be put into the melt after it is etched clean.

The standard boule-shaping technique – cylindrical grinding – is inferior to WEDM because it produces deep microcracks in the material. Grinding is also less efficient because it generates dust that is contaminated with abrasives from the grinding wheel and coolant. Recovering the precious semiconductor from this slurry is far from easy.

The versatility of WEDM enables it to be applied to post-growth processing, such as the dicing of individual devices from a wafer. Traditional machining methods struggle to process thick wafers and complex shapes, but WEDM can perform free-form dicing of any shape. Unlike laser machining, WEDM can handle a variety of wafer thicknesses without compromising the edge's shape or its quality.

Further reading

D Rakwal *et al.* 2008 *Journal of Materials Processing Technology* doi:10.1016/j.jmatprotec.2008.08.027.



About the authors

Dinesh Rakwal (left) is a PhD candidate in the department of mechanical engineering at the University of Utah. His research focuses on wire electrical discharge machining of p-doped germanium and silicon. **Eberhard Bamberg** (right) is currently an assistant professor in the same department. He is the director of the Precision Design Laboratory, which performs research in the areas of precision machine design and non-traditional manufacturing methods for semiconductors.

UK cracks GaN-on-silicon LEDs

GaN-on-silicon LEDs do not have to suffer from high levels of strain that hamper output power. Armed with *in situ* tools for monitoring temperature and wafer bow, our UK-based team has produced flat, low dislocation density 150 mm epiwafers and processed them into devices with internal quantum efficiencies approaching 40%, say **Andrew Phillips** and **Dandan Zhu**.

The US Department of Energy believes that widespread adoption of LED lighting will require cheaper, more-efficient commercial devices. Both of these criteria are captured in its LED roadmaps, which include 150lm/W lamps by 2015 that cost less than \$5 per kilolumen.

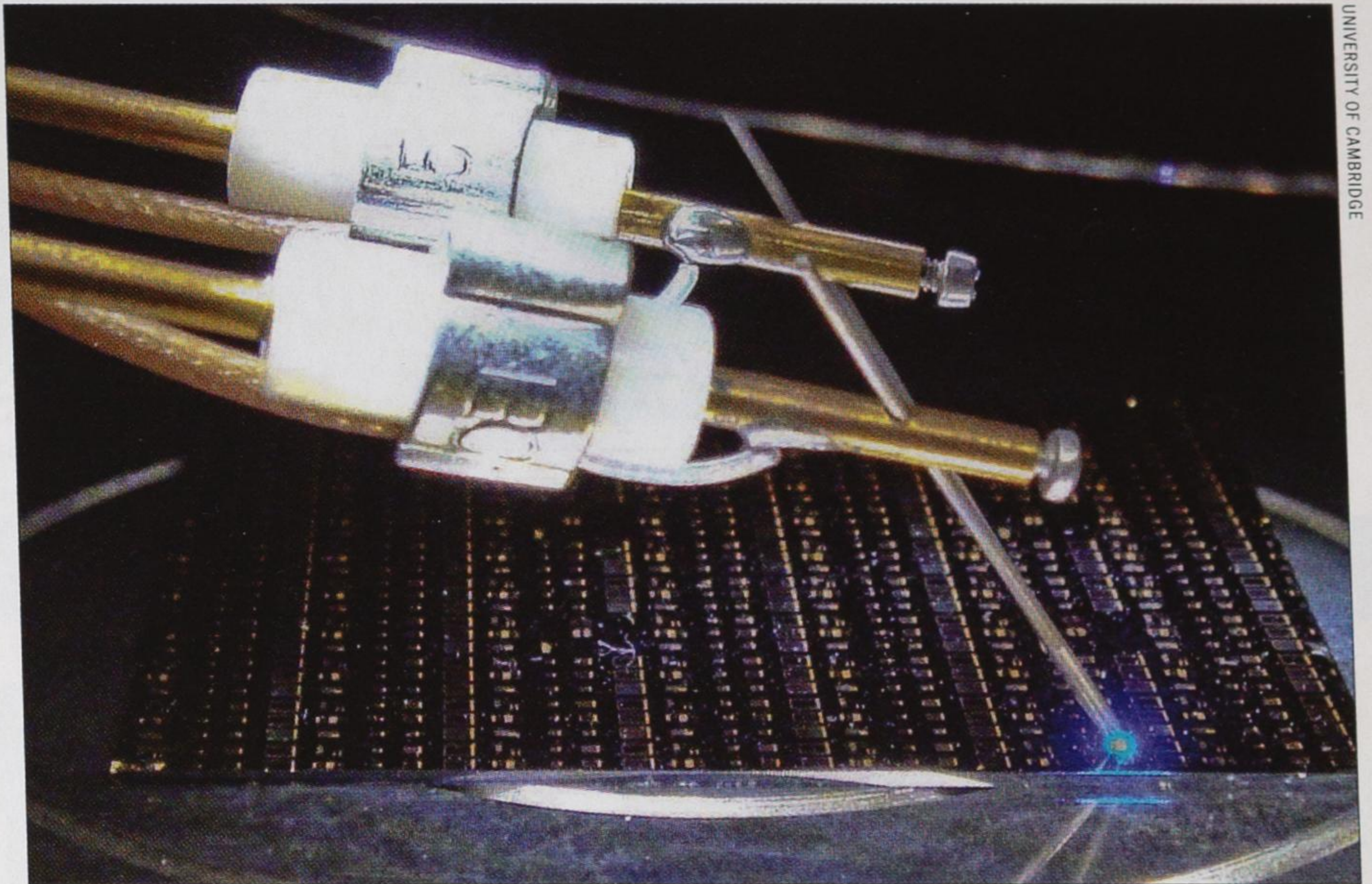
Today LED lighting costs are more than twice that, with the cost of the die alone contributing nearly 50%. But chip costs could fall by an order of magnitude by switching to larger, lower-cost substrates that improve processing efficiency.

Our UK consortium – which is headed by RFMD (UK) and involves contributions from Cambridge University, Aixtron (UK), QinetiQ and Forge Europa – is working towards that goal with a government-funded project that started in April 2007. Backed by £3 million (\$4.5 million), our effort is focused on the development of high-quality LEDs on 150 mm silicon. It has already produced devices with internal quantum efficiencies (IQEs) of nearly 40%.

Development of the growth processes for producing good-quality LED material is being led by Cambridge University and supported by growth and processing at QinetiQ, which uses its broad semiconductor expertise to validate material developments prior to process scale-up for LED manufacture at RFMD. When device manufacture commences, marketing will be carried out by LED applications specialist, Forge Europa.

Silicon substrates have been selected for nitride growth because they combine stability at typical growth temperatures with low cost and are available in diameters of up to 300 mm with a surface suitable for epitaxial growth. Nitride-on-silicon epiwafers also enable processing with standard manufacturing tools employed in the silicon industry, leading to cost-effective production of chips that can be bonded and converted into packaged LEDs.

Although silicon has key advantages over the existing substrate materials used for LED manufacture – sapphire and SiC – it has an Achilles heel: high lattice and thermal expansion mismatches with GaN. Growth directly onto silicon produces tension in the film from the moment that GaN is deposited at a typical growth temperature of 1000°C and this is magnified as the wafer cools to room temperature,



GaN-on-silicon LEDs grown on 150 mm silicon (111) substrates by MOCVD are being developed by a UK government-funded project that is headed by the UK arm of RFMD, with contributions from Cambridge University, Aixtron (UK), QinetiQ and Forge Europa.

due to differences in thermal expansion. Unless managed correctly, this strain can even crack the GaN film. More often it causes the wafers to bow, making them awkward to process in automated tools that are designed for silicon processing. In comparison, when nitrides are grown on SiC the thermal expansion and lattice parameter oppose each other, while on sapphire both terms cause compression of the GaN film, but this does not cause cracking.

The large lattice mismatch between GaN and silicon leads to a relatively high dislocation density for the epiwafers. Nitride LEDs are resilient to surprisingly high levels of defects, but the IQE of blue LEDs declines as dislocation densities exceed 10^9 cm^{-2} .

Silicon's other weakness is its reaction with gases in the growth chamber during the initial stages of growth. Defects form on the surface, leading to a morphology unsuitable for subsequent GaN growth.

The growth process developed at Cambridge University for producing blue-emitting LEDs addresses all of these issues. Epitaxial structures are produced in an MOCVD Aixtron/Thomas Swan close-

Fig. 1. The LED's structure includes a SiN_x layer to reduce dislocations (a). A Laytec Epicurve monitors wafer bow and temperatures are measured with the Aixtron Argus tool (b). Growth can be divided into seven sections: pre-growth heat treatment; growth of the AlN nucleation layer, the buffer, the n-GaN layer, the multiple quantum-well region and the p-GaN layer; and annealing/cooling.

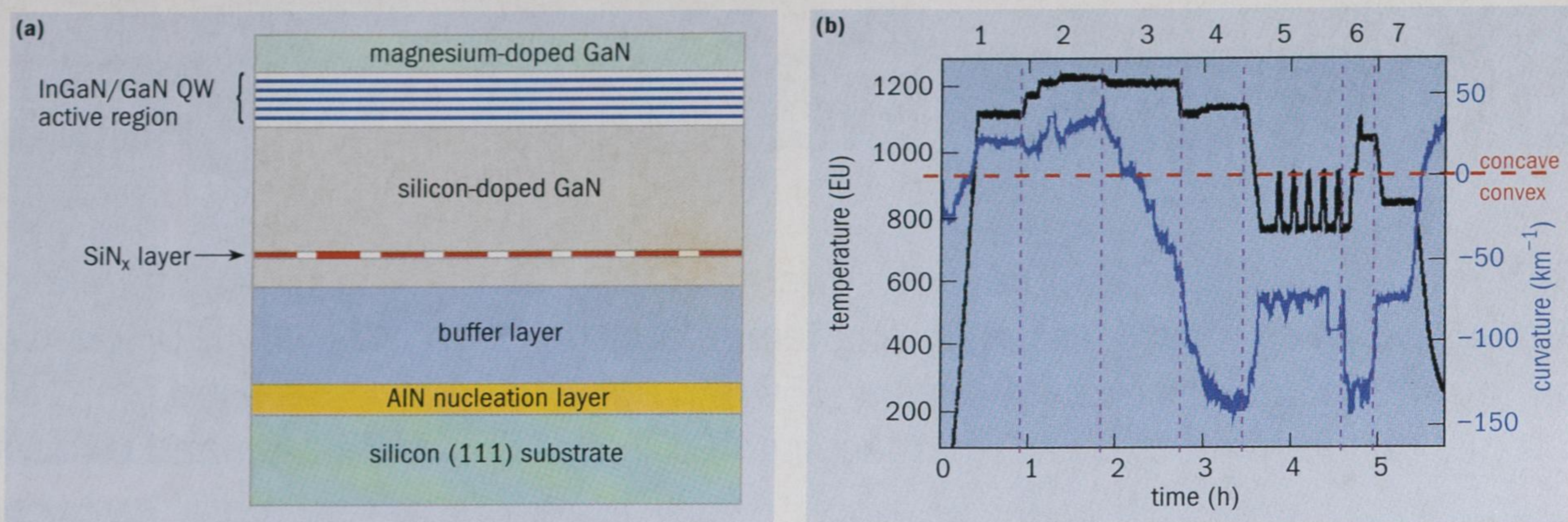
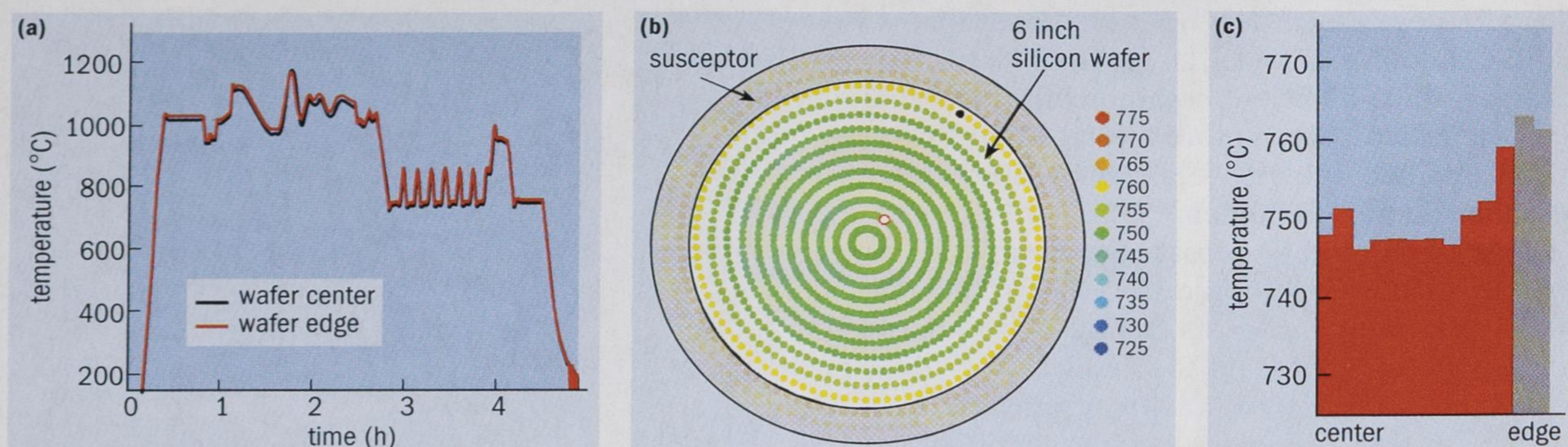


Fig. 2. Aixtron's Argus temperature profiler can reveal the temperatures across the whole of the 150 mm wafer. Any differences can be minimized by independently adjusting the radial zones of the reactor's heater.



coupled showerhead reactor that accommodates a single 150 mm wafer (or multiple 2 inch wafers) and is equipped with *in situ* instruments for measuring wafer bow and temperature. Growth on 150 mm silicon (111) includes the deposition of a complex buffer structure to control strain and wafer curvature. This is followed by the growth of a multiple quantum well (MQW) LED structure with InGaN wells and GaN barriers that emits at 460 nm, and a magnesium-doped p-type GaN (figure 1a).

Substrates are prepared for growth by annealing in hydrogen to remove the native oxide layer and create a terraced, reflowed silicon surface. Growth begins with deposition of an AlN nucleation layer to ensure that the silicon surface does not degrade, followed by a complex buffer structure. Careful control of the composition and thickness of this buffer balances its strain with that induced by thermal expansion mismatch on cooling from the growth temperature.

To improve LED performance, GaN and AlGaIn layers are added on top of the buffer to reduce dislocation density. Inserting a SiN_x layer, a technique used for nitride film growth on sapphire, further cuts threading dislocation density.

In situ tools

Continual monitoring of wafer temperature and bow holds the key to successful, reproducible growth of flat, uncracked material. The substrate temperature in the reactor at Cambridge University is profiled with an Aixtron Argus tool and a LayTec Epicurve provides real-time wafer-bow measurements.

The silicon that we use has a slight convex bow,

which switches to a concave shape after heating and *in situ* annealing because the bottom of the substrate is then at a higher temperature than its top surface (figure 1b). Concave bowing increases with the addition of the AlN nucleation layer, but a convex profile returns with the growth of the buffer and the silicon-doped GaN layer, which introduce increasing levels of compressive stress. The growth of quantum well and barrier layers produces detectable, small changes in curvature, before the wafer becomes even more convex as the reactor temperature is increased for magnesium-doped GaN deposition. Optimizing the magnitude of this bow during buffer growth can produce a perfectly flat wafer after cooling, by providing a match for the tensile stress of the film, resulting from thermal expansion coefficient differences between GaN and silicon.

Development of the growth processes has led to production of 150 mm diameter epiwafers with a surface height variation across their full diameter below 50 μm . These wafers are suitable for processing with RFMD's high-volume production equipment.

Bow must be introduced at the growth temperature to ensure a flat wafer on cooling, but it can also lead to significant temperature variations across the surface caused by differences in the distance between the substrate and the susceptor. Temperature variations are detrimental to InGaIn LED growth because they alter the indium content in the quantum well and its emission wavelength. Fortunately we can detect these temperature variations with our Argus profiler and minimize them by adjusting the power delivered to three heater zones.

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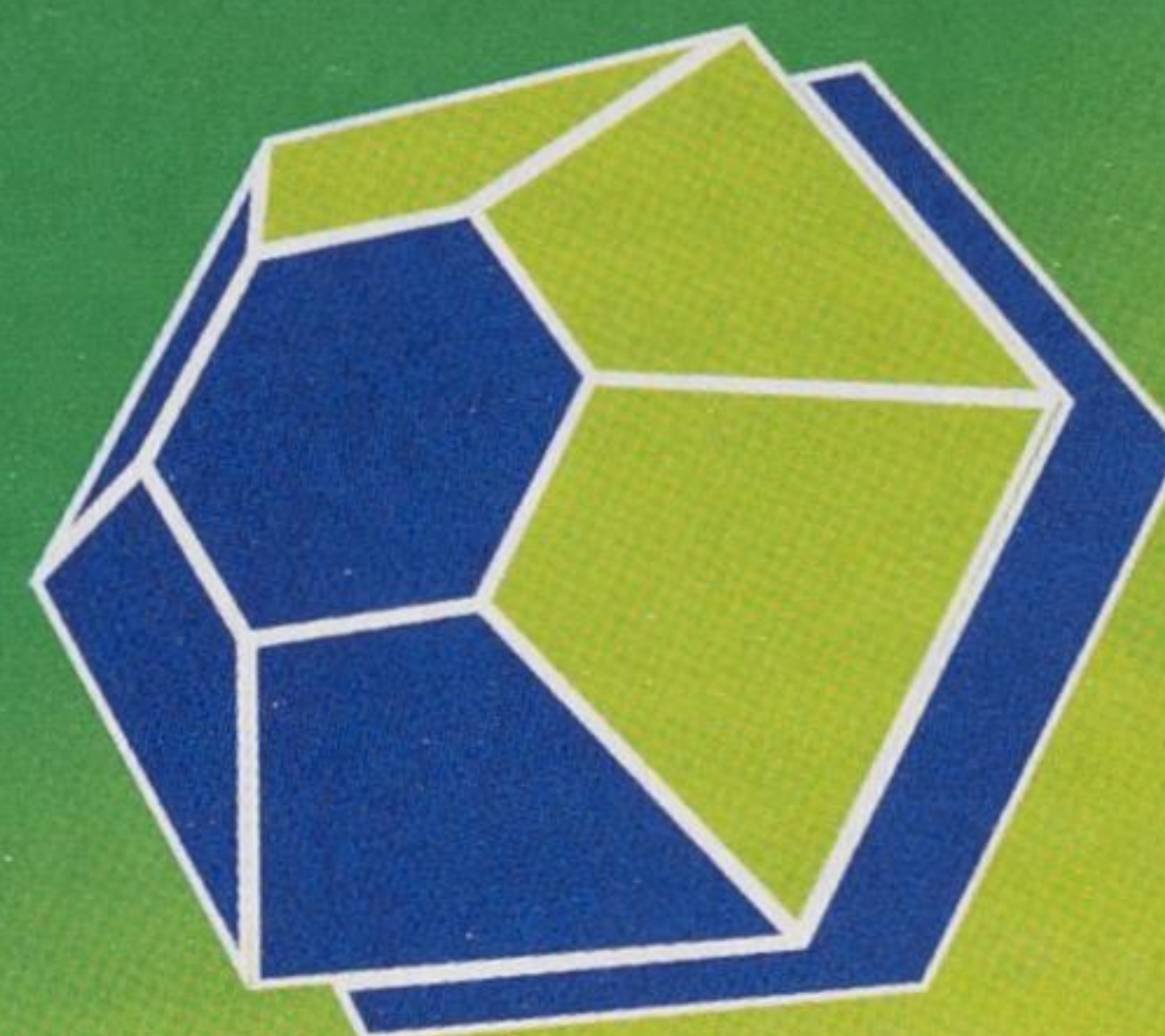


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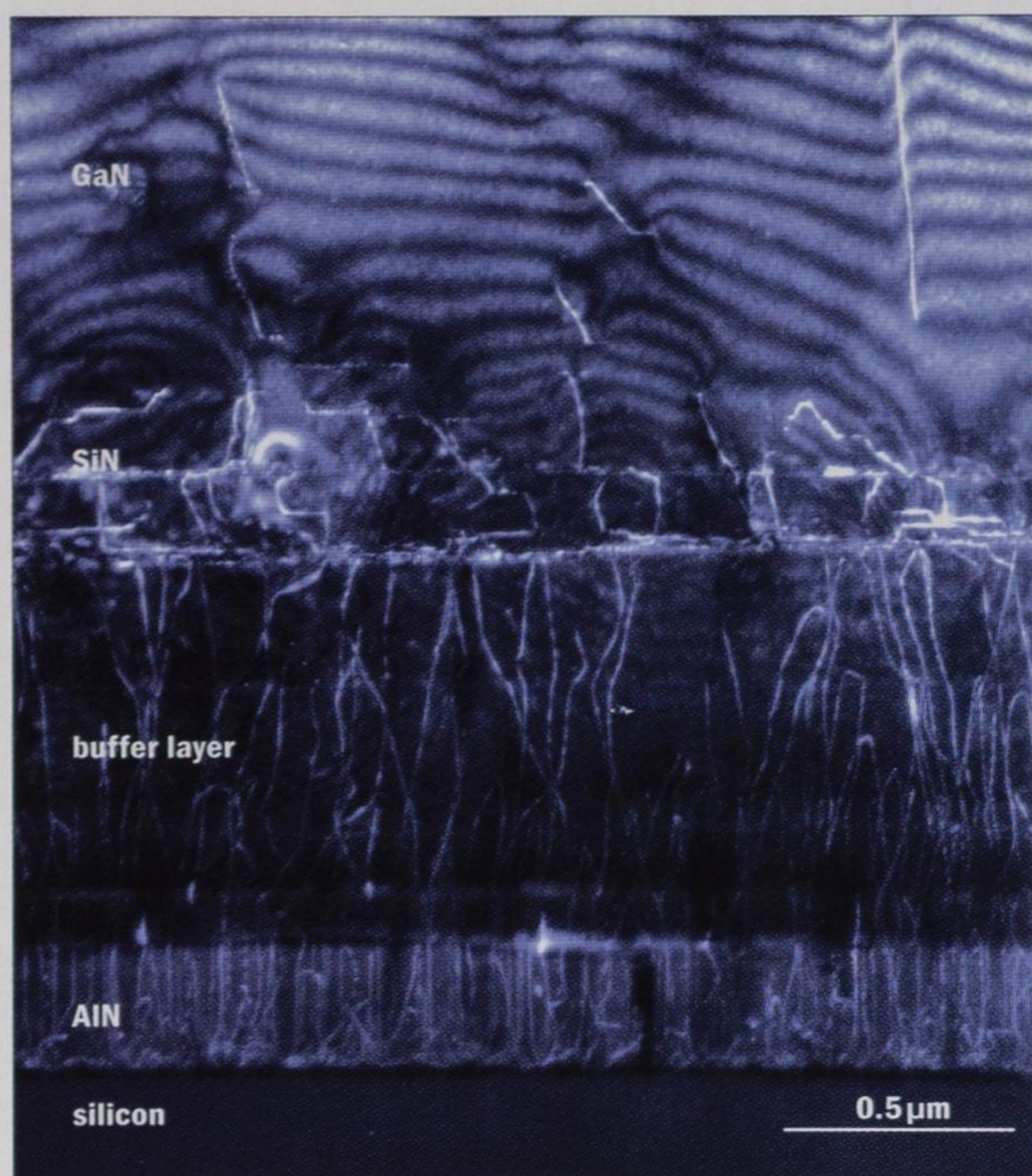


Fig. 3. Weak-beam, dark-field TEM images show that SiN layers can help to reduce the dislocation density in InGaN/GaN LEDs. Pure screw/mixed-type dislocations are visible.

Table 1. Silicon versus sapphire and SiC

Property	Silicon (111)	Sapphire	SiC
Cost per mm ² (a.u.)	1	10	50
Available diameters	up to 300 mm	2–4 inch	2–4 inch
Thermal expansion mismatch to GaN	–50% tensile	+35% compressive	–18% tensile
Lattice mismatch to GaN	+17% tensile	–14% compressive	–3.5% compressive
Conductivity	semiconducting	insulating	conducting

Plus and minus signs are used for parameters greater and less than GaN, respectively.

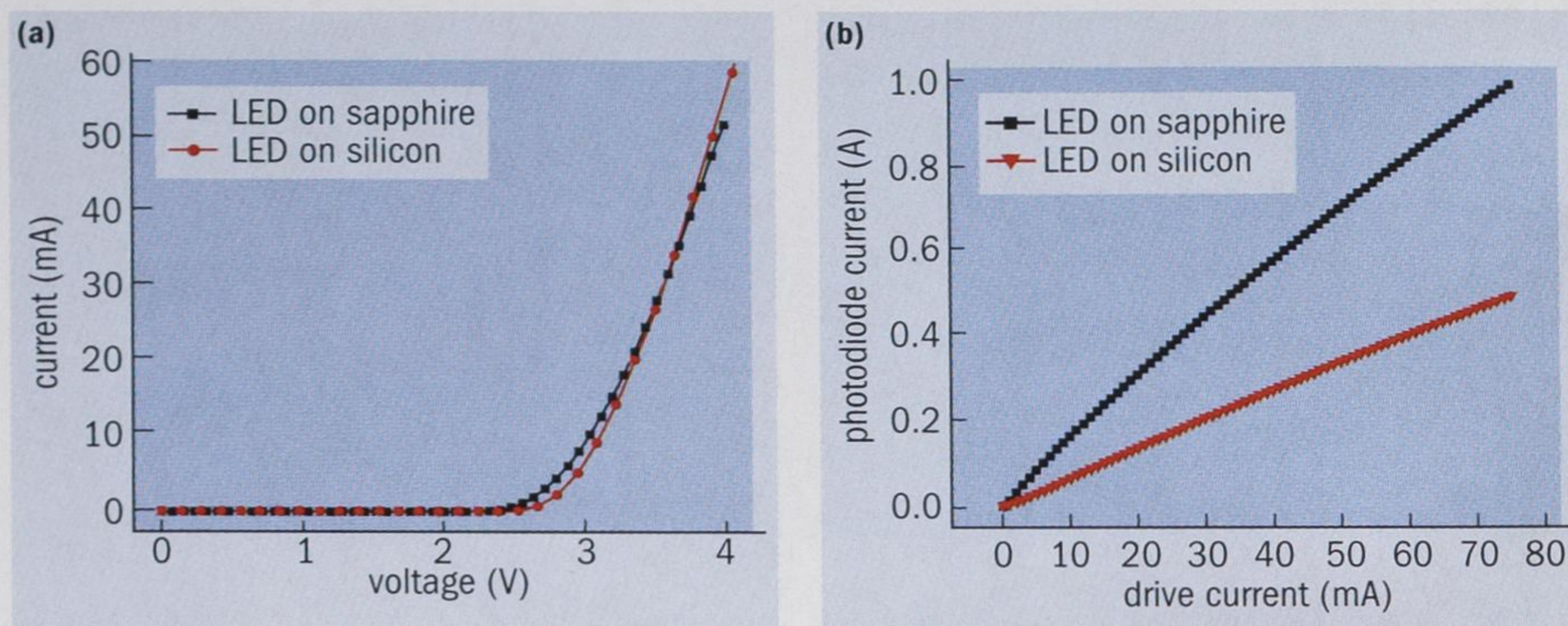


Fig. 4. GaN-on-silicon LEDs produce very similar current-voltage curves to conventional devices (a), but light output from this type of device is about 50% lower (b).

Cross-sectional transmission electron microscopy (TEM) images reveal that the low dislocation density in the device layers is due to a SiN_x layer that causes these defects to bend over and annihilate (figure 3). This also occurs at the AlGaIn/GaN interface, thanks to a compressive stress that results from the larger in-plane lattice parameter of GaN compared with AlN.

The dislocation density in the epiwafers has been assessed with plan-view TEM images using diffraction conditions that reveal all of the dislocations. These images, and those taken with an atomic force microscope after exposing the surface to a silane flux at 860 °C to highlight pits, give values of less than 10⁹ cm^{–2} for the best GaN-on-silicon material.

The IQE of the material has been evaluated by temperature-dependent photoluminescence measurements at the University of Manchester. This approach, which makes the assumption that non-radiative recombination becomes negligible close to absolute zero, gives a room-temperature IQE of almost 50%. Similar structures grown on sapphire with a dislocation density of 10⁸ cm^{–2} have typical values of 70%, indicating that the higher dislocation density of nitride material on silicon may not be a major problem in the production of high-performance LEDs on this substrate.

We have gone on to fabricate LEDs at QinetiQ. Etching formed a mesa that exposed the n-type GaN layer. Deposition of a Ti/Al/Pt/Au alloy followed to produce the n-type contact and the p-type contact was created through addition of semitransparent, annealed NiAu and a thicker gold contact pad.

Our best 0.5 mm × 0.5 mm LEDs have very similar current-voltage characteristics to our GaN-on-

sapphire controls, including a turn-on voltage of about 2.5 V (figure 4). The light output from the top side of both devices has been measured using the same optical arrangement. The sapphire-based controls produce about twice the output of LEDs grown on silicon. Taking into account the highly absorbing silicon substrate, the IQE of LEDs on silicon is 37% according to calculations based on measurements of the total light emitted in the forward direction.

GaN-on-silicon LEDs are still in their infancy, but our initial results are very encouraging. Removing the silicon substrate to prevent light absorption will not be an issue for manufacturers because high-brightness LED production often involves flip-chip mounting and substrate removal. With state-of-the-art packaging and appropriate phosphors, our current devices could deliver 70 lm/W, based on a comparison with LEDs on sapphire. Thanks to the affordability of silicon, this means that GaN LEDs that are grown on silicon will approach the Department of Energy's 2012 target for the cost per kilolumen. This makes our emitters genuine contenders for solid-state lighting and their performance will only get better as *in situ* growth techniques improve, leading to even higher quality material.

Further reading

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About the authors

Andrew Phillips (left) from phconsult is the project co-ordinator and **Dandan Zhu** (right) is a research associate at the University of Cambridge. They thank their collaborators Trevor Martin, Mike Kane, Penny Lane and David Wallis (QinetiQ); Ted Thrush, Clifford McAleese, Maik Haeberlen, Dick Plumb and Colin Humphreys (University of Cambridge); Andrew Pakes and Michael Heuken (Aixtron); Peter Barton (Forge Europa); Stephen Clements and Matthew O'Keefe (RFMD). The consortium thanks the UK Technology Strategy Board for funding (TP/6/EPH/6/1/K2509F) and the Universities of Cambridge and Manchester (Phil Dawson) thank the EPSRC for supporting projects relating to fundamental science of GaN-on-silicon (EP/E035167/1).



R STEVENSON

Chip makers chase fiber-laser boom

Laser diode manufacturers are targeting the fast-growing fiber-laser market with novel technologies that deliver higher output powers and better beam quality. **Richard Stevenson** reports.

Wind the clock back a few years and efficiency was the key metric for high-power laser diode manufacturers. It was a prominent feature in the technical sessions at the Photonics West trade show, and companies involved in DARPA's SHEDS (super-high efficiency diode sources) program used the event to detail their progress towards an 80% efficiency target.

Fast-forward to this year's Photonics West and efficiency is no longer the key talking point. That's not because the goal of the SHEDS program has been met. Instead, it is a reflection of a shift in prioritization of laser diode characteristics. Top of the list is a need to serve today's key applications.

One of the largest applications to emerge is for fiber lasers. This has grown tremendously in recent times, and this year Stephen Anderson of *Laser Focus World* estimated that the market for fiber lasers would be worth more than \$300 million in 2009. The role of the diode source, which can be a single emitter or a bar, is to pump a doped optical fiber featuring Bragg gratings at either end. These act like mirrors to produce a coherent, powerful beam with excellent beam quality, which is able to cut metal sheets and serve defense applications.

Like any source, a fiber laser benefits from a high-

efficiency pump, because it reduces overall running costs and cooling requirements. However, the more important issue is the amount of optical power that can be coupled into the fiber. This is governed by the output power of the diode and its beam quality, which in turn depends on the geometry employed in the chip itself, such as the stripe width and the thickness of various epitaxial layers.

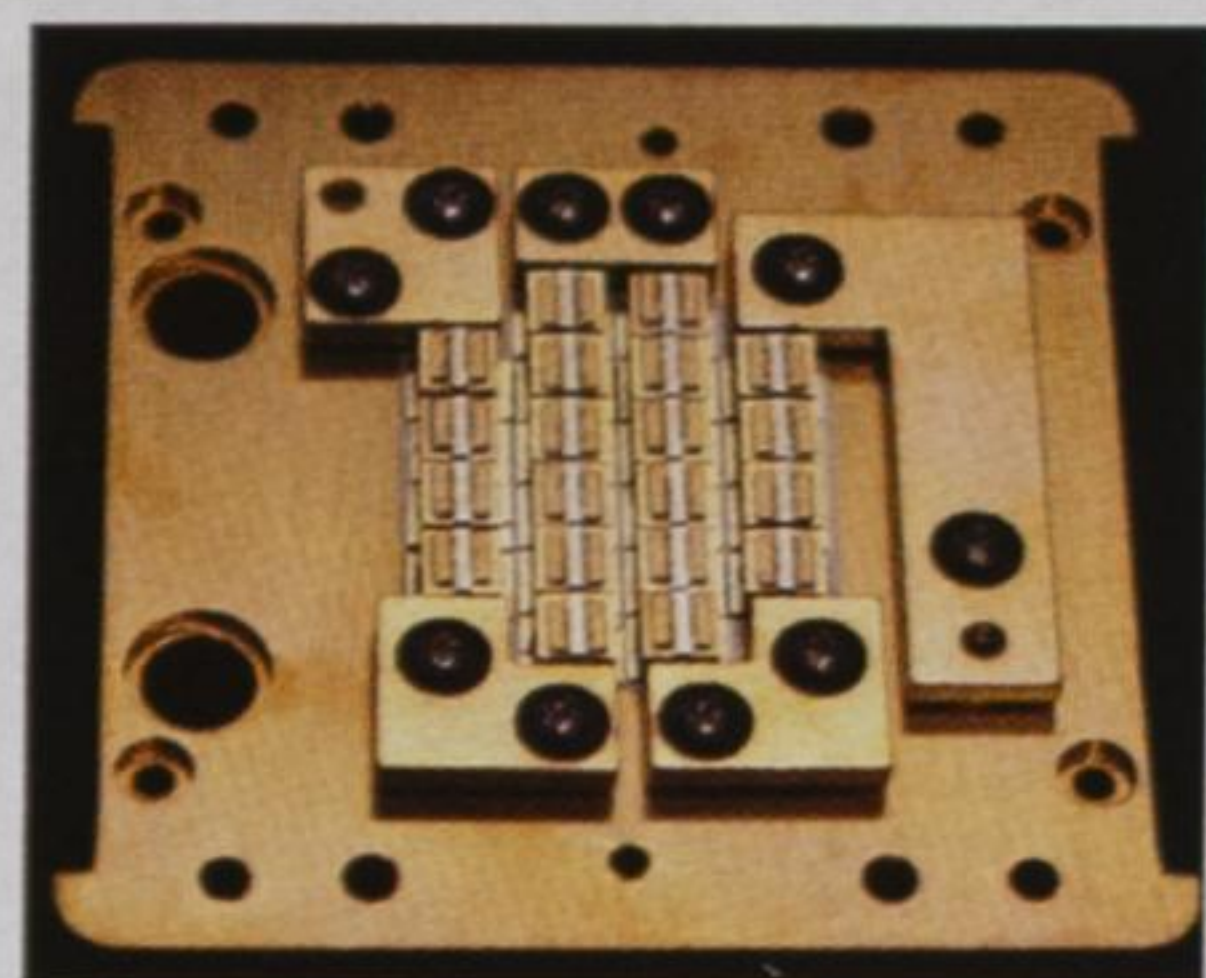
At this year's show, Alfalight unveiled a promising approach for improving beam quality. The US company's new distributed feedback (DFB) laser has an innovative design that emits light through a large rectangular window in the top of the chip, rather than the more conventional edge emission. The new technology features a curved grating in the p-type region, which diffracts light out of the chip, locks the wavelength and maintains an emission bandwidth of less than 0.2 nm.

The company cannot claim that it invented this technology – its roots can be found in the research conducted at the Hughes Research Labs (now HRL) in the 1990s. However, Alfalight's four-year development program has taken the performance of these devices to new levels.

Speaking at the Alfalight stand, vice-president of

SPIE
Photonics West

Photonics West was held at the San Jose Convention Center in California on 24–29 January. The show attracted more than 17,000 visitors.



Alfalight's array of surface-emitting distributed feedback lasers can produce more than 200 W at a drive current of just over 25 A.

marketing and sales, Ron Bechtold, explained that the device has several benefits over the traditional edge-emitting design. It is immune to facet damage because the optical power density in the structure is reduced by four orders of magnitude. In addition, the output can be coupled into a fiber laser with relatively simple optics. And, as with VCSELs, these devices can be tested while still on-wafer.

Bechtold revealed that Alfalight's surface-emitting DBRs include a 6 W, 975 nm laser with a power conversion efficiency peaking at more than 50%, as well as a 2 W version with a diffraction-limited beam. An array of 20 of these devices produced more than 200 W, and another with 30 elements can deliver more than 300 W.

Paul Crump from the Ferdinand Braun Institute for High-Frequency Technology in Berlin, Germany, has addressed the issue of increasing the output power from a single emitter source. According to him, commercial 980 nm broad-area laser diodes used for pumping erbium- or ytterbium-doped fiber lasers produce reliable outputs in the 8–10 W range. His team, however, has now fabricated reliable chips that can produce twice this power.

Crump describes the devices as “super-large optical cavity designs”, which have robust AuSn-based packages. They are grown by MOCVD and contain a 2.4 μm thick waveguide core with an asymmetric-

ally positioned InGaAs/GaAsP double quantum well that minimizes excess resistance and optical absorption from the p-side of the mirror. Reliability tests have been performed on 4 mm long lasers with various stripe widths. They determined that devices with a 96 μm stripe, operating at 20°C, could produce a continuous-wave output of 20 W for more than 4000 hours.

A claim for a completely different concept for coupling laser emission into a fiber laser was made in a talk given by Uwe Strauß from Germany's Osram Opto Semiconductors. He argued that single emitters cannot produce enough output for some fiber lasers, but typical laser diode stacks suffer from cross-talk between the various elements because of the high fill factor used. The ideal solution, according to him, is to combine many single emitters in bars that have far smaller fill factors.

To test this idea Osram has built 808 nm, 880 nm and longer-wavelength laser bars with five emitters and fill factors of less than 20%. These are designed to couple into a fiber laser with a 200 μm core and a numerical aperture of 0.22. Emission from these bars was compared with that produced by five isolated, single emitters. “They are identical and there is no need to use a single emitter,” claimed Strauß, who went on to say that the reliability of the bars is similar to that of the single emitters.

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- D: Materials, Processes, and Reliability for Advanced Interconnects for Micro- and Nano-Electronics
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GENERAL INTEREST

- X: Frontiers of Materials Research

Reflecting layer boosts LED brightness

Slipping a SiO_2 layer into nitride-on-silicon LEDs boosts their brightness, thanks to a substantial reduction in the substrate absorption, explains a research team from Singapore and Germany.

The silicon substrate is an interesting contender for nitride LED growth. On the one hand it is cheap and widely available in large diameters, which gives it the potential to cut LED costs and spur device deployment. Doped substrates should lead to superior device architectures and silicon is also easy to cleave, which simplifies chip fabrication.

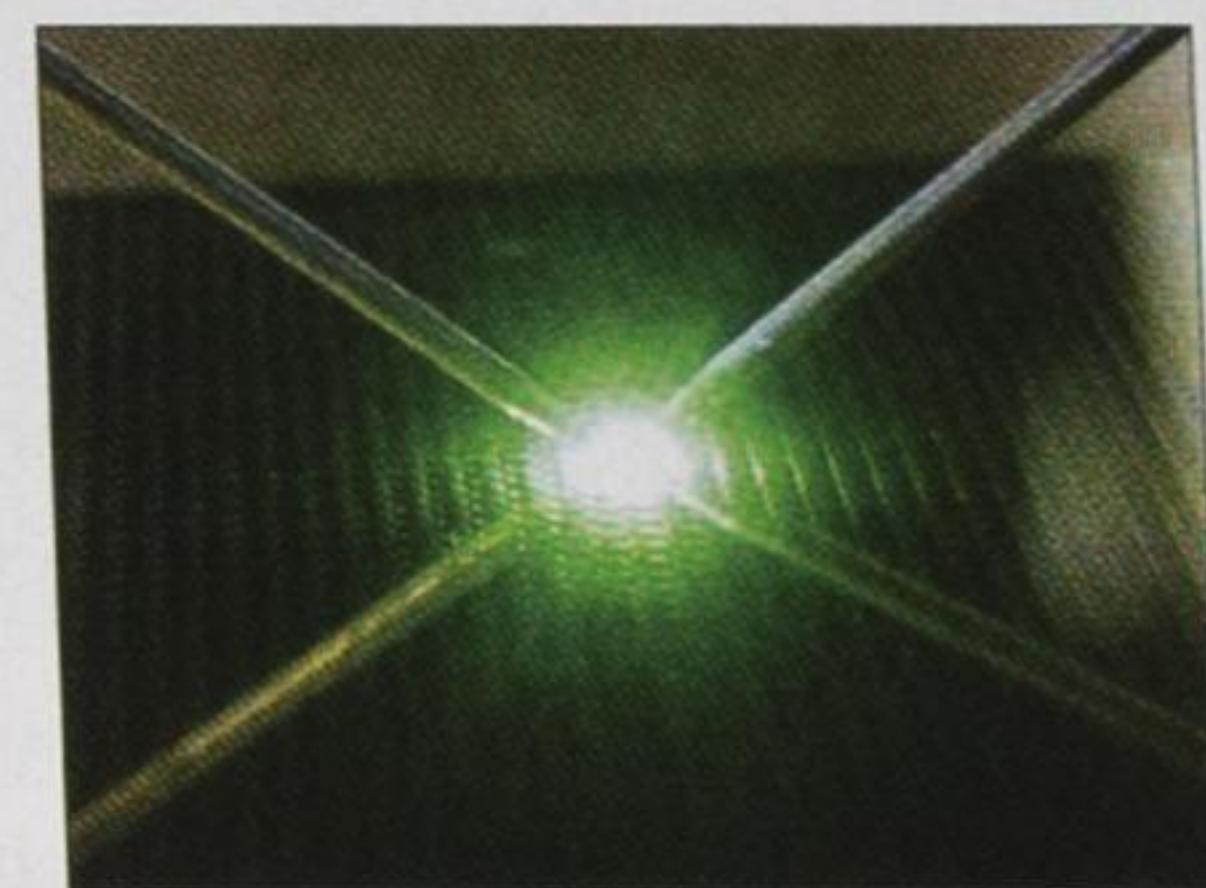
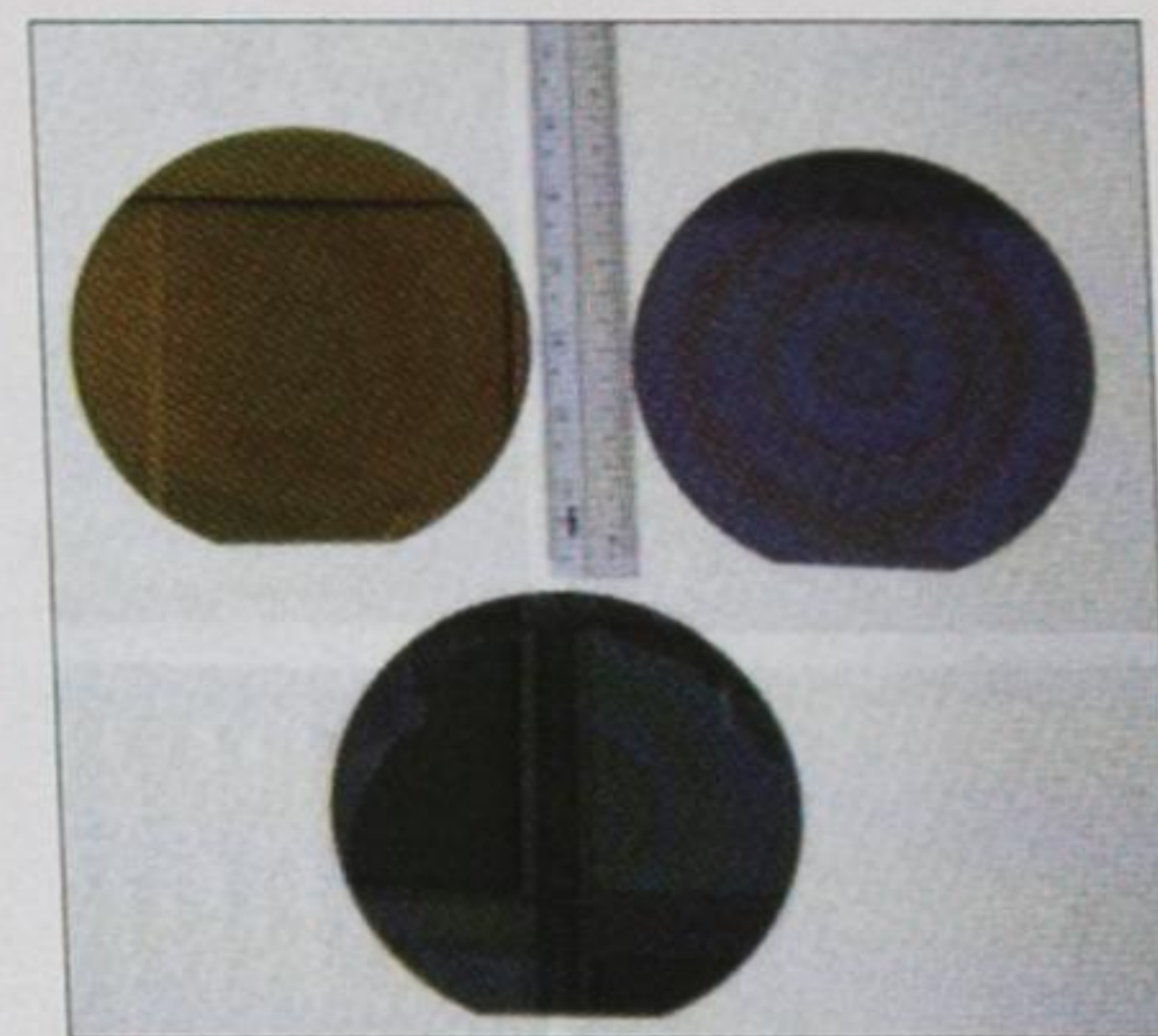
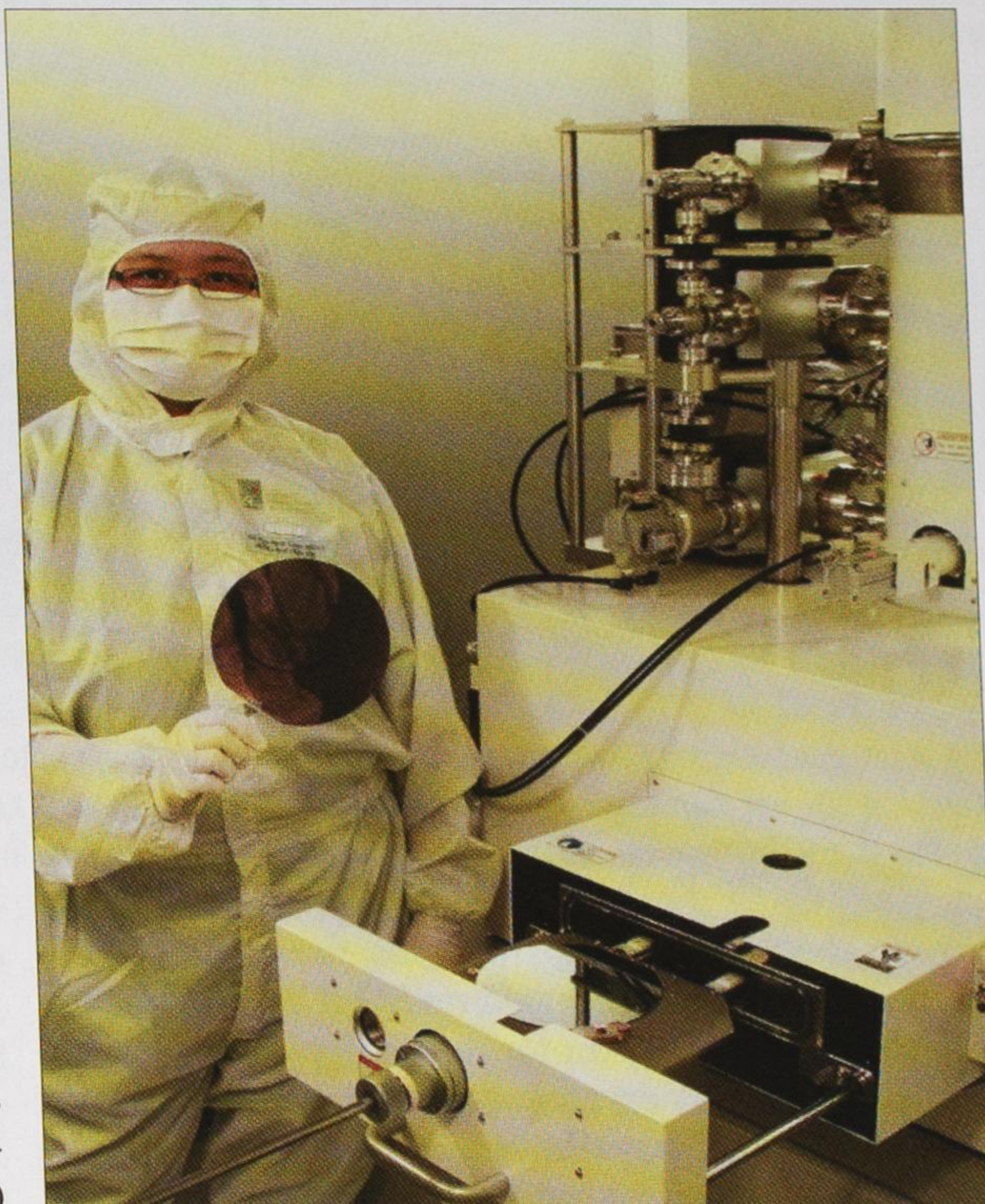
However, these strengths have to be weighed up against high lattice and thermal mismatches between silicon and GaN, which create a tensile stress in the epilayers that degrades their quality and reduces internal quantum efficiencies. Silicon's strong absorption of blue and green light is another drawback, which makes substrate removal essential for making high-brightness emitters. This requires additional processing steps, which have to be capable of transferring large areas of nitride material.

The ideal way forward is to develop an approach that delivers the benefits of silicon, while avoiding its pitfalls. Fortunately at Singapore's Institute of Materials Research and Engineering (IMRE) – which is a member of the Agency for Science, Technology and Research (A*STAR) – our team has identified a platform that goes a long way to satisfying these demands: silicon-on-insulator (SOI) substrates. Armed with this composite we have produced LEDs that benefit from strong reflectivity at visible wavelengths, which stems from the high refractive index contrast between silicon and SiO_2 . This improves the device's light output, which has received an additional boost through the introduction of photonic crystal structures.

GaN-on-SOI LEDs also promise to deliver a relatively high manufacturing yield. More GaN die can be extracted from epiwafers based on SOI than sapphire because these substrates are available in larger diameters. However, a switch to growth on material with a diameter of 200 mm or more may require the development of new MOCVD tools.

One important question that hangs over SOI is its price – it is five times that of silicon (111). But 150 mm SOI substrates are still cheaper than equivalently sized sapphire and prices should fall as silicon device manufacturers purchase more silicon implanted oxide (SIMOX) SOI substrates with diameters of up to 300 mm.

We have built devices that emit in a spectral region known as the green gap, which is a range of wavelengths where it is very challenging to produce LEDs with high quantum efficiencies from either



MOCVD growth on 6 inch silicon-on-insulator substrates produces thick crack-free GaN films that are processed into green and deep-green LEDs. Surface texturing has improved light output.

the InGaN family of alloys or the AlInGaP material system. Devices emitting efficiently at deep-green wavelengths (530–580 nm) are highly desirable because they can improve the color reproduction of displays based on red, green and blue LEDs.

The growth of nitride material on foreign substrates demands minimization of wafer bow, which is often addressed by introducing additional strain-balancing layers. Over the last nine years researchers at the Otto-von-Guericke University, Magdeburg, have been developing growth technologies for this purpose and they can now produce flat GaN-on-silicon epiwafers for LEDs and FETs. This success has encouraged the launch of a university spin-off, Azzurro Semiconductors, which now manufactures large GaN-on-silicon epiwafers.

We are currently working together to develop epitaxial structures on large SOI substrates and our goals are improvements in GaN material quality, elimination of bowing and better device performance. We have also processed InGaN/GaN LEDs from epiwafers grown at Azzurro. These MOCVD-

Fig. 1. (right) On-wafer electrical measurements of deep green, $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$, LEDs reveal a turn-on voltage of less than 3 V. **Fig. 2.** (far right) Electroluminescence spectra of deep-green LEDs feature Fabry-Perot fringes that are caused by multiple reflections at the AlN/silicon/ SiO_2 /silicon and top GaN/air interfaces.

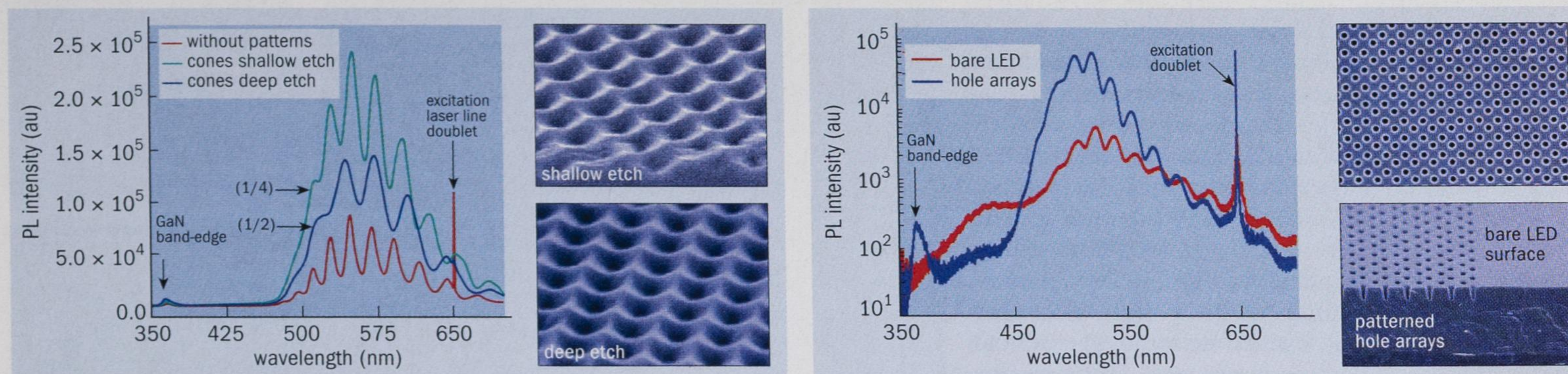
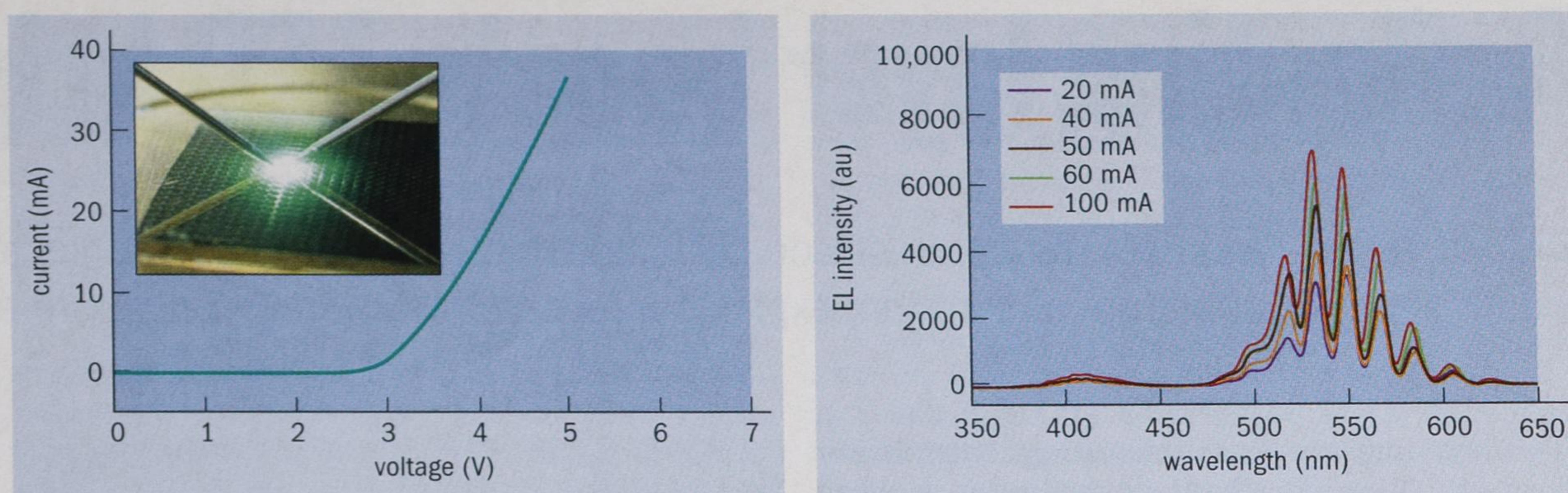


Fig. 3. (left) Surface nanopatterning of the deep-green LED structures produces an increase in photoluminescence, which is highest for shallow-etched material. These structures have been produced by etching 200 nm diameter holes into a SiO_2 mask. The (1/2) and (1/4) are multiplication factors for the intensity from the cones with deep and shallow etch, respectively. **Fig. 4.** (right) Periodic nanohole patterns produce an increase in the photoluminescence emission of green LED structures.

grown devices are the first blue-green and deep-green LEDs to be produced on SIMOX SOI wafers.

The epiwafers feature a thin silicon layer on top of the oxide that creates a compliant platform for nitride epitaxy. This allows the strain produced during growth to be shared between the silicon layer and the lattice-mismatched GaN layer that is deposited during LED growth.

We have produced a range of LEDs using silicon overlayers between 45 and 200 nm thick, and a 150–375 nm thick buried oxide. A high-temperature AlN buffer layer is deposited onto this platform, followed by an aluminum-rich intermediate layer and n-type silicon-doped GaN layers with three strain-compensating low-temperature AlN interlayers. A full LED structure completes the growth, which comprises a 2.70–2.75 μm silicon-doped GaN template, a five-period InGaN/GaN multi-quantum well and a 100 nm thick, magnesium-doped GaN layer.

Material quality has been determined with high-resolution X-ray diffraction, Raman spectroscopy and transmission electron microscopy (see box “Characterizing GaN-on-SOI structures”), before processing the epiwafers into devices at the Science and Engineering Research Council nanofabrication and characterization facilities at IMRE. $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$ square-shaped mesas were formed by multi-mask photolithography and inductively coupled plasma etching, and BCl_3 and Cl_2 gases enabled dry etching of GaN and exposure of underlying n-type silicon-doped GaN. The addition of a

Ni/Au-based p-contact and Ti/Al-based n-contact completed device fabrication.

Current-voltage and electroluminescence tests have been used to assess device performance (figure 1). GaN-on-SOI devices absorb far less light than our equivalents grown on silicon (111), thanks to reflection by the SOI structure. However, even with this benefit our green and deep-green LEDs only emit an average optical power output of 1.1 mW at 20 mA. But substantial improvements in radiant flux should be possible with suitable packaging, full encapsulation and surface roughening of the die.

Our 550 nm, deep-green LEDs have a striking characteristic – strong interference peaks (figure 2). This results from the SOI substrate reflectivity and multiple reflections at the AlN/SOI/ SiO_2 /silicon (111) boundaries. We have modeled this behavior and concluded that the emission profile is governed by substrate reflectivity changes and reflections at the top GaN/air interfaces. The emission of our deep-green LEDs extends to 600 nm and beyond, which suggests that they could provide a phosphor-free, broadband light source.

Maximizing light output

Like many other researchers, we are developing processes for improving LED light extraction, including efforts involving “nanosphere” lithography, reactive ion etching and, most recently, nanoimprint lithography. Research in this direction includes the development of lithographic processes

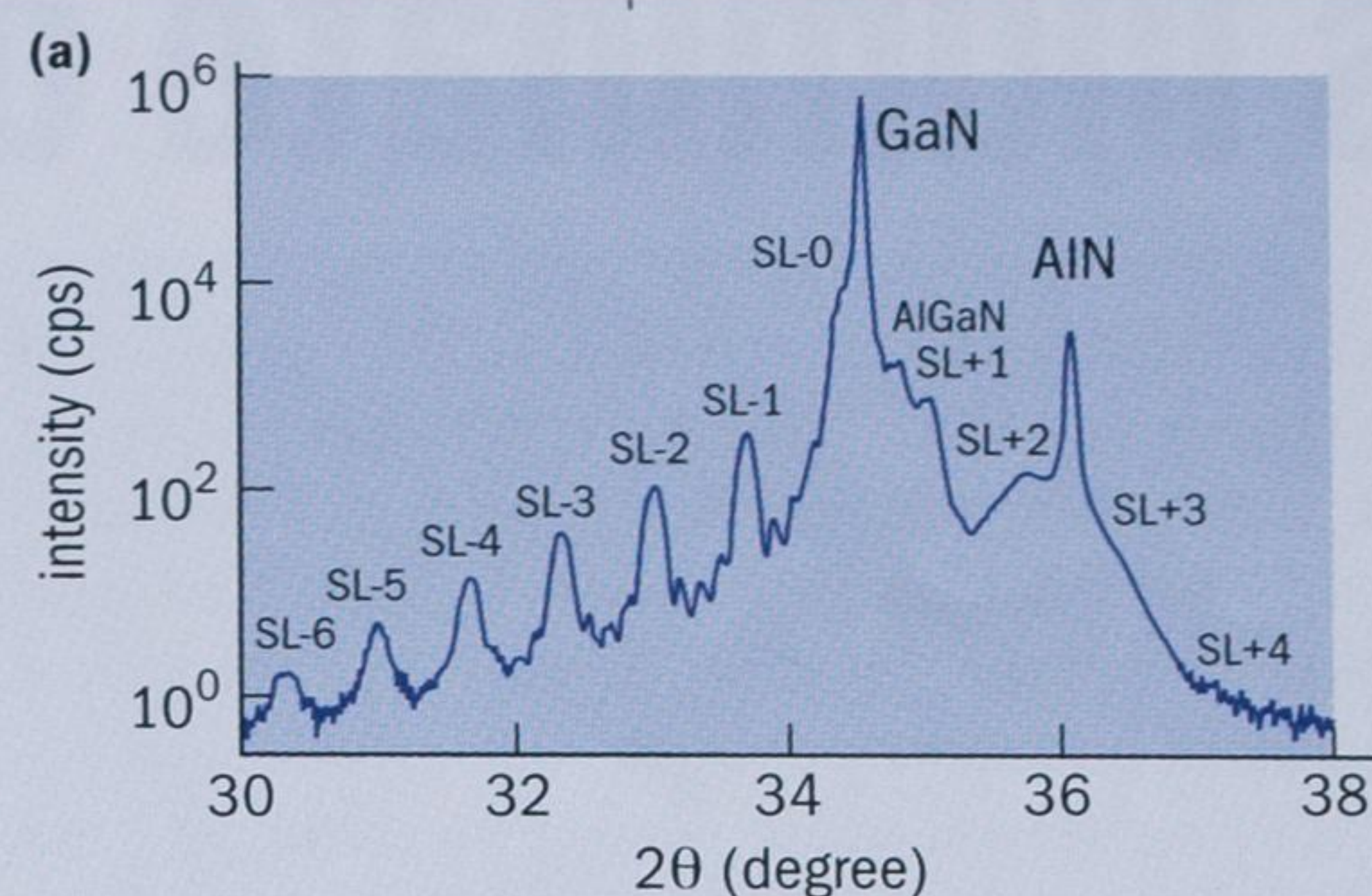
Characterizing GaN-on-SOI structures

Nitride epiwafers grown on SOI substrates have a similar quality to those grown on silicon, according to high-resolution X-ray diffraction (HRXRD), Raman spectroscopy and transmission electron microscopy (TEM).

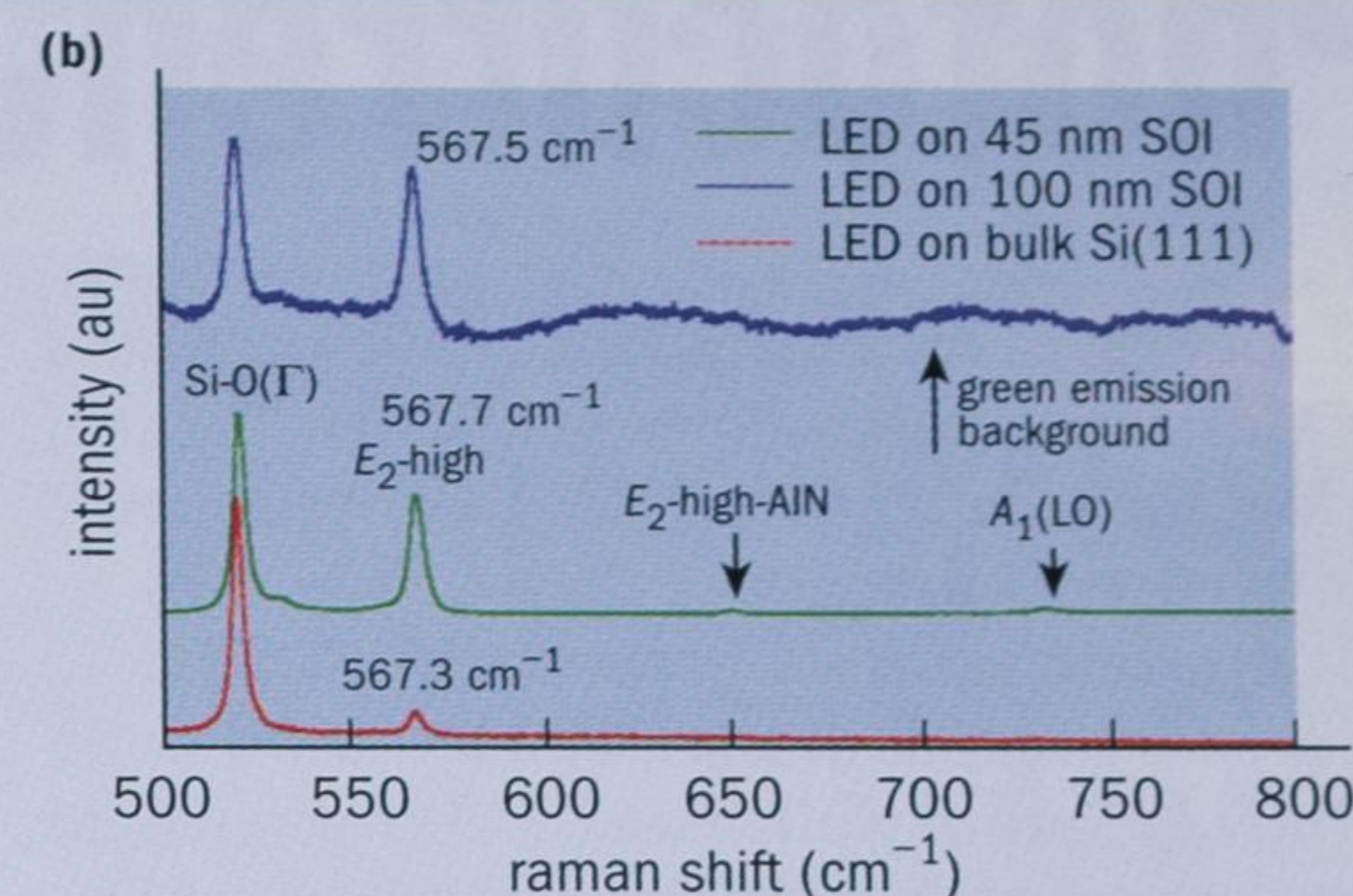
HRXRD shows the high degree of similarity between LEDs grown on three different SOI platforms – a 45 nm silicon overlayer with a 150 nm buried oxide, a 100 nm silicon overlayer with a 175 nm buried oxide and a 200 nm silicon overlayer with a 375 nm buried oxide

(a). The GaN peak's full width half maximum is 420 arcsec, comparable to the value for GaN grown on silicon. The multiple quantum-well superlattice produces many higher-order satellite peaks in the diffraction spectra, indicating that the active region contains high-quality material with sharp interfaces.

There is very little in-plane strain across



LEDs with silicon overlayers that are 45–50 nm and 100 nm thick, according to Raman spectroscopy **(b)**. The “ E_2 -high” optical phonon peak is at $567.2 \pm 0.2 \text{ cm}^{-1}$, which is incredibly close to the phonon peak for GaN on a strain-free, free-standing native substrate ($567.5 \pm 0.2 \text{ cm}^{-1}$). This implies that the



average tensile stress in the LED structure is less than 0.1 GPa.

TEM reveals screw and edge dislocations with a similar density to those in nitride LED structures on silicon. Efforts are underway to reduce the dislocations in the active region, which should help to improve LED efficiency.

for making two-dimensional photonic crystal structures that enhance extraction efficiency while controlling the direction and polarization state of the emitted light. Photonic LEDs can boost output by allowing photons to escape via multiple scattering steps from rough surfaces.

Our photonic crystal structures are created by depositing a SiO_2 mask over the LED and writing a pattern in this layer with electron-beam lithography. Reactive ion etching, followed by inductively coupled plasma etching into the nitride layers, defines the photonic crystals in our green and deep-green LEDs. We have investigated a variety of circular hole arrays with different diameters, including designs that arrange the holes in square and circular patterns.

The most promising design features nanocones on p-type GaN surfaces, which should increase the output of deep-green LEDs emitting at around 550 nm (figure 3). Photoluminescence studies show that the nanocones significantly increase light output, with an enhancement that depends on the internal angle of the cones. Shallow etching improves the outcoupling more than deeper etching, which penetrates into the active region. The latter approach causes plasma damage, but even this leads to a four-fold enhancement in photoluminescence intensity (figure 4).

The development of photonic crystal LEDs on SOI will continue and we have set ourselves the goal of producing electrically driven devices that triple the power output compared with planar GaN equivalents on bulk silicon substrates. Another target is to scale up the nanoimprint lithography process and we are also interested in developing phosphor-free white-light LEDs that generate their emission through careful control of the wavelength-dependent reflectivity of the substrate.

A key strength of the SOI platform is its suit-

ability for forming high-brightness, thin LED chips through simple sacrificial etching of the substrate. The device can be transferred to a high-thermal-conductivity, high-reflectivity platform to produce bright LEDs that could feature advanced light-extraction technologies. A similar process is used to make vertical blue and white LEDs from epitaxial material that is grown on sapphire. However, this requires laser lift-off to free the device from the substrate, which is more expensive than etching.

If SOI substrates are to enjoy commercial success in the manufacture of nitride LEDs, then this platform will have to demonstrate its benefits over a cheaper alternative – silicon – which can be separated from the device by lapping, grinding and plasma flattening. The battleground will be epitaxial quality and it is impossible to predict which type of platform will triumph – both technologies are still in their infancy. However, the more suitable platform will emerge as development moves to growth on 200 mm and even 300 mm material, where wafer bowing will present tougher challenges. But even if SOI loses out to silicon for this particular application, the uptake of SOI for microelectronics, nanoelectronics and the fabrication of optoelectromechanical systems and sensors, could lead to the manufacture of large, integrated chips that benefit from an on-board LED light source. ●

Further reading

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About the authors

Sudhiranjan Tripathy (top left) is a research scientist at the Institute of Materials Research and Engineering (IMRE), the Agency for Science, Technology and Research (A*STAR) in Singapore, and a project leader in the solid-state lighting program.

Armin Dadgar (top right) and **Alois Krost** (bottom left) hold positions at Otto-von-Guericke University and Azzurro Semiconductors.

Siew Lang Teo (bottom middle) and **Vivian Lin** (bottom right) are researchers at SNFC, IMRE.



LEDs

Photocurrents illuminate droop debate

Photocurrent measurements have provided another twist in the debate about the origin of droop, the reduction in GaN LED efficiency at high drive currents.

It has been widely assumed that carriers formed by resonant optical excitation in an InGaN quantum well of an LED are confined to this particular layer. But measurements by Fred Schubert and co-workers at Rensselaer Polytechnic Institute (RPI) have shown that photo-excited carriers can leak out of a well, even when this structure is not biased.

This finding casts a shadow over earlier experimental studies of LED droop. Schubert's team previously claimed that electron leakage is the cause of droop, and they employed the assumption that resonant optical excitation in the InGaN layer of an

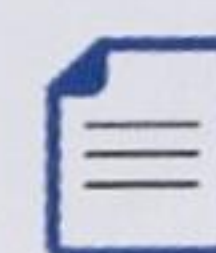
InGaN/GaN heterostructure did not lead to carrier escape in the interpretation of their experiments. The same assumption was also made by Philips Lumileds, which claimed that its optical experiments revealed that droop is caused by Auger recombination.

RPI's current view is that its experiments cannot determine whether Auger recombination or carrier escape is the cause of droop.

Photocurrent experiments were performed on $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$ devices with a conventional InGaN/GaN multiple quantum well and an electron blocking layer. These 460 nm LEDs produced significant photocurrent at all bias conditions when pumped by a 405 nm source. A photocurrent of just over $15\text{ }\mu\text{A}$ is produced at zero-bias under an excitation power of 1 mW.

Some researchers within the LED community think that sample variations are the root cause of the differences in opinion over the origin of droop. To address this concern, RPI has investigated samples from other manufacturers. "We measure carrier escape under resonant excitation in all of them," said Martin Schubert, son of Fred.

The team is now going to revisit its earlier work, including comparisons of external quantum efficiency and photoluminescence efficiency. "We're also going to look closely towards other experiments to gain clearer insight into what is going on in the LED under bias," explained Martin Schubert.



Journal reference

Accepted for publication in *Appl. Phys. Lett.*

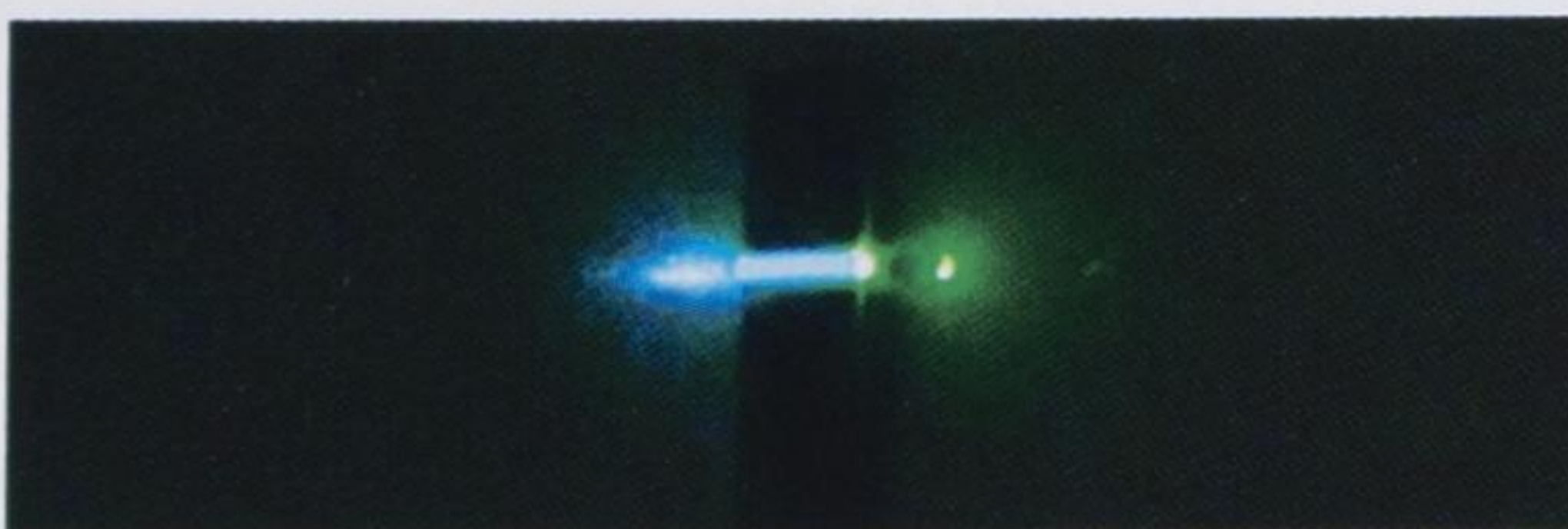
NOVEL MATERIALS

II-VIs produce optically pumped green lasing

The race to produce the first reliable green laser diode has another promising contender. Researchers from Sophia University, Japan, have produced a II-VI heterostructure with a BeZnSeTe active region that produces 548 nm lasing under optical excitation.

This result follows last year's announcement from the University of California, Santa Barbara, of spontaneous emission at 514 nm from a semi-polar nitride laser structure. The Japanese company Rohm is also targeting a green laser and has pushed its electrically pumped non-polar lasers from 405 to 481 nm over the last two years.

Sophia's structure has a threshold excitation density of 70 kW cm^{-2} , and the researchers estimate that the threshold current



Pumping a BeZnSeTe heterostructure with a 355 nm source produces lasing at 548 nm.

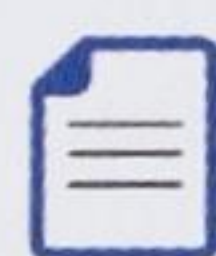
density of a green laser diode fabricated from this material would be $0.2\text{--}0.7\text{ kA cm}^{-2}$.

Materials related to BeZnSeTe, such as ZnCdSe and MgZnSSe, were developed in the 1990s to build blue-green lasers. These devices produced continuous-wave operation at room temperature, but lifetime was limited to 400 hours due to weak crystal bonds that led to defect generation and diffusion.

The latest structures address this issue, thanks to the inclusion of BeSe and BeTe components in the active material, which strengthen the lattice bonds.

Sophia's structure was produced in a two-chamber MBE system. An InP and InGaAs buffer was grown on InP in the III-V chamber, before the wafer was transferred to the II-VI chamber and irradiated with zinc to prevent nucleation of stacking faults. Deposition of the II-VI structure followed, which features a ZnCdSe buffer, MgSe/BeZnTe cladding layers and a BeZnSeTe active region.

Ichirou Nomura from Sophia University says that the biggest obstacle to producing an electrically pumped laser is the barrier to electron transport at an interface in the n-type region. This barrier can be eliminated by introducing a graded superlattice structure – an approach that has already paid dividends in yellow and green LEDs, which have lifetimes of 5000 hours.



Journal reference

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FETs

Non-polar plane boosts threshold voltage

The first *m*-plane enhancement-mode AlGaN/GaN FETs have been built by researchers from the University of California, Santa Barbara (UCSB).

These normally off FETs deliver a threshold voltage of 2 V. This makes them the leading candidate for switching applications, which require a threshold voltage of at least 3 V.

In comparison, enhancement mode *a*-plane

FETs from Mitsubishi Electric have a threshold voltage of 1.3 V and conventional *c*-plane FET designs that incorporate a thin AlGaN barrier, recessed gates or a pn junction gate, have threshold voltages of 1 V or less.

UCSB's transistors were grown by MOCVD on *m*-plane GaN and feature an unintentionally doped 300 nm thick channel layer, a 2 nm thick $\text{Al}_{0.36}\text{Ga}_{0.64}\text{N}$ spacer, a 13 nm thick silicon-doped $\text{Al}_{0.36}\text{Ga}_{0.64}\text{N}$ layer and a 6 nm thick $\text{Al}_{0.36}\text{Ga}_{0.64}\text{N}$ cap. Dry etching created the recessed-gate structure.

Drain-source current density peaked at 130 mA/mm, the on-to-off ratio exceeded

10^6 and transconductance hit 25 mS/mm.

UCSB's Tetsuya Fujiwara believes that threshold voltages of 3 V can be realized with a more appropriate gate metal, and optimization of the insulating and epitaxial layers.

The team also wants to increase the FET's drain current. "Our target is 1 A/mm, which is comparable to polar *c*-plane transistors," revealed Fujiwara. He hopes to realize this goal with δ -doped structures.



Journal reference

T Fujiwara et al. 2009 *Appl. Phys. Express* **2** 011001.

Germanium Substrates: Powering your Growth!



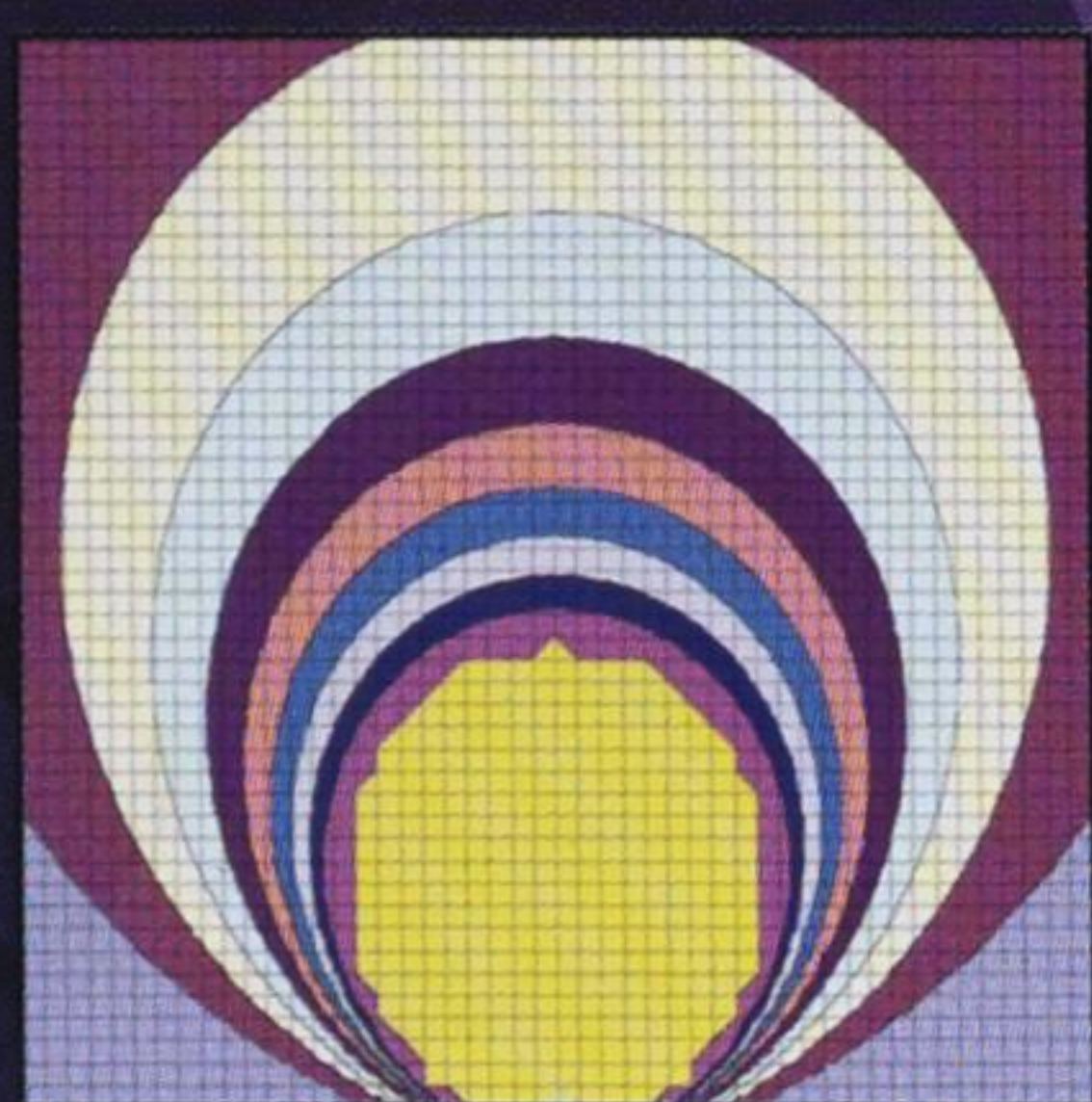
Umicore Electro-Optic Materials is the recognised world leader for the supply of Germanium substrates and offers epi-ready, dislocation free wafers ranging in diameter from 2" to 300 mm. Our material is the substrate of choice for the growth of the world most efficient solar cells used on space satellites and in terrestrial concentrator photovoltaic (CPV) systems.

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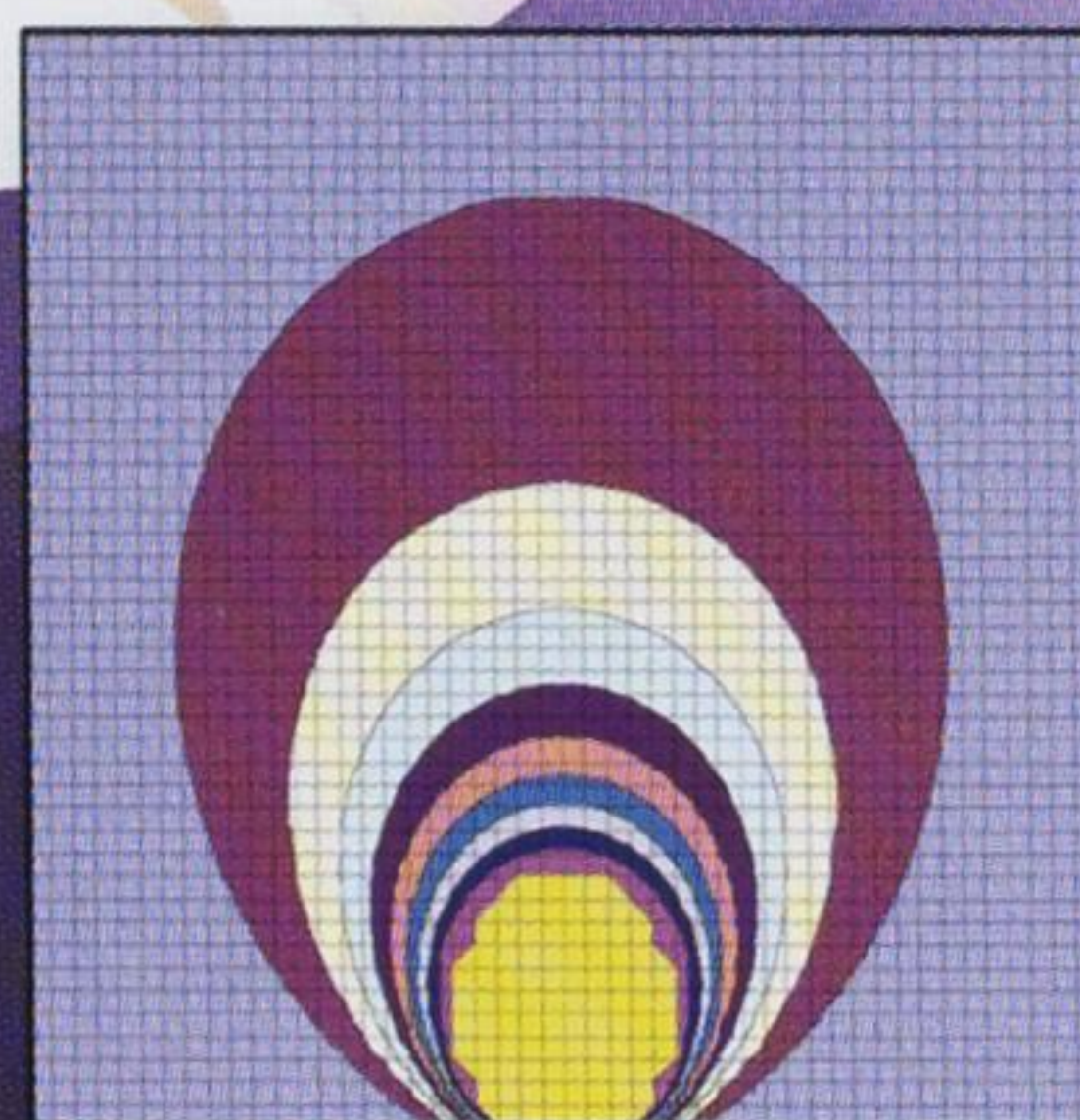
Umicore Electro-Optic Materials: Watertorenstraat 33, BE - 2250 Olen, Belgium

Tel +32 14 24 57 02 - Fax +32 14 24 58 00 - substrates@umicore.com - <http://substrates.umicore.com>

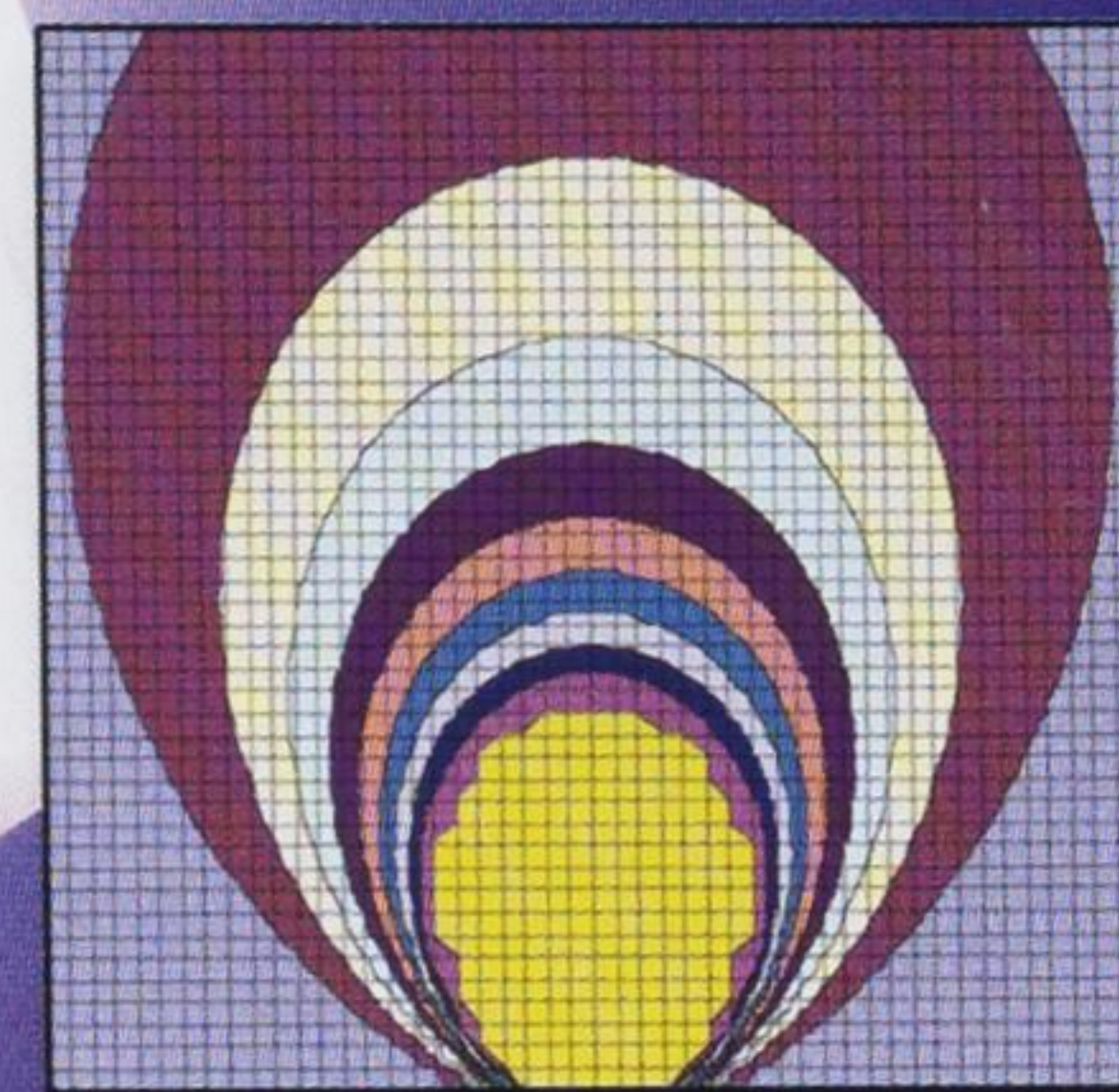
No Guesswork...



22 47.90
Ti
Titanium



78 195.09
Pt
Platinum



79 196.97
Au
Gold

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