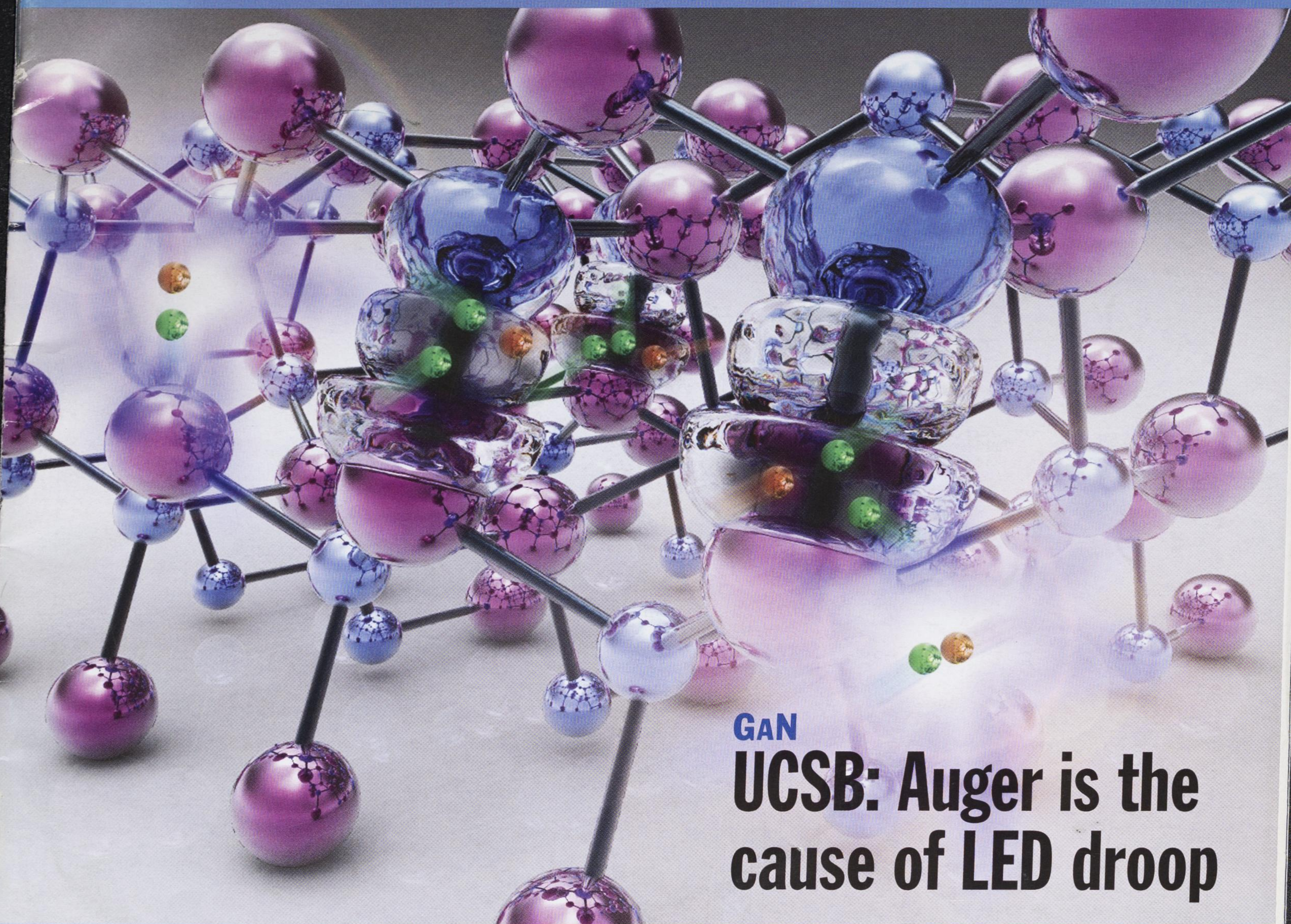


COMPOUND SEMICONDUCTOR

July 2009 Volume 15 Number 5

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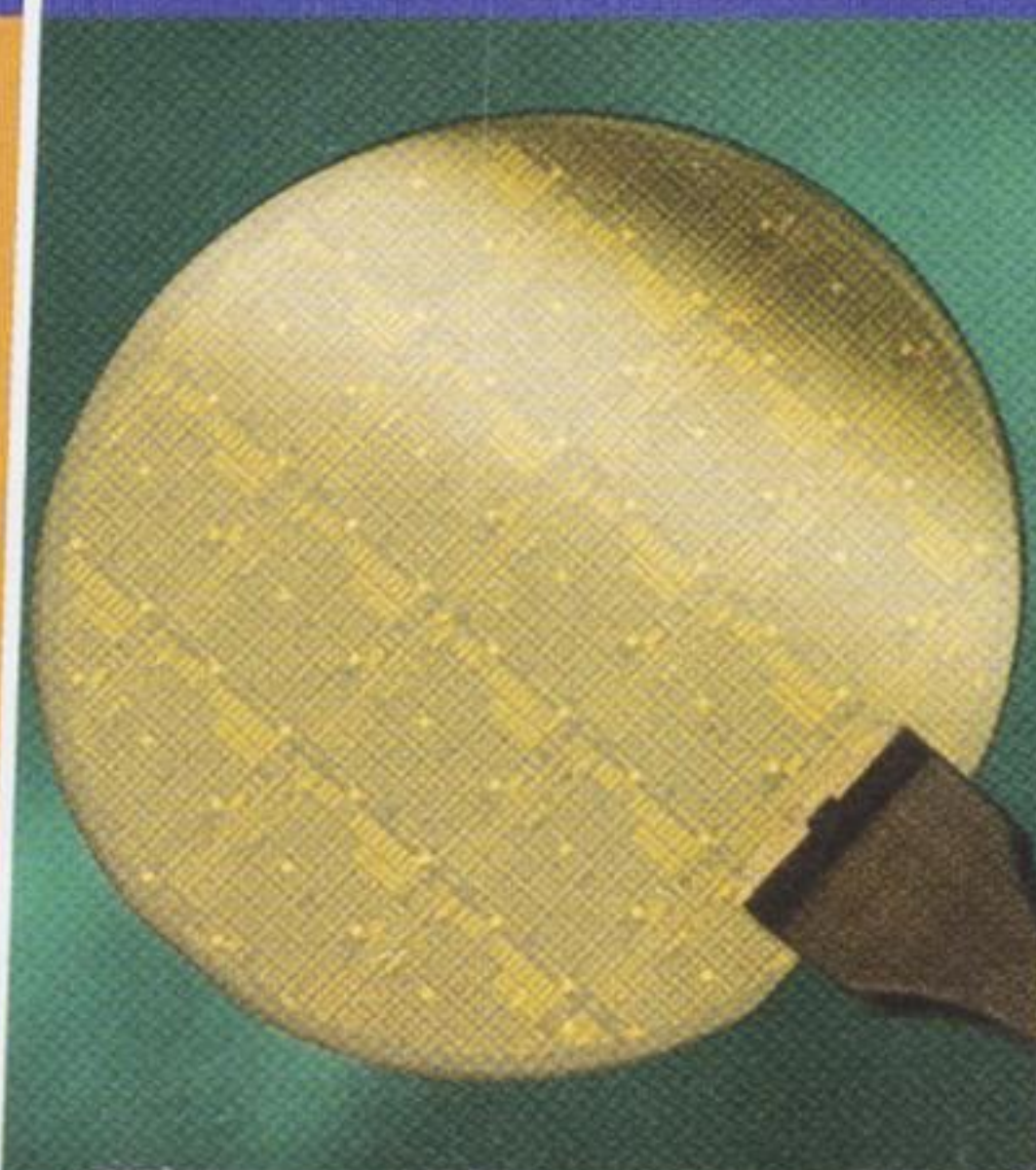


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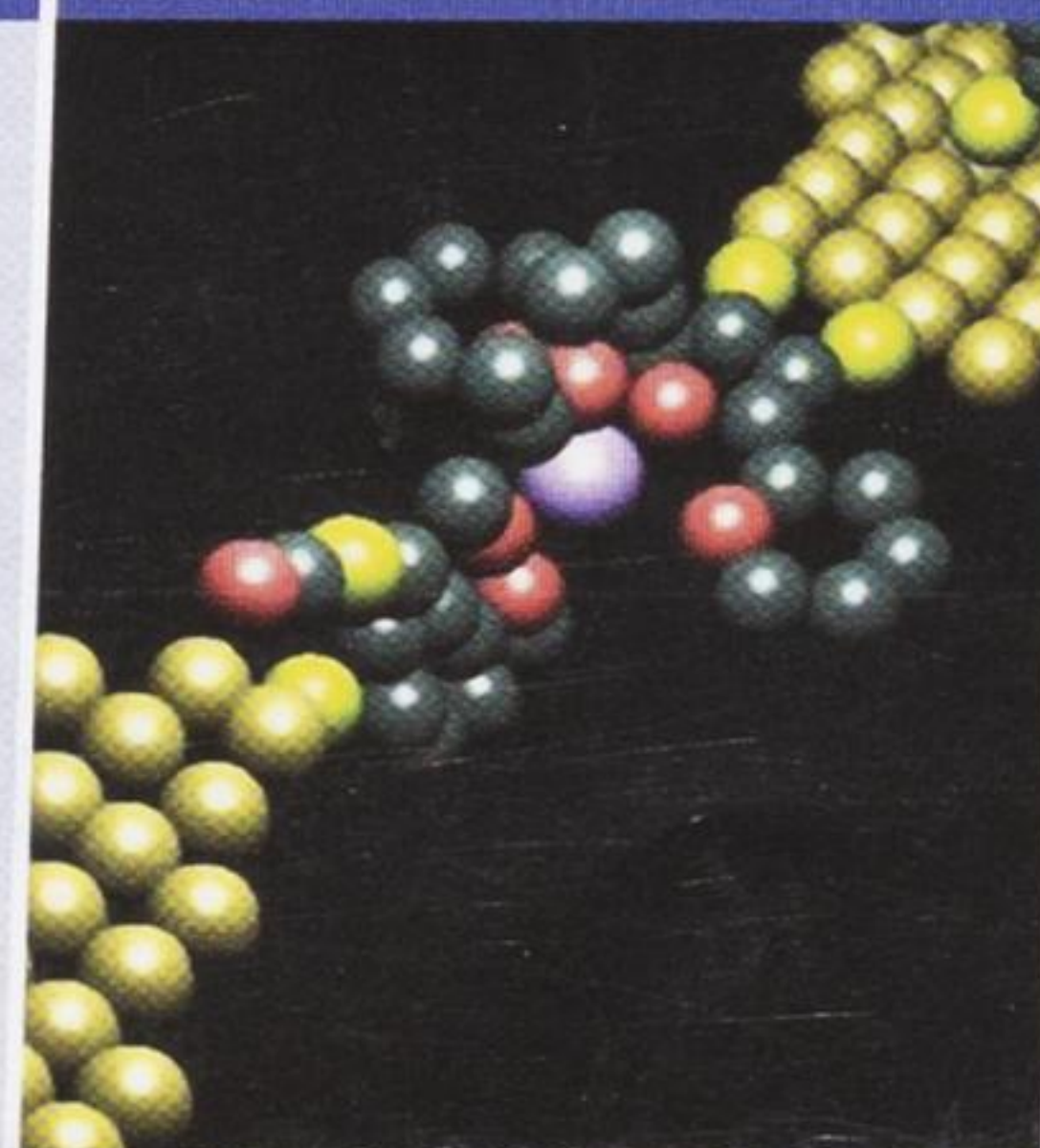
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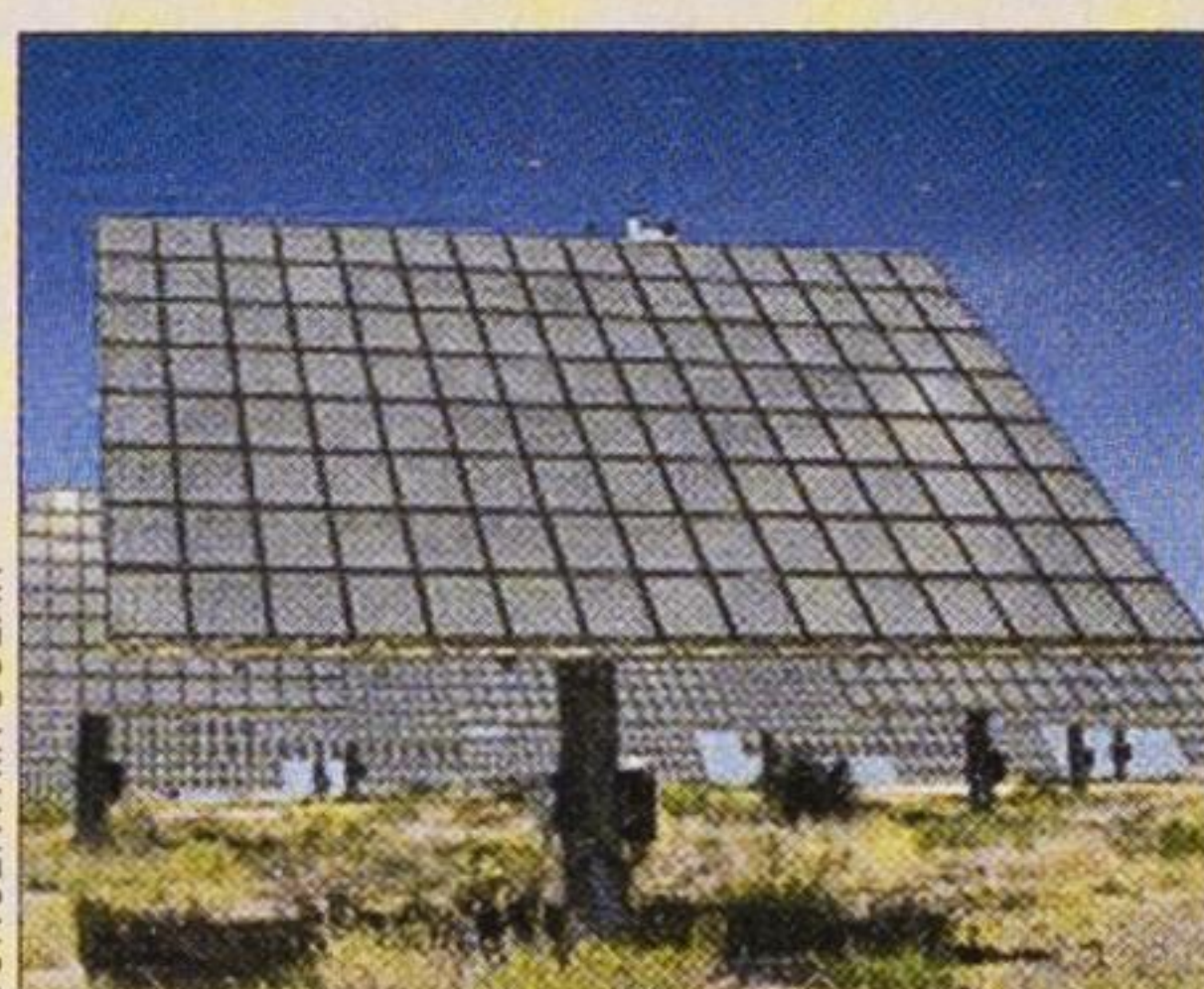
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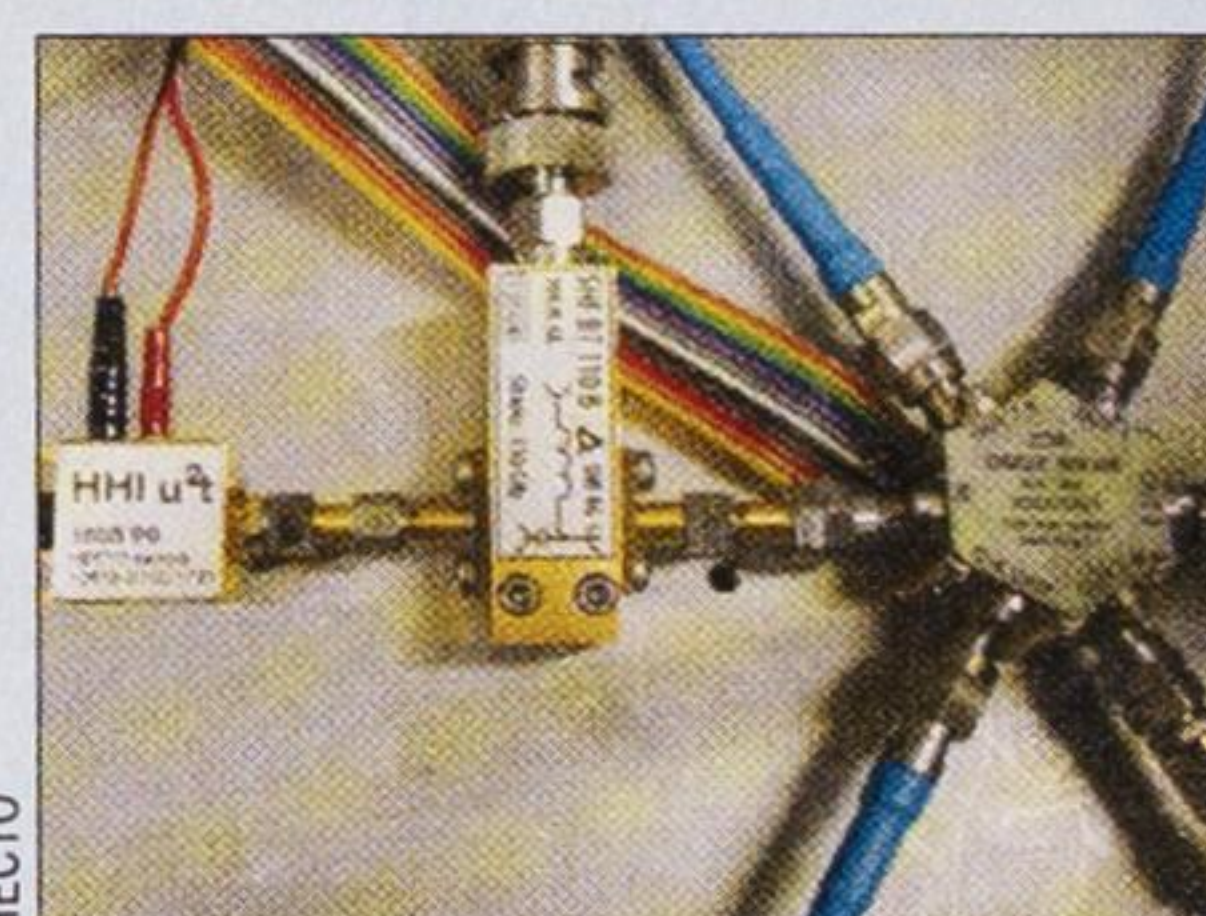
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25 **Submerged electrodes boost high-brightness LED output:** When metal electrodes are placed on the top of an LED, they reduce its emission area and increase internal absorption. But both of these problems can be completely eradicated with a buried n-type contact, say Osram Opto Semiconductors' Berthold Hahn, Karl Engl and Markus Klein.

29 **Miniaturized monolithic transceivers promise to boost Ethernet capacity:** One option for relieving the ever increasing strain on optical networks is to move to far higher bit rates. A European effort called HECTO has adopted that stance and developed 100 Gbit/s Ethernet transmitter chips based on InP, says project leader Urban Westergreen.



HECTO

Next generation

The HECTO project allowed for the design of two generations of components for 100 GbE. **p31**

32 **Research Review:** Oki Electric breaks power density record... Sapphire interlayer aids GaN-on-Si LED output... Silicon boosts InP MOSFET characteristics.

Main cover image: Computational scientists at the University of California, Santa Barbara, are claiming that Auger recombination is the primary cause of droop, the decline in GaN LED efficiency at high drive currents. Electroluminescence involves the radiative recombination of an electron (green) and a hole (orange). See p20. Credit: UCSB.

Editor Michael Hatcher
michael.hatcher@iop.org
Tel +44 117 930 1013. Fax +44 117 925 1942

Features editor Richard Stevenson
richard.stevenson@iop.org
Tel +44 117 930 1192

News editor Andy Exance
andy.exance@iop.org
Tel +44 117 930 1007

Senior sales executive David Iddon
david.iddon@iop.org
Tel +44 117 930 1032. Fax +44 117 920 0977

Business development manager Rosemarie Guardino
Guardino@ioppubusa.com
Tel +1 215 627 0880. Fax +1 215 627 0879

Sales executive Jeffrey Spratley
spratley@ioppubusa.com
Tel +1 215 627 0880

Senior Marketing Executive Claire Webber
claire.webber@iop.org
Tel +44 117 930 1165. Fax +44 117 920 0984

Publisher Michael Hatcher
Production Louise Unwin
Ad production Mark Trimnell
Art director Andrew Giaquinto
Technical illustrator Alison Tovey

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GaN RF takes a step forward



Coinciding with the MTT-S International Microwave Symposium held in Boston last month, the entry by RF Micro Devices (RFMD) into GaN foundry services is a timely move.

With the Defense Advanced Research Projects Agency (DARPA) recently approving the next stages of RF GaN projects led by Raytheon and TriQuint Semiconductor, there is renewed momentum in the sector as the next generation of wireless communications moves from the drawing board and into the field.

RFMD will have some catching up to do, however. It is not directly involved in the DARPA projects relating to GaN device development, whereas key competitors – such as Cree and TriQuint – are.

This may or may not prove to be a critical disadvantage. After all, RFMD's initial success in the GaAs department was based on its licensing of the HBT process first developed at TRW for military applications, rather than developing its own.

Cree, which is well entrenched in DARPA's programs – as a materials supplier and a device and process developer – used MTT-S to demonstrate its GaN technology, which includes 120 W HEMT transistors and a 50%-efficient Doherty amplifier.

Commercial supply deals for GaN RF devices are also coming to the fore. Cree appears to have stolen a march on rival Nitronex, which specializes in GaN-on-silicon technology, with a deal to supply the Korean firm RFHIC, which sells wireless components for cellular LTE and WiMAX applications.

In the longer term, GaN-on-silicon technology may find itself with a bigger, better opportunity in the power electronics sector.

No doubt the latest phases of the DARPA projects, which will focus on improving fab processes and delivering better wafer yields, will benefit the entire GaN community in the long run. The early beneficiaries include TriQuint's epiwafer supplier IQE, which has seen its contract extended.

Whether RFMD can compete with TriQuint and Cree, companies that can exploit their deep entrenchment in the defense community, remains to be seen. The Greensboro, NC, firm is banking on turning around a faster cycle time than its competitors. If it can achieve this while delivering on yield and quality, it should be able to take a healthy slice of GaN business.

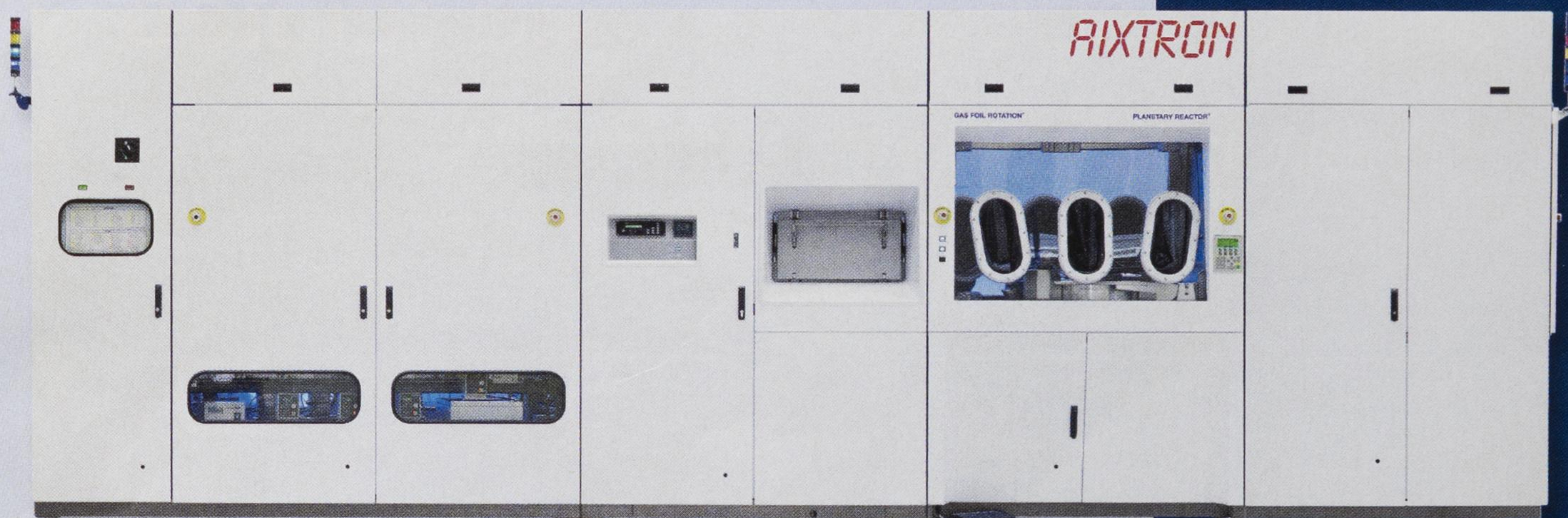
Michael Hatcher *Editor*

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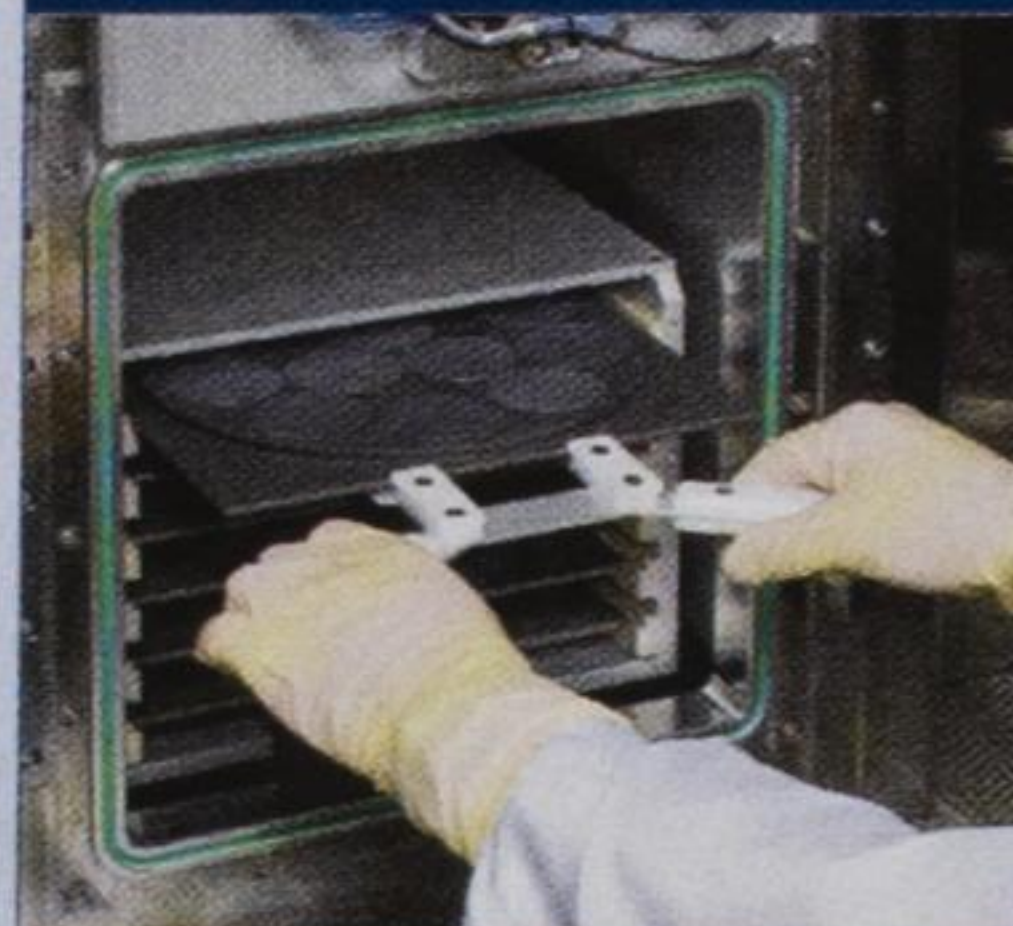
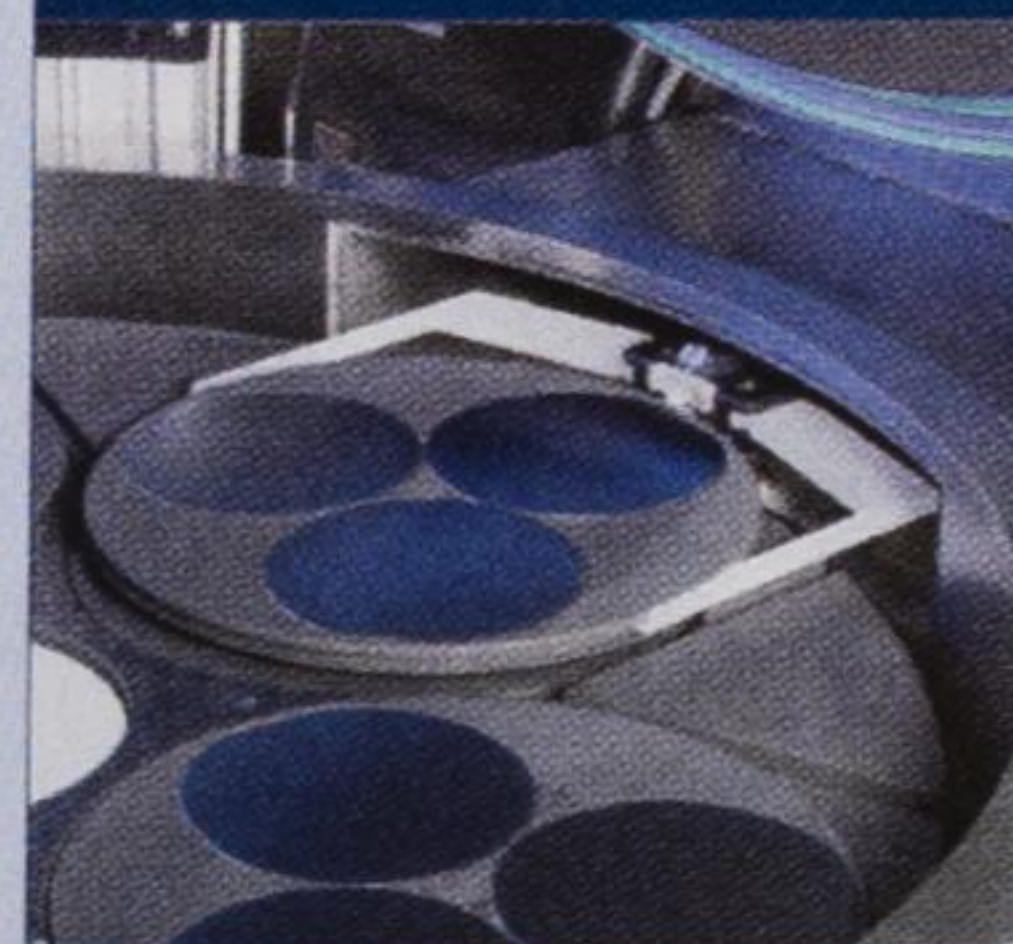
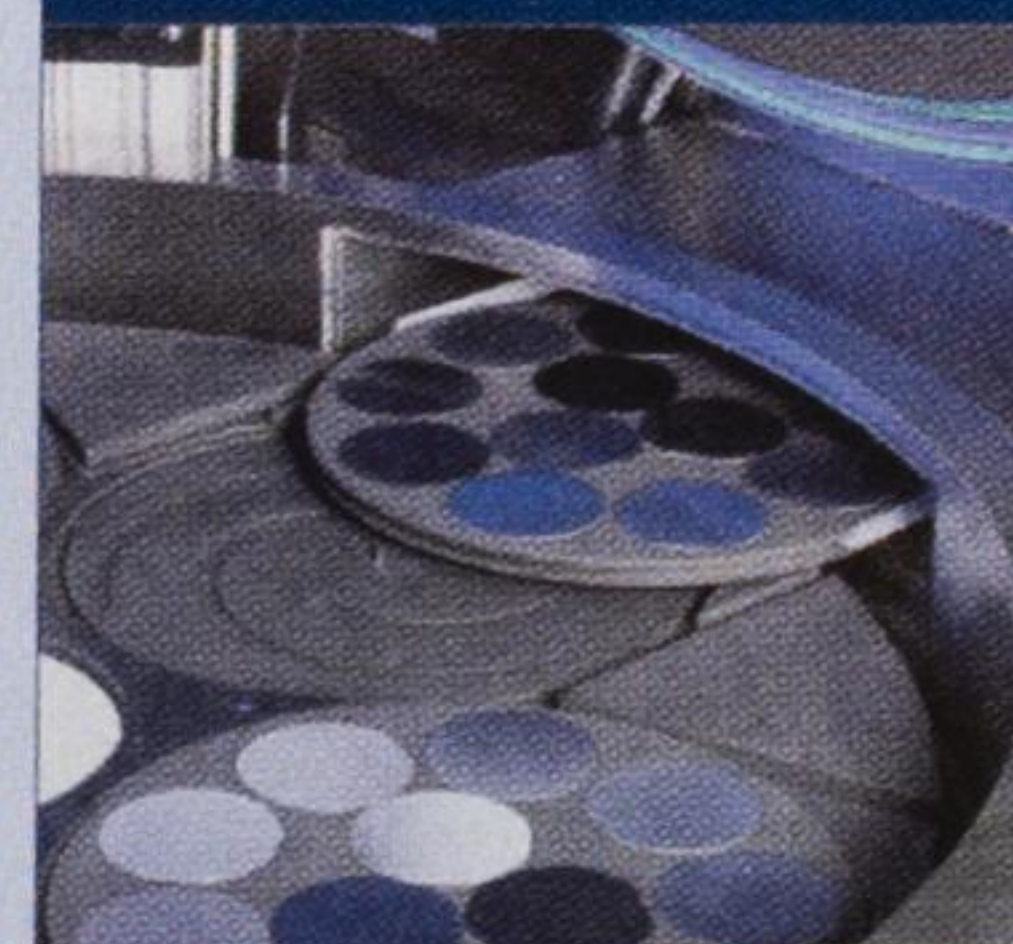
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GaN FOUNDRY

Nitronex snubbed by RFHIC's Cree switch

RFHIC says that GaN-on-SiC devices can be competitive with products manufactured on silicon wafers, thanks to economies of scale offered by its strategic partner Cree.

Cree announced that it had signed a strategic agreement with the fabless Korean wireless component manufacturer to supply it with GaN HEMTs at the beginning of June. This replaces the alliance that RFHIC entered in 2006 with Cree's Durham, NC, neighbor Nitronex, which produces GaN devices on silicon substrates.

Now, RFHIC's chief technology officer Samuel Cho has indicated that the latest deal is part of a clear move away from GaN-on-silicon. "We converted our product line and future direction to Cree's GaN-on-SiC HEMT technology based on its superior thermal and electrical characteristics as well as its outstanding robustness and reli-

ability," he said. "Cree is the clear winner."

The high-volume LED manufacturing business that Cree is better known for is founded on its SiC expertise, and RFHIC says that this is a major attraction. Cree's fab overhead will be shared with its SiC power products, which should bring "a significant cost benefit" in the long run, RFHIC told *Compound Semiconductor*. The collaboration strategy will see Cree focus on device and transistor-level products, and RFHIC working on hybrid and pallet amplifiers.

In response to Cho's comments, Nitronex director of marketing Ray Crampton claims that his company's latest products have better thermal performances than its competitors' offerings. "We have won major military designs at tier one customers based on performance and robustness advantages over SiC-based GaN HEMTs," he said. "Our

robustness is proven and accepted, as is our electrical and thermal performance."

"While I respect the potential of any competitor, RFHIC has not shown the ability to take advantage of the performance benefits of GaN and I don't expect them to be a significant player on the competitive field."

GaN development for RF applications owes a great deal to the DARPA Wide-Bandgap Semiconductor (WBGs) program, which has featured Cree in the largest of its three development projects.

In March Raytheon, which has collaborated with Cree on this project, was the first to announce that it had entered phase III of WBGs with a \$23.9 million contract. Fellow WBGs pioneer TriQuint gained \$16.5 million to progress the strand of the project in which it is leading Lockheed-Martin, BAE Systems, II-VI and IQE RF in early June.

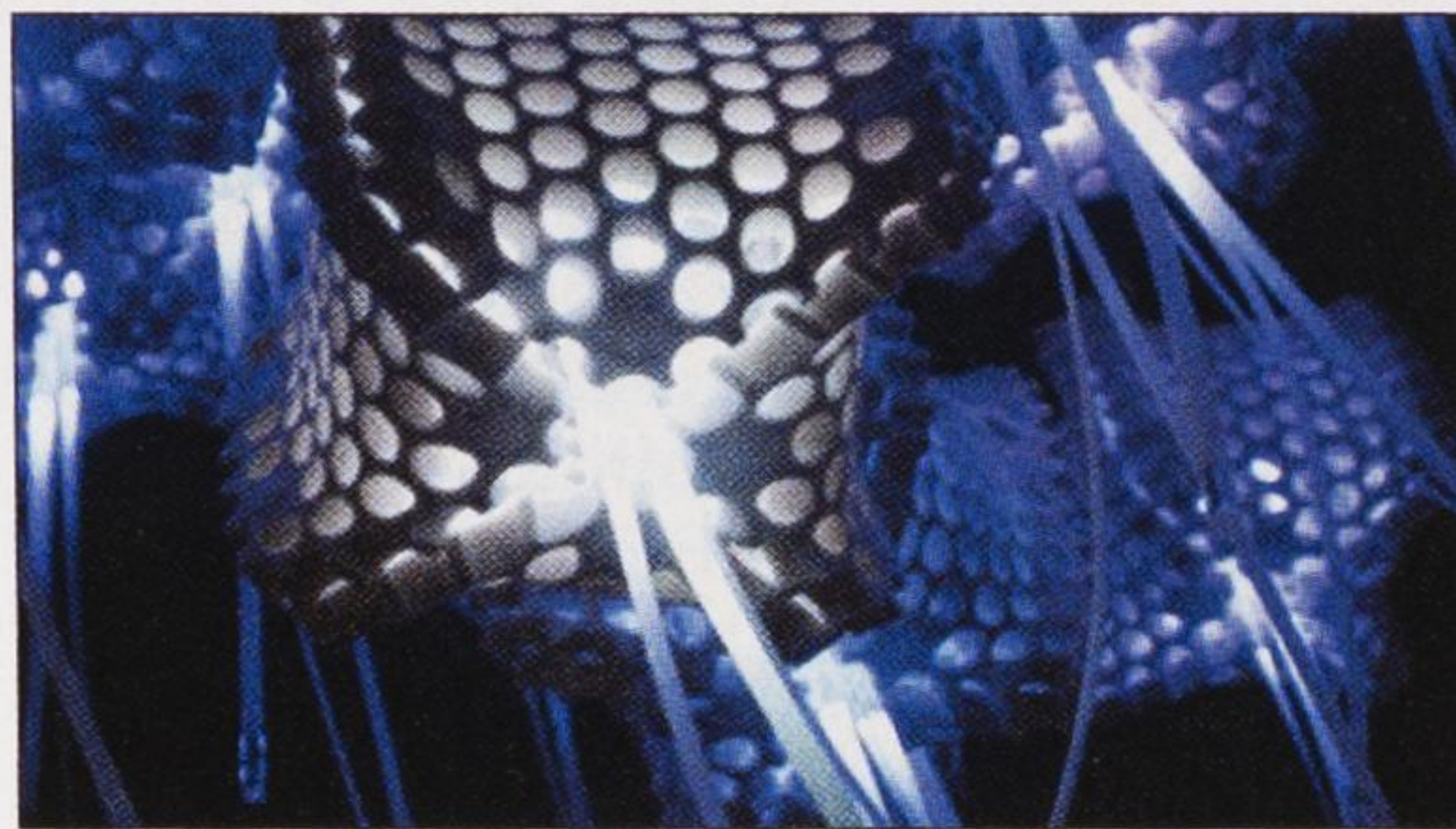
SOLID-STATE ILLUMINATION

Appeals court halts Epistar import ban

Rival AlGaInP LED makers Epistar and Philips Lumileds each claim to have won victory in the latest round of their intellectual property saga.

In May, the US Court of Appeals for the Federal Circuit ruled partly in favor of both companies in a set of disputes surrounding Lumileds' US patent 5,008,718 ('718). While neither chip manufacturer could claim a complete victory, the US International Trade Commission (ITC) was found to have made errors in its previous investigation.

One was that the ITC did not allow Epistar to challenge the validity of the Lumileds patent, while it also made a mistake by extending the "limited exclusion order" (LEO), which barred US imports of Epistar prod-



Philips Lumileds' Rebel LEDs will be classified by color temperature values rather than "warm", "cool" and "neutral", after discussions with designers.

ucts, to other products made by third parties that feature Epistar's AlGaInP chips.

Lumileds picked out the court's confirmation of the ITC's original ruling – that Epistar had infringed the '718 patent – as a positive result.

However, the appeals court overturned the ITC's prior ruling that Epistar could not

contest that patent's validity. Perhaps more worrying for Lumileds is the ruling that the LEO should be referred back to the ITC for further investigation – the result of a change in the law made after the ITC's decision.

Epistar will now proceed with its action against Lumileds in the US District Court of Northern California, in which it accused Lumileds of breaching a 2004 settlement between the two firms.

Lumileds will also pursue a pending infringement suit against Epistar over three patents, including '718.

● Philips Lumileds has also said that it will drop the familiar "warm", "cool" and "neutral" terminology that refers to the color temperature of its white emitters in favor of closely specified numerical values.

The company will now introduce Luxeon Rebel packages using its GaN emitters to produce 2700, 3000, 3500 and 4000 K white light through the course of 2009.

OPTOELECTRONICS

Nichia's green laser diode reaches 515 nm

Nichia has produced individual 515 nm continuous-wave laser diodes, crashing past the 500 nm mark, which was previously the longest wavelength reached by electrically driven InGaN lasers.

The Japanese GaN pioneer did not provide

reliability data for the 515 nm devices, but it also produced 510–513 nm diodes that operate for 500 hours without a change in their electrical characteristics. Beyond 500 hours the lasers' performance steadily degraded. The Nichia researchers estimated their overall lifetime – which is defined as ending when operating current increases by 30% from its initial value – to be 5000 hours.

In an *Applied Physics Express* paper published on May 22, the team developing

the lasers reported a separate confinement heterostructure diode "almost the same as" a design dating back to 2001. Optimized MOCVD processes are critical to producing the high-indium-content material required to access green wavelengths on a free-standing c-plane GaN substrate.

"We improved the growth condition of epitaxial layers," the Nichia team wrote. "The crystal quality was improved even in indium-rich InGaN active layers."

DEVICE CHARACTERIZATION

Atom probe aids UCSB's cluster search



The HR-LEAP tool from Imago Scientific Industries has entered the analytical mainstream, says the firm.

The University of California, Santa Barbara (UCSB) is exploiting a new analytical tool to solve a wide range of problems in GaN-related electronic materials, according to Jim Speck, a professor in UCSB's materials department and a specialist in wide-bandgap semiconductors.

The high-resolution local-electrode atom probe (HR-LEAP) is said by supplier Imago Scientific Industries to be the only one of its type currently in operation in North America. Using it will enable Speck and colleagues at UCSB to analyze materials in three dimensions and on an atomic scale, revealing the composition of structures in unprecedented detail.

"In the area of electronic materials," added Speck, "the atom probe will be used to solve key problems in interfacial chemistry and abruptness, alloy composition and homogeneity, and dopant and impurity concentrations in wide-bandgap semiconductor structures."

Speck told *Compound Semiconductor* that, thanks to the atomic-scale spatial resolution that the probe is capable of, researchers would be able to directly measure nanoscale features that can only be inferred using traditional analysis. The professor confirmed that one of the issues of primary interest to his UCSB colleagues, and a key motivation for acquiring the HR-LEAP tool, was the supposed presence of indium-rich clusters inside InGaN light emitters.

This contentious issue has divided the GaN community, with many believing that such clusters are responsible for the localized excitonic emission that allows these defect-riddled structures to emit light effectively. But in 2007, Colin Humphreys' team at the UK's University of Cambridge investigated

high-quality InGaN structures with an atom probe, finding no evidence for indium-rich clusters at the nanometer scale.

GaN-based research at the same institution is benefiting from an award made under the US economic stimulus plan, with another III-V expert, John Bowers, heading up UCSB's new \$19 million Energy Frontier Research Center (EFRC). As part of work carried out at the Santa Barbara EFRC, which was one of 46 such centers unveiled by the White House on April 27, Speck says that the Imago probe is likely to feature in basic studies of InGaN emitters destined for solid-state lighting applications.

SOLID-STATE ILLUMINATION

Korean companies intensify LED attack

Three major Korean companies are making key investments in their LED manufacturing operations, as the country seeks to become one of the top three LED producers.

Seoul Semiconductor's managing director Sewook Chun says that his company is planning a plant expansion in anticipation of the Korean LED market expanding by 50% on average through to 2011.

According to a recent report from market analyst IMS Research, Seoul Semiconductor became the fourth largest supplier of LED components in 2007. "Philips Lumileds may face competition for third spot from Seoul Semiconductor in the next few years," said IMS expert Jamie Fox.

Meanwhile, Chinese state news agency Xinhua has said that electronics giant Samsung plans another \$60 million investment in its Tianjin LED production facility. A source at the company says that Samsung Electro-Mechanics transferred the Tianjin site to Samsung LED, which was officially founded on April 1. Xinhua quotes Zhang Liang of the Tianjin Economic-Technological Development Area Administration Commission as saying that Samsung's investment would reach \$90 million. He estimated the starting capital value of the site to be \$30 million.

In April, LG Display took a 29.8% stake in Woori LED Co Ltd, for KRW11.9 billion (\$9.65 million), according to Thomson Financial. This is after the leading TFT-LCD manufacturer formed an alliance with US LED maker Cree in January to develop manufacturing facilities for display backlighting.

The Korean government announced a year ago that it would make a KRW3 trillion investment to push its domestic LED facilities further into the global elite.

Chun says that the Korean Agency for Technology and Standards (KATS) is now



Samsung is using Skyworks Solutions' EDGE front ends to power a variety of new handsets including the S5230 mobile phone, one of several new full touch-screen offerings recently launched in European markets. Skyworks is also supporting the Samsung S3310, an ultra-thin quad-band GSM/EDGE phone capable of global roaming. While these models exploit Skyworks' GaAs technology, the company has branched out by buying fabless silicon power amplifier (PA) specialist Axiom Microdevices in early June. The Woburn, MA, wireless chip maker says that Axiom is the world's only high-volume manufacturer of CMOS PAs.

also working to establish the sector as a "green growth industry". After the government initiated Green Growth Seoul in February, in which public institutions exploit solid-state lighting, KATS will also implement a "green standard policy".

"Facilitated by government policies, future demands will consistently grow," the Seoul Semiconductor executive told *Compound Semiconductor*. "LEDs will be comprehensively installed in the buildings of public companies and their use will extend to traffic lights, streetlights, guard lamps and tunnel lights." He says that the Samsung Economic Research Institute has predicted that a boom in the field could create up to 880,000 jobs.

CREDIT CRUNCH

Aviza looks to Sumitomo for rescue

Aviza Technology is set to sell parts of its etch and deposition semiconductor manufacturing equipment business to Sumitomo Precision Products, as it seeks bankruptcy protection. The California-based company filed for protection under Chapter 11 of the US bankruptcy code on June 9 after signing a non-binding agreement with Sumitomo.

"Through the bankruptcy proceedings, the company intends to pursue its proposed strategic transaction and other significant asset sales to maximize value on behalf of

all of the company's stakeholders," Aviza said in a statement. The bankruptcy filing comes after the equipment manufacturer failed to release its financial results for the first quarter of 2009.

Instead Aviza updated its financial position on April 28, saying that it would miss sales and profit guidance by some distance. Having expected revenues of between \$13 million and \$18 million, the firm saw sales of between \$9.5 million and \$11 million.

The sudden decline resulted in a net loss of at least \$5 million, aside from restructuring costs of around \$9.5 million. With cash assets of only \$6.7 million listed on its balance sheet as of December 26, the company was clearly in trouble. In a letter dated May 20 the company's bankers said that it must immediately repay its whole \$29.5 million credit balance.

Aviza had hoped that GaAs-based RFIC and high-brightness LED sectors would help to power a recovery after it shipped a number of systems to leading manufacturers last year. The company had been under threat of expulsion from the Nasdaq exchange for some time because of the low value of its shares, but its bankruptcy finally saw it delisted on June 19.

GaAs MANUFACTURING

RFMD: phone supply chain back in synch

Better-than-expected demand for RF components and a synchronized cell phone handset supply chain have triggered another upward surge in the share price of RF Micro Devices (RFMD).

Presenting to the investor community at the Barclays Capital Wireless and Wireline Conference in May, CEO Bob Bruggeworth

said that the III-V chip maker is seeing significant growth in both its cellular and multi-market product groups.

The positive outlook prompted an upgrade from wireless industry specialist Charter Equity Research, and sent RFMD's share price up nearly 10% to \$2.73. Since hitting a 2009 low of \$0.76 in early March, the firm's share value had more than quadrupled by mid-June. Although Bruggeworth still expects the handset market to contract by between 10 and 12% this year, compared with 2008, he stresses that the industry supply chain is now "synchronized".

In September last year, that synchronicity was disturbed when consumers stopped buying handsets in such large numbers. Within a couple of months, the supply chain had reacted, with demand for components like RFMD's GaAs power amplifiers plummeting as inventories were cleared.

As a result, RFMD's factory utilization rate stood at just 25% in the March 2009 quarter, with the company idling its original 4 inch wafer fab and consolidating III-V manufacturing into its two 6 inch fabs. For the quarter ended June this year, utilization is expected to be in the 75% range, indicating that the supply chain is working normally again.

Outside of handsets, Bruggeworth says that apart from a sluggish market for line amplifiers used in cable TV infrastructure, all product lines are witnessing an upturn in demand. He adds that the firm is working on a new type of switch, based on silicon-on-insulator technology. RFMD currently uses a GaAs PHEMT process to make switches.

Efforts to reduce the size of the GaAs die in its products also appear about to come to fruition, with 40 customers now engaged, and the March to June period representing the first full quarter of volume shipments of products using the smaller die.



From our newsfeed...

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...Raytheon builds more GaAs radars

Raytheon has won a \$54 million US Navy contract to retrofit up to 29 Super Hornet aircraft with APG-79 active electronically scanned array radars. The radars rely on transmit/receive modules populated with GaAs MMICs, many of which are made at the defense firm's Andover, MA, foundry.

...Intel pushes Japanese WiMAX launch

PC processor manufacturer Intel has extended its collaboration with UQ Communications in Japan in which it will promote and expand

the availability of UQ's commercial WiMAX service. The mobile WiMAX offering is officially launched in July, with the help of an additional \$43 million from Intel.

...Jazz makes SiGe tuners for LG TVs

Jazz Semiconductor has entered volume production on a SiGe tuner selected by LG for its high-end flat-panel TVs in partnership with Xceive Corporation. Xceive uses the Californian foundry's 0.18µm SiGe BiCMOS process to shrink its XC5000 tuner's size while retaining performance for analog and digital signals.

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DISPLAY BACKLIGHTING

LED notebook market ramping quickly



Today, at least two-thirds of Dell's E-Family laptops are shipped with LED backlights, and the company will use LEDs in all of its notebooks by 2010.

The proliferation of notebook PCs backlit with LEDs will deliver annual revenues of \$800 million to chip makers next year.

That's according to Jamie Fox, a market analyst at UK-based IMS Research, who describes the ramp as explosive. "Dell has already publicly committed to using LEDs in all [of its] notebooks by 2010, and other manufacturers are also committed to a surge

in LED notebook backlighting in 2009 and 2010," reckoned Fox.

Worth around \$200 million last year, Fox is expecting exponential growth in 2009 and 2010 as the market for LEDs in notebooks doubles year on year. Featuring in around 10% of all notebooks made in 2008, he also predicts that market penetration will approach 50% by 2010. Fox estimates that notebooks typically require between 60 and 70 LED chips.

Because LCD televisions are much larger, and also typically plugged into the mains rather than battery-powered, the TV market is adopting solid-state lighting technology at a much slower rate. Fox also suggests that there have been technical difficulties incorporating LEDs into TV backlights, where picture quality is paramount.

However, with companies like Samsung now marketing the benefits of the technology, Fox admits that the first half of 2009 has seen renewed optimism for LED-lit TVs.

The one downside, as far as the analyst is concerned, is that the market for LEDs used in notebook PCs will saturate rapidly after the next two or three years of explosive growth. At that point, revenues from TV applications and, increasingly, general lighting should be ramping up quickly.

Rival industry researcher Displaysearch sees LED backlight penetration in displays larger than 10 inches reaching 25% by the end of 2009, supporting Fox's longer-term view. It says that 10 million such displays were shipped in the first quarter of 2009.

"As LED production shares the same capacity with the lighting market, the display market has some concerns over availability," warned David Hsieh, Displaysearch's vice-president. "LED supply chain management will be a key factor for panel makers and will reshuffle the competition landscape from now to 2010."

OPTICAL COMMUNICATIONS

Oclaro deal pressures rival captive fabs

The aggressive moves that Oclaro is making to reshape the optoelectronic industry will lead to more sales of laser diode fabs, according to CEO Alain Couder.

Oclaro announced that it will acquire the Spectra Physics high-power diode business of Newport Corporation on June 3. Diode production will move from Spectra Physics' Tucson, AZ, laser fab into its own operations in Caswell, UK, and Zurich, Switzerland.

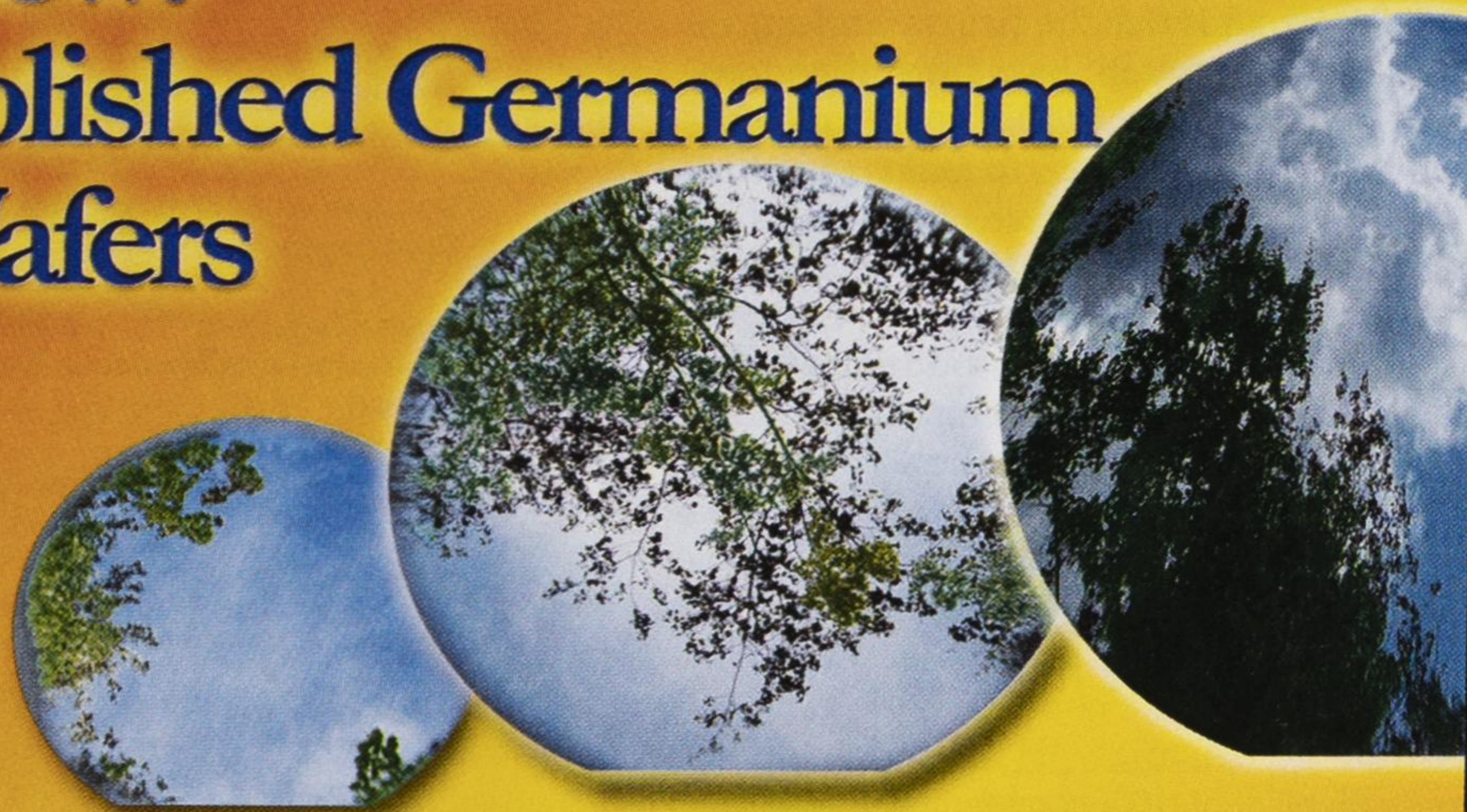
The acquisition is intended to further strengthen Oclaro's technical knowledge in this area, and improve its manufacturing efficiency by increasing utilization of the European fabs. Couder says that this "critical mass" is in distinct contrast to other vertically integrated laser diode manufacturers. "Our view of the industry is that there are too many fabs in the world right now, but some of them are pretty small and not efficient enough," he said.

"Oclaro has been able to build a state-of-the-art fab, which is quite efficient and we are already selling diodes to other companies because we do a better job on performance and cost. We expect that over time some of those companies will decide to divest their fabs and put more business into our business," he added.

Newport has exchanged the Spectra Physics business plus \$3 million in exchange for Oclaro's New Focus brand of photonics products, which are aimed at a broad range of manufacturing industries. The two companies have also signed a four-year supply deal, with Newport pledging to buy all of its diodes from Oclaro for the first year.

The supply deal is "strategic", Couder says, with Newport designing Oclaro components into its products, which should ensure that the relationship continues beyond the initial four-year period. Coming just a few weeks after Oclaro was formed by

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A11 ☐ Other (please specify) _____

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(tick one box only)

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B3 ☐ Academic/government semiconductor research center

B4 ☐ Epiwafer supplier

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B6 ☐ Semiconductor equipment or semiconductor materials company

B7 ☐ Finance or investment firm or market research/analysis

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4. What semiconductor materials/processes are used/developed at the place where you work? (tick all that apply)

C1 ☐ III-Vs: arsenides

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C4 ☐ III-Vs: antimonides

C5 ☐ II-VIs

C6 ☐ SiC

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C8 ☐ Other (please specify) _____

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D3 ☐ Wide bandgap ICs or discretes

D4 ☐ Devices employing SiGe, SOI or other silicon heterostructures

D5 ☐ Telecom laser diodes

D6 ☐ Non-telecom laser diodes

D7 ☐ VCSELs

D8 ☐ LEDs

D9 ☐ Solar cells

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E2 ☐ Semiconductor International

E3 ☐ Solid State Technology

E4 ☐ Laser Focus World

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E6 ☐ Other (please specify) _____

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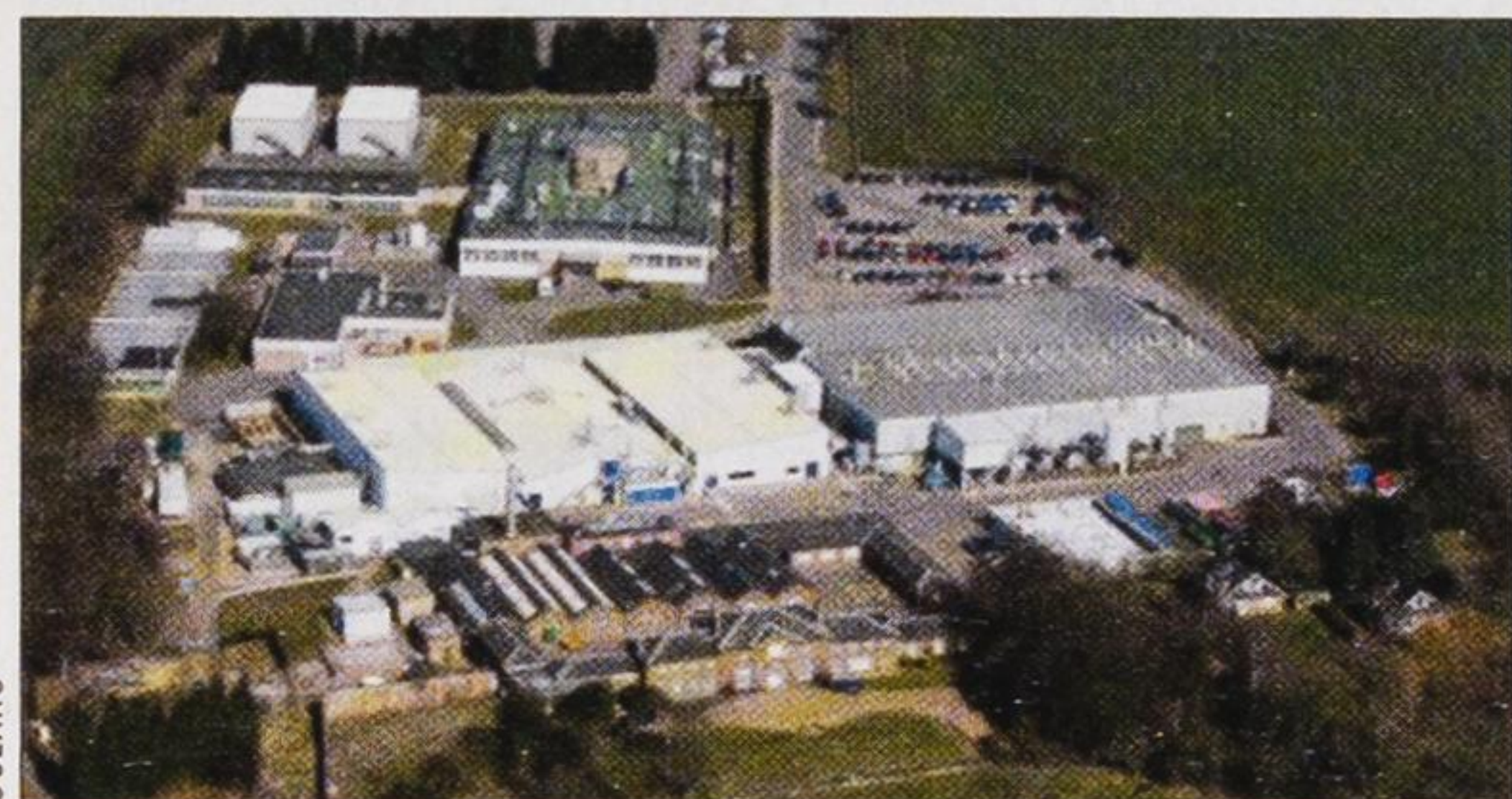
the merger between Avanex and Bookham in late April, this deal increases the firm's focus on telecommunications modules and optical components.

Although InP and GaAs chip manufacturing will move away from Tucson over the next 12 months, some employees will be retained at the site. This team will provide some historical Spectra Physics expertise in systems and packaging that Couder says was otherwise missing from Oclaro's high-power diode business.

The \$3 million should cover the costs of integrating Spectra Physics into Oclaro. Currently, revenues from New Focus and Spectra Physics are equivalent, meaning that the deal should have no overall impact on Oclaro's finances in its current financial year. However, Oclaro claims that in future the deal should add more than \$6 million annually to its earnings before interest, tax, depreciation and amortization.

EUROPEAN PHOTONICS

UK begins drawing optoelectronic plan



Oclaro's InP manufacturing site in Caswell, shown here, is at the heart of the company's in-depth involvement in the UK's optical communication plan.

The UK government is investing £1 million (\$1.55 million) in a series of optoelectronic feasibility studies that it says will lead to "pan-European ultra-fast broadband".

Each of the planning projects will cost between £30,000 and £100,000, and fea-

ture significant contributions from III-V stalwarts Oclaro – formed by the merger of Avanex and Bookham – and IQE.

Mike Biddle, lead technologist at the self-described "business-led public body" the Technology Strategy Board, says that the money should identify networking issues that the UK can help solve.

"Our intention in providing this funding is to help British companies to establish future European collaborations that will participate in larger EU funding initiatives," he commented.

Of the 13 studies in the ultra-fast broadband project, which will go on for up to six months, Oclaro features in six. This includes examining how to increase the deployment of its InP tunable lasers to enable 10 Gbit/s connections at the lowest possible cost.

The San Jose, CA, headquartered optoelectronic component and subsystem manufacturer is also leading an effort looking at how 10 Gbit/s access networks will be established across Europe.

The roadmapping effort also involves leading institutions, including network operator BT, system manufacturer Ericsson and the University of Cambridge. Together the partners will find the best way to maximize opportunities for UK institutions in the next stage of the Photonics21 European technology platform.

A third Oclaro study will look at integrating arrayed waveguide gratings with the tunable lasers produced at its Caswell InP fab, which helps it qualify for UK funding. It will partner with Livingston, Scotland, based component maker Gemfire and the University of Essex in this work.

Epiwafer producer IQE is involved in two studies, and its chip manufacturing foundry partner Compound Semiconductor Technologies (CST) Global is involved with three. The two will work together on the feasibility of producing uncooled AlInGaAs laser diodes at low cost.

"We are looking to solve the paradox of producing diode sources with telecoms

grade quality, with consumer grade pricing," said IQE's project leader Wyn Meredith.

IQE and CST Global are also looking at manufacturing diode lasers with narrower linewidths and better side-mode suppression ratios than the best existing distributed feedback lasers.

Together with Glasgow University, CST Global is also evaluating the possibility of producing optoelectronic integrated circuits that monolithically integrate a resonant tunnelling diode with a laser diode. This could produce a single-chip optical-wireless interface for use in indoor base-stations such as femtocells or picocells.

● CST Global is also set to upgrade its manufacturing equipment thanks to new financing. Backed with £2.15 million from a combination of the private equity group European Digital Partners (EDP) and Scottish Enterprise's co-investment fund, the company will invest the cash in equipment such as new stepper lithography kit.

CST chief executive Neil Martin told *Compound Semiconductor* that this would enable it to make more complex devices, and offer improved quality and service to customers.

Martin added that CST had benefited from growing demand for 1310 and 1550 nm lasers in recent months, thanks to increased deployment of fiber-optic links to provide broadband communication services.

As well as the new equity to bolster its financial position, CST has restructured £1.85 million of long-term debt. The investment follows the recent award of a collaborative £1 million development contract to provide devices for next-generation local broadband access, research that will be supported by the new funding.

"We've had an incredibly successful few quarters of trading and this additional funding will enable us to expand our capabilities and enhance our service offering," Martin commented. "There is no doubt that this investment will allow us to strengthen our position of being a volume supplier of complex quality products."



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...Spire patents GaAs photovoltaic cells smaller than 5 µm

Bedford, MA, based Spire Corporation has been awarded a patent for 50 nm to 5 µm wide photovoltaic devices made from silicon or GaAs. The patent describes injecting these nanophotovoltaic devices into diseased tissue and activating them by the use of suitable radiation.

...Fujitsu develops world's first 100 W class X-band amplifier

Fujitsu Laboratories has used GaN HEMTs to develop a microwave-frequency amplifier that it says is the most efficient of its type and the first to exceed 100 W output. The Japanese researchers used two GaN transistors to make the 101 W, 53% X-band amplifier, which it says should double the potential range of

radar and satellite communications.

...II-VI sells CdZnTe detector business

II-VI Incorporated has sold its eV products X-ray and gamma-ray radiation sensor business to Endicott Interconnect Technologies of New York. The companies did not disclose the value of the deal for the Saxonburg, PA, division.

CONCENTRATING PHOTOVOLTAICS

Concentrix maintains 23% efficiency



Concentrix Solar's installation at Casquemada, near Seville in Spain. Under clear skies, the plant operates at an AC efficiency of 23% – equivalent to the record conversion first achieved last year.

Germany-based concentrated photovoltaics (CPV) pioneer Concentrix Solar says that its plant in southern Spain is now consistently delivering the record power efficiency that it first achieved a year ago.

The company's 5.4 kW demonstration system, located near Seville, reached 23% AC efficiency. Now, its much larger power plant, operated in collaboration with Abengoa Solar, is repeating that achievement on a regular basis – when skies are clear.

The 2 MW facility in Casquemada, also near Seville, features both conventional silicon modules and CPV systems, and is one of the only plants to combine the two.

However, the Concentrix systems provide only 5% of the total power, or 100 kW, at the facility. The Freiburg-based firm says that the impressive efficiency figure will increase significantly once its new generation of Flatcon modules come into use.

First-generation modules are still being used at Casquemada, each of which provides 48 W. "The new CX-75 modules have a power of 75 W and achieve an average efficiency of 27.2%," claimed Concentrix.

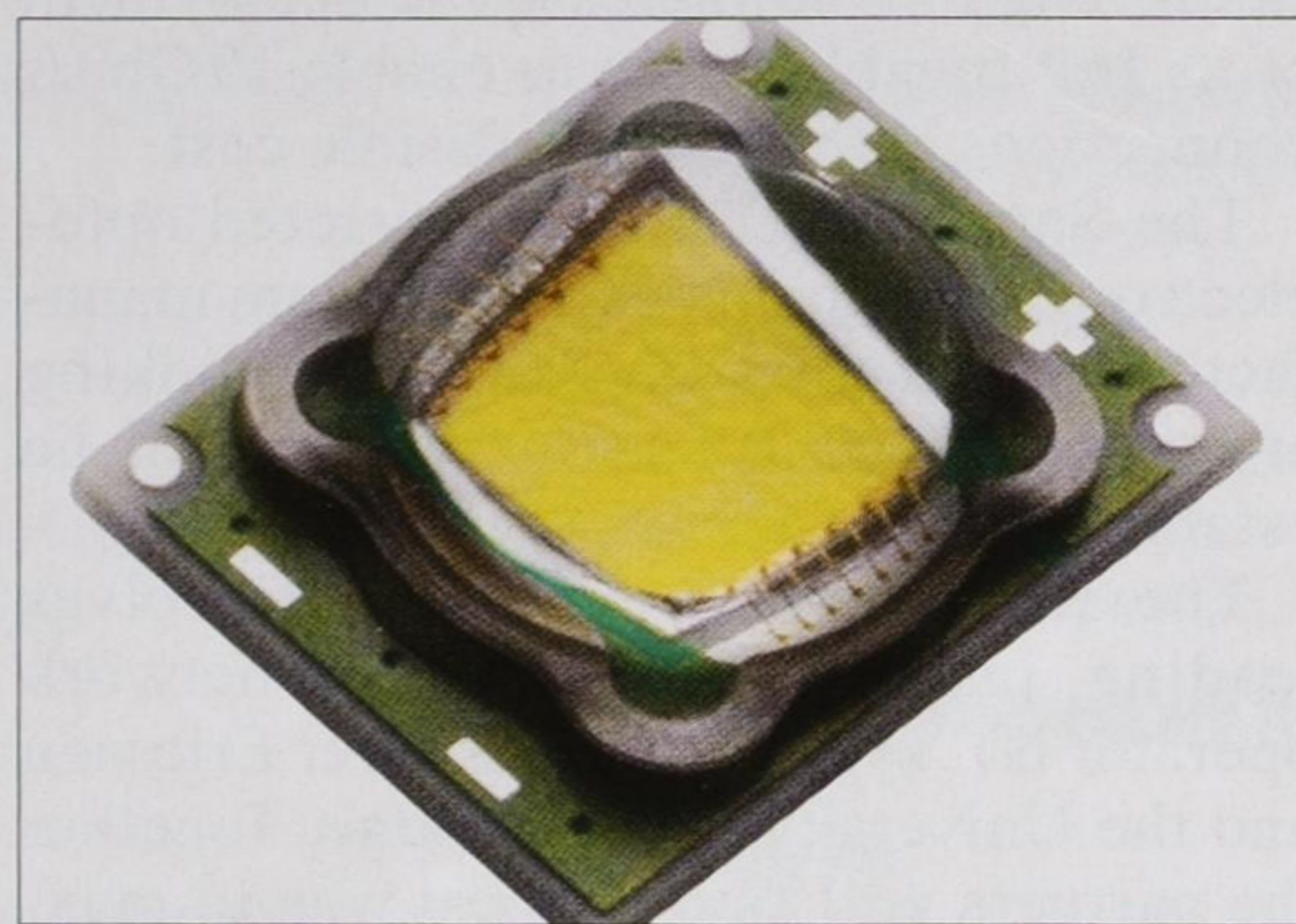
Another pioneering CPV company, US-based SolFocus, recently became the first to meet the IEC 62108 standard, with its SF-1000P modules. Such approval is seen as

a crucial part of CPV industry maturation, as the technology vies to gain a foothold in an increasingly competitive market.

"We have proved that CPV can yield nearly twice the efficiency of traditional PV systems, but meeting the IEC's rigorous CPV requirements proves that SolFocus systems can perform consistently across a variety of climates and environments," said Mark Crowley, SolFocus' CEO.

SOLID-STATE ILLUMINATION

Luminus Devices cashes in on big chips



Designed as a drop-in replacement surface-mount LED, the SST-50-W produces 550 lm at 5.5 W with the help of a 5 mm² die. It can exceed 1250 lm.

Even as Luminus Devices strives to ramp manufacturing to satisfy the surprise popularity of its initial lighting-class LEDs, it has launched two more products in the range.

The market response to the high brightnesses that the Phlatlight lamps produce from large GaN die has been overwhelming.

"The volume is actually higher than we can fulfill right now," Alexei Erchak, Luminus Devices' founder and chief technology officer, told *Compound Semiconductor*. "We are getting a response to these products that exceeds what we could have possibly imagined."

Erchak says that Luminus' capacity-build in response to this demand will be com-

plete in the third quarter of 2009. The ramp will include its epiwafer suppliers, plus chip processing and packaging at its Massachusetts facilities and overseas contract manufacturers.

The demand comes from Luminus' first two white LEDs, which it launched in February, each using a single 3 mm × 3 mm die and producing 1000 lm at 10 W. At the Light-fair show in New York in May, Luminus added the CSM-360-W LED that contains four die and can reach 60,000 lm output.

This brightness level opens the way for solid-state lighting to be used for lighting broad areas, like warehouses, gymnasiums, theaters and even rock concerts. Before this, deploying LEDs in such high-intensity lighting would have been a very complex and expensive undertaking.

Smaller die sizes are also now on the agenda, with Luminus' SST-50-W offering a 5 mm² GaN chip-area LED that can directly replace existing surface-mount LEDs.

In February, Luminus cross-licensed what Erchak calls its "big chip" Phlatlight technology with Japanese GaN pioneer Nichia. In return Luminus gained access to Nichia's patents, allowing it to produce white LEDs as well as the red-green-blue chipsets that it already produced for projection displays.

Nichia wasn't just after the photonic lattice light extraction methods that give the Phlatlights their name, Erchak says. He explains that Luminus has also dealt with thermal, electrical and reliability problems, as well as yield issues related to "big chip".

ADVANCED COMPUTING

IBM expands Euro future logic effort

Computing giant IBM has enlisted two additional European countries to support its hunt for a successor to today's dominant silicon semiconductor technology.

The Polish and Bulgarian governments have signed on to collaborate on the nano-



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...Microsemi adds 20 SiC power modules

The high-power electronics industry is set to benefit from the latest lines of 600 and 1200 V breakdown voltage products from Microsemi, which exploit SiC diodes. The Irvine, CA, chip maker is offering six current rating options for dual-diode modules and four for full-bridge power modules at each voltage.

...Semprius raises \$6.4 m for solar

Semprius, Inc, has received \$6.4 million venture funding to develop solar modules. The Durham, NC, company uses printing of "chips" with an elastomeric stamp to cut the cost of combining different materials, like GaAs on silicon. It says that this will allow low-cost assembly and electricity generation.

...U²T purchases GaAs modulator assets

German optical communications detector and receiver firm U²T has bought the assets of a UK-based GaAs business, adding to its existing InP technology. The additional material platform will allow the company to choose the best system for its 40 Gbit/s and 100 Gbit/s data rate offerings, it says.

technological research agenda established by the IBM Zurich Research Laboratory.

In late May, IBM agreed to help Bulgaria set up a nanotechnology center that will conduct applied research on "advanced virtual substrates for compound semiconductors". Although the center's research specialties will not be confirmed until it is built in one to two years time, IBM's post-silicon CMOS logic plans currently focus on one-dimensional semiconductor nanowires.

Located in Sofia and Botevgrad, the center will include 500m² of cleanroom space that will be equipped according to the needs of the projects. Lithography, deposition, etching and characterization tools will provide the basic capabilities necessary for the kind of research that will be performed.

In the same week in May, IBM agreed that its research scientists would support nanotechnology research in Poland at the Wroclaw Research Center, European Institute of Technology Plus (WRC EIT+). IBM and WRC EIT+ are now discussing several collaborative projects, while IBM will also provide training and consulting services.

IBM's Zurich operation is already acting in a pivotal role in the DUALLOGIC European III-V-silicon integration project.

FINANCIAL RESULTS

Emcore considers selling assets

Emcore is considering raising finance through an equity sale, as the company struggles with tough market conditions and the costly development of its concentrated photovoltaic (CPV) systems.

The Albuquerque fiber-optic component and solar-cell maker was in breach of its Bank of America loan covenants in the quarter ended March 31.

The bank has agreed to reset those covenants for later this year – albeit at the penalty of a higher interest rate and a reduction in the amount of credit available.

Emcore has cut its costs massively over the past few months, slashing the workforce headcount by 30% since September 2008. CEO Hong Hou and predecessor Reuben Richards have taken a 15% salary cut. But even these drastic measures have not been enough to halt a slide in cash assets.

"We continue to pursue and evaluate a number of capital-raising alternatives including debt or equity financing, joint-venture opportunities and the potential sale of certain assets," Hou told investors. "We expect to finalize a definitive agreement within this quarter."

One bright spot amid the financial gloom

is Emcore's satellite solar business. During the latest quarter, it agreed a \$70 million supply deal that will begin shipment in the current quarter. Emcore also said that it is in negotiations on a further \$50 million deal.

Since then the company has announced a contract through to 2014 with Space Systems Loral, and that it will supply approximately \$5 million of solar panels for NASA's Global Precipitation Measurement spacecraft.

While the firm's terrestrial solar business

is performing less well, Hou says that Emcore is ahead of competitors on the development of inverted metamorphic (IMM) cells, which were invented at the US National Renewable Energy Laboratory (NREL).

He believes that IMM cell efficiencies of up to 43% will be achieved before the end of this year, ultimately increasing to 45% under high concentration. NREL won a US Department of Energy prize for the transfer of this technology to Emcore in May.

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LED MANUFACTURING

Volume LED makers reach for lasers



The AccuScribe 2155 laser scribe from Electro Scientific Industries features automated loading and unloading of wafers from and to cassettes.

Diamond is not the best friend of manufacturers seeking to upgrade LED production from 2 to 4 inch diameter wafers, according to Electro Scientific Industries (ESI).

The Portland, OR, equipment vendor reckons that those using diamond-tipped scribes in conjunction with 2 inch wafers will cast them aside as they reach for higher manufacturing efficiency.

CEO Nicholas Konidaris told analysts on May 12 that his company's laser scribing systems are significantly more economical than diamond tools for larger diameters. He cites an LED manufacturer that he recently visited in Japan as saying that increased areas call for a proportionate increase in the number of – and therefore expenditure on – diamond scribes.

"At the same time, you miss the opportunity of being very perfectly aligned in your scribes, and therefore you lose area that you could have devices on," he said. Laser scribing offers more precise alignment, avoiding this waste, the company claims.

ESI partly experienced decreasing sales

in the first three months of 2009, which it blamed on low levels of LED fab utilization, but says that this is now reversing.

Since it bought laser sapphire wafer scribe company New Wave Research in 2007 for \$36 million in cash, ESI boasts that its AccuScribe 2112 system has been increasingly adopted. Offering 12 wafers per hour throughput, the system has been popular with LED manufacturers in Asia.

OPTOELECTRONICS

QPC Lasers: back from the brink

QPC Lasers, the Californian maker of high-power laser diodes, has emerged from near-bankruptcy to continue operating under new ownership.

On June 1, a limited liability corporation known as Laser Operations acquired all of the assets belonging to Quintessence Photonics Corporation, the operating subsidiary of QPC Lasers, Inc. According to its official statement, the new company will "leverage its financial stability and the deep business and managerial experience of its ownership group to support the customer base acquired from Quintessence".

It will pursue applications in the medical, industrial, defense and consumer display markets, which it sees as uniquely suited for the semiconductor laser technologies and products acquired via the deal. No details about the new owners are available yet, although a spokesman for QPC indicated that they comprise senior managers and executives from related niches within the high-technology sector.

In late 2008, bankruptcy proceedings had looked imminent for QPC after it failed to make an interest repayment to its senior creditor, fellow laser maker Finisar.

However, on May 13 the previously unknown Laser Operations emerged to acquire all of Finisar's rights under the loan

agreement, worth about \$6 million in total.

According to a filing with the Securities and Exchange Commission dated May 19, Laser Operations then arranged to conduct a public sale of QPC assets at a Los Angeles law firm – scheduled for June 1.

Following that event, at which Laser Operations made a successful bid of around \$750,000 for the remaining assets, QPC was reborn under the new ownership structure.

RF ELECTRONICS

Graphene-on-SiC FETs near DARPA targets



As part of DARPA's Carbon Electronics for RF Applications program, HRL Laboratories recently demonstrated epitaxial graphene FETs on a 2 inch wafer with a world-record graphene FET mobility.

HRL Laboratories has claimed a leap forward in radio-frequency graphene transistors just days after describing the first such devices in *IEEE Electron Device Letters*.

The Malibu, CA, research institution said that it had made devices from single-layer graphene on 2 inch diameter SiC wafers with much-improved performance figures.

"They have world-record field mobility of approximately 6000 cm²/Vs, which is six to eight times higher than current state-of-the-art silicon n-MOSFETs," said HRL senior scientist Jeong-Sun Moon.

The researcher also described the ratio of on-state current to off-state leakage current, I_{on}/I_{off} , of 19 for the devices as "excel-



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...Cyrium boasts solar market lead

Multijunction solar-cell maker Cyrium Technologies has claimed that its products, which exploit a quantum-dot layer in the epitaxial structure, exceed the performance of all commercial competitor cells. The Ottawa, Canada, company is now supplying its 40% minimum efficiency cells to qualified customers for evaluation, and says that it will

reach 45% in two years.

...HVPE kit finally goes commercial

UK-headquartered Oxford Instruments has officially begun sales of CrystalFlex, its multiwafer hydride vapor phase epitaxy (HVPE) reactor. The company says that HVPE should provide cost-effective production of high-quality GaN, AlGaIn and AlN single-crystal

materials, and is targeting LED manufacturing.

...Obducat prepares for LED growth

Swedish equipment manufacturer Obducat has officially launched the Sindre 400, its high-volume nanoimprint lithography tool for LED manufacturing. The firm has also launched a SEK74 million (\$9.5 million) share offering to support its expansion into this industry.

lent". In comparison, the first graphene RF field-effect transistors that HRL worked on achieved just $200 \text{ cm}^2/\text{Vs}$ field mobility and $I_{\text{on}}/I_{\text{off}}$ of 3–4.

Details of these pioneering $2 \mu\text{m}$ gate-length devices, produced under the US Carbon Electronics for RF Applications program (CERA) were revealed online shortly prior to its latest claims. Originally announced in December 2008, the current-gain cut-off frequency, f_T , for the first transistors was 4.4 GHz.

This DARPA-funded CERA work, performed by HRL and the US Naval Research Laboratory, seeks to exploit graphene for communications, imaging and radar.

For the original devices, the team produced the graphene by evaporating silicon from 6H crystal polytype SiC at around 1600°C and less than 10^{-4} mbar. They used an Aixtron VP508 CVD reactor "because it has excellent temperature uniformity".

As a result, the surface of the 2 inch diameter wafer was covered in the single sheet of hexagonally arranged carbon atoms that constitutes graphene. However, a second graphene layer was also present on top of this across much of the wafer.

The transistors were made using a standard photoresist process and oxygen reactive ion etching. Source and drain contacts were fabricated from an unalloyed combination of titanium, platinum and gold.

Now that some initial limitations have been overcome, Jeong-Sun Moon is confident that the technology can go on and meet the CERA phase I goal of delivering Hall mobility above $10,000 \text{ cm}^2/\text{Vs}$. "The results and rate of progress validate our technical approach," he said.

INDUSTRY EXPANSION

Foxconn patents nanoparticle doping

Electronics manufacturer Foxconn is challenging established LED chip companies and their methods with two US patent applications that exploit nanoparticle dopants to improve performance.

Hon Hai Precision Industry Co, which trades under the name Foxconn and makes products for Nokia, Apple and Dell, filed two applications on May 28. Judged by some to be the largest electronics producer in the world, Foxconn has claimed LEDs that use hydrogenated SiC as their substrates.

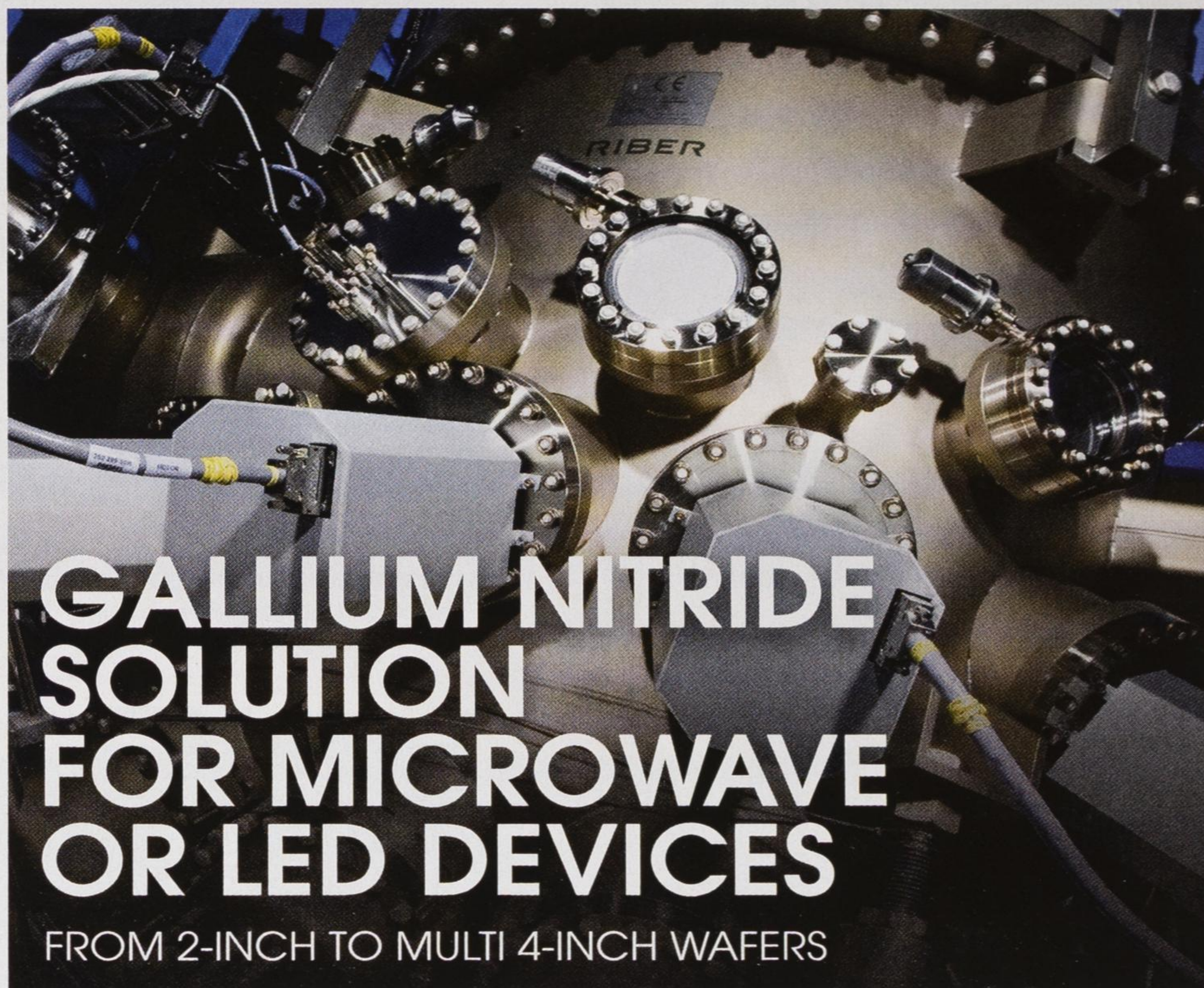
The Taiwan-headquartered company has patented LEDs that can use either InGaN or AlGaAs as their active, single or multiquantum-well layers in application numbers 20090134406 and 20090134380.

In an otherwise typical LED epitaxial structure, the confinement layers either side of the active layers exploit nanoparticles 20–200 nm in diameter as dopants.

Nanoparticles can be made from SiN, SiO, GaO, AlN or BN, and help to improve the crystal quality of the die, writes listed inventor Ga-Lane Chen. Chen is chief technology officer and vice-president of global R&D at Hon Hai Precision Industry. "The nanoparticles can change the lattice con-

stant [of] the n-type and p-type confinement layers and decrease the lattice strain thereof," Chen said.

By reducing the strain, fewer dislocations form when the active layer is deposited on the n-type confinement layer and when the p-type layer is deposited on the active layer. "The decrease of lattice strain weakens the stress generated between the active layer and the confinement layers, and the quantum efficiency is improved," stated the patent.



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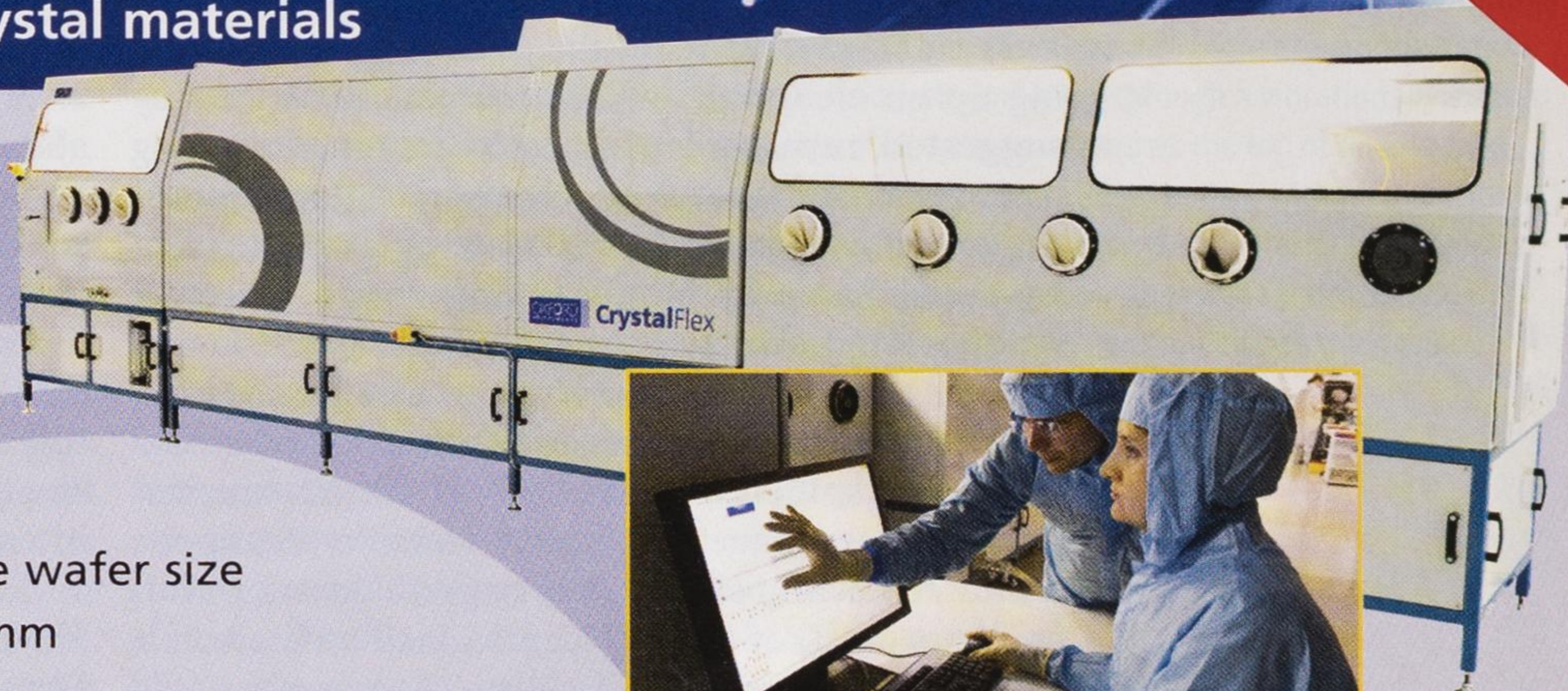
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Single-molecule transistors: lo

As microchips inexorably decrease in size and enter the quantum regime, can single molecules ever replace silicon-based components? **Douglas Natelson** reports.

The first transistor, made more than 60 years ago at Bell Labs, was a couple of inches across. Today, a typical laptop computer uses a processor chip that contains well over a billion transistors, each one with electrodes separated by less than 50 nm of silicon. This continual drive for miniaturization, with the density of transistors doubling roughly every two years, was first noted by Intel co-founder Gordon Moore in 1965, and has been such a mainstay of electronics development that it is now enshrined as “Moore’s law”. These billions of transistors are made by “top down” methods that involve depositing thin layers of materials, patterning nanoscale stencils and effectively carving away the unwanted bits. The end result is billions of individual components on a single chip.

Miniaturization cannot go on forever. We are beginning to run into the problem that the silicon, copper wiring and oxide insulating layers in these devices are all made out of atoms, each about 0.3 nm across. Moreover, when we try to think about how electrons act in small numbers of atoms, we know that we have to worry about orbitals and chemical bonds – quantum mechanics rules at these scales.

In 1974 Ari Aviram and Mark Ratner from the IBM Thomas J Watson Research Center in New York saw the writing on the wall. Rather than giving up on electronics at the molecular scale, they suggested turning lemons into lemonade: using molecules themselves as electronic components. In particular, they suggested making a simple electronic device, a rectifier, by designing a molecule with one end that likes to give up an electron and another end that likes to accept an electron. If individual molecules were able to replace bulk electrical components, then manufacturing and miniaturization might continue all the way down to the atomic scale. After all, chemists can produce enormous numbers (10^{23}) of exactly identical nanometer-scale molecules at a time in a beaker. If each one could take the place of a transistor, that would be enough components for 50 trillion processors.

However, early optimism about single-molecule devices as replacements for semiconductor nanoelectronics has been tempered by an appreciation of the enormous challenges that need to be overcome. For example, having 10^{23} components is not useful if they all have to be positioned with atomic precision to work correctly. We also need to have a good



understanding of how such devices would behave. Remember, the enormous success of silicon electronics has been built on decades of physics, chemistry, materials science and electrical-engineering knowledge. Finally, because individual molecules are so small, it can be incredibly challenging to “see” what is going on in single-molecule devices.

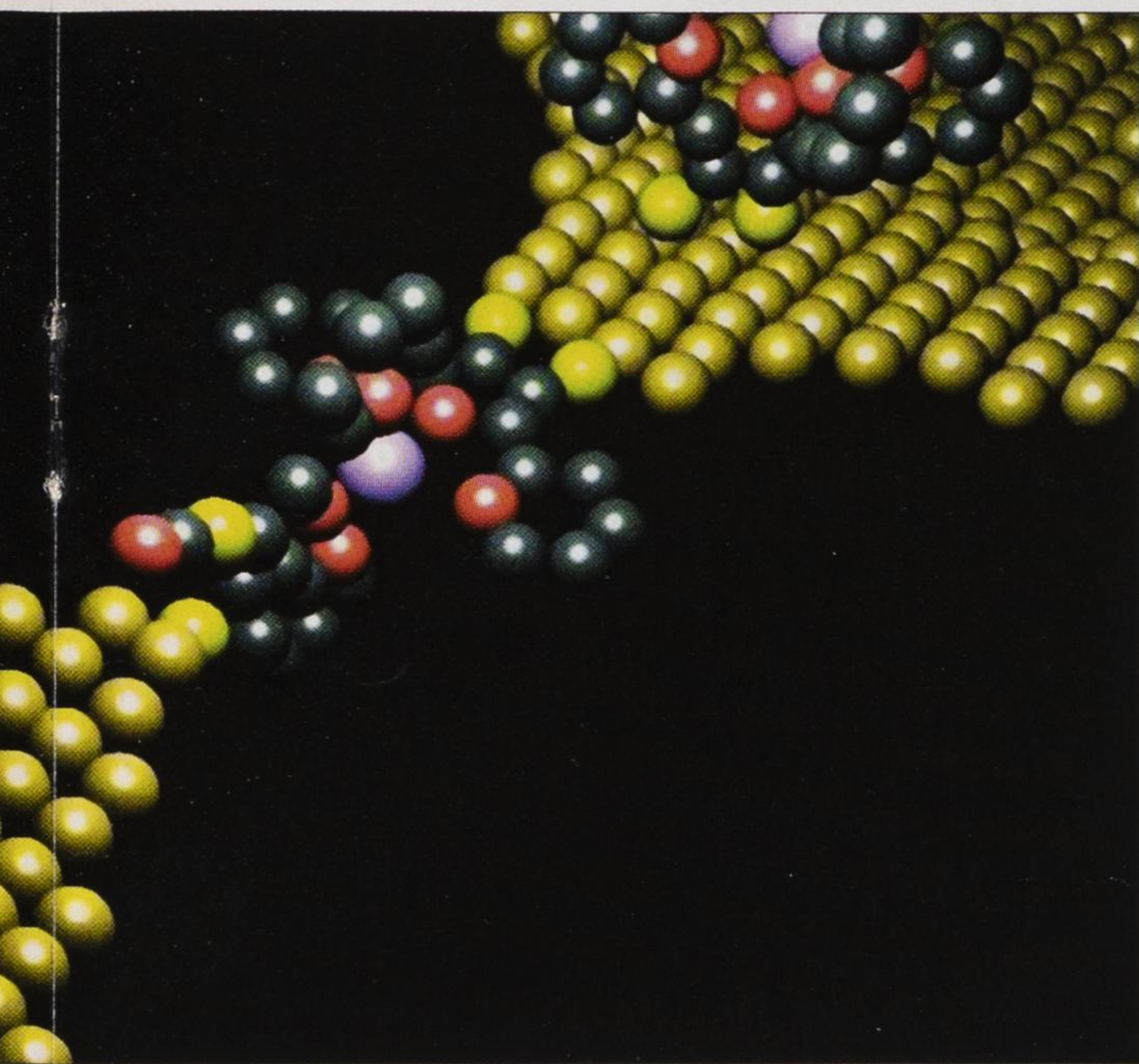
Recent experimental successes, however, have led to a growing appreciation that single-molecule electronic devices can teach us an enormous amount about the physics and physical chemistry that will be relevant in electronics on the single-nanometer scale. As the portfolio of experimental techniques grows beyond simple DC electronic measurements of current as a function of voltage, we are getting a much better sense of the physics relevant at these tiny scales, such as the microscopic origins of dissipation and the importance of electron–electron interactions at the nanoscale.

Moving charge through a molecule

Before we try to do anything too exotic, it is important to understand the basic physics of electronic conduction through molecules. The vast majority of single-molecule electronic measurements so far have focused on precisely this – making sure that we can make single-molecule devices and understanding how electrons move through them. Measuring simple electronic conduction is relatively straightforward: apply a voltage across some device of interest and measure the flow of current at some

J.W. CISZEK

logical successors to silicon?

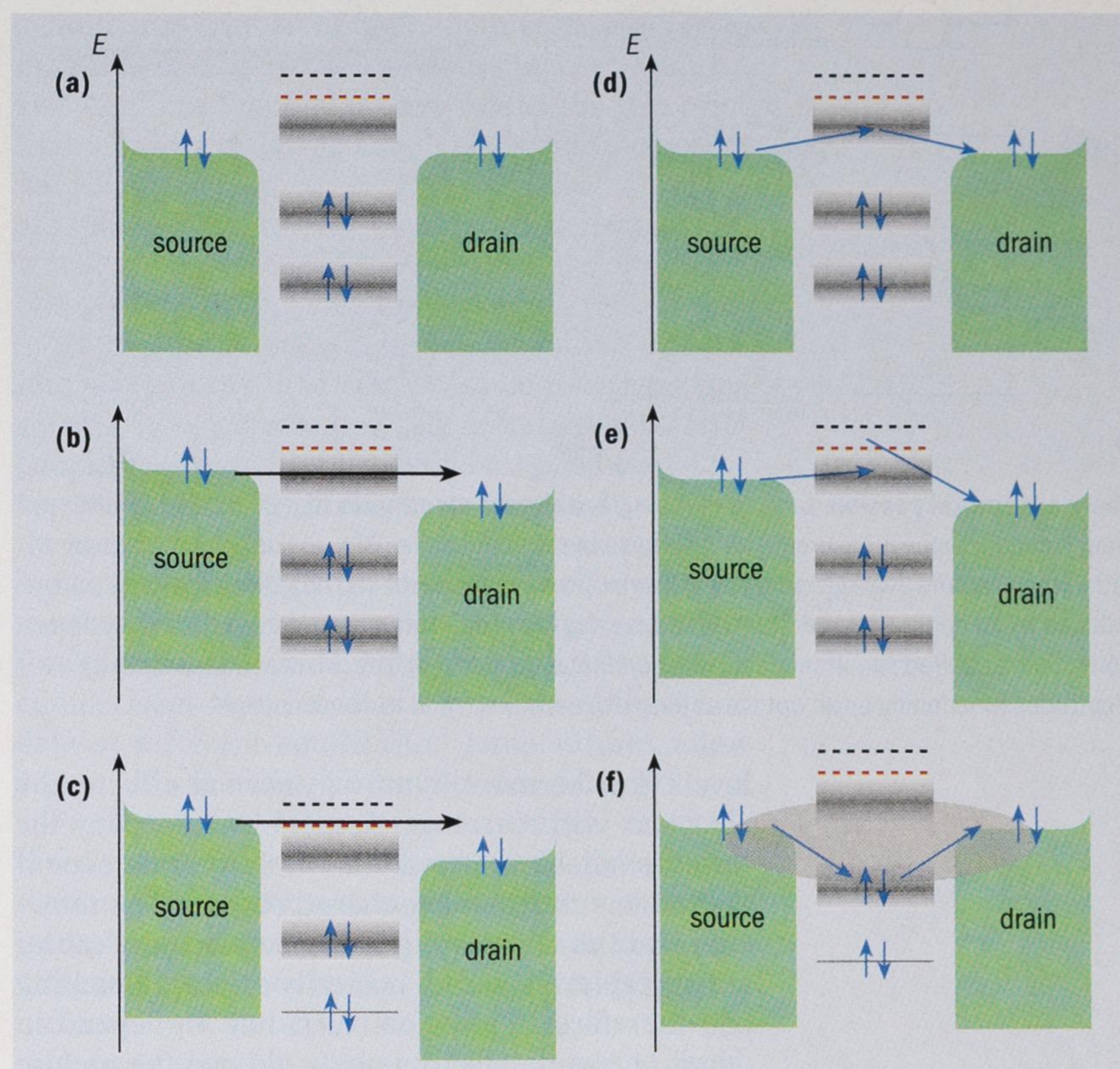


temperature. The form of the current as a function of these two parameters (temperature and voltage) can reveal much about the physics at work.

The tricky bit is that small molecules exist on the single-nanometer scale, and electron motion at these distances is very different to that in macroscopic wires. The quantum nature of the electrons needs to be taken into account. Think about an electron approaching a barrier. Classically, an electron with too little energy to overcome the barrier would be reflected 100% of the time. Quantum mechanically, however, the electron can “tunnel” through the barrier with a probability that depends exponentially on the barrier height and geometry. A related way to think about this is that quantum-mechanical uncertainty allows “virtual” states that violate classical energy conservation as long as the violation is sufficiently brief. Tunnelling and virtual states are part and parcel of charge motion on the molecular scale.

To understand the electronic states involved in conduction, consider two metal electrodes separated by an individual molecule. In isolation, the molecule has a discrete spectrum of states called molecular orbitals. Because the electrons on the molecule are jammed into such a small region, confinement and the electron–electron repulsion cause these states to differ in energy by quite a bit. For example, the differences in the molecular energy levels in dye molecules correspond to the energy of photons of visible light.

On the other hand, in the metal electrodes, we

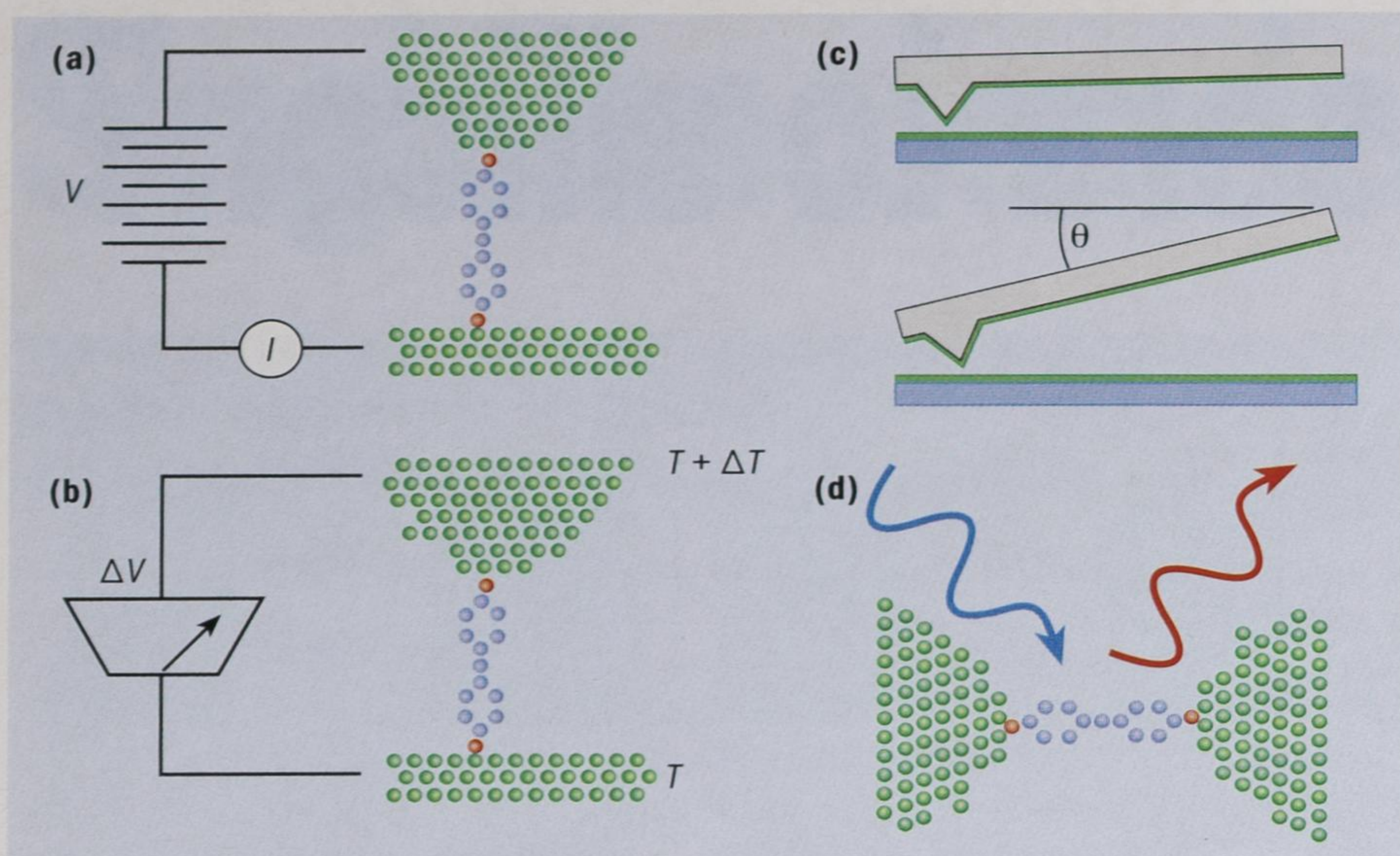


This figure shows the energy levels when a molecule is placed between source and drain electrodes.

(a) The electrodes have so many levels so close together that their states look continuous. The molecular levels are discrete and broadened because of coupling to the source and drain. (b) Electrons need a path to get from source to drain. In resonant tunnelling, the voltage aligns a molecular level with the chemical potential of one electrode and there are empty states available on the other side. (c) You can also get resonant tunnelling through a vibrationally excited molecular level. (d) In off-resonant conduction, a molecular level acts as the top of an effective barrier for tunnelling. (e) An electron can even leave behind vibrational energy without ever “really” occupying the molecule. This is one way that energy can transfer from the electrons to vibrations. (f) Kondo conduction is when an unpaired electron on the molecule does a magnetic dance with the source and drain electrodes, flipping its spin and shuttling an electron across the device.

can usually think of the electrons as wavelike, and because the electrodes are comparatively big, there are many wavelike states, with very minor energy differences between them, so their states look continuous. The Pauli principle means that we can think of each state as only holding two electrons, each with opposite spin. The energy of the highest occupied state is called the chemical potential. As the temperature is increased, electrons can be kicked into higher energy states by thermal fluctuations.

Attaching the molecule to one or both of the metal electrodes changes the situation. Just as atomic orbitals can be coupled to form molecular orbitals, the molecular states couple to the wavelike states in the metal, thus smearing out the molecular energy



There are several possible ways to test single-molecule electronics that do not just involve simple conductance measurements. **(a)** Noise measurements: looking at current fluctuations rather than just the average current. **(b)** Thermopower measurements: observing a voltage induced by an applied temperature difference. **(c)** Force measurements: inferred from cantilever deflection, acquired simultaneously with conductance data. **(d)** Optical measurements: with electrodes functioning as an optical antenna to focus down and transmit out light.

levels. Furthermore, ignoring thermal effects, the electrons will rearrange themselves to occupy the lowest available states of the whole system, even if that means transferring charge between the molecule and the metal. Alignment between molecular and metal levels, which critically affects tunnelling and therefore conduction, turns out to depend in detail on the metals, the molecule and the precise molecule-metal binding.

Now consider applying a voltage between the source and drain electrodes. What happens? The system is driven out of equilibrium, with the source and drain having different chemical potentials, and electrons can start flowing across the device. How they do this depends on where the molecular levels sit.

If the voltage aligns a molecular level with the chemical potential of one electrode and there are empty states available on the other side, electrons can move from source to drain by resonant tunnelling. Under the best of circumstances, this conduction process via a single resonant state results in a conductance of $2e^2/h$, where e is the charge on the electron and h is Planck's constant. Known as the quantum of conductance, it is about $13\text{ k}\Omega$ when translated into a resistance. Such perfect transmission is commonly observed when electrodes are connected by a chain of metal atoms. Molecular conductances are typically orders of magnitude lower, although recent observations by Jan van Ruitenbeek and co-workers at Leiden University in the Netherlands show that high conductances are possible with certain simple molecules such as H_2 .

Even without a molecular level available for the direct flow of electrons, some current can still flow, thanks to quantum tunnelling through virtual states.

From the point of view of an electron at the highest occupied state in one of the electrodes, the situation looks like tunnelling through an effective barrier that is set by the energies of the molecular orbitals.

Finally, the spin of the electron also has profound effects on electrical conduction. Suppose that there is an unpaired electron localized on the molecule. An electron of opposite spin could pair up with the localized electron, but electron-electron repulsion forbids this classically. Still, such a paired state can be a virtual state in a higher-order magnetic dance that flips the localized spin and transfers an electron across the device. This is called the Kondo effect and it can lead to the perfect transmission of electrons in devices even without level alignment.

All sorts of subtleties crop up once the system is driven out of equilibrium. The electrons that do make it through the device are "hot" – out of thermal equilibrium with the electrodes. Such electrons can also dump energy into other degrees of freedom, like molecular vibrations or molecular bonds. These inelastic processes have been of huge interest to physicists in recent years. Identifying particular molecular vibrations through their effect on the conductance can confirm that current really is flowing through the molecule of interest. Furthermore, how energy flows through the electrons and vibrational modes is related both to fundamental questions of irreversibility and to practical concerns about power dissipation in nanodevices.

Measuring single-molecule electrical properties requires getting a single molecule between two electrodes. This can be a real challenge because everything tends to move on the atomic scale (particularly near room temperature), including the molecules and the atomic surfaces of the electrodes.

One common approach is the mechanical break-junction technique. Two pieces of metal (either a metal tip and a flat surface, or two ends of a broken metal wire) are brought in and out of contact, with molecules (on the surfaces or in surrounding solution) occasionally getting between the electrodes. By measuring the conductance throughout the breaking process, histograms of conductance can be compiled. If certain junction configurations are favored by chemistry and atomic bonding, and therefore show up often in the experiment, there will be peaks in the histograms at particular values of conductance. Break junctions were originally developed by van Ruitenbeek and collaborators in the early 1990s to examine atomic-scale metal junctions, and were first applied to study molecules by Mark Reed of Yale University and collaborators in 1997. Recent work, particularly that of NJ Tao's group at Arizona State University, Latha Venkataraman's group at Columbia University and Christian Schönenberger's group at Basel University, has shown that peaks at low conductances can be identified with off-resonant conduction through individual molecules.

Another form of measurement comes from building the single-molecule analogy to transistors. A

gate electrode is employed to shift the molecular levels relative to the source and drain. This is difficult in break junctions, but it is possible if a molecular junction can be made flat on a chip. The most common method of doing this, which was originally developed by Hongkun Park and Paul McEuen in the late 1990s at the University of California, Berkeley (UCB), starts with a pre-formed metal strip and uses a high-density current to push metal atoms around until the strip breaks into electrodes separated by a nanoscale gap. This is called electromigration and it can be used to make source and drain electrodes that are separated at the single-nanometer scale.

As the probability of an electron tunnelling across the gap depends so strongly on distance, the conductance of such a junction is dominated by a volume comparable to that of a single molecule, centered on the point where the electrodes are closest. If the metal is initially coated in a layer of molecules of interest, a molecule may end up within this critical volume after electromigration. Empirically, this seems to work about 10–30% of the time, depending on the details of the process and the molecules.

A gate electrode lying under the junction has some coupling to the tunnelling region, and under ideal circumstances can shift the molecular levels enough to allow changes in the molecular charge state (oxidation and reduction, in the chemist's lingo). Huge challenges in these experiments include the lack of direct microscopy to confirm the presence of a particular molecule in the junction, and the microscopic variation in configuration from device to device. Great care and many control experiments are needed to draw useful conclusions from such single-molecule transistors (SMTs). Recently Dan Ralph's group at Cornell University has been able to create a gated mechanical break junction, combining the electronic tunability of an SMT with the geometric engineering possible in mechanical junctions.

The main advantages of SMTs are their geometric stability, allowing temperature- and magnetic-field dependent measurements with comparative ease, and the ability to change molecular charge states. SMT transport experiments have demonstrated vibrational effects, and have been used extensively to examine Kondo physics in a variety of molecules with both normal and ferromagnetic electrodes.

Beyond current and voltage

Current as a function of voltage can only tell us so much about what is taking place in a single-molecule junction. Recently there has been a great deal of interest in moving beyond "simple" conductance, to tease more information from these nanoscale systems.

For example, rather than just measuring the current, you can measure noise – the fluctuations in the current. Noise in equilibrium is determined by the thermal fluctuations of the electrons and provides a means of assessing temperature. When charge is pushed through the molecule, additional "shot noise" results from the fact that charge is not continuous but

comes in "lumps" of individual electrons. The noise can reveal if interactions lead to the electrons moving in a correlated way. Such measurements have been reported by van Ruitenbeek's group in individual D_2 molecules using a break junction, and predictions exist for pronounced noise signatures of electron–vibrational coupling in molecular junctions.

Similarly, instead of applying a voltage across a molecule, the UCB groups led by Rachel Segalman and Arunava Majumdar have forced the two electrodes to have differing temperatures and monitored the voltage that appears across the molecule. These are pioneering measurements of thermopower, which can provide information about the alignment of the molecule and electrode energy levels.

There is great interest in understanding dissipation and heating in single-molecule junctions, and some way of determining the effective local temperature of the molecule would be a good start. One approach taken by Tao's group is to look at either the mechanical force required to break a single-molecule junction or the distance such a junction may be stretched, as a function of voltage (and therefore current). While the interpretation can be subtle, comparisons between data at various voltages and data at different equilibrium temperatures allow you to infer an effective junction temperature.

Finally, optical measurements of single-molecule junctions may provide another route to similar information. We recently demonstrated that the electrodes in electromigrated junctions are extremely effective optical antennas. The electrodes capture incident light and effectively focus it down to the molecular junction, and similarly allow the molecule to radiate efficiently. This is perfect for doing Raman spectroscopy on individual molecules.

The ultimate limit

Despite some birth pangs, the field of single-molecule electronic devices is alive and well. New efforts are being made to incorporate electronic correlations, spin effects and excited states into theoretical treatments. At the same time, combining conduction with other, complementary, techniques is giving us more tools to examine these tiny structures.

Single-molecule electronic devices are unlikely to replace semiconductor technologies soon. However, single-molecule devices are outstanding tools for examining basic physics issues relevant to any sufficiently nanosized electronic device. It is critical that we develop an understanding of the flow of energy, the mechanisms of dissipation and the engineering of surfaces at the molecular scale. Single-molecule devices are a fascinating laboratory system with which to explore these issues. While silicon is likely to continue dominating nanoelectronics technologies for a long time, these molecular experiments are shedding light on the limits of electronic devices. ●

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About the author

Douglas Natelson (natelson@rice.edu) is an associate professor of physics at Rice University, TX, US.

UCSB blames Auger for droop

The debate over the origin of LED droop rages on, with recent simulations contradicting earlier calculations and claiming that direct Auger recombination is the primary cause. **Richard Stevenson** investigates.

The pertinent question regarding the cause of droop – the decline in GaN LED efficiency at high currents – is this: Auger or not Auger? And if it is Auger, then the obvious follow-up question is what is the exact form of this non-radiative recombination process that limits the output power of high-brightness LEDs.

In the fall of 2007, when Philips Lumileds claimed that Auger is the cause of LED droop, this chip maker failed to elaborate on the finer details. But last summer a partnership between theorists at the universities of Arizona and Marburg claimed that droop was not caused by direct Auger recombination, the interaction between an electron, a hole and a third carrier. Instead they postulated that either defect-assisted Auger recombination or phonon-assisted Auger recombination might be the cause.

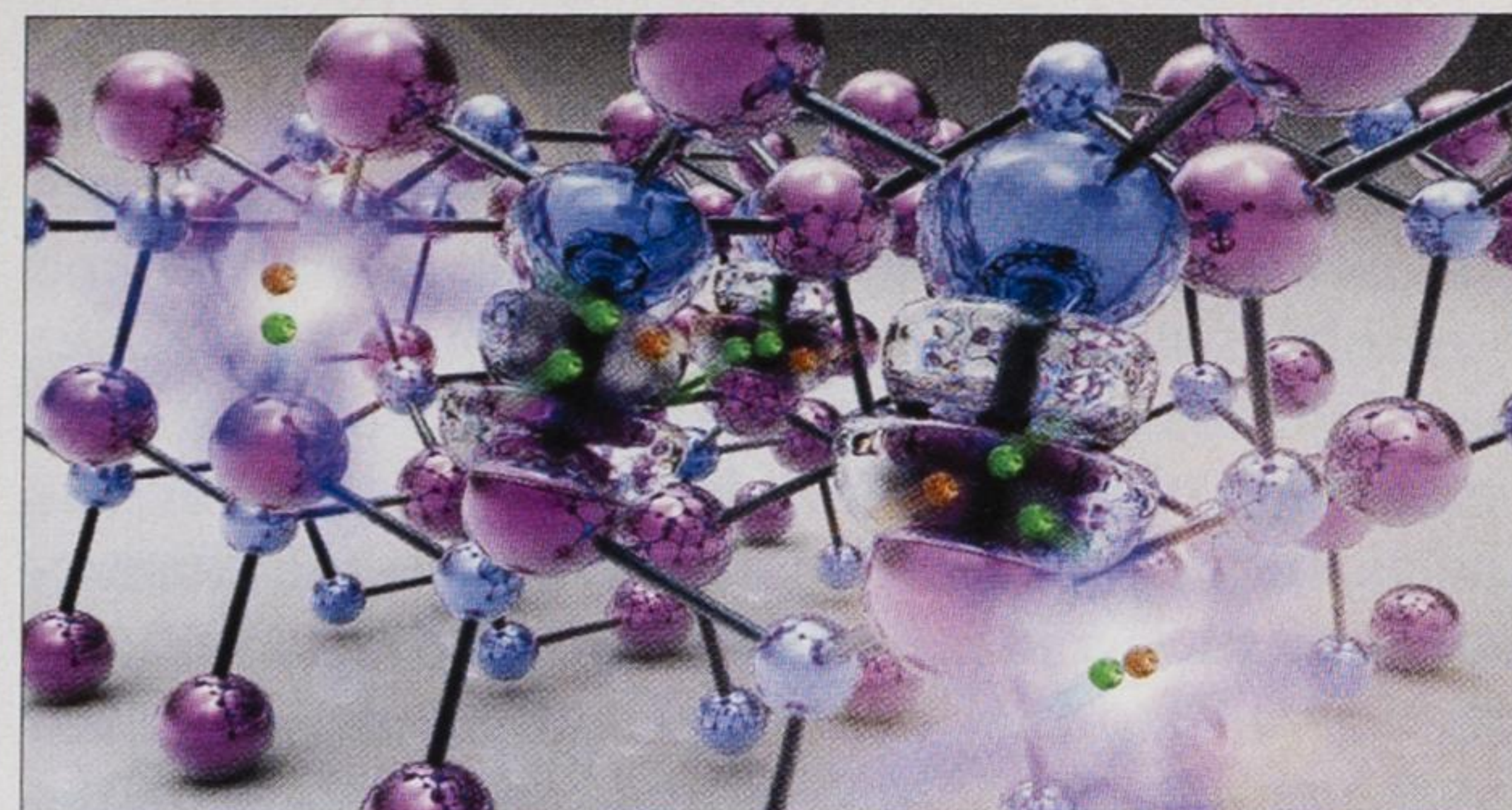
Another group has now entered the debate. Computational scientists at the University of California, Santa Barbara (UCSB), believe that droop is caused by a form of direct Auger recombination – interband Auger recombination (figure 1). Its simulations can even explain the origin of the “green gap”, the decline in GaInN LED efficiency as the wavelength is stretched from the blue to the green.

The discrepancy between the results of the academic teams stems from differences in the modelling of the nitride band structure – the UCSB researchers identified and included a second conduction band. “When we identified this second conduction band we were thrilled,” said team member Patrick Rinke. “Then it was just a matter of working through the theory and putting the calculations of the Auger recombination rate on a rigorous footing.”

The UCSB team has not quantified LED loss due to Auger, because this would also require calculations of the radiative recombination rate and possibly other non-radiative recombination rates. “However, we think that it is significant that our Auger coefficient agrees well with that measured by Philips Lumileds,” said UCSB’s Chris Van de Walle.

One of the limitations of these simulations is that they are based on bulk structures rather than quantum wells, which are the emitting layers in LEDs. “Full first-principle calculations for realistic device structures are beyond the capabilities of current computers,” admitted Van de Walle, “but we are looking into other types of modelling.”

Arizona–Marburg team member Joerg Hader is supportive of the UCSB effort, and says that he has no reason to doubt their results. His team did not consider the transitions to higher conduction bands because the experimental results that they are aware of claim that the separation between the lowest and higher conduction bands in GaN is about 3.5 eV. “This



Several different recombination processes take place in an InGaN crystal. In the normal light-emitting process an electron (green) and a hole (orange) recombine radiatively (bright areas). In the Auger process, an electron can collide with a hole in the vicinity of another electron and transfer energy to the second electron, with no light emitted (dark areas). The likelihood for such an Auger recombination event is greatest in regions where the two-electron probability density is high, which is schematically depicted by the isosurfaces.

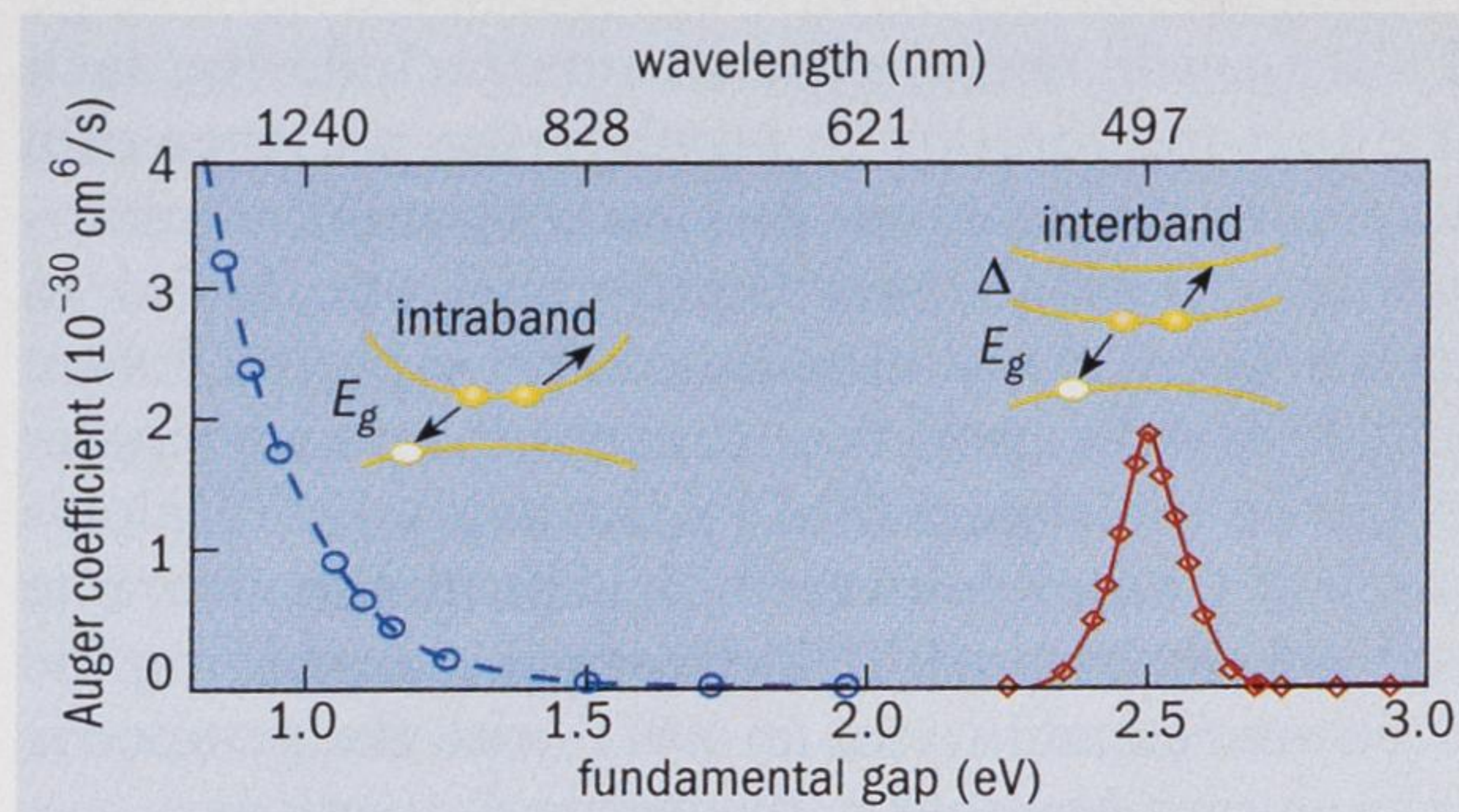


Fig. 1. First-principle calculations by UCSB, which include a second conduction band, reveal the peak in interband Auger recombination in InGaN with a fundamental bandgap at 2.5 eV.

means that for our structure, the higher conduction band cannot be reached by Auger transitions.”

Hader believes that there is an approach that can determine whether interband Auger transitions are the cause of droop. This involves the growth of an AlGaIn/InGaIn structure with AlGaIn barriers that are tuned to prevent these transitions. “If the droop disappears, it would be a strong indication that their assumption is correct,” he said. Getting to the bottom of the cause of droop would be beneficial in several ways – it would allow closure on this debate and it would also enable the design of LED architectures that are efficient at high current densities. ●

Further reading

K T Delaney *et al.* 2009 *Appl. Phys. Lett.* **94** 191109.

J Hader *et al.* 2008 *Appl. Phys. Lett.* **92** 261103.

Trenches turbocharge silicon

AmberWave Systems has a novel technique for creating high-quality films of germanium and III-Vs on silicon – aspect ratio trapping. This involves epitaxial growth into trenches in a SiO₂ layer and promises faster computer processors, say **James Fiorenza**, **Mark Carroll** and **Anthony Lochtefeld**.

CMOS engineers dream of exploiting the properties of superior materials in their silicon devices. Semiconductors that pique their interest include III-Vs such as InAs and InSb, which have far higher electron mobilities than silicon, and germanium, a material with faster holes. If InAs and germanium were used for the n- and p-channels of a CMOS device, then it is theoretically possible to cut power consumption by an order of magnitude, without any sacrifice in chip speed.

Such an advance would have a tremendous, widespread impact. Benefits include dramatic increases in the lifetime of portable devices and massive energy savings at server farms.

The potential pay-offs have not gone unnoticed and they continue to inspire major research efforts to develop III-V and germanium devices for CMOS applications. Industry heavyweights IBM, IMEC, Intel and TSMC have all dedicated substantial programs towards this goal, as have many universities. But even the expertise of all of these researchers is yet to surmount the significant technical barriers that are preventing the commercial realization of III-V and germanium CMOS.

The biggest obstacle is also the most basic: how can III-V and germanium materials be united with silicon without any detriment to their high mobilities? This question is the most pertinent, because it is hard to envisage a CMOS industry based on anything other than silicon. Billions of dollars have been invested in developing sophisticated technologies to process silicon wafers, and any switch to another material would be prohibitively expensive.

The ultimate CMOS solution that complies with this restriction involves integrating the optimum materials for electron and hole transport in the channels of the NMOSFET and PMOSFET, respectively (figure 1). However, realizing this dream is very challenging, and today alternative channel devices are nothing more than a laboratory curiosity.

But recent advances in the field of heteroepitaxy – the epitaxial growth of one crystalline material on another – indicate that the problem is not insurmountable. Improvements have been made for several decades, and at AmberWave, Salem, NH, we have recently pioneered a heteroepitaxy breakthrough. We have developed a technology called aspect ratio

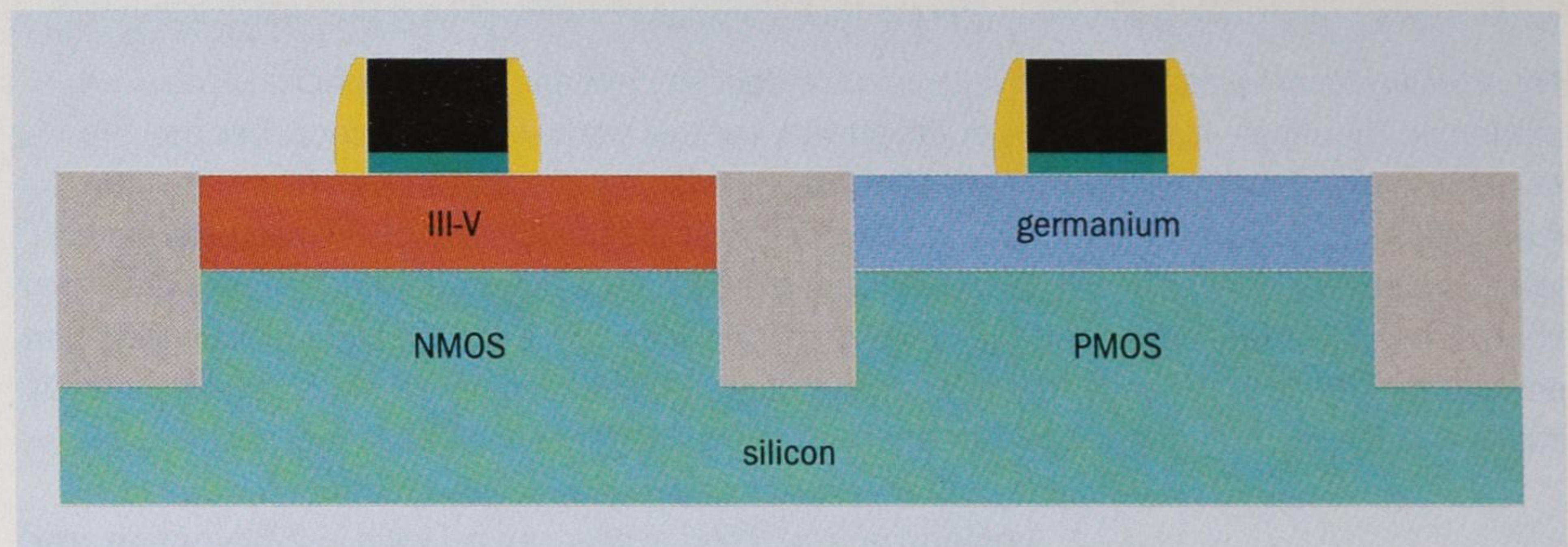


Fig. 1. The ultimate CMOS architecture will employ the best material for carrier transport in each channel. A III-V is preferred for the n-channel and germanium for the p-channel.

trapping (ART) that promises to allow the fabrication of the transistor structures that can lead to the realization of germanium and III-V CMOS.

Efforts directed at the heteroepitaxy of germanium and III-Vs with silicon date back to the early 1980s, and the intervening years have witnessed the development of many different techniques to try and unite these semiconductors. On every occasion the focus has been directed at the fundamental problem associated with the transition between two crystals: a large lattice mismatch that creates a high density of atomic dislocations in the epitaxial layers. The variations in lattice constant are between 4 and 8%, and this gives rise to a threading dislocation density in directly grown epilayers of typically 10^9 cm^{-2} .

These defects hamper device performance. They scatter carriers, reducing their mobility; they trap carriers and shorten their lifetime; and they act as diffusion pipes, which increase the leakage current in the device. If the transistor is to deliver a reasonable performance, the dislocation density must be no more than 10^6 cm^{-2} , and any manufacturable technology could require far fewer defects than this.

Optimizing direct epitaxial growth on silicon is the most obvious approach to cutting the dislocation density. This method of forming germanium, GaAs and InP layers on silicon has been extensively studied by independent research teams, using MBE and MOCVD deposition technologies. These efforts have produced significant reductions in the threading dislocations caused by lattice mismatch, but the residual dislocation density is still about 10^8 cm^{-2} .

In the early 1990s Eugene Fitzgerald and

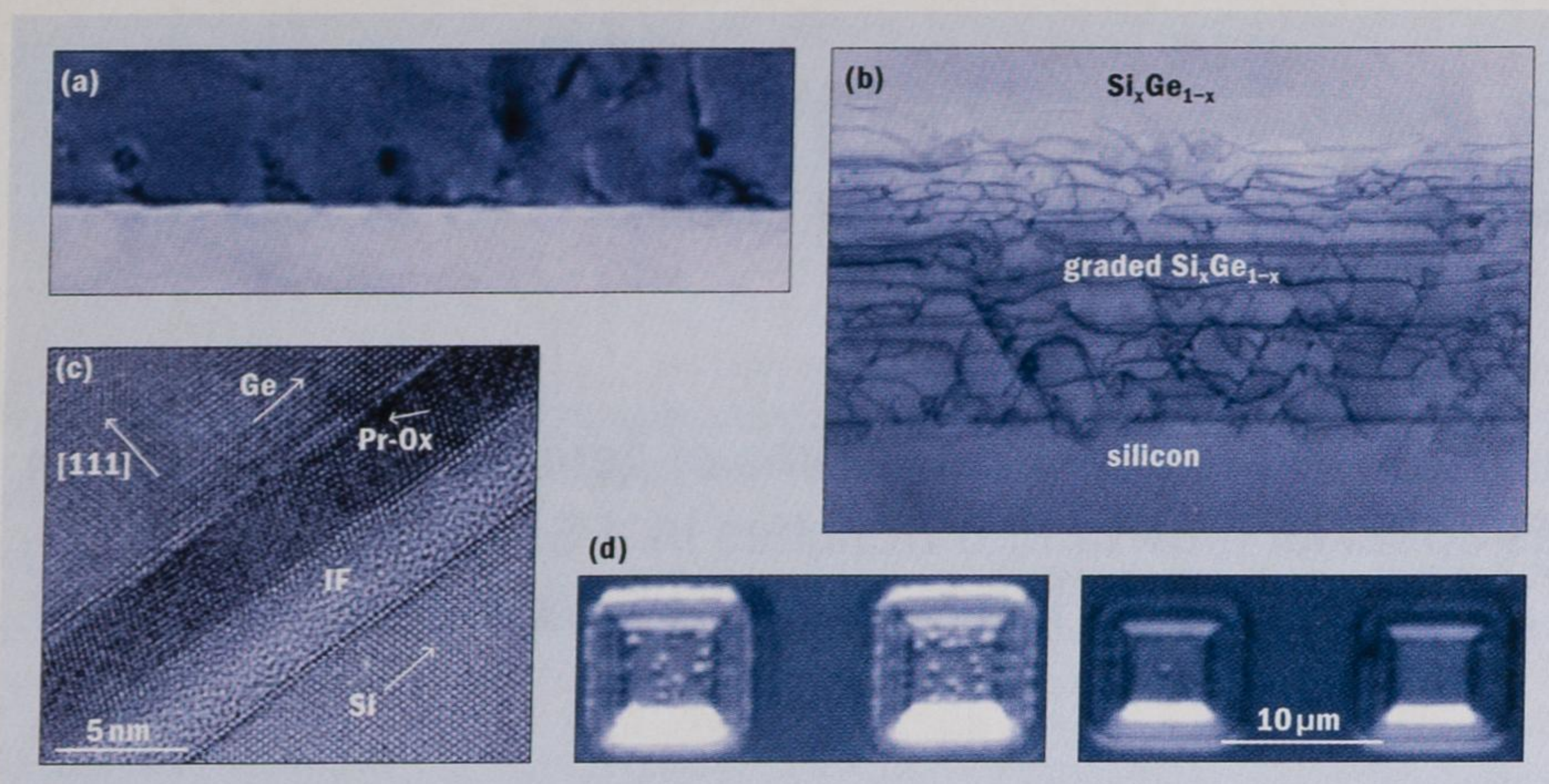


Fig. 2. Many techniques have been developed to deposit III-Vs and germanium on silicon platforms. The simplest approach is direct growth, but this leads to many dislocations that are revealed in cross-sectional transmission electron microscopy images (a). A graded buffer can reduce this dislocation density (b). Efforts are underway to reduce the thickness of the buffer layer and recently the use of a Pr_2O_3 layer has produced some success (c). Another recent approach involves the formation of micron-size mesas, which are subjected to a cyclic anneal that drives dislocations to the edges of these structures (d). The left and right plan views show an SEM image of germanium square-shaped structures in silicon, before and after anneal, respectively.

colleagues at Bell Labs, and Bernie Meyerson and co-workers at IBM, independently explored an approach that tackles these residual dislocations. By turning to a compositional graded buffer, these researchers could gradually increase the lattice constant during epilayer growth and slash the dislocation density in the top of the epitaxial film by a factor of 10^4 (figure 2b). These teams had to use a miscible material system to produce intermediate lattice constants between silicon and the desired epitaxial lattice constant. The $\text{Si}_x\text{Ge}_{1-x}$ system has proved to be convenient for this purpose.

The downside of the graded buffer is its thickness and many types of thinner buffer have been explored. A recent example of this line of enquiry comes from researchers at IHP (Innovations for High Performance Microelectronics) in Frankfurt Oder, Germany (figure 2c). They have shown that thinner buffers are possible by turning to crystalline dielectrics.

Another approach to reducing the residual dislocation density in mismatched epitaxial materials involves epitaxial growth in a confined area, followed by cyclical annealing (figure 2d). This technique, which was pioneered by Lionel Kimmerling's group at MIT, uses the stress introduced by cyclic annealing to drive dislocations in the mismatched epitaxial film to the edges of the epitaxial area.

Although all of these techniques have enjoyed some success, none can approach the ideal solution depicted in figure 1, p21. The graded buffer, which is $10\mu\text{m}$ thick for germanium growth on silicon, is far too thick for CMOS processing, and this ultimately restricts integration to a single material. Thinner buffers, however, have dislocation densities that are too high, while the effectiveness of cyclic annealing is insufficient because some types of dislocation do not move in response to stress and the thermal

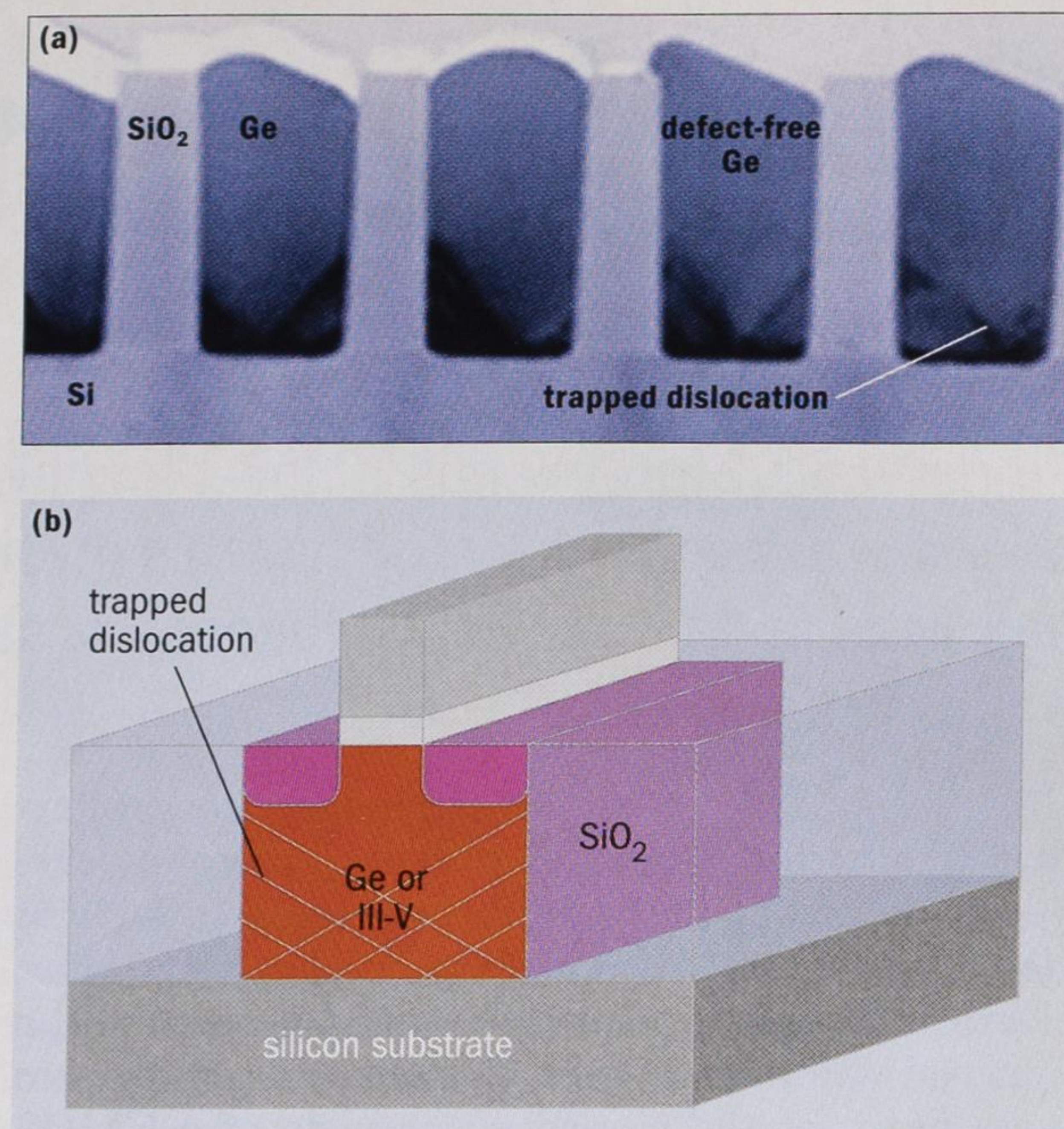


Fig. 3. AmberWave's aspect ratio trapping confines mismatch dislocations to trenches in SiO_2 (a). This enables the optimum channel material to be grown on silicon, followed by the fabrication of the FET on this high-quality epitaxial film.

cycling is too hot for CMOS processes. Put simply, it is not easy to grow low-dislocation III-Vs and germanium on silicon suitable for CMOS.

Aspect ratio trapping

One approach that appears to marry germanium and the III-Vs with silicon successfully, however, is our heterointegration technique, ART. This involves the growth of a mismatched layer on a silicon substrate that contains an additional dielectric layer, which is patterned with high-aspect-ratio holes or trenches. The side walls of the holes in this dielectric trap dislocations originating at the silicon/epitaxy interface and enable the growth of very-low-dislocation-density epitaxial material at the top of the trenches.

Our ART technique comes very close to delivering the ultimate CMOS device. One of its strengths is the very thin trapping layer, which is 100 times thinner than the graded buffer. This can be realized with 100nm wide trenches, leading to the fabrication of structures that are compatible with CMOS processing. And thanks to the flexibility of the technique, different materials such as germanium, GaAs and InP can be selectively integrated on different portions of the wafer.

Dislocation trapping in high-aspect-ratio openings was first demonstrated in 2000 by Fitzgerald's group at MIT. Efforts were led by Thomas Langdo, with collaborators including Anthony Lochtefeld, a co-author of this article, who was a student of MIT professor Dimitri Antoniadis. The key result was the extremely effective defect trapping in high-aspect-ratio 100nm wide holes in SiO_2 , for germanium grown on silicon via ultra-high vacuum CVD.

AmberWave's long-term research program on ART

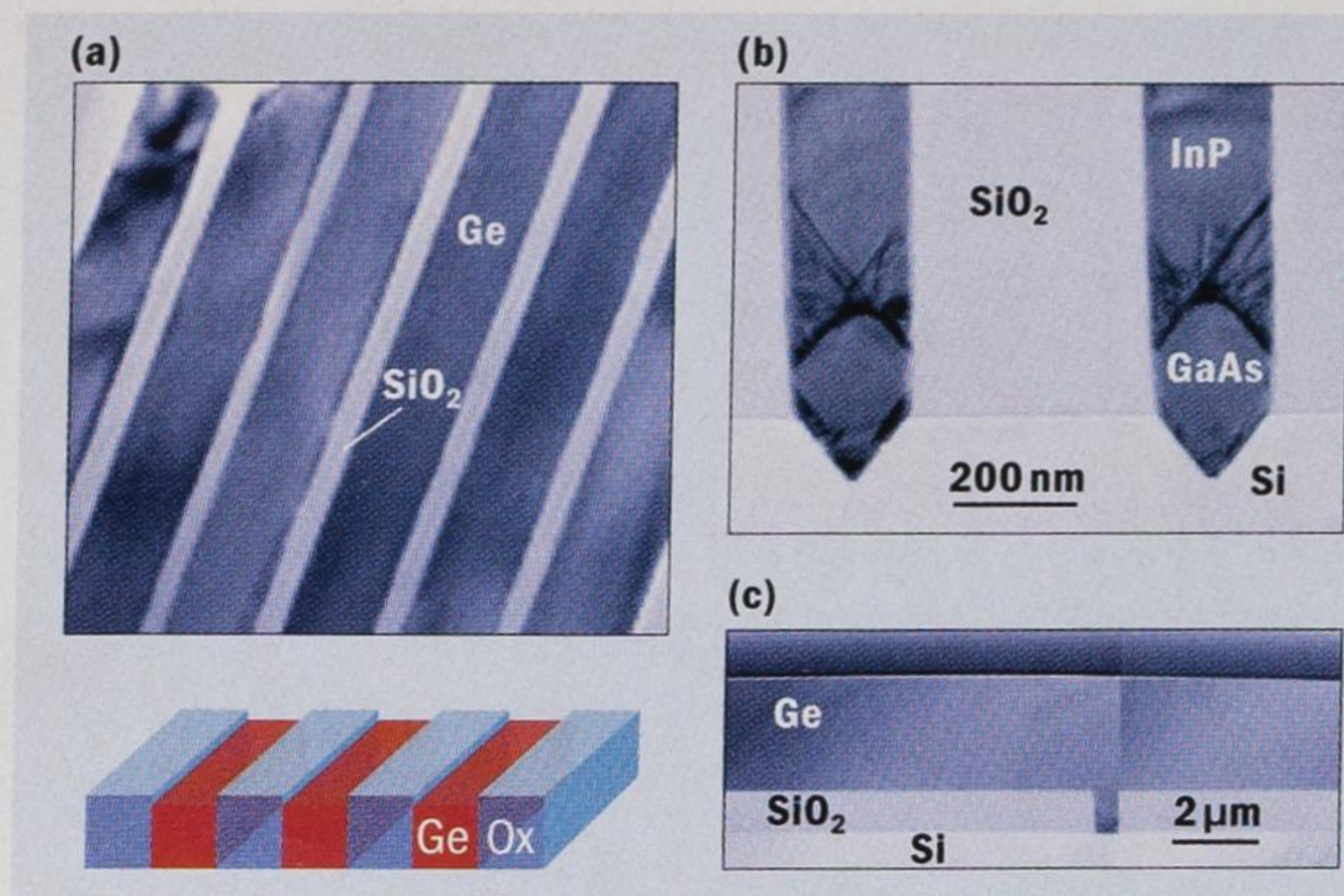


Fig. 4. AmberWave's development of ART started with efforts to perfect the growth of germanium films in trenches formed in a SiO_2 layer (a). ART can also be used to grow III-Vs on silicon. This includes InP, which can be produced using GaAs as a seed layer (b). Further work showed that continued germanium growth out of the trenches, followed by chemical mechanical polishing, creates an epitaxial, low-dislocation-density film that is compatible with CMOS device layout.

kicked off in 2005. Several significant breakthroughs followed, which have helped ART to become a realistic option to enable alternative channel CMOS.

Our initial advances involved germanium growth in the narrow trenches of 500 nm thick SiO_2 films using an ASM Epsilon reduced-pressure CVD reactor. In work led by Ji-Soo Park, we demonstrated that ART is capable of working in trenches of arbitrary length (figure 4a) as well as it had in holes.

Subsequently, in a project headed by Jie Bai, a former AmberWave engineer who is now at Intel, it was shown that dislocations in films with a high lattice mismatch are preferentially orientated perpendicular to the surface of the epitaxial growth. By choosing conditions favoring steep facet formation in a trench early in the growth, it is possible to produce extremely effective dislocation trapping. The facets guide the dislocations to the dielectric sidewalls.

Our next significant advance was the growth of a variety of key materials, including GaAs and InP, by MOCVD (figure 4b). Jizhong Li and co-workers showed that dislocation trapping may universally apply to materials with a cubic lattice structure, such as the binary materials InAs and InSb, and ternaries such as InGaAs and HgCdTe.

More recently we have shown that the dislocation density can remain at a low level when germanium is grown up and out of the trenches. By combining ART with epitaxial layer overgrowth and chemical mechanical polishing, we have gone on to produce 20 μm wide stripes of low-dislocation-density germanium on silicon (figure 4c). Layout restrictions imposed by the trench geometry are thwarted, making ART applicable to virtually any device geometry used in a CMOS layout.

This sequence of milestones in the heteroepitaxy of semiconductor materials onto silicon has been followed by an advance in CMOS. In partnership with Peide Ye's group at Purdue, we have produced a

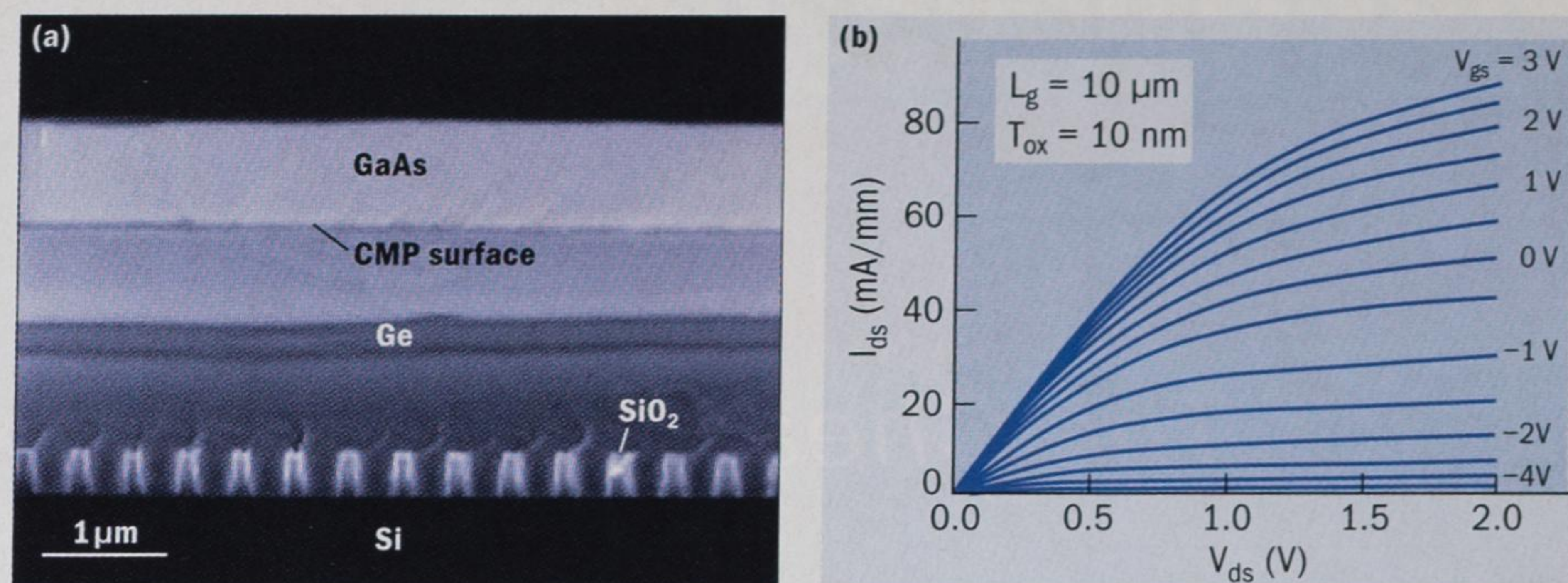


Fig. 5. AmberWave has teamed up with Peide Ye's group at Purdue University to produce the first III-V MOSFET on silicon. The ART technology used is visible in the scanning electron micrograph (a).

GaAs MOSFET on silicon using ART (figure 5).

Device fabrication began with reduced-pressure CVD deposition of germanium, which grew up and out of the trenches to coalesce into a contiguous film. Chemical mechanical polishing planarized this film, before GaAs was deposited by MOCVD. A high-k dielectric was added by atomic layer deposition and then a GaAs MOSFET was created on the planar ART films.

Although these devices are primitive from a scaling perspective – they have a gate length of 10 μm , more than 100 times that of state-of-the-art CMOS – fundamental device results are incredibly encouraging. Electron mobility in these transistors is $503 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, a value higher than that seen in silicon devices and matching that produced by GaAs devices grown on native substrates.

What's more, the advantages of ART are not restricted to MOSFETs – they have the potential to deliver improvements in many other electronic and optoelectronic devices. In the past year we have used ART to produce GaAs resonant tunnelling diodes, which are being investigated for post-CMOS logic and memory applications, in partnership with Sean Rommel's group at RIT. In collaboration with Sarnoff Laboratories we have recently produced GaAs lasers on silicon that will aid the quest for highly integrated photonic circuits, as well as board-to-board and chip-to-chip optical interconnects. Solar cells could also benefit from ART, which has the potential to create multijunction cells on a low-cost silicon platform. In short, ART could transform many types of heterogeneous device.

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About the authors

James Fiorenza (left) is a director of research at AmberWave. He joined AmberWave in 2002 and has directed the aspect ratio trapping research since 2008. **Mark Carroll** (center), director of operations at AmberWave, joined the company in 2000. He is responsible for all facilities, cleanroom and epitaxial growth operations. **Anthony Lochtefeld** (right), AmberWave's CTO, joined the company in 2001. Since 2005 he has led the development of practical solutions for epitaxy of high-quality germanium and compound semiconductor layers on silicon substrates, with applications in CMOS devices, optoelectronic integration and photovoltaics. The authors gratefully acknowledge the contributions of Jie Bai, Zhiyuan Cheng, Jennifer Hydrick, Jason Li, Jizhong Li, Ji-Soo Park and the entire AmberWave operations team.

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Submerged electrodes boost high-brightness LED output

When metal electrodes are placed on the top of an LED, they reduce its emission area and increase internal absorption. But both of these problems can be completely eradicated with a buried n-type contact, say Osram Opto Semiconductors' **Berthold Hahn**, **Karl Engl** and **Markus Klein**.

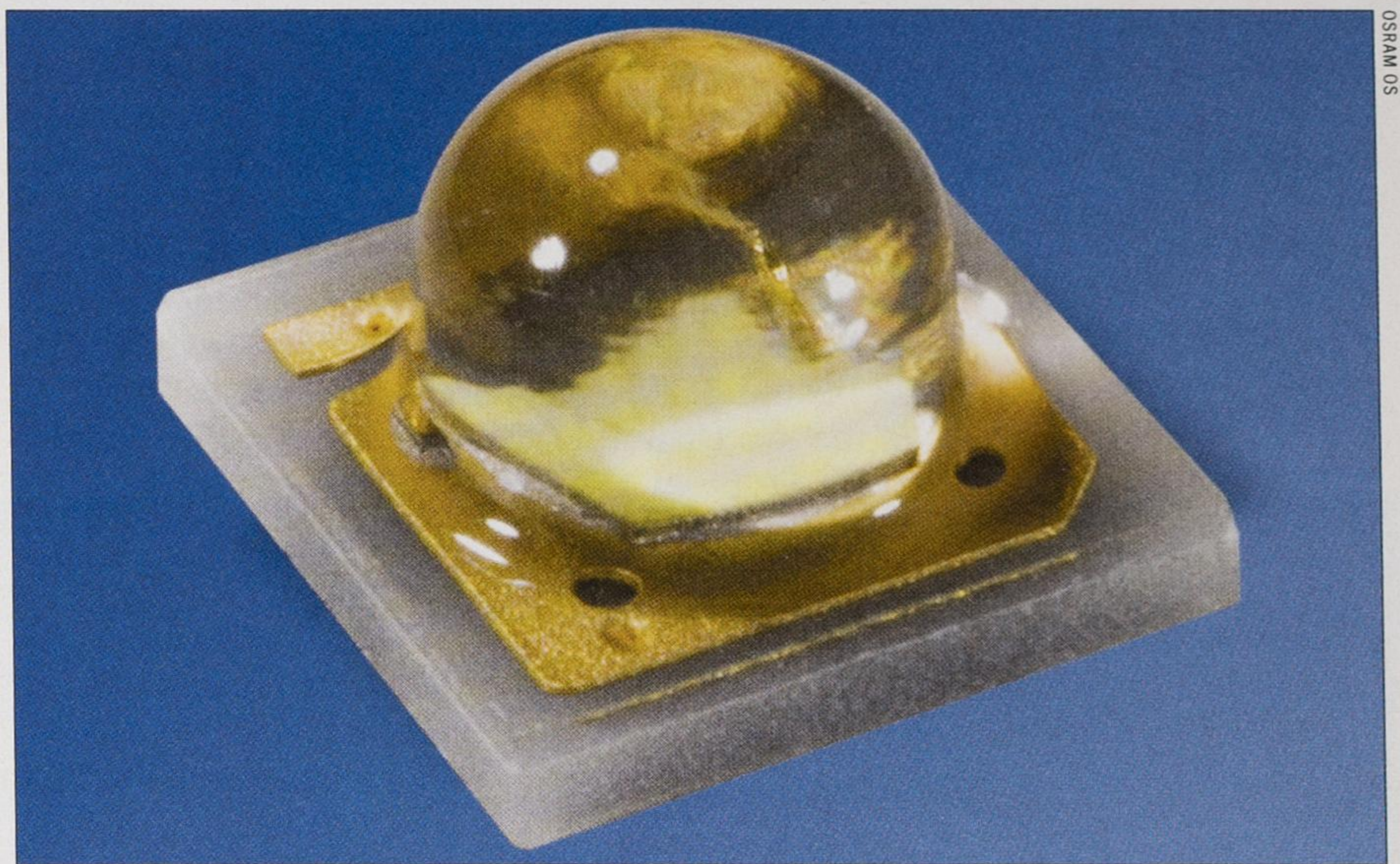
One way to judge an LED's performance is to measure its efficiency at a particular drive current. High efficiencies are relatively easy to realize at low current densities, but efficiency tends to decline as the current is cranked up. However, high efficiencies at high currents hold the key to cutting the electricity bill for lighting, and ultimately spurring the deployment of this light source in more applications.

The pocket projector is one application that is emerging as a beneficiary of higher-performance LEDs. If this product is to project high-brightness images, then LEDs must deliver outstanding luminance at a high drive current and a high efficiency from a small form factor design operating within a limited power budget.

Another opportunity for LEDs is automotive headlights, which require die that operate at high current densities and deliver a scalable light output. Last, but by no means least, is the lucrative general lighting market. This demands new, low-cost device structures with very high efficacy, excellent scalability and exceptional stability over many years of operation. At Osram Opto Semiconductors we have developed an innovative LED design that fulfills all of these goals. At the heart of this groundbreaking chip is a new approach to electrode design.

Our latest LED draws on our ThinGaN technology, employing a soldering method to add a reflecting metallic film prior to removal of the sapphire substrate by a laser lift-off technique. This process, which we introduced in 2003, is superior to conventional flip-chip technologies that attach LEDs upside down on a pre-mounted board. This unites entire epiwafers to carrier wafers. By carefully selecting the solder, it is possible to introduce a highly reflective layer between it and the epitaxial film.

ThinGaN technology produces LEDs with highly reflective mirrors and well defined scattering surfaces (figure 1). Waveguiding and absorption are potential problems in this type of structure, but they are mitigated by introducing some degree of surface roughness. In principle, all of the light could be coupled out of the chip if there is no internal absorption



Osram's Oslon LED was unveiled in May and measures just 3 × 3 mm. This high-brightness LED package produces a well defined emission profile and delivers up to 130 lm at 350 mA in cool white.

because every photon has numerous chances to find an escape cone. However, in practice out-coupling of 75–80% is realized, due to internal absorption.

These LEDs have a proven set of attributes that empowers them to serve backlighting, solid-state lighting and automotive applications. However, there is still room for improvement because the metallic n-contact grid that distributes the current on this side of the device hinders the total light extraction. The reduction in light output stems from absorption by the metal film and a reduction in the active emitting area.

Improving the design of the metallic contact is not easy though. Increasing the separation of the metallic line contacts that form the grid diminishes absorption in the LED, but also leads to inferior current spreading. Low current spreading is a major problem in high-power chips due to the low lateral conductivity in the n-type GaN layer, which is less than 5 µm thick. The other obvious option for reducing light absorption is to decrease the width of the

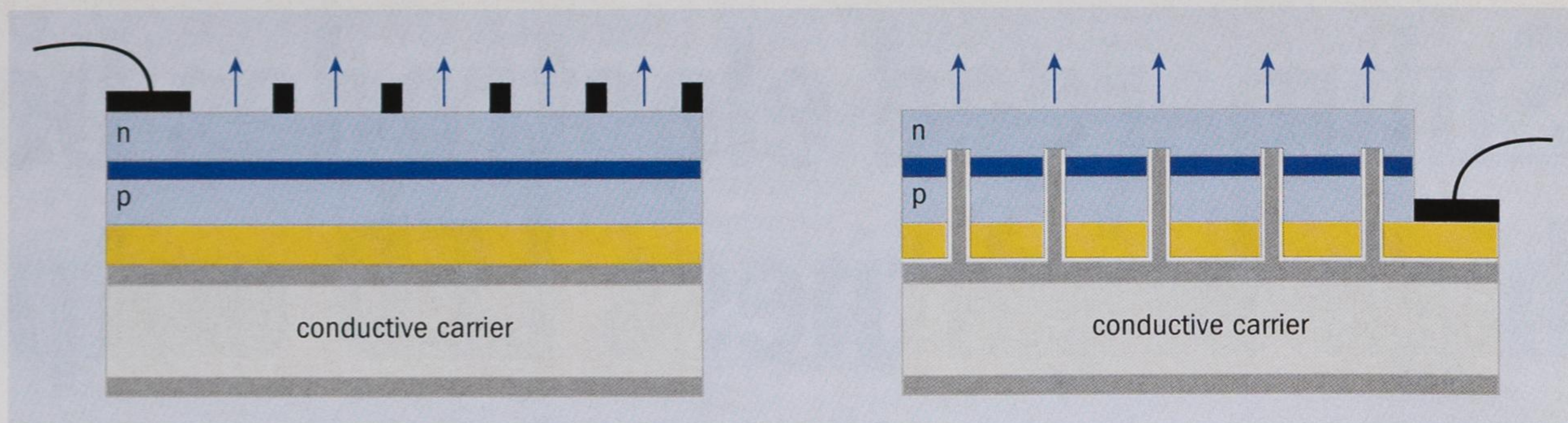


Fig. 1. Osram's first generation of ThinGaN LED chips featured a metallic grid on the top of the device that reduced its active area and increased light absorption. The latest design combats these weaknesses by burying the n-type electrode in the epistructure.

metallic lines that form the grid, but this again pays the penalty of inferior current spreading.

A far better approach is to completely eliminate the metallic grid contact from the top of the chip and bury it under the p-contact. This is the option that we have selected and it exploits a novel reflecting n-contact. This is created by forming a grid of vias that penetrate through the p-type material and into the n-type layers.

We use a highly reflective, silver-based layer for the p-contact, which is ideal for injecting electrons into the device. The p-contact is then covered with an insulating layer that prevents electrical shorting of the two electrodes through the reflecting layer.

This type of LED is manufactured by growing the epistructure on sapphire, bonding the wafer to a carrier and then removing the original substrate by laser lift-off. By carefully designing and controlling the mechanical carrier and the interconnect it is possible to build a mechanically stable device that features homogenous heat spreading. These attributes have enabled our LEDs to pass reliability assessments set by the automotive industry, including temperature cycling and stress tests at elevated temperatures and high humidity levels.

Our latest generation of LED chips combines increased wall-plug efficiency with a higher quantum efficiency that stems from reduced light absorption by the n-contact. This improvement, which is greater at high current densities, results from a better epitaxial structure that reduces the serial resistance. Thanks to lower ohmic losses, our 1×1 mm devices can operate at drive currents of up to 3 A.

Combating droop

Any LED that is driven hard suffers from droop – a reduction in LED efficiency as the current is cranked up. The origin of droop is controversial, but our research efforts have led us to conclude that it is caused by a form of Auger recombination – a non-radiative process that involves three or more carriers, including at least one electron and one hole.

It's not possible to eliminate Auger recombination in LEDs – electrons and holes have to be brought together so that the device can emit light. But the extent of Auger recombination can be diminished significantly by increasing the volume of the active

region, because this form of non-radiative recombination is proportional to the cube of the carrier density. We have adopted this approach and minimized the current density in a multiquantum-well device.

Our new design is paying dividends. 1×1 mm chips emitting at 440 nm have a peak external quantum efficiency and a wall-plug efficiency of 68% (figure 2). An output of 640 mW is produced at 350 mA, rising to 3.2 W at 3 A. White-emitting chips are fabricated by adding a phosphor. These deliver a peak efficacy of 136 lm/W and a maximum output of 830 lm at 3 A.

The emission pattern from these LEDs is independent of drive current, even at high densities, which makes this design ideal for deployment in automotive headlamp systems, and projection and illumination applications. Because this light source is a genuine surface emitter, the technology is not only fully scalable, it is also capable of forming homogeneously emitting, high-luminance multichip arrays.

We have also produced green LEDs that emit at 523 nm and deliver a peak efficacy of more than 200 lm/W. This source, which is a promising candidate for forming high-performance projection systems based on red, green and blue sources, produces 117 lm (100 lm/W) at 350 mA and 224 lm at 1 A.

To aid and simplify customer transition to our latest generation of LED chip technology (UX:3), we produced a design with dimensions and primary optical characteristics that are compatible with our first generation of ThinGaN devices. Upgrading existing products is then possible without changes to the optical design parameters of the secondary optics.

Compatible LED packages are used to fully exploit the strengths of our latest chips. This type of housing enables a high degree of linearity between the light output and the drive current, and offers the opportunity to produce sophisticated optical designs. A good thermal package is incorporated in this product, which employs stable materials to ensure a long lifetime for the chip. Other features include a small footprint, a versatile optical interface and decoupling of the electrical and thermal paths, which means that changes to chip polarity do not affect the customer's PCB layout.

An example of this type of package was unveiled in May – the Oscon SSL. Thanks to the strong over-



About the authors

Berthold Hahn (left) heads LED chip development at Osram OS. He joined the company after completing his doctorate at Regensburg University in 1998, and has led several epi and product development projects relating to InGaN high-power LEDs.

Karl Engl (center) is responsible for engineering high-power InGaN-based LED chips. **Markus Klein** (right) heads the business segment solid-state lighting at Osram OS. He has a doctorate from the Technical University of Karlsruhe, Germany, and more than 15 years of R&D experience in the electronics industry. The authors are grateful for the financial support by the German Federal Ministry of Education and Research BMBF, under contract No. 13N9400.

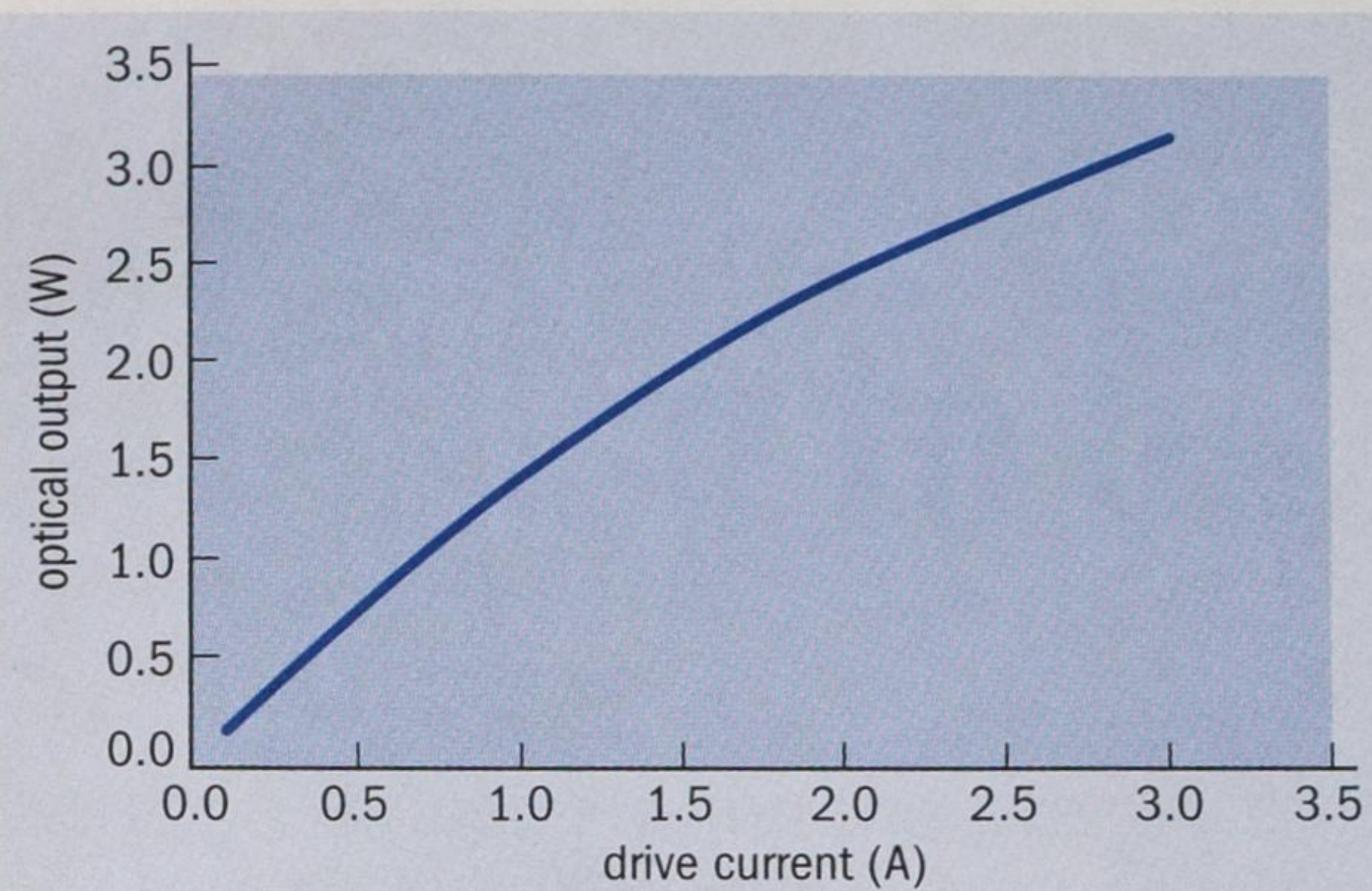


Fig. 2. Osram has combated LED droop with a multiquantum-well active region that has a very low current density. This reduces Auger recombination in the device.

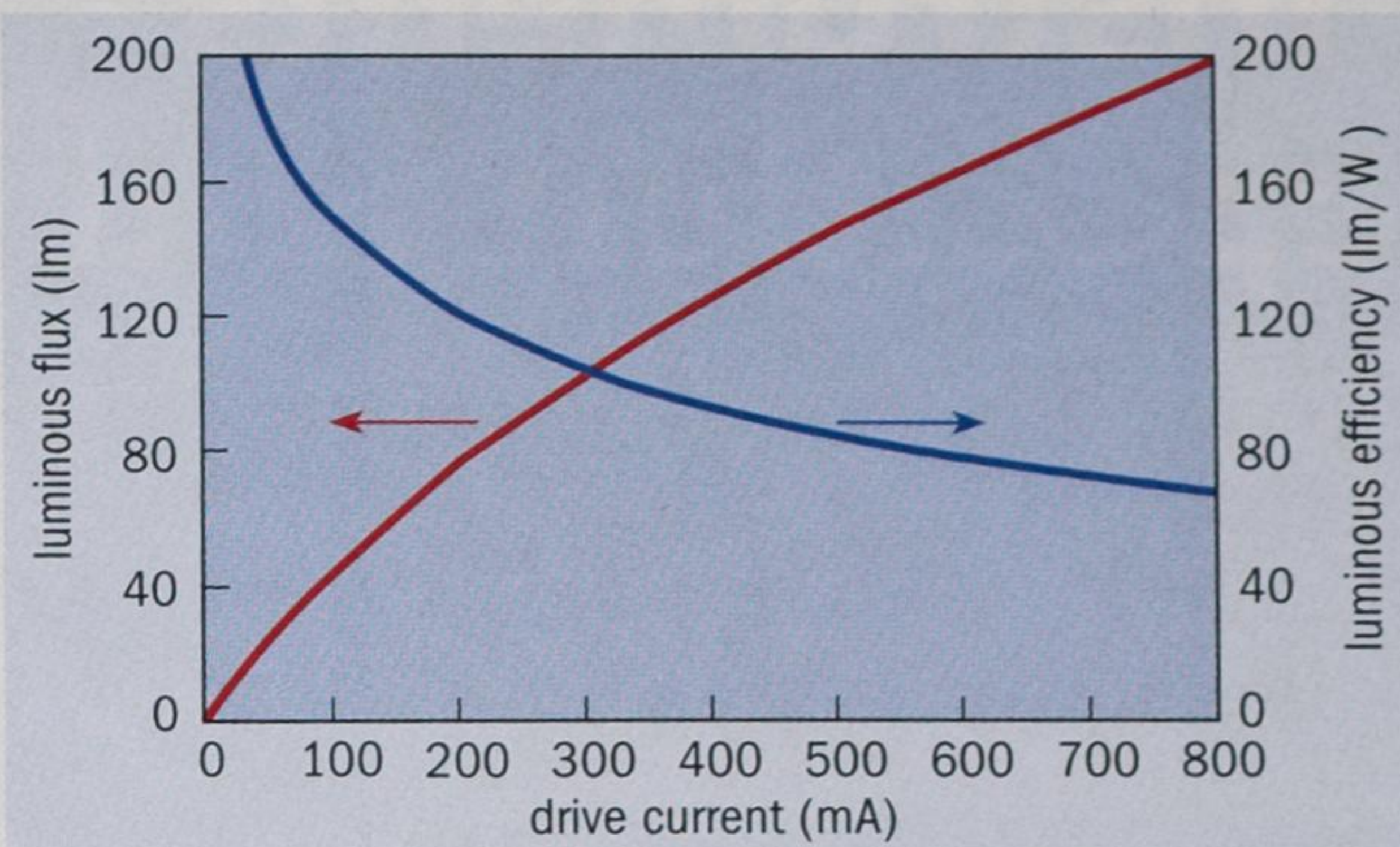


Fig. 3. Green LEDs with a peak emission wavelength of 523 nm have been produced using Osram's latest chip design. These emitters are promising candidates for white-light sources based on the color mixing of red, green and blue LEDs.

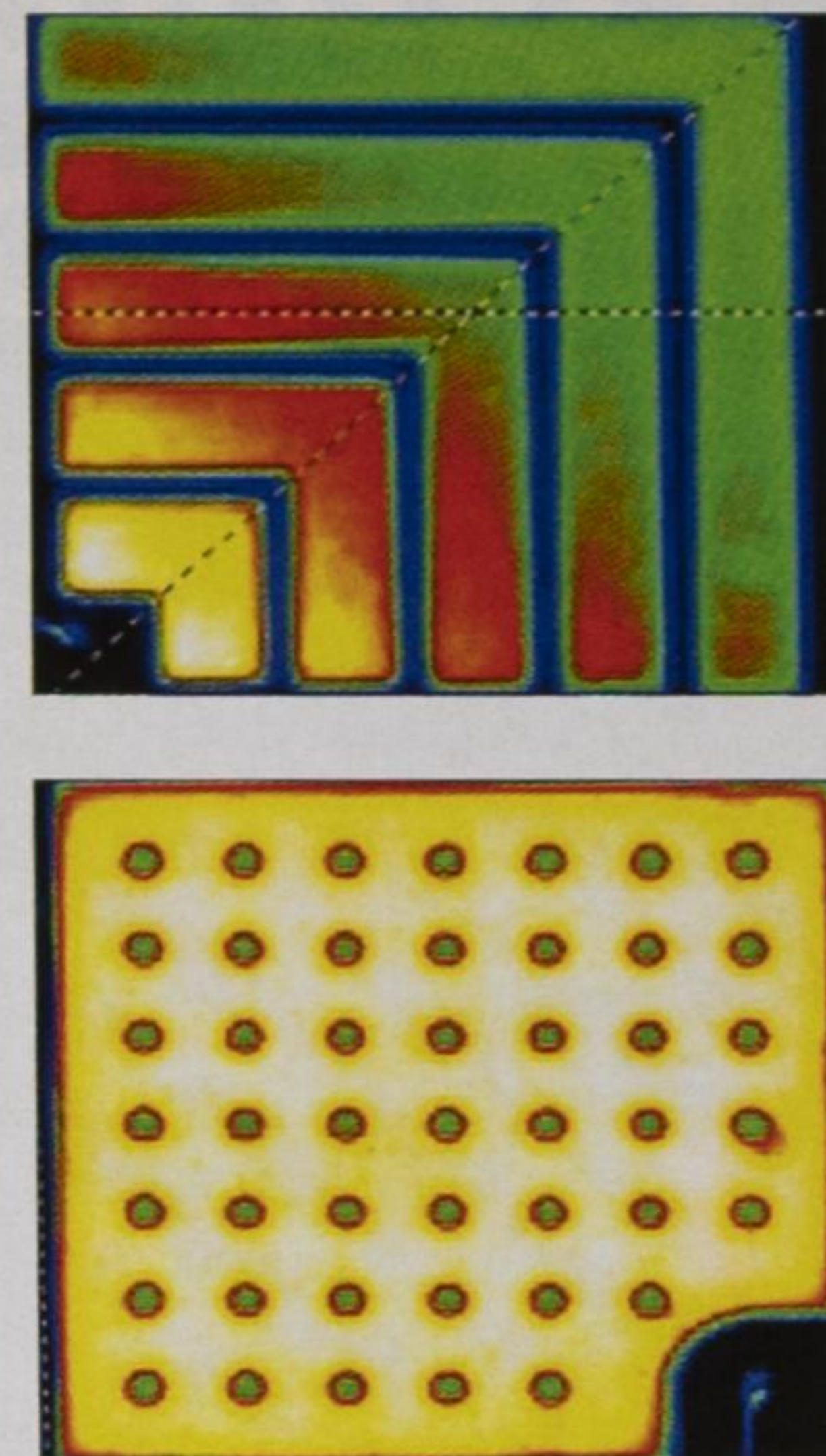


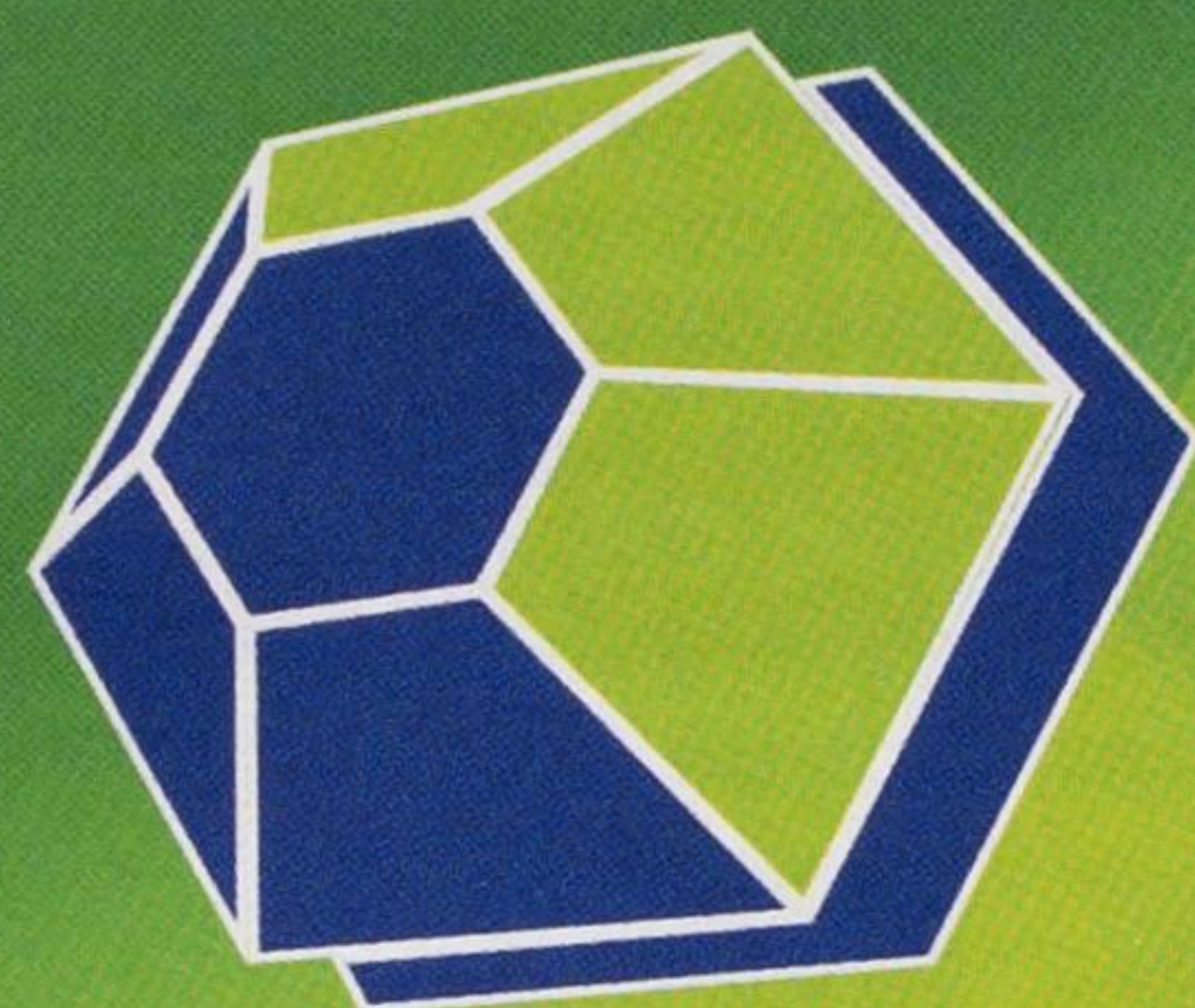
Fig. 4. The latest generation of ThinGaN LEDs employs a superior electrode geometry that leads to a more uniform emission from the chip at high current densities.

lap with the ThinGaN family, it has been relatively easy to manufacture this product in high volumes.

One of the merits of the Osram SSL is its thermal resistance of just 7 K/W, which simplifies thermal management and allows the product to serve high-power-density applications. The combination of a ceramic and silicone package ensures high reliability and allows decoupling of electrical and thermal interfaces. Lighting designers will also appreciate the flexibility of this package. It has a footprint of just 3×3 mm and enables the emission of a well

defined beam that is easy to couple to secondary optics. If particularly bright illumination or color mixing is required, it is easy to combine several light sources into clusters.

Lighting, projection and automotive applications will benefit from our UX:3 chip technology because it provides a high-efficiency, high-current platform that draws on proven ThinGaN processes. Its small size and compatibility with a thermally optimized package creates a cost-effective, highly flexible light source that operates at very high efficiencies. ●



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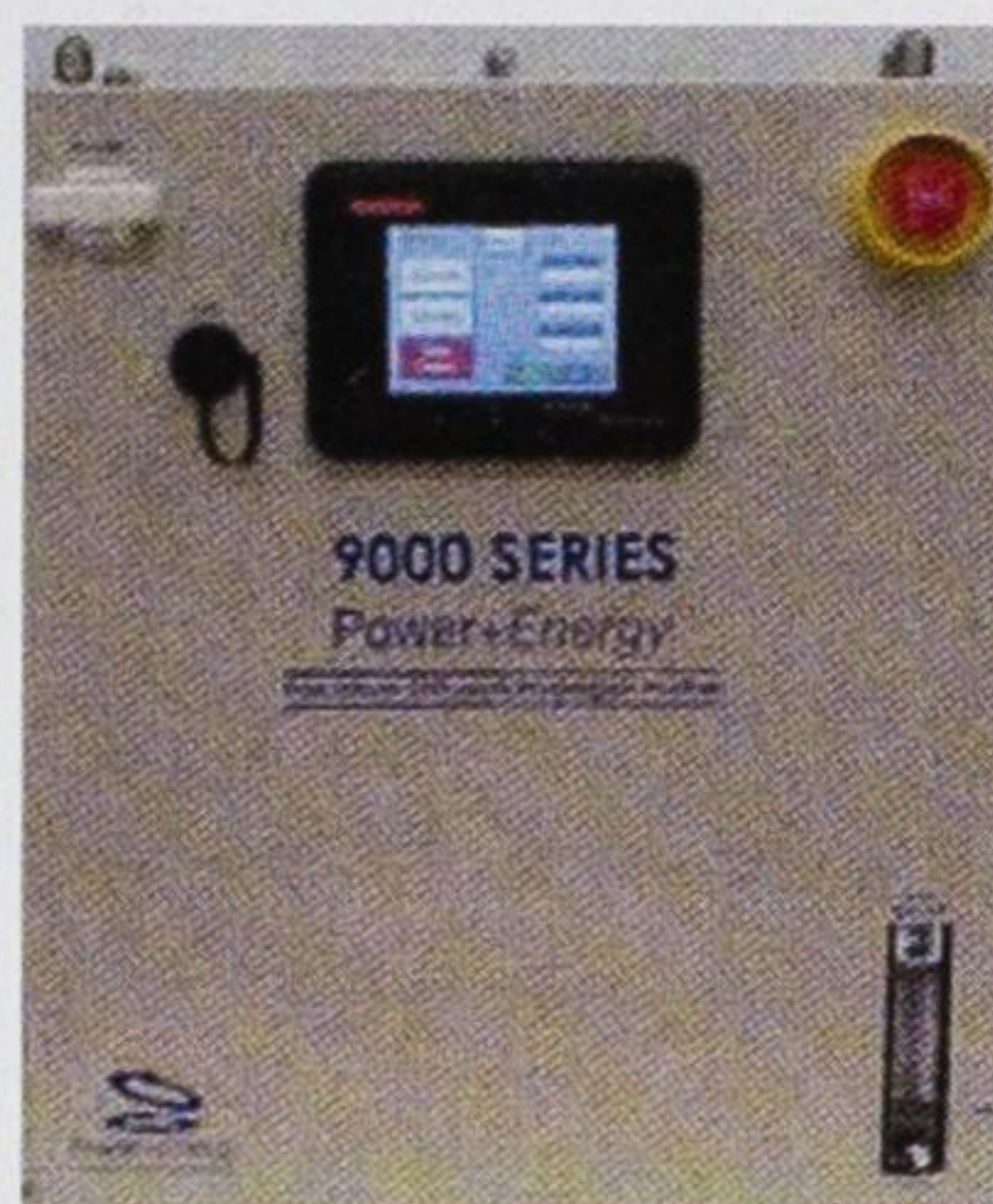
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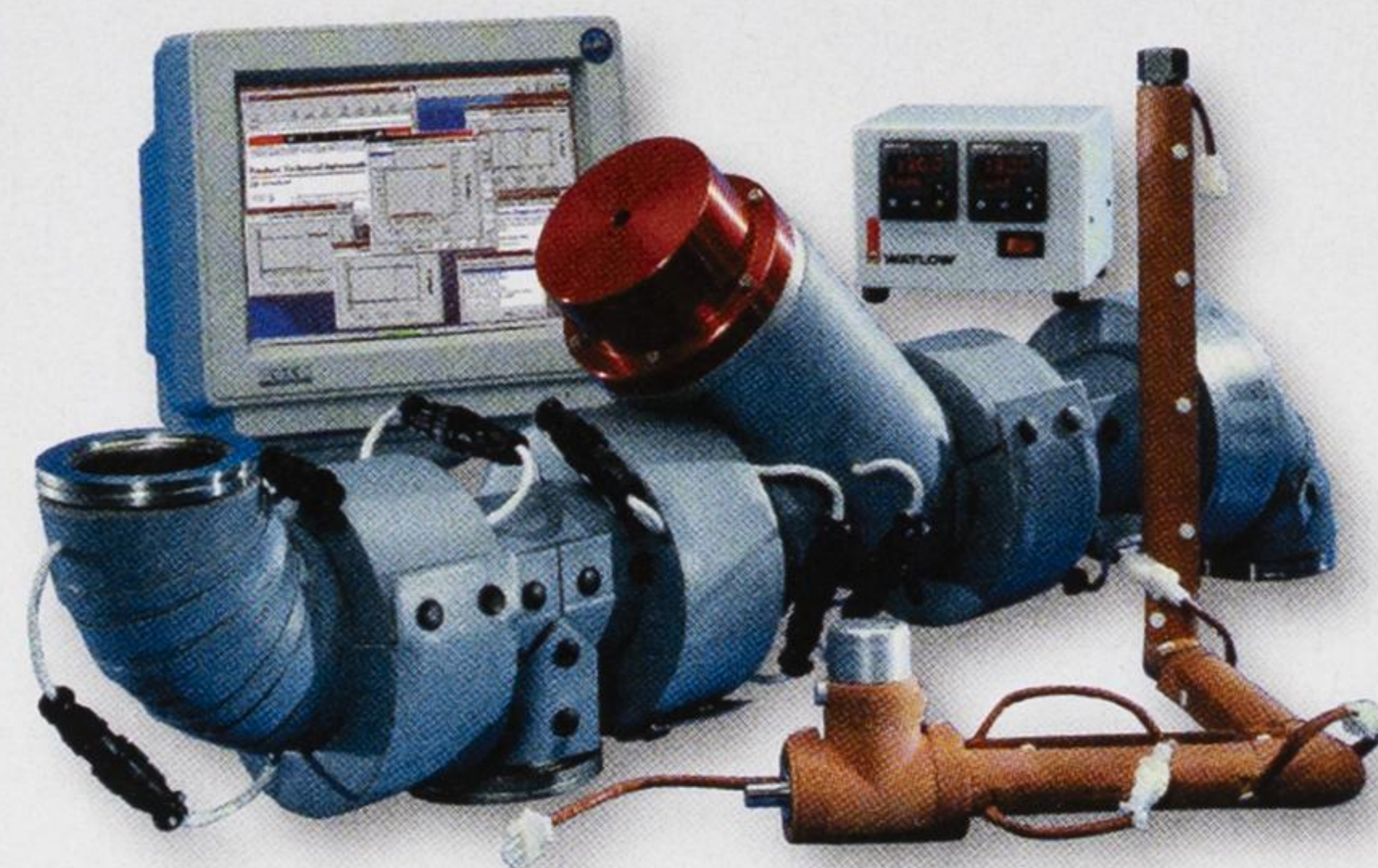
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Fax: +49 (0) 7253 9400-900

Web: www.watlow.com/semicon

Miniaturized monolithic transceivers promise to boost Ethernet capacity

One option for relieving the ever increasing strain on optical networks is to move to far higher bit rates. A European effort called HECTO has adopted that stance and developed 100 Gbit/s Ethernet transmitter chips based on InP, says project leader **Urban Westergreen**.

Internet usage is changing. The number of individuals who are going online is on the rise and they are using this technology for an increasing range of activities, such as watching videos and gaming via broadband access.

These changes in behavior are driving a rocketing rise in data transfer that places greater strain on internet infrastructure. To reduce this burden, developers of technologies for fiber-optical communications are continuing to search for new ways to increase transmission capacity. This quest involves all parts of the fiber-optical communication chain, from backbone networks that provide access for individual users, to local connections between computers in the same building.

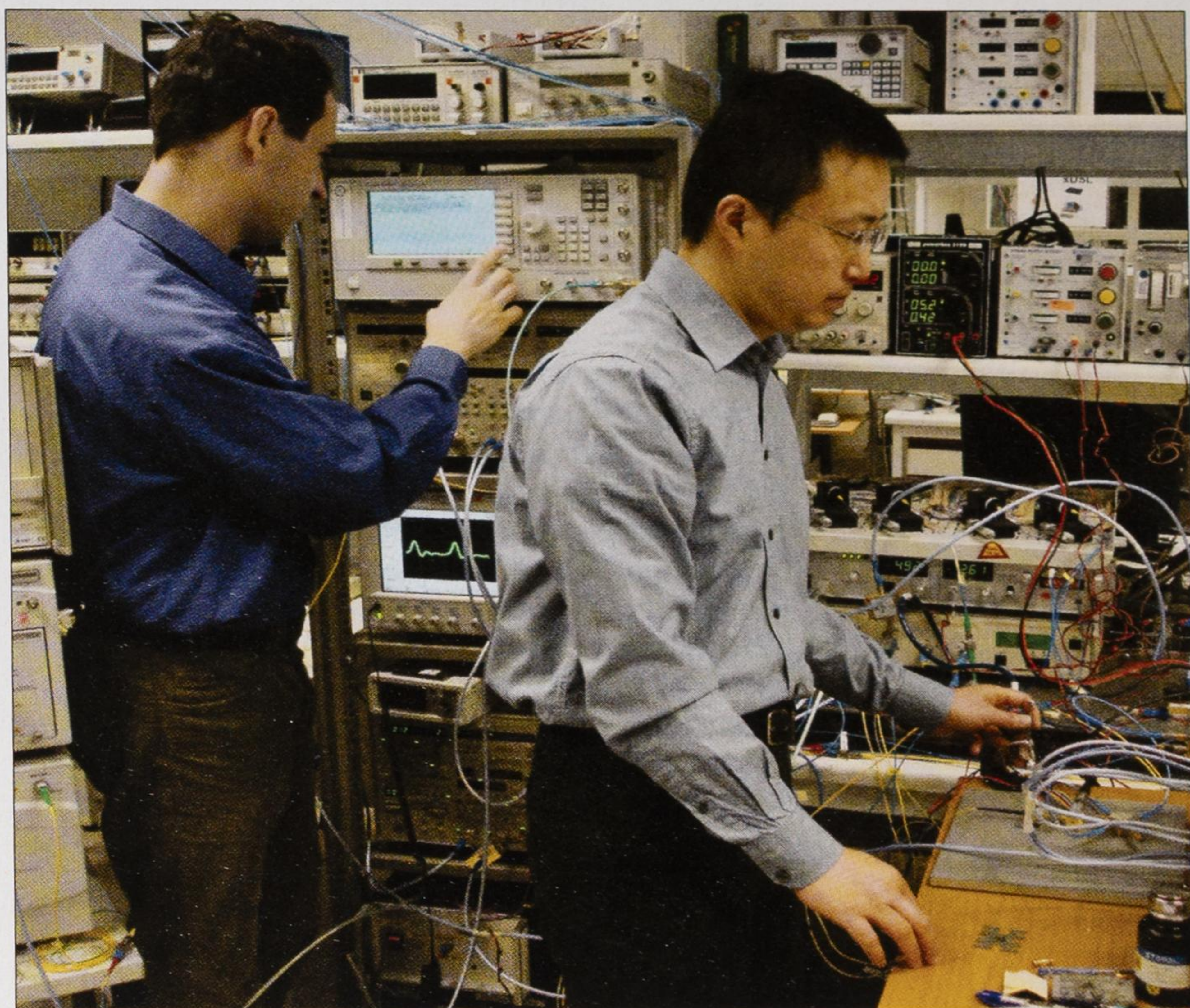
Linking computers together in a business environment is increasingly undertaken with Ethernet technologies. In the 1990s this type of infrastructure provided data transfer at 10, 100 and finally 1000 Mbit/s, and Ethernet speeds are now up to 10 Gbit/s (10 GbE).

European efforts

The next step will be 100 GbE. This race is already underway, and organizations such as the Institute for Electrical and Electronic Engineers (IEEE) and the International Telecommunication Union's telecommunication standardization sector (ITU-T) are currently developing standards for fiber-optical transmission equipment that will enable those higher-capacity networks. Standards, along with multi-source agreements, are essential for driving the development of faster Ethernet networks, because they enable the builders of networks to source components from a variety of manufacturers.

Fabricating components for 100 GbE is very challenging because the route to higher speeds involves shrinking the component size. Scaling can cut capacitances, inductances, resistances and transit times, but success demands increased control of the dimensions, which in turn pushes up the complexity of fabrication.

To spur faster transmitters and receiver development, the European Union started to fund a



The HECTO project, which is led by the KTH Royal Institute of Technology, allowed for the design of two generations of components for 100 GbE. Earlier this year the first-generation devices were tested in the systems laboratory of Acreo. Testing of the second generation will follow.

handful of projects from 2005 to develop suitable technologies. These efforts, which marry the talents of universities with the expertise of companies involved in the telecommunications industry, include: a €5.7 million (\$7.7 million) effort entitled “integrated photonic mm-wave functions for broadcasting connectivity (IPHOBAC)”, which combines radio and optical technologies; a project called “optoelectronic integration for 100 Gbit/s Ethernet optical networks (GIBON)”, which is led by the Alcatel-Thales III-V lab and backed by €1.9 million of funding; and a €6.6 million project led by Alcatel-Lucent, “100 Gbit/s carrier-grade Ethernet transport technologies (100GET)”.

The roles of the HECTO partners

The HECTO consortium consists of nine partners from Denmark, Germany, Sweden and Greece: three academic institutions, three industrial laboratories, two SMEs (small or medium-size enterprises), and a multinational provider of optical networks. These partners are as follows:

- KTH Royal Institute of Technology, Kista, Sweden. This partner coordinates the project and develops optoelectronic transmitter devices.
- Fraunhofer Gesellschaft, Heinrich-Hertz-Institut (FhG/HHI) in Berlin, Germany, which is developing optoelectronic receiver devices and providing systems testing.
- Syntune AB, which is based in Kista, Sweden. This company co-operates with KTH on the

development of semiconductor processing methods for optoelectronic transmitter devices.

- Fraunhofer Gesellschaft, Institut für Angewandte Festkörperphysik (FhG/IAF) in Freiburg, Germany. This institution develops all of the electronic circuits for the transmitter and receiver, including the multiplexer, modulator driver amplifier, clock and data recovery circuit, and demultiplexer. These circuits are enclosed in packaged modules.
- DTU Photonics in Copenhagen, Denmark, which is part of the Technical University of Denmark. This institution performs device testing.
- Acreo AB, an SME in Kista, Sweden. The research institute operates a fiber-optical

communication test-bed that can perform field trials to evaluate the combined performance of transmitters and receivers. This will be carried out at the end of the project.

- U²T Photonics AG, an SME in Berlin, Germany, that packages the optoelectronic devices into transmitter and receiver modules.
- Nokia Siemens Networks in Munich, Germany. This company is involved with the drafting of international standards and ensures relevant specifications for all of the components produced in the HECTO project.
- University of Peloponnese, Greece, which is responsible for studying the systems aspects of the components, including application areas.

We are also developing components for 100 GbE through a €3.8 million, three-year project called HECTO (high-speed electro-optical components for integrated transmitter and receiver in optical communication). This effort, which kicked off in November 2006 and is partly funded by the European Union, draws on the expertise of industrial and academic researchers from nine institutions (see box “The roles of the HECTO partners”). Its focus is the scaling of commercial component architectures employed for 10 GbE, so that they can offer a cost-competitive option for the deployment of 100 GbE.

The HECTO project has four primary objectives. The first is the full development of packaged transmitters and receivers that are suitable for optical systems based on serial 100 GbE signals. We are focusing on a single data stream at 100 Gbit/s, which needs a total transmission of about 110 Gbit/s to accommodate error-correction coding. Another target is to determine the specifications for all interfaces of the photonic components. This has to take into account emerging relevant standards, the identification of application areas for the components and the impact that this has on their specifications. The other two goals are to test the fully packaged transmitters and receivers in laboratory system test-beds and perform field trial tests; and to exploit the results of the project, through component vendors Syntune and U²T Photonics, which are consortium partners.

A two-pronged attack

During the HECTO project we have intentionally developed two distinct generations of hardware. As the project has progressed, we have modified the exact specifications for the transmitter and receiver

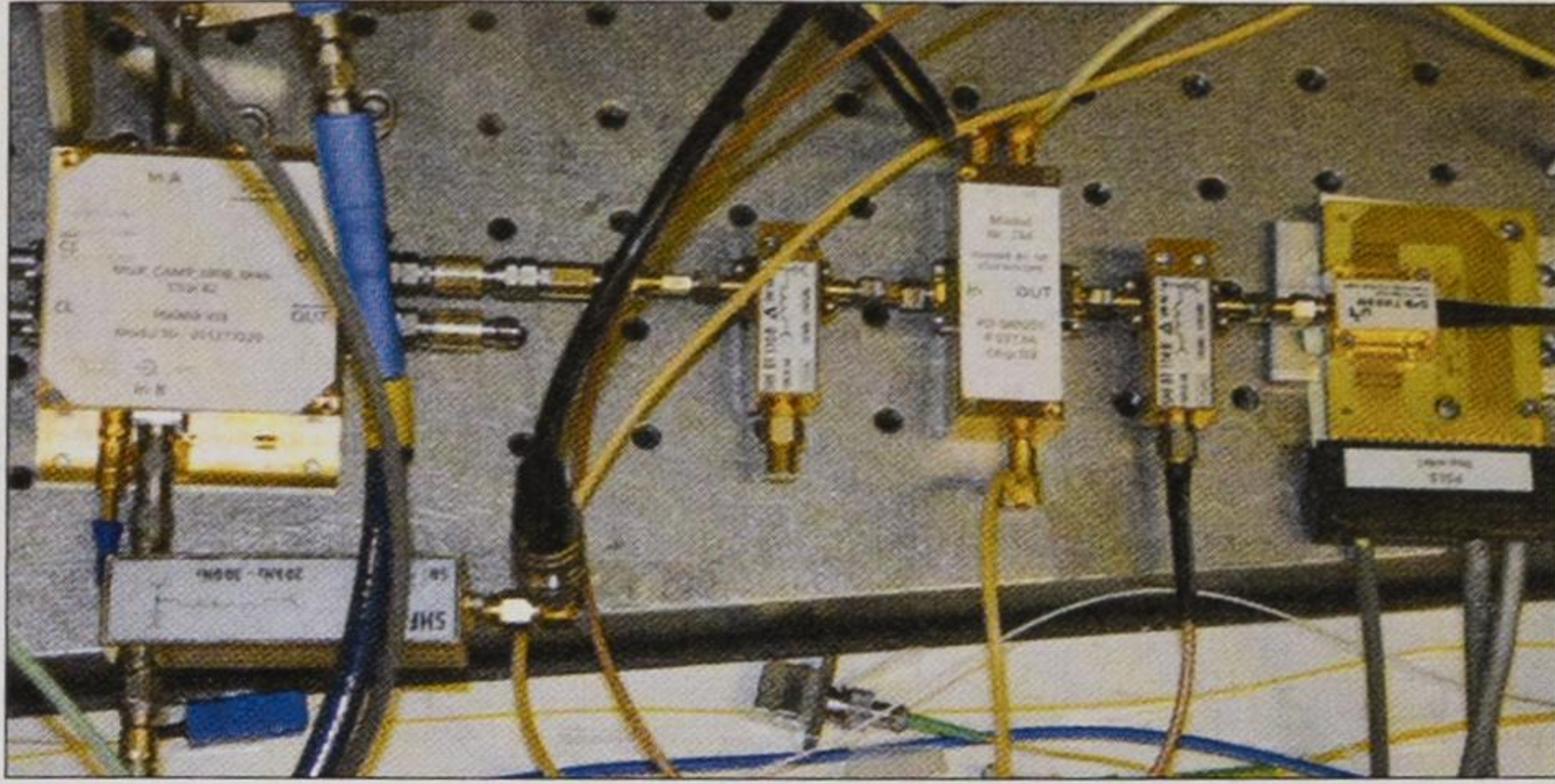
modules. These adjustments are partly driven by a greater awareness of how we can optimize our technology, but they also allow us to accommodate any changes in standardization.

We evaluated the performance of our first generation of semiconductor devices last year. Although these chips could be viewed as just a test run that provides useful input to a subsequent set of devices, the results produced by these components have been published and they have attracted significant international interest. Tests are now underway to evaluate the performance of all parts of the transmitters and receivers in optical networks.

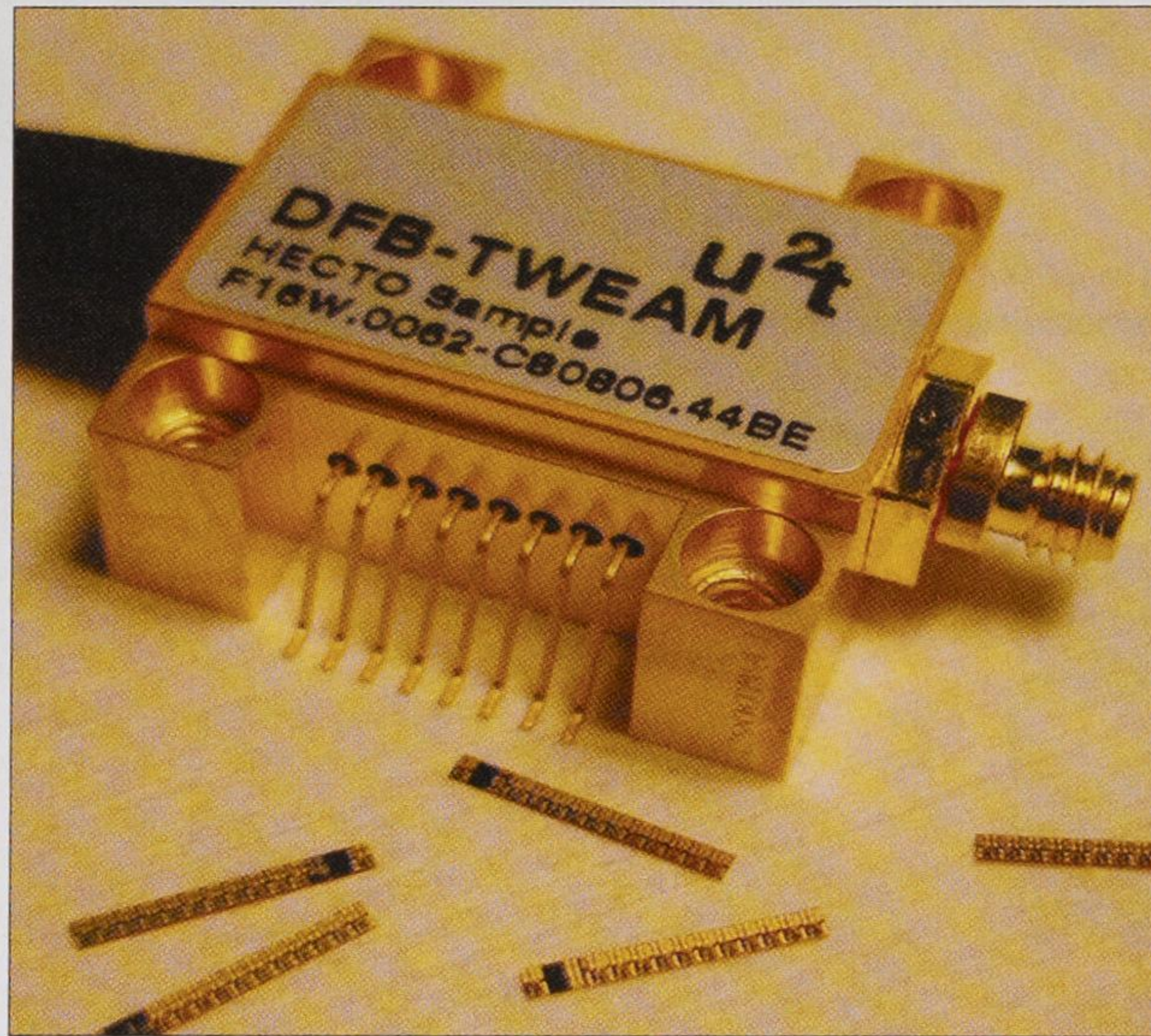
One of the initial highlights of our project is a transmitter that was produced by KTH and Syntune, which combines a light source and a light-intensity modulator on one chip with dimensions of just 1 mm × 0.5 mm. This features the first modulator design capable of 100 GHz that can be monolithically integrated with a distributed feedback (DFB) laser.

The DFB laser design employed in this transmitter spans the 1530–1550 nm range. This allows the source to be used in wavelength-division multiplexed fiber-optical communication systems that simultaneously transmit the light pulses from several lasers down a single fiber.

The modulator features a quantum-well stack and changes to the voltage applied across the device produce strong variations in absorption at the laser's wavelength. A distributed microwave design is used in the travelling-wave electroabsorption modulator (TW-EAM), with the electrical signal following the light path and interacting with it over a length of about 0.2 mm. The short interaction length cuts electrical power consumption and increases the



The first generation of transmitter modules was tested in a set-up that included a 2:1 multiplexer circuit in a square-shaped package (left), a modulator driver (middle), and a laser and modulator combination in the package on the test card (right). A number of biasing circuits (bias-Ts) were included.



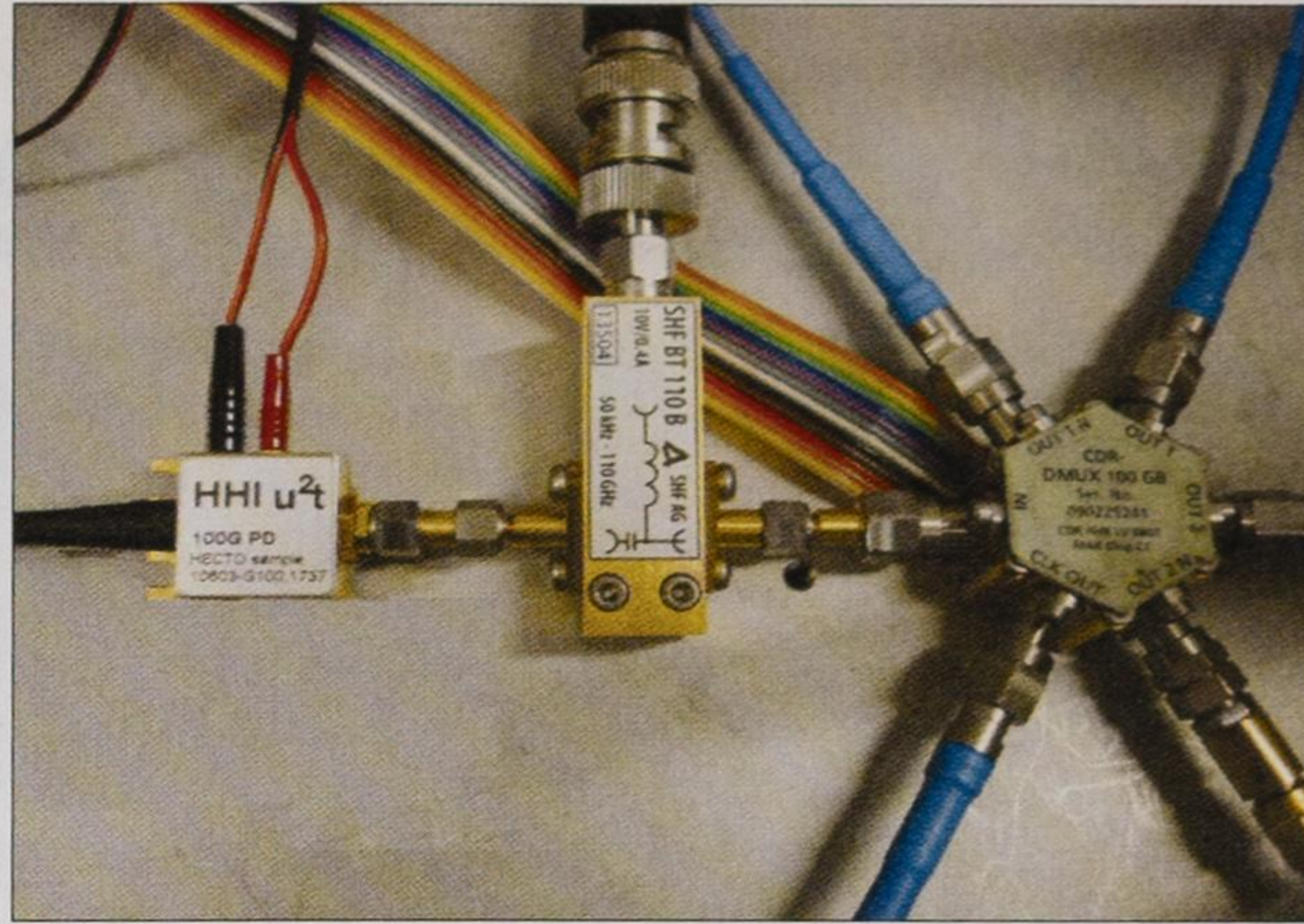
Optoelectronic device packager U²T Photonics has produced a module containing a distributed feedback laser and a travelling-wave electro-optic modulator that is designed by KTH and Syntune. This device provides good electrical matching to standard high-frequency electronics. The modulator and laser are integrated on a single chip. An array of these transmitters is shown to the front of the module in the image.

maximum bit rate.

We are now well into the final year of the HECTO project, and one of the outstanding tasks is to take our second-generation components and evaluate them in trials at Acreo's test-bed in Kista. It is likely that the modules that were built in this project will eventually be deployed in more general measurement equipment for high-speed components for fiber-optical communications.

100 Gbit/s and beyond

The optical components that are built in the HECTO project use the same form of optical signals used today in 10 GbE. With this approach, the light intensity is switched between a high and a low power level to encode every binary bit in the data stream. This approach, known as on-off keying, is an economically viable solution at lower bit rates. However, at data rates of 100 Gbit/s and beyond the construction



First-generation receivers were tested in a set-up that included a photodetector in a square package (left) and a 1:2 demultiplexer in a hexagonal package (right).

of the electrical circuit and electrical interconnects is very challenging, because they have to handle a frequency range that spans 0 Hz to around 100 GHz. This is 10 times as wide as that needed for 10 GbE.

To span this wider range we have miniaturized some parts of the electrical circuitry because this reduces loss and microwave reflections. For example, the diameter of the coaxial cable is just 1 mm. However, making this cable smaller pays the penalty of increased fragility and leads to greater electrical loss due to the finite conductivity of gold.

Increasing bit rates beyond 100 Gbit/s with the same type of solution would require further refinement to the electrical parts of the transmitters and receivers, and this would be very challenging. So we believe that it is more likely that other approaches will be used to move to faster speeds. One further downside of on-off keying is that it needs a relatively large optical bandwidth, and this is a weakness in wavelength-division multiplexing systems that use a narrow channel spacing to maximize capacity.

Several partners in the HECTO program are also participating in the 100GET project, which is investigating the benefits of other forms of optical signal. Options for improving the spectral efficiency of the light signal include schemes that modulate the intensity of the light and its phase. This effort is still at an early stage, but there are no obvious reasons why it will not be possible to slash the size of the relatively bulky components currently used in the lab to those realized in the HECTO project. Massive year-on-year increases in internet traffic are sure to continue, and these types of components will be needed to deliver the required expansion of internet capacity.

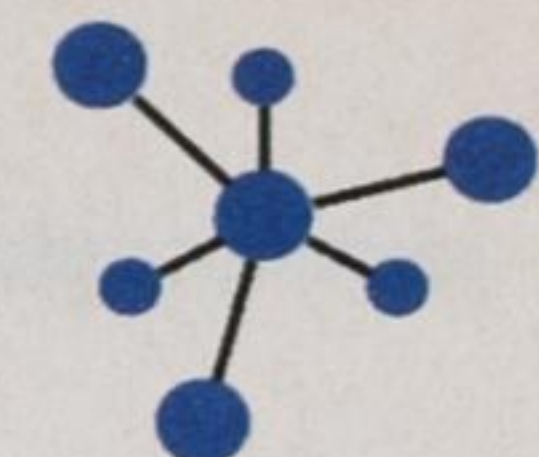
Further reading

www.celtic-initiative.org/Projects/100GET/
www.hecto.eu
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www.ist-gibon.eu
 M Chacinski *et al.* 2008 *IEEE Electron Device Letters* **29** 1312.



About the author

Urban Westergreen is the coordinator of the HECTO project. He is an associate professor in the Laboratory of Photonics and Microwave Engineering at KTH, and his principle area of research is the design and measurement of receivers and transmitters for fiber-optic communication at very high bit rates. During the last few years he has focused on state-of-the-art electroabsorption modulators.



GAN-ON-SILICON HEMTs

Oki Electric breaks power density record

Researchers at Oki Electric say that they have broken the output power density record for a high-voltage GaN HEMT built on silicon.

The Japanese team's transistor, which could be used to provide amplification in a 3G network base station, delivers 12.88 W/mm.

The output power from Oki's device is still inferior to that produced by GaN-on-SiC equivalents, which can deliver more than 30 W/mm at 4 GHz. However, lead author Shinichi Hoshi points out that silicon substrates have one considerable advantage – they are 100 times cheaper.

He thinks that the team's success stems from addressing two weaknesses of GaN-on-silicon HEMTs: a high parasitic loss, which

degrades RF performance; and the substrate's low thermal resistance that hinders heat dissipation from high-power devices.

High parasitic loss is caused by the conductive layer at the silicon–GaN interface, which results from gallium diffusion into the substrate. Oki's engineers have developed a proprietary growth process that eliminates this layer, according to carrier concentration profiles measured by the capacitance-voltage method.

GaN HEMTs fabricated with the superior growth process delivered a hike in the maximum oscillation frequency from 13.8 to 101.4 GHz.

Substrates just 60 μm thick were employed

for the growth and improvements in the transistor's thermal management enabled the record-breaking output of 12.8 W/mm at a drain-source voltage of 70 V, alongside a large signal gain of 19.2 dB. At 5 GHz, output power is 7.5 W/mm and gain is 12.8 dB.

The researchers are now starting to study device reliability. Hoshi says that the team has performed preliminary reliability tests at 70 V and the results suggest that the HEMTs do not suffer from a substantially rising gate leakage current, or a falling output power.



Journal reference

S Hoshi et al. 2009 *Appl. Phys. Express* **2** 061001.

EPITAXY

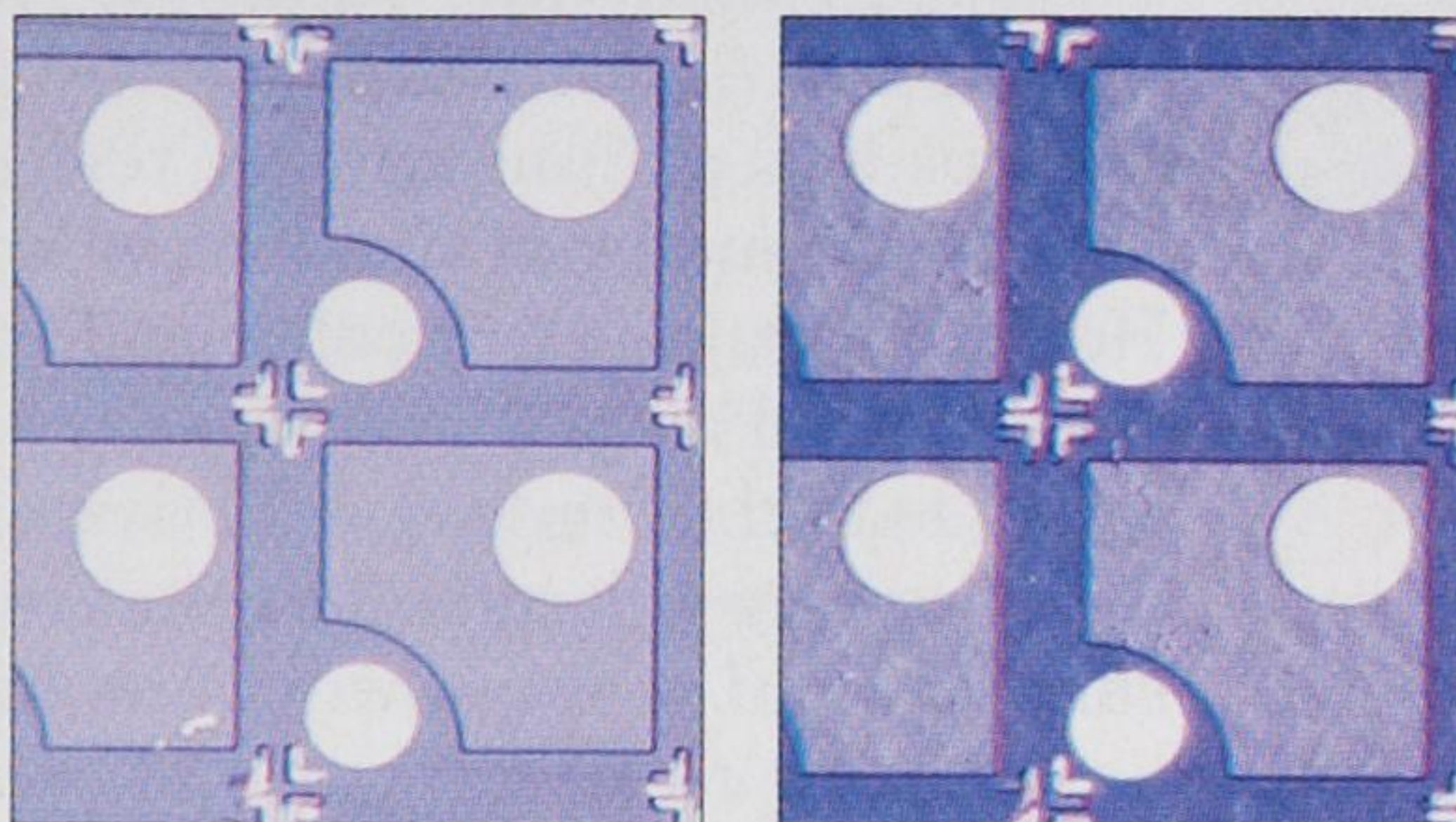
Sapphire interlayer aids GaN-on-Si LED output

Ian Ferguson and co-workers at Georgia Institute of Technology have produced crack-free GaN-on-silicon LEDs that feature an Al_2O_3 interlayer and produce similar internal quantum efficiencies to controls grown on sapphire.

Silicon substrates are a desirable platform for LED production due to their low cost. However, successful growth of LEDs on silicon requires overcoming issues related to the thermal and lattice mismatch between the two materials.

Ferguson's team has addressed this by adding a 5–20 nm thick Al_2O_3 interlayer by atomic layer deposition, before growing nitride epilayers in an Emcore D-125 MOCVD system.

The silicon-based devices emit at a longer wavelength than their sapphire counterparts,



Researchers have fabricated 350 μm $\times$ 350 μm GaN-on-silicon (left) and GaN-on-sapphire (right) LED structures with internal quantum efficiency of more than 30% at room temperature.

due to tensile strain and higher indium composition in the active layer. Two emission peaks are produced by this LED and the researchers believe that this may be caused by non-uniformity in the composition of the InGaN in the quantum wells.

The researchers fabricated their LEDs on 2 inch silicon substrates that were cut into halves or quarters. "The size limitation

stems from our oxide deposition system, which until recently could only accommodate these smaller wafer sizes," said lead author William Fenwick.

Reducing LED manufacturing costs will require the growth of devices on far larger silicon substrates, where issues such as wafer bow and thin-film uniformity come into play. "However, our initial attempts to scale the process to larger substrates have shown promise," said Fenwick, "and we are hopeful that we can demonstrate a process on larger silicon substrates in the near future."

He believes that the particular architecture of the team's LEDs will allow novel approaches to device processing. "The use of the oxide layer will allow for wet etch removal of the substrate, opening the door to new approaches to light extraction and thermal management."



Journal reference

W Fenwick et al. 2009 *Appl. Phys. Lett.* **94** 222105.

INTEGRATION

Silicon boosts InP MOSFET characteristics

InP MOSFETs with a HfO_2 gate dielectric can deliver higher drive current, higher transconductance and a lower gate leakage if they contain a silicon passivation layer, according to researchers at the University of Texas at Austin.

This team claims that the improvements stem from addressing the poor quality of the interface between the gate and InP that tends

to suffer from Fermi level pinning. Poor quality interfaces continue to plague the development of all forms of III-V MOSFET, which have the potential to offer a superior performance to silicon equivalents that are used in microprocessors, thanks to higher electron mobilities.

Engineers at Austin produced InP MOSFETs with a 1 nm thick silicon passivation layer and a 5.1 nm thick HfO_2 gate, and compared their performance with control devices that just employed a 7 nm thick HfO_2 gate.

The silicon interlayer tripled transconductance to 2.3 mS/mm, increased the drain

current from 5.9 to 25.9 mA/mm and cut gate leakage from 3.9×10^{-2} to 1.32×10^{-2} A cm^{-3} . Sub-threshold swing, which determines the voltage swing needed to switch the MOSFET from its off-state to its on-state, was reduced from 137 to 103 mV/decade.

Author Yen-Ting Chen says that the team now plans to investigate the role of the silicon interface passivation layer on III-V MOSFETs that feature other high-k dielectrics.



Journal reference

Y-T Chen et al. 2009 *Appl. Phys. Lett.* **94** 213505.

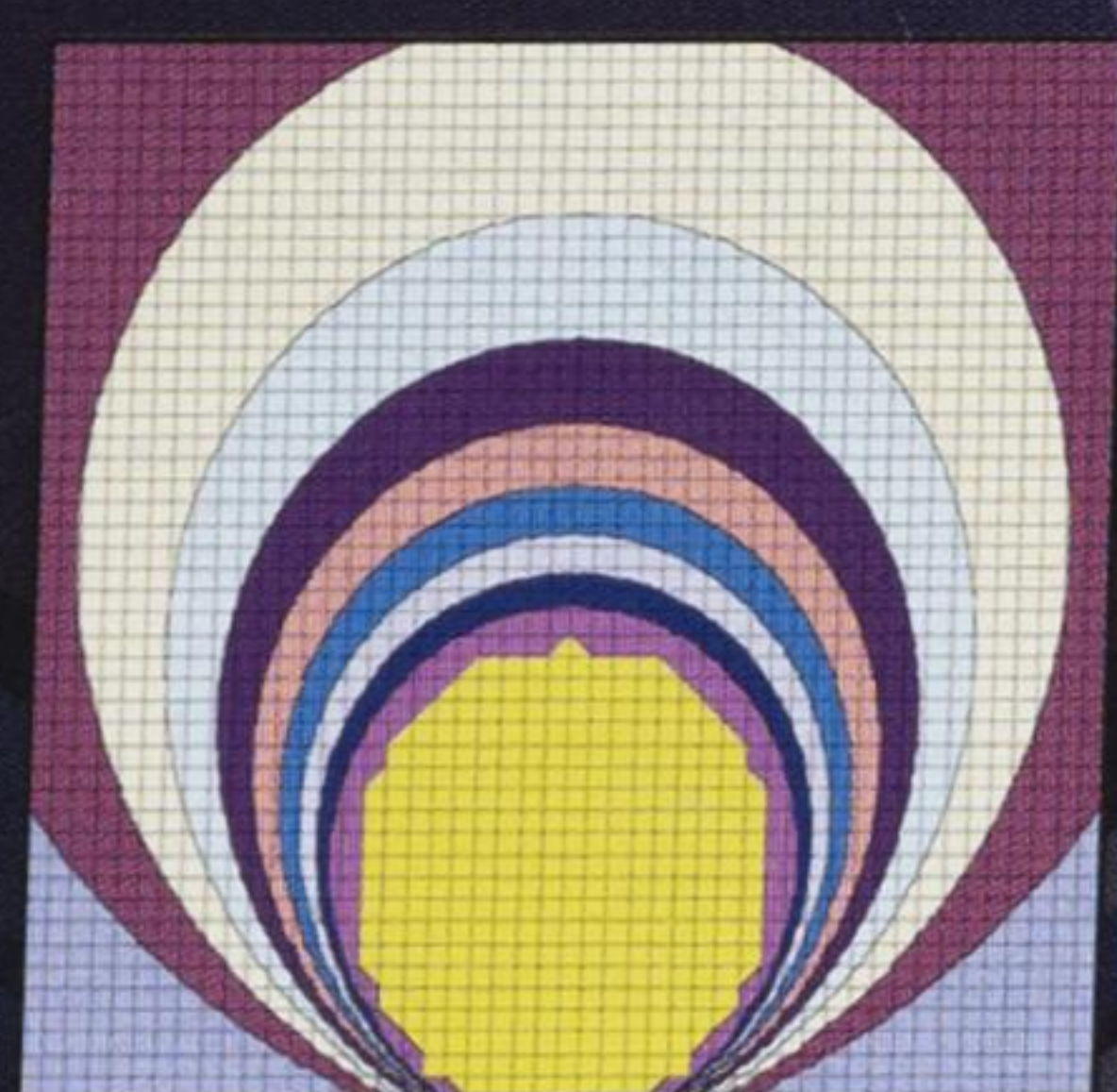
Germanium Substrates: Powering your Growth!



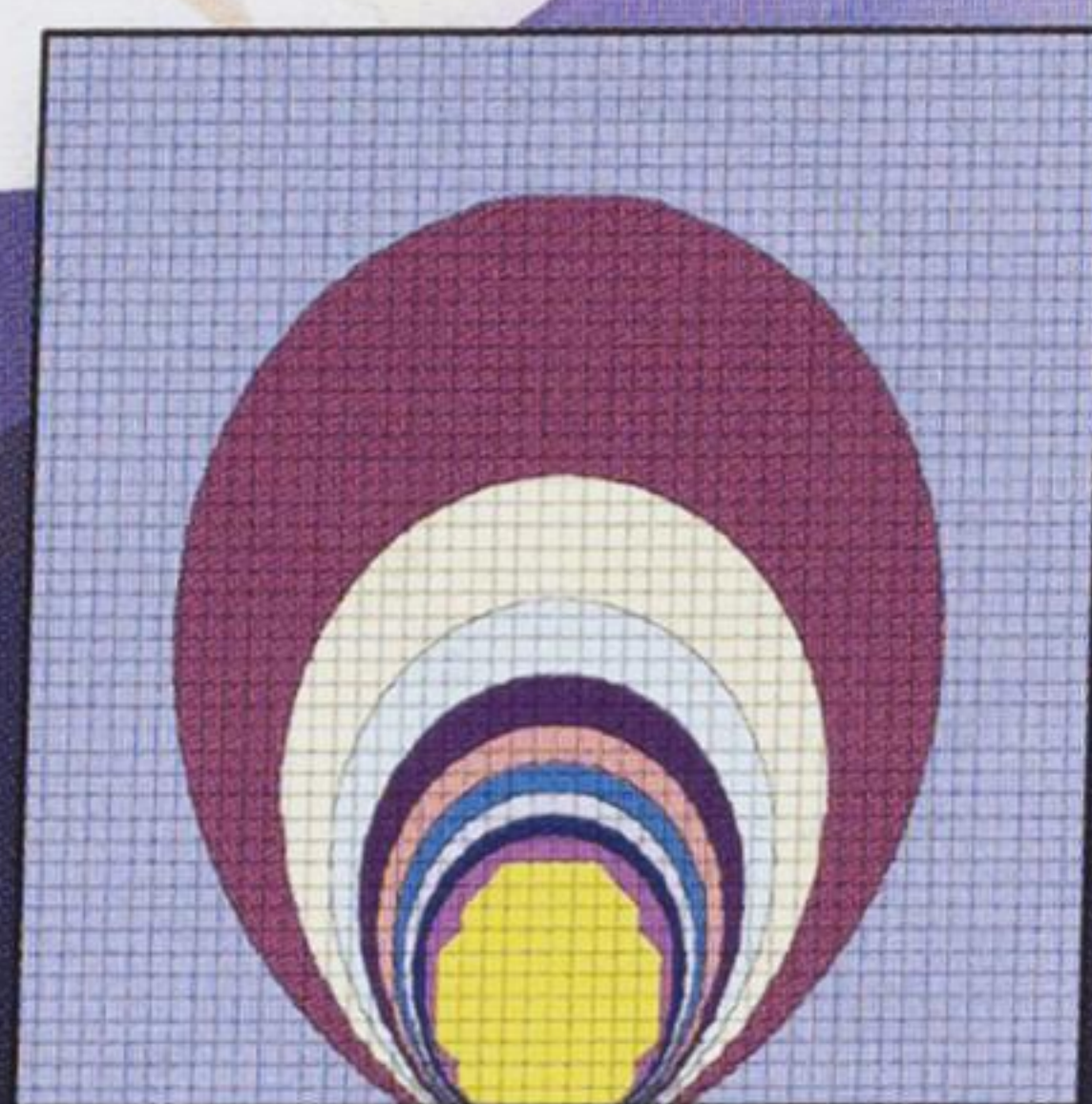
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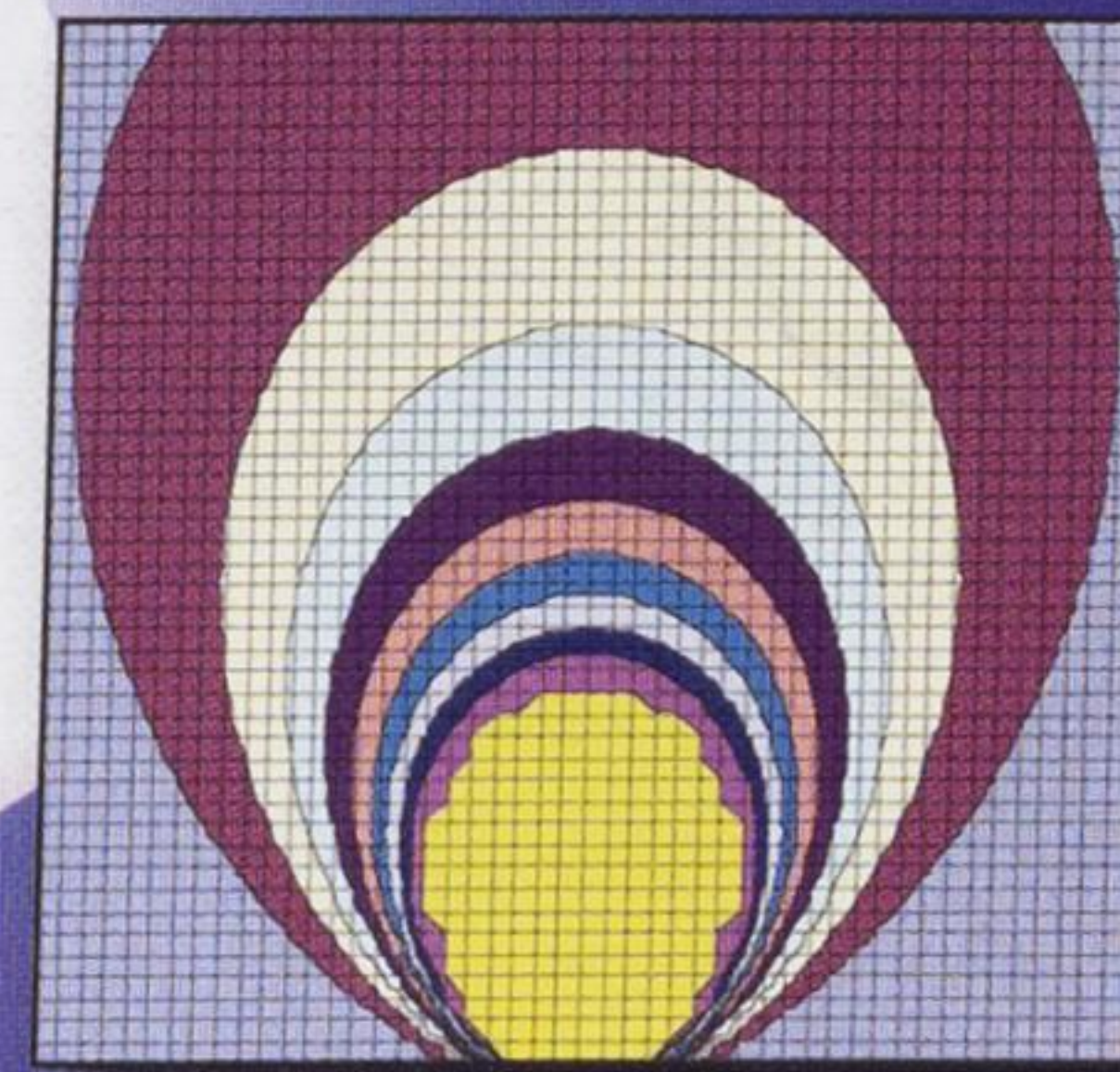
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