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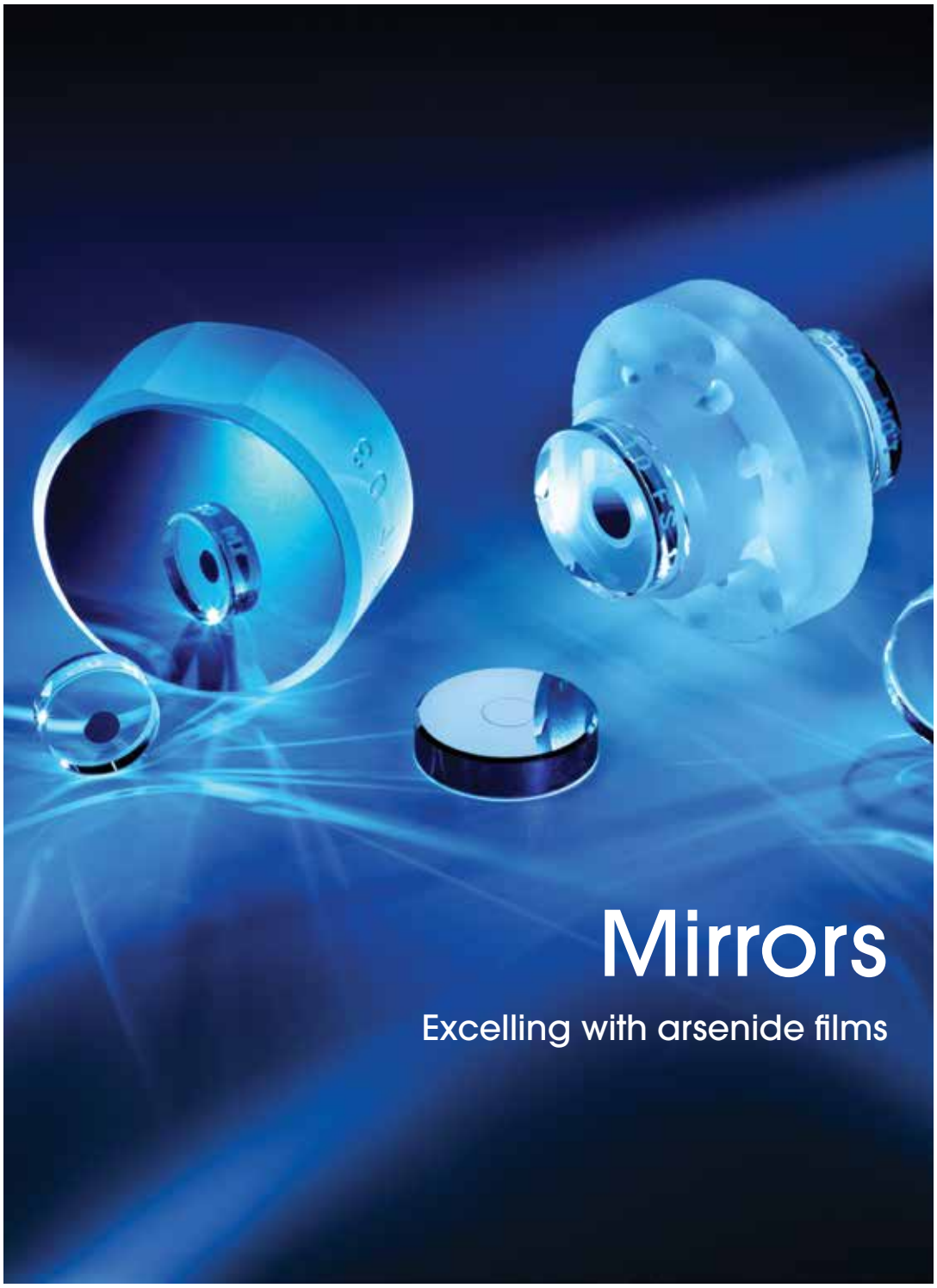
Scrutinising the purity of metal-organic sources

Uniting high-mobility transistors on silicon

Producing high-quality semi-polar substrates

Integrating GaN lasers and photodetectors



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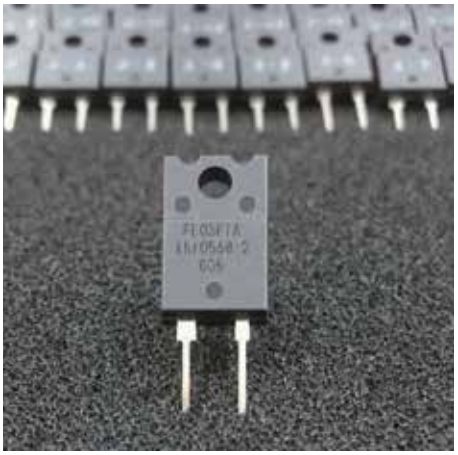
Viewpoint

By Dr Richard Stevenson, Editor

Gallium oxide: Fulfilling the promise

SILICON DIODES and transistors are the incumbent power devices, offering affordability, reasonable performance and are limited range of operating temperatures. Taking away market share are devices made from SiC and GaN, which sport better performance, but command higher prices.



Many will view SiC and GaN as heavyweights, outgunning silicon chips in efficiency and maximum operating temperatures. But I'd argue that it is better to consider them as middleweights, packing a good punch, but one that's not as strong as that from the true heavyweights: AlN, diamond and Ga_2O_3.

The leading pioneer of the latter material is the Japanese start-up Flosfia. It gave a keynote presentation at this year's highly successful CS International Conference and recently spoke to us in an exclusive interview (see *Gallium oxide: Ready to take on SiC and GaN* on p.18).

Flosfia is at that tricky stage, trying to convert promising results into profitable production. It has a lot in its favour: thanks to a bandgap of around 5 eV, diodes have been demonstrated with an on-resistance that is one-seventh of that of the best commercial SiC device; and the company has plenty of cash to fund its ramp up from R&D fabrication to high-volume manufacturing.

Swelling its coffers has been a recent injection of $5.4 million, which includes a contribution from Yaskawa Electric. The cash will help the company to start delivering 5 A, 600 V Schottky barrier diodes in 2018. MOSFET sampling is slated for 2019. Initial production costs are expected to be as high as those for SiC and GaN. However, diodes could reach cost-parity with silicon in 2019.

Helping to hit this cost target is the company's novel, proprietary growth technology: mist epitaxy. Sapphire substrates are loaded into a chamber, heated, and then exposed to a fine mist of particles that are swept in on a carrier gas. When this mist, which contains metal compounds, hits the hot substrate it decomposes. This leads to the deposition of a film of gallium oxide.

Production costs could be very low, because the whole process can be cycled through rapidly, as the chamber never needs to be evacuated completely.

Flosfia clearly has a great deal of promise. But will it be able to wrestle market share from the makers of silicon, SiC and GaN devices? I'm hopeful, but we'll just have to wait and see.

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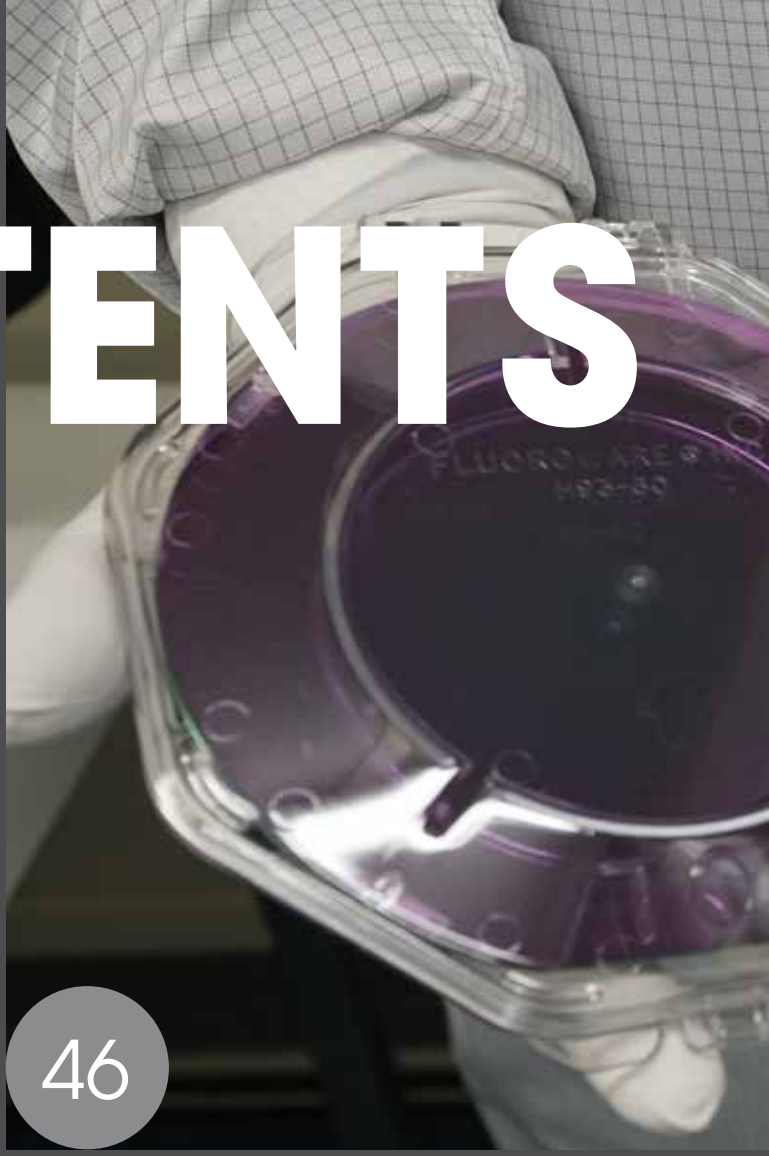

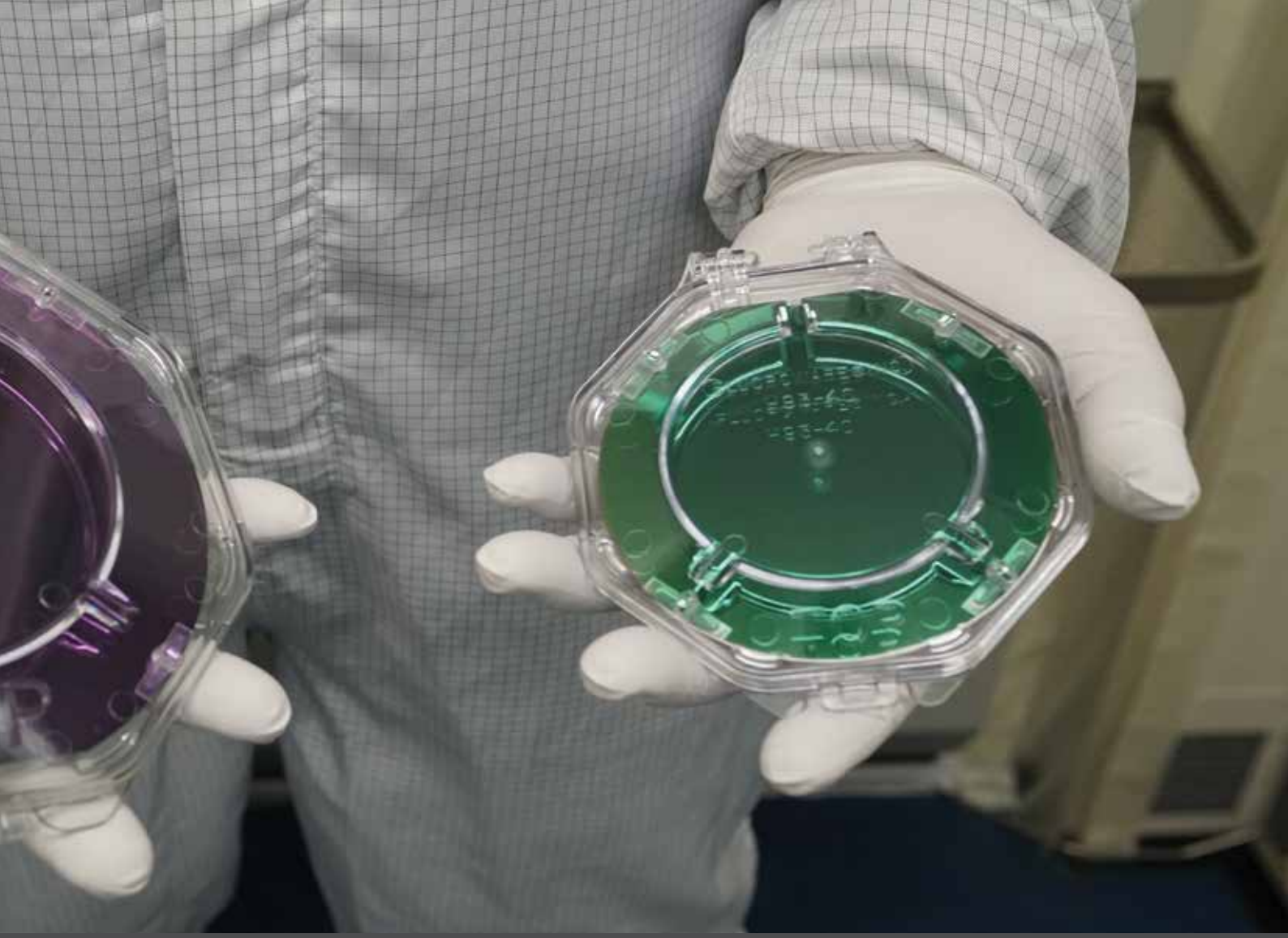

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GaN RF power devices gaining market share

ABI RESEARCH forecasts that GaN RF power devices will represent nearly 25 percent of all high-power semiconductors for mobile wireless infrastructure in 2017.

"The increasing and critical need for wireless data remains an important market driver," says Lance Wilson, Research Director at ABI Research. "LTE and the initial building blocks of 5G will fuel the market's growth for the next five years."

RF power amplifiers (RFPA) are integral parts of all basestations for cellular and mobile wireless infrastructure. They represent one of the most expensive component sub-assemblies in modern wireless infrastructure equipment, and both their performance and cost are important drivers in basestation design. The RF power semiconductors used in these power amplifiers must keep pace with the economic and technical realities facing designers and users of these RF power amplifiers.

"Efficiency, physical size, linearity, and reliability are among the principal concerns," concludes Wilson. "As price pressures become fiercer, new and innovative techniques and materials must be used to reduce the cost of this important component part while still maintaining performance."

The Asia-Pacific region, including China, will drive present and future revenue. These findings are from ABI Research's RF Power Semiconductor Devices for Mobile Wireless Infrastructure report.

CST Global recently announced that it will be leading a UK government-funded research project to develop next generation GaN laser technology.The CoolBlue research project (or 'Quantum Cooling using Mode Controlled Blue Lasers') with academic partners Glasgow and Aston Universities, is funded through the Engineering and Physical Sciences Research Council (EPSRC).

"The CoolBlue project starts in April 2017 and will last 14 months," explains Thomas Slight, development engineer at CST Global and project lead. "CoolBlue seeks to develop next generation GaN laser technology for use in atomic-cooled, quantum sensors. Traditional laser sources have proven too complex and inefficient to produce commercially, in this application. However, direct blue laser diode sources offer increased power and simplicity, with the opportunity to miniaturise quantum sensor formats and produce them in a robust format."

Sivers IMA to acquire Scottish laser maker

SIVERS IMA, a Swedish company, has announced its acquisition of Compound Semiconductor Technologies Global, a maker of III-V compound semiconductor lasers based in Scotland.

Sivers IMA is fabless supplier and developer of microwave and millimeter wave products for advanced WiGig / 5G wireless and radio frequency, network applications. Its merger with CST Global adds direct fibre optic network products to its portfolio. These include the leading edge optical lasers used in datacentre, cloud and the 'fibre-to-the-subscriber' markets. Both companies are growing more than 45 percent, year-on-year growth.

Neil Martin, CEO of CST Global,said: "CST Global is pleased to merge with Sivers IMA group. Sivers IMA can now supply photonic, microwave and millimeter wave solutions for the rapidly expanding data centre, cloud and telecommunications markets in China, Europe and America."

Aixtron receives repeat order from Sumitomo

Deposition equipment company Aixtron has delivered a CRIUS MOCVD system with 4-inch wafer configuration to Japanese group Sumitomo Electric Device Innovations (SEDI).

SEDI wants to boost the production of GaN-on-SiC devices for RF data transfer applications including for the upcoming 5G wireless mobile network. The system has been put into operation in the fourth quarter 2016. SEDI has longstanding experience with Aixtron's Close Coupled Showerhead technology which enables easy scalability.The new reactor is equipped with optional features such as dynamic gap adjustment, ARGUS in-situ temperature control and the EpiCurve TT metrology system. The ARGUS monitoring device provides full wafer mapping in real time for optimum control of the growth process. Extended flexibility is enabled by allowing the adjustment of the process gap between the showerhead and the substrate.

SEDI already has a range of GaN HEMT devices on offer for radar, mobile phone base-stations, and general applications. These GaN-on-SiC HEMT devices enable high power amplification at operating frequencies of up to 14 GHz RF.

Fraunhofer Group and Leibniz Association to collaborate on future technology

TO REINFORCE the position of Europe's semiconductor and electronics industry within global competition, eleven institutes within the Fraunhofer Group for Microelectronics have, together with two institutes within the Leibniz Association, come up with a concept for a cross-location research factory for microelectronics and nanoelectronics.

The focus of the cross-institute work will lie on four future-relevant areas of technology: silicon-based technologies; compound semiconductors and special substrates; heterointegration; and design, testing and reliability.

The German Federal Ministry of Education and Research (BMBF) is providing support with the necessary investment. On April 6, 2017, Research Minister Johanna Wanka handed over the grant approvals – €280 million for Fraunhofer and €70 million for Leibniz.

For more than 20 years, the Fraunhofer institutes within the Group for Microelectronics and the Leibniz institutes involved have supported German industry with application-oriented research and development for high-tech products.

To be able to offer even smaller companies top technology under optimum conditions, eleven Group institutes, as well as the Leibniz Institute for Innovative Microelectronics (IHP) in Frankfurt/Oder and the Ferdinand-Braun-Institute, Leibniz Institute for Maximum-frequency Technology (FBH), in Berlin will combine their technology research into a joint, cross-location technology pool called the 'Research Fab Microelectronics Germany', and expand on it. The institutes' existing locations will be retained, while expansion and operation will be coordinated and organised in a shared business office. The aim is to be able to offer customers from large industry, small and medium enterprises, and universities the entire value chain for microelectronics and nanoelectronics in an uncomplicated manner and from a single supplier.

The establishment of the Research Fab Microelectronics Germany will be a unique offering available to the German and European semiconductor and electronics industry. The cooperation of a total of 13 research institutes and more than 2,000 scientists is already the world's largest pool for technologies and intellectual property rights within the area of smart systems. This new form of cooperation will make a major contribution to strengthening European industry's competitiveness internationally.

The Microelectronic Fab for Research Germany will represent a reorganisation of more than 2000 scientists and the necessary equipment for technological research and development under a single, virtual roof. In the medium term, the measure is expected to create an additional 500 jobs for highly qualified candidates. Within Research Fab Microelectronics Germany, FBH brings in its expertise in the development of energy-efficient semiconductor components. It researches novel materials and develops the required devices for applications like electro mobility, renewable energy, or mobile communications of the future.

The institute also develops innovate devices for the terahertz region which target, e.g., non-destructive testing and quantum technology, prospectively enabling data transfer free of eavesdropping and high-precision measurements. Moreover, FBH expands its existing cooperation with the IHP, in which both institutes combine the high output powers of InP devices with the complexity of silicon technology by offering hetero-integrated circuits.

The IHP contributes with its know-how in the field of complex silicon-based RF and photonic technologies. The new technical options of the IHP will enable the development of novel devices and capable basic technologies for highly integrated circuits, which will be applied within Research Fab Microelectronics Germany.

In addition to the research on integration possibilities of new materials systems into a silicon platform, the quick transfer of research and development results into industry-ready manufacturing processes is a main target of the cooperation. This way, applications in the field of communications, the information transfer of ever increasing data rates, or security technology based on latest research results shall be possible in a timely manner.

Osram IR LEDs provide better camera image contrast

OSRAM OPTO SEMICONDUCTORS is expanding its offering of high-power infrared LEDs for illumination solutions to include a new wavelength (810 nm) for camera systems, such as those used to read license plates.

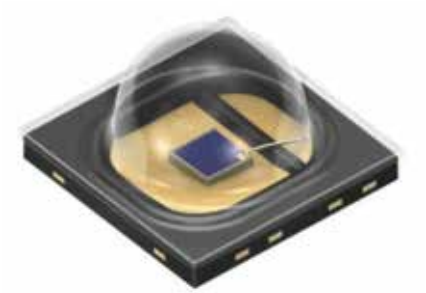
The additional wavelength can be used to improve image contrast making it easier to read patterns from recorded images, says Osram. Moreover, camera sensors have higher sensitivity at 810 nm. At the same optical output, the new device therefore extends the range of camera systems as compared to 850 nm.

Greater image contrast for easier analysis
The newly available wavelength is said to be particularly advantageous for applications requiring superior image contrast. Wavelengths of 850 nm and 940 nm typically used in today have difficulty creating high-contrast images of certain colour combinations.

Camera systems supporting automatic license plate recognition at toll stations or entrances to parking garages are a perfect example. The SFH 4703AS gives these cameras higher-contrast images for many types of license plates, making it easier to retrieve the license plate numbers. As a result, automated barriers function more smoothly, reducing waiting times for drivers. And other camera applications also stand to benefit from the new component, such as traffic monitoring and CCTV systems.

This new wavelength comes with the bonus that the spectral sensitivity of typical camera sensors is higher in this range than for 850 and 940 nm. Using a light source with the same optical output, an 810 nm system will achieve a greater detection distance than was previously possible. Alternatively, this also allows designers to reduce the number of components if they wish to maintain the same range. However, designers should bear in mind that humans do perceive infrared light as a mild red glow, and this is stronger at 810 nm than at 850 nm.

Osram Opto Semiconductors already provides 810 nm emitters for iris scanners in mobile devices. For the SFH 4703AS, developers mounted the highly



efficient chip manufactured in nanostack technology in the tried-and-tested Oslon package for illumination applications. At 1 amp current, the emitter generates 1 watts optical power. The beam angle of +-45° allows for broad illumination, with a resulting radiant intensity of 630 milliwatts per steradian (mW/sr) at 1A. The component measures 3.85 mm by 3.85 mm, and is 2.29 mm high including the lens.

With this new device, designers can now choose from mutually compatible emitters in three different wavelengths. These can be combined within a single illumination unit or used to convert existing systems to another spectral range without the need for layout changes.

Transphorm develops two new GaN power chips

POWERAMERICA has announced that thanks to its funding, California-based Transphorm has developed two new products: a bilateral switch which will enable two to four times part count reduction and loss reduction; and a 900 V GaN HEMT, which will enable increased energy efficiency.

The products are used to convert power in applications such as power supplies, solar inverters, AC-AC converters, industrial converters and electric vehicles.

Backed by $70 million from the US Department of Energy over five years, PowerAmerica is working to accelerate the adoption of advanced semiconductor components made with SiC and GaN into a wide range of products and systems.

Transphorm already has several GaN products on the market in the 650 V range, which have helped to dispel doubts about the reliability and manufacturability of GaN. Previously, though, 900 V GaN was not thought possible. While Transphorm had set a roadmap target to develop the higher node, Transphorm's partnership with Power America enabled them to focus specifically on the higher node 900 V GaN devices.

"The fact that PowerAmerica provided 50 percent of the funding for this project allowed us to focus on it as a roadmap item and develop streamlined technology – and offer first engineering samples with a datasheet – within a year," said Transphorm co-founder and COO, Primit Parikh. PowerAmerica helped to get us to the next level with our product."

Primit added: "Working with PowerAmerica, we were able to leverage our strong baseline of industry's highest reliability-highest quality GaN to improve existing technologies and get them closer to product commercialisation. PowerAmerica helped accelerate and risk reduce our roadmaps of these advanced devices."

Transphorm has preliminary samples released to select customers, and is continuing to focus on broader product release.

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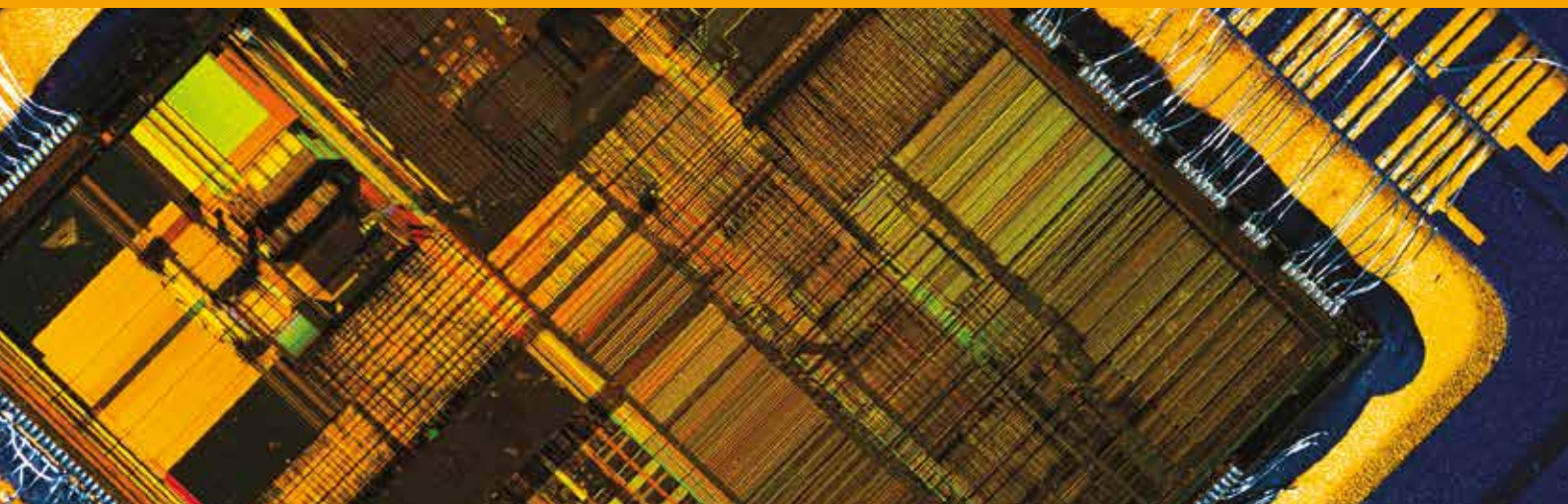


Tyndall to lead world's first photonics packaging pilot line

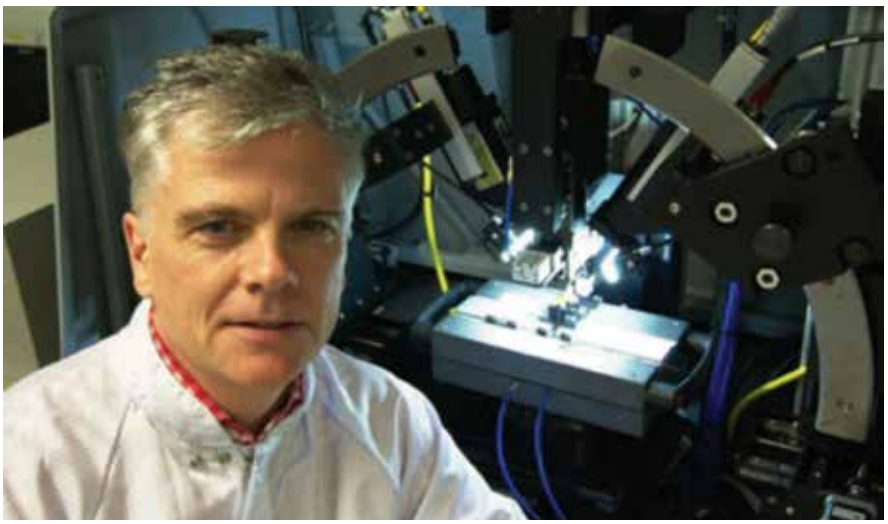
THE VALUE of the photonics market is expected to be worth over €615 billion by 2020. With Europe's share of the production technology market currently at 55 percent, the European Union, in partnership with Photonics21, Europe's premier photonics industry body, has identified photonics as a Key Enabling Technology (KET) critical for the future economic development of Europe.
To provide Europe with a state-of-the-art infrastructure, supporting the industrial development and manufacture of Photonic Integrated Circuits (PICs), the EU is investing €15.5 million in a new international consortium called PIXAPP, which will be led by Ireland's Tyndall National Institute.

Speaking from the Photonics21 AGM in Brussels, PIXAPP Pilot Line Director and Head of Photonics Packaging Research at Tyndall National Institute, Peter O'Brien (pictured below) said: "The consortium involved in PIXAPP, led by Tyndall, has an unmatched record of excellence in delivering many world 'firsts' in PICs. We will establish 'best in class' PIC packaging technologies that are cost-effective and scalable to high volume manufacture.

We will offer these technologies through a single easy access point, which we call the Pilot Line Gateway, which is located at Tyndall. Furthermore, we plan to train and educate the photonics workforce of the future by creating a unique laboratory based training programme. This programme is a game-changer not only for the European photonics industry but also global photonics."

Packaging PICs can represent up to 80 percent of the cost of photonics components so it is a critical area for the industry. PIXAPP is the world's first open access PIC assembly and packaging pilot line, combining a highly-interdisciplinary team of Europe's leading industrial and research organisations. Partners in the UK, Germany, France, Belgium, Netherlands, Finland, Italy and Czech Republic each bring their own particular expertise to provide SMEs with a unique infrastructure to help them exploit the breakthrough advantages of PIC technologies.

"In the past, it has been very expensive to manufacture high volumes of PICs, and more expensive and challenging again to package them. This is creating a bottleneck for production, which is impacting the potential for growth in the photonics industry. I am confident that Tyndall National Institute's leadership will deliver market success for Europe and drive our competitiveness across the communications, medical, automotive, energy, safety and defence sectors globally," said Jose Pozo, director of the European Photonics Industry Consortium.



AMS to acquire Princeton Optronics

AMS, an Austrian supplier of high performance sensor and analogue solutions, has signed an agreement to acquire 100 percent of the shares in VCSEL firm Princeton Optronics, in an all-cash transaction.

Headquartered in Princeton, NJ (USA) with a total of 37 employees, Princeton Optronics develops and supplies high performance VCSELs. In the mobile and consumer markets, Princeton Optronics realises benchmark power efficiency and accurate control of beam divergence to create application benefits. In automotive and industrial, Princeton Optronics' technology enables high temperature operation and delivers high power pulsed lasers and laser arrays which support future automotive and industrial applications. The use of VCSELs is expected to gain momentum in optical sensor solutions for the Human Machine Interface (HMI).

The company has an annual revenue run-rate of around $10 million and is profitable. The transaction includes an upfront consideration of $53.3 million in cash and a substantial cash earn-out consideration related to realised 2017 and 2018 revenues, with a potential maximum earn-out value of $75 million. The transaction is expected to close within six months and is subject to certain approvals and the occurrence of certain conditions defined in the agreements with the sellers.

Alexander Everke, CEO of AMS, commented on the transaction: "Adding the illumination source expands AMS' optical sensor solutions offering, with the light path optics covered by Heptagon and the light sensor including filters by AMS. "Leveraging this portfolio AMS can now design and manufacture the most complete and differentiated optical solutions for future growth areas like mobile 3D sensing and imaging or automotive autonomous driving.

IQE posts double digit growth in revenues and profits

IQE plc, a supplier of advanced wafer products and wafer services to the semiconductor industry, has announced its final results for the year ended 31 December 2016.

Financial highlights include strong financial performance with continued double digit growth in revenues and profits. Revenues were up 16 percent to £132.7 million (previous year was £114.0 million); adjusted operating profit up 17 percent to £22.1 million; and adjusted fully diluted EPS up 15 percent to 3.0p.

According to the company a diverse range of growth drivers and end markets has enabled 19 percent growth in wafer sales, reflecting organic growth in all markets, supplemented by a currency tailwind in H2. Photonics revenues up 43 percent to £22.8 million; wireless revenues up 15 percent to £91.3 million; infraRed revenues up 19 percent to £10.6 million; US dollar strengthened 11 percent against sterling in H2 following Brexit vote in June License income was £6.7m higher than expected, but lower than prior year (£8.0m) which included a significant element of upfront income. Key milestones delivered on several major photonics programmes during H2 2016, providing significant growth opportunities for 2017 and beyond, according to the company. Progress with new cREO technology, for example, has delivered some early wins, including delivering a step change in GaN on Silicon technology (the elimination of 'parasitic channel'), and engagement in development programmes for advanced RF filter applications;

In addition, IQE's successes include: a key customer engaged in end market qualification using the company's GaN on Silicon, signifying that this technology is close to commercialisation." And then start a paragraph. "According to IQE, positive market dynamics are at play, including increasing M&A and sector investment, reflecting the increasing focus on compound semiconductors as a critical enabling technology to major growth themes, including high speed communication, the internet of things, big data, advanced medical technology, energy efficiency, and autonomous vehicles.

IQE's Joint Ventures in the UK and Singapore mark key milestones in their development as centres of excellence in driving innovation and commercialisation of advanced CS technologies. The UK Joint Venture was a catalyst to securing around £300 million of funding towards the continued development of a UK CS Cluster, and the Singapore JV has been selected as a partner in a major programme for CS on silicon technology. Drew Nelson, IQE CEO, said: "IQE delivered a strong set of results in 2016, with revenues up 16 percent, PBT up 17 percent, and EPS up 15 percent. The continuing growth in revenues, profits and cash generation is being enabled by the Group's portfolio of cutting edge intellectual property, and is being delivered through a diverse range of growth engines.

"Revenues were up in all key markets: wireless, photonics and InfraRed. Photonics continues to be the star of the show with 43 percent year on year growth in sales. This is being driven by VCSEL and InP technologies which enable a broad range of applications from fibre optic communication, to advanced sensors, and industrial processes. "The depth and breadth of photonics development programmes and customer qualifications provide a solid platform for continued strong growth over the coming years. "InfraRed sales were up 19 percent with several notable contracts wins during 2016. Our largest division, Wireless, performed well, with revenues up 15 percent. "Our focus on building a strong IP portfolio reflects our vision of global leadership across a range of markets as advanced semiconductor materials become an increasingly important enabler of a wide range of electronics applications. This strategy underpins strong financial performance, and the exciting outlook we see for our business."

Seoul Semiconductor files patent lawsuit in Germany

SEOUL SEMICONDUCTOR has filed a patent infringement lawsuit in Germany in the District Court of Düsseldorf against Mouser Electronics, an electronic components distributor, asserting infringement of an LED patent.

According to the complaint, the accused products include LEDs for high-power light emission. Further investigation suggests that the accused products from Mouser are manufactured by multiple LED companies, including Everlight Electronics, a top-10 LED maker.

In the lawsuit, Seoul has sought a permanent injunction, damages, and recall and destruction of the allegedly infringing products.

The asserted patented technology serves to efficiently extract light emitted from the internal LED structure by treating LED chip surfaces, thereby significantly improving light intensity and brightness. This patented technology has been widely used for various high-power LED applications, such as automobile lighting, cell phone flashlights, outdoor lighting, UV LED appliances, and others.

According to market research firm IHS, the LED penetration rate in automobile headlamps is expected to increase sharply to 32.3 percent by 2021 from the current penetration rate of

16.4 percent. This high-power LED technology is already being used for exterior automobile lighting including headlights and daytime running lights.

Furthermore, it is expected to become a significant technology for electric vehicles and autonomous vehicles, which require high-power LED lighting with high heat dissipation for energy efficiency.

In addition, this high-power LED technology also applies to LEDs for mobile phone flashlights, which require higher light intensity. Because margins for flashlight LEDs are higher than those for backlights, the flashlights LED market has still grown steadily despite the overall decline in the IT sector LED market.

Further, this high-power LED technology is widely applicable to general lighting products for outdooring illumination and commercial or industrial uses because such technology substantially enhances light efficiency and improves the brightness per unit area obtained from the LED. The technology is also widely used in manufacturing UV LEDs for sterilization, purification and curing processes. The UV LED application market is expected to grow rapidly, reaching $800 million by 2020.

Beginning with this lawsuit, Seoul plans to actively defend its patent assets against infringing high-power LED technologies. Seoul has already identified infringements of other patents it possesses that relate to high-power LEDs and will be considering additional infringement lawsuits.

Ki-bum Nam, VP of the Lighting Business Department at Seoul Semiconductor, said: “The asserted patent is considered an essential technology for manufacturing high-power LEDs and has been widely used in various LED applications.”

Nam added: “However, there are many LED products currently on the market that infringe this patented technology, so we have decided to begin enforcing our patent rights in such cases. To create a fair market competition and promote technological innovation, we continuously take all actions necessary to deter such infringement and protect our intellectual property.”

Riber posts strong improvement in 2016 earnings

MBE equipment company Riber is releasing its full-year earnings for 2016, showing a strong growth in business. Full-year revenues for 2016 climbed 29 percent from 2015 to €16.5 million, with growth driven by all product lines and accompanied by a significant upturn on various industrial markets.

The gross margin came to €6.0 million, representing 36.4 percent of revenues, up from 14.9 percent in 2015. This turnaround reflects the improvement in sales margins, benefiting from a better product mix, which has also led to €0.6 million of provisions for inventories being reversed. Operating income totalled €1.1 million, following a reduction in operating expenditure to €7.1 million in 2016, down from €8.3 million in 2015, resulting from a positive change in other operating income and expenses, while sales, administrative and R&D costs remain virtually unchanged.

R&D efforts have been maintained to develop RIBER’s range of products and services for its customers. Consolidated net income shows a significant year-on-year improvement, with a loss of €1.1 million, versus €6.3 million in 2015.

Cash, net of financial debt, is up to €2.5 million at December 31, 2016, compared with €0.1 million at end-2015. It improved by €1.7 million during the second half of the year, following the capital increase carried out in August 2016 and order down payment received at the end of the year. In addition, the company repaid all its financial debt for €0.7 million and its shareholders’ equity represented €15.5 million at December 31, 2016. Outlook for 2017.

In view of the order book at December 31, 2016, the orders received since the start of the year and the outlook for orders to be delivered in 2017, Riber is confirming its forecast for revenue growth of at least 30 percent compared with 2016.

US missile defence agency taps Raytheon for GaN upgrade

THE US Missile Defence Agency has awarded Raytheon a $10 million contract modification to continue the development of hardware and software that will add GaN semiconductor technology to the AN/TPY-2 ballistic missile defence radar.

GaN increases the radar's range, search capabilities and enables the system to better discriminate between threats and non-threats. GaN technology also increases the system's overall reliability while maintaining production and operational costs, according to the company.

"AN/TPY-2 is already the world's most capable land-based, X-band, ballistic missile defence radar," said Raytheon's Dave Gulla, vice president of the Integrated Defence Systems Mission Systems and Sensors business area. "Adding GaN technology modernises the system so it can defeat all classes of ballistic missiles in extreme operational environments."

The AN/TPY-2 is on pace to be the world's first transportable, land-based ballistic missile defence radar to use GaN technology. The AN/TPY-2 radar operates in two modes: In forward-based mode, the radar is positioned near hostile territory, and detects, tracks and discriminates ballistic missiles shortly after they are launched; In terminal mode, the radar detects, acquires, tracks and discriminates ballistic missiles as they descend to their target. The terminal mode AN/TPY-2 is the fire control radar for the Terminal High Altitude Area Defence ballistic missile defence system, by guiding the THAAD missile to intercept a threat.

Raytheon has been developing GaN for 19 years and has invested more than $200 million to get this latest technology into the hands of military members faster and at lower cost and risk.

Everlight opens automotive factory in Taiwan

LED company Everlight Electronics has opened a new factory in Taiwan dedicated to automotive products. The Miaoli Tongluo New Factory is the result of investments of more than $300 million.

Everlight started to expand its automotive activities in 2014. Today, the company owns a comprehensive portfolio of automotive products for interior/exterior vehicle applications. All products are sulphur-resistant and passed the corrosive gases test for H_2S, SO_2, CL_2 and NO_2, etc, according to the company. Thus the caveats against LED products which failed the sulphur-resistance test, in terms of brightness, colour coordinates, voltage and function failure, etc, can be effectively reduced.

The factory combines human factor engineering and automation AOI that clearly divide warehousing and production. This concept takes care of the connection routes between upstairs and downstairs at the same time. RFID (Radio Frequency Identification) was introduced to aid the MES (manufacturing execution system) in process control. All products will be engraved with as laser code before die bonding, for the convenience of tracking the in-process and post-process status of the product.

Aixtron posts highest first quarter revenues since 2011

AIXTRON has announced its financial results for Q1 2017 with total revenues increased to €53.6m (Q1/2016: €21.4m; Q4/2016: €89.8m). This figure represents the highest Q1 revenues since 2011.

Order intake in Q1/2017 came to €61.9m, 39 percent higher than in the previous year (Q1/2016: €44.4m; Q4/2016: €60.5m). This was due to consistently high demand of equipment for LED, telecom and optoelectronic applications, according to the company.

As of March 31, 2017, the equipment order backlog totalled €87.6m, a 12 percent increase on the figure of €78.1m at the beginning of the year (March 31, 2016: €67.7m).

Cash and cash equivalents (including cash deposits with a maturity of more than 90 days) increased to €193.6m as of March 31, 2017, as against €160.1m as of December 31, 2016.

As in previous quarters, the key driver for the development in revenues and order intake was demand for production systems for specialty LED, telecom and optoelectronics, as well as for memory applications. This in turn was mainly attributable to emerging technology trends, such as big data, cloud computing, electro mobility, and the upcoming 5G mobile communication standard.

First measures to focus R&D spending for the development of future technologies, were freezing the product development for III-V-materials for future generation logic chips (TFOS).

Cost of sales for Q1/2017 increased to €40.0m year-on-year, equivalent to 75 percent of revenues (Q1/2016: €18.3m, or 85 percent of revenues; Q4/2016: €60.5m or 67 percent of revenues). This was a reflection of the corresponding revenue levels as well as low margin AIX R6 sales from inventory and a write down of €1.0m related to the TFOS activities during Q1/2017. Gross profit and gross margin in Q1/2017 improved to €13.6m and 25 percent respectively against the previous year but fell on a quarterly comparison (Q1/2016: €3.1m, 15 percent gross margin; Q4/2016: €29.4m, 33 percent gross margin) mainly due to above mentioned reasons.

Operating expenses in Q1/2017 increased to €26.4m (Q1/2016: €17.8m; Q4/2016: €21.4m). This was mainly due to higher R&D expenses which included a €5.6m write down of assets related to Aixtron's TFOS activities.

"Aixtron has a wide portfolio of enabling technologies for highly diversified applications and industries. To better focus R&D costs for the development of future technologies, we will group our portfolio for future technologies and transfer it into clearly defined independent units to be financed with respective technology partners", comments Kim Schindelhauer, CEO of Aixtron SE.

"In a first step to focus our research and deevelopment expenses in the future, we wrote down assets totaling €6.6m resulting from freezing our product development for III-V-Materials for future generation logic chips (TFOS). We will not spend further R&D until a firm timeline for the introduction of this material application has been set and a partner covers the required developments costs. Then, we are fully committed to support our customers to introduce TFOS materials to the market."

The revenue development in the first three months of 2017 was supported by the solid order backlog at the end of 2016. The comparatively high order intake in Q1/2017 supports managements' expectation on the development of revenues and order intake during 2017.

Consequently, management reiterates the full year 2017 guidance given in February 2017 with an order intake and revenues between €180 and 210 million.

VTT shows in-moulded LED roll-to-roll process

VTT Technical Research Centre of Finland has performed all manufacturing stages for a flexible in-moulded LED foil in a roll-to-roll process. The purpose of this demo is to prove the suitability of the technique for the highly cost-effective manufacture of products such as flexible LED displays containing printed electronics.

A demo was presented at the LOPEC fair for printed electronics in Munich, Germany. All smart electronics in products such as wrist-wearable computers are on a rigid board under the face of the watch. The roll-to-roll technique enables electronics to be printed on a plastic or elastomeric foil, which has various benefits such as thinness, lightness, elasticity and transparency.

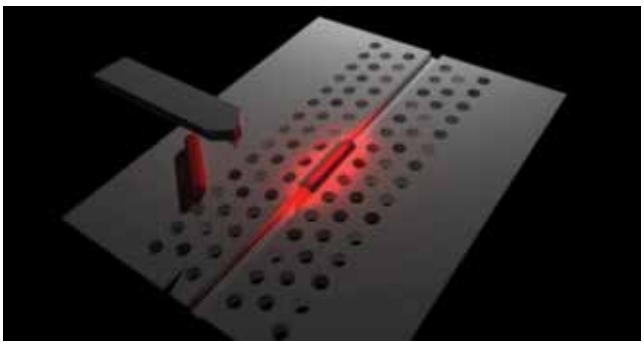
In hybrid-integrated systems, separate components are mounted on a printed electronic foil, after which the foil can be overmolded with thermoplastic or thermoplastic elastomer, using the injection moulding process.

"For the wristband demo, we performed all the key manufacturing stages for printed hybrid systems – the printing of conductors, the assembly of semiconductor LEDs and the overmolding – using the roll-to-roll technique. This enables the mass manufacture of small-sized, easy-to-use, flexible electronics in a cost-effective manner," says Sami Ihme, senior scientist.

In practice, the roll-to-roll overmolding of a printed electronic foil involves feeding a LED foil with a foilfeeder into a mould, in which the overmolding is done. This technique is normally used to decorate plastic for various consumer products. However, the manufacture of flexible electronics – in place of graphics – involves feeding electronics with a range of electrical and optical features into a mould.

NTT team advances photonics integration

PHOTONIC INTEGRATION is still in its infancy. One of the most serious obstacles it faces is the need to use a variety of materials to achieve different functions, many of which aren't compatible with silicon integration technology.



Attempts so far to place a variety of functional nanowires within photonic circuits to reach desired functionalities have shown that, while entirely possible, nanowires tend to be too small to effectively confine light. While bigger nanowires can improve the light confinement and performance, it increases both energy consumption and device footprint - both of which are considered 'fatal' when it comes to integration.

Addressing this problem, a group of NTT Corp. researchers in Japan came up with an approach that involves combining a sub-wavelength InAsP/InP nanowire with a photonic crystal platform, which they report this week in their paper 'Continuous-wave operation and 10-Gb/s direct modulation on InAsP/InP sub-wavelength nanowire laser on silicone photonic crystal' which was published in the journal *APL Photonics*.

Photonic crystals – artificial structures whose refractive index is periodically modulated – are at the heart of their work. "A small local refractive index modulation of a photonic crystal produces strong light confinement that leads to ultrahigh-quality optical nanoresonators," said Masaya Notomi, a senior distinguished scientist for NTT Basic Research Laboratories. "We make full use of this particular feature in our work."

Back in 2014, this same group demonstrated that it was possible to strongly confine light in a sub-wavelength nanowire with a diameter of 100 nm by placing it on a silicon photonic crystal.

At that time, "it was a preliminary demonstration of the confinement mechanism, but with our present work we've successfully demonstrated sub-wavelength nanowire device operation on a silicon platform by using this method," Notomi said. In other words: While a sub-wavelength nanowire can't become a resonator with strong light confinement on its own, when placed on a photonic crystal it causes the refractive index modulation needed to generate the light confinement.

"For our work, we carefully prepare a III-V semiconductor nanowire with sufficiently large optical gain and place it within a slot of a silicon photonic crystal by using the 'nanoprobe manipulation technique,' which results in an optical nanoresonator," said Masato Takiguchi, the paper's lead author and a researcher working within Notomi's group at NTT Basic Research Laboratories. "With a series of careful characterizations, we've demonstrated that this sub-wavelength nanowire can exhibit continuous-wave lasing oscillation and high-speed signal modulation at 10 Gbps."

To use nanowire lasers for photonic integration, three essential requirements must be met. "First, a nanowire should be as small as possible for sufficiently strong light confinement, which ensures an ultrasmall footprint and energy consumption," Takiguchi said. "Second, a nanowire laser must be able to generate high-speed signals. Third, the lasing wavelength should be longer than 1.2 microns to avoid absorption in silicon, so it's important to create sub-wavelength nanowire lasers at optical communication wavelengths – 1.3 to 1.55 microns – capable of high-speed signal modulation."

In fact, previous demonstrations of nanowire-based lasers "have all been at wavelengths shorter than 0.9 microns, which can't be used for silicon photonic integrated circuits - except a pulsed lasing demonstration of relatively thick micron-wire lasers at 1.55 microns," Notomi said. This is presumably because the material gain is smaller at longer wavelengths, which makes it difficult for thin nanowires to achieve lasing. Beyond this, "zero demonstrations of high-speed modulation by any types of nanowires have materialized," he noted. This is also due to the small gain volume. "With our present work, we've solved these problems by combining a nanowire and a silicon photonic crystal," Notomi said. "Our result is the first demonstration of continuous-wave lasing oscillation by a sub-wavelength nanowire, as well as the first demonstration of high-speed signal modulation by a nanowire laser."

The group could achieve 10-Gbps modulation, which is comparable to conventional, directly modulated high-speed lasers used for optical communications. "This proves that nanowire lasers show promise for information processing - especially photonic integrated circuits," Notomi said. The most promising application for the group's present work is nanowire-based photonic integration circuits, for which they'll use various nanowires to achieve different functionalities - such as lasers, photodetectors, and switches in silicon photonic integrated circuits.

"It's expected that processors equipped with an on-chip photonic network will be needed within about 15 years, and nanowire-based photonic integration will be one possible solution," Notomi said. In terms of lasers, the group's next target is to integrate nanowire lasers with input/output waveguides.

"Although this type of integration has been a difficult task for nanowire-based devices, we expect it will be much easier in our platform because the photonic crystal platform is intrinsically superior in terms of the waveguide connection," Takiguchi said. "We'll aim for room temperature current-driven lasing as well."

The group also plans to use the same technique to create "photonic devices other than lasers by choosing different nanowires," Takiguchi said. "We want to demonstrate that we're able to integrate several photonic devices by having different functionalities on a single chip."

Cree announces joint venture with Sanan Optoelectronics

CREE is forming a joint venture – Cree Venture LED Company – with the Chinese firm Sanan Optoelectronics to produce and deliver high-performing, mid-power lighting class LED packaged products.

The exclusive arrangement will serve expanding markets of North and South America, Europe and Japan, and serve China and the rest of the world on a non-exclusive basis.

Using Cree's portfolio of patents and global sales channels, this joint venture will bring to market a broad portfolio of high-performance mid-power products to serve the fast growing, $4 billion global mid-power LED market. With this agreement, Cree says its LED business is now able to serve the broader needs of the general illumination (indoor and outdoor lighting), horticultural and other evolving LED markets.

"This joint venture builds on both companies' leading product and channel capabilities to give Cree the ability to provide our LED customers a complete range of high-power and mid-power LED products to serve a broad range of markets and applications," said Chuck Swoboda, Cree president and CEO. "The addition of the mid-power LED products in this new joint venture to Cree's industry-leading high-power products gives us an unparalleled LED portfolio," stated Dave Emerson, Cree LEDs senior vice president and general manager. "With our LED systems expertise, customers are able to work with our existing channels to find the best LEDs for their applications."

Located in Hong Kong, Cree Venture LED Company, will be led by TK Ong, general manager, who brings to the joint venture extensive experience in the LED market, and will be governed by a board of directors with members from both companies. Cree will own 51 percent of the joint venture, and Sanan will own 49 percent of the joint venture.

Cree and Sa'an will be working in the coming months to incorporate, fund and commence operations of the joint venture, and are targeting initial product sales by the joint venture in the third calendar quarter of 2017. Cree will receive royalties from the joint venture on its patent portfolio.

Monocrystal develop wafers for microLEDs

SYNTHETIC sapphire firm Monocrystal has released a new range of 'Ultra-Clean' sapphire wafers, which it says achieve a breakthrough in wafer surface quality required by high-precision optoelectronic applications such as microLEDs. A microLED is the next generation light source, that has advantages over a conventional LED in terms of brightness and power consumption. Monocrystal's Ultra-Clean (UC) sapphire wafers have only 20-50 particles of no more than 1 μm in size on their surface; they are specially designed for microLED production.

"MicroLED is a very promising technology which requires a new approach in many aspects, including sapphire wafer surface preparation. Our UC-wafers with a very low particle count will allow our customers to achieve their target epitaxial yields, which is crucial for microLED successful development and further commercialisation," Monocrystal's CEO Oleg Kachalov commented.

"Our new UC-wafers are also compatible with the conventional PSS process. It is an advanced cost-saving solution, which eliminates the pre-cleaning step and allows PSS-makers to increase their yields up to 95-99 percent after the first pass. We have already received a very positive feedback on the UC-wafers from several long-term customers. We are encouraged to further develop sapphire processing and cleaning technologies to assist customers in achieving advantages on the market," added Monocrystal's VP sales Mikhail Berest.

Passive GaN mixers reach new benchmark of linearity

FOR DECADES, GaAs has been the process of choice for passive mixers fabricated on MMIC technologies. However, in terms of linearity, GaAs mixers tend to have input third-order intercept (IP3) points that reach +20 to +24 dBm, which is typically only 3 to 8 dB above the applied LO drive.

This level of 'linear efficiency', which is newly defined as the difference between IP3 and LO drive level, is one reason higher IP3 has generally been unachievable in GaAs.

Over the past year, mixer experts at Custom MMIC have been exploring the use of GaN processes as the basis for extremely linear RF mixers to break through this linearity 'stalemate'.

Deducing that the high linearity performance of GaN power amplifiers may cross-over to other critical microwave components, Custom MMIC engineers have gone through several iterations of GaN mixer technologies and typologies with several of their key foundry partners.

Ultimately, the fruits of their efforts have led to passive GaN mixer designs that surpass all GaAs passive mixer designs in terms of the ratio of input third-order intercept point (IIP3) to local oscillator (LO) drive - a figure-of-merit Custom MMIC is coining as Linear Efficiency.

From S-band to K-band (2 GHz to 19 GHz) these new passive GaN mixers are demonstrating IIP3 figures well above 30dBm, LO drive levels around 20 dBm, and linear efficiencies above 10dB.

Gallium oxide:
Taking on GaN and SiC

Follow massive investor funds, Flosfia is poised to deliver high performance, affordable gallium oxide devices, reports Rebecca Pool.

In early March Kyoto University start-up Flosfia revealed that it had won an incredible JPY 750 million – £5.4 million – in finance to commercialise corundum structured gallium oxide Schottky barrier diodes and MOSFETs.

With the ample funds coming from investors old and new – including Yaskawa Electric, Future Venture Capital, Energy & Environment Investment and more – Flosfia will now develop its own production lines, with a view to launching commercial production in 2018.

"We have existing, new and strategic investors in this round of funding, which is a great sign for our technology and reflects that we are moving forward," highlights Takuto Igawa, vice president of marketing at Flosfia.

"Yaskawa is one of the biggest industrial global businesses in the world and they have joined us as an investor and also a user of our devices."

Flosfia was founded in March 2011, by Kyoto University researchers Toshimi Hitora, Shizuo Fujita and Kentaro Kaneko to commercialise a CVD process called 'Mist Epitaxy'. It is a novel growth method for depositing layers of gallium oxide onto sapphire substrates. Ultimately, it enables the fabrication of Ga_2O_3 power devices.

Ga_2O_3 comes in five different phases, with its α-phase taking the same corundum crystal structure as Al_2O_3 or sapphire, opening the door to stress-free epitaxy of Ga_2O_3 layers on sapphire substrates.

Indeed, as early as 2008, Flosfia co-founder and technology pioneer, Professor Shizuo Fujita, successfully deposited thin films of α-Ga_2O_3 onto sapphire substrates. And today, the refined growth process produces dislocation-free epilayers on four inch sapphire substrates, a critical step towards reaching cost-parity with the industry incumbent, silicon.

Fujita and colleagues at Flosfia have also developed a 'lift-off' proprietary process to transfer the α-Ga_2O_3 layers from the sapphire substrate to a high thermal conductivity metal support, alleviating the thermal management issues that plague SiC and GaN power devices.

The researchers claim that the process has been honed for the high throughput and easy-handling of wafers. And as Flosfia external director, Naonori Kurokawa highlights: "Using the sapphire substrate is much much cheaper than using SiC".

From a device point of view, Ga_2O_3 has a Baliga figure of merit some 20 times higher than SiC and bandgap of around 5 eV. As a result, these ceramic oxide devices can achieve higher operating voltages and lower on-resistances than SiC and GaN equivalents, as Flosfia demonstrated with its first Schottky barrier diode (SBD) in 2015. The 521 V device had an on-resistance of just 0.1 mΩ cm^2, lower than that of any commercially-available SiC diode.

"We're are only a six-year-old start-up but we have already beaten the on-resistance world record," says Kurokawa. "What's more our 600 V, 5 A device is almost ready. Development in the last couple of years has been huge."

Towards commercialisation

Right now, Flosfia is sampling SBDs in industry standard TO-220 packages with its industrial partner, Japan-based robotics manufacturer, Yaskawa Electric, with a view to delivering commercial devices in 2018.

"Based on our sample tests we will soon determine the final product specification," says Igawa. "Our 600 V, 5 A device will be coming very soon."

The company also aims to sample MOSFETs in 2019, taking these to commercial production from 2020. "We will target markets all over the world, and our first product, the 600 V, 5 A diode, will be used for power factor correction," says Igawa.

As device development and performance continues apace, Flosfia still has to deliver on one key factor; cost. From the outset, the company stated it would deliver devices at a cost to match the silicon equivalent, and according to Flosfia president, Toshimi Hitora, this is coming.

"We are still in our research and development phase, so we can't confirm costs yet, but come mass production of our Schottky barrier diodes in 2018, I know we will reach cost-parity with GaN and SiC devices," he says. "We then intend to reach cost-parity with silicon in 2019."

"Mist-epitaxy is a safe, low-cost and energy-saving technology for growing oxide semiconductors to suppress device cost so power devices can become ubiquitous," he adds.

Flosfia Chief Executive, Toshimi Hitora, is ready to take Ga_2O_3 Schottky barrier diodes and MOSFETs to market.

Kaiam eyes datacentre growth

As datacentre traffic soars, US photonic integrated circuit pioneer, Kaiam, buys a second UK facility to track growing markets, reports Rebecca Pool.

THIS MARCH US-based photonic integrated circuit pioneer, Kaiam, revealed that it had agreed to buy the manufacturing facilities of Compound Photonics in Newton Aycliffe, UK.

The move provides much needed manufacturing space for Kaiam's growing lines of optical transceivers. However, the new facility also delivers an extensive cleanroom, with 3- and 6-inch wafer lines, for processing III-V devices, including pHEMTs, HBTs, photodetectors and lasers.

"The Newton Aycliffe site is a world-class facility in both capabilities and scale for producing III-V devices," highlights Kaiam chief executive, Bardia Pezeshki. "With this we now have everything we need to be the leading manufacturer of future optical transceivers."

Kaiam was founded in 2010, with the goal of commercialising a MEMS-based platform to assemble photonic integrated circuits. Here, the MEMS platform acts as a substrate for individual optical components. Micro-lenses and solder balls are attached to the platform at locations where optical coupling is required. Optical components, such as InP lasers and modulators, are first loosely mounted onto this platform using conventional assembly tools, and then each micro-lens is automatically oriented via MEMS to optimise alignment.

In this way, the entire assembly can be precisely aligned to meet the tight tolerances demanded by the optical communications industry for applications such as optical transceivers.

Following several rounds of funding and successful transceiver demonstrations, Kaiam acquired the Scotland-based facilities of its silicon-based planar lightwave circuit (PLC) supplier, Gemfire, in 2013. Kaiam quickly established silica-on-silicon lines at the facility and started manufacturing its 'SCOTS' – Silicon Carrier for Optical Terabit Systems – PLCs.

Crucially, vertical integration meant the company could combine integrated optical components fabrication with its MEMS-based platform and swiftly ship 40G and 100G transceivers demanded by the likes of Amazon, Facebook, Microsoft and Google for datacentres.

MOCVD reactor for III-V materials growth: Kaiam will use the instrument to develop and manufacture InP PICs.

Fast forward four years and the demand for bandwidth from datacentres continues to grow. As Pezeshki highlights: "There is so much more machine-to-machine traffic now, which means the demand for bandwidth within the datacentre is enormous."

And as the chief executive adds, four years ago' industry optical communication speeds leapt from 10 Gbit/s to 40 Gbit/s. "We rode that wave and that fueled growth," he says. "So now we are moving from 40 Gbit/s to 100 Gbit/s, and we're making 100G transceivers out of Livingston [Scotland]."

But Livingston is out of space. Clearly Kaiam's precision approach has met with success and as the demand for datacentre transceivers soars, so the company needs to keep pace; cue Newton Aycliffe. As Pezeshki says: "Our existing manufacturing facility in Livingston is full so the Newton Aycliffe facility provides us with the space we need to expand into almost immediately."

MEMS platform: Kaiam's cutting-edge optical transceivers will soon be ready to ship from new UK manufacturing facilities.

The company will first start to manufacture PLCs and package optical transceivers at the new facility. But in the coming years, the facility, with its fully operational III-V wafer fab, is set to offer so much more.

"The acquisition not only allows us to ramp product in the short term but gives us access to advanced integrated InP PICs at low cost, that we will need in the long term," says Pezeshki.

Right now the company buys in individual InP laser chips, and packages the devices with its integrated optics to deliver transceivers. But as Pezeshki points out, transceiver complexity is set to rise.

"So rather than packaging individual, directly modulated lasers, it would make sense to integrate InP lasers with modulators and potentially other components and form PICs with multiple functions on a single photonic integrated circuit." he says. "Multiple InP PICs, each at a different wavelength, would form more complex assemblies."

"We could fabricate these single chips in the Newton Aycliffe fab and then combine these with our silica waveguides," he adds. What's more, the future could be sooner rather than later. Pezeshki reckons that in around two years, his company will begin to deliver InP photonic integrated circuits.

And as he points out, the optical transceiver platforms for future 400G markets will need much more complex lasers.

"Our plan is not to manufacture direct modulated lasers as we can already buy those in. Instead, we intend to build more sophisticated InP PICs that you generally can't buy."

But for existing Compound Photonics employees at Newton Aycliffe, the acquisition also means 'business as usual'. The facility will continue to churn out GaAs transistors, with any spare capacity on the III-V line being used to fabricate Kaiam's silica-on-silicon PLCs.

"GaAs device fabrication is completely new to us, but it helps to pay the bills," says Pezeshki. "Other companies such as Skyworks and WIN Semiconductors are profitably making GaAs pHEMTs, so it is possible we could expand this business and generate more cash."

But in the meantime, the California-based company is focused on ramping up transceiver production at Newton Aycliffe. "With this acquisition we've got the factory, the equipment and a top-notch engineering team," highlights Pezeshki. "This is such a great deal, and the timing couldn't be better."

CS industry awards 2017

WINNER

IBM

INNOVATION AWARD

ENTRY: Hybrid InGaAs/SiGe CMOS Circuits

SCIENTISTS at IBM Research GmbH achieved the first demonstration of an InGaAs/SiGe CMOS technology on Si substrate using processes suitable for high-volume manufacturing on 300 mm wafers. InGaAs/SiGe hybrid integration is the main path to enable further improvement of power/performance trade off metrics for digital technologies beyond the 7 nm node. Based on selective epitaxy their approach yielded functional inverters and dense arrays of 6T-SRAMs the basic blocks of digital CMOS circuits.

This work, first of a kind,was previously presented at a recent VLSI Technology conference. It concludes a series of key demonstrations for InGaAs/SiGe CMOS reported in multiple contributions and highlights for the last four years at IEDM meetings and VLSI Technology Symposia. Since many years the technological bottleneck is to demonstrate a path that enable simultaneously the growth of defect-free InGaAs the fabrication of high performance InGaAs field effect transistors "on-insulator" and their co-processing with SiGe devices all on a silicon substrate. A few approaches have been proposed but the work nominated is the only one that reports basic building blocks of digital circuits at relevant dimensions and achieves a major milestone towards a manufacturable hybrid InGaAs/SiGe CMOS technology. It features in a single technology the selective growth of high quality InGaAs-on-Insulator regions, and the fabrication of InGaAs finFETs with physical gate length L_g = 35 nm and good device characteristics and the processing of functional 6T-SRAM cells with a cell area ≈0.4mμ².

All metrics compare favourably to industrial state-of-the-art numbers (e.g. ≈0.1μm² for an SRAM cells in 22 nm technology). It clearly highlights the potential of the nominated work as the method of choice to co-integrate InGaAs and SiGe MOSFETs for advanced CMOS technology. It also opens the door towards future low cost RF or photonic circuits based on a similar hybrid III-V silicon technologies.

Dr. Veeresh Deshpande displays his Innovation Award

Industry comment

"High-mobility channels made from III-Vs and SiGe hold great promise for addressing the looming power bottleneck in CMOS. Integrating these materials is challenging, and IBM's approach holds much promise."

CSindustry awards 2017

WINNER

OXFORD INSTRUMENTS

The Business of Science®

HIGH-VOLUME MANUFACTURING AWARD

ENTRY: PlasmaPro100 Polaris Etch System

LAST YEAR Oxford Instruments announced the development of a SiC via plasma etch process using its PlasmaPro100 Polaris system.

SiC is becoming an increasingly important material, particularly for high performance GaN RF devices using SiC as a substrate. A smooth via etch through the SiC is essential to the functioning of these devices.

Capabilities of Oxford Instruments' SiC via process include high SiC etch rate enabling maximum throughput; smooth sidewalls for problem free post etch metallisation; and high selectivity to underlying GaN layer giving a smooth, low damage stop onto the GaN device layers.

Other features include clamping of sapphire carriers using Oxford Instruments' unique patented Electrostatic Clamp technology ensuring good sample temperature control and maximum yield; the capability of etching SiC and GaN in the same tool through advanced plasma source technology; and high utilisation provided by long Mean Time Between Cleans (MTBC).

Industry comment
"Uniform, fast etching of SiC is crucial to the future of high-performance GaN devices. Addressing this need is Oxford's PlasmaPro100 Polaris Etch System."

Dr Mark Dineen (left) and Mike Steel receive the award for Oxford Instruments

CSindustry awards2017

WINNER

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Marena Achenbach, Business Development for Element 6, recieves the Substrates and Materials Award from Richard Stevenson Editor of Compound Semiconductor

SUBSTRATES AND MATERIALS AWARD

ENTRY: Element Six TM200

ELEMENT SIX's TM200 is the highest thermal conductivity bulk heat spreader material available in the market with room temperature thermal conductivity >2000 W/mK (more than 5x copper or 10x other commonly used ceramic materials).

Element Six has developed specialized chemical vapor deposition (CVD) processes to produce free standing diamond substrates that deliver this market's leading thermal conductivity. Designed to enable extreme performance thermal packaging for use in high power, or high power density devices, TM200 enables increased power and reliability and reduced system size.

Element Six's TM200 is a top tier grade of CVD diamond thermal material. In achieving the properties discussed previously, as well as extreme isotropy in thermal conductivity ($k_{crossplane}/k_{inplane}$~1.0), the synthesis was tuned to satisfy such technical and commercial criteria:

All aspects of transport phenomena, chemistry and electromagnetic affects that can have significant impact on the figures of merit of any CVD diamond process which are: Repeatability of process; Volume growth consistent with cost/performance metrics; Thickness uniformity; Process stability to achieve a total of diamond thickness greater than 3 μm; High average bulk thermal conductivity (Quality of growth); Scalability, meaning each stage can in principal be reproduced, measured and controlled while the increasing the throughput and/or growth area, Consistent nucleation and seeding methodology.

Synthesizing CVD diamond covers only half the engineering technology to manufacture the TM200. Post-synthesis processing covers the other half. Through novel techniques and advanced engineering practices, Element Six fabricates the TM200 with exceptional dimensional tolerances, for instance specifications: Planar dimensional tolerance = -0.0/+0.1mm; Thickness tolerance = ±0.050 mm; Polished Surfaces: R_a < 10 nm; No more than ± 10 nm variation of R_a (over 25 mm diameter); Flatness < 0.010 mm (over 25 mm diameter)

All the above has been incorporated in a platform that delivers more than 2000 W/mK thermal conductivity with 10^{12} Ω-cm bulk and 10^{10} Ω-cm surface resistivity; a truly great feat in engineering product development. This advanced grade of CVD diamond thermal material offers developers of high power, or high power density devices a thermal solution which can successfully operate within extreme performance environments. The TM200's combination of properties, such as high thermal conductivity, electrical insulation, low density and chemical inertness has been designed specifically for advanced thermal management packaging applications.

Industry comment
"Substrates often hold back the performance of GaN RF devices. Removing this limitation is Element Six's diamond."

CS industry awards 2017

WINNER

qorvo all around you

DEVICE DESIGN AND PACKAGING AWARD

ENTRY: RF Fusion Portfolio

MAKERS of flagship smartphones seek to squeeze the highest levels of functionality and performance into ultra-slim handsets. Because these high-end phones are designed for global or super-regional use they also need to integrate support for many different regional LTE bands as well as multiple carrier aggregation (CA) band combinations.

The RF Fusion portfolio of solutions from Qorvo contains multiple high-performance modules focused on differentiated performance – achieved by integrating Qorvo's leading technologies such as NoDrift and LowDrift filters along with advanced power amplifier (PA) and switch technologies. All delivered in the industry's smallest form factors.

Qorvo's RF Fusion provides OEMs with a complete RF Front End (RFFE) solution that incorporates all major transmit and receive functionality including support for major frequency bands into three compact modules covering the high-band, mid-band and low-band regions of the spectrum. The architecture is also designed to integrate support for the rapid deployment of CA in markets worldwide.

Frans Frielink, Business Developer accepts the award

Industry comment
"Moore's Law is at play in the handset component market, with new generations of product having to deliver better performance from a smaller footprint. Leading the way right now is Qorvo's RF Fusion."

Examples of optics incorporating substrate-transferred crystalline coatings. Various geometries and substrate materials may be coated with this technique.

Semiconductor **supermirrors**

Advancing precision laser optics with substrate-transferred epitaxial films

BY GARRETT COLE, MARK WHITE, MARKUS ASPELMEYER AND CHRISTIAN PAWLU FROM CRYSTALLINE MIRROR SOLUTIONS

MULTILAYER optical interference coatings are everywhere. They are employed in consumer products, including anti-reflection coatings in spectacles, cameras, binoculars, consumer electronics, and residential and commercial lighting; they are in industry, in lasers, inertial navigation systems, and tools for lithography and wafer inspection; and they are in scientific labs, in the mirrors, beam-splitters, and polarizers found in fundamental experiments, such as the detection of gravitational waves.

All of these coatings are essentially alternating layers of high and low refractive index materials that provide wavelength selective reflectance – and as you'd expect, you get what you pay for. At the lower end are coatings formed through the evaporation of metals and dielectric films, and at the other extreme are ultra-low-loss coatings formed from high-density sputtering of amorphous multilayers. In total, this optical coatings industry is worth billions of dollars.

The current 'gold standard' for the optical interference coating is the ion-beam sputtered multilayer. Primarily,

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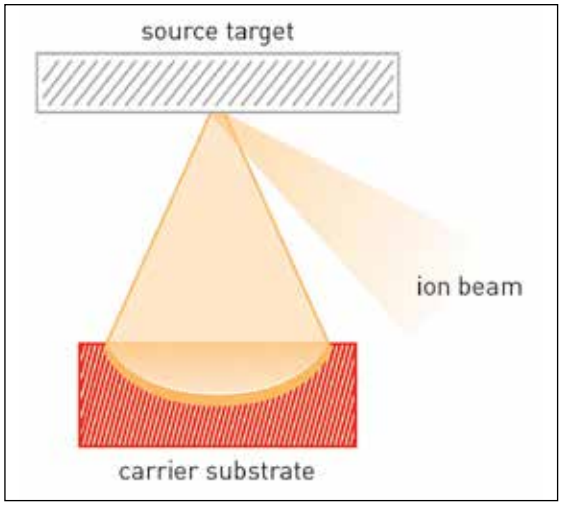

Figure 1: Ion beam sputtering (IBS) is used to deposit low-loss multilayers of amorphous metal oxides. In this case, a beam of ionized noble gas atoms impinges on a metallic target and, reacting with an oxidizing chamber environment, is directly deposited on an optical substrate.

it consists of alternating layers of amorphous metal oxides – most commonly the pairing of high-index Ta_2O_5 and low-index SiO_2. So long as there is reasonable adhesion with the base substrate, the sputtered films can be coated on nearly any surface, even those that are patterned.

One of the strengths of this technology, originally developed for the construction of ring-laser gyroscopes, is the very low levels of optical scatter and absorption loss. The loss levels are so low that they are measured in the parts per million. It is a level of performance that has enabled ion-beam sputtering to be firmly established as the prime technology for generating ultra-low-loss reflectors in the visible and near-infrared.

In general, such interference coatings have little overlap with the compound semiconductor industry. But there is one key exception: the VCSEL. This class of laser diode features a multi-quantum-well active region sandwiched between two epitaxial mirrors, typically referred to as distributed Bragg reflectors, which consist of alternating layers of high and low refractive index semiconductors.

A distinct disadvantage of defect-free epitaxial multilayers, compared with sputtered films, is their need for substrate lattice matching. The growth of these single-crystal epilayers must proceed on a planar surface with a nearly identical inter-atomic spacing, as well as a matched crystalline symmetry. Due to this stringent constraint, substrate options for direct crystal growth are severely limited. Consequently, while ion-beam sputtering has been used to make many high-end coatings in a wide variety of general optics applications, compound semiconductor interference coatings, such as distributed Bragg reflectors based on the pairing of GaAs and AlGaAs, have, so far, been confined to the domain of surface-normal optoelectronics.

At Crystalline Mirror Solutions, a spin-off of the University of Vienna, we have overcome this limitation. Our team, based in Santa Barbara, CA, and Vienna, Austria, (with in-house epitaxial capabilities in Zurich, Switzerland) has developed the expertise to extract and transfer epitaxial multilayers from their native growth wafers to bulk optical substrates, so they can compete head-to-head with direct deposited amorphous coatings.

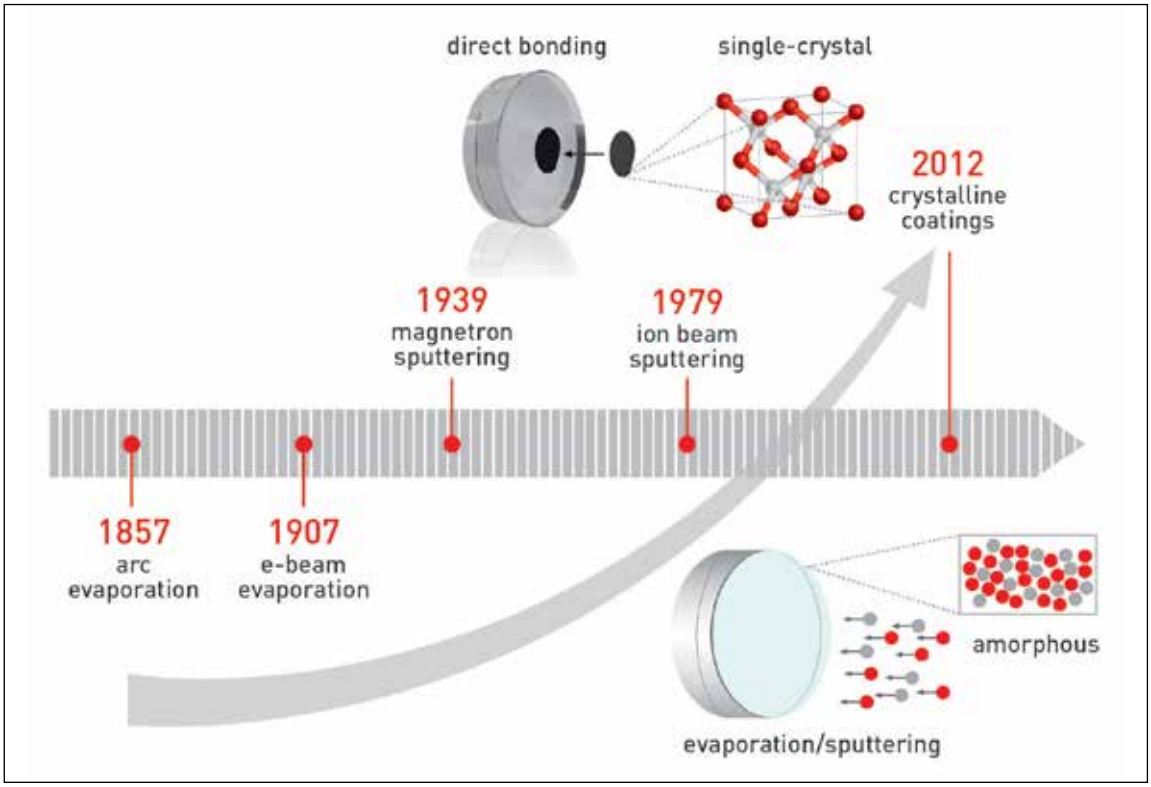

Figure 2: A brief timeline of optical coating techniques, highlighting the approximate development dates for various processes. Crystalline coatings represent a significant departure from all previous techniques involving amorphous or poly-crystalline materials, in that the constituent materials of the coating are single-crystalline materials.

Our structures combine exceptional optical performance with a number of unique and advantageous physical properties that are enabled through the use of compound semiconductor materials. These include a high mechanical quality factor for minimising Brownian noise, a wide transparency window from roughly 900 nm to 10 μm enabling very low-loss mirrors to be realized in both the near- and mid-infrared spectral region, and a superior thermal conductivity – at least an order-of-magnitude higher than that for traditional sputtered films.

Fabrication of our mirrors is based on substrate-transfer and direct bonding, and draws on traditional semiconductor processes, such as epitaxial growth, lithography, and various wet and dry etching techniques. Production begins with the growth of epilayers by MBE, which is chosen for its capability to realise materials of exceptional purity. This high purity leads to very low levels of background doping and absorption, properties that yield ultra-high reflectivity supermirrors. Fabrication is completed by removing the single-crystal multilayer from the original growth wafer and transferring it to the final optic, using post-growth wet and dry etching.

One of the strengths of our pioneering technology is that it allows the direct bonding of epitaxial coatings to curved surfaces. Currently, the radius of curvature can be as tight as 10 cm.

The majority of our work involves coating fused silica substrates and producing near-infrared optics with a centre wavelength between 1000 nm and 2000 nm. However, we have realized high-quality crystalline coatings on a wide variety of substrates, including silicon, sapphire, SiC, diamond, YAG, and YVO_4. The maximum coating area for a continuous structure is limited to the size of the original growth wafer, so we are able to offer material with dimensions up to 20 cm in diameter.

With prototype coatings fabricated in 2012, we first published the results of our process in 2013 in a joint paper with Jun Ye's group at JILA in Boulder, CO (reference included in the caption of Figure 4 below). Following four years of refinement, our substrate-transferred crystalline coatings have now emerged as an alternative high-performance option for optical interference coatings in demanding optics applications.

Our coatings in the near-infrared, for centre wavelengths spanning 1064 nm to 1560 nm, have an excess optical loss – given by summing scatter and absorption – of less than 5 parts per million. Assuming a finite optical transmission, the reflectivity of such a mirror is 0.999992, and the cavity finesse is up to 400,000 at the telecom-relevant wavelength range near 1550 nm. This level of optical performance is fully on par with that of high-quality, ion-beam sputtered

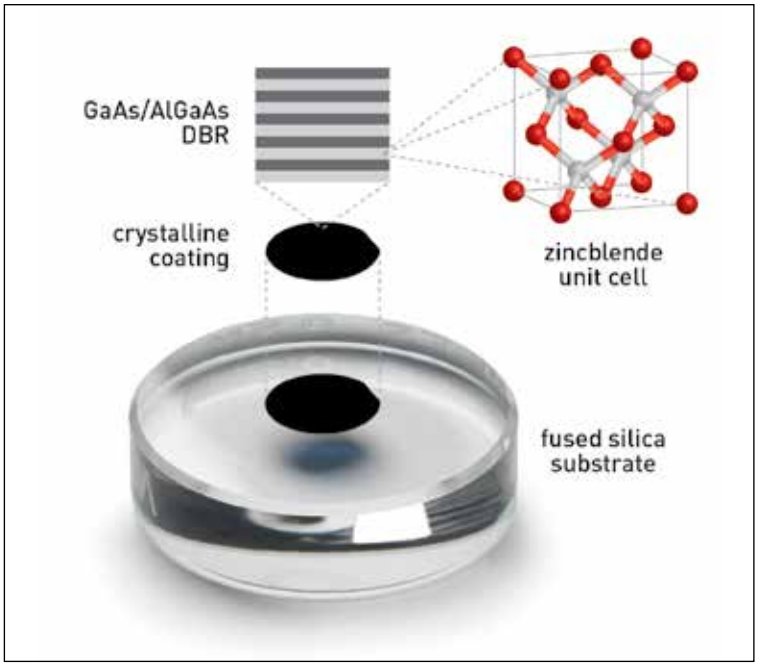

Figure 3: A typical semiconductor supermirror consists of a fused silica optical substrate and a direct-bonded crystalline coating. The 8 mm-diameter coating disc consists of an alternating stack of high-refractive-index GaAs and low-index $Al_{0.92}Ga_{0.08}As$ layers. Following a lithographic process to define and etch the lateral geometry of the coating, the epitaxial film stack is removed from the growth wafer and fused to the final optic, in this case a 25.4 mm-diameter by 6.35 mm-thick fused silica substrate, with a 0.5 m-radius of curvature.

films, and it confirms that an optimized MBE process can produce films that combine extremely high purity with high surface quality. However, one aspect that is typically overlooked in the development of precision optical components is the material's mechanical quality factor, *Q* – this quantity is the inverse of the mechanical dissipation, or imaginary component of the Young's modulus. For some advanced systems, such as precision interferometers utilized for the measurement of gravitational waves and stabilizing reference cavities for optical atomic clocks, it is *Q* that governs the ultimate stability of the system and sets the noise floor for unwanted thermo-mechanical fluctuations of the object.

There will always be some movement of any optical element, because constituent atoms will fluctuate in position due to random Brownian motion. However, the magnitude of this random motion, and thus the limiting noise in terms of displacement sensitivity, will depend strongly on the mechanical *Q* of the constituent materials of the system. The performance of today's precision optical interferometers is so high that this ultimate thermal noise limit is now becoming a significant impediment to further improvement.

The good news is that a switch from existing, high-performance optical coatings to our semiconductor supermirrors can improve the mechanical *Q* by a

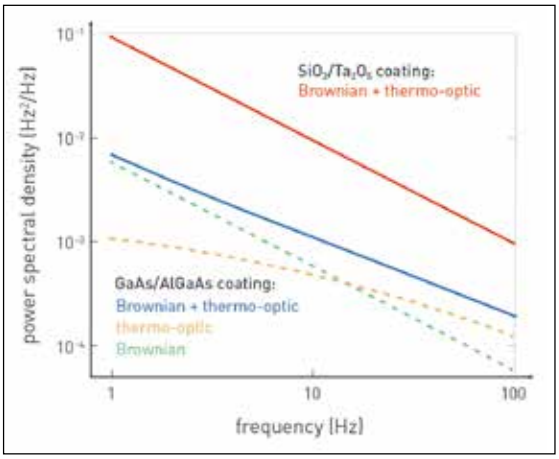

Figure 4: Demonstration of the significant reduction in mechanical damping and thus the limiting coating thermal noise for substrate-transferred crystalline coatings. At 1 Hz the AlGaAs crystalline coating yields a ten-fold improvement in Brownian noise over traditional ion beam sputtered coatings based on SiO_2/Ta_2O_5 multilayers. This plot is reproduced from G. D. Cole, W. Zhang, M. J. Martin, J. Ye, M. Aspelmeyer, "Tenfold reduction of Brownian noise in high-reflectivity optical coatings," Nature Photonics **7** 644, August 2013.

factor of 10 to 100. It is this immediate reduction in mechanical loss and resulting reduction in Brownian thermal noise that provided the original impetus for developing our technology, and is now a driving force for its refinement.

Over the last few years we have manufactured and delivered optics that are being used in the construction of the world's most stable laser systems, which are located in various international metrology laboratories. This includes: room temperature and cryogenic reference cavities for lasers operating at telecom-relevant wavelengths near 1550 nm; dedicated systems targeting clock transition wavelengths for trapped aluminium-ion clocks, as well as neutral atom lattice clock systems based on strontium and ytterbium; and prototype optics for exploring performance improvements that may be possible with crystalline coatings in gravitational wave astronomy.

During the years that follow, our coatings should lead to advances in optical interferometers for precision metrology, with one highlight being the significant improvement in clock performance that can be realized with the roll-out of mHz-linewidth laser systems.

Mid-infrared possibilities

Another attribute of our epitaxial multilayer structure is its exceptionally high optical transparency over a wide spectral range. With this GaAs-based material system, low optical losses can be maintained over a range that extends from approximately 900 nm to 10 μm – and potentially beyond. In contrast, amorphous metal oxides tend to exhibit significant excess absorption beyond 2 μm.

Recent investigations of our semiconductor supermirrors for use in optical sensing in the mid-infrared – the centre wavelengths for these mirrors are from 3 μm to 4 μm – highlights their exceptional performance. Direct absorption measurements at 3.7 μm reveal limiting losses as low as 5 parts per million. This level of performance opens the door to new scientific discoveries in chemical kinetics, via time-resolved optical frequency comb spectroscopy.

Efforts in this direction include a ground-breaking experiment led by Jun Ye's group at JILA, a joint institute of NIST and the University of Colorado Boulder. Using an experimental set-up that included our mirrors, these researchers delivered a breakthrough in the understanding of combustion by unlocking the fundamental reaction kinetics of the deuterated hydroxyl molecule, OD, and carbon monoxide. Under thermal reaction conditions, Ye and co-workers observed, for the first time, trans-DOCO (the deuterated analogue of the trans-hydrocarboxyl radical). This elusive, short-lived intermediate compound is crucial for processes relevant to earth and planetary sciences, and the burning of fossil fuels.

We believe that this type of mirror can be further improved, leading to an optical loss at the parts-per-million level in this difficult wavelength window. Our superlattice stacks can be transferred to a variety of mid-IR compatible substrates, including single-crystal silicon, zinc selenide, calcium fluoride, germanium, and GaAs.

Superior conductivity

Opportunities for our mirrors exist in high-power laser systems for materials processing. These systems require optics with minimal thermal distortion and excellent thermal conductivity – criteria that our mirrors excel in. Compared with the incumbent technology, amorphous metal oxides, our mirrors have a significantly higher thermal conductivity – it is typically 30 $W\,m^{-1}K^{-1}$ versus 1 $W\,m^{-1}K^{-1}$ for low-loss metal oxides.

While our company and technology may still be quite young, we have already demonstrated that our substrate-transferred, compound-semiconductor-based optical interference coatings can radically enhance performance in critically demanding optics applications.

This virtue, combined with optical absorption levels below parts per million, makes our mirrors an excellent choice for reflectors in demanding laser-processing applications. Here, they should enjoy the greatest success in kilowatt-class CW or quasi-CW laser systems that are employed for cutting, welding and brazing. And if the semiconductor supermirrors have to operate in harsh thermal environments, they can be united with thermally-optimized substrate materials, such as diamond or SiC. This promises to redefine the performance metrics for reflectors operating in these conditions.

While our company and technology may still be quite young, we have already demonstrated that our substrate-transferred, compound-semiconductor-based optical interference coatings can radically enhance performance in critically demanding optics applications. This is due to their tremendous attributes: the lowest mechanical loss, and thus Brownian noise; the highest thermal conductivity; and the widest spectral coverage of any optical coating technology. Looking ahead, there is a bright future for crystalline coatings in applications requiring the ultimate levels of optical, thermal, and optomechanical performance.

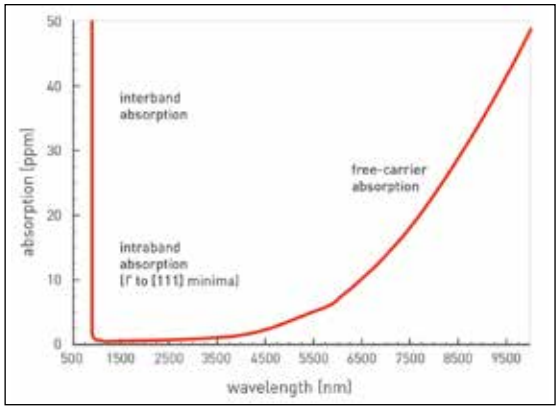

Figure 5: Calculated absorption loss as a function of centre wavelength for unintentionally doped GaAs/$Al_{0.92}Ga_{0.08}As$ Bragg mirrors. This theoretical curve assumes background *n*-type doping in the epitaxial films with a concentration at the low 10^{14} cm^{-3} level, yielding ppm-level losses in the near-infrared (from 1000 nm to 1600 nm) as verified experimentally. The curve also takes into account the dispersion – that is, the variation in refractive index with frequency – of both the high- and low-index layers, as well as the variation in penetration depth with wavelength for mirrors covering the range from just below the GaAs absorption edge at about 870 nm at 300 K to 10 μm. For wavelengths beyond approximately 5 μm free-carrier losses become a significant impediment to low-loss operation.

Uniting high-mobility transistors on silicon

Selective epitaxy can scale field-effect transistors featuring InGaAs and SiGe channels to small enough dimensions for next-generation CMOS

BY LUKAS CZORNOMAZ FROM IBM

THERE ARE THREE KEY components in today's information technology. One, involving smartphones and Internet-of-Things technologies, is a dense, mobile network of nodes for collecting and pre-processing data. Another is the efficient, broadband infrastructure that transmits the data. And the third, coined Cloud Infrastructure, is the de-materialized space for high-performance data storage and processing.

For the electronic devices found at the beginning and at the end of this chain, it is becoming tougher than ever to reduce power while increasing performance. Here, compromise is the name of the game, commonly seen in the reduced battery life of smartphones and the tremendous challenges for cooling datacenters.

If we rewind the clocks to the first few decades of the silicon industry, the situation was markedly different. Back then geometrical scaling delivered the desired gains in performance and reduction in power with every new technology node. But now new materials are needed to maintain progress. This began with the introduction of high-κ gate dielectrics in 2007 at the 45 nm node. By replacing SiO_2 with HfO_2, designers have been able to maintain the supply voltage while keeping the parasitic power associated with the gate leakage at acceptably low levels.

Nowadays, meeting the targets in power consumption call for a substantial reduction in the supply voltage. A promising approach for delivering the next revolution in the semiconductor industry is to switch from silicon to compound semiconductor channel materials. This move increases carrier mobility, allowing for a trimming of power consumption while increasing performance. Success on both these fronts is possible, because the supply voltage can be reduced

while maintaining a large drain current, and therefore a high performance level.

The increases in mobility with this radical move are substantial. For the benchmark material, silicon, electron and hole mobility is typically 1400 $cm^2 V^{-1} s^{-1}$ and 450 $cm^2 V^{-1} s^{-1}$, respectively. In comparison, electron mobility in InGaAs is more than six times higher, exceeding 10000 $cm^2 V^{-1} s^{-1}$, and hole mobility in germanium is four times higher, and can be as high as 1900 $cm^2 V^{-1} s^{-1}$.

Thanks to these far higher values, an advanced CMOS technology can propel the power-performance trade-off to a level that conventional silicon CMOS can only reach after two-to-three scaling nodes. However, optimizing electron and hole transport separately implies to have two different compounds (InGaAs

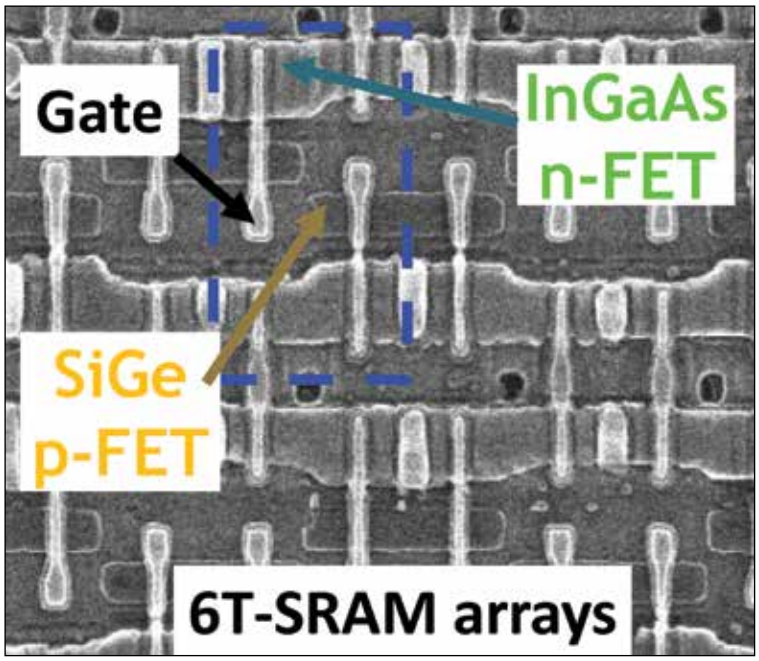

Figure 1. A top-view, scanning electron microscopy image of an InGaAs/SiGe 6T-SRAM array on silicon with a cell size of 0.4 μm^2. This image is taken after completion of front-end-of-the-line fabrication.

and SiGe) co-integrated on the same chip, which is a major challenge

Up until now, despite much effort, the industry has not been able to demonstrate a suitable co-integration technology. It is a tall order, requiring the fulfilment of many criteria. The technology must be suitable for silicon substrates and it has to be compatible with thestandard CMOS design environment. What's more, it must simultaneously allow the growth of defect-free InGaAs, the fabrication of high-performance InGaAs FETs, and the co-processing of these transistors with SiGe devices.

At IBM Research in Zurich, our team has more than ten years of expertise on this topic. This expertise has been built over time through many achievements including: the development of unique methodologies to integrate InGaAs with large-size, bulk silicon substrates; the building of CMOS-compatible transistors and optimization of their performance; and the demonstration of hybrid CMOS circuits, including the evaluation of their impact on future CMOS technology nodes.

Our latest and major highlight has been the first demonstration of an InGaAs/SiGe CMOS technology on a silicon substrate, using fabrication processes suitable for high-volume manufacturing on 300 mm wafers. This recent work breaks new ground by demonstrating basic building blocks of digital circuits at relevant dimensions. It is a major milestone towards a manufacturable, hybrid InGaAs/SiGe CMOS technology, which is the main path for enabling further improvement in the power/performance tradeoff for digital technologies beyond the 7 nm node.

Based on selective epitaxy, our novel approach has yielded functional inverters and dense arrays of 6T-SRAMs (see Figure 1).

Production of these circuits began by integrating InGaAs and SiGe crystals on silicon substrates with a novel, patented, selective growth process – it is based on MOCVD, and forms thin InGaAs platelets in empty oxide cavities (see Figure 2). Note that although this circuit integration has been demonstrated on a SiGe-on-insulator wafer, it can be readily implemented on bulk silicon or on silicon-on-insulator.

Processing began with dry etching, to form *p*FET active regions that can be either mesas or fins. We then formed empty SiO_2 cavities. They offer access to the silicon substrate, which acts as a crystalline seed. Following this, we refilled the empty cavities using an InGaAs epitaxy step. During this, the growth direction changed from vertical to lateral. Switching the growth direction is advantageous, as it allows the handling of defect filtering with a minimal area penalty, while defining *n*FET active regions by the lateral growth direction.

A noteworthy merit of this approach is that it is well-suited to the high density requirements for CMOS technology. Referred to as confined epitaxial lateral overgrowth, it belongs to a family of template-assisted selective epitaxy techniques.

Once the InGaAs areas have been integrated next to the SiGe areas on the silicon substrate, FinFETs are fabricated. For this, we use a CMOS-compatible self-aligned flow that enables aggressive scaling of transistor density. InGaAs fins are defined by dry etching with an inductively coupled plasma, before plasma-enhanced, atomic-layer deposition adds a high-κ and metal-gate stack of Al_2O_3, HfO_2 and TiN. Once the gate has been dry etched, SiN sidewall spacers are formed, before selective n^+ InGaAs raised source and drain regions are grown epitaxially. Standard tungsten-plug contacts are then realized.

One of the significant challenges that we have faced is the need to develop new fabrication processes to accommodate the very different process requirements of InGaAs and SiGe. That's because typical wet clean and dry etching processes for SiGe are not selective to InGaAs; different surface preparations are needed for the high-κ gate stacks for InGaAs and SiGe; InGaAs and SiGe require different source and drain materials; and both materials require very different processing thermal budgets. Addressing these requirements implies numerous key findings discovered over years of experimentation, converging into the establishment a novel process flow.

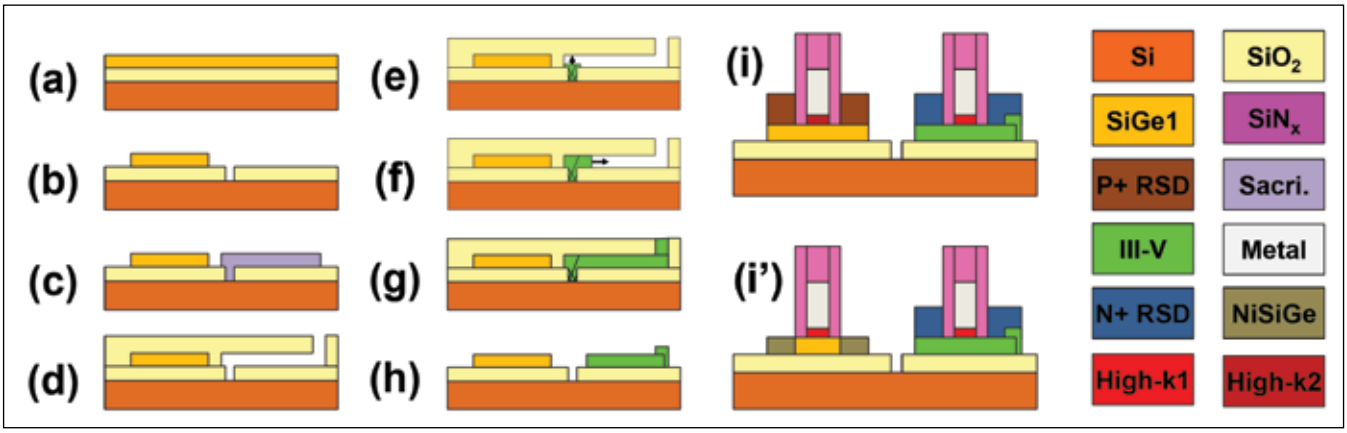

Figure 2. Etching the SiGe-on-insulator wafer (a) defines the *p*FET active region and an opening for the silicon seed (b). Sacrificial material is then added (c), before capping with an oxide and adding an opening to this layer. Sacrificial material is removed (d), before InGaAs grows from the seed (e) through the neck (f) to fill the cavity (g). The oxide cap is removed (h), before forming a *n*FET active region and ultimately InGaAs *n*FETs and SiGe *p*FETs (j). A simplified process using a common high-κ/metal gate has been pursued by IBM Zurich (i').

Another key to our success has been the development of a design-technology co-optimization algorithm that is able to adapt standard IP blocks to the novel III-V selective growth in oxide cavities. Armed with this, we have optimized the placement of seeds and cavity openings.

We used this algorithm for the fabrication of dense 6T-SRAM arrays with a 'thin-cell' configuration. Our physical demonstrators have a cell size below 0.45 μm^2. Even smaller values should be possible, as our scalability studies show that our technology is compatible with 7 nm node ground rules.

Our demonstration of scaled InGaAs/SiGe hybrid CMOS circuits has profound consequences for manufacturing technologies. It breaks the conventional wisdom that hybrid InGaAs/SiGe CMOS technology, although being widely acknowledged as the ideal option, is intrinsically limited by engineering bottlenecks, and is therefore unlikely to be commercialized.

Thanks to our efforts, it is now possible to merge processes, metrology, and practices for materials as different as silicon, III-Vs and IV-IVs into a single processing environment. This is not only great news for the future of digital applications – it also opens the door to the development of fabs designed for system-on-chip circuits, tightly integrating logic with other technologies such as wireless, power and optical technologies.

Further reading

L. Czornomaz *et. al.* "First Integration of InGaAs/SiGe Channels into Dense SRAM Arrays with sub-0.45 μm^2 Cell Size Fabricated Using Standard CMOS Processes," VLSI Technology (VLSI Technology), 2016 Symposium on, p. T9-2, Jun. 2016

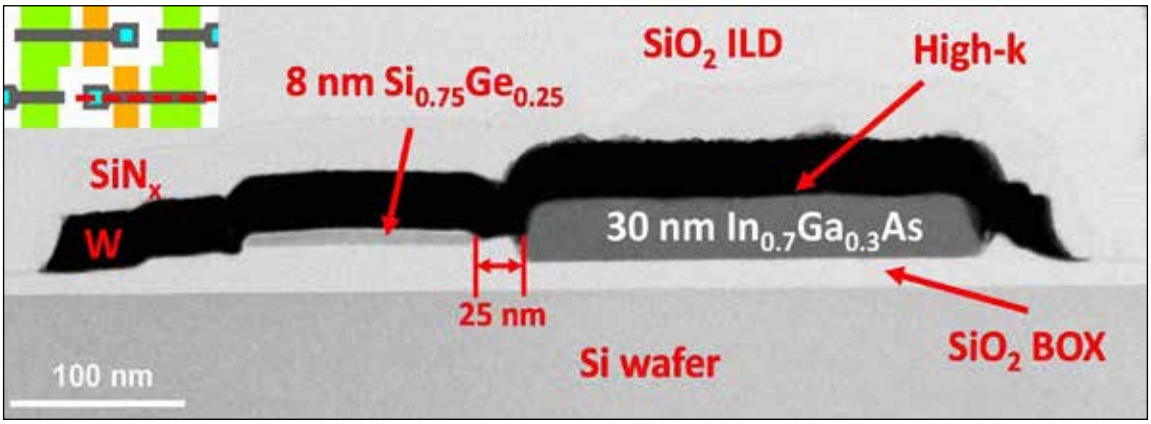

Figure 3. The cross-section through the gate of a CMOS inverter of a 6T-SRAM cell, where SiGe and InGaAs channels are integrated side by side on a silicon substrate. Separation between the two high-mobility channels is as small as 25 nm.

EVALUATING THE CAPABILITY OF UV LEDS

A true appreciation of the performance of a UVC LED requires an understanding of its temperature dependent output power and its spectral profile

BY LEO SCHOWALTER FROM CRYSTAL IS

THERE ARE CRITICAL consequences to inadequate disinfection of drinking water and medical surfaces. Consider these two statistics: one in ten people still have no access to clean drinking water; and one in every 25 patients acquires an infection while hospitalized, causing healthcare costs to escalate by billions of dollars.

Fortunately, a revolution is underway, and new solutions are modernizing the way disinfection is being accomplished with greater design flexibility and cost effectiveness. A new generation of products is appearing that are equipped with powerful LEDs that emit in the UVC band, which spans 200 nm to 280 nm. Armed with these solid-state sources, more compact designs can be introduced in everything from portable systems for drinking water purification to hospital infrastructure that combats airborne infections.

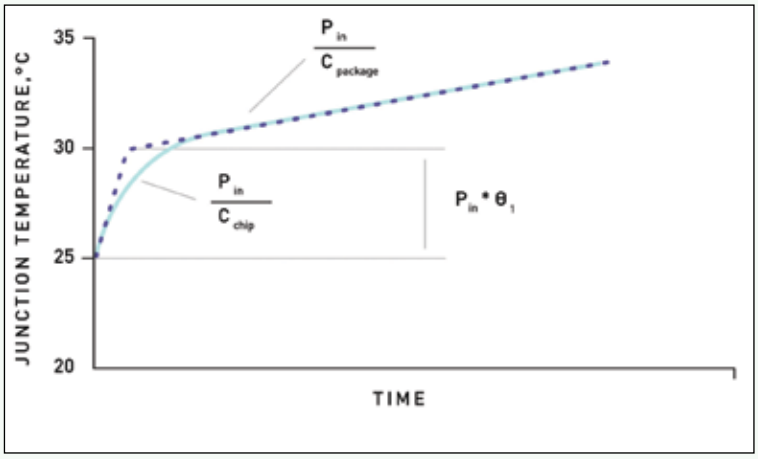

Figure 1. A very simple model for the temperature rise in a typical Crystal IS Klaran diode as a function of pulse length. Note that Klaran UVC LEDs are manufactured on native AlN substrates, so will heat up very quickly and (nearly) uniformly, due to the high thermal conductivity of AlN. While generally this model applies to all UVC LEDs, diodes fabricated on Al_2O_3 have an order of magnitude lower thermal conductivity, and may have more temperature variation across the chip at higher powers.

With adoption of UVC LEDs on the rise, the number of manufacturers offering these devices is increasing, and there is more interest than ever in quantifying the performance of the light source. Key performance characteristics in these applications are output power and germicidal effectiveness.

Power output factors

With all types of LEDs, regardless of their emission wavelength, light is emitted out of the front of the device, while heat is extracted from the back. During operation, as the junction temperature increases, the LED's light output decreases.

With a visible LED, typically 40 percent to 60 percent of the electrical energy is converted to heat. That is considerable, but in the case of UVC LEDs, 95 percent or more of the energy is converted to heat. Therefore, it is critical to properly manage the heat to maintain light output. This concern is amplified by the market drive to decrease LED footprint, resulting in compact packages, which limit built-in heat absorption or dissipation design options.

To appreciate the importance of good thermal management, note that if a UVC LED has not been mounted to a heat management system, it can reach 200°C in less than a second. At this temperature, the device output will drop to near zero and have a very short lifetime.

For customers seeking to characterize diodes without soldering them to a thermal management system, a pulse measurement approach is recommended to limit heat generation within the device and provide reliable, repeatable output power measurements. This is the same process Crystal IS and other

manufacturers are adopting to measure UVC LED output as these devices are commercialized.

We can use a very simple model for the temperature rise in a typical Crystal IS Klaran diode as a function of pulse length or duration (Figure 1). Heat is carried away from the chip by thermal conduction of the gold bump bonds used to attach it to the rest of the LED package. Because the thermal resistance within the chip is much smaller than the bonds and the heat capacity of the chip is much smaller that the heat capacity of the package, the chip temperature will rise rapidly. This will continue until the temperature difference between the chip and the package is approximately equal to the product of the input power times the thermal resistance, at which point the heat generated in the chip will be approximately equal to the heat carried away by thermal conduction.

Following this initial hike in temperature, the junction temperature rises more slowly as the package heats up. After a few milliseconds, the slope of the temperature rise approaches the power in, divided by the capacity of the package. The temperature continues to rise until a significant amount of heat can flow into the ambient environment.

After the first few milliseconds of operation of the LED, keeping the package cool requires heat to flow away from the package to the heat sink (this is illustrated in Figure 1). When this happens, the thermal resistance between the package and the thermal management system is determined by the combination of the quality of the solder to the heat sink, and the ability of the heat sink to either absorb energy, or radiate it to the environment.

If the device is operated without a heat sink, the junction temperature will continue to rise, which will lead to a decrease in light output. Nonetheless, using a pulse mode can still carry out an accurate output power characterization of the diode. To improve accuracy and reproducibility, the power output should be measured during the gradual increase portion of the curve, not in the steep incline of the first

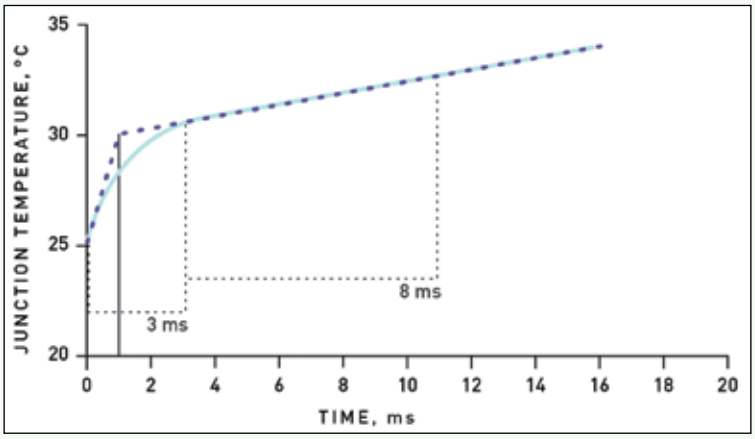

Figure 2. Crystal IS measures Klaran device power by waiting 3 ms after the start of the current pulse and integrating the output power for 8 ms.

millisecond. This allows the temperature difference between the chip and the package to stabilize at approximately the same value it will have between the LED chip and solder pads. In addition, the power measurement should be taken at the shortest time possible – just enough to capture the diode's power output while minimizing the package's heat induced temperature rise. We measure devices by waiting 3 milliseconds (ms) after the start of the current pulse and then integrate the output for 8 ms, which means we stop integrating 11 ms after the start of the pulse (Figure 2).

There are pitfalls associated with the failure to appreciate the influence of the measurement time when attempting to determine the output power of a UVC LED. If we take an example using a Crystal IS Klaran LED with a specified output power of 20 mW operated at an ambient temperature of 25°C. The heat capacity of the package is approximately 20 mJ/K, which means the slope for the temperature rise is approximately 200 K/s for a 4 W input power. As this diode has a specified thermal derating of 0.5 percent per Kelvin, power will fall by 5 percent if the junction temperature increases by 10°C.

We then assess the output power of our LED by driving it with an 80 ms pulse, and measuring the output power after 40 ms for 40 ms. During this

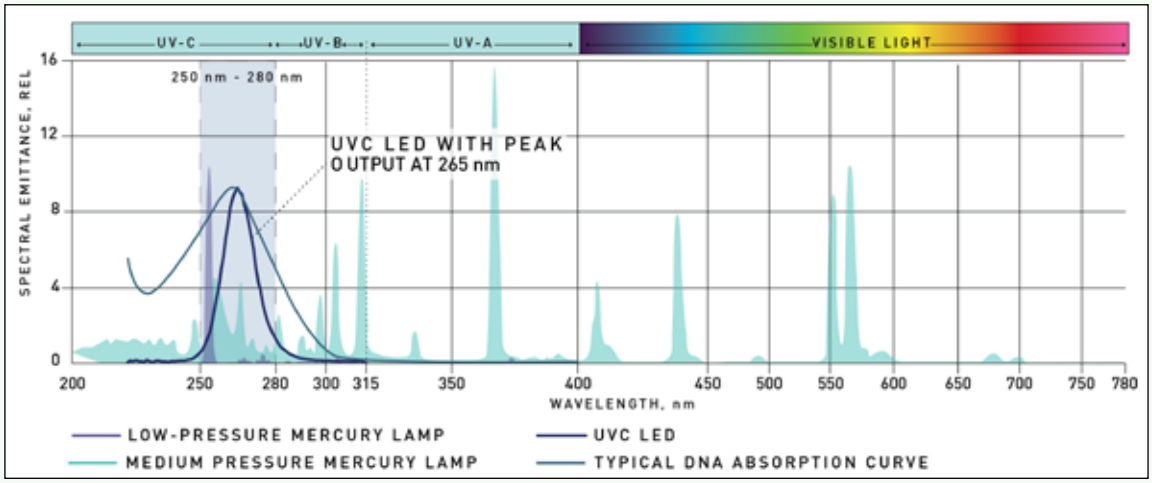

Figure 3. Spectral comparison of low and medium pressure mercury lamps versus LED in relation to typical DNA absorption curve.

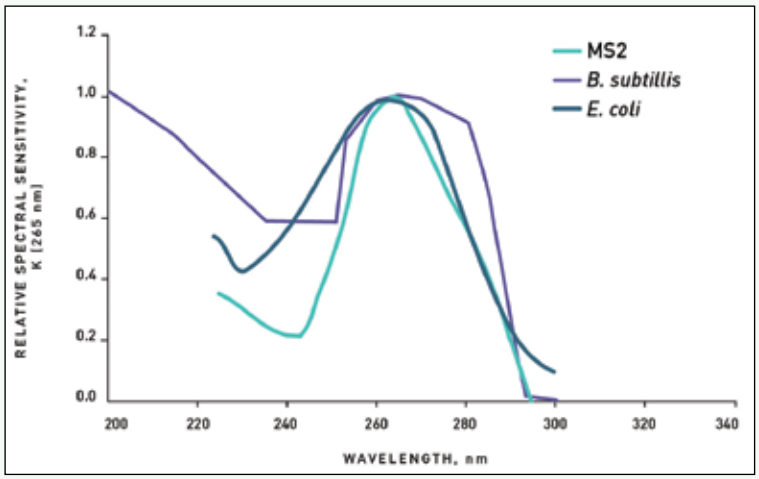

Figure 4. Action spectra of common target/challenge microbes in water disinfection normalized to 1 at 265 nm. The action spectrum of B. Subtillis as defined by the ÖNORM Standard; E. coli as outlined in *A review of UV lamps* by Henk F. J. I. Giller, in WEF 2000; and MS2 as found in *This Way Forward: Addressing Action Spectra Bias Concerns In Medium Pressure UV Reactors*, Bryan Townsend, et al.

process, the chip's temperature has an initial jump in the first millisecond, due to heating. After that, within the first 40 ms the junction temperature increases an additional 8°C – that's 0.2°C per millisecond – with respect to the package. Once 80 ms has elapsed, which occurs following another 40 ms of the diode being run without a heat sink, the junction temperature increases another 8°C. During the first 40 ms, the instantaneous power of the diode drops by 4 percent, and it falls by this amount again in the next 40 ms. So, assuming that measured power is obtained by averaging the power between 40 ms and 80 ms, the measured decrease in power is 6 percent.

When measuring power output with a goniometer, it is important to resist the urge to assume a particular radiation pattern. It is tempting to save time by measuring the radiant intensity for one LED, and then, after recording the power of subsequent diodes at one fixed angle, use this single value to infer the total power of the diode. This is flawed when the radiant intensity varies between devices, due to differences in packages or manufacturers.

In practical terms, this average is obtained by integrating the power for 40 ms, and dividing the measured energy detected by that integration time. This gives an integrated power is 18.8 mW, which is a 6 percent reduction of the 20 mW specified power. This difference in the measured output, compared with that specified on the data sheet, highlights the impact of the increased junction temperature.

Unique challenges

UVC LEDs are specified to run at a maximum input power and operate within a pre-determined design temperature range. These design specifications are outlined on the diode's product data sheet and manufacturers calibrate their testing equipment to ensure the product shipped to customers meets these specifications. To ensure component quality, customer quality control engineers should test/measure an LED like the OEM. In the previous example, an integrating sphere was used to measure the total power output of the Klaran diode during pulse mode.

Manufacturers adopt one of two methods for measuring the light source's radiant flux, often noted as the device power. They either use an integrating sphere, which collects all the light from a source placed inside the sphere; or they turn to a goniophotometer, which records the radiant flux of a light source from many different angles around the source to yield a radiant flux as a function of angle. Armed with the later, it is possible to calculate the radiant per solid angle, which is called the radiant intensity – integrating this over all angles yields the radiant flux for the light source.

When measuring power output with a goniometer, it is important to resist the urge to assume a particular radiation pattern. It is tempting to save time by measuring the radiant intensity for one LED, and then, after recording the power of subsequent diodes at one fixed angle, use this single value to infer the total power of the diode. This is flawed when the radiant intensity varies between devices, due to differences in packages or manufacturers. The use of integrating spheres avoids this issue, because they are designed to accurately measure the power emitted by the diode, regardless of the radiation pattern.

Determining germicidal power

Knowing an accurate value for the power output of a UVC LED does not, in itself, reveal the capability of this source for a disinfection system. That's because the effectiveness of this radiation is wavelength dependent, with light in the range of 250 nm to 280 nm most effective at inactivating the DNA of microorganisms, rendering them unable to reproduce.

Historically, disinfection has been accomplished by low and medium pressure mercury arc lamps. Low pressure lamps emit a single wavelength of 253.7 nm, so the total output power of the lamp is equivalent to the output power in the UVC range, albeit at a sub-optimal wavelength. Medium pressure lamps, in contrast, emit a broader spectrum, including wavelengths in the germicidal range, plus those that do not contribute to disinfection. With these lamps, typically just 20 to 30 percent of the light is emitted in the UVC range.

With UV LEDs, the spectral profile is much more suitable (see Figure 3). The continuous spectral response of these sources deliver greater overlap with the most critical wavelengths for disinfection, making them more efficient light sources for these systems. However, these differences in emission spectra require a new methodology to account for disinfection effectiveness.

It's a situation that is very similar to the one faced by makers of visible light sources. They measure brightness with the lumen, a unit that takes into account the spectral response of the human eye. For UVC LEDs, what matters is the power output that inactivates pathogens. This is known as the 'germicidal power'.

The most accurate method to specify the required germicidal power for a particular application is to know both the specific pathogen to be inactivated, and its action spectrum – that is, this pathogen's unique profile of sensitivity, by wavelength, to a light-source. Once that is known, the germicidal power of the UVC LED can be determined by the cross product of the light source and the action spectrum for the pathogen.

Different pathogens have different levels of susceptibility to UVC energy (see Figure 4 for an example). Although all peaks close are to 265 nm, the peak absorption wavelength for DNA, there are variations in the sensitivity to discrete wavelengths (see Table). Multiplying the emission of UVC diodes by a weighting determines the power output, in terms of the power available for the disinfection of a specific pathogen.

As applications for UVC LEDs expand, the number of providers will increase. This has pros and cons for OEMs, who have greater choice, but must contend with greater variation between product specifications. When an engineer designs and develops a product, they may prefer to observe the spectrum of an individual light source, so that they can determine the optimum benchmark performance criteria. But high-volume manufacturers desire a more systematic approach for specifying germicidal output power. This is possible with convolution – that is, the normalizing of LED output in terms of germicidal power.

We have evaluated the performance of UVC LEDs from a number of manufacturers, by plotting the ratio of germicidal-to-total power, as a function of wavelength (see Figure 5). This reveals that when the total diode power output is the same for all providers, there is still a significant variation in germicidal power, due to differences in peak wavelength. For example, a 285 nm LED from one supplier can have the same total power as another at 265 nm, but only 40-50 percent of the germicidal effect.

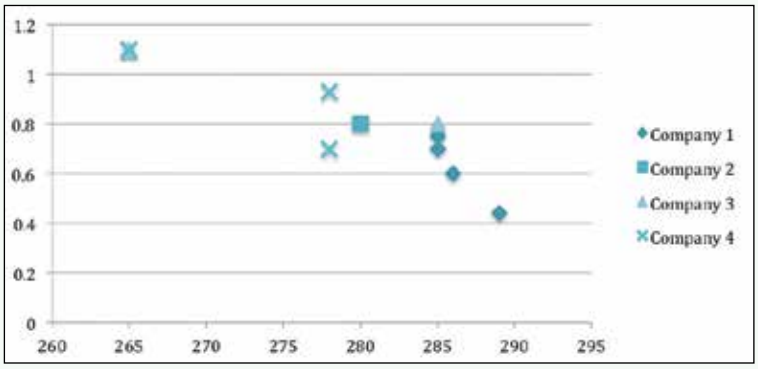

Figure 5. Ratio of total power to germicidal power, based on the ÖNORM standard for a range of commercially available UVC LEDs. Even minor changes in wavelength have a significant impact on the germicidal power available. This is a particular problem at longer wavelengths, where the efficacy of the radiation is rapidly changing with wavelength.

Also note that there is an inconsistency in germicidal effect as diodes stray away from the peak absorption of DNA (see Figure 5). This is important, for it could mean the difference between meeting the dosage requirements for safe drinking water, and failing to do so, which would leave active pathogens to infect customers.

While complex microbiological systems have no single approach that fits all needs, specifying light sources based on germicidal powers does offer a step forward in simplification, allowing engineers to create reasonable designs for manufacturability. These sources combine a higher efficiency in germicidal wavelengths with a compact footprint, and can produce a reduction of more than 99.99 percent in pathogens, giving them proven effectiveness in water disinfection. In the coming years, there is no doubt that there will be an uptake in UVC LEDs for disinfection.

Wavelength	Weighting for *B. subtillis*	Weighting for *E. coli*	Weighting for MS2
250 nm	0.62	0.80	0.58
253.7 nm	0.82	0.85	0.77
260 nm	0.98	0.95	0.98
265 nm	1.00	1.00	1.00
270 nm	0.99	0.90	0.88
275 nm	0.96	0.80	0.79
280 nm	0.91	0.60	0.67
285 nm	0.70	0.40	0.59

Preparing the way for high-quality mass-producible semi-polar GaN

Careful control of epitaxy, in part through facet engineering, can create a semi-polar GaN template on sapphire that is ideal for the mass-production of ultra-efficient LEDs

BY JIE SONG AND JUNG HAN FROM YALE UNIVERSITY

THERE HAVE BEEN no major breakthroughs in LED technology in recent years. While progress is still being made, gains in the efficacy of lighting products are now steady, yet sluggish. And although there is still a tangible performance gap between "tier 1" and "tier 2" vendors, it is narrowing.

Further expansion and penetration of solid-state lighting hinges on a step change in performance. This could come from solving either of two biggest outstanding technology issues, which are known as the efficiency droop and wavelength droop. The former is the rapid decrease in an LED's external quantum efficiency above a current density of typically 1 A cm^{-2}, while the latter refers to the systematic decrease in InGaN LED efficiency from blue to green, yellow, and amber.

Both these issues, which have been the subject of much investigation, are beyond the scope of this article. However, they are included as a backdrop to the semi-polar technology developed by our team at Yale University and Saphlux that has the potential to take LED performance to a new level.

While details of various mechanisms that contribute to the droop continue to court debate, there is a consensus of opinion that the polar nature of the wurtzite GaN crystal configuration, in particular the strong polarization-induced electric field along the *c*-axis (0001), plays a central role in complicating and compromising the performance of GaN light emitters. The presence of high electrostatic fields in III-nitride heterostructures is well known, with reports of its existence appearing as far back as the late 1990s. Since then, researchers have been hunting for more favourable GaN orientations.

A tough start

Early success came at Paul-Drude Institute, Berlin. These researchers revealed that non-polar [$10\bar{1}0$] *m*-plane GaN can be grown on foreign substrates. Their technology, referred to as the beginning of the Gen 1 approach for preparing non-polar and semi-polar GaN on planar heteroepitaxial substrates, produced films with a rather primitive material quality. Stacking faults and dislocations riddled the epilayers (see Figure 1).

It did not take long for researchers in the III-nitride community to turn to their toolkit of approaches for eliminating defects. That included epitaxial lateral overgrowth (ELO), a technique that can suppress structural defects from heteroepitaxy. The ELO technique, which we describe as the Gen 2 approach, is known to deliver success on *c*-plane GaN, where it leads to the formation of dislocation-free layers. But when it is applied to non-polar and semi-polar GaN planes, new stacking faults form in the overgrown region along the -*c*-axis [$000\bar{1}$]. The tenacity and

recurrence nature of these stacking faults has cast serious doubt on the ultimate viability of non-polar and semi-polar devices.

One of the critical advances within the nitride community in the years spanning the late 1990s to the middle of the following decade was the use of hydride vapour phase epitaxy (HVPE) to prepare *c*-plane GaN with a thickness in the millimetre or even centimetre range. This technology, perfected by several Japanese semiconductor manufacturers, is capable of growing GaN at hundreds of microns per hour. It enables the preparation of GaN crystals that are shaped like hockey pucks and have a thickness of 5 mm or more. Manufacturers take the upper portion of these pucks, which have a very low density of dislocations, and slice them into free standing GaN wafers. This yields high-quality wafers that support the commercialization of performance demanding applications, such as blue laser diodes.

These GaN pucks can also be sliced at different angles to produce samples with different crystallographic orientations. This approach becomes a convenient shortcut for researchers to quickly access high-quality, non- and semi-polar GaN to validate the anticipated benefits.

Further success came in 2005, when researchers at UCSB, working with Mitsubishi Chemical Corporation, built the first non-polar, *m*-plane GaN LEDs on a free-standing GaN substrate. These devices delivered an instantaneous, compelling improvement in light output, asserting the promises of non-polar and semi-polar orientations while emphasizing the importance of employing a low-defect template.

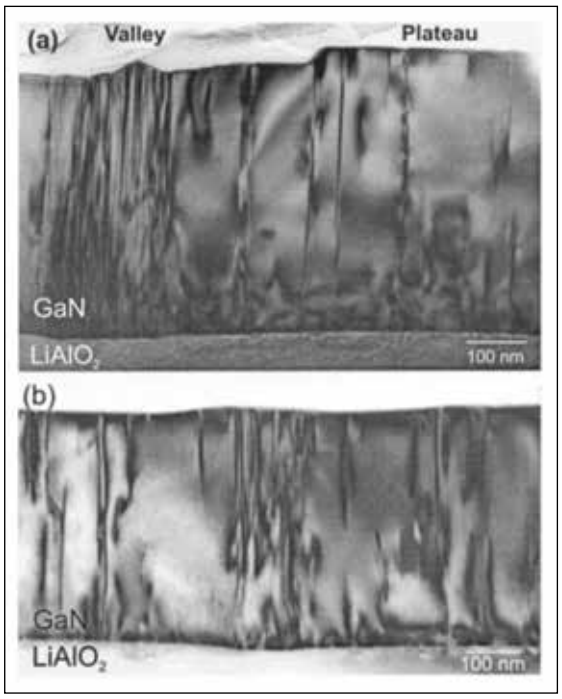

Figure 1. Cross-sectional g = <1$\bar{1}$00> two-beam bright-field transmission electron microscopy images near the [11$\bar{2}$0] zone axis of two samples. The defects running through the layers are identified as basal plane stacking faults. Reprinted with permission of AIP Publishing.

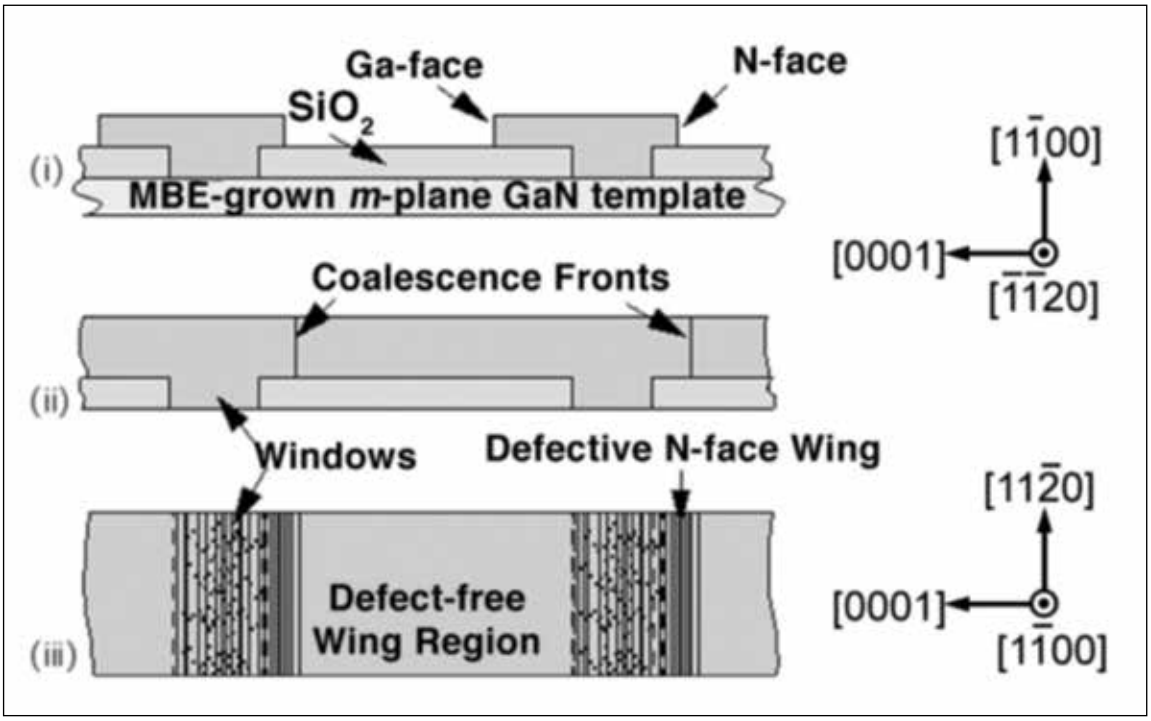

Figure 2. The growth evolution for (1$\bar{1}$00) GaN formed by epitaxial layer overgrowth. Reprinted with permission of Japan Society of Applied Physics.

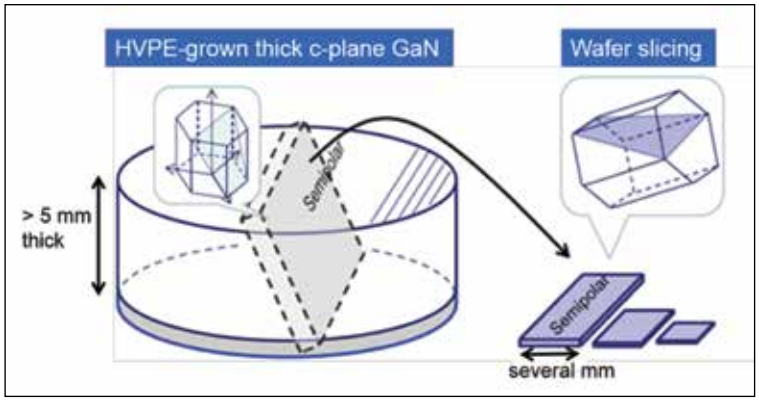

Figure 3. Semi-polar GaN bulk substrates can be produced via HVPE growth of thick, *c*-plane GaN bulk substrates and subsequent cross-slicing.

Between 2007 and 2014, academic groups and industrial labs, including those at Sumitomo, Sony, Nichia, and Osram, have reported performance enhancements. Measurements made in these facilities show that devices formed from various semi-polar orientations, prepared by cross-slicing of GaN crystal pucks, are less prone to current and wavelength droop. This validates the potential for next-generation GaN devices formed on orientations with reduced polarization fields.

The main drawback of HVPE-grown, free-standing GaN substrates is that they are difficult to scale-up and manufacture. Due to the geometry of the GaN puck, cross-slicing at a high angle to the *c*-plane (to move away from the polar-axis) yields tiny strips with irregular, inconsistent dimensions (see Figure 3). This form of substrate is a nonstarter for any serious LED-based research and development activity in growth and processing. In spite of the compelling results from a handful research labs specialized in coping with these defect-free, free-standing non- or semi-polar GaN pieces, the majority of the III-nitride community has yet find a way to cross the chasm, and to commercialize non- and semi-polar GaN technology. This situation could change if high-quality GaN can be made through hetero-epitaxy on large-area, mainstream substrates, such as sapphire or silicon. Beginning from 2008, several groups began to investigate a new approach to accomplishing this, which we refer to as orientation-controlled epitaxy (OCE) on patterned sapphire substrates.

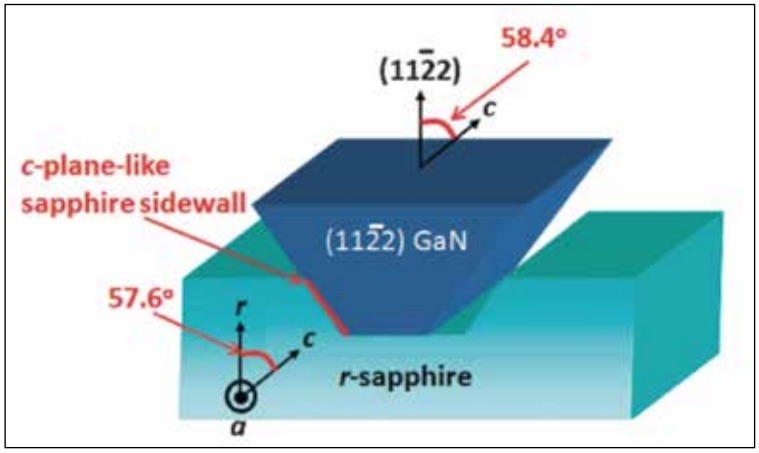

Figure 4. Growth of semi-polar (11$\bar{2}$2) GaN layer on a maskless, patterned *r*-plane sapphire substrate. Reprinted with permission of AIP Publishing.

Revisiting, improving

The idea of OCE on sapphire originated from an earlier work by Nobuhiko Sawaki at Nagoya University in Japan. That team demonstrated selective growth of GaN on inclined {111} sidewalls of stripe patterned silicon substrates. The GaN growth proceeds in the *c*-direction, inclined to the surface normal, which can coalesce to produce a flat semi-polar or non-polar surface depending on the inclination angle of the sidewalls. This method allows a new definition and design of epitaxial relations between the layer and the substrate. Success stemmed from integrating several established techniques, including high-precision patterning of sapphire substrates, selective area growth, and the preparation of large-area, arbitrarily orientated sapphire substrates (see Figure 4).

With this approach, to realise the required final GaN surface orientation, one must simply calculate the required direction for the GaN *c*-axis (as well as the corresponding *a*- or *m*-axis). Together, these GaN axes will uniquely specify the orientation of the c-plane sapphire that is inclined from the surface normal. By applying simple geometric algebra, it is possible to determine: the crystallographic plane for the sapphire surface; the direction of trenches that should be opened up; and the angle of inclination of the trench sidewalls, such that one of the sidewall facets will have the *c*-plane sapphire orientation that supports the desired semi-polar or non-polar GaN surface.

This orientation-controlled approach, which we refer to as Gen 3, has several advantages over other approaches. First, the lattice and crystallographic mismatches that plague planar semi-polar and non-polar heteroepitaxy are no longer an issue. Instead, formation of semi-polar and non-polar material becomes an exercise in *c*-plane growth of GaN on *c*-plane sapphire – a topic that the III-nitride community has mastered for a few decades. Second, orientation-controlled epitaxy employs selective-area overgrowth, a technique proven to be effective in reducing the densities of threading dislocations. And third, this approach is capable of producing, at least in principle, every possible non- and semi-polar orientation by design.

Using *r*-plane and (22$\bar{4}$3) plane sapphire, with a trench angled at 58° and 75°, we have prepared (11$\bar{2}$2) and (20$\bar{2}$1) GaN, respectively (see Figure 5). What's more, by combining orientation-controlled epitaxy with the nitridation of *c*-plane sapphire, we have been able to change the growth of GaN on (0001) sapphire sidewalls from the (0001) plane to the (000$\bar{1}$) plane, making it possible to produce the (20$\bar{2}$1) plane on GaN-on-sapphire. Together these three demonstrations show that it is possible to produce any semi-polar GaN orientation of GaN-on-sapphire.

Unfortunately, orientation-controlled epitaxy is not a perfect solution, as nasty stacking faults remain present in these Gen 3 layers (Figure 6). Again, it is the tenacity of stacking faults that presents an

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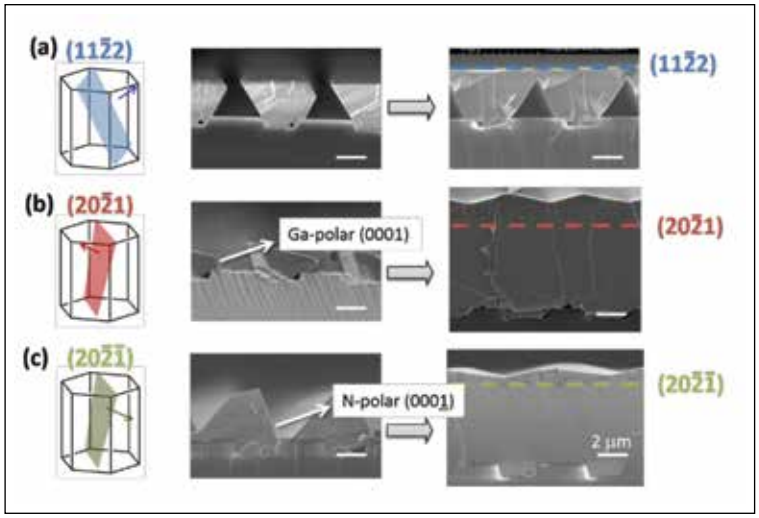


Figure 5 Cross-sectional scanning electron microscopy images of (a) (11$\bar{2}$2), (b) (20$\bar{2}$1), and (c) (20$\bar{2}\bar{1}$) GaN films grown on sapphire substrates. Left and right columns of scanning electron microscopy images correspond to a short growth time before coalescence and a long growth time after coalescence, respectively.

impasse for mass-producible, semi-polar GaN-on-sapphire.

After reviewing a large volume of experimental work, we conclude that basal plane stacking faults are typically generated in non- or semi-polar GaN growth when the N-polar basal plane (000$\bar{1}$) front is brought into contact with (or over) a foreign surface, such as the surface of SiO_2, during overgrowth. This led us to develop a refined version of our process, which we call facet-engineered, orientation-controlled epitaxy, or the Gen 4 process.

Eliminating the faults

According to the classical theory of crystal growth, the Wulff principle states that rapid-growing facets tend to become extinct, and that a crystal would be bound by slow-growing facets under equilibrium. In our Gen 4 process, our proprietary method accelerates the typically slow-growing N-polar plane, to the extent that the N-polar GaN basal plane disappears very quickly. This eliminates the formation of basal plane stacking faults.

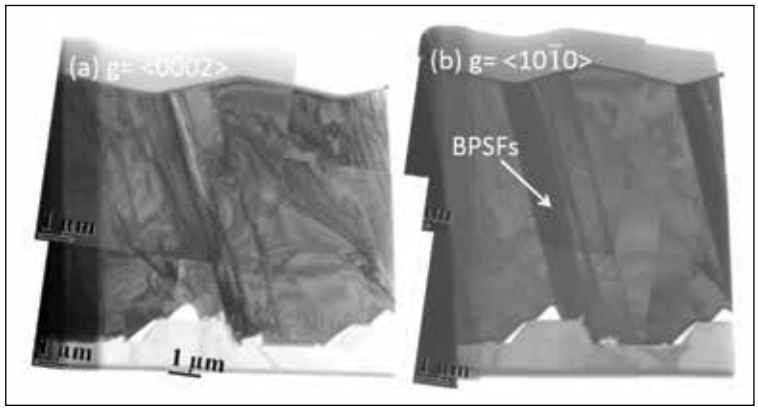


Figure 6. Cross-sectional transmission electron microscopy images of (20$\bar{2}$1) GaN grown on patterned sapphire by orientation controlled epitaxy (Gen 3) under two-beam conditions with g vectors of (a) <0002> and (b) <1$\bar{1}$00>, respectively.

To demonstrate the capability of our technology, we have incorporated this technique in the growth of (20$\bar{2}$1) GaN-on-sapphire. X-ray diffraction shows two peaks corresponding to GaN (20$\bar{2}$1) and sapphire (22$\bar{4}$3) diffractions, indicating that a single (20$\bar{2}$1) orientation of GaN has been achieved with direction parallel to the sapphire (22$\bar{4}$3) orientation (see Figure 7 (a)).

With this approach, we have eliminated the basal plane stacking faults in (20$\bar{2}$1) GaN. Work from Kazuyuki Tadamoto's group from Yamaguchi University, Japan, shows that in plan-view cathodoluminescence images, the non-radiative centres associated with stacking faults cause them to be exhibited as dark bands/straight lines. That feature is not present in our images – all we see are dark spots, due to the extension of threading dislocations from GaN-on-sapphire heteroepitaxy (see Figure 7(b)).

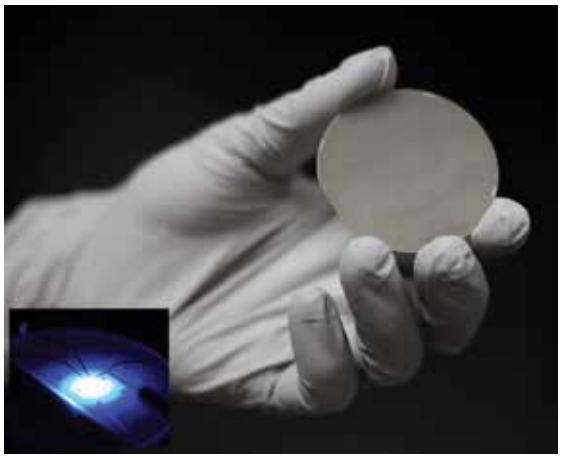
To take a closer look at the microstructure of our material, we have turned to transmission electron microscopy (TEM, see Figure 7(c)). Numerous TEM studies reveal no detectable stacking faults, confirming again that our Gen 4 technique is effective at suppressing basal plane stacking faults through the elimination of N-polar planes.

We have also inspected the defects over a 2-inch wafer, using plane-view cathodoluminescence (see Figure 7(d)). Inspecting different positions indicates that we can achieve large-area, stacking-fault-free (20$\bar{2}$1) on a 2-inch sapphire substrate. This is a very promising result, and more should follow, as our technology is applied to the growth of other semi-polar and non-polar orientation stacking-fault-free, GaN-on-sapphire substrates.

There's no doubt that it's a long road to reach defect-free, semi-polar and non-polar GaN layers on large-area, mass-producible wafers. This is highlighted by our plot of the density of stacking faults in semi-polar and non-polar GaN on various heteroepitaxial substrates (see Figure 8). Successive generations of growth technologies have initially reduced stacking fault densities from generally above 10^5 cm^{-2} to 10^3-$10^4$$cm^{-2}$, before we eliminated them. This eradication is a significant milestone toward mass-producible truly high-performance semi-polar LEDs, as even one stacking fault in these devices is one too many.

Having addressed the fundamental issue of the control and elimination of stacking faults for semi-polar GaN layers on sapphire, we are cautiously optimistic that semi-polar and non-polar LEDs on sapphire will impact, if not displace, mainstream

c-plane LEDs in the future. With improvements in the incumbents nearing saturation, the 'end of Moore's law' could be in sight for *c*-plane LEDs, forcing the community to look for and adopt new directions, both figuratively and (in our case) literally.



Further reading

Y. J. Sun *et. al.* J. Appl. Phys. **92** (2002)
B. A. Haskell *et. al.* Appl. Phys. Lett. **86** 111917 (2005)
N. Okada *et. al.* Appl. Phys. Express **2** 91001 (2009)
P. deMierry *et. al.* Appl. Phys. Lett. **96** 31918 (2010)
B. Leung *et. al.* J. Cryst. Growth **341** 27 (2012)
Y. Honda *et. al.* J. Cryst. Growth **242** 82 (2002)

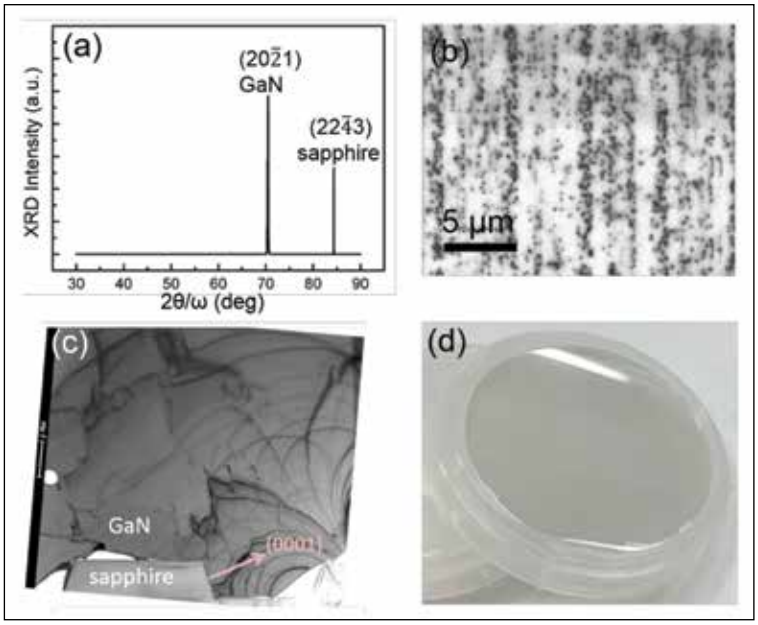


Figure 7. (a) X-ray diffraction 2θ/ω scan about (20$\bar{2}$1) GaN grown on sapphire. (b) Plan-view panchromatic cathodoluminescence image of (20$\bar{2}$1) GaN grown on sapphire cannot uncover any stacking faults. (c) Cross-sectional transmission electron microscopy image under two-beam condition taken along a diffraction vector of $g = <10\bar{1}0>$. (d) A photo of a 2-inch, stacking fault-free (20$\bar{2}$1) GaN grown on sapphire.

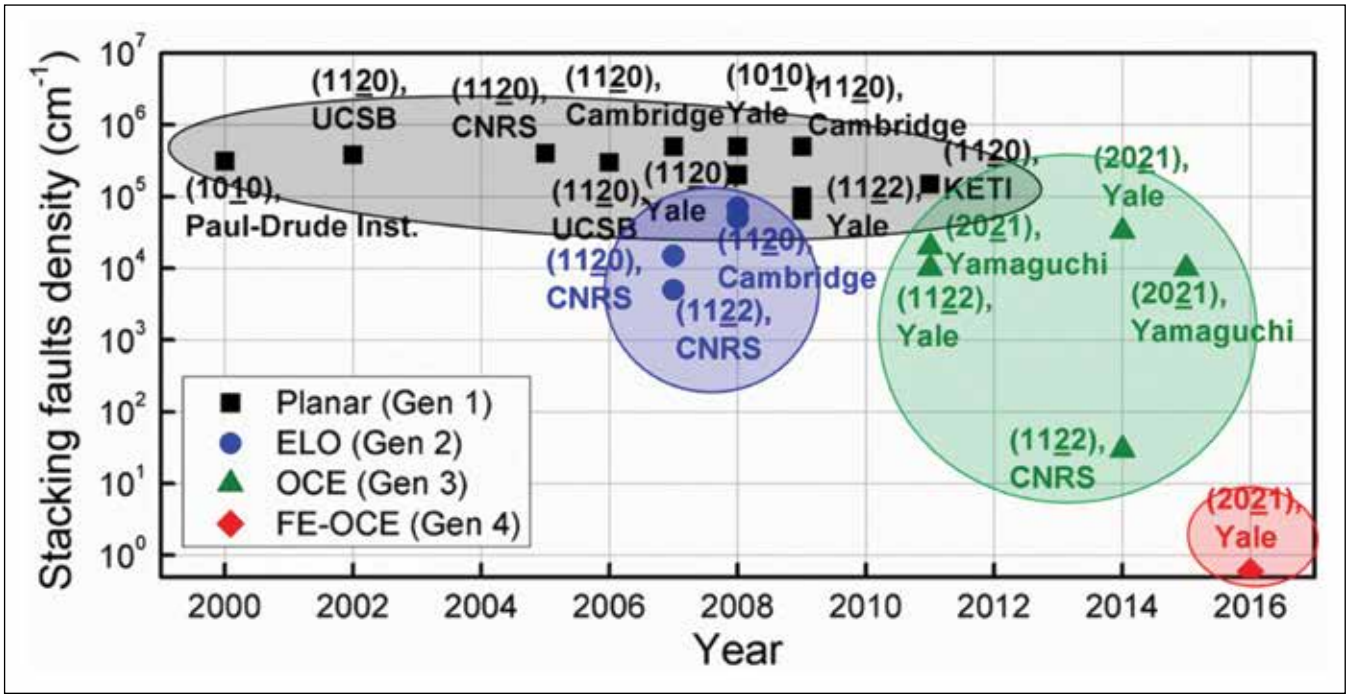
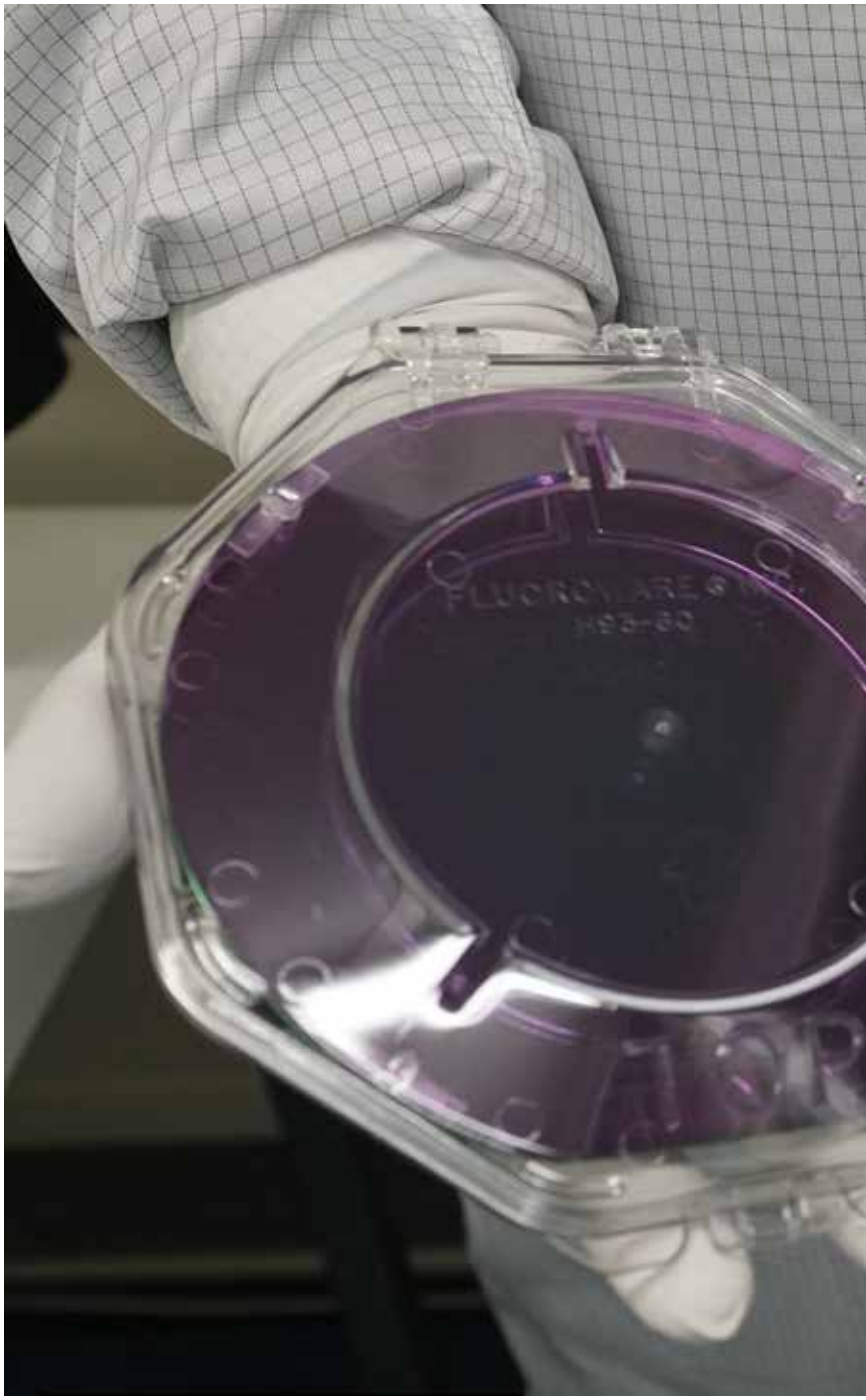


Figure 8. Successive generations of growth technologies have lowered and then eliminated the stacking faults density in semi-polar and non-polar GaN grown on sapphire substrates.

BRINGING SILICON CARBIDE TO THE MASSES



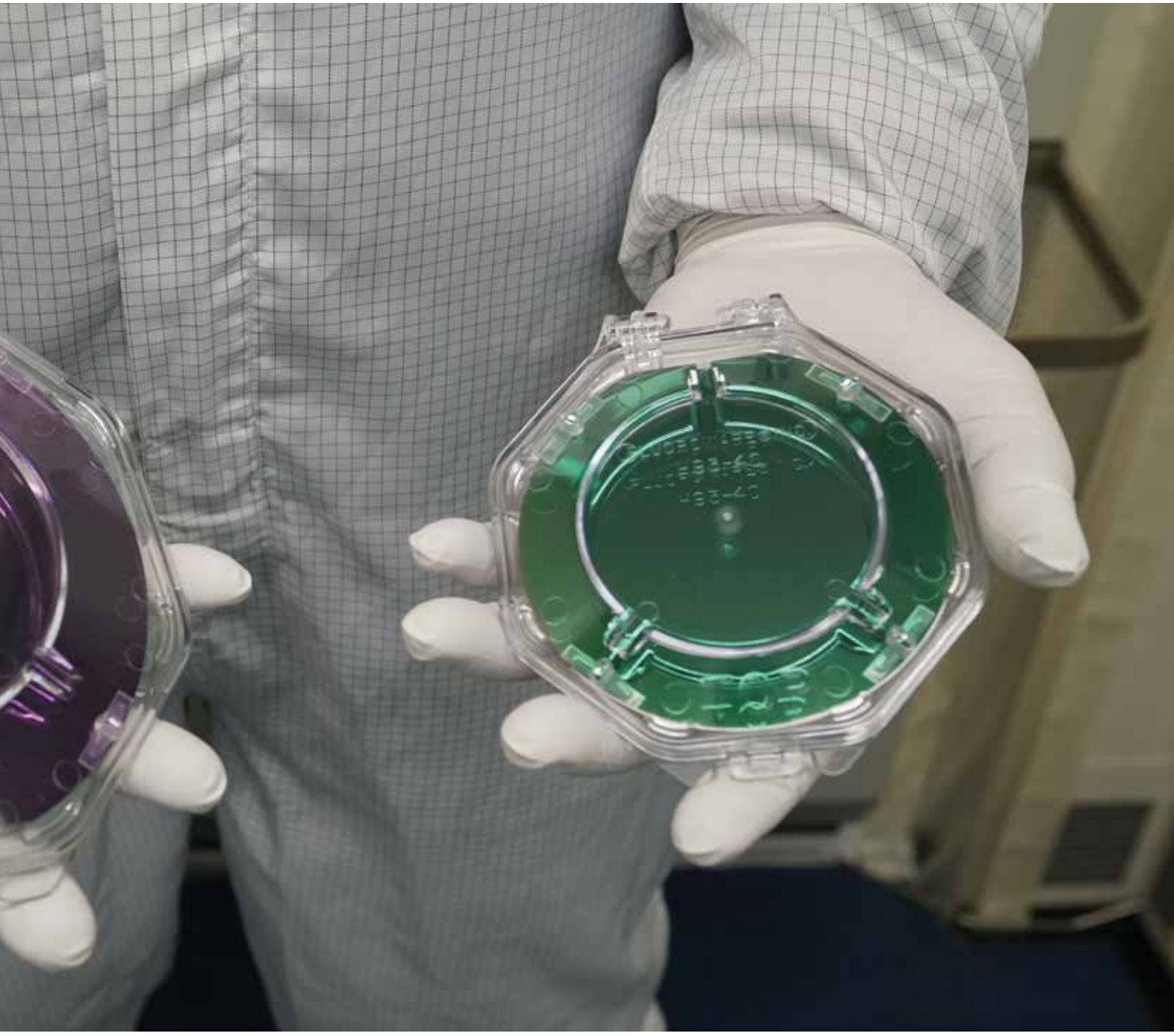
Turning to CVD for the growth of cubic SiC on silicon slashes material costs and delivers a hike in the scale of production

BY GERARD COLSTON AND MAKSYM MYRONOV FROM ADVANCED EPI MATERIALS AND DEVICES

SiC is well-established as an ideal compound semiconductor material for applications in power electronics, harsh environment sensing and biomedical devices. It excels in these areas because of its wide bandgap and strong bonding structure, attributes that allow it to operate at higher temperatures, block higher voltages and withstand even the nastiest of chemicals.

Manufacture of SiC devices tends to employ native substrates, which have commercially available since the early 1990s. This foundation is not ideal, however, as it is pricey – it can be a few orders of magnitude more expensive than silicon wafers. It can also be plagued with device killing defects, and it is limited in size. Although substrates are getting larger, by the end of last year the maximum diameter of commercially available SiC was only 150 mm.

An attractive way forward is to grow SiC on silicon. This slashes the cost of the substrate, which can now have a size of 300 mm or more. When grown on this platform, the SiC films have a cubic crystal structure, and are known as 3C-SiC (see Figure 1). This orientation is less common than the 4H and 6H polytypes used today to manufacture various



compound semiconductor devices, such as LEDs, power diodes and transistors.

Epitaxial growth of 3C-SiC on a silicon substrate has many commercial advantages, but process engineers have failed to fulfil its promises of low costs and high volumes. Progress has been held back by the high temperature of the conventional growth process employed to grow high-quality 3C-SiC on silicon. Typical temperatures are 1390 °C, and this restricts growth to non-standard, high-maintenance hot-wall CVD reactors that lag behind the capability of those associated with traditional silicon growth technology.

Growth temperatures are so high that they are very close to the melting temperature of silicon, causing several issues associated with the maintenance and lifetime of the CVD reactors.

Adding insult to injury, high growth temperatures produce significant thermal stresses between 3C-SiC and silicon. This warps the wafers, making them unsuitable for wafer-scale device fabrication (see Figure 2).

To reduce the cost per wafer, many SiC device manufacturers have moved to multi-wafer reactors to

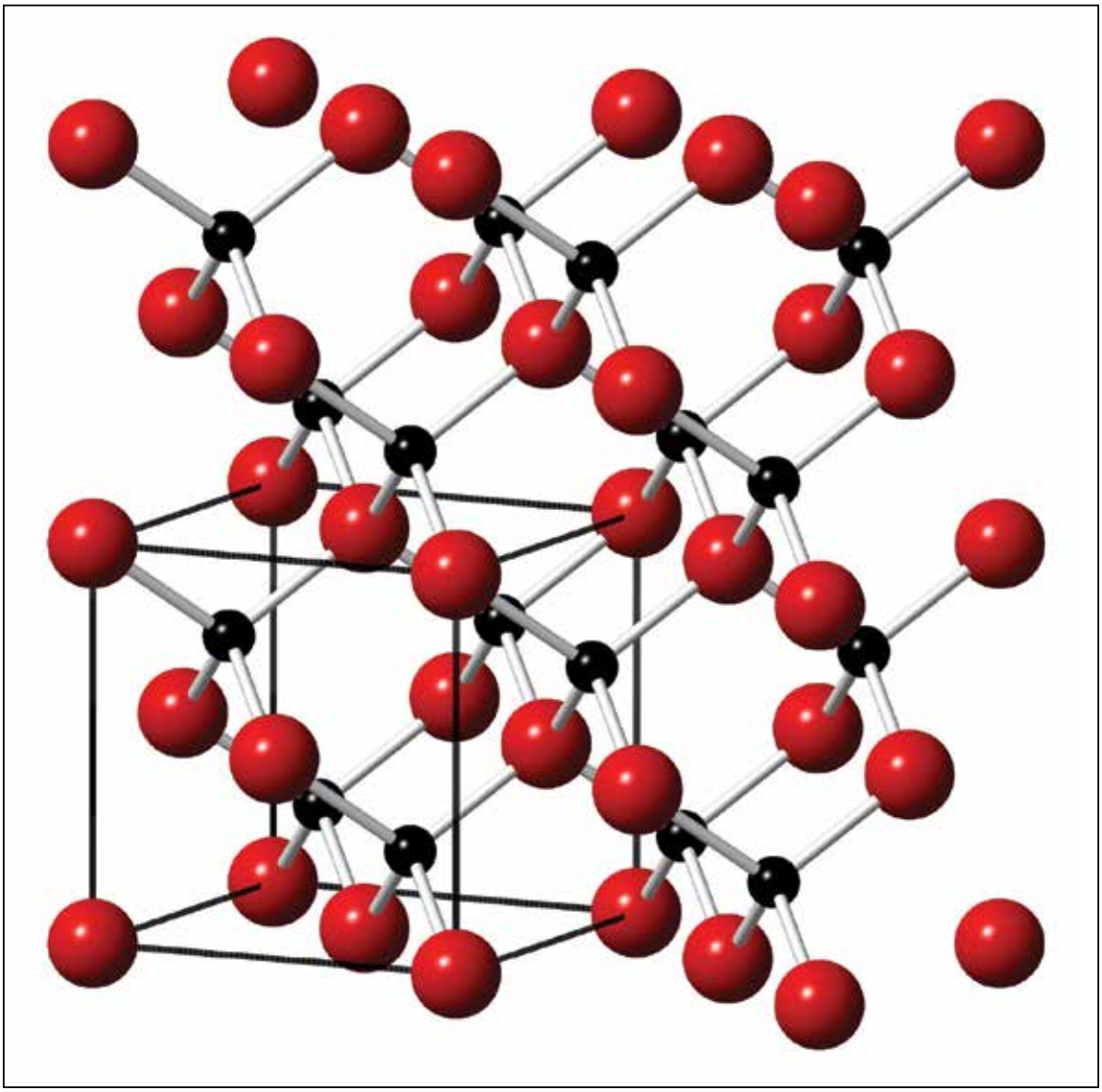


Figure 1. The crystal structure of 3C-SiC has the same basic structure as that of silicon and diamond. The red spheres represent silicon atoms and the black represent carbon. The cube shows the cubic unit cell.

increase throughput. However, it is tricky to realise satisfactory wafer-to-wafer uniformity, yield takes a hit, and there is a need to use far larger chambers.

So what's changed?

The founders of Advanced Epi started addressing these concerns at the University of Warwick, led by Maksym Myronov. Within the research group, efforts over the last eight years have been directed at the development of novel growth processes for various group IV semiconductors, including SiGe, germanium, SiC, GeSn and GeSnSi.

During the last few years, attention has turned to SiC, with the focus on commercial viability. Aware of the downsides of the hot-wall CVD growth process, the team has looked to the silicon industry for a solution. Success has followed, with research unveiling high-

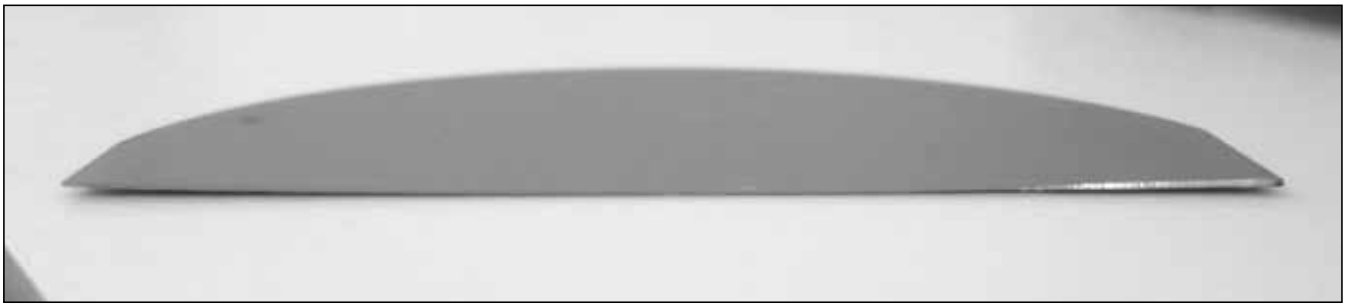


Figure 2. A typical cross-section of a 100 mm diameter high-temperature grown 3C-SiC epi-layer grown using a traditional high-temperature process. The thermal stresses cause bowing of the wafer.

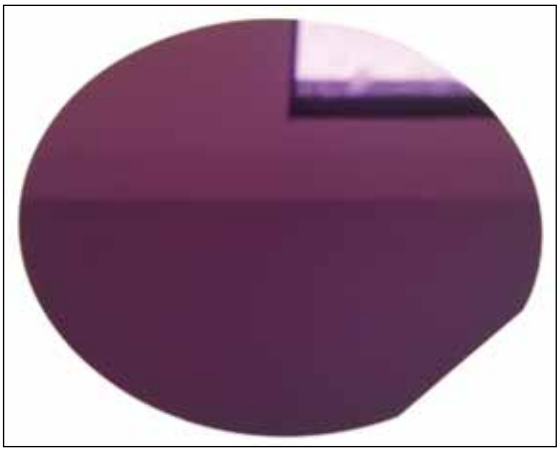


Figure 3. A 100 mm diameter 3C-SiC-on-silicon (001) epiwafer grown using Advanced Epi's low-temperature growth process. The mirror-like surface indicates low roughness. The film's colour is caused by the interference of light within the semi-transparent 3C-SiC epi-layer. It is an indicator of the excellent thickness uniformity across the wafer.

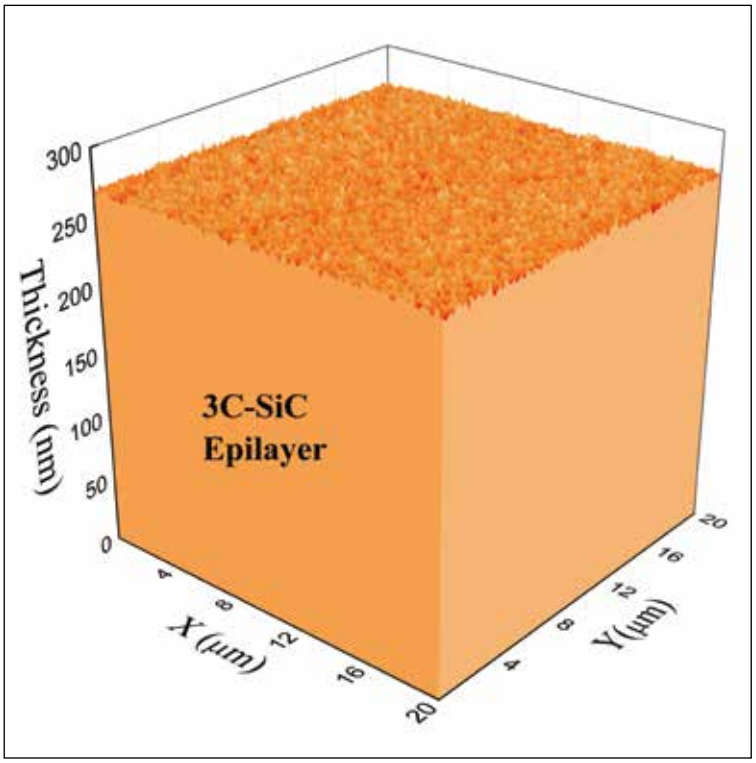


Figure 5. The root-mean-square roughness of Advanced Epi's 3C-SiC-on-silicon epi-wafers can be below 2 nm, according to atomic force microscopy scans of the surface.

quality crystalline growth of 3C-SiC at reduced growth temperatures. A spin-off, Advanced Epi Materials and Devices Ltd, followed, where both authors have leading roles. Together, we have spent the last six months overseeing the development of a wafer-scale process, improving material properties and refining the reproducibility of 100 mm diameter silicon wafers (see Figure 3).

Our growth process addresses the issues of scalability and cost with a novel, low-temperature growth process that takes place on standard silicon wafers (see Figure 4). Cubic SiC is grown at 1200 °C, a temperature low enough to allow the process to be carried out in any standard silicon-based cold-wall CVD system, such as an ASM Epsilon tool.

Merits of the single-wafer reactors used in the silicon industry include high throughput, uniform growth across a large diameter wafer, and excellent wafer-to-wafer reproducibility. These virtues deliver many advantages over the traditional high-temperature growth process of 3C-SiC, such as higher volume production, superior material quality, integration with other group IV and III-V semiconductors grown on silicon or silicon-on-insulator wafers, and scalability up to 300 mm wafers and beyond. An additional advantage is that as we use standard silicon-based growth processes, we will be able to offer 3C-SiC on silicon material on a similar scale and cost to that of silicon epitaxy, once we have scaled up to volume production.

The high crystalline quality of our 3C-SiC epilayers has been verified by in-depth characterisation. Studies show that our monocrystalline 3C-SiC is state of the art, with a surface roughness below 2 nm, even for growth rates exceeding 10 μm per hour (see Figure 5).

Another advantage of the lower growth temperature process is a significant reduction in residual wafer bow. Accurate measurements using stylus profilometry reveal that warp is not more than 30 μm for 3C-SiC grown on standard thickness, 100 mm

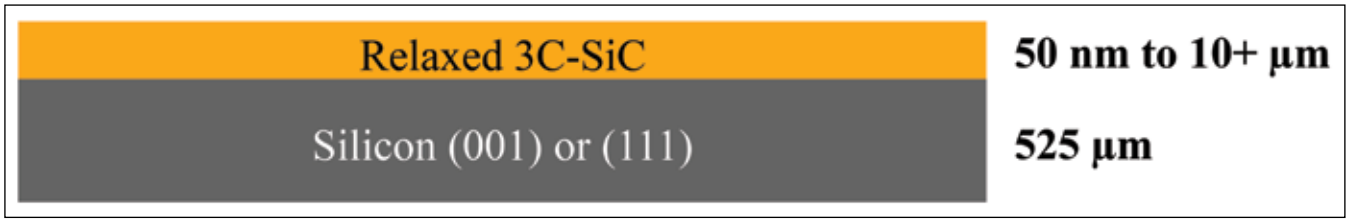


Figure 4. Advanced Epi's low-temperature process is capable of growing very thin, crystalline 3C-SiC films suitable for virtual substrates and sensitive sensing devices. Thicker layers of several microns are suitable for power electronic devices.

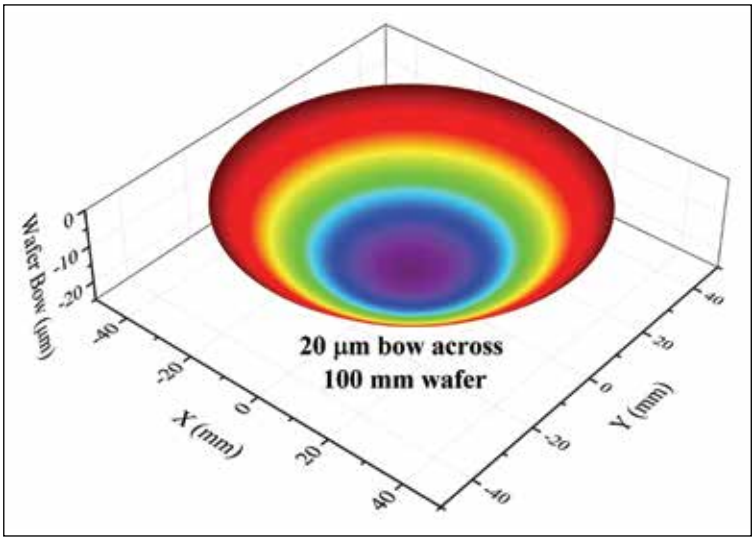


Figure 6. Wafer bow across a 500 nm-thick, 3C-SiC-on-silicon epiwafer grown on a standard 525 μm thick, 100 mm diameter silicon wafer. Parabolic wafer bow of 20 μm is measured up to the edge of the wafer.

diameter silicon wafers with an epilayer thickness of 500-1000 nm (see Figure 6).

Epiwafers as flat as this can be used directly for wafer-scale device fabrication and other processes – there is no need for complex techniques to compensate for bow. This suppression of wafer bow stems from the almost complete release of strain in the 3C-SiC epilayers, and minimisation of the thermal mismatch between the epilayer and the silicon substrate. If it is warranted, further reduction in wafer bow may be accomplished with standard compensation techniques used in the silicon industry, such as selective epitaxy or growing on thicker substrates.

Strengths of our 3C SiC include an unusually high resistance, an intrinsic room-temperature sheet resistance that exceeds 200 kΩ/sq, and an opportunity to introduce electrically active impurities into 3C-SiC films during epitaxy. Thanks to the latter, it is possible to produce *n*- and *p*-type 3C-SiC without having to resort to post-growth ion implantation or high-temperature annealing. This paves the way for the fabrication of a range of more complex 3C-SiC based electronic devices.

What applications?

Our 3C-SiC material is suitable for a range of applications. Its potential scale and competitive cost make it ideal for very high volume device production, where the advantages of 3C-SiC are required, but affordability plays a big factor. Due to these strengths, one area that we are targeting is sensing in harsh environments. For devices that range from simple temperature or pressure sensors to photodiodes with a spectral responsive ranging from less than 200 nm to around 550 nm, our 3C-SiC can form the basis of a new range of products that combine operating temperatures exceeding 500 °C with the capability to handle corrosive atmospheres and environments with thermal and mechanical shocks.

These properties are desirable for many applications within industrial, automotive and aerospace sectors. Our material can meet the cost and volume requirements, with tests showing no structural degradation to 3C-SiC epilayers during prolonged annealing at temperatures above 1000 °C.

The chemical resistance of 3C-SiC makes it an ideal material for various microelectromechanical systems (MEMS). Production of these devices can often involve the formation of suspended structures, which tend to be fabricated with a range of complex processes.

As 3C-SiC resists the effects of almost all chemical etchants, it is straightforward to fabricate suspended micro-wires for temperature sensing, and to make

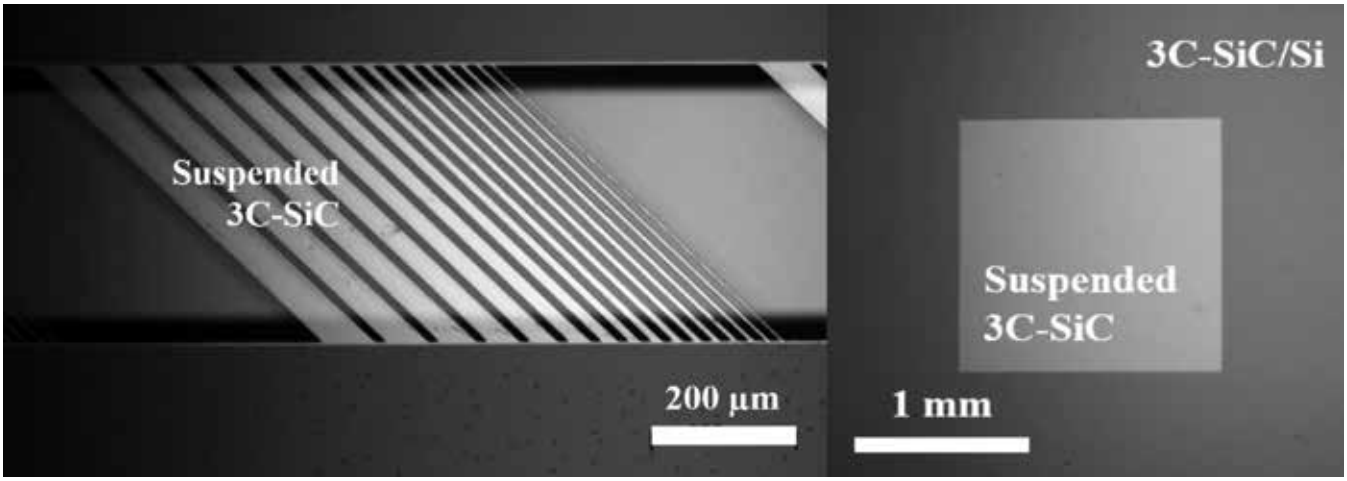


Figure 7. Suspended 3C-SiC microwires (left) and a square membrane (right) for MEMS applications fabricated using the anisotropic wet etching of the underlying silicon. As the 3C-SiC is resistant to almost all chemical etchants, fabrication of suspended structures is significantly easier than with other materials.

Connecting the photonic integrated circuits community

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B2B specialist publisher and event organiser Angel Business Communications, publisher of Compound Semiconductor Magazine and organiser of CS International and PIC International conferences has announced the launch of Photonic Integrated Circuits (PIC) Magazine, a new quarterly digital magazine which aims to provide timely, comprehensive coverage of every important sector within the photonic integrated circuits industry.

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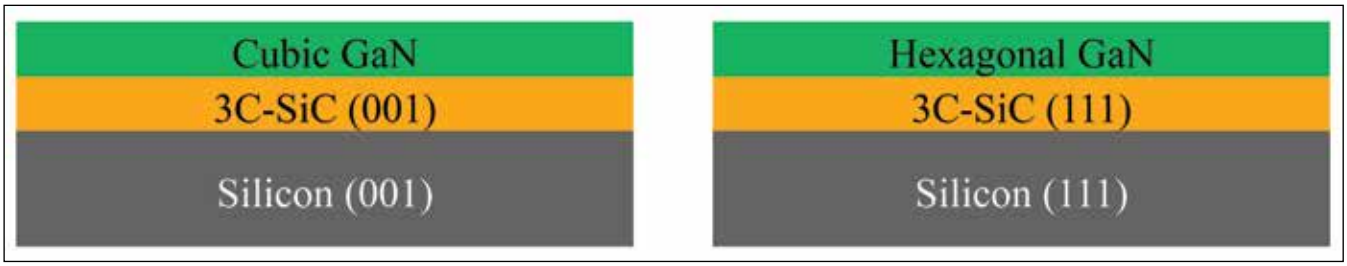


Figure 8. 3C-SiC is suitable as a virtual substrate for both cubic and hexagonal GaN, depending on the crystal orientation of the silicon substrate. In each case, lattice mismatch is approximately 3.5 percent.

membranes for pressure transducers (see Figure 7 for an example).Another potential market for 3C-SiC on silicon is as a template for GaN growth. Like SiC, GaN exhibits polytypism, with commercial blue and ultra-violet LED production involving growth of the hexagonal phase (see table 1 for material properties). When 3C-SiC is grown on a silicon (111) substrate, this produces the ideal template for hexagonal GaN, due to a lattice mismatch of approximately 3.5 percent at the SiC-silicon interface. Reducing mismatch between GaN and silicon is valued highly, because it holds the key to reducing the intrinsic defects found in GaN when this material is grown on highly mismatch substrates, such as silicon or sapphire. Note that the lattice mismatch between GaN and silicon is about 17 percent at room temperature.

One attract alternative is to use our material as a template for the growth of cubic GaN. This polytype has been very difficult to grow and nigh-on impossible to commercialise, but it can offer some exciting advantages for pushing emission of nitride LEDs to longer wavelengths and addressing the 'green gap' – the unwanted decline in LED efficiency from blue to green, where the human eye is at its most sensitive. The challenge is that before cubic GaN can address the green gap, growers of this material will need to overcome many challenges before it is suitable for producing product. The use of our technology is not limited to a range of optoelectronic devices. GaN grown with our technology can also aid high frequency and power devices, thanks to its increased thermal conductivity that increases the capability of the device to dissipate heat.

What's next?

Our technology promises to break new ground by driving the integration of SiC into the mass semiconductor market. As our 3C-SiC-on-silicon heterostructure can be implemented in several device

Figure 9. Advanced Epi's vision is for 3C-SiC-on-silicon material to make disruptive improvements within various industrial sectors.

Property	Silicon	3C-SiC	4H-SiC	Diamond	Gallium Nitride	
Crystal Structure	Cubic	Cubic	Hexagonal	Cubic	Cubic	Hexagonal
Lattice Constant (Å)	a = 5.431	a = 4.360	a = 3.073 b = 10.053	a = 3.567	a = 4.52	a = 3.186 b = 5.186
Bandgap (eV)	1.1	2.4	3.2	5.5	3.3	3.5
Electric Field Breakdown (V/cm)	3×10^5	3×10^6	3×10^6	10^6 - 10^7	5×10^6	5×10^6
Thermal Conductivity (W/cm/°C)	1.3	3.6	3.6	6-20	1.3	1.3

Table 1 Basic properties of relevant semiconductor structures. Both the cubic and hexagonal form of GaN are shown. Although 3C-SiC has a lattice parameter of 4.36 Å, when it is grown on the (111) orientation its surface lattice constant is the same as that of 4H-SiC (3.073 Å).

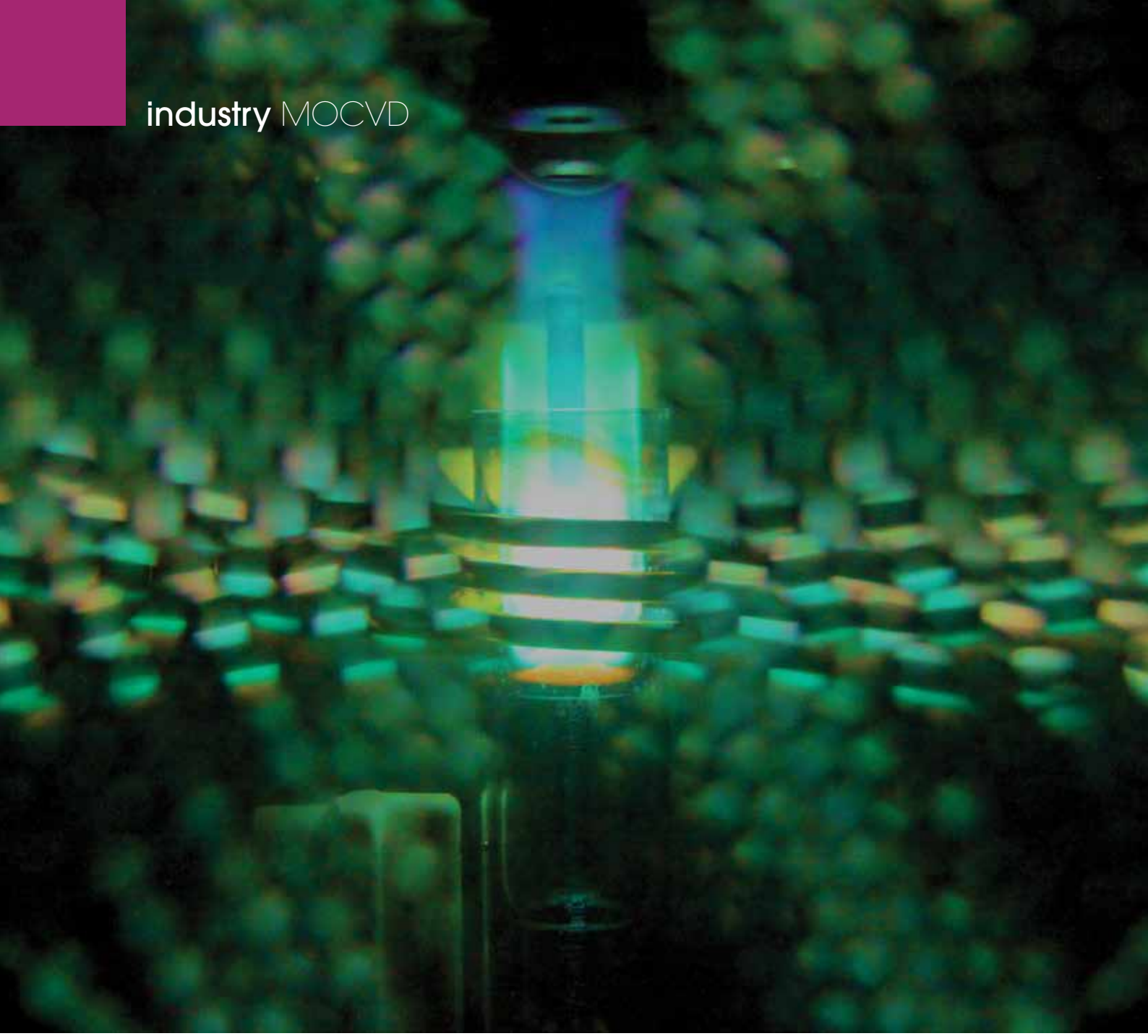
structures with standard silicon processing techniques, it has the potential to find application across a wide range of sectors (see Figure 9). Although we are in our infancy, we are developing the technology at an incredible rate, thanks primarily to the scale of the silicon-based growth method. Efforts are now being directed at developing various sensing device structures in-house, utilising the properties of 3C-SiC to fabricate temperature, pressure and ultra-violet sensors for applications in demanding environments.

To bring this material to the required commercial specification, using only standard silicon-based foundry processes, we are working with UK and international device manufacturers.
We are also working closely with growers of GaN to demonstrate that 3C-SiC material is a great foundation for the growth of both hexagonal and cubic GaN. These efforts demonstrate that our technology delivers the predicted advantages over other substrates, in terms of final device characteristics.

While developing our processes, we are constantly looking for new opportunities and collaborators in any field that could benefit from our 3C-SiC epiwafers. Our 100 mm epiwafers are ready for preliminary trials, and we can grow material to a range of specifications for different applications, including: thickness, crystal orientation and electrical properties.

Due to demand from our customers and collaborators, we are currently scaling up our production to include 150 mm diameter wafers, and under special request we can go up to 200 mm with the facilities that we currently have available to us.

While developing our processes, we are constantly looking for new opportunities and collaborators in any field that could benefit from our 3C-SiC epiwafers. Our 100 mm epiwafers are ready for preliminary trials, and we can grow material to a range of specifications for different applications, including: thickness, crystal orientation and electrical properties. Due to demand from our customers and collaborators, we are currently scaling up our production to include 150 mm diameter wafers, and under special request we can go up to 200 mm with the facilities that we currently have available to us



Scrutinising **metal-organics**

Dissolving group III sources in the right organic solvent lays the foundation for rigorous analysis of chemical purity

BY PAUL WILLIAMS AND ANN HUGHES FROM PEGASUS CHEMICALS

One of the factors governing the performance of all compound semiconductor devices – from VCSELs to LEDs, power devices and solar cells – is the quality of the metal-organic precursors used to grow the epilayers by MOCVD.

For high-yield, high-volume manufacture of state of the art devices, process engineers need to employ high-quality sources to ensure reproducible, consistent production of uniform films. These engineers must also carefully select their metal-organic precursors to ensure high-quality layers, and they should optimise the efficiency associated with MOCVD by controlling stoichiometry, layer thickness and surface conformity.

Left: The lit plasma torch used for chemical analysis

Another consideration for the process engineer is the level of purity required for an epilayer. This is not fixed, but depends on the role of the layer within the device. So the level of purity must be known – and it is the responsibility of the chemical supplier to provide this information.

To build and maintain customer confidence, the chemical supplier must use an accurate, reliable methodology for determining purity. Through analysis, data may be generated that controls the chemical manufacturing process, ensures quality and delivers batch-to-batch reproducibility. Efforts will include the analysis of organic contaminants, the oxygen level and the metal contaminants of the metal-organic precursors.

There are several methods for preparing metal-organics for chemical analysis, all with their pros and cons. At Pegasus Chemicals of Sandycroft, UK, we have recently added to the options, with an approach that excels in its simplicity and its robustness.

The most common methods for metals analysis of metal-organic precursors are inductively coupled plasma mass spectrometry and inductively coupled plasma, optical emission spectrometry. For both these techniques, the chemical for analysis must be prepared in such a manner that it can be introduced into the analytical tool as a liquid. Note that the front-end of both these spectroscopy systems are similar, comprising a sample container, liquid pump, spray chamber, nebuliser, inductively coupled plasma torch and RF coil (see Figure 1).

Maintenance of the inductively coupled plasma is accomplished by interacting an RF field with an ionised argon gas. The argon plasma that results reaches temperatures of 10000 °C. This is sufficient to completely atomise the elements in the sample, and allow for their analysis by optical emission or mass spectrometry, depending on the analytical tool.

For the analysis of liquid and solid chemicals using inductively coupled plasma techniques, there are three common methods for sample preparation: direct injection; digestion; and evaporation, followed by acid digestion. With direct injection, an organic solvent (matrix) is used to dissolve the sample, with the solution introduced directly into the inductively coupled plasma system. If digestion is adopted, the sample is digested or decomposed, before dissolving it in an acid and introducing to the inductively coupled plasma system. And if the sample is volatile, there can be an evaporative step, followed by acid digestion of non-volatiles (see Figure 2).

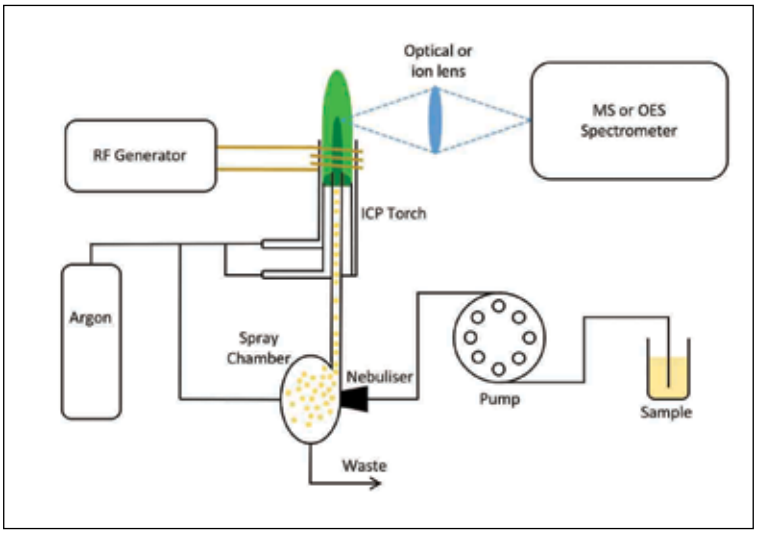


Figure 1: Schematic if sample introduction system and inductively coupled plasma torch.

Group III challenges

There are unique challenges associated with the analysis of the high purity metal-organic precursors used in the compound semiconductor industry. The three main sources – tri-methyl-aluminium (TMA), tri-methyl-gallium (TMG) and tri-methyl-indium (TMI) – are all pyrophoric, catching fire the instant they are exposed to air. This complicates their analysis, as well as their manufacture and shipping. Another impediment is that a common approach is not easy, as TMA and TMG are liquids, whereas TMI is a solid. From a supplier's perspective, what is wanted is a single, specialised, sample preparation technique that is safe and allows the preparation of samples from all the metal-organic precursors.

Digestion is arguably the most well used method for preparing samples for inductively coupled plasma analysis. Essentially, it involves transferring the sample to a liquid state, before it is introduced into the inductively coupled plasma system and decomposed in the plasma. The choice of acid depends on the sample being analysed, and on the metals being determined. Dilute acids are often used, such as nitric acid (HNO_3), hydrochloric acid (HCl), sulphuric acid (H_2SO_4) and hydrofluoric acid (HF).

Preparation may also involve heating the sample and acid mixture for sufficient time to ensure adequate digestion. There are also alternative techniques, such as microwave or UV digestion. But whatever route is taken, the result is usually a clear, particle-free dilute aqueous acid solution that can be easily introduced into the inductively coupled plasma.

In general, this method is usually representative of the sample. What's more, the aqueous acid is easily

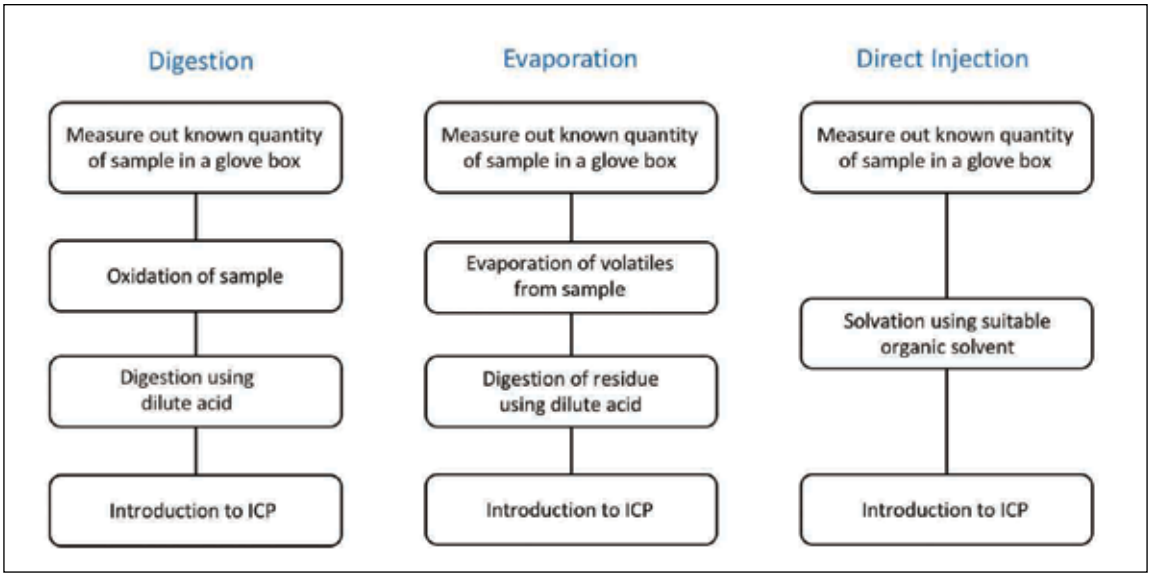


Figure 2: Schematic diagram highlighting the key steps in the three sample preparation techniques.

nebulised (becomes a mist), it passes through the inductively coupled plasma easily, and it is easy to standardise. However, when it comes to the group III metal-organics, there is one immediate issue: they must be mixed with an aqueous acid to ensure digestion. As these chemicals react vigorously with water, typically catching fire, it is tricky to mix them with an acid. However, back in the early 1980s, several groups published work that revealed that a controlled reaction is possible by introduce freezing acids to the chemical. Unfortunately, the reactivity of TMA is so high that it is not compatible with this technique.

As the metal-organics are volatile, evaporative techniques are an option for sample preparation. The material for analysis is placed in a closed container with an inlet and outlet tube, and evaporation takes place under an inert gas using a moderate temperature. Once evaporated to dryness, the residue within the container is digested with a suitable acid.

One of the merits of the evaporative sampling technique is that it overcomes the significant handling and safety issues related to adding a pyrophoric chemical to an aqueous acid. In addition, this approach safely yields an aqueous acid solution, which can be easily nebulised and passed through the inductively coupled plasma, enabling analysis of the metal-organic precursors. However, this method hinges on the evaporated sample providing a very accurate representation of the original sample – and that's not guaranteed, as any volatile contaminants could be lost during the evaporation process.

We are able to address this concern with direct injection. Our approach, which is based on previous work using a technique now optimised by Pegasus, involves using an organic solvent to dissolve the sample for analysis, before it is introduced into the inductively coupled plasma.

There are several challenges associated with this sample preparation technique. It is critical that the organic solvent, or solvents, used for dissolving the organometallic chemical give a free flowing, non-pyrophoric, clear, particle-free liquid that can be nebulised and introduced into the inductively coupled plasma.

That's not the only challenge, as there can still be issues in the actual measurement and preparation of standards. Previously, the metal-organic sources were in an aqueous acid solution, and now they must be in the same organic solvents, the matrix. It is also crucial to ensure that the plasma is not extinguished. This may require a different nebuliser design and the optimisation of the inductively coupled plasma.

Success with our approach requires the selection of the right organic solvent for dissolving the organometallic chemical precursor. However, once sample preparation and the sample introduction system are optimised, this method is capable of providing a representative analysis of the sample, as all of the organometallic chemicals are introduced to the inductively coupled plasma for analysis.

Whatever method is adopted, the chemical industry must provide a certificate of analysis that presents a list of metal contaminants. Typically the certificate details the method of analysis and the approach for the handling of the data produced by the analytical tool. However, it can also be argued that the methodology used for sample preparation could be included, as it is equally important. This information is particularly needed when highly reactive pyrophoric chemicals are being analysed, as it is not always possible to safely use standard aqueous acid digestion techniques. The direct injection method using an organic matrix addresses this, and in our view it is the leading approach for accurate analysis of metal-organic chemicals.

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Schottky barrier diodes: Cutting carbon with *m*-plane GaN

Switching from the *c*-plane to *m*-plane cuts the carbon concentration in Schottky barrier diodes, leading to lower leakage currents

A TEAM of Japanese engineers are claiming to have broken new ground with Schottky barrier diodes that feature the first lightly *n*-doped, non-polar GaN.

The researchers from the National Institute of Advanced Industrial Science and Technology (AIST) in Tsukuba, are not alone in trying to improve device performance with free-standing substrates, which ensure superior material quality. However, if the far more common *c*-plane of GaN is adopted, there is a priced to pay for a reduction in imperfections in material quality: carbon contamination. The unwanted contaminant is introduced during the MOCVD growth process, when incomplete decomposition of the gallium source leads to a high level of carbon in the epilayers, resulting in inferior electrical performance in the devices that follow.

Although it is possible to cut the level of carbon on the *c*-plane, it requires high growth pressure or high V/III ratios, equating to either an increased ammonia flow or a reduced flow for the gallium source. Whatever the approach, the upshot is a cut in productivity.

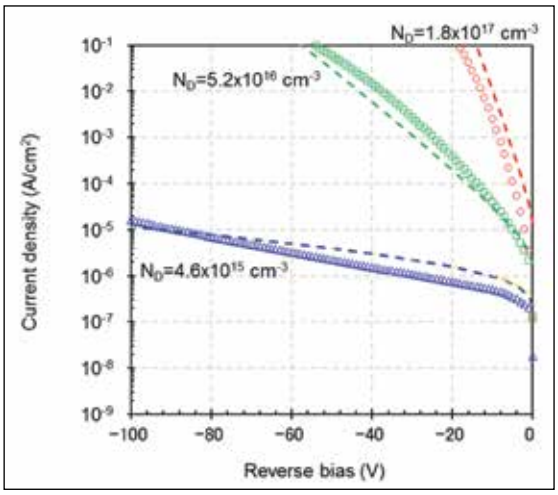
Lead author of the team from AIST, Hisashi Yamada, claims that the situation is markedly different with *m*-plane GaN. With this substrate, very low carbon concentrations can be realised under very low V/III ratios. "This leads to high productivity for the very thick vertical devices that can achieve high breakdown voltages," says Yamada.

He and his co-workers fabricated their diodes on HVPE-grown, *m*-plane GaN made by Mitsubishi Chemical. This foundation, which had a 5° offcut towards the [000$\bar{1}$] direction, has a threading dislocation density of less than 5 x 10^6 cm^{-2}.

This choice of off-cut is based on Yamada's previous experience, gained at UCSB, where he formed LEDs on *m*-plane GaN. "Without the off-cut, the surface consists of multi-facets, which would impact device properties."

Today, the downsides of substrates of *m*-plane GaN are high costs and limited size. However, Yamada believes that this could change, citing last year's report of 2-inch diameter, *m*-plane GaN, by Mitsubishi. "I expect substrates will be available in the market in the near future."

To determine the ideal growth conditions on the *m*-plane of GaN, the team produced GaN epilayers at 1120 °C, 1160 °C and 1200 °C, using V/III ratios of 1,000, 2,000 and 4,000. Secondary-ion mass spectroscopy revealed that oxygen and carbon levels were below the detection limits of 6 x 10^{15} cm^{-3} and 4 x 10^{15} cm^{-3}, respectively. For silicon, the lowest concentration, 1 x 10^{17} cm^{-3}, was obtained with a V/III ratio of 1,000 and a growth temperature of 1120 °C. Silicon is believed to come from the reactor hardware, and could be eliminated by switching to SiC-coated graphite.



Reductions in carrier concentration lead to far lower leakage currents in GaN Schottky barrier diodes. Dashed lines are calculated values, using a thermionic field emission model.

Schottky barrier diodes with a 4 μm-thick, silicon-doped GaN layer were formed using the best conditions – a growth temperature of 1120 °C and a V/III ratio of 1,000. Atomic force microscopy on the GaN epilayer revealed a root-mean-square surface roughness of 0.6 nm, with steps and terraces orientated towards [000$\bar{1}$].

To investigate leakage currents, the team measured current-voltage characteristics on diodes with different doping levels in the GaN epilayer. Using a reverse bias of up to 100 V, Yamada and co-workers found that reductions in carrier concentration led to far lower leakage, even without the use of field plates (see Figure).

Yamada and his colleagues are now focusing on establishing the relationship between the off-cut angle of the *m*-plane substrate and device performance.

Reference

H. Yamada *et. al*. Appl. Phys. Express **10** 041001 (2017)

Uniting lasers and photodetectors in GaN

Switching to the semi-polar plane increases the responsivity of a waveguide photodiode

A collaboration between researchers in the US and Saudi Arabia has integrated a GaN laser and photodetector on the same chip, to create a device that offers optical power monitoring and on-chip communication.

The team believes that their device is the first to operate in the visible spectrum and deliver photonic integration via the use of the same InGaN/GaN quantum-well active region.

"Such a device is important for achieving a feedback loop to enable constant luminous lighting and realising high date rate, visible light communication systems – a step towards high-quality, smart lighting," argues corresponding author Boon Ooi from King Abdullah University of Science and Technology.

One of the merits of the work is that it avoids the strong internal electric field on the *c*-plane, which causes a large separation between the absorption and emission peaks. The approach of Ooi's group, working with researchers at the University of California, Santa Barbara, and King Abdulaziz City for Science and Technology, is to fabricate their photonic chip on the semi-polar plane of GaN.

Their chip features a 505 μm-long, 405 nm laser. Near its rear facet, separated by 5 μm, is a 90 μm long waveguide photodiode. Between the laser and photodiode is an isolation trench, formed by focused ion beam milling. This allows the two devices to operate independently, thanks to an isolation resistance of about 1 MΩ.

Integrating a GaN laser and waveguide photodetector could aid smart lighting, by allowing the monitoring of optical power.

Measurements from the front facet of the laser, which is operated continuously, reveal a threshold current of 130 mA and a slope efficiency of 0.4 W/A. This is in good agreement with measurements of the waveguide photodiode at zero bias, which show a significant increase in photocurrent when the laser diode's current is increased to 130 mA. At higher drive currents, lasing kicks in, and there is a significant increase in the photocurrent in the waveguide photodiode. This behaviour shows that the waveguide photodiode can be used for on-chip power monitoring.

Biasing the photodiode leads to enhanced optical responsivity. When driving the laser with 5 μs pulses at a 10 percent duty cycle to minimise heating, an increase in the bias from 0 V to 10 V leads to an increase in responsivity – the ratio of the photocurrent to the incident optical power – from 0.0018 A/W to 0.051 A/W. According to the team, this figure of merit is far higher than that for equivalent photodiodes on the *c*-plane, which have a responsivity of 0.001 A/W to 0.01 A/W.

Frequency measurements on the waveguide photodiode indicate a 3 dB bandwidth of 230 MHz. This is vastly superior to GaN Schottky barrier photodiodes and *p-i-n* photodiodes, which have figures of 5.4 MHz and 10-20 MHz. Ooi attributes the far higher frequency of their waveguide photodiodes their small size, stemming from the narrow ridge design, and the higher responsivity in the semi-polar plane. The higher speed is claimed to showcase the potential of the chip as an integrated receiver for on-chip communication and visible light communication.

Even higher levels of performance should be possible. According to Ooi, the DC and high frequency photoresponse characteristics of the waveguide photodiode could be improved by optimising the design, including the form factor and the facet angle. "By reducing the junction capacitance to about 5 pF, a 3-dB bandwidth of more than 500 MHz is expected." Meanwhile, the efficiency of the laser could be increased by optimising the facet and turning to high-quality high-reflection coatings.

Plans for the future include the development of a multiple-section integration technology. This could enable complex monolithic on-chip integration of III-N light emitters and receivers for smart lighting, displays, and visible light communication.

Adding more functionalities could lead to photonic integrated circuits for optical switching, clocking and optical interconnects.

Reference

B. Ooi *et. al.* Appl. Phys. Express **10** 042201 (2017)

Scrutinising traps in SiC MOSFETs

Simple approach highlights the benefits of nitridation

RESEARCHERS in Japan are pioneering a new, simple approach to quantifying traps at the SiO_2/SiC interface of the SiC MOSFET.

Lead author of the paper detailing the work, Tetsuo Hatakeyama from the Advanced Power Electronics Research Centre at Tsukuba, says that this effort is motivated by the urgent need to address weaknesses at the SiO_2/SiC interface, which is the most important part of the SiC MOSFET.

The performance of this device is held back by a high MOS channel resistance, resulting from the low mobility at the SiO_2/SiC interface. A high density of traps at the interface is probably the root cause of this weakness.

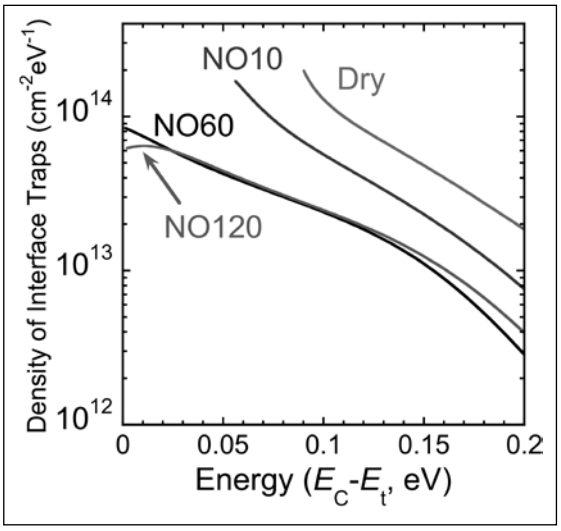
Measuring the density of traps at interfaces is normally accomplished by high-low capacitance-voltage measurements. But this is not suitable for the oxide-semiconductor interface in SiC MOSFETs.

When making high-low capacitance-voltage measurements of any device, it is assumed that traps only respond to low frequencies, and are not influenced by the high frequencies, typically 100 kHz to 1 MHz. However, that's not the case with SiC MOSFETs. "They respond to the high frequency, because of the low excitation density to the conduction band," explains Hatakeyama. The upshot is an underestimate of the density of traps near the edge of the conduction band of this SiC MOSFET.

To address this weakness, Hatakeyama and his colleagues, working with researchers at the University of Tsukuba, have developed an approach based on the combination of Hall measurements and split capacitance-voltage measurements. With the later, the capacitance of the gate is split into a source-gate component, and a gate-substrate component.

"In the case of the split-CV method, one terminal is connected to the gate electrode," explains Hatakeyama. "The other terminal is connected to the source or drain, or both. The substrate is grounded."

To determine the trap density with the approach of Hatakeyama and co-workers, the first step is to measure the free carrier density as a function of gate voltage with Hall effect measurements. After this, the split-CV method determines the capacitance between the gate and channel as a function of gate voltage. Integrating this reveals the total density of carriers at the interface induced by the gate voltage. The trapped carrier density is given by taking this figure for the total density of carriers at the interface, and subtracting the free carrier density, which has been given by Hall measurements. Via calculation, the density of interface traps near the conduction band is known.



Post-oxidation annealing of SiC MOSFETs in nitric oxide for either 60 minutes or 120 minutes leads to a substantial reduction in the density of interface traps.

The Japanese team has used its technique to determine the effect of nitridation on the density of interface states in SiC MOSFETs. Nitridation is a common method for improving this interface – it is used by the likes of Wolfspeed, Rohm, ST and Mitsubishi. Working with devices that have a thermally grown oxide with a thickness of 50 nm, the team annealed one sample in nitric oxide for 10 minutes, another for 60 minutes, and a third for 120 minutes. A non-annealed device acted as the control.

Measurements of field effect mobility highlighted the benefits of nitridation, with the best result, a value of nearly 40 $cm^2 V^{-1} s^{-1}$, coming from a sample undergoing treatment for 60 minutes. Note, however, that this mobility is far less than that for bulk 4H SiC, which is typically 1000 $cm^2 V^{-1} s^{-1}$. Dividing the free carrier density by the total carrier density gives the free carrier ratio, which increased from 4 percent to 30 percent with nitridation. However, even 30 percent is a low figure, which may partially account for the far lower mobility at the SiO_2/SiC interface compared to bulk SiC.

Calculations show that nitridation enables a 75 percent reduction in the density of interface states at 0.1 eV below the conduction band (see Figure). However, this density is still in excess of 10^{13} $cm^{-2} eV^{-1}$.

Hatakeyama and co-workers are now planning to characterise SiO_2/SiC interfaces in a variety of SiC MOSFETs, in the hope that this will uncover a technique for improving this critical part of the device.

Reference

T. Hatakeyama *et. al.* Appl. Phys. Express **10** 046601 (2017)

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VENDOR VIEW Proton Site

On-site hydrogen generation: smart choice to improve process results

Hydrogen is widely used to support a variety of industrial applications worldwide, due to its ability to meet the specific needs of high purity industrial applications, ranging from semiconductor manufacturing and epitaxy to heat treating and materials processing.

Relying heavily on hydrogen to maintain process results, many operations personnel are responsible for evaluating which gas supply method will best suit their operation. Over time, this task can become daunting, because as businesses grow, increasing amounts of hydrogen are needed to satisfy elevated levels of production demand. This spike in hydrogen usage has translated into a collection of issues for facility operation.

Hassles such as inefficient production practices, fire permit restrictions, space limitations, increased costs, dangerous hydrogen storage and handling can make gas sourcing especially problematic.

Offering clear advantages over older, conventional methods of hydrogen supply such as delivered gas, dissociated ammonia and exo or endo gas, hydrogen generated on-site is a drier and safer alternative. A high performance solution to suit businesses small and large, on-site gas generators satisfy demand by producing hydrogen at its point of use with no inventory of flammable or poisonous gas. Hydrogen generation systems are easy to permit, easy to install, and operate automatically. Market data shows more and more stakeholders are making the switch to gas generators, eliminating the need for delivery and storage of hazardous gases within the industry.

With more than 2,500 systems installed in over 75 countries, Proton OnSite hydrogen generators are consistently creating value around the world. Utilizing advanced Proton Exchange Membrane (PEM) electrolysis, with a high differential pressure design, our on-site hydrogen generators produce very pure hydrogen in a safe, reliable, and cost effective package.

Our industrial customers are particularly impressed with the fact that they are able to realize rapid paybacks while dramatically improving facility safety. The on-site generators eliminate the need for stored hydrogen, while meeting the daily requirements of various industrial processes. Thus, providing an attractive return on investment for customers and improving site security, safety and personnel productivity.

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