COMPOUND SEMICONDUCTOR

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

VOLUME 30 ISSUE II 2024

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INSIDE
News, Analysis, Features, Editorial View, Research Review and much more

Unconventional crystallinity

Cubic GaN promises to address the low efficiency of the microLED, a key ingredient in head-mounted displays

Tuneable lasers: The elusive trifecta

Integrated tuneable laser assemblies offer wide tuning, nanosecond switching and a narrow linewidth

A novel form of Schottky diode

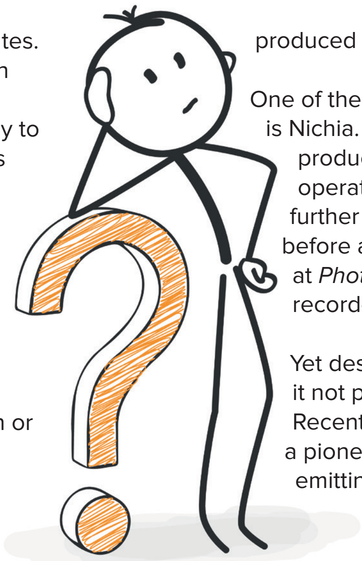
Reliable and efficient, the merged *p-i-n* SiC Schottky diode has a low forward voltage and high surge-current capability

VIEWPOINT

By Richard Stevenson, Editor

A better solution?

The VCSEL has many wonderful attributes. It's efficient, it can be modulated at high speeds, it's compatible with on-wafer testing, and it emits a circular beam that is easy to focus. For all these reasons and more, VCSELs emitting in the infrared have already enjoyed two killer applications, as transmitters in datacom links and as optical sources in facial recognition systems.



Due to the many strengths of the VCSEL, much effort has been devoted into extending its emission to visible wavelengths. However, stretching from the infrared to either the green or the blue has proved anything but easy.

The biggest challenge is making the mirrors that surround the light-emitting region. For infrared VCSELs, both mirrors are formed by interleaving layers of AlGaAs and GaAs. This pairing is an ideal duo, enabling a significant difference in refractive index that ensures high reflectivity, while offering good lattice matching that prevents the build-up of significant strain, as well as the opportunity to provide electrical conductivity, essential for the injection of carriers that are crucial to device operation.

To realise lasing in the blue or green, there's a need to switch material system, with that based on GaN the obvious front-runner. However, the nitride material system doesn't have a convenient pair of materials for making strain free, high-conductivity mirrors with a high reflectivity.

That's not proved a show stopper. Progress has been made with novel architectures, often involving one nitride-based mirror and another made from dielectrics, with GaN-based VCSELs now emitting more than ten milliwatts. But production is complex, and it's not yet clear whether blue and green VCSELs will ever be produced in volume.

One of the trailblazers of the GaN-based VCSEL is Nichia. Back in 2008, it claimed to have produced the first GaN-based VCSEL operating at room temperature. Reports of further progress followed through to 2012, before a long period of silence, shattered at *Photonics West* 2021 with claims of a record-breaking green emitter.

Yet despite Nichia's hard-won success, it not putting all its eggs in one basket. Recently, this company has teamed up with a pioneer of the photonic-crystal surface-emitting laser (PCSEL), Susumu Noda from Kyoto University. Together they have produced GaN-based, green-emitting variants of this class of device with an output of 50 mW and an emission wavelength that can be arbitrarily tuned (for more details, see p. 51).

What's particularly appealing about the PCSEL is the simplicity of the fabrication process. Epitaxial growth is relatively straightforward, and the photonic crystal is defined by the well-known techniques of electron-beam lithography and reactive-ion etching.

However, there's still much work to do. Wall-plug efficiencies of Nichia's PCSELs are around 0.1 percent, way short of the values needed for practical devices. So, it will be interesting to see what the company does next. Having wrestled with the VCSEL for many years, is it going to drop this project now and just focus on pursuing the PCSEL, given its great prospects for high-volume manufacture? It's a tough question – and one that not just I will want to know the answer.

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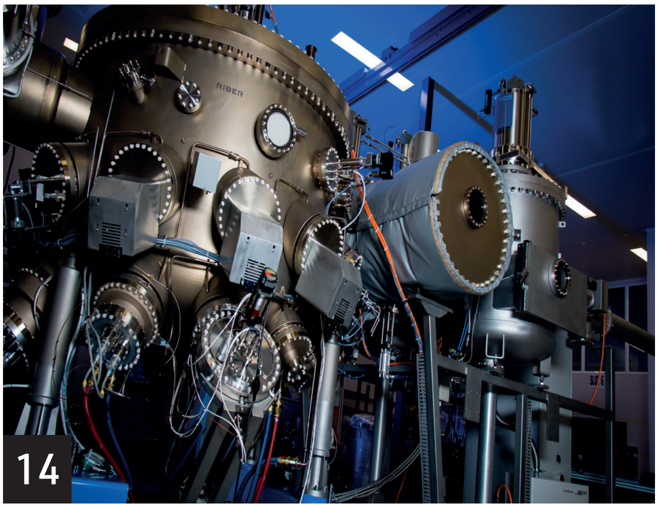
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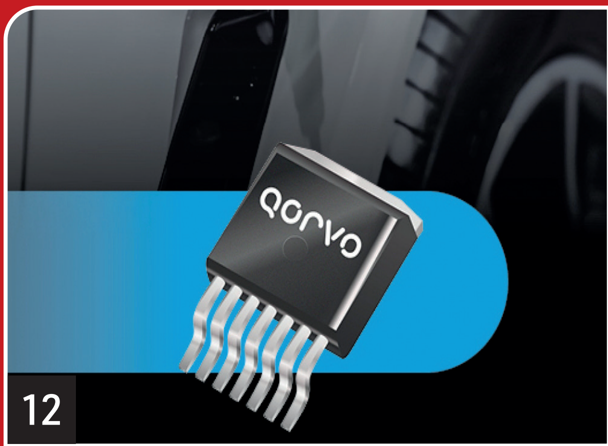

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Stronger, faster, lighter

Lehigh University nets $1.1 million to develop ultra-wide bandgap materials for military radar

Siddha Pimputkar, assistant professor of materials science and engineering at Lehigh University, has been awarded a $1.1 million grant from the DEVCOM Army Research Laboratory to research the development of ultra-wide bandgap (UWBG) semiconductor materials for use in RF.

"The Army is interested in radio frequency emitters, radar systems, that perform at higher power levels and frequencies to let them go farther into the field," Pimputkar said. "To do that, you need better semiconductor materials."

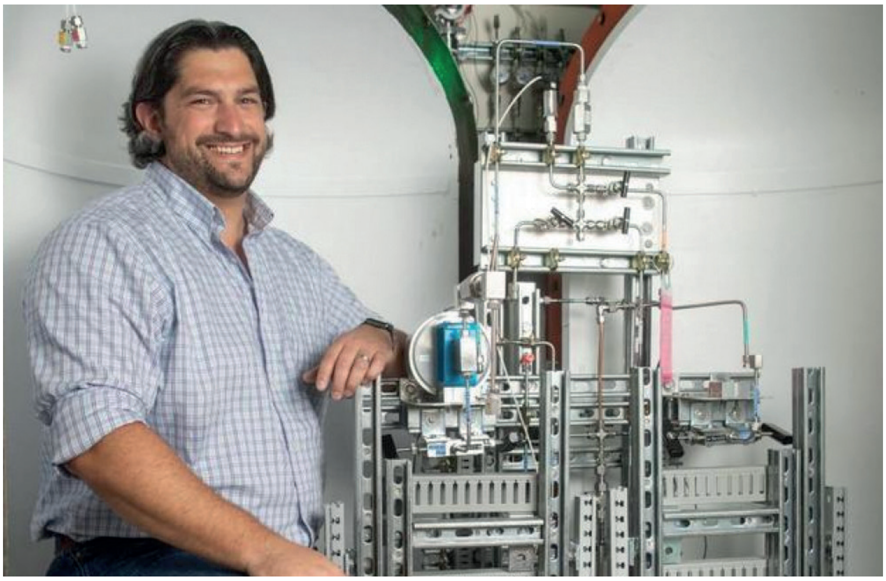
While wide bandage materials like GaN and SiC remain in relatively early stages of adoption, the military is already looking to benefit from materials with even higher capabilities. In 2020, the US Army Combat Capabilities Development Command/Army Research Laboratory/US Army Research Office (ARO) issued a call for proposals to develop UWBG RF electronics.

"The challenge now is, can we do even better than GaN and SiC?" Pimputkar said. "Now we're talking about materials that used to be considered insulators, but if we can control the electron concentrations in them, we can consider them ultra-wide bandgap semiconductors."

Exceeding diamond

Diamond is considered by many to be the leading UWBG material for applications due to an advantageous combination of material properties. It has the potential to perform well in high-voltage and high-frequency applications, and recent advances have made it possible to grow single crystal synthetic diamonds in laboratory settings.

However, there are challenges to using diamond as a semiconductor material, including difficulties in doping the material for some applications.



Pimputkar believes that cubic boron nitride (c-BN), holds the greatest potential for power electronic applications. The compound's atoms are arranged in a structure similar to that of diamond and the material has a wider bandgap of 6.4 eV compared to 5.5 eV for diamond.

But c-BN comes with challenges of its own – namely, growing it at crystal sizes needed to produce wafers

Currently, the process for growing bulk, single crystal c-BN is similar to that of synthesizing diamonds, requiring high pressures and high temperatures while yielding crystals only millimetres in size.

"For electronics, you need crystals of centimeters or inches to create wafers," Pimputkar said. "I want to find a way to grow c-BN using a process that actually scales to an industrial level."

The path there is two-pronged. One goal is to grow c-BN using a new process that requires less pressure. The other is to grow it large enough to make a device enabling the measurement of the saturation velocity of electrons in c-BN, something that has been done so far only using computational methods.

"Based on figures of merit, c-BN is the best," he said. "Now, can we make a c-BN device that can substantiate the promised properties of the material? No one has been successful in doing that yet."

Pimputkar theorises that the process of growing c-BN at lower pressures can be enabled by beginning with a seed crystal of c-BN and depositing more BN onto its surface using a new synthesis pathway and appropriate catalysts. He believes this method can produce the desired cubic crystal structure and not just the more readily grown hexagonal structure.

"While hexagonal boron nitride (h-BN) is a fantastic material in its own right, we are learning how to coax out the cubic version," he said.

Pimputkar's lab has established expertise in researching nitride growth processes under his prior NSF CAREER grant.

The lab has been investigating the c-BN growth question for approximately a year and a half, roughly halfway through the initial three-year US Army grant period, which could be extended up to two additional years.

US DoE offers $544 million loan to SK Siltron

Loan is meant to expand US manufacturing of SiC wafers for electric vehicles

SK SILTRON has been awarded a $544 million conditional loan by the US Government's Department of Energy to help increase SiC wafer production for electric vehicles.

The loan is made under the DoEs Advanced Technology Vehicles Manufacturing Loan Program.

The loan will increase manufacturing capacity at SK Siltron CSS' Bay City, Michigan facility and create up to an additional 200 skilled jobs, according to the company, or an estimated total of 450 workers by project completion in 2027.

SK Siltron acquired DuPont's Compound Semiconductor Solutions (CSS) business in March of 2020. Since then, SK Siltron CSS has focused on rapidly expanding its production capacity and has already increased by several multiples since the acquisition, including through the purchase and initial investment in the new Bay City, Michigan facility that is currently being outfitted.

In November of 2022, SK Siltron CSS announced a long-term supply agreement with Qorvo; in January of 2024, another long-term supply agreement was announced between SK Siltron CSS and Infineon Technologies.

"This project is an important step towards ensuring a resilient and robust supply chain in the United States, and we are proud to bolster domestic semiconductor manufacturing," said SK Siltron CSS CEO Jianwei Dong.

"Completion of our facility with support from ATVM funding not only strengthens our nation's manufacturing technology, but also fuels job creation, laying the foundation for innovation and economic growth in Michigan and the broader United States."

Final approval of the loan remains subject to completion of certain closing conditions; and if finalised, the financing will help SK Siltron CSS leverage its two existing Michigan manufacturing plants to address this market gap.

£11 million for University of Bristol WBG/UWBG research centre

REWIRE IKC to focus on power conversion for wind energy, EVs, smart grids, and high temperature applications

UK's University of Bristol will be home to a new £11 million Innovation and Knowledge Centre (IKC) called REWIRE, looking into next generation high voltage electronic devices using wide/ultra-wide bandgap (WBG/UWBG) compound semiconductors.

The centre will focus on power conversion for wind energy, electric vehicles, smart grids, high temperature applications, device and packaging, and improving the efficiency of semiconductor device manufacture.

The project is being led by Martin Kuball and his team at the University of Bristol, with support from partners at the Universities of Cambridge and Warwick. Industry partners including Ampaire, BMW, Bosch, Cambridge GaN Devices (CGD), Element-Six Technologies, General Electric, Hitachi Energy, IQE, Oxford Instruments, Siemens, ST Microelectronics and Toshiba will also be supporting the project. The University of Bristol team specialising in semiconductors has also recently been awarded £5 million from the Engineering and Physical Sciences Research Council (EPSRC) to develop the next generation of AlGaN solid-state circuit breakers.

It is anticipated these circuit breakers will greatly improve efficiency and voltage range, potentially enabling global energy savings of up to 20 percent compared with continuing with existing technologies.

Bristol is one of two new IKCs announced being funded by the EPSRC and Innovate UK, both part of UK Research and Innovation.

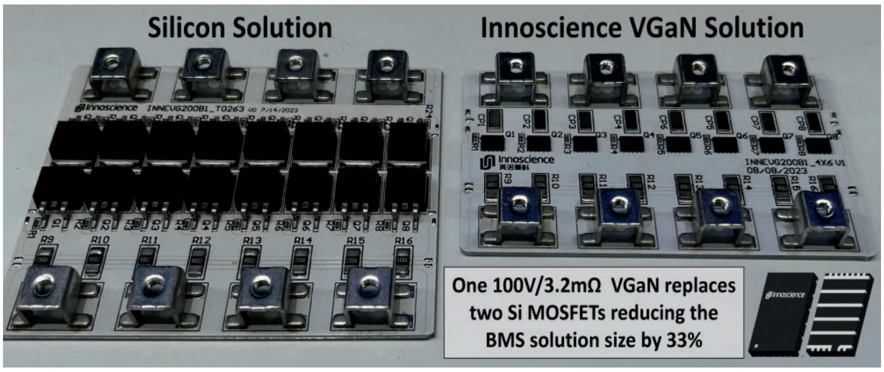
The second IKC at the University of Southampton, awarded £11 million and creating the 'Cornerstone' Information and Knowledge Centre, will improve development and commercialisation of silicon photonics technologies in the UK.

Innoscience announces 100 V bi-directional GaN IC

INNOSCIENCE has launched a 100 V bi-directional member of the company's VGaN IC family, suitable for 48 V or 60 V battery management systems, high-side load switches in bidirectional converters, and switching circuits in power systems.

According to Innoscience, one VGaN can replace two back-to-back silicon MOSFETs, reducing battery management system size by 33 percent.

The new INV100FQ030A 100 V VGaN IC supports two-way pass-through, two-way cut-off and no-reverse-recovery modes of operation. Devices feature a low gate charge of just 90 nC, dynamic on-resistance of 3.2 mΩ and a 4 mm by 6 mm package size.



The 100 V GaN series products are in mass production in En-FCQFN (exposed top side cooling) and FCQFN packaging.

Amperesand raises $12.45 million to transform power grids

Company to roll out SiC-based solid state transformer technology tested on the Singapore grid

A NEW GRID infrastructure company called Amperesand, founded by industry veterans from ABB, General Electric, Siemens and Vestas, has announced seed financing of $12.45 million.

The funding will help the company roll out infrastructure solutions powered by solid-state transformer technology. The aim is to facilitate bidirectional energy flow, intelligent monitoring and energy management with native integration of mixed AC/DC systems, to enable the rapid adoption of EV fast charging, energy storage and renewable energy systems.

The SiC-based technology has already been tested on the Singapore grid at a 1.5 MW scale through a 7-year research programme executed by the Energy Research Institute at Nanyang Technology University of Singapore.

Amperesand will initially target the EV fast-charging infrastructure market, with initial delivery of systems in the US and Singapore planned for 2025. Xora Innovation and Material Impact co-led financing with participation from TDK Ventures and Foothill Ventures.

"Over 7 years ago, Anshuman [Tripathi, Amperesand co-founder and VP of Engineering] and leaders from Singapore's research ecosystem had the foresight to project the evolution of SiC technology, and the rapidly evolving requirements of power grids, leading to the creation of a highly ambitious solid-state transformer research program at NTU. The time for commercialisation of SSTs is now right from both a technology and market readiness perspective, and we are excited to partner with the founding team we consider to be in pole position," said Phil Inagaki, managing director at Xora Innovation.

According to the International Energy Agency's, the demand for next-generation DC fast-charging infrastructure alone is projected to grow to 200 GW by 2030, representing a market opportunity exceeding $200 billion.

GF GaN fab to benefit from $1.5B CHIPS Act funding

Direct funding for GlobalFoundries will create new manufacturing capacity and capabilities

THE US Department of Commerce has announced $1.5 billion in planned direct funding for GlobalFoundries as part of the US CHIPS and Science Act. This investment will enable GF to expand and create new manufacturing capacity and capabilities including securing essential GaN chips for automotive, IoT, aerospace, defence, and other vital markets.

GF is the first pure-play foundry to receive a major award (over $1.5 billion) from the CHIPS and Science Act, designed to strengthen American semiconductor manufacturing, supply chains and national security.

Part of the proposed funding will support the creation of the first US facility capable of high-volume manufacturing of next-generation GaN semiconductors for use in TVs, power grids, data centres, 5G and 6G smartphones and other critical technologies. This will be at the site of GF's longest continuously operated fab, a 200mm facility in Essex Junction, Vermont. The GaN project was also awarded £35 million in US government funding in October 2023.

The $1.5 billion investment will also help upgrade and expand capacity at GFs existing Vermont facilities. In addition, it will go towards GF's Malta, NY, fab by adding technologies already in production in GF's Singapore and Germany facilities geared towards serving the US auto industry.

Overall, based on market requirements and demand, GF plans to invest more than $12 billion over the next 10 plus years across its two US sites through public-private partnerships with support from the federal and state governments as well as from its ecosystem partners, including key strategic customers.

"These proposed investments, along with the investment tax credit (ITC) for semiconductor manufacturing, are central to the next chapter of the GlobalFoundries story and our industry. They will also play an important role in making the US semiconductor ecosystem more globally competitive and resilient and cement the New York Capital Region as a global semiconductor hub," said Thomas Caulfield, president and CEO of GF.

"With new onshore capacity and technology on the horizon, as an industry we now need to turn our attention to increasing the demand for US-made chips, and to growing our talented US semiconductor workforce."

"Semiconductors are in everything from our cellphones, to refrigerators, to cars, and our most advanced weapons systems, and access to them carries important economic and national security implications. It was the shortages of semiconductors during the Covid-19 pandemic that raised prices for consumers and led to the shutdown of automobile manufacturing sites across the country," said Secretary of Commerce Gina Raimondo.

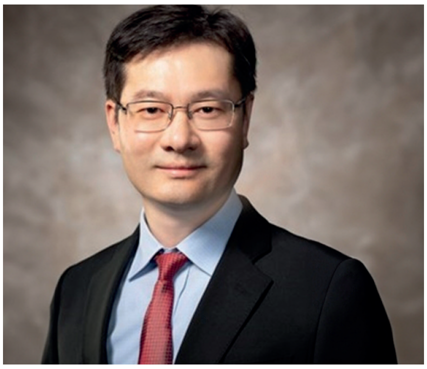
Raimondo added: "Thanks to the CHIPS and Science Act, we're working to onshore these critical technologies in order to bolster the supply of domestic chips that are essential to manufacturing cars, electronics, and national defense systems in New York, Vermont, and states across the country."

To attract and cultivate a pipeline of semiconductor talent that will be needed in New York and Vermont, GF has announced a new student loan repayment programme to help current employees and new recruits pay down student loan debt. The new benefit programme is part of the company's multi-million-dollar investment to strengthen the semiconductor talent workforce by helping to ease the financial burden of higher education and training of the company's present and future employees.

GF is also partnering with universities and community colleges nationwide to help build a diverse workforce and semiconductor talent pipeline. As part of receiving CHIPS and Science Act funding, GF will continue to invest in and develop new workforce development efforts including curriculum development, internship and apprenticeship programmes, K-12 STEM outreach as well as additional education and training programmes.

NSF funds research into gallium oxide traction inverters

Project explores integration of gallium oxide packaged power modules to enhance the performance of EVs



THE US National Science Foundation has given a $300,000 grant to Xiaoqing Song, an assistant professor in the University of Arkansas to support his research on advancing high density and high-operation-temperature traction inverters.

Song's project explores the integration of Ga_2O_3 packaged power modules to enhance the power density and temperature range of electric vehicles. Collaborating with the National Renewable Energy Laboratory, the project sets out to innovate power module packaging, establish reliable strategies for Ga_2O_3 power devices and demonstrate the capabilities of a high density, high temperature traction inverter.

"By eliminating technical barriers for gallium oxide device integration, this project will foster the development of next-generation, high density and high-operation-temperature power converters," Song said.

The traction inverter, responsible for converting stored DC power into AC power to drive electric motors, stands to benefit significantly from Ga_2O_3.

Song said, "Gallium oxide can make the traction inverter smaller, lighter, more efficient and capable of operating across a wider range of temperatures."

One challenge addressed in the project is the low thermal conductivity of Ga_2O_3, which hinders efficient heat removal. Song plans to develop advanced power module packaging techniques that enable low thermal resistance, low parasitic inductances and high-temperature operation capability.

"National Renewable Energy Laboratory (NREL) has significant experience in power module simulation, fabrication and characterisation, as well as world-class experimental and lab capabilities for evaluating and designing efficient and reliable power electronics systems. The PI will collaborate with them to design and develop a gallium oxide-based high density and operation-temperature traction inverter for automotive applications. This project will help establish a long-term partnership with NREL that can catalyse further research and development of ultra-wide bandgap power semiconductor devices," Song said.

Song shared that the collaboration with the NREL aims to design and develop a Ga_2O_3-based high density and high-operation-temperature traction inverter for automotive applications, fostering a long-term partnership that can drive further research in ultra-wide bandgap power semiconductor devices.

"Other applications include power grids, data centres, renewable energy, space and defence," Song added.

The success of the project, he believes, will provide valuable insights into Ga_2O_3 device modelling, packaging, gate driving, protection and application in power converters. These advancements are expected to catalyse progress in transport electrification and the deployment of Ga_2O_3 technology in challenging environments.

Qorvo boosts performance in 750V EV designs

SiC FET offers 9mΩ $R_{DS(on)}$ to reduce conduction losses and maximise efficiency

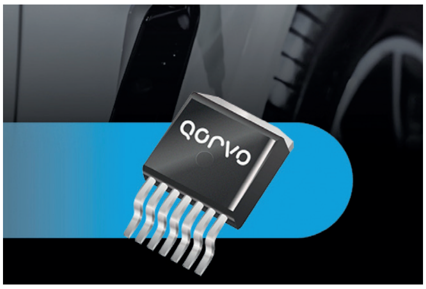
Qorvo has launched an automotive-qualified SiC FET offering what it believes is an industry-best 9 mΩ $R_{DS(on)}$ in a compact D2PAK-7L package.

This 750V SiC FET is the first in a new family of pin-compatible SiC FETs from Qorvo with $R_{DS(on)}$ options up to 60mΩ, making them well suited for electric vehicle (EV) applications, including on-board chargers, DC/DC converters and positive temperature coefficient heater modules.

The UJ4SC075009B7S features a 9 mΩ typical $R_{DS(on)}$ at 25°C needed for reducing conduction losses and maximising efficiency in high-voltage, multi-kilowatt automotive applications. Its small, surface-mount package enables automated assembly flows and reduces customer manufacturing costs.

This new 750 V family complements Qorvo's existing 1200 V and 1700 V automotive SiC FETs in D2PAK packaging to form a complete portfolio addressing EV applications that span 400 V and 800 V battery architectures.

Ramanan Natarajan, director of Product Line Marketing for Qorvo's Power Products, said, "The launch of this new family of SiC FETs demonstrates our commitment to providing EV powertrain designers the most advanced and efficient solutions for their unique automotive power challenges."



These fourth generation SiC FETs use Qorvo's cascode circuit configuration, in which a SiC JFET is co-packaged with a silicon MOSFET to produce a device with the efficiency advantages of wide bandgap switch technology and the simpler gate drive of silicon MOSFETs.

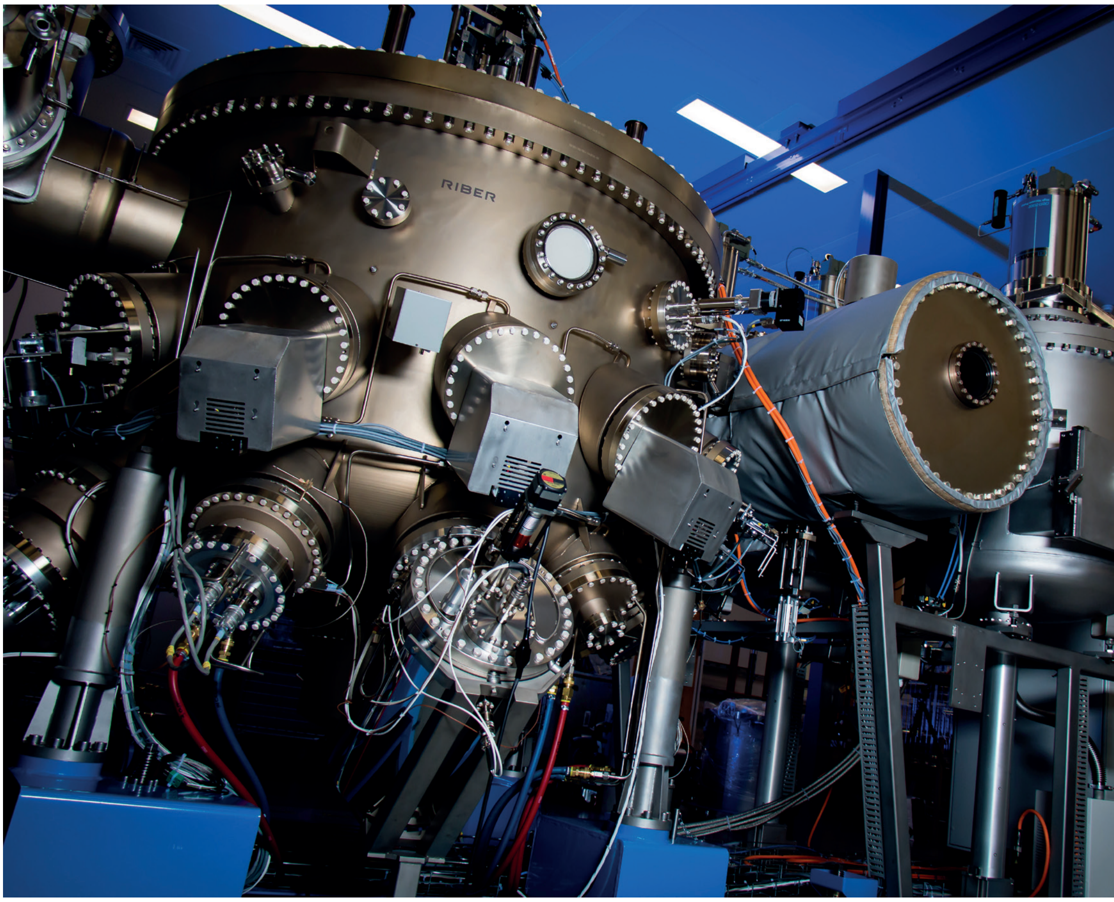
Porotech partners with PSMC for microLEDs

PORO TECHNOLOGIES, a UK-based microLED company, and Taiwan's Powerchip Semiconductor Manufacturing Corp (PSMC), have announced a strategic partnership in microLEDs for consumer display applications.

The focus is on manufacturing 200 mm GaN-on-silicon microLEDs for mass production. The companies will be combining PSMC's wafer manufacturing expertise with Porotech's technologies in PoroGaN microLED-on-silicon, dynamic pixel tuning, and the GaN-on-silicon platform.

Tongtong Zhu, CEO and Founder of Porotech, commented: "Our

collaboration with PSMC signifies a momentous step forward for mass-producing the microLED-on-silicon technology for display applications. This strategic partnership speaks volumes about our shared dedication to innovation and excellence. GaN-on-silicon's role in microLED-on-silicon tech advancement is undeniable."



The Riber MBE 8000, the company's flagship production tool, has been developed in collaboration with US epiwafer provider Intellepi.

The growth of MBE

With ramping sales of production tools and emerging longer-term opportunities, Riber's revenue is set to stay on an upward trajectory

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN OUR COMMUNITY, it's often said that MOCVD is the tool of choice for epitaxial growth in high-volume fabs, while MBE is the preferred technique for the academic researcher. But the reality is far more nuanced. While it is true that MOCVD dominates chip production, sales of MBE tools to makers of compound semiconductor devices are rising, and will continue to do so.

It is a trend that is helping to swell sales at Riber, the French producer of a wide portfolio of MBE tools. Annual sales of the company's epitaxial systems climbed by 96 percent between 2022 and 2023 to hit €29.0 million, and total revenue for this year is expected to surpass last year's €39.2 million, which included €10.3 million for services and accessories.

According to the company's CEO, Annie Geoffroy, Riber's success stems from both a rise in its global sales of MBE tools, and an increase in its market share.

Accounting for almost two-thirds of Riber's 2023 revenue are sales to Asia. This success, so far from the company's head-quarters on the outskirts of Paris, is attributed to establishing local support for its customers. Such efforts have been up and running for 12 years, and have helped Riber win overseas business and strengthen its relationship with its customers.

Recent dealings with Asian chipmakers includes an order placed this January for a pair of MBE 412 systems for device development, and an MBE 6000 that will be employed to increase the production of GaAs pHEMTs.

Despite this device being replaced by silicon-on-insulator technology in the majority of smartphones, it is still being produced in volume worldwide.

"Some customers in the US are still making pHEMTs," reveals Riber's marketing manager

Another of Riber's diversifications is the pursuit of MBE within the silicon industry. The established electro-optical modulators using *p-n* junctions formed from silicon are encroaching their performance limit, and gains can be realised by turning to functional oxides, such as $BaTiO_3$

Claudine Payen, who believes that these transistors may have specific requirements that demand growth by MBE.

Another industrial market for Riber is that of the VCSEL. Interest in increasing the production efficiency of this form of laser has led the French outfit to develop a new tool, the Riber MBE 8000, in collaboration with US epiwafer provider Intellepi.

"We worked on the design of the 8000 to have a big capacity and also very, very good uniformities," says Payen. She explains that this tool, capable of accommodating four 200 mm wafers, can also be used for other epitaxial designs demanding excellent layers, very tight interfaces, and a high degree of thickness and compositional uniformity.

According to company CTO, Jean-Louis Guyaux, there is a lot of interest in Riber's tools for the growth of InP avalanche photodiodes, as well as GaN-based LEDs emitting in the UVC. For the later, a new pilot line has been established that features a Riber MBE 49, a tool that can be used for growth on a single 200 mm wafer, or for multiple 100 mm wafers.

Over the last two-to-three years, Riber has also drawn on MBE to develop a technique for the passivation of laser bars, coating them with ZnSe. The company's completely automated tools carry out this task under vacuum in high-volume fabs.

Another of Riber's diversifications is the pursuit of MBE within the silicon industry. The established electro-optical modulators using *p-n* junctions formed from silicon are encroaching their performance limit, and gains can be realised by turning to functional oxides, such as $BaTiO_3$, argues Guyaux. He adds: "It's pushed, of course, by the current datacom silicon market, but there is a lot of interest there for quantum computing with photons."

Stalwart systems

Due to the long lifetime of MBE systems, most orders are placed to increase capacity, rather than replace an older tool. As the growth chamber is made from stainless steel, it could last forever with regular maintenance and the replacement of parts.

"The obsolescence is coming mainly from the electronics," says Guyaux, who explains that the servicing of production tools may include upgrading electronics and control software, and introducing new *in-situ,* real-time instruments.

Within academia, it's not uncommon for epitaxial growth to be undertaken in tools dating back to the 1980s. However, Riber still nets orders for new tools for universities, often when new research projects win funding that includes an allocation for purchasing a new growth tool.

"There's also this matter of size," says Payen, who points out that legacy equipment may only accommodate very small wafers, while projects need to demonstrate processes on the larger wafers.

One of the company's goals for 2024 is to advance the proven capabilities of its MBE 8000.

Another is to continue its work on a project called ROSIE, short for Riber Oxide Silicon Epitaxy, involving the development of this growth technology for 300 mm wafers. Guyaux sees such efforts as crucial to the evolution of the semiconductor industry. He forecasts a future beyond III-V fabs, silicon fabs, and the subsequent marriage of these two technologies. Silicon will be the only technological platform to survive, due to its capability to address very large markets, but III-Vs and SiC will be added to this foundation.

"This is where MBE has a real advantage, due to its thermal budget," claims Guyaux. He points out that with MOCVD, the high temperatures needed to crack the precursors threaten to damage the wafer, an issue that may be avoided by MBE growth.

Another fundamental change to the compound semiconductor industry could be the development of hybrid epitaxial tools that combine MBE with other growth technologies.

Riber is working on this – another reason to believe that the company is well-positioned for the coming years. As well as healthy orderbook, rising sales, and an expanding portfolio of MBE tools, it is preparing for a future that is forecast to witness some major changes within our industry.

Saving the planet with ultrafast GaN

A new CEO at QPT, along with a game-changing award and additional funding, will help to drive the commercialisation of GaN-based power modules operating at breath-taking speeds

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

2024 is sure to be a pivotal year for QPT, the UK-based developer of compact GaN-based modules operating at revolutionary switching speeds.

In just the last few weeks QPT has appointed its first CEO and netted an award that will provide a springboard to gaining traction in the marketplace. Soon to follow is an imminent round of funding that will help double the size of its engineering team, and ultimately speed the commercialisation of the Cambridge start-up's miniature modules. These GaN-based modules are said to be smaller and more efficient that those employing silicon and SiC transistors.

QPT's new CEO, serial entrepreneur and semiconductor industry veteran Rupert Baines, cites many reasons for taking up his new role.

They include the company's ground-breaking technology, substantial commercial prospects and the opportunity to contribute to a greener planet.

The company's technology is certainly radical, bringing elements of the RF to the power domain.

"There are engineers who understand gigahertz, and some of them are using GaN transistors, but those tend to be in the milliwatts or a few watts range," says Baines, who adds: "And you've got people in the power electronics world, who are talking about kilohertz and tens of amps." Bringing all of this under one roof, modules from QPT use gigahertz signal frequencies while delivering hundreds of amps and kilowatts of power.

Although this marriage has much appeal, it's not easy to make it work: "That's why we've got so many patents. That's why the engineering is so cool."

The building of the QPT modules involves uniqueness at many levels, including implementation, the design, the circuit boards and the layout, with success hinging on tight control of design, construction, integration and testing.

"We can't just send a kit out and licence the design," argues Baines, who points out that the only practical business model requires in-house building and selling of modules and sub-assemblies as integrated systems.

QPT is well down the road to commercialising its technology, having produced a robust, early-stage product that satisfies electrical and safety requirements. The next step, says Baines, is to share the modules with customers that will give them "a really good kicking".

Helping to do just that is the global provider of electrification and automation technologies, ABB. Last year this multi-national ran a competition called the Power Density Start-up Challenge, associated with motor drive products. QPT netted the prize, collecting its award this January.

"We didn't expect to win," admits Baines. He and his colleagues felt that their radical technology would be seen as too risky and in need of further development. "[ABB] just said: 'We're looking for disruption, we're looking for new ideas'."

A joint development and an integration project is now being set up by ABB and QPT that will help drive the commercialisation of the technology. Efforts will include system integration and system-level testing.

Another goal for QPT is to raise investment, beginning with a funding round of over £1 million. That's small fry for a technology start-up, but QPT is a small team that's not involved in chip-making. "It's system level integration," says Baines. "By comparison, it's relatively cheap". Some investment will come via Crowdcube, a platform that allows the public to invest.

This additional funding will allow QPT to double its engineering team to around a dozen staff. At this stage, the company is not recruiting sales executives, because it is yet to have a mature product. "We're still at the iterating, optimising, talking to customers, doing a redesign phase," explains Baines.

During module development, QPT sourced its transistors from GaN Systems. Uncertainty hung over this when Infineon acquired the fabless Canadian chipmaker in the second half of 2023. However, supply has continued, and is going well.

"We've got a very good relationship with Infineon," remarks Baines. "We like their transistors and they've given us a lot of low-level engineering input – a lot more than you get in a normal data sheet, so we really understand their devices."

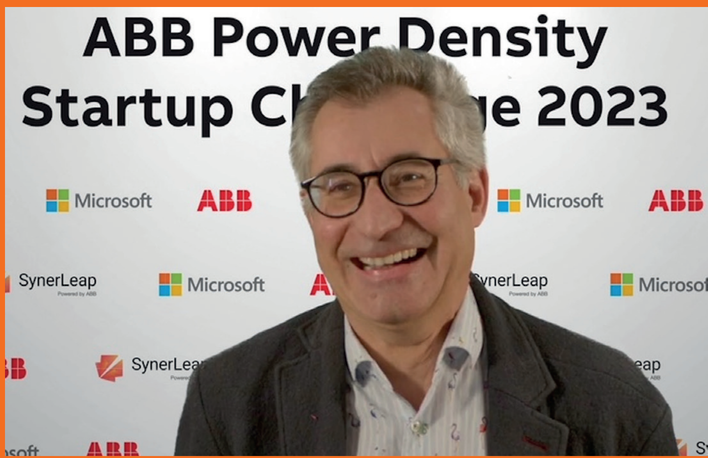
However, that's not to say that QPT will only ever use one supplier of GaN transistors. "I'm sure we will work with others, for some applications or products," says Baines.

By partnering with a number of GaN chipmakers and selling modules to many companies, QPT will increase the chances that its technology will be deployed in many applications, including electric heat pumps and cars.

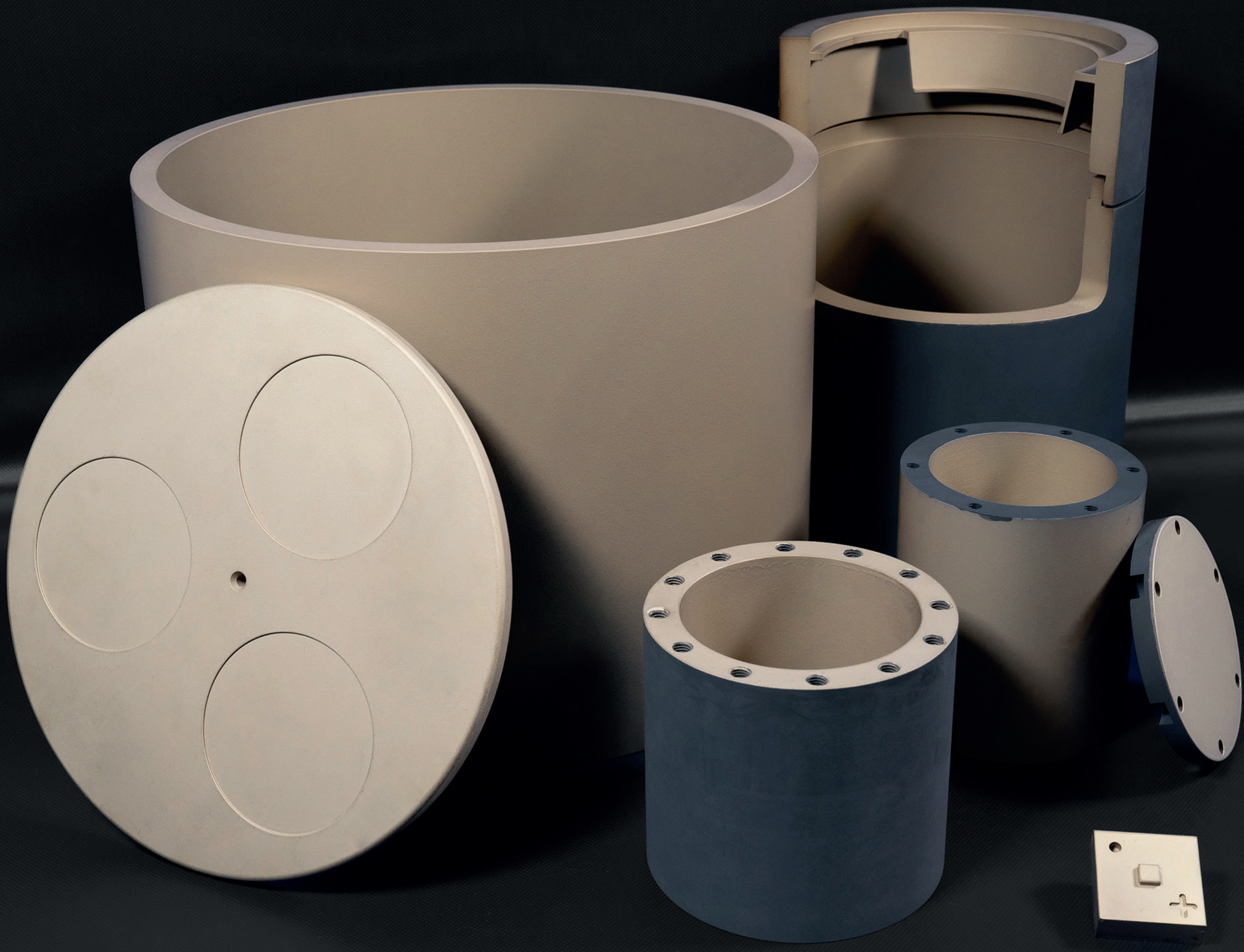
"At the moment, a lot of that is shockingly inefficient," says Baines, "so this is really important, not just for the industry, but for the planet."

Rupert Baines, CEO of QPT

For the last two years Rupert Baines has been an advisor to QPT. Over that time he has been getting closer to the company, leading to his participation last year in discussions surrounding fundraising and the growth of the start-up. These conversations led him to take on the role of CEO, which he will start on 1 April after: relinquishing his position as an entrepreneur-in-residence at a VC fund; and ceasing to chair a UK working group, which considers the semiconductor strategy for the UK telecom industry.



Baines hopes that his experience as an engineer and product manager will serve him well when CEO. He argues that good decisions involve understanding the issues of the engineers and the demands of the customers, before finding the right balance these competing requirements.



Coating at its best

Spraying graphite parts with tantalum carbide cuts the cost of producing SiC crystals and epilayers

BY CHRISTIAN REIMANN, MATTHIAS TREMPA, KEVIN SCHUCK AND MICHAEL LANG FROM FRAUNHOFER IISB, AND TORSTEN KORNMEYER AND DIRK MUETZENICH FROM THE NIPPON KORNMEYER CARBON GROUP

THE SEMICONDUCTOR INDUSTRY is booming, with one prime example the field of SiC power electronics. Here many high-volume fabs are either under construction or expansion, to support an increase in the production of SiC devices, which are being deployed in electric vehicles.

While every boom offers a great opportunity to increase profits, it also brings its own unique challenges. Crucial to ramping global SiC chip production is the manufacture of high-quality SiC crystals, wafers and epitaxial layers. In this context, it is crucial to consider the role of semiconductor-grade graphite materials, which are used in the equipment that enables the growth of SiC crystals and the deposition of SiC epitaxial layers. Graphite, which is valued for its thermal insulation capabilities and inertness, is the preferred material for crucibles and susceptors in crystal-growing systems, and for planetary discs and satellites in epitaxial systems.

Killer degradation…

The production of SiC crystals involves harsh process conditions. The total corrosion of a graphite crucible may occur after just a few processes, due to temperatures of over 2000 °C and extremely corrosive gas species that contain silicon. For instance, the production of SiC epitaxial layers involves: process temperatures that peak at 1600 °C; the combination of silane and propane, which are responsible for the growth of the SiC layer; and hydrogen and in some cases hydrochloric acid. The latter two can be used as carrier gases, or for very corrosive etching.

As well as simply eating up the graphite components, the harsh process conditions alter the emissivity and morphology of the component surfaces. This is a significant issue, severely impairing the reproducibility of the production processes and in turn having an impact on the resulting process stability – and thus the material quality of the SiC crystals and epitaxial layers. Another major drawback is that the harsh conditions can cause free carbon and carbon particles to be released from the corroded graphite parts, threatening the production of high-quality SiC semiconductor material.

Due to these considerable concerns, process engineers tend to only use these heavily stressed components a few times, and sometimes just once. It is a constraint that causes consumable material graphite to contribute significantly to the manufacturing costs of SiC crystals and epitaxial layers.

...and graphite shortages

It's of little surprise that graphite is in great demand in many sectors, due to its desirable physical and mechanical properties and its capability to form a wide range of geometries. Unfortunately, today's graphite industry cannot keep pace with the strong expansion plans of the global SiC industry, and competition between end users for the best possible supply of graphite is already underway. Fortunately, there's a game-changing solution that kills two birds with one stone. It's the introduction of protective layers, which tackle both the degradation of graphite parts and the graphite delivery shortage. It's a most welcome introduction, given the drastic increase of lead times for graphite components, driven by the booming semiconductor sector.

Today, protective coatings based on tantalum carbide (TaC) are already in use. The merits of this material include a melting temperature of over 3800 °C and a very good chemical resistance to reactive gases. Up until now, the approach to producing state-of-the-art TaC protective coatings is to use Chemical Vapour Deposition (CVD) to deposit this material on graphite components, a process that produces semiconductor-clean and gas-tight layers with a thickness of typically up to 35 µm. However, there are disadvantages of this technology, with the main drawbacks including high manufacturing costs, and once again, long delivery times. In addition, there are material issues, with cracks appearing through 100 percent dense crystalline TaC layers during repeated heating and cooling of the components. These cracks expose the underlying graphite, which strongly degrades over time and has to be replaced.

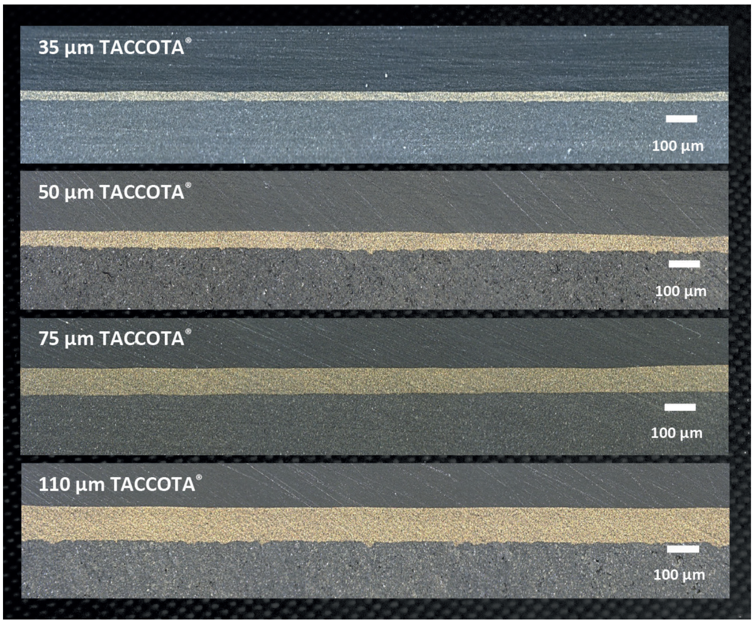


Figure 1. The TaC process technology developed at Fraunhofer IISB allows adjustment of desired coating properties, such as thickness, shown here in the range 35 µm to 110 µm.

The spray solution

Motivated by addressing all these shortcomings, those of us at Fraunhofer IISB started to develop a disruptive coating technology more than five years ago, with the aim of compensating for the disadvantages of the state-of-the-art approach. We began with very simple laboratory-scale tests, involving the coating and evaluation of graphite shards.

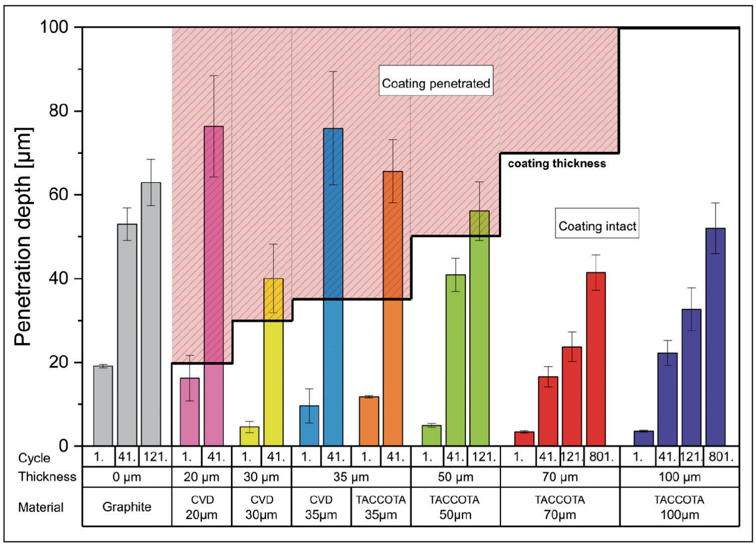


Figure 2. Scratch test results of Tacotta spray coating with variable thicknesses versus CVD TaC coatings performed after DIN50324 / ASTM G99 and G133. These results reveal an enhanced wear resistance due to increased coating thickness.

Over the years, our TaC coating technology has grown out of its children's shoes. Helping on this front has been the feedback from potential end users – it has been key to the further development of our technology. Today, our patented approach combines a water-based spray coating with subsequent temperature treatment. One great asset of our technology is that it is incredibly flexible when it comes to coating components of different sizes and geometries. Unlike CVD deposition of TaC, partial coating and component refurbishment is also possible. What's more, our technology is environmentally friendly, easy to industrialise, and free from conflicting materials.

We have evaluated the properties of our TaC coating. It is resistant to temperatures of more than 2500 °C and corrosive gases. The thickness of the coating is variably adjustable in the range of 20 µm to 200 µm (see Figure 1), ensuring protection impact for extremely lengthy process times and a high number of cycles. Another benefit of our technology is that it produces TaC coatings with tremendous mechanical stability, thanks to interlocking with the underlying porous graphite. We have demonstrated this attribute with so called scratching-tests (see Figure 2).

Figure 3. SiC wafer carrier before (right) and after (left) several standard SiC epilayer processing runs.

Following two years of pre-development, we shared the potential of this newly developed technology with a number of investors. Our technology

Proven coatings

To investigate the contamination that results from a TaC coating during real application conditions, a case study has been performed at Fraunhofer IISB using a single-wafer SiC epitaxy reactor. For this purpose, semiconductor grade epi-ready SiC wafers have been processed at typical growth conditions – such as 1600 °C, and reactive gas flows of hydrogen, silane and propane – using a mean time for the growth of the SiC epi-layer of around 1 hour. For each run a virgin SiC wafer has been used and analysed at the upper surface (silicon side) by vapor phase decomposition, inductively coupled plasma mass spectrometry. This form of spectrometry determines the contamination level.

	Epi-Run	#1	#2	#3	#10	#11	#12	Ref.	Ref.
Detec-tion limit (dl)	Susceptor	CVD TaC	CVD TaC	CVD TaC	TACCOTA	TACCOTA	TACCOTA	Unused SiC wafer	Industry Epi reactor (CVD TaC)
	Wafer carrier	CVD TaC #1 (1st use)	CVD TaC #1 (2nd use)	CVD TaC #1 (3rd use)	TACCOTA #2 (1st use)	TACCOTA #2 (2nd use)	TACCOTA #2 (3rd use)		
0.065	Li	<dl	<dl	<dl	<dl	<dl	<dl	<dl	n.m.
0.371	Na	<dl	<dl	4.536	1.199	<dl	3.750	1.068	n.m.
0.198	Al	2.570	<dl	<dl	<dl	1.213	4.155	<dl	n.m.
0.265	K	<dl	<dl	1.889	0.847	<dl	3.183	0.364	0.053
0.158	Ca	<dl	0.282	0.275	4.850	1.766	<dl	18.78	<dl (0.05)
0.125	Ti	<dl	<dl	<dl	0.229	<dl	0.664	<dl	<dl (0.03)
0.164	V	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.02)
0.431	Cr	<dl	0.490	<dl	<dl	<dl	<dl	<dl	0.105
0.124	Mn	<dl	<dl	<dl	<dl	<dl	<dl	<dl	0.488
0.375	Fe	<dl	2.575	<dl	<dl	<dl	<dl	<dl	0.306
0.062	Co	<dl	<dl	<dl	<dl	<dl	0,265	<dl	<dl (0.02)
0.783	Ni	1.456	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.25)
0.551	Cu	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.14)
0.206	Zn	<dl	<dl	0.233	0.178	0.075	0.150	<dl	<dl (0.05)
0.976	As	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.21)
0.015	Sr	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.003)
0.026	Cd	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.004)
0.007	Ba	<dl	<dl	<dl	0.180	0.234	0.128	0.051	<dl (0.001)
0.002	Ta	119.0	71.98	5.101	26.67	5.977	0.269	0.066	0.058
0.010	Pb	<dl	<dl	<dl	0.022	<dl	<dl	<dl	<dl (0.002)
0.037	Bi	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.001)

Values for surface contamination in 1 x 10^{10} cm^{-2}, measured by vapor phase decomposition, inductively coupled plasma mass spectrometry on the silicon side of epi-ready SiC wafers. Each run has used a virgin cleaned SiC wafer.

The first experiment involved three subsequent epitaxial runs and a virgin CVD TaC-coated setup. For this experiment, the set-up included a wafer carrier, which is directly in contact with the lower SiC wafer surface, and a susceptor chamber where the wafer carrier is embedded. Measurements show very low contamination levels for almost all measured elements for all three runs (see the figure above and to the right for contamination levels on the wafer surface). However, the surface contamination with tantalum coming from CVD TaC is initially quite high, and still at high values of more than 5 x 10^{10} cm^{-2} after the third run.

These results have been compared with those obtained with a virgin Taccota set-up. In this case, the initial tantalum contamination is around 75 percent lower, and after three runs it is below 0.3 x 10^{10} cm^{-3}, a much more acceptable level. This low ground level of contamination has been observed for the other measured elements.

This study demonstrates that Taccota is ready for semiconductor application from a contamination point of view, opening the door to real application tests at the sites of manufacturers of SiC devices.

impressed the Nippon Kornmeyer Carbon Group (NKCG), a joint-venture between the German-based Kornmeyer Group and Nippon Carbon Japan. They have licensed our technology from Fraunhofer IISB and produced TaC-coated graphite parts for their customers. Our collaboration, which started in 2021, immediately bore fruit. Already, the reusability of our TaC coating for the the production of SiC crystals has been successfully demonstrated several times. In addition to this valued reusability for SiC epitaxy, we have shown that there is no contamination from the TaC layer, and that the processed SiC wafers are free from any surface contamination (see Figure 3 and the text box "Proven coatings").

We have even demonstrated that the tantalum contamination that occurs during epitaxy on SiC wafers with virgin TaC-coated graphite components is reduced by 75 percent in the first processes, compared with state-of-the-art CVD coatings. Thanks to this, our technology enables longer production campaigns with one graphite setup.

The uptake of the TaC coating technology, which we refer to as Taccota, has increased following its proven success in PVT and the epitaxial SiC crystal growth process. The management of NKCG is investing in a significant increase in production capacity along the entire value chain, from CIP feedstock to the TaC-coated finished parts, and it is also funding the introduction of an industry-leading quality control and management system. This investment is enabling NKCG to address the demand of graphite in this massive market, and fulfil its long-term strategic growth plan, together with its cooperation partner Fraunhofer IISB.

Carbon: The power to materialise the future

NIPPON KORNMEYER
CARBON GROUP

Since 1968, the Kornmeyer family has been supplying and innovating the carbon-based materials market. Today Nippon Kornmeyer Carbon Group (NKCG) is a company jointly operated by the shareholders of Kornmeyer Carbon Group GmbH in Germany and Nippon Carbon Co. Ltd. In Japan, a Tokyo stock exchange listed carbon manufacturer.

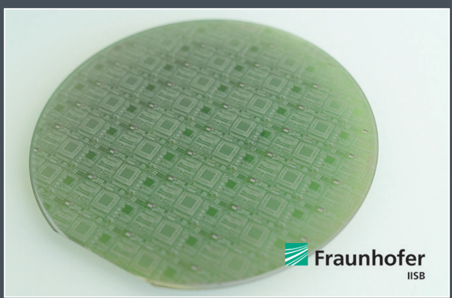
NKCG specializes in design and modelling, manufacturing, purification and several kinds of surface coatings, as well technical support of carbon-based and other ceramic materials. Decades of experience in the semiconductor industry, and material know-how combined with scientific expertise, enables NKCG to be a reliable partner along the entire process chain.

Intelligent Power Electronic Systems and Technologies

According to its motto, the Fraunhofer Institute for Integrated Systems and Device Technology IISB, founded in 1985, conducts applied research and development for the direct benefit of industry and society.

With scientific expertise and comprehensive systems know-how, IISB supports customers and partners worldwide in transferring current research results into competitive products, applied e.g. in electric vehicles, aviation, production, and energy supply.

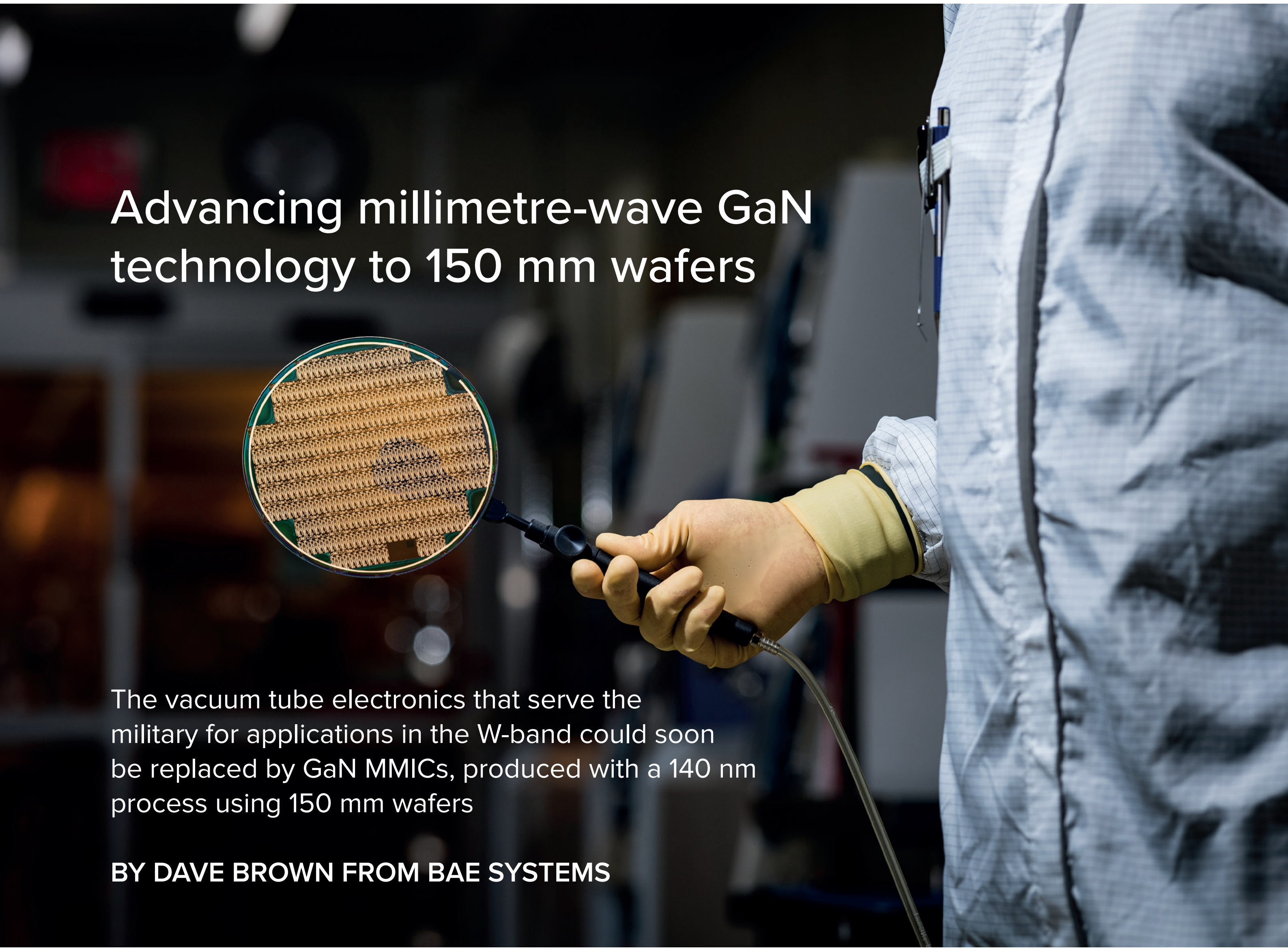
➤ Fraunhofer IISB develops power electronics for the mobility sector, such as converters and e-drives for various types of vehicles all the way to components for the charging infrastructure. Credit: Kurt Fuchs, Fraunhofer IISB.



➤ Fully processed 150 mm 4H-SiC High Temperature CMOS Wafer. Credit: Elisabeth Iglhaut, Fraunhofer IISB

The institute consolidates its activities in the two major business areas of Power Electronic Systems and Semiconductors. In doing so, it comprehensively covers the entire value chain from basic materials to semiconductor device, process, and module technologies to complete electronics and energy systems.

As a unique European competence center for SiC, IISB is a pioneer in the field of protective coatings like TaC, as well as SiC for graphite parts used in semiconductor materials production and processing.



Advancing millimetre-wave GaN technology to 150 mm wafers

The vacuum tube electronics that serve the military for applications in the W-band could soon be replaced by GaN MMICs, produced with a 140 nm process using 150 mm wafers

BY DAVE BROWN FROM BAE SYSTEMS

FOR A MULTITUDE of RF systems, a critical component is the GaN-based Monolithic Microwave Integrated Circuit (MMIC). Products incorporating this technology are deployed in wireless base stations, SATCOM terminals, and are a core enabler of 5G systems. In addition, due to a level of performance that's not possible with silicon-based electronics, GaN MMICs feature in defence systems for radar, missile seekers, electronic warfare, and communications.

In all these applications GaN transistors make a welcome contribution, thanks to their capability to provide the best combination today for any semiconductor technology, judged in terms of high-frequency operation, low noise, high linearity, and high output power density.

RF GaN is now in a new era of maturity. RF systems employing this wide bandgap semiconductor are fielded across a broad range of domains and missions, with GaN MMICs with a high manufacturing readiness level present in a number of defence and commercial foundries throughout the world. Over the next decade this technology is sure to progress towards more advanced process nodes, featuring gate lengths below 150 nm. This scaling of dimensions will extend operating frequencies through the millimetre-wave spectrum towards 100 GHz while increasing instantaneous bandwidth. Simultaneously, there is a maturing of process capability, involving increased wafer diameters and line yields, that will drive up foundry capacity and reduce the cost per chip. It's a direction of travel that will spur greater market penetration of GaN MMIC products.

At BAE Systems, a leading supplier of microelectronics, we are designing, developing and producing custom RF integrated circuits for a broad range of defence electronic systems. Our efforts are in demand, because MMIC-based products that meet the needs of the defence industry are rarely available from commercial sources, due to the complex nature of this technology, combined with unique and challenging performance requirements.

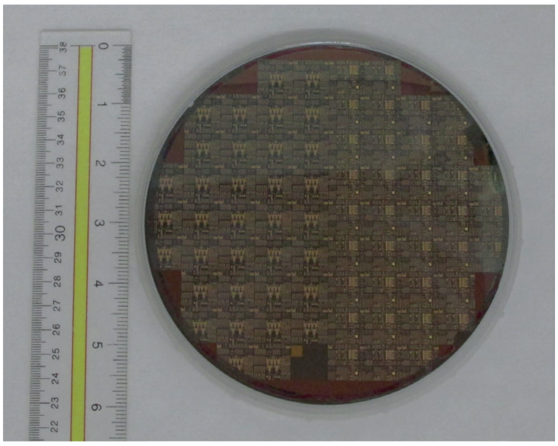
We produce our GaN-based MMICs at the BAE Systems' Microelectronics Center (MEC). This is a Department of Defense (DoD) trusted foundry located in Nashua, NH, that's dedicated to the manufacture of custom GaAs and GaN circuits. Our MEC is a vertically integrated facility that has all the capabilities needed to develop and produce advanced microwave products. This 110,000 ft^2 facility is home to a wafer foundry, MMIC and RF module design teams, on-wafer RF testing, wafer dicing, inspection, post processing, reliability qualification, a microwave module prototyping facility, and a production factory for microwave power amplifier modules utilising our GaN MMICs.

Established in 1984, our MEC has a long history of delivering GaAs and GaN-based microwave products for the DoD. One unique aspect of our foundry is the 150 mm wafer line, offering a higher product yield and a lower chip cost than the industry standard processes based on 100 mm diameter wafers. Our MEC's 150 mm wafer processing line started running production GaAs processes in 2004, with the first 150 mm GaN MMICs reported ten years later.

The 150 mm GaN wafer processes developed at our MEC produce devices with a high yield, excellent performance and impressive reliability – the mean time-to-failure is more than 10 million hours at a channel temperature of 200 °C. In progress at the MEC is a multi-year modernisation project that will add wafer capacity, enabling us to keep pace with the growing demand within the DoD for advanced RF MMIC components.

Miniaturising GaN

Back in 2018, BAE Systems signed a cooperative agreement with the Air Force Research Laboratory (AFRL) to transfer an advanced, high-performance 140 nm GaN process developed by AFRL's research fabrication facility to our production-focused foundry. This new process, with a shorter gate length and superior transistor performance, augments our existing GaN capability and targets applications at millimetre-wave frequencies from 20 GHz to 50 GHz. This frequency domain helps us serve modern defence applications, which are now demanding higher operating frequencies and wider



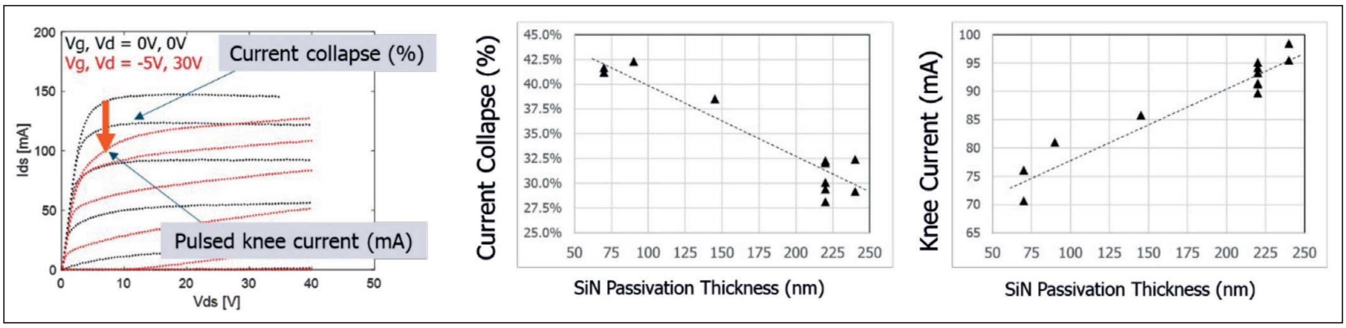
➤ Figure 1. A completed 6-inch GaN-on-SiC wafer fabricated using BAE Systems' 140 nm process.

instantaneous bandwidth, often within small form factor payloads that have limited prime power and thermal management capability.

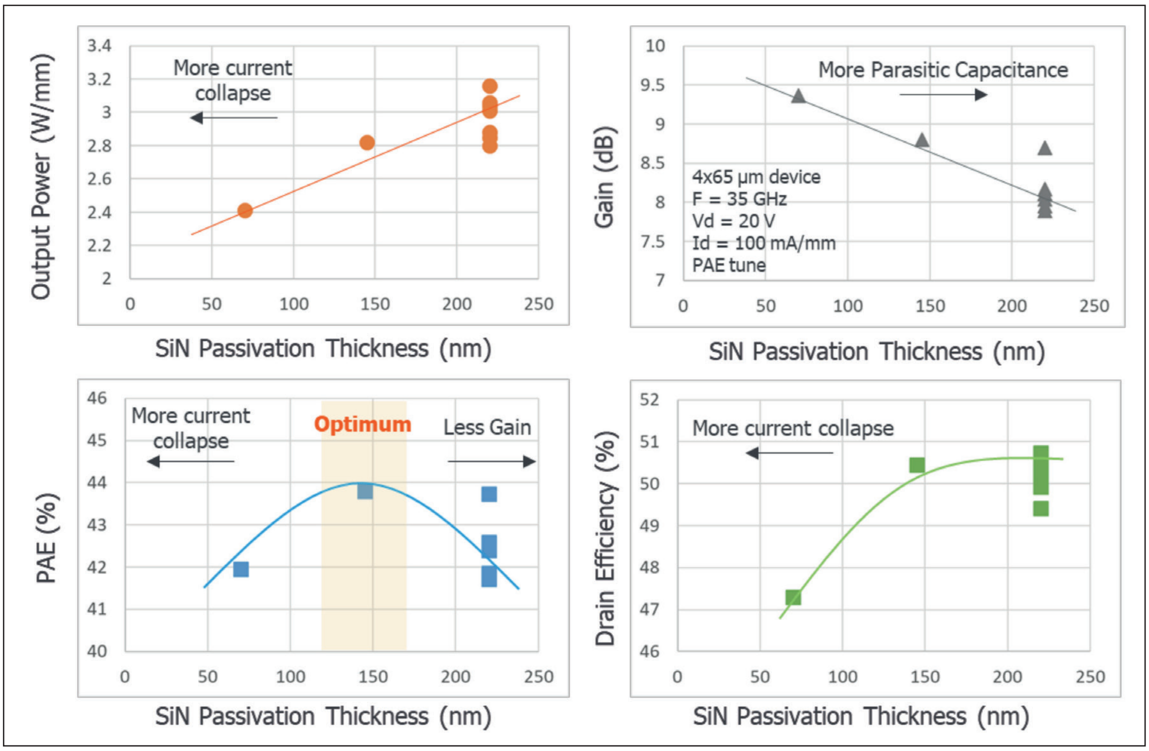
Often our state-of-the-art GaN production devices have an output power that is thermally-limited. To address this drawback, we have tailored our 140 nm GaN technology to offer improvements in gain and power-added efficiency at frequencies up to 50 GHz, while still providing sufficient output power density to meet mission requirements. Through this 'lab to fab' collaboration model, we have successfully transitioned our process and demonstrated state of the art performance, yield, and reliability on our 150 mm production line.

The epitaxial structure for our GaN MMICs is produced by loading SiC substrates in an MOCVD chamber and growing an iron-doped buffer, ollowed by a GaN channel, a 1 nm-thick AlN spacer, a 17 nm-thick $Al_{0.28}Ga_{0.72}N$ layer and a 2 nm-thick GaN cap. We process our epiwafers into devices with a 140 nm gate length. They do not feature source-connected field plates, as this allows us to enhance device gain and reduce parasitic drain-to-source capacitance. Using a gate-source spacing of 0.5 µm and a gate-drain spacing of 2.0 µm, we trim the source resistance and realise a breakdown voltage in excess of 80 V.

To minimise source inductance and enable our microstrip MMICs to operate at high frequencies, we thin substrate thickness to 50 µm. To the best of



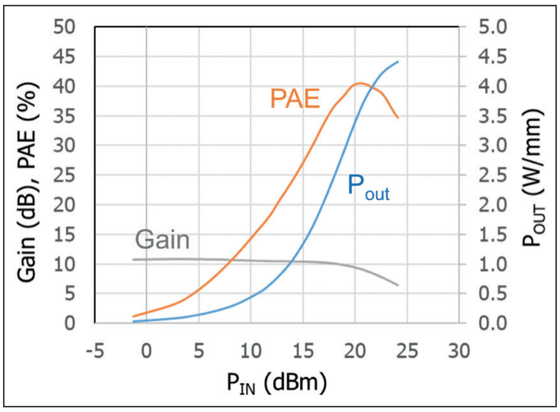
➤ Figure 2. Pulsed current-voltage (I-V) characteristics, including current collapse and pulsed knee current, explored for devices with different SiN passivation thickness. SiN thickness correlates strongly with current collapse.



➤ Figure 3. Ka-band load pull measurements at 35 GHz on devices with different SiN thicknesses. Measured power, efficiency, and gain follow expected trends, with thicker SiN reducing current collapse while also increasing parasitic capacitance. A thickness of about 150 nm is optimal for maximising power-added efficiency (PAE).

our knowledge, this represents the first GaN MMIC process on 150 mm wafers that are thinned to that thickness.

During the development of our 150 mm MMIC process, we discovered that SiN passivation plays a crucial role in determining large-signal device performance. We investigated the impact of passivation thicknesses ranging from 50 nm to 250 nm on the maximum efficiency at Ka-band.

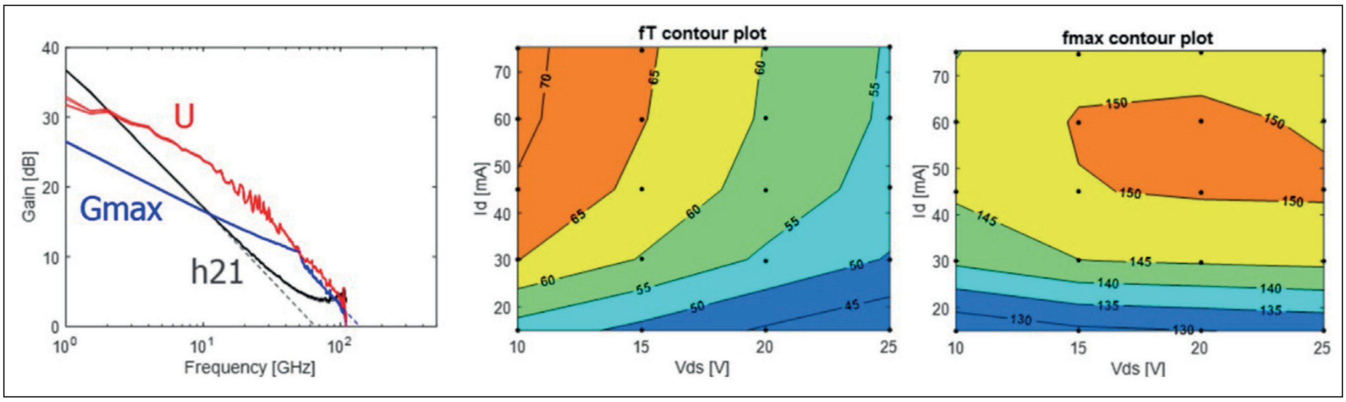


➤ Figure 4. Ka-band, CW, load pull power sweep measured on the optimised device design at a drain voltage (V_D) of 28 V, a drain current (I_D) of 100 mA/ mm, and a frequency of 35 GHz. The device shows a peak power-added efficiency (PAE) of 40 percent, with peak output power of 4.4 W/mm.

This work involved characterisation of 4 x 65 µm and 4 x 75 µm devices, using DC, small-signal, pulsed current-voltage, and Ka-band load-pull performance measurements.

Our devices exhibit a maximum drain current of more than 1.3 A/mm, with a peak transconductance in excess of 390 mS/mm. The DC characteristics are consistent across all passivation thickness variants. Our pulsed current-voltage characteristics on 140 nm devices with different SiN thicknesses are summarised in Figure 2. This data shows that there is a fall in current collapse as the thickness of passivation increases, a finding that is consistent with previous reports within the scientific literature.

During load pull tests, we have observed a clear correlation between current collapse, the pulsed knee current and power performance (see Figure 3 for a summary of the load pull characteristics, such as output power, gain, power-added efficiency and drain efficiency, measured at 35 GHz for devices with different SiN passivation thicknesses). We have acquired our data at a peak power-added efficiency, using a drain voltage of 20 V and a drain current of 100 mA/mm, conditions that optimise efficiency. There is a clear trend in output power, which is boosted by thicker passivation. We attribute this to a greater reduction in current-collapse in the knee region of the current-voltage plane.



➤ Figure 5. Small signal RF measurements of the 140 nm technology, measured on 4 x 75 µm unit cell devices. Under nominal operating conditions, at a drain voltage of 20 V with a drain current (I_D) 100 mA/mm, the devices achieve a cut-off frequency (f_T) of 50 GHz and a maximum oscillation frequency f_{max} of 145 GHz. The f_T and f_{max} contour plots show the impact of quiescent bias on the cut-off frequency.

Plots of power-added efficiency follow a different trend, peaking for a SiN thickness of about 150 nm. The position of this peak is governed by both: the drain efficiency, which improves with thicker passivation, thanks to a reduction in current collapse; and a degradation in device gain with thicker passivation, due to additional parasitic capacitance. We have carried out a power sweep of this optimised device (see Figure 4). At nominal operating conditions of a drain-source voltage of 20 V, this optimised device has a cut-off frequency of 50 GHz and a maximum oscillation frequency of 145 GHz (see Figure 5).

Replacing tubes

In contrast to commercial uses, DoD RF applications target dominance of the full electromagnetic spectrum. This requirement drives a need for amplifiers that cover multiple octaves of instantaneous bandwidth with very high output power levels. Historically, this need has been met by travelling-wave tube amplifiers and other vacuum electronics. However, it is also possible to fulfil these requirements with GaN technology, as we demonstrated at the 2023 *International Microwave Symposium* in San Diego (Figure 6).

At that symposium we reported a 32-38 GHz MMIC. This three-stage, reactively matched power amplifier has a 5 mm by 6 mm footprint and 16.8 mm total transistor periphery. It is a design that uses a 1:2:4 drive ratio to provide sufficient drive to the output stage at baseplate temperatures of up to 125 °C, and features Lange couplers in a balanced configuration to realise efficient on-chip power combining and improve the voltage standing-wave ratio. There are some trade-offs in performance with our design to ensure unconditional stability at temperatures down to -50 °C. Even despite these trade-offs to performance, our MMIC deliver a 25 W output power at a power-added efficiency of more than 20 percent – this represents the highest measured output power from a single die at this frequency range.

We are now developing a new GaN technology. Based on a 90 nm HEMT process and leveraging advanced process features, this technology will enable amplifiers to deliver a higher performance while maintaining customer affordability. This process primarily targets power amplifier applications in the W-band, a frequency domain spanning 75 GHz to 110 GHz and encompassing a local minimum in the atmospheric absorption spectra. We expect this portion of the electromagnetic spectrum to be exploited by radar, missile seekers, synthetic-aperture radio imaging, E-band radio and 6G applications. In the near term, we expect that the proliferation of RF components in this frequency band will drive the need for the US DoD to access the best high-frequency GaN technology, to ensure that it maintains dominance over the electromagnetic spectrum. This need will be met by our 90 nm process, which we will qualify

Based on a 90 nm HEMT process and leveraging advanced process features, this technology will enable amplifiers to deliver a higher performance while maintaining customer affordability. This process primarily targets power amplifier applications in the W-band, a frequency domain spanning 75 GHz to 110 GHz and encompassing a local minimum in the atmospheric absorption spectra

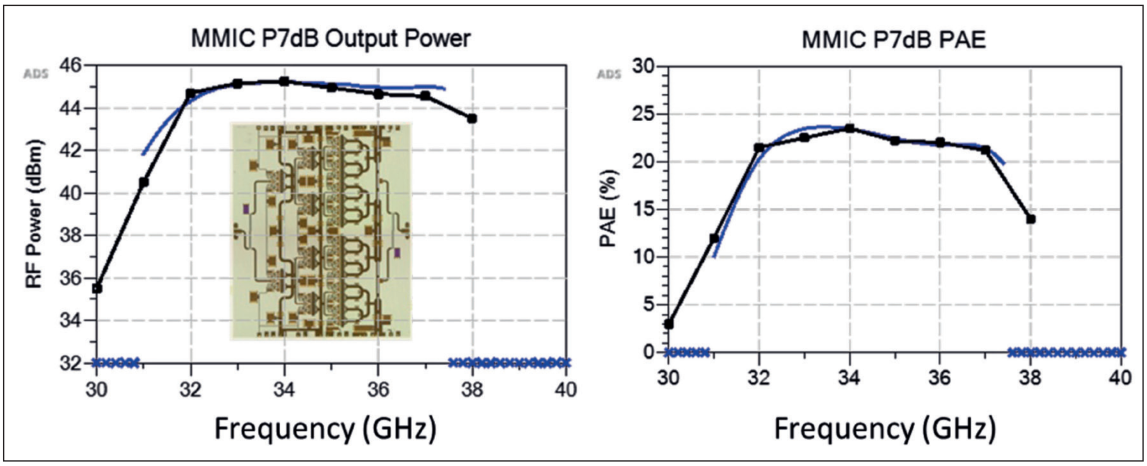


Figure 6. Simulated (blue lines) and measured (black data points) on-wafer power performance of the 32-38 GHz power amplifier MMIC designed into BAE Systems' 140 nm GaN technology.

in the near future with 150 mm wafers.

Our goal is to continue to drive our GaN technology towards more advanced nodes that offer best-in-class defence electronics that meet the needs of the DoD and the warfighter. The electronic-warfare experience at BAE Systems spans more than 60 years, and over that time it has provided assistance in electronic support (rapid detection, missile warning), protection (RF/IR countermeasures, off- and on-board systems), and attack (threat analysis and response, RF/threat management).

Our electronic-warfare systems operate on more than 80 percent of US fixed-wing military aircraft, including platforms such as F-15, B-2, F-22, and F-35.

As part of our commitment to meet the needs of the DoD, we make our GaAs and GaN technologies accessible to the US Defense industry at large through our open foundry service, where we fabricate custom MMIC designs for our customers. We currently offer 100 nm and 70 nm GaAs pHEMT processes, in addition to our 180 nm and 140 nm GaN-on-SiC processes, all on a 150 mm wafer diameter.

Boosting performance with the merged *p-i-n* SiC Schottky diode

Delivering greater reliability at high efficiency, the merged *p-i-n* SiC Schottky diode combines a low forward voltage with high surge-current capability

BY LLEW VAUGHAN-EDMUNDS FROM NAVITAS SEMICONDUCTOR

THE WIDE-BANDGAP REVOLUTION in power conversion is well under way. To fulfil efficiency and power density targets in energy-conscious applications, designers are now rejecting silicon devices in favour of alternatives delivering superior performance.

Offering the greatest commercially maturity within the wide bandgap fraternity is SiC. Producers of this class of semiconductor have now released several generations of diodes and power MOSFETs, each offering successively improved performance. Sales of these devices have soared in recent times to hit nearly $3 billion last year, and growth is forecast to continue at around 40 percent per year as deployment expands into evermore applications.

SiC devices outperform their silicon counterparts in both conduction and switching characteristics. First to market within this family of power devices is the SiC Schottky barrier diode. Compared with the silicon fast-recovery diode, it has a lower forward voltage and a superior reverse recovery. One upshot of these strengths is a tremendous reduction in overall energy losses. Yet another merit of the SiC

Schottky barrier diode is a stable reverse-recovery time over the full operating temperature range. In comparison, the silicon fast-recovery diode is impaired by an lengthening recovery time at higher temperatures.

However, the SiC Schottky barrier diode is far from perfect. All Schottky diodes, regardless of material system, are inherently vulnerable to current surges. This is a known hazard in power-factor correction circuits, used in power supplies for converters and inverter systems.

One option for addressing this issue is to turn to *p-i-n* diodes, which offer greater reliability in such situations. However, reliability is traded for reduced efficiency, due to a higher forward voltage. It's not a great compromise, as a lower energy efficiency is undesirable. In equipment such as server power supplies, a diminished efficiency leads to a higher electricity bill, increased cooling management and a slower return on investment.

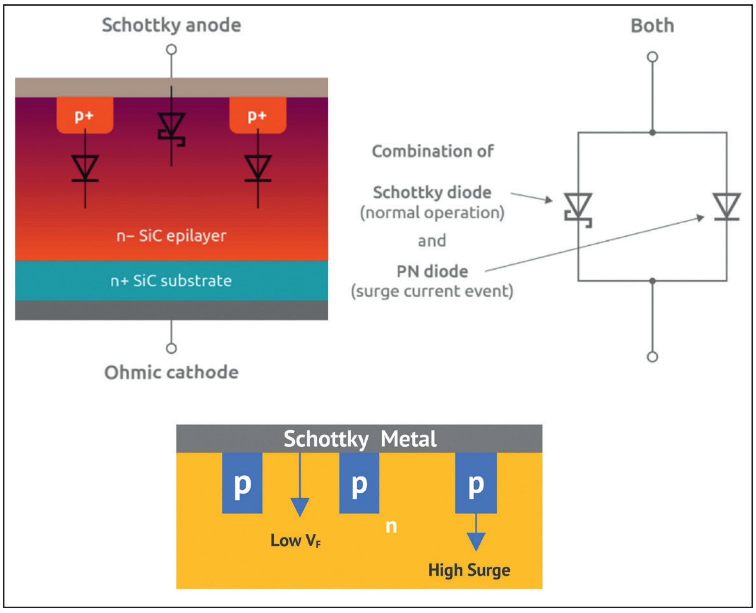
A compelling solution is the merged *p-i-n* SiC Schottky (MPS) diode. This device marries the best features of Schottky and *p-i-n* diodes in a single device by combining the surge-current robustness and low reverse leakage of the *p-i-n* diode with the low forward voltage of the Schottky structure. Equipped with a superior breakdown voltage, excellent reverse-recovery characteristics, stability over temperature, and the high-temperature operating capability associated with all SiC devices, the MPS diodes that have been introduced in power factor correction and boost circuits are enhancing reliability and significantly increasing the overall efficiency of the power-conversion system.

Design and optimisation

A key difference between a conventional Schottky part of the device structure and the MPS diode is that the latter contains additional *p*-doped wells, implanted in the drift zone. These wells form a *p*-ohmic contact with the metal at the Schottky anode, while also creating a *p-n* junction with the SiC drift layer. The result is effectively the combination of a Schottky diode and a *p-i-n* diode, connected in parallel (see Figure 1).

With this design, in normal operation the Schottky carries almost the entire current. On the other hand, during high-current surges, the voltage across the MPS device rises, causing conduction in the drift layer of the *p-i-n* diode. As this intrinsic diode has a lower resistance than the Schottky, current is diverted, reducing dissipation and relieving thermal stress.

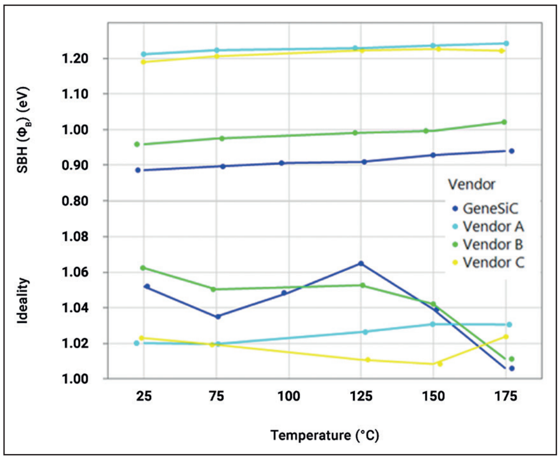
When the MPS diode operates under reverse bias, the maximum field strength occurs across its drift region. This contrasts with the situation in a standard Schottky architecture, where the greatest field strength occurs at the metal barrier. A downside of the Schottky diode is that imperfections in the barrier allow a relatively large leakage current to flow. That's not the case with the MPS diode, which benefits from moving the maximum field strength away from the metal barrier. This design ensures that the leakage is lower than that of a standard SiC Schottky diode.



➤ Figure 1. MPS diodes combine *p-i-n* and Schottky diode attributes.

By optimising the dimensions and doping of the *p*-type wells, device designers can engineer the forward voltage drop, surge-current capability and leakage current of the MPS diode to meet specific requirements. Additional improvement comes from thinning the substrate below the drift region. This trims the MPS forward voltage and the thermal resistance between the Schottky area and back-side metallisation, leading to lower energy losses, enhanced thermal efficiency and greater reliability.

At Navitas, we have an enviable track record in developing and producing SiC MPS diodes. Now in their fifth generation, our 650 V SiC MPS diodes feature a high surge-current capability and a low forward voltage to minimise losses in the forward-biased mode. Our devices also offer an extremely low reverse-leakage current and high avalanche



➤ Figure 2. Low-current, forward current-voltage (I-V) characteristics for 10 A SiC MPS diode.

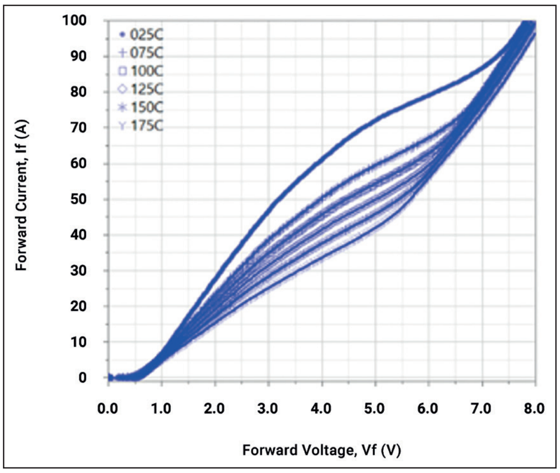


Figure 3. High-current, forward current-voltage (I-V) characteristics from 25 °C to 175 °C.

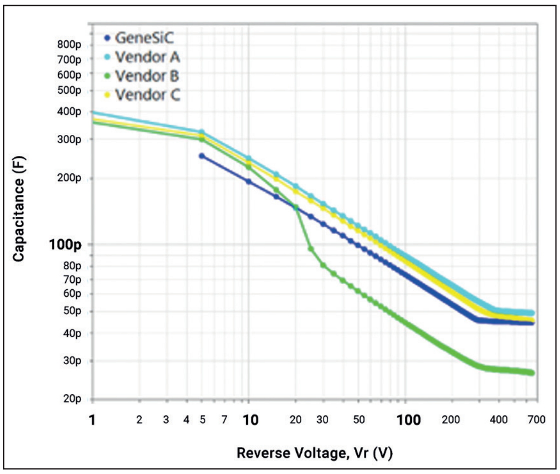


Figure 4. Capacitance-voltage (C-V) curves for Navitas and competitor SiC MPS diodes.

robustness. It is a combination of attributes that comes from optimising the device architecture and engineering the barrier metallurgy to ensure an ultra-low Schottky barrier height of just 0.88 eV at 25 °C.

One of the downsides of typical Schottky and MPS diodes, which feature a titanium metal barrier, is a trade-off between the Schottky barrier height and the reverse leakage current. Thanks to our novel, proprietary barrier metal, our MPS SiC diodes have a Schottky barrier height that's more than 26 percent lower than alternative titanium-barrier devices, and a leakage current of just 100 nA – that is at least six times lower than the norm. In addition, our devices offer enhanced shielding of the Schottky metal interface, minimising any increase in reverse leakage current at higher voltages.

We have measured the forward current-voltage characteristics of these diodes at low currents and at temperatures from 25 °C to 175 °C (see Figure 2). These results reveal consistent linearity across this wide temperature range, indicating a stable Schottky barrier height, indicative of a good spatial homogeneity of the Schottky metal interface.

There is a small increase in the Schottky barrier height. That's a common tendency amongst MPS diodes from various vendors. One way to evaluate this increase is to consider 'ideality', a measure of how closely the diode's behaviour conforms to the ideal diode equation under different conditions. Ideality typically decreases with temperature, and has a value that's close to 1 in well-behaved diodes under normal conditions. If there are deviations from this value, they tend to come from unwanted effects, such as recombination currents and parasitic series resistances. Note that real-world diodes can depart from ideal behaviour, and often display an ideality greater than 1.

We have also recorded the current-voltage characteristics of our MPS diodes at higher currents (see Figure 3). These plots, taken at various

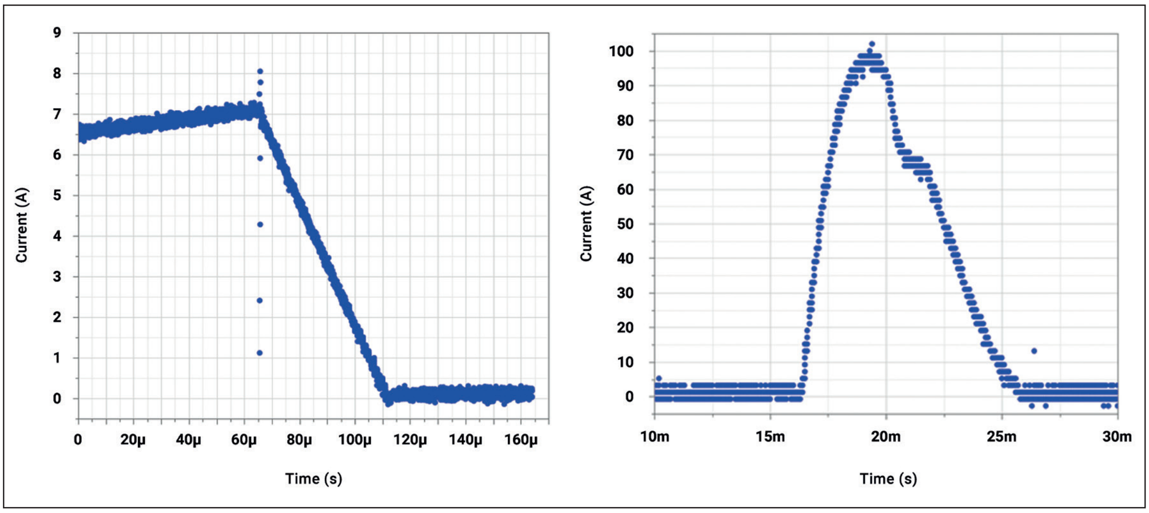


Figure 5. (a) Avalanche testing and (b) surge current characteristics of Navitas MPD diodes.

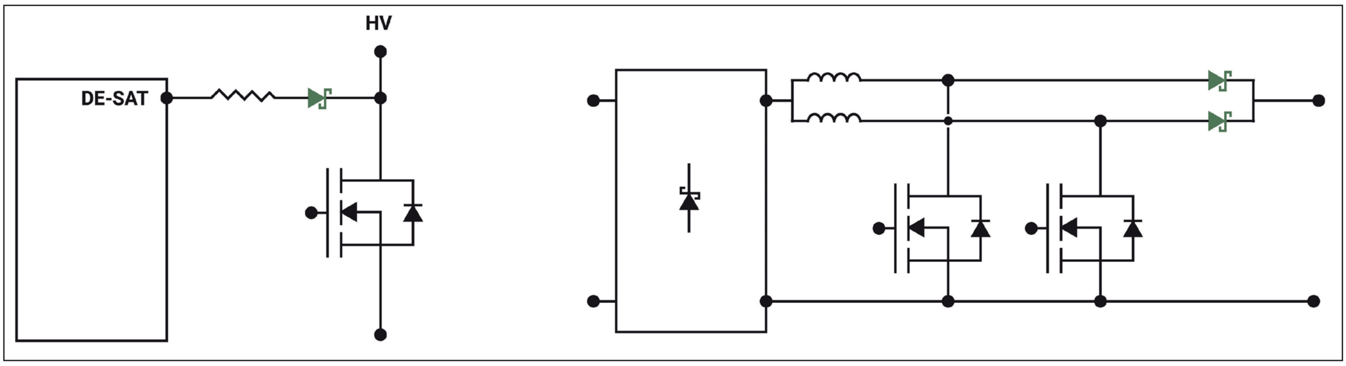


Figure 6. Navitas MPS diodes in a desaturation detection circuit and an interleaved power-factor correction (PFC) circuit.

temperatures, show that there is a cross-over from unipolar (SiC Schottky) to bipolar (*p-i-n*) operation at about 90 A at 25 °C. This cross-over decreases to 50 A at 150 °C. Our plots also show a lowering of the knee-voltage at higher temperatures, which helps maintain a low temperature co-efficient of the on-state voltage drop at the rated current of 10 A.

To benchmark our devices, we have compared the capacitance-voltage curves of our diodes with those of rival products. These plots reveal that our MPS diode has one of the lowest values of capacitance charge, which ensures low reverse-recovery losses.

The low capacitance charge also enables our MPS diodes to have a good value for the common figure-of-merit for this device, defined as the product of capacitance charge and forward voltage. While improvement on one of these fronts tends to be detrimental to the other, a good figure of merit balances a low forward-voltage drop, key to trimming power losses, with a low capacitance charge that ensures superior switching performance. Attaining the lowest possible value for each helps to enhance the overall diode performance in power electronics applications.

Another important characteristic for the MPS diode is its level of avalanche robustness. We assess this with unclamped inductive switching tests. Values for the current waveform under unclamped inductive switching and current-surge conditions reveal a high value for the non-repetitive surge current, confirming our diode's robustness (see Figure 5).

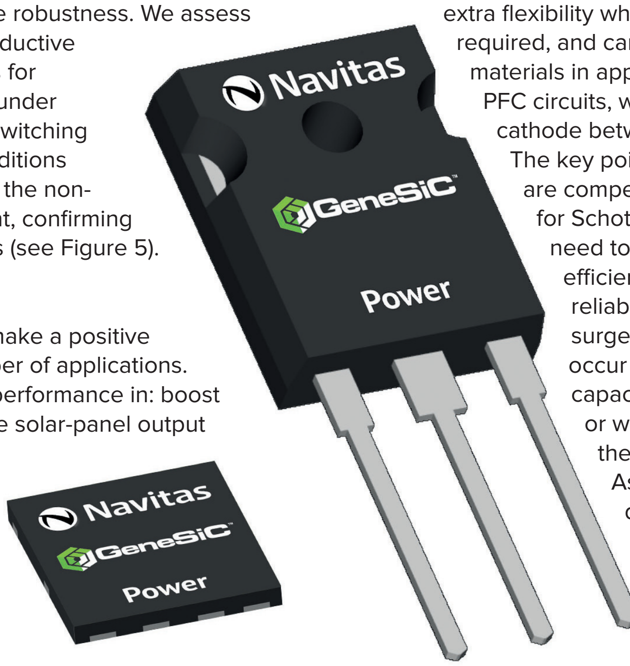
Made for TV

Our MPS diodes can make a positive contribution to a number of applications. They offer a superior performance in: boost circuits, which raise the solar-panel output voltage to the 450-600 V required for the inverter; and in power-factor correction circuits, which are mandatory in line-powered applications above 75 W, according to IEC/EN 61000-3-2. Power-factor correction circuits are used in power supplies for telecom equipment, for data centre servers and for lighting systems.

SiC MPS diodes can also deliver benefits in consumer devices, such as televisions. With the advent of 4K UHD, the latest displays are demanding significantly more power than their predecessors, leading to a greater emphasis on efficiency, for both realising a suitable energy rating and for maintaining proper performance. As well as satisfying this requirement, efficient power supplies usually improve the performance of the display. Often the power supply is positioned directly behind the display, and if it generates too much heat due to a low efficiency, this impairs colour rendition.

We offer our SiC MPS diodes in various package options, which can deliver several advantages in different applications. For high-voltage sensing circuits, like desaturation detectors for overcurrent protection, as well as in the gate-drive bootstrap circuits of high-side switches (see Figure 6), the DO-214 and TO-252-2 packages are ideal solutions.

On the other hand, the TO-247-3 package provides extra flexibility when high-power density is required, and can help reduce the bill of materials in applications like interleaved PFC circuits, which share a common cathode between two diodes. The key point is that SiC MPS diodes are compelling direct replacements for Schottky diodes in circuits that need to combine a high energy efficiency with robustness and reliability when exposed to surge currents. Such conditions occur when powering highly capacitive or inductive loads, or when the power quality of the main AC line is poor. As a straightforward drop-in replacement, our devices are easy to design-in for a significant boost in power-conversion efficiency.



A red-letter day for the microLED

Switching to the cubic form of GaN promises to address the low efficiency of the red microLED, a key ingredient in tomorrow's head-mounted displays

BY MARTIN LAMB FROM KUBOS SEMICONDUCTORS

TODAY, big technology players are driving an explosion of interest in augmented reality (AR) and virtual reality (VR) applications. It is a sector that will be worth many tens of billions of dollars by the end of this decade, and is already triggering frantic development activity within the supply chain. For providers of the key enabling hardware, components and materials, substantial investment has flowed in recent years, spurred on by the opportunity to make a significant contribution to cost-effective, head-mounted displays delivering a world-beating user experience.

A key enabling technology for all AR and VR headsets is the display. Candidate technologies that are being pursued include liquid-crystal-on-silicon (LCoS), organic LEDs (OLEDs), miniLEDs and microLEDs. Already a number of early, head-mounted display products have been launched, with the aim of establishing a foothold in the market.

It may appear that all of these display technologies are promising, since they offer some of the required functionality for AR/VR applications. But the harsh reality is that in many cases they are little more than stop-gaps, falling short of the target for a variety of reasons. High on this list of shortcomings are: a limited battery life; undesirable heating of the headset; and poor visibility of the display in bright conditions, a drawback that leads one to question the usefulness of this technology in genuine AR situations. And on top of these considerations, there is the issue of cost, as well as that of affordability for the consumer.

It is widely acknowledged that if it can be made to work at a full commercial level, the microLED will offer the optimum combination of attributes for this application. By drawing on this miniature source of light, there is the potential to produce near-eye displays that combine affordability with a high efficiency and brightness. According to Yole Intelligence, microLED revenue driven by AR/VR applications will rocket towards the end of this decade, to potentially reach around $1 billion.

However, despite the many millions of dollars that have been invested in the development of the microLED and its associated technologies during the last few years, the commercial success of this emitter is incredibly limited. Today, the microLED is currently confined to a few high-end TV applications, where the resolution of the display can be catered for by simply shrinking current LED technology. When it comes to head-mounted displays, very few early product offerings employ microLEDs – OLEDs and LCoS are preferred, despite their limitations. Given this state-of-affairs, it is obvious that despite significant progress, outstanding issues must be addressed surrounding microLED display technology. Towards the top of this to-do list is the industrial realisation of small-form LEDs with suitable efficiency at longer wavelengths, such as green, amber and red. That's unlikely to be addressed with ease, as it appears that improvements in performance that come from squeezing conventional devices are dwindling. So, since a breakthrough is required, a radical approach is called for. However, there are constraints, as ideally the solution must drop into existing manufacturing lines, while delivering a better performance than today's long-wavelength microLEDs.

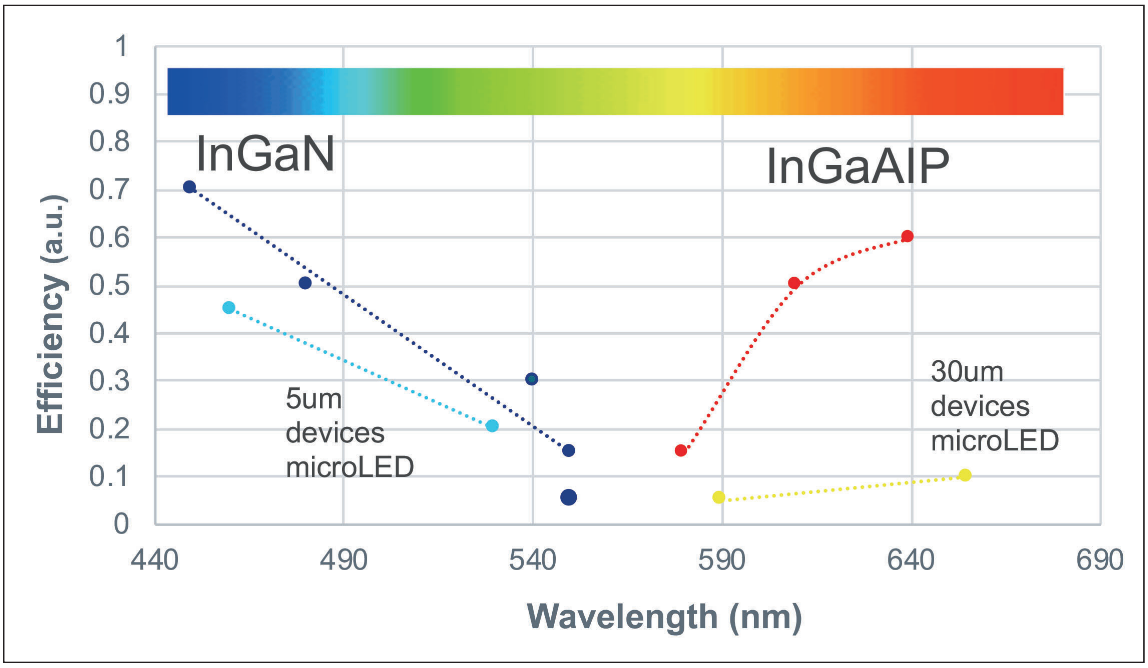
A solution offering much promise is now in the early stages of commercialisation by our team, Kubos Semiconductors. Drawing on technology developed at the University of Cambridge, we initially focused on addressing the shortfall in LED efficiency in the green part of the spectrum, an issue commonly referred to as the 'green gap'. However, recently we have started to expand our exploitation of cubic GaN, using this lesser-known form of GaN for the fabrication of longer-wavelength microLEDs. Read on to discover why cubic GaN holds the key to unlocking the AR/VR displays markets, and why conventional forms of LEDs are inherently compromised for these applications.

Efficiency challenges

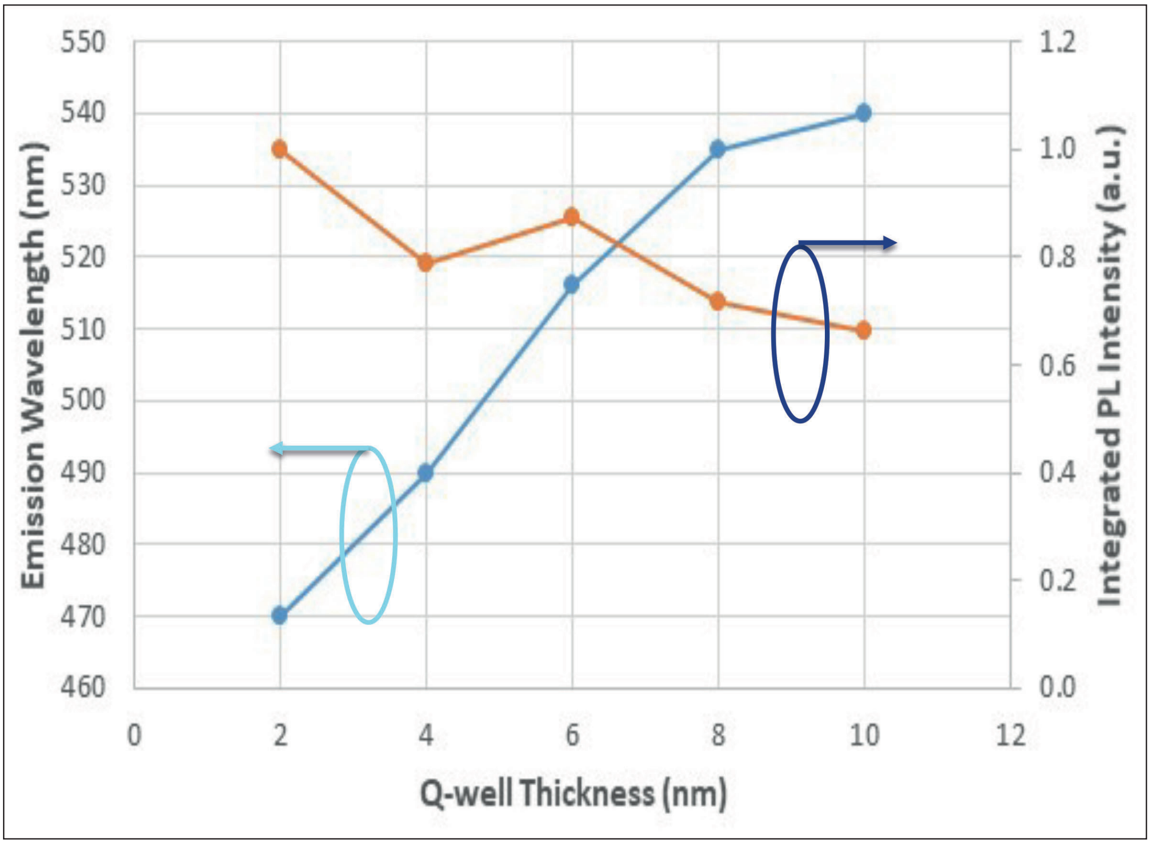
One of the primary pain points facing every would-be maker of microLED displays is the poor efficiency of small-form LEDs. While microLEDs are often defined as having lateral dimensions of less than 100 µm, for typical near-eye displays these dimensions have to shrink to the order of 5 µm and below. At such small dimensions efficiency takes a big hit and drags down critical system attributes in AR/VR headsets, notably those discussed previously. While it might be tempting to think that the brightness of low-efficiency displays can be offset by cranking up the drive current of the microLEDs, this compromises the battery life and generates more stray heat in the headset, which must be dispersed.

Typical high efficiency, large area LEDs are usually constructed from one of two material systems. At the heart of most blue and green emitters are diode structures fabricated from multiple layers of alloys of hexagonal crystalline indium gallium nitride (h-InGaN). Meanwhile, red devices are made from structures comprising multiple layers of alloys of cubic crystalline aluminium indium gallium phosphide (AlInGaP). For both classes of device, efficiency varies with wavelength (see Figure 1), creating an issue that industry continues to wrestle with.

The drivers behind these deleterious trends are well-documented. With the h-InGaN material system it is possible to produce large-scale, blue LEDs with very high efficiency, but this metric falls as the emission wavelength increases, with low values in the green and pitiful ones in the red.



➤ Figure 1. Efficiency versus wavelength for nitride and phosphide LEDs. There is a relatively moderate fall in efficiency in nitride-based devices as their size is reduced to 5 µm. For phosphide-based devices, even reducing the lateral dimensions to 30 µm leads to a significant reduction in efficiency.



➤ Figure 2. The relationship between quantum well thickness, photoluminescence emission wavelength and photoluminescence intensity. Source: University of Cambridge

Explaining this trend are the inherent internal electric fields, present in the quantum wells that form the active part of the device. These fields give rise to the Quantum Confined Stark Effect (QCSE), a phenomenon that pulls apart electrons and holes in the wells, thereby hampering the recombination process that is responsible for light emission. These electric fields are a consequence of both spontaneous polarisation, which results from the asymmetry of the hexagonal crystal lattice; and piezoelectric polarisation, driven by the strain in the structure that arises from the lattice mismatch between the InGaN alloy used in the active region, and the adjacent GaN layers and the substrate.

An additional drawback of the InGaN system is the unwanted consequences associated with increasing the indium content, which is needed to narrow the bandgap of the material and propel its emission to longer wavelengths. Sadly, rising indium content increases the mismatch between the active regions of the device and adjacent layers, resulting in an increase in strain, a stronger QCSE, and ultimately reduced radiative recombination in devices with a longer emission wavelength. Adding insult to injury, the stronger internal electric fields limit the width of the quantum wells that can be employed, and place further constraint on the tools that device designers need to access longer wavelengths.

For the producers of AlInGaP, one consideration is the choice of substrate. Typically, they will use GaAs, or possibly GaP. The former is plentifully available at large diameter and reasonable cost, but it is possible that it could lead to concerns associated with the presence of arsenic in consumer applications

With the AlInGaP system, it is possible to produce highly efficient, large-scale LEDs emitting in the red and amber. However, efforts to shorten the emission towards the green by adjusting alloy composition lead to a transition from a direct to an indirect bandgap for the quantum wells, thereby inhibiting carrier recombination and suppressing the device's emission efficiency. Due to the limited bandgap of the phosphides, it is completely impossible to cover the blue end of the spectrum with this material system.

For the producers of AlInGaP, one consideration is the choice of substrate. Typically, they will use GaAs, or possibly GaP. The former is plentifully available at large diameter and reasonable cost, but it is possible that it could lead to concerns associated with the presence of arsenic in consumer applications. Meanwhile, the downside of GaP is that it is challenging to produce large diameter material, although it may be possible to overcome this by turning to a composite substrate. Nevertheless, despite these issues, and a lack of simplicity that comes from having to use two fundamentally different material systems to address the range of colours required for a display, the AlInGaP system does have potential for providing red devices, so long as they maintain their efficiency advantages over h-InGaN at the smaller scale.

And therein lies the problem. As is clear to see in Figure 1, the emission efficiency plummets when shrinking the lateral dimensions of LEDs made from these material systems to a few microns. This fall in efficiency stems from the increased ratio of sidewall surface area to active volume, a condition that causes recombination processes that occur at or near the sidewalls of the device to dominate its characteristics. If these processes result in the non-radiative recombination of carriers – and the evidence is that they do – the emission efficiency is greatly reduced in small form devices.

Managing these undesirable surface-related phenomena has been a major focus for the LED industry. Measures that have been taken include the application of coatings to passivate surfaces, and the use of thermal treatments to repair crystalline damage that's inflicted by dry etching, which is used to form LED mesas.

In the h-InGaN system these treatments are reasonably effective: the material is reasonably hard and can be repaired, but the act of shrinking the device still results in a significant reduction in efficiency. Devices emitting in the blue and the green are probably adequate, particularly given the increased sensitivity of the human eye to green light, but in the red region where the underlying efficiency is already low for large LEDs, the reduction in scale makes the efficacy questionable in today's small devices made in h-InGaN. For AlInGaP, the picture is even bleaker. In this material system there is a higher surface recombination velocity, which magnifies the surface recombination problem, and makes size reduction an even greater challenge. As a consequence of these efficiency-related issues, the production of red microLEDs based on either h-InGaN or AlInGaP remains a work-in-progress.

These problems have been well known for a long time. Efforts to tackle them date back more than a decade, and have been supported by millions of dollars of investment. But there's yet to be a significant breakthrough – so perhaps it is time for a new approach.

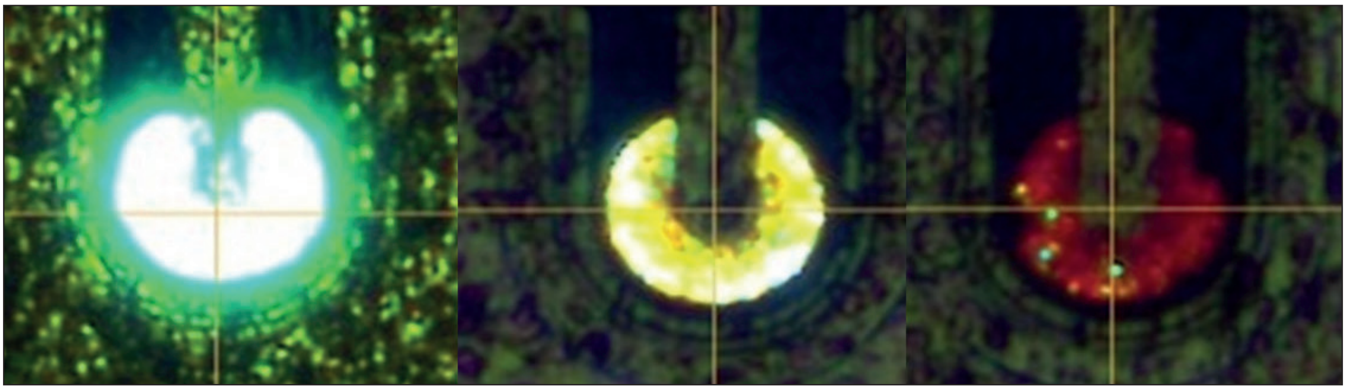
The case for cubic GaN

While many companies continue to throw money and resources at conventional material systems, there's no sign of a breakthrough. What's far more likely is progress on this front will continue to be slow, incremental and costly.

Given this unappealing prospect, there is much to like about the technology that we are pioneering. By taking a fundamentally different approach, we are opening the door to realising an efficiency performance in the longer-wavelength microLEDs that the industry craves, while ensuring that red, green and blue microLEDs can be produced with a single material system. In addition, our technology has the benefits of being fully scalable, and able to be simply 'dropped into' existing manufacturing lines. In short it is GaN, but not as the world knows it: it's cubic GaN.

It has long been known that the group III nitrides, namely AlN, GaN and InN, and all their well-related alloys, tend to crystallise in a stable hexagonal structure. This is the structure of the LEDs that light our homes, our streets and our offices. However, the group III nitrides can also crystallise in a cubic structure. This alternative form, denoted c-GaN or c-InGaN for the ternary alloy, offers a number of potential benefits over the established structure.

One of the major benefits of c-GaN is that it is completely free from the internal electric fields that cause the QCSE and are to blame for the collapse in efficiency with increasing wavelength. The absence of internal electric fields, resulting from the higher symmetry of the cubic crystal structure, offers the possibility of using wider quantum wells to access longer wavelengths, an approach that's precluded in h-InGaN devices. Another advantage is a reduction in screening at high drive currents, giving diminished blue shift compared to that observed in h-InGaN devices where a device might emit red light



➤ Figure 3. Kubos' cubic InGaN microLEDs produced using MOCVD and demonstrating green, amber and red emission.

> In c-GaN it is possible to enjoy a higher hole mobility and a higher maximum hole concentration than it is in h-GaN. These are valued attributes, as the ability to realise highly conductive *p*-type layers is vital to successful LED operation at high current densities.

at low drive currents and yellow or green light as the current is increased.

Another advantage of c-GaN is its more favourable bandgap. For this form of GaN, the bandgap is 3.2 eV, compared to 3.4 eV for h-GaN. The reduction in bandgap means that the baseline emission from a device employing c-GaN will be at a longer wavelength, even before the addition of indium. Thanks to this, wells with a lower indium content can access a given wavelength when compared with h-InGaN devices, enabling improved crystal quality. It is also possible to turn to wider wells with this material system, thereby equipping device designers with an additional degree of freedom.

As well as these strengths, associated with the light-generation process, there are merits realised by superior carrier transport. In c-GaN it is possible to enjoy a higher hole mobility and a higher maximum hole concentration than it is in h-GaN. These are valued attributes, as the ability to realise highly conductive *p*-type layers is vital to successful LED operation at high current densities.

While c-GaN has many strengths over h-GaN, both materials have much in common. Consequently, it's anticipated that the measures for mitigating the influence of a fall in device efficiency with scaling can be transferred from one form of GaN to another.

Given these very compelling arguments, on paper at least, c-GaN and its alloys are poised to revolutionise the microLED business, so long as the theoretical advantages can be delivered in practice.

State of play

We have made much progress with our technology. We have established and are now commercialising a reliable and scalable route for manufacturing single phase, cubic III-nitride epilayers. Our material is grown on a standard, vicinal (001) silicon substrate that's coated with a thin epitaxial layer of 3c-SiC to provide a reasonable lattice match and a suitable cubic template. Growth involves industry-standard MOCVD equipment and precursors.

We have demonstrated growth on 150 mm diameter substrates and our potential to scale to larger diameters is clear. Additional advances include the fabrication of test diodes, using processes similar to those employed for h-InGaN.

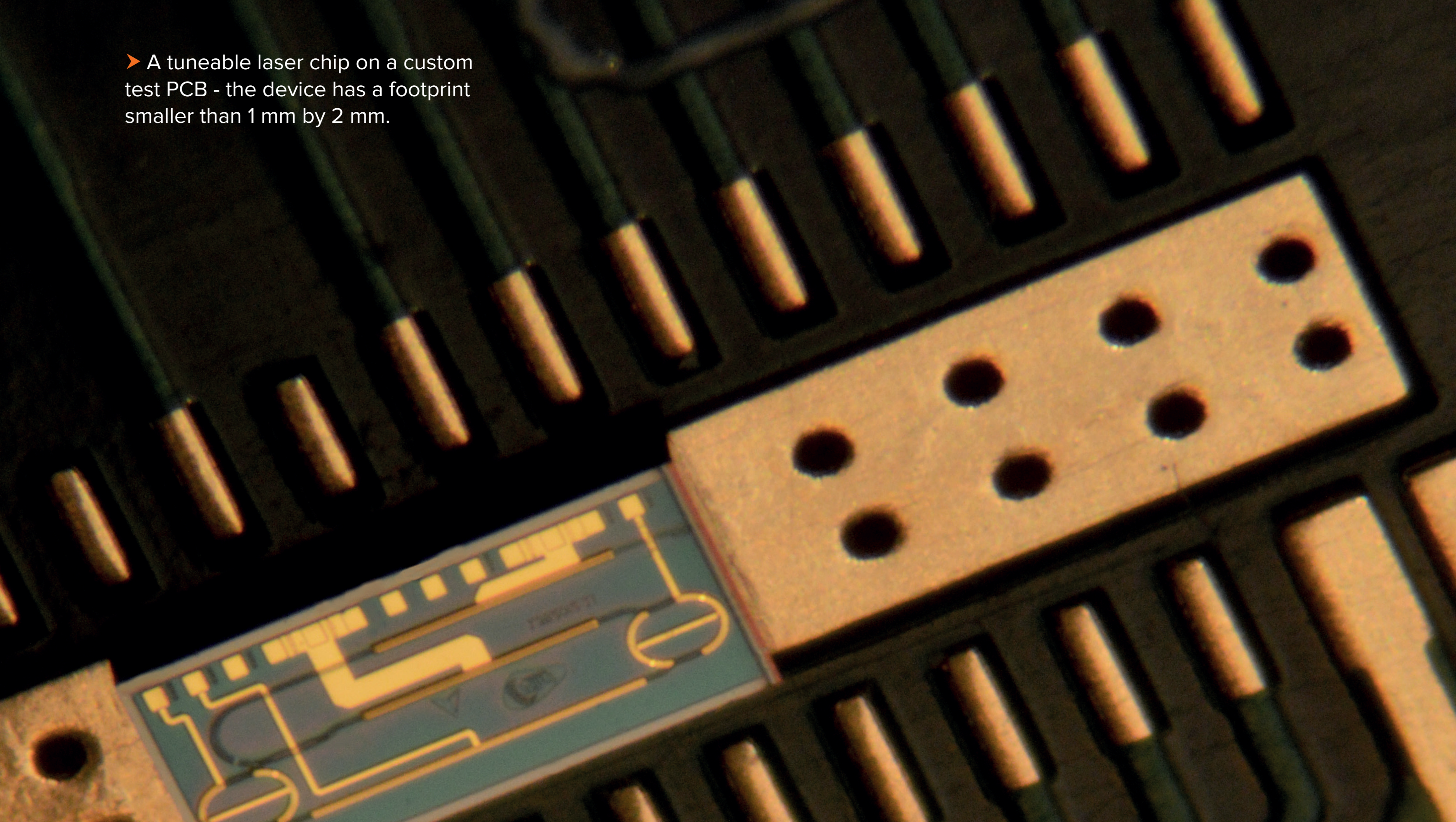
One of the highlights of our progress to date is the confirmation that by switching from h-GaN to c-GaN it is possible to produce longer-wavelength emitters with considerably reduced indium content in the quantum wells. We have produced LEDs emitting at 540 nm with an indium content of 10 percent. In h-InGaN, such a device would typically require around 17 percent indium content at 450 nm.

Another potential benefit that we have verified is that wider wells can produce emission, thanks to the absence, or at least the substantial reduction, of the internal electric field within the device. We have produced emitters that have 10 nm-wide wells, which would lead to very little emission in h-InGaN (see Figure 2).

We have also demonstrated that this material system can be engineered to generate light across the whole visible spectrum, potentially opening the way for a monolithic solution.

In addition to these performance benefits, we have shown that it's possible to process c-InGaN layers into test devices using existing manufacturing lines. This supports the thesis that the material might behave similarly to h-InGaN with respect to measures aimed at managing the impact of size reduction on LED efficiency. It also suggests that this material could be a drop-in replacement for h-InGaN. While we still need to work on optimising the efficiency of the emission of our devices, we have already provided ample evidence that for any project aiming to produce adequate efficiency in the green, amber, and red, the cubic InGaN system is worthy of consideration.

Encouragingly, our work is already receiving recognition. Recently, we won support for a project aimed at making red microLEDs, with funding coming from Innovate UK's Future Economy Investor Partnerships scheme. This investment will help us build on the exciting signs that cubic GaN can genuinely circumvent the physics that causes the bottleneck in the performance of longer-wavelength microLEDs, providing a near-term breakthrough for miniaturised red emitters that everyone has been looking for to unlock the AR/VR display market. Switching to the cubic form of GaN promises to address the low efficiency of the red microLED, a key ingredient in tomorrow's head-mounted displays.



A tuneable laser chip on a custom test PCB - the device has a footprint smaller than 1 mm by 2 mm.

Tuneable lasers:
The elusive trifecta

Integrated tuneable laser assemblies serving in the C- and O- bands excel on three fronts by offering the unique combination of wide tuning, fast-nanosecond switching and a narrow linewidth

BY CAOLÁN MURPHY, SHANE DUGGAN, GAURAV JAIN, CRISTIAN VARGAS, AND DESI GUTIERREZ FROM PILOT PHOTONICS

TUNEABLE LASERS are now established as a key enabling technology in a wide range of applications, spanning various fields from optical communications to sensing.

In telecommunication infrastructure, particularly in the long-haul and metro networks, widely tuneable lasers with a low linewidth are indispensable components. When incorporated in coherent transceivers, their low linewidth enables increased data rates by supporting advanced modulation formats within dense wavelength-division multiplexing systems. The wide wavelength tuneability is a valued asset, simplifying network design and management by enabling resources to be dynamically assigned and optimised while reducing inventory requirements.

Meanwhile, in optical fibre sensing applications, such as fibre Bragg grating sensing, fast-swept tuneable lasers are used to interrogate sensors with Bragg gratings inscribed into optical fibres. These gratings reflect specific wavelengths of light, based on the strain and the temperature applied to the fibre, to create a distinctive spectral signature. When lasers offer fast switching and are widely tuneable, this enables precise and fast wavelength sweeps across the fibre Bragg grating sensor's bandwidth to ensure real-time, accurate readings of strain or temperature.

Fast tuneable lasers have also played a key role in the development of many optical switching architectures, involving rapid adjustments to the laser wavelength to quickly switch or route optical traffic without having to convert signals to the electronic form.

There is no doubt that the versatility of the tuneable laser has enabled widespread applications. However, today's commercially available widely tuneable lasers still fall short in some areas. In particular, they struggle to serve in applications requiring phase-sensitivity and very fast-switching/sweeping.

For instance, for frequency-modulated continuous-wave lidar, a cutting-edge technology in autonomous vehicles and remote sensing, they are not adept at providing the low linewidth and ultra-fast sweeping capabilities needed to precisely measure distances and velocities. Additionally, in systems that employ coherent optical time-domain reflectometry and optical frequency-domain reflectometry, rapid, phase-sensitive tuning is critical for accurate detection of disturbances or variations along the optical fibre, or for other devices under test. If optical packet or optical burst systems are to re-emerge, they will have to align with the demands of today's high-speed data transmission, which requires not only very fast wavelength switching, but the ability to handle phase-sensitive modulation formats.

Unfortunately, today's widely tuneable semiconductor lasers are not great allrounders. Typically, they offer either a narrow linewidth or fast tuning – but not both. An example is the sampled-grating distributed Bragg reflector laser, which is capable of tuning across tens of nanometres using the Vernier tuning effect, thanks to a current-injection-based tuning mechanism that enables swift optical switching. However, this comes at the expense of increased phase noise and broader linewidths, rendering this design unsuitable for the aforementioned applications.

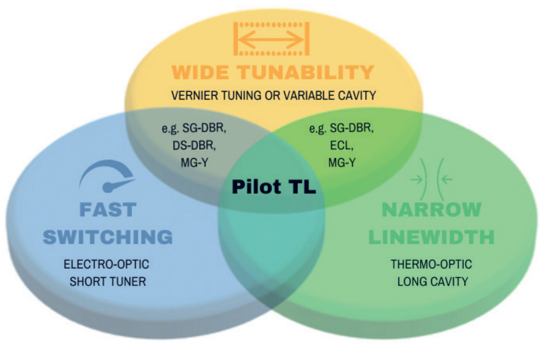
The alternative is to make use of an equivalent thermally tuned laser. This class of laser is capable of realising similar tuning ranges, while boasting low linewidths. However, fast electronic tuning is sacrificed. Similarly, SiN ring-resonator-based devices major in ultra-low linewidths via thermal tuning, but dramatically reduce switching speeds, also limiting usage in these applications.

The elusive combination of a broad tuning range, narrow linewidth and either rapid switching or sweeping, has been a long-standing industrial challenge. Breaking through this impasse to fulfil the elusive trifecta is our team at Pilot Photonics of Dublin, Ireland. Working with the InP foundry Smart Photonics, we are trailblazing lasers that blend all three desirable properties.

➤ Figure 1. Tuneable laser form factor offerings: Photonic Integrated Circuit (PIC), the laser cavity consists of a gain section providing optical gain in either the C or O bands, two ring sections that act as tuneable mode selectors through the Vernier effect, and a common phase section to allow finer tuning of the laser cavity mode; 14-pin butterfly package; OEM benchtop unit; nano-integrated tuneable laser assembly package.

Available in both the C-band and O-band, our ground-breaking lasers unlock new possibilities across a spectrum of applications, from lidar to optical coherence tomography, dense wavelength division multiplexing, coherent optical communication, distributed fibre sensing, gas sensing, sensor interrogation, fibre optic testing, and optical switching. That's a vast and varied range of applications.

Currently available in a 14-pin butterfly package, or instrument formfactor, our nano-integrated tuneable laser assembly that's targeting high-volume communication applications will be released later this year (see Figure 1). Each package features an integrated feedback control, based on wavelength-meter and wavelength-locker systems. Incorporated in the wavelength meter are a linear filter and a photodetector, employed to estimate the current lasing wavelength, and a wavelength locker that consists of an etalon and photodetector – this allows the monitoring of the wavelength on a 50 GHz or 200 GHz grid. Combining the two feedback systems ensures closed-loop control of the device during operation.



➤ The three desirable characteristics for tuneable lasers, as well as the typical design rules required to achieve them. Few designs are able to achieve the combination of wide tunability, fast switching and narrow linewidth.

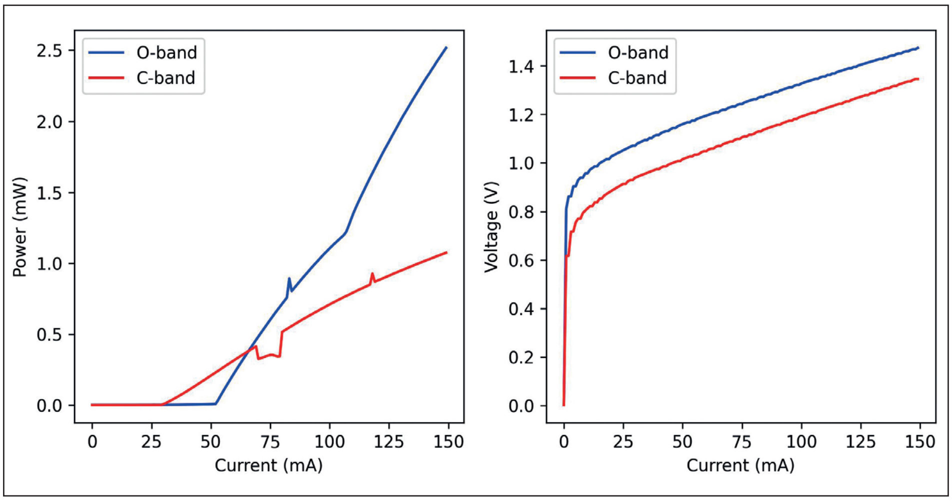


Figure 2. Example of Light-Current (L-I) and Current-Voltage (I-V) curves. The C-band device has a threshold current of 30 mA, while the O-band device has a higher threshold of 50 mA. However, a higher slope efficiency in the O-band device results in a higher optical power at a nominal current of 100 mA. The O-band device is expected to operate at a higher voltage due to the wider bandgap required to generate light in the O-band.

Monolithic dual ring architecture

Our lasers are fabricated on a monolithic InP chip utilising an active-passive integration scheme. The design employs a looped cavity with a gain section that provides optical gain, and two ring-resonators that act as transmission filters for wavelength selectivity through Vernier tuning (see Figure 1 for details). The ring-resonators, which are electro-optically tuned through reverse-bias voltage application, have remarkably low dark currents – they are in the low milliampere range. These low-power, low-current passive tuning sections are crucial to realising optimum device performance. Low dark currents minimise linewidth broadening and device power consumption, while low heat dissipation in the tuning sections eradicates troublesome slow thermal transients. Thanks to these strengths, we realise nanosecond-level switching speeds.

Wide-band tuning is achieved with the Vernier effect. The desired emission wavelength is selected through the overlap of the transmission filters of two ring resonators, each with a slightly different free spectral range. These filters produce a series of discrete lasing modes when one ring is tuned relative to the other. A long phase tuning section in the large outer loop provides fine tuning of the cavity mode within the ring filter envelope.

One of the benefits of the Vernier mechanism is that it opens up an avenue for 'step-and-sweep' style tuning, important for many frequency-modulated continuous-wave lidar systems. The idea behind step-and-sweep is as follows: tune the rings relative to each other to produce a series of discontinuous hops between ring modes (step), before ramping the phase section with a defined signal to produce a continuous change in frequency (sweep) within each of these modes.

To increase the output power, we integrate a semiconductor optical amplifier. This boosts the output to 30 mW (+14 dBm), with further increases

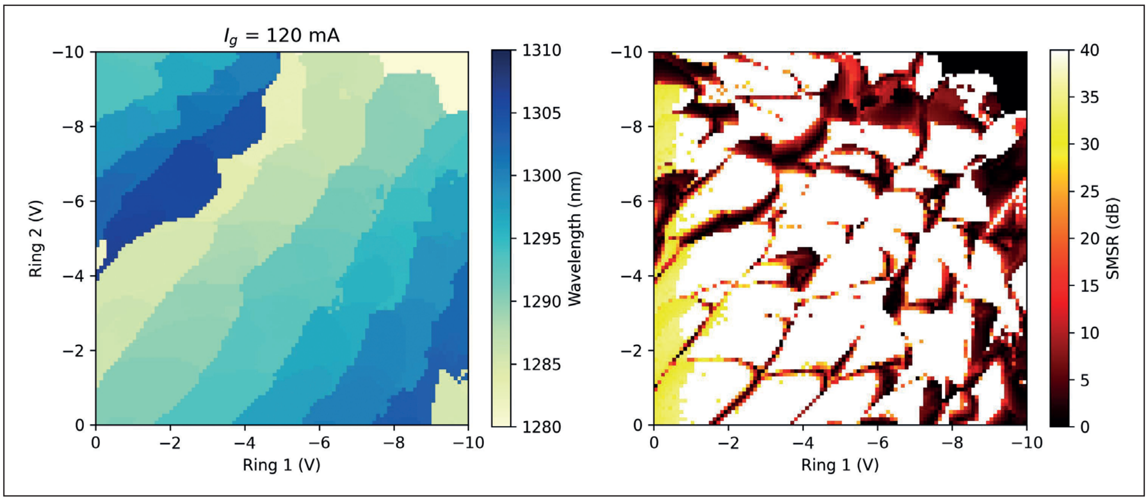


Figure 3. Mode maps generated by sweeping voltages to the two ring tuners (with current into the gain section and voltage to the phase section held fixed). The wavelength map on the left shows a series of discrete regions, in which wavelength is relatively fixed (the modes). A map of the side-mode suppression ratio (SMSR) on the right indicates regions where only a single lasing mode is dominating. Regions of low SMSR (<30 dB) indicate a transition between modes (mode hops).

expected. The addition of this amplifier also enables output power stabilisation, thanks to the possibility to readjust the output independently from the cavity.

We have recorded the characteristics of our original C-band designs and our more recent designs in the O-band. By plotting light-current-voltage curves, we have determined the likes of lasing threshold, slope efficiency and power consumption. Our C-band devices, which do not include a semiconductor optical amplifier, produce an optical output power of 0.5-1.0 mW. O-band variants have a higher lasing threshold but compensate with higher optical powers. Without the addition of the amplifier, the output power is 1.0-2.5 mW (see Figure 2). During normal operation, the devices typically consume 130 mW, excluding the power drawn by the thermo-electric cooler.

For the spectral characterisation of our devices, we use 'mode-maps'. These two-dimensional maps represent the tuning space of the laser – in other words, the lasing wavelengths produced by every combination of voltages supplied to the two rings on a two-dimensional grid (see Figure 3 for more details). These wavelength maps feature a series of discrete regions (modes), in which the wavelength varies continuously. Crossing a boundary between the modes results in a wavelength discontinuity, known as a mode-hop.

Another important quantity to record on these maps is the side-mode suppression ratio. The value for this ratio offers an insight into the competing modes in the optical spectrum – when this ratio is low, that's below 30 dB, a mode hop is about to occur.

These maps can also be used to determine suitable operating points for the laser under step-and-sweep operation, and to identify optical switching pairs.

By sweeping the phase section, the tuning space for these maps expands into the third dimension, providing a more comprehensive characterisation. However, such maps are much more difficult to visualise.

We have used mode maps to determine the tuning range for our lasers. It's nearly 30 nm in the O-band and over 35 nm in the C-band.

Once a suitable set of operating points are extracted from the mode maps, it is possible to measure the optical switching speed (see Figure 4). To validate the nano-second switching speeds expected from the device, we use a simple frequency discrimination technique. By supplying one or more tuners with a low-frequency square-wave signal, with a suitable amplitude to produce a hop between two modes, we produce a repetitive optical switching signal. Following photodetection, this produces an electrical signal of the same frequency as the input signal, with the rise/fall time being equal to the optical switching time.

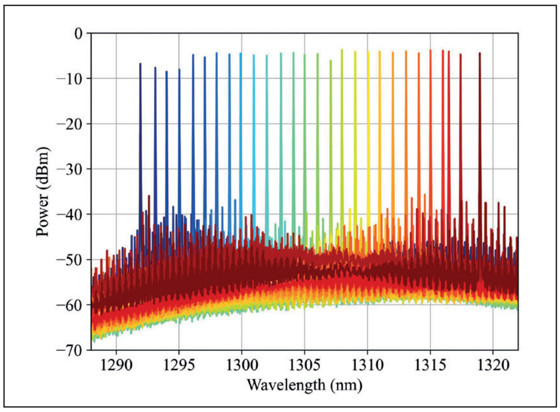


Figure 4. A set of individual spectra taken across the optical O-band. Each line represents a discrete tuning mode of the laser.

Using this method, we have recorded switching speeds consistently below 10 ns, and as short as 3.6 ns (see Figure 5 for more details). That's up to three orders of magnitude faster than typical lasers based on thermal tuning.

Having established that our laser is fast, the next crucial question is this: what is its noise characteristics, and in particular its linewidth? To answer this, we have used a delayed self-heterodyne technique to measure the linewidth, obtaining values from 400 kHz down to 100 kHz in both C- and O-band devices (see Figure 6). While this is still broader than most external-cavity-type

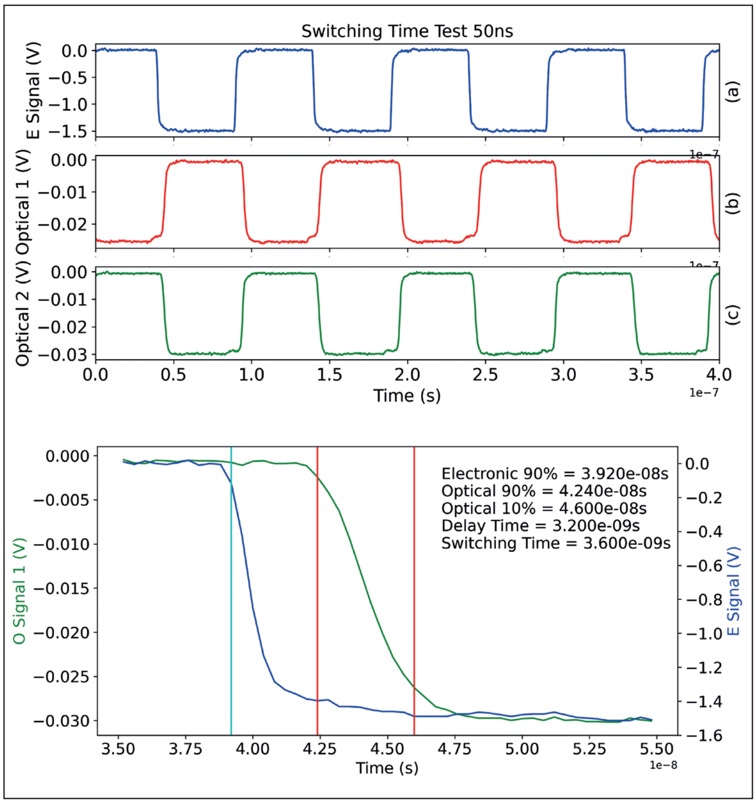


Figure 5. A switching speed measurement taken using a frequency discriminator. The square-wave voltage applied to one of the rings (a) produces two complimentary optical signals (b), (c) – one for when the optical filter is centred on each of the two switching modes. The switching time is equal to the fall time of the optical signal, measured to be 3.6 ns.

lasers, it is a significant improvement over fast-tuning sampled-grating distributed Bragg reflector lasers, which would be expected to have linewidths in the megahertz range. The level of noise indicates that our devices are suitable for coherent transmission applications. With our collaborators in Dublin City University, we have proven this, realising 480 Gbit/s 16-QAM transmission over 25 km of optical fibre. This result demonstrates the capability of our lasers for serving in optical access, metro, and data-centre networks.

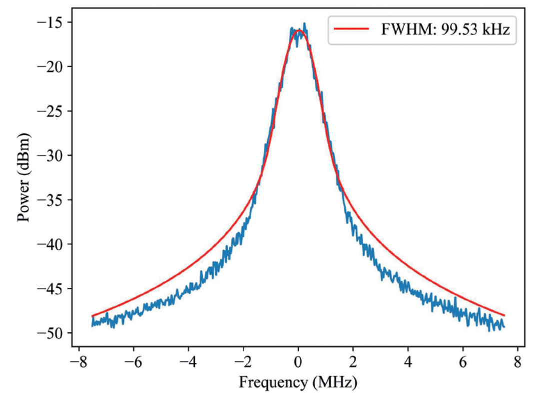
Future impact

According to the *Tunable Laser Market Research Report*, published by Market Research Community, the tuneable laser market is projected to grow by 8.8 percent per year from now to 2030, by which time it will climb to $23.2 billion. Helping to fuel this growth will be improvements to the technology, such as those just described, that will enable new applications, enhance existing ones and have far-reaching impacts on healthcare, telecommunications, transportation and many other sectors.

There is no doubt that producing tuneable lasers that combine wide tunability with a low linewidth and either ultra-fast switching or sweeping is an important step forward. In the optical networking field, it enables new datacentre switching architectures that promise to trim power consumption by keeping as much traffic in the optical domain as possible, and only converting to the electronic domain the traffic that is necessary.

The evolution of telecom protocols like 5G and the anticipated 6G necessitate ever-faster laser switching speeds, wide tunability, and low latency – all are required to ensure the seamless communication that's essential for our connected future. Moreover, the impact of lasers that excel on all these three fronts extends to advancements in metrology techniques, benefiting applications such as lidar, healthcare diagnostics and industrial sensing, where phase sensitivity and speed are critical.

Key to the potential of this unique laser is its monolithic integration. Thanks to this, it can be manufactured at wafer scale using today's InP processing techniques, ensuring a cost profile that is compatible with the very high-volume applications envisaged today and into the future.



➤ Figure 6. Spectrum fitted to a Voigt profile. Lorentzian linewidths as low as 100 kHz have been recorded.

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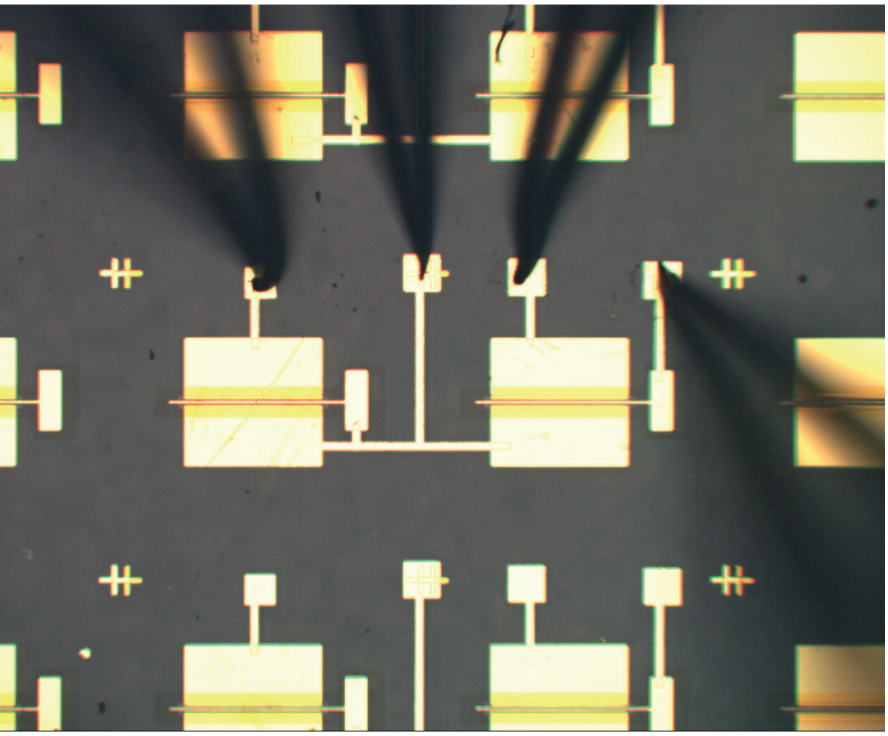
Ga_2O_3 ICs offer exceptional promise for extreme environments

Fabricating logic circuits and flash memory highlights the potential of Ga_2O_3 ICs for serving in extreme environments

BY VISHAL KHANDELWAL, SARAVANAN YUVARAJA, XIAO TANG AND XIAOHANG LI FROM KAUST

MOST COMPUTERS have a relatively easy life. Whether in the form of a desktop, a laptop or a mobile device, they don't tend to suffer from severe heat or cold, they don't take much physical punishment, and thanks to the Earth's magnetic fields, they are not bombarded by radiation.

But that's not the case for all computers. Some have to endure extreme environments, including the likes of extreme cold, intense heat, electrical storms and high-energy radiation. For example, when computers are deployed in space missions, such as interplanetary space exploration, they are subjected to extreme temperatures and intense levels of radiation. High levels of radiation are also found in terrestrial nuclear reactors, while temperatures extremes are present at geothermal sites and in cryo electronics, a promising option for quantum computing.



At the heart of every computer are electronic ICs, which, when operating in extreme environments, have to function flawlessly under the likes of electrical storms, temperatures close to absolute zero and intense radiation. As these conditions threaten to damage and eventually degrade the IC, it is critical to develop electronics specifically designed to excel in these challenging environments.

For computers that operate in extreme environments, the two most important scenarios to consider are a high level of radiation and extreme temperatures. Each presents their own set of challenges and opportunities.

Let's begin by considering radiation. This damages electronic systems through energetic particles and strong electromagnetic fields, creating issues that include resets, failures, signal glitches, noise, physical damage, and system shutdown. One of the drawbacks of most of today's space electronics, which is based on silicon, is that it can only handle radiation up to 5 krad without damage. So, to operate in conditions where radiation is stronger, electronics are covered by heavy radiation-protecting shielding. However, even with this shielding, electronics degrades over time, reducing functionality and thus the lifetime of the space mission. For instance, the expected lifetime of satellites with silicon electronics is just 3 to 5 years, while the requirement for those in a geostationary orbit is much longer, typically 10 to 20 years. Due to this, solutions are needed to improve radiation tolerance in various digital and mixed-signal electronics, including ASICs and FPGAs, as well as complex heterogeneous integration microsystems.

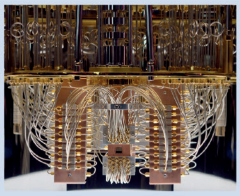
	Space	Petrochemical	Geothermal	Quantum
				
Temperature	2K - 500 °C	200 °C	400 °C	≤4 K
Radiation (Rads/yr)	30-1141	NA	NA	NA

Table 1. Working conditions of electronics in extreme environments.

In terms of temperature, standard silicon electronics is quite limited, with reliable operation possible between -40 °C to 150 °C. This is a major concern in a variety of applications. In oil and gas drilling, petrochemical applications and hypersonic vehicles, temperatures can reach up to 400 °C. In space, temperatures can be even higher – the surface of Venus is 460 °C – but in outer space is can be as low as −271 °C, so the electronics on board both space satellites and rovers has to operate over a very wide temperature range. To ensure optimal system performance, it is crucial that sensors, communications systems and control circuitry function effectively under these extreme temperatures.

Note that not all extreme conditions come from external factors; high power can stress microelectronics and their surroundings. Due to this, it is essential to develop new devices that are capable of managing high voltages, high currents and high powers, as well as advanced insulating materials and low-loss passive components. This approach is necessary to ensure the reliability and functionality of electronic systems operating in challenging environments.

Computing and material requirements

The use of computing chips in extreme environments is characterised by a greater variety of applications and heavy workloads. Specifically, in applications such as space exploration, the geothermal and petrochemical industries, as well as quantum computing, there is often the requirement for computers to be rugged, light, compact, and energy efficient. In addition, these computers must be capable of withstanding extreme conditions, such as low and high temperatures and strong radiation (see Table 1), ideally without having to draw on a heavy and bulky payload for temperature management and radiation shielding.

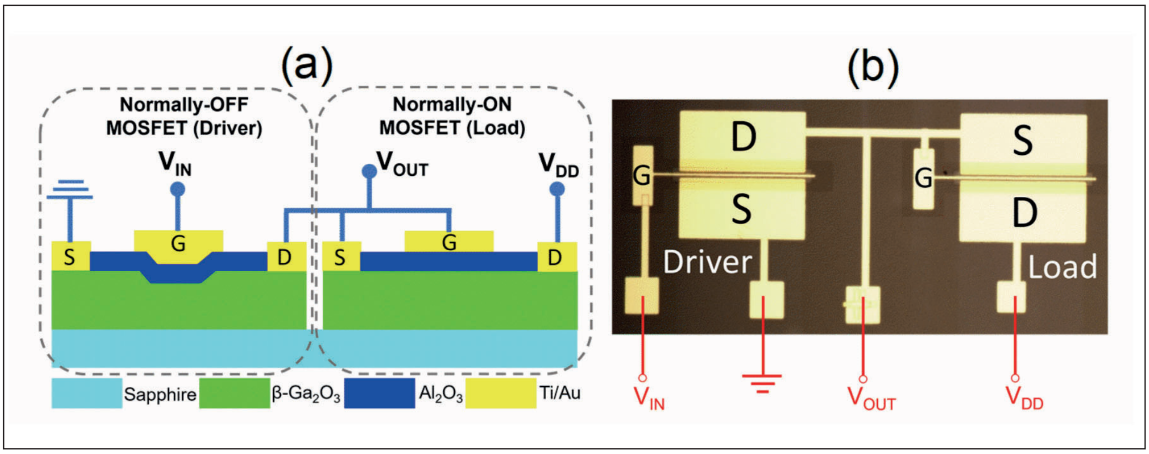
For any electronic IC chip, the basic underlying technology is based on semiconductor materials capable of offering insulating and conducting properties, when subjected to an external electrical or optical ‘bias’. To build robust computing chips, ideally these materials can endure extreme environments. That means that as well as resisting melting, these materials are capable of withstanding potential failures caused by thermal or mechanical stress. In addition, they need to remain stable, avoiding degradation due to changes in their structure caused by heat, or surface damage resulting from the likes of diffusion, oxidation, vaporisation or ablation.

A number of elemental and compound semiconductor materials have been explored over the years, with efforts motivated by understanding their properties and determining their capability for producing various devices. Amongst them, silicon serves as the foundational source for all electronic innovations that exist in our daily lives. It is abundant and scalable, with a high mobility for electrons and holes, but due its narrow bandgap, its usage is constrained in harsh environmental conditions.

Two materials with a wider bandgap, GaN and SiC, provide a better performance, in terms of high temperature capability and radiation tolerance. However, both offer limited performance at low temperatures, with carriers in both bulk materials

Properties	Si	GaN (bulk/2DEG)	4H-SiC	Ga_2O_3
Bandgap (eV)	1.12	3.3	3.4	4.8
High Temperature	No	Yes	Yes	Yes
Low Temperature	No	No/Yes	No	Yes
Radiation resistivity	Poor	Good	Good	Excellent
Native oxide	Yes	No	No	Yes
Field Effect Mobility ($cm^2 V^{-1} s^{-1}$)	450	133/500	<40	<100

Table 2. Physical properties of silicon, GaN, 4H-SiC, and Ga_2O_3 for applications in extreme environments.

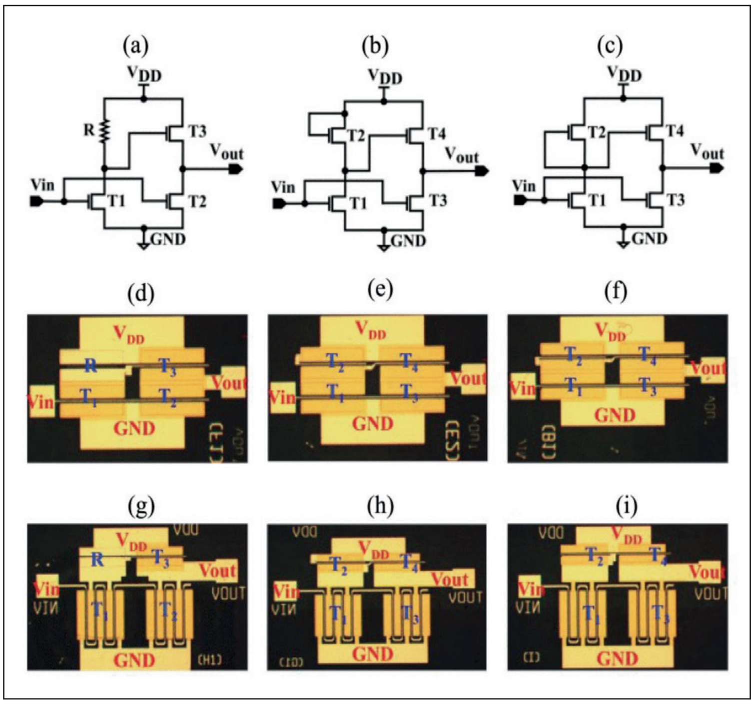


➤ Figure 1. A Ga_2O_3 DCFL inverter (a) cross-sectional diagram. (b) An optical microscope image of the DCFL circuit.

freezing out below 40K. (Note, though, that GaN transistors based on a polarisation-induced carrier gas are not sensitive to low temperature.) Additionally, GaN and SiC lack native oxides, potentially resulting in less stable IC operation in extreme environments. For instance, a single event burnout due to heavy ion damage is a big issue for SiC MOSFETs.

A far more attractive candidate may be Ga_2O_3. As well as being blessed with a larger bandgap than GaN and SiC, it offers well-balanced properties, and there are no significant drawbacks that might hinder its performance (see Table 2, which highlights the physical properties of silicon, GaN, 4H-SiC, and Ga_2O_3 for applications in extreme environments).

Ga_2O_3 is a great allrounder, offering superior properties in all extreme environmental conditions, including low and high temperatures and high levels of radiation, while maintaining a decent mobility. Another important attribute of Ga_2O_3 is that native bulk substrates can be produced at a lower cost than GaN and SiC substrates, crucial for low cost and scalability of ICs, thanks to the opportunity to use low-cost melt-grown techniques. Further improvement of heteroepitaxial Ga_2O_3 could further lower the cost significantly.



➤ Figure 2. Ga_2O_3 dual-stage inverter circuits. (a) pseudo-R, (b) pseudo-E, and (c) pseudo-D schematics. Fabricated devices with transconductance ratio, KR, of 1. (d) pseudo-R. (e) pseudo-E. (f) pseudo-D. Fabricated devices with a KR of 28.8. (g) pseudo-R. (h) pseudo-E. (i) pseudo-D.

Blessed with an ultra-wide bandgap and extensive electron doping capabilities, Ga_2O_3 provides a promising solution for handling high powers – high-voltage and large-current electronics, as well as extreme temperature applications. During the last decade or so, Ga_2O_3-based transistors and Schottky diodes have been extensively studied, yielding impressive results that include a voltage handling capacity of around 8 kV and operational temperatures of up to 500 °C.

However, to operate in extreme environmental conditions, there is a need for electronic systems, which process and store information, to incorporate vital electronic components – specifically, logic circuits and flash memory built on Ga_2O_3.

Our team from King Abdullah University of Science and Technology (KAUST) is embarking on this challenge, and has already taken strides towards developing an advanced computing and memory chip that operates reliably in extreme temperatures. Breaking new ground, we have demonstrated the functionality of logic and memory components using heteroepitaxial β-Ga_2O_3, grown on a sapphire substrate. This triumph takes us closer to realising highly dependable, efficient, and compact computing systems designed to withstand extreme conditions.

Initial investigations

Our research has focused on Ga_2O_3 logic inverter circuits based direct coupled FET logic (DCFL), pseudo-CMOS, and Ga_2O_3/NiO ambipolar CMOS ICs. We have also looked at Ga_2O_3 flash memory, designed with a floating gate configuration. Both our Ga_2O_3 logic circuits and our flash memory are realised on heteroepitaxial grown β-Ga_2O_3 on sapphire and silicon substrates.

The Ga_2O_3 DCFL inverter is realised through monolithic integration of top-gated normally-on (depletion-mode) and normally-off (enhancement-mode) Ga_2O_3 transistors. These devices, formed on sapphire substrates, work as a load and driver respectively. To realise normally-off operation, we employ a recess etched gate technique (see Figure 1(a) and (b) for a cross-sectional diagram and an optical microscopy image of Ga_2O_3 DCFL inverter circuits). This DCFL logic inverter shows successful operation, with a voltage gain of around 2.5 V.

Measurements show that our DCFL inverters, operating as single-stage inverters, exhibit elevated power dissipation. This arises from incomplete turn-off of the load thin-film transistor (TFT), when the driver TFT is active.

One way to address this incomplete turn-off is to introduce pseudo-CMOS topologies – they minimise power loss by providing a more effective turn-off of both the load TFT during pull-down and of the driver TFT during pull-up. We fabricate these Ga_2O_3 pseudo-CMOS inverters in three configurations: pseudo-R, pseudo-E, and pseudo-D. The circuits use two different transconductance ratios, either 1 or 28.8 (see Figure 2). Note that the optimised pseudo-CMOS circuit exhibits the least peak power consumption, just 0.2 nW, and the maximum gain of 8 at a positive supply voltage, V_{DD}, of 3 V.

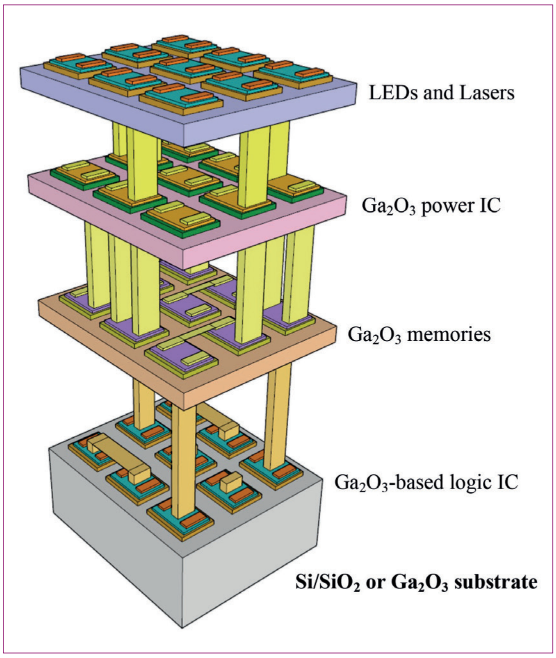


Figure 5. Future vision: 3D heterogeneous integration of various devices. Stacking involves combining various components made from different semiconductor materials, with the goal of creating a highly robust 3D heterogeneously integrated system for harsh environment applications.

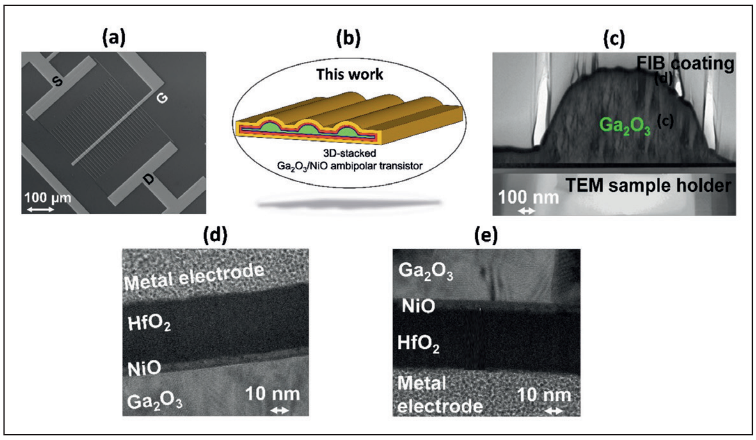


Figure 3. (a) Scanning electron microscopy and (b) diagram of 3D-stacked Ga_2O_3/NiO heterojunction ambipolar transistors. Here, Ga_2O_3 and NiO are the *n*- and *p*-channels respectively. (c) Cross-sectional transmission electron microscopy image of the gate region with zoom-in (d) bottom and (e) top areas of a dome-shaped fin.

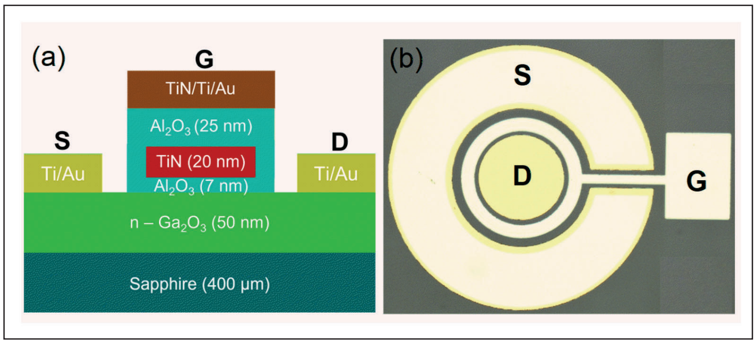


Figure 4. Floating gate Ga_2O_3 flash memory (a) cross-section schematic and (b) top microscope image.

To obtain a CMOS configuration, we have explored the seamless integration of Ga_2O_3 NMOS with *p*-type semiconductor-based PMOS. Using *p*-NiO, we fabricated the first Ga_2O_3-based ambipolar CMOS logic circuits with NiO and Ga_2O_3 as a *p*- and *n*-channels (see Figure 3). Notably, both the *n*- and p-channels offer excellent stability at temperatures of up to 300 °C.

Every electronic circuit requires a logic circuit to process the data, as well as memory to store it. After realising our Ga_2O_3 logic circuit, we fabricated a heteroepitaxial Ga_2O_3 non-volatile flash memory using a conventional floating gate configuration.

Notably the Ga_2O_3/NiO ambipolar transistors comprise advanced gate-all-around and vertical-stacking architectures, showing that Ga_2O_3 ICs could benefit from processing technologies being established in latest silicon fabs.

Every electronic circuit requires a logic circuit to process the data, as well as memory to store it. After realising our Ga_2O_3 logic circuit, we fabricated a heteroepitaxial Ga_2O_3 non-volatile flash memory using a conventional floating gate configuration. This involves using TiN for the floating gate, and Al_2O_3 for tunnelling and blocking oxides (see Figure 4(a) for cross-sectional schematics, and Figure 4(b) for the optical image of the fabricated device).

Our results are encouraging. The flash memory offers a large memory window of more than 4 V, and data retention is in excess of 5000 s. The programming operation of the memory provides a positive threshold voltage of 0.3 V, creating a new pathway for producing normally-off transistors for low static, low-loss electronic circuits.

While Ga_2O_3 has great potential on its own, there is also the possibility for 3D integration with other material systems. It is possible for Ga_2O_3 logic ICs to be vertically stacked with SiC MOSFETs, Ga_2O_3 memories, GaN RF components and optoelectronic devices (see Figure 5). This shows that depending on application and environmental conditions, Ga_2O_3 may be used on its own to produce ICs, or combined with other material systems.

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COMPANY NAME/LOCATION:

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Im Nassen 3 | 53578 Windhagen | Germany

BOARD OF MANAGEMENT:

Torsten Kornmeyer | Takeshi Kawazoe

HISTORY:

In business since 1968 - Nippon Kornmeyer Carbon Group (NKCG) is a company jointly operated by the shareholders of Kornmeyer Carbon-Group (Germany) and Nippon Carbon Co. Ltd. (Japan), a Tokyo stock exchange listed carbon manufacturer.

1968: Foundation of KOGO mechanics by Winfried Kornmeyer, first own workshop with several CNC equipment; 1969: Jointly developed first graphite heated vacuum furnace of its kind with Schmetz, Menden, one of the leading manufacturer of vacuum furnaces; 1982: First mover with direct heated charging rack (Carbon Composites) for the vacuum brazing of coolers in the automotive production; 2012: Start of new purification and coating center in Windhagen with several new furnaces (CVI & CVD processes); 2016: Nippon Carbon Co., Ltd. Japan acquired shares of the company which then was renamed into "Nippon Kornmeyer Carbon Group".

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Nippon Carbon Co., Ltd. The raw material and R&D base: Nippon Carbon, since its establishment in 1915, has developed a variety of products featuring carbon's prominent attributes. The main manufacturing and sales domains are carbon fiber products used for aerospace technology and general industry, High Purity Treatment Graphite used when producing crystalline silicon, Anode Materials for Lithium Ion Battery, Silicon Carbide Continuous Fibers mainly provided for the aerospace industry, impervious graphite and chemicals used for chemical industrial devices and equipment such as heat exchangers, flexible graphite for the automobile industry, and other carbon products.

NUMBER OF STAFF:

800 (group)

PRODUCT RANGE:

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CERTIFICATION:

DIN EN ISO 9001:2015

COMPETITIVE ADVANTAGES:

NKCG is proactively researching and exploring new applications of existing processes and promoting new technologies. The access to the R&D center of Nippon Carbon Group in Japan supports our local engineering team to act fully integrated in the application and product improvement process. The Nippon Carbon Group manufactures a complete range of carbon specialties, NKCG supports its customers with engineering, machining and coating services.

SERVICE POTENTIALS:

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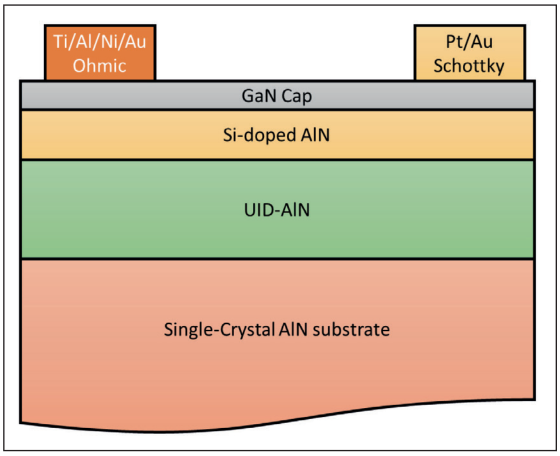
Advancing the AlN Schottky barrier diode

Formed on native substrates, AlN Schottky barrier diodes offer a 3 kV blocking voltage and excellent performance at elevated temperatures

ENGINEERS at Arizona State University are claiming to have produced the first AlN Schottky barrier diodes on single-crystal AlN substrates that can block 3 kV. These devices are said to offer excellent high-temperature performance and rectifying behaviours.

The team's success is a noteworthy breakthrough. While AlN has much promise, thanks to its high critical field and its large Baliga's figure of merit, the development of this class of power device is still in its infancy, due to challenges in material growth, contacts, doping, and fabrication.

"[Our] results show the potential of AlN as an ultra-wide bandgap semiconductor and represent a big step towards the development of multi-kV AlN high-voltage and high-power devices," argues team spokesman Houqiang Fu.



➤ AlN Schottky barrier diodes with a 3 kV blocking voltage are produced via MOCVD on native substrates.

He and his co-workers recent triumph builds on earlier work involving the production of AlN-on-sapphire diodes capable of blocking 1 kV. Switching to a native substrate has trimmed the defect density, which holds back device performance, including the blocking voltage.

Production of the 3 kV Schottky barrier diodes began by loading bulk AlN substrates, produced by physical vapour transport, into an MOCVD reactor. On this foundation the team deposited a 1 μm-thick unintentionally doped resistive buffer, followed by a 200 nm thick AlN layer doped with silicon at a concentration of 1×10^{19} cm^{-3}, and a 2 nm-thick unintentionally doped GaN cap.

To assess the crystal quality of the epilayers, the team considered the thickness of the peaks obtained by high-resolution X-ray diffraction. This suggest a dislocation density of 10^4 - 10^5 cm^{-2} – that's three orders of magnitude below that for AlN grown on sapphire.

Following chemical cleaning of the epiwafers, the engineers fabricated Schottky barrier diodes using a conventional photolithography and lift-off process. They produced a portfolio of devices, with the distance between the ohmic and Schottky contacts varying from 50 μm to 350 μm. None of the devices employed field plates, passivation, or edge termination structures.

Electrical measurements revealed on-off ratios of 10^5 - 10^6, and a turn-on voltage of around 2.5 V.

The team have also studied the ideality factor. A perfect device would have a value of 1, with values closer to this indicating a higher quality of the diode, due to fewer defects causing trap states at the metal-semiconductor interface. As the distance between the ohmic and Schottky contacts increased, the ideality increased from 4.29 to 7.52. This led the team to deduce that current transport is likely to be influenced by surface states and/or the resistance of the AlN epilayers due to a relatively low carrier concentration.

Increasing the temperature of the diodes with the best ideality factor from 298K to 623K revealed good temperature stability. With increasing temperature, the on-off ratio increased from 10^6 to 10^8, the Schottky barrier height went up from 0.89 eV to 1.85 eV, and the ideality factor fell from 4.29 to 1.95.

Reverse-bias measurements reveal that regardless of the distance between the ohmic and Schottky contacts, the diodes are capable of blocking 3 kV, the limit of the team's apparatus.

One of the next goals for Fu and co-workers is to improve the reverse and forward electrical performance of their high-voltage AlN power diodes.

For reverse performance, efforts will focus on incorporating edge termination techniques, such as field plates, and introducing surface passivation. It's hoped that this will trim the reverse leakage current and boost the breakdown voltages to 10 kV.

"For the forward performance, we will continue to improve the ohmic and Schottky contacts, to enhance forward current conduction and reduce on-resistance through surface treatment and optimised thermal annealing," adds Fu.

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PCSELs produce green emission

By adjusting the dimensions of a photonic crystal, green emission is arbitrarily tuned over a 15 nm range

A PARTNERSHIP between Nichia and Kyoto University is claiming to have produced the first photonic-crystal surface-emitting laser (PCSEL) that emits in the green.

Spokesman for this team from Japan, Natsuo Taguchi, who holds positions at both Nichia and Kyoto University, says that green PCSELs have high potential, thanks to their tremendous beam quality. This class of laser produces single-mode operation in both the vertical and lateral direction, and combines a narrow divergence angle with a beam quality that is close to that of an ideal Gaussian beam.

Green-emitting PCSELs could replace solid-state lasers, according to Taguchi, winning deployment in applications that including imaging for displays and bioscience.

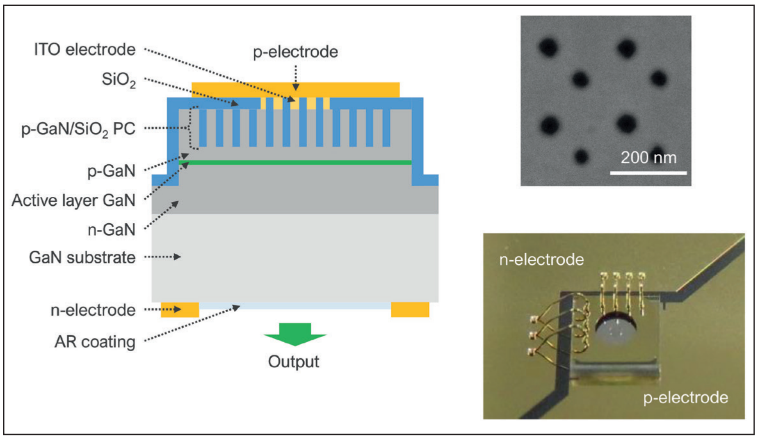
Another merit of the PCSEL is that it's possible to engineer the emission wavelength with great precision through careful selection of the dimensions of the photonic structure.

"The lasing wavelength can be arbitrarily tuned," says Taguchi, "which enables us to create arbitrary colours through colour mixing." As well as providing a valuable attribute for display applications, this tunability allows emission to be tailored to the peak absorption efficiency of fluorescent dyes.

The green PCSEL pioneered by Taguchi and his colleagues features a double-lattice photonic crystal, incorporated to improve control over interference produced by the laser.

To form the photonic crystal structure, the engineers deposit a layer of indium tin oxide (ITO) above the GaN stack – a heterostructure consisting of an *n*-type layer, and active region and a *p*-type layer – and then use electron-beam lithography and reactive-ion etching to define device dimensions. By adopting this approach, it is possible to undertake optical characterisation of the epistructure via photoluminescence before finalising the details of the photonic crystal lattice.

Holes created by etching are filled with SiO_2 using a plasma CVD process. This step protects the photonic crystal's side walls from conducting particles, which threaten to cause current leakage and hamper stable operation of the PCSEL. Filling holes with SiO_2 also increases the effective refractive index of the photonic crystal layer, leading to a shift in the distribution of the fundamental mode to this layer, and ultimately an enhanced coupling between the guided light and the photonic crystal.



➤ Green-emitting PCSELs with a double lattice produce an output of up to 50 mW

Note, though, that there is also a downside associated with the addition of SiO_2: a reduction in the refractive index contrast between the *p*-GaN layer and the photonic crystal. However, this can be offset by enlarging the fill factor of the photonic crystal.

After filling the holes with SiO_2, the team removed the ITO film, apart from a 300 μm-diameter central circular area that is used for an electrode, and then exposed the *n*-GaN layer, before adding electrodes and an anti-reflection coating (see Figure for the design of the PCSEL).

Driven with 500 ns pulses with a repetition frequency of 1 kHz, the team's PCSEL produced a steep increase in power output at a current density of 3.89 kA cm^{-2}, and delivered a maximum output of around 50 mW at a drive current of about 5 A. The corresponding wall-plug efficiency is around just 0.1 percent.

By adjusting the dimensions of the crystal lattice, the team demonstrated that it can arbitrarily tune the emission wavelength from 505.7 nm to 520.5 nm.

Taguchi says that one of the next goals is to increase the wall-plug efficiency of their PCSELs. This will be realised by optimising the design and the fabrication of the photonic crystals, to increase the intensity of in-plane coupling of the photonic crystal layer and vertical radiation. "Simultaneously, the epitaxial layer will be optimised to reduce the lasing threshold."

REFERENCE

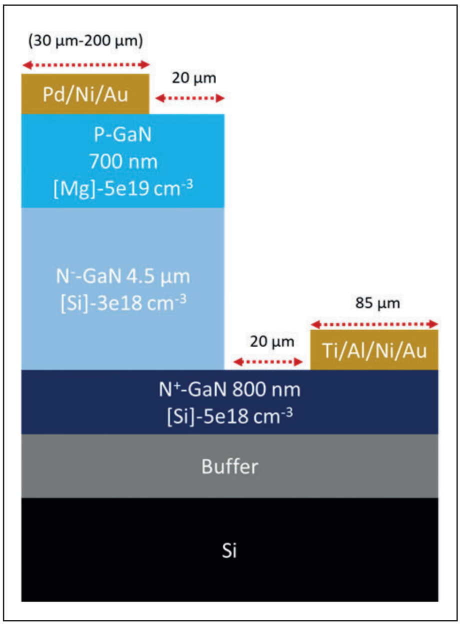
➤ N. Taguchi *et al.* Appl. Phys. Express **17** 012002 (2024)

Realising avalanche in GaN-on-silicon diodes

Thanks to a low dislocation density in the epilayers, GaN-on-silicon diodes with a blocking capability above 800 V are capable of avalanche behaviour

A COLLABORATION between engineers at the University of Lille and Siltronic is claiming to have broken new ground by producing the first GaN-on-silicon diodes with avalanche capability. The team's vertical devices, offering avalanche capability, combine the high performance of a wide bandgap semiconductor with the low cost of large diameter silicon substrates.

Benefits of avalanche capability include providing a safety margin at the system level, and by operating safely at close to breakdown, an opportunity to use relatively small devices.



➤ Avalanche capability is realised with pseudo-vertical GaN-on-silicon diodes.

"Lateral GaN HEMTs cannot offer avalanche due to the peak electric field at the gate vicinity," explains team spokesman Youssef Hamdaoui from the University of Lille. He adds that one consequence of this is that the safe operating voltage of the lateral devices is typically much lower than the hard breakdown voltage. "Such a voltage derating results in large gate-drain distances and therefore large device dimensions."

Prior to this recent work of Hamdaoui and co-workers, GaN devices with avalanche capability had been limited to: native substrates, which are expensive; and sapphire substrates, which are held back by low thermal dissipation.

Hamdaoui believes that the team's triumph will raise a few eyebrows within the wide bandgap power electronics community, because the high dislocation densities associated with GaN growth on silicon were thought to prevent avalanche capability.

Growth of the team's epiwafers took place at Siltronic, using an industrial MOCVD reactor capable of accommodating 150 mm wafers.

"The quality of material was enhanced by a specific engineered buffer that helps to filter the dislocation density," remarks Hamdaoui, who adds that the specific details of this approach will be published later this year.

Fabrication of the diodes began by loading a 150 mm silicon substrate in an MOCVD reactor and depositing a proprietary buffer stack, followed by an 800 nm-thick n^+ GaN layer, a 4.5 µm-thick *n*-type GaN drift layer, and a 700 nm-thick *p*-type GaN layer.

Plasma-enhanced CVD of a SiO_2 layer that is patterned by reactive-ion etching created a hard mask for mesa etching, undertaken with an inductively coupled plasma process. The engineers etched deep into the epistructure, reaching the n^+ GaN layer, and creating sidewalls with an angle of 75° that spread the electric field at the edge of the device over a distance that is larger than the drift region thickness. By taking this approach, it is possible to manage the electric field around the anode electrode.

To complete the fabrication of the diodes, Hamdaoui and co-workers added *n*-type and *p*-type contacts (see figure for more device details).

Measurements of the forward characteristics of diodes with a 30 µm anode diameter and a 70 µm top mesa diameter revealed a threshold voltage of 4.5 V and a differential on-state resistance below 0.35 mΩ cm^2. According to the engineers, a lower threshold voltage can be realised by optimising the *p*-type ohmic contact.

Investigations of reverse characteristics revealed a blocking capability above 800 V, corresponding to an estimated critical peak electric field of 2.3 MV/cm.

Studying reverse characteristics of current density as a function of voltage at different temperatures enabled the team to determine that under a high reverse bias, carriers flow through a specific path with high energy, enabling the accumulation of additional charge carriers. This is said to lead to impact ionisation, which enables avalanche capability. The team also observed an increase in breakdown voltage with increasing temperature. This is claimed to be a strong indication of avalanche capability.

Hamdaoui and co-workers are planning to continue to optimise their vertical GaN-on silicon devices. The short-term goal is to produce 1200 V class diodes with avalanche breakdown capability. Looking further ahead, they are aiming to develop vertical transistors, such as trench MOSFETs, based on their optimised material system.

REFERENCE

➤ Y. Hamdaoui *et al*. Appl. Phys. Express **17** 016503 (2024)

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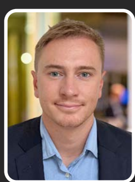

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