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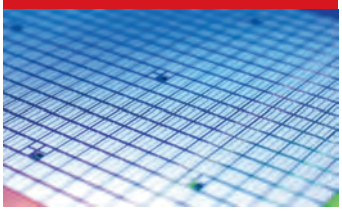
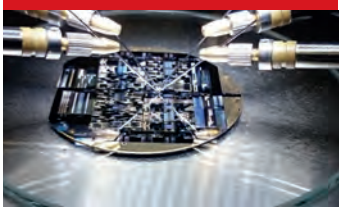
Hybrid growth promises better laser diodes

Comb lasers advance computing power

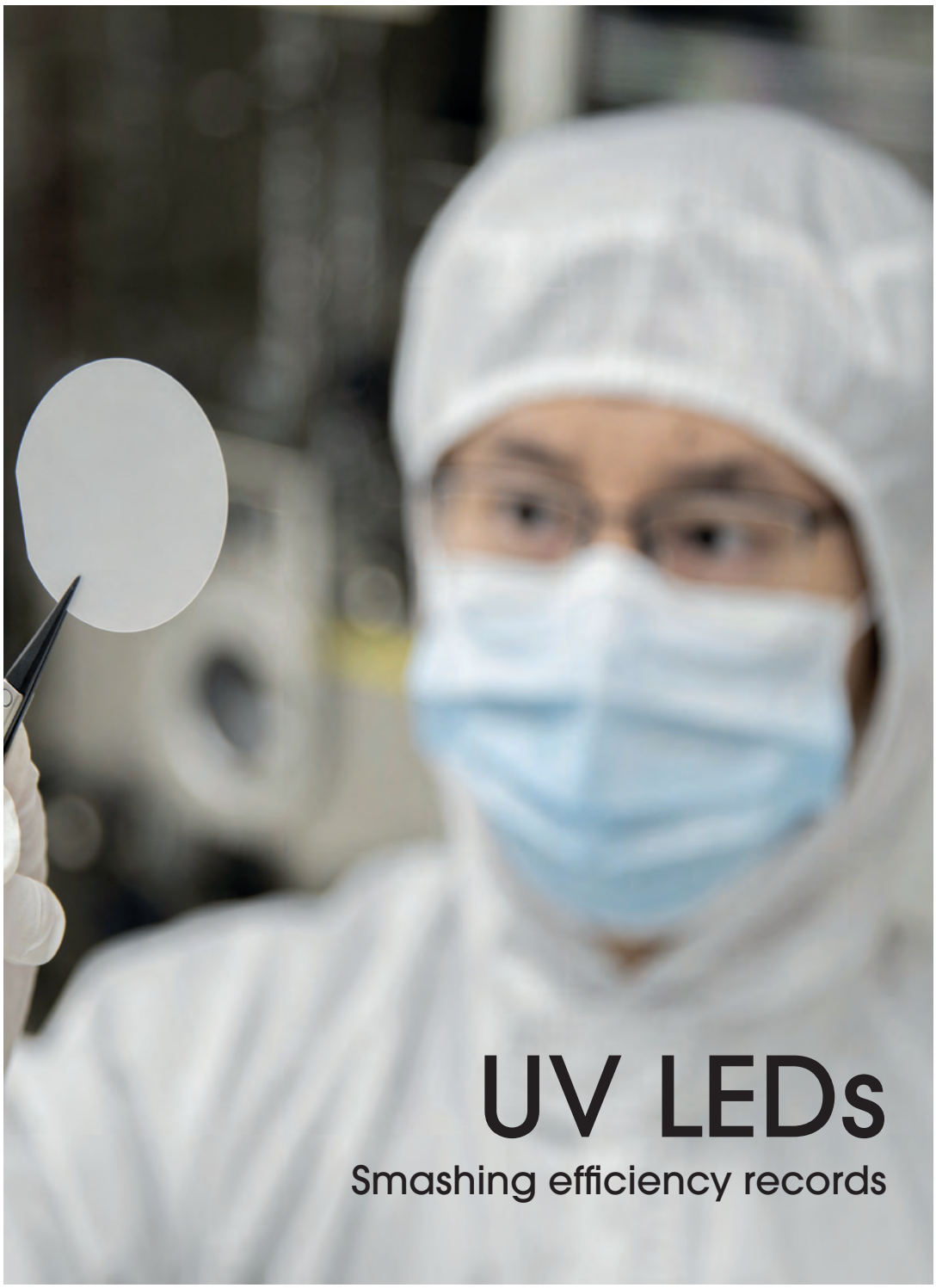
Finding a better face for the SiC MOSFET



PICs: Plug-and-play characterization



RF GaN: Big revenues, bright future?



UV LEDs

Smashing efficiency records

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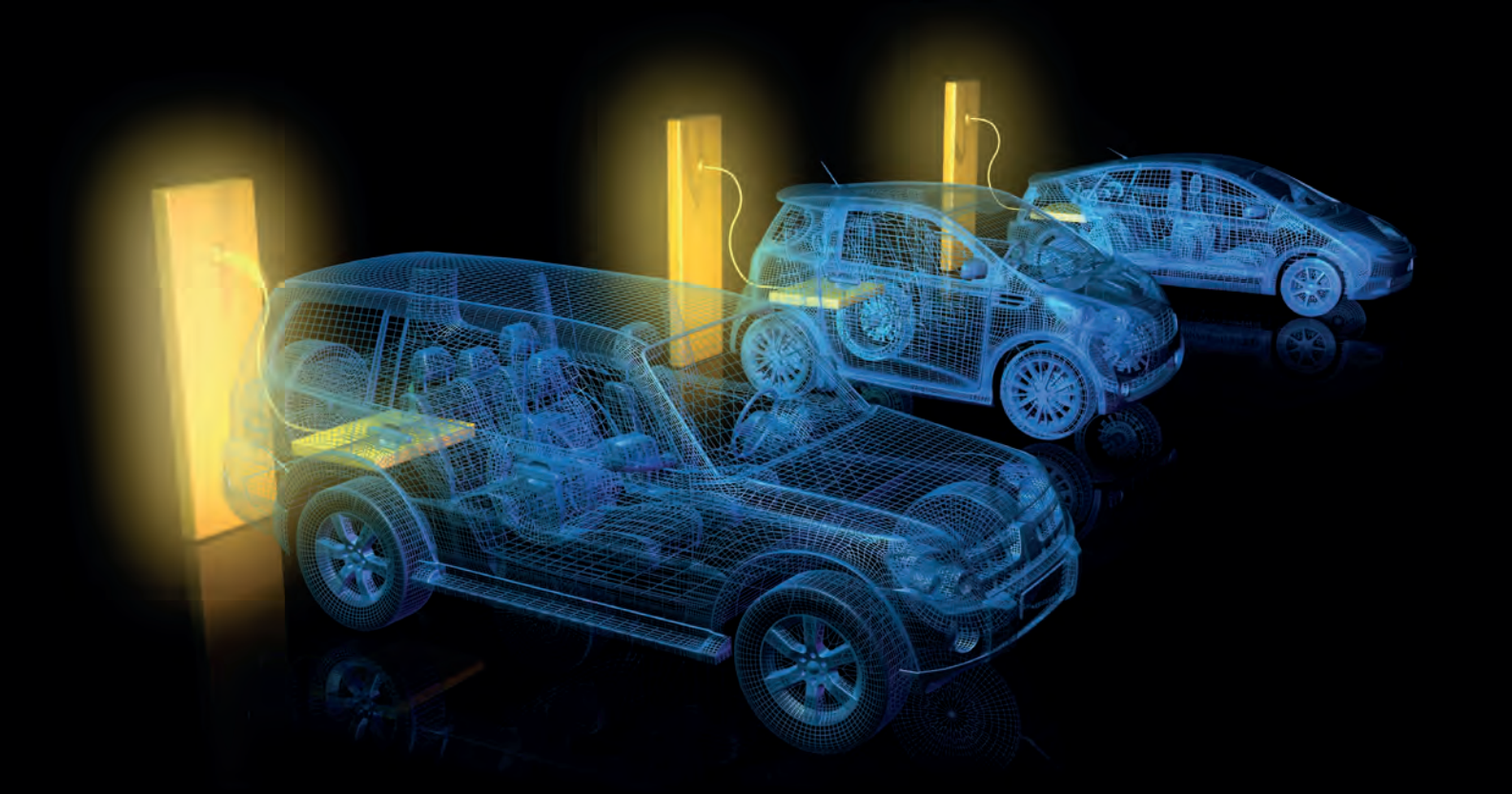

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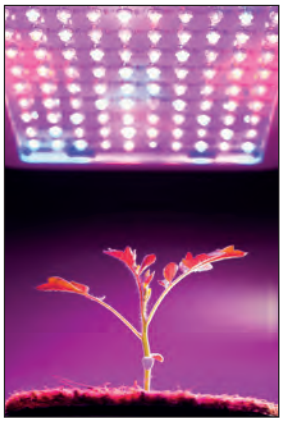
Viewpoint

By Dr Richard Stevenson, Editor

Breakthroughs in the deep UV

LEDs that emit in the deep UV are notorious for feeble output powers and incredibly short lifetimes. Both get worse as the wavelength decreases.

However, improvements are possible. Recently, a partnership between researchers at Asahi Kasei Corporation and Crystal IS has unveiled a suite of devices that can operate for over 3000 hours and deliver record efficiencies between 230 nm and 237 nm (see p. 66) ; and a collaboration between scientists at the University of Science and Technology of China and Huazhong University of Science and Technology has smashed the record for wall-plug efficiency for 280 nm LEDs (see p. 20).



Given that deep UV LEDs have been in development for decades, you would expect that all the latest improvements came through esoteric refinements. But the reality is more complex, involving excelling in the basics, as well as turning to innovation.

It is well known that oxygen is to be avoided in UV LEDs, as it leads to energy-sapping point defects that can move through the device. The team from Kasei Corporation and Crystal IS have driven this down by investing in a more modern MOCVD reactor, optimising the growth conditions and turning to sources with greater purity. All these moves are thought to have lengthened the lifetime of their devices.

After thinning their UV-emitting chips and mounting them in a transparent flip-chip package, the team are getting output powers of just over a milliwatt at 100 mA drive currents. That's an improvement, but external quantum efficiencies and wall-plug efficiencies are still well below one percent.

Why are they so low? It's primarily because as emission wavelengths head towards the deep UV, extraction efficiencies plummet, with much of the light failing to exit the chip. The team is now proposing a novel solution to address this: extract the emission from the edge of the chip.

For the team from China, a radical architecture is behind the record-breaking wall-plug efficiencies – they are a whopping 20 percent for their 280 nm emitters. In their design, a conventional LED is monolithically united with a photoelectric converter that multiplies holes by impact ionisation, before these carrier are re-injected into the active region.

While this team's success is driven by a trail-blazing architecture, they have also worked hard to address many of the well-known weaknesses in the UV LED. They grow device layers on a patterned sapphire with a silica array, as this reduces dislocations in the materials an aids light extraction; and they turn to mis-cut substrates to reduce the internal electric fields that pull apart electrons and holes. So they get the basics right, and use this as a strong foundation for their innovation.

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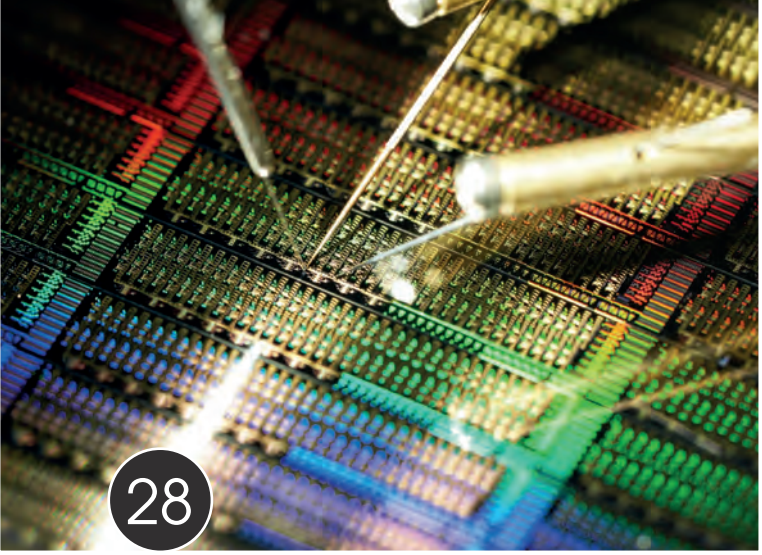

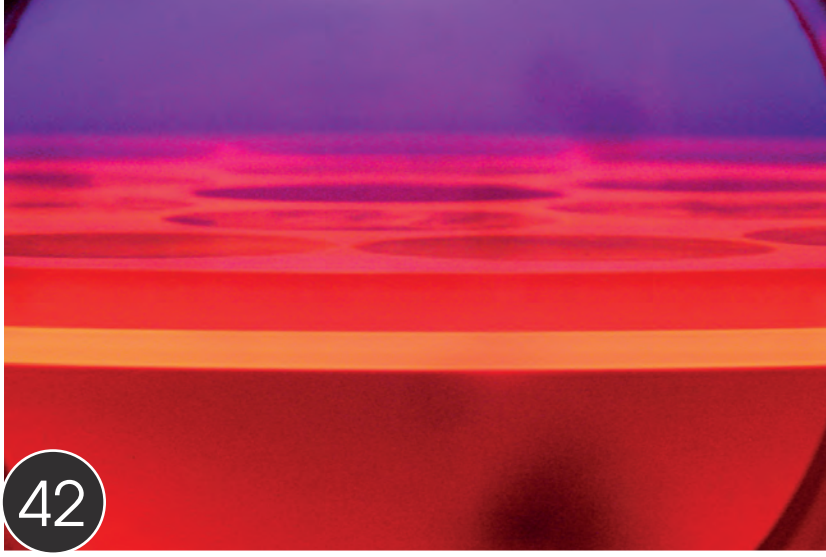

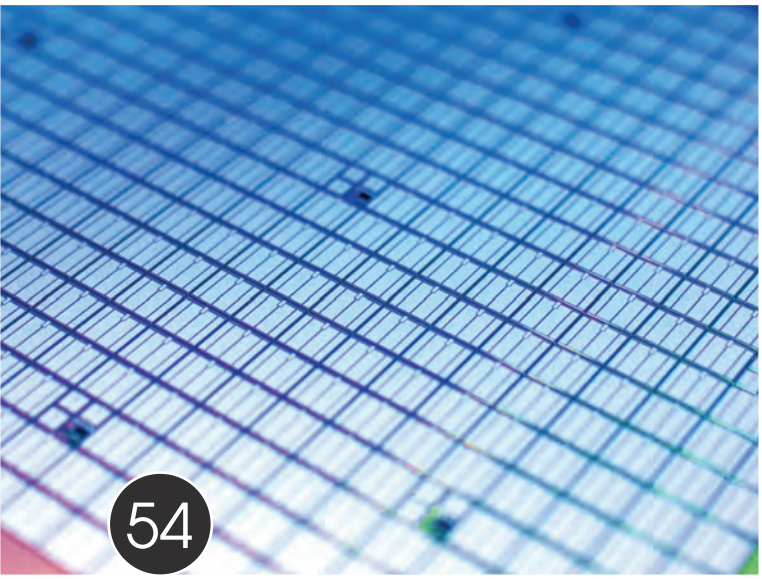

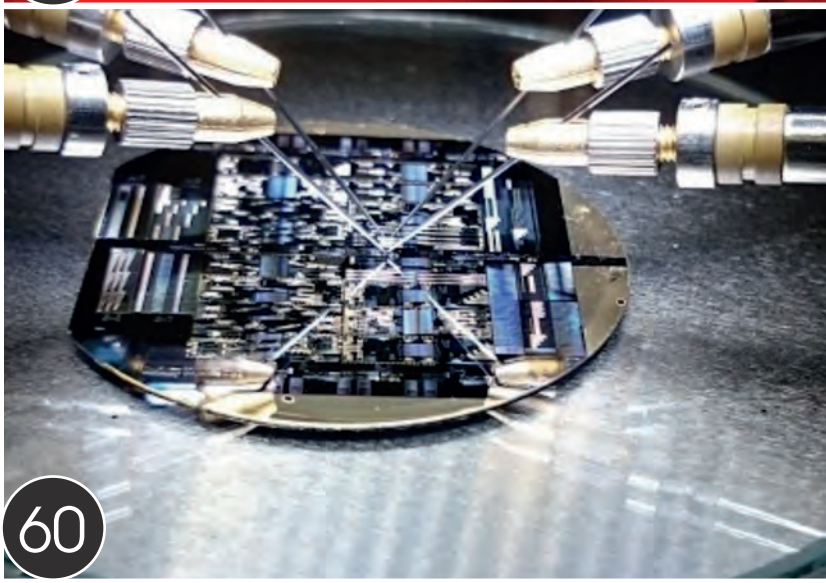

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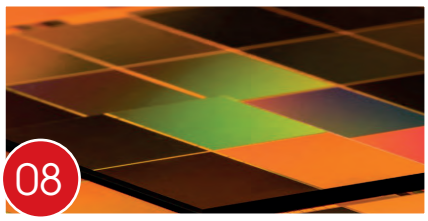

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Transphorm and Magneti Marelli sign partnership

ITALIAN AUTOMOTIVE supplier Magneti Marelli and US GaN company Transphorm have signed a partnership agreement for developing power converters, onboard chargers and inverters for electric and hybrid vehicles.

Working alongside Transphorm engineers, Marelli engineers will be able to use their experience to advise on product development relevant to its ongoing investment in the development of e-powertrain solutions for electric vehicles and also for motorsport applications. For such joint development and co-working of engineers, Transphorm will exclusively cooperate with Marelli for two years, to enable the development of new technologies for electric vehicles.

Joachim Fetzer, CEO, electric powertrain, Marelli, said: "Electric Vehicle power conversion is fundamentally important to the future of electric vehicles and investment in technologies like this are critical to ensure the very highest performance of electric vehicles at a lower cost. We are delighted to partner with Transphorm, who are true leaders in the market.

Fetzer added: "This partnership allows us to work with the Transphorm team to shape and improve products that will ultimately ensure improved performance, efficiency of power electronics and ultimately lower the cost of electric vehicles."

Primit Parikh, co-founder and COO, Transphorm, said: "Automotive and EVs represent one of the largest opportunities for GaN in power conversion and our partnership with a global leader like Marelli is a strong testament to the quality, reliability, manufacturing and overall product performance of our GaN solutions.The long-term innovative system level vision of the Marelli Electric Powertrain team will be extremely valuable in furthering GaN in the electric vehicle."

Imec and CST Global integrate InP light sources

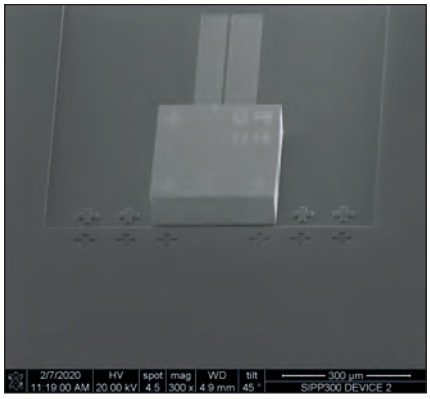
BELGIAN research hub Imec and CST Global, a UK-based designer and manufacturer of III-V compound semiconductors for photonics products, announce the successful integration of InP distributed feedback (DFB) lasers from CST Global's InP100 platform into Imec's integrated silicon photonics platform.

Interfaces for hybrid integration of InP DFB lasers and reflective semiconductor optical amplifiers (RSOA) will become available as part of Imec's silicon photonics prototyping services in the first half of 2021, following further optimisation and qualification work in 2020. This joint Imec-CST Global technology offering is expected to boost the adoption of silicon photonics in cost-sensitive applications, including optical interconnects, sensing, computing and beyond.

Silicon photonics technology has made great progress over the past decades and is used extensively in a variety of applications – from fiber-optic communications to sensing. Technology platforms have evolved into mature vehicles and are available to industry and academia for prototyping, low-volume and higher-volume manufacturing. But a widely available, cost-effective solution to integrate light sources in silicon photonic chips has been missing, hampering the adoption of silicon photonics in cost-sensitive markets. As silicon does not emit light efficiently, light sources made of III-V semiconductors are typically implemented as separately packaged components. Such external light sources typically suffer from higher coupling loss; a large physical form factor; and a substantial packaging cost.

Imec has recently joined forces with CST Global to extend Imec's silicon photonics technology portfolio with passively assembled, edge-emitting, InP DFB lasers and InP RSOAs. This collaboration, which started in 2019, has now resulted in the first successful assemblies of C-band (1530-1565 nm) InP DFB lasers onto Imec's platform. The InP lasers were 'flip-chip' integrated onto the silicon photonic circuits through a die-to-die bonding process, aligning efficiently and coupling more than 5 mW into the SiN waveguides on the chip.

Joris Van Campenhout, program director optical I/O at Imec: "We are excited to work with CST Global to extend Imec's silicon photonics portfolio with hybrid integrated InP light sources. Our first passive laser assemblies have demonstrated excellent initial results."



"Throughout 2020, we will further optimise the precision and throughput of the laser assembly process; extend the functionality to include RSOA integration at 1310/1550 nm wavelengths; and perform reliability qualification. We expect that the availability of these hybrid, integrated light sources will boost industrial uptake of silicon photonics devices in a variety of cost-sensitive markets. Early access through Imec's iSiPP200 prototyping services is anticipated by the first half of 2021."

Antonio Samarelli, integration manager at CST Global: "We are extremely pleased to be working with Imec on this project. The hybrid integration of InP light sources (DFBs and RSOAs), designed and fabricated on CST's InP100 manufacturing platform, combined with the iSiPP platform allow the creation of powerful photonic integrated circuits for advanced components with improved performance and lower cost in the future."

CST Global will continue to work closely with Imec to extend the functionality and capabilities of the InP100 platform to meet the InP light source requirements of novel, advanced PICs for high volume commercial applications.

Nexperia partners with Ricardo on GaN-based EV inverter for electric vehicles

NEXPERIA, a maker of discretes, MOSFETs and GaN FET components and analogue and logic ICs, has announced a partnership with automotive engineering consulting company, Ricardo, to produce a technology demonstrator for an EV inverter based on GaN technology.

GaN is the preferred switch for these applications as GaN FETs lead to systems with greater efficiencies at lower costs with improved thermal performance and simpler switching topologies. In automotive terms this means that the vehicle has a greater range – the major concern for anyone looking to buy an electric vehicle. GaN is now on the brink of replacing silicon based IGBTs and SiC as the preferred technology for the traction inverters used in plug-in hybrids or full battery electric cars.

Nexperia announced a range of AEC-Q101-approved GaN devices last year, providing automotive designers with an ever-widening portfolio of proven, reliable devices in this high-efficiency technology, providing the power density required for electrification of the powertrain.

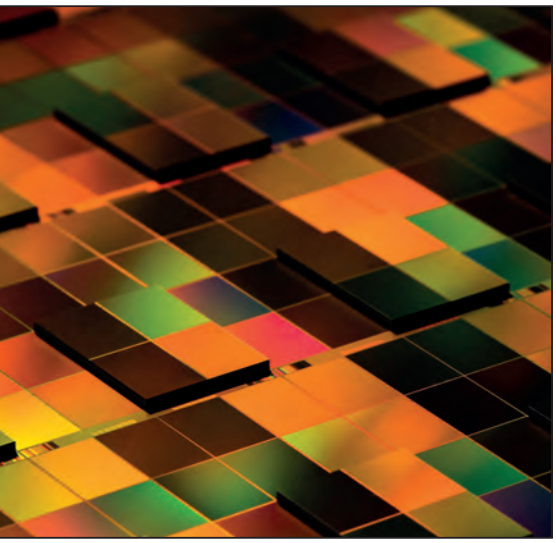
Ricardo is very well regarded in the automotive industry. This global engineering innovation company designs and consults on concepts within the automotive industry, including the manufacture of prototypes and demos, and boast collaborations with high-profile leading brands such as McLaren and Bugatti. Ricardo was the perfect partner for Nexperia for this project.

Michael LeGoff, general manager GaN, Nexperia: "By designing our GaN devices into an inverter and trialling them through Ricardo, we will be able to better understand how a vehicle can be driven safely and reliably. We are developing a real solution that I think a lot of automotive designers will be interested in having a look at and will find extremely advantageous."

Adrian Greaney, director technology & products, Ricardo: "Semiconductor technology is key to the efficiency of the inverter system and the role that it plays in the performance and efficiency of an electrified vehicle. By delivering significant benefits in terms of the switching speed and efficiency, gallium nitride is a real enabling technology. As well as leading to increased range, it allows us to reduce the package size and weight of the inverter, which provides greater powertrain design flexibility as well as contributing to vehicle mass reduction. There are also many associated benefits when we look at the design from a system level, and Ricardo is therefore pleased to be collaborating with Nexperia on GaN devices."

EVG opens heterogeneous integration centre

EV Group (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has established the Heterogeneous Integration Competence Centre, which is designed to assist customers in using EVG's process solutions and expertise to enable new and enhanced products and applications driven by advances in system integration and packaging.



The Heterogeneous Integration (HI) Competence Centre combines EVG's wafer bonding, thin-wafer handling, and lithography products and expertise, as well as pilot-line production facilities and services at its state-of-the-art cleanroom facilities at EVG's headquarters in Austria, supported by EVG's worldwide network of process technology teams.

"Heterogeneous integration fuels new packaging architectures and demands new manufacturing technologies to support greater system and design flexibility, as well as increased performance and lower system design costs," stated Markus Wimplinger, corporate technology development & IP director of EV Group.

"EVG's new HI Competence Centre provides an open access innovation incubator for our customers and partners across the microelectronics supply chain to collaborate while pooling our solutions and process technology resources to shorten development cycles and time to market for innovative devices and applications enabled by heterogeneous integration."

EVG has an extensive background in heterogeneous integration, providing solutions for this technology trend for more than 20 years.

Among these are: permanent wafer bonding – including direct fusion and hybrid bonding for 3D packaging and metal bonding – and die-to-wafer bonding with and without collective carriers for integration of III-V compound semiconductors and silicon as well as high-density 3D packaging; temporary bonding and debonding, including mechanical, slide-off/lift-off, and UV laser assisted; thin-wafer handling; and innovative lithography technologies, including mask aligners, coaters and developers, and maskless exposure/digital lithography. In the field of permanent bonding, EVG pioneered the patented SmartView wafer-to-wafer alignment system more than 20 years ago, and has refined this technology over the years to support breakthrough technology advances such as backside-illuminated CMOS image sensors and more recently the first demonstration of sub-100-nm wafer-to-wafer alignment overlay for hybrid bonding – enabling devices such as 3D backside-illuminated CMOS image sensors and memory-on-logic stacking. EVG developed the first temporary bonding systems for ultra-thin wafers as early as 2001, which are essential for 3D/stacked die packaging, as well as revolutionised low-temperature laser de-bonding for ultra-thin and stacked fan-out packages.

In lithography, EVG says that it cemented its position as a recognised technology leader with the delivery of the first UV moulding solutions for high-volume production of wafer-level optics more than a decade ago, and has since led the proliferation of nanoimprint lithography to high-volume manufacturing.

EVG continues to break speed and accuracy barriers in mask alignment lithography for advanced packaging and, more recently, unveiled the world's first highly scalable maskless exposure technology, which addresses emerging requirements in high-volume manufacturing back-end lithography.

Qorvo completes custom MMIC acquisition

QORVO has completed its acquisition of Custom MMIC, a supplier of high-performance GaAs and GaN monolithic microwave integrated circuits (MMICs) for defence, aerospace and commercial applications.

As part of Qorvo's Infrastructure and Defense Products business, the Custom MMIC team will continue to expand its millimetre-wave capabilities for products used in defence phased array and AESA radars, electronic warfare, satellite communications, wireless backhaul and microwave test equipment.

James Klein, president of Qorvo Infrastructure & Defense Products said, "Custom MMIC's best-in-class die and packaged components augment our power amplifiers to enable multi-chip modules for a broad range of defense, aerospace and commercial applications."

"We look forward to building on Custom MMIC's reputation as an outstanding strategic supplier to leading defense prime customers, as we expand our millimetre-wave capabilities and product offerings for defense and commercial markets, including 5G."

Chelmsford, Massachusetts-based Custom MMIC was founded in 2006 and has extensive experience developing MMICs at frequencies up to 70 GHz.

Custom MMIC adds small signal millimetre-wave expertise and a portfolio of more than 180 standard products including LNAs, mixers, attenuators, phase shifters and switches.

Custom MMIC president and CTO Paul Blount joins Qorvo as a director of engineering for Infrastructure and Defense Products.

SK Siltron acquires DuPont SiC wafer division

SK SILTRON, a maker of semiconductor wafers, has completed the acquisition of DuPont's SiC wafer unit. The acquisition was decided through a board meeting in September and closed on February 29.

The $450 million acquisition is to meet the demand from consumers and governments for sustainable energy and environmental solutions. SK Siltron will continue to invest in related fields even after the acquisition, which is expected to increase SiC wafer's production and create additional jobs in the US. The primary site for the business is in Auburn, Michigan, about 120 miles north of Detroit, USA. Through this acquisition, SK Siltron, based in Gumi, South Korea, is expected to maximise its R&D and production capabilities and synergy between its current major businesses, while securing new growth engines by entering rapidly expanding areas.

SK Siltron is South Korea's only producer of semiconductor silicon wafers and one of the top five global wafer manufacturers with annual sales of 1.542 trillion won, accounting for about 17 percent of global silicon wafer sales (based on 300 mm). To sell silicon wafers, SK Siltron has overseas subsidiaries and offices in five locations – the United States, Japan, China, Europe and Taiwan. The US subsidiary, established in 2001, sells silicon wafers to eight customers, including Intel and Micron.

SK Siltron is an affiliate company of Seoul-based SK Group, South Korea's third-largest conglomerate. SK Group has made North America a global hub, with its investments in the US in batteries for electric vehicles, biopharmaceuticals, materials, energy, chemicals and ICT, reaching $5 billion in investments in the US over the past three years.

STMicroelectronics and TSMC Collaborate on GaN

STMICROELECTRONICS and TSMC, the world's largest dedicated foundry, are collaborating to accelerate the development of GaN process technology and the supply of both discrete and integrated GaN devices to market. Through this collaboration, ST's GaN products will be manufactured using TSMC's GaN process technology.

Power GaN and GaN IC technology-based products will enable ST to provide solutions for medium- and high-power applications with better efficiency compared with silicon technologies on the same topologies, including automotive converters and chargers for hybrid and electric vehicles. Power GaN and GaN IC technologies will help accelerate the trend of the electrification of consumer and commercial vehicles. "As a leader in both wide bandgap semiconductor technology and in power semiconductors for the demanding automotive and industrial markets, ST sees significant opportunity in accelerating the development and delivery of GaN process technology and bringing power GaN and GaN IC products to the market. TSMC is a trusted foundry partner that can uniquely meet the challenging reliability and roadmap evolution requirements of ST's target customers," said Marco Monti, president of STMicroelectronics' Automotive and Discrete Group.

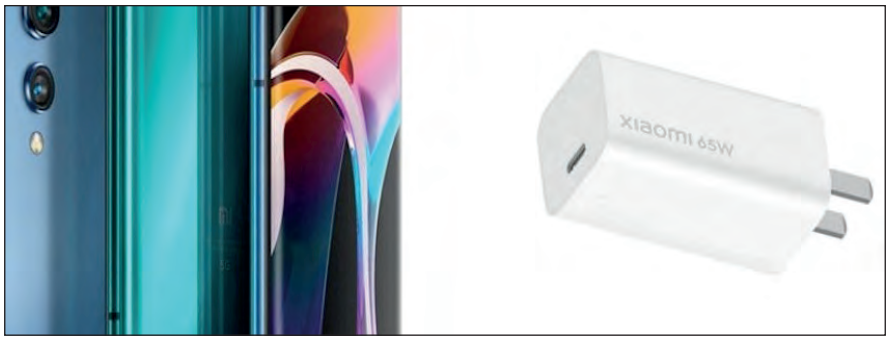
"This cooperation complements our existing activities on power GaN undertaken at our site in Tours, France and with CEA-Leti. GaN represents the next major innovation in power and smart power electronics, as well as in process technology," said Kevin Zhang, Vice President of Business Development at TSMC. "We look forward to collaborating with ST and bring the applications of GaN power-electronics to Industrial and Automotive Power Conversion".

"TSMC's leading GaN manufacturing expertise, combined with STMicroelectronics' product design and automotive-grade qualification capabilities, will deliver great energy efficiency improvement for industrial and automotive power conversion applications that are more eco-friendly and help accelerate the electrification of vehicles."

ST expects the delivery of first samples of power GaN discrete devices to its key customers later this year, followed by GaN IC products within a few months.

Xiaomi chooses Navitas GaN chips for phone charger

NAVITAS SEMICONDUCTOR has announced that its GaNFast charging technology had been adopted by Xiaomi for the flagship Mi 10 PRO smartphone. It now takes only 45 minutes to charge the Mi 10 PRO from 0 to 100 percent.



Xiaomi's 65 W GaN charger uses Navitas' NV6115 and NV6117 GaNFast power ICs which are optimised for high-frequency, soft-switching topologies. Monolithic integration of FETs, drivers and logic delivers a small, fast, 'digital-in, power-out' power conversion module. Using GaNFast, Xiaomi's 65 W GaN charger is only 56.3 mm x 30.8 mm x 30.8 mm, which is half the size of standard adapters.

"GaN as a new semiconductor material has brought unimaginable effects to the charger," said Jun Lei, Xiaomi chairman and CEO. "It enables the charger to become extremely small and the charging efficiency extremely high. The 65 W GaN charger is only half the size of the 65 W traditional charger that comes as standard with our Xiaomi 10 PRO."

Xiaomi invested earlier in Navitas Semiconductor to lay the groundwork for this cooperation, which has also enabled Navitas Semiconductor to broaden its sales channels.

Gene Sheridan, CEO of Navitas Semiconductor, said: "I am very pleased to see Xiaomi's open attitude towards new materials and new technologies. From the start, Navitas has focused on the technology application and innovation of GaN materials."

"GaNFast power ICs are monolithic integration of FET, drive and logic and achieve extremely small application size and high efficiency. For manufacturers who want to lead with technology, GaNFast enables high performance and drives product differentiation."

Yingjie Zha, general manager of Navitas Semiconductor China, said: "The battery capacity of smartphones, tablets and laptops is increasing, while consumers are eager to have a faster-charging experience. GaNFast technology has the advantages of small size, light weight and high efficiency, which makes it extremely attractive."

"GaNFast technology brings the industry a small, efficient charger that can quickly charge electronic products such as mobile phones and laptops."

TMD takes share in GaN PA specialist diamond microwave

Diamond Microwave Limited, a UK-based technology specialist in high-performance microwave power amplifiers, has announced that TMD Technologies, a London-based manufacturer of high-performance equipment for the microwave industry, has become a shareholder in DML.

Diamond Microwave has been a pioneer in the development and manufacture of advanced compact GaN-based microwave high-power solid-state power amplifiers for the radar, electronic warfare, communications and aerospace sectors. DML's chip and wire GaN technology is particularly suited to these demanding applications, where their power-to-volume performance is a leading-edge capability differentiator.

DML's CEO, Richard Lang commented: "We are delighted to welcome TMD as an investor. This is a welcome step in enhancing our existing relationship and further developing our joint interests in world-class amplifier products. TMD is an ideal partner for DML, bringing the possibility of new channels through which to develop and exploit our solid-state power amplifier technology."

Dave Brown, TMD's Group CEO, added: "We have been collaborating with Diamond Microwave for several years and are very pleased with this latest development, which is a logical step forward in our business relationship. Their specialised technological expertise has proved particularly successful across the aerospace and defence industries and complements our current technologies targeted at this market sector. We are looking forward to increased involvement with this forward-looking company – to our mutual benefit".

Celebrating the partnership with a virtual meeting are (left to right): Howard Belk, engineering director, Diamond Microwave; Richard Lang, CEO, Diamond Microwave; Dave Brown, group CEO, TMD Technologies; Nigel Hann, sales director, TMD Technologies Ltd.

Vixar launches high efficiency multi-junction VCSEL

VIXAR, a subsidiary of Osram, has launched its multi-junction VCSEL technology.

The new multi-junction VCSEL boasts a world-record 60 percent power conversion efficiency at 940 nm, significantly higher than the single-junction performance of 53 percent.

The new multi-junction technology is said to represents the next leap forward for the VCSEL industry. The technology can be applied to products in the company's portfolio and boasts slope efficiencies of 2 W/A in dual junction and 3 W/A in triple junction. It offers a world-record 60 percent power conversion efficiency — significantly higher than the comparable single-junction's performance of 53 percent peak wall-plug efficiency.

Greater efficiency reduces the overall thermal load. Higher power density leads to a reduced chip and package size, enabling simpler optic designs and system architecture.

The higher slope efficiency means that a much lower pulsing forward current is required to reach the same optical power as a single-junction VCSEL. The advantage for customers is greatly reducing the current required, which improves the switching speed of the driver. This reduction of current allows the VCSEL to deliver a remarkable one nanosecond pulse for tens or even hundreds of watts.

"Our record-setting multi-junction technology now puts us in a leading position in the VCSEL market" said Klein Johnson, co-founder and CTO of Vixar.

"Our VCSEL technology solves a critical need for customers and is poised to play a key role in shaping the next generation of consumer, industrial and automotive applications."

STMicroelectronics to acquire majority stake in Exagan

STMicroelectronics has signed an agreement to acquire a majority stake in French GaN innovator Exagan. Exagan's expertise in epitaxy, product development and application know-how will broaden and accelerate ST's power GaN roadmap and business for automotive, industrial and consumer applications. Exagan will continue to execute its product roadmap and will be supported by ST in the deployment of its products.

Terms of the transaction were not disclosed and closing of the acquisition remains subject to customary regulatory approvals from French authorities. The signed agreement also provides for the acquisition by ST of the remaining minority stake in Exagan 24 months after the closing of the acquisition of the majority stake. The transaction is funded with available cash.

"ST has built strong momentum in SiC and is now expanding in another very promising compound material, GaN, to drive adoption of the power products based on GaN by customers across the automotive, industrial and consumer markets" said Jean-Marc Chery, president and CEO of STMicroelectronics.

"The acquisition of a majority stake in Exagan is another step forward in strengthening our global technology leadership in power semiconductors and our long-term GaN roadmap, ecosystem and business. It comes in addition to ongoing developments with CEA-Leti in Tours, France, and the recently announced collaboration with TSMC."

Founded in 2014 and headquartered in Grenoble (France), Exagan is dedicated to accelerating the power-electronics industry's transition from silicon-based technology to GaN-on-silicon technology, enabling smaller and more efficient electrical converters. Its GaN power switches are designed for manufacturing in standard 200 mm wafer fabs.

Infineon announces 650 V SiC MOSFETs

INFINEON TECHNOLOGIES is expanding its SiC product portfolio with 650 V devices. With the newly launched CoolSiC MOSFETs the company says that it is addressing the growing demand for energy efficiency, power density, and robustness in a wide range of applications. Amongst them are server, telecom and industrial SMPS, solar energy systems, energy storage and battery formation, UPS, motor drives as well as EV-charging.

"With this launch, Infineon complements its broad silicon, SiC, and GaN-based power semiconductor portfolio in the 600 V / 650 V power domain," said Steffen Metzger, senior director high voltage conversion at Infineon's Power Management & Multimarket Division. "It underlines our unique position in the market being the only manufacturer with such a broad offering for all three power technologies. Additionally, the new CoolSiC family supports our claim to be the number one supplier of SiC MOSFET switches for industrial purposes."

The CoolSiC MOSFET 650 V devices are rated from 27 mΩ to 107 mΩ. They are available in classic TO-247 3-pin as well as TO-247 4-pin packages, which allows for even lower switching losses. As for all previously launched CoolSiC MOSFET products, the new family of 650 V devices are based on Infineon's state-of-the-art trench semiconductor technology.

Maximising the strong physical characteristics of SiC, this ensures that the devices offer superior reliability, best-in-class switching and conduction losses. Additionally, they feature highest transconductance level (gain), a threshold voltage of 4 V and short-circuit robustness.

650 V CoolSiC MOSFETs are said to offer many benefits in comparison to other silicon and SiC solutions such as switching efficiency at higher frequencies and high reliability. Thanks to the low on-state resistance dependency on temperature they feature an excellent thermal behaviour. The devices also have body diodes retaining a low level of reverse recovery charge, roughly 80 percent less than the best superjunction CoolMOS MOSFET.

The commutation-robustness helps in achieving, very easily, an overall system efficiency of 98 percent, such as through the usage of continuous conduction mode totem-pole power factor correction (PFC).

To ease the application design using CoolSiC MOSFETs 650 V and to ensure high performance operation of the devices, Infineon offers dedicated 1-channel and 2-channel galvanically isolated EiceDRIVER gate-driver ICs. This solution – combining CoolSiC switches and dedicated gate-driver ICs – helps lowering system costs as well as total cost of ownership and enables energy efficiency gains. The CoolSiC MOSFETs also work seamlessly with other ICs from Infineon's EiceDRIVER gate-driver family.

Qorvo launches highest-performance wideband GaN PA

QORVO has introduced what it believes is the world's highest-performance wideband power amplifier (PA). Designed for electronic warfare, radar and test instrumentation applications, the TGA2962 breaks through multiple performance barriers with an industry-leading 10 W of RF power over the 2-20 GHz frequency range, 13 dB large-signal gain and 20-35 percent power added efficiency. This combination delivers the flexibility that system designers need to improve system performance and reliability while reducing component count, footprint and cost.

Roger Hall, General Mananger of Qorvo's High Performance Solutions business, said: "Qorvo has taken a significant step forward in the wideband space with the TGA2962, enhancing not just frequency range but every other performance aspect. No other company offers a single PA with this output power, bandwidth, power-added-efficiency and large signal gain."

The TGA2962 is built on Qorvo's GaN QGaN15 process technology. In addition, improved component integration – and use of a smaller driver amp enabled by the 13dB large-signal gain – result in a smaller device, making this a compelling solution for programmes that require size, weight, power and cost improvements.

Eric Higham, director of the Advanced Semiconductor Applications service and the Advanced Defense Systems service for Strategy Analytics, said: "The defence market, primarily radar and

communications applications, is seeing strong growth from new systems and major platform upgrades. This is also providing fuel for the GaN growth engine and should bode well for companies like Qorvo."

The TGA2962 wideband 10 W GaN PA is available now as a die to qualified customers.

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RF GaN: big revenues, bright future?

Despite billion dollar revenues forecast to roll in from 5G infrastructure and defence in just three years, GaN may not have hit the big-time quite yet, reports Rebecca Pool.

4G and 5G cell site base station

WHEN IT COMES to RF GaN, the future looks bright, according to the latest figures from Eric Higham, analyst, at Strategy Analytics. As he forecasts in *RF GaN Market Forecast: 2018 to 2023*, revenue for RF GaN-enabled devices grew by nearly 22 percent in 2018, and is set to surpass $1.7 billion in 2023.

The drivers for this burgeoning growth come from 4G and 5G base station deployments, as well as defence applications. But the pathway to the billion dollar big-time may not be plain sailing.

In the past, silicon-based laterally-diffused metal-oxide semiconductor (LDMOS) devices have been widely used in base station RF power amplifiers, but, as always, change is afoot. Since the beginning of 4G LTE deployment across China in 2014, equipment manufacturers and operators have embraced GaN with open arms, with the healthy revenue rises ensuing.

Given this, RF GaN has been steadily displacing LDMOS in base station power amplifiers. And while LDMOS technology still holds the largest revenue share right now, GaN is expected to continue to displace it, especially at higher frequency 5G deployments including millimetre-wave bands, from 30 GHz to 300 GHz.

But as Higham cautions, a 'storm cloud on the horizon' is looming for GaN RF power amplifiers in 5G base stations. In sub-6 GHz 5G spectrum bands, more and more radiators are set to be added to the antennas in massive MIMO systems, to ease beam-forming.

"More radiators means you are more able to adapt, say, the shape of that beam, to make [data delivery] as efficient as possible for the operator," highlights Higham. "But as you add more and more radiators, the transmit power for each power amplifier goes down, which means SiGe and CMOS are now more inexpensive options [than GaN]."

And while GaN can offer, for example, greater power-added efficiency and power density compared with the silicon-based technologies, operators have always tended to demand a lower power bill.

"Both GaN and silicon camps can make compelling arguments for their technologies but at the end of the day the market will choose," says Higham. "If an operators rolls out a 600 or 700 MHz 5G network, then that will likely have LDMOS in it due to its pricing."

"LDMOS could remain the largest power technology for base stations in one, two, maybe three years," he adds. "However, the 5G spectrum mix of sub-6 GHz frequency versus high-frequency millimetre wave will be clearer in the next 18 months."

Infrastructure uncertainties are not the only cloud on GaN's horizon. Ongoing political tensions could also soften GaN growth in this market sector as China tech giant, Huawei, remains firmly fixed on the US Bureau of Industry and Security 'Entity List'.

"Huawei has been pretty proactive in adopting GaN, probably more so than other equipment suppliers," says Higham. "So if its market share goes down, then that could have an impact on GaN's market share."

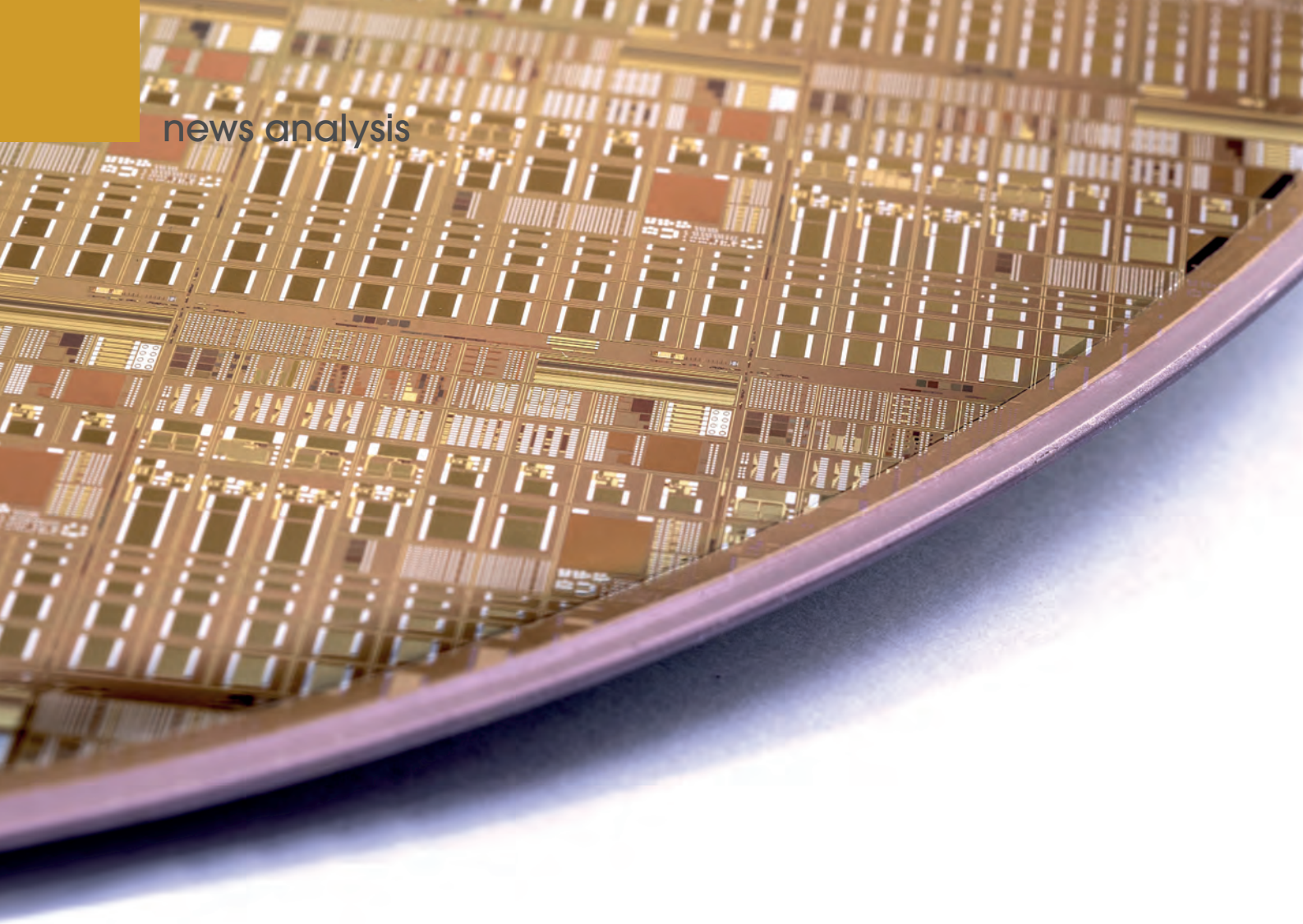
What's more, China could well push ahead with growing its own compound semiconductor 'eco-system', a move that would spell bad news for GaN players across the rest of the world. According to Higham, the Chinese government has poured billions into upgrading Sanan IC's compound semiconductor foundry while Huawei recently revealed a handset comprising components from domestic suppliers only.

"I don't know how good the Huawei phone is, and you can't build a foundry on Monday and have it up and running on Tuesday," says Higham. "But if China really pushes ahead to have a domestic capability then that will put a lot of other manufacturers at risk."

In the meantime, defence markets are set to provide respite from 5G infrastructure and political uncertainties. Thanks to a wave of defence programmes reaching production, major retrofits as well as procurements from US, China, Russia and other nations, Higham predicts the defence market will grow a little faster than the commercial sectors in the near-term. And, crucially, GaN has already proven itself in key defence market segments, radar and communications.

"The radar folk don't pull out a clean sheet of paper without writing GaN on it, and all the latest active electronically scanned array [antennas] use GaN," says Higham. "GaN is also being adopted very quickly in tactical radios and other communications applications that demand higher operating frequencies and bandwidths."

"So today, or at least until we see more certainty around 5G, the defence sector is safer than the infrastructure market," he adds.



Qromis: ready for business

As the GaN market gathers momentum, Qromis is serving up fab-friendly substrates and epi-wafers to ease device manufacture, reports Rebecca Pool.

IN JANUARY THIS YEAR, Silicon Valley based Qromis revealed two developments that signal the company is on the cusp of rapid expansion.

For starters, the fabless, wide bandgap materials business has just received an undisclosed investment from The Mirai Creation Fund, led by Japan-based investors SPARX.

At the same time, it has also signed a licensing agreement with Shin-Etsu Chemical, a Japan-based silicon wafer and materials manufacturer, to produce substrates and epiwafers for GaN power/RF electronics, LED devices and more.

Qromis' latest developments follow five years of development of its novel materials technology for substrates. And right now, chief executive, Cem Basceri, is excited.

"We've developed this unique CMOS fab-friendly substrate technology that is scalable and stress-matched to GaN," he says. "It sounds simple but it's taken years of development and investment."

"Now, a device manufacturer can take our substrate, and without any challenges, make many different device features," he adds. "This is extremely valuable."

Rapid progress

Qromis launched back in 2015 to commercialise its Qromis Substrate Technology, QST. Ready for GaN epi-growth, these substrates comprise an engineered coefficient of thermal expansion (CTE)-matched core onto which several engineered layers are deposited. A top thin silicon interface is also deposited onto the engineered layers.

Crucially, the CTE-matched core has a thermal expansion that closely matches the thermal expansion of the GaN-AlGaN epitaxial layers, enabling the deposition of low dislocation density, crack-free GaN epitaxy from a few microns to bulk-like thickness.

As Basceri highlights: "We did this so that the substrate would be stress-matched with GaN without any cracking or wafer breakage issue and also to prevent substrate cross-talk in integrated circuits, which is a big issue on silicon."

Qromis has already released 6- and 8-inch GaN-ready QST substrates as well as 6- and 8-inch 'templates' with 5 μm and 10 μm GaN layers. What's more, 200 V and 650 V GaN HEMT epi-wafers, based on 6-inch and 8-inch QST substrates, are being fine-tuned for commercial devices while 900 V and 1200 V GaN HEMT epi-wafers are also being developed and sampled.

The company's rapid technology development follows partnerships and collaborations with a host of industry players up and down the supply chain. Within a year of launching, the company had partnered with Vanguard International Semiconductor, licensing its key technologies to the Taiwan-based silicon foundry for manufacturing.

Since 2016, the company has also worked closely with microelectronics innovation hub, imec, Belgium, on device fabrication, developing GaN power devices, in discreet and monolithically-integrated ICs forms, on 200 mm QST substrates in an advanced CMOS silicon pilot line.

Imec and Qromis have also been collaborating with GaN MOCVD equipment manufacturer, Aixtron, Germany, on GaN-on-QST epitaxy development. The results have been quite remarkable.

As Basceri points out, the industry standard platform for GaN-on-silicon has been 150 mm wafers. And while imec has pioneered the development of 200 mm GaN-on-silicon wafers for HEMTs to 650 V operating voltages, thermal mismatch between the GaN/AlGaN layers and silicon has stymied device fabrication at higher voltages.

Imec and Qromis have since developed enhancement mode *p*-GaN discrete and IC power devices on 200 mm QST substrates with epitaxy layers grown in Aixtron's G5+ C 200 mm MOVCD platform. Crucially, imec was able to port its *p*-GaN e-mode power device technology to Qromis' 200 mm GaN-on-QST wafers in its silicon pilot line, and also demonstrate high-performance power devices.

"Vanguard then decided to licence imec's device technology, GaN power epitaxy and processes and the company is currently manufacturing and tuning devices to [partner's] specifications," says Basceri. "This has been a big turning point."

Ramping manufacture

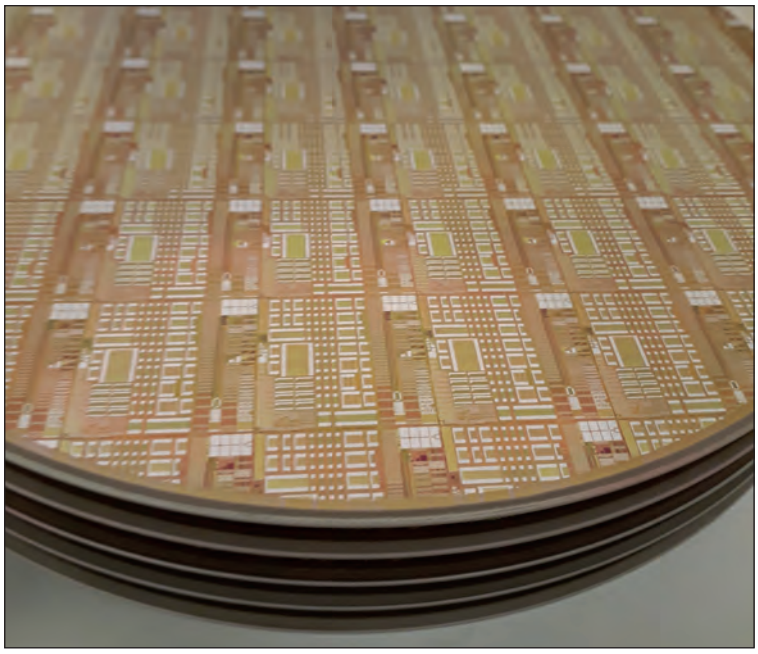
In line with healthy GaN growth forecasts, Basceri says Vanguard will 'open its doors to everybody' later this year, offering GaN power, and later RF, device manufacturing services on the 200 mm diameter QST platform. This has also prompted the Qromis chief executive to establish a second manufacturing source for QST substrates and GaN-on-QST epitaxy wafers, in the form of Shin-Etsu Chemical. Importantly, with this partnership, QST-based materials products will be commercially available from both Shin-Etsu and Qromis for industry players.

According to Basceri, Shin-Etsu is going to aggressively move ahead with the development of GaN-related products, supplementing its existing line-up of GaN-on-silicon, SOI and silicon wafers. As he says: "From what we hear from our partners and customers that use Vanguard, we are expecting wafer demand to reach tens of thousands of wafers in the next three-to-four years."

With its substrates, Qromis will address a range of applications starting with GaN power and RF devices and later LED devices, such as microLEDs, and sensors. One of the key markets will be electric vehicles – as Basceri points out, a significant portion of SPARX's Mirai Creation Fund comes from Toyota Motor Corporation, which is heavily entrenched in this market.

"We expect to start ramping up 200 millimetre manufacturing between 2021 and 2022, and I would also expect to see an overall demand for 300 millimetre wafers starting by 2025 for which we have already started to receive some initial inquiries," says Basceri. "Several years ago, there were missing links in the GaN business, but the tipping point is now here."

Qromis, Chief Executive, Cem Basceri



EpiPix: a new way with microLEDs

University of Sheffield spin-out, EpiPix, is set to deliver the ultra-high brightness, ultra-small microLED arrays that industry players crave. Rebecca Pool finds out more.

EARLIER THIS YEAR, the UK-based University of Sheffield launched a spin-out company, EpiPix, to develop and commercialise microLED technology for display panels in augmented and virtual-reality devices, smart watches, mobile handsets and more.

Based on many years of GaN semiconductor research from Professor Tao Wang, based at the University's Centre for GaN Materials and Devices, the company has already demonstrated prototype micro-LED arrays on single wafers with microLED pixel sizes from 30 μm down to 5 μm and less.

The launch comes at a time when Apple has ploughed some $2 billion into microLED development, myriad companies from Plessey and Glo to Lumens and Sharp have demonstrated microdisplays on CMOS backplanes, and patent fillings are going through the roof. EpiPix chief executive, Dennis Camilleri, is excited.

"We are already engaged in discussions with major end-user customers for AR/VR applications, manufacturers of smart watches and smart phones and also LiFi companies," he says.

"For many applications the key technical driver is to produce very small microLEDs that will give you that high resolution, high brightness display," he says. "We are going to produce less than five micron-size microLEDs and this is what all these major companies are interested in."

A direct approach

Your typical III-nitride microLEDs are manufactured using standard photolithography processes followed by dry-etching on a III-nitride LED wafer. However, dry-etching induces surface damage to the microLED, particularly at lower microLED diameters, degrading optical performance, including internal and external quantum efficiencies. As a result, industry players, far and wide, have struggled to fabricate high-brightness, microLEDs with dimension below 5 μm.

Given this, Wang and colleagues decided to take a different tack and for the past five years have been developing a direct epitaxial method for fabricating ultra-small and ultra-bright InGaN micro-LEDs that eliminates the need for dry-etching.

Here an *n*-GaN layer is grown onto a silicon or sapphire substrate to create an as-grown *n*-GaN template. A SiO_2 film is then grown onto the *n*-GaN layer, with an array of holes of the required microLED shape and diameter. LED structures can then be grown onto this pre-patterned SiO_2 microhole arrayed template to form the microLED arrays.

Crucially, the method uses standard MOCVD processes, and the arrays are designed to be compatible with any existing microdisplay fabrication technique including, pick-and-place and mass transfer technologies.

"Wang's process does not involve dry-etching, damage and optical degradation, and so we've been getting some very good external quantum efficiencies with our micro-LED arrays," says Camilleri. "This is why this process is attracting so much interest."

Indeed, earlier this year, Wang and colleagues unveiled high luminance green microLED array bare chips, with a diameter of 3.6 μm, inter-pitch of 2 μm and a record external quantum efficiency of 6 percent. This result has been quickly published in *ACS Photonics*. According to Camilleri, the researchers have fabricated blue microLEDs and are also developing red versions. EpiPix is also working with packaged chips.

"This figure of 6 percent for a very small green microLED is a world record," he says. "We are not using any reflective layers and no additional processing is taking place... This is pure light coming out of the microLED array."

EpiPix has a worldwide exclusive licence to commercially exploit the IP from the University of Sheffield... and when our customers scale up manufacturing of products based on our microLEDs, then EpiPix could licence IP out to them

So what now for EpiPix? As Camilleri points out, the start-up is operating on a commercial technology centre business model and will carry out product development, testing and validation of device performance, as demanded by end-user customers.

"EpiPix has a worldwide exclusive licence to commercially exploit the IP from the University of Sheffield... and when our customers scale up manufacturing of products based on our micro-LEDs, then EpiPix could licence IP out to them," he says. "We will be piloting assembly, production and packaging to ensure applications work but we don't see ourselves as a volume manufacturer of microLEDs."

So far, fabrication has taken place on 2-inch wafers, and now EpiPix will scale this to 4-inch or 6-inch substrates. The next 18 months to two years will also be spent on product development, beta prototyping, testing and providing samples to customers. And with process and device validation in hand, the microLED wafers will be ready for high-volume manufacture.

"These devices can also be used for high-speed data transmission in LiFi applications, but I expect the first applications to be AR and VR as well as smart watches and mobiles," says Camilleri. "In around two years, I want to be selling our microLED arrays to at least half a dozen global corporates in these applications."

A massive boost for **UV LED efficiency**

The monolithic integration of a conventional LED structure and a multiplicative photoelectric converter propels the wall-plug efficiency of deep UV LEDs emitting at 280 nm to more than 20 percent

BY HAIDING SUN FROM UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA AND HANLING LONG, FENG WU, JIANGNAN DAI AND CHANGQING CHEN FROM HUAZHONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

FOR MANY DECADES, the most common source of UV light has been the mercury lamp. It has netted substantial sales, due to its widespread use in air/water purification, sterilization, phototherapy, lithography and UV curing. However, it is a source of UV emission that is far from ideal: it consumes much energy; lamps don't last long; and it contains mercury, which is toxic. The latter a big deal, as concerns over health continue to grow. For example, an international treaty known as the Minamata Convention on Mercury is calling for mercury-containing products to be progressively prohibited by the end of this year.

A UV LED under operation

The leading environmentally-friendly, energy-efficient alternative to the mercury lamp is the UV LED. This device, which is also renowned for its small size and long lifetime, spans a spectral range from 210 nm to 360 nm by varying the aluminium content in the AlGaN quantum wells. As well as offering an alternative to the UV lamp in some applications the UV LED can also be used for new tasks (see Figure 1). This helps the device to capture even more revenue. According to market analyst Yole Développement, the market size for the UV LED will grow from $500 million in 2019 to $1 billion in 2023.

The Achilles heel of the UV LEDs is its low efficiency. Compared to its blue cousins – which feature InGaN quantum wells, produce extremely high external quantum efficiencies and have a wall-plug efficiencies exceeding 80 percent – the performance of the UV LED is pitiful. As the wavelength drops below 360 nm efficiency plummets. For emission at 280 nm, the external quantum efficiency and wall-plug efficiency are typically just 6 percent and 5 percent, respectively.

It is possible to improve efficiency by refining the device. Efficiencies increase by: reducing defects and dislocations in the epilayers; improving *n*- and *p*-type doping efficiencies, to create conductive films for better current injection; re-designing the device for better light extraction; and employing a superior AlGaN-based quantum well and barrier design in the active region.

Our team from the University of Science and Technology of China and Huazhong University of Science and Technology has produced more efficient UV LEDs by making much progress on all these

UV LEDs that smash the record for wall-plug efficiency are made on sapphire substrates

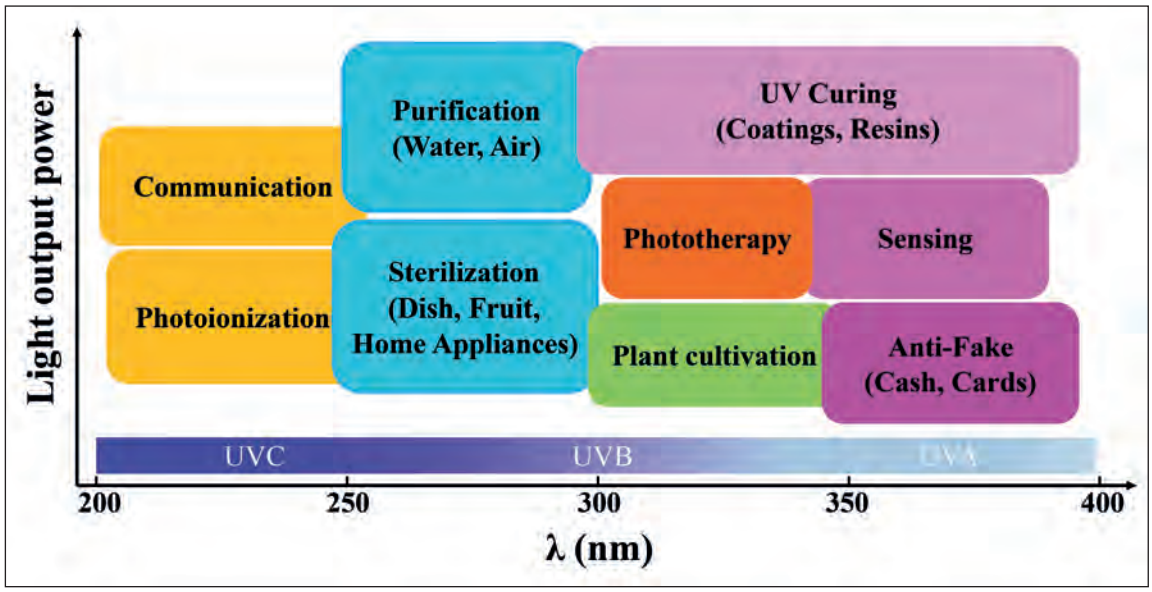
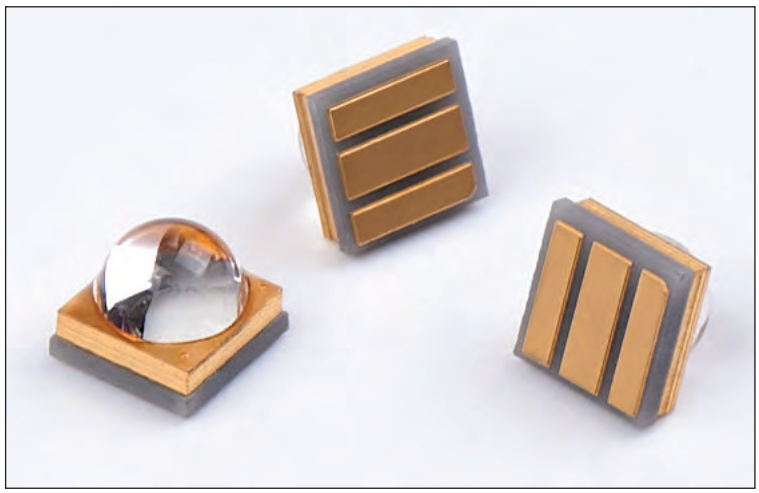


Figure 1. There are many applications for UV LEDs

fronts. However, this approach only gets us so far – so we have gone on to deliver a step change in performance by combining these refinements with a novel architecture that combines a conventional LED structure with a multiplicative photoelectric converter. Read on to discover the secrets of our success.

Conventional strategies

We grow our heterostructures for our UV LEDs on sapphire, a low-cost transparent substrate. We avoid native AlN because it is prohibitively expensive. The downside of sapphire is that is has lattice and thermal expansion mismatch with the nitride layers, leading to an inferior crystalline quality that drags down the radiative recombination efficiency. To tackle this issue, we have turned to pyramidal patterned sapphire, a foundation that supports lateral overgrowth during AlN epitaxy. The AlN films that result have excellent crystal quality. According to the full-width at half-maximum of the peaks produced from X-ray diffraction rocking curves, the threading dislocation density is less than 3×10^8 cm^{-2} (see Figure 2 (a)). We have also undertaken reciprocal space mapping – this shows that the epilayers are free from strain. Based on these findings, we know that we can supress the density of non-radiative recombination centres in the active region of our UV LEDs, and ultimately realise a high radiative recombination efficiency in these devices.



Packaged UV LEDs

The benefits of patterning a substrate are not limited to the better material quality that comes from annihilation of dislocations. In addition, texturing boosts the output from the chip. This is particularly important in the deep UV, where the optical polarisation induced by the unique valance band structure within the active region limits the light extraction from the device. Unfortunately, the transverse-electric mode, which dominates in blue LEDs and aids extraction, is overtaken by the transverse-magnetic polarisation mode.

Previous work by our team has shown the benefits of using a moth-eye microstructure on sapphire's bottom surface of a flip-chip UV LED (see Figure 2(b)). With this pattern the uniformly periodic microstructure extends the light extraction angle. Note that this particular microstructure enhances the transverse-electric mode. It has a distribution with a dominate contribution in the vertical direction, which is easier to extract.

We realise an additional increase in light extraction by modifying light polarisation via strain modulation in the AlGaN quantum wells. By ensuring compressive in-plane strain in the wells we promote emission of the transverse-electric mode, leading to a hike in light-extraction efficiency for the UV LED.

Recently, we have made further gains by combining patterned sapphire with a silica array (see Figure 2(c)). This modification reduces threading dislocation density and enhances light extraction efficiency, thanks to a large difference in refractive index between the AlGaN epilayers and the patterned sapphire with a silica array. Another factor that governs the

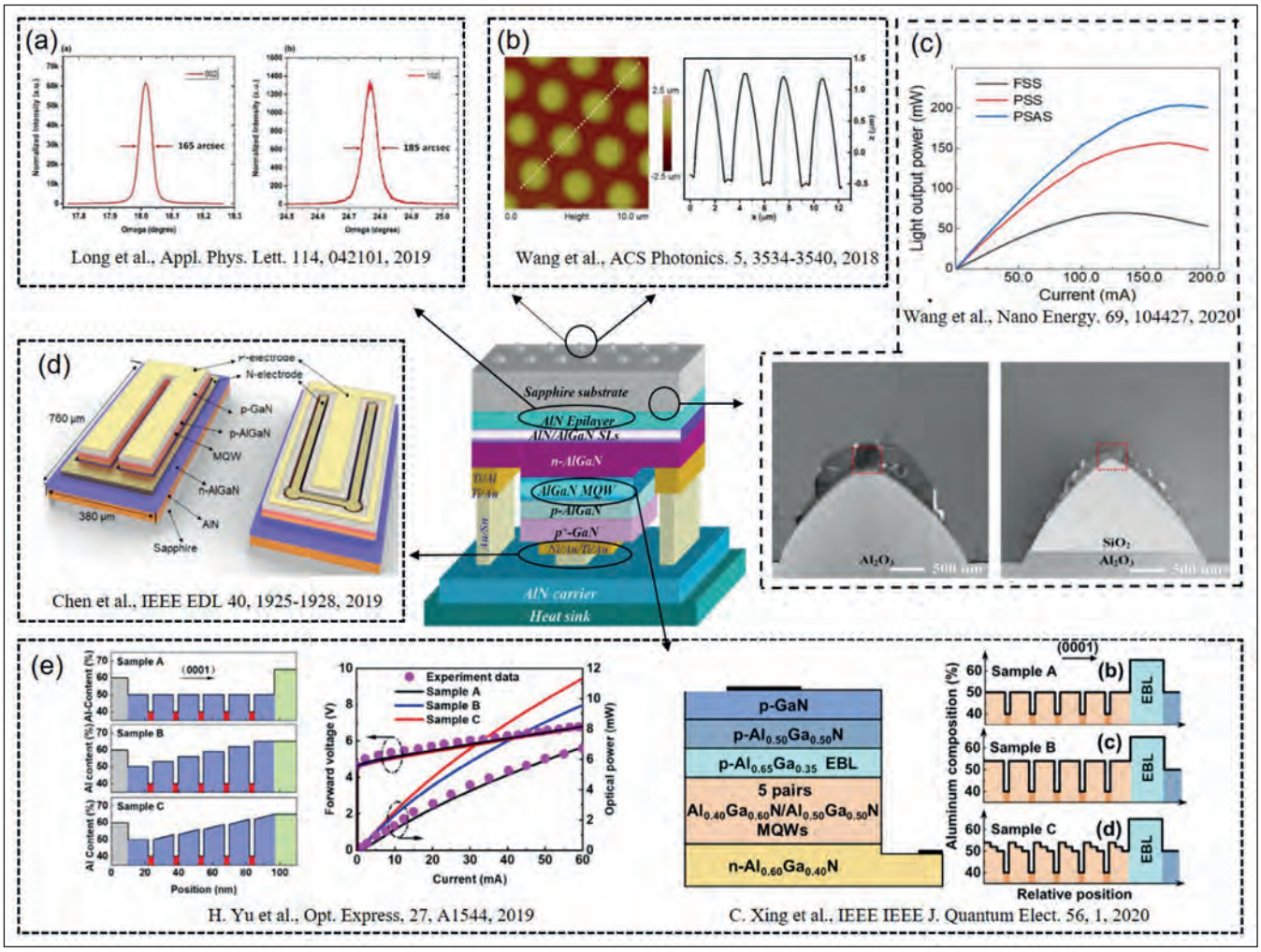


Figure 2. Strategies to improve the performance of UV LEDs. (a) Patterned sapphire substrates enhance the crystal quality of epitaxy AlN. H. Long *et al*. Appl. Phys. Lett. **114** 042101 (2019) (b) Fabricating moth-eye microstructure on the sapphire bottom surface of flip-chip UV LEDs enlarges the light extraction angle. S. Wang *et al*. ACS Photonics **5** 3534 (2018) (c) Switching to a patterned sapphire with silica array (PSSA) reduces the threading dislocation density and enhances light extraction efficiency, thanks to the large refractive index contrast between the epilayers and PSSA. S. Wang *et al*. Nano Energy **69** 104427 (2020) (d) Novel electrode patterns can optimise current-spreading in a UV LED chip. Q. Chen *et al*. IEEE Elect. Dev. Lett. **40** 1925 (2019) (e) Designing the band structure of the AlGaN quantum wells heterostructure in the active region improves radiative recombination. H. Yu *et al*. Opt. Express **27** A1544 (2019); Ren *et al.* J. Phys. D Appl. Phys. **53** 073002 (2020)

performance of the UV LED is how efficiently the current can be injected into the device. As sapphire is insulating, it is impractical to adopt a vertical LED architecture. Due to this, the most common design for improving current injection and light extraction is based on a flip-chip bonding technology. Unfortunately, current crowding results, deteriorating device performance.

One option that we have developed for increasing the uniformity of current spreading in UV LED chips is to introduce novel electrode patterns (see Figure 2(d)). With this design, the *n*-type electrode surrounds its *p*-type counterpart to provide sufficient current paths for carrier transport.

Last but by no means least, UV LEDs are hampered by the strong spontaneous polarisation and the piezoelectric polarisation field in the AlGaN material system. Due to the quantum confined Stark effect, the wavefunctions of the electron and hole are pulled in opposite directions, suppressing effective radiative recombination. To address this, a variety of forms of bandgap engineering have been pursued to increase the internal quantum efficiency, suppress the current leakage and diminish efficiency droop at high current injection (see Figure 2(e)).

Part of the reason behind the high quantum efficiency of blue LEDs is the indium segregation in the InGaN quantum wells. Segregation results in carrier localisation effects, increasing the likelihood of radiative recombination. With the AlGaN quantum wells required for UV LEDs, segregation is far less pronounced, because aluminium atoms have a far lower mobility than gallium. Localisation can also

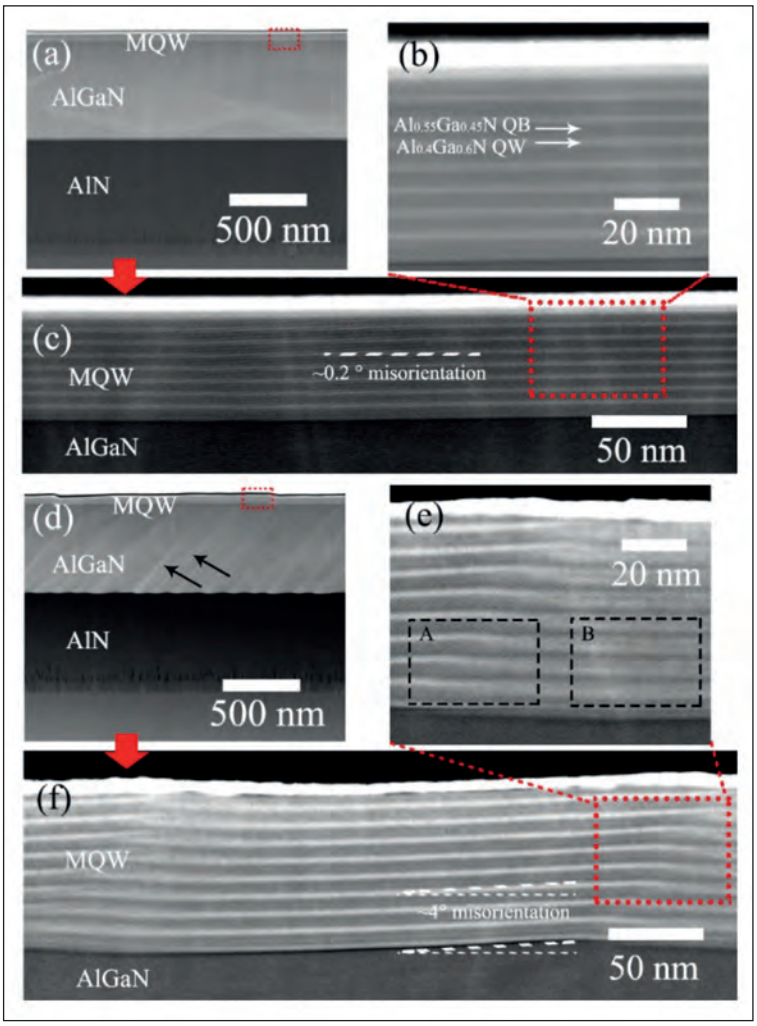
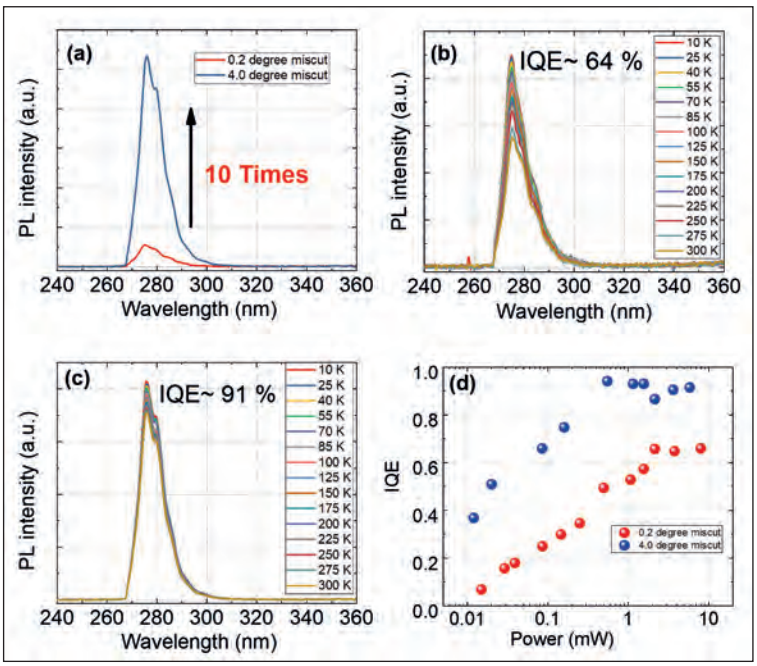


Figure 3. Cross-sectional scanning transmission electron microscopy image of AlGaN multi-quantum wells grown on (a-c) 0.2° and (d-f) 4° misoriented sapphire substrates. H. Sun *et al*. Adv. Funct. Mater. **29** 1905445 (2019)



result from thickness variations, but it is challenging to introduce, because aluminium and gallium atoms are a similar size.

The good news is that we are able to replicate the carrier localisation effects in blue LEDs in our UV emitters with a new kind of nanoscale structure, which we refer to as wavy quantum wells. We artificially create a 'phase separation', leading to compositional inhomogeneities in AlGaN alloys.

We produce LEDs with these wavy quantum wells by growing aluminium-rich deep UV LEDs on misoriented sapphire substrates with a significant mis-cut angle – it is as large as 4° (see Figure 3). The 280 nm LEDs produced by this process benefit from the semi-polar template that results – it produces a reduced polarisation field, in addition to increased carrier localisation.

Measurements on these devices produce much better results than those made using flat sapphire. Photoluminescence intensity is at least ten times higher; internal quantum efficiency is six times higher at low excitation laser power, with a record result of over 90 percent; carrier lifetime is far longer, reaching 1.60 ns on 4° misoriented sapphire, compared with just 0.06 ns on 0.2° misoriented sapphire; and wafer-level output power of the UV LEDs is two-to-three times higher (see Figures 4 and 5).

Even with this improvement to the internal quantum efficiency of the UV LED, the wall-plug efficiency is typically below 5 percent for devices emitting below 300 nm. To reach far higher values requires a radical change to the design. We have done just that, realising a record wall-plug efficiency of 21.6 percent through the monolithic integration of a deep UV LED with a multiplicative photoelectric converter.

A radical architecture

Our novel device tackles the extremely low injection efficiency in conventional deep UV LEDs that is to blame for the unsatisfactory efficiency. In our radical design, the *p-i-n* GaN structure acts as an electric-optic converter and hole-multiplier, absorbing deep UV photons and generating electron-hole pairs. These carriers are pulled apart by the extremely high electric field. Holes are then multiplied by impact ionisation, before being re-injected into the active region, where they take part in radiative recombination (see Figure 6).

Left: Figure 4. (a) Room-temperature photoluminescence (PL) spectra of AlGaN multi-quantum wells (MQWs) grown on 0.2° and 4° sapphire substrates. Temperature-dependent PL spectra of AlGaN MQWs grown on (b) 0.2° and (c) 4° misoriented substrates. (d) Internal quantum efficiency (IQE) as a function of pumping power for both MQWs grown on 0.2° (red dots) and 4° (blue dots) misoriented substrates. H. Sun *et al*. Adv. Funct. Mater. **29** 1905445 (2019)

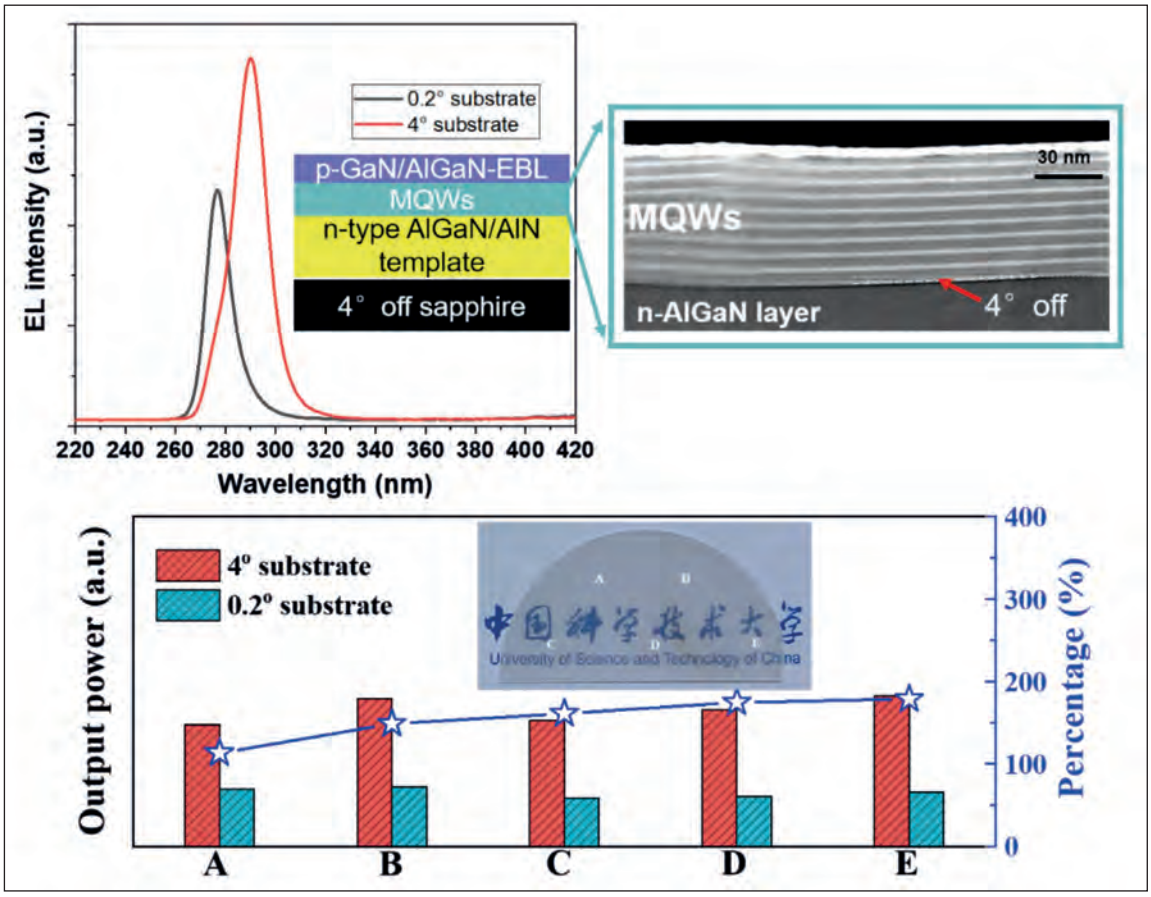


Figure 5. Electroluminescence (EL) spectra and output power comparison. H. Sun *et al.* Adv. Funct. Mater. **29** 1905445 (2019)

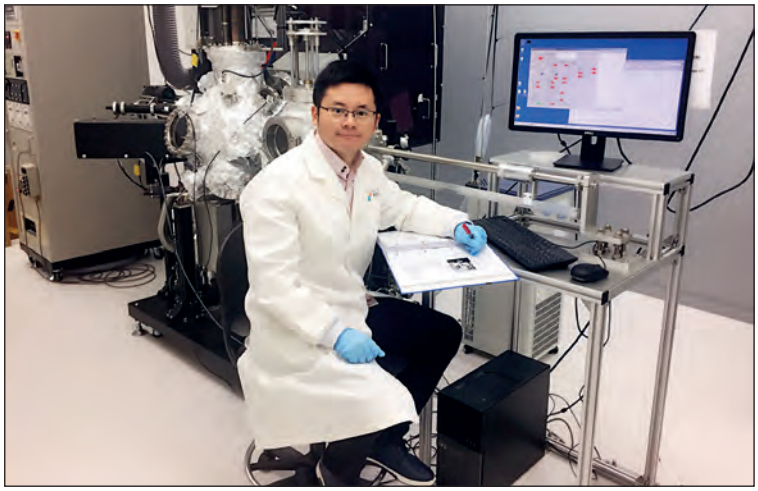
To investigate the photoelectric characteristics of our new device, we have compared its electroluminescence spectra to that of a conventional UV LED (see Figure 7(a) and (b)). Note that our new device exhibits a voltage-dependent characteristic, due to the reverse-biased multiplicative photoelectric converter. Plots of light output reveal an identical power when the conventional device is run at 4.88 V and 1.87 mA, and the novel LED is driven at 19.5 V and 7.85 μA. From these figures we can conclude that the wall-plug efficiency in the conventional device is 0.36 percent, while that with the photoelectric converter is 21.6 percent – that is 60 times higher.

The current-voltage characteristics are markedly different from the norm in our novel device (see Figure 8). For our conventional UV LED, turn-on is at 4.5 V, while the leakage current is very low, indicating that it is reliable. In comparison, for our record-breaking LED, there are three distinct regions that span different ranges of operating voltage (for details, see Figure 8).

We have simulated the electric field profile of the *p-i-n* GaN region under a 6 V bias (see Figure 9(a)). Calculations reveal that the electric field extends into the *n*-GaN layer, and that the *i*-GaN layer is completely depleted. What's more, these simulations show that the strength of the electric field exceeds 5 MV/cm, making it strong enough to realise Geiger mode multiplication in GaN material.

Our modelling also offers an insight into the operation of our LED. When deep UV photons are absorbed within the device, they generate an electron hole pair, and due to the reverse bias in the multiplicative photoelectric converter, electrons drift to the anode and holes to the cathode. Due to Geiger mode, each carrier is multiplied several dozens of times in the multiplicative photoelectric converter, before it is re-injected into the active region. This results in a significant enhancement for the hole-injection efficiency in this class of LED. Photon recycling can also take place in this device (see Figure 9(b)) for details).

Material deposition for device fabrication



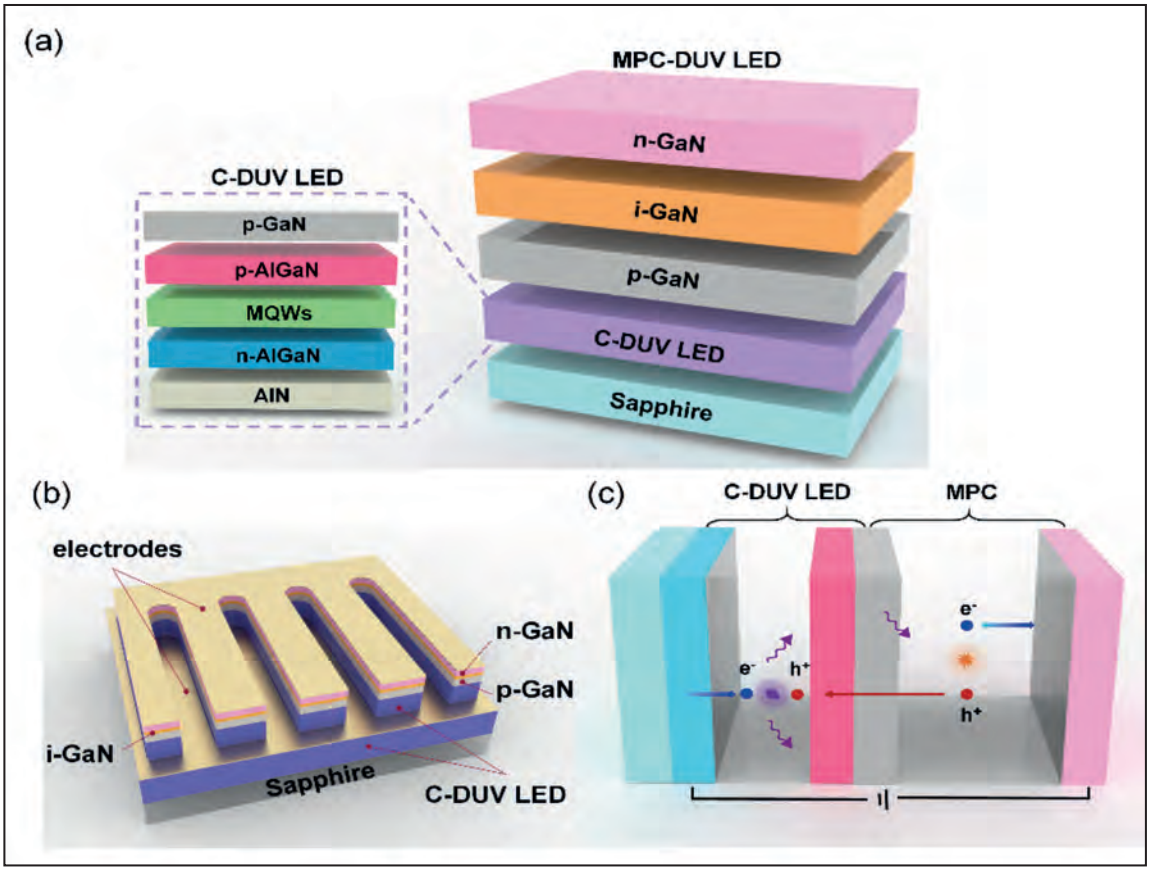


Figure 6. (a) The design of a conventional deep UV LED (C-DUV LED) and a multiplicative photoelectric converter deep UV LED (MPC-DUV LED). (b) Device structure of MPC-DUV LED. (c) An illustration of the carrier recombination and photon recycle process of the MPC-DUV LED. For more details see: S. Wang *et al*. Nano Energy. **66** 104181 (2019).

The novel device that we have developed promises to realise far more than just a hero result in a lab. Its mass-production is not that difficult, as the multiplicative photoelectric converter can be grown *in-situ* using conventional MOCVD. The challenge is to improve the light output power of this form of LED.

Although there are applications where low-power deep UV LEDs can serve, such as microLEDs, many opportunities require sources with a high power. We are targeting this goal by optimising the epitaxial structure and fabrication process.

While a 20 percent wall-plug efficiency is a very encouraging result, there is still much work to do. We hope that further increases in both the external quantum efficiency and the wall-plug efficiency are within our grasp by improving the material quality, the doping efficiency, and light extraction. Such efforts will take place during the on-going transition period from the mercury-based UV lamp to AlGaN-based UV LEDs, and will help to increase the adoption of clean, reliable UV sources. Given the rapid development in visible InGaN-based LEDs, all of us have good reason to be optimistic about the realisation of highly efficient, high-power deep UV LEDs in the near future.

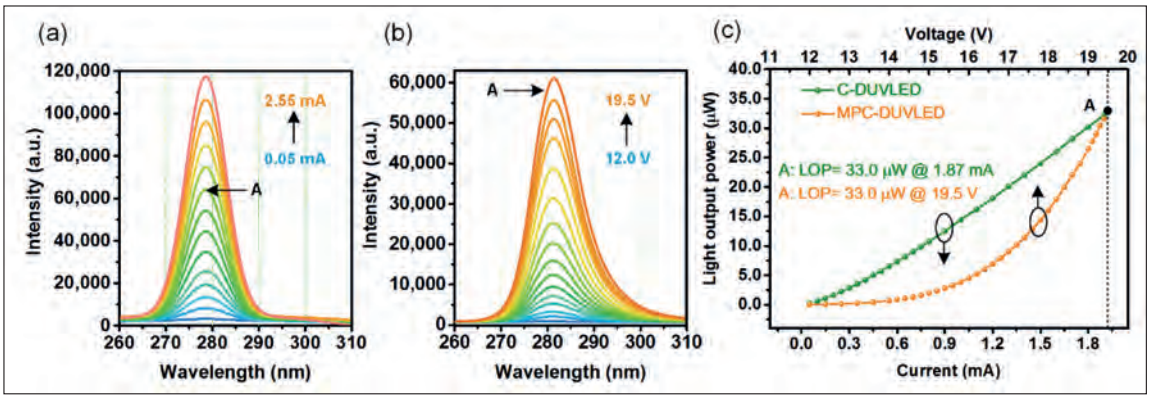


Figure 7: Electroluminescence (EL) for (a) the conventional deep UV LED (C-DUV LED), and (b) the multiplicative photoelectric converter deep UV LED (MPC-DUV LED). (c) Light output power for the MPC-DUV LED and the C-DUV LED. More details are provide in: S. Wang *et al*. Nano Energy. **66** 104181 (2019).

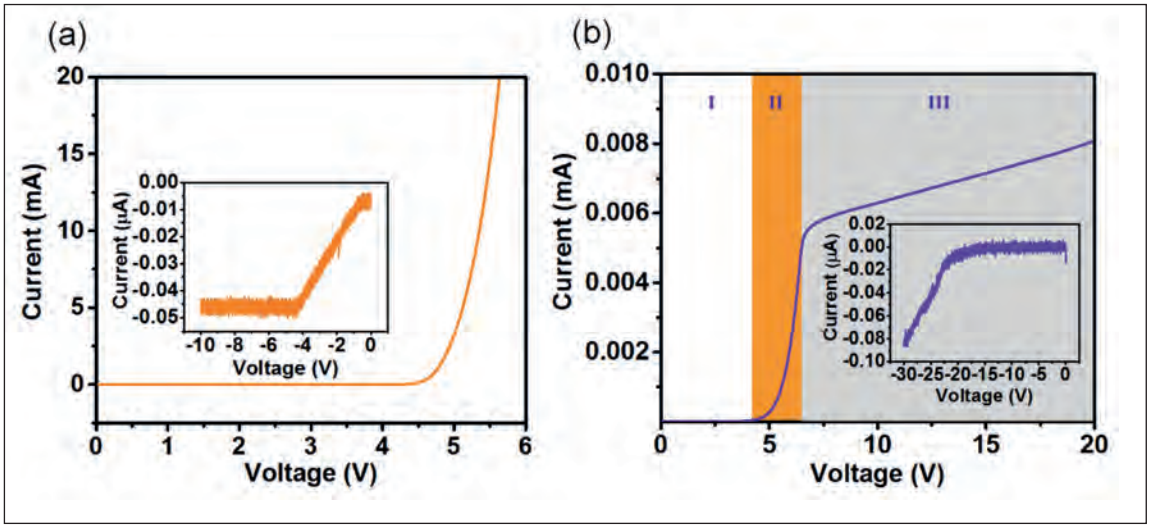


Figure 8. Current-voltage characteristics of (a) a conventional deep UV LED (C-DUV LED) and (b) a multiplicative photoelectric converter deep UV LED (MPC-DUV LED). Insets show the reverse bias conditions. For region I and II, the curve is similar to that of the C-DUV LED, however, the current level is almost three magnitudes lower. For region III, which begins at 6.6 V, the current tendency changes abruptly, indicating minority carriers are effectively suppressed by the space charge region in the *p-i-n* GaN structure, and that the overall current may be limited by the reverse drift current. It may be attributed to the increase in the series resistance of the *p-i-n* GaN structure compared to region II. For more details please see: S. Wang *et al*. Nano Energy. **66** 104181 (2019).

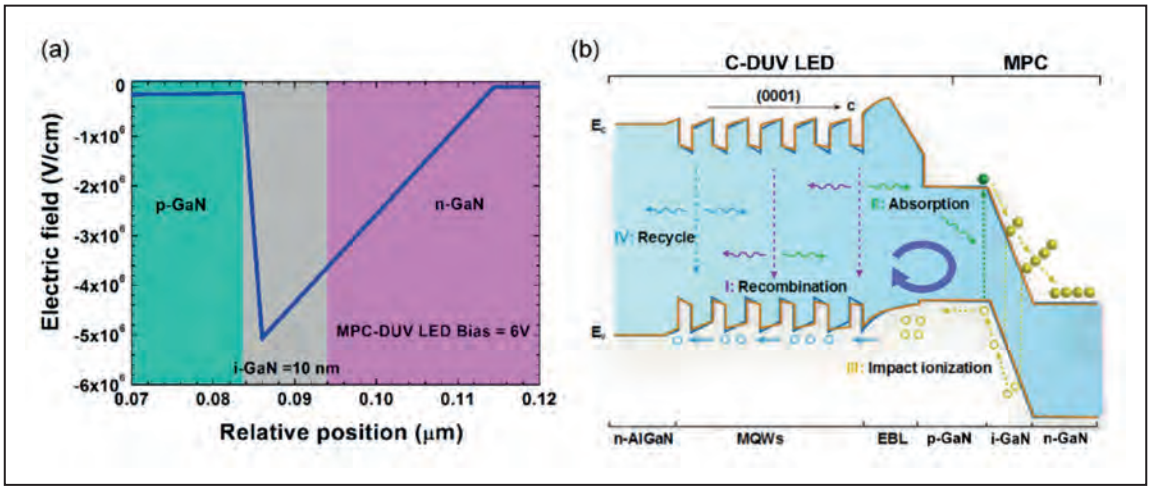


Figure 9. (a) Electric field profile across the multiplicative photoelectric converter (MPC) structure in the MPC-deep UV LED at a 6 V bias. (b) The photon recycling, gain and output process for the MPC-DUV LED. In the initial recombination process I, half of the DUV photons propagate to the *n*-AlGaN layer and escape successfully, as shown by the purple arrows. The other half of the DUV photons propagate towards the MPC structure, and almost all are absorbed by the *i*-GaN layer of the MPC structure, indicated by the green arrows. DUV photons are absorbed and generate new electron-hole pairs, as shown in process II. In process III, carriers are multiplied under Geiger mode, and collide with other atoms, ionising more carriers. The multiplied holes are re-injected into the multi-quantum wells (MQWs), and contribute to new radiative recombination, as shown in process IV. Note that for conventional DUV LEDs, only steps I and II take place. More details are provided in: S. Wang *et al*. Nano Energy. **66** 104181 (2019).

Further reading

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Ren *et al.* J. Phys. D Appl. Phys. **53** 073002 (2020)
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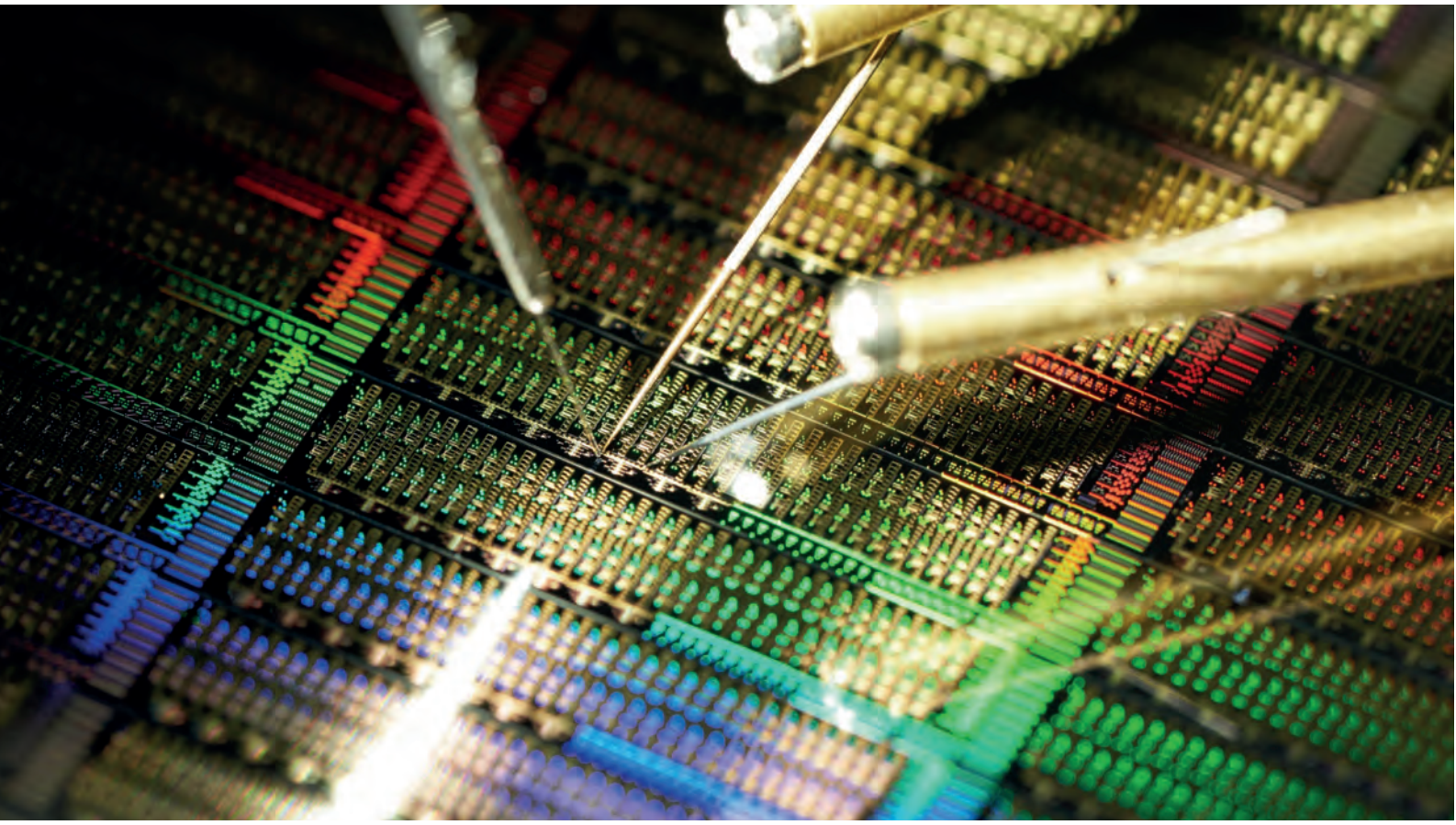


Comb lasers advance high-performance computers

By tackling a bottleneck in bandwidth, multi-wavelength quantum dot lasers are enabling improvements in high-performance computers

BY GEZA KURCZVEIL, DI LIANG AND RAY BEAUSOLEIL FROM HEWLETT PACKARD ENTERPRISE

GROWTH IN DATA is occurring at a phenomenal rate. Now it takes just two years to produce 90 percent of all the data on the internet. That has major implications, particularly as it comes at a time when the performance of single cores has stagnated (see Figure 1 (a)).

To make headway, efforts are no longer directed at trying to increase the clock speed of single cores, but are focused on the construction of processors with more and more interconnected cores, and limited private memory on one socket. This new architecture makes much sense, given that memory is cheap, the opposite of what it was when the first computers were being built. In future, high-performance computers will feature a massive pool of memory at the centre, surrounded by many compute nodes located at the periphery, with all nodes having access to the full memory pool (see Figure 1 (b)).

A key requirement for this new high-performance computer architecture is a massive communication link for the massive pool of memory. Without this, there would be insufficient throughput of data between memory and compute nodes.

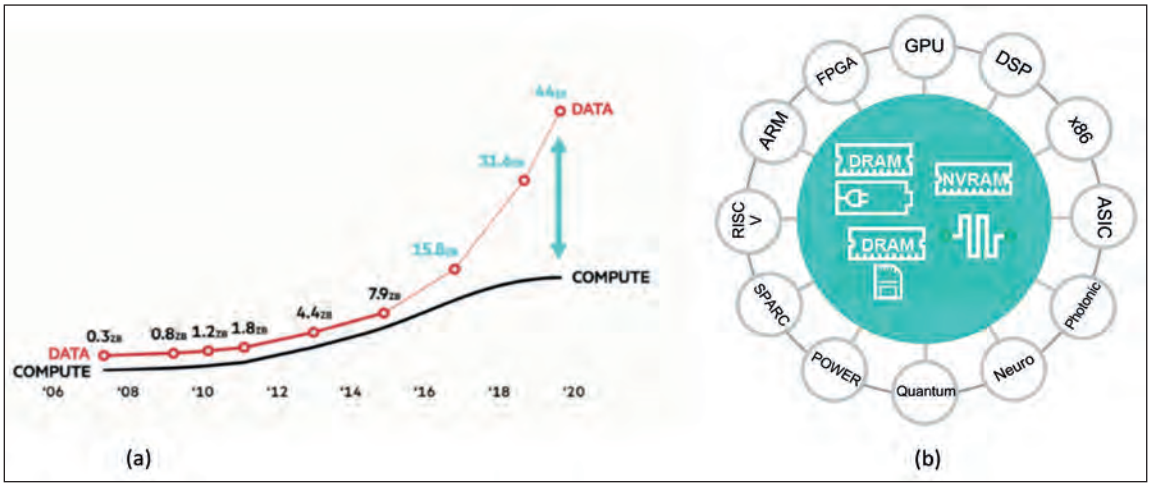


Figure 1. (a) While memory has gotten cheaper over time and there has been an exponential rise in the generation of data, single-thread performance has stagnated. (b) In memory-driven computing a massive pool of memory is at the centre of the architecture, and application-specific compute nodes are placed at the periphery. Each compute node has access to the full memory pool.

One option for the data link is electronic interconnects, such as copper wires. However, they suffer from significant losses, high power consumption, and cross-talk at higher frequencies. A far better alternative is optical interconnects, which address all the weaknesses of wires while allowing the transmission of multiple wavelengths. Data can be transmitted through these links using a technology known as wavelength division multiplexing, which avoids any crosstalk between channels. It is a well-established approach for routing internet traffic when distances and bandwidths are large enough to justify the cost – and as deployment has increased, prices have fallen, making these links common-place in applications where distances are on the order of just a metre. As that's a length scale found in high-performance computing, optical links are already used for rack-to-rack connections.

High-performance computers require aggregated data rates of terabits per second. Today, this rate is out of the reach of a single laser, so the aggregated data rate is sliced up between many lasers, each making an equal contribution. Although individual lasers can transmit at above 200 Gbit/s, data rates of only up to 20 Gbit/s are actually used, to minimise energy consumption.

A common approach for operating these lasers is amplitude modulation. But this has a downside, producing sidebands above and below the original optical carrier wavelength (see Figure 1 (c)). Due to this, the sidebands of one channel have to be sufficiently separated from those of the neighbouring channels to minimise crosstalk. When driving a laser with amplitude modulation at a data rate of 50 Gbit/s,

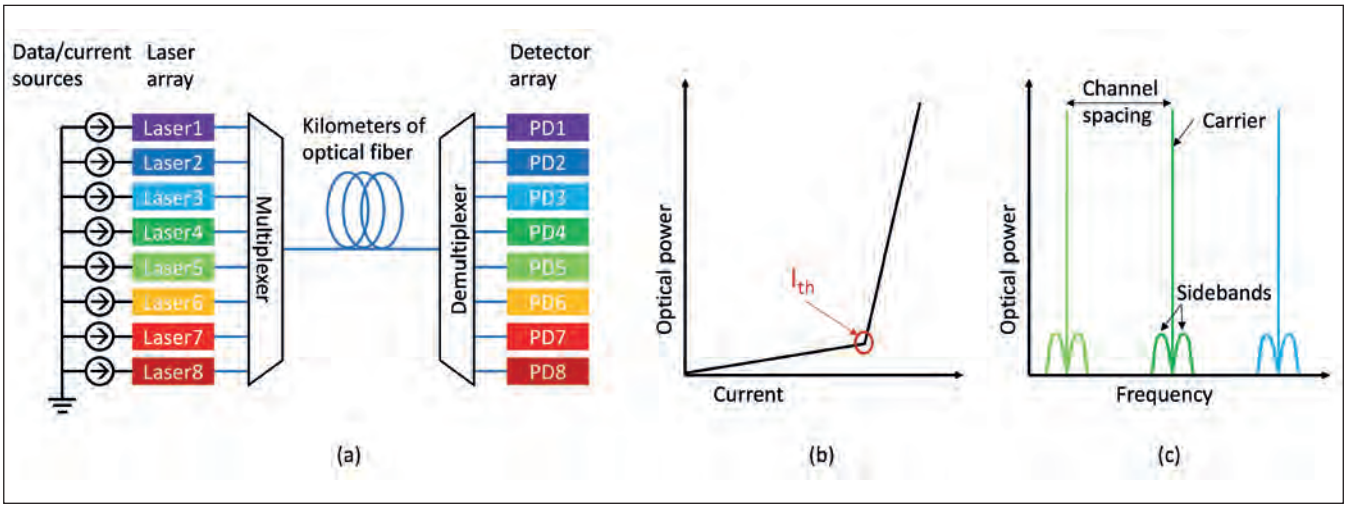


Figure 2. (a) A typical optical link consisting of several single-wavelength lasers. Data are encoded on the optical signal by turning each laser on and off. (b) The output power of a laser as a function of injection current. Once data are encoded onto a laser signal, sidebands are generated. As long as the sidebands of neighbouring channels do not overlap, there is no crosstalk between channels. This is accomplished by limiting the modulation speed.

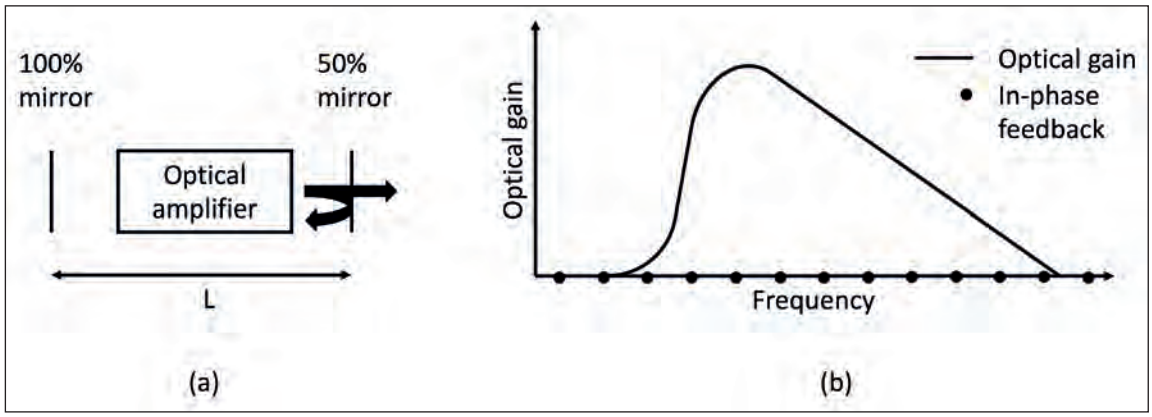


Figure 3. (a) A basic laser cavity contains an optical gain amplifier, surrounded by a pair of mirrors. (b) Lasing occurs at frequencies where light experiences a positive net gain and the feedback from the mirrors is in phase with the light in the cavity.

there needs to be a 3.5 THz channel spacing to minimise crosstalk.

To transmit data using wavelength-division multiplexing, signals from a number of lasers are united by an optical multiplexer, routed through a fibre, and sent to a demultiplexer that returns the data back to a collection of signals at different wavelengths. Photodetectors then convert all of these signals into electrical signals, which is the form required by today's processors and memory. Note that this scheme, which works very well, is particularly attractive for links with low-to-medium volumes of traffic, because it allows unused channels to be turned off, saving power.

Unfortunately, wavelength-division multiplexing is not easy. There are often imperfections in the laser production process, resulting in variations in the lasing wavelength. Addressing this requires active monitoring and tuning. If there are many channels, and the spacing is below 100 GHz – this is the case in dense wavelength division multiplexing – variations in wavelength can create significant problems. In such situations, rather than using many single-wavelength lasers, it is better to use one laser that provide multiple wavelengths – a comb laser.

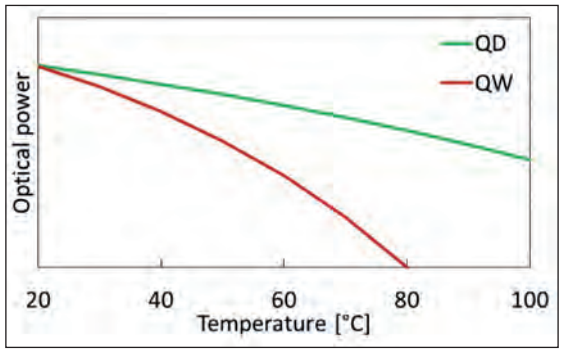


Figure 4. As the temperature of the laser junction increases, optical output power decreases. Due to the three-dimensional confinement of electrical carriers, the power drop in quantum-dot lasers is far smaller than in traditional quantum-well lasers. This makes quantum-dot lasers especially attractive for applications where temperature control is impossible or limited.

Comb credentials

A key difference between a conventional, single-wavelength laser and that with a multiple wavelength comb is the reflectivity of the mirrors. Conventional lasers need an additional bandpass filter inside the cavity – or at least a narrow-band mirror – to ensure single-wavelength lasing, while comb lasers employ a more straightforward design, tending to consist of a long cavity and broadband mirrors (see Figure 3(a)). For cleaved lasers, which can be formed with cleaved facets, the cavity can be 0.5 mm or longer, depending on the desired channel spacing.

With a comb laser, the spacing between the lines is fixed. Although changes in temperature shift the entire comb to either higher or lower wavelengths, once one knows the wavelength of one of the comb lines, one knows the wavelengths of them all. That's because the channel spacing is determined lithographically, and it is therefore a prescribed, controllable design parameter.

Given the great simplicity of the design of the comb laser, one may wonder why anyone would ever go to the trouble of making a single-wavelength laser. The reason is that when a comb laser is built with the most commonly used optical gain medium – a stack of quantum wells – this device is impaired by an intrinsic material property known as mode partition noise. This impediment produces random fluctuations in optical power for every comb line. Although these fluctuations, occurring on a nano-second timescale, do not alter the total optical power, they are a show-stopper for error-free data transmission. That's because it is not possible to transmit an optical 'one' while the power of a comb line has randomly dropped to zero.

So why have comb lasers suddenly risen in popularity, given these issues? Ironically, the recent success has nothing to do with comb lasers. Instead, progress has been driven by the development of a relatively new gain medium, quantum dots. Researchers in Japan pioneered these low-dimensional structures, developing a laser with greater tolerance to temperature variations. By switching from wells to dots they were able to increase the confinement of electrical carriers, with early experimental work verifying an increase in high-temperature gain stability

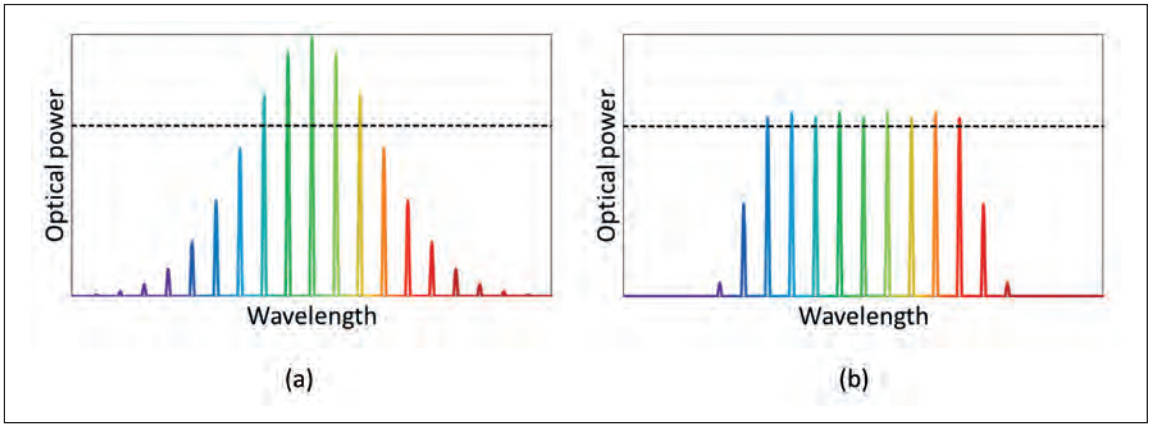


Figure 5. (a) Some comb lasers exhibit a Gaussian distribution of amplitudes. The dashed line indicates a hypothetical power level for noise-free data transmission. Comb lines with less power cannot be used, so they reduce the device efficiency. (b) Quantum-dot-based comb lasers produce a more rectangular optical spectrum. This device has the same total power as the one in (a). Note that more channels satisfy the power requirement for noise-free data transmission.

(see Figure 4). After this success, it took a few more years until a collaboration between researchers in Germany and Russia investigated the topic of mode partition noise in quantum dot comb lasers. This work revealed that the introduction of dots quashed the partition noise in these devices.

Not all comb lasers are created equally. Some are more practical than others for data communication, because they combine a low mode partition noise with a flat comb that ensures that all channels have similar signal-to-noise ratios. Poor candidates for high-performance computing include lasers with frequency combs generated in SiN resonators, as they show a Gaussian distribution of comb line amplitudes (see Figure 5 (a)). The good news, for reason yet to be understood, is that the combs from quantum-dot lasers produce flat spectra with a relatively uniform power over a large number of comb lines (see Figure 5 (b)). However, not all comb lasers are suitable, as there are problems with pulsed variants (for details see the box "The problems of pulsed comb lasers").
Encoding independent data streams on each comb line is not as straightforward as for a single-wavelength laser. Turning the laser on and off by modulating its injection current encodes the same data stream on all the comb lines, which is inefficient.

Instead, our team at Hewlett Packard Enterprise has the comb laser on at all times (see Figure 6) and places several micro-ring modulators outside of the laser – we have one for each comb line (see Figure 7 (a)). This approach exploits a key characteristics of micro-ring modulators, a wavelength dependent loss (see Figure 7 (b)). By adjusting the voltage of the *p-n* junction of the micro-ring, we shift the wavelength of maximum loss, which is the resonance wavelength. To generate an optical 'one', we tune the resonance wavelength away from the comb line; and to produce a 'zero', we line-up the resonance wavelength with the comb line.

Our micro-ring modulators are compact, with a diameter of around 10 μm. With proper design, they can transmit data at 50 Gbit/s. The full-width-half-maximum of the micro-ring's resonance is ideal, being wide enough to capture an entire comb line, but narrow enough to allow neighbouring comb lines to be transmitted without any loss in optical power. Selecting the resonance wavelength of the micro-ring is relatively easy, as it can be tuned by adjusting the

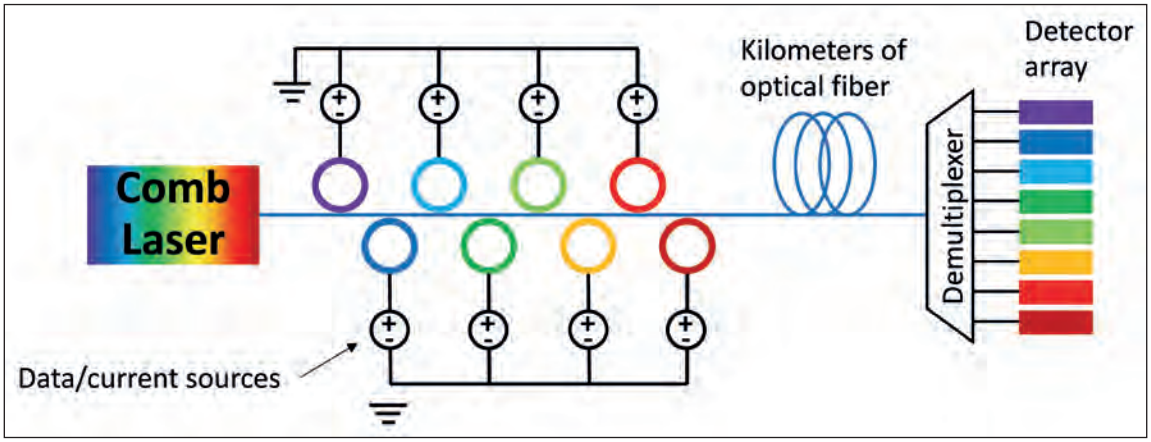


Figure 6. An optical link based on a comb laser. Rather than directly modulating the laser, external modulators are used to encode data on individual comb lines.

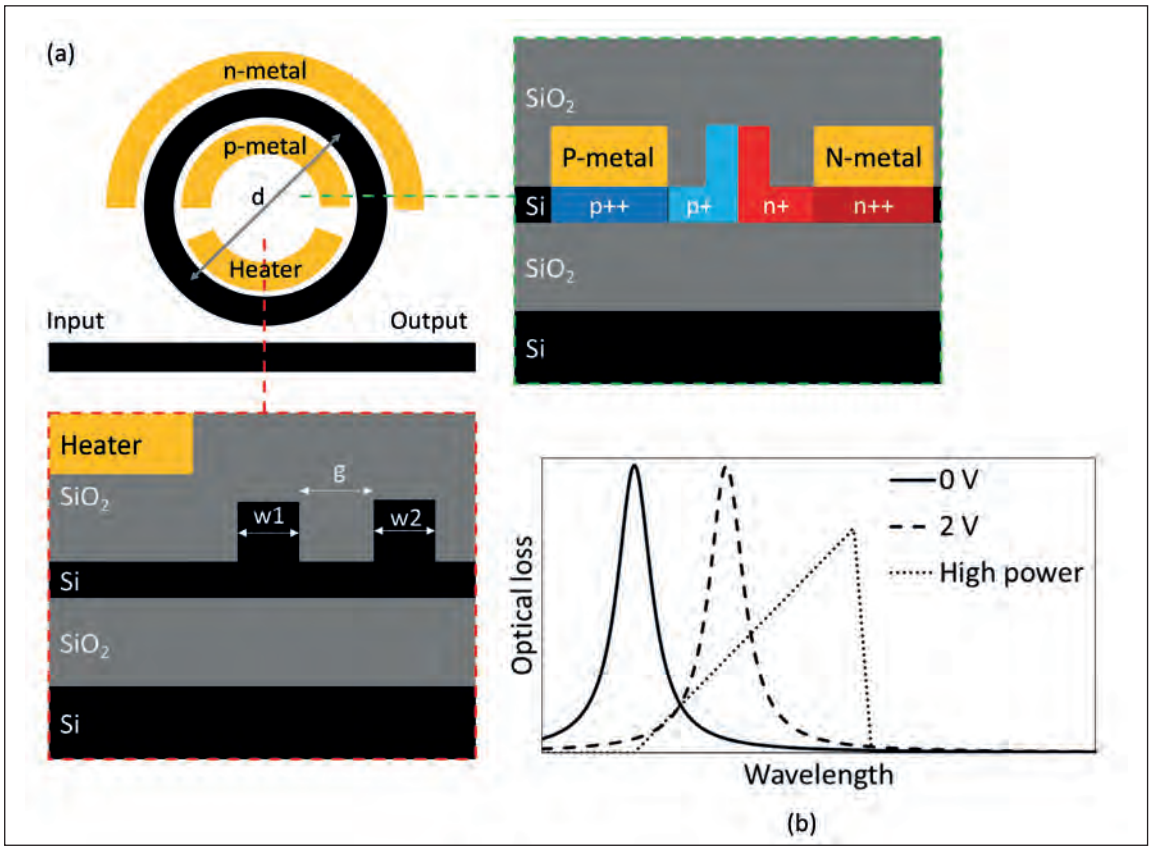


Figure 7. (a) Top-down and cross-sectional diagrams of a micro-ring modulator. (a) The wavelength-dependent loss of a ring modulator has a resonance that can be engineered using parameters *d*, *g*, *w1*, and *w2* in (a). In addition, it can be tuned using a power-hungry heater. Data are encoded by applying a voltage across the *p-n* junction. (b) The shape of the modulator's resonance becomes highly distorted at high optical powers, making pulsed lasers less desirable as a light source.

diameter of the ring, its inner width, and its thickness. One of the constraints of micro-ring modulators is that they impose a limit on optical power. If it is too high, non-linearities degrade the contrast of the resonance, and in turn lower the signal-to-noise ratio of the encoded data (see Figure 7 (b)). Due to this restriction, it is far better to operate comb lasers with a constant optical power. Fortunately, that's a great operating regime for this class of laser, thanks to its gain recovery characteristics.

There will always be a shift in the lasing wavelength of the comb laser, even if the micro-ring is perfect. What's needed is some form of tuning or tracking to maintain a line-up between the ring's resonance wavelengths and the temperature-shifted comb lines. One option is to apply a voltage to the *p-n* junction, but this results in excess optical loss, in the form of free-carrier loss.

The common way to avoid this is to use a resistive heater to locally change the ring's temperature. In turn, this shifts the refractive index of the cavity, and can deliver large changes to the resonance wavelength. However, resistive heaters are wasteful, requiring up to tens of milliwatts to shift the wavelength by just a nanometre. We prefer a more energy-efficient approach, using a capacitor to tune the resonance wavelength. With our design, a layer of semiconductor material is placed on top of the micro-ring, and inserted between is a 20 nm-thick layer of dielectric, such as SiO_2 or Al_2O_3 (see Figure 8). Electrodes are added to the silicon and the semiconductor to form a metal-oxide-semiconductor capacitor. When a voltage is applied to this device, sufficient electrons and holes accumulate at the dielectric interfaces to produce a change in the refractive index of the micro-ring, and its resonance wavelength. As the current flowing through the capacitor is incredibly small – it is only around 100 fA – the resulting tuning is 10^{-9} mW/nm, giving an increase in efficiency of nine orders of magnitude compared with a resistive heater.

To manufacture these comb lasers in high volume, using a high yield, low-cost process, they must be integrated on silicon substrates. Our short-term solution is to take GaAs-based epitaxial wafers, which contain our quantum dot structures, and use a molecular bonding technique to attach them to silicon-on-insulator wafers. We then selectively remove the GaAs substrate to leave a 1-2 μm-thick epitaxial stack on silicon, and process this material in the same way that is used to produce conventional GaAs lasers. However, we have the benefit of using much larger, stronger wafers.

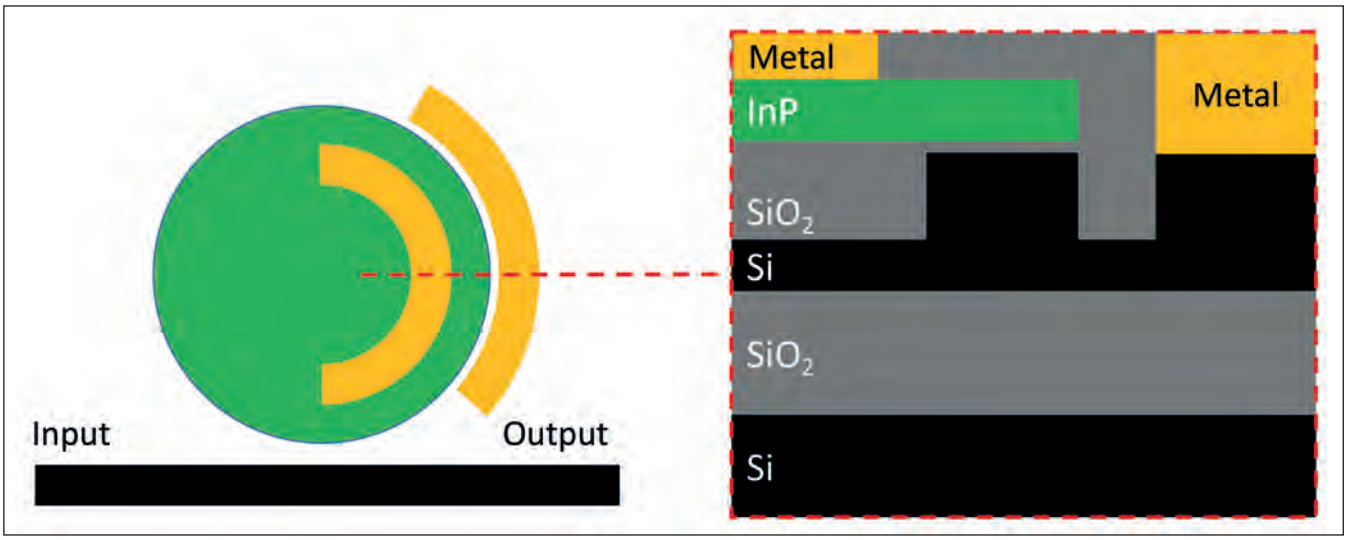


Figure 8. A MOS tuner provides much more efficient resonance tuning than a thermal tuner. When a voltage is applied to the contacts, charges accumulate at the SiO_2 layer, which is between the silicon and the InP. Charge accumulation is sufficient to change the refractive index and thus the resonance wavelength. However, since no current flows through the capacitor, power consumption is negligible.

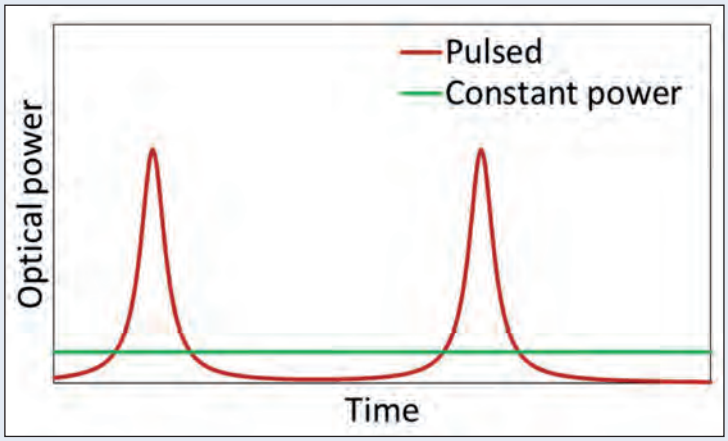
A great strength of this process is that the silicon layer in these lasers provides both a mechanical substrate and an optical waveguide (see Figure 9 (a)). Silicon is ideal for waveguiding – it has a far lower optical loss than those made with GaAs or InP systems, and it allows us to make: high quality laser mirrors; MOS tuners for near zero-power tuning; and vertical grating couplers, which allow rapid, wafer-level device testing. With this approach we have fabricated comb lasers operating up to 100 °C (see Figure 9 (c)), and variants that provide 14 channels for error-free, high-speed modulation (see Figure 9 (d) and (e)).

Longer term, our plan is to produce comb lasers by growing quantum-dot-containing layers directly on silicon. This is far from easy, due to the large lattice mismatch between silicon and GaAs. Left unchecked, this results in a high density of defects that drag down device reliability, and can even kill lasing operation in an instant. Some groups have turned to thick buffer layers to reduce the strain in the quantum dot layers, but this hampers efficient coupling of light from the quantum dot layers to the silicon. Due to this, teams that have made devices that are based on direct growth of quantum dots on silicon have only used silicon as a mechanical carrier.

While comb lasers are very attractive, we are not advocating their use in every optical link. Since all channels in a comb laser are always on, comb lasers are only attractive for dense wavelength division multiplexing links that have a high volume of traffic at all times. Use a comb laser with many channels in a link with little traffic, and lots of power will be wasted by the unused channels, because they cannot be turned off. For links with low and medium levels of traffic, using an array of single-wavelength lasers may offer a more energy efficient solution.

The problems of pulsed comb lasers

WHEN COMB LASERS produce a pulsed output, or are temporally modelocked, the average optical output power is constant, but the energy of one period is compressed (see figure below). This can cause two problems. One potential issue is that the higher instantaneous power, contained in pulses typically as short as 2 ps, accelerates device failure, such as catastrophic optical mirror damage. This is particularly problematic in comb lasers, as a failure impacts all channels. The second issue is that the high output power of the peaks impairs the contrast of the resonance, and ultimately reduces the signal-to-noise ratio of the encoded data.



Pulsed lasers are a form of comb laser that emit periodic pulses. The two devices shown here have the same average power, but the pulsed laser has a much higher peak power than the constant-power laser. The presence of pulses can have unwanted consequences such as reduced laser reliability and reduced signal-to-noise ratio of the encoded optical data.

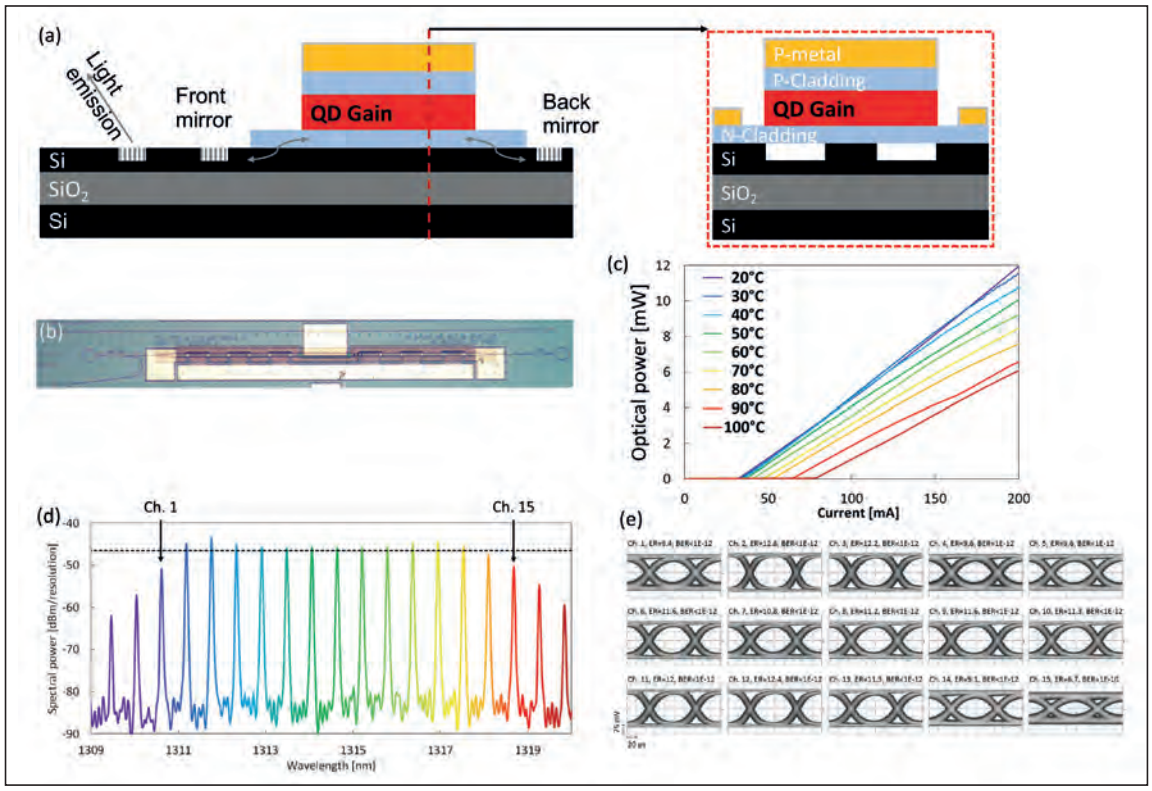


Figure 9. (a, b) Cross-sectional diagrams of a quantum-dot comb laser on a silicon-on-insulator substrate. Thin epitaxial layers between the top silicon and the quantum-dot gain allow efficient transfer of light between them. (b) Top-down photograph of a fabricated comb laser on silicon using wafer bonding. (c) Optical output power as a function of current and temperature showing excellent high-temperature performance. (d) Optical spectrum of a comb laser showing multiple comb lines with a quasi-rectangular shape. 12 comb lines within 3 dB of the peak (dashed line) are observed. (e) Eye-diagrams and bit-error-ratios (using an external modulator) showing error-free performance in 14 of the 15 channels that were measured (the bit error rate is no more than 10^{-12}).

There are two remaining challenges to overcome before comb lasers are ready to light up the next generation of high-performance computers. The first of these is device reliability. Since all channels are created in one laser, when a device fails, it impacts all channels. One way to partly offset this risk is redundancy.

The second challenge is to devise an effective approach to increasing the number of channels. Although the spacing between the channel is inversely proportional to the length of the laser, making a laser longer is not a recipe for success. What happens is that as the channel spacing gets narrower, the individual channel rate has to be reduced to maintain a low cross-talk between the channels. The upshot is that there is no increase in the aggregated bandwidth.

A more promising solution is to increase the width of the optical window for the comb lines. The upper limit for this is determined by the gain bandwidth of the optical amplifier, which is typically 50 nm wide. Through engineering, this has the potential to be increased to more than 100 nm. However, even for 'regular' optical amplifiers with a 50 nm gain bandwidth, the combs that result are typically just 15 nm wide. At present, the reason for this is unclear, but several hypotheses have been suggested.

One possible explanation is spatial hole burning, and another is group velocity dispersion – that there is imperfect mode spacing of a comb, resulting from a wavelength-dependent refractive index. If either of these are the cause, they can be addressed by engineering. Analytical models are being developed to help understand the impact of these phenomena, and experiments are underway to verify the models. When success follows, we shall be a step closer to implementing the efficient, high-speed optical links required to maintain progress in high-performance computing.

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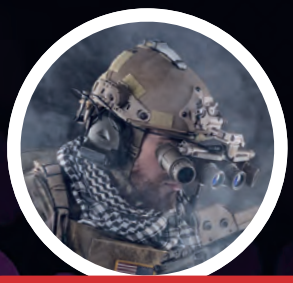


Infrared

Solar

CMOS++

Power

Uniting III-Vs with silicon for **beyond-5G front-end modules**

Combining aspect ratio trapping with nano-ridge engineering enables 300 mm substrates to provide a platform for the fabrication of GaAs/InGaP HBTs that deliver amplification in the millimetre-wave

BY ABHITOSH VAIS FROM IMEC

FOR THE FIRST FOUR GENERATIONS of mobile communication technology, changes to the transmission frequencies have been evolutionary, rather than revolutionary. The operating frequency has moved up from just below a gigahertz to several gigahertz and the bandwidth has widened from tens of kilohertz to tens of megahertz.

Viewed in these terms, 5G is a radical departure from what has come before (see Figure 1). It will still involve some transmission at a few gigahertz – known as the sub-6 GHz bands – but in addition, it will use millimetre-wave frequencies, which are needed to address the bandwidth limitations at current frequency bands.

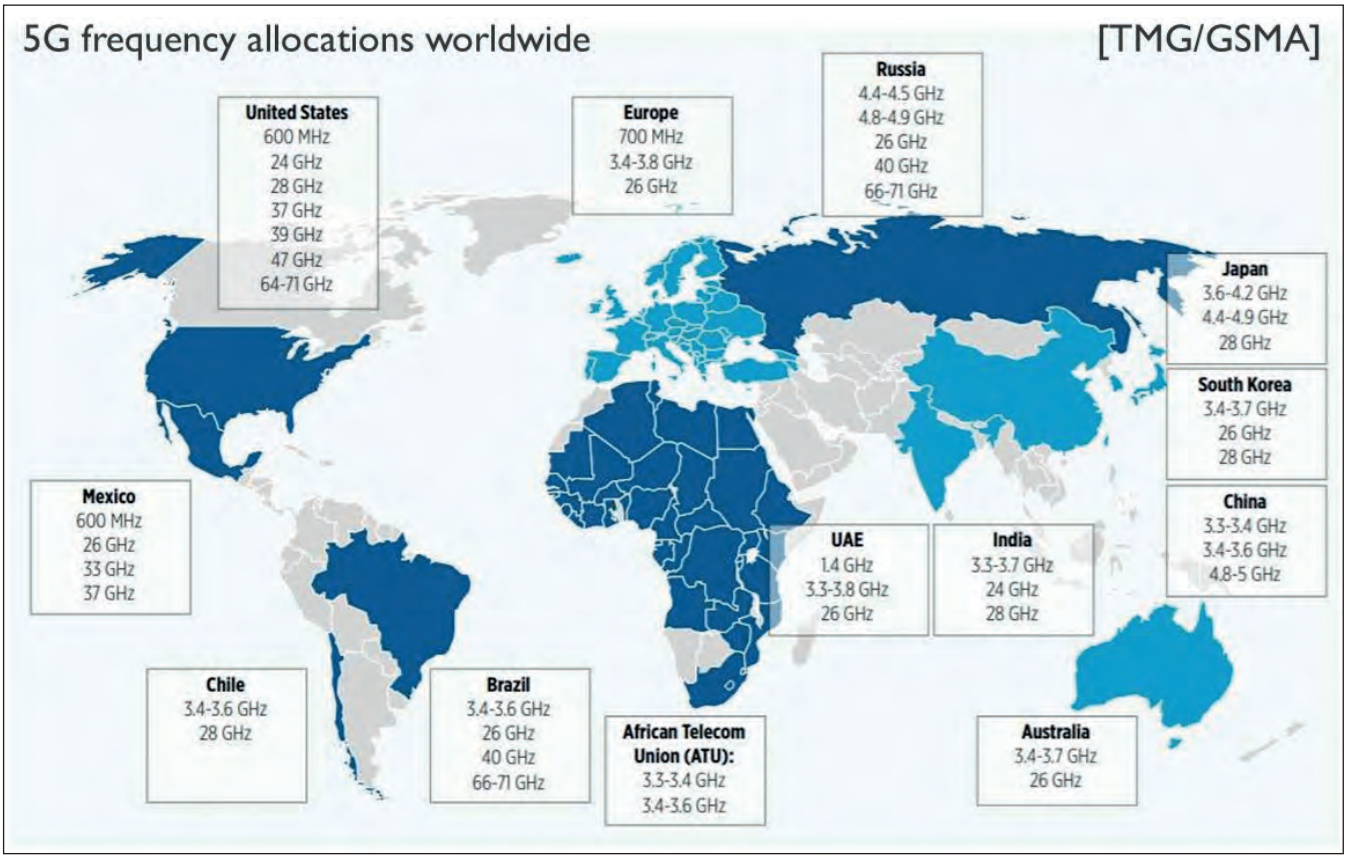


Figure 1. Frequency band allocations for 5G deployments across the world. [TMG/GSMA], https://www.gsma.com/spectrum/wp-content/uploads/2019/10/mmWave-5G-benefits.pdf

One of the downsides of using bands in the millimetre wave, such as those centred around 28 GHz and 39 GHz, is that they suffer from far greater attenuation. To address this, there needs to be an introduction of a network of small cells, as well as new designs for the handset, leading to an increased complexity in the front-end design.

A key ingredient in today's handsets is the GaAs/InGaP HBT, fabricated on expensive GaAs substrates. This class of transistor is used to make power amplifiers, which feature in separate modules, each covering a different frequency band.

As 5G operating in the millimetre-wave domain is rolled out, the RF performance from these transistors must be maintained or even improved while lowering cost, increasing the flexibility in circuit design, and trimming power losses and the chip footprint. Unfortunately, existing commercial technologies are struggling to satisfy all these requirements for enabling a good RF front-end module, so there is a need to turn to innovative materials and device architectures.

At imec, we have developed a hybrid III-V/CMOS technology that promises to deliver the low form factor and low costs required for millimetre-wave RF applications. It harnesses the power handling (see Figure 2) and the linearity at high frequencies associated with III-V systems, while drawing on advanced CMOS back-end-of-line processes for the creation of complex control circuitry. What's more, thanks to co-integration, there is the potential for improved energy efficiency for the overall circuit, leading to a power-efficient, low-cost millimetre-wave technology that could be produced in high volume.

One of the biggest challenges in uniting III-V materials, such as GaAs, with silicon is the large lattice mismatch. Epitaxial growth on a lattice-mismatched substrate leads to generation of defects – mainly threading dislocations. These imperfections induce an unwanted leakage current, degrading device performance.

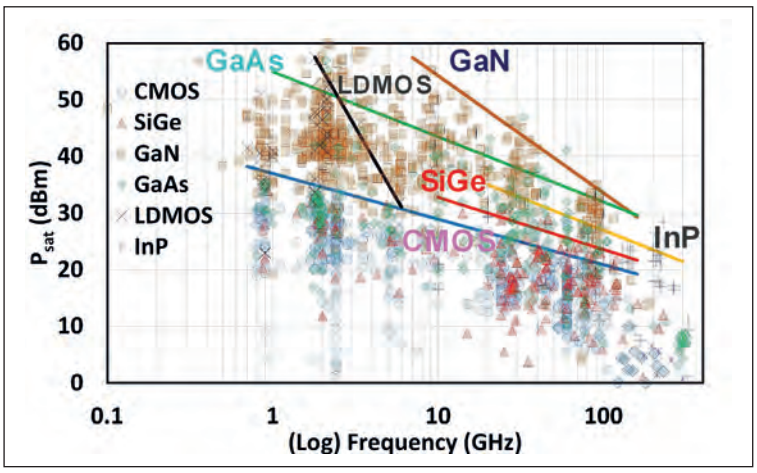


Figure 2. Technological trends in output power, P_{sat}, for different technologies with respect to operating frequencies. Solid lines are only to guide the eyes. [H. Wang, *et al*., "Power Amplifiers Performance Survey 2000-Present," [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html]

Some research teams have tried to lower the density of these defects by inserting a strain-relaxed buffer layer between the substrate and the device. However, there is a significant additional cost associated with adding layers of either SiGe, germanium or a III-V metamorphic stack that needs to be more than 10 μm-thick to reduce defect density to an acceptable value.

Whatever approach is used to create a CMOS/III-V technology, it must include standard silicon substrates to keep complexity and cost in check.

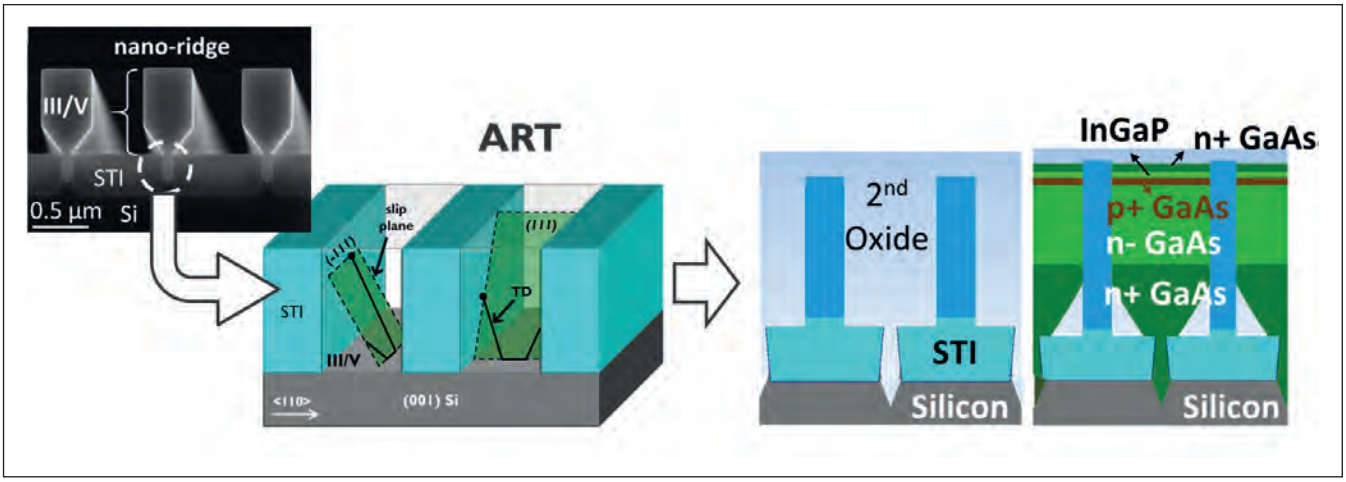


Figure 3. An illustration of the features of aspect ratio trapping (ART) and nano-ridge engineering to grow nano-ridges. Note that due to ART, the threading dislocations are trapped inside the narrow trench while a relatively defect-free nano-ridge is grown inside the second oxide.

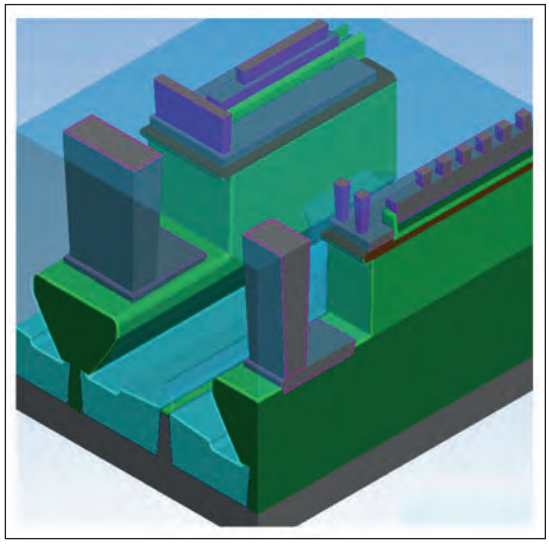


Figure 4. III-V HBTs can be integrated on a 300 mm silicon wafer using a CMOS-compatible process flow developed at imec.

Aspect ratio trapping

Our approach combines aspect ratio trapping, where defects are confined to the bottom of narrow trenches, with nano-ridge engineering, which leads to an increased, defect-free III-V volume that can be used to fabricate devices (see Figure 3). Further processing of the nano-ridges, using a fully CMOS compatible flow, creates the final device (see Figure 4), and ultimately enables co-integration with silicon CMOS devices.

One of the strengths of this approach is that it enables the integration of silicon substrates and III-V materials without having to grow thick buffer layers or to turn to expensive substrates. In addition, we can draw on our expertise on III-V-on-300 mm silicon – developed in the context of CMOS scaling and silicon CMOS.

We produce our nano-ridges by growing III-Vs on 300 mm silicon (001) wafers with a double-oxide structure (see Figure 4). The first SiO_2 layer is a 400 nm-thick shallow trench isolation (STI) template.

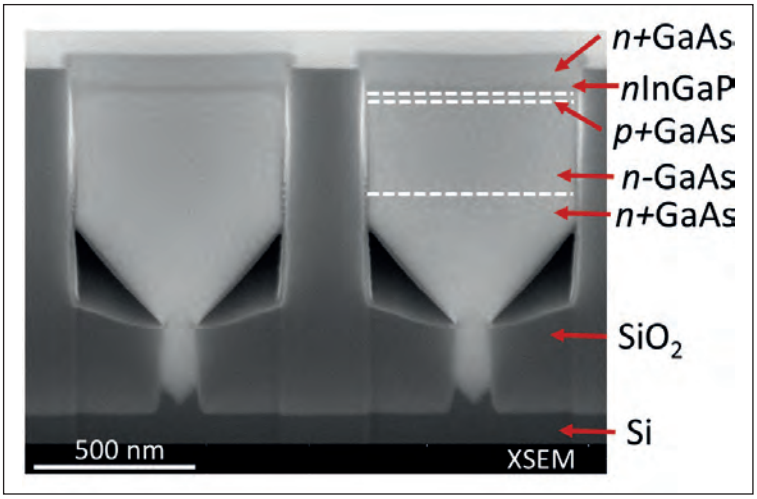


Figure 5. Cross-section scanning electron micrograph (XSEM) of the GaAs/InGaP nano-ridges grown on a 300 mm silicon substrate using nano-ridge engineering. Notice the absence of defects inside the active device stack.

This features a pattern of narrow trenches that are 80 nm wide, and have a silicon {111}-faceted V-groove at the bottom. The pitch is 800 nm. On this we add a second oxide layer, which is 1000 nm-thick. Processing this creates 600 nm-wide trenches, centred on the narrow trenches below.

Using selective-area growth, we deposit III-V material in the narrow trenches. The large lattice mismatch between silicon and the III-Vs leads to the generation of defects, but they are confined to the bottom of this trench, thanks to its high aspect ratio. This ensures that the material growing out from the narrow trench is free from threading dislocations.

Our next step is to turn to nano-ridge engineering to widen the nano-ridge, so that a (001) growth facet can be maintained, enabling a flat interface. If nano-ridge engineering is allowed to grow a free-standing structure, a large box-like shape results. We avoid this by adding a second oxide template. Once the nano-ridge reaches the second oxide, sidewall deposition is reduced in the device's active region.

Growth of the III-Vs on the processed 300 mm silicon wafers takes place in a low-pressure MOCVD chamber using standard liquid precursors for the group III and group V sources. Doping is realised with the addition of carbon tetrabromide and silane.

Note that as well as being able to produce traditional box-like growth of III-Vs on silicon, nano-ridge engineering can yield different shapes by carefully adjusting the growth conditions. This allows good control of the nano-ridge profile at the nanometre scale.

Defect characterisation

We evaluate the effectiveness of our approach by analysing the defect density in the nano-ridge. One of the most common techniques for scrutinising material is transmission electron microscopy. We have used a form of this known as high-angle annular dark-field scanning. This technique, which can expose defects in the trench, reveals that the III-V device stack is free of misfit dislocations (see Figure 5 and 6). Although the standard form of transmission electron microscopy provides better accuracy in uncovering defects, it has a very small scanning area, making it rather cumbersome for a reliable determination of the defect density.

Another common technique for scrutinising material is electron channeling contrast imaging. It is a relatively fast option for generating a statistically relevant dataset. Using this technique, we have found that the threading dislocation density at the surface of the GaAs nano-ridges is below 3 x 10^6 cm^{-2}. As the value of the defect density is limited by the inspection area, we envisage that the actual threading dislocation density in the GaAs nano-ridges could be even lower than this.

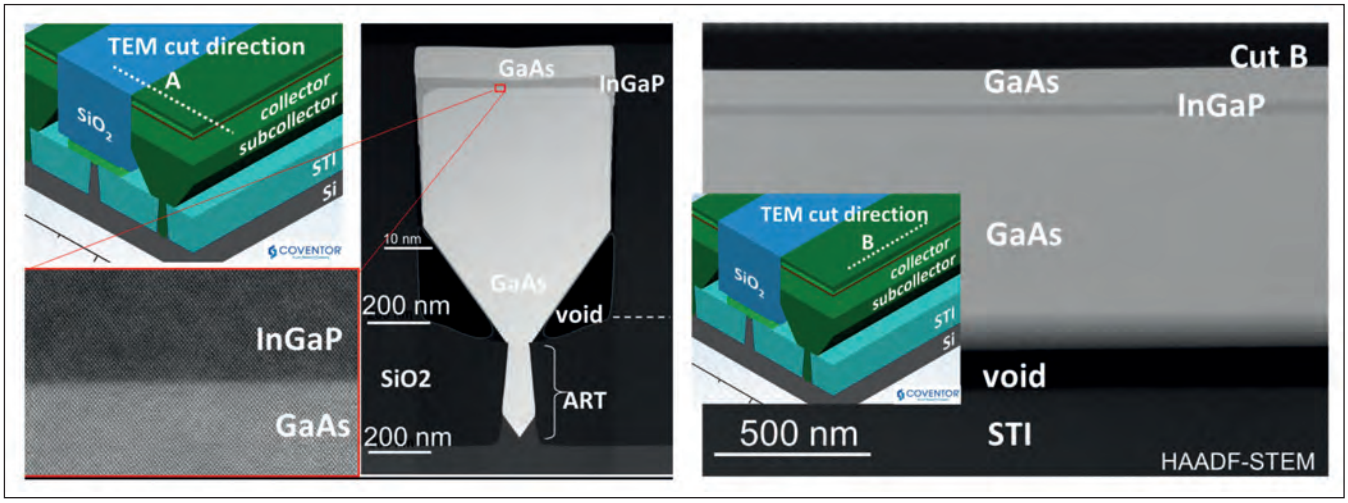


Figure 6. High-angle annular dark-field scanning transmission electron microscopy of the nano-ridge across the width (left) and along the length of the nano-ridge (right).

Based on this finding, we know that the threading dislocation density in our ridges is low enough to prevent it from having a significant impact on our devices.

Epitaxial systems with mismatched lattice constants can also be riddled with planar defects. Our approach traps this form of defect in {111} planes parallel to the sidewalls, but when planar defects run perpendicular to the sidewall there is the possibility of them ending up in the device stack. Here, this density could be between 0.14 μm^{-1} and 0.45 μm^{-1}. The good news, however, is that as planar defects do not involve open crystal bonds or a pronounced strain field, they will have less impact on device performance than dislocation defects.

HBTs on 300 mm silicon

Drawing on our capability to grow defect-free III-V layers on silicon, we have recently demonstrated GaAs/InGaP HBTs that are monolithically integrated on a standard 300 mm silicon substrate. This success provides a stepping-stone towards the fabrication of InGaAs-based devices for beyond-5G applications.

Our breakthrough is based on a stack of *n*-InGaP/*p*-GaAs/*n*-GaAs layers that exhibit HBT characteristics. The emitter-base and base-collector diodes show ideality factors of around 1.2 and 1.4, respectively, highlighting the good quality of these junctions and the materials that form them. Additional evidence of the high material quality of this structure is a DC

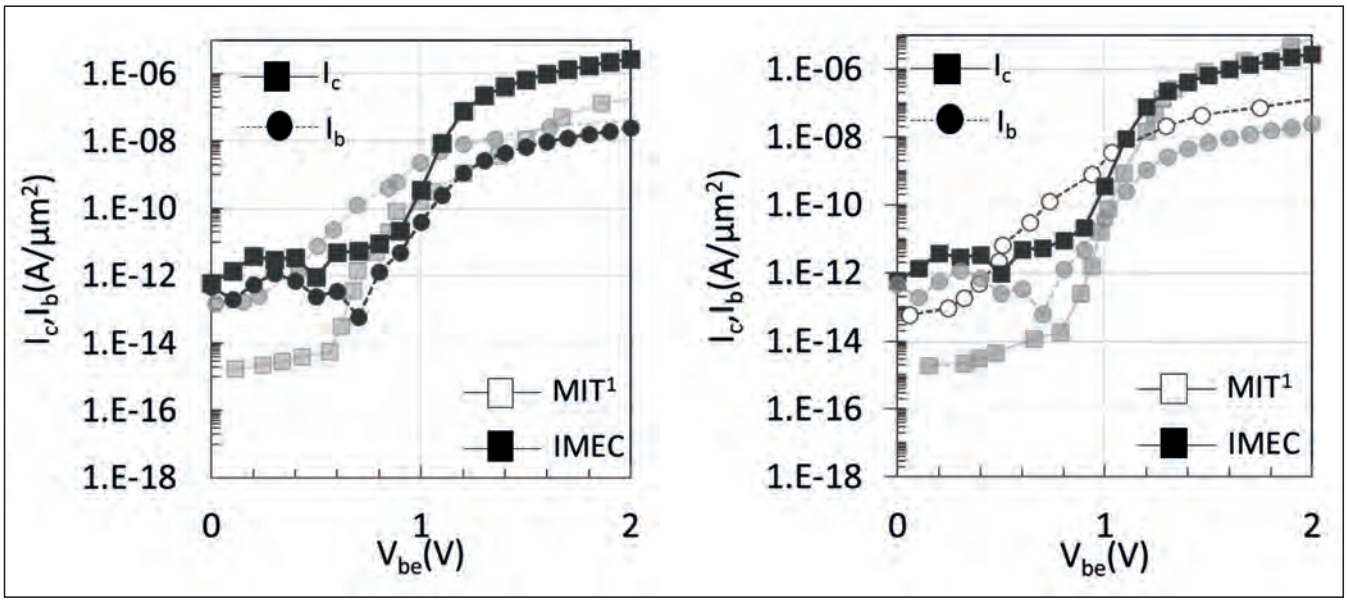


Figure 7. Comparison of electrical characterization (Gummel plots) of the devices fabricated in this work with that of reference devices [1] with strain-relaxed buffer layers (presented at IEDM 2019). [1] C. Heidelberger *et al*. Journal of Applied Physics **123** 161532 (2018).

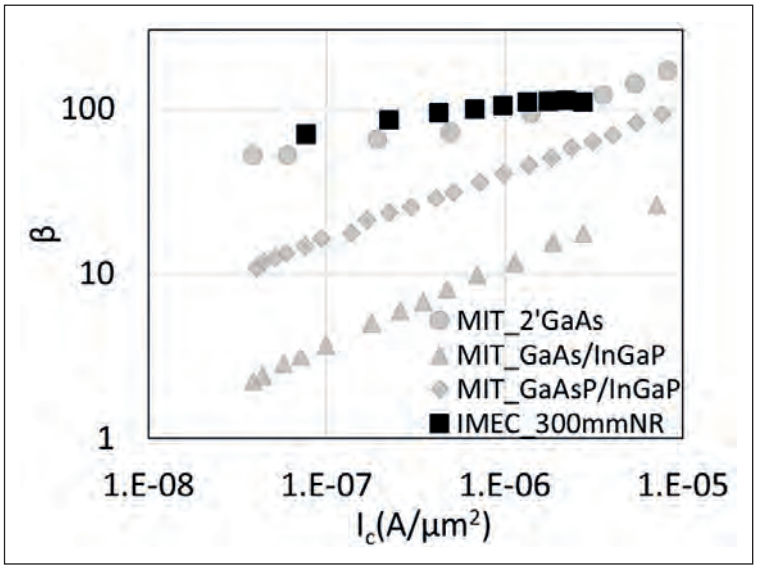


Figure 8. Comparison of DC current gain of the HBT devices fabricated on nano-ridge engineering based GaAs/InGaP stack with that of reference devices [1] with strain relaxed buffer layers (presented at IEDM 2019). [1] C. Heidelberger *x*. Journal of Applied Physics **123** 161532 (2018)

current gain of more than 110 and a breakdown voltage between the collector and base of 10 V.

To benchmark our device, we compared its transfer characteristics with HBTs with a similar design that were formed on a 2-inch GaAs substrate and a thick strain-relaxed buffer layer with similar defect density (see Figure 7). Encouragingly, our device outperforms that made on the thick buffer, and its key traits are very similar to a device made on a high-quality 2-inch GaAs substrate (see Figure 8). This finding supports our claim that the quality of our material produced by nano-ridge engineering on 300 mm silicon is sufficient enough – we don't need thick strain-relaxed buffer layers or expensive substrates.

Thanks to our successes, we have high hopes for our technology. One of its strengths is that it shows how III-Vs and silicon CMOS can combine to serve 5G and millimetre-wave applications. This can be accomplished with InGaAs HBTs on a 300 mm silicon substrate, a combination that could find deployment in RF applications beyond 5G.

We take great heart from the initial performance of our hybrid III-V/CMOS technology, which leads to devices with a comparable performance to those made on high-quality GaAs substrates, and we look forward to further explorations in nano-ridge engineering, to uncover its full potential.

Hybrid growth promises better performing laser diodes

Adding tunnel junctions by remote-plasma CVD will lead to more-powerful, more-efficient GaN lasers

BY JOSH BROWN, BRAD SISKAVICH AND IAN MANN FROM BLUGLASS

THE DEVELOPMENT of high-brightness GaN-based lasers is opening the door to new and exciting applications. This class of lasers is starting to be used for industrial welding, biotech-flow cytometry, displays, and general and automotive lighting. Sales in these sectors are tipped to rocket over the next few years.

To turn the promise of significant commercial success into reality, there has to be an improvement in the optical performance and the energy conversion of these lasers. Efforts need to be directed at extending their spectral range, increasing their power, and boosting their efficiency and brightness.

At BluGlass Limited of Silverwater, Australia, we have a novel technology for addressing many of these challenges – low temperature, ammonia-free GaN deposition. It is a supplementary growth method that is based on remote-plasma CVD and offers laser diode manufacturers performance and cost advantages over the traditional MOCVD-only process. To ensure that this technology has commercial impact, last October we launched a laser diode business for exploiting our unique remote-plasma CVD growth

Layer	Thickness (nm)	Doping (cm^{-3})	Composition	Absorption Coefficient (cm^{-1})	Optical Loss (cm^{-1})
p++ contact	20	1.5E20	GaN	375	0
p-AlGaN cladding	500	1.0E20	$Al_{0.08}Ga_{0.92}N$	250	18.8
p-WG	100	2.0E19	GaN	50	11.9
EBL	12	1.5E20	$Al_{0.2}Ga_{0.8}N$	375	14.7
2x InGaN/GaN MQW	2.7 / 9.0	-5.0E16	$In_{0.11}Ga_{0.89}N$/GaN	12	1.4
n-WG	100	-2.0E17	GaN	12	4.0
n-AlGaN cladding	1000	-3.0E18	$Al_{0.067}Ga_{0.933}N$	12	2.2

platform for the manufacture of high-brightness GaN lasers.

During the growth of laser diodes, remote-plasma CVD offers an 'active-as-grown' buried *p*-GaN technology. It enables the production of high-performance tunnel junctions, without the need for post-growth annealing for the activation of the magnesium acceptors.

Originally, we developed our 'active-as-grown' tunnel junctions for use in LEDs, but now they are being deployed in unique laser diode designs. Our hope is that this technology will help to bridge the substantial gap between the performance of these two optoelectronic devices – in state-of-the-art GaN-based laser diodes, conversion efficiency is still only around 40 percent, compared with nearly 90 percent in GaN-based LEDs.

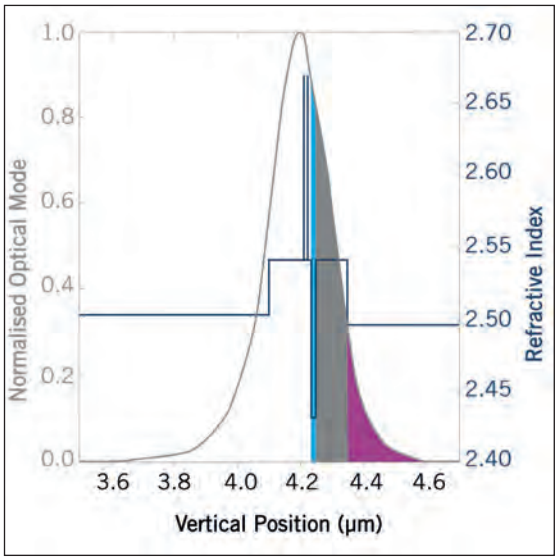


Figure 1. (a) (top) Structure of standard laser diode without a tunnel junction and (b) (left) normalised optical mode and refractive index profile.

The problems of *p*-doping

There are many factors behind this low conversion efficiency for laser diodes. Quite a few relate to the high activation energy of the magnesium acceptor in *p*-type, magnesium-doped layers of GaN and AlGaN. Due to an activation energy of around 170 meV, typically just 1 percent of the magnesium atoms contribute to the free-hole concentration. Consequently, to make viable devices, magnesium doping levels in *p*-type layers have to be cranked up – they are often up to 100 times higher than the silicon doping in *n*-type layers.

Putting so much magnesium in the epilayers is not ideal. It leads to low hole mobilities, high resistivities and a high optical loss – and it ultimately drags down the conversion efficiency of the laser diodes. Optical losses occur in the *p*-side, and are most acute in the *p*-AlGaN cladding layer. To ensure confinement of the optical mode within active region and waveguide layers, this cladding has to have a relatively low refractive index. However, this cannot prevent a fraction of the mode overlapping the *p*-doped, AlGaN layer. As there are high levels of magnesium in this layer, the absorption coefficient is very high – it typically exceeds more than 100 cm^{-1} – and it contributes a significant fraction to the total optical loss in this class of laser.

The *p*-type resistive loss comes from a combination of the series resistance in the *p*-AlGaN cladding and the high *p*-side contact resistance. Together, this can account for up to 50 percent of the power consumption, when this device is driven at operating current densities well above the lasing threshold. These losses manifest themselves in the form of Joule heating.

The tremendous tunnel-junction

We are able to address the optical and resistive losses in GaN-based laser diodes with a technology that sidesteps the problems associated with *p*-doping of GaN. We draw on our previous success, which involves using remote-plasma CVD to grow active-as-grown tunnel junctions for cascade LEDs that address efficiency droop. Now we are applying the technology and the techniques to laser diodes. In these devices, we replace the *p*-type metal ohmic contact with a lower-resistivity *n*-type ohmic contact, enabled by a GaN-based tunnel-junction that provides conversion between *n*-type and *p*-type regions. This design

Layer	Thickness (nm)	Doping (cm^{-3})	Composition	Absorption Coefficient (cm^{-1})
n++ contact	20	1.5E20	GaN	375
n-AlGaN cladding	500	5.0E18	$Al_{0.08}Ga_{0.92}N$	125
n++	30	2.5E20	GaN	627.5
p++	10	1.0E20	GaN	250
p-WG	60	2.0E19	GaN	50
EBL	12	1.5E20	$Al_{0.2}Ga_{0.8}N$	375
2x InGaN/GaN MQW	2.7 / 9.0	-5.0E16	$In_{0.11}Ga_{0.89}N$/GaN	12
n-WG	100	-2.0E17	GaN	12
n-AlGaN cladding	1000	-3.0E18	$Al_{0.067}Ga_{0.933}N$	12

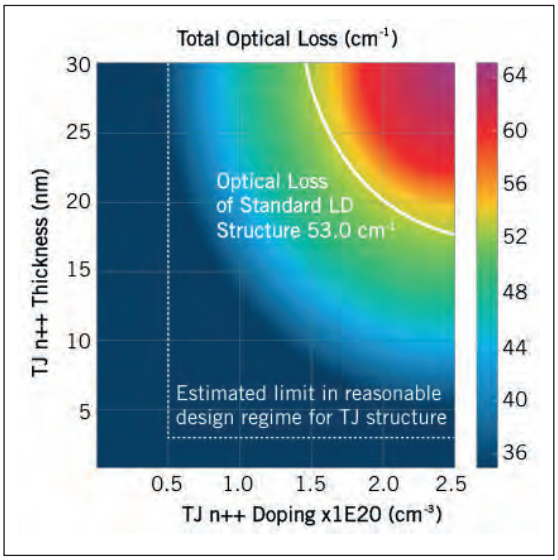


Figure 2. (a) (above) Tunnel-junction laser diode structure and (b) (right) total optical loss as function of thickness and silicon doping levels in the n^{++} layer of the tunnel junction.

eliminates the high *p*-side contact resistance that plagues conventional laser diodes.

With this approach, optical and resistive losses in the *p*-AlGaN cladding layer remain. To address this, the tunnel junction must be positioned deeper within the structure – it needs to be moved to within or even below the *p*-AlGaN cladding layer. Doing this enables the highly resistive *p*-AlGaN cladding layer to be replaced with much lower resistance *n*-AlGaN. In turn, this reduces the optical absorption coefficient, due to the lower silicon-doping requirements.

Great care is needed in designing the tunnel-junction and selecting its location. It must be positioned so that any increase in optical losses associated with its addition is offset by a comparable reduction in losses that come from the replacement of *p*-type layers with those that are *n*-type. In addition, it is crucial to ensure that the resistance in the tunnel-junction is low enough to be offset by the reduction in series and contact resistance. It is only by meeting both of these criteria that the tunnel-junction laser diode can offer a viable solution to increasing the conversion efficiency of GaN-based lasers.

We have investigated how the structure and placement of the tunnel junction impacts the optical losses in laser diodes. To do this, we have simulated various laser diode structures (see Figure 1 (a) for details of the design and the absorption coefficients that have been used). This has included calculations of the refractive index profile and distribution of the optical mode. For these simulations, values for the absorption coefficients of the *n*-type and *p*-type layers have been based on benchmark doping levels. Results show that a large proportion of the total optical loss – it is more than 80 percent – is associated with the *p*-side of the device (see Figure 1 (b)). Losses are high in the electron-blocking layer, the *p*-type waveguide, and the *p*-cladding layers.

With this benchmark in place, we repeated the simulation for a laser diode that incorporates a tunnel-junction (see Figure 2(a) for details of the design). This has the same base structure, but has: a tunnel-junction at the top of the *p*-type waveguide; and rather than a *p*-type AlGaN cladding and a heavily *p*-type doped contact layer, an *n*-type AlGaN cladding and a heavily doped *n*-type contact layer.

One of our simulations considered the total optical loss as a function of layer thickness and silicon doping level in the heavily-doped *n*-type layer of the tunnel junction (see Figure 2 (b)). As expected, greater losses come from thicker, more heavily-doped junctions. Included in this plot is a white contour line, which corresponds to the total optical loss of the standard laser diode, which does not have a tunnel

Layer	Thickness (nm)	Doping (cm^{-3})	Composition
p++ contact	20	1.5E20	GaN
p-AlGaN cladding	500	1.0E20	$Al_{0.084}Ga_{0.916}N$
p-WG	105	2.0E19	GaN
EBL	12	1.5E20	$Al_{0.2}Ga_{0.8}N$
3x InGaN/GaN MQW	3.0 / 6.5	-5.0E16	InGaN/GaN
n-WG	110	-2.0E17	GaN
n-AlGaN cladding	1500	-3.0E18	$Al_{0.068}Ga_{0.932}N$
n-GaN	2800	-1.0E19	GaN
Buffer	3900	-	GaN
Sapphire Substrate			

Figure 3. A standard MOCVD laser diode on a sapphire structure.

junction. If devices with a tunnel junction are to be a success, then they will have to have a total optical loss that is less than this.

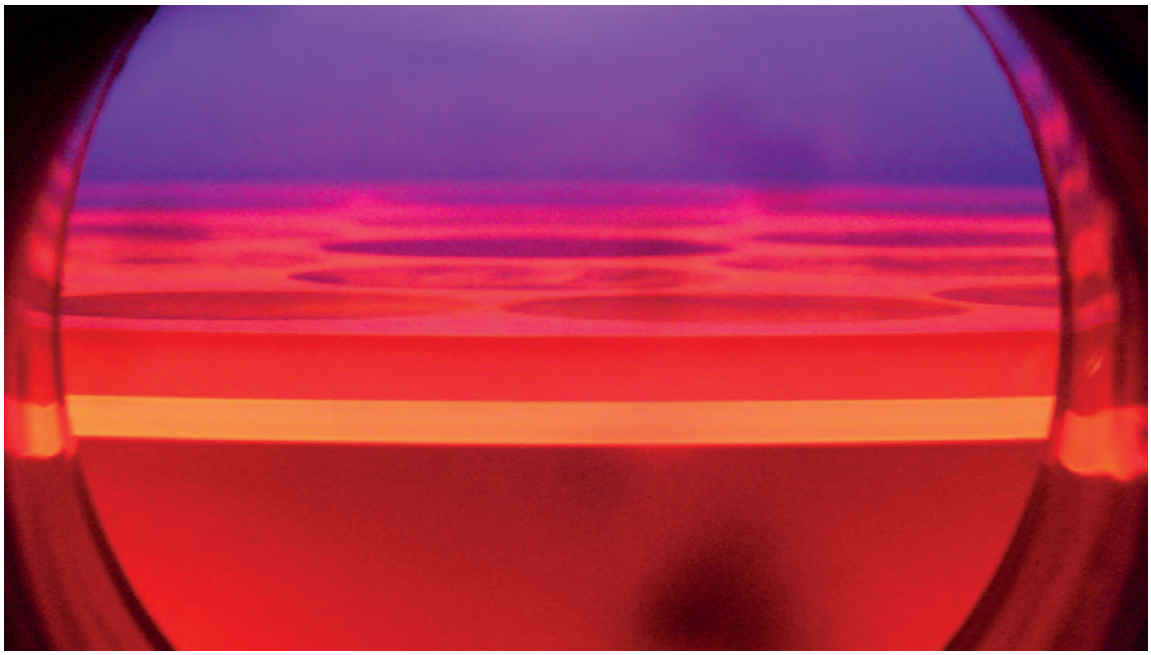
The simulation provides an estimate of the upper limit for the doping and the thickness that can be tolerated within the heavily-doped *n*-type layer of the tunnel junction to ensure a net overall reduction in optical loss for this type of laser. In this figure, the white dashed line offers an estimate of the lower limit for thickness and doping values in the heavily doped *n*-type layer to realise reasonable tunnelling behaviour.

Working devices

To put these simulations to the test, we have fabricated laser diodes on sapphire substrates. Using MOCVD, we have produced lasers with a structure that is similar to that detailed in Figure 1, and is shown in Figure 3.

Through a collaboration with researchers at the University of New Mexico, we have been able to process our epiwafers into ridge-waveguide laser diodes. Pulsed measurements reveal the relationship between the output of this device, the applied voltage and the drive current (see Figure 4). Emitting at 397 nm, these lasers produce an output power from one facet of up to 155 mW. The voltage required to run these devices could be improved with further optimisation of the *p*-AlGaN cladding layer.

Our next step has involved integrating the tunnel-junction grown by remote-plasma CVD within these



The inside of an remote-plasma CVD chamber during growth, showing active nitrogen.

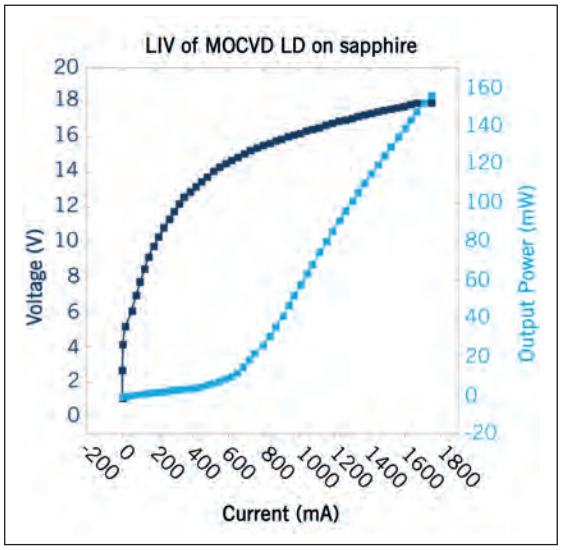
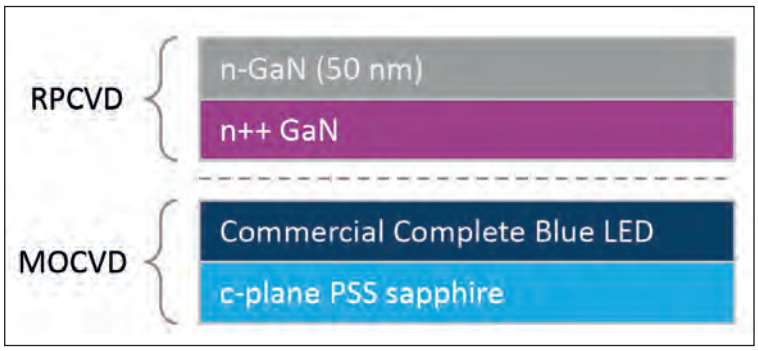


Figure 4. Light-current-voltage measurements of an MOCVD-grown laser diode on a sapphire substrate.



Sample	TJ n++ thickness (nm)	TJ n++ Doping (cm^{-3})	ΔV_f (V)
A	23.0	2.4E20	0.70
B	13.0	2.4E20	0.65
C	13.0	1.3E20	0.91
D	13.0	8.0E19	1.08
E	7.4	2.4E20	0.88
F	4.6	2.4E20	1.04
G	3.5	2.4E20	1.15
H	2.5	2.4E20	1.48

Figure 5. (a) Hybrid MOCVD/remote-plasma CVD tunnel-junction structure and (b) a table of n^{++} parameters used to optimise the tunnel junction for laser diode applications. The delta V_f in the last column refers to the difference in forward voltage, V_f, of the tunnel-junction LED compared with the reference LED using ITO.

lasers diodes, and seeing if this improves device performance through reductions in optical loss and device resistance. We were keen to find out if tunnel junctions could be grown with a low enough doping and/or thickness in the heavily-doped *n*-type layer to yield a net reduction in optical loss compared to our reference. We also wanted to discover whether the addition of the tunnel junction produced only a small increase in drive voltage.

To optimise our tunnel junctions for laser diodes, we began by growing them by remote-plasma CVD on commercially sourced blue LEDs. For the current spreading layer, we used a top *n*-doped GaN layer, rather than indium tin oxide (see Figure 5 (a) for a diagram of the device). Measurements on a portfolio of processed and packaged devices with different forms of tunnel junctions show that, in general, tunnel junctions with a higher level of doping produce a smaller voltage drop during operation (see Figure 6 (a)). Note that the light output from all devices is similar.

We have simulated the total optical loss for lasers with all of these forms of tunnel junction (see Figure 6 (c)). Encouragingly, the laser with the tunnel junction that has the smallest increase in drive voltage has a total optical loss of 47.9 cm^{-1} – that's just below the contour line that represents the total optical loss of the standard laser diode without a tunnel junction. This is a crucial finding, as it reveals that laser diodes that have a tunnel junction grown by remote-plasma CVD and are optimised to have the lowest increase in the drive voltage can yield a net reduction in total optical loss. This paves the way to improved devices, which feature a reduced series and contact resistance, due to the replacement of *p*-type cladding and *p*-type contact layers with *n*-type cladding and *n*-type contact layers.

Building on this discovery and our demonstration of lasing behaviour from laser diodes that do not contain tunnel junctions and are formed by MOCVD, we have recently gone on to grow lasers with tunnel junctions by combining MOCVD and remote-plasma CVD. These devices, grown completely within our facilities, have a foundation of *c*-plane free-standing GaN. On this we grow layers up to the heavily *p*-type tunnel junction layer by MOCVD, before adding the remaining layers by remote-plasma CVD (see Figure 7 (a) for a diagram of this device).

Collaborators at the University of New Mexico have processed our structures into ridge-guide lasers. Testing of these devices is in its infancy. We do have results of current-voltage characteristics obtained when driving the laser in pulsed mode. Further development is required to fully characterise the optical output of these devices, but initial results are encouraging, with lasers exhibiting normal diode behaviour without breakdown at up to 20.5 $kAcm^{-2}$ (see Figure 7 b).

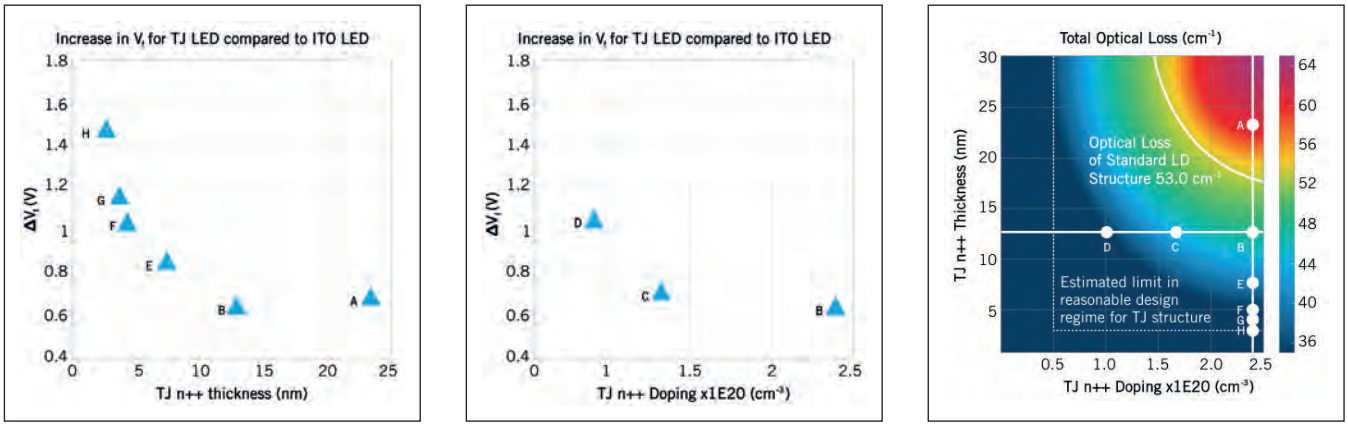


Figure 6. (a) Tunnel junction LED delta V_f compared to a reference LED with ITO for tunnel junctions with n^{++} doping of 2.4 x 10^{20} cm^{-3} and different n^{++} thickness and (b) n^{++} thickness of 13 nm and different doping levels. (c) Location of the simulated optical loss for tunnel junction laser diode with the same tunnel junction structure as tested on the LEDs.

Unlocking opportunities

Efforts at developing our tunnel-junction laser diode technology will continue, with the goal of unleashing the potential of new GaN laser diode designs across multiple wavelengths and power levels, so that this class of device can serve a wide variety of applications. We are off to a good start, as our initial results demonstrate the promise of remote-plasma CVD tunnel junctions for realising *p*-AlGaN-free laser diode structures that offer improved device performance, thanks to reductions in optical loss and series and contact resistance.

Note that we are not alone in championing the benefits of tunnel-junctions in laser diodes. Joachim Piprek, founder and president of NUSOD, has calculated that conversion efficiency could increase from 30 percent to 60 percent with the addition of a tunnel junction. However, he reported that the potential improvements were limited, due to the additional optical loss associated with the highly-doped layers in the tunnel junction.

As we have shown, this limitation can be overcome. By suitably controlling the doping and thickness in the n^{++} layer of the tunnel junction, we can produce low-loss tunnel-junction laser structures with a net reduction in total optical loss compared with standard lasers. A reduction in both Joule heating losses and optical losses is promised, leading to higher conversion efficiencies in GaN laser diodes. That's the target for us, as we continue to improve laser diode performance with bespoke solutions for existing customers, and start to work with new laser diode developers, so that the market will benefit from greater availability of high-brightness devices that incorporate tunnel junctions grown by remote-plasma CVD.

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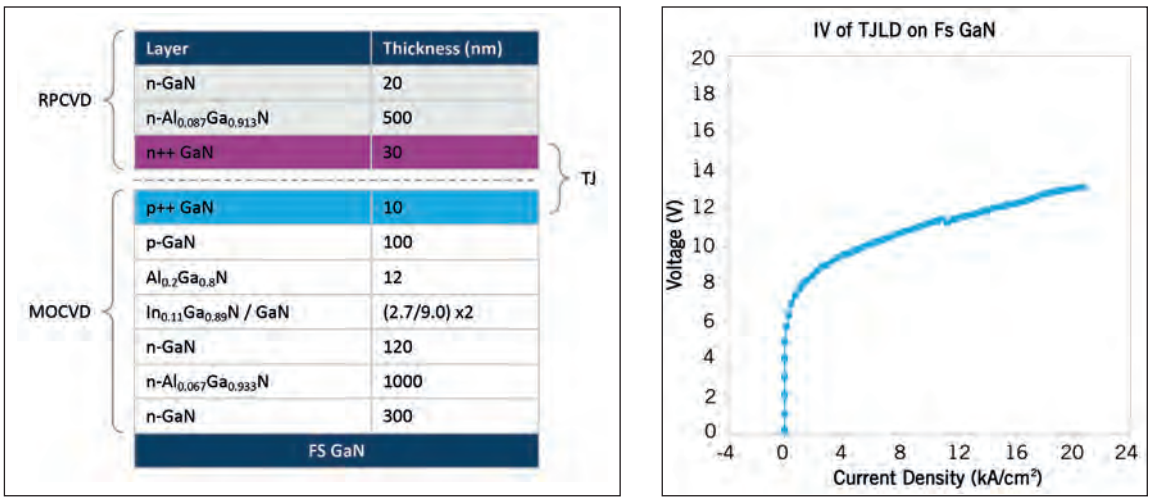

Figure 7. (a) Tunnel junction laser diode structure and (b) light-current-voltage data from a processed laser diode.

Unlocking the potential of SiC power modules with graphite

Replacing the copper core in insulated metal substrates with highly oriented graphite boosts thermal conductivity of the SiC power module while trimming its weight

BY WEI FAN AND DAWN KRENCISZ FROM MOMENTIVE QUARTZ TECHNOLOGIES, GARRY WEXLER FROM HENKEL CORPORATION AND EMRE GURPINAR AND BURAK OZPINECI FROM OAK RIDGE NATIONAL LABORATORY

CHOOSING YOUR NEXT CAR is far from easy. As part of being environmentally responsible, you will certainly want to consider purchasing a vehicle that runs solely on battery power. While such a vehicle will undoubtedly help to curb your carbon footprint, will it have sufficient driving range? Or will your car run out of juice on one of your long trips?

To avoid agonising over this dilemma, what is needed is the development of vehicles with a longer range between recharges. Increasing energy storage in the battery will help, along with a hike in the performance of the power electronics.

Such efforts are already underway in the United States supported by a Department of Energy roadmap that details requirements for next-generation electric drive systems. Targets include: a doubling of power handling capability to allow the electric traction drive system to handle peak powers of up to 100 kW; and a hike in power density from 13.4 kW/litre in 2020 to 100 kW/litre in 2025. Research institutes and industrial partners have been pouring tremendous resources and efforts into the development of the next-generation power electronics for electrical vehicles (see Figure 1).

Increases in power density must be accompanied by improvements to the thermal management system. However, this must be accomplished without adding weight to the vehicle, as weight will negatively impact travel range. Meeting this requirement demands more advanced thermal management methods beyond traditional heat pipes, water cooling, and fans.

Tackling this challenge of improving the thermal management of SiC power modules while trimming their weight is the objective of a collaborative partnership between Momentive Quartz Technologies, Henkel Corporation (Henkel) and Oak Ridge National Laboratory (ORNL). Working within the US Department of Energy Electric Drive Technologies Consortium, this partnership – from now on referred to collectively as the 'Group' – is redesigning the insulated metal substrate. This technology is light weight, featuring a thermally conductive graphite core. Armed with this approach, engineers can cut substrate weight by 30 percent and increase the power loading for the SiC power module by 15 percent or more, thanks to a near doubling of thermal conductivity.

Figure 1. An EV test platform at ORNL that was used to evaluate power modules for wireless charging

This technology promises to revolutionise the standard isolated multi-chip SiC power module. Today, if you cut open one of these modules you are likely to find SiC dies, on either a direct bonded copper or insulated metal substrate, mounted to a thick copper

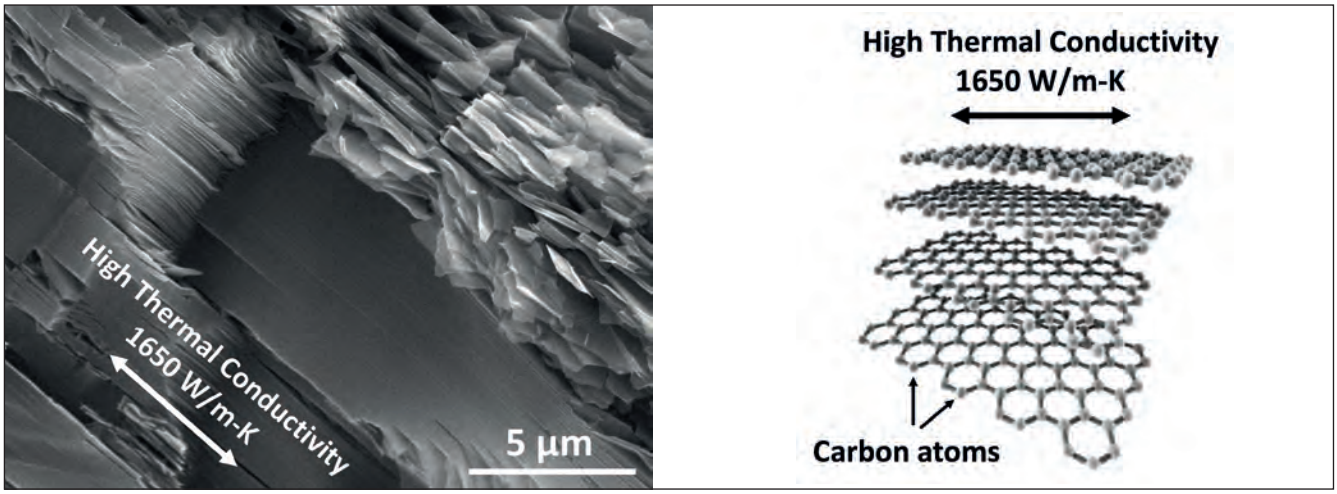

Figure 2. Cross-sectional view, provided by a scanning electron microscope, of Momentive Quartz Technologies' thermal pyrolytic graphite cores (left). An illustration of this material, showing well-aligned graphene basal planes (right).

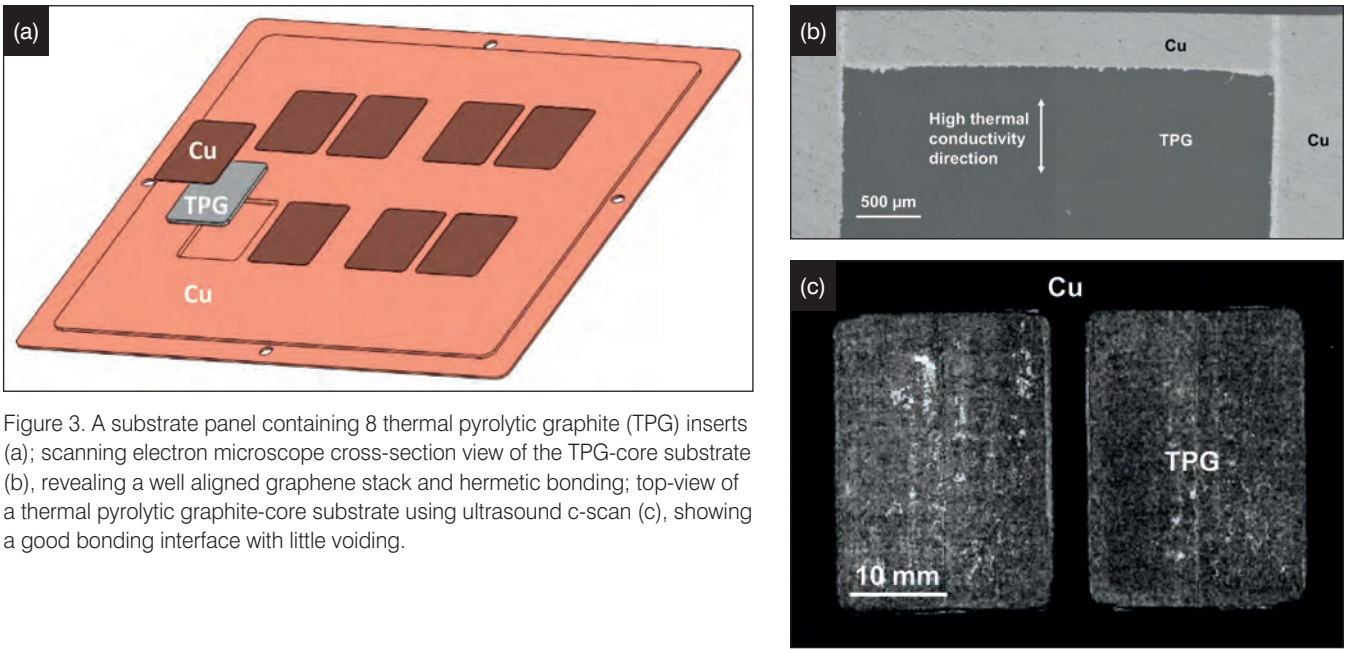

Figure 3. A substrate panel containing 8 thermal pyrolytic graphite (TPG) inserts (a); scanning electron microscope cross-section view of the TPG-core substrate (b), revealing a well aligned graphene stack and hermetic bonding; top-view of a thermal pyrolytic graphite-core substrate using ultrasound c-scan (c), showing a good bonding interface with little voiding.

base plate. These parts will be united by solder or epoxy bond layers.

When a direct-bonded copper substrate is used, it will typically provide good thermal conductivity and electrical isolation. Unfortunately, this usually comes at the expense of a thermal expansion mismatch, chemical instability, substrate rigidity, and a limit to layer thickness. These restrictions tend to hamper the performance of SiC power modules.

The common alternative, the insulated metal substrate, is made by stacking metal layers – often copper or aluminium – to a thermally conductive, electrically isolating dielectric layer. The result is a low-cost, flexible circuit structure that can be tailored by varying the thickness of the metal and dielectric layers. Unfortunately, the thermal conductivity in the dielectric has shown to be inferior to that of the ceramics in a direct-bonded copper substrate. However, given the design flexibility and reliability of this technology, there is no doubt that insulated metal substrates could trump those based on direct-bonded copper, as long as there is an increase in the thermal conductivity of the metal layer in contact with the SiC dies.

The Group's collaboration is able to draw on the expertise of Momentive Quartz Technologies, which, along with its legacy, has been an industry leader in thermal management in the aerospace, telecommunications and defence sectors for more than half a century. Within its portfolio, there is the: TC1050

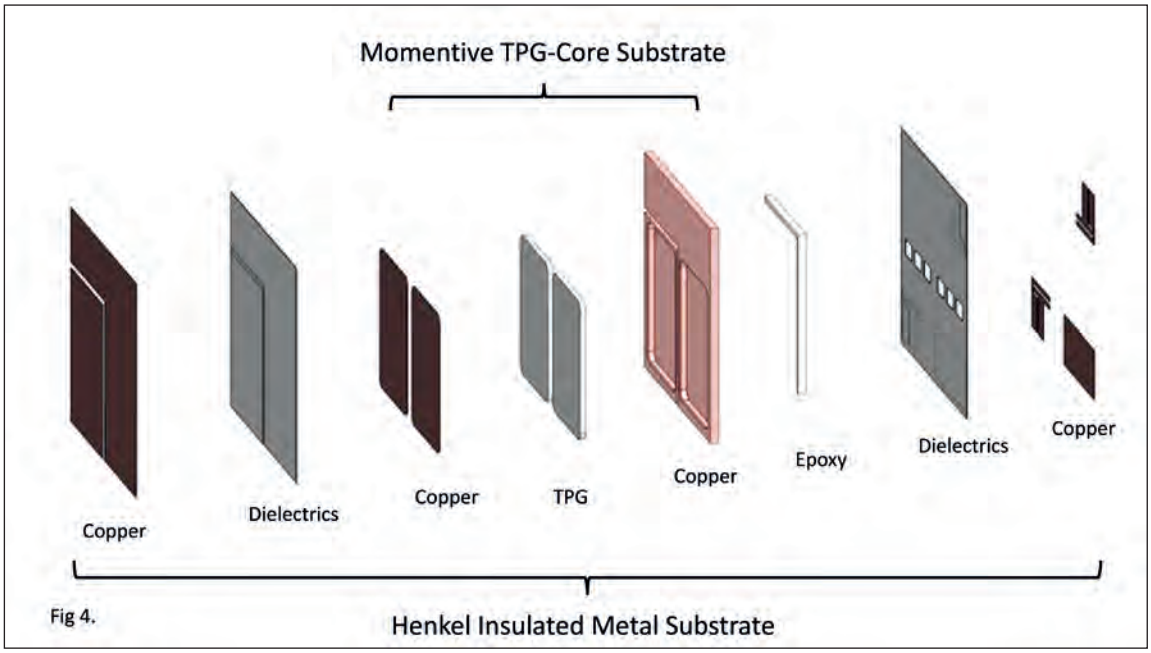

Figure 4. A seven-layer thermal pyrolytic graphite-core insulated metal substrate structure utilising proprietary materials and processing technologies from Momentive Quartz Technologies and Henkel.

heat spreader, deployed since the 1990s for board-level thermal management; the TMP-EX heat sink, introduced in 2011, that matches the coefficient of thermal expansion of the chip; and the TMP-FX thermal straps, which provide flexible heat conduction in tight spaces.

Glorious graphite

For all these products, the key ingredient is Momentive Quartz Technologies' thermal pyrolytic graphite, a material first produced in the 1960s when the current business was part of Union Carbide. This form of graphite, produced by CVD at over 2000 °C, is made up of millions of stacked layers that are highly oriented graphene planes. They equip the material with extremely high thermal conductivity (see Figure 2). Parallel to its basal plane, the thermal conductivity is 1650 W m^{-1} K^{-1} – four times the value of copper. Another merit of this material is that it is light weight. Its density is just 2.25 g/cm^3 for thermal pyrolytic graphite, which is one-fourth the density of copper.

Encapsulating a core of this form of graphite into a copper substrate enables a high thermal conductivity to be combined with a low mass. The Group was able to accomplish this by drawing on Momentive Quartz Technologies' proprietary bonding technology to ensure excellent thermal and mechanical joints between the graphite insert and the copper enclosure. The high quality of this bond is evident in the scanning electron microscopy and ultrasound c-scan images (see Figures 3 (b) and (c)). They reveal a hermetic, nearly void-free encapsulation.

One of the characteristics of the thermal pyrolytic graphite inserts is their anisotropic thermal conductivity. This allows the orientation and layout of the graphite within the copper enclosure to be tailored to the application. Measurements with a Netzsch Nanoflash 476 reveal a thermal conductivity of 760 W m^{-1} K^{-1} in a structure of thermal pyrolytic graphite sandwiched between copper. This conductivity is nearly double that of copper. At

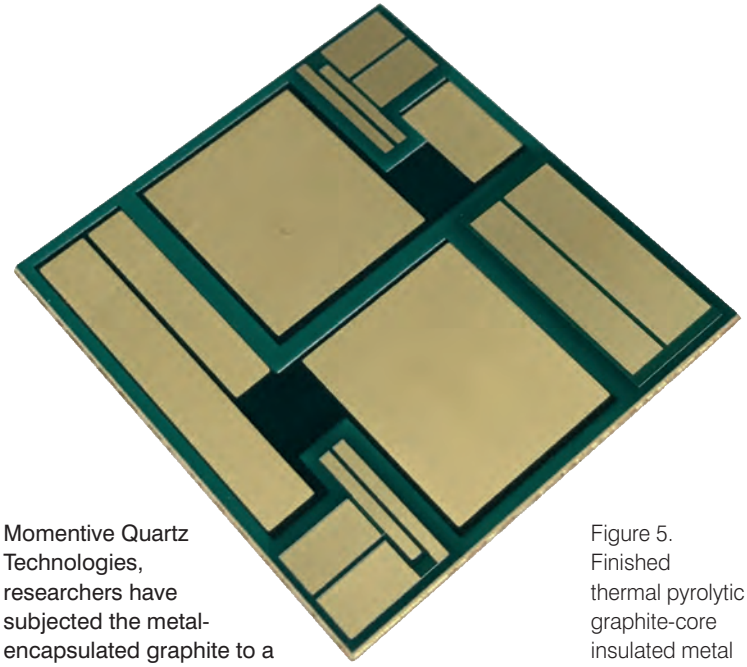

Figure 5. Finished thermal pyrolytic graphite-core insulated metal substrate with patterned copper circuit layers and dielectrics on both sides.

Momentive Quartz Technologies, researchers have subjected the metal-encapsulated graphite to a range of other tests, including thermal cycling and mechanical shock and vibration. This examination demonstrates the outstanding thermal performance and reliability of this hybrid structure.

To ensure that this material technology can be used as a functional circuit for a SiC power module, collaborator Henkel Corporation deployed Momentive Quartz Technologies' graphite-core heat spreader in its insulated metal substrates. For more than two decades, Henkel has provided thermal-cladded insulated metal substrates to the power electronics and LED lighting industries. These substrates have proven to be particularly well suited to today's higher-watt-density and surface-mount applications, such as SiC power modules. Once the graphite is encapsulated inside the copper, it can be used directly in place of monolithic metal in Henkel's lamination process (see Figure 4). Note that the benefits of switching from a solid copper core to one

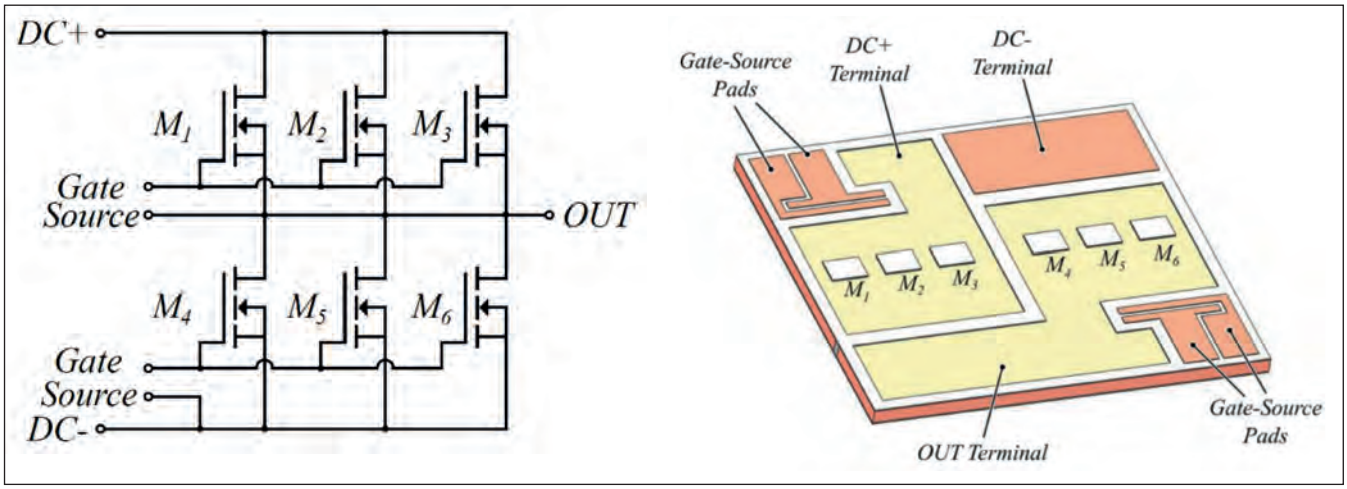

Figure 6. Electrical schematic of a half-bridge module (left) and insulated metal substrate circuit layout (right). More details are given in https://doi.org/10.1115/IPACK2019-6436

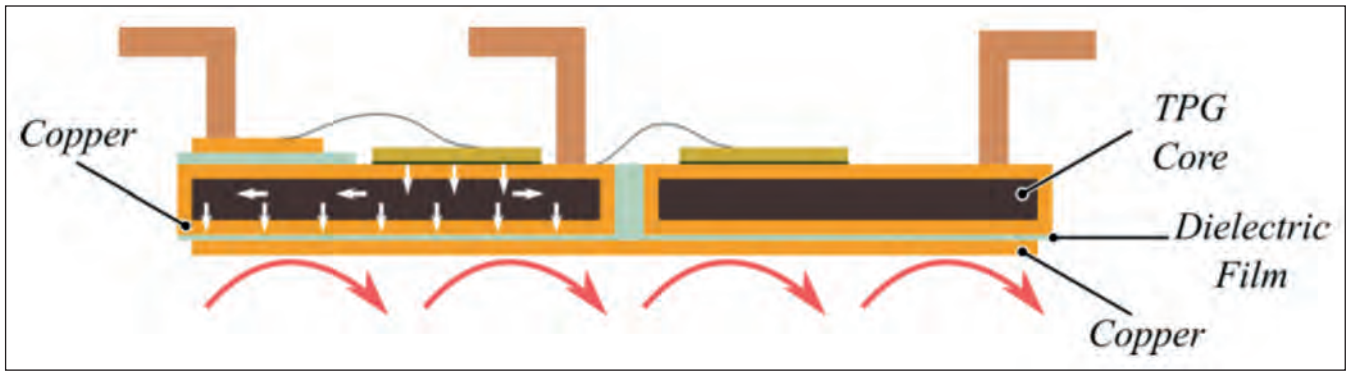

Figure 7. Conceptual module design using thermal pyrolytic graphite core to channel the waste heat away from the dies. More details are given in https://www.energy.gov/sites/prod/files/2019/06/f63/elt208_gurpinar_2019_o_4.9_3-41t.pdf

that contains graphite are not limited to an increase in thermal conductivity, as they also extend to a 30 percent weight reduction.

During the fabrication of the insulated metal substrates, technologists at Henkel uses a proprietary coating technology to apply dielectric layers to the graphite-core substrate plane and the copper foil layers (see Figure 5). Adding these dielectric layers is critical to meeting the breakdown voltage requirements. Engineers at Henkel can also include features such as non-conductive, epoxy-filled grooves that provide electrical isolation between poles.

Proven credentials

To demonstrate the power of this approach, the Group constructed a testing platform, a common half-bridge SiC MOSFET inverter module (see Figure 6). In this design, Momentive Quartz Technologies' graphite inserts were positioned directly under the SiC dies. With this arrangement, waste heat was extracted through the thickness, towards the terminals, where it could transfer to Henkel's thermally conductive dielectric layers (see Figure 7). In addition to reducing the thermal resistance of the copper substrate, the heat spreading provided by the thermal pyrolytic graphite increased the effective contact area of the dielectric layer, and thus its heat conductance. According to modelling by those on our team at ORNL, there was an immediate improvement in temperature uniformity for the insulated metal substrate with the thermal pyrolytic graphite core, associated with the higher in-plane heat conduction of this form of graphite (see Figure 8).

An additional insight provided by the thermal analysis was a significant reduction in junction temperature – it is 11 °C cooler in both steady and cycling states. As a result of this, 15 percent more power can be generated by the SiC power module for the same temperature as a standard insulated metal substrate. Yet another demonstrated advantage of using graphite is the reduction in the difference in the junction temperature when the power is on versus when it is off (see Figure 9).

To validate their modelling, the scientists at ORNL conducted bench-top measurements to compare the performance of SiC power modules of insulated metal substrates with copper cores and thermal pyrolytic graphite cores (see table 1). Preliminary measurement of the assembled power modules confirmed the earlier

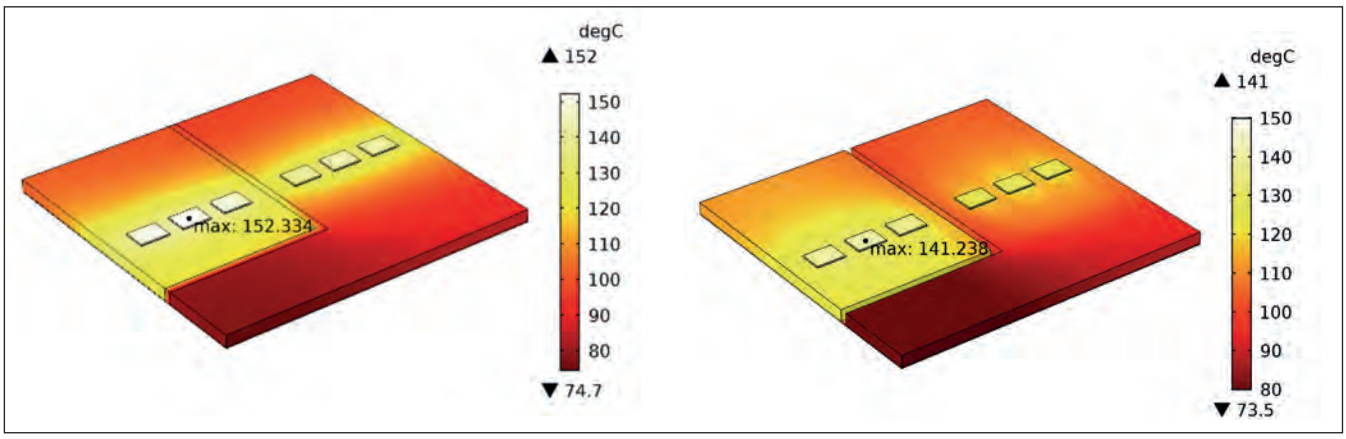

Figure 8. Thermal analysis of a SiC module using insulated metal substrates with a copper-core (left) and thermal pyrolytic graphite core (right). The results demonstrate the improvement in heat spreading by the two thermal pyrolytic graphite cores. More details are given in https://www.energy.gov/sites/prod/files/2019/06/f63/elt208_gurpinar_2019_o_4.9_3-41t.pdf

modelling results. The testing is on-going, with those at ORNL assessing the final package performance, durability and reliability of insulated metal substrates with thermal pyrolytic graphite cores (see Figure 10).

The efforts of this collaboration showcased the merits of using thermal pyrolytic graphite cores in insulated metal substrates. Compared to conventional copper cores, the switch to this form of graphite effectively doubled thermal conductivity, while trimming weight by almost one third. This solution, with demonstrated manufacturability, can also enable an increase in heat load, improved reliability, simplified module design and a reduction in both assembly costs and the number of steps. By orienting the graphite within the copper core, heat conduction can be optimised for die size, location, circuit pattern and power loading.

The technology could also enable more sophisticated multi-layer power board designs that address thermal, electrical and weight issues simultaneously. Working under the support of the Department of Energy, the Group is playing its part in working toward this goal as a continued effort to refine its technology, so that it can unleash the potential of SiC devices and push their implementation in electric drive systems.

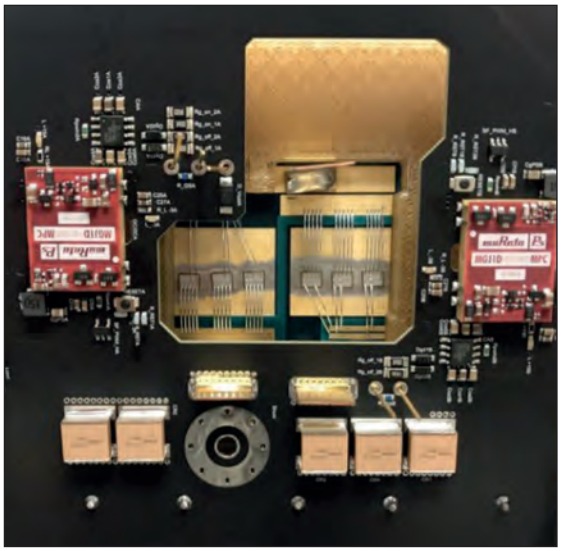

Figure 10. Assembled SiC power module using a thermal pyrolytic graphite-core insulated metal substrate.

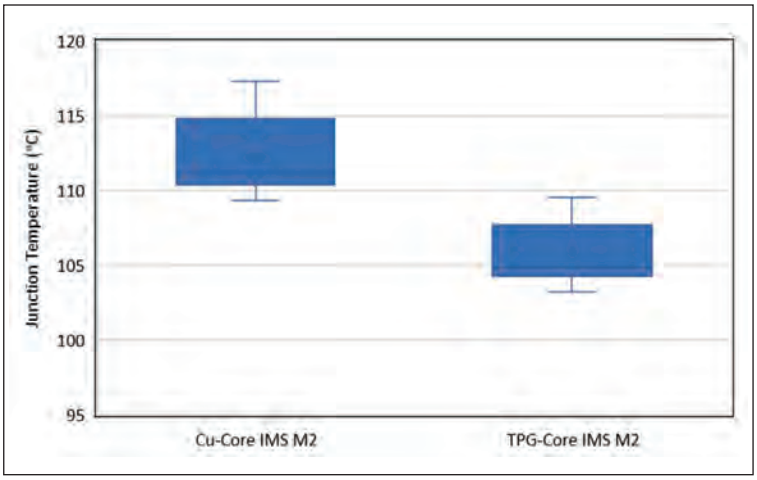

Figure 9. Plotting the SiC MOSFET junction temperature during power cycling revealed a 1.8 °C reduction in temperature range using the thermal pyrolytic graphite-core insulated metal substrate.

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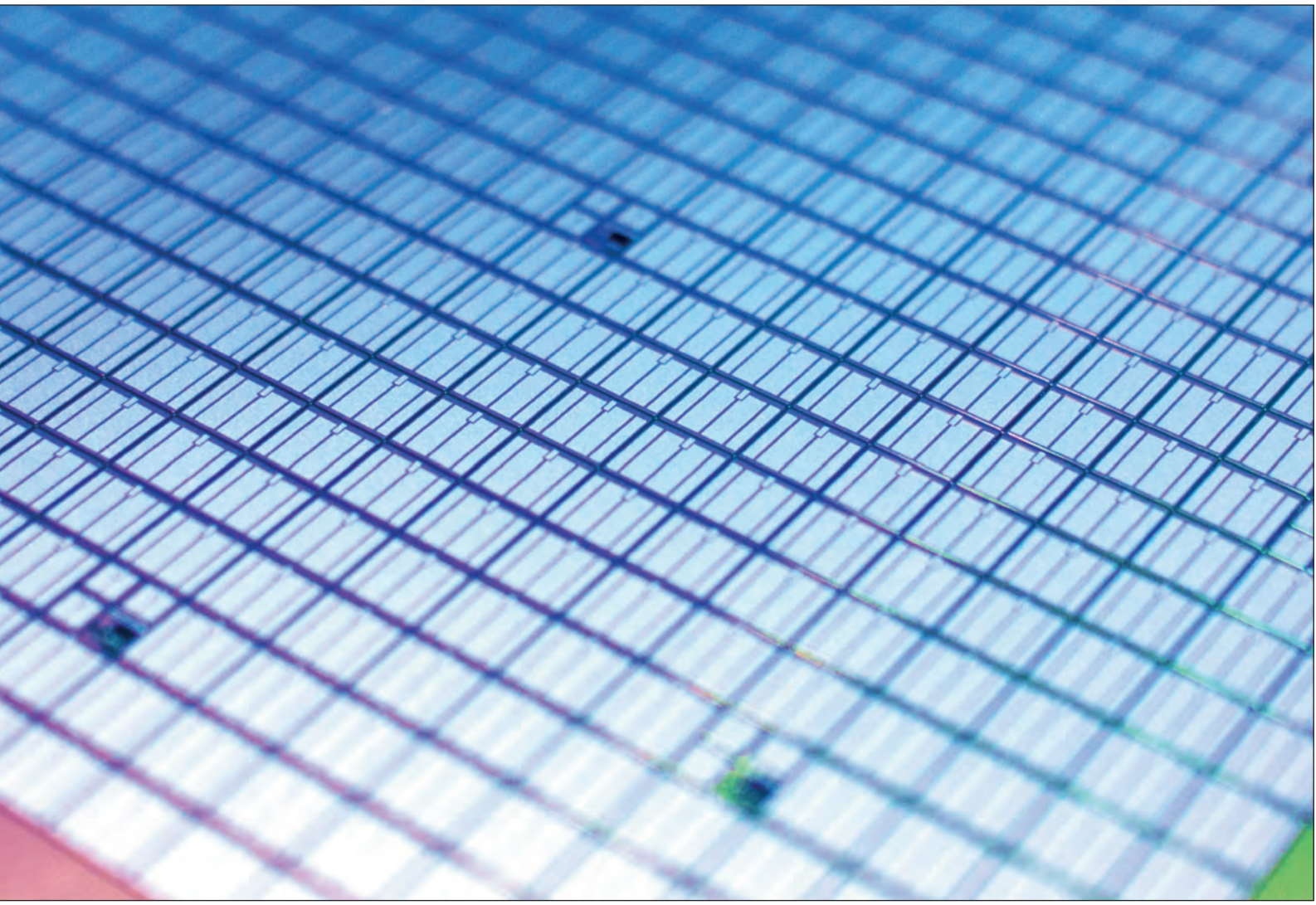
	Thermal Conductivity [W/m-K]			Junction Temperature T_{max}		Junction Temperature Variation
	x	y	z	@ steady state	@ power cycle	@ power cycle
Cu-core IMS	395	395	395	152°C	113°C	8.6°C
TPG-core IMS	1155	130	760*	141°C	104°C	6.8°C

Table 1. Thermal performance comparison of insulated metal substrates with a copper core and a thermal pyrolytic graphite core. * Measured value using Nanoflash method.



A better face for the SiC MOSFET

SiC MOSFETs with a V-grooved trench reduce on-resistance and trim switching losses

BY KOSUKE UCHIDA AND TAKASHI TSUNO FROM SUMITOMO ELECTRIC INDUSTRIES

WHEN THE LEADERS of the most powerful countries met at the World Economic Forum in January, one topic dominated the agenda – climate change. For many of them, this is by far the biggest issue of our age, with action needed right now to cut carbon footprints.

There are so many opportunities to do this. Some are at the national level, such increasing the number of nuclear power plants and solar farms. There are also changes that companies can make, such as investing is more efficient machinery, and there are personal decisions, such as moving to a more plant-based diet and taking fewer flights.

Within this mix, one of the options for saving energy and curbing carbon dioxide emissions is the introduction of more efficient power control technologies. They are widely deployed, playing an

essential role in electric vehicles, in renewable energy systems, and in industrial motor drives.

Most of today's power devices are made from silicon. Their performance has improved over many decades, but they are now encroaching theoretical limits, calculated from their physical properties. This means that it is no longer possible to make significant reductions in power loss, which comes from conduction and switching losses.

What's needed is to replace silicon devices with those made from wide bandgap materials, such as SiC and GaN. This pair attract much attention because they have the upper hand over silicon on many fronts, including a higher dielectric breakdown electric field, a superior electron saturation velocity, and a greater thermal conductivity. Thanks to these characteristics, SiC and GaN provide a higher breakdown voltage and a reduced on-resistance, leading to lower conduction losses.

A noteworthy difference between SiC and GaN is the quality of the crystal. Bulk SiC has fewer crystal defects, enabling the manufacture of high-quality SiC epitaxial substrates, and in turn the production of vertical SiC power devices. These devices, which use the whole surface of the epitaxial layer, combine a high current with a breakdown voltage of 600 V or more. Due to this, SiC is expected to have its greatest success in high-voltage applications that achieve high power, while GaN is expected to be used in low output power applications.

SiC devices will displace the silicon insulated-gate bipolar transistor (IGBT), which combines a high breakdown voltage with a low resistance. Due to this device's bipolar operation, switching losses increase with the electron-hole recombination time. That's not the case with the SiC MOSFET, a unipolar device that provides high-speed switching and a higher breakdown voltage.

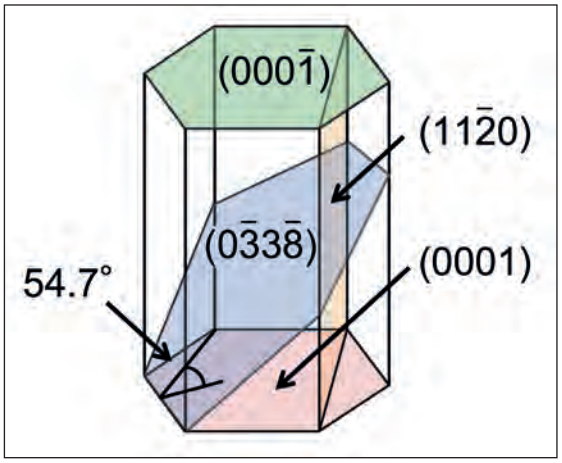


Figure 1. Major crystal faces in 4H-SiC. The (0$\bar{3}$3$\bar{8}$) face is located at an off-angle of 54.7 degrees from the (0001) face.

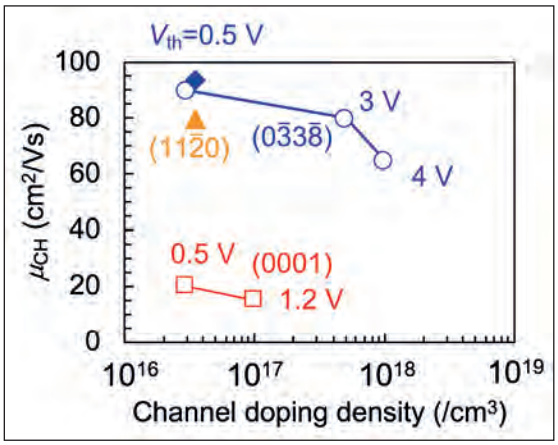


Figure 2. The doping density dependence of channel mobility of SiC lateral MOSFETs. The (0$\bar{3}$3$\bar{8}$) face shows a higher channel mobility and a higher threshold voltage than other crystal faces.

A great groove

At Sumitomo Electric Industries Ltd., Japan, we have developed a new architecture for the SiC MOSFET. It features V-groove trenches, enabling us to exploit a face with a higher mobility.

This development is able to draw on our vast experience surrounding the production of compound semiconductor products, which include GaN HEMTs, GaAs FETs and the substrates that form their foundation. More recently, we have been developing SiC crystals, and have gone on to start mass production of 6-inch SiC epitaxial substrates, which we refer to as EpiEra. They are produced using a high-quality, cost-effective growth technology – we have named this our multi-parameter and zone-controlled SiC growth technology. We use a unique simulation technique to determine the most appropriate doping concentration uniformity for realising the intended device performance and yield. Through vertical integration of our SiC material and device technologies, we produce SiC MOSFETs with a high performance and a high yield.

We have developed our novel MOSFET architecture because the channel mobility in conventional designs is substantially lower than the bulk mobility, due to a high interface state density. To demonstrate what can be achieved, we fabricated a lateral MOSFET on 4H-SiC(0$\bar{3}$3$\bar{8}$) face, which is located at an off-angle of 54.7 degrees from the (0001) face (see Figure 1).

Our results show that this is the best face for making SiC MOSFETs, because the channel mobility is highest for all doping concentrations, due to a lower interface state density and a higher free-electron ratio (see Figure 2). When employing a doping concentration of 10^{18}/cm^3, a high channel mobility of 60 cm^2 V^{-1} s^{-1} is realised alongside a threshold voltage that is as high as 4 V – this is high enough to suppress erroneous ignition at high temperatures.

To exploit the benefits of this face, over the last few years we have developed and commercialised the 4H-SiC V-groove trench MOSFET, a device we refer to as a VMOSFET. Recently, efforts have been

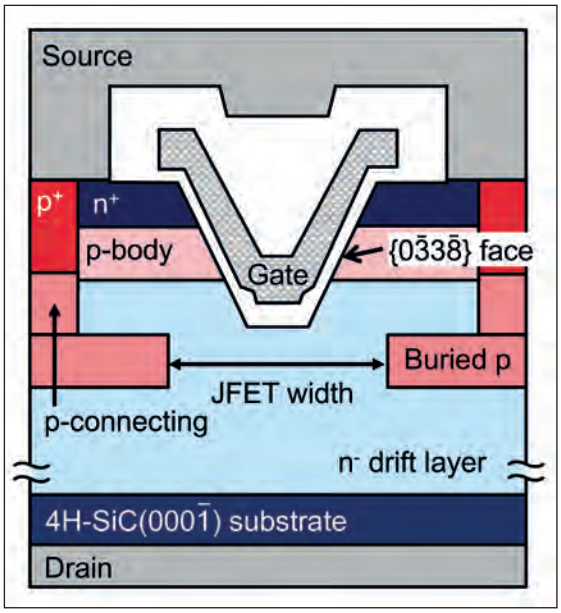


Figure 3. A cross-sectional view of a SiC VMOSFET.

directed at high power conversion efficiency, so that the devices can handle hundreds of amps and have a breakdown voltage above 1 kV. These transistors feature 4H-SiC{0338} trench side walls that have a higher channel mobility than other SiC crystal faces (see Figure 3 for a diagram of this structure). Using this design, channel resistance can be reduced while realising a high channel density.

The key to producing this device is the use of a chemical etching process to form the V-groove trenches. We use silicon dioxide as the etching mask, with etching undertaken at around 900 °C in a chlorine ambient. During this process, chlorine produces a chemical change in the surface, with SiC converted to carbon, which then reacts with oxygen. The resultant silicon chloride and carbon dioxide vaporizes at a high temperature (see Figure 4).

This process exposes {0338} faces, which are extremely stable. Note that with a conventional process to form U-shaped trenches, such as reactive-ion etching, this would lead to etching damage and the formation of sub-trenches. The high-quality of the faces produced by our process can be seen in the images of a scanning electron microscope (see Figure 5).

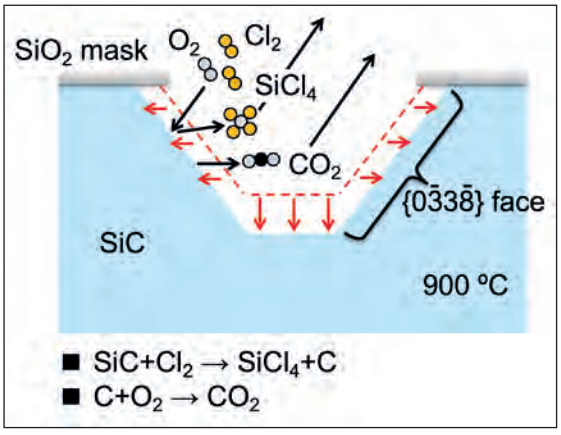


Figure 4. Chlorine etching creates the V-grooves of the MOSFET.

A shortcoming of the trench structure is that the gate oxide film that forms on the bottom of the trench breaks easily when a high voltage is applied to the device. When this happens, the electric field concentrates on the gate oxide film. To address this and enhance the reliability of the VMOSFET, we implant *p*-type electric-field-alleviating regions around the groove bottom. With this addition, the application of a high voltage to the drain electrode causes the electric field to concentrate on the buried *p*-region edge. Making this modification alleviates the electric field on the gate oxide film.

With this design, we are able to increase the switching speed and reduce switching loss by reducing the parasitic capacitance between the gate and drain electrodes. This is accomplished by creating a source potential, by electrically connecting the buried *p*-regions to the source electrode with *p*-connecting regions.

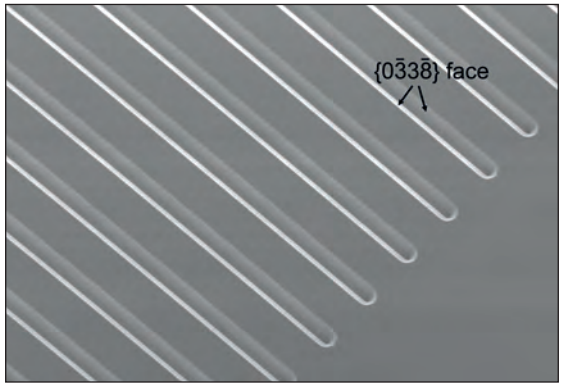


Figure 5. Scanning electron microscopy (SEM) image of a V-groove.

Proven reliability

To ensure a low on-resistance, and a low oxide electric field that leads to long-term reliability, it is crucial to optimise the JFET width and the width between the buried *p*-regions. Our efforts related to this include our investigation of the relationship between the oxide electric field and the lifetime under a drain bias condition.

An estimate of the lifetime under a high-temperature reverse-bias condition has been obtained with test dies that have a dedicated structure. To increase the oxide electric field, dies with a V-groove gate trench structure have a large JFET width compared with the VMOSFETs designed for mass production. These tests have been conducted at an ambient temperature of 175 °C. The oxide electric field in these transistors has been calculated using Technology CAD simulation. Calculations of the electric field distribution reveal that the oxide electric field is highest on the bottom oxide edge, due to electric field crowding (see Figure 6).

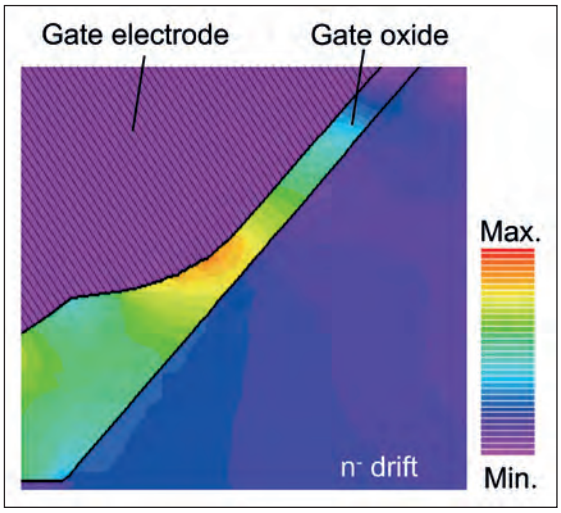


Figure 6. Electric field distribution around the V-groove trench bottom calculated by technology CAD for a lifetime estimation.

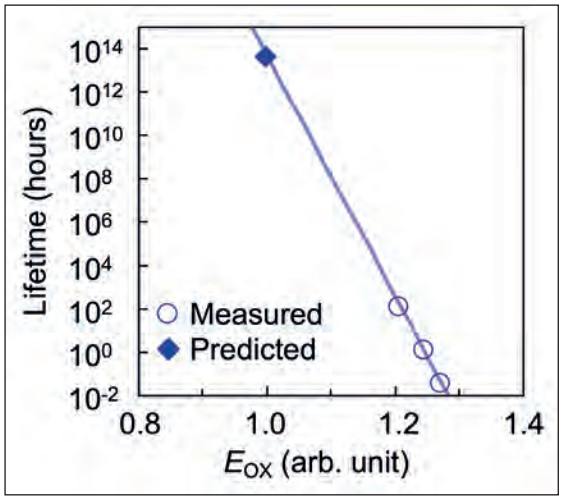


Figure 7. Long-term lifetime of VMOSFETs. Lifetime is estimated under a drain bias condition at T_a = 175 °C in the case of a 10 percent cumulative failure rate. The predicted lifetime is equal to 200 years under a 0.1 ppm cumulative failure-rate condition.

After we carried out the high-temperature reverse-bias tests, we analysed the damaged point of the VMOSFETs. We found that its location corresponded to our simulation's highest point for the oxide electric field.

Using these measurements, we have determined the impact of the oxide electric field on the lifetime. A plot for a 10 percent cumulative failure rate is shown in Figure 7.

For high-reliability applications, our target lifetime is more than 20 years for a 0.1 parts-per-million cumulative failure rate. We exceed this by a significant margin. For an oxide electric field of 1.0 – note that this is an arbitrary unit – the predicted lifetime is 4.5 x 10^{13} hours. That equates to a lifetime of 200 years under a 0.1 ppm cumulative failure rate condition, according to our calculations that relate the lifetime to the cumulative failure rate.

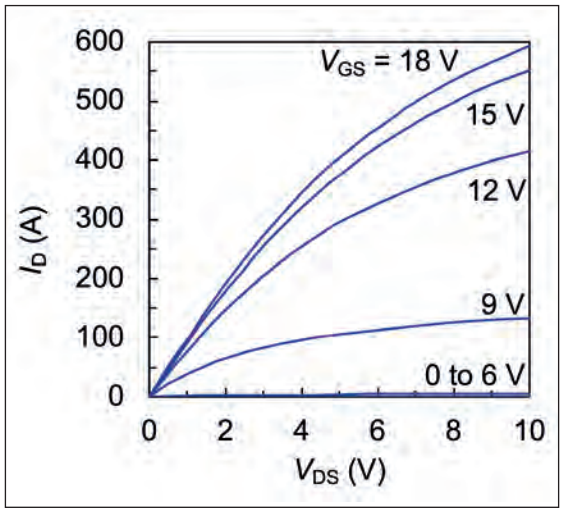


Figure 8. I_D-V_{DS} characteristics (V_{GS} = 0 – 18 V) at T_j = 25 °C. The VMOSFETs exhibit a high current capability of 200 A DC and 600 A pulse.

Drawing on the high-temperature reverse-bias tests, we used simulations to design a structure that has a low on-resistance and an oxide electric field of 1.0 at a drain bias of 1200 V. This led us to fabricate VMOSFETs with an optimised design on a 150 mm wafer. Operating at a junction temperature of 25 °C, the resultant 6.0-mm-square die can handle a DC current of 200 A and pulses up to 600 A (see Figure 8). The specific on-resistance is just 3.1 mΩ cm² for a gate-source voltage of 15 V and a drain-source voltage of 1 V; and at 25 °C, the threshold voltage is 4.6 V, for a drain-source voltage equal to the gate-source voltage, and a drain current density of 1 mA/mm².

The breakdown voltage is well above the target, capable of withstanding up to 1640 V (see Figure 9). Another encouraging attribute is the small gate-to-drain capacitance – it is just 15 pF at a drain-source voltage of 800 V – enabling effective suppression of

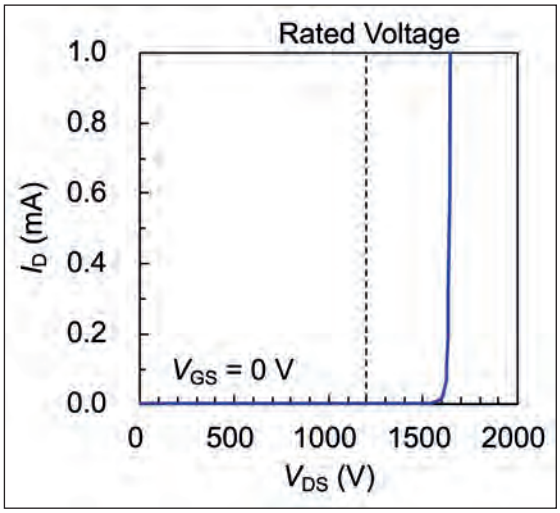


Figure 9. Blocking characteristics. The VMOSFETs show an adequate margin against a rated blocking voltage of 1200 V.

Table 1. Sumitomo Electric Industries' line-up of VMOSFET products.

Current Range		<10A	30A	100A	≦200A	≦400A	≦600A
Discrete	600-900V	✓	✓	✓			
	1,200V	Now	Now	Now			
	1,700V	Now	Now	Now			
Module	1,200V				Now	Now	✓
	1,700V				Now	Now	
	3,300V					✓	

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Module
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self-turn-on, due to the grounded buried *p*-regions that effectively block lines of electric force from the drain electrode.

We have also performed a double pulse test with an inductive load, using a SiC Schottky barrier diode for the free-wheel device (see Figure 10 for details). This test highlights our VMOSFETs fast switching speed and low switching loss. Rise and fall times are 16 ns and 7 ns, respectively; and turn-on and turn-off energy loss are just 260 μJ and 270 μJ, making the total switching loss only 530 μJ.

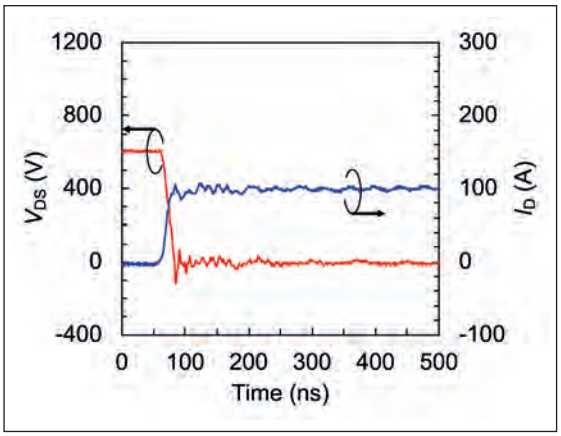

Figure 10. Fast switching characteristics of VMOSFETs under double pulse test. Conditions for this test are: R_G = 1.0 Ω, V_{GS} = +15/-5 V, V_{DD} = 600 V, I_D = 100 A, L = 100 μH.

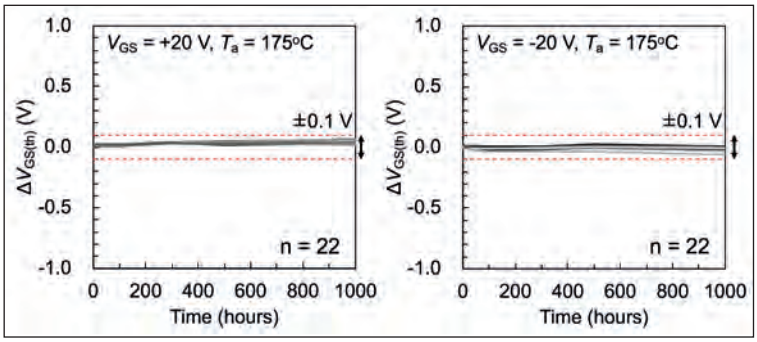

Figure 11. Stable threshold voltage of a VMOSFET under a high temperature gate bias test of V_{GS} = +20 V (left) and -20 V (right) at T_a = 175 °C.

Further testing involved evaluating the threshold voltage stability of our VMOSFETs. Evaluation of 22 samples at 175 °C revealed threshold voltage shifts of less than 0.1 V after a 1000 hour high-temperature gate-bias test. This small shift is evidence of the stability and high quality of the gate oxide on {0$\bar{3}\bar{3}$8} crystal faces.

Our successful development of our 1200 V / 200 A VMOSFET has enabled us to expand our line-up for this class of transistor (see Table 1). From a user's perspective, the adoption of VMOSFETs allows: better performance at both the component and system level; greater capability in designing far smaller components; and a stable supply chain and better quality management. We anticipate that the superior characteristics of our VMOSFETs, which combine low power loss and high reliability, will underpin further expansion in the SiC market.

A part of this R&D was carried out as one of the Super clean room Power Electronics Line (SPEL) joint research consortium activities hosted by the National Institute of Advanced Industrial Science and Technology.

Further reading

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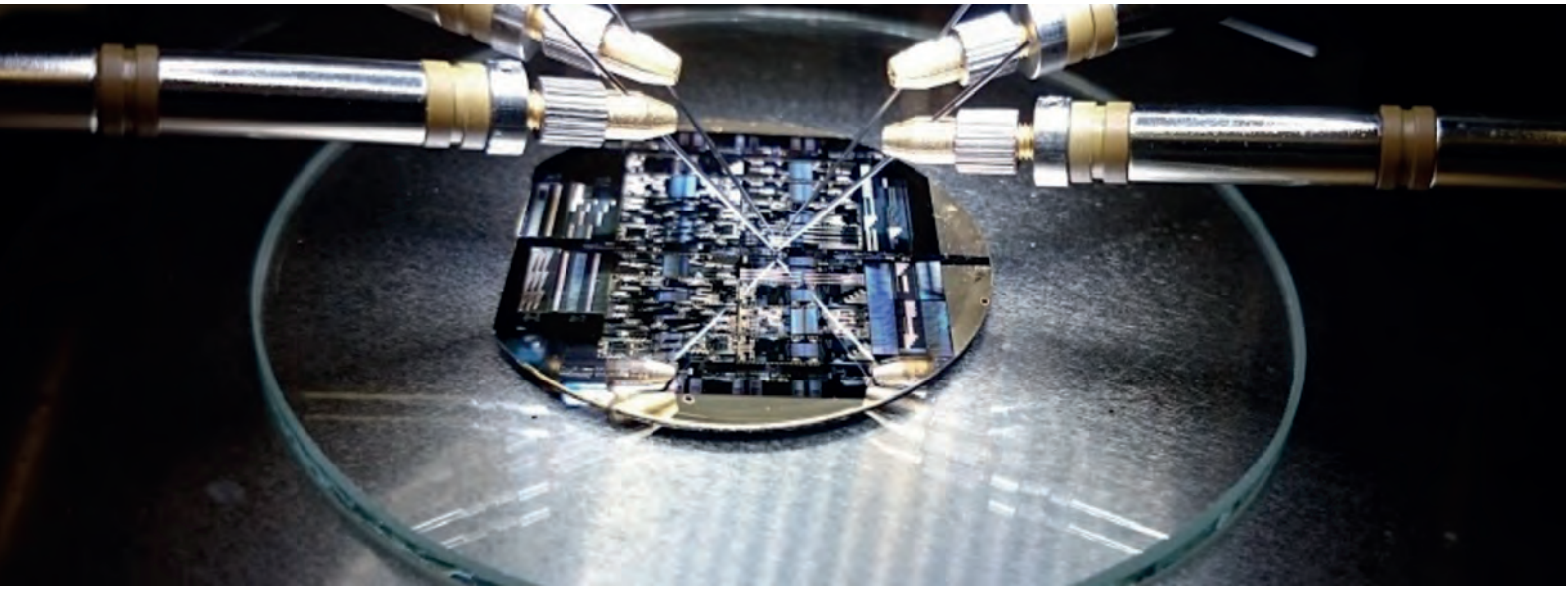

Plug and play characterization

An integrated electrical test platform builds on the advantages of foundry services by offering chip-level test and characterization

BY AXEL SCHOENAU, MORITZ BAIER, FRANCISCO SOARES, GUILLAUME BINET, NORBERT GROTE, JONAS HILT, PETER HELLWIG, RONALD FREUND AND MARTIN SCHELL FROM THE FRAUNHOFER HEINRICH HERTZ INSTITUTE

THERE ARE MANY APPLICATIONS for the InP PIC. It is already deployed in sensing, telecommunication, biophotonics and signal-processing – and it may not be long before it is used in quantum optics, LiDAR and AI. This technology has much appeal in all these applications, due to its low cost and the opportunity to slash the size compared with classical optics.

Manufacturing InP PICs involves several complex, costly processing steps. But this does not have to prohibit researchers at companies and universities from investigating this technology, thanks to the availability of photonic InP foundry services. By sharing wafer space with other customers, fabrication costs for a whole wafer can be distributed between the various parties (see Figure 1). Using a process design kit, each customer can place pre-defined building blocks of active and passive integrated components on the InP wafer according to the foundry's design rules.

Many of these building blocks have to be actively controlled. Current sources are needed to control light sources, such as distributed feedback lasers and distributed Bragg reflector lasers, and also gain sections, thermal optical phase shifters and heaters.

In addition, there is a need for voltage sources, used to control electro-absorption modulators and photodiodes. PICs also feature appropriate metal routing, to facilitate probing and simplify wire bonding to either electronics or an interposer board.

If a customer does not require packaging, bare InP PICs are shipped to the customer in a gel pack (see Figure 1). On arrival, the customer has to undertake experimental verification of the prototype. That's not easy, as it requires measurement equipment with a total price tag of several hundred thousand euros or more, and experience in handling PICs, to prevent them from damage.

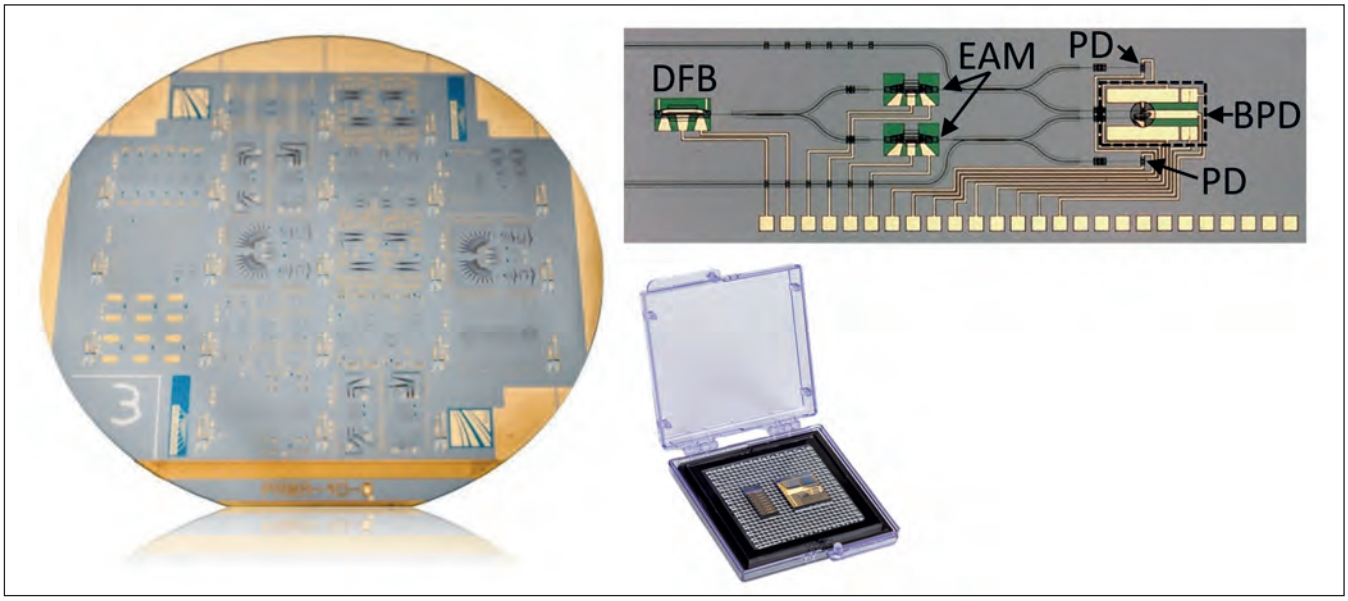

Figure 1. A 3-inch InP based multi-project wafer containing customers' PIC designs and test structures (left). Single PIC with metal routing for on-chip DC characterization of balanced photodiodes (BPDs) (top right). This chip contains distributed feedback lasers (DFBs), electro-absorption modulators (EAMs) and photodiodes (PDs). Bare chips in a gel pack before shipping to the customer (bottom right).

To overcome these daunting obstacles, our team at the Fraunhofer Heinrich Hertz Institute has developed an integrated test platform for generic PICs. Our work builds on the InP PIC foundry services that we offer. Those working in this industry now have the opportunity to access foundry services that are no longer restricted to epiwafer growth and processing, but extend to test and characterization.

Conventional PIC measurements

One of the expenses for engineers carrying out their own PIC testing is the purchase of a temperature-controlled chuck. It is needed to house the PIC and provide mechanical stabilisation, which can be realised with a vacuum. Further expense may be incurred to couple a fibre to the PIC. If that's required, equipment is needed for coarse and fine alignment. A translation stage for each fibre ensures coarse alignment to the waveguides or on-chip spot size converters, while fine alignment can be realised with piezo motors with sub-micron step sizes. An example of a PIC measurement set-up is illustrated in Figure 2.

A popular choice for the input light source for the PIC is an external cavity laser. It provides well controlled wavelengths and powers. Experimental set-ups also tend to include optical switches, used to direct out-coupled light to detection and analysis instruments, such as optical spectrum analysers and photodetectors. As testing may also involve electrical biasing and sweeps, there is the need for current and voltage sources, in combination with corresponding meters. To apply these currents and voltages to PIC building blocks, researchers often use probe needles (see Figure 3).

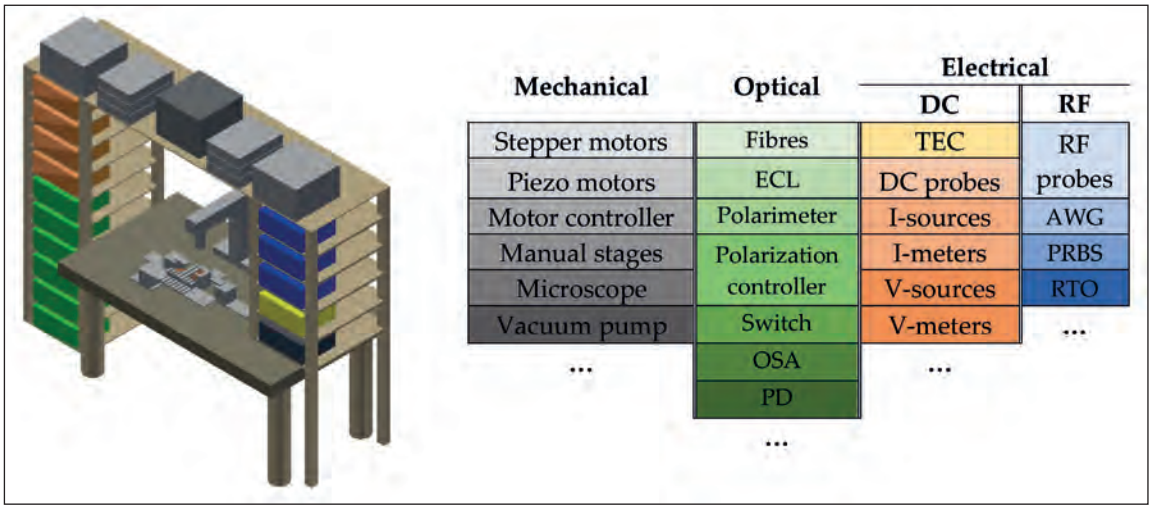

Figure 2. Schematic of a conventional PIC measurement set-up (left). Listed mechanical, optical and electrical systems (right).

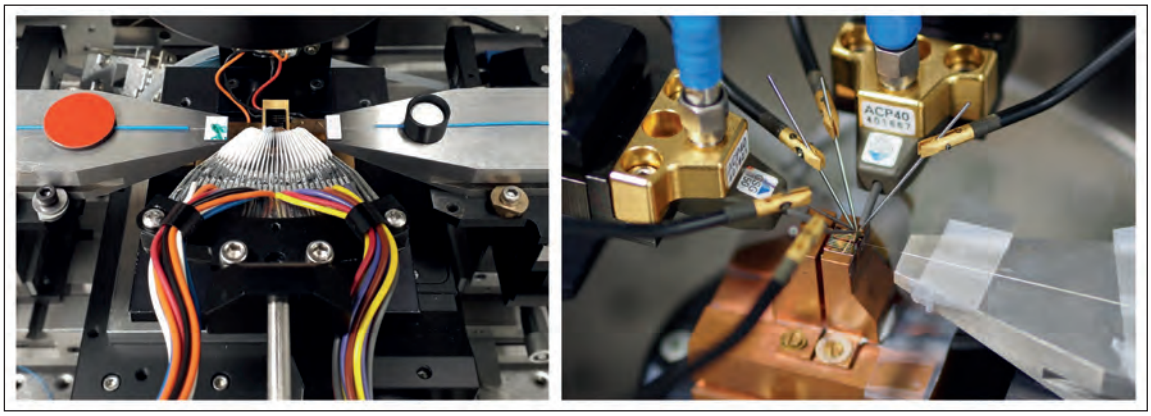

Figure 3. Electrical probing of a PIC with a 26 needle DC multiprobe (left), RF probes and single needles contacting a PIC (right, image courtesy of Weiming Yao, Department of Electrical Engineering, Photonic Integration, TU Eindhoven).

Measurements of data transmission require additional equipment, such as arbitrary waveform generators, pseudo-random bit stream sources and real-time oscilloscopes. If high-frequency measurements are to be made, RF-probes have to be placed on the PIC besides biasing needles. That's tricky, requiring many probes to be positioned on a chip that is smaller than a finger nail.

Simplifying evaluation

Given all these challenges associated with evaluating a PIC, affordable plug-and-play characterization is highly desirable. We are giving this to our customers with our new PIC evaluation set-up, which we have named PIConnect. By featuring integrated laser drivers and general purpose current and voltage sources, it enables parallel operation of PIC building blocks. Researchers investing in a PIConnect receive a mainboard, which contains all sources plus a plugged-in micro-controller board, as well as a PIC Board on a cooling stack to assemble the PIC (see Figure 4).

The mainboard contains eight current sources, eight voltage sources, four laser drivers, and one temperature controller that supports a 10 kΩ thermistor temperature sensor. The temperature controller drives currents up to ±1.5 A.

Each of the current sources provides an output current of up to 200 mA at up to 5 V. Voltage monitoring is integrated. For the voltage sources, the output can be adjusted between -10 ... +10 V. The current, which has integrated monitoring, cannot exceed 20 mA. Laser drivers can deliver currents up to 200 mA at a maximum voltage of 3 V. For this first-generation product, all measurements are made with 12-bit resolution.

To evaluate the PIC, it has to be mounted on the PIC Board and bonded to equally spaced pads. Connecting the PIC Board to the mainboard is done by a flexible flat cable containing 50 wires. The PIC Board is positioned on a cooling stack with a 20 mm by 20 mm Peltier element that enables precise temperature controlling through a 10 kΩ thermistor. Within this set up, the Peltier element is directly connected to the thermo-electric controller on the mainboard (see Table 1 for details of the hardware specifications).

To access the information generated by PIConnect, it is connected to a PC via Ethernet using a web interface. A Python-based graphical interface enables the setting of constant currents and voltages, and

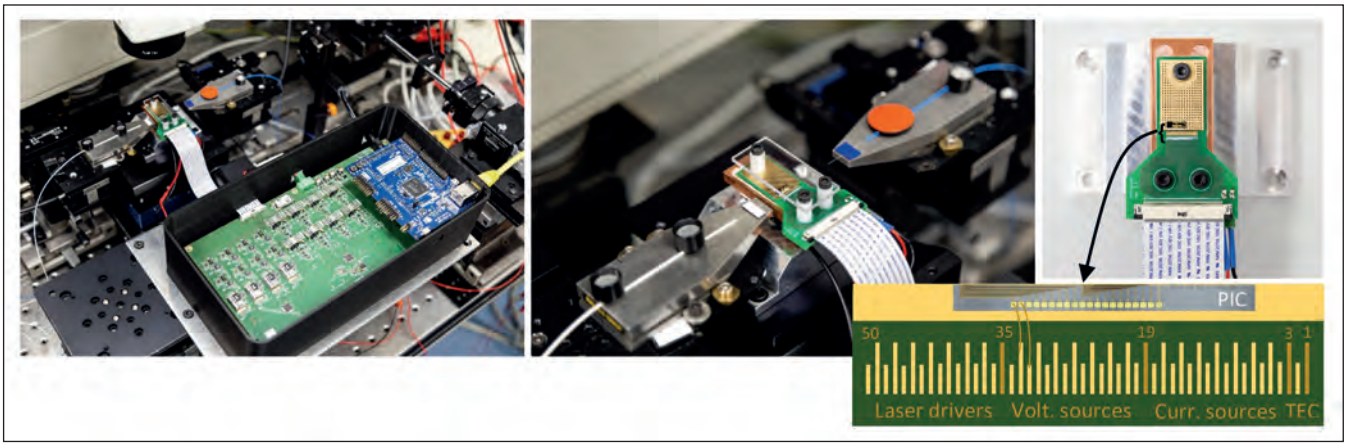

Figure 4. PIConnect comprised of mainboard (that has 8 current sources, 8 voltage sources, 4 laser drivers (Thorlabs MLD203P1) and one temperature controller (Thorlabs MTD415T)) with a microcontroller board (SAME70 XPLAINED) and PIC Board integrated in an existing measurement set-up (left). Photograph of the PIC assembled on the PIC Board with a Peltier element and mechanical mounting plate (centre). Fibre coupling is undertaken using tapered fibres and piezo actuators. Glued and wire-bonded PIC on a PIC Board (top right) and pinout of the PIC Board bond pads (bottom right; shows only exemplary wire bonding). The pitch between two adjacent pads is 200 μm.

Controller/Sources	Amount	Pin	Specs	Resolution	Monitoring
TEC controller	1	1-2	10 kΩ thermistor, ±1.5 A	0.7 mA	
Current source	8	3-18	Max. 200 mA @ max. 5 V	50 µA, 1.2 mV	Voltage
Voltage source	8	19-34	-10…+10 V @ max. ±20 mA	5 mV, 10 µA	Current
Laser driver	4	35-50	Max. 200 mA @ max. 3 V	50 µA, 0.7 mV	

Table 1. Components of the mainboard with specifications and pinout.

applying sweeps within defined ranges (see Figure 5). We recommend using predefined Python written functions when embedding PIConnect into an existing measurement set-up. Adopting Python's Application Programmable Interfaces equips the user with complete control of automated measurements in the kilohertz-regime – the only limit is the web interface speed.

Demonstrating capability

To demonstrate the capability of our PIConnect, PIC Board and mainboard are introduced to our existing PIC measurement set-up, which is shown in Figure 4. We use a polarimeter PIC as our showcase device under test. This chip has a Mach-Zehnder based structure, which uniquely maps measured photocurrents to the corresponding input polarization of the light. The polarimeter PIC works for wavelengths across the entire C-band and beyond, but here it is demonstrated at just 1530 nm. We presented the details of this PIC at OFC 2019.

During this test we launched 595 distinct polarizations across the Poincaré sphere into the polarimeter. The polarization states of the light are recorded using blue circles (see Figure 7). For this measurement, five integrated photodetectors are biased at -2 V, and at each polarization the photocurrents are recorded by PIConnect.

This test platform produces a mean mapping accuracy of around 1.8°. This low value highlights the competitive performance of PIConnect. We will offer PIConnect as an additional service to our customers. We know that they will welcome its introduction, as it is more than ten times more cost effective than the laboratory equipment normally used for PIC characterization, such as the combination of multiple dual-channel source meters, a Peltier controller and probing mechanics.

Note that it is possible to use two or more mainboards in parallel. This offers a straightforward approach to scaling the number of laser drivers, and current and voltage sources. To adopt this approach, the PIC Board must be re-designed so that it can connect several flat cables.

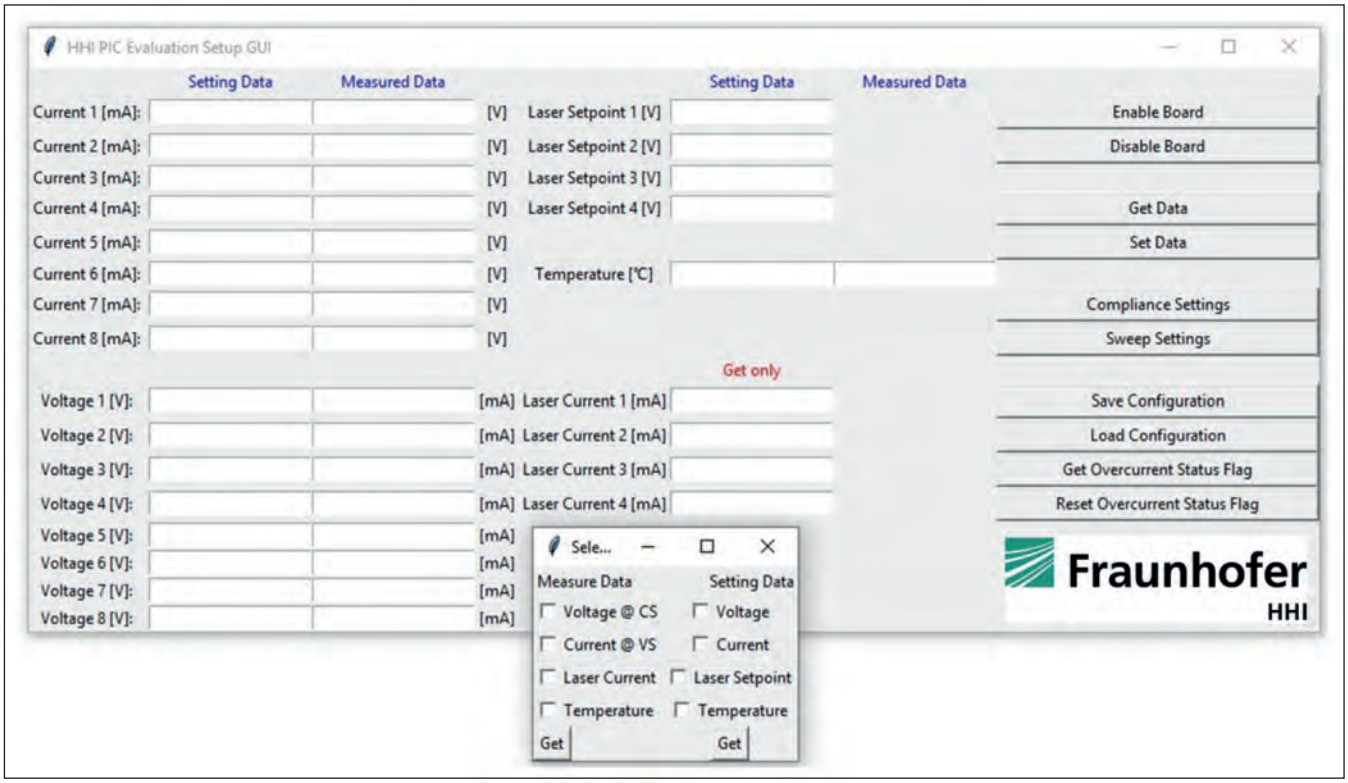

Figure 5. Python-based graphical user interface for setting and getting measurement parameters. Single sweeps, saving and loading are also possible.

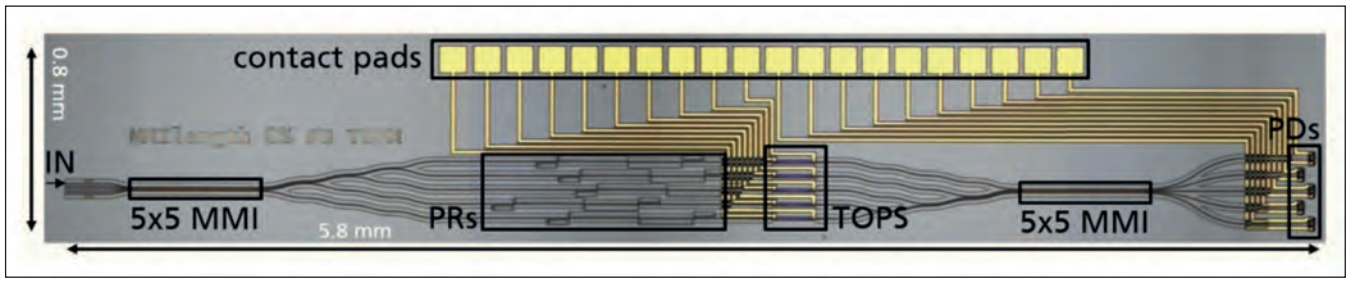

Figure 6. Integrated polarimeter PIC. Light is coupled from a fibre into one of the input ports on the left side. Five on-chip photodetectors (PDs) measure the photocurrents, and five thermal-optic phase shifters (TOPS) tune the configuration. The PIC further consists of polarization rotators (PR) and multimode interferometers (MMI).

We are continuing to work on simplifying PIC characterization. Through our involvement in the EU Horizon 2020 project InPulse – short for Indium-Phosphide Pilot Line for up-scaled, low-barrier, self-sustained, PIC ecosystem – we are working on automated, standardised routines to characterise PICs. The test platform will be exploited to offer a rigid, predictable and reproducible verification mechanism for process design kit contents and customer designs.

Together with the joint European platform for photonic integrated components and circuits (JePPIX), we will be offering PIConnect as an additional option to the customers of multi-project wafer runs. Our next step, enabled by general PIC design rules, is to make PIConnect available to customers using other foundries. A longer term goal is to integrate optical coupling and RF feeds, to improve the functionality of PIConnect. Through our efforts, lower-cost, simpler options for testing InP PICs are going to be available to more players within this industry – and that will help to grow the market for this technology.

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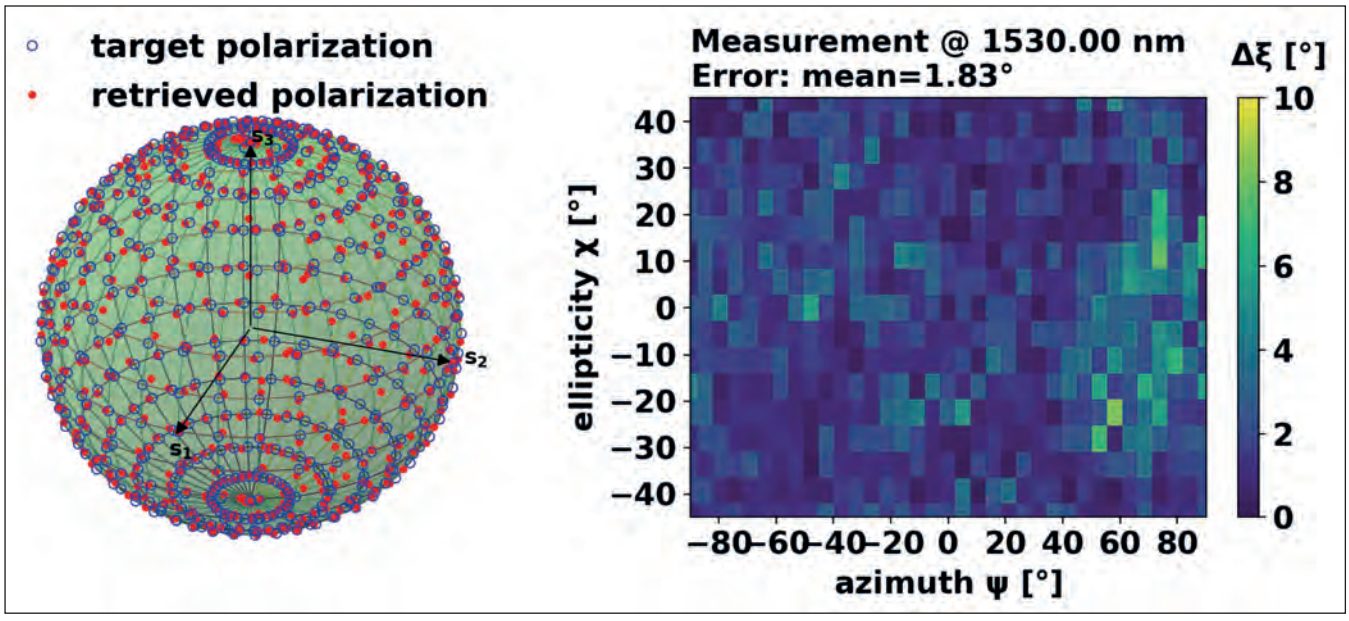


Figure 7. Experimental results at a wavelength of 1530 nm using PIConnect. On the left is a Poincaré sphere, 595 target (blue circles) and retrieved (red dots) polarizations are visualised. The corresponding heatmap on the right shows the measurement accuracy $\Delta\xi$ of the PIC. $\Delta\xi$ gives the angular measurement error on the Poincaré sphere. For this measurement the average is 1.83°.

Longer lasting UVC LEDs

A reduction in oxygen levels is believed to be behind a substantial increase in the lifetime of UVC LEDs

Engineers at Japan's Asahi Kasei Corporation and the US firm Crystal IS are claiming to have set a new benchmark for the lifetime of UVC LEDs. Efforts by this partnership have resulted in usable lifetimes of up to 3600 hours for devices with emission wavelengths between 230 nm and 237 nm, driven at 20 mA.

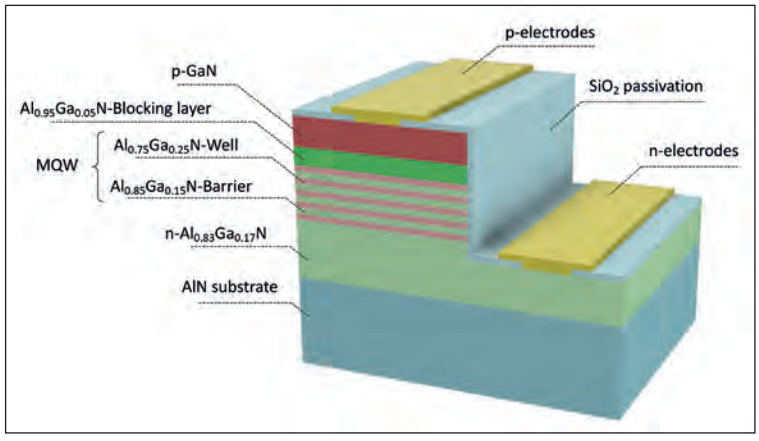
"This [lifetime] is quite important for real-world applications, such as nitrogen oxides gas sensing," argues team spokesman Akira Yoshikawa from Asahi Kasei.

Another breakthrough is the record-breaking wall-plug efficiency, resulting from improvements to internal quantum efficiency.

Yoshikawa and co-workers speculate that the increase in the lifetime of their UVC LEDs comes from a reduction in the level of oxygen impurities in the aluminium-rich nitride layers. These impurities degrade device performance by creating energy-sapping point defects that move under high current densities.

A reduction in oxygen levels in the epilayers has partly come from a switch from an Emcore MOCVD reactor to an Aixtron close-coupled showerhead design. The latter also improves reproducibility. "However, we have found that oxygen impurity concentrations also depend crucially on the growth conditions and the purity of the metal-organic source materials," says Yoshikawa.

An additional success, which helps to increase the efficiency of the UVC LED, is a reduction in forward voltage – at 100 mA, it is just 6.3 V, well below previously reported values of 9 V or more. This advance stems from optimising the rapid thermal annealing process and adjusting the ratio of two of the common metals used for the *n*-type contact. The team discovered that aluminium should be three times as thick as gold to produce the best anodes with a Ti/Al/Ni/Au stack.



LEDs with an improved anode and a low level of oxygen combine a record-breaking efficiency with a long lifetime.

The team's devices are a relatively conventional design for UVC LEDs. Produced on single-crystal AlN substrates made by Crystal IS, they feature five quantum wells, an electron-blocking layer and a *p*-type GaN contact (see Figure).

Scrutinising the device structure with cross-sectional high-angle annular dark-field scanning electron microscopy reveals abrupt interfaces between all of the layers, and an absence of dislocations, even in the *p*-type contact. The team attributes the lack of dislocations to pseudomorphic growth on low defect AlN substrates.

Measurements of the external quantum efficiency of the LEDs were made on chips thinned to 100 μm, and flip-chip packaged into a surface mount device with a UV-transparent quartz lid.

Driving these packaged devices with 40 μs pulses to avoid self-heating determined external quantum efficiencies of 0.42 percent, 0.36 percent, 0.28 percent and 0.21 percent for LEDs driven at 100 mA and emitting at 237 nm, 235 nm, 233 nm and 230 nm. Corresponding output powers were 22 mW, 1.9 mW, 1.5 mW and 1.2 mW, respectively.

Studies on 20 packaged LEDs driven at 20 mA revealed that after 3600 hours of operation, output power dropped by between 20 percent and 40 percent. Note that these values ignore an initial power drop of 10 percent over the first 46 hours, a typical burn-in period for commercial LEDs.

Goals for the team are to improve the light extraction efficiency and to see if even shorter-wavelength LEDs can deliver useful levels of irradiance. A significant challenge for LEDs with a wavelength of 240 nm or less is realising a high extraction efficiency, because the polarisation of the light tends to cause photons to propagate parallel to the surface of the chip.

"One approach we are examining is to extract the UVC emission from the edge, which may give us a significant increase in light intensity," says Yoshikawa.

Reference

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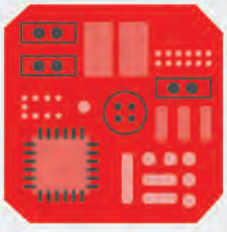


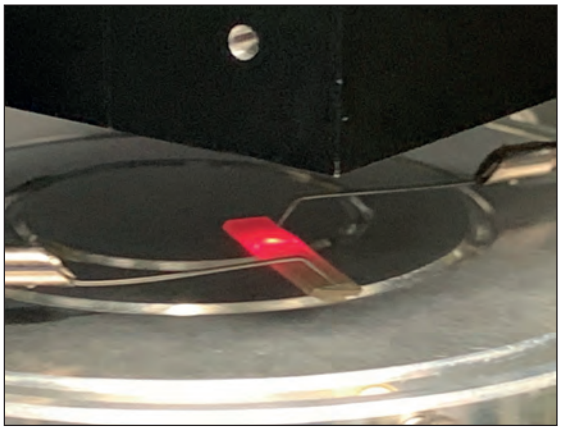
Building brighter red LEDs

Switching the substrate for the growth of red-emitting nitride LEDs from sapphire to gallium oxide increases the efficiency of the emitter

Researchers at King Abdullah University of Science and Technology say that they are taking the performance of red-emitting, InGaN-based LEDs to a new high. The team's LEDs, which emit at around 665 nm, break efficiency records and have an incredibly low forward voltage.

These successes will aid the development of high-performance, GaN-based red LEDs, which could be combined with blue and green cousins to form full-colour microLED displays and phosphor-free white lighting products.

One of the reasons behind the team's success is a switch from the most common substrate used to make GaN-based LEDs, sapphire, to gallium oxide. This move, which replaces the aluminium atoms in the substrate with gallium, reduces lattice mismatch, leading to a lower in-plane stress in the epilayers. In turn, there is an increase in the efficiency of indium incorporation in the InGaN layers – this aids the growth of indium-rich layers, needed to reach longer wavelengths.



Gallium oxide substrates help to propel emission to deep within the red spectral range.

The other key to record-breaking performance in the red is the use of an MOCVD reactor that can produce InGaN epilayers at higher temperatures. "The higher growth temperature realises the higher-quality InGaN quantum wells," explains team spokesman Kazhurio Ohkawa.

For the growth of their red emitters, the team starts with templates purchased from Novel Crystal, Japan. The engineered substrates have a foundation of 680 μm-thick, tin-doped β-Ga_2O_3, and are topped with a pattern of silicon nitride masks that increase light extraction efficiency. Grown over and around the masks – they are 2 μm in diameter, 1 μm high and separated by a 4 μm pitch – is a 5 μm-thick layer of *n*-type GaN.

On this template Ohkawa and co-workers deposit an epitaxial stack that includes: a 15 period undoped superlattice; a blue-emitting quantum well, added to improve the crystal quality of the red-emitting quantum wells; and a red-emitting region that contains two 2.5 nm-thick, $In_{0.35}Ga_{0.65}N$ quantum wells. In this region there is also an 18 nm-thick $Al_{0.15}Ga_{0.85}N$ barrier, designed to deliver strain compensation and increase the external quantum efficiency of the device.

LEDs with dimensions of 650 μm by 250 μm were produce from the epiwafer. These devices feature a 90 nm ITO top contact, added by electron-beam lithography, and a Cr/Ni/Au contact to the *n*-type region, exposed by inductively coupled plasma etching.

Driven at room-temperature, these emitters produce a large blueshift in electroluminescence peak with drive current – it moves from 691 nm at 5 mA to 631 nm at 100 mA. The team attributes this shift to the screening of the piezoelectric field in the active region and band filling of localised states.

At a 20 mA drive current, emission is at 665 nm, a colour described by Ohkawa as "stunning red". He warns that most reports of red LEDs are for devices that only emit between 600 nm and 630 nm, a spectral range with significant overlap with orange – it spans 590 nm to 620 nm. According to Ohkawa, red really begins at 620 nm.

Although the performance of the LEDs produced by Ohkawa and co-workers are record-breaking, the external quantum efficiency at 20 mA is only 0.19 percent. Encouragingly, the forward voltage is just 2.45 V, compared with between 3.7 V and 4.4 V for previous red-emitting LEDs. This substantial decrease is due to improvements in quality and design, according to Ohkawa.

The next goals for the team are to increase the efficiency of their red LEDs, and to produce yellow laser diodes emitting between 540 nm and 600 nm, a spectral range that has not been reached with either InGaN or InGaP lasers.

Reference

D. Iida *et al.* Appl. Phys. Express **13** 031001 (2020)

Droplets spawn single-photon sources

Dots formed by droplet epitaxy and high-temperature crystallisation produce single-photon emission at a telecom transmission window

Researchers at Japan's National Institute for Materials Science are claiming to have produced the first quantum dots by droplet epitaxy that provide single-photon emission at 1.55 μm.

According to team spokesman Kazuaki Sakoda, one of the applications that could benefit from this work is quantum cryptography, using standard optical fibre infrastructure.

He told *Compound Semiconductor* that droplet epitaxy is not a new growth process. "It was proposed in 1991 at our institute. However, thanks to its considerable freedom regarding the choice of materials and substrates, progressive numbers of researchers are now working with this technique."

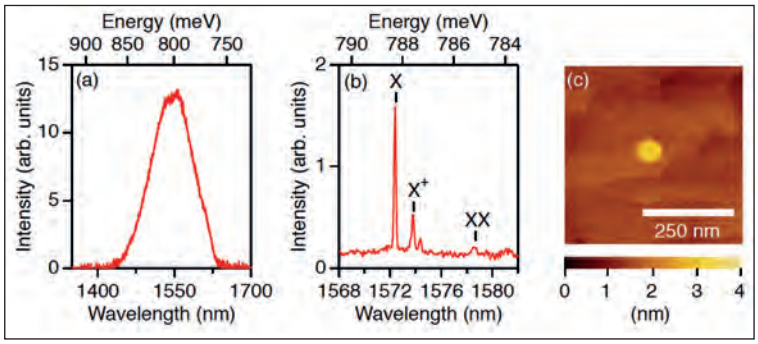
Sakoda and colleagues do not use the Stranksi-Krastanow mode, the more common approach for producing dots, because it creates asymmetric dots that are unfavourable for entangled pair generation.

Back in 2016 the team reported its use of droplet epitaxy to produce dot emission beyond 1.5 μm. However, those InAs dots that were embedded in InAlGaAs had not been optimised, and the dot density was too high to allow one of them to be isolated using standard micro-optics. This sample also suffered from a relatively large distribution in dot size, with careful dot selection needed to find a dot emitting at 1.55 μm.

The team's latest work addresses both of these issues by combining droplet epitaxy with high-temperature crystallisation. The resulting sample, used alongside a state-of-the-art superconducting photon detector, allows the study of single-photon emission dynamics in the standard telecom C-band.

To produce the sample, the researchers loaded an iron-doped InP(111)A semi-insulating substrate into a solid-source MBE tool and grew a 200 nm-thick $In_{0.52}Al_{0.12}Ga_{0.36}As$ barrier at 490 °C, and then a 0.5 monolayer of InAs. After decreasing the temperature to 400 °C, they formed indium droplets by adding a 0.25 monolayer of indium at a growth rate of 1.6 monolayers-per-second, before introducing an arsenic flux into the chamber to crystallise the InAs dots from the indium droplets. After annealing for 5 minutes at 450 °C, the team capped the dots with a 100 nm-thick layer of $In_{0.52}Al_{0.12}Ga_{0.36}As$.

Imaging this sample with an atomic force microscope revealed that the dots are 2 nm high discs with a typical diameter of 48 nm (see figure). Their density is about 6 x 10^8 cm^{-2}.



Luminescence from: (a) a large ensemble of dots, and (b) a single dot excited at 40 nW. The emission lines labelled X, X^+ and XX correspond to neutral excitons, positively charged excitons and neutral biexcitons. (c) atomic force microscopy of a typical dot.

Sakoda and co-workers have investigated the optical characteristics of the dots by placing the sample in a cryostat, cooling it to 8K, exciting the material with a titanium sapphire laser and recording the resultant spectral emission.

Note that the high cost associated with cooling the sample to such a low temperature is acceptable for quantum cryptography, according to Sakoda. "However, other applications, such as medical imaging, surely need higher operation temperatures. This is what we are doing now."

The optical emission from an ensemble of the dots is a Gaussian-like peak with a full-width at half maximum of about 100 nm – this is more than two times narrower than that associated with the work reported in 2016.

Sakoda says that the width of the emission is sufficiently narrow. "We are able to pick up an ideal dot among plenty of dots around the target wavelength of 1.55 micron."

Measurements with a Hanbury Brown and Twiss set-up produce a signal that shows a clear anti-bunching dip, indicating that the probability of emitting two photons at one time is very close to zero.

"In next few months, we would like to demonstrate the emission of quantum entangled pairs," says Sakoda. Once that is accomplished, they plan to develop dot-based LEDs that work at higher temperatures.

Reference

N. Ha *et al.* Appl. Phys. Express **13** 025002 (2020)

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