# CS COMPOUND SEMICONDUCTOR

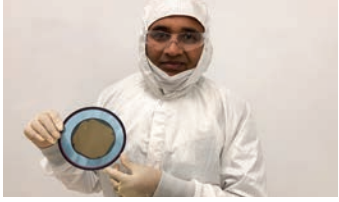
Connecting the Compound Semiconductor Community

Volume 24 Issue 7 OCTOBER 2018 @compoundsemi www.compoundsemiconductor.net

## GaN MMICs empower satellite communication

## Enhancing millimetre-wave radar with GaN

## Manufacturing InP lasers in a GaAs fab

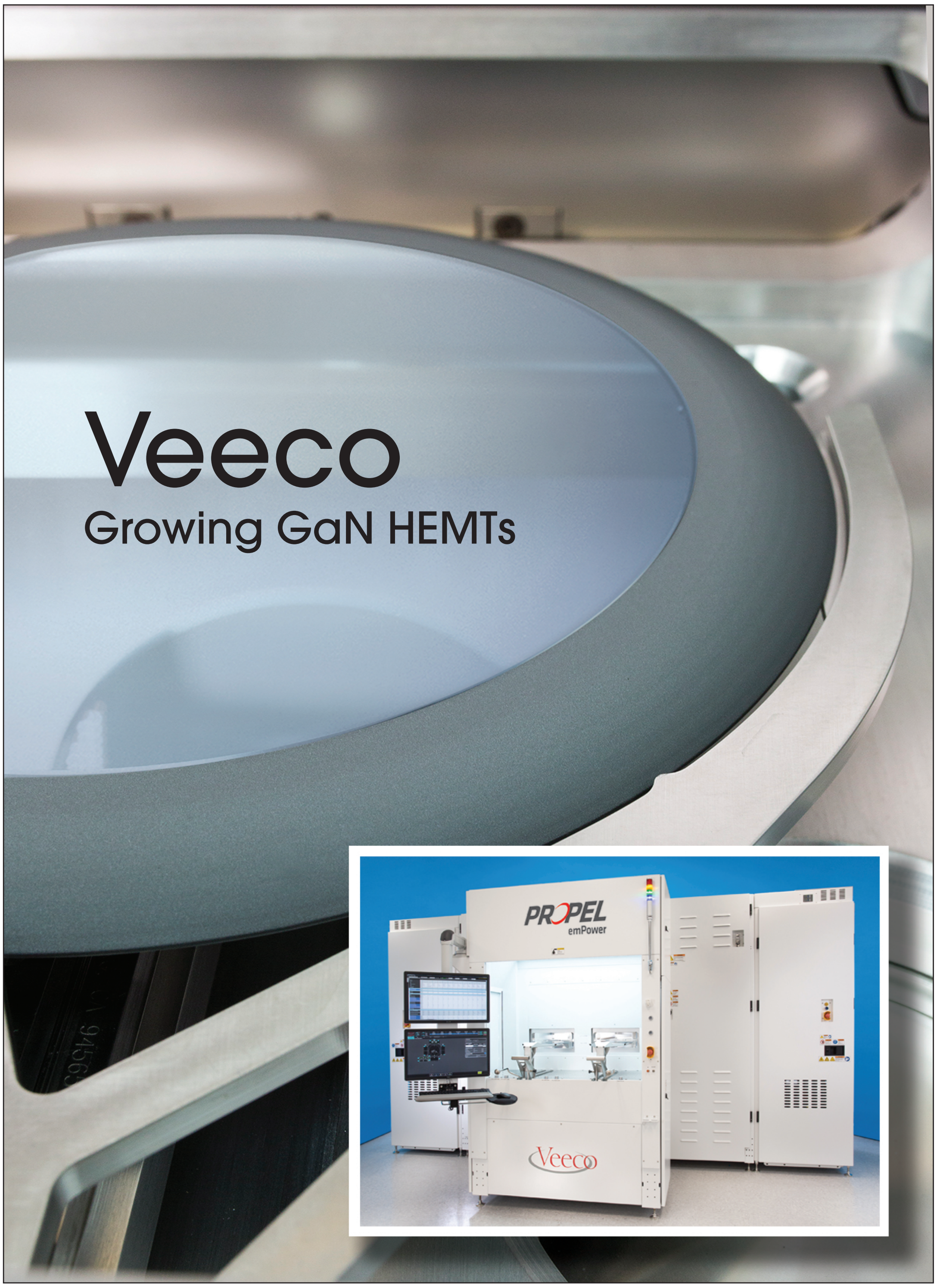


## Branching out from LEDs to a CS foundry

## Unlocking the mammoth potential of microLEDs

# Veeco

## Growing GaN HEMTs



**inside** News Review, News Analysis, Features, Research Review, and much more...
Free Weekly E News round up go to: www.compoundsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

# Viewpoint

By Dr Richard Stevenson, Editor

## Soaring SiC

I GOT A MASSIVE BUZZ attending year's European Conference on SiC and Related Materials (ECSCRM). This industry has just embarked on a golden era, and it was a joy to be surrounded by such optimistic, happy delegates.

One could argue that I should not have been surprised by this. After all, market analysts have been tipping sales of SiC devices and materials to take off for many years. But there have been delays and pushbacks.

Now, however, revenue is undoubtedly rocketing. How do we know? Well, at ECSCRM, spokesman for II-VI and GT Advanced Technologies both told delegates that there is plenty of business for all suppliers of SiC material. Peers aren't rivals anymore – instead, it is silicon that is the enemy.

Helping to take on this foe is Wolfspeed. It's parent company, Cree, is shifting its focus away from the cut-throat LED business to SiC materials and devices. By 2023 Wolfspeed is targeting to quadruple annual revenues from $200 million to $800 million.

Further evidence of a booming industry emerged from the exhibition hall. Far more companies are here than in the meetings of yesteryear, including new players sporting innovative technologies.

Excitement in the exhibition hall hit a new high on the third day of the event, thanks to the arrival of an all-electric Jaguar, the iPACE. This head-turner accelerates from standstill to 60 mph in just 4.5 s, tops out at almost 125 mph, and can cover 292 miles on a single charge.

Today, the power electronics in this Jag is made from silicon. But the fact that representatives of this automaker were at the meeting rammed home the point that the car industry is taking SiC seriously.

The automotive industry is highly conservative, so there's still work to do to generate the test data that proves that when SiC diodes and transistors are deployed in electric vehicles, they are reliabile and robust. But once this is done, and similar demonstrations are provided for planes and electrical grids, growth in SiC sales should not be limited to just the next few years – instead, that era should turn out to be just the tip of the iceberg.

| | | |
|---|---|---|
| **Editor** Richard Stevenson | richardstevenson@angelbc.com | +44 (0)1291 629640 |
| **Contributing Editor** Rebecca Pool | editorial@rebeccapool.com | |
| **News Editor** Christine Evans-Pughe | chrise-p@dircon.co.uk | |
| **Sales Executive** Jessica Harrison | jessica.harrison@angelbc.com | +44 (0)2476 718209 |
| **USA Representatives** Tom Brun Brun Media | tbrun@brunmedia.com | +001 724 539-2404 |
| Janice Jenkins | jjenkins@brunmedia.com | +001 724-929-3550 |
| **Publisher** Jackie Cannon | jackie.cannon@angelbc.com | +44 (0)1923 690205 |
| **Director of Logistics** Sharon Cowley | sharon.cowley@angelbc.com | +44 (0)1923 690200 |
| **Design & Production Manager** Mitch Gaynor | mitch.gaynor@angelbc.com | +44 (0)1923 690214 |
| **Circulation Director** Jan Smoothy | jan.smoothy@angelbc.com | +44 (0)1923 690200 |
| **Chief Executive Officer** Stephen Whitehurst | stephen.whitehurst@angelbc.com | +44 (0)2476 718970 |

**Directors** Bill Dunlop Uprichard – EC, Stephen Whitehurst – CEO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway

**Published by** Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 E: info@angelbc.com

Compound Semiconductor is published eight times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/e158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50.

US mailing information: Compound Semiconductor, ISSN 1096-598X, is published 8 times a year, Jan/Feb, March, April/May, June, July, August/September, October, November/ December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. The 2018 US annual subscription price is $198. Airfreight and mailing in the USA by agent named Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Periodicals postage paid at Jamaica NY 11431. US Postmaster: Send address changes to Compound Semiconductor, Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Printed by: The Manson Group. ISSN 1096-598X (Print) ISSN 2042-7328 (Online) © Copyright 2018.

Volume 24 ISSUE 7 OCTOBER 2018

# CONTENTS

## 16 COVER STORY

### Mastering MOCVD of GaN HEMTs

Veeco's Propel single-wafer MOCVD system is ideal for developing and manufacturing RF and power electronics: it has a very high up-time; an incredibly wide processing window; and it has the capability to create epiwafers with great uniformity, excellent doping profiles and very sharp interfaces

## 22 From LED maker to CS foundry

Sanan is branching out from LED manufacturing with foundry services for power, RF and optical devices

## 28 SiC industry embarks on a golden era

SiC production is ramping so fast that all those involved will reap the rewards

## 34 GaN empowers satellite communication

GaN enables powerful, compact transmitters for demanding satellite communications

## 40 Making InP lasers in GaAs fab

Costs come down when InP lasers are produced on a 4-inch GaAs line

## 48 Propelling MEMS VCSELs into the mid-infrared

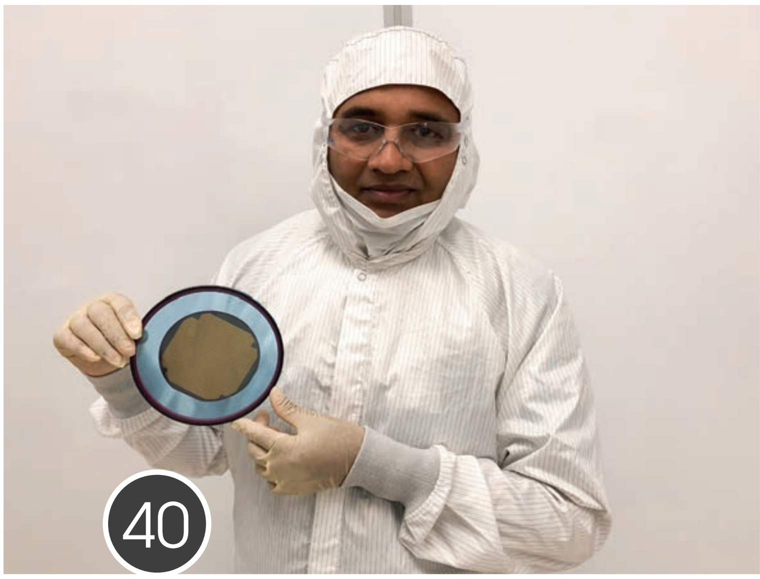
For gas sensing in the mid-infrared, the MEMS VCSEL is the ideal source: it is low in cost, provides great spectral purity, and offers wavelength tuning that is fast and wide

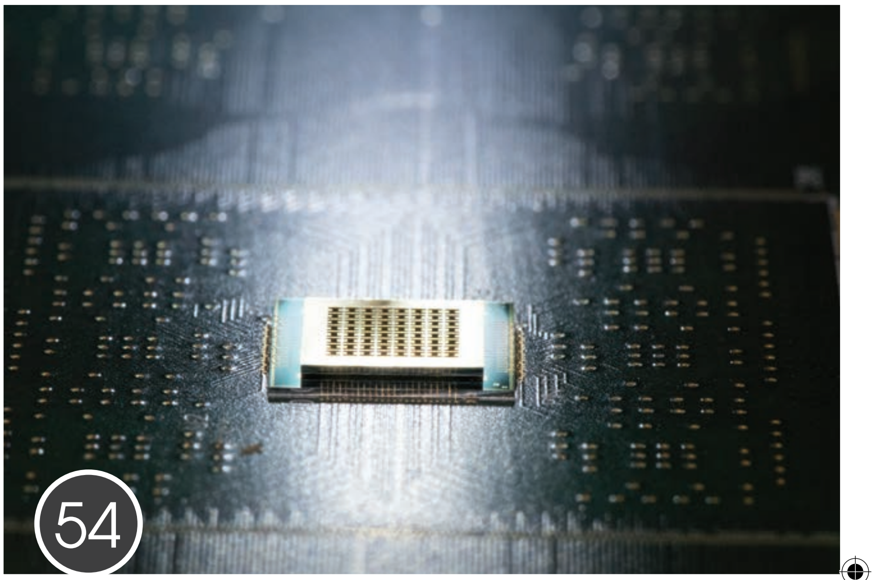
## 54 Enhancing millimetre-wave radar with GaN

Three-dimensional heterogeneous integration of GaN and silicon creates promising arrays for 235 GHz radar


22


34


40


54

## news

06 BAE and US Air Force Lab sign GaN agreement

07 EU PIC project to develop next generation chemical sensors

08 SETi files patent infringement litigation

09 Plessey to work with JDC on microLEDs

10 Dowa samples highest power short-wavelength IR LEDs


08

## news analysis

### 12 GaAs solar cell to challenge efficiency records

Magnolia Optical Technologies teams with DARPA to take single-junction, GaAs solar cell efficiencies to 30 percent and beyond

### 14 MicroLEDs with mammoth potential

First came Samsung's 'The Wall', followed by LG's counter-offer that raises the bar even further


12

## research review

### 59 Equipping InGaN solar cells with tunnel junctions

Combining MOCVD and MBE creates the first InGaN solar cell with a tunnel junction

### 60 Perfecting trenches in GaN with photo-chemical etching

Photo-chemical etching of GaN yields deep trenches with smooth sidewalls and a high aspect ratio

### 61 Streamlining single-facet coupling

A U-shaped waveguide with a Euler spiral aids hybrid photonic integration

# BAE and US Air Force Lab sign GaN agreement

BAE SYSTEMS has signed a cooperative agreement with the Air Force Research Laboratory (AFRL) for Phase 1 of a technical effort to transition GaN semiconductor technology developed by the US Air Force to its Advanced Microwave Products (AMP) Centre.

As part of the effort, BAE will transfer and further enhance the technology, and scale it to 6-inch wafers to slash per-chip costs and improve the accessibility of this defence-critical technology. Under the agreement, BAE will work with AFRL to establish a 140-nanometer GaN MMIC process that will be qualified for production by 2020, with products available to Department of Defense (DoD) suppliers through an open foundry service.

"Millimeter-wave GaN technologies today are produced in research and development laboratories in low volumes at high associated costs or in captive foundries that are not broadly accessible to defence suppliers," said Scott Sweetland, Advanced Microwave Products director at BAE Systems. "This effort will leverage AFRL's high-performance technology and BAE Systems' 6-inch manufacturing capability to advance the state of the art in GaN MMIC performance, reliability, and affordability while providing broader access to this critical technology."

The work on this project will primarily take place in BAE's 70,000-square-foot Microelectronics Centre (MEC) in Nashua, NH, where engineers research, develop, and produce compound semiconductor materials, devices, circuits, and modules for a wide range of microwave and millimetre-wave applications. The MEC has been an accredited DoD Category 1A Trusted Supplier since 2008, and fabricates integrated circuits in production quantities for critical DoD programmes.

As part of the project, the AMP Center team will work closely with the company's FAST LabsT research organization and MMIC design experts from ENGIN-IC.

# Module packaging driven by SiC and GaN

THE INTRODUCTION of the wide bandgap semiconductors SiC and GaN is pushing the development of new power module packaging solutions, according to a new report by the market research and strategy consulting company, Yole Développment.

The power module packaging industry is currently worth $1.2 billion, a little more than a third of the total power module market. The market's CAGR between 2017-2023 will be 8.2 percent, coming close to a $2 billion business opportunity by 2023.

"It is a very dynamic market, where continuous innovations and material enhancements and a lot of R&D investment are needed", comments Alejandra Fuentes Suarez, technology and market analyst at Yole.

SiC technologies are expected to reach 29 percent CAGR between 2017 and 2023.

The latest Model3 inverter from Tesla is one example, showing the added-value of STMicroelectronics' SiC power module, reverse engineered by System Plus Consulting (a Yole company). The module contains two SiC MOSFETs with an innovative die attach solution and connected directly on the terminals with copper clips and thermally dissipated by copper baseplates.

System Plus Consulting's report, *Automotive Power Module Packaging Comparison 2018* details the physical composition and cost of ten modules for automotive applications from five different manufacturers. Analysts reviewed the different topologies and techniques used for the module packaging. Under this new report, System Plus Consulting's analysts highlight the specificities of each solution, defined by the car makers."There is not yet a standardised package in automotive application" comments Farid Hamrani, cost engineer at System Plus Consulting.

With two major technical trends, over-molded double-side cooled modules for hybrid cars and single-side cooled modules with pin-fin baseplates for full electric cars, this industry is dominated by IGBT power modules. "The IGBT power module market grew 18.1 percent in 2017", said Milan Rosina, senior technology and market analyst, Power Electronics & Batteries at Yole. "No doubt today, that IGBT modules are driving the power module packaging materials business."

Indeed 2017 was an impressive year for the IGBT power module market. And 2018 perspectives are even better, with over 20 percent growth in the first half of the year. The main explanation of this drastic market explosion is the boost from the EV/HEV sector, especially in China. It has also been an exceptional year for industrial motor drives in Asia. In parallel, other device modules, like those based on MOSFETs and bipolar transistors, show a slight decrease.

Consequently the overall power module market is expected to be over $5.5 billion in 2023. This promising market is directly beneficial for the packaging material business.

# EU PIC project to develop next gen chemical sensors

LETI, a research institute of CEA Tech, has announced the launch of the REDFINCH consortium to develop the next generation of miniaturised, portable optical sensors for chemical detection in both gases and liquids. Initial target applications are in the petrochemical and dairy industries.

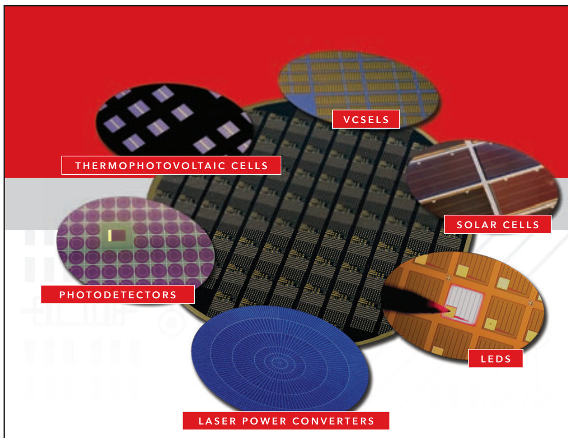
The consortium of eight European research institutes and companies will focus on developing novel, high-performance, cost-effective chemical sensors, based on mid-infrared photonic integrated circuits (MIR PICs). Silicon PICs create extremely robust miniature systems, in which discrete components are replaced by on-chip equivalents.

This makes them easier to use and reduces their cost dramatically, expected at least by a factor of 10. To develop these chemical sensors, the consortium must overcome the significant challenge of implementing these capabilities in the important mid-infrared region (2-20 μm wavelength range), where many important chemical and biological species have strong absorption fingerprints.

This allows both the detection and concentration measurement of a wide range of gases, liquids and biomolecules, which is crucial for applications such as health monitoring and diagnosis, detection of biological compounds and monitoring of toxic gases.

"Despite the mid-infrared wavelength region's importance for a wide range of applications, current state-of-the-art sensing systems in the MIR tend to be large and delicate. This significantly limits their spreading in real-world applications," said Jean-Guillaume Coutard, an instrumentation engineer at Leti, which is coordinating the project.

"By harnessing the power of photonic integrated circuits, using hybrid and monolithic integration of III-V diode and interband cascade and quantum cascade materials with silicon, the consortium will create high-performance, cost-effective sensors for a number of industries." In addition to Leti, whose expertise includes the design and manufacture of PICs on a 200 mm pilot line and integrated photoacoustic cells on silicon, the consortium members and contributors include: Cork Institute of Technology (Ireland) – PIC design & fabrication, hybrid integration; Université de Montpellier (France) – Laser growth on silicon, photodetector growth; Technische Universität Wien (Austria) – Liquid spectroscopy, assembly/test of sensors; mirSense (France) – MIR sensor products, laser module integration; Argotech a.s. (Czech Republic) Assembly/packaging of PICs; Fraunhofer IPM (Germany) – gas spectroscopy, instrument design/assembly; and Endress+Hauser (Germany) – process gas analysis and expertise, testing validation.



# SETi files patent infringement litigation

UV LED specialist Sensor Electronic Technology – part of Seoul Semiconductor and Seoul Viosys – has filed a patent infringement lawsuit against both Bolb and Quantum Egg in the US District Court for the Northern District of California.

In its complaint, SETi asserts that Bolb and Q-Egg are selling UV LED steriliser devices that infringe on six LED patents. The asserted patents cover fundamental technology for UV LEDs, encompassing UV LED steriliser structures and drivers, chip fabrication, and epitaxial layer growth. SETi is a pioneer in the UV LED industry. Since its establishment in 1999, it has been dedicated to the research and development of patented UV LED technologies. SETi's expertise in the UV LED area has been recognised with numerous government project grants focused on UV LED technology, including for the US Defense Advanced Research Projects Agency (DARPA).
SETi has also collaborated with Seoul Viosys, a UV LED company based in South Korea. This collaboration has resulted in the development of Violeds technology, an innovative, clean technology suitable for disinfection, deodorisation, phototherapy, and curing with the use of UV LEDs. Violeds technology has reportedly been used by the National Aeronautics and Space Administration (NASA) aboard the International Space Station.

The market value of these UV LED technologies has been growing exponentially. In 2017, the projected value of the UV LED market was estimated at $223 million and is tipped to increase to $1.224 billion by 2022 – a growth rate of more than 33 percent per year. The UV LED appliance market has similarly expanded to numerous fields, including curing machines, medical devices, and purification devices. In particular, the sterilisation and purification market is projected to increase significantly over the next few years.

"SETi strongly opposes the distribution of products in the market that infringe our patents. For this reason, our company will be undertaking enforcement actions against suspected infringers where appropriate and necessary," stated SETi officials.

"While SETi is pleased to see market growth for UV LED technologies, it is important that such growth is accompanied by fair competition, including respect of intellectual property," the officials continued. "SETi believes that an increasing number of products in the marketplace infringe on SETi's established patents. In order to protect its valuable intellectual property, SETi has committed to monitoring the market for patent infringement and engaging in enforcement activities."

# Emcore introduces laser module for 5G wireless

EMCORE, a provider of advanced mixed-signal optics for networks and defence systems, has introduced the Model 1998 cooled, coaxial DFB laser module for next-generation wireless fibre optic link applications.

The 1998 laser module features wide bandwidth above 6 GHz and is designed for 5G wireless, Distributed Antenna Systems (DAS), L-Band and S-Band signal distribution. The model 1998 and Emcore's complete line of lasers and optical receivers for wireless were displayed at the Mobile World Congress Americas (MWCA), at the Los Angeles Convention Centre.

The migration to 5G wireless networks is fast approaching with Verizon's planned deployment of its fixed wireless 5G in up to five markets by the end of 2018, and 5G hotspots from AT&T expected by late 2018. Full-blown 5G smartphones are expected to be launched in the first half of 2019.

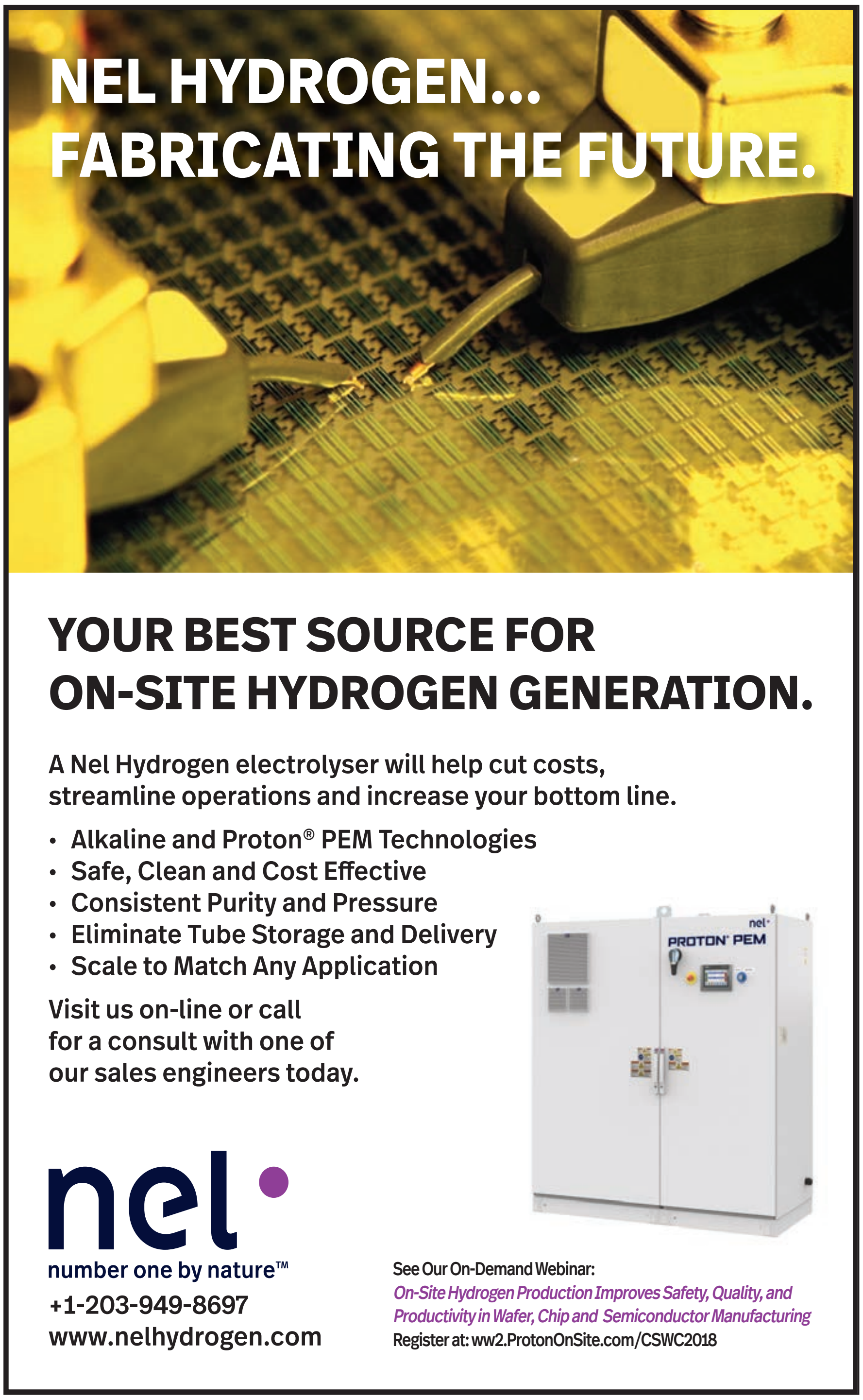
Emcore's new 1998 is an ultra-linear, coaxial 1550 nm DFB laser module optimised for 5G wireless remoting fibre optic links. It is designed to enhance bandwidth and signal integrity for delivery of consistent, reliable wireless signals.

The laser is packaged in a compact, hermetic, cooled TOSA (Tunable Optical Sub-Assembly) with monitor photodiode, thermistor, TEC (Thermoelectric Cooler), optical isolator and flex circuit for integration into various transmitter configurations. It delivers superior optical performance over an enhanced temperature range of -40°C to +85°C.

"Our new 1998 laser builds upon Emcore's long history of high-performance designs for CATV, wireless and high-speed digital applications and will continue to raise the performance bar in linear fibre optic transmission for emerging 5G networks," said Gyo Shinozaki, VP of marketing for Emcore. "With bandwidth above 6 GHz, the 1998 will deliver maximum high-speed signal integrity for 5G, DAS and long-distance fibre optic link networks," added Shinozaki.

At MWCA, Emcore will also show its 1618A and 1718A, 6.5 GHz DFB laser modules and its 5200 Series 3 and 6.5 GHz fibre optic links.

The 1618A and 1718A lasers are packaged in Emcore's classic 14-pin butterfly cooled laser form-factor and deliver highly-linear, superior optical performance at 1310 nm and 1550 nm wavelengths. The 5200 series are a compact, weatherproof fibre optic transmitter and receiver pair for Inter-Facility Link (IFL) applications where high-performance under demanding conditions is critical.



# Dowa samples highest power short-wavelength IR LEDs

TOKYO-BASED Dowa Electronics Materials has successfully developed short-wavelength-infrared LED chips with output power 3.5 times higher than existing products. It has started delivering samples.

The figure of 6.8 mW (with 350 µm square size, applying a direct current of 100 mA at room temperature) is believed to be the highest ever output power for this kind of device. Peak wavelength is 1300 nm.

LED-based optical sensors feature advantages such as a smaller size, lower power consumption and longer life time. In addition, because near and short-wavelength-infrared light with a wavelength range between 800 nm and 2,000 nm is highly penetrative to organisms, the application of short-wavelength LEDs are proceeding in fields such as agricultural and food analysis, medicine and healthcare. In particular, in the field of healthcare, the market for which is set to expand rapidly, LED-based sensors are expected to enable to measure blood glucose level without blood drawing.

The newly developed short-wavelength-infrared LED chips can balance higher output power and a smaller chip size, which are usually a trade-off, and are significantly improved in optical output, which is required for sensor applications.

Dowa will expand these technologies to peak wavelengths of 1450 nm and 1650 nm, widening the lineup.

In the field of gallium-based compound semiconductor, Dowa offers a portfolio ranging from materials, such as high-purity gallium, to wafers, LED chips and some lamp modules. Dowa also has abilities to flexibly accommodate a variety of needs, such as customising wavelengths.

Dowa will focus on enhancing the features of next-generation products and streamlining production to further expand its semiconductor business.

# HLJ expands VCSEL production with Aixtron tool

AIXTRON has announced that Taiwanese VCSEL epitaxy and chip manufacturer, HLJ Technology has ordered multiple AIX 2800G4-TM MOCVD sets to increase its wafer capacity as well as its epitaxial wafer size production line from 4-inch to 6-inch for high-volume manufacturing of VCSELs.

Aixtron's fully automated Planetary Reactor systems will be supplied in 8 x 6-inch configuration in the course of Q4/2018 and beyond.Larry Lai, General Manager of HLJ, comments: "In order to meet fast growing market demand for VCSEL both at epi wafer and chip levels, we decided to expand to 6-inch epi wafer manufacturing. Starting from Q4/2018, two sets of newly ordered Aixtron MOCVD systems are scheduled to arrive at HLJ. In Q2/2019, the first complete high-volume VCSEL production line will be ready."

"We are very pleased that our new customer HLJ has picked the AIX 2800G4-TM system as it offers best-in-class high-volume VCSEL epi and chip manufacturing processes," says Bernd Schulte, president of Aixtron SE.

"Looking forward to our cooperation with HLJ, we will support the company in the alignment of their production processes to our equipment technology in the best way possible."

# CST Global adds InP epitaxial overgrowth capability

CST GLOBAL has added an in-house InP epitaxial overgrowth capability to its foundry production services. The process is critical to the manufacture of high-volume, DFB lasers used in world-wide, passive optical network (PON) markets.

InP epitaxy is deposited using a vapour-phase epitaxy process, applied by CST Global's commercial, MOCVD reactor.

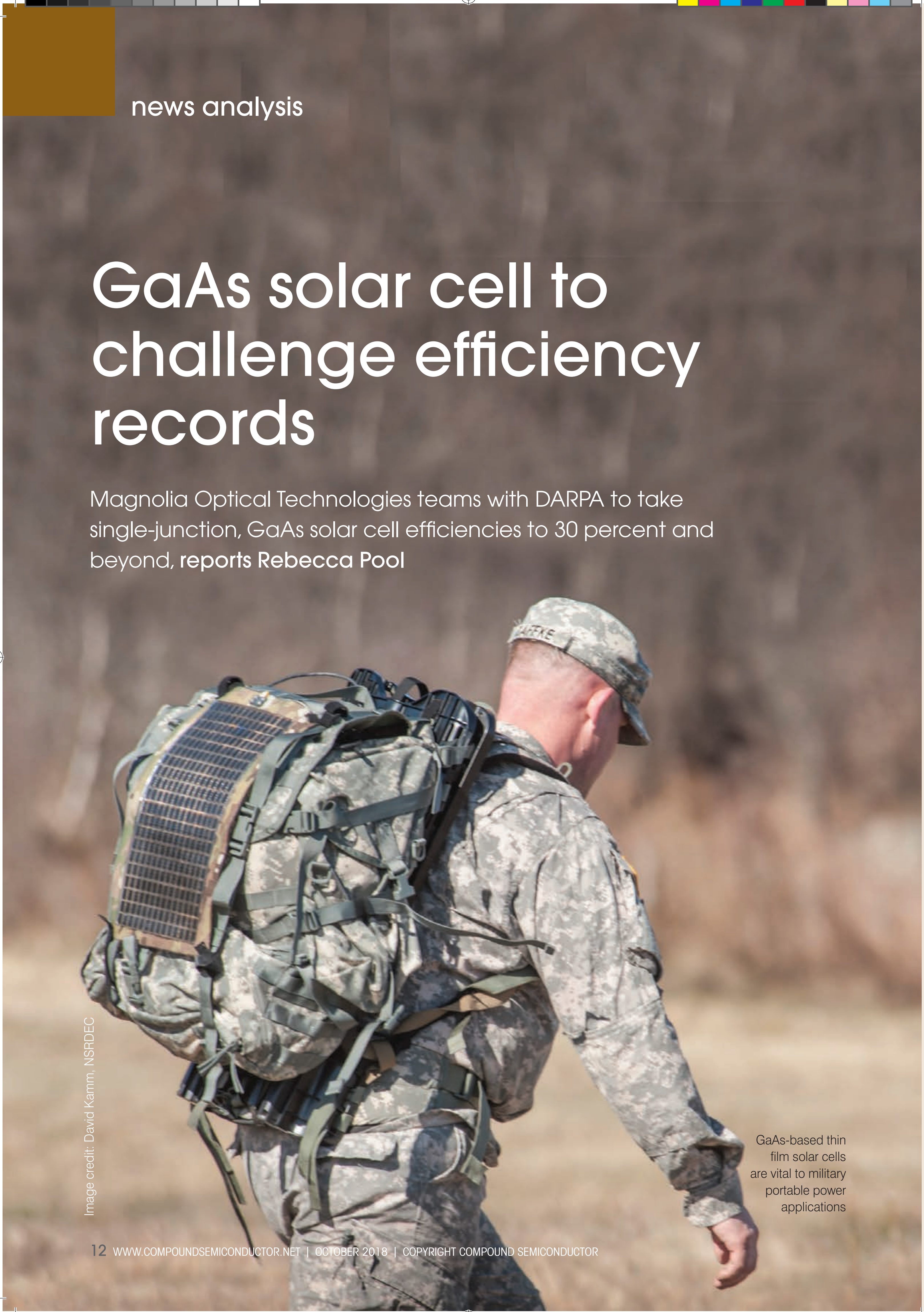
Euan Livingston, VP sales and marketing at CST Global said: "Adding InP epitaxial overgrowth to our foundry capability brings a critical production process in-house, where previously it was out-sourced. It not only mitigates production bottlenecks, but also reduces DFB laser production times."

"Over the past year, we have significantly increased the capacity of our factory in Blantyre, Scotland, to meet the high demand for DFB lasers used in PON markets."

"Epitaxial overgrowth is a challenging process to master. We recognise that the combined expertise of our development and operations teams has been essential to the successful introduction of this new process."

# GaAs solar cell to challenge efficiency records

Magnolia Optical Technologies teams with DARPA to take single-junction, GaAs solar cell efficiencies to 30 percent and beyond, **reports Rebecca Pool**



GaAs-based thin film solar cells are vital to military portable power applications

Image credit: David Kamm, NSRDEC

EARLIER THIS YEAR, Magnolia Optical Technologies revealed it is working with DARPA to develop high efficiency GaAs-based solar cells for military portable power, as well as potential drone and space applications.

Following many years of research on thin-film structures, Ashok Sood, President of Magnolia, is confident the $1.5 million project, part the of DARPA Phase II Small Business Innovation Research Programme, will deliver the cost-effective, highly efficient solar cell that industry craves.

“The goal of the program is to develop high-efficiency, thin GaAs-based solar cells that are cost-effective to produce for soldier’s portable power applications and maintain performance over changing environmental conditions,” he says. “We are in the process of demonstrating this capability with DARPA... we know it can be done.”

Today’s technology-of-choice for photovoltaics in space, the III-V multi-junction solar cell, packs a powerful punch for its weight, with decades of research having raised efficiencies to more than 30 percent.

Multi-junction devices use multiple bandgaps, or junctions, that are tuned to absorb a specific region of the solar spectrum. A high-bandgap top cell absorbs high energy photons while a slightly lower bandgap material, placed beneath, absorbs lower-energy, longer-wavelength photons. Typical multi-junction cells use two or three absorbing junctions, with the maximum efficiency increasing with the number of junctions.

But while multi-junction solar cell efficiencies have raised many an eyebrow, so have the costs. The devices’ many thick, complex epitaxial layers are expensive to fabricate, leaving this high-cost solar cell largely up in Space.

What’s more, multi-junction solar cells are highly sensitive to changes in the solar spectrum; not so helpful back on Earth, where the spectral distribution of incident light varies wildly throughout the day, and year.

Efforts to tackle these issues are gathering momentum, with, for example, NASA having funded research to increase photon collection at the top cell as well as integrate III-V cells onto silicon. However, Sood and Magnolia chief technology officer, Roger Welser, are taking a different approach.

Focusing on single-junction solar cells, rather than multi-junction devices, the researchers are exploiting nanostructures to deliver cost-effective, efficient III-V devices with a favourable power-to-weight ratio.

To this end, they are embedding novel designs of quantum dots or wells into III-V absorber layers, with these nanostructured absorber layers then being incorporated to the single-junction cells.

Efficiencies of today’s GaAs-based single-junction devices come in at more than 26 percent, and using absorber layers can extend the infrared absorption of such devices, boosting conversion efficiencies to a theoretical high of 40 percent. The figure would be fantastic, but as Sood puts it: “If we can get anywhere around 30 percent on a single junction with these quantum structures, then that will be a very big event.”

## The problem with III-V nanostructures

Efficient photovoltaic energy generation demands device structures that can absorb a wide spectrum of incident radiation – including infra-red wavelengths – while extracting the photogenerated carriers at high voltages. Nanostructured quantum well and quantum dot solar cells hold vast promise here, because, as Sood and Welser emphasise: “The nano-enhanced III-V absorber layers provide a pathway to extend infrared absorption.”

Given this, Sood and colleagues have been designing solar cells with novel quantum well profiles that they reckon will raise efficiencies towards 30 percent and beyond.

Tailoring the compositional profile of InGaAs wells is known to suppress the recombination losses that deplete efficiency. So with this in mind, the researchers have been growing various types of step-graded quantum wells and inserting these into absorbing layers to inhibit this phenomenon further and extend infrared absorption.

According to Sood, their experiments on solar cells with novel step-graded well structures show promise, although he is yet to be drawn on performance figures.

“We are working with DARPA and demonstrating a prototype device to show that we can really do this,” he says. “If we can use our quantum structures and quantum dots in single-junction solar cells to get the same kind of performance as triple-junction devices, that is going to be a big thing.”

Following the DARPA Phase II SBIR Program, Sood and colleagues intend to work with industry players to develop their technology further for portable power and Space applications for the military.

“The photovoltaic market is growing rapidly with a wide range of defence and potential commercial applications,” says Sood. “Commercialisation has to be our next step.”

# MicroLEDs with **mammoth potential**

First came Samsung's 'The Wall', followed by LG's counter-offer that raises the bar even further. But will these demonstrations led to super-sized micro-LED TVs reaching our homes anytime soon, **asks Rebecca Pool**

IN SEPTEMBER, South Korean electronics giant, LG, introduced a gargantuan 175-inch microLED TV for ultra-large display applications, in response to Samsung's 146-inch beast, 'The Wall', launched in January this year.

As display markets get ready for, literally, the next big technology, Samsung has secured its supply of micro-LEDs from Taiwan-based PlayNitride while industry reports indicate LG is sourcing chips from Epistar, Taiwan, and HC SemiTek, China.

"This industry sector is in its early stages but is growing and developing very, very fast," highlights n-tech Research analyst, Boris Kobrin. "Commercialisation has only started this year, but all the major display businesses and OEMs are working on prototypes, which are now being brought to the market."

Micro-LEDs based on InGaN semiconductors and developed by Hongxing Jiang and Jingyu Lin, then at US-based Kansas State University, first emerged at the turn of this century. Research swiftly continued far and wide and come 2012, Sony had released its 55-inch 'Crystal LED Display', comprising around 6 million microLEDs. Larger iterations have followed from Sony, Samsung and now LG, while industry players keenly anticipate further devices from Apple and Facebook.

"Scalability is the draw for micro-LEDs in these extra-large displays," points out Kobrin. According to the analyst, next generation digital cinemas demand high dynamic range, super-high density, high brightness and contrast displays that state-of-the-art projectors and screens just can't offer. Meanwhile, laser colour video displays are expensive, while manufacturing OLED displays beyond some 65 inches is technically challenging as well as costly.

"However, microLEDs offer extraordinary contrast, brightness and scalability," says Kobrin. "More than 98 percent of a pixel is empty space, as the tiny pixel contains a very tiny microLED... so [system] cost doesn't scale with area, it actually scales with resolution, which is a big deal for these huge-area displays."

"Displays in digital cinemas and home theatres are going to be dominated by microLEDs due to these capabilities that you just cannot find in any other technology, not even the OLED," he adds.

But micro-LEDs markets are not all about size. While the latest TV behemoths promise higher-than OLED brightness at a near-LCD cost, the actual microLED also provides tip-top power efficiency, high contrast, high brightness and a longer lifetime than the OLED.

Given this, Kobrin reckons the near-eye augmented reality/virtual reality projector market is one to watch. "This application requires very high resolution, high brightness and contrast as well as low weight and a small form factor," he says. "The microLED provides all of these needs very well."

Factor in anticipated demand from the smart watch market as well as automotive head-up displays, and Kobrin predicts that the global microLED market will swell from $2.7 billion in revenue in 2019, to a hefty $10.7 billion in 2022. Still, challenges exist.

Quality variability across GaN wafers has plagued manufacturers, although, for example, companies such as US-based Optovate are developing selective array transfer processes to deal with this issue. At the same time, problems over display drivers as well as faltering efficiencies for smaller microLEDs are also reportedly being solved.

For Kobrin, a key issue has been ‘mass transfer’. Super-high resolution, contrast and brightness applications, namely extra-large displays and near-eye AR/VR projectors, require very high pixel density displays that are difficult to manufacture using traditional pick and place transfer processes.

Here, the microLED display is assembled, one sub-pixel at a time, onto a CMOS backplane. So, for a 4K television with some 25 million sub-pixels, this is time-consuming and expensive. What’s more, many pick and place processes can, at best, only handle 50 μm pixels, but future displays will house pixels with smaller sizes.

Thankfully, as Kobrin highlights, myriad companies have been springing up to deliver a range of mass transfer manufacturing processes in which thousands and thousands of sub-pixels are simultaneously moved from a sapphire or silicon donor carrier to the display substrate.

For example, US start-up, Uniqarta, has developed a ‘Laser Enabled Advanced Placement’ process in which a laser transfers dies from a carrier to a substrate at a rate of up to 100 million units an hour. This is orders of magnitude faster than traditional pick and place processes.

Meanwhile SelfArray, US, is pioneering a ‘directed self-assembly’ process in which LED dies, covered with a pyrolitic graphite film and placed onto a vibrating magnetic stage, align with the magnetic field, and are then transferred to the display substrate. The company claims, once mature, the technology will manufacture a 4K TV in minutes.

“We need to see huge numbers of chips being transferred, even for small devices,” says Kobrin. “The finished technology does not exist, but companies are developing processes and I would expect to see some of these acquired by large corporations, such as Facebook and Google.”

“It is also not yet obvious which technology will win but to me, it looks like the laser-based transfer technologies have the advantage,” he adds.

But as issues are ironed out one by one, supply chain chinks remain under close review by many in the industry. It’s no secret that the complex and lengthy micro-LED display supply chain remains fragmented as combining LED production with display manufacturing and assembly has not been easy.

“It is not certain at this point how this issue will play out,” says Kobrin. “Will the large players take charge and create a vertically integrated structure... or will the semiconductor foundries reconfigure and update lines with the required epitaxial growth? This now needs to be seen.”

# Mastering MOCVD of GaN HEMTs

Veeco's Propel single-wafer MOCVD system is ideal for developing and manufacturing RF and power electronics: it has a very high up-time; an incredibly wide processing window; and it has the capability to create epiwafers with great uniformity, excellent doping profiles and very sharp interfaces

BY VINOD MERAI FROM VEECO INSTRUMENTS

THERE IS NO DOUBT that GaN is a great material for making electronic devices. It enables high power densities, great efficiencies and elevated operating temperatures; it sports high levels of mechanical stability, hardness, and thermal conductivity; and it has a very low sensitivity to ionizing radiation. Armed with these attributes, GaN devices are unlocking the door to a new generation of commercial products that are far smaller, lighter and less power hungry than their predecessors.

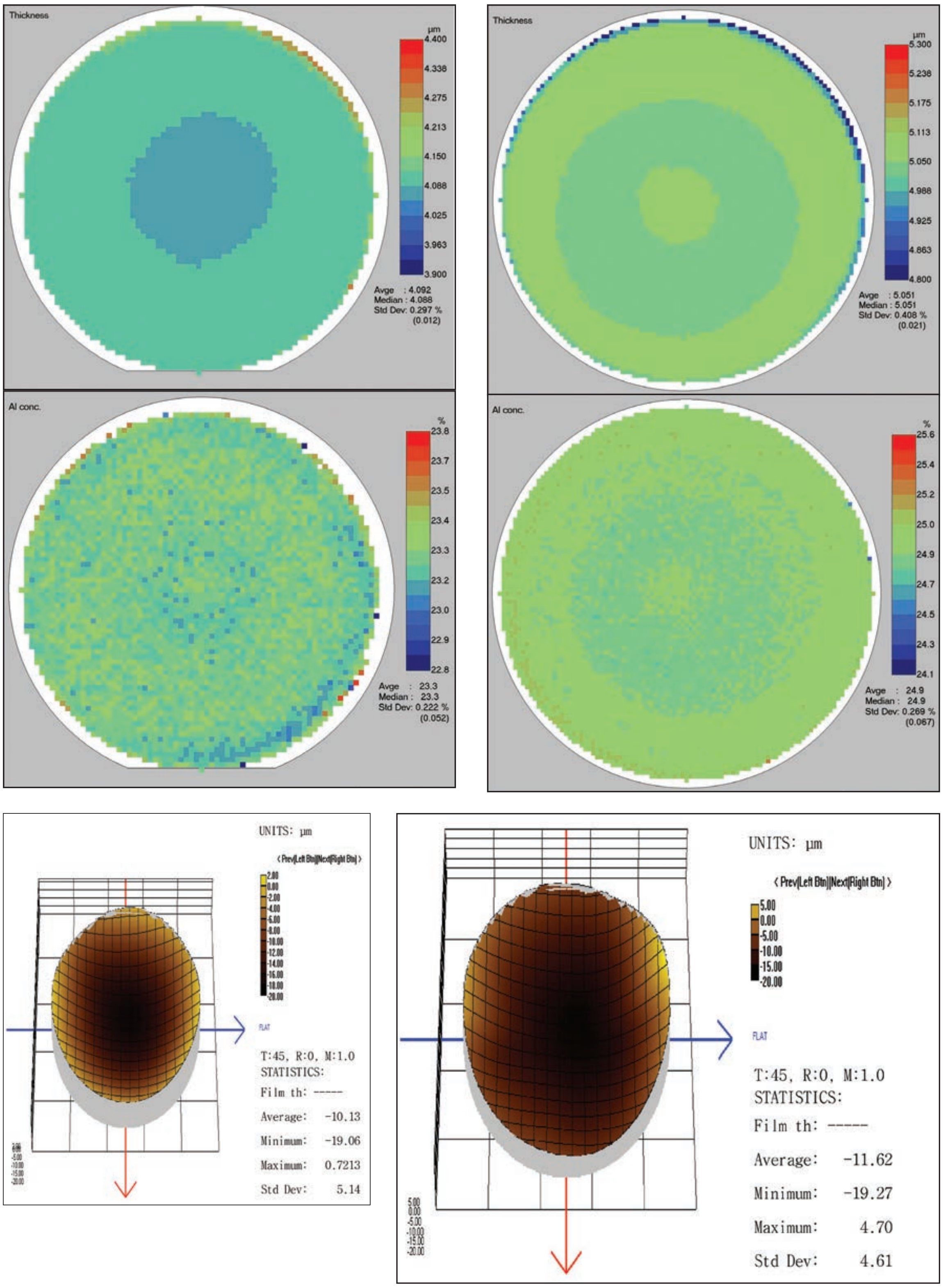
One sector where these devices are making an impact is power electronics. Here, concerns relating to integration and reliability are getting retired, and sales are on the up, thanks to the superior performance and smaller form factors offered by GaN over the incumbent technology, silicon. Revenue is tipped to rocket over the next few years, according to many market research firms including Yole Développement in its Power GaN report, 2017 edition (see chart). Primary drivers include growing sales of devices that operate at around 200 V and are used for the likes of wireless charging, LiDAR and class D amplification, alongside those at around 600 V to 700 V that are used in power supplies in data centres and electric and hybrid electric vehicles.

The other significant sector for GaN electronics is RF. The impending roll-out of 5G is great news for the makers of these devices, which are already being

used in base stations, and could extend their reach into micro and metro cells and potentially on to femto-cell/home routers and eventually handsets.

In both the power electronics and the RF sectors, the dominant GaN device is the HEMT. This device, which can be grown on a SiC substrate but is increasingly on silicon, is vastly superior to the silicon MOSFET, thanks to a breakdown field that is higher by an order of magnitude, a higher electron mobility, and a higher power efficiency at high frequencies. These strengths enable the GaN HEMT to produce a high current density and fast switching with a low drain-source resistance – and to ultimately lead to a smaller footprint device with high-temperature operation and low conduction and switching losses.

That's not to say the GaN HEMT is perfect. Production of this device – including costs for epitaxy and downstream device processing and packaging – is higher than that for the silicon MOSFET. What's more, performance is hampered by charge trapping and current collapse, issues that are being actively resolved to fulfil reliability targets.



Veeco's Propel MOCVD System provides excellent within-wafer uniformity on 6-inch (left) and 8-inch (right) wafers in terms of (from top to bottom) thickness, composition, and bow control.

## A single-wafer solution

At Veeco Instruments we are addressing all these needs of the makers of GaN-on-silicon HEMTs with our Propel MOCVD System. This single-wafer tool may raise a few eyebrows, given the historical usage of batch tools in the compound semiconductor industry. However, our approach follows in the footsteps of those taken in the silicon semiconductor industry, which has switched from batch silicon epitaxy tools to single-wafer successors to realise best-in-class performance.

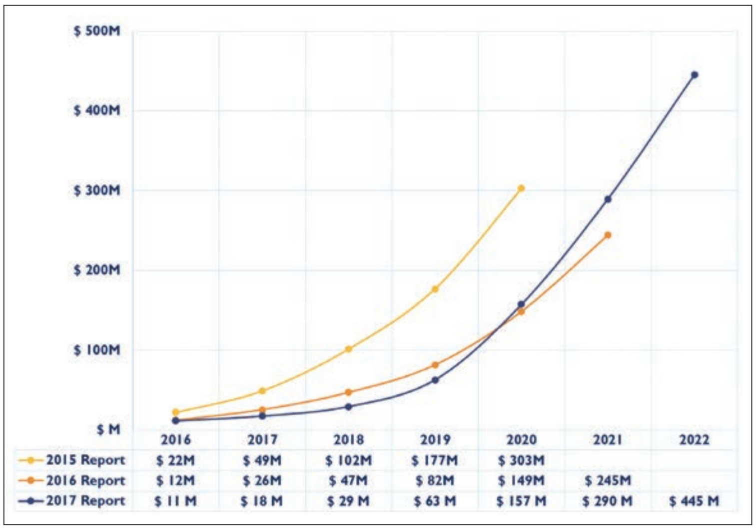
Great performance goes hand-in-hand with very competitive production costs. Using the Propel System, our engineers have demonstrated epitaxial stacks for RF and power devices that meet performance targets at the lowest competitive overall cost, in the context of both development and production environments.

One of the reasons that production costs are so low is that the growth rates with the Propel System are up to double those for batch tools. The higher growth rate, realised without compromising crystal quality and reducing the total cost per wafer, is due to the high dynamic range of the V/III ratio injected across the substrate.

Helping to drive down production costs is the method of operation for the Propel tool: it is held in vacuum throughout the production campaign. This eliminates the need to open the chamber, and aids the use of longer production campaigns – they can exceed 120 runs. Operating in this manner, uptime can be more than 90 percent.

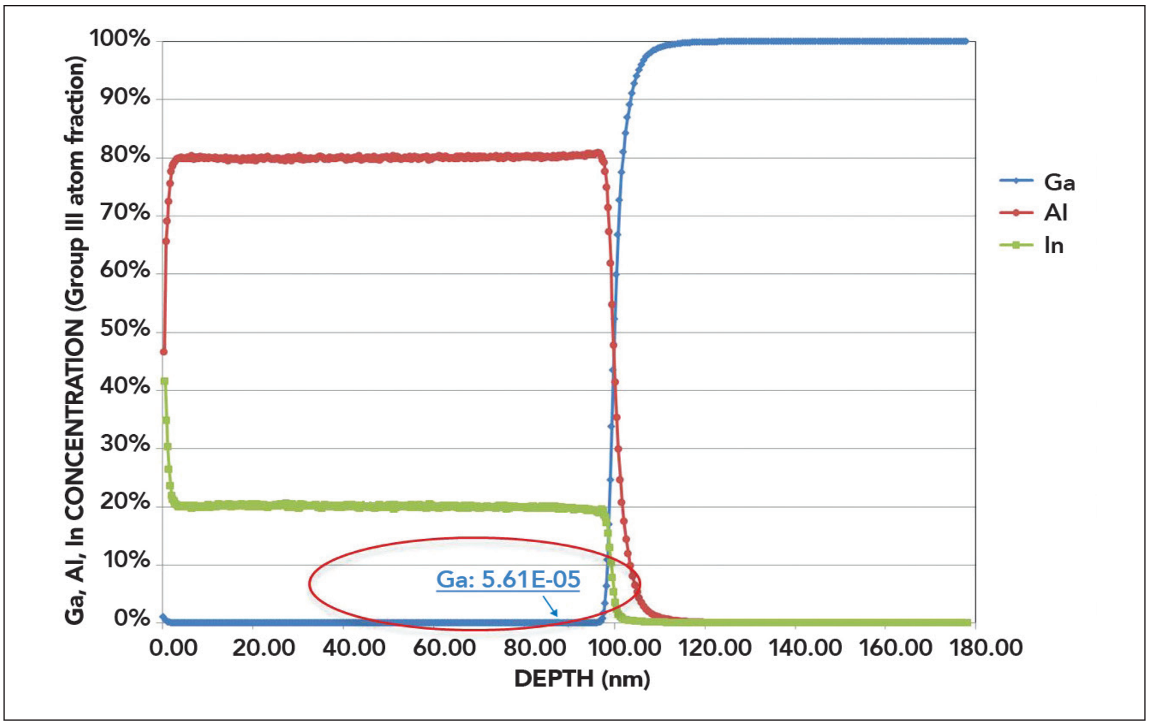
To trim running costs even further, we have designed the Propel System so that minimal parts are required for operation. Our users benefit from the lowest consumables cost compared with other MOCVD systems, thanks to improved wafer carriers and particle filters. With our single-wafer system, the injector remains clean at all times, making it ideally suited to both R&D and production.

We know that when our customers are developing new products, they need MOCVD tools that have wide process windows, so that they can explore the entire process space; and faster learning cycles with reduced numbers of processed wafers. Most current batch systems fail to do so. That's a major impediment, because it severely limits the development and hampers further optimization of GaN HEMTs for power and RF applications.
Within the silicon industry, single-wafer tools are used in a multiple chamber configuration. So that our customers can enjoy the same benefits, we have designed the Propel System to be used within our multiple chamber system, to provide the highest yield and uptime.

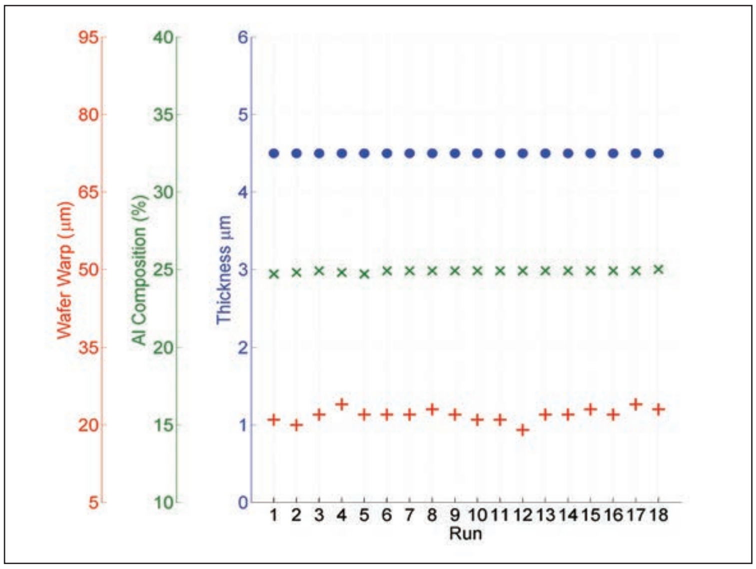


Market analyst Yole Développement is predicting that the GaN device market will rocket over the next few years

For success in the market place, it is essential to combine low production costs for the GaN HEMT with



The sharp interface enabled by a single-wafer Propel MOCVD System provides a high two-dimensional electron gas mobility. Higher mobility in turn enables higher threshold voltage and frequency response with lower on-resistance and current leakage, enhancing device reliability.



Veeco's Propel MOCVD System provides predictable outcomes for GaN applications in both development and production environments.

high performance. So it is critical that the epilayers of the chip are high in quality and have excellent uniformity and run-to-run stability, to ensure production of consistent products with a high yield. The Propel System helps engineers to excel in this endeavour.

## Propel's pedigree

Part of the reason behind the success of the Propel System is that it draws on established, high-performance technology developed over many years. For example, Veeco's TurboDisc technology provides best-in-class composition uniformity for the AlGaN and InAlN barrier layers. And within-wafer uniformity is designed into the tool, by leveraging complete elimination of residual carrier effects, combined with our proprietary Uniform FlowFlange and SimmHeat technology. Additional key features are seamlessly integrated bow measurements, direct on-wafer temperature control and the siting of the pre-cursor injector zone away from the boundary layer – together, these features help to ensure run-to-run stability for a wide range of process conditions.

Uniformity of the doping is also far better with the Propel System. Thanks to uniform injection, uniform carbon doping can be realised consistently from the centre of the wafer to its edge. That's not the case for cross-flow-based systems producing linear depletion. With smaller substrates, complex impertinent layers can be added to tackle this issue. However, that's not so easy with larger substrates.

This doping uniformity results in sharp interfaces, which is further aided by the use of uniform injection across the substrate, and very low residency times. In contrast, planetary systems employ linear depletion, and have residency times that are up to ten times longer, leading to inferior interfaces.

Uniform injection and very low residency times also help to ensure no memory effects. This freedom equips the engineer with the opportunity to incorporate dopants such as magnesium and iron, and to optimize doping levels across multiple runs. It is a feature that is highly valued for both R&D and high-volume production.

In comparison, to eliminate memory effects in systems that inject pre-cursors into the boundary layer, such as showerhead and cross-flow reactors, engineers have to determine and optimize both *in-situ* baking and conditioning requirements for each stack. This severely limits R&D teams in their process window optimization.

Another asset of the Propel System is that it frees engineers from undertaking run-to-run particle management. No longer is there a need to develop and maintain chemical cleaning steps between epistack growths. Instead, inherent low particle adders are in place, ensuring best-in-class device yields.

## Future proofing

Customers want to be able to use our tools for many years. To enable this, we have future-proofed the Propel System. Today, GaN transistors tend to be grown on 6-inch silicon, and over the coming years 8-inch wafers will become more common. The Propel platform configuration accommodates both sizes, and has the head room to go to even larger wafers.

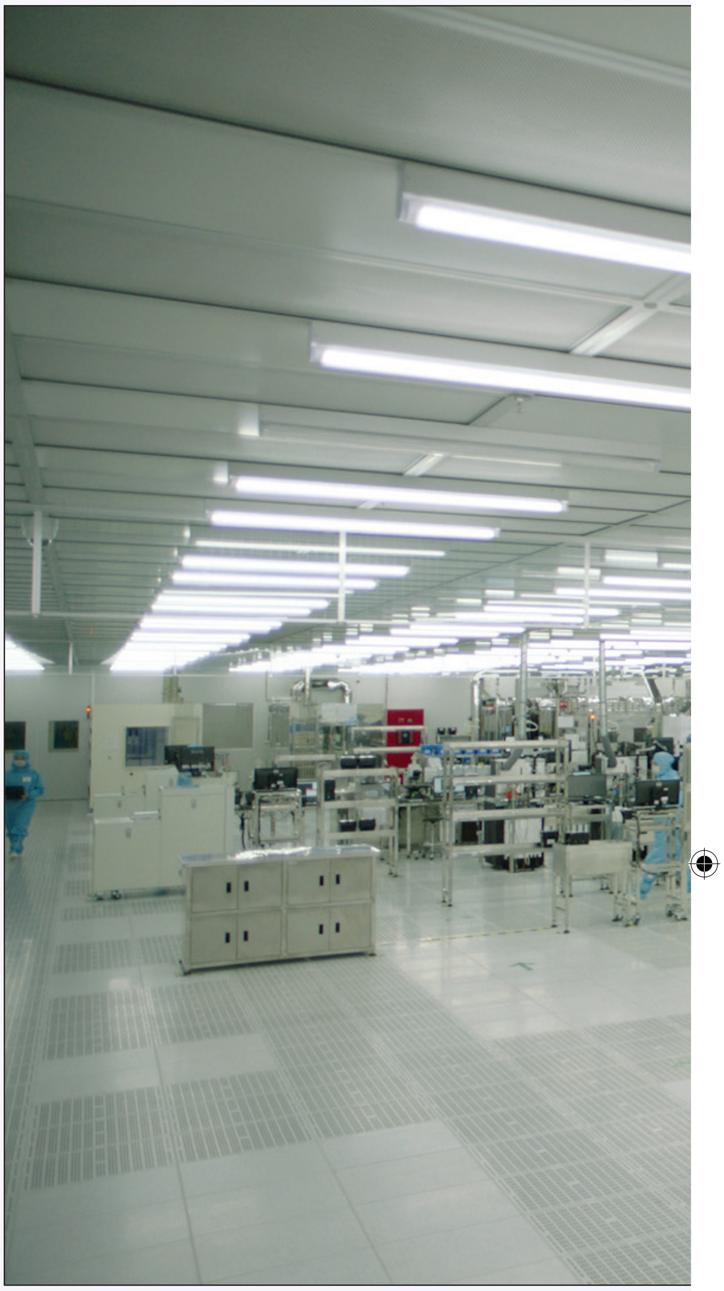
Migrating to larger wafers is a challenge with some batch reactors. Due to their cross-flow design, depletion across the wafer surface restricts scaling to 8-inch wafers. But with the Propel platform, 8-inch wafers can be produced with the same uniformity and bow control as 6-inch wafers. This capability gives the engineers working with 8-inch wafers a highly versatile knob for reducing device costs. Not only are epi costs lower for 8-inch; chipmakers can generate additional savings in downstream processing and packaging costs.

Given its capability on many fronts, the Propel System is undoubtedly the ideal tool for supporting the ramp in production of GaN-on-silicon HEMTs for RF and power applications. Its merits include a very wide process window; ground breaking throughput; the lowest cost of ownership; and thanks to single-wafer TurboDisc technology, industry-leading dopant control and compositional uniformity.

Armed with these attributes, leading device companies and research institutes that we collaborate with are able to tackle the tough challenges of maximising transistor performance, trimming RF loss and harmonic distortion, and improving device reliability. Using the Propel System, these engineers are equipped with superior film-deposition control for buffer quality improvement, and are able to incorporate hard-to-deposit materials, such as magnesium and iron. More importantly, these engineers can fulfil their goal of creating a highly repeatable manufacturing process that achieves high final device yield – a feat that cannot be accomplished with such success with a batch system.

# From **LED maker** to CS foundry

Sanan is branching out from LED manufacturing with foundry services for power, RF and optical devices. Discussing the motivation for this move, as well as the goals and implications, is **Raymond Biagan, Director, North American Sales and Marketing Communications for Sanan Integrated Circuit (Sanan-IC).**



Q **Sanan Optoelectronics is the biggest LED chipmaker in China, with more than half of the domestic market. What is behind the launch of the foundry, Sanan Integrated Circuit, which started in 2014?**

A We want to leverage our leadership and years of high-volume, high-scale GaAs and GaN [LED] epiwafer manufacturing knowledge and expertise. We see RF, power electronics, optical and filters equally as high-volume as LEDs.

We have a large pool of MOCVD reactors from the Sanan Optoelectronics parent company's LED-chip business. From there we want to expand and explore other high-volume, high-spec lateral markets, such as RF devices for 5G cellular, IoT, Wi-Fi, 5G sub-6 GHz, power electronics – that is the high-current, high-voltage FETs and diodes used in data centres and wireless charging – and also optical. Optical includes photodiodes and VCSELs.

Q **What types of foundry services are you offering?**

A We are a process technology platform provider of compound semiconductor foundry services and are open to various types of contract manufacturing and business models, from epiwafer, fabrication, processing and DC chip probe to full-up RF known-good-die test services. We're open to any of these contract manufacturing sub-services including processing of consigned epiwafers. In RF, we carry GaAs

HBTs, pHEMTs, BiHEMTs, integrated passive devices and well as SAW/TC-SAW filters. We will also offer InP HBTs. For power electronics, we have GaN-on-silicon, and SiC-on-SiC. For optical, we carry GaAs and InP for the photodiodes, VCSELs and edge-emitting laser diodes.

**Q Are you working with large companies, small start-ups, or both?**

A We service both. It's our intent and our mission to serve and focus on high-volume applications in the areas of RF, power electronics and optical. So we naturally reach, engage and seek out these fabless semiconductor companies and integrated device manufacturers who focus on these high volumes. But we are also quite aware of the upcoming and merging start-ups that serve such markets.

**Q Do you have a minimum order size?**

A For mass production, our 6-inch wafer offering comes in 18 wafers per lot. We require a one-lot minimum and a lot multiple. For R&D engineering we can support any low-volume quantity up to the point of production.

**Q Hoe much of your business is overseas?**

A We initiated our sales and go-to-market strategy in mainland China, as our fab and headquarters is in China. But starting this year we have

Sanan IC factory in Xiamen City, Fujian, China; the country's first 6-inch compound semiconductor wafer foundry.

expanded our sales and marketing efforts beyond China to the rest of the world.

**Q How do you protect the IP of your customers?**

A To ensure and gain confidence of our customers, and the confidentiality of our GDS2 design database, we have been ISO 27001 certified. So we have strict compliance to IP and database security management control, and procedural systems for the customer's hardware, old wafers and samples, their software, and their GDS design databases.

**Q Your manufacturing capability is on a 6-inch line. Do you see that as an advantage?**

A Historically, compound semiconductor manufacturing has been on 2-inch and 4-inch. 6-inch is not new, but it's more recent. 6-inch capability, with backward compatibility to a 4-inch line, is what we offer. That benefits high-volume production. It's quick to ramp up.

**Q When a customer works with you, how long does it take from placing an order to receiving the first product?**

A Once the GDS2 is uploaded in job view, it takes five-to-seven days to produce the mask, depending on the mask layers. Then we initiate the wafer start with the mask set on. Typically, from wafer start to wafer out could go as soon as two weeks – what we call a super-hot lot. Our customers are loving their R&D engineering efforts running on a few weeks' turnaround for engineering wafers.

This is a key selling point compared with an external foundry. For GaAs, other foundries might have a couple of weeks longer lead time. But in the context of our GaAs pHEMT competing with silicon-on-insulator for switches and low-noise amplifiers, that world is more a 20-week standard lead time. Maybe a super-hot lot is 14-16 weeks at best.

Sanan IC wafer fabrication engineers processing compound semiconductor wafers.

**Q You ship full wafers and diced wafers on blue tape. Do you have partners that can provide a packaging service?**

A We don't have a specific partner to recommend to our customers. Most of the back-end suppliers for packaging and test are in domestic China, or surrounding countries like Malaysia, Taiwan and South Korea. So logistically, it helps to be shipping from our Xiamen fab to the local region for the back-end suppliers.

In the context of packaging and test, we do have a roadmap in support of copper pillar. That's coming out in Q2, to be able to support those platforms and wafers that need chip-scale package type die.

**Q Are your engineers able to offer expertise, in terms of device design?**

A We do not have in-house capability for device design. We are strictly a foundry service. Device design is more product orientated.

We do outsource and contract out limited bare-bones devices for the purposes of sampling for customer evaluation. For example, when we get customer interest in high-output-power power amplifiers, they typically want to go beyond the standard unit cell samples. They want to see some power cell samples – where these are high outputting power amplifiers – to check power handling and output power capability. So we do outsource the development, for sampling purposes, of power cells.

**Q What characterisation is undertaken for the final product?**

A When we ship die, we have DC probe test results, and we quantify the yield per wafer. We can share and review our test limits and test criteria with our end customers, which will correlate to our final test data of our products.

**Q Do you test every die?**

A We do 100 percent of the product die on a given wafer for DC chip probe. If the chip probe yield is high, the test percentage can be reduced or skipped, like for HBT products to minimize test time and therefore cost. We do have RF testing capability at the die level, but there is a cost that would be incurred for that.

**Q What are your capabilities for failure analysis?**

A We have quite an extensive failure analysis lab that benefits from learned knowhow and experience from our parent company. Our lab is equipped with multiple machines, including focused ion beam; we also support transmission and scanning electron microscopy. We have a polisher, a chemical decapsulation machine, a laser decapsulation machine and emission microscopy.

**Q Tell me a little bit about the strengths of your HBT technology?**

A Sanan IC provides competitive HBT process technologies with dry etch and ledge with 0.5 micron for high power gain, compared to the conventional process with wet ledge with 1.0 micron. We also provide devices with both high linearity power and high ruggedness VSWR through epi structure design.

These performance benefits can be used for applications such as Wi-Fi 11ac/ax and 4G/5G sub-6 gigahertz power amplifiers. We are also developing InP HBT, complemented by 0.15/0.1 micron pHEMT for future 5G millimetre-wave power amplifier applications.

**Q What is your product portfolio for power devices?**

A We offer GaN-on-silicon and SiC epi on SiC.

For GaN-on-silicon, we offer a 650 volt power GaN E-mode FET primarily intended for high power density and high efficiency AC-to-DC and DC-to-DC converters in fast charging portable chargers/adapters and electric vehicles, followed by low voltage versions – 200 volt, 100 volt and 60 volt – for more consumer-orientated AC-to-DC and point-of-load DC-to-DC power supplies such as wireless charging and backplane switch-mode power supplies for data centres and base stations. Under development is an E/D mode MISFET with two flavours: 650 volt and 1.2 kilovolt.

On the SiC side we offer different voltage and current ratings for Schottky barrier diodes. These devices could work hand-in-hand with high-power silicon IGBTs, silicon super-junction MOSFETs or SiC MOSFETs. The SiC Schottky barrier diodes come in flavours of 650 volt and 1.2 kilovolt. They range from 2 amps to 40 amps on the 650 volt. For 1.2 kilovolt, we have 10 amp and 20 amp versions. Again, these are primarily targeted to similar applications, ranging from PV inverters, electric-vehicle charging, industrial motor drivers, power factor correction and so on.

The headquarters of Sanan Integrated Circuit (Sanan IC) features China's first 6-inch GaAs wafer fab.

Beyond SiC Schottky barrier diodes we have a roadmap to support MOSFETs next year. We are looking at 900 volt and 1.2 kilovolt, to fill out our portfolio of high-voltage switches.

**Q What is your line-up for optical products? And how will this expand in the coming years?**

A Today, for optical we have a hybrid model. We have a traditional foundry, but at the same time our optical device division offers optical devices such as photodiodes, edge-emitting laser diodes and VCSELs.

For more advanced products, we plan to also offer electro-modulated lasers and tunable lasers in the future. For VCSELs, it will be other flavours – not just for consumers who need sensing, but for industrial applications. We also have plans for high-power lasers for medical and industrial [applications]. Our path to expand further is to commit to technology breakthroughs and innovation through collaborating with universities and the optical industry, where we'll have strategic initiatives and alliances.

**Q What are the goals for the foundry for the rest of this year and beyond?**

A Our goal for the rest of the year is to expand our customer engagement beyond China, into APAC, North America and Europe. We've started doing that for the last few months.

Our goal and vision is to support high-growth markets such as 5G, cellular, IoT, data centre and electric vehicle. We will continue to track those markets and react to their technical requirements and capacity requirements.

Equally important for us as we ramp up is to get worldwide market acceptance. This means good quality process technologies; good, stable, high production capability; high quality control and reliability.

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

# CS INTERNATIONAL 2019 CONFERENCE DATES & SPEAKERS ANNOUNCED!

Preparations for CS International 2019 have got off to a tremendous start, with a record breaking number of industry leading speakers and sponsors already confirmed to participate with 6 months to spare.

Returning to the Sheraton Airport Hotel in Brussels on 26-27 March 2019, the highly regarded CS International Conference, which is in its ninth year will once again bring together key players from the compound semiconductor industry from across the supply chain for two-days of technical tracks and exhibit opportunities.

With an attendance in 2018 of over 350 senior level delegates including representatives from Sony Corporation, imec, Veeco and AIXTRON among many others, the event hit record numbers for attendance.

CS International is part of AngelTech, a brand which delivers insightful, engaging and high-valued conferences that have tremendous synergy. The current line-up, attracting more than 600 delegates, consists of co-located Compound Semiconductor (CS) International, Photonic Integrated Circuits (PIC) International, and Sensor Solutions International (SSI).

Delegates can choose to dip in and out of every session to put together their own tailor-made programme by selecting from over 100 invited talks, delivered by leaders of the most innovative companies within their sector. Those attending can also spend time at the exhibition hall, supported by over 60 companies detailing the latest advances in materials, equipment and software; and play their part in two awards ceremonies, which acknowledge the most important breakthroughs within these industries.

## 5 New Themes for 2019:

### Targeting transportation

Can the strengths of SiC drive its adoption in electric vehicles? And what are the opportunities for III-V optoelectronics in the cars of today and tomorrow?

### Pushing the performance envelope

Where will heterogeneous integration take us? And how can we extract the ultimate performance out of wide bandgap semiconductors?

### Speeding communication

Are faster lasers going to lead us into a new era of communication? Or will it be the build out of 5G?

### Propelling the power electronics revolution

How can the manufacture of SiC devices evolve, so that they capture a greater share of the power electronics market? And what are the opportunities for the GaN-on-silicon HEMT?

### Opportunities for LED and lasers

Can the MicroLED make an impact? And what are the emerging markets for visible lasers?

**Speakers confirmed to date include:**
AIXTRON, ASAHI KASEI, Attolight, Beneq, Enkris Semiconductor, EpiGaN, IBROW Project, Evatec, Exalos, Ferrotec, GaN Systems, IEMN, IHS Markit, II-VI, imec, Integra, Intengent, KLA-Tencor, Nanometrics, Nanotronics, Nanowin, National University of Singapore, Qorvo, Revasum, Rohm Semiconductor, Sino-Nitride Semiconductor, Sony Corporation, Strategy Analytics, Veeco, WIN Semiconductors, X-Fab Semiconductor, Yole Développement

# Book your place NOW!

**www.csinternational.net/register to secure your place**

**It's set to be another sellout**

## PLATINUM SPONSORS

AIXTRON
attolight™
Beneq
CATAPULT Compound Semiconductor Applications
EpiGaN
FerroTec
KLA-Tencor
nanometrics
nanotronics
Nanowin 苏州纳维科技有限公司 Suzhou Nanowin Science and Technology Co.,Ltd
Revasum
中镓科技集团 SINO NITRIDE
Veeco
YOLE Développement

## GOLD SPONSORS

Accel-RF Instruments Corporation
BRUKER
CS CLEAN SOLUTIONS
ims chips
IQE
LAYTEC Knowledge is key
Panasonic
VEM Vacuum Engineering & Materials

## WIFI SPONSOR

BROLIS SEMICONDUCTORS

## PORTFOLIO SPONSOR

Plasma-Therm

## DELEGATE BAG SPONSOR

qorvo
all around you

## SUPPORTED BY

EPIC European Photonics Industry Consortium

angel tech

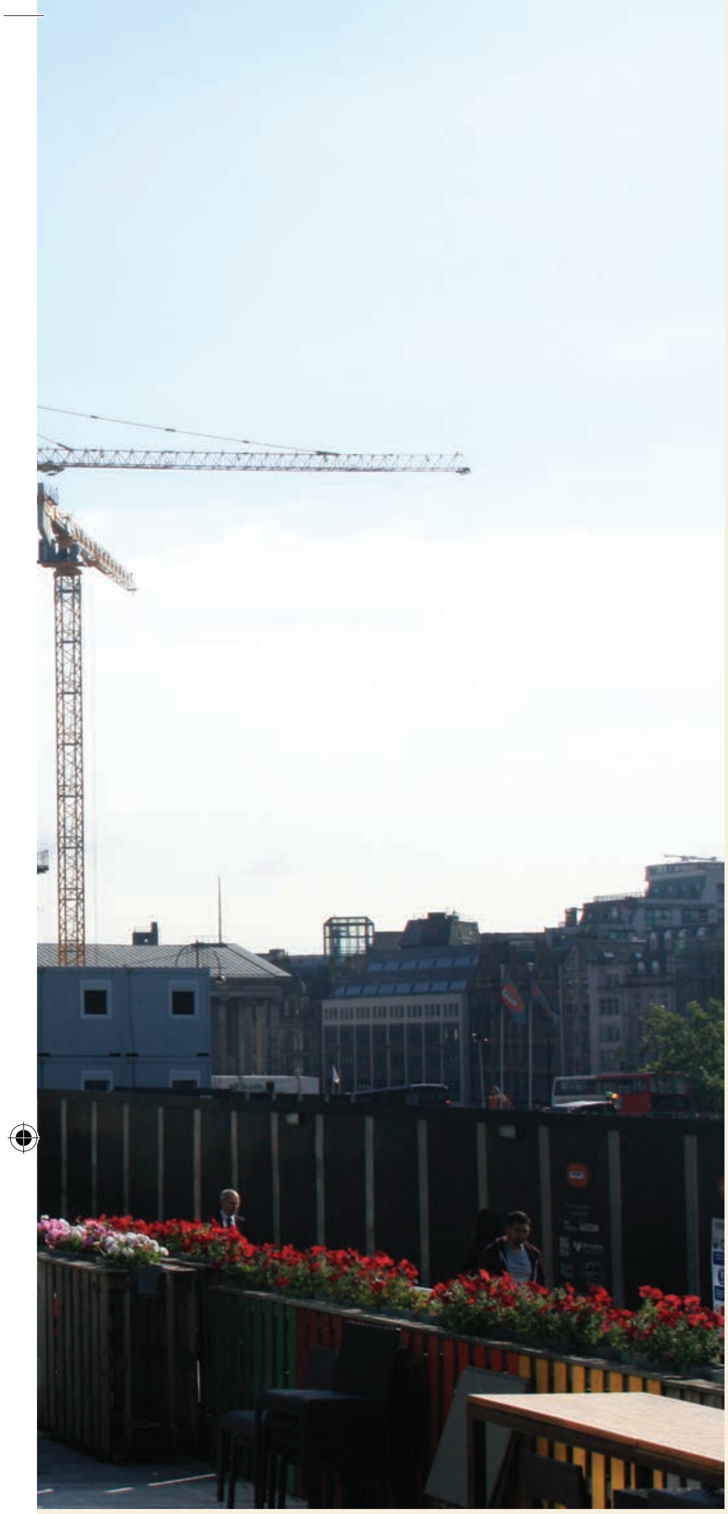
## 3 Conferences, 2 Days, 1 Ticket

CS INTERNATIONAL CONFERENCE
PIC INTERNATIONAL CONFERENCE
SSI INTERNATIONAL CONFERENCE

# SiC industry embarks on a golden era

SiC production is ramping so fast that all those involved will reap the rewards

BY RICHARD STEVENSON



ON THE UP is the city of Birmingham, located in the heart of the UK. Cranes crowd its skyline, helping to re-generate a centre that will be bold, confident and self-assured. For those living and working here, the emerging architecture is shaping an optimistic view of the future.

Falling in to the beat of this city are those that came here this September to attended the twelfth European Conference on SiC and Related Materials (ECSCRM). Like its predecessors, this conference covered ways to identify and classify defects. But this topic no longer takes centre stage – that position is now occupied by leading makers of SiC materials and devices, outlining their plans for tremendous ramps in revenue over the coming years.

Illustrating how great an opportunity there is right now for the SiC industry, Andy Souzis from SiC substrate supplier II-VI remarked: “Our competitors are not Cree, Dow and Tanka Blue. There’s enough business for all of us.”

Souzis, who spoke in a well-attended industrial session, revealed that II-VI is investing “tonnes of money” in capital growth equipment. The company expects sales from its SiC business to climb by 50 to 60 percent per year between 2017 and 2023.

Echoing these sentiments, Henry Chou from GT Advanced Technologies argued that there is now enough business for all the SiC crystal growth players. In his opinion, there is currently a shortage of 6-inch SiC, with the lack of supply having a big impact on the merchant market.

To start to address this, GT is producing and selling SiC crystal boules – its business plan relies on its customers processing this material into wafers.
GT has just built a facility that will have a capacity of 1,000 wafers per month – and if it needs to increase production by adding new tools, that is simply a matter of “copy and paste”, according to Chou, who told delegates: “We plan to revolutionise the supply chain.” Prices for SiC are expected to tumble, with GT’s material costs for SiC production tipped to fall by a factor of three-to-four by 2023.

Ramping of chip production also featured in the industrial session. Chris Dimino from Wolfspeed, A Cree Company, began his talk by explaining that the management of the parent company is shifting its focus from LEDs to SiC. The goal for Wolfspeed is to ramp its SiC annual sales from $200 million in 2017 to $800 million by 2022. Dimino said that the company has already made a good start: year-on-year revenue is up by 50 percent and there has been a recent signing of a long-term supply agreement with Infineon for 6-inch SiC wafers. This is the size that the market is moving too, but right now there is still much interest in 4-inch material.

Domino revealed that Wolfspeed is investing across the board in tools to increase capacity. Purchases included MOCVD reactors and metrology equipment. And if, in future, more floor space is needed to accommodate more machines, there is a building on the campus that engineers can move in to.

STMicroelectronics is also cranking up chip production. Speaking on behalf of the company, Mario Saggio claimed that the total addressable market for SiC devices could climb to $2 billion by 2025, and hetipped this sector to grow over the next decade at a compound annual growth rate of 45 percent. To take advantage of this, ST is expanding its capacity by 275 percent between 2017 and 2022. Further ahead,

Nearly 40 companies were represented in the Exhibition Hall. This is an increase compared with the ECSCRM conferences of yesteryear, underscoring the growth of the SiC industry.

capacity will be even higher, partly due to a switch to production on 8-inch SiC, scheduled for introduction in 2025.

As well as increasing the volume of its existing products, ST will be introducing new generations of devices. The 650 V, 1.2 kV and 1.7 kV MOSFETs offered today will be superseded by devices with a lower specific on-resistance and a lower driving voltage.

Support the growth of the market for ST and its peers, MOCVD manufacturers are updating their tools. Aixtron's Frank Wischmeyer told delegates that the AIX G5 WW C will launch next year. This fully automated tool, equipped with auto-temperature correction, is claimed to double throughout compared to its predecessor, the G5 WW, while trimming the cost of ownership by 30 percent.

Another company launching new tools is LPE of Milan, Italy. This family run business, which claims to have 80 percent of the market in China, currently offers a fully automated, small footprint, single-wafer reactor, the PE106A. This will be joined by the PE206A and PE208A, designed for 6-inch and 8-inch wafers. This duo has been developed during participation in the EU-funded project REACTION ECSEL.

## Transportation, inverters and smart grids

Part of the reason why SiC device sales are taking off is that their producers are now thinking much more about the needs of their customers. That's certainly the case with Infineon, which has devoted much effort to improving its system expertise.

Spokesman for the German electronic powerhouse, Peter Friedrichs, explained that he and his colleagues are now making dedicated products targeting specific applications. By understanding their customers thinking, they gained greater insight in to when end users would switch to SiC, and when silicon would be retained, even though its performance is inferior.

The PV inverter is a market where SiC is enjoying success, argued Friedrichs. He explained that the makers of these units place a great premium on efficiency, and value the reduction in the total bill of materials – it is 15 percent to 20 percent lower when using SiC, because the wider bandgap offers an opportunity to work at higher frequencies, and in turn this trims the cost of other components.

Charging points for electric vehicles provide another opportunity for SiC devices to replace those made from silicon. The current generation of charging stations have been built by stacking liquid-cooled 15 kW units, but the aim is to replace these with those operating at 60-75 kW. This hike in power density is only possible by turning to SiC, according to Friedrichs.

Another promising market for SiC power devices is in aircraft. Shane O'Donnell from Microsemi Corporation detailed this opportunity: he explained that by 2037 the number of passenger aircraft will have increased from 21,500 to 48,000, through the building of thousands of new planes that will feature more power electronics. Airlines are conscious of their environmental impact, and the motivation for using more power electronics in planes is that it replaces some pneumatic and hydraulic sources, ultimately saving fuel. Another benefit of a move to power electronic is that it could reduce maintenance, thereby increasing the proportion of time that the plane spends in the air.

If SiC devices are to win deployment on planes – where they would be used in the primary flight control systems such as ailerons, rudders and elevators – they will have to prove their reliability over a wide range of operating conditions. O'Donnell explained that on the runway in the likes of Dubia, temperatures can be as high as 50 °C, but on the flight they would be far lower. So temperature cycling is a consideration. Devices must also be able to withstand varying levels of humidity, vibration and shock, and exposure to X-rays.

O'Donnell and his colleagues have been putting SiC diodes and MOSFETs through their paces and the results, so far, are said to be "very positive". Testing above 80 °C has not exposed any issues, and operation beyond 110 °C is thought to be "very possible".

If SiC MOSFETs are to succeed in this applications, they will have to win the nod over the silicon IGBT. In SiC's favour is a reduction in power dissipation by about 25 percent, and a higher operating temperature – particularly beneficial if the transistors need to be situated near the engine. However, these strengths need to be weighed against the cost of the SiC MOSFET, which is still high, according to O'Donnell, and the need for further qualification to validate ruggedness and reliability in an industry that is, as one would expect, highly conservative. In addition, effort needs to be devoted to optimising packaging, which in its current form is failing to exploit the high-temperature capability of SiC.

The grids of tomorrow offer yet another market for SiC. Outlining this opportunity, Michel Mermet-Guyennet from the Supergrid Institute in Villeurbanne, France, compared the performance of 3.3 kV silicon IGBTs and SiC MOSFETs, two options for use in high-voltage DC-to-DC convertors. In terms of performance, the class of device with the wider bandgap has the edge, enabling high-voltage DC converters to have losses that are 50 percent lower, a volume that's reduced by one-fifth, and a mass trimmed by 14 percent.

One of the biggest obstacles to the adoption of the SiC MOSFET is its reliability: it needs to deliver 40 years of continuous operation.  The most likely cause of failure, according to Mermet-Guyennet, is gate oxide reliability. To drive deployment of SiC MOSFETs in the electrical grids of tomorrow, Mermet-Guyennet believes that new standards for the devices will have to be introduced, along with the launch of higher-voltage products. "Manufacturers are not interested in 10 kV and 15 kV products."

## To higher voltages

However, this may be changing. At ECSCRM, Edward Van Brunt from Wolfspeed told the audience that his company's production of 3.3 kV and 10 kV transistors was moving to its 6-inch line.

Wolfspeed has always been at the forefront of SiC MOSFET development, and in Van Brunt's talk he discussed the methods used to demonstrate the device's robustness and reliability. The two devices scrutinised were: a 3.3 kV, 40 A MOSFET with a 27 $\mu$m-thick drift layer, a 50 m$\Omega$ resistance, and a chip size of 4.9 mm by 7.7 mm; and a 10 kV, 15 A MOSFET with a 100 $\mu$m-thick drift layer, a 300 m$\Omega$ resistance, and a chip size of 8.1 mm by 8.1 mm.

Evaluation of both of these MOSFETs began by applying a voltage across the gate for 1000 hours. With the 10 kV device, the surface roughness can be as high as 14 nm, so it is of comparable thickness to that of the gate.

No failures occurred, so a time-dependent dielectric breakdown test followed. This indicated that the failure time for the 3.3 kV MOSFET at 175 °C exceeds 3000 years – and for the 10 kV cousin, this time to failure is even longer. High-temperature gate bias testing also produced encouraging results, with no failures observed in three lots of 25 transistors.

Another evaluation used by Van Brunt and co-workers was a high-temperature, reverse-bias test, which involved applying an electric field between source and drain. For this test, higher voltage devices are actually at an advantage, because their thicker drift layers lead to a lower electric field strength. In Wolfspeed's 3.3 kV and 10 kV MOSFETs, they are 2.1 MV/cm, and 1.8 MV/cm. "[These values] are much less than those for commercial, lower voltage devices," explained Van Brunt.

High voltages are needed to conduct these tests, and if care is not taken in designing the rig, damage to it may occur. Wolfspeed has given much thought to testing, and this allows experiments to uncover the ruggedness of both the 3.3 kV and 10 kV devices.

The final test applied to the MOSFETs involved biasing the gate to the off-state, driving current through the device, and seeing if anything breaks. It's not an easy test to undertake as the power dissipation in the

Built in 1991 at a cost of £200 million, The International Convention Centre (ICC), Birmingham, played host to the twelfth European Conference on SiC and Related Materials (ECSCRM). The ICC, which has a capacity to hold 8,000 delegates, includes a symphony hall that can seat more than 2,000.

Car marker Jaguar, which has a factory in Birmingham, brought its iPACE to the exhibition hall. The all-electric car is powered by a 90 kWh, 388 V lithium-ion battery, and has a range of 480 km.

10 kV device can hit 205 W $\text{cm}^{-2}$, while that in the 3.3 kV device can peak at 640 W $\text{cm}^{-2}$. Device heating results, and this can lead to thermal runaway.

One solution is to turn to a pulsed DC test. However, this is difficult to implement and it extends the time taken: for example, when the duty cycle is one-third, the time to test lengthens from 1000 hours to 3000 hours.

To avoid this, Van Brunt and co-workers mount their devices on a large heatsink and use a large fan to cool the chip. Using this approach, tests on 61, 3.3 k V MOSFETs and 65, 10 kV variants, revealed “absolutely no change” in the forward drop in the body diode. In addition, no shifts were observed in other device characteristics, such as the on-resistance.

Another company producing high-voltage devices is Hitachi. At ECSCRM, company spokesman Naoki Watanabe described the development of 6.5 kV SiC IGBTs, which have lower on-resistances at high voltages than their MOSFET cousins.

Watanabe explained that one issue with conventional SiC IGBTs, which feature *n*-type layers well over 100 $\mu$m-thick, is their high switching losses. To reduce this, and maintain the low on-resistance, he and his co-workers introduced a drift layer just 60 $\mu$m-thick. This led to a 80 percent reduction in turn-off loss compared with a device with a 140 $\mu$m-thick drift-layer, and a 89 percent reduction compared with a device with a 170 $\mu$m-thick drift-layer.

Simulations of the MOSFET with the thinner drift layer revealed a low carrier concentration near the emitter. To address this, Watanabe and co-workers have introduced a box cell layout and a hole-barrier structure.

Another issue with this design is that the voltage between the collector and emitter increases in steepness as this device is turned off. That’s a major concern, because it threatens to lead to a malfunction in a power system.

The team at Hitachi have modified their device to prevent this from happening. They introduce a two-part drift layer with a higher doping on the collector side. Testing reveals that this refinement prevents any slope steepening during turn-off. Voltage overshoot is reduced from 5.3 kV to 4.9 kV, and there is suppression of the ringing and current curves. Encouragingly, these gains come without any degradation to on-state and off-state characteristics.

Operating at an even higher voltage is the gate turn-off thyristor (GTO). This class of device is ideal for pulsed power applications and hybrid DC circuit breakers, thanks to its absence of a gate oxide layer that opens the door to extremely high junction temperatures and very high currents.

Last year, Wolfspeed’s Sei-Hyung Ryu reported a 15 kV, *p*-type GTO at the International Conference on SiC and Related Materials (ICSCRM) – and in Birmingham, he went one better, revealing the results for a *n*-type variant. Switching from *n*-type to *p*-type increases carrier lifetime, slashing switching speed by more than an order of magnitude.

Measurements on the 1 $\text{cm}^2$ GTO, which had an 0.465 $\text{cm}^2$ active area, revealed a turn-off time of 170 ns – 45 times faster than that of the *p*-GTO. Turn-on time is also superior, at 102 ns rather than 140 ns. Operating at 15 kV, the leakage current is just 0.17 $\mu$A. “That’s miniscule compared with silicon devices,” claimed Ryu.

To improve the GTO, Ryu and his co-workers will work on improving the carrier injection in their devices. Their efforts, along with others in this community, should lead to many new and exciting results reported at next year’s ICSCRM in Japan – and also the next ECSRM meeting, which will be in Torres in 2020.

At both these meetings, delegates will hear not only of the progress made in device performance, but also in sales and market penetration. If these advances live up to those predicted in Birmingham, those that attend will be in the midst of a golden era for this industry.

# PIC INTERNATIONAL CONFERENCE

## Why should you choose to sponsor with PIC International?

- Are you looking to accelerate your growth and reach the major players in the integrated photonic circuits industry?
- Do you want to educate, influence and network with the industry?

If you have answered yes to any of the questions above, then PIC International 2019 is the perfect event for you. Here are but a few reasons why you must consider sponsorship.

### Reasons to sponsor

1. Access and network with the leading players across the global photonic integrated circuits industry
Going from strength-to strength, the fourth edition of PIC International 2019 will allow you to engage with 300+ senior decision makers from the major companies along the entire value chain of the integrated photonics industry in one dedicated exhibition hall, including over 30 international experts, who will speak at the conference.

2. Raise brand and company awareness
We have an intensive and multi-faceted marketing program available and already underway, which includes email marketing, social media, conference partners, direct mail and live events in addition to promotion in the PIC Magazine digital portfolio  Coupled with the marketing program, the support of our highly esteemed Conference association and media partners ensure your company, product and service will achieve maximum visibility within the industry for the next 6 months.

3. Thought leadership and credibility
Aligning with the leading global photonic circuits industry conference will give you a great opportunity to be positioned as a thought leader in the industry. Engage in debate, share insights and expertise on industry challenges with your peers.

4. ROI and long-term partnerships
Many of our sponsors repeatedly support the event year on year, demonstrating how the industry trusts the PIC International brand as the leading information and networking resource to deliver the best programme and ROI. Unparalleled networking opportunities enable you to both build existing and generate new relationships and demonstrate ROI by aligning with the conference brand.

5. Accessibility
We have opportunities to suit all budgets.

6. Post-event exposure
Even when the event is over, you will be included in off-season conference promotional activities, plus the PIC digital portfolio as well as the fortnightly email newsletter.

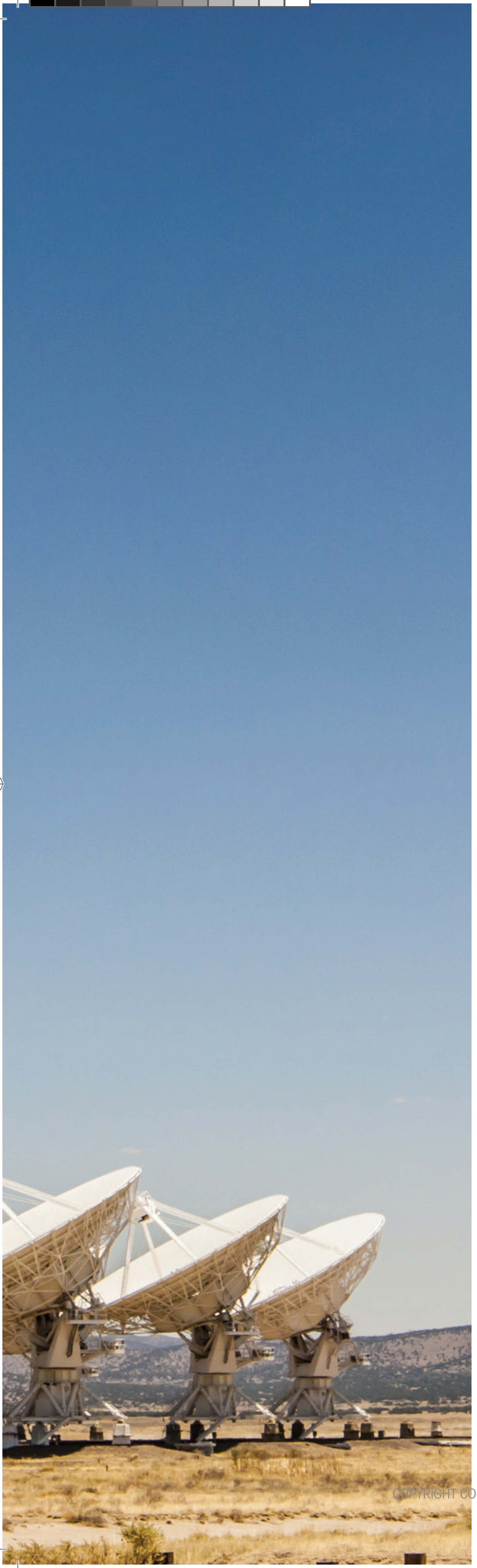
Contact: sponsor@pic-international.net to discuss opportunities with the PIC International Conference and Exhibition team or by calling +44 (0)2476 718 970 today.

Sponsorship opportunities are limited.

# GaN empowers satellite communication

GaN enables powerful, compact transmitters for demanding satellite communications

BY MIKE COFFEY, STEVE RICHESON AND MICHAEL DELISIO FROM MISSION MICROWAVE



THROUGHOUT the history of radio communications engineers have craved more transmit power. This statement is as true today as it was in Marconi’s lifetime.

One sector where there is a particularly strong desire for higher transmit power is satellite communications. Here high-power amplifiers and block upconverters have to generate signals that are powerful enough to offset path loss and spreading. In a traditional satellite communication link (see Figure 1), microwave-frequency radio signals are transmitted from a point on earth to a distant satellite in a geostationary orbit that is 35,000 km away – that’s a distance of almost six times the earth’s radius.

The most common frequency domains for the satellite communications uplink are X-band (7.9-8.4 GHz), $K_u$-band (13.75-14.5 GHz), and $K_a$-band (29-31 GHz). Transmitter output power at these frequencies needs to be high, because satellites receive only a miniscule fraction of the power transmitted in their direction. Typically, a communications satellite may receive just a few picowatts of power from an earthbound transmitter that broadcasts tens of watts.

A weak signal reaching the satellite’s receiver is not the only issue, however. That signal is coming from a single spot on the surface of the earth that could be masked by the background noise from our warm blue planet, alongside plenty of other potentially inferring signals.

Improvements to the link can result from increasing the power of the transmitter, as this allows the satellite’s receiver to ‘hear’ signals that appear much ‘louder’. But that’s not all. High powers also equip the engineer with greater flexibility when they design the link. Armed with a higher transmit power, engineers can create links with higher data rates, by employing larger bandwidth carriers with more complex modulation schemes to encode the data onto the microwave carrier. In addition, higher transmit powers increase the ruggedness of the link – even when it is raining, attenuating the microwave signal, the link is still available. And last, but by no means least, increasing the output power of the transmitter allows a shrinking of the aperture size of the uplink antenna, and ultimately a more compact, mobile platform.

The latter strength is a big deal in today’s satellite industry. That’s because many satellite terminals are no longer fixed to the ground. Instead they are mobile, serving airborne, maritime, vehicular, and tactical military applications.

This mobility is essential for several new satellite communication networks that are under development, and employ constellations of low- or medium-orbit satellites, which need to be tracked as they move across the sky.

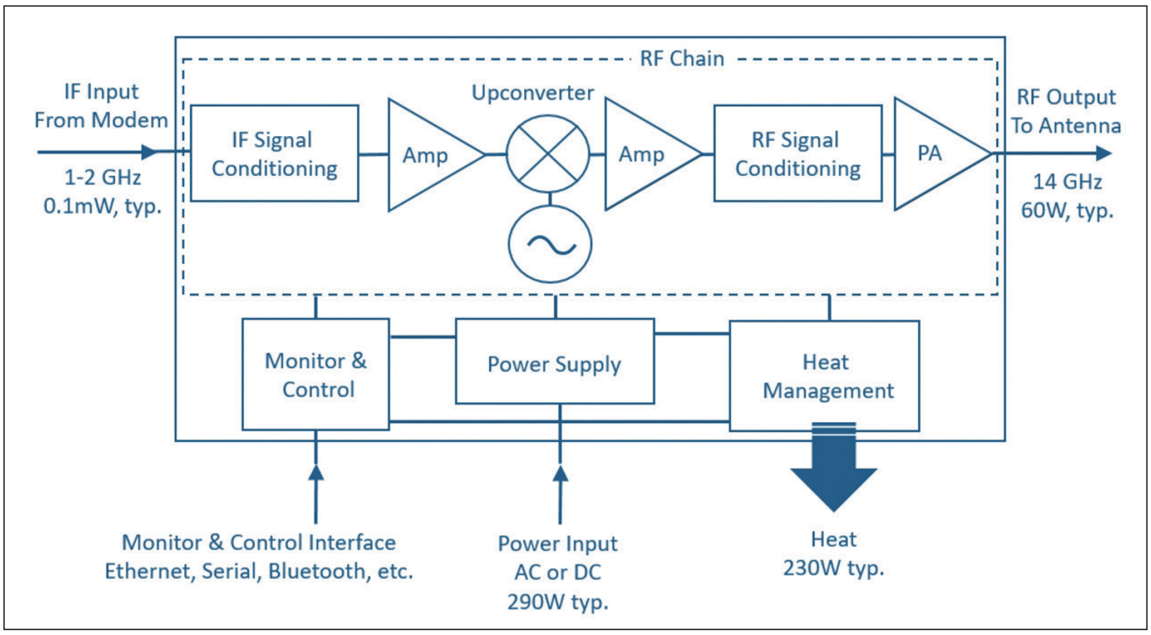


Figure 1. Uplink transmitters for satellite communications perform two main functions: frequency upconversion and amplification. This package is often called a block upconverter (BUC). It accepts a low-power, low-frequency modulated signal from a satellite communication MODEM, and upconverts the signal to the specified uplink frequency band; in this example the output frequency is $K_u$-band, but X-band and $K_a$-band BUCs are popular as well. A power amplifier (PA) boosts the upconverted microwave signal to the output needed for the satellite communication link. Here the transmitter power is 60 W, but higher power terminals are possible. Thermal management is important to ensure that the electronics do not overheat. The prime power to the block upconverter could be an AC or DC voltage, depending on the application. Monitor and control signals provide telemetry between the block upconverter and the user. Finally, the entire system must be enclosed in a rugged, weatherproof package.

For satellite communication platforms that have to be mobile, or rapidly moving, key attributes for the transmitter are that it is small, lightweight, and draws minimal power. Success on all these fronts ensures that the transmitter is easy to move, and that the link is provided with great power efficiency.

The demand for a higher transmit power is often at odds with the requirements for mobile applications. Generally, higher-power transmitters tend to be larger and heavier, and often less efficient. That means that they tend to need more power to operate, and dissipate more heat.

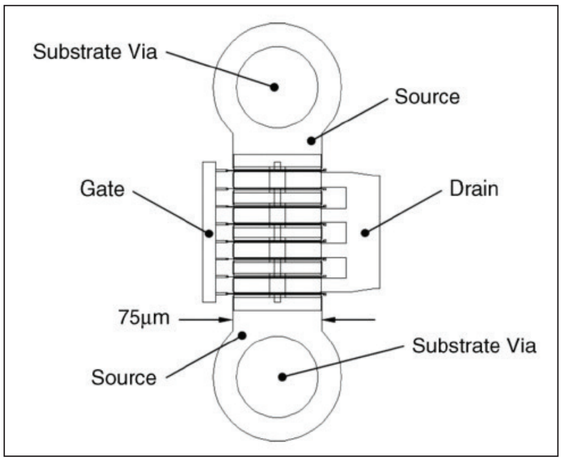


Figure 2. Typical layout for a single GaN-on-SiC transistor. There are eight gate fingers with a width of 75 µm,creating a 600 µm device. Several devices are power-combined in the final output stages of GaN MMIC power amplifiers.

Fortunately, a step-change in performance – in terms of size, weight, and output power – is possible by replacing the incumbent technology with new designs based on GaN. Switching from GaAs, the outgoing solution, to GaN is enabling solid-state power amplifiers to combine high efficiencies with impressive output powers while maintaining very compact form factors. And as GaN technology matures, this trend is sure to continue.

## GaN MMICs: Providing the power

The key device for GaN is the HEMT. It is the building block for the production of GaN MMICs, which provide more output power per die than entire block upconverters built using older, last-generation GaAs technology and designs.

For X-, $K_u$- and $K_a$-band frequency satellite communications, GaN HEMTs, grown on SiC substrates, typically have gate lengths of 150 nm to 250 nm. Shrink this and higher frequencies are possible. Reducing to a 90 nm gate length enables operation in the millimetre-wave domain (greater than 30 GHz), and even higher frequencies have been reported for gate lengths as short as 20 nm.

Realisation of higher output powers has hinged on several breakthroughs: T- and Γ-gate technology; the introduction of the field plates, which holds the key

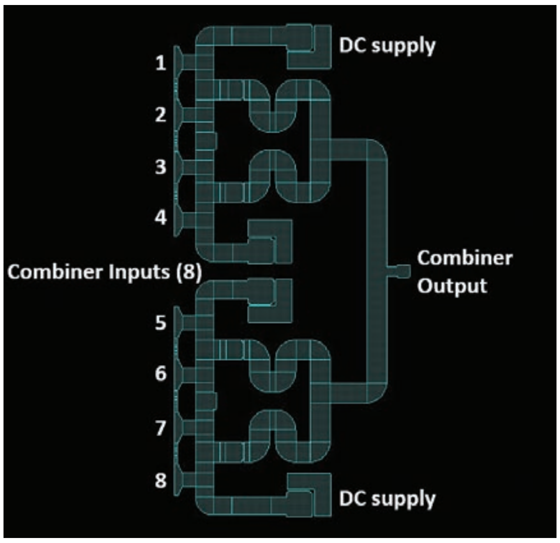


Figure 3. An example of a final stage of a GaN MMIC power amplifier eight-way combiner. Eight transistors (left) are power combined, supplied with DC and routed to the single output (right).

to higher-breakdown voltages; and the global push for higher data rates and more output power from the terminals.

Many chipmakers are manufacturing such devices. At Qorvo, Wolfspeed/Cree, Northrop Grumman Aerospace Systems, HRL Laboratories, BAE, and WIN Semiconductor, device fabrication is routine, with published amplifier data revealing that power levels are in the 3.0 W/mm to 5.0 W/mm range. At lower frequencies, even higher power densities are possible, with values exceeding 10 W/mm at supply voltages of 50 V or more.

Thanks to the high power density of GaN, even modest-sized transistors can provide substantial output. For example, a single device with eight gate fingers and 75 µm of gate width can generate over 3 W of output power (see Figure 2).

Even higher powers can come from uniting several transistors with on-chip combiners (see Figure 3 for an example of an eight-way combiner). Adopt this approach and a single-chip GaN MMIC can produce an output power of more than 60 W in X-band and 20 W in $K_a$-band.

The availability of these incredibly powerful GaN MMICs enables the construction of power-combined block upconverters delivering output powers that were previously unimaginable. What's more, these powerful systems are made from fewer parts than their GaAs cousins, and deliver greater efficiency. Thanks to these strengths, there is no doubt that GaN MMIC power amplifiers will be the main driver in solid-state satellite communication block upconverters for many years to come.

## Great power in a small package

At Mission Microwave of Santa Fe Springs, CA, we have built a line of block upconverters for satellite communications around these powerful, efficient GaN MMICs. A prime example of this is our 100 W, $K_a$-band block upconverter that is 14 cm in diameter, 34 cm in length and weighs slightly over 4.5 kg (see Figure 4). In comparison, state-of-the-art GaAs $K_a$-band block-up converters from five years ago could only generate half that power – and they did so from a unit that's three times as large and heavy. What's more, our 100 W converter draws less than half of the power from the prime supply.

The differences can be even more striking in the $K_u$-band. Operating in this spectral range is our 25 W 'Flatpack' amplifier, designed to be thin enough to be inserted directly into a modern flat satellite communication terminal for applications requiring either high mobility or the ability to track a moving satellite (see Figure 5). Competing block upconverters are up to four times larger than this unit. By trimming size and weight, while upping efficiency, our block upconverter is enabling a new generation of compact, mobile satellite communication terminals for both commercial and military applications.

The key to building these compact, powerful block

Figure 4. Mission Microwave's satellite communication block upconverter portfolio. From left to right, 200 W, 100 W, and 25 W $K_a$-band block upconverters that can efficiently provide linear output powers in industry-leading compact packages. At Ku-band, similarly-sized upconverters can provide 200 W, 100 W, and 55 W of output power.

Figure 5. Mission Microwave's block upconverter. This 0.8 kg, 25 mm-thick package can be integrated directly into a flat-panel antenna system.

upconverters is to use a highly integrated design. As output power requirements tend to exceed those produced by a single MMIC, we use a hierarchy of power-combining manifolds with low losses. This preserves efficiency.

Today's GaN MMICs are more efficient than their predecessors, but due to operation at far higher power densities, effective thermal management is critical to ensuring that chips maintain reliable operation. To accomplish this, we undertake thermal, electrical and mechanical design together, in order to optimize the form factor. Other steps that we take to maximise performance are: design the upconverter and signal processing circuitry, to ensure that these components are integrated properly into the unit; custom design the power supply, monitor and control circuitry around the GaN-based power amplifier; and design custom circuitry to extend the useful operating power of our block upconverters.

## Leading with linearity

Designers of power amps love to quote saturated output power because this is the biggest number. But it is not the most meaningful one in a radio communication system, because it is the fidelity, or linearity, of the amplifier that limits usable power. Ideally, the amplitude and phase of the output signal of the power amp are independent of the power level. In practice, however, amplifiers saturate, preventing the output from exceeding a hard-limited maximum, or 'saturated', power. Complicating matters, the amplitude and phase of the amplifier's gain changes with respect to the signal level, especially near saturation. The downside is nonlinear distortion of the output signal, leading to of out-of-channel interference and increased bit error rates.

These drawbacks are a big deal. Transmitters are moving to higher and higher data rates, enabled by operators turning to ever more complex modulation schemes. With these data transmission technologies, linearity is at a premium. To meet requirements, block upconverters are 'backed off' from their maximum output power. This move meets linearity requirements and avoids creating signal impairments, which can either degrade link performance or potentially interfere with signals using adjacent channels.

Unfortunately, however, GaN-based amplifiers can be especially susceptible to nonlinear distortion; despite having high saturated output powers, linear output powers of early GaN block-up converters were no better than those of their GaAs-based counterparts. But there is some good news: the linearity of the amplifier can be improved with linearizer circuitry. Many techniques are available, all striving to reduce the dependence of the amplifier's gain magnitude and phase on the drive level.

A common approach for characterising the linear output power of an amplifier that is used for satellite communication is to consider the third-order intermodulation distortion curves. They are produced

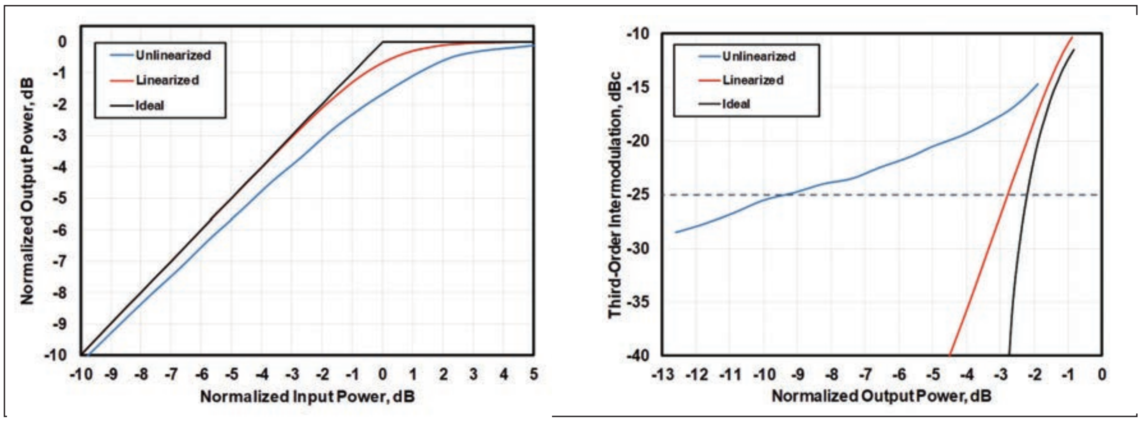


Figure 6. GaN-based amplifiers require linearization to extend their useful output power.

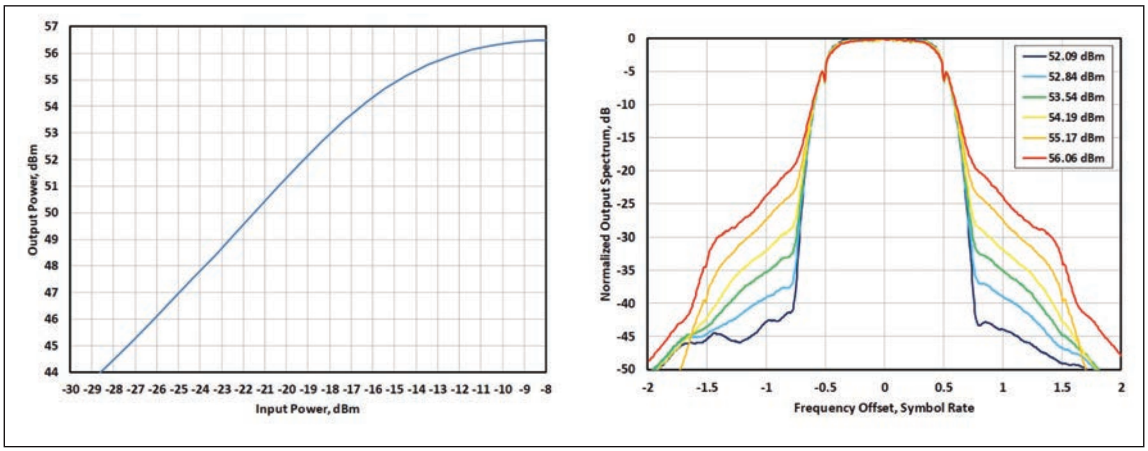


Figure 7. Mission Microwave's 400-W $K_u$-band block-up converter generates unrivaled output powers in an industry-leading form factor.

by feeding in to the unit two equal-amplitude tones, separated in frequency by a few megahertz. Any nonlinear distortion is exposed as additional tones appearing in the output spectrum. Typically, for satellite communication distorting tones should be at least 25 dB below signal tones.

Using this approach to evaluating linearity, an ideal amplifier must be backed off from saturation by just over 2 dB (see Figure 6). In comparison, an unlinearized amplifier, exhibiting a rather 'soft' gain saturation that is typical of a GaN-based amplifier, has to be backed off by over 9 dB to meet the desired linearity. Far better, though, is our linearized amplifier. This is within 1 dB of ideal, increasing the useful output power by 6 dB over the unlinearized variant.

## Pushing to higher powers

We are not resting on our laurels, but continually striving to fulfil the demand for ever increasing transmitter output powers. Recently, we have built a block upconverter that delivers 400 W of saturated power in the $K_u$-band (see Figure 7).

To evaluate the linearity of this amplifier, we have used another common metric for satellite communication amplifiers: spectral regrowth. For this test, the block upconverter transmits a digitally modulated waveform, just as it would in a real application. Chosen is Offset Quadrature Phase Shift Keyed (OQPSK) modulation, at 10 million symbols per second.

If there is no distortion in this test, the output spectrum of the amplifier will appear as a flat rectangular pulse, with very little power at frequencies offset by more than one symbol rate from the centre. Increase the output power, though, and distortion will kick in. Power will begin to grow outside this main channel, and the spectrum will appear to grow shoulders.

For a typical specification for a satellite communication amplifier, the block upconverter will produce spectral regrowth of less than 30 dB below the main channel at a frequency offset of one symbol rate from the centre. For our 400 W amplifier, this threshold is crossed at an output power of approximately 54.5 dBm (280 W) – this is backed off by less than 2 dB from the 400 W saturated output. Note that we realise similar results with our 200 W units operating in the $K_a$-band. Our next steps are the designing and testing of units that are capable of delivering 800 W in the $K_u$-band and 400 W in the $K_a$-band. Were it not for GaN-based MMICs, these power levels would be impractical in a commercial solid-state transmitter.

This will not be the limit of what is possible, as engineers are continuing to make advances in semiconductor devices and materials, propelling operating frequencies and breakdown voltages to new highs. There are also efforts underway to deal with the ever-increasing heat dissipation, including growing the GaN layers on high-thermal-conductivity substrates like diamond, or integrating microfluidic cooling channels into the chip. Such efforts will result in more and more output power from GaN-based MMICs, which will in turn enable higher-power communications transmitters.

Our team can be guaranteed to put this power to good use. Demands for connectivity are only going to increase, along with requests for smaller mobile terminals, which could open the door to sales in new sectors, such as maritime, aviation, consumer, commercial, and government markets.

**Further reading:**

K. Shinohara *et al*. IEEE Trans. on Electron Devices **60** 2982 (2013)

Qorvo, TGA2312-FL 9-10 GHz 60 Watt GaN Power Amplifier, http://www.qorvo.com/products/p/TGA2312-FL, published online, 2017

Wolfspeed, CMPA1D1E030D Datasheet, https://www.wolfspeed.com/rf/products/satellite-communications/cmpa1d1e030d, published online, 2018

Win Semiconductor, "MMIC Advanced Technology," https://www.winfoundry.com/Tech/tech_advanced?year=2018, published online, 2018

C. Campbell, "Microwave Monolithic Power Amplifier Design," Wiley Encyclopedia of Electrical and Electronics Engineering. John Wiley and Sons, Inc (Published Online), April 2013

# Making InP lasers in GaAs fab

Costs come down when InP lasers are produced on a 4-inch GaAs line

BY DEBDAS PAL, JAMES CARTER AND DEYIN ZHAO FROM MACOM

IN THE 1970s, InP lasers came on in leaps and bounds. It is from that decade that has emerged the distributed feedback laser, a device that operates in a single mode and produces emission with a narrow spectral width. By adjusting its emission to the absorption minimum of optical fibre, transmission over vast distances is possible – it is for that reason that distributed feedback lasers lie at the heart of fibre-optic networks. Shipments of these devices continue to rise, to satisfy a seemingly insatiable demand for data.

More recently, sales of another device in the InP laser portfolio, the Fabry-Pèrot laser, have also taken off. Its performance is not as impressive as that of the distributed feedback laser – it sports a wider spectral

width and multiple modes – but that's good enough for low-data rates over shorter distances, where a lower price, resulting from reduced complexity, is a major asset.

Revenue for both classes of lasers is climbing, due to an ever-increasing demand for bandwidth. It is now at unprecedented levels, thanks to the emergence of new applications, such as smart homes, e- health, e- learning, wearables, smart cities and 3D HD video. This has led to substantial worldwide deployment of FTTx networks, alongside enormous demand from the data centre domain.

Manufacture of the vast majority of distributed feedback and Fabry-Pèrot laser takes place on dedicated InP lines, where 2-inch or 3-inch wafers are processed using conventional cleaved facet technology. That's far from ideal on two fronts: the wafers are small, hampering economies of scale; and cleaving, which creates a manufacturing bottleneck. Furthermore, the current cleaved facet process has several disadvantages, one of them being that any defects created at the facet, due to mechanical cleaving, are a potential reliability risk. In addition, it is difficult to control the placement of the facet at the correct location on the ridge. However, the biggest issue of all is that the wafers are singulated into bars and stacked for facet coating, before the bars are then separated and tested individually – that's clearly not a high-volume production process.

## Sharing tools

At MACOM we are addressing every one of these weaknesses head-on by making our InP lasers on our 4-inch GaAs IC line with an etched-facet technology. By sharing existing equipment and infrastructure with that used for producing GaAs products, we not only reduce development costs, but also those associated with manufacturing, thanks to the sharing of fixed costs with other products.

Our etched facet technology has numerous advantages over its mechanical counterpart. Its greatest strength is that it is a high-volume production process – it enables on-wafer testing, with the pick-up of only good devices; and wafers do not have to be singulated to make bars and create a stack for facet coating. Another key attribute is that there is far greater freedom in the creation of the facet. No longer does it have to be made along a crystallographic angle of the wafer.

We produce our InP distributed feedback and Fabry-Pèrot lasers at our world-class GaAs IC fabrication facility, which is based in Lowell, MA. The facility is primarily used for manufacturing GaAs-based MMICs and GaAs/AlGaAs diodes, using the most cost-effective mainstream manufacturing process technologies.

Using high quality equipment that offers excellent process control, we have process modules for photolithography, implantation for isolation, metallization, dry/wet etch and back-side process. Photolithography is carried out using several high-

A 4-inch InP wafer of edge-emitting lasers for optical communications.

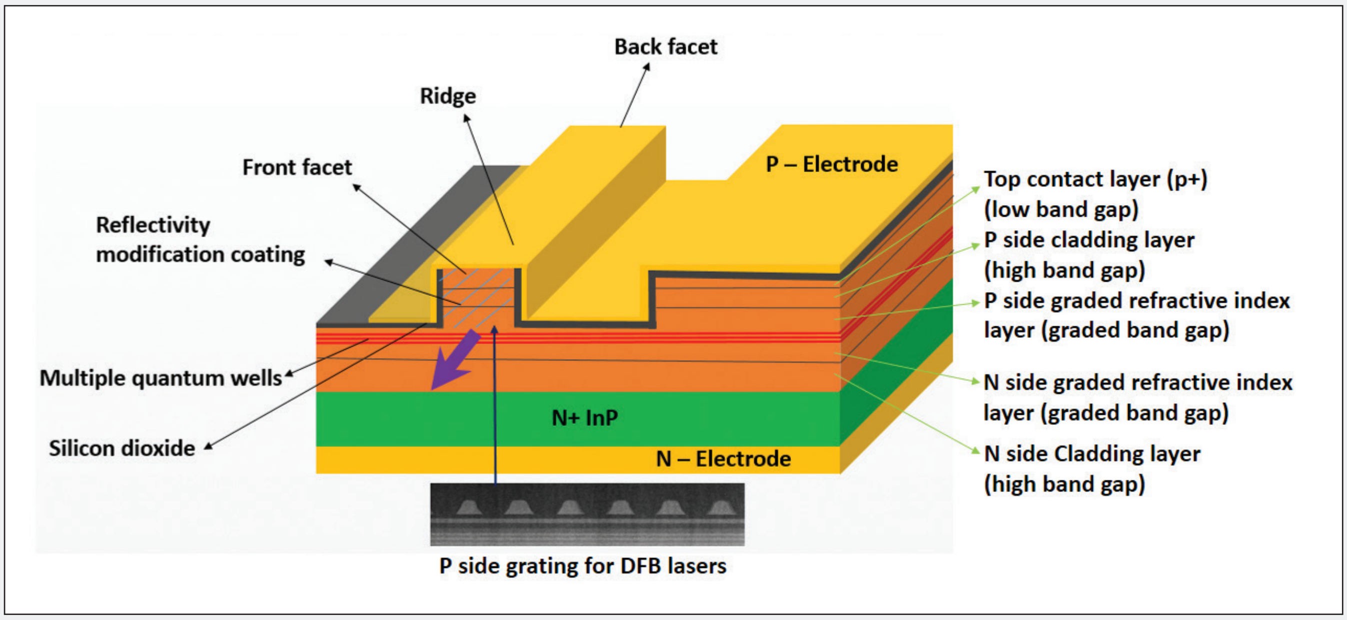


Figure 1. Ridge waveguide, edge-emitting lasers feature quantum wells for carrier confinement and cladding regions and ridges for optical confinement. Inserting the grating in the distributed feedback laser ensures single-mode output.

quality steppers and e-beam writing tools, and the addition of ohmic and Schottky contacts are undertaken in multiple metallization systems, including those based on electron-beam and sputtering, using a variety of dome configurations. Our engineers also use: high-quality lift-off process tools and remote plasma cleaning process equipment to clean wafers and deliver defect-free devices; PECVD systems for the deposition of silicon nitride and silicon dioxide; and various dry etch tools, equipped with different gases, for etching semiconductor and dielectric layers. Our well established back-side processes include mounting, photo-processing with an infra-red mask aligner, grinding, polishing, back metal, dismount and cleaning. To monitor the processes and determine critical device dimensions, engineers turn to several high-end tools, including various scanning electron microscopes, automated optical inspection tools, optical and laser microscopes and profilometres.

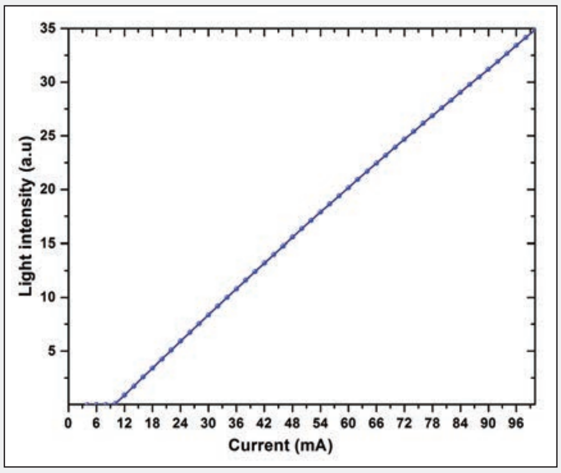


Figure 2. Light intensity versus injection current for an MACOM 2.5 Gbit/s Fabry-Pèrot laser.

Adjusting this GaAs IC line so that it also produces InP lasers has not required substantial capital expenditure, because many of the existing tools can be used to manufacture photonic devices and control the production processes. Note that as well as keeping a close eye on the processing equipment, we use several in-line test systems, which can test process control monitor structures. This offers an insight into the health of the processes and the devices.

The lasers that we make emit at around either 1.55 μm, the sweet spot for low optical loss in a fibre, or 1.33 μm, where dispersion is minimum. For these wavelengths, various quaternaries can be used for the active region, but InGaAlAs is preferred in the quantum well, because it increases the speed of the laser and improves its high-temperature performance. Surrounding this layer are those made from the likes of InGaAs, InGaAsP, InGaAlAs and InAlAs – these are used to inject the carriers into the active region, confine them there, and control the optical modes within the chip.

Fortunately, there is much common ground between this set of materials and those used to make GaAs-based pHEMTs. The later are grown on semi-insulating GaAs, and primarily contain epitaxial layers of AlGaAs, InGaAs, InGaP and AlAs.

There are differences between lasers and pHEMTs, due to changes in composition required to ensure lattice-matching to either GaAs or InP substrates, and differences in dopants. For pHEMTs, the only dopant is silicon, while photonic structures may incorporate small amounts of silicon, zinc or boron.

However, it is the high degree of commonality between the two systems that allows many of the process modules used for the production of GaAs devices to also play a role in the manufacture of InP-based lasers. For example, both classes of device can be made using the same tools for photolithography, annealing, thinning and the addition of metal and dielectric layers.

## Making lasers

Manufacture of our distributed feedback and Fabry-Pèrot lasers begins with the growth, by MOCVD, of heterostructures on 100 mm-diameter, $n^+$ InP substrates. The structures contain a multi-quantum well active region, surrounded by graded-index separate confinement heterostructure layers, and a heavily doped, *p*-type InGaAs contact layer to improve the ohmic contact.

The high spectral purity of the distributed feedback lasers comes from the incorporation of a grating within the device. To form this, an InGaAsP layer is grown in the *p*-side of the structure. After the grating is created in this layer, regrowth takes place in an MOCVD chamber. The wafer is then removed and an oxide layer deposited, to form insulating pads underneath metal bond pads. Defining the facets and ridge follows, with different dimensions serving different applications. A *p*-type ohmic contact is then deposited on the ridge and on the oxide, a back metal is added on the $n^+$ InP substrate, and the structure is then subjected to a rapid thermal anneal.

To modify the reflectivity of the facets, so that the device targets a particular application, we use different facet coating layers for our distributed feedback and Fabry-Pèrot lasers. After this, we test our lasers on-wafer at different temperatures. This includes an assessment of their most fundamental characteristics, revealed by the light output of the device as a function of injection current.

For our 2.5 Gbit/s Fabry-Pèrot lasers, measured at 25 °C, there are no kinks in the curve, indicating the absence of any instabilities in spatial and spectral modes (see Figure 2). Lasing begins at 8 mA, and the calibrated slope efficiency is around 0.48 mW/mA. The multiple longitudinal modes in the emission profile, centred around 1310 nm, are a characteristic of the Fabry-Pèrot architecture (see Figure 3).

Our portfolio of Fabry-Pèrot 1310 nm lasers also includes those that operate at 10 Gbit/s and have a threshold current of 6.5 mA. Measurements at 25 °C reveal that there is just a small variation in threshold current, which averages 6.5 mA. The variation in threshold current between wafers is small, indicating that the epitaxial wafers are of good quality, and there is little variation in the production process (see Figure 4).

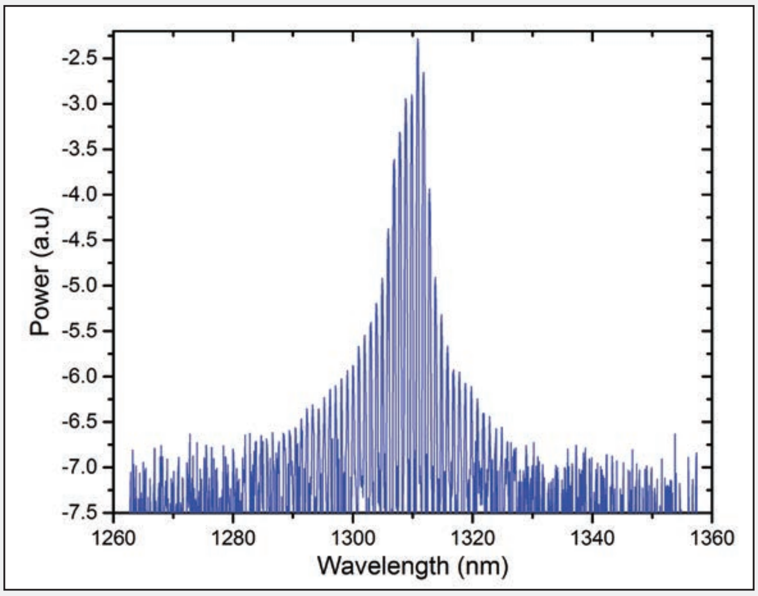


Figure 3. Emission spectrum showing different longitudinal modes from an MACOM Fabry-Pèrot laser at 25 °C. The injection current was about 28 mA.

To measure the on-wafer, small-signal optical modulation response at 25 °C, we have used the Anritsu VNA and O/E calibration module. This reveals an increase in bandwidth with injection current (see Figure 5). That's primarily because cranking up the current increases the photon density within the cavity. Driven at 45 mA, bandwidth at the 3 dB point is about 15 GHz, which is well above the requirement for 10 Gbit/s operation.

For our 1310 nm distributed feedback lasers, as expected, emission is single mode (see Figure 6). The side-mode suppression ratio, defined as the ratio of the power of the side mode to the main mode, is around 46 dB. This high value reflects the high degree of stability of the laser. The small variation in wavelength of these devices, along with their high side-mode suppression ratio, indicates that we have

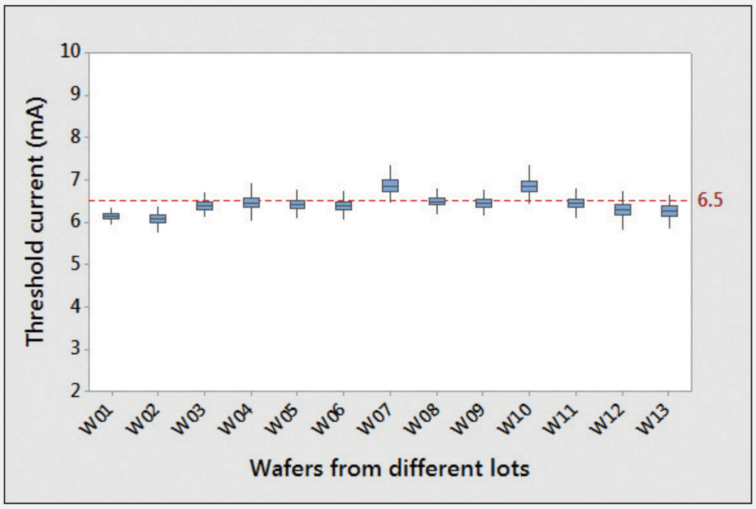


Figure 4. Box plot of the threshold current of 10 Gbit/s Fabry-Pèrot lasers on different wafers of multiple lots at 25 °C.

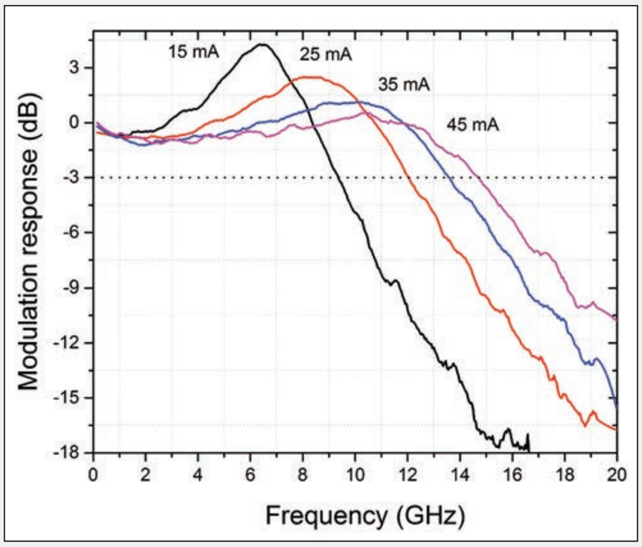


Figure 5. Small-signal response of 10 Gbit/s Fabry-Pèrot lasers at 25 °C. The 3 dB bandwidth increases with injection current. It is about 15 GHz at 45 mA.

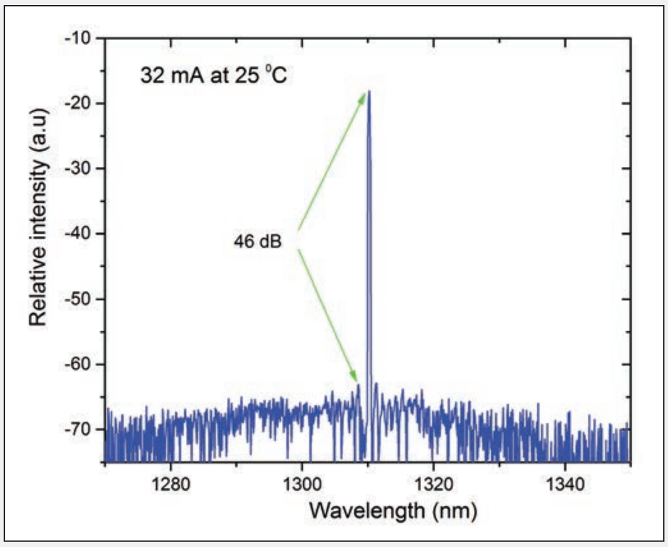


Figure 6. Single-mode spectrum of a 2.5 Gbit/s distributed feedback laser observed at 25 °C. The side mode is suppressed by 46 dB. The applied current was about 32 mA.

robust control in our manufacturing process (see Figure 7). Operating at 25 °C, these lasers have a threshold current of around 12 mA and a slope efficiency of 0.47 mW/mA. These values are well within the range desired by customers, and have enabled us to ship millions of 2.5 Gbits/s distributed feedback lasers for GPON applications.

Successes with our 2.5 Gbit/s and 10 Gbit/s Fabry-Pèrot lasers and our 2.5 Gbit/s distributed feedback lasers have encouraged us to expand our portfolio with devices operating at higher speeds.

The key to increasing the speed of our distributed feedback lasers, and enabling them to operate at high temperatures, is to install a complex grating in the active layer. We will accomplish this with our existing equipment.

Production of these more complex lasers will need to replicate the approach we take with GaAs IC products. With those devices, the ohmic metal is deposited at the beginning of the flow, enabling the creation of process control monitoring structures. They allow in-line monitoring of electrical characteristics.

At present, the process control monitoring in place for laser production is not as sophisticated as this. There are process control monitors on the wafers, but they are only used for measuring etch depth, and the thicknesses of the oxide layer, metal, and facet coating layers. Verification of reflectivity and refractive index comes from separate monitors in the deposition system. What's missing are structures for in-line electrical measurements that monitor contact resistance and diode characteristics. With the laser process flow, the metal layer is deposited at the end of the flow, so there is little benefit in process control monitoring at this point.

As we develop our technology for process control monitoring, we shall continue to refine our approach to high-volume manufacturing of InP lasers on our 4-inch GaAs line. Production costs for these chips will come down, driving up their deployment – maybe one day they'll even be as widespread as the LED.

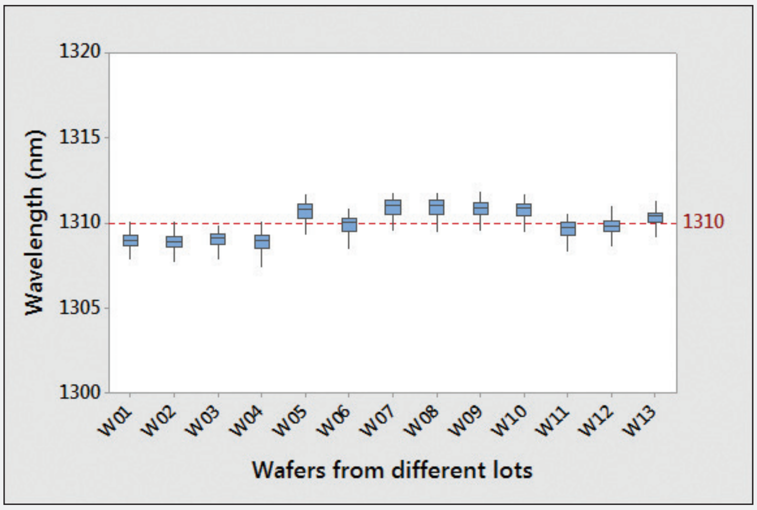


Figure 7. Box plot of emission wavelength of 2.5 Gbit/s distributed feedback laser on different wafers from multiple lots.

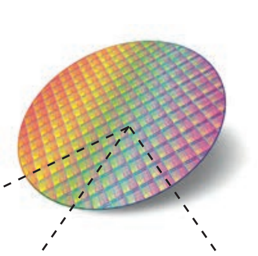
**Further reading:**

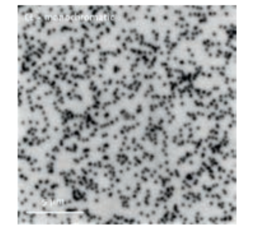
A. Behfar et al. SPIE's oemagazine p. 27 February 2005 attolight™

# Wafer cathodoluminescence for production statistical process control

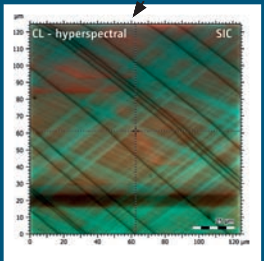
## Wafer incoming
## Blank wafer control
## Crystalline growth processes

- Non-destructive
- Nanometer level
- Buried defects quantification
- Crystal defects quantification
- Doping uniformity
- Strain
- Optical spectrum signature

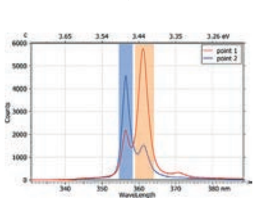




CL – Monochromatic



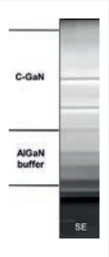
CL – Hyperspectral



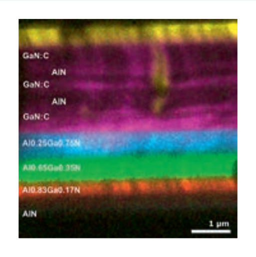
Spectra

## Power & RF (GaN + SiC) HEMT

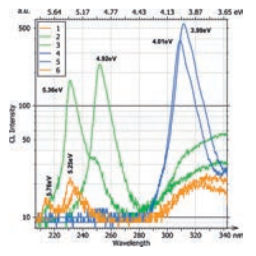
Nanoscale GaN HEMT layer composition & strain distribution



SEM

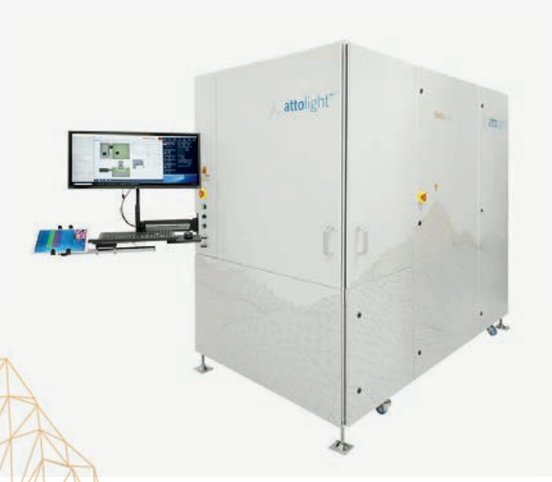


Cross section HEMT



Al% in AlGaN

## Säntis 300



- Up to 300 mm wafer tool
- High-throughput CL-SEM
- Unique scanning modes
- Up to 300 µm FOV
- Simultaneous SEM imaging, hyperspectral imaging and Optical signature acquisition
- Automated wafer bow mapping and correction

www.attolight.com

# PIC INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the global integrated photonics industry

# PIC INTERNATIONAL 2019 CONFERENCE
## DATES & SPEAKERS ANNOUNCED!

Preparations for PIC International 2019 have gotten off to a terrific start with a record breaking number of industry leading speakers and sponsors already confirmed to participate with 6 months to spare.

Returning to the Sheraton Airport Hotel in Brussels on 26-27 March 2019, the fourth edition of PIC International Conference, will once again bring together key players of the worldwide photonic integrated circuits industry from across the entire value chain for two-days of technical tracks and exhibit opportunities.

With an attendance in 2018 of over 300 senior level delegates including representatives from Facebook, Intel, IBM and the European Commission among many others, the event hit record numbers for attendance.

PIC International is part of AngelTech, a brand which delivers insightful, engaging and high-valued conferences that have tremendous synergy. The current line-up, attracting more than 600 delegates, consists of the co-located Compound Semiconductor (CS) International, Photonic Integrated Circuits (PIC) International, and Sensor Solutions International (SSI) conferences.

Delegates can choose to dip in and out of every session to put together their own tailor-made programme by selecting from over 100 invited talks, delivered by leaders of the most innovative companies within their sector. Those attending can also spend time at the exhibition hall, supported by over 60 companies detailing the latest advances in materials, equipment and software; and play their part in two awards ceremonies, which acknowledge the most important breakthroughs within these industries.

## 5 New Themes for 2019:

### PICs Today – Datacom, Imaging and Transport

Today's primary PIC applications in data centers and telecom are foundations for new opportunities. We will explore PICS for healthcare, diagnostics, imaging/ranging and vehicle automation as well as new approaches for data transport.

### PIC Innovation – EPDA, TAP & PICs Beyond Datacom

Electro-photonic design automation (EPDA) paired with automated test, assembly and packaging (TAP) are essential for ensuring rapid PIC development cycles and quality control. We will explore how tools and processes will enable greater yield, reliability and sector growth

### PICs Reimagined – Hybrids and Materials Innovation

PIC innovation is already linked to hybrids – InP lasers are driven by silicon chips and die-level devices are combined into modules. While silicon photonic (SiP) optimization continues we will concurrently explore the benefits of bringing compound semiconductor technologies such as GaAs, GaN, lithium niobate, and silicon carbide into PIC development programs

### PIC ROI – Show Me the Money

While manufacturers are working to automate PIC assembly, packaging and test, we will examine how existing and future sector investments will reap dividends. What cycles should investors anticipate? How can financiers accurately gauge product potential within emerging PIC sectors?

### PICs Beyond 100G – Evolution and Revolution

PICs are poised to transform many end use markets as global semiconductor innovation shifts resources from electrons to photons. We'll explore near-term opportunities and potentially disruptive, long-range advantages that PICs can offer today's service providers and end users with a focus on healthcare, autonomous driving, defense and security; artificial intelligence, AR/VR and the IoT

## Speakers confirmed to date include:

AIM Photonics, Ciena, CORNERSTONE, EPIC, EpixFAB, European Commission, Facebook, FICONtec, Finisar, Hong Kong University of Science & Technology, Infinera, IQE, Juniper Networks, Kaiam Corporation, LIGENTEC, LightCounting, Lightwave Logic, Luceda Photonics, Lumerical Solutions, Multiphoton Optics, Nanoscribe, PhotonDelta, Physik Instrumente, SMART Photonics, Strategy Analytics, Synopsys, Teem Photonics, Tyndall National Institute, VPIphotonics

---

# Book your place NOW!

**www.picinternational.net/register to secure your place**

## It's set to be another sellout

---

## PLATINUM SPONSORS

CORNERSTONE
ficonTEC micro assembly machines
LUCEDA PHOTONICS
lumerical
Multiphoton Optics®
nanoscribe
SMART PHOTONICS
SYNOPSYS®
teem PHOTONICS
VPIphotonics DESIGN AUTOMATION

## GOLD SPONSORS

bay photonics
EXFO
Fraunhofer Heinrich Hertz Institute
IQE
santec
VTT

## WIFI SPONSOR

BROLIS SEMICONDUCTORS

## LANYARD SPONSOR

IQE

## DELEGATE BAG SPONSOR

SMART PHOTONICS

## SUPPORTED BY

EPIC European Photonics Industry Consortium
imec
LIGENTEC

---

angel tech

## 3 Conferences, 2 Days, 1 Ticket

CS INTERNATIONAL CONFERENCE
PIC INTERNATIONAL CONFERENCE
SSI INTERNATIONAL CONFERENCE

# Propelling MEMS VCSELs

## into the mid-infrared

For gas sensing in the mid infra-red, the MEMS VCSEL is the ideal source: it is low in cost, provides great spectral purity, and offers wavelength tuning that is fast and wide

BY VIJAYSEKHAR JAYARAMAN, CHRISTOPHER BURGNER AND ANTHONY CAZABAT FROM PRAEVIUM RESEARCH AND STEPHEN SEGAL, KEVIN LASCOLA AND FRED TOWNER FROM THORLABS QUANTUM ELECTRONICS

THE START OF THE TWENTY-FIRST CENTURY will go down in history as the age of the sensor. They are poised to monitor everything from large industrial power plants to automobiles, household appliances, and individual physiology.

A key application in this emerging field is environmental gas sensing. There are engineers working in governmental programmes, universities, and start-ups that are striving to develop low-cost, rapid, accurate and mobile technologies to quantify concentrations of harmful pollutants, such as the likes of nitrous oxides and carbon monoxide.

To aid this effort, the US Advanced Research Projects Agency is running a programme called MONITOR – Methane Observation Networks with Innovative Technology to Obtain Reductions. The programme is devoted to developing components and systems for early detection of methane leaks. Now in its later stages, it promises to significantly reduce greenhouse gas emissions, as well as provide economic benefit to oil and natural gas producers by preventing loss of valuable product. Spin-off gas sensing technology from this effort will enhance combustion monitoring for enhanced fuel efficiency, as well as enable the monitoring and real-time optimization of industrial processes.

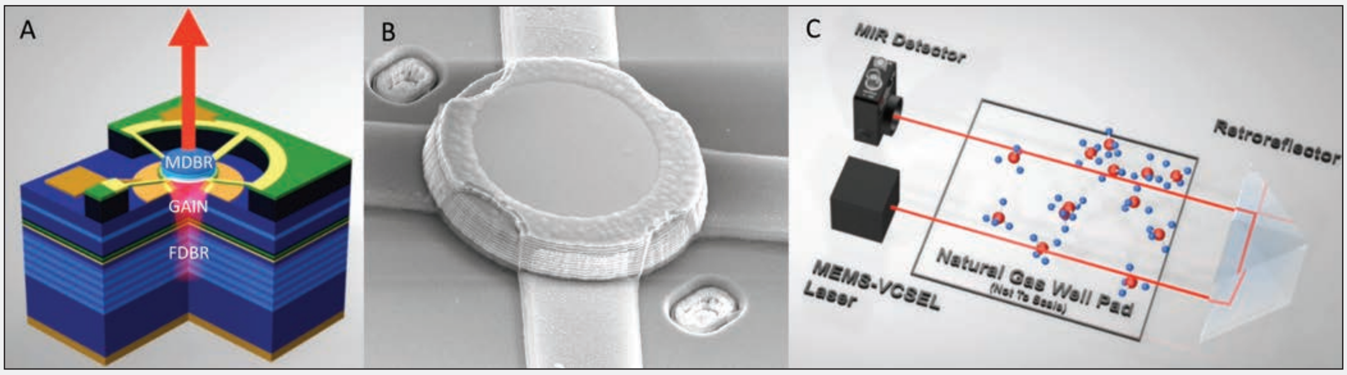


Figure 1. (a) Praevium, in collaboration with Thorlabs, is developing mid-IR MEMS-VCSELs for gas sensing. Chip dimensions are typically 0.6 mm by 0.6 mm. The laser produces a beam in the mid-IR that is about 20 microns in diameter (b) Scanning electron microscopy of actual actuator in the near-IR, showing an airgap size relative to the multi-layer, moveable distributed Bragg reflector. (c) Natural gas well pad methane detection with a MEMS-VCSEL. Figures provided by Thorlabs.

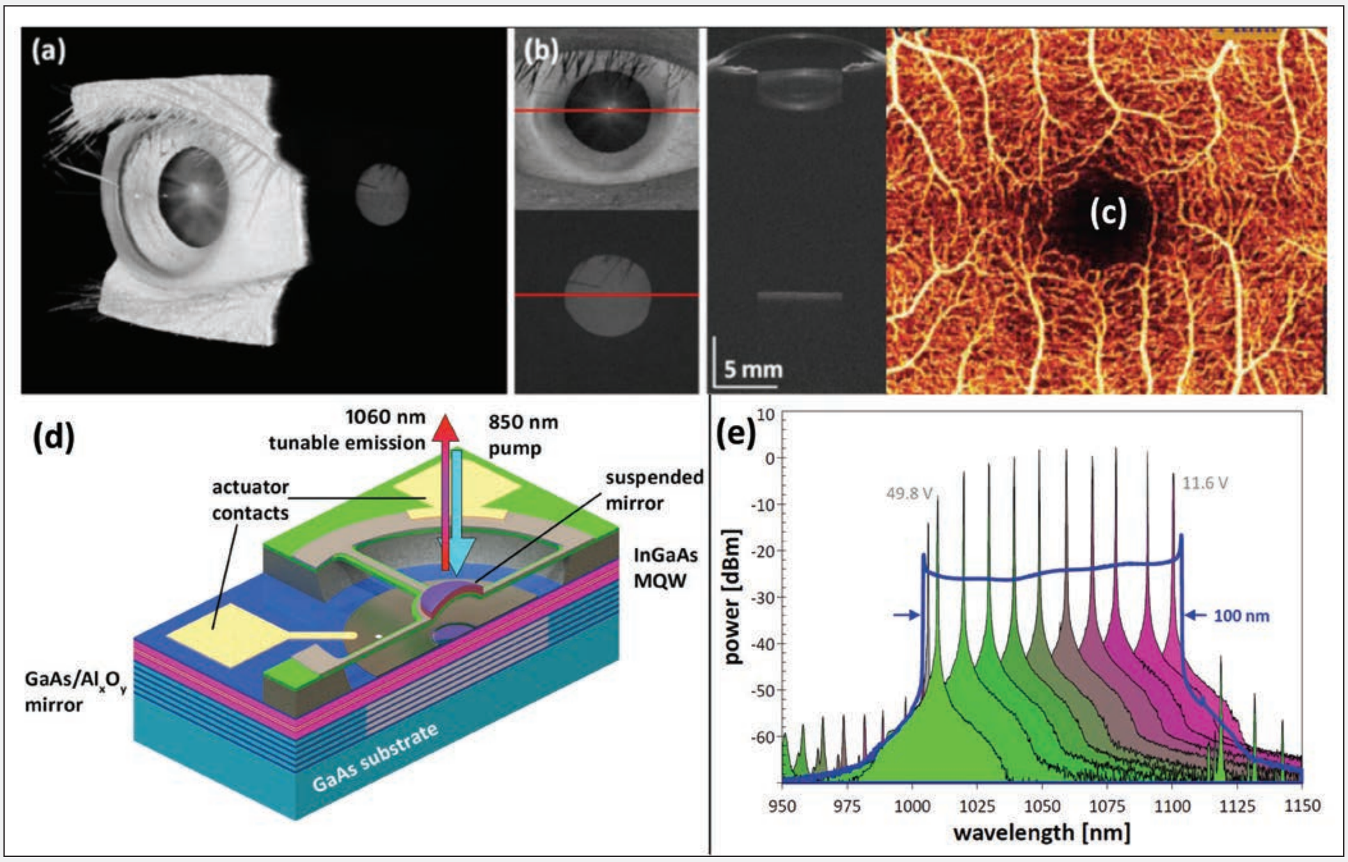


Figure 2. Key 1050 nm MEMS-VCSEL results from Praevium/Thorlabs/MIT. (a) Three-dimensional, whole eye imaging using swept-source, optical coherence tomography with the 1050 nm MEMS-VCSEL depicted in Figure 2 (d) (a, b from Grulkowski *et al*. Biomedial Optics Express **3** 2733 (2012)). Note simultaneous acquisition of anterior eye and retina. (b) Cross sections from the three-dimensional image in (a). (c) Swept-source optical coherence tomography angiographic image of retinal vasculature, using 1050 nm MEMS-VCSEL. (John *et al*. Journal of Lightwave Technology **33** 3461 (2015)). (d) Optically pumped 1050 nm MEMS-VCSEL structure, showing fully oxidized bottom mirror, InGaAs multi-quantum well gain region, and 850 nm pump wavelength. (e) Typical 100 nm tuning range of MEMS-VCSEL in 2 (d), under static (peaks) and dynamic (blue) operation ((d) and (e) from Jayaraman *et al*. Electronics Letters **48** 1331 (2012)).

At Praevium Research of Santa Barbara, CA, working in collaboration with strategic partner Thorlabs, we are playing a vital role in the MONITOR programme. Our focus is developing micro-electro-mechanical systems (MEMS) VCSELs operating near the methane absorption region, which is around 3.3 μm.

We are pursuing this technology because it provides an unprecedented combination of high performance and low cost. Success has already been demonstrated at the near-IR, and can be extended to the mid-IR. In the near-IR, we have produced commercial devices for swept-source, optical coherence tomography medical imaging. Lasers emitting at 1050 nm provided a source for ophthalmic imaging, while those at 1310 nm and offering a wider tuning range have been launched for research and clinical endoscopic and ophthalmic applications.

A key attribute of our lasers is their tunability. This is used to identify gases via a technique known as laser absorption spectroscopy. Tuning the emission and detecting its absorption enables accurate, remote, and rapid quantification of the concentration of the gas, along with its temperature and pressure.

Our tunable lasers have the potential to combine low cost with high performance, attributes that promise to open the door to widespread proliferation of laser absorption spectroscopy for gas sensing. They have the upper hand over the incumbent source in the mid-IR, which is the edge-emitting laser. It is held back by its limited tuning range, speed and a high cost for volume applications.

## MEMS-tunable VCSELs

Like every laser, our MEMS-VCSEL employs a gain region that generates and amplifies light. This is sandwiched between two mirrors that form a resonant optical cavity (see Figure 1). The bottom mirror is a fixed multi-layer distributed Bragg reflector, and the top mirror a movable cousin, suspended on a flexible membrane. The latter mirror is separated from the underlying gain region by a 1-2 μm airgap.

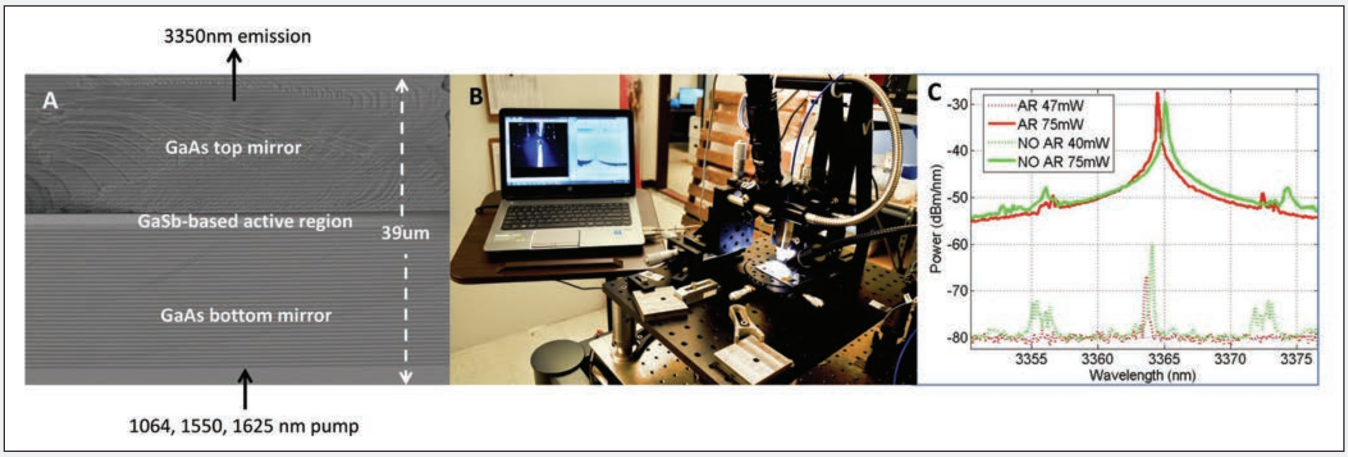


Figure 3. (a) Scanning electron microscopy of a double wafer-bonded device structure. (b) Photo of experimental setup and first recorded room-temperature CW spectrum from March 2017. (c) Demonstration of lasing below (dashed) and above (solid) threshold spectra, using a 1625 nm pump (measurement made in 2018). Note that a doubling of pump power results in a 30 dB increase in output power.

To tune the wavelength of our source, we apply a voltage between the gold contacts. This deforms the membrane, contracts the airgap, and blue-shifts emission of the MEMS-VCSEL.

Our MEMS-VCSELs have the potential to outperform existing mid-IR sources in four key areas: cost, tuning range, spectral purity and tuning speed.

The lower cost results from the manufacturing process. As is the case with near IR VCSELs, MEMS-VCSELs can be fabricated and tested at the wafer scale. With this approach, a 4-inch wafer can yield thousands of devices from a single process run. A key feature of our devices is that even small deflections of the flexible membrane account for a significant fraction of the optical cavity. This enables our near-IR MEMS-VCSELs to routinely produce a tuning range of around 10 percent of the centre wavelength (see Figure 2(e)).

Special purity of our devices is excellent. With a cavity length of the order of microns, our MEMS-VCSELs operate naturally with a single longitudinal mode, corresponding to a narrow line-width and a high spectral resolution. This enables the resolving of closely spaced spectral lines. What's more, tuning occurs continuously, without mode hopping.

The tuning speed of our devices is orders of magnitude faster than that of existing edge-emitting mid-IR tunable lasers. The low mass of the MEMS mirror can produce a mechanical resonance exceeding 1 MHz with full tuning range.

## Challenges in the mid infrared

It is not easy to transfer our success in the near IR to the mid-IR so that our sources can be used for gas sensing. While gain material, grown on GaSb substrates, can produce room-temperature CW operation in the 3-4 μm range in edge-emitting lasers, replicating this performance with a VCSEL has not been possible. Due to resistive heating, VCSELs have been limited to room-temperature, pulsed operation.

Another challenge is that at longer wavelengths it is more difficult to realise current constriction, a pre-requisite for efficient overlap of the injected

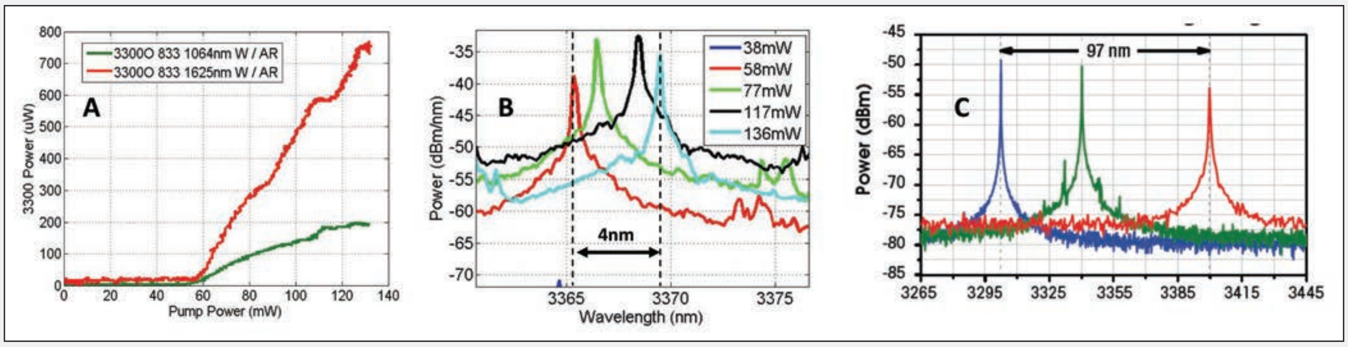


Figure 4. (a) Output power as a function of pump power for 1064 nm and 1625 nm pumping. Note that the 1625 nm pump does not hit thermal rollover, while additional heating with the 1064 nm pump does cause thermal rollover. (b) Demonstration of 4 nm tuning by 1064 nm pump power variation. (c) Wavelength variation across the bonded sample demonstrates airgap tuning over 97 nm, and feasibility of 100 nm MEMS tuning.

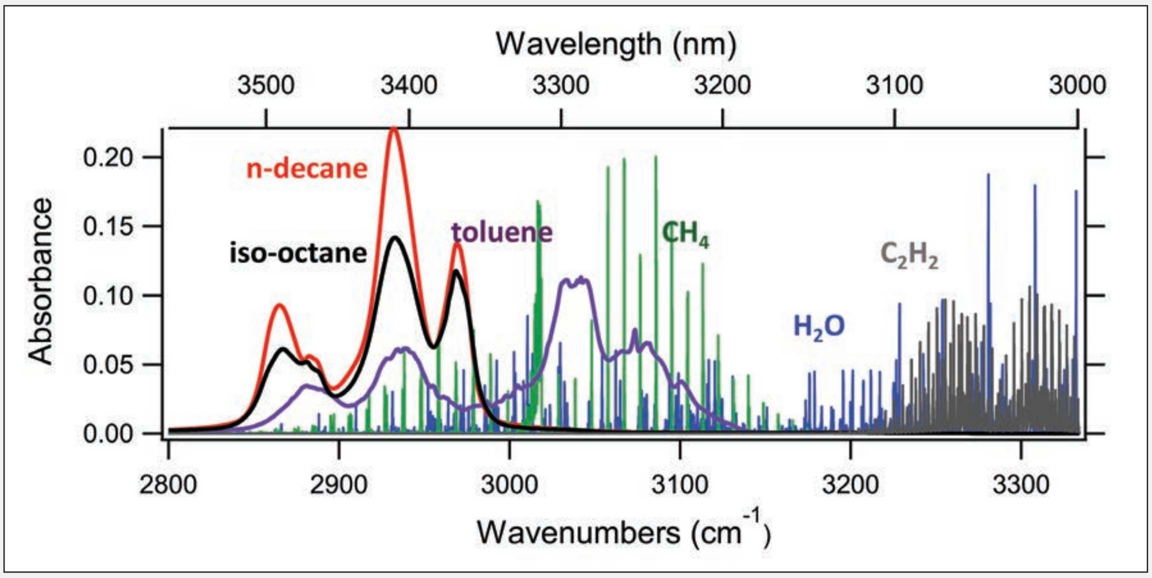


Figure 5. Industrially and environmentally important absorption lines in the 3.0 μm to 3.6 μm region. Figure provided by Greg Rieker at University of Colorado Boulder.

current with the optical mode. This exacerbates heat generation in mid-IR VCSELs.

On top of these issues, there are difficulties associated with scaling the thickness of the DBR mirror. Fixed mirrors operating at around 3.3 μm have been produced by other teams, using the pairing of GaSb and AlAsSb. However, the typical thickness of this mirror is about 12 μm. Add a gain region, typically 3 μm-thick, and the challenge is to grow a complex 15 μm-thick heterostructure using a material system that is considerably less mature than that of GaAs.

We side-step this issue with a wafer-bonded GaAs/AlGaAs mirror. Note that wafer-bonding is a tried-and tested technique, used in our 1310 nm MEMS-VCSELs and widely adopted in the silicon MEMS industry.

Taking this approach greatly relaxes the epitaxial growth complexity for the GaSb portion of the structure. Now growth is just a few microns of the gain region – this is a similar thickness to that of commercially available, edge-emitting lasers. Although there is still a complex mirror to grow, this is accomplished with the far more mature GaAs material system, which is capable of routinely providing structures of the order of 18 μm-thick. Such mirrors may be grown routinely with excellent thickness control and surface morphology. This has enabled, for example, the demonstration of extremely low mid-IR optical losses in GaAs/AlGaAs mirrors by a team at Crystalline Mirror Solutions (see “Semiconducting supermirrors” in the May 2017 issue).

## Lasing in the mid-IR

In March 2017, we combined two wafer-bonded GaAs/AlGaAs mirrors with a multi-quantum well mid-IR gain region epitaxially grown on GaSb. The structure that resulted provided the first ever demonstrated of a CW VCSEL operating at room-temperature with emission near the methane absorption lines around 3.3 μm (see Figure 3). To do this, we employed optical pumping in a fixed wavelength structure, circumventing the problems of resistive heating and current constriction. This success serves as a reliable stepping stone to electrical pumping, as well as offering a viable commercial path in its own right.

It is worth noting that this laser is 39 μm thick – it combines two 18 μm-thick GaAs/AlGaAs mirrors with a 3 μm-thick, GaSb-based active region. It is not feasible to produce such a thick epitaxial structures in a single epitaxial growth, underscoring the strength of wafer bonding.

We have produced room-temperature CW lasing by optically pumping our devices with 1064 nm, 1550 nm and 1625 nm sources.  The pump threshold, around 55 mW, is largely independent of pump wavelength (see Figure 4). Note that 55 mW is a pessimistic assessment of threshold, as we have not fully characterized the optical losses between the pump and VCSEL active region, including losses in the GaAs substrate through which the pump enters.

Encouragingly, pump powers of up to around 130 mW with a 1625 nm source do not lead to thermal rollover for our VCSEL, which produces a peak output of 0.8 mW. The absence of thermal rollover underscores the excellent thermal conductivity of our architecture.

Additional merits of our VCSEL are: a thermal tuning range of 4 nm with pump power variation, which is sufficient to span at least one methane line (see Figure 4(b)); and lasing over 100 nm (see Figure 4(c)). The latter arises because the VCSEL, comprising a fixed gain region and fixed pair of GaAs mirrors, has voids in the bonded interface at different parts of the wafer. This unintentional airgap tuning demonstrates the feasibility of tuning over at least 97 nm by using a variable airgap.

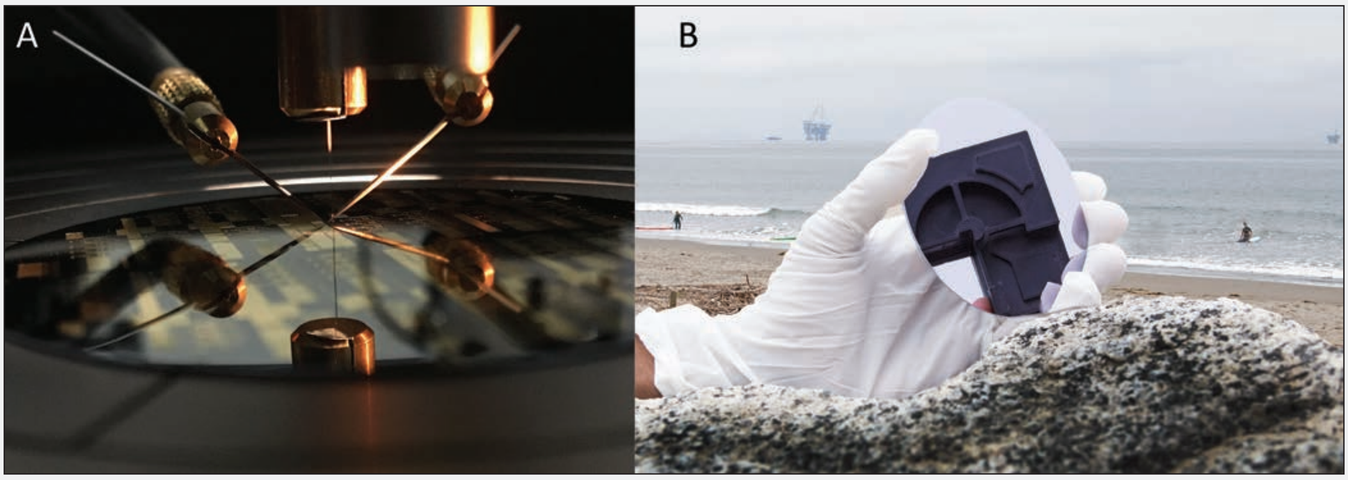


Figure 6. (a) Automated wafer-level testing for near-IR MEMS-VCSELs (from Thorlabs) (b) Reflection of MEMS-VCSEL model in 4-inch GaAs mirror wafer centred at 3325 nm, along part of the Santa Barbara coastline where there is an oil platform in the distance. Early leak detection with MIR MEMS-VCSELs may, one day, help preserve environmentally sensitive regions like this one.

We believe that our results verify our approach. By combining GaAs/AlGaAs mirrors with a GaSb-based active region, we have produced a source with enough power for methane sensing applications. This can go to market, as cost can be low, by utilising the lower cost of the 1550 nm telecommunications pump.

Our source also promises to revolutionise what is possible. With a lasing range of almost 100 nm, our 3.3 μm MEMS-VCSEL could provide a source for detecting multiple species with a single instrument (see Figure 5). Commercial sensors with this capability don't exist today, but they could follow soon, thanks to a technology that offers a pathway to wafer-scale fabrication and low cost.

## Bright prospects

The history of the VCSEL suggests that there will be a good future for the mid-IR MEMS-VCSEL. Its established cousin, the near IR VCSEL, first produced a room-temperature CW output in 1989, thanks to efforts at Bell Laboratories. Thirty years on, the near IR VCSEL is occupying a number of high-volume markets. They include the smartphone, where multiple near IR VCSELs lie at the heart of sophisticated facial recognition and augmented reality systems. Duplicating this near-IR success with MIR MEMS-VCSELs will not be easy, but there are compelling reasons for optimism.

While optical pumping provides a viable commercial path in its own right, the ultimate low-cost sensor will be electrically pumped. Making this transition is far from trivial, but the high thermal conductivity of the GaAs material system provides an ideal marriage partner for the thermally sensitive GaSb material system.

The costs of these chips should not be too high. Production can include the bonding of 4-inch GaSb wafers to 4-inch GaAs, leading to a yield of around 10,000 devices per full wafer run. With full-wafer-level testing available, the prospect of low cost seems entirely feasible. Note that the addition of a MEMS actuator to a VCSEL cavity should not substantially increase cost, provided the actuator can be made with high yield and tested at the wafer level.

Supporting the commercialisation of these devices will be the expertise that we are acquiring through our active involvement in a US government programme to develop high-yield, fully-wafer-level tested near-IR MEMS-VCSELs. Producing these devices, which emit at 1050 nm, will open the door to success in the mid-IR – and in turn inaugurate an era of low-cost environmental sensors.

○ The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000538. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

**Further reading:**

V. Jayaraman *et al*. Electron. Lett. **48** 1331 (2012)
V. Jayaraman *et al*. Electron. Lett. **48** 867 (2012)
W. Bewley *et al*. Appl. Phys. Lett. **109** 151108 (2016)
G. Veerabathran *et al*. Appl. Phys. Lett. **110** 071104 (2017)
V. Jayaraman *et al*. "Room temperature continous wave mid-infrared VCSEL operating at 3.35 μm," Proceedings of the SPIE **10052** February 2018
J. Jewell *et al.* Appl. Phys. Lett **55** 424 (1989)

SEMICON® EUROPA

Co-located with electronica 2018

This year SEMICON Europa will be the strongest single event for electronics manufacturing in Europe and is broadening the range of attendees across the electronics supply chain. The event covers the areas of Materials, Semiconductors, Frontend and Back-end Manufacturing, Advanced Packaging, MEMS/Sensors, Power and Flexible Electronics, and Automotive. **We connect the breadth of the entire electronics supply chain** by including applications such as the Internet of Things, Artificial Intelligence, Machine Learning, and other adjacent markets.

## CONFERENCES:

- Automotive Forum
- 22nd Fab Management Forum
- 2018 FLEX Europe - Be Flexible
- Advanced Packaging Conference
- Strategic Materials Conference

## EXHIBITION AND FREE PROGRAMS:

- Showfloor (Hall A4)
- TechARENA
- TechLOUNGE
- Talent & Leadership in the Digital Economy

## EXECUTIVE NETWORKING EVENTS:

- Executive Keynote Opening
- SEMI Networking Night

## KEY FACTS

More than ...

35% visitors represent engineering job functions

70% involved in purchasing decisions

33% are executives and senior managers

8,700 visitors from 85 countries registered in 2017

## INCREASE YOUR EXPOSURE!

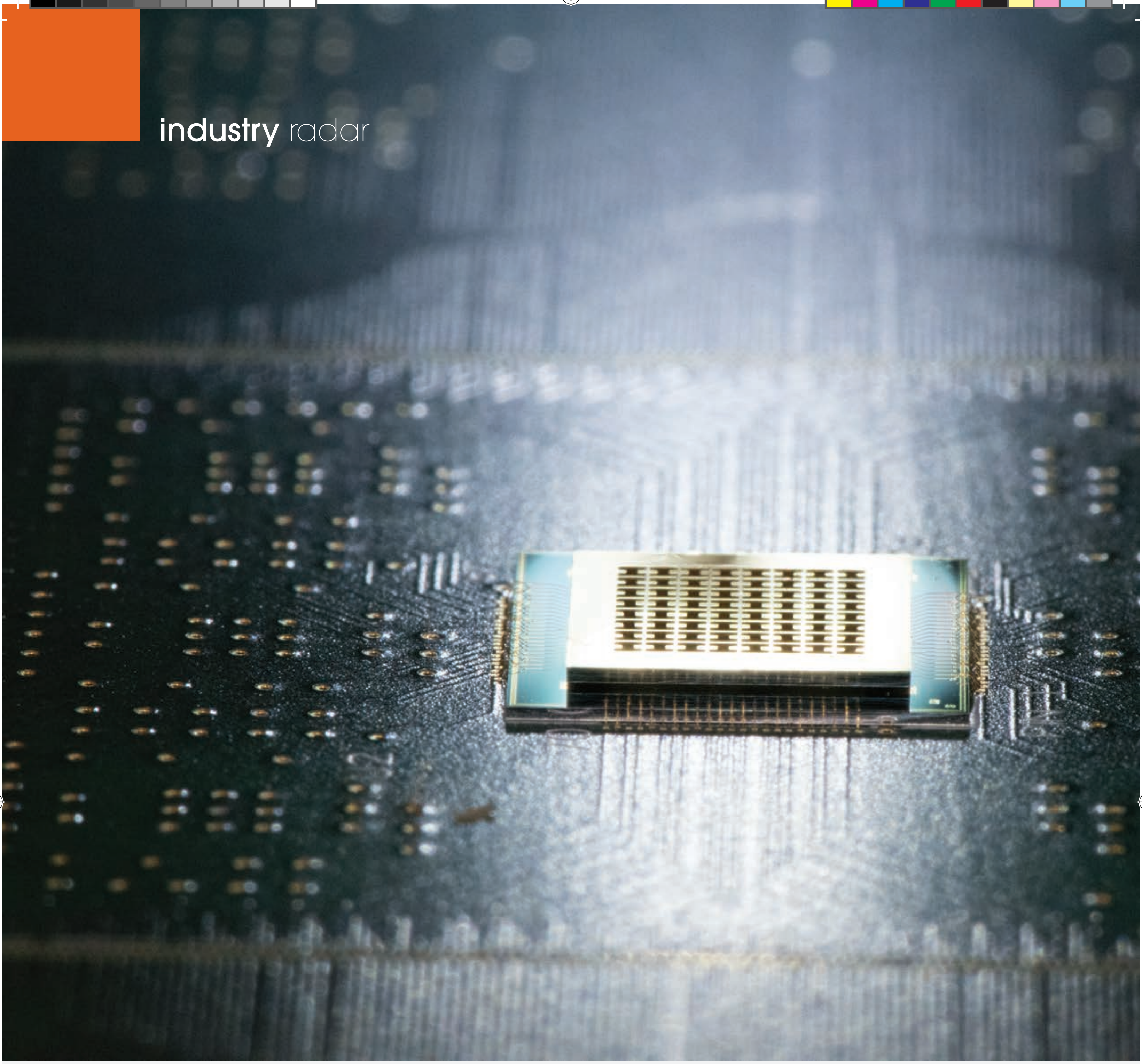
Contact us to **become a sponsor!**
SEMI Europe Sales:
Denada Hodaj, dhodaj@semi.org

To **reserve your booth** contact
SEMI Europe Tradeshow Operations:
SEMICONEuropa@semi.org

**REGISTER NOW!**

semiconeuropa.org

semi



# Enhancing millimetre-wave radar with GaN

Three-dimensional heterogeneous integration of GaN and silicon creates promising arrays for 235 GHz radar

**BY FLORIAN HERRAULT AND JONATHAN LYNCH FROM HRL LABORATORIES**

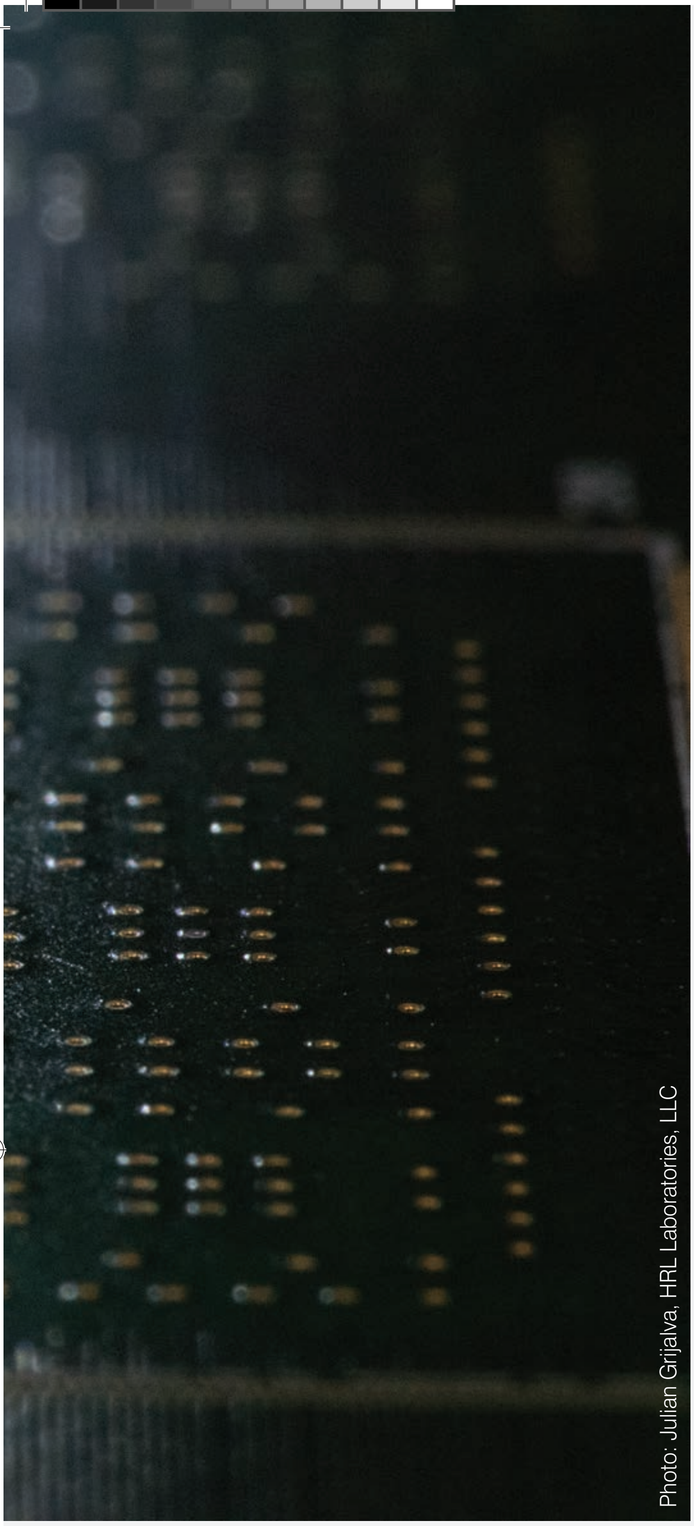


Photo: Julian Grijalva, HRL Laboratories, LLC

MILLIMETRE-WAVE RADAR is an attractive technology for numerous military and commercial applications. Its capability to penetrate through obscurants makes it a promising option for collision avoidance in degraded visual environments, for security screening, and for local-area force protection.

For many of these tasks, millimetre-wave radar will ideally offer a high angular resolution. However, it is challenging to provide this capability with an imaging system that is compact and low in cost.

To meet this challenge, DARPA ran a programme – Advanced Scanning Technologies for Imaging Radars (ASTIR) – that aimed at trimming the size and cost of a form of phased-array radar providing high-resolution imaging on stationary platforms. The technologies developed in this effort target millimetre and sub-millimetre wave frequency bands between 70 GHz and 700 GHz, because this spectral domain minimises aperture size for a given angular resolution. To produce images with thousands of pixels while keeping costs reasonable, those working in the programme used methods of beam steering that are conducive to size scaling.

At HRL Laboratories, LCC, of Malibu, CA, our role within the ASTIR programme was the development of a form of phased array operating at 235 GHz. We refer to it as CASA, short for a Coded Aperture Subreflector Array. The word ‘subreflector’ is meant to suggest that the phased array could be combined with a passive main reflector that provides a large aperture for high resolution, and a subreflector that enables electronic beamforming.

We selected a frequency of 235 GHz, because this is compatible with radar transceivers under development on other programmes. Note, however, that our technology is scalable to higher frequencies.

The foundation for our development of CASA is our Coded Aperture Radar. This features a tile approach that minimizes size and complexity. By combining wafer-level fabrication and integration, we produce tiles containing thousands of elements at a low cost.

Lying at the heart of our Coded Aperture Radar are single-bit phase shifters that are positioned behind each antenna element and modulate the element signals (see Figure 1(c)). As radar signals are received and reflected, the phase shifters rapidly switch through a prescribed set of states, creating a sequence of pseudorandom antenna patterns. The angular location of scatterers can be estimated from the complex fields associated with the aperture codes. These fields may be determined through simulation or measurement.

One of the merits of this technique is that, compared with a traditional digital beamforming approach, it is considerably less computationally intensive. In addition, there may be tremendous simplification of the RF front-end electronics by leveraging computational power.

The architecture of our CASA (see Figure 1) is based on an element pitch of 700 µm, which corresponds to approximately half a wavelength associated with the operating frequency of 235 GHz. The RF portion, consisting of microfabricated ridged waveguide

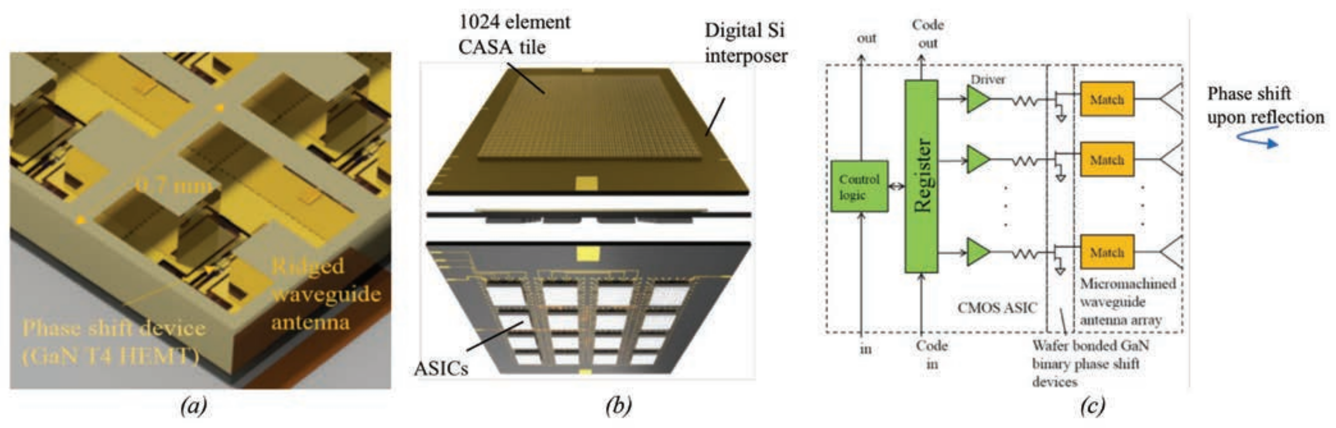


Figure 1. The Coded Aperture Subreflector Array (CASA) structure. (a) A waveguide antenna is coupled to a single electronic device for 0/180° phase shift. (b) The CASA tiles interface to ASICs that control the phase shifter states through a two-sided interposer. (c) Block diagram of the HRL coded aperture radar approach developed during the programme ASTIR (Advanced Scanning Technologies for Imaging Radars). A micromachined antenna array with GaN HEMTs bonded to it provides 0/180° phase shift upon reflection. The phase shifter states are controlled by shifter registers and output drivers.

antennas and our RF GaN HEMTs, resides entirely within the CASA tile. Phase shifter control pads on these tiles connect to a silicon interposer via backside through-silicon interconnects and solder bumps. The control lines feed through to the back side of the interposer, where they connect to the phase shifter control ASICs. Scalability is possible, because each ASIC, which controls 64 phase shifters, is physically smaller than the corresponding 64 CASA elements.

We use open-ended ridged waveguide antennas, because they have a great set of attributes. Merits include an efficiency exceeding 95 percent, a small size that is compatible with our 700 μm pitch, compatibility with wafer-level fabrication, and the opportunity to undertake simple MMIC integration using gold-gold thermo-compression bonding.

To form the antenna array, we use silicon micromachining processes that provide high dimensional accuracy and uniformity. Deep reactive ion etching of 370 μm-thick silicon wafers is followed by 1.5 μm of sputtered gold, creating ridged waveguide array structures (see Figure 2(a)). By optimising various processing parameters, high-quality structures are produced with smooth sidewalls.

The dimensional tolerances of our features are tightly held with excellent repeatability. Measurements of the ridge gap distance, a critical 220 μm feature, indicate average values on one side of 224.2 μm with a standard deviation of 0.2 μm, and on the other side 243 μm with 0.7 μm standard deviation. Note that all these values come from data measured across thousands of elements. The difference between the two sides is due to a repeatable sidewall taper, which is created during etching. We have taken this into account in our design.

A benefit of the silicon micromachining process is that it guarantees a low level of defects. In our 1024-element arrays, there are, on average, fewer than two defects. After etching, we coat our array wafers with gold, before dicing them into arrays of various sizes.

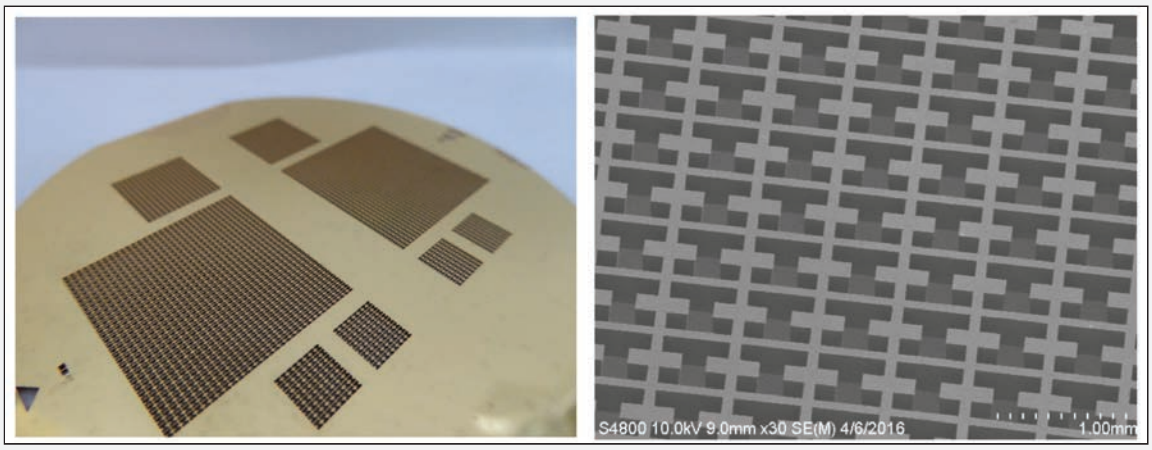


Figure 2. Ridged waveguide antennas are high in efficiency and compatible with wafer-scale micromachining and 3D die stacking technologies. Gold-metalized, silicon-etched antennas show high dimensional accuracy and a low number of defects across thousands of elements.

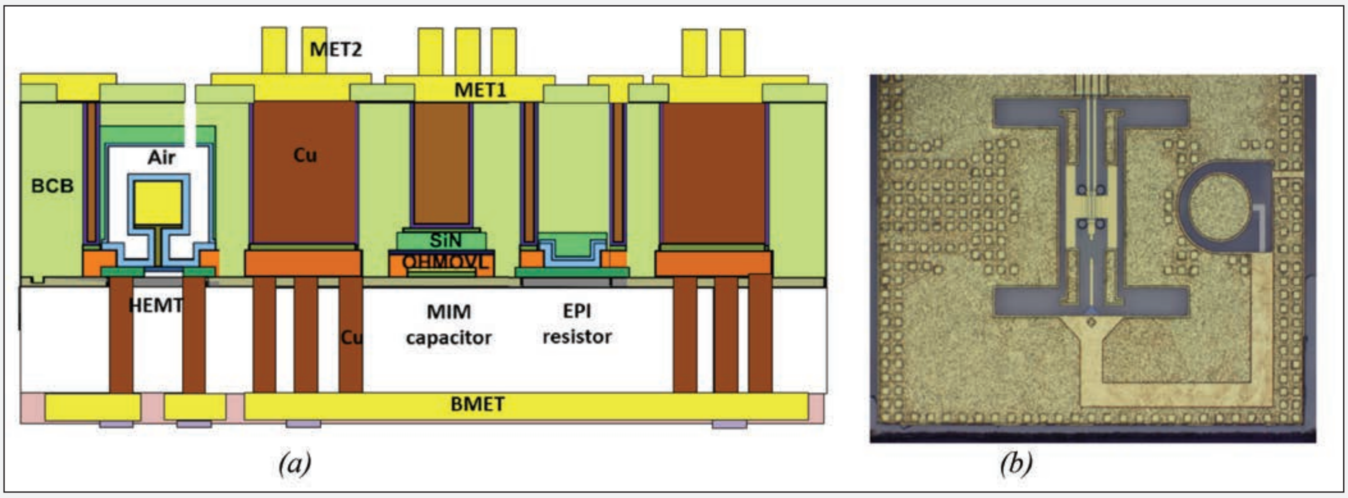


Figure 3. (a) Illustration showing HRL's T4 GaN HEMT structure, which is a copper damascene process with BCB and an air box around the device gate. Process modifications include MET2 for antenna bonding, solid copper vias through a 100 μm-thick SiC substrate, fine feature backside patterning, solder mask dielectric, and nickel pads for solder bonding. (b) Photograph of one MMIC element.

## Integration with GaN MMICs

Our binary phase shifters are constructed with our highly-scaled GaN T4 HEMT technology, which features 40 nm gate lengths and is capable of producing transistors that have a cut-off frequency of 400 GHz, and a maximum oscillation frequency of 600 GHz. For this particular work, the MMICs must provide 235 GHz operation and be compatible with the die stacking process of the CASA tile. We do this by employing a modified version of our T4 HEMT (see Figure 3). Taking 100 μm-thick SiC substrates, we produce transistors with a 40 nm gate length that are covered by BCB dielectric and joined to other components by solid copper interconnects, fabricated using a damascene process.

To reduce the parasitic capacitance, we create an airbox around the gate of the HEMT device. Modifications to process include the insertion of solid copper vias through the SiC substrate, followed by chemical-mechanical polishing of the back side, to produce a surface finish that supports the fine features needed for back side interconnects. Adding a MET2 layer to the top side facilitates antenna array bonding, and the addition of a dielectric layer and nickel pads on the back-side provides a solder mask and a region for solder bonding, respectively. Each of the resulting chips contains an 8 by 8 array of MMICs for 235 GHz operation, permits gold-gold bonding on the top side, and supports solder interconnects on the back side.

CASA tiles are formed by attaching these MMICs to the metallized antenna array by a gold-gold thermocompression bonding process. Any non-ideal planarity between the two mating surfaces is compensated by the 10-μm gold MET2 cubes that reside on the top surface of the MMIC (see Figure 3(b)).

We have produced CASA tiles with 1024 elements, formed from an array of 4 by 4 chips, each containing

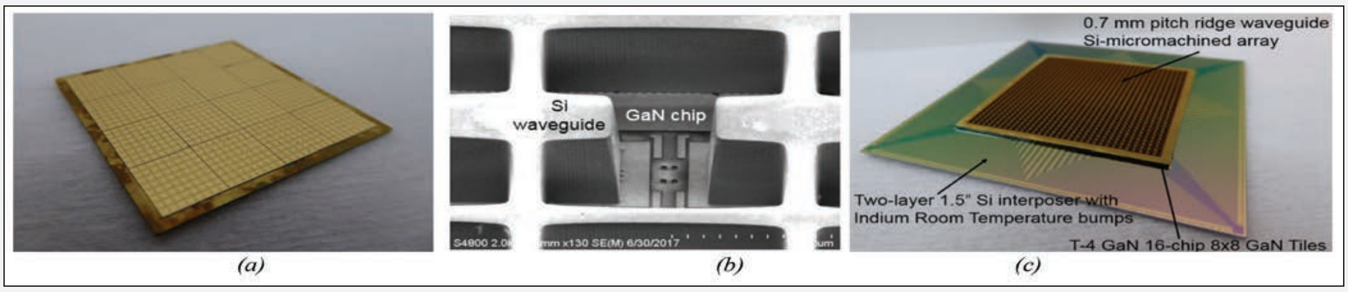


Figure 4. (a) A 32 x 32 element array is formed by bonding sixteen MMICs, each containing an 8 x 8 array of phase shifters, to a 32 x 32 array of antennas. The photo above shows the MMIC side of the assembly, which is then flipped over and solder-bonded to an interposer board (Figure 4(c)). (b) Scanning electron microscope image from the antenna side showing the ridge waveguide and the GaN phase shifter. (c) Photograph of the 1024-element CASA array on a single-side interposer. The CASA tile was bonded using indium bumps at room temperature (evaluation test structures of the same size showed 100 percent indium bonding yield after electrical testing). A phase shifter controller board was implemented using commercial analogue switch ICs for testing. The interposer/tile assembly was then integrated onto the phase shifter controller board using wire bonds.

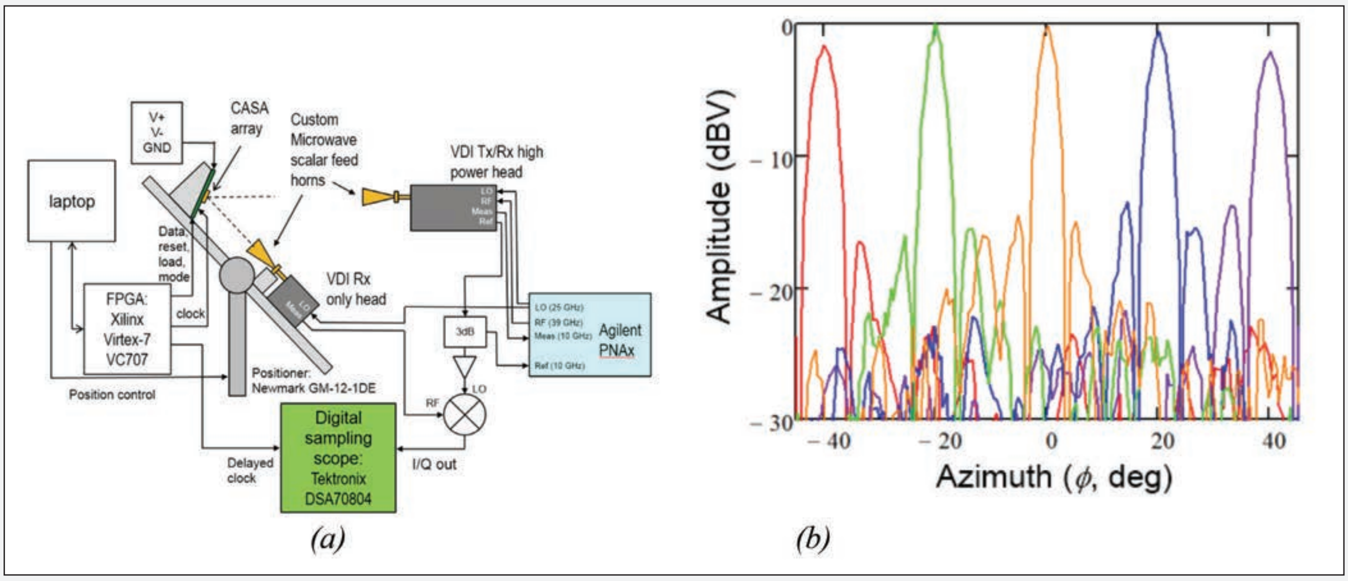


Figure 5. Far-field measurements obtained by mounting the array assembly and a WR-4.3 extension head on a positioner and illuminating the array with a transmitting extension head fixed in the far field. The receiving head was mounted with a scalar feed horn about 3 cm away from the array assembly and 22.5° off-axis, with the array and the receiving head located on a two-axis positioner. A transmitting head was located about 0.9 m from the array on a fixed platform with the antenna aimed at the positioner's central axes. The measured output is demodulated by the transmit reference signal using a phase detector whose output is then recorded by a digital sampling scope. (b) Azimuth pattern cut for beams (with nulls) steered in azimuth in 20° steps demonstrating beamforming.

an array of 8 by 8 MMICs (see Figure 3 (a)). When we produce these CASA tiles, which have sides of approximately 23 mm, our placement accuracy for each of the MMICs exceeds 5 μm, and the gaps between adjacent MMICs are less than 20 μm.

The CASA tiles are bonded to an interposer. One of our early demonstrations involved bonding to a single-sided fan-out interposer with phase-shifter control signals routed to its periphery (Figure 4(c)). This is an important step towards the highly-compact two-sided version with backside ASIC chips (see Figure 1(b)).

To evaluate the performance of our CASA tiles, we collected far-field data for the reflect array, using a vector network analyser with extension heads to record the scattered fields in an anechoic chamber. These measurements involved splitting off the reference signal from the transmit head to the LO input of a phase detector, and supplying the signal from the receive head to the RF input. A real-time digital sampling oscilloscope recorded the baseband output at each positioner orientation, while the phase shifters switched through a set of states. By repeating this measurement over a set of orientations, scattered pattern data is provided for each of the codes. This reveals that the CASA 235 GHz phased array is operating properly (see Figure 5(b) for digital beamforming data from the reflect array with beams formed at 20° intervals in the azimuth plane).

Our work showcases how the combination of RF GaN, advanced back-end-of-the-line processes for III-V device technologies, 3D die stacking, and tile architectures, can aid the production of scalable millimetre-wave phased arrays in imaging applications. Results indicate that our CASA technology is a viable approach for affordable, high-resolution imaging radar.

More generally, next-generation millimetre-wave subsystems require advances in heterogeneous integration of chips with different form factors, drawing on different technologies. We are leveraging such advances to build leading-edge, high-frequency modules for millimetre-wave imaging and communication.

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

**Further reading:**

F. Herrault *et al*. CS-Mantech-2018

J.J. Lynch *et al*. SPIE DCS 2017

J.J. Lynch IEEE Trans. Aero. And Elect. Sys. **52** 918 (2016)

K. Shinohara *et al*. IEEE Trans. Elect. Dev. **60** 2982 (2013)

# Equipping InGaN solar cells with tunnel junctions

## Combining MOCVD and MBE creates the first InGaN solar cell with a tunnel junction

A TEAM from the US is claiming to have broken new ground by fabricating the first InGaN solar cell that sports a tunnel junction.

Their effort will help to unlock the great potential of InGaN solar cells, which combine high-temperature operation with high radiation resistance, a high absorption coefficient and a tunable bandgap across the entire visible spectrum.

According to the team from Georgia Institute of Technology, Arizona State University and PhotoNitride Devices, one of the key merits of using a tunnel junction in an InGaN solar cell is that it substitutes a high resistance *p*-GaN contact layer for an *n*-type top contact, which lowers sheet resistance and improves carrier extraction.

Those are not the only benefits, however: metal electrode coverage can also be greatly minimized on the top surface, leading to an increase in the light coupling to the solar cell, says lead author of the paper reporting the work, Ehsan Vadiee from Georgia Institute of Technology.

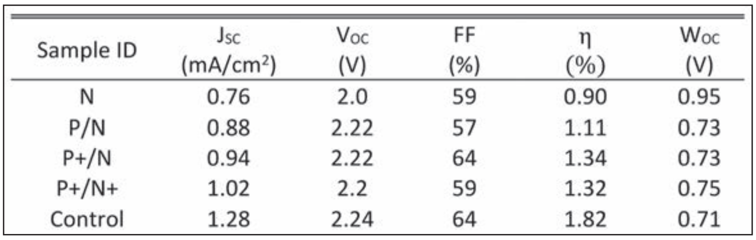
Other groups have taken a different approach to addressing the high-resistance of *p*-GaN: the addition of a layer of ITO, which has a typical sheet resistance of just 40 - 50 Ω/sq. But there are downsides with this, argues Vadiee, such as free carrier absorption losses and additional fabrication steps.

To produce the team’s devices, Vadiee and co-workers grow the epilayers of the InGaN cell by MOCVD, before switching to MBE for the formation of the tunnel junction.

“Achieving a GaN homojunction tunnel diode via MOCVD is not possible with the current state of technology, as high carrier concentrations, which are necessary for tunneling, are not achievable via MOCVD,” explains Vadiee.

When switching from MOCVD to MBE, there is a risk of introducing contaminants to the surface of the sample.

But this can be avoided, argues Vadiee, by undertaking an effective surface preparation of the sample before loading it into an MBE chamber. The team have studied the impact of different types of tunnel junction on the performance of their solar cell, which contains a 20 period multi-quantum well structure with 3 nm-thick InGaN wells separated by 5.6 nm-thick GaN barriers. In addition to an ITO control, tunnel-junction were formed with *n*-type layers, and different forms of *p*-*n* junction (see table for details).



| Sample ID | $J_{SC}$ (mA/cm²) | $V_{OC}$ (V) | FF (%) | η (%) | $W_{OC}$ (V) |
|---|---|---|---|---|---|
| N | 0.76 | 2.0 | 59 | 0.90 | 0.95 |
| P/N | 0.88 | 2.22 | 57 | 1.11 | 0.73 |
| P+/N | 0.94 | 2.22 | 64 | 1.34 | 0.73 |
| P+/N+ | 1.02 | 2.2 | 59 | 1.32 | 0.75 |
| Control | 1.28 | 2.24 | 64 | 1.82 | 0.71 |

Due to a tunnel junction that is too thick, the control device with an ITO layer outperforms InGaN cells with tunnel junctions in five key figures of merit: short-circuit current density ($J_{SC}$), open-circuit voltage ($V_{OC}$), fill-factor (FF), efficiency (η) and bandgap-voltage offset ($W_{OC}$).

Measurements of the short-circuit current density, open-circuit voltage, fill-factor, efficiency and bandgap-voltage offset, reveal that the control outperforms all the tunnel-junction devices in every key figure of merit.

An insight into this finding is provided by a plot of the external quantum efficiency of all the cells as a function of wavelength. This reveals that the efficiency in all the hybrid cells plummets below 365 nm.

To blame are thick, highly doped MBE-grown top layers with a strong absorption at short wavelengths. According to calculations by the team, for a sample with 170 nm-thick re-grown *n*-type GaN, more than four-fifths of the photons with wavelengths below 350 nm that impinge on the device are absorbed before they reach the active region. Vadiee and co-workers plan to address this by trimming the thickness of the tunnel junction to less than 30 nm.

Another goal for the team is to fabricate a double-junction InGaN solar cell that incorporates a tunnel junction and realises a high open-circuit voltage and short-circuit current.

### Reference

E. Vadiee *et al*. Appl. Phys Express **11** 082304 (2018)

# Perfecting trenches in GaN with photo-chemical etching

Photo-chemical etching of GaN yields deep trenches with smooth sidewalls and a high aspect ratio

A VERY PROMISING architecture for GaN power devices is the vertical superjunction. Simulations suggest devices with this design, which sports *p-n* columns, can combine a very high breakdown voltage with a minimal on-resistance.

Fabrication of a GaN superjunction device has not followed, due to the lack of a process to produce trenches in the *n*-type layer with an apertures of a micron or so, and an aspect ratio of more than ten – but this could now change, thanks to the development of a process for GaN photo-chemical etching by a partnership in Japan between SCIOCS and Hosei University.

This collaboration uses a sodium hydroxide electrolyte to etch GaN at a rate of about 25 nm/min. The trenches that result have smooth sidewalls, a depth that can exceed 20 µm, and an aspect ratio of more than seven. After using the process developed by this team, completion of super-junction devices could be realised by backfilling the trenches with HVPE-grown GaN, which can provide *p*-type conduction without the need for a magnesium activation process.

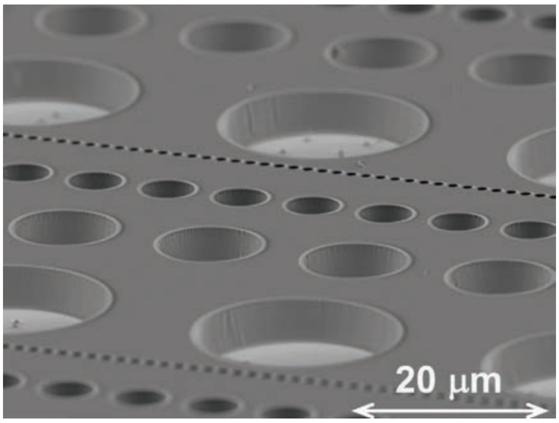


Photo-chemical etching produces circular trenches with a depth of 7.7 µm and diameters of 1 µm, 5 µm 10 µm and 20 µm in GaN Schottky barrier diode epiwafers.

GaN can also be etched with an inductively coupled plasma. But, according to the team, this is not suitable for forming deep, narrow and uniform trenches in GaN. That's because it causes damage to the material, and there is low etching sensitivity between the GaN and the etching mask.

Switching to either neutral-beam etching or atomic-layer etching eliminates the damage caused by the plasma, but etching rates are too low for forming deep trenches. The team developed and refined its process by etching trenches in free-standing, 2-inch GaN substrates with epitaxial structures for Schottky barrier diodes (a 5.8  µm-thick layer of *n*-type GaN doped with silicon to a level of 1.5 x $10^{16}$ $cm^{-3}$) and *p-n* junction diodes (formed by growing a 2 µm-thick $n^+$ interlayer in GaN, followed by: a 10 µm-thick $n^-$ drift layer, doped with silicon to a level of 2 x $10^{16}$ $cm^{-3}$; and then 500 nm-thick and 20-nm thick layers doped with magnesium to levels of 5 x $10^{18}$ $cm^{-3}$ and 2 x $10^{20}$ $cm^{-3}$, respectively). To form an etching mask, 50 nm-thick layers of titanium were deposited by vacuum evaporation, before electron-beam evaporation and lift-off enabled selective removal of material.

To form the trenches, the engineers etched GaN in a 0.01M sodium hydroxide solution, using a platinum counter electrode for the cathode and the GaN epitaxial surface for the anode. Etching took place using a 1 V bias between the anode and cathode, under illumination of 9 mW $cm^{-2}$, provided by a mercury-xenon lamp.

The team found that etching at 24.9 nm/minute produced a smooth surface, but at 175.5 nm/minute, it gave a rough etched surface. However, the rough surface would still be acceptable for wafer-dicing.

Corresponding author Fumimasa Horikiri says that the team's process is almost optimised for obtaining flat etched surfaces for Schottky barrier diodes. "From the view point of the etching rate, I think that it can be improved about two order magnitude." This can be done, to propel etching rates to speeds comparable with dry etching, by replacing the 0.01M solution of sodium hydroxide with a 1M variant.

Horikiri and his co-workers have etched a variety of trenches in both types of epiwafer (see Figure for an example). Their highest aspect ratio of 7.3 came from a trench with a 3.3 µm width and a depth of 24.3 µm.

One of the next goals for the team is to scale up its set-up for photo-electrochemical etching so that it is suitable for processing 2-inch to 4-inch wafers. "We will [also] demonstrate that this technique has capability for N-polar face selective etching or wafer dicing," added Horikiri.

## Reference

F. Horikiri et al. Appl. Phys Express 11 091001 (2018)

# Streamlining single-facet coupling

## A U-shaped waveguide with a Euler spiral aids hybrid photonic integration

A TEAM from Finland has developed a novel, low-loss U-bend waveguide that will help to improve hybrid photon integration.

Carrying out photon integration is not easy, because it is a challenge to efficiently couple silicon waveguides and III-V gain material in a manner that is straightforward and repeatable.

The common approach involves flip-chip bonding, followed by the butt-coupling of silicon waveguides to a III-V chip with an alignment process that has sub-micrometre tolerances. But as the input and output ports of the III-V chip are on opposite sides, alignment of waveguides is required on opposite facets, demanding precise control of the length of the III-V die.

Avoiding this complexity, the researchers from Finland are pursuing a U-shaped waveguide architecture that removes the need for a high level of dicing accuracy.

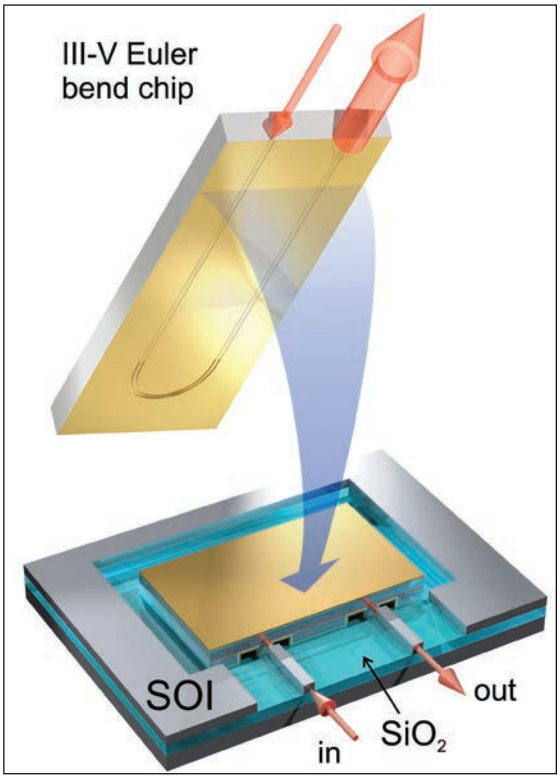
Further benefits of this approach are: that just one edge of the die needs to be aligned with precision; and the spacing between input and output ports can be defined by lithography, leading to a coupling accuracy that is comparable to that realized with heterogeneous and monolithic integration.

The team from Finland are not the first to investigate U-shaped waveguides. But they are breaking new ground, according to team spokesman Heidi Tuorila, by targeting: lower losses for a given bend radius, a larger tolerance to assembly errors, a wavelength that is compatible with silicon photonics, and a smaller size.

Another feature of their work is the adoption of a Euler spiral, which reduces the bending radius in the bending direction to minimize loss in this section. “This is an old optics principle, known also as a clothoid curve or Cornu spiral,” explains Tuorila.

She and her co-workers fabricated waveguides in heterostructures containing two InGaNAs quantum wells surrounded by 318 nm-thick AlGaAs waveguides and 1 μm-thick AlGaAs claddings.

Using two photolithography steps, the researchers formed a range of waveguides with widths varying from 1 μm to 2.5 μm and bend radii from 1 μm to 200 μm. In the first of these steps, patterning defined an etching mask for the bent and straight waveguides, before shallow etching took place through the *p*-cladding. The second step involved protecting straight rib waveguide sections with a photoresist, before etching all the way through to the *n*-side cladding.



A U-bend waveguide simplifies photonic integration by allowing the input and output ports to be on the same facet of the chip

Following this, the team selectively added SiN to the top of the waveguide to ensure mode guiding, thinned the substrate to 110 μm, and metalised the *n*- and *p*-sides. With this design, the U-bend structures could be operated as laser diodes.

“Laser diodes offer a simple and fast assessment of the efficiency and enable estimation of the losses,” explains Tuorila. “Making an amplifier would require more intensive characterization of the gain.”

Measurements of the light output powers at currents up to 200 mA revealed that single pass loss is about 1.1 dB for a U-bend with a radius of curvature of 83 μm and a band length of 519 μm. Additional measurements revealed that gain can be as high as 60 $cm^{-1}$, significant exceeding the measured bend loss.

Tuorila and her co-workers are now extending their design to other optoelectronic devices important for hybrid integration, such as electro-absorption modulators. “In the long term, we are targeting to demonstrate higher-level circuit functionality on silicon photonics using this flexible design approach.”

### Reference

H. Tuorila *et al.* Appl. Phys. Lett **113** 041104 (2018)

# green pages directory

To promote your Products and Services contact:
Shehzad Munshi
T: +44 (0)1923 690 215
E: shehzad.munshi@angelbc.com

**AIXTRON**
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

Non Contact Measurements
Resistance, Resistivity
Wafer Thickness
**KITEC**
microelectronic technologie
Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

**Temescal**
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

**EPIGAN**
Email: info@epigan.com
www.epigan.com

**Fil-Tech**
Tel: + 1 617-227-1133
Fax + 1 617-742-0686
Email: paula@filtech.com
www.filtech.com

**Veeco**
Tel: 516-677-0200-1222
Fax: 516-714-1231
Email: jpina@veeco.com
www.veeco.com

**brewer science**
Tel: +001 573-364-0300
Email: sales@brewerscience.com
www.brewerscience.com

**DOWA**
DOWA ELECTRONICS MATERIALS CO., LTD.
Tel: +1-408-236-7560
Email: asaharah@diccny.com
www.dowa-electronic.co.jp

**WATLOW**®
Powered by Possibility
www.watlow.com

**INNOVION**
FOUNDRY ION IMPLANTATION
Tel: +1 408 501 9100
Fax: +1 408 501 9110
Email: sales@innovioncorp.com
www.innovioncorp.com

**PARTICLE MEASURING SYSTEMS**®
a spectris company
Tel: +1 303.443.7100
Email: info@pmeasuring.com
www.pmeasuring.com

**TYSiC**
1st SiC-epi Foundry in China
Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

**III/V-Reclaim** GaAs InP
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.de

**Masimo**
semiconductor
Tel: +1 603 595 8900
Email: sales@masimo.com
www.masimo.com

**UMC** UNITED MINERAL & CHEMICAL CORP.
MBE Specialists
Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

**kSA**
k-Space Associates, Inc.
Tel: +1 734-426-7977
Email: requestinfo@k-space.com
www.k-space.com

**CS CLEAN SOLUTIONS**
Tel No: +49 (89) 96 24 00-0
Fax No: +49 (89) 96 24 00-122
Email: sales@csclean.com
www.csclean.com

中镓科技集团
**SINO NITRIDE**
Contact: Jiao Chen
Email: jiao.chen@sinonitride.com
Tel: +86 0769 86739999
Fax: +86 0769 86719996
www.sinonitride.com

**evatec**
process systems
Tel: + 41 81 403 8000
Fax: + 41 81 403 8001
www.evatecnet.com

**Vistec**
Electron Beam
Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

**Sanan Integrated Circuit Co., Ltd.**
Tel: +1 949 241 9501
Email: ray@sanan-ic.com
www.sanan-ic.com/en

**MATERION**
Tel: +1 800 327 1355
Email: advancedmaterials@materion.com
www.materion.com/advancedmaterials
Europe: +441 488.686056
Asia: +65 6559.4450

**APPLIED ENERGY SYSTEMS**
Tel: +001 610-647-8744
info@appliedenergysystems.com
www.appliedenergysystems.com

**Pegasus**
Tel: +44 (0)1244 521869
Email: info@pegasuschemicals.com
www.pegasuschemicals.com

# Showcase your presence to the global CS industry for 12 months

Compound Semiconductor magazine is the primary information resource for professionals working with compound semiconductor materials and devices.

Each issue of the magazine is distributed in print and digitally to over 60,000 professionals worldwide.

With the largest and most diverse global audience of qualified buyers served by any compound semiconductor focused magazine, secure a corporate partnership and buyers guide entry today and receive 12 months of promotion and exposure to the cs industry across the magazine portfolio including:

- 12 months of promotion and exposure in eight issues of both the print and digital versions of Compound Semiconductor featuring your logo and company details in the Green Pages Directory
- 12 months of promotion and exposure on the Compound Semiconductor website **www.compoundsemiconductor.net** featuring a Buyers Guide entry and hyperlinked company logo
- An opportunity to sponsor one of our e-news alerts sent out to over 60,000 industry professionals with text and a standard web banner

**To find out more, contact:**

**Stephen Whitehurst**
CEO
stephen.whitehurst@angelbc.com
T:+44 (0) 2476 718970

**Jackie Cannon**
Publisher
jackie.cannon@angelbc.com
T: +44 (0) 1923 690200

**Adam Richardson**
Marketing Manager
adam.richardson@angelbc.com
T: +44 (0) 2476 718970

# CS INTERNATIONAL CONFERENCE

# Why should you choose to sponsor with CS International?

- Are you looking to accelerate your growth and reach the major players in the compound semiconductor industry?
- Do you want to educate, influence and network with the industry?

If you have answered yes to any of the questions above, then CS International 2019 is the perfect event for you. Here are but a few reasons why you must consider sponsorship.

## Reasons to sponsor

1. Access and network with the top strategists within the compound semiconductor industry
As the market leading global compound semiconductor conference for almost a decade, CS International 2019 will allow you to engage with 350+ senior decision makers from the major companies along the entire value chain of the compound semiconductor industry in one dedicated exhibition hall, including over 30 international experts, who will speak at the conference.

2. Raise brand and company awareness
We have an intensive and multi-faceted marketing program available and already underway, which includes email marketing, social media, conference partners, direct mail and live events in addition to promotion in the prestigious Compound Semiconductor print and digital magazine. Coupled with the marketing program, the support of our highly esteemed Conference association and media partners ensure your company, product and service will achieve maximum visibility within the compound semiconductor industry for the next 6 months.

3. Thought leadership and credibility
Aligning with the premier compound semiconductor conference will give you a great opportunity to be positioned as a thought leader in the industry. Engage in debate, share insights and expertise on industry challenges with your peers.

4. ROI and long-term partnerships
Many of our sponsors repeatedly support the event year on year, demonstrating how the industry trusts the CS International brand as the leading information and networking resource to deliver the best programme and ROI. Unparalleled networking opportunities enable you to both build existing and generate new relationships and demonstrate ROI by aligning with the conference brand.

5. Accessibility
We have opportunities to suit all budgets.

6. Post-event exposure
Even when the event is over, you will be included in off-season conference promotional activities, plus the CS print and digital magazine as well as the weekly email newsletter.

Contact: sponsor@cs-international.net to discuss opportunities with the CS International Conference and Exhibition team or by calling +44 (0)2476 718 970 today.

Sponsorship opportunities are limited.