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Pureon drives SiC wafer manufacturing to a new level

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SiC unlocks the door to uncooled electronics capable of handling the cold temperatures found on Venus

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VIEWPOINT

By Dr Richard Stevenson, Editor

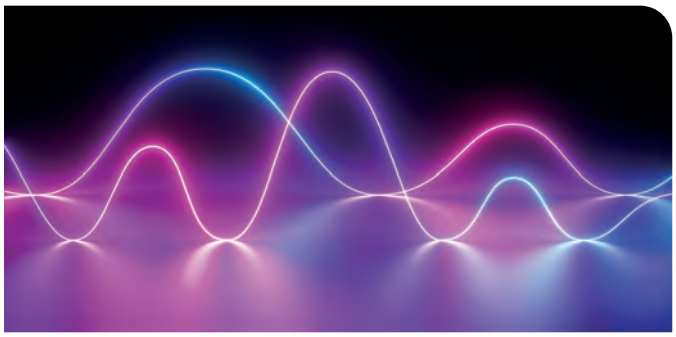
Conquering the deep UV

IT IS COMMON KNOWLEDGE that the Achilles' heel of semiconductor light sources is their feeble emission in the deep UV. That's not that surprising, given that devices emitting in that spectral domain are plagued by point defects that sap efficiency and an incredibly high degree of internal reflection that hampers light extraction.

However, substantial progress is being made, with breakthroughs reported this year in LEDs and lasers – these accomplishments are detailed in this edition's research review. These gains in performance are significant stepping stones towards the commercialisation of GaN-based emitters for disinfection, curing and free-space communication. Note that for the latter, it is a major asset to have wavelengths within the UVC, which is the spectral range from 200 nm to 280 nm. That's because emission is then in the solar-blind region, where there is minimal interference, as well as the opportunity for non-line-of-sight communication, thanks to very strong atmospheric scattering.

For LEDs with a standard emitting area, record-breaking output powers have resulted from switching from a single-emitter to an array of 16 by 16 microLEDs with diameters of 25 μm (see p. 61). In comparison, for similar structures with smaller arrays of larger emitters, the output did not even beat that of the standard LED – while with the 16 by 16 array, output rocketed to almost 85 mW, nearly an order of magnitude higher than the control. The team attributes this leap in output power to a suppression of light absorption and a homogeneous injection current.

For lasers in the UVC, the milestone of continuous-wave emission is tantalisingly



close (see p. 58). Lasers with an output power of around a milliwatt are now capable of this form of emission at an ambient temperature of 5 °C.

Success has come from combining the knowledge gained from prior work with a new architecture. The team that has had this success has built on the merits provided by using a free-standing AlN substrate and polarization-induced doping. To realise continuous-wave emission, their ground-breaking design combines these virtues with: an active region with fewer point defects, and thus a higher quantum efficiency; a cladding layer with a high aluminium content that cuts the leakage of optical modes; and a pair of *n*-type electrodes on the top of the laser that reduces its resistance.

Even better results are on the horizon for both the UVC LED and the laser. The LED promises to produce an even better performance by using a larger array of smaller emitters, while the laser has the potential to deliver emission at higher temperatures by increasing the injection efficiency – it is currently just 10 percent. Realising such success will enable devices operating in the UVC to take a significant step towards shedding their tag of being poor light emitters.

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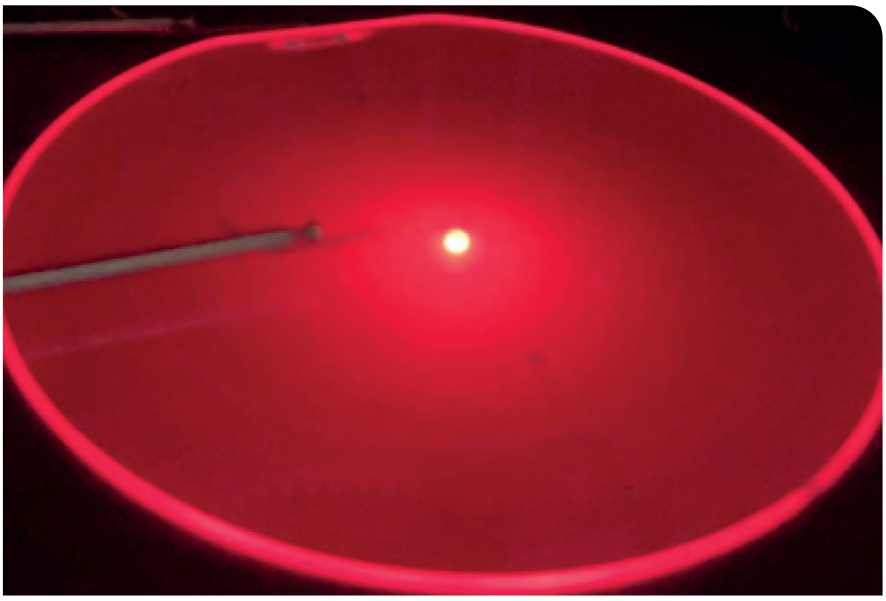
Soft-Epi to ship GaN red epiwafers for microLEDs

SOFT-EPI, a South Korean company that specialises in GaN-based epitaxial growth using MOCVD, has announced that it is shipping GaN red epiwafers for microLEDs. The company says its breakthrough technology can mass-produce red LEDs using existing MOCVD without additional equipment investment. MicroLEDs are considered a key technology for the metaverse platform for enabling next-generation displays for augmented reality, virtual reality, mobile phones, and smart watches.



To make these displays with microLEDs, existing AlGaInP red LED technology has been used. However, AlGaInP has a problem: its efficiency plummets as the chip size becomes smaller, due to its high surface recombination rate.

Also, because it is mechanically weak, the yield drops sharply when transferring, and the expensive wafer prices make the process cost high. Due to these issues, red GaN epi has been receiving much attention from the display industry as an alternative solution, not least because it uses the same material as blue and green microLEDs.

So far, due to technical difficulties, only three or four companies worldwide are known to have succeeded in making GaN LEDs. And these are known to have exclusive contracts with Meta and Google, says James Kimoon Lee, VP of Sales and marketing at Soft-EPI Inc. "It means microLED developers are having difficulties in their R&D because they cannot get red GaN epi elsewhere," he adds.

Inseong Cho, CTO of Soft-Epi, said: "Efficiency still needs to be improved, but it is now good enough compared to top tier developing companies, or we might be top. Anyone interested can visit our homepage where we open our achievement. And we will continue to improve performances along with customers."

Soft-Epi uses patterned sapphire, but the technique is applicable to sapphire, silicon, SiC and GaN. The standard wafer sizes is 4-inch, but 2-inch and 6-inch are available. Wavelength is 620 nm to 670 nm. Wall Plug Efficiency is said to be over 2 percent. Ultimately, this technology will make red, green, and blue sources on one wafer simultaneously. There are also plans to remove the transferring process.

Soft-Epi has already succeeded in making red and green emitters on one wafer, and has a plan to add blue to this pairing this year.

IQE delivers first 8-inch VCSEL wafers

IQE, a supplier of compound semiconductor wafer products and advanced materials, has announced the world's first commercially available 200 mm (8-inch) VCSEL epiwafer.

IQE says its 200 mm epiwafers will enable a step-change in unit economics for compound semiconductors, leading to the expansion of the market it can target. The increase in wafer size will expand to new foundry partnerships, including silicon-based foundries. Furthermore, it enables the integration of compound semiconductors on silicon, allowing adoption across a wider range of devices and applications.

IQE's 200 mm VCSEL development is an example of the company's continued innovation with the aim of expanding the market for wireless and 3D sensing. 3D sensing was made economical within premium smartphones in 2017 when IQE developed and scaled VCSEL epiwafers from 100 mm to 150 mm. The introduction of 200 mm is said to create opportunities beyond the smartphone, into a broad range of intelligent connected devices and also enabling applications in the Metaverse.

Americo Lemos, CEO of IQE, commented: "As we set out in our results in March, a key focus area is growing our business by extending our roadmap to 200 mm to establish new foundry partnerships. This advancement will expand the market for both wireless and photonics applications and service the growing demand for compound semiconductors as macro trends such as 5G and the Metaverse proliferate and capture more value for our technology."

Vertical integration shapes the SiC ecosystem

THE SiC device market will reach $6.3 billion in 2027, according to Yole Développement.

Poshun Chiu, technology and market analyst, Compound Semiconductors & Emerging Materials at Yole, comments: “With more 800 V EVs coming, SiC is expected to grow quickly. Meanwhile, charging infrastructure and photovoltaics are two markets supporting the EV trend. More chargers are needed to support the increasing volume of EVs, and renewable energy shares the same objective of zero CO_2 emission with EVs. These are the markets for SiC to gain more momentum.”

SiC market players are working hard to generate more revenue in this multi-billion-dollar business. Companies including STMicroelectronics, Wolfspeed, Onsemi, and Infineon Technologies have announced billion-dollar revenue objectives. Despite the different paths chosen by each player, the similarity of business model among them can be clearly identified.

The IDM – integrated device manufacturer – business model is the one chosen by leading players to supply devices, especially power modules. This business model represents a higher dollar value to grow the revenue.

The SiC ecosystem has been reshaped by major players in the past years. According to Yole, two main trends impact its supply chain: vertical integration of wafer manufacturing, and module packaging, to gain more revenues in the coming years. In this context, end-system companies, for example, automotive OEMs, are adopting SiC quicker and more flexibly to manage the supply with multiple wafer suppliers in the market.

Innovative approaches to SiC wafer production have been proposed. Even now, the SiC wafer still accounts for a major part of the cost of a SiC device. According to Amine Allouche, technology and cost analyst at System Plus Consulting: “SiC raw wafer cost represents more than 60 percent of the epi-wafer cost for 1200 V SiC MOSFETs. Even though SiC wafer capacity has been expanding, there is still a strong motivation for innovation in quality, throughput, and cost.”

8-inch SiC wafers are considered as the critical step to scaling up production. The objective is clearly to increase yield and gain advantages in the next round of competition. Major IDMs are developing their own manufacturing capability of 8-inch SiC wafers; already, some wafer suppliers are shipping samples.

Another approach to optimising the wafering process is to produce more wafers from a single boule. Solution suppliers, such as DISCO, have developed laser cutting systems to increase throughput; Infineon Technologies has qualified its ‘cold split’ technology; and Soitec has applied its SmartCut technology to produce a SiC wafer that combines a thin layer with a lower defect rate and a handle wafer with lower resistivity. Meanwhile, Japanese company, Sumitomo Metal Mining, has planned to ramp up its engineered SiC wafers in the coming years; and KISAB, a Swedish start-up, is offering wafer-based approaches to offer high-quality SiC wafers.

With a multi-billion-dollar prospect in the coming five years in a strong market mainly driven by EV applications, SiC is expected to enter more and more applications. To make it happen, ecosystem evolution and innovations are the most critical factors to watch. IDM is the main business model in SiC. In addition, major SiC players are moving all along the supply chain toward the module level. The strategy is to create value. In parallel, innovation never stops. Therefore, new entrants are bringing new approaches to improve scaling, throughput, quality, or cost.

Penn State to lead $7.5 million study of radiation effects on GaN

TO BETTER PREDICT and mitigate radiation-induced damage of wide bandgap semiconductors, the US Department of Defense has awarded a team led by Penn State a five-year, $7.5 million Defense Multidisciplinary University Research Initiative Award.

According to Rongming Chu, who will spearhead the project, wide bandgap semiconductors, such as GaN, are inherently more resistant to radiation, due to stronger atomic bonds. However, researchers have yet to reach the full potential of radiation hardness in wide bandgap semiconductor electronics.

"Preliminary studies have indicated that the radiation resistance appears to be limited by defects in the semiconductors, rather than by the material's intrinsic properties," Chu said. "In this project, we seek to understand the radiation effects of these defects, so that we may develop a strategy to redesign the wide bandgap semiconductor device for the ultimate radiation hardness."

Examples of defects include unwanted impurities, displacement of atoms from their original sites, and dangling atomic bonds at the interface between dissimilar materials.

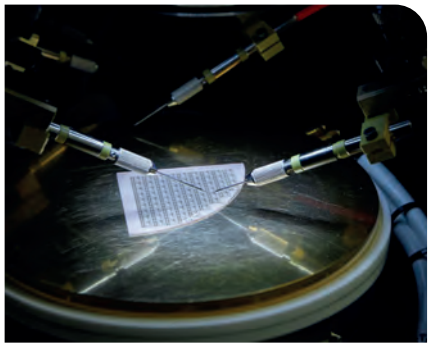
"There is a risk of these defects becoming electrically active under a high electric field, with energetic electrons, causing detrimental effects to device performance," Chu said.

"Today's wide bandgap semiconductor electronic devices are designed such that this risk is minimised under normal operating conditions. However, radiation can force the device out of its normal operating condition by exciting additional energetic electrons interacting with the pre-existing defects. It can also knock atoms out of their original positions, modifying pre-existing defects and generating new defects."

The project will have an interdisciplinary team. Collaborators include Patrick Lenahan, distinguished professor of engineering science and mechanics; Miaomiao Jin, assistant professor of nuclear engineering; and Blair Tuttle, associate professor of physics, all from Penn State; and Tania Roy, University of Central Florida; B. Reeja Jayan, Carnegie Mellon University; and Michael Flatté, University of Iowa.

Chu noted that, at Penn State, the team will use tools and experts affiliated with the Radiation Science and Engineering Center and the Nanofabrication and Materials Characterisation User Facilities at the Materials Research Institute.

"The strength of our project comes from a combination of expertise: my research group's capabilities on GaN devices, Lenahan's expertise in defect spectroscopy, Jin's radiation damage modeling, Tuttle's defect theory work, Roy's electrical characterisation of radiation effects, Jayan's defect



structure characterisation and Flatté's transport theory work," Chu said.

"The teamwork also extends beyond the investigators of this MURI project – especially Michael Lanagan, professor of engineering science and mechanics, who was very instrumental in coordinating this multidisciplinary team effort."

The grant will support 16 graduate students, including 11 at Penn State, to perform multidisciplinary research encompassing physics, computation, materials science and engineering and electrical engineering, as they pursue a variety of master's degrees and doctorates.

"Not only will the research prepare next-generation technologists to take on technical challenges, but, through our collaborative work with national laboratories and industry stakeholders, the students will also learn the professional skills needed bridge fundamental research to real-world applications," Chu said.

ST and Macom make RF GaN-on-silicon prototypes

STMICROELECTRONICS and Macom Technology Solutions have announced the successful production of RF GaN-on-silicon prototypes.

The companies say that prototype wafers and devices manufactured by ST have achieved cost and performance targets that would allow them to effectively compete with the incumbent LDMOS and GaN-on-SiC technologies on the market.

These prototypes are now moving to the next big milestones – qualification and industrialisation. ST is on target to hit these milestones in 2022. With this progress, ST and Macom have begun discussions to further expand their efforts to accelerate delivery of advanced RF GaN-on-silicon products to the market.

"We believe that the technology has now reached performance levels and process maturity where it can effectively challenge the established LDMOS and GaN-on-SiC and we can offer attractive cost and supply-chain advantages for high-volume applications, including Wireless Infrastructure," said Edoardo Merli, Power Transistor Sub-Group general manager and executive VP of STMicroelectronics. "Commercialising RF GaN-on-silicon products are the next big milestone in our collaboration with Macom and with continued progress, we look forward to fully realising the potential of this exciting technology."

"Together, we continue to make good progress in moving the GaN-on-silicon technology towards commercialisation and high-volume production," said Stephen Daly, Macom president and CEO. "Our collaboration with ST is an important part of our RF Power strategy and I am confident that we can win market share in targeted applications where the GaN-on-silicon technology meets the technical requirements."

RF GaN-on-Silicon offers high potential for 5G and 6G infrastructure.

The long-term incumbent RF power technology, LDMOS, dominated early-generation RF power amplifiers. GaN can offer superior RF characteristics and significantly higher output power than LDMOS for these RF PAs. Further, it can be manufactured on either silicon or SiC wafers.

RF GaN-on-SiC can be more expensive because of the competition for SiC wafers from high-power applications and because of its non-mainstream semiconductor processing.

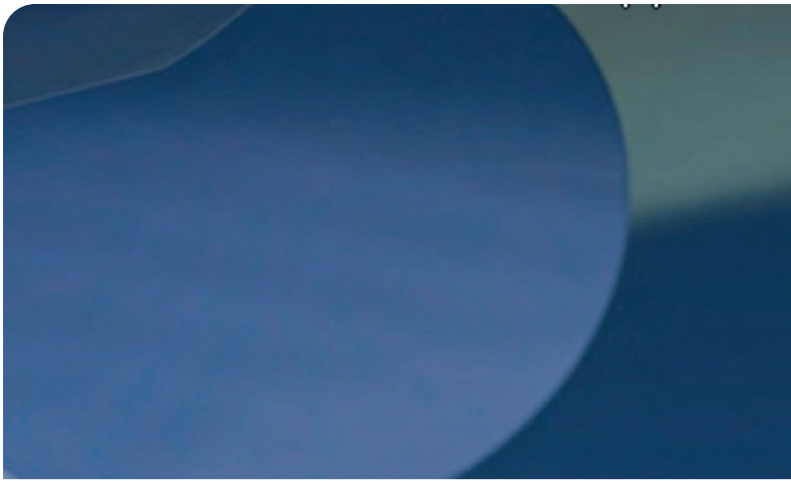
On the other hand, the GaN-on-silicon technology under development by ST and Macom is expected to offer competitive performance paired with large economies of scale, enabled by its integration into standard semiconductor process flows.

Soitec releases first 200 mm SmartSiC substrate

Soitec, the French semiconductor materials specialist, has released its first 200 mm SiC SmartSiC wafer. With the release, Soitec says it is now able to enlarge its SiC product portfolio beyond 150 mm, take the development of its SmartSiC wafers to the next level and cater to the growing demand of the automotive market.

The 200 mm SmartSiC substrate emerged from Soitec's pilot line at its Substrate Innovation Centre within CEA-Leti in Grenoble. The release enabled Soitec to demonstrate the quality and performance of a 200 mm SmartSiC wafer and conduct a first round of key customer validations.

Soitec launched the construction of a new fab in France, Bernin 4, in March 2022. It is primarily dedicated to manufacturing of SmartSiC wafers in 150 mm and 200 mm and is expected to be operational by the second half of 2023. Soitec's SmartSiC technology is said to significantly enhance the performance of power electronics devices and boost electric vehicles' energy efficiency. The technology consists in bonding a very thin layer of high-quality SiC to a very low resistivity polySiC wafer.



"Soitec's SmartSiC substrates will be key for energy-efficient electromobility," says Christophe Maleville, CTO of Soitec. "Our unique technology allows us to pioneer cutting-edge engineered substrates and open up new perspectives for power electronics in the automotive and industrials markets."

He added: "The addition of 200 mm to our SiC substrate family allows us to further differentiate our portfolio and address an even larger variety of customer requirements, in terms of product quality, reliability, volume, and energy efficiency. The release of a 200 mm SmartSiC wafer is an important milestone in the development and deployment of our SmartSiC technology. It underpins our technological leadership, our capability to drive innovation and launch next-generation wafer technologies."

Lumileds adds new high power horticulture and stadium LEDs

Lumileds has announced two new LEDs. The first is the Luxeon SunPlus HPE, a high power, deep-red (660 nm) LED designed specifically for the horticulture lighting industry. The second is the Luxeon HL2Z, an un-domed, CSP, single-sided, high-power LED for stadium lighting that delivers more than 315 lumens and more than 160 lumens-per-Watt from a compact 2.3 mm^2 package that is just 0.36 mm high.

Luxeon SunPlus HPE is is said to achieve the highest PPF and PPE from its industry standard 3.5 mm^2 ceramic package. The new deep-red LED is part of the SunPlus horticulture portfolio that covers a broad range of wavelengths and colours, including white, purple, and lime, in a variety of mid-power, high-power, and CoB packages which offers flexibility to growers to create a specific Lighting mix required for various types of crops to give growers the edge.

"Much of the horticulture market is adopting solutions that use a mix of white and deep-red LEDs," said LP Liew, senior product marketing Manager at Lumileds. "The new Luxeon SunPlus delivers top notch performance. And it's available with extremely short lead-times. At the end of the day, it's the highest performing LED and its shipping."

According to Lumileds, its Luxeon SunPlus HPE has the robustness to stand up to harsh horticulture environments and deliver the longevity expected of all Luxeon LEDs. It pairs exceptionally well with the high-efficacy Luxeon SunPlus 3030 and 5050 LEDs, the two most commonly deployed white LEDs. This white and deep-red horticulture combination can significantly drive down the system cost and reduce operating costs, due to the solution's superior efficacy. The Luxeon SunPlus HPE, with its industry standard package, has various off-the-shelf optical solutions available to enable designers to select the right viewing angles to achieve the appropriate intensity of light for the crops. Luxeon SunPlus is a single portfolio engineered to address the full breadth of horticulture lighting applications.

The Luxeon HL2Z has already been adopted by M3 Innovation, whose MAKO Sports Lighting Solution (pictured above) uses the Luxeon HL2Z to deliver 150,000 lumens from each of its modules designed to illuminate athletic fields, parks, stadium fields and other outdoor facilities. "With Luxeon HL2Z, we were able to completely re-think what can be achieved in a sports lighting solution, the power, optical control, and design possibilities are what made the MAKO disruptive in the market" said Joe Casper, executive officer at M3 Innovation.

"Customers that are engineering street lights, stadium lights and other high luminance directional applications benefit from an un-domed source as it makes it easier to increase optical efficiency and to realize narrow beam angles and complex light distributions," said Alvin Yeoh, product manager. "With Luxeon HL2Z, everything from array configuration design to DLC qualification is simplified and system costs can be lower by 20 percent or more."

In addition to the available LM80 data, rayset data and visual inspection prove the excellence of Luxeon HL2Z's colour consistency across the beam, enabling it to support high quality illumination indoors or outdoors. Luxeon HL2Z is specified for R9≥ 40 for 70CRI, R9 ≥ 0 for its 80CRI, and R9 ≥ 50 for 90CRI parts meaning that solutions with Luxeon HL2Z can qualify for DLC Standard or Premium listing.

SK raises stakes in local SiC power specialist

SK Inc, the holding company of the South Korean SK Group, is acquiring a majority stake in local SiC power semiconductor manufacturer Yes Power Technix.

SK is spending $94.8 million to raise its stake from 33.6 percent to 95.81 percent in order to advance into the EV component business.

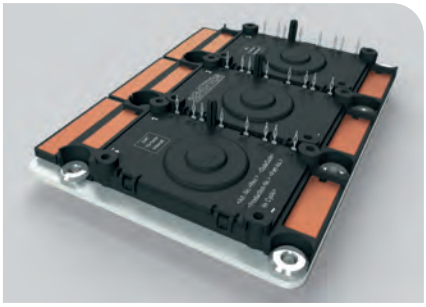
Yes Power Technix, founded in 2017, is South Korea's only power semiconductor company specialising in the design and manufacture of SiC power chips widely used in electric vehicles. SK said it aims to expand the power semiconductor portfolio to other high value-added products, such as GaN-on-SiC power chips used in satcoms and radar devices.

ST reveals details of Semikron SiC partnership

STMICROELECTRONICS has revealed that it is supplying SiC technology for the eMPack electric-vehicle (EV) power modules from Semikron, one of the world's leading manufacturers of power modules and systems.

This is the result of a four-year technical collaboration between the two companies to design-in ST's advanced SiC power semiconductors. SiC is quickly becoming the automotive industry's preferred power technology for EV traction drives, contributing to greater driving range and reliability. Semikron recently announced it had secured a billion-euro contract to supply their innovative eMPack power modules to a major German car maker, beginning in 2025.

"ST's industry-leading SiC device-manufacturing capabilities and in-depth expertise with the technology enabled us to integrate these cutting-edge semiconductors with our advanced manufacturing processes, which enhance reliability, power density, and scalability to meet the needs of the automotive industry," said Karl-Heinz Gaubatz, Semikron CEO and CTO.



"As we now move towards volume-production, our collaboration with ST brings the assurance of a robust supply chain that gives control over quality and delivery performance. Leveraging our SiC technology, Semikron's advanced scalable eMPack family of power modules is ready to make a major contribution towards zero-emission motoring," said Edoardo Merli, Power Transistor Sub-Group general manager and executive VP of STMicroelectronics.

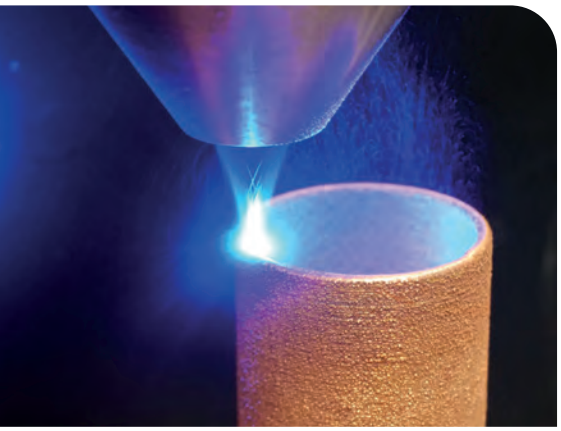
"In addition to its transformative effect in e-mobility, our SiC technology, now in its third generation, is driving increased efficiency, performance, and reliability in sustainable energy and industrial power-control applications."

Engineers from ST and Semikron cooperated to integrate ST's SiC MOSFETs, which control power switching in the main EV traction inverter, with Semikron's fully sintered direct pressed die (DPD) assembly process. DPD enhances module performance and reliability and enables cost-effective power and voltage scaling. Using the parameters of ST's SiC MOSFETs, supplied as bare dice, Semikron has established 750 V and 1200 V eMPack platforms, addressing applications from 100 kW to 750 kW and battery systems from 400 V to 800 V.

Laserline unveils 3kW CW output blue diode laser

LASERLINE presented the world's first blue diode laser with a 3 kW CW output power at *Laser World of Photonics 2022*. The laser was especially designed for welding, cladding and additive manufacturing of copper components. It is a further milestone in the power development of blue high-power diode lasers.

Back in 2019, Laserline presented the world's first blue CW diode laser with up to a 1 kW CW output power, whose power was subsequently raised to 2 kW just a year later. The blue 3 kW diode laser that is now being showcased in Munich displays the highest performance class of industrial lasers in the blue wavelength spectrum to date. In line with the 1 kW and 2 kW Laserline diode lasers, the new laser operates at a wavelength around 445 nm.



This spectral range is absorbed much better by non-ferrous metals, such as copper and gold, compared with infrared radiation. Among other benefits, this allows heat conduction welding of copper components close to the surface, along with more energy-efficient and climate-friendly processes.

Increasing the CW output power to 3 kW now makes it possible to have additional application options. In joining and cladding processes, much faster welds and higher deposition rates can be achieved. In the case of keyhole welding of electrical conductors, such as copper hairpins, larger cross-sections can be handled with moderate heat input using blue lasers only.

Where hybrid solutions combining blue and infrared lasers continue to be required, less infrared energy is needed today. This clearly optimises the operation costs and the CO_2 balance of the applications.

Laserline has also introduced a new high-power-cladding-solution based on a 45 kW IR diode laser. This was developed in cooperation with the Fraunhofer Institute for Material and Beam Technology. This high-power-cladding-solution is meant to optimise the industrial cladding of components that are subject to wear and corrosion.

Being the first process of its kind, it enables wear and corrosion protection coatings for large components – such as power plant elements, brake discs, hydraulic cylinders or plain bearings – to be readily implemented for series-production and in a cost-effective manner.

Access to the use of a higher diode laser power class with up to 45 kW output power further increases the efficiency and productivity of the process. This enables higher order rates and larger quantities at reduced process costs.

II-VI makes multimillion-dollar expansion in Taiwan

II-VI Incorporated will extend its ion implanter disk refurbishing services to Asia, with a multimillion-dollar expansion in Hsinchu City, Taiwan, which is expected to come online in July 2022.

The acute shortages of semiconductor devices in the global supply chain are driving strong demand for refurbishment of wafer fabrication equipment.

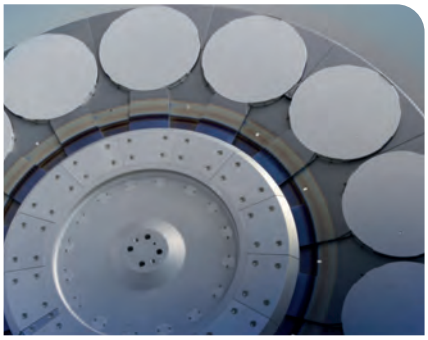
The expansion in Taiwan will effectively double II-VI's global disk refurbishing capacity. Batch implanter tool owners in Asia will benefit from a rapid turnaround service that will enable them to maintain their tools in operation and sustain their production output.

"The market demand for used ion implant equipment already exceeds availability by about a factor of ten, including in Asia," said Sohail Khan, executive VP, New Ventures & Wide-Bandgap Electronics Technologies.

"Our 25 years of expertise and innovations in disk refurbishment enable our customers to achieve an average of 30 percent savings on cost-of-ownership over OEM service," added Khan.

"By coming to us, customers will reduce their maintenance costs and get the most out of their ion implanter equipment from higher reliability and longer service life."

II-VI implants tens of thousands of wafers per week and adds tools and capacity as required to support

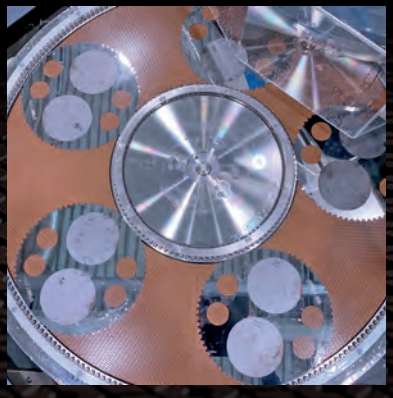


customers' changing needs. The company maintains a large complement of high- and medium-current and high-energy production implanters handling 2-inch to 12-inch substrates.

II-VI provides ion implantation services for silicon and compound semiconductor wafers, including heated ion implantation for SiC wafers.

PUREON

Pureon – A total process solution provider for SiC Wafering



Are you looking for a **solution provider** to help **increase SiC wafer production**? Discover our complete set of solutions for SiC wafering process from ingot slicing to CMP Polish!

Pureon solutions highlights

- **Trusted solution provider** to the SiC substrate manufacturing market for nearly 20 years
- Innovative developer of environmentally friendly wire saw slurries
- Engineered slurry formulations providing process efficiency and stability
- Broad polishing pad offering for all process steps
- Customized process solutions: pad and slurry combinations for optimum cost of ownership

Pureon offers eco-friendly **wire sawing slurries** for slicing of the SiC ingots. Next generation non-oil based wire saw slurries are enabling faster cuts and improved wafer geometry.

Pureon provides the market leading **polishing pads** for SiC wafer manufacturers! They are uniquely designed for diamond mechanical polishing and final CMP polishing of SiC wafers where flatness and ultra-precision surface finish are critical. Higher removal rates coupled with lower defects make these the go to solution for the SiC wafer manufacturers.

Diamond polishing slurries from Pureon are eco-friendly and ideal for polishing SiC wafers! The water soluble, ready-to-use diamond suspensions are designed for rapid and stable processing of SiC wafers. Our slurry suspensions are optimized for highest performance in finishing processes from bulk to fine polishing on various pad combinations, ultimately producing sub nanometer SiC surface roughness.

IRINO – The next generation processing solution for the SiC wafering process! The new composite polishing pad is poised to provide step function improvements in bulk processing of SiC substrates by providing dramatically enhanced material removal rates compared to traditional polishing methods. You can use it for rapid bulk processing of super hard materials such as SiC wafers and accelerate your wafering process to achieve your goals!

Get in touch with us and learn more about our solutions.
Pureon AG, Kreuzlingerstrasse 1, CH – 8574 Lengwil, pureon.com

Building a photonics ecosystem for Europe

By 2030, PhotonDelta intends to have created a pan-European integrated photonics industry that will churn out 100,000 wafers a year. Here's how, reports REBECCA POOL

IN APRIL THIS YEAR, PhotonDelta, of The Netherlands, secured a mighty €1.1 billion in public and private funds to kick-start a pan-European integrated photonics industry. By 2030, the photonics umbrella organisation, which provides InP, SiN and silicon photonics production and prototyping facilities, aims to have created an 'ecosystem' of hundreds of companies delivering more than 100,000 wafers per year, and photonics-related products, to industries worldwide.

As PhotonDelta chief executive, Ewit Roos, highlights, funds will be invested in photonics start-ups and other businesses to scale activities, expand production and research facilities, attract engineers and also to develop, what he describes as, a 'world-class' design library.

"Two to three years ago no-one spoke about strategic autonomy in Europe, but the current chip shortage and today's geopolitical situation have triggered European policymakers to make sure we are not dependent on Asia and the US for this key technology," highlights Roos. "As well as this, we've also seen a need to accelerate the development of photonics technologies in The Netherlands and the rest of Europe."

Indeed, thanks to the likes of Philips and Mathworks, The Netherlands has a rich heritage in tech research and development, with myriad home-grown start-ups already forming the basis of a photonics supply-chain. For example, in The Netherlands alone, LioniX International, Bright Photonics and Smart Photonics have been pushing back the boundaries of photonics design and fabrication, while Phix has been developing photonic integrated circuit (PIC) packaging processes. Staying in The Netherlands, start-ups and scale-ups such as Surfix, MantiSpectra, Quix, Effect Photonics, and so many more, have developed PICs for a broad range of applications, whilst across Europe, a vast array of start-ups including aiXscale Photonics, Germany, and Ommatidia LiDAR, Spain, have been following similar trajectories. What's more, Belgium-based imec is home to SiN and SiPh platforms for CMOS-compatible PIC fabrication; and joint European platform for photonic integrated components and circuits, JePPIX, can be used to develop prototypes based on InP and SiN photonics.

"In The Netherlands, we are strong in research, photonics integration and parts of [photonic chip] manufacturing, but you need all kinds of other expertise to make photonic integrated circuits," says Roos. "At PhotonDelta, we want to bring all of this together and increase the pace of development for photonics manufacturing, in both the front-end and back-end... My dream is that we do for photonic integrated circuits what TSMC has done for today's electronic ICs."

Planning the future

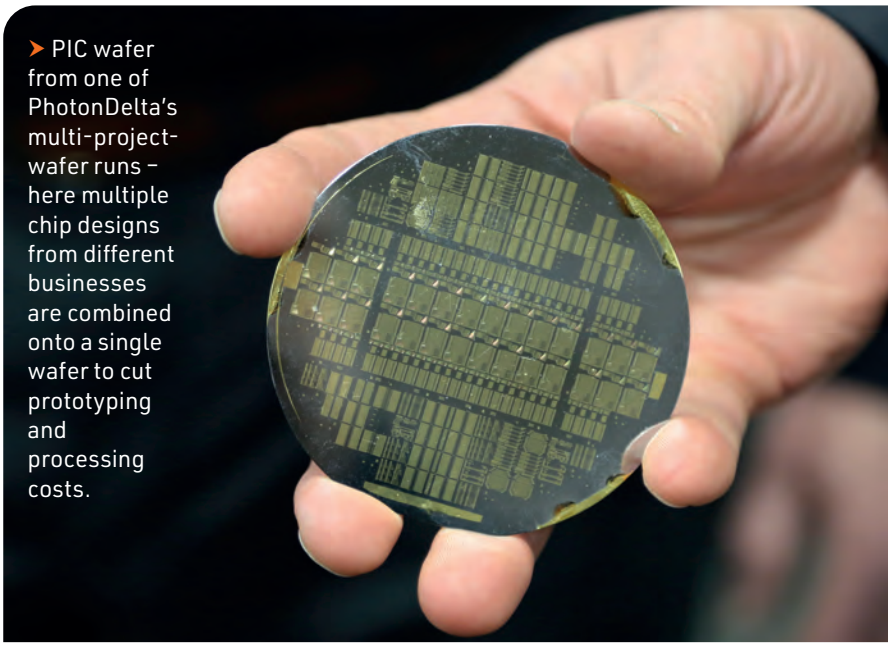
Since 2019, PhotonDelta has been investing in in many start-ups, including Effect Photonics, to develop its DWDM optical SoC technology, Phix, with its high volume PIC back-end foundry packaging facility, and Smart Photonics and its InP foundry processes. Looking forward, investment will continue up and down the integrated photonics supply chain, but at faster pace. Roos points to InP production at Smart Photonics' foundry, SiN PIC development at LioniX, and quantum photonic processor development at QuiX, also of The Netherlands, as just a few investment targets.

Along the way, PhotoDelta has also been offering the legacy semiconductor industry practice of multi-project wafer runs with partners Smart Photonics, LioniX, imec and JePPIX, to reduce the cost of PIC protoyping. "All these players will be receiving a lot of support from us, and it's also important that

➤ A quantum photonic processor from QuiX, of The Netherlands. [Daniel Verkijk, QuiX Quantum]

we work with imec, as we will then have all the important platforms; CMOS, silicon photonics, InP and SiN," points out Roos. "We're not necessarily doing anything new with these firms, but we are accelerating activities."

Critically, Roos is keen to ensure that large-scale photonics production is reliable, stable and robust. Looking at wafer production, some 5,000 4-inch InP wafers are currently being manufactured at Smart Photonics, but Roos anticipates some 100,000, 6-inch InP wafers being produced every year come 2030. LioniX could also be churning out up to 50,000 8-inch SiN wafers, a year, by the same time. Meanwhile, Roos hopes to achieve fully-automated, higher-speed back-end production come 2030 with a comprehensive design library and automated wafer-scale, generic, integration technology across silicon, silica and InP substrates. "You can only survive if you have a world-class library of building blocks that can be used in manufacturing," he says.



PIC wafer from one of PhotonDelta's multi-project-wafer runs – here multiple chip designs from different businesses are combined onto a single wafer to cut prototyping and processing costs.

"We have put a lot of emphasis, in the next six years, on application technology," he adds. "And to be more focused on what high-volume customers require for next-generation applications, be it for automotives, biosensing, agriculture, quantum photonics – you name it."

Clearly, a solid pan-European photonics integration supply chain will demand an equally solid workforce. Roos is confident this will follow, and highlights how Dutch photolithography systems manufacturer, ASML, attracts tens of thousands of job applications every year thanks to its attractive working environment and conditions. Still, the PhotonDelta chief executive is keen to keep an eye on the rest of the world.

"European sovereignty doesn't mean you have to have all of your volume production capacities within European borders – that would be insane and against all economic rules," he says. "But we need to have strategic assets within our borders so the world also comes to us – and for us, this will be photonics integrated circuits and photonics engines."

The billion dollar fab that could change industries

In an iconic moment for silicon carbide and electric vehicles, Wolfspeed opens 'the first, largest and only 200 mm SiC fab in the world'. What comes next, asks REBECCA POOL

On the day that Wolfspeed opened its 200 mm automotive-qualified SiC fab in Mohawk Valley, Upstate New York, the SiC tech supplier also announced a multi-year agreement with Lucid Motors, to supply SiC power semiconductors. Right now, these can be found in the luxury, all-electric Lucid Air.

The two industry developments go hand-in-hand because, as Lucid's senior vice president of product and chief engineer, Eric Bach, exclaimed at the company's ribbon-cutting event: "We need every single SiC chip that we can get." Indeed, a few weeks earlier, Rohm Semiconductor revealed that Lucid was using its SiC MOSFETs in the Air's on-board charger. However, the latest events also signal to the SiC industry that great things are coming.

Officially opened on April 25th and dubbed 'the first, largest and only 200 mm SiC fab in the world', the Mohawk Valley facility is churning out SiC MOSFETs and packaging these up into its XM3 half-bridge power module. Six of these SiC packages will be used in each Lucid Air power-train inverter, providing the low switching losses and high power density necessary for the sedan's modest-sized, 74 kg, 500 kW electric motor.

➤ Wolfspeed is making wafers for Lucid Air electric cars – an Air vehicle cuts the ribbon at the new 200 mm SiC facility.

The Air itself is Lucid's first production model, and has already won the *2022 MotorTrend Car of the Year*, beating the all-electric Porsche Taycan and Mercedes-EQ EQS. The vehicle boasts up to 1100 horsepower and an impressive range of 520 miles.

As Wolfspeed chief executive, Gregg Lowe – who perhaps not surprisingly drives a Lucid Air – highlighted at his facility opening: "This all-electric car has every whistle and bell you can imagine; it's breaking all kinds of electric vehicle records including driving range and recharge time."

Accolades aside, the new facility opens at a time when the buoyant SiC industry is bucking general, worldwide trends. Driven by electric vehicles, analysts predict billion dollar growth for the SiC market with France-based Yole Développement forecasting figures beyond $6 billion by 2027, up from $1 billion in 2021.

In preparation, SiC players far and wide, including Sanan IC, Rohm, II-VI and Infineon, have been building up production capacities. But what sets the new Wolfspeed facility apart is its 200 mm wafers.

Competitors are working on this larger wafer size – for example, STMicroelectronics announced its first 200 mm SiC wafers for prototype devices in July last year while Sanan IC has aired hopes of manufacturing many thousands of 200 mm wafers come 2024. Still, the Mohawk facility is the world's first 200 mm fab, which could accelerate the

industry transition to the larger wafer size, given many companies work with legacy 200 mm silicon wafer equipment. Current yield figures are not available, but the larger-sized wafer is set to raise chip yields by nearly 85 percent compared with 150 mm wafers, helping to ensure the future wafer supply many manufacturers are still striving to truly secure.

Further expansion

Following Wolfspeed's billion dollar investment, the Mohawk Valley SiC fabrication facility comes in at 674,000 ft^2 and is home to a 150,000 ft^2 clean room. Coupled with expanding operations in Durham, North Carolina, Wolfspeed intends to establish what it calls a national SiC corridor along the US East Coast, and also raise SiC wafer and device production capacity by 30-fold, by 2024, from 2020 levels.

Looking beyond 2024, this figure is only set to swell. In its latest earnings call, on 4 May, for the third fiscal quarter of 2022, Wolfspeed revealed a revenue of $188.0 million, a 37 percent revenue increase compared to the same time in 2021, and up 9 percent from the previous quarter in 2022.

In the same call, Lowe also pointed to future capacity expansion saying: "A top priority going forward is increasing capacity for both materials and devices... Wolfspeed will very likely need to add more materials production as well as consider the construction of another wafer fab."

"At this point in time, I can't tell you precisely when and where, but it will certainly be sooner than we anticipated back at our Investor Day [November 2021]," he added.

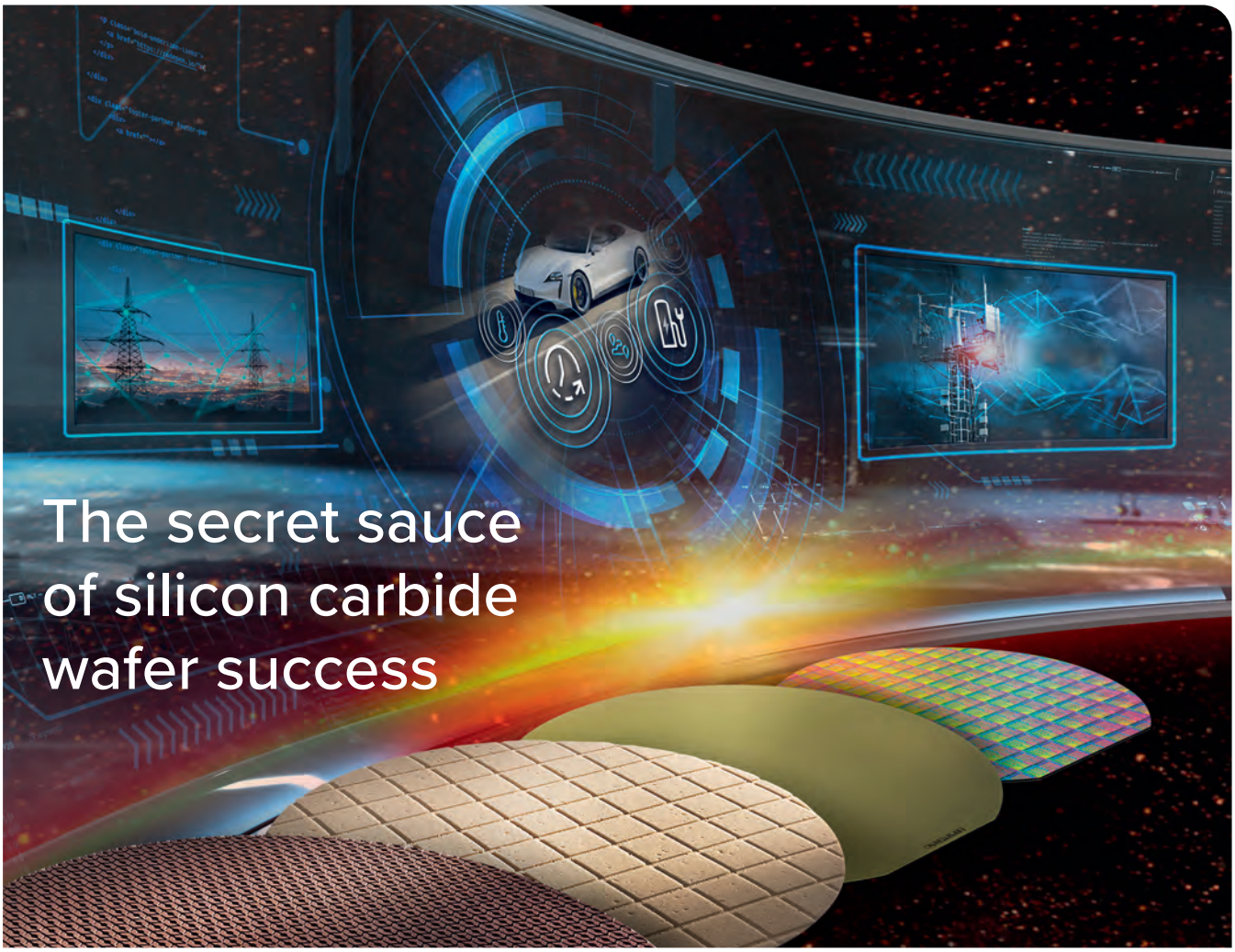
This spells good news for manufacturers of SiC devices worldwide, the future SiC industry, but also the US East Coast, a region that many at Wolfspeed's ribbon-cutting event referred to as 'Silicon Carbide Valley'. While the Mohawk facility has already generated more than 200 jobs, come 2029 numbers are expected to rise to 600. And along the way, Wolfspeed has been investing millions of dollars in neighbouring SUNY Polytechnic Institute, creating an internship programme, scholarship scheme as well as two endowed faculty chairs, to secure its future workforce.

As SUNY Poly acting president, Tod Laursen, highlighted at the event: "We now have the opportunity to build a curriculum specific to the SiC industry, collaboratively with our industry partner [Wolfspeed]."

And his words were backed by New York governor, Kathy Hochul, who also said: "Tell us the skills that you need and we will make sure that our world class institutions in the Mohawk Valley are teaching those skills... [This] is where it's happening, I can feel the energy."

➤ Chief executive of Wolfspeed, Gregg Lowe, shows New York governor, Kathy Hochul, the manufacturing processes at the new SiC fabrication facility in Marcy, New York, US.

The Air itself is Lucid's first production model, and has already won the 2022 MotorTrend Car of the Year, beating the all-electric Porsche Taycan and Mercedes-EQ EQS. The vehicle boasts up to 1100 horsepower and an impressive range of 520 miles



The secret sauce of silicon carbide wafer success

Nearly all devices we use today depend on semiconductors. New technical advancements and requirements necessitate the use of silicon carbide (SiC) for many demanding semiconductor applications. Due to its physical and electronic properties, SiC based devices are well suited for high temperature and high-power/high-frequency electronic devices enabling the advancements in Electric Vehicles (EVs), 5G and IOT technologies. While they bring a lot of benefits for the end-user, the production of high-quality SiC substrates presents many challenges to wafer manufacturers. Pureon has been providing state-of-the-art solutions to SiC wafer manufacturers for over 15 years in the various process steps of slicing and surface finishing.

BY DR. WILLIAM GEMMILL, TERRY M. KNIGHT, DIPL.-ING. HELGE WILLERS, DR. RAVI BOLLINA AND ARTHUR LENART FROM PUREON

LIVING HAS BECOME SMARTER! Our day starts with the alarm from our smartwatch. We clap our hands to turn on the light in our smart home. While we wait for the coffee machine to make our coffee, we check our smartphone for the latest news and updates. Then we unplug our electric vehicle from the charger and drive to work. At work we do our job by being connected to the whole world with the help of cloud-based computers and audiovisual communication systems.

Semiconductors improve our daily lives

We have followed Gordon Moore's Law to once unimaginable levels, and semiconductors have revolutionized the way we work, communicate, travel, entertain, harness energy, and treat illness. They not only make useful devices of our daily life possible, but also make them more compact, less expensive, and more powerful. Take for example the evolution of mobile phones: The first devices

in the 80s were very heavy, cost nearly as much as a car, and held a charge for only about 30 minutes of talk time. Today, our smartphones are highly intelligent mobile devices, nearly as powerful as a regular computer and are available for everybody. Amazingly, the greatest potential still lies ahead. As the building blocks of technology, SiC based semiconductors will continue to enable great breakthroughs: from aerospace and consumer electronics to energy and medicine – entire industries will be transformed. A good example for this transformation is the automotive industry. Electric vehicles have evolved from an ecological niche product to a preferred everyday alternative. This development was supported by more powerful electric drivetrains, using higher currents and more effective circuits. This is where Silicon Carbide plays a dominant role.

Why Silicon Carbide?

The answer is quite simple: more power, higher efficiency and better reliability at higher voltages. There is a transformation not only in the industry but also of semiconductor materials itself. To handle the increased requirements of electric devices, SiC has become the preferred substrate material for advanced semiconductors, especially for power electronics. It allows a 10x higher dielectric breakdown field strength, 15x higher breakdown voltages and offer 3x higher thermal conductivity. In addition, SiC enables higher operating temperatures (up to 400°C vs 150°C for Silicon) and has a 2–3 times higher current density.

The ability of SiC semiconductors to perform at high temperatures, voltages and power has resulted in its increased demand in multiple industries. Data centers for example use SiC for power supplies enabling substantial reduction in power required for cooling systems.

In addition, uninterruptable power supply (UPS) systems ensure a stable, consistent source of power. Another example are 5G base stations: they process an increasing amount of data resulting in a rise of power requirements. SiC semiconductors are used for MHz switching and deliver increased power at a reduced size.

Breakthrough for electric vehicles thanks to SiC

Especially the automotive industry benefits from the advantages of SiC. Thanks to the higher efficiency of SiC semiconductors, manufacturers like Porsche were able to make the transition from 400 V to 800 V batteries. This results in faster charging times, smaller batteries and longer ranges. Other applications that benefit from SiC:

- **On-board battery charger:** Converts the external AC into DC to charge the battery and can double the power in half the size
- **On-Board DC/DC Converter:** Converts the on-board battery voltage into a clean ~12VDC bus to power on-board equipment

"The future of e-mobility will be shaped to a large extent by further improvements in efficiency. To achieve this, losses must be reduced above all by means of appropriate new technologies. High voltage levels such as 800 volts are just as much a part of this as very efficient semiconductors based on silicon carbide and intelligent thermal management. The Taycan already demonstrates this in part, but technological progress still offers plenty of potential for further improvements in future Porsche models."

Dr. Michael Steiner, Dr. Ing. h.c. F. Porsche AG
Member of the Executive Board - Research and Development

- **Powertrain:** The inverter, electric motor, and its mechanical attachment to the driveline. Switching losses to less than 80% with 30% smaller size. Results in a smaller battery (less weight, less heat) and longer range
- **Off-Board DC fast charger:** Faster DC charge stations for rapid recharging

Challenges for the industry

As the demand over the next five years is expected to increase massively, the main challenge for the industry is not only the sheer volume of wafers required but also the changing specifications of the wafers to reflect those of silicon wafers. Tighter tolerances and specifications will push current and future manufacturing methods. Innovation will be critical to overcome these challenges. Taking a proactive approach to anticipate shifts in manufacturing technologies requires developing a deep relationship with process engineers and R&D based upon trust and know-how to develop next generation products.

SiC substrate manufacturers have the drive to improve process efficiency and reduce wafer production costs because the market is striving for power device price parity with Si based devices. Furthermore, the enormous growth in demand (production ramps, new facilities, etc.) and the navigation of global supply chain constraints amidst a surge in demand for both SiC based applications and an overall surge in demand for all types of semiconductors requires innovation in the manufacturing processes.

Optimizing costs from the beginning

Cost per wafer will become a driving factor when developing or optimization of a process step. Most will look to decrease process times, or cheaper consumables, thinking that will drive down the cost. As SiC is increasingly adopted in device manufacturing and moving from a R&D material to commercialization, increase in yield is where a significant improvement in cost of ownership will be achieved. Maximizing yield while minimizing rework, will increase throughput on existing processes.

A major challenge for the industry is the lack of availability of reliable partners for providing surface finishing solutions in manufacturing processes. Unproven solutions and unreliability in new vendors cause the risk of slowing or even halting production or scale-up efforts. This often leads to long lead times for consumables, tools and customer qualification which is a massive hindrance to expand production capacity. That is why consumables have an impact on the whole process. The consistency of pads, slurries and templates run-to-run and lot-to-lot is critical in this effort in optimizing yields.

PUREON- A total process solution provider for silicon carbide wafering

Pureon has many years of experience in the semiconductor industry and has developed proven solutions for wafer production. Pureon supports manufacturers to establish reliable and efficient processes. Pureon's semiconductor history with two decades of developing products for the SiC market, contributes to overcoming the critical manufacturing challenges.

Early engagements with customers in their roadmaps to identify bottlenecks, define resources and expectations is critical. As a consumable manufacturer with in-house wafer processing capability, Pureon is able to conduct testing and generate data with its own polishing and surface laboratories. This capability provides both Pureon with significantly shorter development cycle times and customers with representative data to mitigate risk in the testing and qualification of new products. This benefits wafer manufacturers by shortening the testing and acceptance at their sites. Pureon teams up with OEM's to run full scale tests to confirm findings. This removes the challenge of a customer having to take a tool or cell out of production to do testing and collect data to compare to current process of record.

Optimizing current and developing new processes

A major challenge for the industry is the limited

availability of ingots and wafers, thus increasing the demand to ship anything that can be made. This has emphasized the importance of efficient and reliable production processes. However, any process change could lead to a full requalification, which could take months. Therefore, manufacturers have the drive to optimize their current production processes to benefit from lower process costs. Pureon supports this effort in supplying solutions that extend consumable lifetimes and shortening cycle times, while optimizing and improving yields.

At the same time the market requirements are changing. Hence, the industry is migrating closer to prime silicon wafer specs, requiring manufacturers to develop new processes. A good example is the move from 150 mm to 200 mm wafers, requiring completely different manufacturing flow and equipment. To realize high volume manufacturing processes for these new requirements, new manufacturing technologies are being introduced in all process steps. Pureon's focus on innovation and forward-looking development strategies are uniquely positioned to provide SiC wafer manufacturers with next-generation solutions, supporting the market's maturation through increasing productivity and reducing cost of ownership.

Multi-wire saw processing of SiC ingots – secret sauce for optimum ingot slicing

To prepare SiC substrates for device fabrication one must first cut wafer blanks from the single crystal or ingot. The primary way to do this is through the use of a multi-wire saw that utilizes a thin wire moving at high speeds in combination with a diamond abrasive slurry to precisely cut wafer blanks from the SiC ingot. Major inputs to this process include speeds and feeds, type and size of wire, and the properties of the diamond abrasive slurry. The quality of the cut is judged in the responses of wafer shape, namely bow, warp and total thickness variation (TTV). Successfully cutting high quality blanks at the wire saw step is arguably the most important step of the wafer production process, as downstream improvements in wafer shape are very difficult to achieve.

Pureon provides solutions for the wire saw process in the form of the diamond abrasive slurry and close collaboration with wire saw OEMs as well as customers to optimize this process. Within the wire saw slurry consumable space there are two types: oil-based and non-oil-based formulations. Pureon offers both oil-based (WSO) and non-oil-based (WSG) slurry solutions. Pureon proprietary chemistry and classified diamonds in the slurries provide lot-to-lot consistency which translates to reproducible processes at the customers' site. Furthermore, this eliminates the need to in-house mix wire saw slurry and reduces overhead. Whether it is the first wafer or the 1000th wafer, the properties of the TTV, bow, warp and surface quality are precisely controlled. Hence improving the yield and quality of the wafers.

"As the world develops into a greener and more connected place, evolving technology is enabling this new reality. New semiconductor materials make energy conversion and transmission more efficient. Innovative optical systems transmit exponentially growing amounts of data with ever increasing speeds. The processes used to manufacture the high-tech components and systems that are the building blocks of our future world need to evolve at the same pace. That is the reason why for us at Pureon, progress is never finished. Innovation comes with a deep understanding of polishing processes and materials. Therefore, customers across the world look at Pureon: As a leading manufacturer of diamond abrasives, slurry formulations and polishing pads, we put our in-depth expertise to work every day. Our application experts and abrasive specialists are striving to develop tailor-made polishing solutions for the SiC market, always with the needs of our customers in mind."

Martin and Daniel Spring
CEOs of Pureon

Exciting opportunities for multi-wire-saw processes

Pureon's latest advancements in wire saw slurry offerings are exhibiting exciting opportunities to improve bow, warp, and TTV compared to existing solutions, all while reducing the environmental and occupational hazards associated with traditional oil-based slurries. Recent advances in non-oil based slurry formulation designs are proving to provide excellent wafer quality. These solutions are enabling customers to produce higher quality wafers off the

Wire Saw Slurry	Description	Performance*	
		TTV (μm)	Warp (μm)
Oil-based	Oil-based slurry	4-6	8-15
WSG-52	1st generation non-oil based slurry	5-7	8-15
WSG-56	Next generation non-oil based slurry	2-4	5-8

➤ Table 1. Data collected on 25 wafers cut using 3-6 μm diamond with 160 μm straight wire.

➤ WSG is an advanced glycol based diamond suspension for multi wire saw slicing of SiC boules- with proprietary additives for enahnced stability of the suspension.

saw, setting their subsequent processing up for success as seen in Table 1.

Diamond mechanical polishing of SiC wafers

The next major process in the manufacture of SiC substrates is the mechanical polishing of the wafers using a polishing slurry containing diamonds and a polishing pad. Typical processes are performed on either double side, single side or some combination of double and single side polishing tools. The output from this process step is to present a very flat and relatively low roughness wafer to the final polishing operation.

Critical inputs include the proper selection of diamond based polishing slurry and polishing pad, processing parameters such as polishing pressures, and table speeds, as well as machine selection. Of the critical inputs, the polishing slurry and pad contribute the most to a successful process optimization. Pureon has identified optimum process solutions when it comes to providing customers with maximum process performance in terms of material removal rates, wafer shape, and surface quality, by marrying the appropriate polishing pad and polishing slurry with respect to installed tooling. Pureon's extensive experience in the processing of SiC wafers via diamond mechanical polishing can be leveraged to maximize process efficiency no matter the tool set in customers facilities. Table 2 describes the DMP process flow for bulk and fine removal steps.

Diamond based slurry development has, over the years, been a major focal point for Pureon's innovation team. The company has identified highly optimized formulations that allow for modulation of material removal rates on the different faces of the SiC substrates. Pureon identified diamond types that work synergistically with the appropriate polishing pads and process parameters that continue to extract more performance from this process and drive efficiency gains, see for example Figure 1. Pureon sees great opportunity in driving down cost of ownership for this process step as the 150mm SiC substrate market matures in the coming years.

Chemical mechanical polishing of SiC wafers

The final major process of SiC wafer production is typically referred to as the chemical mechanical polishing (CMP) step. This process step aims only to prepare the substrate surface for epitaxial growth, while imparting zero or as little as possible change to wafer shape. This is typically achieved using a highly reactive chemical based polishing slurry and a polyurethane based or a urethane impregnated felt type of polishing pad to remove only a few microns from the wafer surface. Wafers are delivered to the polishing pad and held in place via a template or wafer fixture in single-side batch tools or via vacuum chuck with a backing film in single-wafer tools. The materials used in these wafer carriers are exposed to the highly reactive chemistry of the polishing slurry, thus requiring robust tolerance to the reactive chemistry.

Pureon continues to develop advanced wafer carriers and films for use in this process to extend the service life, resulting in improved cost of ownership. Pureon has also worked closely with the industry to bring two new polishing pads for SiC CMP to the market as recently presented at the 2021 ECSCRM in Tours, France. These next generation CMP polishing pads are enabling higher productivity and increased quality from the CMP process. The formulation of final polishing slurries has been the subject of extensive research over the years, and innovation continues in this area. Therefore, it is critical for optimization to have a deep understanding of the interactions between the different consumables combinations in this process step. Pureon works closely with final CMP slurry providers to couple their technology with the optimum polishing pad, pad conditioning process

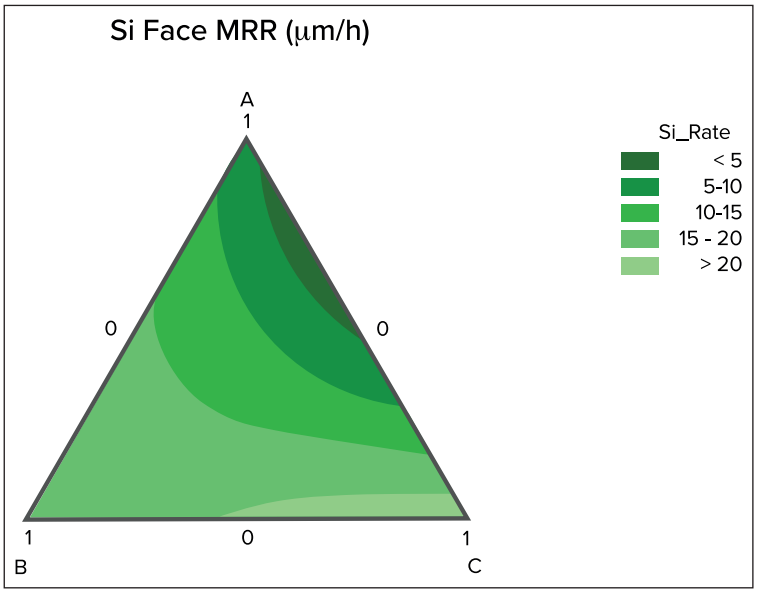
Process Step	Process Goals	Inputs	Outputs
Bulk DMP	● Maximize MRR ● Remove saw damage ● Improve geometry	● As-cut wafers ● Pad & Slurry ● Process	● Wafers near target thickness ● Appropriate geometry
Fine DMP	● Minimize roughness ● Reduce sub-surface damage	● Bulk DMP process wafers ● Pad & Slurry ● Process	● Sub 1 nm roughness ● Low surface defects ● Wafers ready for CMP

➤ Table 2. Goals, inputs and outputs for successful DMP processes.

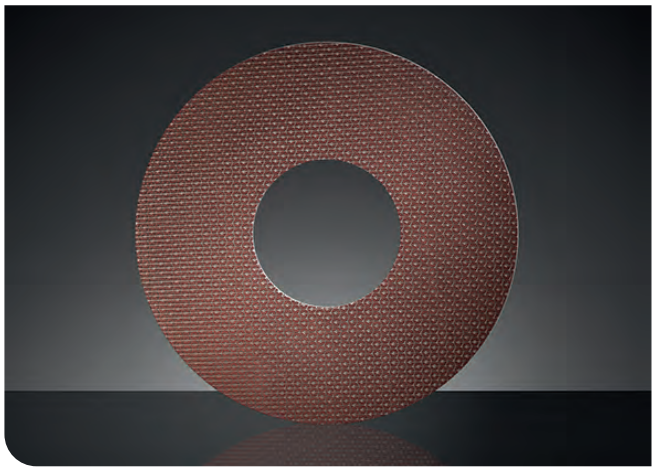
and wafer templates or carrier films. Advancements in final CMP polishing pad technology continue to drive increases in productivity. Pureon continues to drive innovative solutions for consumables and processes for the final polish of SiC wafers.

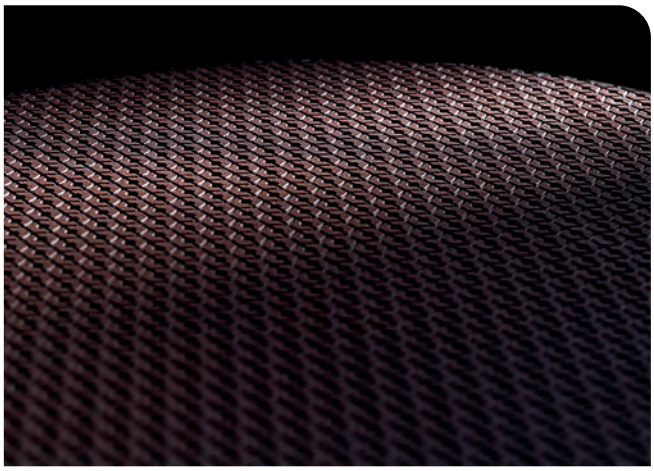
Driving into the future with Pureon

The growth of the SiC device market requires significant advancements in substrate manufacturing, both in the current state and in the development of next generation substrates. Pureon has been supporting the SiC wafering industry for almost 20 years with their knowledge, solutions, and experience in this market. Their experts continue to innovate, to improve substrate yields and lower the cost of SiC wafers, thus enabling a faster adoption of this technology. Pureon drives SiC manufacturing to new limits, enhancing all our lives. That's why innovation and pushing the limits never ends at Pureon. Learn more about their newest solution for lapping SiC wafers using the new pad IRINO-PRO-C. More details and technical presentations will be made during the ICSCRM in Davis, Switzerland, from 11 - 16 September 2022.



➤ Figure 1. Representative silicon face MRR (μm/h) response surface in a three component mixture design using 3 μm monocrystalline diamond.





➤ Combined with application-tailored diamond suspensions from Pureon, IRINO-PRO-C allows for high surface qualities and impressive stock removal rates at the same time.

Makers of epitaxial tools take the top spots

Those making MOCVD and MBE reactors have grabbed the top three places on this year's share price leaderboard

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

WE ARE LIVING in turbulent times. Just as we started hoping we were entering a more prosperous era, thanks to widespread roll-out of vaccines that would help us to approach normality, Putin's forces invaded Ukraine. Now bloodshed dominates our news, and we are all having to contend with far higher prices for fossil fuels.

Against this backdrop, many companies feel like boats in a storm, tossed about by forces beyond their control. Over the last few years they have had to endure the fall-out from Covid – including staff off work, working from home, and disruptions to supply lines – and the recent hike in energy bills. All are taking their toll on profitability.

These factors are also to blame for a sluggish stock market. Over the last 12 months the Dow Jones has remained broadly flat, while European and Asian shares have tended to fall in value. Caught up in this malaise are technology stocks – the NASDAQ is slightly down on where it stood a year ago – and it's of little surprise that the valuation of the majority of compound semiconductor companies has fallen over this timeframe.

However, whether it's simply a matter of being in a more sheltered place at a bad time, or being able to navigate a better path in treacherous conditions, some of the firms within our industry have not been hit as hard as others. Producers of epitaxial equipment have fared particularly well, with German MOCVD maker Aixtron seeing its share price rise by 18 percent in the last 12 months. There are times when this gain might have been good enough for a mid-table spot on our shareprice leader board, but this year it has put the German outfit in the lead by a considerable margin.

Aixtron accelerates

Look at the financial figures and Aixtron has good reason to claim the top spot. Sales for fiscal 2021, which is aligned with the calendar year, totalled

➤ Left: The AIX G5+ is said to be a state-of-the-art planetary reactor module for growing GaN-based epilayers on 150 mm and 200 mm silicon, sapphire and SiC substrates.

€420 million – that's up almost 60 percent year-over-year – while shipments hit a record €181 million in the fourth quarter. Margins are healthy and increasing, with gross margin rising from 40 percent to 42 percent year-over-year. This has helped to drive up the consolidated net profit from fiscal 2020 to 2021 by 175 percent to €94.8 million.

Soaring sales have come from shipments to chipmakers in various sectors. In fiscal 2021, revenue for MOCVD tools sold to makers of SiC and GaN power electronics doubled year-over-year, with sales to the optoelectronics and solar sectors not far behind. LED-related revenues increased by 39 percent compared with 2020.

Speaking to investors on 24 February, 2022, on the release of the fiscal 2021 results, company CEO Felix Grawert explained that for the GaN power electronics sector, Aixtron is at the start of a growth cycle that will last for several years. Behind this ramp is the increased adoption of GaN-based power switches in IT infrastructure, renewable energies, data centres and white goods. "Some customers are even telling us that their roadmaps have been pulled in by two-to-three years due to the acceleration of adoption," remarked Grawert. Within this dynamic market, Aixtron is supporting substantial expansions at existing customers and shipping tools to new players.

Grawert has been delighted to see a growth in orders from SiC chipmakers, which accounted for 15 percent of all equipment orders in the fourth quarter. Based on the order pipeline, further growth is expected, supported by a new tool that accommodates 6-inch and 8-inch wafers. "Even though it is still in development, we are already receiving sizeable orders for it," remarked Grawert. Aixtron continues to play a key role within the LED market. While the microLED sector grabs the headlines, sales are also strong for MOCVD reactors for red, orange and yellow LEDs that are deployed in fine-pitch displays and horticulture applications, such as indoor farming.

Within the emerging microLED industry, Aixtron is involved in a number of major development projects involving large consumer electronics players and LED specialists, such as HC SemiTek.

"We get clear signals from customers that innovative displays of the next generation will be based on microLEDs, rather than OLED displays," commented Grawert. "This is very good news for us, as our MOCVD epi tools are very well positioned here, and the same properties become relevant that make us so successful in GaN power, and in lasers and VSCELs."

Manufacture of microLEDs is forecast to accelerate towards the end of this year and continue through 2023 and 2024. Aixtron's tools will initially be used to produce devices for smartwatches, followed by high-end TVs. Further ahead, microLEDs will be deployed in smartphones, AR/VR glasses, laptop displays and possibly cheaper medium- and large-size TVs. "It will be a multiyear roadmap of different types of displays," remarked Grawert, who added that the company is so confident that microLEDs will dominate the display industry that it has closed down its OLED subsidiary APEVA.

As well as increasing its orders in sectors that are growing, over the last few years Aixtron has been winning market share amongst the makers of MOCVD tools, according to analyst Gartner. In 2018 Aixtron accounted for 46 percent of a $553 million market, and by 2020 its share had risen to 58 percent of a $438 million market.

Compound Semiconductor Shareprice Leaderboard

Rank	Company	Ticker	Share value, April 27, 2021 ($)	Share value, April 27, 2021 ($)	% appreciation	Change in Rank
1	Aixtron (Frankfurt)	AIX	20.12*	23.66*	17.6	+5
2	Veeco	VECO	23.29	23.43	0.6	+3
3	Riber (Paris)	RIB	1.91*	1.80*	-6.1	+11
4	NASDAQ composite	IXIC	14170.91	12918.00	-8.8	+7
5	Lumentum	LITE	94.90	85.21	-10.2	+11
6	Wolfspeed	WOLF	119.76	104.20	-13.0	-5
7	Rubicon	RBCN	10.54	8.97	-14.9	+7
8	II-VI	IIVI	74.56	61.99	-16.9	-5
9	Infinera	INFN	9.80	8.01	-18.3	+1
10	Skyworks	SWKS	201.18	116.51	-42.1	-5
11	Qorvo	QRVO	200.36	112.82	-43.7	-5
12	WIN Semiconductor (Taipei)	3015.TWO	12.67*	6.99*	-44.8	+1
13	AXT	AXTI	11.61	6.04	-48.0	-11
14	Emcore	EMKR	6.69	3.42	-48.9	-2
15	IQE (London)	IQE	79.36*	38.05*	-52.0	-6
16	IPG Photonics	IPGP	234.06	95.44	-59.2	-8

* * Converted to dollars using the exchange rates on 27 April of 1 EURO = 1.0556 USD, 1 GBP = 1.2537 USD and 1 TWD = 0.033956

➤ Many companies in the compound semiconductor industry, haver seen their share price fall over the last 12 months.

Thanks to a very healthy market share in a growing market, Aixtron is predicting that its order book will total between €520 million and €580 million this year. Sales are tipped to surpass those from 2021, rising to between €450 million and €500 million.

"We believe that in 2022, half of the order intake will be from power electronics," revealed Grawert, who said two-thirds of that will come from GaN, and a third from SiC.

Grawert said that Aixtron is working with two of the biggest chipmakers within the SiC market. "From these very large players, we have received very sizable orders, and we expect to receive additional very sizable orders throughout 2022." The company has also either been qualified, or is in the process of being qualified, by another ten or so customers that are producing SiC devices. None of them are in the top five SiC device makers today.

For fiscal 2022, the other half of Aixtron's orders will come from makers of optoelectronic devices. This is a mix of producers of lasers, including VCSELs and sources for optical networks, and various forms of LED – in that sector there is roughly a 50/50 split between makers of fine pitch/miniLEDs and those producing microLEDs.

Veeco's valuable portfolio

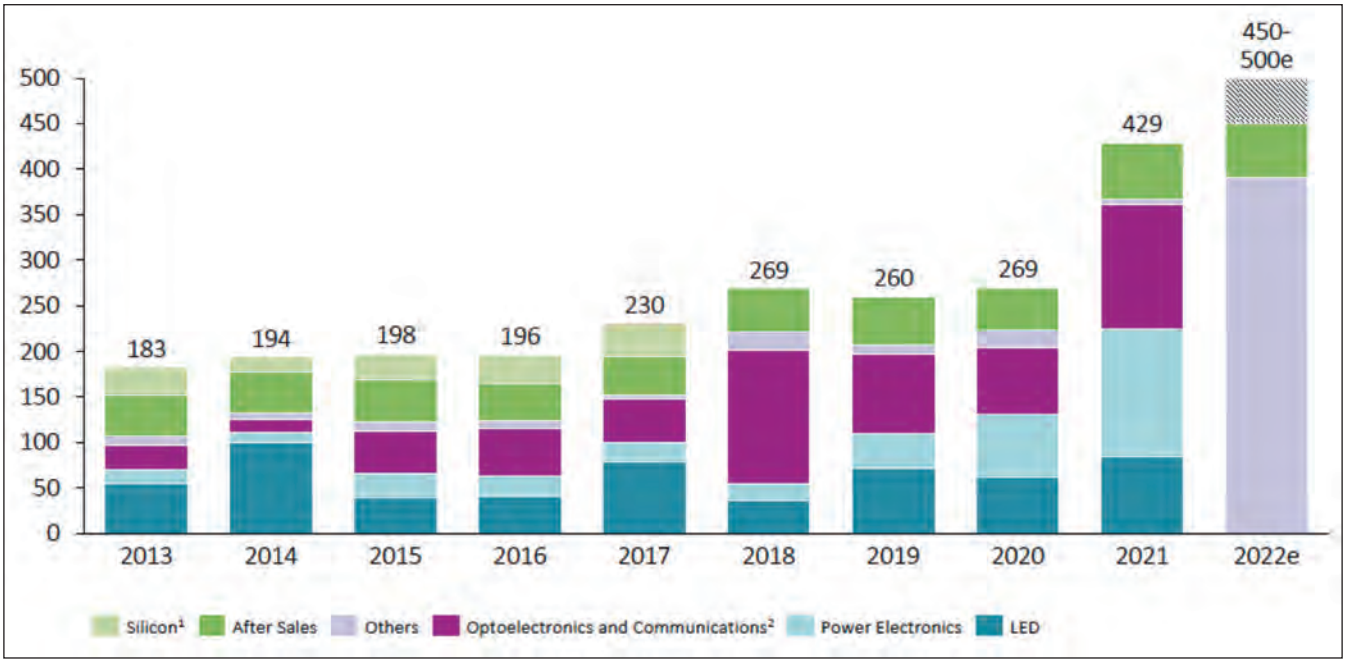
Second on the Compound Semiconductor share price leaderboard is Aixtron's biggest rival, Veeco, that has had a sales headwind in the form of trading tension between the US and China. There has been a fractional gain over the last 12 months in the Veeco's valuation. Sales have has a good year across a portfolio of tools that include those for MOCVD, laser annealing and ion implantation.

For fiscal 2021, which aligns with the calendar year, Veeco reported revenue of $583 million, up 28 percent compared with the previous year, and claimed 'significant' profitability. Commenting on these results in an earnings call on 16 February, 2022, CEO Bill Miller remarked: "We're thrilled with our progress in '21 and equally as excited about our growth prospects going forward."

The lion's share of Veeco's 2021 revenue came from semiconductor sales, associated with the shipment of tools for laser annealing, advanced packaging, lithography and ion-beam deposition. This part of Veeco's business brought in $247 million in fiscal 2021, a year-over-year increase of 49 percent. In comparison, the compound semiconductor division, which is a combination of MOCVD tools and those for wet processing, netted $107 million. That's a figure similar to that for 2020.

"However, normalizing for about $20 million of one-time commodity LED sales of slow-moving inventory in 2020, the $107 million in 2021 represents underlying growth in the areas where we currently focus," remarked company CFO John Kiernan during the February earnings call.

The other significant sector for Veeco is data storage. This brought in $169 million in 2021, up 37 percent over the previous year. Within Veeco's compound semiconductor portfolio, its wet



➤ Figure 1: Aixtron's sales have taken off over the last few years, driven by a surge in sales to makers of power electronic devices. Note that: (1) the company sold its silicon ALD/CVD product line in 2017; and (2) that sales allocated to optoelectronics and communications include revenue associated with consumer optoelectronics, solar, telecom/datacom and wireless/RF communications.

processing equipment is claimed to offer excellent process control and flexibility, by being suitable for many different materials. During the fourth fiscal quarter, 2020, Veeco shipped multiple systems to photonics and RF customers.

According to Miller, Veeco's MOCVD business is starting to see traction within the photonics market, thanks to a multi-system order for its Lumina platform that can be used to produce red microLEDs, speciality red and orange LEDs, edge-emitting lasers and VCSELs.

"Longer term, we believe we're well positioned for the microLED and 8-inch GaN power opportunities with both our Lumina and Propel platforms," added Miller, saying that he expects sales from the compound semiconductor division to grow significantly this year.

This positive outlook has contributed to a guidance between $640 million and $680 million for 2022. The principal drivers for this strong outlook are 35 percent year-on-year growth in semiconductor and compound semiconductor markets.

Rallying Riber

French maker of MBE tools, Riber, has enjoyed a relatively good 12 months. This has helped the company climb 11 places up the leaderboard and grab the third spot. Over that timeframe sales have remained steady, but they are forecast to rise throughout this year.

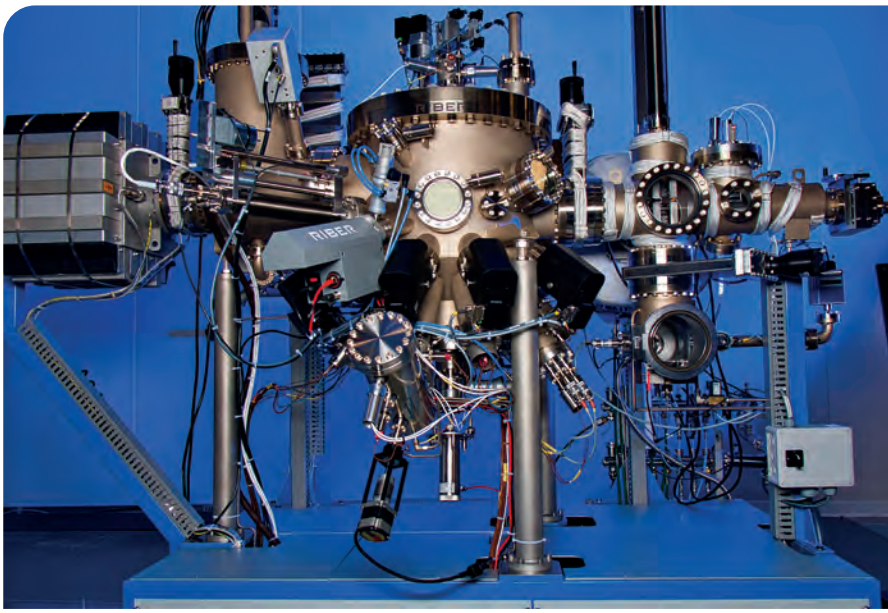
For fiscal 2021, which tracks the calendar year, revenue totalled €31.2 million, up 3 percent year-over-year. Sales of eight MBE systems netted €17.4 million, with the remainder of revenue attributed to services and accessories. Gross margin hit 35.4 percent, up 5.3 percent compared with 2020, helping the French outfit to report a profit of €1.5 million.

Plenty of orders have been placed with this MBE specialist over the last few months. The company had orders for three MBE systems at the begining of the year, and another six in the first quarter 2022. Riber is also enjoying a 'robust' level of orders for services and accessories. Taken together, these bookings are worth around €24.0 million. In the latest quarter, additional orders have been placed, with the company stating that it has 'a strong pipeline of prospects'.

Another reason why Riber is upbeat is that it believes that it is well positioned to support the emergence of a stronger European semiconductor industry. The French firm is forecasting profitable growth, founded on its technological and industrial know-how, and its capacity for innovation.

IPG slumps

Many compound semiconductor chipmakers have seen their valuation plummet over the last 12 months. Falls of 40 percent or more have happened at some of the biggest players, including RF industry stalwarts Qorvo and Skyworks, leading epiwafer supplier IQE, and substrate specialist AXT. But none of them are at the bottom on our leaderboard – that distinction falls to fibre laser manufacturer IPG, which has seen its share price fall steadily over the last 12 months from just over $230 to just below $100. Looking at the company's financials, the figures are certainly not that bad – there's a healthy profit and sales growth, but not necessarily as fast as investors had been hoping for.

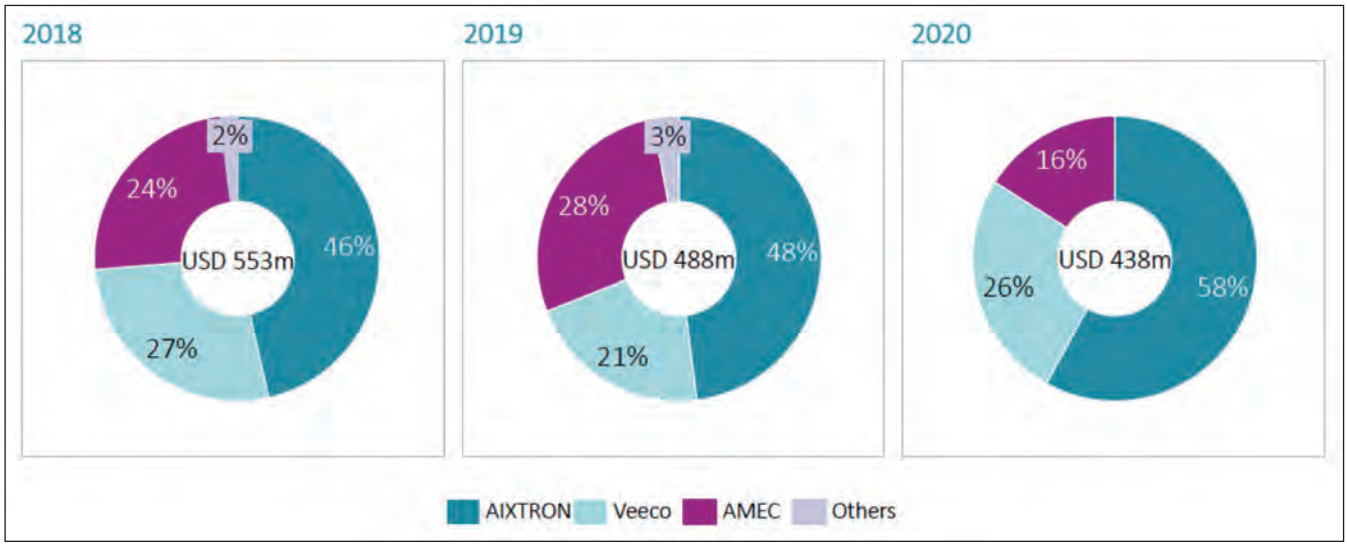


➤ Sales of MBE reactors for R&D provide a significant share of Riber's sales, which are forecast to increase in the coming years.

For fiscal 2021, which follows the calendar year, IPG has posted sales of $1.46 billion, up 22 percent over 2021, alongside a profit of $278 million, 74 percent higher than the previous year. And for the fourth quarter – the latest to be reported – revenue hit £364 million, an 8 percent increase over the equivalent quarter of the previous year, while gross margin climbed by 190 basis points over that timeframe to hit 45.5 percent.

However, while the overall picture is positive, there are some small concerns within these figures. One is that sales to China fells 4 percent between quarters three and four, due to a reduction in revenue from high-power cutting applications – and another is that gross margin fell over that timeframe, due to a combination of an increase in the cost of products sold, inventory provisions, higher shipping costs and unabsorbed manufacturing expenses.

Offering more insight into the state of the business during a call on 15 February, 2022, to discuss quarter four earnings, company CEO Eugene Scherbakov explained that the recent fall in sales to China's high-power cutting market was offset by increased revenue from high-power-laser shipments



➤ Figure 2: According to analysis from market research firm Gartner, Aixtron has strengthened its grip on the MOCVD market over the last few years.

for cutting applications to customers in Europe, North America and Japan, as well as strong welding revenue.

IPG has also enjoyed exceptional growth in the sales of its lasers for welding, driven by demand for AMB (adjustable mode beam) lasers used in EV manufacturing, and the company is excited by its introduction of a handheld welder, known as LightWELD. Commenting on both successes, Scherbakov began by remarking: "Our AMB lasers provide a broad range of beam tuneability that enables superior speed, better weld quality, ability to weld disparate materials, and spatterless welding, which is extremely important in the EV battery manufacturing process."

Scherbakov continued by comparing LightWELD to traditional forms of welding, arguing that the new alternative is easier to use, faster, more precise, welds a wide range of materials better, and incorporates surface-cleaning capability. "These qualities significantly reduce preparation, processing and post-processing times, resulting in lower total operating costs for our customers."

Looking several years ahead, Scherbakov has a great deal of confidence in the company's future, thanks to the substantial investment that automakers will be making in their EV production capability over the next three-to-five years. "We are supplying laser solutions for battery welding and thin foil cutting applications, cleaning and hairpin welding in an electric battery and motor assembly, as well as some body-in-white applications."

However, for the next year or so, IPG's forecasts involve some uncertainty, partly due to limited visibility. Also concerning investors is short-term revenue growth that is unlikely to impress. While the long-term forecast is for double-digit growth, the company stated in its quarter-four earning call that sales are expected to increase by just 3-6 percent for this fiscal year – and it has since withdrawn that guidance, due to impact from the war in Ukraine.

While this conflict is impacting many companies through increased utility prices, IPG has even more significant issues to deal with. It has 2,000 employees in Russia, working in production and R&D. These facilities supply components to IPG sites in Germany and the US, as well as producing finished products for China and the US. Last year, shipments from IPG's Russian operations supplied approximately $100 million of finished product for the Chinese market.

One issue facing IPG is the increase in lead times and shipping costs for components and lasers to and from its Russian operations. To mitigate this, the company has built up several months of critical inventory in Russia to support sales. When commenting on this situation at the start of March, IPG stated that its Russian facility could ship optical and other components to its affiliates from Russia. However, as sanctions evolve, plans cannot be made with much confidence.

While many other companies in the compound semiconductor sector are not affected as directly by the war in Ukraine as IPG, they will be impacted by higher energy prices and reduced consumer confidence. However, as Europe shifts to wean itself off of Russian gas and oil, this could work out well for our industry in the long term, accelerating the shift to renewable sources and EVs. This will result in surging sales of GaN and SiC power electronics. So there's hope – but having said that, it's still hard to know what the next few years hold for our industry and for humanity as a whole.

Delagates at this year's CS Mantech were not far from the historic Bixby Creek Bridge, found along the world famous Highway 1 in Monterey County, California.

Strengthening the credentials of the III-V transistor

Fast transistors are poised for far greater deployment, thanks to efforts by fabs and those working on internal production lines

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

IF YOU ARE A VETERAN of this industry, you will remember the days of GaAsMantech. At that conference chipmakers would champion breakthroughs in the design and production of III-V transistors serving in a variety of applications – primarily mobile communication.

It's now been more than a decade since that conference series, always held in North America, changed its name CSMantech to reflect a greater diversity of devices. Over the intervening years the GaN HEMT has come on in leaps and bounds to dominate an agenda that also highlights advances in SiC power electronics and optoelectronic devices. However, the conference still provides a platform for reporting significant breakthroughs associated with the manufacture of III-V transistors.

At this year's conference held in Monterey delegates detailed: the introduction of foundry services for making sub-terahertz transistors from 150 mm wafers; efforts at improving the manufacturing readiness of InP HEMTs that feature an InAs channel and can operate at hundreds of gigahertz; an overgrowth-and-plasma-treatment process promising to speed a novel HBT; and a hybrid etching process to boost the yield and breakdown voltage of a GaAsSb/InP HBT. Taken together, these advances should ultimately drive the deployment of better III-V transistors in 5G and 6G networks, in space, and in test and measurement equipment.

Faster foundries

For the manufacture of RF devices for mobile communication, providers of epiwafers and foundries have been playing a key role for many years. These players are currently developing and launching products that will allow design engineers to work with far higher frequency transistors.

One of the leading III-V foundries that is working on a portfolio of sub-terahertz transistors is WIN Semiconductors of Taiwan. According to Cheng-Kuo Lin, who spoke on behalf of the company at CS Mantech, new device designs are needed to reach this frequency domain. That's because the company's established technologies – the GaAs pHEMTs and InGaP HBTs that have been widely used in MMICs for power amplifiers, low-noise amplifiers and switches – are unable to provide sufficient power gain in amplifiers at sub-terahertz frequencies.

To provide customers with products operating at those very high frequencies, engineers at WIN have been developing three different technologies for production on their 150 mm line: InP HBTs, and metamorphic and pseudomorphic HEMTs with a gate length of just 100 nm.

Lin told *Compound Semiconductor* that the strengths of the mHEMT are its ultra-low noise and its high gain in the D-band, which spans 110 GHz to 170 GHz. In comparison, the pseudomorphic HEMT majors on the maturity of its epitaxial process and the device's higher operating voltage. "The limitation could be the operating frequency," remarked Lin, who argued that for frequencies above 170 GHz, the InP HBT is a stronger candidate that is capable of integrating more RF function blocks.

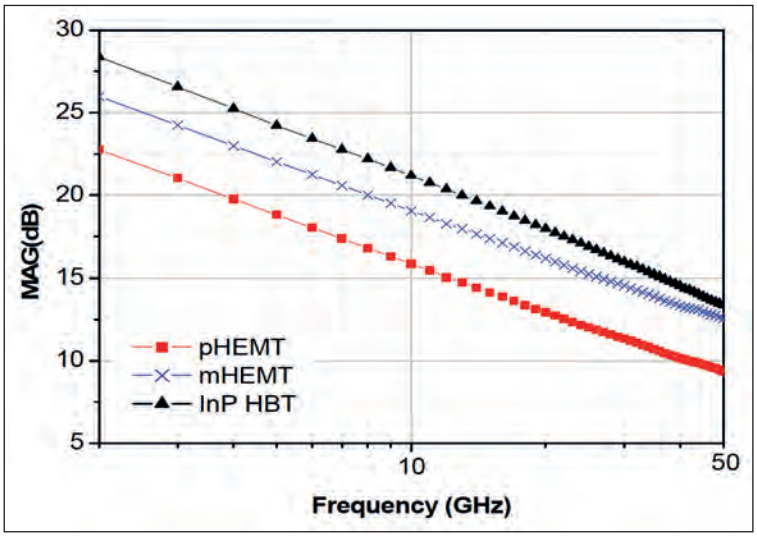
The 150 mm epiwafers for WIN's pHEMTs are grown by MOCVD on GaAs substrates and feature an indium-rich InGaAs channel that provides high mobility, ensuring excellent carrier transport. GaAs substrates also provide the foundation for the mHEMTs, grown by MBE. These epiwafers, which also have an InGaAs channel, use a metamorphic buffer to trap dislocations and adjust the lattice constant from that associated with GaAs to that for InP.

Compared with another device, the InP HEMT, the metamorphic HEMT delivers comparable performance for significantly less expense. As well as a higher price for the substrate, the epi for the InP HEMT is more expensive, due to a longer growth time. Another factor in favour of the mHEMT is that its epiwafers are more widely available than those for InP HEMTs, due to the difference in the substrate.

The 100 nm gate lengths of the mHEMTs and pHEMTs, which hold the key to reaching higher frequencies, are formed by electron-beam lithography. Production of the pHEMT also involves: the addition of source and drain ohmic contacts, device isolation by ion implantation, SiN passivation, and the formation of a 2 μm air bridge. Fabrication of the mHEMT employs similar steps, but isolation is carried out by wet etching.

To assess device uniformity, WIN's engineers produce maps of wafer uniformity. These plots reveal a threshold voltage variation, in terms of one-σ, of just 17 mW and 16 mV for pHEMTs and mHEMTs that populate these 150 mm wafers. The low values, claimed to be an industry milestone, confirm that the gate is able to control the channel without any concern over leakage. The implication for customers is that they can expect to get a high product yield from these wafers.

Measurements of the maximum available gain put the InP HBT out in front, and the mHEMT ahead of the pHEMT (see Figure 1). This plot suggests that the maximum oscillation frequency (f_{max}) is 353 GHz for the HBT, 321 GHz for the mHEMT, and 247 GHz for the pHEMT. The pHEMT produces the highest power density of 724 mW/mm, compared with 248 mW/mm for the mHEMT and 2.59 mW/μm² for the HBT.



➤ Figure 1. WIN Semiconductors has developed three new foundry processes for producing III-V transistors for millimetre-wave applications on a 150 mm line. The InP HBT process provides the highest gain, followed by the 100 nm mHEMT and pHEMT processes.

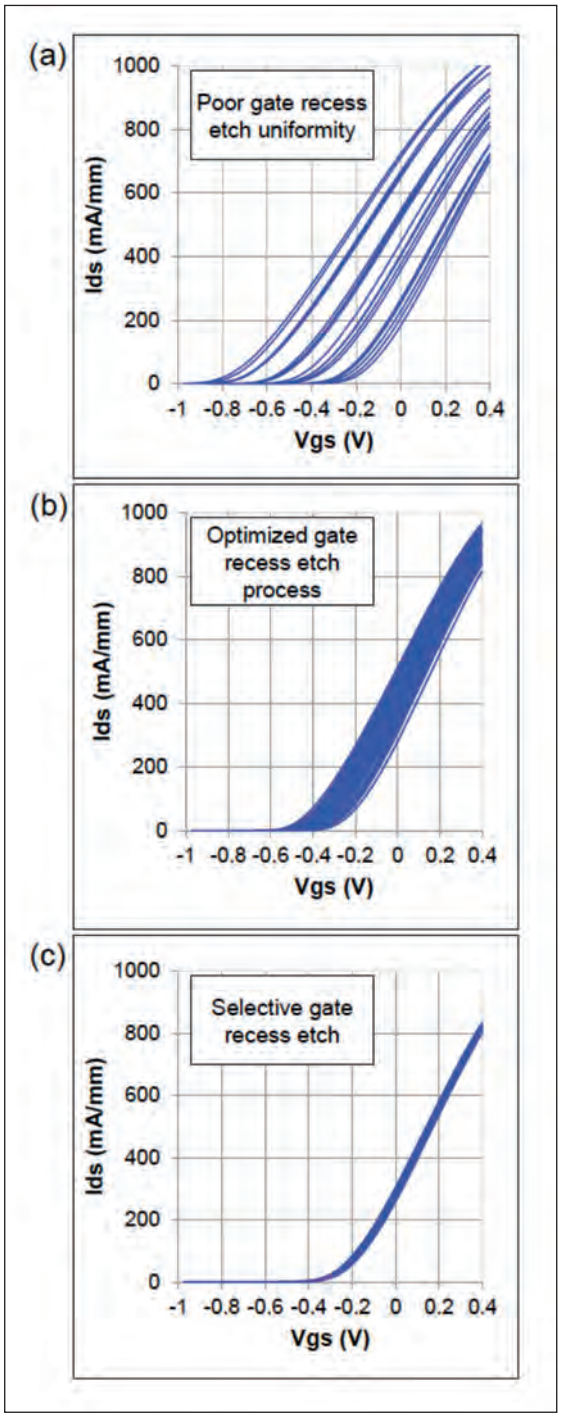
All three classes of transistor have undergone high-temperature operating lifetime tests. For the mHEMT, testing involved 500 hours of operation at an ambient temperature of 165 °C and a drain voltage of 2 V. Under these conditions the threshold voltage, the transconductance, the maximum drain current and the gate leakage shifted by less than 20 percent, leading engineers to conclude that the mHEMT passed this test. Also passing its test is the pHEMT, while the HBT is still under investigation.

Thanks to the positive results with the pHEMT, this device is now available to customers, which can use WIN's process design kit (PDK) to create their MMICs. For the mHEMT the process is finalised and the PDK ready, but it will be the end of this year before an official release. However, customers can already participate in "early engagement", according to Lin.

Engineers will continue to improve the HBT before it's released. "We're going to get higher performance by optimising the emitter size from 0.8 micron to 0.5 micron," remarked Lin, who revealed that our team's plans extend to adding a copper-pillar to the HBT wafer to minimise deleterious effects associated with wire bonding.

Refining the process

At Northrup Grumman much effort is being devoted to improving production processes for transistors that feature an InAs composite channel and operate at frequencies approaching 1 THz. Two decades



➤ Figure 2. To improve the manufacturing readiness of its HEMTs that feature an InAs composite channel, engineers at Northrup Grumman have been developing a new process for the gate recess etch. The original process produces a poor gate recess etch uniformity (a). This is improved with an optimised gate recess etch (b), while an even smaller variation is yielded with a selective gate recess etch.

of development, funded by agencies associated with the military, has helped drive this technology's development and take it to a manufacturing readiness level of 3 to 4 – this means that devices can be produced in a lab. Now work is underway, outlined at CS Mantech by Northrop Grumman's Feifei Lian, to improve the maturity of this device's production process. The aim is to close the gap with the company's InP HEMT technology, which is capable of producing devices in volume on an internal 100 mm line.

Lying at the heart of this emerging generation of devices from Northrup Grumman is a high-electron-mobility InAs channel. Responsible for the transistor's high frequency and low power prowess, this channel is clad by a pair of lattice-matched InGaAs layers. Additional features of this transistor are its low-resistance ohmic contacts, realised by the inclusion of a Schottky barrier layer and a heavily doped cap in the epitaxial structure, and T-gates with dimensions from 25 nm to 70 nm, defined by electron-beam lithography.

To advance the manufacturing readiness of these devices, Lian and co-workers have had to transfer their MBE growth process from a single-wafer tool, used to produce a 75 mm epiwafer, to a multi-wafer MBE reactor that accommodates multiple 100 mm wafers. Encouragingly, the average value for the electron mobility in the channel is higher for wafers produced with the multi-wafer tool. Initially, growth on this higher-throughout reactor led to a larger variation in the ohmic contact resistance for the HEMTs, but this issue has been resolved by modifying the doped cap design.

Lian and colleagues have also taken a close look at the gate formation process, which must be carefully tuned to consistently realise uniform electrical characteristics and a high gate yield. The gate recess is key, as it influences many device characteristics, including transconductance, the pinch-off voltage and breakdown. If there is poor control over the gate recess depth, this can result in enhancement-mode devices with extremely thin Schottky barriers, a very high gate leakage, poor noise and compromised reliability, due to metal diffusion.

To try and improve the gate formation process, engineers at Northrop Grumman have investigated two potential refinements to their gate formation process. One involves using an optimised wet etch processes and semiconductor surface treatments to ensure a uniform etch initiation and progression; and the other introduces an etch stop process, with the wet etch stopping on a layer embedded in the barrier. The latter leads to excellent uniformity, but often at the expense of a reduction in device performance (see Figure 2). To increase the process margin, etch-stop processes can employ a significant over-etch, but this widens the recess region, increases access resistance and ultimately diminishes device gain.

Lifetime testing on HEMTs produced with the selective gate recess etch show a projected mean-time-to-failure of 1.9×10^7 hours at a junction temperature of 125 °C. According to the team, this indicates that these devices have sufficient reliability to serve in space missions that are categorized as class A, which means that failure would have extreme consequences to either public safety or to high-priority national science objectives.

Advancing instrumentation

For those that have been increasing the high-

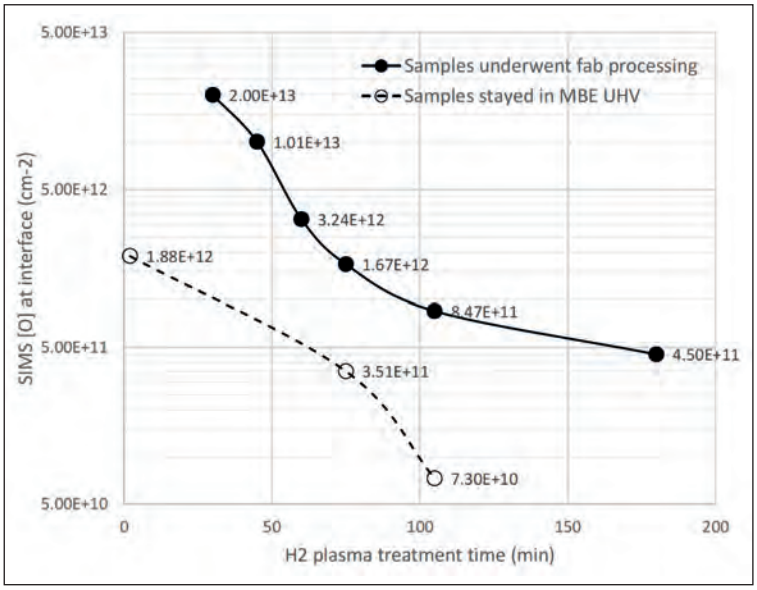
frequency capability of SiGe BiCMOS technology, much progress has come from the introduction of an epitaxial regrowth step for the SiGe base. This refinement has increased f_{max}, along with the current gain cut-off frequency (f_T) and the ring oscillator delay. Today's state-of-the-art BiCMOS processes employ either a selective or a non-selective re-growth of a highly doped base – this trims base resistance and improves high-speed performance, allowing designers to use faster transistors or enjoy a wider design margin.

At Keysight Laboratories, engineers are investigating whether there is a similar opportunity for their GaAsInP/InP double HBTs, which are widely used in the company's high-speed test and measurement instruments. Speaking on behalf of this vertically integrated instrumentation maker at CS Mantech, Barry Wu described a low-temperature GaAsSb extrinisic base regrowth process involving an *in-situ* hydrogen plasma treatment and MBE non-selective regrowth of the base. This promises to build on Keysight's double HBT technology platform that already has tremendous high-speed capability. In its latest guise, this is capable of producing a 0.5 µm device with an f_T of 280 GHz and an f_{max} of 580 GHz.

The company's latest investigations have involved a Veeco Gen200 multi-wafer MBE system and a Veeco UNI-Bulb hydrogen remote-plasma source with an RF generator. These tools are connected, allowing wafer transfer under ultra-high vacuum.

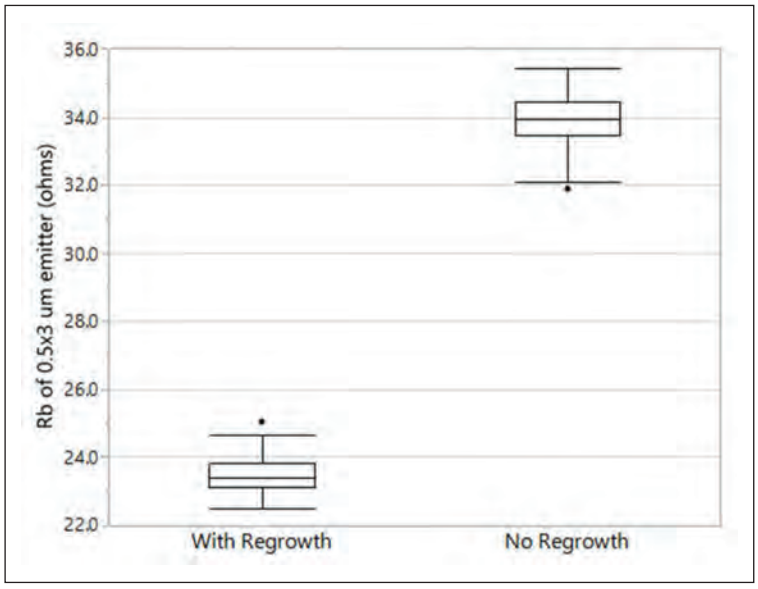
Prior to plasma treatment and regrowth, epiwafers with a 250 nm-thick $GaAs_{0.51}Sb_{0.49}$ layer underwent typical III-V semiconductor fabrication processes, such as ashing and wet de-oxidation. Following plasma treatment, the wafers were loaded into the MBE system, used for the re-growth of a 50 nm-thick layer of GaAsSb doped to about 5×10^{20} cm^{-3}.

Engineers at Keysight considered the impact of variation in treatment time, and also the influence of fab processing. According to secondary-ion mass spectrometry, plasma treatment for 105 minutes decreased the oxygen profile by a factor of around 50 (see Figure 3). This technique also revealed that the oxygen concentration is significantly lower at the regrowth interface than the epilayer-substrate interface; and that the carbon doing level in the regrown GaAsSb is more than 1×10^{21} cm^{-3}, which is sufficient for an extrinsic base.



➤ Figure 3. Engineers at Keysight Technologies have started to investigate the benefits of hydrogen plasma treatment to reduce the base resistance in their double HBTs. Slashing the oxygen content trims the base resistance by 30 percent, an encouraging sign for speeding the transistor.

➤ Keysight produces double HBTs for use in its high-speed instrumentation.



➤ Figure 4. The extrinsic base regrowth undertaken at Keysight Technologies is able to cut base resistance by 30 percent while not adversely impacting uniformity.

Measurements on Keysight's wafers show that regrowth of an extrinsic base layer led to a 30 percent fall in the base resistance. Encouragingly, this reduction did not impact uniformity, with a tight intra-wafer uniformity retained (see Figure 4).

According to Wu, a lower base resistance has several benefits, including holding the key to improving the IC ring oscillator frequency, which enables a faster IC speed. It also helps to trim the noise figure and improve bias stability.

Hybrid etching

Another team that's breaking new ground for the double HBT is Milton Feng's group from the University of Illinois at Urbana-Champaign (UIUC). Commenting on their record-breaking results, unveiled at CS Mantech, team member Yulin He told *Compound Semiconductor*: "Compared to previously reported competing devices, the InP DHBTs of this work – with a thicker collector and lateral scaling, well controlled by hybrid etching – achieve a higher breakdown voltage at the same f_T." These transistors, formed with a combination of dry and wet etching, provide a breakdown voltage in excess of 11 V, an f_T of 135 GHz and an f_{max} of 245 GHz (see Figure 5). These figures indicate that this form of HBT is a very promising candidate for millimetre-wave 5G: the value for f_{max} is around four times that for the 5G millimetre-wave bands found at 26 GHz, 28 GHz and 39 GHz; and the high breakdown voltage makes the device suitable for operating in the 3-5 V range, while accommodating any voltage swings.

Transistors formed with a combination of dry and wet etching provide a breakdown voltage in excess of 11 V, an f_T of 135 GHz and an f_{max} of 245 GHz. These figures indicate that this form of HBT is a very promising candidate for millimetre-wave 5G.

Additional opportunities for these double HBTs are in amplifiers operating at more than 70 GHz, and in high-speed testing instruments, such as those made by Keysight.

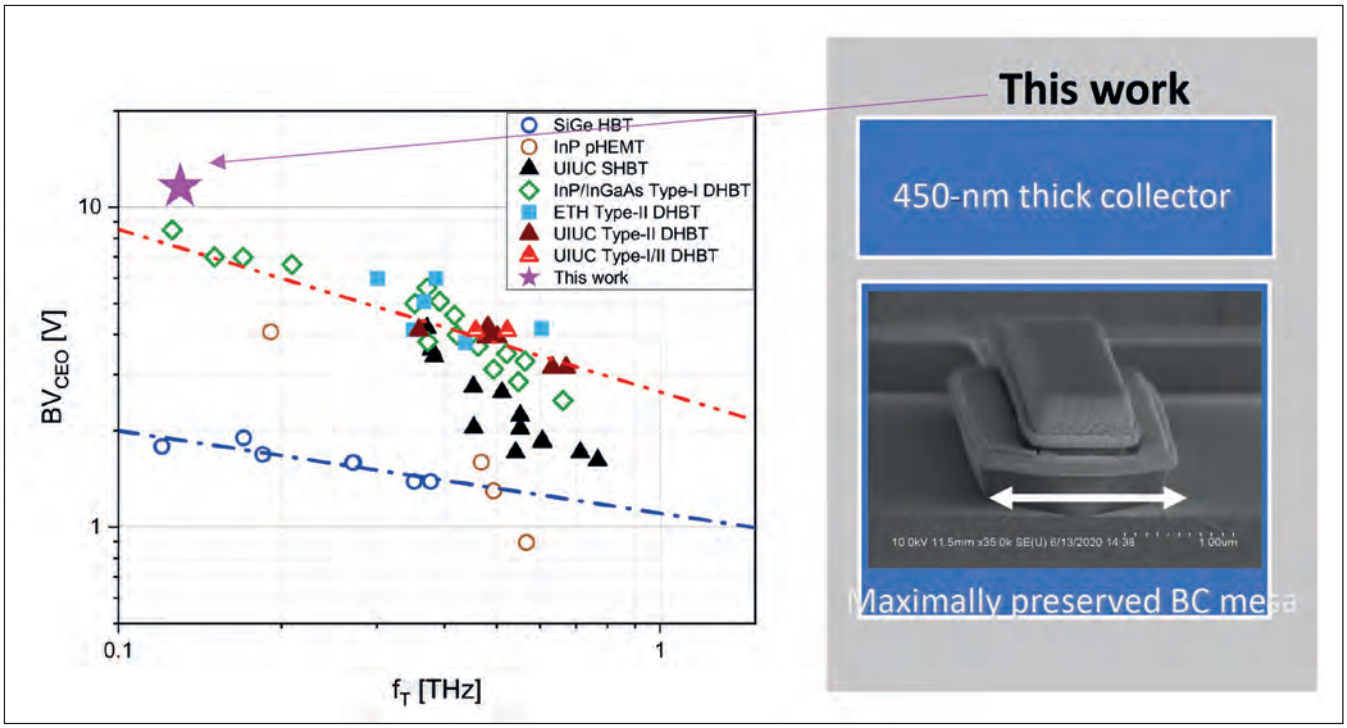
The team from UIUC demonstrated the capability of their hybrid etching process by producing double HBTs from 4-inch epiwafers grown by MBE on semi-insulating InP substrates. He and co-workers compared a variety of techniques for processing epitaxial stacks, which featured: a 15 nm-thick strained AlInP layer for launching hot electrons; a 40 nm-thick, carbon-doped and compositionally graded GaAsSb base layer, which promotes electron flow by a built-in field; and a 450 nm-thick InP layer that ensures a high breakdown voltage and enhances the power handling capability of the device.

Success at UIUC has come from combining wet etching with inductively coupled plasma reactive-ion etching (IPC RIE). This pair of etching processes is employed to form the mesa structures and, crucially, to isolate the active region and the base metal post. After the team fabricated their active device, they planarized their sample, passivated it with bencozyclobutane, employed an etch-back process to expose the post metal, and added the coplanar-waveguide with a metallization step.

When forming the emitter-base mesa, it is standard practice to use wet-etching, with the emitter metal acting as the etching mask. During this step, it is critical to realise a lateral undercut of the emitter-base mesa, and this ensures a low base epitaxial resistance and prevents shorting with the base contact.

For this etching, sulphuric acid is used to treat the emitter cap, while hydrochloric acid treats the emitter. The team have found that they can enhance the controllability of this process by cooling the hydrochloric acid to 0 °C – this slows the etching rate, enabling fine-tuning of the wet etch duration.

The base-collector mesa is traditionally formed by wet etching. This is not ideal, as it produces a huge undercut and a low yield. These weaknesses have motivated He and colleagues to pursue their hybrid etching approach. They are championing a combination of methane and hydrogen for



dry etching, rather than a chlorine gas, because this ensures smother surfaces and more vertical sidewalls.

Using an Oxford Plasmalab 100 ICP TIE tool for this step, the team has realised a yield of over 90 percent. That's twice that for the wet-etching approach, which had been preferred for its simplicity. According to He, the merits of the hybrid etching approach extend beyond greater controllability, especially when forming the base-collector mesa and realising isolation, to an increase in the number of degrees of freedom associated with the process.

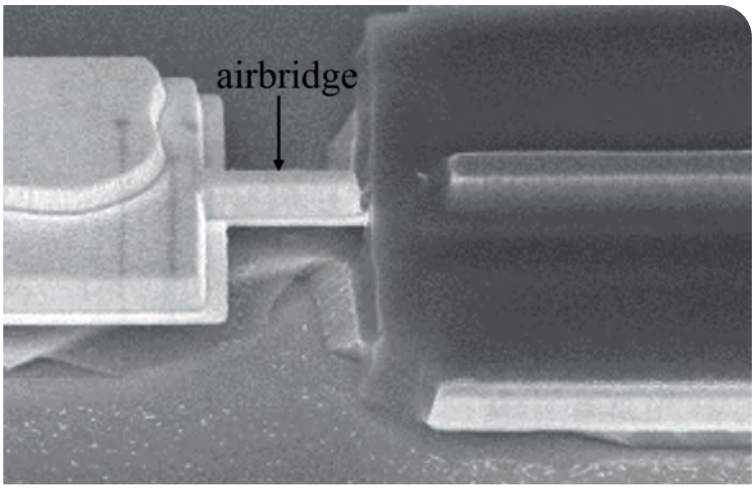
To produce double HBTs, there is also the need to isolate the active device from the base post, in order to trim parasitics. If wet etching were used to clear all the conductive layers below the airbridge, this would lead to non-uniformity, with the exposed metal catalysing faster acid etching. There is the threat of metal collapse, due to an excessive metal undercut. A better approach, pursued by the team from UIUC, is to begin by using a methane-based plasma to undertake a well-controlled dry etch, before turning to a systematic wet-etch to ensure isolation with improved uniformity. Scanning electron microscopy of double HBTs produced by this approach highlights the vertical etch to the substrate and the formation of the airbridge at the interconnect with a lateral undercut (see Figure 6).

The engineers are planning to optimise the performance of their devices. Efforts will include the introduction of an emitter ledge to improve the performance of the millimetre-wave power amplifier.

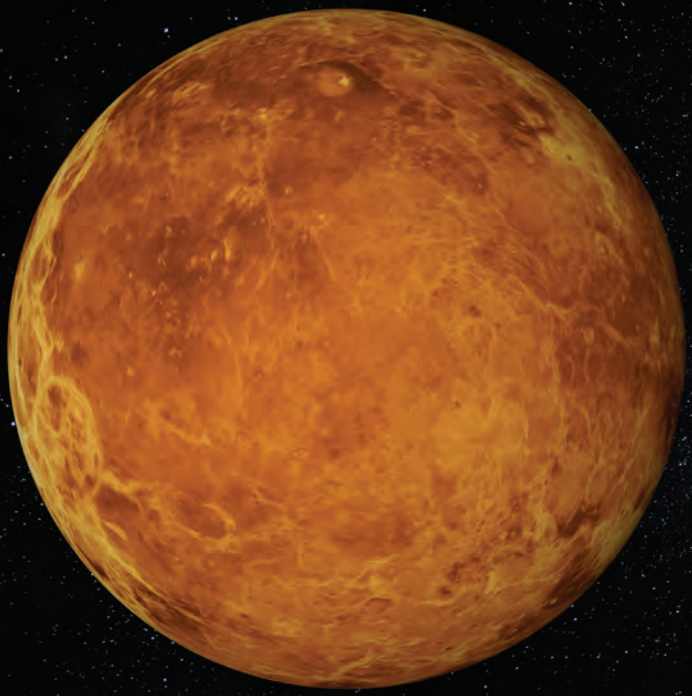
"This can reduce the emitter peripheral recombination current, thereby improving the RF current gain and increasing the operating frequencies," said He, who added that they may also look at following in the footsteps of Keysight by adding an extrinsic base regrowth step to their process.

As demonstrated at CSMantech, those at UIUC, Keysight, WIN and Northrup Grumman are helping to drive III-V transistors to a new level of performance. That's clearly important, given the role that these devices will have to play in future mobile networks, as well as other applications.

➤ Figure 5. Milton Feng's team at the University of Illinois at Urbana-Champaign have realised a a higher breakdown voltage at the same f_T by turning to a thicker collector and lateral scaling, well controlled by hybrid etching.



➤ Figure 6. Engineers at the University of Illinois at Urbana-Champaign produce double HBTs with improved uniformity and isolation by combining a methane-based plasma that ensures a well-controlled dry etch with a systematic wet-etch.



Venturing to Venus

SiC unlocks the door to uncooled electronics that's capable of handling the extreme temperatures found on Venus

BY CARL-MIKAEL ZETTERLING AND MATTIAS EKSTRÖM FROM KTH ROYAL INSTITUTE OF TECHNOLOGY

Is there life beyond Earth? And if so, how intelligent is its form? These are two intriguing questions, piquing the interest of much of humanity. In a search for answers, we have built ever more powerful telescopes that probe into the deeper reaches of the universe, and embarked on missions to nearby planets, to examine what they are made of.

Why Venus?

In the last few years there has been much interest in Venus. Back in 2020, scientists uncovered possible signs of life in its cloud layers, evidenced by traces of phosphine that could not be explained in other ways. This has spurred the planning of a number of missions to this second planet from the Sun. NASA has two tentative trips scheduled for 2028-2030: one is entitled DAVINCI+, short for Deep Atmosphere Venus Investigation of Noble gases, Chemistry, and Imaging; and the other is VERITAS, and acronym for Venus Emissivity, Radio Science, InSAR, Topography, and Spectroscopy. The European Space Agency also has Venus on its agenda, through a project called EnVision, which will investigate the atmosphere, surface and sub-surface of this planet; and there is a private mission planned by Rocket Lab, slated for 2023 – a probe will analyse Venus from an altitude of 30 miles, scrutinising atmospheric layers for phosphine and hunting for proof of previous life.

Missions to Venus are certainly not new. There were many between 1960 and 1981, involving fly-by, orbiters, probes and landers. These efforts established that the surface temperature of this planet is as high as 460 °C, which makes exploration extremely challenging. Between 1976 and 1981 the

Soviet Union put a number of Venera landers on the surface, equipped with heat shielding for the silicon electronics. But even with this assistance, the electronics only survived for up to two hours (although that mission still provided colour images of the surface).

The benefits of developing electronics that is capable of handling the extreme temperatures found on Venus would actually accomplish far more than simply determining whether Venus ever supported life. Success on this front would also help us to understand far more about the nature of our own planet. Why? Well, Venus is similar in size to Earth, and it has an atmosphere containing 96 percent CO_2. Consequently, understanding the climate of Venus could help us to understand what is happening at home, by providing a second reference point that would improve our computer models. Armed with more rigorous, reliable models, we would be in a better position to understand our atmosphere's composition and temperature variations.

Efforts at gaining a better insight into Venus' climate must consider whether this planet still has active volcanoes. This is an outstanding question with important implications, as active volcanoes offer one explanation for the planet's sulphuric acid content. One way to detect volcanic activity is to use seismometers, which would require another lander mission to Venus. However, if this is to be of value, the electronics in the seismometer would need to survive 2 months or 2 years, rather than just a couple of hours.

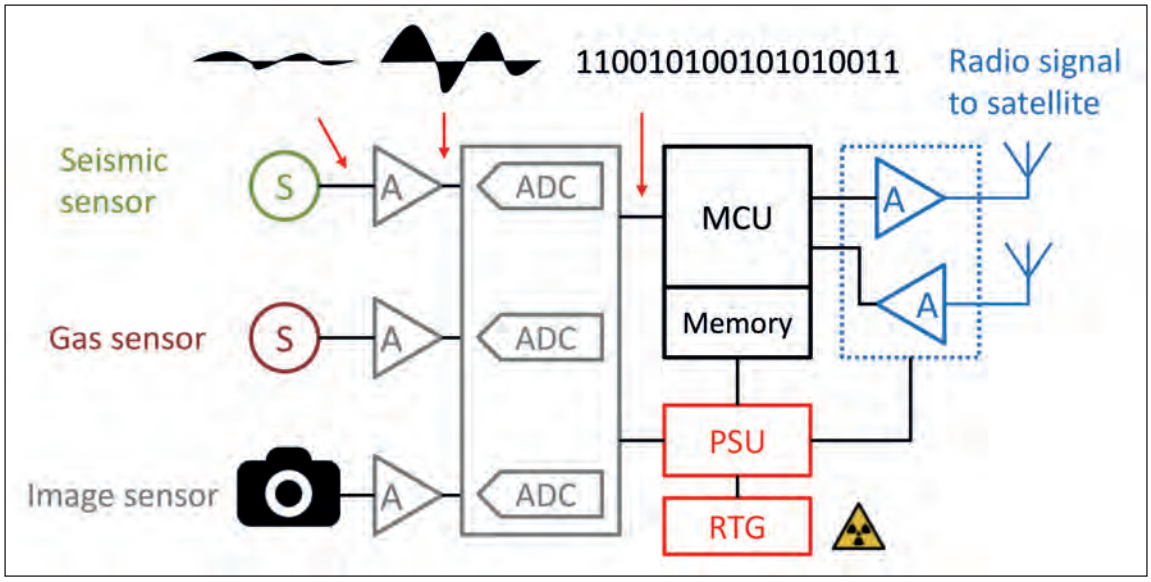
Why is there a temperature limit?

All classes of semiconductor have an intrinsic temperature limit. Heating this material generates carriers, in the form of electron-hole pairs. For devices at room temperature, these carriers are hardly noticeable, except in sensitive systems where there is added noise – it is for this reason that radio telescope receivers are cooled. At elevated temperatures leakage currents escalate, causing some sensors to lose their sensitivity, power consumption to increase, and most transistors to operate less optimally. At even higher temperatures far greater issues arise, with semiconductor devices no longer able to block the applied voltage and catastrophic failure occurring. To try and prevent this from happening, in many high-power electric circuits heat sinks and fans extract the heat from the devices.

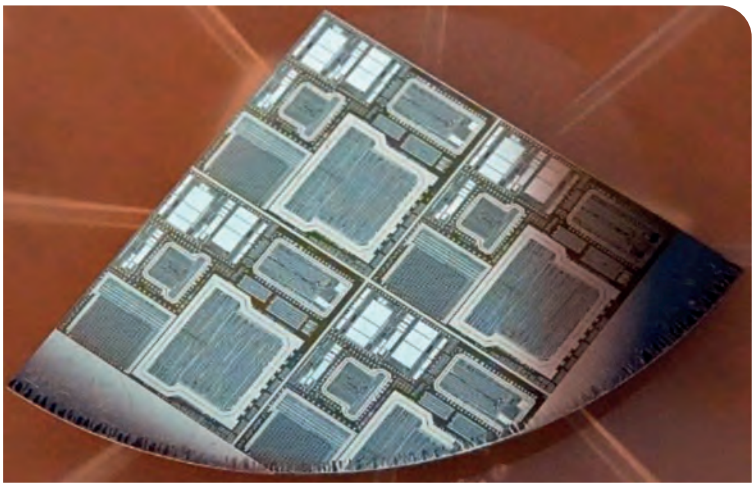
Why SiC?

Governing the operating temperature of every semiconductor device is its bandgap. The thermally generated carriers – referred to as the intrinsic concentration in physics text books – depend on the energy bandgap in an exponential relation, causing the increase of conductivity to rise exponentially with temperature.

Due to this relationship between the bandgap, the temperature and the conductivity, SiC is far better than silicon at handling the heat. SiC is blessed with a bandgap of 3.2 eV, compared with just 1.12 eV for silicon. Thanks to a tripling of the bandgap, devices made from SiC can operate at up to at least 800 °C, compared with around just 200 °C for silicon. What's



➤ A block diagram of the proposed Venus Lander. This should be seen as an example of the electronic building blocks needed for a typical system. Different sensors are used, and amplifiers are needed in many cases to increase the signal level, prior to conversion to a digital signal in an Analogue-to-Digital Converter (ADC). The microcontroller (MCU) with memory stores the data until it can be sent to a satellite for relaying to Earth. The radio transceiver activates when the satellite is in range, with the microcontroller sending stored data. The power supply unit (PSU) converts energy for different parts, and turns off units when not used. One possible high-temperature power supply would be a Radioisotope Thermal Generator (RTG).



A sample SiC chip with all the developed circuitry. The rather massive leads encircling the individual circuits are power conductors. While BJT circuits take more current than those based on MOSFETs, chip heating is not a problem on Venus. Photo: Jörgen Städje.

more, the wider bandgap reduces sensitivity to radiation damage.

Right now, sales of SiC devices are ramping fast, with SiC MOSFET switches and power Schottky diodes winning substantial sales, thanks to their capability to operate at high voltages with low on-state and switching losses. Compared with incumbent silicon devices, those made from SiC benefit from a critical field for breakdown that is almost ten times higher, allowing the device's blocking region to be ten times thinner and have almost a hundred times higher doping. The upshot of these attributes is that, for the same blocking voltage, SiC devices have an on-resistance that is 200 to 400 times lower than their silicon siblings. Many manufacturers are offering SiC diodes and transistors rated between 600 V and 3300 V, which are being deployed in power supplies and electric vehicles.

Our solution

Our team at KTH Royal Institute of Technology, Sweden, has spent several years developing SiC electronics that is capable of handling the high temperatures found on the surface of Venus. We have taken a slightly different approach from what you might expect, shying away from using MOSFETs, the most common form of transistor deployed in today's ICs. That's because MOSFETs are impeded by a relatively high level of vulnerability to the gate oxide, and a threshold voltage that varies by -1 V for an increase of 100 °C. A better option is the bipolar junction transistor (BJT), which offers a performance that changes far less with temperature – for instance, the built-in voltage of the *p-n* junctions shifts by just -0.2 V for an increase of 100 °C. Using the BJT, we are able to design all the circuits we need, drawing on advice provided in text books from the 1960s.

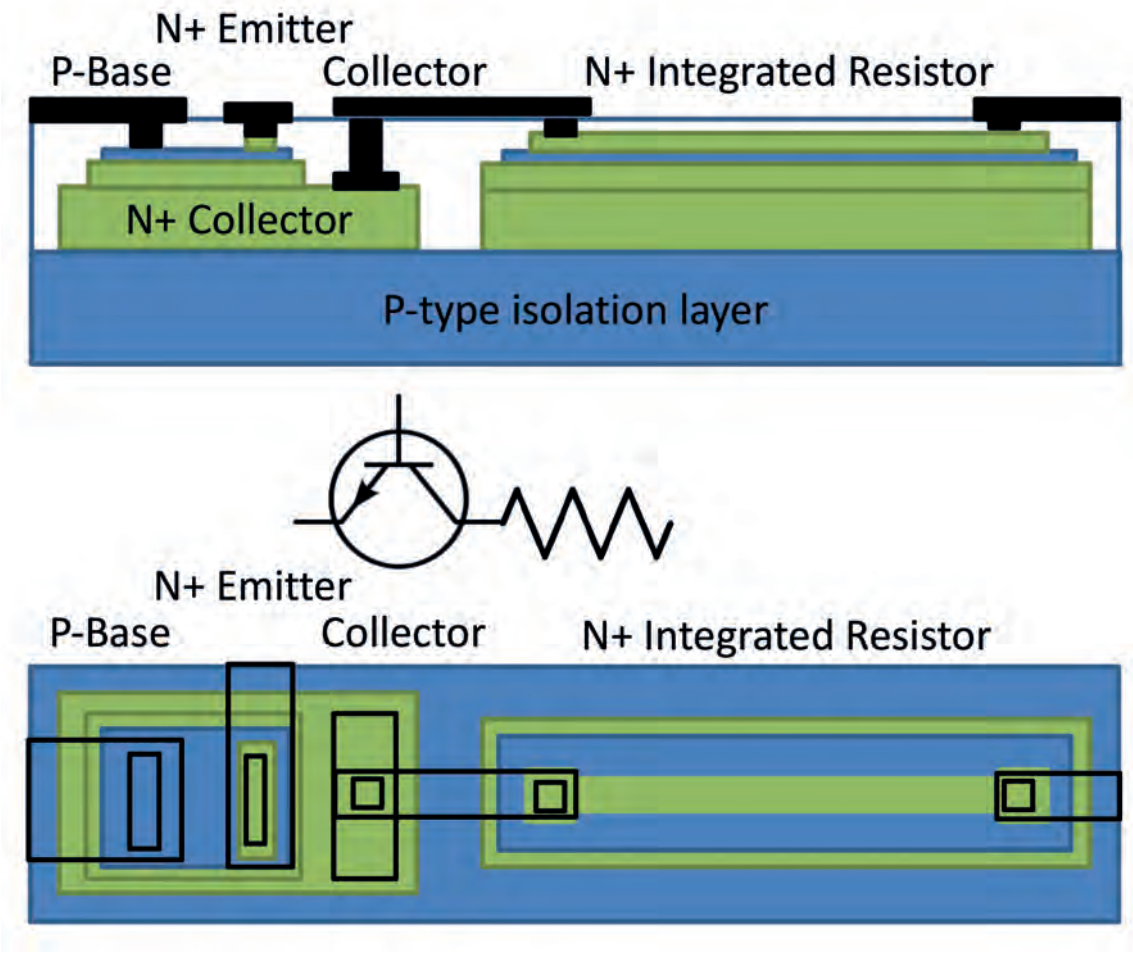
ICs also require resistors and capacitors, which can be made using the process steps employed for making the transistors. We avoid ion implantation, because this introduces electron-hole recombination centres. Instead, we define all our doped regions with the combination of epitaxial growth of SiC layers and dry etching, which defines the geometry of the features.

During our campaign, we have developed a self-aligned method to form contacts. We use SiO_2 to isolate the components and the two metal layers from one another. To produce a flat surface, we have turned to chemical mechanical polishing, due to the large variation in topography after dry etching.

A minimum embedded system for a Venus lander typically has: sensors to measure temperature, seismic activity and UV light; amplifiers to increase the signal level; analogue-to-digital converters, to convert to digital values that can be stored; a microcontroller (MCU) with memory (SRAM) to collect data and communicate; a radio transceiver to communicate with an orbiting satellite; and a power supply unit.

During our five-year project Working on Venus, which started in 2015, we have built and demonstrated circuits separately, with PhD students taking responsibility for separate parts. Crucial overarching requirements during this effort were that: the process design would include all components; the process design kit would be used to handle the simulation models of the transistors for temperatures up to 500 °C; and the construction of the larger circuits would draw on standard design-

ICs also require resistors and capacitors, which can be made using the process steps employed for making the transistors. We avoid ion implantation, because this introduces electron-hole recombination centres. Instead, we define all our doped regions with the combination of epitaxial growth of SiC layers and dry etching, which defines the geometry of the features



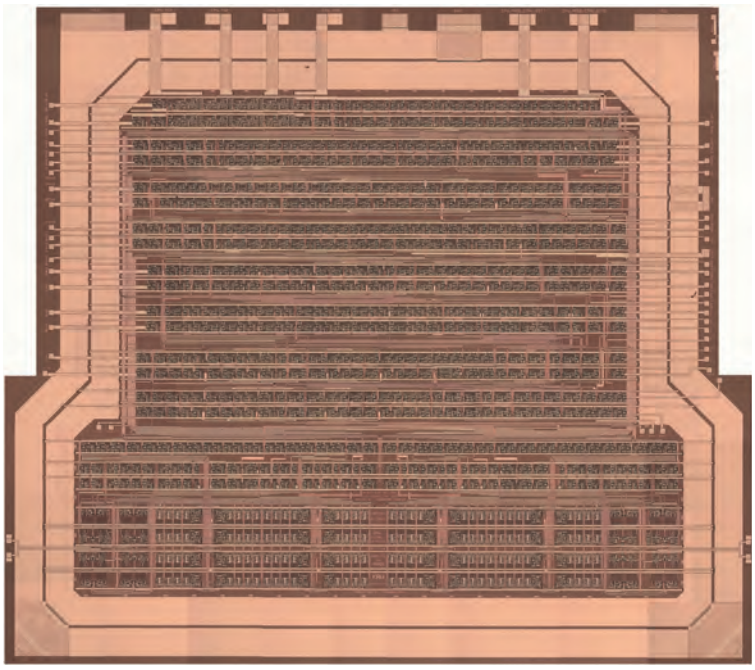
➤ Cross-section and top view of the integrated circuit elements used: the transistor, the resistor and the capacitor. These components are isolated from each other using a *p-n* junction beneath the collector region, and SiO_2 in the trenches etched between the components. Around a dozen mask layers are required for the full process with two metal interconnect layers.

rule-checking and layout, while comparing with schematic checkers.

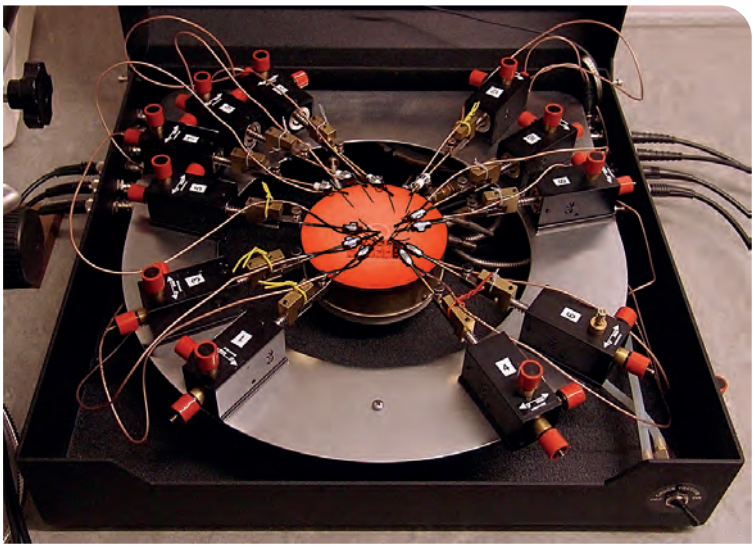
Did we succeed?

Our efforts have paid substantial dividends, enabling us to demonstrate separately all the parts in the block diagram up to 500 °C. This success has provided a foundation for making several amplifiers, since different sensors need different impedance matching. We have also made Flash and successive-approximation ADCs. Our efforts have not had to include developing either gas- or temperature sensors, as both were available prior to our project. We have confirmed that suitable seismic sensors can be made using silicon, if the readout electronics is made in SiC. In addition, we have demonstrated radio circuits. This is not easy, with characterisation of a 59 MHz signal at 500 °C challenging, as normal coaxial cables and connectors cannot be used. We have also investigated the capability of non-volatile ferroelectric memory, in the form of thin-film vanadium-doped bismuth titanate.

The most challenging construction was the microcontroller with SRAM, due to the large number of transistors involved. As a standard package can't withstand high temperatures, we wanted to measure our circuits on-wafer. Unfortunately, this limits the



➤ A circuit featuring a 4-bit microcontroller with SRAM. It consists of 5900 transistors and 3900 resistors, and draws 1 A at 15 V. There are many silicon microcontrollers that are more efficient, but this one works at 500 °C. A 4-bit external bus allows on-wafer probing on the hot stage. Photo: Shuoben Hou.



➤ Hot stage with needle probes to measure electrical characteristics from room temperature to 600 °C on SiC wafers. Photo: Jörgen Städje.

number of needle-probes we can use in our setup to around a dozen, an issue we address by introducing a 4-bit external bus. The other connections were for the power supply and ground, the two-phase clock, and other control signals.

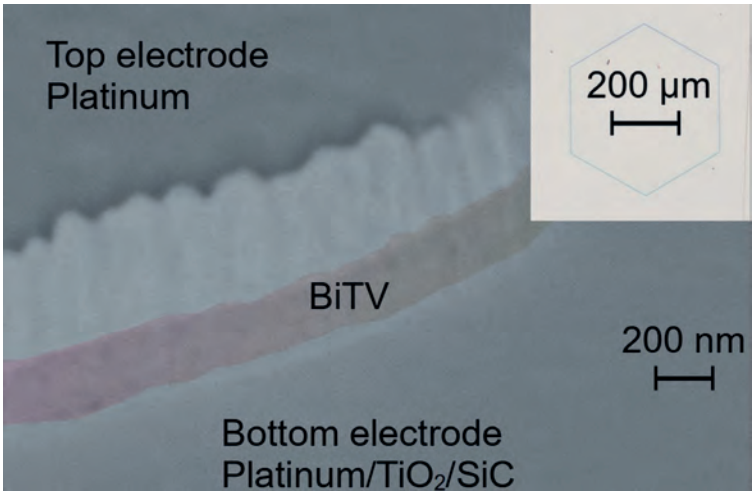
One task we still need to tackle is to improve the temperature stability of the metallisation system. Currently we employ aluminium, which melts at 660 °C. If we could switch to an interconnect system using a refractory metal, such as tungsten, this would enable electronic circuits to operate at even higher temperatures. According to demonstrations at NASA, SiC circuits can operate at 800 °C, even for extended time.

While we have shown that an entire uncooled electronic system operating at very high temperatures can be built using SiC, packaging these devices is an entirely different story. Plastic packages are not an option, as they will not work above 125 °C. Far more promising are ceramic packages, but they are not generally characterized for temperatures above 230 °C. This, though, is a chicken-and-egg problem: there is no drive to design and characterise such packages until there is commercial need for them, while it's not possible to commercialise high-temperature electronics until there are high-temperature packages. For our high-temperature characterization of radio circuits, we use custom-made low temperature co-fired ceramic carriers to mount the SiC transistors.

Fortunately, packaging need not be an insurmountable problem. What's more, even though Venus' atmosphere cannot be kept out of the lander structure, as it's composed of mainly CO_2 it will not attack the circuitry. Note that the surface pressure is of no importance.

We would be delighted to participate in one of the missions to Venus. But that's not our only goal – there are also opportunities for us associated with terrestrial applications. To that end we have also made a 555 timer from SiC. It operates at up to 500 °C, and can be used for timer, delay, pulse generation and oscillator applications. In addition, we have been collaborating with researchers at University of Arkansas in Fayetteville, who have been using our models and process technology to design high-temperature ICs for geothermal and space applications.

Shuoben Hou is acknowledged for manufacturing the SiC wafers, and Muhammad Shakir is acknowledged for making the process design kit and drawing the lithography masks. Jörgen Städje is acknowledged for the photographs and encouraging our work.



➤ Scanning electron microscopy image of a non-volatile ferroelectric capacitor using thin-film BiTV (vanadium-doped bismuth titanate). The inset shows the optical photograph.

FURTHER READING

➤ The full PhD theses of several of the PhD students (Ekström, Hou, Shakir, and Waqar) in the Working on Venus project is available from **www.workingonvenus.se;** previous work from KTH on high temperature SiC circuits is available at **www.hotsic.se**

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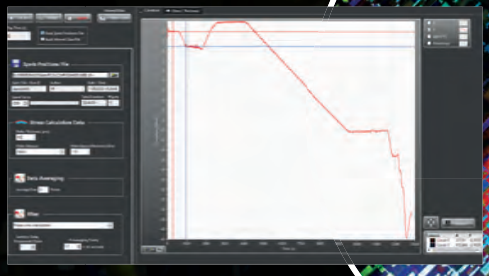

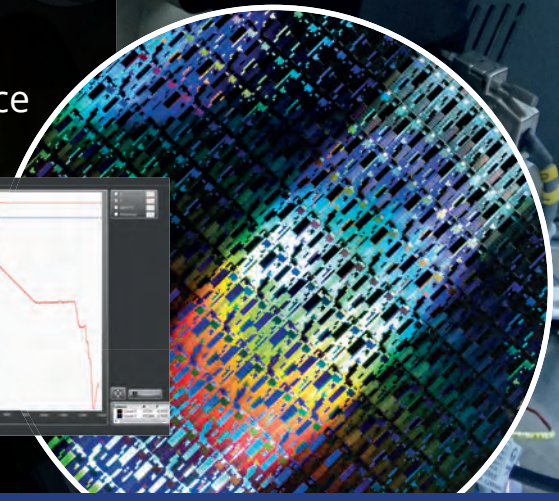

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Experimental investigations underscore the opportunities for GaN HEMTs in 5G and 6G networks

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

MANY OF US DREAM of a more powerful car, a bigger TV, a brand-new smartphone or a better pair of speakers. But it's not failing to own any of them that ruins our day. What irks us is when an item of ours that we really depend upon stops working. When that happens, we are painfully reminded that reliability really matters.

Within the semiconductor industry, reliability is given the high priority that it warrants. Over many years, a great deal of effort has been devoted to analysing and improving the reliability of devices, with much progress reported at the International Reliability Physics Symposium (IRPS).

While presentations at this annual gathering are still dominated by discussions of devices formed from silicon, there is also significant coverage of those made from wider bandgap materials. Last year, we covered presentations at IRPS related to improving the robustness of the SiC MOSFET (see issue IV, pages 32 to 38), and here we report on studies related to the GaN RF HEMT that were presented at this year's meeting, held in late March. While Covid thwarted an in-person gathering in 2021, this year attendees had the choice of either heading to Dallas, TX, or staying at home and taking part on-line.

The handful of presentations on GaN RF HEMTs highlighted its high power, high efficiency and its ability to operate at high frequencies. Thanks to these attributes, this device is already enjoying much success in mobile infrastructure, as well as defence applications. According to French market analyst Yole Développement, global revenue for the GaN HEMT is undergoing double-digit growth, with sales forecast to surpass $2 billion by 2025.

However, this rosy future should not imply that the GaN HEMT is close to perfection. The reality is that there is much room for improvement. One major issue is charge trapping – this may occur within the barrier, at the interface between this layer and the cap, or in either the channel or the buffer. There are also flaws associated with the use of non-native substrates that lead to dislocations, micro-cracks and warpage of the wafer.

At this year's IRPS, engineers reported investigations related to a variety of weaknesses associated with the GaN HEMT, and how this could impact its reliability. Those efforts involved studies of devices that can target millimetre-wave 5G, and a discussion of how GaN HEMTs could play a role in 6G, which will require data transfer at far higher frequencies.

Targeting millimetre-wave 5G

One of the leading producers of GaN HEMTs for RF applications is the US-based chipmaker Wolfspeed. Speaking on behalf of the company at IRPS 2022, Satyaki Ganguly outlined the capability of Wolfspeed's GaN HEMTs for sub-6 GHz 5G communications, as well as detailing very encouraging investigations of variants with a shorter gate length that are suitable for millimetre-wave 5G.

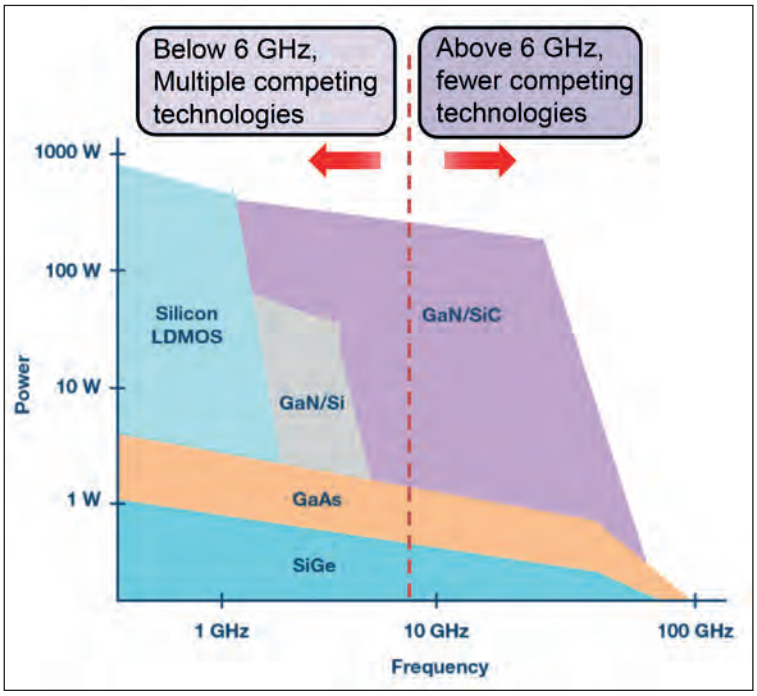
For frequencies of just a few gigahertz, several material technologies can be used to produce transistors with sufficient power, including those based on SiGe, silicon LDMOS, GaAs, and GaN built on both silicon and SiC. "But a higher output impedance and a higher power density definitely makes GaN devices more power efficient than others," argued Ganguly, who claimed that GaN-on-SiC also allows DC power savings when employing massive MIMO and beam-forming technologies.

"Above 6 gigahertz, for millimetre-wave applications, the benefit of GaN is more obvious," added Ganguly, who pointed out that GaN-on-SiC has a far higher output power at millimetre-wave frequencies (see Figure 1).

Ganguly went on to explain that Wolfspeed's RF GaN HEMTs are grown on semi-insulating SiC, and feature an AlN barrier and a source-connected field plate. For frequencies below the millimetre-wave, the company offers devices with gate lengths of 0.4 μm and 0.25 μm, with both designs having variants for operation at 28 V, 40 V and 50 V.

Stretching to the millimetre-wave requires a reduction in gate length. This is accomplished with an i-line stepper, employed for producing HEMTs with a 0.15 μm gate length. These transistors, designed to operate at 28 V, have a very impressive set of attributes, including a breakdown voltage in excess of 84 V, a low leakage, a cut-off frequency (f_T) of more than 30 GHz, high linearity, an output power of more than 3.5 W/mm, and a power-added efficiency at 30 GHz of more than 30 percent. A three-stage MMIC built with this technology can deliver an output power in excess of 5 W, and operate with a power-added efficiency of more than 30 percent.

Ganguly said that qualification tests on these 0.15 μm HEMTs, produced with what is referred to as a 'V5 GaN HEMT process', were a resounding success. No failures were observed during high-temperature reverse-bias tests, DC high-temperature operating life tests, temperature cycles, and RF high-temperature operating-life tests.



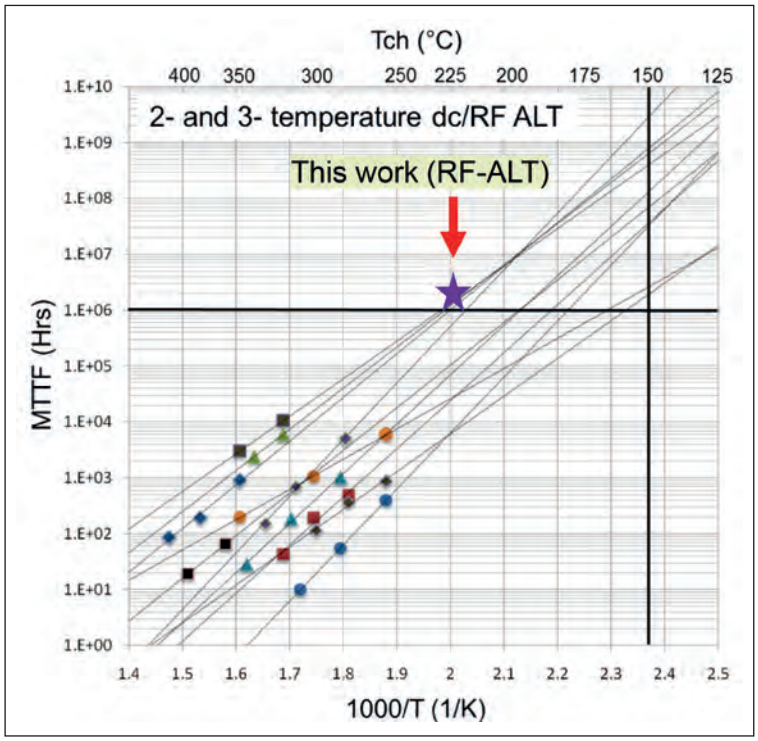
➤ Figure 1. For high powers at a high-frequency, GaN-on-SiC is the outstanding candidate.

The Wolfspeed engineers have also investigated long-term reliability, with RF and DC accelerated-life testing. Defining failure as a drop in output power by more than 1 dB or a catastrophic failure, they determined a mean-time-to-failure of more than a million hours – that's greater than 100 years – at a junction temperature of 225 °C using RF accelerated life testing. According to Ganguly, a plot of the median-time-to-failure as a function of temperature is similar for devices produced with the G28V5 process and the established G50V3 process, suggesting both these technologies have similar failure modes.

For the DC accelerated lifetime testing, the team defined failure as a 15 percent reduction in the maximum drain current. This suggested a median-time-to-failure of more than 10 million hours at a junction temperature of 225 °C. However, this impressive result must be viewed with some caution, warned Ganguly: "Although the DC result might look attractive, it might not be the most important reliability aspect at normal operating conditions. It gives an overly optimistic prediction."

Ganguly benchmarked performance against a range of devices provided in a survey by David Via from ARFL. This exercise suggests that Wolfspeed's HEMTs have an impressive value for median-time-to-failure (see Figure 2). When presenting this data, Ganguly remarked that to the team's knowledge, it is the first to report reliability RF accelerated life testing data for a gate length as short as 0.15 μm.

According to Ganguly, over time the specifications for 5G millimetre-wave HEMTs could shift from a



➤ Figure 2. Benchmarking the reliability of Wolfspeed's GaN HENT against data presented by David Via from AFRL shows that the former has an impressive level of reliability.

junction temperature of 225 °C to 275 °C. Although this would shorten the median-time-to-failure, this might be addressed by introducing the company's sunken source-connected-field plate design, used to target X-band applications. With that technology, Wolfspeed has demonstrated a saturated output power of more than 10 W/mm, a linear gain in excess of 18 dB, a power-added efficiency beyond 60 percent and a median-time-to-failure of more than 100 years at a junction temperature of 275 °C. These promising figures suggest that even better results are on the horizon for millimetre-wave HEMTs.

Perfecting processing

As one would expect, when different processes are used to produce GaN RF HEMTs, this impacts the carrier trapping within the device, as well as its reliability and performance. A partnership between the University of Padova and UMS has undertaken investigations of this nature, with findings presented at the IRPS by PhD candidate Francesca Chiocchetta.

The portfolio of HEMTs produced by Chiocchetta and colleagues include a control device, formed by using plasma-enhanced CVD to passivate the transistor and CF_4 plasma etching to define the gate foot; and variants that employ either low-pressure CVD for passivation, or gate foot etching with a CHF_3 plasma.

Investigations of these GaN-on-SiC HEMTs by the European team included high-temperature reverse-bias testing. This considered both gate leakage currents and what is referred to as a 'belly shape effect' – this phenomenon, offering an insight into the presence of donor traps between SiN and the GaN cap, is associated with the profile of the gate-source current for small positive gate voltages.

For the device produced with the different form of etching, the results of the high-temperature reverse-bias test included a significant increase in gate leakage, and a belly shape that is ascribed to emission from Coulombic-based traps. "So we can say that the etching variant made with trifluoromethane does not improve the reliability of the device," reasoned Chiocchetta.

Introducing low-pressure CVD for passivation benefitted the HEMT. It reduced gate leakage and suppressed the belly shape effect. "We can say that we have a better stability of gate characteristics," argued Chiocchetta. To investigate trapping behaviour in their HEMT portfolio, the team turned to drain-current transient measurements. Plotting drain current as a function of time uncovered two transients associated with the de-trapping process. The etching and passivation processes only influenced the slower transient, which is thought to be related to hopping and surface phenomena.

Chiocchetta revealed that the team is now starting to investigate gate stress prior to breakdown, using electroluminescence to identify defects along the gate finger. It is hoped that after identifying the exact location of the defects within each device, they could undergo a deeper analysis with the likes of transmission electron microscopy. This might expose differences between the reference device, and the passivation and etching variants.

Investigating traps

During the production of RF GaN HEMTs, process engineers introduce iron dopants to the buffer layer to ensure that it is semi-insulating. This step also increases the breakdown voltage, but traps are added that threaten to degrade reliability.

At the University of Modena, researchers have been investigating the influence of iron-traps on the time-dependent voltage of 0.1 μm GaN-on-SiC HEMTs. The team have uncovered a time-dependent occupancy of iron-traps in their devices that they claim can seriously affect the reliability of GaN HEMTs deployed in the upcoming 5G revolution.

The engineers arrived at this conclusion after experimentally evaluating the time-dependent breakdown voltage on scaled GaN HEMTs, and investigating the correlation between the time-dependent breakdown voltage and iron-trap dynamics. Spokesman for the researchers, Marcello Cioni, told delegates at IRPS that the goal of their work had been to evaluate the time-dependent breakdown voltage of GaN HEMTs through pulsed

current-voltage characterization, realised by varying the length of the off-state pulse. Efforts involved applying short drain-source voltages to a device in its off-state, and using the drain current to reconstruct the breakdown curve at up to 3 mA/mm, for a range of off-state times.

The engineers have defined the breakdown voltage as that at which the drain current starts to increase vertically. "This is a signature of avalanche generation," remarked Cioni, who said that for this to occur there needed to be a leakage path and a high electric field.

To identify the cause of the leakage path, Cioni and co-workers measured the drain, gate and source currents for a range of drain-source voltages. Plotting all three currents exposed source-injection as the cause of the device's breakdown.

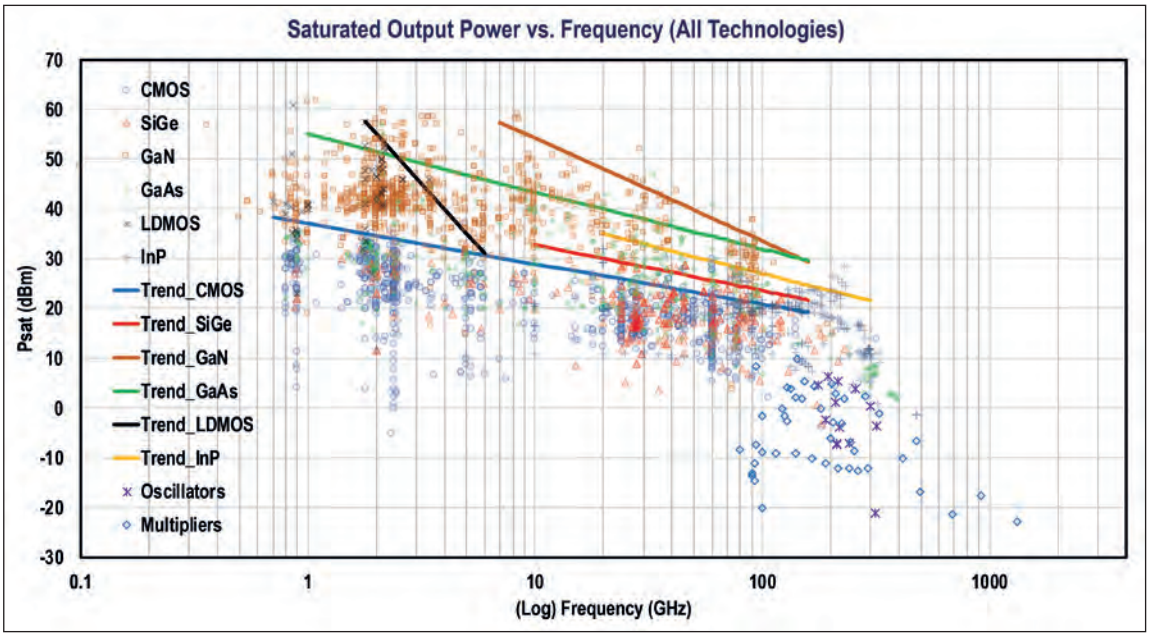
By combining simulations with measurements of the drain current at different drain-source voltages, for a range of off-state times, the team concluded that for longer off-state times the trapped electron concentration increased, reducing the free carrier concentration in the high field region. This results in a higher electric field for device breakdown. With shorter off-state times, the concentration of trapped electrons in iron-traps lowers, and the free-electron concentration increases, reducing the electric field required to trigger breakdown. Another impact of shorter pulses is an increase in the avalanche rate, which also leads to a lower breakdown voltage.

By combining simulations with measurements of the drain current at different drain-source voltages, for a range of off-state times, the team concluded that for longer off-state times the trapped electron concentration increased, reducing the free carrier concentration in the high field region

GaN for 6G

Over the next few years the roll-out of 5G will continue. For those that already access this network, their service may not yet include millimetre-wave transmissions, so there is clearly still a long way to go. However, despite much work still to do, some engineering teams are already considering the successor, 6G, which could start to be deployed from around 2030.

Those that are evaluating what form this technology may take, and what role GaN may have to play within it, include Ned Cahoon from GlobalFoundries



➤ Figure 3. For all semiconductor technologies, there is a significant reduction in the saturated output power with increasing frequency. This data comes from the *Power amplifier performance survey*, provided by Hua Wang and co-workers from Georgia Institute of Technology.

US. At IRPS he presented details of the capability of 6G, the frequencies it may adopt, and the chip technologies that are best placed for building this next-generation network.

One may wonder whether there is even a need for 6G, given the capability of what we have today. However, Cahoon thinks so, pointing to an insatiable demand for data, along with bandwidth and data rates that are doubling roughly every 18 months. He told delegates that the recent increase in data transfer has been driven by video – this year it has been forecast to account for 79 percent of mobile traffic – while the drivers of tomorrow will be a combination of immersive video and multi-sensory experiences, sensor-driven AI metadata, and holographic telepresence.

"6G promises an order or orders of magnitude improvement over 5G network performance," remarked Cahoon, who added that it would offer data rates of up to 1 Tbit/s, an ultra-low latency of 0.1 ms, and high accuracy positioning of around 1 cm, enabling joint sensing and communication functions.

To provide all this capability, there is need to use the sub-terahertz domain, taking advantage of the huge amount of available spectrum between 100 GHz and 300 GHz. Within this domain, the corresponding wavelength is around a millimetre or so. That leads to finer resolution radar, which supports the joint communication and sensing objectives of 6G, and enables the use of smaller antenna.

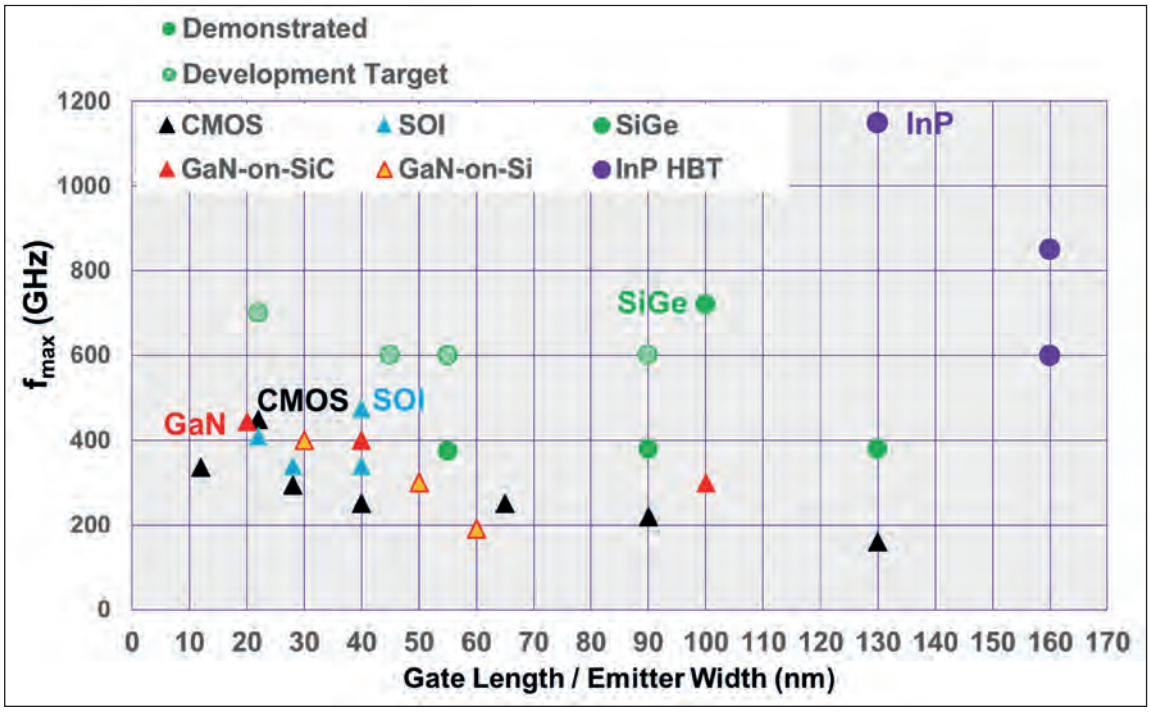
There are challenges associated with the sub-terahertz range. "Losses are much higher above 100 gigahertz," explained Cahoon, who pointed out that free-space loss increases with the square of the frequency, and in addition the routing loss on and off of the chip is very high.

"More importantly, the fundamental device performance is much worse," he added, illustrating this point by showing that for all technologies – that includes CMOS, SiGe, GaN, GaAs, LDMOS, InP, oscillators and multipliers – the saturated output power falls with increasing frequency (see Figure 3). "So all of the parameters that are important at the phased-array front-end of the antennae interface get worse – for the PA, the gain output power and efficiency are much worse; for the LNA, the gain and noise figure is much worse – and this directly impacts the transmit output power and the receive sensitivity." In turn, the link range and data rate are impaired.

Another major issue with increasing frequency, and the corresponding reduction in wavelength, is the reduction in phased-array spacing. Going from a 28 GHz die with an 8 by 8 array to a 300 GHz equivalent slashes the chip size from 47 mm by 47 mm to just 5 mm by 5 mm. As well as a need to scale size while accommodating circuitry in less space, there is a thermal management challenge to overcome.

Fortunately, phased-array technology addresses the reduction in the output power of semiconductor technologies at higher powers, alongside the increased propagation loss, thanks to a combination of concentrating the emitted power into a focused beam and enhancing the sensitivity at the receiver.

"This array-gain benefit lowers the power-per-element that is required," explained Cahoon. "In addition, the number of elements that can fit within an given aperture size increases with frequency



➤ Figure 4. The maximum oscillation frequency for some semiconductor technologies is not high enough for them to be candidates for 6G technology. The rule-of-thumb is that fmax should be at least five times the value of the carrier frequency.

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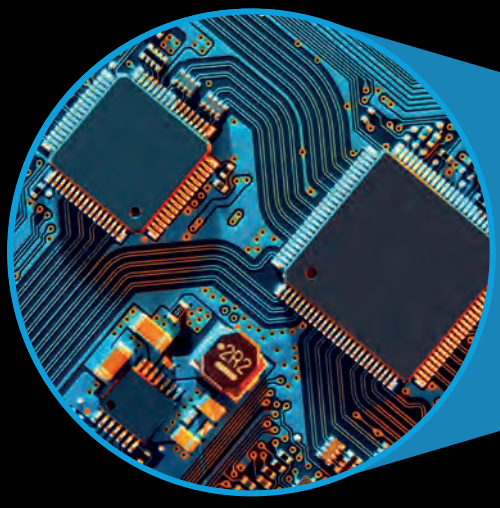

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squared, so that the end result is that even when we move to sub-terahertz frequencies, we can maintain the same link budget as, say, a 5G millimetre-wave phased array, using a lower power output per element, and having a smaller physical array aperture, but yet within that array having many, many more elements."

As f_T and the maximum oscillation frequency, f_{max}, need to be roughly five times that of the carrier frequency used, for 6G these values need to be in excess of 500 GHz. That rule-of-thumb suggests that CMOS and SOI technologies come up short, as they have a performance that plateaus around 450 GHz (see Figure 4). While GaN is also short of that benchmark, peaking at around 420 GHz, SiGe and InP have demonstrated success beyond the high-frequency target.

Cahoon also compared the various technologies for front-end performance, and argued that InP and GaN come out on top. "These material systems have significant advantages over silicon, including a higher breakdown voltage, much higher current and power densities, and a higher electron mobility and saturation velocity." The upshot of these attributes is a significantly better power amplifier at sub-terahertz frequencies.

However, there are challenges with InP and GaN technologies, warned Cahoon. He pointed out the limited-to-no logic integration, addressed by multi-chip architectures, and the relatively high costs compared with silicon technologies. Cahoon stressed that for all semiconductor technologies, it is imperative to have a comprehensive RF reliability methodology. "This is particularly important at 6G, where we are already challenged for device performance." Hitting a high level of performance while ensuring reliability will be far from easy. Adding to the challenge with both 5G and 6G is the need to handle complex waveforms with high peaks, a condition that caused devices to move through a range of degradation regimes.

"Thus it's important to have harder-validated, physics-based reliability degradation models that can be plugged into a reliability simulator that can do lifetime calculations based upon this complex waveform."

Cahoon also reviewed D-band performance of PAs produced with various technologies. He pointed out that the power-added efficiency of silicon is low, at around 13 percent. InP has the highest figure in this regard, hitting 32 percent, while GaN produces the highest output power. For the low-noise amplifier, it's a similar story, with InP offering the lowest noise figure. As well as PAs and low-noise amplifiers, phased-arrays are needed for 5G and 6G networks. Cohen introduced this topic by describing a typical 5G 28 GHz state-of-the-art array, made by Analog Devices. Formed with a 45 nm silicon-on-insulator process, this 256-element antenna-on-board phase array had chips on one side of the PCB and the antennae elements on the other. With each chip dissipating about 5 W in this 50 mm by 50 mm array, there is a dissipated power density of around 10 W cm^{-2}. To extract the heat, there is a large heat sink in thermal contact with the chips.

To progress to 140 GHz arrays, suitable for 6G, the dissipated power density threatens to spike, but must be maintained to 10-20 W cm^{-2}. This plays into the hands of compound semiconductor devices. "We can see the traction of the higher efficiency of indium phosphide for reducing total array power, but this comes with the challenges of the lack of integration capability and the high cost of indium phosphide today." So it might be that SiGe devices are adopted, driven by current efforts to improve its high-frequency capability. With 6G still some way off, it's hard to tell at this stage what role GaN will play there. But for millimetre-wave 5G, there's a great opportunity, supported by efforts to deepen the understanding of impediments to reliability and how to address them. Success on this theme promises to be one of the highlights of the IRPS meeting for several years to come.

Taking transparent conducting oxides into the deep UV

How do you combine high conductivity with excellent transparency in the deep UV? By turning to gallium oxide and a family of stannates

BY KEVIN LEEDY, HYUNG MIN JEON AND DAVID LOOK FROM THE U.S. AIR FORCE RESEARCH LABORATORY

Within the arena of transparent conducting oxides (TCOs), indium tin oxide (ITO), an In_2O_3-rich compound of In_2O_3 and SnO_2, has long reigned supreme: it is inexpensive, easy to deposit as a thin film, offers 90 percent transmission at wavelengths longer than 350 nm, is compatible with standard fabrication processing and, last but by no means least, has excellent electrical properties. So, given all these attributes, surely ITO is a near ideal material for myriad applications. What could possibly be missing? Well, there is a fly in the ointment of this venerable oxide, along with that of most of its peers: a bandgap that quite simply comes up short for applications requiring a source of emission deep within the ultraviolet range – that is, wavelengths below 320 nm.

Enter two new classes of wide bandgap oxide that overcome these weaknesses: β-Ga_2O_3 and $SrSnO_3$. According to recent research, they can break through this UV barrier, while demonstrating conductivities on par with those of existing TCOs.

This pair of oxides forms part of a family of TCOs that exhibit the unlikely combination of high electrical conductivity and optical transparency. Most are single or multi-component metal oxides

that are predominantly polycrystalline or amorphous. These oxides include CdO, the first recognized TCO, and various compositions of In_2O_3, SnO_2 and ZnO doped with a number of species. In some cases, development of these TCOs has been motivated partially by concerns related to indium supply.

Many different approaches can be used to deposit TCOs, including solution-based techniques and a number of chemical and physical vapour deposition methods. The TCOs produced by all these approaches tend to have moderately high bandgaps of more than 3 eV, rendering them potentially useful for a wide range of applications, including electrochromic windows, photovoltaics, solar cells, conductive anti-reflection coatings, transparent thin-film transistors, laser diodes, and flat panel and touch-sensitive displays.

For TCOs, making the leap to an ultra-wide bandgap – that is, a bandgap of more than 3.9 eV – is contingent on finding an amenable combination of substrate and film. While many wide bandgap materials could serve as the substrate, depositing a high-conductivity TCO has been elusive.

But progress is being made, spurred on by efforts from 2012. Back then, researchers at the National Institute of Information and Communications Technology in Tokyo demonstrated the first homoepitaxial β-Ga_2O_3 transistor, leveraging an edge-defined film-fed β-Ga_2O_3 substrate with a doped β-Ga_2O_3 channel layer. This trail-blazing work ignited worldwide research on β-Ga_2O_3 substrates, epitaxial growth and semiconductor development. Critical to optimising transistor performance is minimizing the on-resistance of the ohmic contacts. One promising solution is to use a heavily n^{++} doped homoepitaxial layer in the contact regions.

Our team at the US Air Force Research Laboratory is taking on this challenge. Our efforts allow us to work with a highly conductive layer and a substrate that is transparent, thanks to a 4.6 eV bandgap (see Figure 1 for how β-Ga_2O_3 and $SrSnO_3$ are expanding the capability of the portfolio of high conductivity TCOs).

In our work, we have grown homoepitaxial silicon-doped Ga_2O_3 layers by pulsed laser deposition on semi-insulating, iron-doped Ga_2O_3 (010) single-crystal substrates from Novel Crystal Technology. Our film growth involved directing a KrF excimer laser, operating at a 10 Hz repetition rate and providing an energy density of 3 J cm^{-2}, at a Ga_2O_3 - 1 wt. percent SiO_2 ablation target. We deposited our films under argon at a pressure of 13 Pa, using a substrate temperature of 590 °C.

Armed with attributes

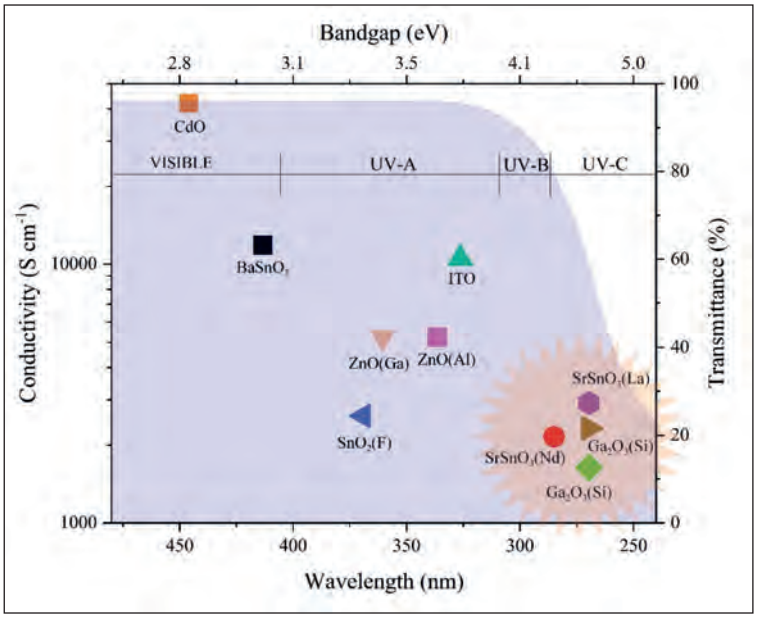
To elucidate film quality, we undertook structural and chemical analyses of our material. X-ray diffraction rocking curves revealed a sharp film peak overlapping the substrate peak, indicating high-quality epitaxy. For silicon-doped β-Ga_2O_3 films with thicknesses from 40 nm to 512 nm, the average [020] full-width at half-maximum is 46.8 arcsec, compared with 32.4 arcsec for the β-Ga_2O_3 substrate.

Scrutinising β-Ga_2O_3 films with atomic force microscopy revealed a smooth surface. Its root-mean-square roughness is about 0.4 nm, only slightly rougher than that of the bare substrate, which has a value of around 0.1 nm.

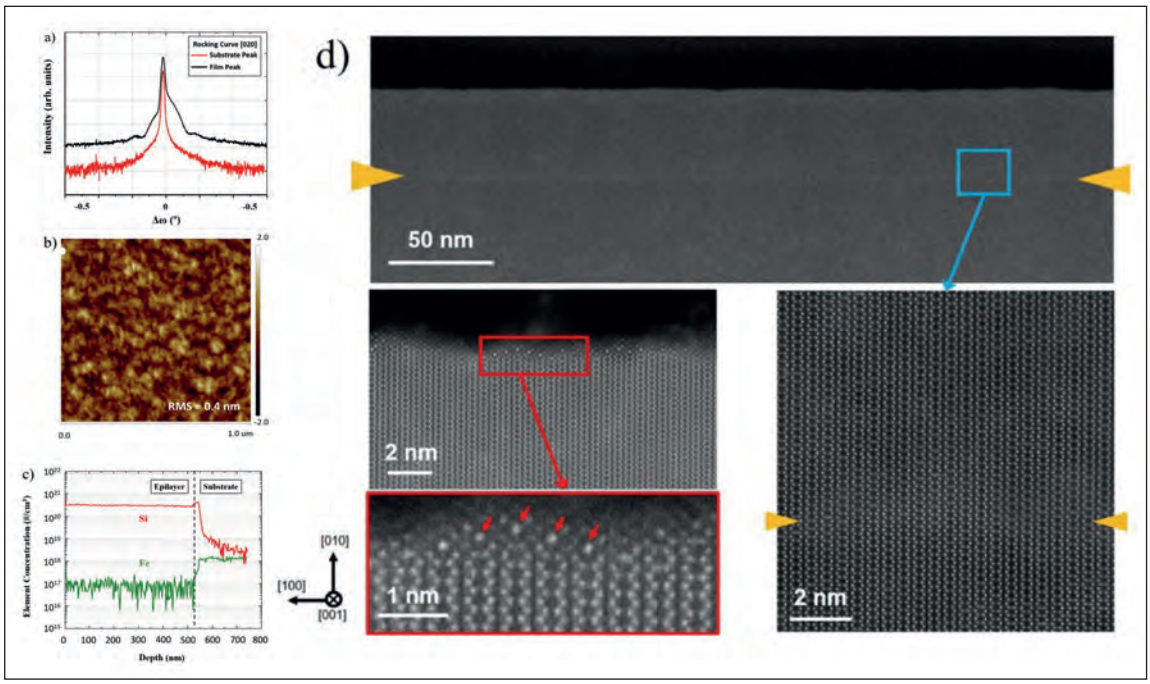
The chemical content throughout our β-Ga_2O_3 layer is uniform, according to depth profiles obtained by secondary-ion mass spectrometry (SIMS) of silicon and iron in a 512 nm-thick representative film. Measuring the silicon level allowed us to determine the extent of chemical incorporation in this layer. Meanwhile plotting the iron concentration enabled us to find out if any of the compensating iron in the substrate, added to make it insulating, out-diffused into the film. As the concentration of iron is around 10^{17} cm^{-3}, it has no impact on film conductivity, and is far below the silicon-dopant level of 3 x 10^{20} cm^{-3}.

We turned to Hall-effect measurements to evaluate the transport properties of our oxide. These measurements indicate a room-temperature conductivity of 2323 S cm^{-1}, approximately a quarter of the value for ITO of 1 x 10^4 S cm^{-1}. Resistivity is 4.3 x 10^{-4} Ω-cm, carrier concentration 2.24 x 10^{20} cm^{-3} and mobility of 64.5 cm^2 V^{-1} s^{-1} (see Figure 1). To form ohmic contacts we deposited a Ti/Al/Ni/Au stack on the sample corners, before annealing this structure for 1 minute at 470 °C under a flow of nitrogen gas.

Comparing the charge carrier concentration obtained by Hall measurements to the silicon



➤ Figure 1. Film conductivity as a function of wavelength for TCOs. Until the recent discovery of wide bandgap β-Ga_2O_3 and $SrSnO_3$ there had been an abrupt boundary at around 330 nm (3.8 eV). The purple shaded region associated with the right Y axis corresponds to a portion of an optimal window transparency extending into the UV range. Adapted from Zhang *et al*. Nature Materials **15** 204 (2016).



➤ Figure 2. X-ray diffraction rocking curves (a), atomic force microscopy surface scan (b), secondary-ion mass spectrometry depth profile (c) and cross-sectional transmission electron microscopy images (d) of homoepitaxial silicon-doped β-Ga_2O_3 films grown by pulsed laser deposition on iron-doped β-Ga_2O_3 substrates. Adapted from Jeon *et al*. APL Materials **9** 101105 (2021).

concentration, determined by SIMS, enabled us to calculate values for the electrical activation efficiency of 77 percent for a 40 nm-thick film, and 56 percent for a 512 nm-thick film. For those of you interested in a detailed analysis of the relationship between doping and Hall-effect results in silicon-doped β-Ga_2O_3, take a look at the box "Delving in to doping" on p. 54.

Confirmation of our film's structure and its quality has been provided by high-resolution scanning tunnelling electron microscopy. Images obtained with this form of microscopy show bright contrast at the interface between the film and substrate, likely originating from point defects. While this film is in the form of the β-phase, there is a very thin surface layer of γ-Ga_2O_3 [110], less than 1 nm-thick. Note that a γ-Ga_2O_3 surface layer has also been observed in β-Ga_2O_3 films grown by MBE, suggesting that the γ-Ga_2O_3 surface layer occurs due to an intrinsic growth mechanism during homoepitaxial β-Ga_2O_3 [010] deposition.

To assess the transparency of this TCO over a wide spectral range, we have undertaken transmittance and reflectance measurements from 190 nm to 3200 nm (6.52 eV to 0.387 eV). These studies, considering a 512 nm-thick silicon-doped β-Ga_2O_3 film grown on a double-side polished β-Ga_2O_3 substrate, reveal transmittance and reflectance, while allowing us to calculate absorbance (see Figure 3). According to these measurements, optical transmittance is about 70 percent from 3.7 eV (335 nm) to 0.56 eV (2214 nm), and falls in the deep UV, reducing to 20 percent at 4.42 eV (280 nm). In this region, the optical transmittance of the highly conductive silicon-doped β-Ga_2O_3 is much smaller than that of the undoped β-Ga_2O_3 – for example, it is roughly half at 280 nm. We have also found that the bandgap of this highly conductive β-Ga_2O_3, having a value of around 4.596 eV, is below that of undoped β-Ga_2O_3, which is typically 4.9 eV. We consider this to be the result of competition between a lower conduction-band edge and a higher Fermi level, both due to heavy doping.

Our primary motivation for developing epitaxial β-Ga_2O_3 is that this material can serve in power devices, such as lateral and vertical FETs and Schottky barrier diodes. All these devices promise to capitalise on the theoretical critical field strength of β-Ga_2O_3 – it can withstand fields as high as 8 MV cm^{-1}. As it is possible to *n*-type dope β-Ga_2O_3 over a large carrier concentration range, this will open the door to a number of intriguing possibilities for advanced device operation.

There are several reports of the Hall-effect mobility versus carrier concentration for β-Ga_2O_3 films formed with a variety of deposition techniques and containing different dopants (see Figure 4). This body of work, published since 2012, includes films formed by MBE, MOCVD, HVPE, low-pressure CVD, mist CVD and pulsed laser deposition. According to literature, silicon, tin and germanium are the principal dopants investigated so far, and the preferred β-Ga_2O_3 substrate orientation is (010). There are fewer reports using (001) and (100).

We have identified three ranges of carrier concentration, corresponding to notional functional regimes. For high-power vertical devices blocking 1 kV or more, doping should be below 2 x 10^{17} cm^{-3}; for lateral power switching, where voltages are below 1 kV, doping is varied from 2 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}; and for optimal device ohmic contacts, doping needs to be degenerate, with a value in excess of 4 x 10^{19} cm^{-3}. As stated already, our film formed by pulsed laser deposition has a conductivity of 2323 S cm^{-1} (designated by red stars in Figure 4),

and could be used as an improved transistor ohmic regrowth contact layer. In this guise, it has been implemented with moderate success.

In addition to our efforts, other researchers are making improvements to the conductivity of β-Ga_2O_3 epitaxial film conductivity, using methods that are more scalable and commercially viable. Those at The Ohio State University have used MBE to demonstrate delta silicon-doped layers (structures with alternating highly doped and unintentional doped layers) with a mobility of 83 $cm^2 V^{-1} s^{-1}$ and sheet resistance of 320 Ohm/sq, and integrated this structure in a FET. Also generating impressive results is the team at the University of Utah, recently reporting a conductivity of 1635 S cm^{-1} for β-Ga_2O_3 grown by MOCVD (see Figures 1 and 4). Their technology, specifically developed for realising an improved ohmic contact, enabled them to produce a fully MOCVD-based MESFET with channel layer, using a 600 °C regrowth process yielding a 73 Ohm/sq sheet resistance. At the U.S. Air Force Research Laboratory, we continue to refine our pulsed laser deposition process to realise higher conductivities. We hope it will not be long before our higher conductivity data, along with improved results from groups using MOCVD and MBE, will be shared.

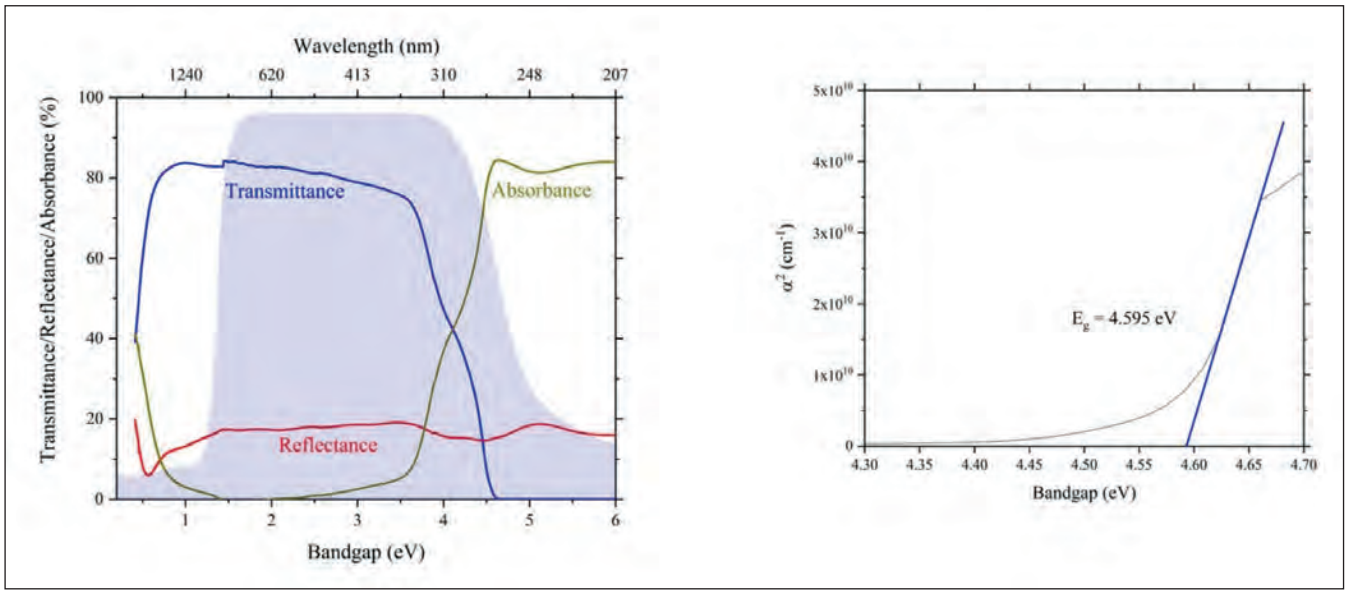
Striking stannates

Within the ultra-wide bandgap TCO landscape, β-Ga_2O_3 is not alone; new reports of TCO stannates are equally intriguing. As one might expect, results vary, depending on the composition of the stannate. For $BaSnO_3$ doped with lanthanum, conductivity is excellent, at around 10^4 S cm^{-1}, but the bandgap is just 3 eV. More promising is lanthanum-doped $SrSnO_3$, exhibiting a conductivity of 2930 S cm^{-1} (plotted in Figure 1) and an estimated bandgap of 4.6 eV, according to results at Hokkaido University using MgO substrates, pulsed laser deposition and a growth temperature of 790 °C.

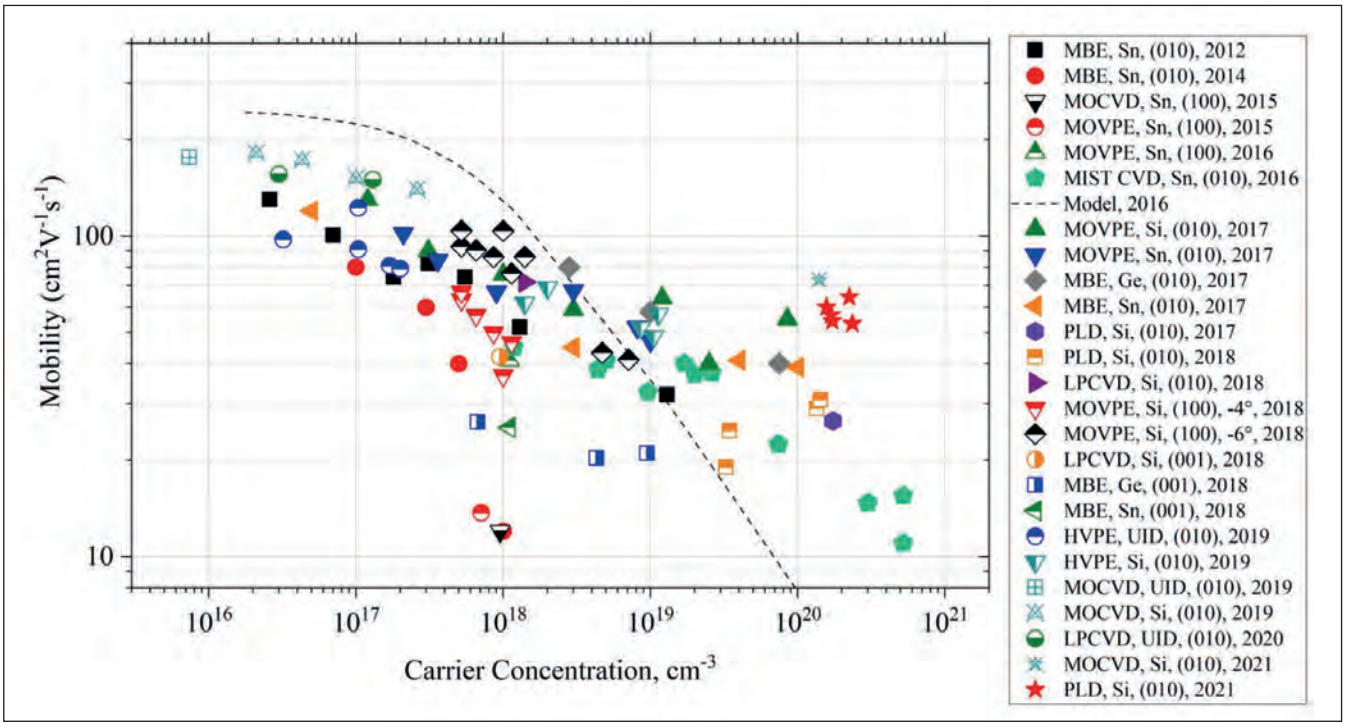
It's worth noting that in stark contrast to the single-crystal epilayer formed during homoepitaxial β-Ga_2O_3 growth, these heteroepitaxial $SrSnO_3$ films have a distinct grain structure. Although this compromises crystal quality, it is beneficial on one front: the lateral grain growth from a 790 °C post-deposition vacuum anneal increases the activation efficiency of the lanthanum ions, and ultimately boosts conductivity.

Researchers at the University of Minnesota have also been exploring the potential of stannates. They have reported a conductivity of 2157 S cm^{-1} for neodymium-doped $SrSnO_3$ grown on a lattice-mismatched $GdScO_3$ substrate with an undoped buffer layer (see Figure 1). While this team did not measure the bandgap of their oxide, they indicated that it is likely to lie between 4.1 eV to 4.6 eV. The mid-point of this range has been adopted in Figure 1.

By turning to non-native substrates and polycrystalline morphology, those working in this field now have many exciting avenues for future device development. ITO and ZnO-based films have a tremendous advantage in this regard, as they are generally substrate agnostic, with polycrystalline or amorphous films resulting. As previously stated, stannates also offer some versatility, as they can be grown on MgO or other substrates. However, it is worth considering that many device demonstrations already accomplished with the β-Ga_2O_3 system and its native substrate have drawn on the opportunity to add charge carriers, either by doping during epitaxial growth or by ion implantation – both are commercially



➤ Figure 3. Transmittance, reflectance, and absorbance measurements made on a 512 nm-thick silicon-doped β-Ga_2O_3 [010] (a). The purple shaded region corresponds to an optimal transparent window. Measured bandgap energy of 4.595 eV from a silicon-doped β-Ga_2O_3 [010] film (b). Adapted from Jeon et al. APL Materials **9** 101105 (2021). The bandgap has been calculated from a linear plot of α^2 versus energy E. The absorption coefficient α is calculated from a formula that holds for small α as well as large α. (Note that the usual Tauc plot of $(\alpha E)^2$ versus E is correct only for amorphous materials.)



➤ Figure 4. Hall effect mobility versus carrier concentration for *n*-type homoepitaxial β-Ga_2O_3 films in the recent literature. Data points in the legend are identified by deposition technique, dopant (if used), substrate orientation and year of publication. Adapted from Jeon et al. APL Materials **9** 101105 (2021).

viable processes. With the stannate system, which is not as advanced as β-Ga_2O_3, device demonstrations are yet to be reported. However, neodymium-doped $SrSnO_3$ has shown a very promising mid-level doping of 3.7x10^{18} cm^{-3}, suggesting that it might be suitable to modulation.

It is routine to form high-quality β-Ga_2O_3 films on native substrates. Fortunately, these substrates can be produced from the melt. That has helped to support rapid device development, and enabled the demonstration of substrates up to 100 mm in diameter. Today, the primary method for making semi-insulating β-Ga_2O_3 substrates is edge-defined film-fed growth, a process used by Novel Crystal Technology and widely adopted for producing

DELVING IN TO DOPING

Highly-doped semiconductors often experience self-compensation, a process in which a dopant produces donors and acceptors, instead of just one or the other. In the case of silicon-doped β-Ga_2O_3 we expect silicon atoms to occupy gallium sites and produce Si_{Ga} donors (charge Z_D = +1) that result in *n*-type conductivity, which is observed. However, to minimise the energy of the crystal, acceptors are incorporated by generating gallium vacancies V_{Ga}. These defects are triple acceptors (charge Z_A = -3) that, as well as reducing the free electron concentration, greatly increase electron scattering, varying as Z_A^2. According to density functional theory, silicon-related acceptor complexes Si_{Ga}-V_{Ga} (Z_A = -2) and 2Si_{Ga}-V_{Ga} (Z_A = -1) can also form, providing another drag on concentration and mobility.

We have used temperature-dependent Hall-effect measurements to determine donor N_D and acceptor N_A concentrations as a function of measured mobility and free-electron concentration for each possible value of acceptor charge Z_A = -1, -2, or -3. More recently we have modelled 40 nm-thick and 512 nm-thick silicon-doped β-Ga_2O_3 films that have silicon concentrations of 3 x 10^{20} cm^{-3} and 4 x 10^{20} cm^{-3}, respectively, according to SIMS. For the special case of the three possible acceptor charges being equally likely, Hall-effect analysis predicts silicon concentrations of 3.0 x 10^{20} cm^{-3} and 3.7 x 10^{20} cm^{-3}, respectively. As these numbers are so close to the SIMS results, the case of three possible acceptor charges is certainly a valid possibility. However, another possibility is that the charge Z_A = -2 is dominant, in which case the Hall-effect prediction would be 2.6 x 10^{20} cm^{-3} and 3.2 x 10^{20} cm^{-3}, respectively.

While more data are required to reach a rigorous conclusion, the Hall-effect model appears to be valid and well worth exploring in greater detail. Indeed, if gallium vacancies are responsible for most acceptors, it is well worth exploring approaches that reduce their concentration. Applying this strategy to gallium-doped ZnO is known to deliver success, with zinc vacancies greatly reduced when annealing the sample face down on a zinc foil under a forming gas ambient.

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sapphire. Meanwhile, growth of β-Ga_2O_3 by the Czochralski method, which has long been utilized for making silicon wafers, is under development by Northrop Grumman Synoptics.

Possible pathways

What should be the next step for wide bandgap TCOs? Although not capitalizing on their material transparency, one immediate integration path is their expanded use as regrowth layers for β-Ga_2O_3 FETs. Efforts in this direction would be beneficial, given that despite significant progress in β-Ga_2O_3 power devices over the last ten years, low-resistivity ohmic contacts are immature and not widely integrated. Note that other techniques, such as spin-on-glass and ion implantation, have also been developed to target lower contact resistance.

A second implementation path entails solar-blind detectors, a class of device that is sensitive to light at wavelengths shorter than 280 nm. When deep-UV photodetectors operate at high temperatures, they have the potential to serve in space communication, UV astronomy, and pollution analysis. Conventional UV photodetectors are impaired by their high dark current leakage, attributed to the narrow bandgap of the silicon-based structures. Switching to wide bandgap materials with high conductivity expands the range of radiation detection, to cover the optical spectrum into the ultraviolet domain, while improving high-temperature performance. Options include SiC, GaN, ZnO, and β-Ga_2O_3. However, SiC, GaN, and ZnO have bandgaps narrower than 4.42 eV, so alloying with another element is needed to increase the bandgap to this critical value and limit absorption of light to wavelengths below 280 nm. Alloying is far from ideal, though, as it leads to large defect densities associated with lattice mismatch.

A more promising candidate is β-Ga_2O_3, which is intrinsically suitable for deeper UV photodetectors – that is, no alloying is required. The pairing of highly conductive β-Ga_2O_3 with a native substrate leads to fewer defects and potentially benefits from homogenous thermal expansion. Note that as β-Ga_2O_3 has a low thermal conductivity, additional studies are required to assess potential thermal limitations.

Another weakness of traditional silicon-based photodetectors is the need for significant cooling to improve the external quantum efficiency. While photodetectors based on β-Ga_2O_3 are in their infancy, initial demonstrations provide a promising performance and uncooled operation, indicating that these devices are a potential alternative to solar-blind detectors made with other materials.

Finally, there is the possibility of improving the capability of β-Ga_2O_3 by alloying it with another material and realising an even higher bandgap. Using MOCVD, β-Ga_2O_3 alloyed with 33 percent aluminium yields a mid-10^{18} cm^{-3} carrier concentration. Building on this is the fabrication of an aluminium-alloyed Ga_2O_3/Ga_2O_3 stack that creates a highly conductive thin channel (2DEG) at its interface. The mobility of electrons in the channel is high as impurity scattering is avoided. It is possible that superlattice-based aluminium-alloyed Ga_2O_3/Ga_2O_3 on a native substrate will provide sufficient conductivity as a deeper UV TCO material.

We see the realization of high conductivity in β-Ga_2O_3 and $SrSnO_3$ as a watershed moment for envisioning TCO applications that extend 'deep' into the UV. With our pulsed laser deposition process we have produced β-Ga_2O_3 with a conductivity of 2323 S cm^{-1}, but the electrical activation efficiency and transmission in the UV are far from ideal. It is paramount to undertake further studies and realise even higher conductivities. We predict that this is possible by increasing the electrical activation efficiency to around 90 percent.

That's by no means the only challenge to address to make these materials relevant and useful for TCO-centric applications. There's much to do, as efforts must be directed at substrate development, mitigation of low conductivity, compatibility with other layers and processing requirements, ensuring short- and long-term stability under environmental conditions, and introducing complimentary *p*-type materials. Motivating all this work will be fulfilling the promise of β-Ga_2O_3, which has great potential as a TCO and beyond.

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ANGEL EVENTS

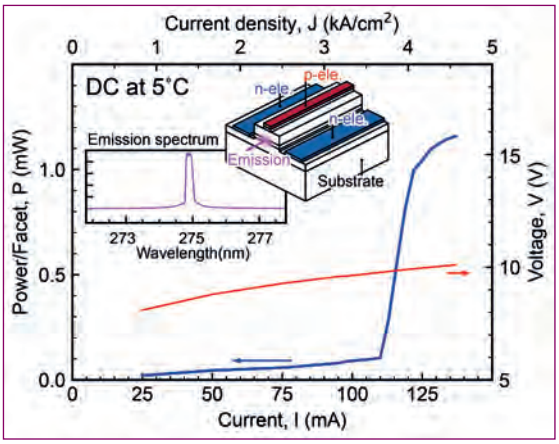
UVC laser delivers continuous emission

Combining a pair of *n*-type electrodes with increased optical confinement enables the first continuous-wave emission in the UVC

A TEAM of researchers from Japan is claiming to have produced the first laser diode that delivers continuous-wave emission in the UVC, which is the spectral range spanning 280 nm to 200 nm. Operated at 5 °C, the device produced by the partnership between Asahi Kasei Corporation and Nagoya University emits an output power of just over 1 mW at 275 nm.

"We believe the accomplishment reported here is a leap towards a practical UVC laser diode," remarked team spokesman Ziyi Zhang, who is affiliated to both Asahi Kasei and Nagoya University. According to him, a UVC laser could be deployed for various tasks, including biological and chemical sensing, particle detection, rapid sterilisation, solar blind communication and materials processing.

➤ CW emission came from the introduction of a pair of *n*-type electrodes and an increase in the material quality of the active region.



The team's triumph came from combining recent breakthroughs in UV laser design with the introduction of an architecture with a higher degree of optical confinement and the addition of a pair of *n*-type electrodes. The resulting UVC continuous-wave laser, which is grown on free-standing AlN, features: an active region with a high internal quantum efficiency; polarization-induced doping; a cladding layer that ensures greater optical confinement; and a pair of *n*-type electrodes, added to the top surface.

Note that while *n*-type electrodes are normally placed on the back surface of a laser diode to ensure a low-device resistance, this is not the first time that they have been added to the top of this class of device. Such a configuration has been employed before for lasers grown on sapphire.

Zhang and co-workers made their breakthrough by evaluating the performance of a portfolio of devices produced by MOCVD on single-crystal AlN substrates.

The team produced a control by depositing an epitaxial stack that contained: a 350 nm *n*-type $Al_{0.7}Ga_{0.3}N$ cladding layer; a 100 nm-thick $Al_{0.63}Ga_{0.27}N$ waveguide, containing a pair of 4.5 nm-thick quantum wells; a 320 nm-thick *p*-type distributed polarization-doped cladding; and a *p*-type contact layer. Dry etching and cleaving created a device with a 5 μm-wide mesa stripe and a 600 μm-long cavity. To increase facet reflectivity to 90 percent, the team deposited 5 pairs of HfO_2/SiO_2.

A variant with an $Al_{0.75}Ga_{0.25}N$ cladding layer allowed Zhang and colleagues to consider the implications of differences in the optical confinement in the quantum well. Increasing the aluminium content lowered the refractive index, cut the leakage of optical modes and reduced the threshold current under pulsed-mode operation. However, all of this came at the expense of an increase in series resistance.

Building on this insight, the team went on to produce a pair of devices – they only differed in having either one or two *n*-type electrodes beside the mesa stripe. Both designs had a higher quantum efficiency than their predecessors, thanks to a reduction in point defects in the quantum wells.

Electrical-optical pulsed measurements on these devices, packaged in TO-cans, revealed a threshold current density of just 2.8 kA cm^{-2}, attributed to the increase in internal quantum efficiency. Switching from a single *n*-type electrode to a pair of them trimmed the resistance from 20 Ω to 12 Ω and enabled the first CW emission. Lasing began at a threshold current density of 3.7 kA cm^{-2}.

According to the team, efforts should now be directed at realising a lower threshold current density for CW lasing. This could come from a higher internal quantum efficiency and an increase in the injection efficiency, which is probably still below 10 percent – in comparison, that figure for the InGaN-based laser diode is typically 60 percent or more.

Zhang revealed that he and his co-workers will continue to improve their device, with the goal of producing a UVC laser with a performance suitable for user testing. "Given the history of laser diode development at any wavelength range, achieving continuous-wave oscillation at room temperature is the next milestone for device performance."

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Novel field plate boosts the blocking voltage

Reducing the electric field strength in the SiO_2 layer increases the breakdown voltage of β-Ga_2O_3 Schottky barrier diodes

A TEAM FROM Japanese has increased the blocking voltage of its β-Ga_2O_3 Schottky barrier diodes by introducing a staircase field plate on a deep trench that is filled with SiO_2. This new archirecture, realised by researchers from the National Institute of Communications Technology (NICT) and Tokyo University of Agriculture and Technology, has increased the diode's blocking from 1.43 kV to 1.66 kV.

The success by the team is another step towards fulfilling the promise of β-Ga_2O_3 power devices, which have the potential to outperform those made from SiC and GaN while costing less to make.

One downside of the Japanese team's latest diode is that its high blocking voltage has come at the expense of an increase in the on-resistance, which climbed from 4.7 mΩ cm^2 to 7.6 mΩ cm^2. According to team spokesman Masataka Higashiwaki from NICT, if the blocking voltage could exceed 2 kV while the on-resistance were kept below 5 mΩ cm^2, this would be an important accomplishment for the power device community.

Success in this regard may be just around the corner, given that the relatively high-resistance associated with the high-blocking-voltage device originated from a weakness in processing: namely, incomplete removal of the surface-depleted-region formed during annealing. "We consider that it is relatively easy to decrease the on-resistance by just optimizing the process conditions a little more," remarked Higashiwaki.

The team identified the superior architecture for their β-Ga_2O_3 Schottky barrier diode by fabricating and investigating three different designs: the control with a conventional field plate, and variants with a staircase field plate and a trench staircase field plate.

Modelling all three designs with Silvaco Atlas software showed that for the architectures with the conventional field plate and the staircase field plate, blocking 2 kV would cause the peak electric field in the SiO_2 layer to hit 12.9 MV cm^{-1} and 12.8 MV cm^{-1}, respectively. As the theoretical breakdown electric field for SiO_2 is just 10 MV cm^{-1}, both designs are likely to fail below 2 kV. A better performance can be expected for the trench staircase field plate architecture, as this has a peak electric field in the SiO_2 layer of 10.0 MV cm^{-1} when blocking 2 kV.

Devices with all three designs were formed by growing a 13 μm-thick *n*-type Ga_2O_3 layer by HVPE on an n^+ Ga_2O_3 (001) substrate. Diode fabrication required several steps, including etching, plasma-enhanced CVD of SiO_2, and the addition of metal contacts by evaporation and lift-off.

Measurements reflected the simulations, with the trench staircase field plate comming out on top, blocking up to 1660V. Benchmarking this device showed that it produced state-of-the-art values for the combination of breakdown voltage and on-resistance.

While even higher values for breakdown voltage have been reported by a team at Cornell using simple trench Schottky barrier diodes, this came at the expense of a higher on-resistance.

Remarking on the pros and cons of different designs, Higashiwaki said: "The simple trench Schottky barrier diodes developed at Cornell are suitable for enhancing the breakdown voltage; however, the active area becomes small, leading to an increase in on-resistance." Note that with the trench staircase field plate design, there is no sacrifice in the active area.

The team always intended to apply the etching process developed for their Schottky barrier diodes to vertical FETs. They are now pursuing that goal.

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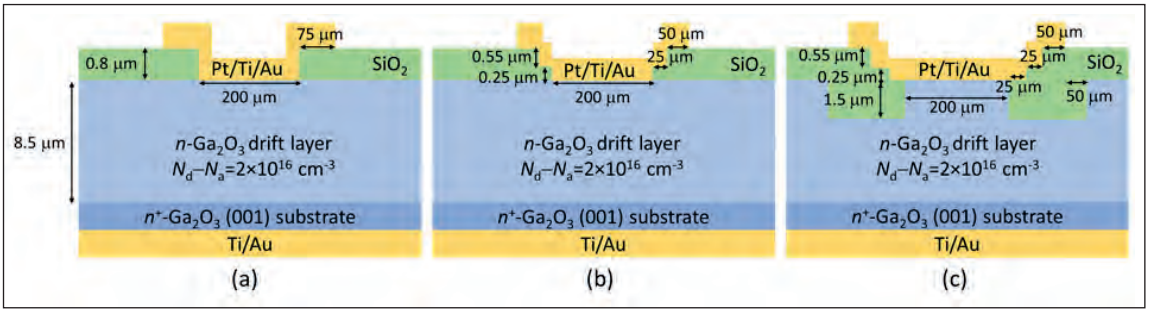


➤ The β-Ga_2O_3 Schottky barrier diode with the trench staircase field plate (c) can withstand a higher blocking voltage than the variant with a staircase field plate (b). The lowest blocking voltage comes from the diode with the conventional field plate (a).

MicroLEDs propel UVC output

An array of UVC microLEDs that is the size of a standard chip delivers an output power of over 80 mW

LEDs operating in the UVC – that's the spectral domain that spans 200 nm to 280 nm – are renowned for a feeble output. But this reputation should soon be shattered, thanks to a collaboration in China led by Peking University that has broken new ground for the output power from a standard-sized chip. The team's best device, containing 16 by 16 microLEDs and emitting at 280 nm, produces more than 80 mW output when driven at 230 mA.

According to team spokesman Xinqiang Wang from Peking University, the very strong emission produced by these LEDs stems from realising a high wall-plug efficiency at a high injection current.

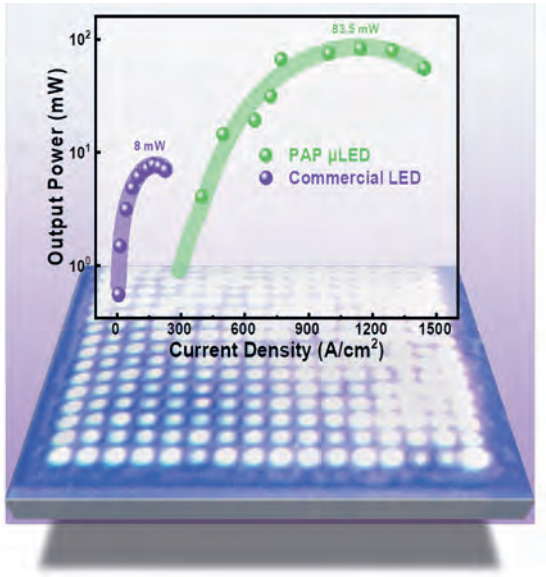
"Conventional state-of-the art planar deep-UV LEDs at 265–280 nanometres typically show their highest value of wall-plug-efficiency at a very small current density, typically lower than 50 A cm^{-2}," remarked Wang. Due to this, conventional devices are only capable of a low light output power.

"In our work, both the light output power and the wall-plug efficiency of our parallel-array planar microLEDs reached their maximum values at current densities larger than 700 A cm^{-2}, making them quite preferable for practical applications," added Wang.

As well as being suitable for many applications often discussed for UVC LEDs, such as disinfection and curing, they could be used for free-space communication, thanks to their high modulation speed. Emitting at 280 nm, the team's UVC LEDs are within the solar blind region, enabling communication that avoids interference from ambient conditions. Another merit of using such short wavelengths is that it allows non-line-of-sight communication, thanks to abundant atmospheric scattering by molecules and aerosols.

The parallel-array planar LEDs developed by Wang and co-workers have several features that help to increase light output power and wall-plug efficiency. Microcontacts are introduced on top of the *p*-GaN to trim absorption from the *p*-type ohmic contact, and the cylinder-shaped mesas are coated with an aluminium mirror to ensure isotropic light extraction. In addition, the device is designed to ensure a homogeneous current distribution; the size of the emission region is reduced to enable a higher current density; and tensile stress is reduced with a smaller mesa size, decreasing the proportion of transverse-magnetic polarized light that hampers light extraction.

A range of devices have been produced by the team: a 16 by 16 array with 25 μm-diameter emitters; an 8 by 8 array with 50 μm-diameter emitters; a 4 by 4 array with 100 μm-diameter emitters; a 2 by 2 array with 200 μm-diameter emitters; and a conventional control, fabricated from the same wafer. All variants have a total emission area of 0.125 mm^2, equal to that for a conventional device.



➤ When parallel-array planar UVC LEDs have emitters with a diameter of just 25 μm, the output power exceeds that of a conventional device by an order of magnitude.

The control produced a peak output of 8 mW at 170 A cm^{-2}. This power exceeded that for devices with emitters with diameters of 50 μm or more. In stark contrast, the device with a 16 by 16 array of 25 μm-diameter emitters delivered an output power of 83.5 mW at a current density of 1150 A cm^{-2}, while its wall-plug efficiency peaked at 4.7 percent at 775 A cm^{-2}. Superior performance is attributed to a suppression of light absorption and a homogeneous injection current.

For solar blind communication, the more powerful device has the most promise, as its high light-output-power at a high current density, allied to its small size, has the greatest potential for realising a high modulation bandwidth over a long distance. Measurements on this device using orthogonal frequency-division multiplexing revealed a data rate of just over 1 Gbit/s at a bit-error rate of 1.3 x 10^{-2}.

One of the next goals for the team is to fabricate parallel-array planar deep-UV microLEDs with even smaller pixel size, for example, 1 or 2 μm.

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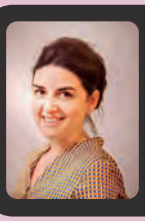

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