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As well as new materials, better devices result from the introduction of superjunctions, extra channels and many gates

SHIFTING FROM LIGHT TO SOUND

Directing high-frequency sound around a chip positions GaN as a promising platform for acoustic-wave devices

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VIEWPOINT

By Dr Richard Stevenson, Editor

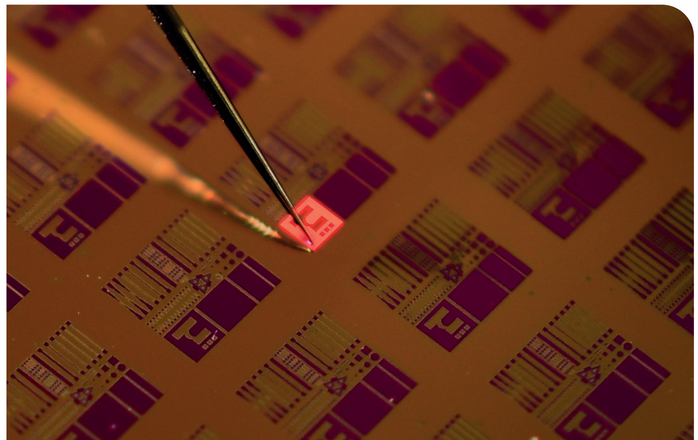
Inspirational innovation

THERE'S tremendous innovation on so many fronts to thank for making the compound semiconductor sector so vibrant and fascinating, and giving us all so much to discover and digest. Details of many of these breakthroughs populate this publication, with this issue reporting several advances in device performance that have been underpinned by trailblazing material science.

For developers of smaller displays based on microLEDs that are targeting augmented-reality, one of the biggest challenges is to realise an efficient, compatible red emitter. The device needs to be grown on silicon, as this allows the substrate to be bonded to a silicon IC that drives the pixels. Unfortunately, the conventional epitaxial stack for making red LEDs is off limits, as it contains arsenic, which is outlawed in CMOS processing lines that are ideal for volume production. This roadblock has led many researchers to turn to nitrides, using an increase in indium content in the wells to propel emission from the green to the red. But as the wavelength gets longer efficiency plummets.

An attractive alternative approach, unveiled by imec spin-off Micledi at this year's Consumer Electronics Show in Las Vegas, is to produce red LEDs from an arsenic-free epi-stack based on AlInGaP. Devices drawing on this quaternary can emit at considerably longer wavelengths than their GaN-based cousins while producing a far sharper spectral peak that aids the focusing of emission into a viewing angle (for more details, see p.14).

Another company reaching far longer wavelengths than its peers is the German



maker of VCSELs, Vertilas. For many years it has pioneered the production of VCSELs that combine InP-based quantum wells with an InP-based mirror and another made from a dielectric (reasons behind this pairing are discussed in the company's contributed feature, starting on p. 38). Initially developed for gas sensing, Vertilas' VCSELs are now targeting optical communication and sensing, with the introduction of arrays amplifying the output of these sources.

In addition to these advances in photonics, in this issue you can read about progress in phononics. As sound waves in the gigahertz domain have a wavelength that is similar to light in the telecommunication band, there is an opportunity to route sound waves through structures with similar dimensions to photonic integrated circuits. Investigating this possibility is a team from the University of Bristol, UK, which is developing a GaN-on-SiC technology that could aid the design RF systems (see p. 50 for details).

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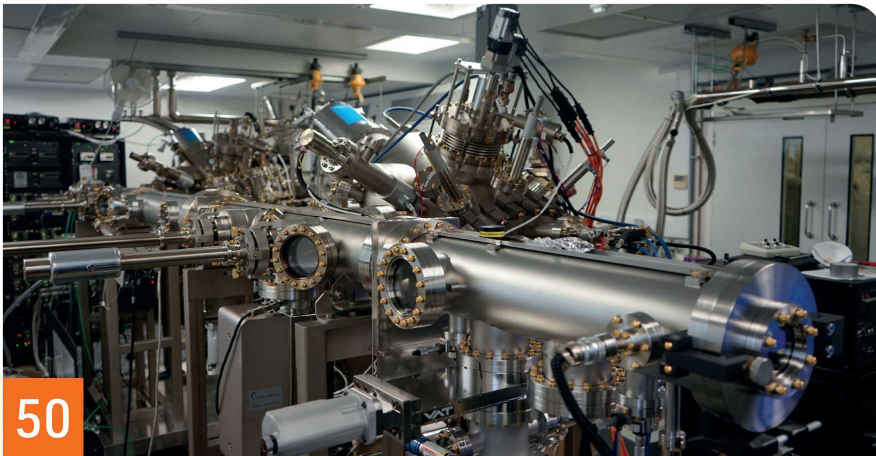

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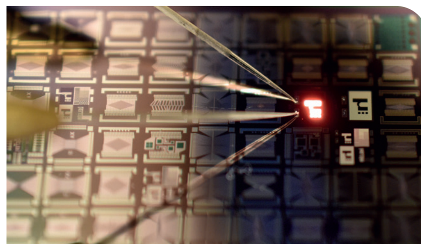

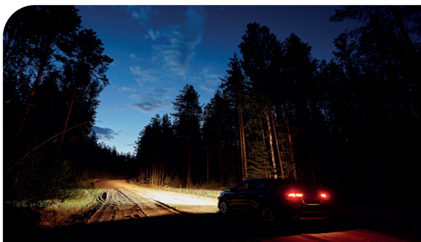

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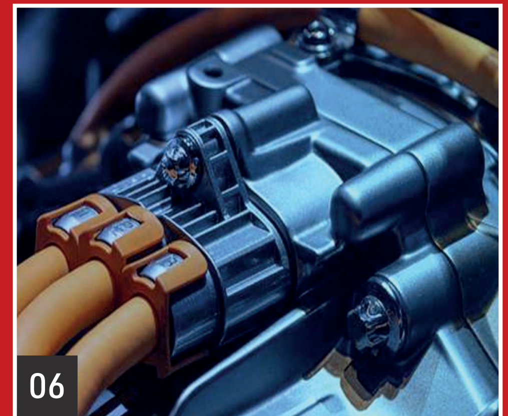

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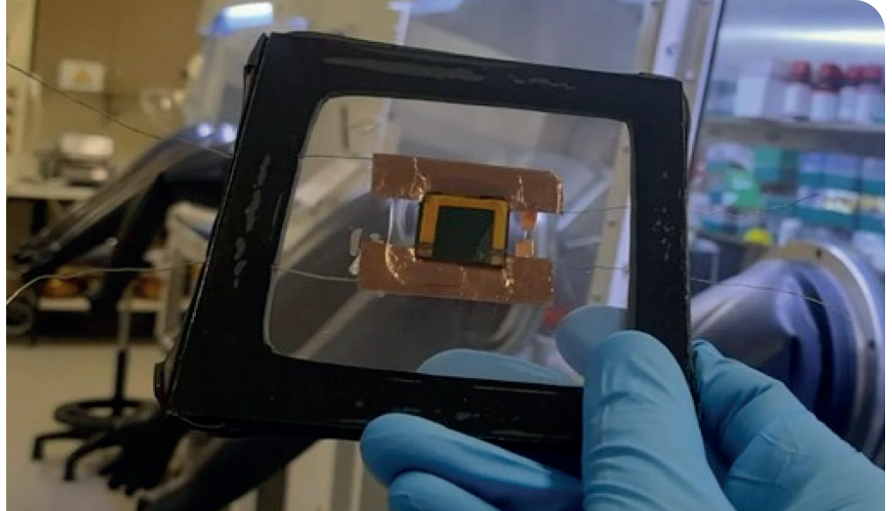
Perovskite tandem is 30.3 percent efficient

Australian National University team builds on previous record

RESEARCHERS at The Australian National University (ANU) have achieved an efficiency of 30.3 percent for a tandem solar created by mechanically stacking a perovskite cell on top of a silicon cell. Their findings have been published in *Advanced Energy Materials*.



Lead author of the study The Duong says: "With these tandem solar cells, the perovskite top cell can efficiently absorb the blue light and transmit the red light to the silicon bottom cell, producing significantly more energy from sunlight than each individual device."

"We've achieved an efficiency of 30.3 percent for mechanically-stacked perovskite-silicon tandem cells – meaning 30.3 percent of sunlight is converted into energy. In comparison, commercial silicon solar cells have an efficiency of around 20 percent."

This work builds on a previous record set by ANU researchers in 2020. Their new technique not only improves efficiency, but enhances the operational stability of the solar cells.

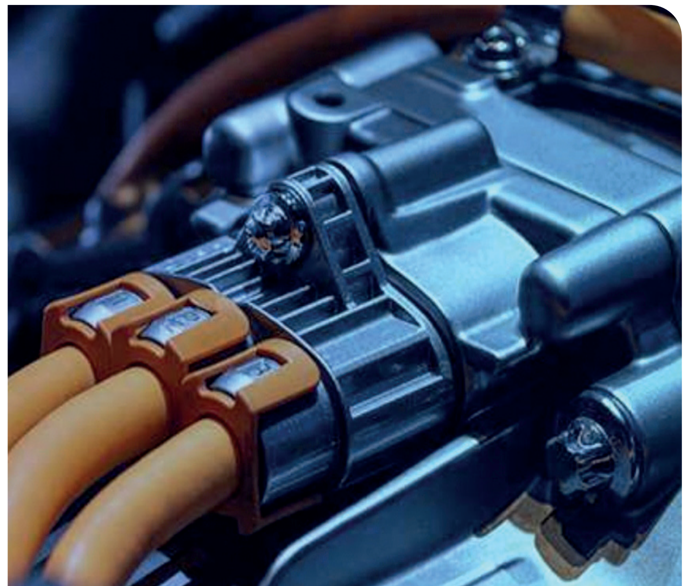
"Surpassing the 30 percent mark is significant," Duong said."That's currently considered the efficiency threshold for the commercialisation of tandem technology like that used in our study."

"The current predictions are that tandem solar technology will be in mass production by 2026. However, more work is still needed to upscale and ensure the technology can be stable in the field over 25 to 30 years."

The team is now working to further improve the efficiency and stability of their solar cells.

Wolfspeed and ZF to build SiC fab in Germany

US SiC CHIP MAKER Wolfspeed and German automotive giant ZF Friedrichshafen plan to build a $3 billion wafer factory in Germany to make chips for EVs and other applications, according to recent reports in the German business newspaper *Handelsblatt*. Production should begin in four years at the site in the southwest German state of Saarland, the report added.



Wolfspeed CEO Gregg Lowe said last year that the company was considering building a semiconductor factory in Germany, and that an investment decision would depend on the subsidies it received. ZF and Wolfspeed already have an ongoing strategic partnership to create electric drivelines, announced in November 2019.

ZF has sales to automakers of $33.4 billion in 2020. It is a worldwide supplier of driveline and chassis technology for cars and commercial vehicles, along with specialist plant equipment, such as construction equipment. It is also involved in rail, marine, defence and aviation industries, as well as general industrial applications.

German President visits Infineon Kulim fab site

€2 billion compound semiconductor fab will be ready for equipment in summer 2024

GERMAN PRESIDENT Frank-Walter Steinmeier visited Infineon Technologies Kulim site in Malaysia, as part of his trip to Asia. Infineon is building a new plant there for €2 billion that will focus on SiC and GaN semiconductors.

Kulim 3 will be ready for equipment in summer 2024 and will create 900 jobs. Infineon confirmed that construction work is on schedule.

During Steinmeier's visit (pictured right), Infineon presented its investment in expanding the exhaust air purification system at the Kulim site. Avoiding CO_2 emissions is a clear priority for Infineon in implementing its climate strategy.

The upgrade in Kulim is expected to result in an approximately 8 percent reduction of global direct site-related emissions by the end of the 2023 fiscal year, compared with the previous year.

A planned new exhaust-air purification system in Austin, TX, will lead to further savings. The company has also set the goal of operating 100 percent of its plants in Malaysia with green electricity in the future and is in close exchange with local suppliers and the government to this end. The initiative will help further improve Infineon's positive climate contribution.

Today, the company's energy-efficient solutions help save 33 times the amount of CO_2 emitted during production.

"Infineon is fully aligned with the trends of decarbonisation and digitalisation," said C.S. Chua, president and MD of Infineon Asia Pacific.

"The growing demand for renewable energy, e-vehicles, as well as energy-efficient applications, will lead to a strong increase in the demand for power semiconductors. Our investments in Kulim and beyond are laying the foundation for being able to serve this growing need as well."

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Ams Osram to benefit from Apple microLED use?

Ams Osram has formed the tightest collaborative relationship with Apple in the field of microLEDs, says TrendForce

ACCORDING to TrendForce, Apple is expected to adopt microLEDs for its consumer electronic products in the close future, with the Apple Watch likely be the first product to feature a microLED display in 2024. Then, during the period from 2026 to 2030, the application scope of microLEDs could expand to encompass AR headset displays, smartphone displays, automotive displays, and so on.

The Apple Watch as a product line was launched in 2015. The Apple Watch Ultra, the latest model, was released near the end of 2022 and offers improvements to display specifications. Apple enlarged the display size to 1.93 inches and raised the display brightness level to 2,000 nits. These upgrades indicate that smartwatch brands continue to seek a larger and sharper display that can show text clearly in an outdoor setting.

TrendForce believes Apple will make a breakthrough for its smartwatch in 2024 by incorporating microLEDs. With this technology, the display of the Apple Watch could exceed 2 inches and achieve an even higher contrast level. Such improvements would satisfy the viewing needs of professionals and enthusiasts of various outdoor sporting activities.

TrendForce points out that Apple has always been careful about adopting a new technology. However, once Apple decides to use a particular technology, the company usually tries to apply it across different product lines, as has been the case with OLED displays.

Factors for microLED adoption

Whether microLEDs are incorporated into smartwatches, AR headsets, or smartphones, two major factors will determine the market competitiveness of this technology. The first factor involves lowering the costs of microLED chips.

A notable solution to make the production of microLED chips much more economical is to enlarge the wafers that they are made from. Currently, the production lines for the mainstream microLED chips take in 6-inch wafers. Switching to 8-inch wafers will result in a considerable cost reduction.

The second factor concerns flexibility. MicroLEDs have to work with different types of backplanes that contain glass, CMOS, etc. A reliable semiconductor manufacturing process is needed to serve as the basis for scaling up production. Such a process is also critical for the provisioning of a total solution (i.e., from chip production to mass transfer, inspection and repair).

Among suppliers for LED chips, Ams Osram has formed the tightest collaborative relationship with Apple in the field of microLEDs, because it has advantages in addressing the two aforementioned factors. In the future, Ams Osram will very likely become Apple's key partner in supplying the microLED components that are embedded in next-generation displays, says TrendForce.

For the new display technologies emerging recently, microOLEDs and microLEDs are the ones capable of meeting the demand for a high number of pixels per inch. However, microOLEDs cannot reach the higher level of brightness that microLEDs can achieve.

It is rumoured that Apple will be unveiling a headset featuring a microOLED display this year. Nevertheless, in the development of AR headsets over the medium to long term, TrendForce believes building a headset with a completely transparent display will require optical waveguides. However, incorporating optical waveguides will reduce the original brightness of a display by as much as 99 percent. Therefore, microLEDs with their huge brightness advantage can provide the sufficient leeway to compensate for this massive loss of brightness.

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Ams Osram qualifies Aixtron tools for microLEDs

AIX G5+ C and G10-AsP MOCVD systems now qualified on 200 mm wafers for a microLED application

AIXTRON has announced that Ams Osram has qualified the Aixtron AIX G5+ C and G10-AsP MOCVD systems on 200 mm wafers for a microLED application.

The MOCVD systems AIX G5+ C and the new G10-AsP from Aixtron SE offer Aixtron planetary technology, which is said to be paving the pathway for the next generation of high-resolution microLED displays.

In spring 2022, Ams Osram announced plans to create additional manufacturing capacity in 200 mm for the production of LEDs and microLEDs at its existing location in Malaysia. The MOCVD systems are expected to help enable volume production of microLEDs for a new generation of display applications.

“Aixtron and Ams Osram have a long-standing cooperation, and we are familiar with the performance and quality standards of the equipment. For an ambitious project like the development and production of microLED for AsP and GaN devices, we needed exactly such a partner at our side”, says Robert Feurle, executive VP and head of Business Unit Opto Semiconductors at Ams Osram.

Felix Grawert, CEO and president of Aixtron SE, adds: “The G10-AsP and AIX G5+ C qualification at Ams Osram is a very important milestone in our company’s history. Ams Osram is a world-class LED manufacturer and perfectly positioned to enable the fundamental new technology that will come to market. We are on the verge of a technology shift away from conventional display technologies to a new type of microLED displays.”

Grawert added: “Now, Aixtron is entering one of the future’s growths markets that has an enormous potential, and we are doing this with a perfect partner at our side.”

The production of microLED comes with special requirements, including a special transfer process where many thousands of LED chips are picked up and transferred. Any defect can result in dead pixels that can make an entire array useless. Hence, an almost error-free epitaxy is necessary, minimising defects and allowing for high yield and economically viable production of microLEDs. Aixtron’s new G10-AsP epitaxy tool has been designed to address the specific needs of this application.

SLED has record breaking optical power

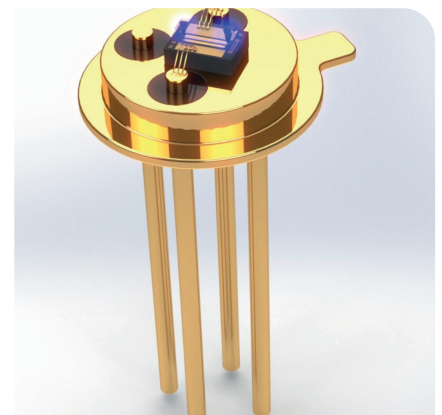
iSLight, a spin-out of Tyndall National Institute, Ireland, has developed ground-breaking speckle-free, surface-emitting blue superluminescent LEDs.

The newly developed technology, unveiled at *SPIE Photonics West*, in San Francisco, has a world record-breaking peak optical power of around 2.2 W under pulsed operation, with high-resolution beam quality.

Thanks to wafer-scale packaging and testing, the GaN-based SLEDs should have a lower production cost than commercial lasers maintaining similar power density and efficiency, according to iSLight. In addition, they are more compact, and they can be scaled in power by going to arrays. Scaling in volume is possible using 100 mm diameter GaN wafers.

Applications that could benefit include machine inspection instruments, direct imaging lithography, VR/AR headsets, projection displays, microscopy imaging systems, lighting systems and 3D printing.

SLEDs exploit the process of amplified spontaneous emission, where the light of spontaneous emission is amplified only in a single pass through an optical waveguide as compared to amplification over multiple roundtrips in a laser diode. Any kind of feedback in the optical cavity is avoided in a SLED, resulting in a broadband spectrum



with no amplitude modulation (spectral ripple).

While the iSLight SLEDs are currently blue (400-450 nm), they can scale to other wavelengths (green, red, infrared).

Onsemi and VW cement SiC collaboration

Companies are developing a complete traction inverter solution for the OEM's modular car platform for electric vehicles

ONSEMI has signed a strategic agreement with Volkswagen to provide modules and semiconductors that enables a complete electric vehicle (EV) traction inverter solution for VW's next-generation platform family. The semiconductors are part of an overall system optimisation and provide a solution that will support the front and rear traction inverters in the VW models.

As part of the agreement, Onsemi will deliver in a first step its EliteSiC 1200 V traction inverter power modules. The EliteSiC power modules are pin to pin compatible to easily scale the solution to different power levels and types of motors. Teams from the two companies have been collaborating for more than a year on the optimisation of the power modules for the next generation platform, with pre-production samples under development and evaluation.

"The superior performance and quality of Onsemi's traction inverter modules together with our joint efforts to create the best system solution enable us to deliver the outstanding driving experience and quality customers expect from a VW group vehicle," said Karsten Schnake, head of the operative and strategic semiconductor taskforce COMPASS at VW.

"Onsemi's broad portfolio of intelligent power and sensing solutions further allows us to offer cutting-edge technologies and features in our EVs, from the traction inverter and beyond. Beside this milestone, Onsemi with its balanced production facility layout in the USA, Asia and Europe, including the plant in the Czech Republic, is the perfect match to support our strategic markets with all high-voltage solutions and more."

With 19 wafer fabrication and packaging manufacturing sites, Onsemi provides VW with more than 500 different devices – including IGBTs, MOSFETs, image sensors and power management integrated circuits. In addition to its versatile portfolio, Onsemi has a vertical SiC production chain that includes volume boule growth, wafering, substrates, epitaxy, device fabrication, best-in-class integrated modules and discrete package solutions, that perfectly supports a secured supply chain.

"Our broad manufacturing footprint – including a resilient end-to-end SiC supply chain – empowers Onsemi to deliver the supply assurance OEMs demand," said Simon Keeton, executive vice president and general manager, Power Solutions Group, Onsemi.

The inverter solution for EVs consists of Onsemi's EliteSiC 1200 V 3x Half-Bridge Modules, and this system solution supports both axle inverters covering a wide range of power.

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World's first monolithic InGaN RGB LED for microLED displays

Soft-Epi and Sundiode develop an RGB stacked epiwafer for microLEDs

IN A WORLD FIRST, Soft-Epi and Sundiode are claiming to have jointly developed a monolithic red, green and blue (RGB) stacked epiwafer for microLED displays using only InGaN materials without wafer bonding. This is said to be another big step for microLED displays after the development of an InGaN-based red LED last year.

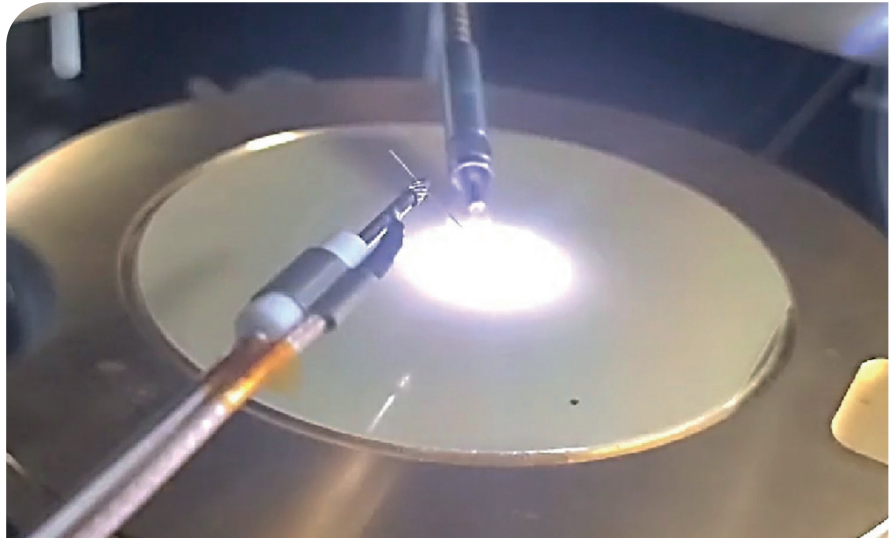
South Korean-based Soft-Epi has a GaN epitaxy technology, with a focus on manufacturing InGaN epitaxial growth for visible light including nitride-based red LEDs.

Sundiode is a US Silicon Valley based company that develops microLED technology for display applications, including augmented reality (AR) and mixed reality (MR), as well as heads-up displays (HUDs).

In order to realise a next-generation full-colour micro-LED display with ultra-high resolution (5000 ppi), it's necessary to go through a very complicated process of using wafer bonding technology and removing the substrate after individual epitaxial growth of R, G and B on each wafer. This process has been the biggest problem in implementing full-colour microLED displays.

The two companies have realised the RGB epitaxial layers with independent *p-n* junctions on a single substrate with a single epitaxy growth without an additional wafer-bonding process. This new development has been made through Soft-Epi's epitaxial growth technology and Sundiode's design technology.

The collaboration's approach is completely different from the previous conventional method, wafer-bonding technology, or a colour control method using wavelength shift according to current density change. It is a monolithic stacked RGB structure that can drive RGB colours independently. This is regarded as an ideal RGB pixel structure for manufacturing high-resolution micro-displays.



Monolithic RGB epitaxial growth technology has the advantage of greatly simplifying the process of manufacturing a high-resolution full- colour micro-display compared with the existing conventional method of bonding individual red, green, and blue wafers, or the method of implementing RGB by repeating epitaxial growth several times using selective growth technology.

It is also expected to greatly contribute to the manufacturing process of microLED displays for large screens (signage, TV, etc.). Compared to the existing method, the number of chips used can be reduced by a third, and the chip transfer process can be reduced to a third or less, which will lead to significant manufacturing costs reductions.

This development is expected to be an important milestone in manufacturing technology for high-resolution, full- colour micro displays based on microLEDs. An expert in microLEDs said for this development, "Soft-epi has cracked the code for microLED, and it's an important milestone for high-resolution, full-colour micro displays."

Soft-Epi and Sundiode are now developing a monolithic RGB micro display prototype as the next step. They expect that this successful development of the monolithic RGB epiwafer is significant, in that it has secured an important basic technology that enables high-resolution micro-displays suitable for AR and MR as well as HUD devices.

> Monolithic RGB epitaxial growth technology has the advantage of greatly simplifying the process of manufacturing high-resolution full-colour micro-display

Veeco acquires Epiluvac

Swedish CVD epitaxy firm brings advanced SiC experience to Veeco

VEECO INSTRUMENTS has acquired Epiluvac, a privately held manufacturer of CVD epitaxy systems that enable advanced SiC applications in the electric vehicle market.

Epiluvac, based in Sweden, was founded in 2013 by a highly experienced team in SiC. Epiluvac's technology platform combined with Veeco's global go-to-market capabilities create a significant long-term growth driver for Veeco.

The SiC device market is forecasted to grow at approximately a 30 percent compound annual growth rate (CAGR) from 2023 through 2027, according to Yole Group. Accordingly, the SiC epitaxy equipment market is expected to grow at a CAGR of approximately 15 percent over the same time period, based on Yole Group and internal Veeco estimates.

"The Epiluvac team has developed a superior platform and process know-how aligned with markets that are a great strategic fit for Veeco," said Bill Miller, Veeco's CEO. "Their well-designed CVD platform achieves high productivity, is easy to maintain, and has superior process control capability that make it uniquely qualified to produce devices that enable lighter, smaller and more efficient power-conversion systems."

Miller added: "This acquisition accelerates our penetration into the emerging, high-growth SiC equipment market by reducing our time to market."

"We are excited to join Veeco, a recognised leader in semiconductor and compound semiconductor capital equipment," commented Per-Anders Eriksson, Epiluvac's CEO.

"Our complementary technology platforms, along with Veeco's extensive worldwide sales, service and manufacturing capabilities, will position us well to help our customers enable accelerated SiC adoption. The decades of research and development the Epiluvac team has invested in this demanding epitaxial process will be a great asset to Veeco's already impressive process capabilities."

The purchase price for Epiluvac, payable in cash, is $30 million at the time of closing, with a potential additional $35 million in performance based earn-outs. The impact to Veeco's financial results are not expected to be material in 2023 and volume revenue is expected to begin in 2024.

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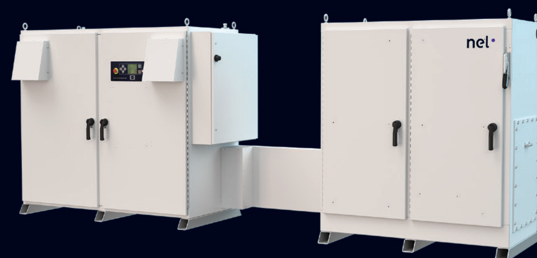

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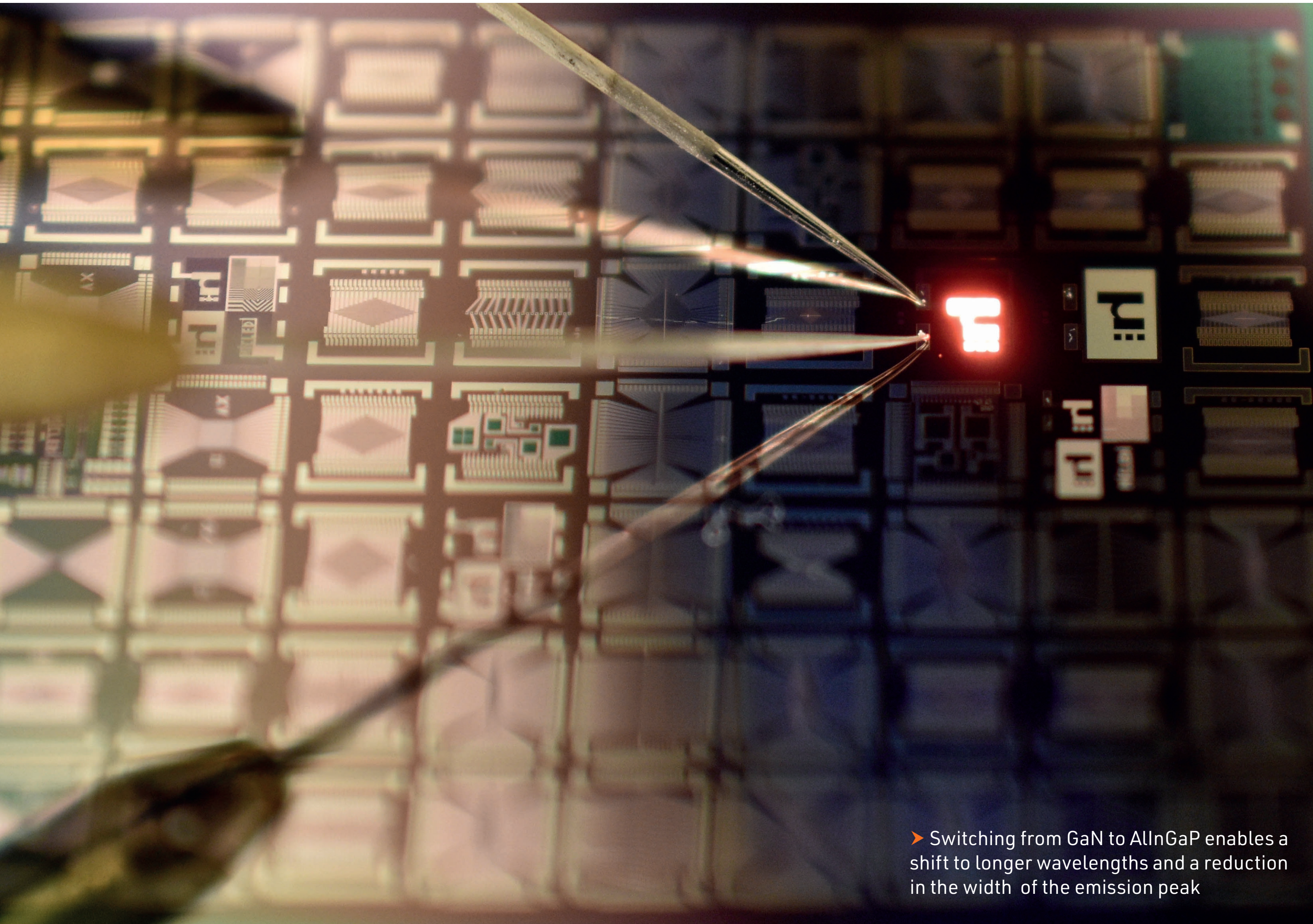


Switching from GaN to AlInGaP enables a shift to longer wavelengths and a reduction in the width of the emission peak

Red microLEDs: Brighter and better

Moving to arsenic-free AlInGaP-based heterostructures enhances the key characteristics of red microLEDs while retaining their compatibility with CMOS processing lines

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

INTEREST in displays based on microLEDs is sky high. The tremendous capabilities of these miniature marvels – including exceptional efficiencies, a simple approach to scaling dimensions and incredibly long lifetimes – makes them very attractive candidates in many forms of display, from smartwatches and augmented-reality glasses through to TVs and video walls.

However, realising commercial success in all these types of display will not be easy. For the production of larger displays there has to be a picking and placing of millions and millions of tiny red, green and blue LEDs, a task that cannot be completed quickly enough with today's tools.

It is more likely that the first significant sales of displays deploying microLEDs will come from an uptake of augmented reality. For this type of application, arrays of single-colour LEDs formed on silicon wafers can be bonded to 'backplane' ICs that

drives the pixels – with colour images constructed via optics that draws together the emission from red, green and blue arrays.

The challenge with this approach is to produce efficient emission in the red. It's not possible to shrink the conventional red-emitting LEDs used for the likes of automobile brake lights to the micro-scale, because these established devices contain arsenic, which is outlawed in CMOS lines. And the obvious alternative, extending the emission of nitride-based devices that excel in the blue and green to the red, leads to plummeting efficiencies.

But there is a way to avoid both these pitfalls: make red microLEDs from an arsenic-free stack that's based on AlInGaP and grown on silicon. That's the trailblazing technology developed by imec spin-off Micledi, which unveiled its triumph at this year's Consumer Electronics Show (CES), held in Las Vegas at the beginning of January. The devices produced in this manner are a more compelling alternative to the company's more conventional, GaN-based red microLEDs, which emit broader emission at shorter wavelengths.

Micledi's first AlInGaP microLEDs have an emission peak at 653 nm. That's probably about 15-20 nm higher than needed, according to the company's VP of Business Development, Harold Blomquist. However, he says that it's nice to have the extra headroom.

As well as substantially stretching to longer wavelengths, Micledi's AlInGaP microLEDs provide a far narrower spectral width, with a full-width at half-maximum below 9 nm, compared with less than 50 nm for nitride-based variants. This hike in spectral purity aids efforts to direct far more of the emitted light into the viewing angle, thanks to less dispersion.

The Belgium-based company decided to develop AlInGaP microLEDs because they reasoned that they may have more promise than their nitride siblings, which have shown slow progress, despite being studied by many groups for many years. Working with partners, Micledi's recent success is the culmination of at least a year's efforts.

Production of the company's displays starts with the sourcing of epiwafers from various suppliers. "We are really agnostic to epi-materials, because good epi comes in 6-inch wafers, it comes in 8-inch wafers, and we want to use the best epi material," argues Blomquist.

Epiwafers are chopped into display-sized chiplets, which are bonded to a 300 mm carrier wafer and dispatched to a semiconductor fab, where 300 mm lithography defines the dimensions of the microLED. This approach ensures very tight process control and excellent repeatability across the entirety of every wafer.

Not that long ago it was far from easy to secure a slot in a 300 mm fab, but times have changed markedly, says Blomquist. "We're not bound by 18-to-24 month sold out manufacturing profiles. There is today a much more open-minded interest in looking at [processing our material] as a way to utilise older process nodes."

The sector with the biggest promise right now, stylish glasses sporting microLED-enabled augmented reality, is still to emerge. But variants of this technology are starting to appear in industrial and enterprise sectors, through product launches from the likes of Vuzix and Magic Leap, both exhibitors at CES.

In industry, augmented-reality glasses are able to aid the capability of operators at work stations, offering guidelines, instructions, and providing images of what to do; and in medicine they can support surgeons, who are better-positioned to exchange ideas with other medical professionals located outside the operating theatre.

As well as substantially stretching to longer wavelengths, Micledi's AlInGaP microLEDs provide a far narrower spectral width, with a full-width at half-maximum below 9 nm, compared with less than 50 nm for nitride-based variants

While some will be sceptical whether AR glasses will ever catch on with consumers – there are those that will surely shy away from such an immersive experience – Blomquist is adamant that this technology will take off. He is convinced that AR glasses will become a must-have for younger generations, who will revel in reading their latest messages and following social media while their phones remain in their pockets.

Before this revolution takes place, there will have to be improvements to the brightness of displays, alongside a trimming of their operating power, size and weight.

Alongside these long-term goals, Micledi has another, based on the driving technology. The company currently uses a passive matrix, which provides a lot of flexibility, in terms of illumination, images and device characterisation. "But we are working very seriously on bringing out an ASIC backplane, to bring an active matrix solution into the marketplace just after the middle of the year."

With progress on multiple fronts, Micledi is destined to be a key player in the growth of microLED displays.

MicroLEDs revolutionise the headlight

Working together, Nichia and Infineon have unveiled a compact, ground-breaking automotive light engine with over 16,000 microLEDs

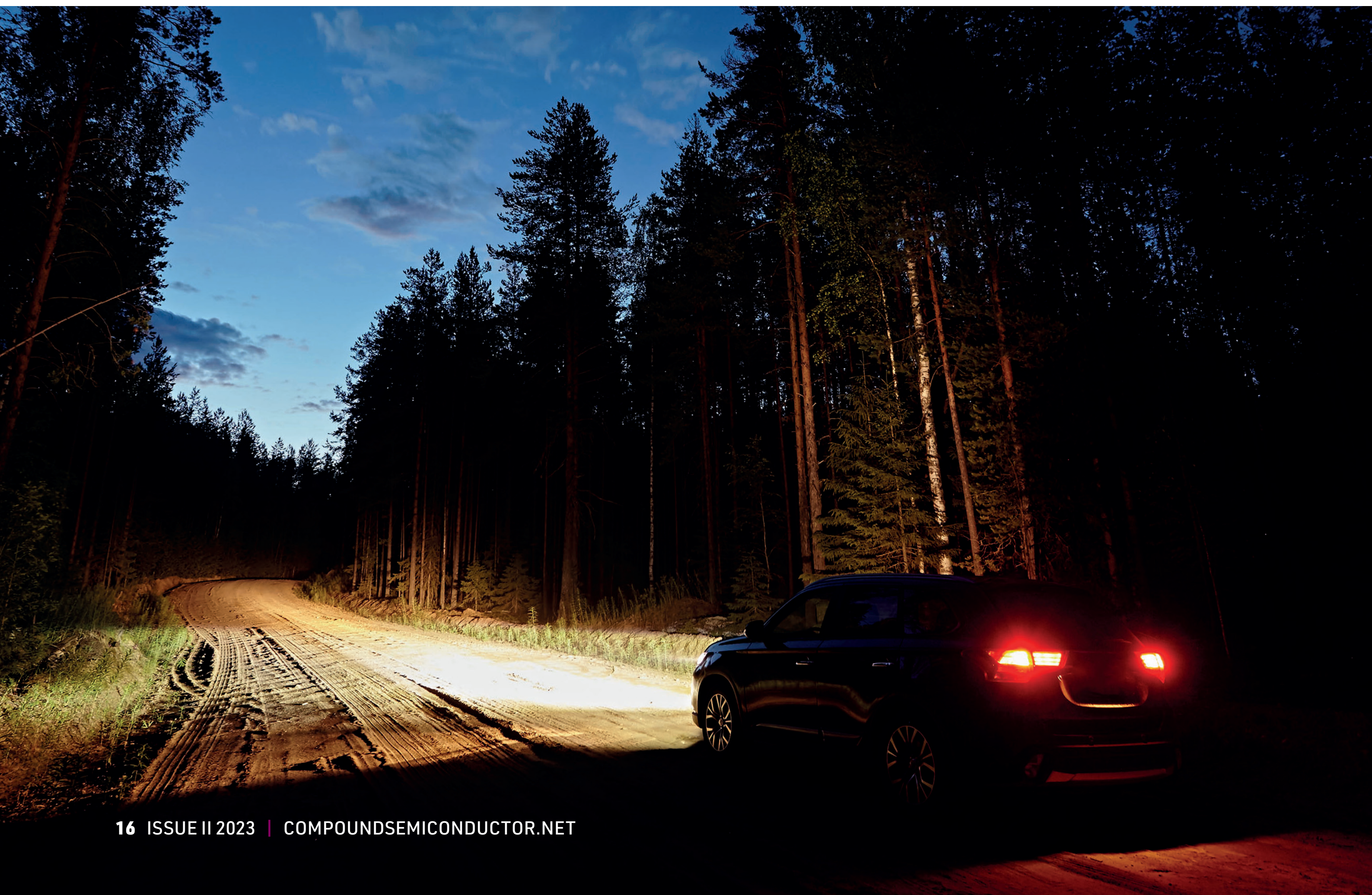
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

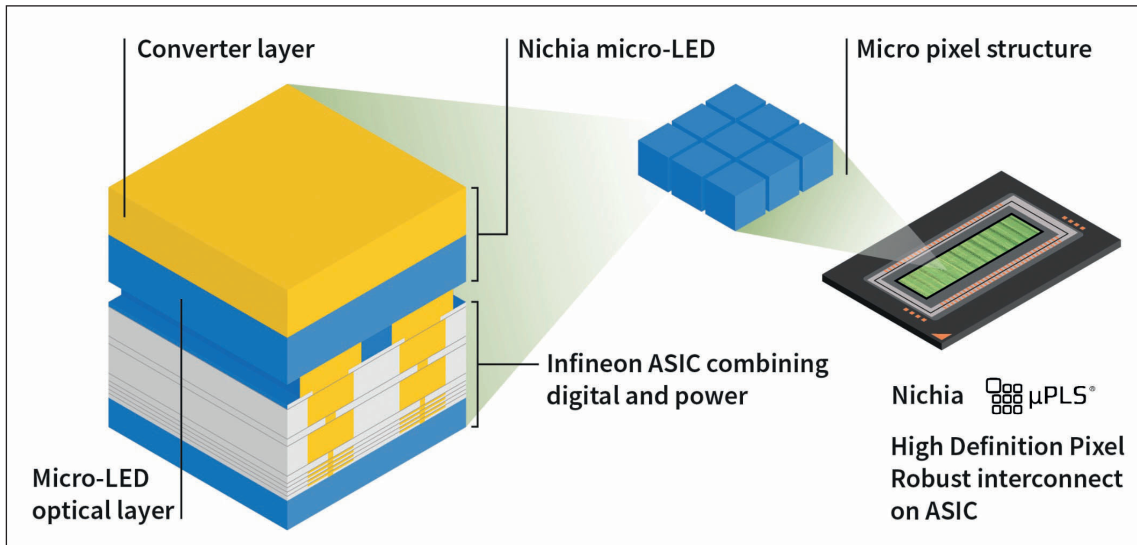
OVER MANY YEARS, the car industry has been migrating from traditional light bulbs, including halogens, to ever-more-powerful LEDs – they are more efficient, more robust and longer lasting. This transition began with red brake lights, and more recently these sources have played an increasing role in indicators and headlights, with many top-of-the-range models now sporting a matrix LED technology that enables an adaptive driving beam.

Now matrix LED technology is taking a leap forward, thanks to a partnership between two giants of our industry, Nichia and Infineon.

At the start of this year they unveiled an incredibly compact light source for the headlamp that's free from mirrors, the norm for a high-definition matrix technology, and packed with far, far more LEDs than ever before.

This product, drawing on Nichia's expertise in LEDs and Infineon's pedigree in drive electronics, is described by this pair as a micro-Pixelated Light Solution. It enters a market that is starting to see matrix LED technology trickle down from high-end cars to the likes of VW, as well as some models from Opel, which places a premium on lighting performance.





The new automotive light engine, sporting 16,384 microLEDs, draws on Nichia's prowess in LEDs and Infineon's expertise in silicon IC drive electronics.

The number of LEDs in the matrix LED headlights already on the road can be as few as just 8, although units housing 70, 84 or 102 LEDs are also common.

"84 pixels is already a very good solution, in terms of matrix illumination of the road," comments Robert Remmers, Infineon's Product Line Manager for the jointly developed automotive light engine that houses thousands of microLEDs. "However, what customers want is a finer graduation of the light, or finer control of the light on the road."

Remmers adds that with 16,384 microLEDs, their collaboration's automotive light engine offers all this and more: "For example, you could mark certain tracks on the road, where you need to drive through a construction site, or have illumination of pedestrians on the side of the road."

Another strength of the new automotive light source over the incumbent is its *modus operandi*. This difference is comparable to the difference between LCD and OLED TVs – with former, all the pixels are on all the time, while with the latter, they are only on when needed, saving energy.

As well as requiring the LEDs to be constantly on, the incumbent form of high-definition matrix headlight is compromised by the incorporation of mirrors, leading to bulky units. Remmers compares their size to that of a brick, adding that they are also expensive, heavy and difficult to implement.

"If you look at our solution, it is essentially just one small chip," enthuses Remmers, who suggests that the size of this unit is around just twice that of a computer mouse.

The new light source has been put through its paces in driving tests. "We see that it's very bright," remarks Remmers, who attributes the exceptional intensity of light projection to the high drive currents for the microLEDs, as well as their high level of efficiency.

If even brighter sources are needed, car makers could consider headlights based on lasers, a technology pioneered by BMW and Audi. However, this class of headlight has failed to gain much traction in the market. That may be because its capability to illuminate several hundred metres of road is only of much value when driving at speeds beyond that allowed in many countries. Many drivers may argue that it's actually more useful to have a higher fidelity of lighting over a shorter range, a feature provided by the micro-Pixelated Light Solution.

It has taken three years for Nichia and Infineon to co-develop and launch their revolutionary automotive light engine. While some might think that's a long time, it's not when you consider all the work that's needed to prepare a product for the automotive market. This sector is renowned for its rigorous, conservative approach to qualifying parts.

Another factor to consider is the level of innovation that's been needed to bring this particular product to market. Part of the development involved the design of a new 50 μm by 50 μm microLED by Nichia to ensure that it would illuminate the road with sufficient brightness. Both parties then had to work together to ensure a sufficiently robust connection between the emitters and the driver IC chip, produced by Infineon.

"If you take all these factors into account, I would say it's truly amazing how we have managed to do this," remarks Remmers.

Ownership of the product lies with Nichia; it is responsible for generating sales. However, the first model to be fitted with the revolutionary headlight will not come from Asia, but Europe.

This does not surprise Remmers, who points out the high level of innovation introduced in European luxury cars. "It's just a natural evolution that it started here in this particular case."

Scrutinising SiC with X-ray topography

X-ray topography, already on the cusp of revolutionising the quantification of dislocations in SiC wafers, is now available in a high-throughput form that accelerates progress

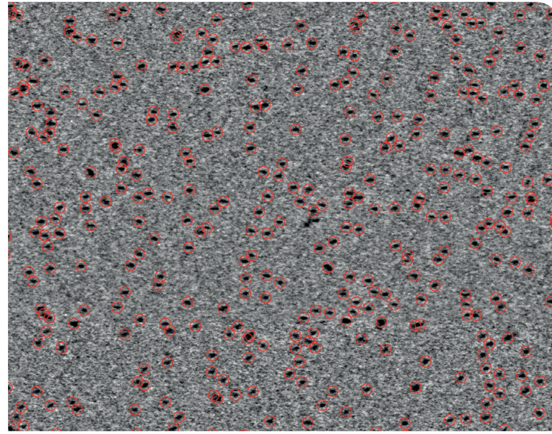
BY CHRISTIAN KRANERT AND CHRISTIAN REIMANN FROM FRAUNHOFER IISB AND SHINTARO KOBAYASHI, YOSHINORO UEJI, KENTA SHIMAMOTO AND KAZUHIKO OMOTE FROM RIGAKU

SILICON CARBIDE is now a mature material that enjoys substantial success in the power electronics sector. Devices made from this semiconductor are currently displacing silicon-based incumbents, especially in the fast-growing market of electric mobility, where SiC is being adopted in both vehicles and charging infrastructure.

Alongside ramping sales of SiC devices, there has been a tremendous improvement in the quality of the material, as well as increases to wafer diameter to 150 mm and 200 mm. However, when it comes to crystalline material quality, SiC is certainly not as perfect as silicon.

One of the weaknesses of SiC is that it contains dislocations. These imperfections are not going to completely vanish from this material in the short term, and their presence matters – they can have a severe impact on the yield, the performance and the reliability of the final devices. Due to this, there's a need to know the dislocation density of a SiC wafer, a metric that reflects the quality of the material. In fact, such information is more prised than ever, because the high standards within the automotive industry are pushing supply chains towards a complete tracking of all components, from raw material to the final product. Consequently, characterising dislocations in the substrate material provides a valuable piece of information for qualifying suppliers, and for tracking device failure.

Until recently, the 'gold standard' for quantifying dislocations in SiC substrates involved etching this material in an aggressive alkaline melt heated to roughly 500°C. But this approach is far from ideal. One major weakness is that it is destructive to epi-ready wafers. As every SiC boule may differ from the next, wafer manufacturers analyse at least one wafer from every boule to ensure that they meet the required specifications. Assuming an average yield of 30 to 40 wafers per boule, this etching-based evaluation incurs a yield hit of around 3 percent, a loss that could be eradicated with a non-destructive characterisation technique. Additional drawbacks include those related to the stability of the etching process, the reliability of automated etch pit counting and a lack of standardisation.



➤ Figure 1. Typical TSD density mapping obtained with the Rigaku XRTmicron. Red circles indicate automatically detected locations of screw dislocations.

Addressing all of these concerns is high-resolution, lab-scale X-ray topography (XRT). This technique builds on synchrotron XRT measurements, which

Rigaku XRTmicron tool features

THE XRTmicron from Rigaku is a fast, high-resolution X-ray topography system for non-destructive imaging of crystallographic defects for samples up to 300 mm in diameter. It has a wide range of capabilities, including:

➤ The ability to determine various types of dislocations and non-uniformities within many types of bare single crystal wafers, including: semiconductors (for example silicon, germanium, diamond, SiC, GaN, AlN, GaAs, InP, CdTe, CdZnTe); oxides (such as sapphire, ruby, garnets, vanadates, niobates, quartz); halides (for example, fluorides, bromides); wafers with epilayer structures; partially processed wafers; and bonded wafers. All may be imaged in reflection and transmission mode.

➤ A scan speed that's ten times higher than that of conventional systems, thanks to the combination of: a high-brilliance dual-wavelengths X-ray source, the MicroMax-007 DW, that uses the Kα lines of copper (40 kV, 30 mA) and molybdenum (50 kV, 24 mA); and X-ray mirrors optimised for topography.

➤ Capturing of digital images of crystallographic defects, by either: a high-resolution XTOP (5.4 µm per pixel); a ultra-high resolution HR-XTOP (2.4 µm per pixel) CCD camera; or the new HYPIX3000 detector for FastBPD measurements and a fast, high-quality overview scan.

➤ Cross-section topography, including 3D defect reconstruction. This gives the possibility to localize defect structures within the sample volume.

➤ The opportunity to mount samples horizontally, to ensure minimum artificial strain. Part of the measuring procedure is an automatic wafer curvature correction, to ensure best defect image quality.

➤ Fully automatic operation of all system components, including the X-ray anode, detector and optics switch, optics and sample alignment, and image collection. With the optional wafer handler, batches of 25 wafer can be measured without user interaction.

➤ For SiC application, the XRTToolbox software, which provides standardised analysis procedures to conveniently determine TSD and BPD densities from XRTmicron measurements.

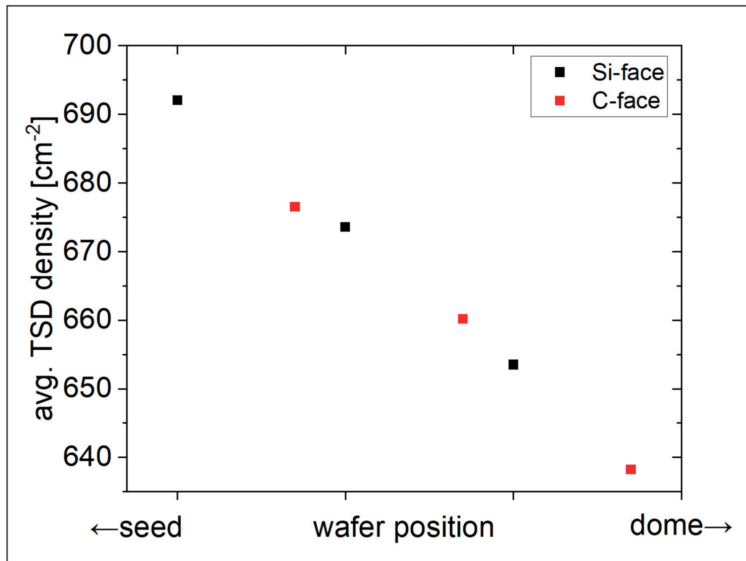


Figure 2. Pushing the limits of accuracy: Three neighbouring wafers from the same crystal were measured by XRT on both sides, and the average TSD density over the wafer area taken. As well as resolving the decreasing trend of dislocation density from seed to dome, the data reveals which face of the wafer is facing which direction. One might even estimate the spacing between the individual wafers.

have always been used to identify and detect dislocations – but those measurements are typically performed only locally, and require beam time at synchrotron facilities, so are unsuitable for use in an industrial setting.

These limitations make the Rigaku XRTmicron, which brings high-resolution XRT to the lab, a game changer. This instrument allows engineers to visualise single dislocations, thus making it possible to quantify them. As dislocation images recorded by XRT originate purely from local crystallographic strain, this technique is not derailed by variations in doping concentration between different wafers.

While these advantages have much promise, those within the SiC industry seek assurance that the results provided by this non-destructive technique are consistent with those that come from etching. Investigating whether this is the case is our team at the Centre of Expertise for X-ray Topography, a research collaboration between Rigaku Corporation and Fraunhofer IISB. We address market needs by drawing on Rigaku's excellence in building state-of-the-art X-ray tools and Fraunhofer IISB's competences along the SiC value chain.

We have found that once those working in industry have been assured of the validity of XRT, their interest in this technique rapidly increases, along with demands, particularly regarding measurement times. To address this specific demand, we have introduced the FastBPD approach: it brings high-speed, full-wafer XRT measurements to labs and industry lines. But let's start this story at the beginning…

From TSDs…

The most common polytype of SiC substrate is the 4H variant, which is usually grown by physical vapour phase technology. The material that results contains various defects with different properties. Historically, 4H-SiC contained large volumetric defects, like polytype inclusions, but now they tend to be eliminated completely from prime grade material. Unfortunately, micropipes and stacking faults are still present, leading to almost certain device failure. However, the propensity of these imperfections has plummeted in recent years – and for R&D purposes, the presence of these extended defects can be spotted easily by the naked eye in X-ray topograms.

This leaves us with three common types of dislocation: threading screw dislocations (TSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs). With the conventional approach to identify these dislocations, standard potassium hydroxide etching of the silicon-face of SiC substrate material, etch pits from TSDs and TEDs are not easily distinguished. Since today's prime grade material has far fewer TSDs than TEDs, it is a challenge to determine the TSD density reliably. To overcome this issue, technicians can turn to C-face etching, or add oxidising agents to the potassium hydroxide melt. But this introduces new challenges. The reality is that the SiC world has lacked a technique to reliably quantify the TSD density in substrates, often resulting in the omittance of TSD densities in industrial wafer specifications.

An absence of data for the TSD density matters, because this class of dislocation can wreak havoc in some type of device. For example, if TSDs are present in the channel region of MOSFETs, this can promote electric breakdown, leading to device failure. Another issue is that depending on epitaxial conditions, growth pits can occur at the locations of the TSDs, creating device processing issues and ultimately causing device failure.

For the detection of TSDs, XRT is peerless. With correct diffraction conditions, the topographic image almost exclusively exposes individual dark spots, each corresponding to a single TSD (see Figure 1). Simply counting these spots provides the density of TSDs. However, those working within industry have had to be convinced of the capability of XRT before they are willing to make the switch to this technique. They have required reassurance of how the results by XRT relate to those realised by etching, and they needed convincing of the reliability and the accuracy of defect detection.

We have undertaken tests to evaluate how XRT compares against five other experimental techniques. Our goal was to verify that counting based on XRT contrast delivers the same

> We have undertaken tests to evaluate how XRT compares against five other experimental techniques. Our goal was to verify that counting based on XRT contrast delivers the same information as conventional approaches

information as conventional approaches.
The five other experimental techniques were: examining etch pits after epitaxy, which allows one to distinguish between TSDs and TEDs; inspecting etch pits, following etching in a melt of potassium hydroxide and sodium peroxide; counting hillocks on the C-face of SiC after etching in potassium hydroxide; using grazing incidence synchrotron XRT, as this can identify TSDs; and scrutinising growth pits after epitaxy, an approach that allows engineers to relate material imperfections to weaknesses associated with device processing. All five comparisons affirmed the capability of XRT, with tests yielding identical dislocation distributions, numbers, and positions. Based on this overwhelming agreement, we are in no doubt whatsoever over the validity of XRT measurements for TSD detection.

If XRT is to be used in industry, tools that apply this technique must deliver reliable results. To confirm that this requirement is met, we developed a measurement and analysis routine – this included measurement parameters, guidelines for the required image quality, and a robust but fast analysis algorithm, which required less than 5 minutes to analyse the full topogram of a 150 mm wafer. We have found that our instruments provided a high measurement repeatability, giving values within 3 percent of one another, and an inter-machine reproducibility with a similar error. Drawing on this exceptional degree of accuracy, engineers can even measure differences in TSD density between neighbouring wafers (see Figure 2).

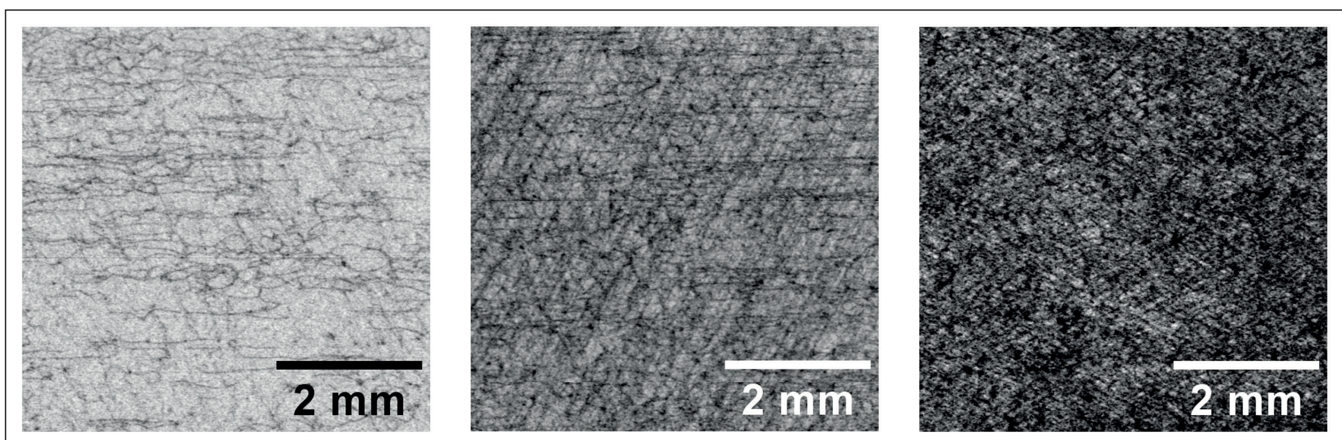
The opportunity to undertake non-destructive measurements awakens a desire to measure more wafers per SiC boule. However, if this is to happen, there needs to be an increase in throughput. To ensure this is possible, we have adapted partial wafer measurements to the XRT approach. Thanks to this refinement, one can measure the average TSD density of a full 150 mm within 30 minutes with an error of less than 10 percent.

This chapter of this particular story culminated with the publication of SEMI M91, an industrial standard describing TSD detection by XRT. This documentation ensured that XRT is now an established tool for dislocation detection and, in the case of TSDs, has overtaken the old *de-facto* standard by becoming a regular alternative.

...over BPDs...

For companies working with SiC substrates, the opportunity to undertake non-destructive detection of TSDs is a compelling reason to invest in XRT for material characterisation. But that is not the only benefit: there is also the detection of other types of defects, including BPDs.

With XRT, it is more challenging to quantify the detection of BPDs than TSDs, because it is more complex than simply counting points. BPDs appear



➤ Figure 3. Typical X-ray topograms in transmission geometry, mainly showing basal-plane dislocations as curvilinear features. Sub-figures show different dislocation densities, increasing from left to right. A measurement of individual lines is only possible at low dislocation densities, those below 500 cm^{-2} (left image). A different analysis strategy is required for higher dislocation densities. Using integral image analysis, this limitation has been overcome, allowing the measurement of very high BPD densities of 5000 cm^{-2} and above.

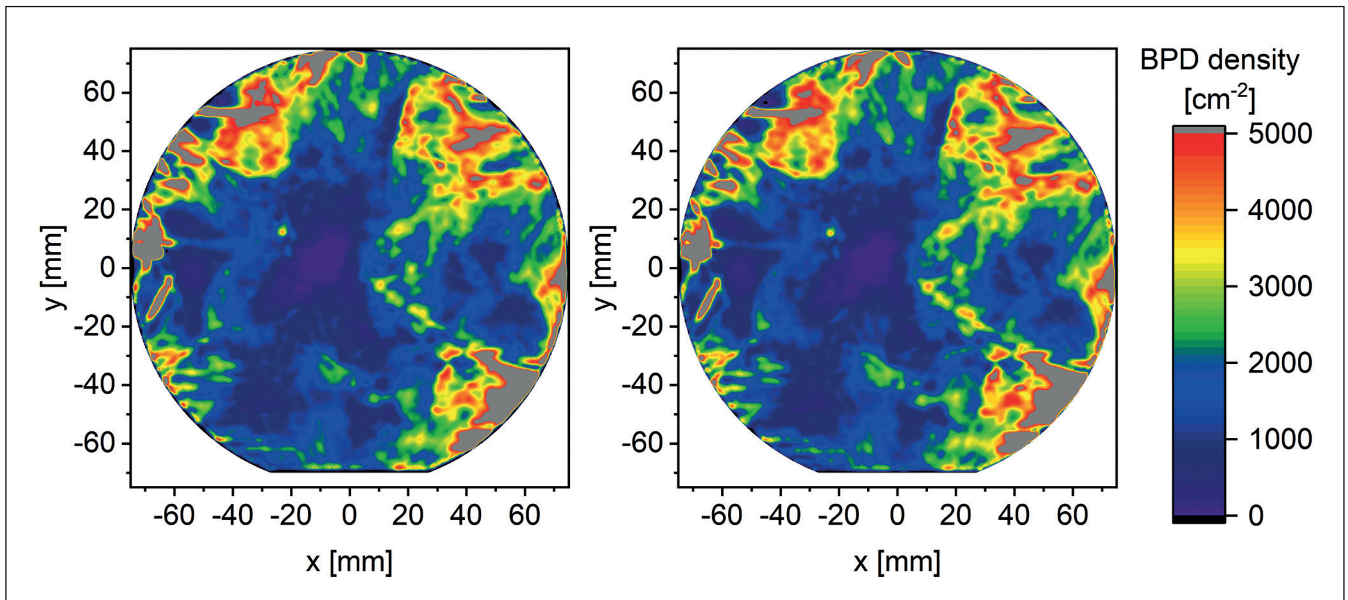


Figure 4. BPD density distribution obtained by X-ray topography. Left plot: Measurement using the standard XRTmicron setup, requiring a measurement time of about 1 hour. Right plot: Measurement of the same wafer in only 5 minutes using the FastBPD setup. The mappings are essentially identical, both qualitatively and quantitatively.

as lines in the topogram, and they start to overlap at moderate densities, due to their extended shape. Thus, it is hard to tell where one BPD starts and another ends (see Figure 3).

Another impediment is that the visibility of BPDs using surface-sensitive measurements in a reflection geometry is poor, even for extremely long measurement times. Thus, switching to a transmission geometry is beneficial from a measurement point of view, but brings another challenge: then it is not clear whether a single BPD actually intersects with the interface, resulting in an etch pit.

We overcame these problems with a calibrated, integral approach. Rather than trying to measure the length of visible lines or count them, not knowing whether or not they intersect with the surface, we pursued an approach where we start by analysing local areas and generating a value of arbitrary unit for each region. We have shown that the values we obtain are proportional to the actual BPD density, measured by etch pit counting. Thanks to this relationship, a calibration curve allows us to generate BPD density mappings that reproduce the corresponding BPD etch pit density very well.

Again, industry acceptance has required proof of the accuracy of our new technique. Helping with this endeavour are our findings from a study of wafers from almost all major SiC manufacturers. After XRT measurements, we undertook potassium hydroxide etching on all these wafers and discovered some wonderful news – the calibration curve is the same for all manufacturers. The implication is that the calibration curve of one wafer can be used for evaluating another. Therefore, the calibration procedure only requires an initial calibration with a single, suitable wafer, or possibly a small set of them. Afterwards, the calibration curve can be used over and over again. Drawing on this, we have determined that the accuracy of the BPD density is more limited by the quality of the etch pit data used as input for calibration than by the XRT measurement itself.

While this routine is robust against material variation, there is a drift over time, similar to that found when performing alkaline etching. However, we have been able to address this concern by quickly developing a recalibration routine. We have shown that by measuring a recalibration wafer alongside the sample wafers, it is possible to significantly enhance the reproducibility of this approach.

Next to cost savings, the non-destructive nature of XRT brings a second benefit into play: because you can regularly measure the same sample, as well as monitoring any drift in the system, you can directly fix it. This ensures a third benefit: inter-lab comparisons are now much easier, and can be realised by just exchanging wafers measured in both (or multiple) labs. Due to this, we now view XRT as a more reliable method than potassium hydroxide etching for BPD detection in standard wafers.

...to FastBPD

So far, we have found three drawbacks with BPD detection by XRT. This first is that the lattice curvature has to be homogeneous and rather low in value, roughly not exceeding 10 km^{-1}. This requirement is fulfilled by typical production grade wafers, but not strictly by all wafers available in the marketplace, so there is the possibility for some measurement error. Second – and for the same reason – there's a need for careful alignment of the wafers, as otherwise measurement could

yield unreliable data. Third, which is not actually a problem, but rather refers to a desire described above: if one can measure non-destructively, one wants to do so as quickly as possible.

The good news is that Rigaku recently refined its XRT hardware, creating a modified version of XRTmicron that features a measurement mode called FastBPD. This mode, now available, slashes the measurement time from an already fast 1 hour per 150 mm wafer to an inline-compatible 5 minutes per 150 mm wafer – that's a breakthrough in the industrial application of XRT. Through intensive testing, we have determined that the measurements obtained with this rapid approach to BPD measurement are fully consistent with established process, as well as data provided by etching (see Figure 4). Thanks to this, all of our findings for BPD quantification can be directly applied to FastBPD measurements.

You would expect that faster measurements would have several unwanted side-effects, such as impacting reliability and increasing the importance of sample preparation. But the opposite is actually true for FastBPD: it is almost immune to issues related to wafer curvature, and it can measure the wafers that caused severe problems with the original hardware. According to our tests, the acceptable variation of the offcut is as high as ±0.5° over the wafer area, corresponding to a homogeneous lattice curvature of around 100 km^{-1}, a value that is far from acceptable for any production-grade wafer. Thanks to this, in practical terms the problem of wafer curvature is eliminated completely.

An insensitivity to wafer properties simplifies alignment issues. With FastBPD, one option is to carry out regular alignment, which is far faster than alignment with the original tool. This approach allows the measurement of wafers with a strange curvature, as well as those with off-cut or orthogonal misorientation. Another option, suitable when all the wafers are within a tight spec, is to undertake all measurements without alignment.

It is impressive to see how much progress has been made in so little time with the XRT technique. Go back ten years and dislocation counting by XRT could only be carried out at synchrotron facilities, where lengthy measuring times were mandatory for full-wafer scans. With the appearance of the XRTmicron in the market, measurements have been brought in house, and the time taken trimmed to the hour range, strengths that piqued additional industry interest. Within the last three years there have been new milestones, with our launch of tools that make this technique better-suited to industry, by offering robust measurements and the capability to count TSDs and BPDs. Now, thanks to the introduction of the FastBPD, a full 150 mm wafer measurement and analysis takes just 5 minutes, giving those that work within the SiC industry the support they need to drive the revolution in power electronics.

Center of expertise for X-ray topography

IN 2021, Rigaku Corporation and Fraunhofer IISB established the Center of Expertise for X-ray Topography in Erlangen, Germany. This facility has been formed to help the semiconductor industry improve and better understand wafer quality and yield, through the use of Rigaku XRTmicron advanced X-ray topography equipment.

Industry benefits from this recent research venture, which combines the competences of the X-ray instrumentation manufacturer Rigaku with the know-how and research network of Fraunhofer IISB, an institute with expertise in semiconductor manufacturing and processing. The partners at Fraunhofer IISB are particularly knowledgeable in the field of crystallographic defects, their occurrence and their impact on device performance – this is a topic of great importance.

One of the roles of Fraunhofer IISB is to develop, test and evaluate analysis routines for detection and quantification of crystallographic defects in single-crystal semiconductor wafers, before transferring these procedures to industrial application. The researchers are also establishing a common language (standardisation) for the detection and quantification of crystallographic defects in single-crystalline semiconductor wafers using XRT.

In general, the Center of Expertise for X-ray Topography acts as a tool demonstrator, performing service-oriented measurements with short feedback loops, and as a competent R&D partner.

Inauguration of the Center of Expertise for X-ray Topography with Michael Hippler (right), President of Rigaku Europe SE and Martin März, Member of the Board of Directors at Fraunhofer IISB, unveiling a new X-ray topography tool.

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Multi-dimensional power devices

Advancing power electronics is not all about new materials. Architectures really matter, with the likes of superjunctions, multiple channels and multiple gates offering the opportunity to revolutionise power devices

BY YUHAO ZHANG FROM VIRGINIA TECH

POWER ELECTRONICS is key to realising high-efficiency energy conversion in various applications, including data centres, electric vehicles, electric grids and renewable energy processing. The global market for power semiconductor devices and ICs is already worth $40 billion per annum, and it is rapidly increasing.

Many working in this sector hold the belief that to advance power devices there's a need to introduce new materials. Transistors made from silicon should be replaced by those made from wide-bandgap semiconductors, such as SiC and GaN, and there will come a time when it's right to move on to ultra-wide-bandgap variants, such as Ga_2O_3, AlN and diamond.

But my view, shared by colleagues including Florin Udrea of the University of Cambridge and Han Wang of the University of Southern California, is that innovation in device concept and architecture is equally important – and such innovation is material agnostic. This has led us to publish a roadmap late last year for device architecture innovation (for the details of that paper, see Further Reading).

History supports our position. Just track the evolution of silicon power devices before the advent of wide bandgap materials. During that era, innovation in device architecture drove the development of power electronics, from the commercialisation of thyristors in the 1950s to the power MOSFETs of the 1970s and the insulated gate bipolar transistors (IGBTs) of the 1980s. We believe that a new wave of power devices hinges on the introduction of multi-dimensional architectures.

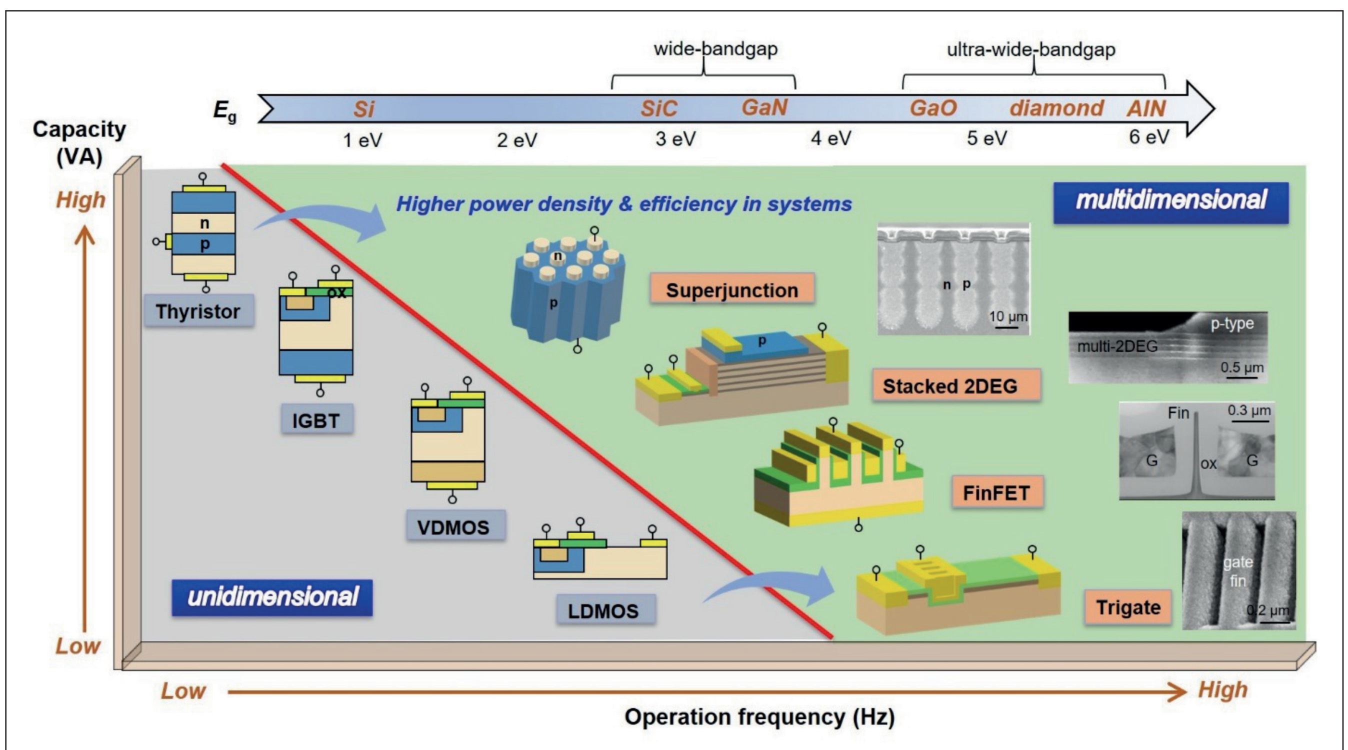

Figure 1. Power capacity and frequency trade-off of 1D and multi-dimensional power devices.

The role of the power device is to conduct a high current in its on-state, block a high voltage in its off-state, and be capable of continuously switching between these two states at a high frequency. For conventional power devices, such as MOSFETs and IGBTs, the main current flow and the blocking electric field are aligned in same direction, rendering them as effective uni-dimensional devices.

Recently, several innovative architectures have been developed that introduce electrostatic engineering in at least one additional geometrical dimension. Such architectures include super-junctions, multiple channels and multiple gates. Depicted in Figure 1, these multi-dimensional devices overcome the capacity-frequency trade-off that holds back the performance of their conventional cousins, enabling them to realise a lower power loss and a higher frequency. Armed with these attributes, designers can enhance the efficiency of their power electronics systems, while reducing the form factor.

Unipolar power devices are also hampered by another trade-off that fundamentally limits their performance: the relationship between the breakdown voltage and the specific on-resistance. As shown in Figure 2, when multi-dimensional devices are made in silicon, SiC and GaN, they can surpass their respective 1D material limits. What's particularly encouraging is that their performance can be continuously enhanced by scaling certain structural parameters. This has spawned a new band of device limits, beyond the 1D limit line for each material. In stark contrast, most 1D unipolar power devices gain little improvement with geometrical scaling. Hence, there's a compelling need to re-write the performance limits and the figures of merit for multi-dimensional power devices.

For superjunction devices, the electric field is modulated in a plane that's perpendicular to the direction of current conduction. This class of power device is formed by creating alternating *n*-type and *p*-type regions. Charge balancing leads to a uniform electric field and a superior blocking voltage, regardless of the doping in each region. With this architecture, the doping level can be increased by orders of magnitude, slashing on-resistance.

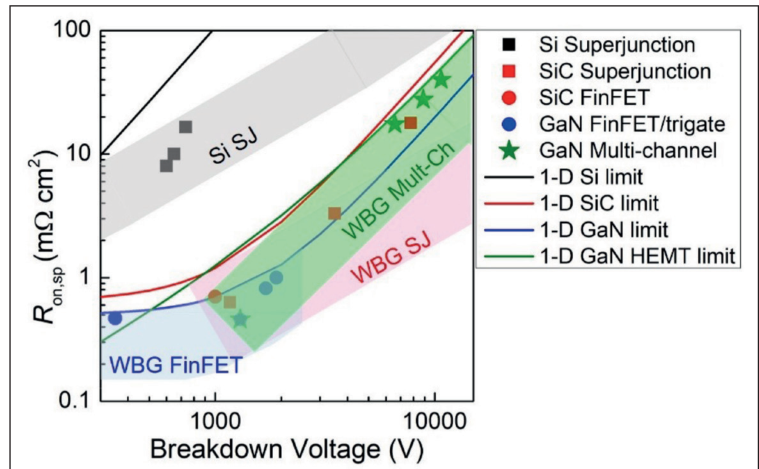

Figure 2. Specific on-resistance and breakdown voltage trade-off of 1D material limits and multi-dimensional power devices demonstrated in silicon and the wide-bandgap semiconductors SiC and GaN.

Since the introduction of CoolMOS in the late 1990s by Siemens, now Infineon, the silicon superjunction has been a spectacular commercial success. And in 2016, the superjunction family welcomed a new member, in the form of SiC, with this device exceeding its 1-D performance limit.

For GaN, breakthroughs coming from the introduction of new architectures have included the development of devices with multiple two-dimensional carrier channels aligned perpendicular to the plane of current conduction. In such devices,

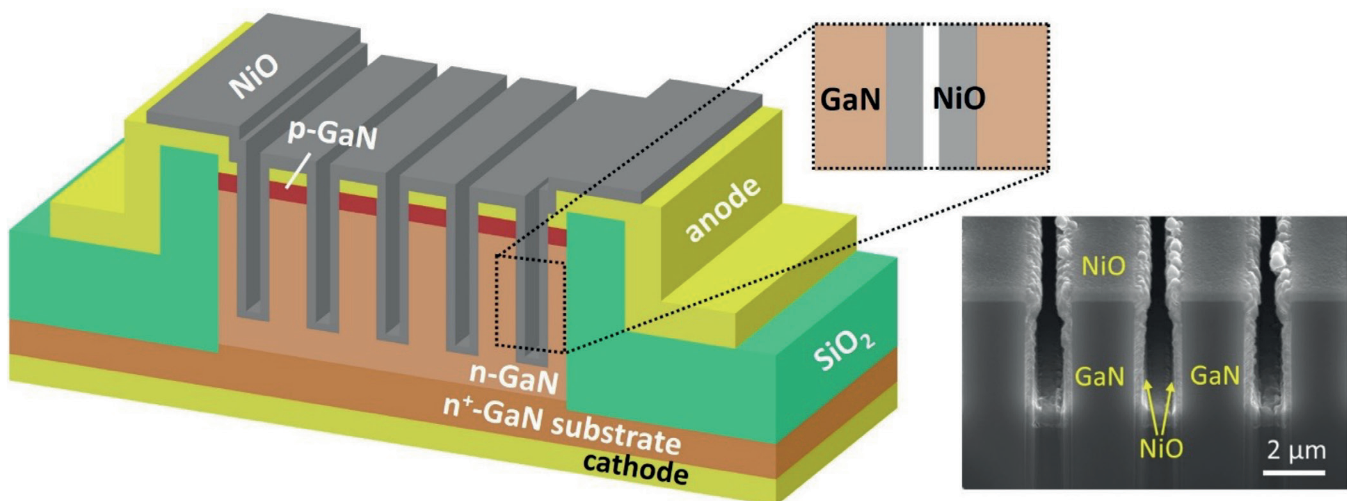

Figure 3. 3-D schematic of the vertical GaN superjunction diode and the zoom-in illustration of a NiO/GaN unit-cell (left). Cross-sectional scanning electron microscopy image of the superjunction region (right).

the polarisation charges, as well as a possible additional *p*-type cap layer, can be self-balanced in the device off-state, fulfilling a functionality similar to that of a superjunction. Using this approach, our teams at Virginia Tech, University of Southern California, and University of Cambridge, have demonstrated multi-channel AlGaN/GaN devices blocking 10 kV, a performance that exceeds the limit of 1D lateral GaN devices.

For transistors operating below a kilovolt, the channel resistance can dominate the device's on-resistance. To slash resistance, device designers can turn to multi-gate architectures and submicron fin-shaped channels. The fin is a particularly attractive option, as it shifts carrier transport away from the low-mobility surface channel, thereby increasing the overall channel mobility.

This approach is widely applicable, with trigates and FinFETs demonstrated in various power transistors, including MOSFETs and HEMTs, using multiple materials.

Late last year, working with additional collaborators, our teams broke new ground, unveiling the first vertical superjunction in GaN. This success, unveiled at the 2022 International Electron Devices Meeting, builds on the heterojunction with *p*-type NiO, which was sputtered conformally on the sidewalls of the GaN pillars (see Figure 3). Thanks to charge balancing between NiO and GaN, our superjunction provides a blocking voltage of 1100 V and a specific on-resistance of 0.15 mΩ cm^2. This level of performance exceeds the 1D limit for GaN.

While we have illustrated the benefits of multi-dimensional architectures to power devices, the gain they can deliver can also be enjoyed elsewhere. For radio-frequency devices, they can deliver improvements in power, frequency, and dynamic range.

Note that we are not disputing the benefits that can be wrought be introducing new semiconductor materials. But the next time you need to build a better device, don't just think about switching materials – also consider what might be possible with a refined architecture.

FURTHER READING

- Y. Zhang *et al*. "Multidimensional device architectures for efficient power electronics," Nat. Electronic. **5** 723 (2022)
- M. Xiao *et al*. "First demonstration of vertical superjunction diode in GaN," 2022 International Electron Devices Meeting (IEDM), 35.6, Dec. 2022.

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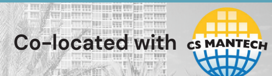

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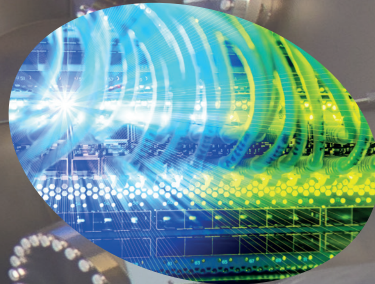

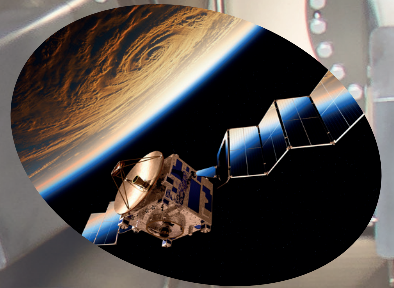

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Sterilising with far UVC

A revolutionary short-period superlattice holds the key to high-performance LEDs emitting deep within the UVC

BY WILLIAM LEE AND LIAM ANDERSON FROM SILANNA

ONE OF THE lasting legacies of the pandemic is an increased interest in establishing efficient ways to deactivate harmful micro-organisms. Of the many options available, one that has received a tremendous amount of attention is UV sterilisation, especially in the form of the UV LED. This source offers a compact form factor, a chemical-free nature and high germicidal efficiency. However, UV LEDs come with a severe health warning: sterilisation based on most of these sources is inherently dangerous for everyday consumer use, due to the damaging effect of UVA, UVB and UVC radiation on skin and eyes.

Fortunately, there's a solution, involving heading further into the UVC. According to a number of recent studies, when UV light is shorter than 240 nm, it is fully absorbed by our *stratum corneum*, the outermost layer of skin, which is 10-40 μm-thick and made up of dead cells. Due to this, light in the far UVC deactivates viruses and bacteria, but does not penetrate the shield of dead cells, so is ideal for sterilisation, because it leaves healthy cells unharmed and safe from damage.

Drawing on this insight, in 2020 *The American Conference of Governmental Industrial Hygienists* issued a *Notice of Intended Change*, which proposed an increase in the exposure limit to 8 hours, for skin and eyes subjected to UV light with a wavelength less than 240 nm. This move propels far-UVC LEDs into the spotlight, as successful commercialisation of high-power sources based on this device would enable effective sterilisation tools in homes, on public transport and on planes. Implement this strategy and when the next pandemic arrives, far UVC LEDs could provide the best weapon in our defence.

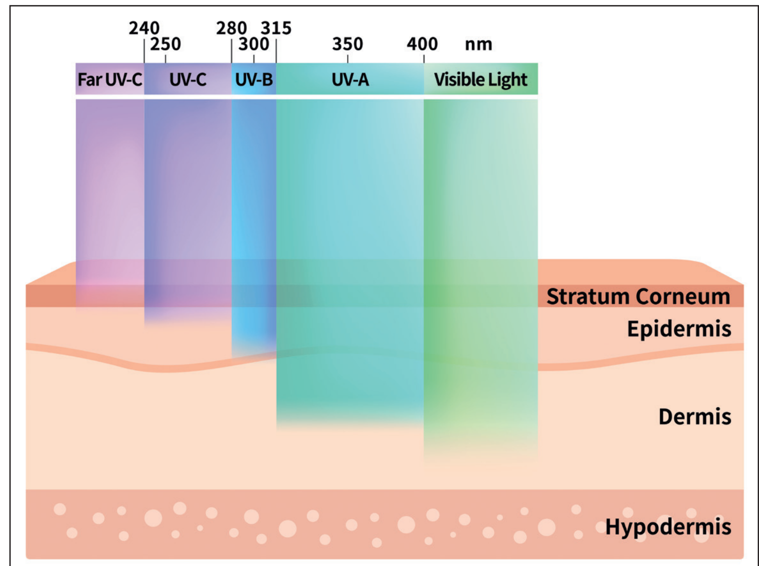
Making far-UVC LEDs

Unfortunately, stretching the emission of the LED to the far-UVC is far from easy. Ever since Nobel prize winner Shuji Nakaruma generated *p*-type doping in GaN and demonstrated the blue LED, researchers have been developing LEDs that emit at shorter and shorter wavelengths. Realised by increasing the aluminium content in AlGaN ternary alloys, this has led to the manufacture and commercialisation of LEDs emitting in the UVA, the UVB, and more recently, the UVC. However, there is a roadblock at 260 nm, due to an inherent and unique property of the AlGaN material system that is hampering the production of high-power, efficient LEDs emitting in the far-UVC.

The inherent drawback of AlGaN comes from its bandstructure at high aluminium content. For this alloy, the valence band is split into the heavy hole, light hole, and spin split-off sub-bands, with an ordering that depends on various physical parameters of the ternary alloy. For a low aluminium content, the heavy-hole band is the top-most band, with the majority of electron-hole recombination taking place between the conduction band and the heavy-hole band. When this happens, this transition is polarised in a way that favours vertical optical emission, corresponding to transverse electric polarisation, an orientation that assists the coupling of light out of the structure.

Once the aluminium content in AlGaN passes a critical juncture, the ordering of the bands flips, with the top-most band becoming the spin split-off band. This band is unique – unlike the other two, its optical transition is dominated by transverse magnetic polarisation. Light with this form of polarisation has an escape cone that's parallel to the surface. This orientation increases total internal reflection, and causes more of the light that's generated within the structure to be trapped and unable to escape. For far-UVC LEDs emitting below 240 nm, the aluminium content is beyond this cross-over point, making the extraction of light a substantial challenge.

Unfortunately, this is not the only difficulty that's encountered when heading deeper into the UVC. The higher bandgaps found in this domain hamper the provision of free electrons and holes, the ingredients for the light-generating recombination process. In GaN-based LEDs operating at longer wavelengths, free electrons and holes tend to be provided by *n*-type and *p*-type dopants, respectively. As these impurities often sit at states close to the conduction band and valence band, they can generate free electrons and holes easily at room temperature. But for higher bandgaps, such as those required for the far-UVC, the two bands are so far apart that it is a challenge to find suitable impurities capable of providing states close enough to the conduction band and valence band. This fundamental limitation of wide bandgap semiconductors is another obstacle to realising efficient, far-UVC LEDs.

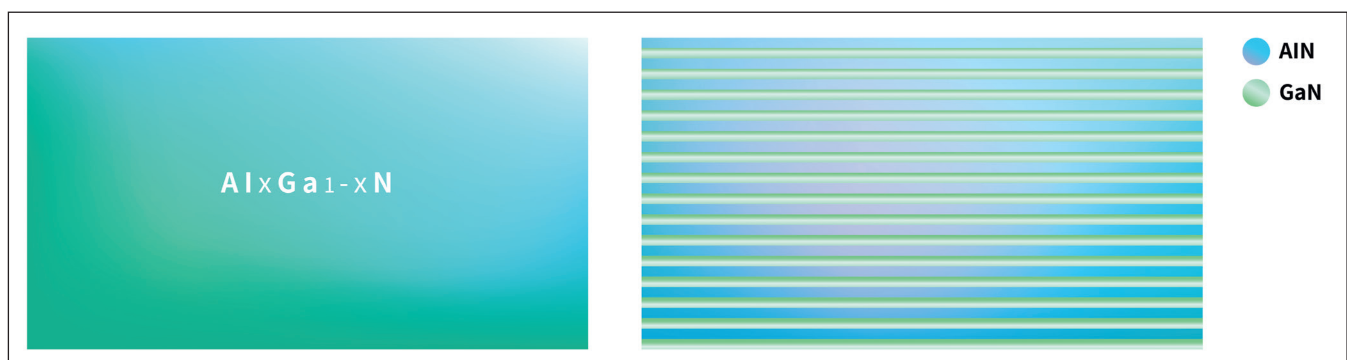


➤ Figure 1. When UV light shines on our skin most is absorbed while some is reflected. Absorbed UV penetrates deep into our skin, where it is scattered and absorbed by our cells, causing damage. However, if the wavelength of the incident light is in the far-UVC range, it does not penetrate past the *stratum corneum*, a layer of dead cells protecting living skin cells. Consequently, UV light in this region is safe for our skin. For similar reasons, the same wavelength range is safe for our eyes.

The strength of the superlattice

To overcome these problems and make LEDs that emit in the far-UVC, our team at Silanna of Brisbane, Australia, is pioneering the production of devices employing binary AlN/GaN short-period superlattices. With this modification, we avoid the light polarisation and doping issues that plague equivalent composition AlGaN devices. This unlocks the door to high-power far-UVC LEDs, which could be used for skin and eye-safe personal sterilisation.

Superlattices are structures with alternating materials, repeated many times. As its name



➤ Figure 2. Silanna overcomes most issues surrounding the traditional bulk AlGaN material (left) that limits far-UVC emission by replacing this alloy with a short-period superlattice consisting of alternative layers of AlN and GaN, each with a thickness of the order of monolayers (right).

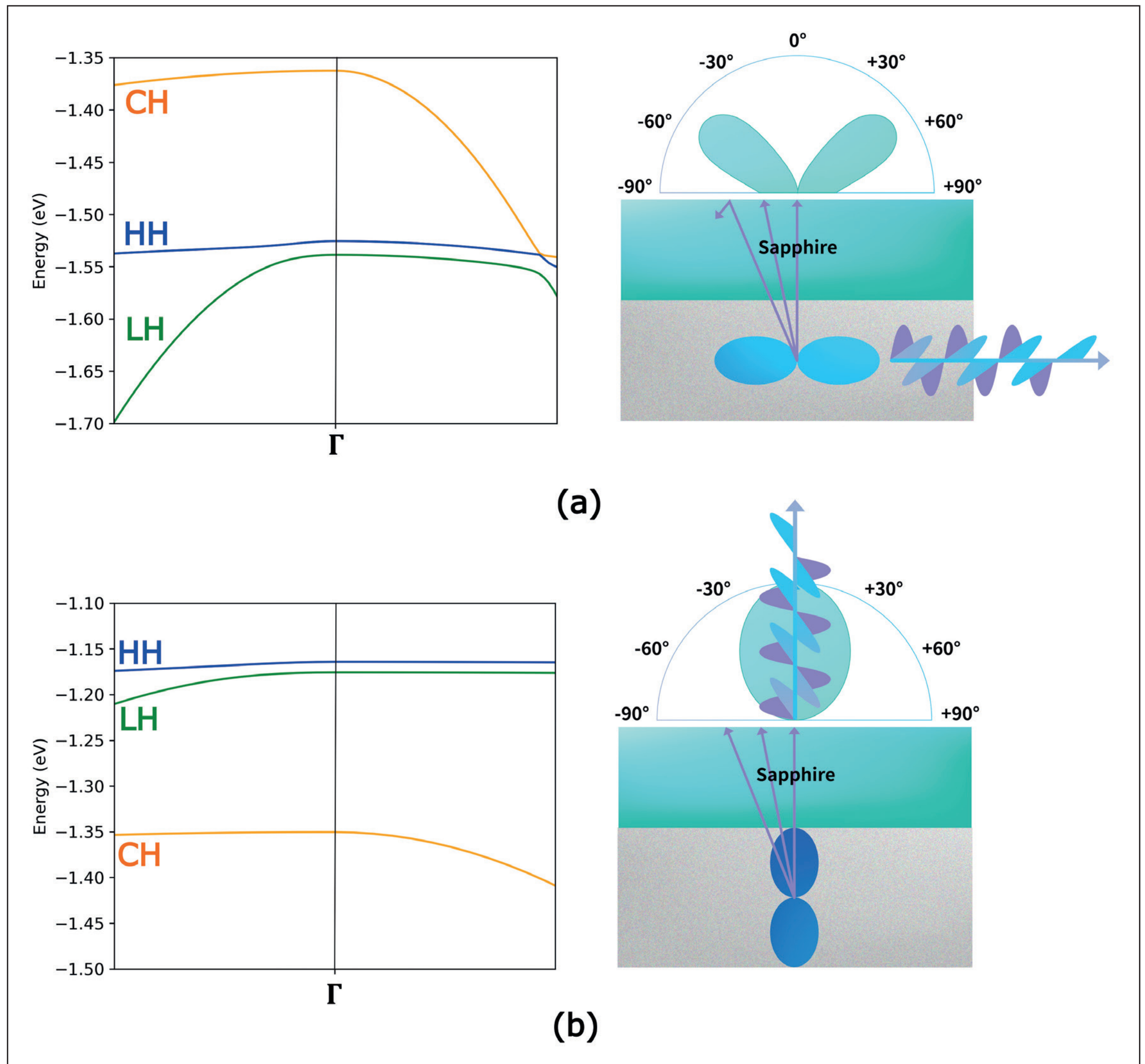
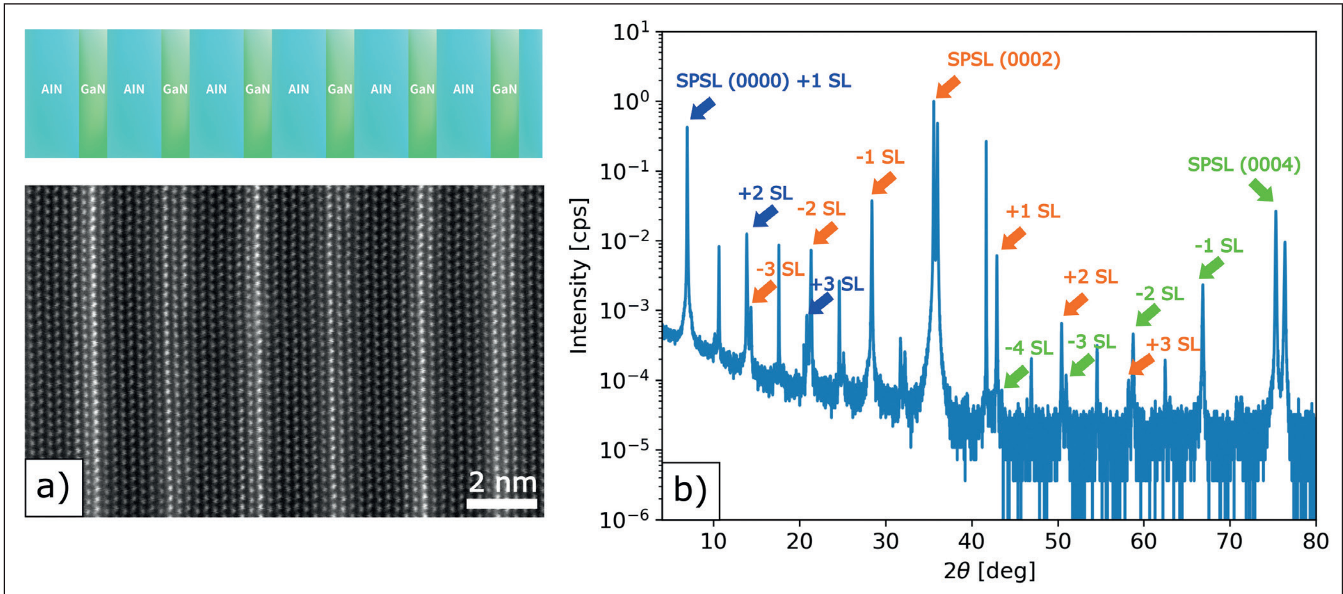


Figure 3. (a) The valence band ordering of $Al_{0.8}Ga_{0.2}N$, showing that the spin split-off (CH) band is at the top of valence band at the gamma point (left). The CH band promotes emission with an optical dipole that is parallel to the surface, resulting in reduced centre irradiance and poor light extraction from the top/bottom surface (right). (b) The valence band ordering of a 1ML:4ML GaN/AlN short-period superlattice, which has an equivalent aluminium content of $Al_{0.8}Ga_{0.2}N$. The effect of the short-period superlattice is to put the heavy hole (HH) and light hole (LH) band above the CH band, resulting in emission with optical dipoles perpendicular to the surface. This allows a strong centre irradiance to be maintained, with most of the emitted light able to escape the structure.

suggests, in a short-period superlattice, the period of each set of repeating layers is very small – of the order of angstroms to a few nanometres. By using a short-period superlattice with layers just a few atoms thick, we alter the conduction and valence bands to such an extent that the resulting structure is essentially a new material, different from both its constituent layers and the equivalent AlGaN material. This entity, formed from a stack of hundreds of periods of AlN and GaN layers, is ideal for making a far-UVC LED, because it tackles light extraction and conductivity problems head-on.

In the active region of our device, we sandwich thin GaN 'well' layers between AlN 'barrier' layers. The quantum confinement that results creates high-energy occupied states within GaN that are dependent on its thickness. Due to this, despite the relatively low bandgap of GaN, its thickness can be tuned to generate states emitting in the far-UVC.

What's more, the sub-band ordering of GaN is maintained in the valence band of the short-period superlattice, due to the way that regularly incorporated gallium-atoms modify the crystal structure, no matter the thickness of the GaN well or the effective aluminium content. This means that far-UVC emission obtained from the active region of our devices is predominantly transverse electric



➤ Figure 4. (a) Transmission electron microscopy image of a typical short-period superlattice, showing layers of AlN (dark) and GaN (bright). This atomic scale image shows that the constituent layers are distinct, with well-defined interfaces, confirming the high quality of the short-period superlattice. (b) X-ray diffraction ω-2θ scan of a typical short-period superlattice, showing a wealth of satellite peaks. The observation of high-order satellite peaks for multiple reflections (colour coded) underscores the extremely high quality short-period superlattice produced by the Silanna process.

– a vertically directed emission that can escape the structure far more easily.

Another strength of our design is that the GaN well within the short-period superlattice aids the generation of free holes and carriers. This benefit arises because the conduction bands of the wells are significantly closer to the dopant impurity levels, compared with their AlGaN counterparts. Thanks to this, our devices offer a route to ionising impurities at room temperatures, thus providing free carriers.

The other significant advantage of our architecture is that by keeping the AlN barriers thin, our repeating short-period superlattice enables quantum tunnelling through electrically active layers, improving electron and hole injection into the active area. Our wells offer a significantly improved recombination efficiency, because they are thin enough to significantly increase carrier overlap in the emitting areas, by reducing the quantum-confined Stark effect despite the strongly polarised lattice of GaN and AlN.

Merits of MBE

Due to the precise thickness control required for making a III-N short-period superlattice, we do not produce our devices by MOCVD, the most common approach for making GaN-based LEDs. Instead, we use MBE, a kinetic non-equilibrium process that's frequently used at the forefront of material research. With this form of epitaxy we can realise precise thickness control and produce high-quality short-period superlattices featuring barriers with monolayer thickness and wells with abrupt interfaces.

Our far-UVC LEDs are produced using the only production-grade nitride MBE system in the southern hemisphere. With this tool we can deposit highly uniform short-period superlattices on 150 mm sapphire substrates with a thickness accuracy within a single layer of ±0.2 monolayers.

According to X-ray diffraction ω-2θ scans, our short-period superlattices are of excellent quality. This is evident by the number of characteristic satellite peaks, as well as their intensity and sharpness.

➤ Figure 5. Heterostructure for Silanna LEDs, utilising the short-period superlattice through almost the entirety of the device stack.

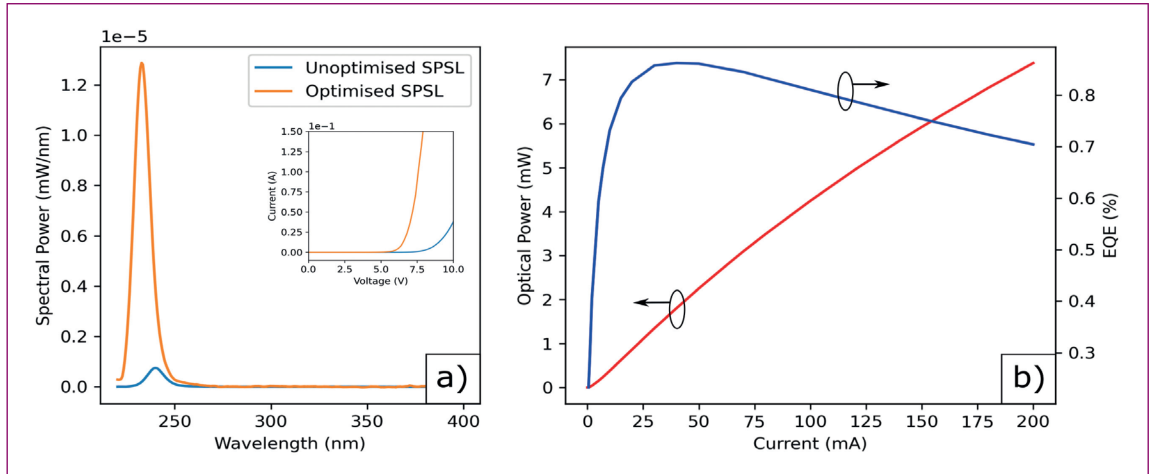


Figure 6. (a) Electroluminescence spectrum of Silanna far-UVC LEDs, showing an over-20-times improvement in emission output after optimisation of the short-period superlattice. The inset shows the effect of optimisation on the electrical properties of the LED, including a reduction in the operating voltage at 200 mA to below 7.5 V. (b) Wafer-level plots of output power versus current, and external quantum efficiency versus current, of one of Silanna's best dies emitting at 235 nm. Measurements show a power of over 7 mW at 200 mA, and a maximum external quantum efficiency of over 0.8 percent.

Confirming the structural perfection of our epilayers is transmission electron microscopy, which reveals the abrupt interface of alternating layers of AlN and GaN.

As expected, and unlike AlGaN, our short-period superlattice is capable of high *n*-type conductivity, using silicon as a dopant. Resistivity measurements reveal that for a structure with an aluminium content equivalent to $Al_{0.8}Ga_{0.2}N$, resistivity is just 0.015 Ω cm. This value is significantly lower than that reported by others for $Al_{0.8}Ga_{0.2}N$, underscoring the doping benefits of our short-period superlattice technology.

To fully exploit the merits of our short-period superlattice, this structure features in almost the entirety of our LED. Producing such a device poses unique challenges, including those related to carrier transport. The ease with which carriers quantum tunnel through our short-period superlattice is

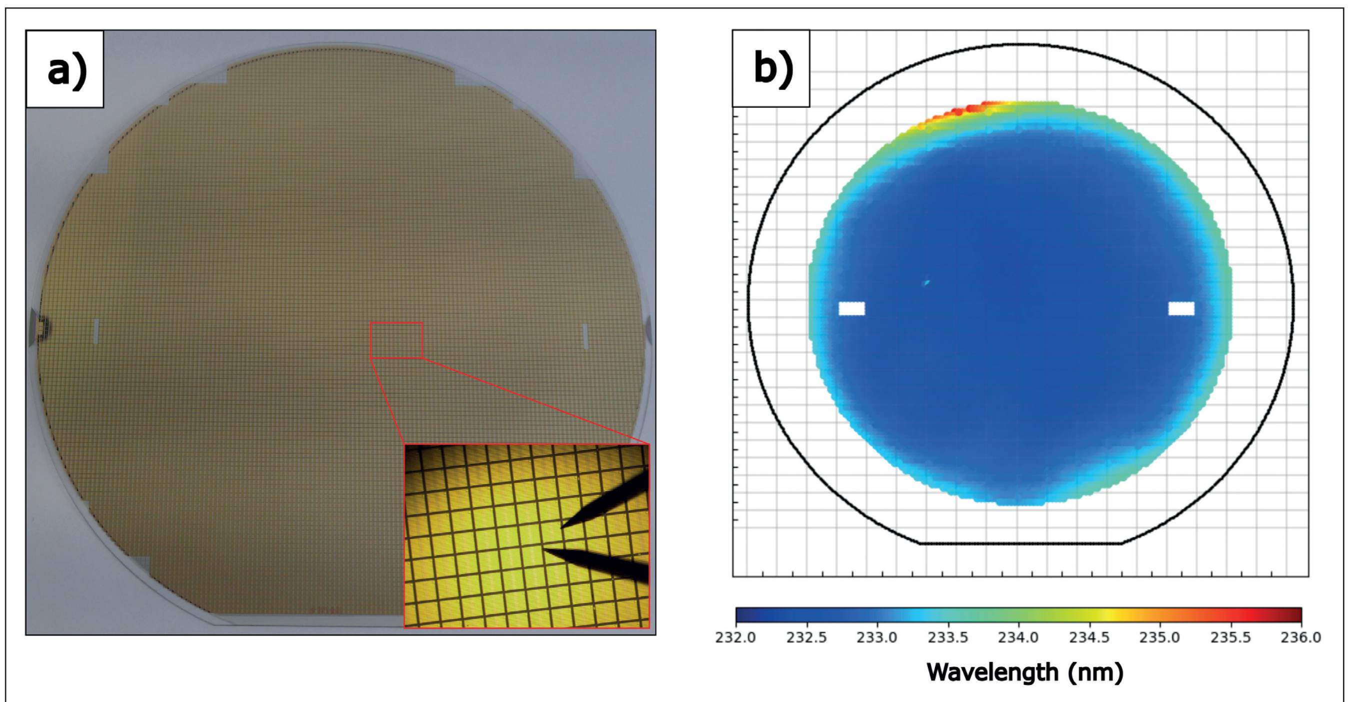


Figure 7. (a) Silanna's 150 mm wafers are fully utilised, with over 10,000 die fabricated from each wafer. (b) The uniformity of the 150 mm MBE process ensures that the majority of die produced within one wafer run have very similar properties. For example, the wavelength variation is typically only a few nanometres across the majority of the 150 mm wafer.

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With the passing of the CHIPS Act, a blueprint to advance US semiconductor manufacturing competitiveness is needed now more than ever. More than 80 industry leaders, educational institutions and public sector leaders from states around the nation came together to collaborate and develop the **National Semiconductor Economic Roadmap**. The first-of-its-kind roadmap identifies goals and objectives across four critical pillars: infrastructure, supply chain, workforce, and entrepreneurship to ensure global competitiveness. Now, it's yours.

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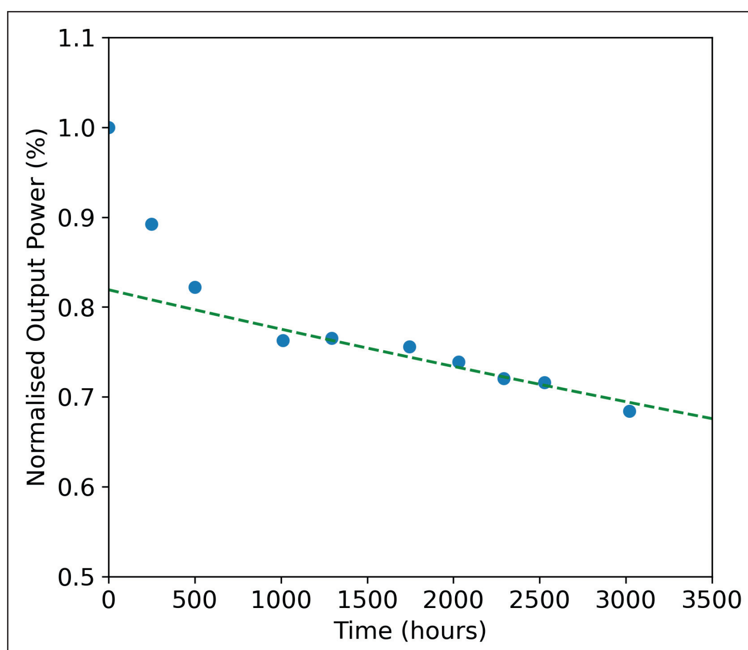

Figure 8. As per the IES standard TM-21, the L70 lifetime of Silanna's product has been evaluated using an average normalised output value, observed over 78 samples. The resulting L70 is 2500 hours with a similar B50L70 value. It is expected that the die lifetime can be further extended using a pre burn-in procedure.

both a blessing and a curse: it enhances carrier injection into the active region, but also promotes carrier overshoot into the doping layers, cutting recombination efficiency. However, it is possible to balance carrier injection and carrier overshoot by carefully designing the electron-blocking layer, which sits between the active layer and the p-layer. In our short-period superlattice structures we can enjoy a similar outcome by adjusting the thicknesses of barrier and well, to tune the degree of quantum tunnelling through the device.

Before we optimised our device, we produced a benchmark with an arbitrary short-period superlattice that had been shown to emit at the correct wavelength. Driven at 8.5 V, this far-UVC LED emitted 0.03 mW at 20 mA.

We have optimised our device structure by: increasing the barrier width in the active layer, so that this strikes a balance between electron injection and overshooting into non-active regions; using an *n*-doped layer with barrier and well-widths optimised to strike a balance between carrier transport and optical properties; and employing a short-period superlattice with an optimised grading profile as an additional electron-blocking layer. These improvements have increased the output power of our die by almost 20-fold while maintaining a low drive voltage. Our latest far-UVC 235 nm sources typically operate below 7 V at 20 mA, which is lower than comparable products on the market. For this drive current, output power is typically 0.7-0.8 mW, higher than most commercially available far-UVC LEDs. Through further improvements to device design and process, we have even demonstrated an output power of 7 mW at 200 mA, for a 235 nm LED at the wafer level. This is the highest value ever reported in this wavelength range, realised for a device operating at just under 8 V.

The added bonus of our uniform 150 mm wafer process is that we produce many die within a single run. Right now, we can make over 9,000 die that pass our product specs from a single wafer. Note that every one of them has a wavelength within a few nanometres of our target.

One of the merits of producing a large number of die is that it allows us to properly evaluate product reliability. This assessment shows that our far-UVC LEDs are more reliable than most on the market. Results from more than 160 die show an L70 lifetime of over 2000 hours, using TM-21 valuation. A significantly longer lifetime is possible after burn-in.

Currently, we have established two product lines based on our short-period superlattice technology – the far-UVC 235 nm SF1 series we demonstrated here, and the deep-UVC 255 nm SN3 series. This portfolio provides the perfect solution for various deep and far-UV use cases, such as water sterilisation, sensing, and instrumentation applications.

However, the promise of the short-period superlattice extends beyond just these opportunities. Due to the unique nature of this technology, it is easy for us to produce LEDs of any wavelength in the deep to far-UVC, using the same process and a simple adjustment in thickness. This allows us to target new applications requiring UV emitters at wavelengths currently unavailable, such as those within the 240-250 nm range.

In the near future, we will focus on further optimisation and improvement to the two existing wavelength ranges, and push the boundaries to realise even higher output powers in the far-UVC region below 230 nm. Supporting such efforts is our recently commissioned brand-new production facility in Brisbane, Australia, featuring state-of-the-art equipment and facilities – this will aid us in our goals of developing new technologies and processes. Further foundations supporting tomorrow's success are our ISO90001 certification and our long history in electronics production and manufacturing. Thanks to all these attributes, we are perfectly positioned to turn our next technology breakthrough into brilliant products for our customers.

FURTHER READING

- ACGIH 2021 TLVs and BEIs: Based on the Documentation of the Threshold Limit Values for Chemical and Physical Agents & Biological Exposure Indices; American Conference of Governmental Industrial Hygienists: Cincinnati, OH, 2021

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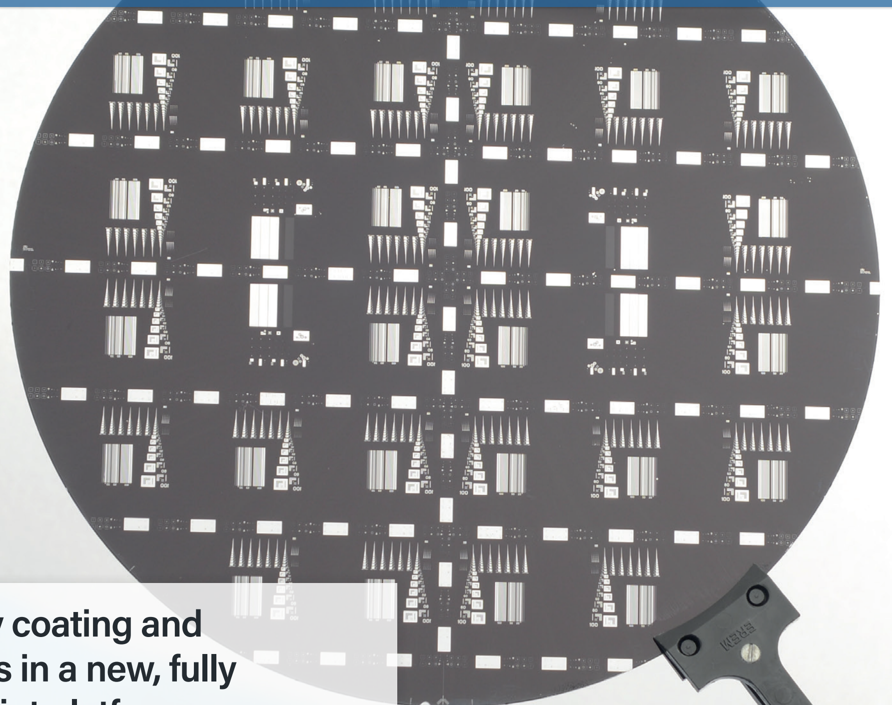

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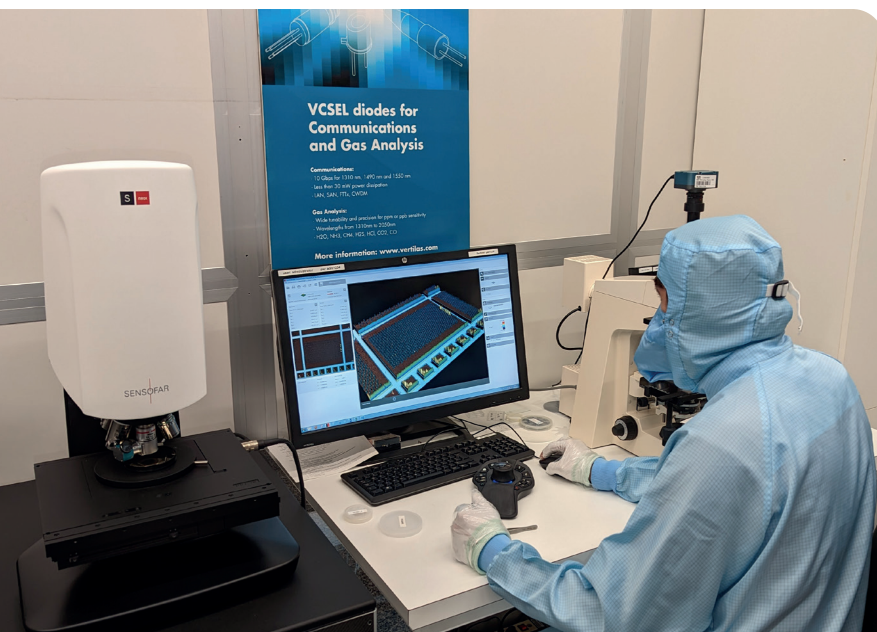
Multiple opportunities for long-wavelength VCSELs

Propelling VCSEL emission further into the infra-red with InP-based designs creates lucrative opportunities in data transmission and sensing markets

BY CHRISTIAN NEUMEYR FROM VERTILAS

TWO DECADES of substantial sales have helped to establish the VCSEL as a mainstream laser technology. Initial success came from short-reach optical communication, with devices emitting at 850 nm enjoying widespread deployment in data centres. And more recently, 3D sensing has become the ultimate killer application for VCSELs, such as 940 nm variants that enable facial recognition in many models of smartphones.

Additional opportunities are now emerging further into the infra-red, particular for wavelengths between 1.3 μm and 2.3 μm, where VCSELs can offer an attractive alternative to edge-emitting lasers. VCSELs that operate in this spectral range can provide eye-safe sources for sensing, and find applications in optical networks, where they draw far less power than the incumbents, enabling high-density multi-channel interconnects.



At Vertilas of Garching, Germany, we are ideally placed to capitalise on these new opportunities. We have more than 20 years of experience in producing lasers, including tremendous expertise in the manufacture of InP-based VCSELs that emit at longer wavelengths within the near infra-red.

Following the launch of our company in 2001, we enjoyed initial commercial success from a portfolio of VCSELs for gas sensing, with products covering more than 15 wavelengths from 1.3 μm to 2.3 μm. Since then we have expanded our horizons. More recent breakthroughs include: the development of the fastest 1.3 μm and 1.55 μm single-mode lasers for optical data transmission, delivering 40 Gbit/s data rates in 2017 and 2014, respectively; and the launch of 1.3 μm 2D VCSEL arrays for 3D sensing applications in 2022 (see "Key technology milestones of Vertilas InP VCSELs" for a more detailed account of our triumphs).

The VCSELs and VCSEL arrays that we produce are well suited for applications in data communications and metro networks, which are built around 10, 100, and 400 Gbit/s modules and interconnects. New data centres and infrastructure for fast-growing cloud applications are increasingly based on single-mode fibre transmission, so there is a significant opportunity for sales of energy-efficient long-wavelength sources that meet this criterion.

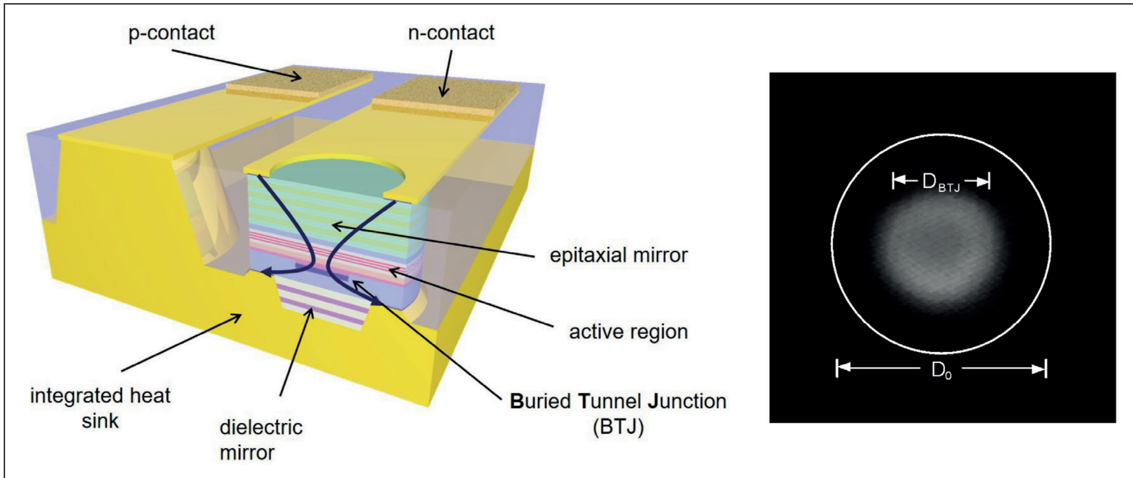


Figure 1. Vertilas' InP BTJ design and BTJ defined active area D_{BTJ}.

Our 10 and 40 Gbit/s VCSELs are strong contenders in this market, combining a single-mode output with ultra-low electrical power consumption – it is less than 20 mW. As VCSELs are also renowned for their small die size and integration capabilities, our devices are ideal for multi-channel grey or multi-colour dense-wavelength-division multiplexing optical interconnects and modules.

As well as eye-safety, our long wavelength 2D VCSEL arrays have additional merits for serving 3D sensing and illumination markets. Whether deployed in robotics or autonomous vehicles, face and gesture recognitions systems or automotive lidar, our sources can help to prevent sunlight interference while ensuring cost-effective small-form-factor packaging.

InP: The essential ingredient

Our VCSELs are notably different from their short-wavelength cousins, which have enjoyed so much success in data centres and facial recognition. Those devices are based on GaAs, a material system that limits the emission wavelength to around 1 µm. Introducing novel alloys, such as the dilute nitride GaInNAs, can allow the output to extend further into the infra-red, with the ceiling raised to 1.3 µm. But there needs to be a radical departure from the norm to span the domain from 1.3 µm to 2 µm, with a switch from GaAs to InP providing by far the best option.

To make this transition, we have addressed a number of key technological challenges. One downside of the move to longer wavelengths is that the distributed Bragg reflector, which requires exceptional reflectivity, is hampered by a lower refractive index contrast between suitable materials and a higher thermal resistance.

Additional challenges include developing an approach to implement reliable, defined current confinement, and to ensure an effective current flow from the active area to the heat sink. Once we addressed these design-related issues, we still had to: demonstrate high-performance, single-mode laser characteristics; realise singlets and 1D and 2D arrays; introduce cost-effective production, assembly and test procedures; and make sure that our VCSELs offered long-term reliability and adhered to industry qualifications, such as those of Telcordia.

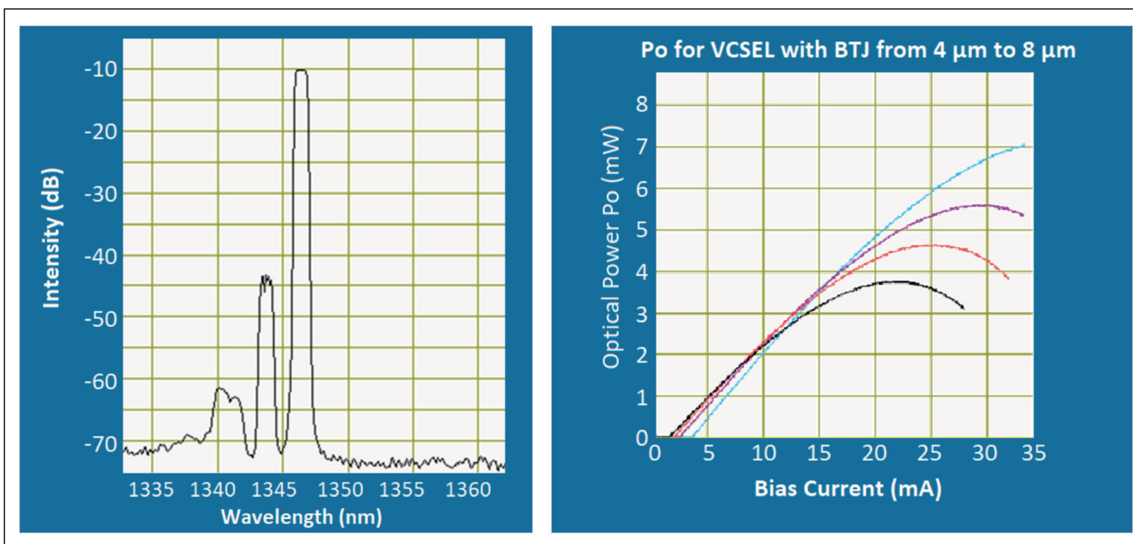


Figure 2. Optical spectrum of a multi-mode VCSEL and output power of the Vertilas single-mode and multi-mode (8 µm) InP VCSELs.

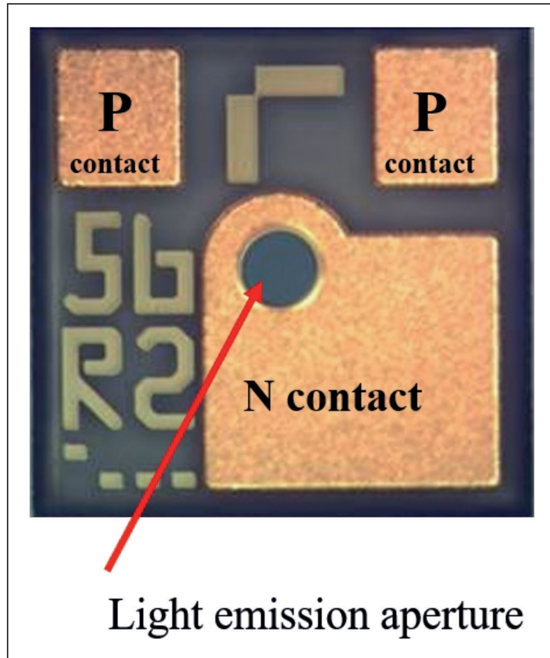


Figure 3. InP BCB VCSEL (top view).

Taking on these challenges led us to create a novel laser design. By implementing a new concept, and integrating innovative device functions, we have realised VCSELs that can perform at up to 90°C.

Initially, we focused on the thermal management of our VCSEL and the design of its active region. While targeting these objectives, we had in mind the need to develop a device with low power dissipation, high performance and long-term reliability. The design that resulted is shown in Figure 1.

If we were to use epitaxial DBRs for the top and bottom mirrors, as is the case with a GaAs VCSEL, this would result in a very 'thick' device. So we combine one epitaxial DBR with a dielectric variant. The epitaxial DBR, which is lattice-matched to the InP substrate, consists of a high number of InAlAs/InGaAlAs mirror pairs, leading to a relatively high thermal resistance. Depending on the target wavelength, we use between 30 and 40 mirror pairs to realise a DBR with a thickness of around 8 μm and a reflectivity of around 99.6 percent. In comparison, GaAs/AlAs DBRs realise the same reflectivity with less than 20 mirror pairs. However, despite the increased effort and the thicker DBRs, it is acceptable to pursue this approach.

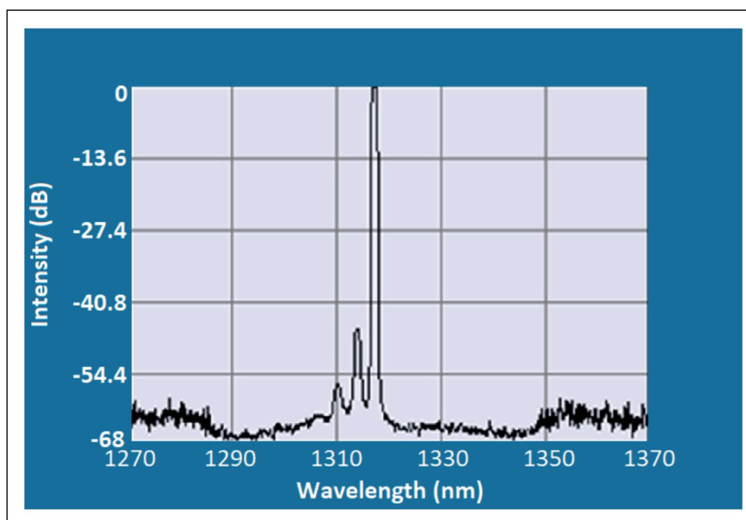


Figure 4. Single-mode VCSEL optical spectrum .

The same cannot be said for the bottom DBR. This mirror requires a reflectivity of 99.9 percent, leading to a total device thickness of potentially 20 μm or more. As well as high production costs stemming from the long epitaxial growth time, such a device would suffer from a compromised thermal performance, due to its high thermal resistance. The hottest spot within the VCSEL is the active region, and it's essential to have a very effective heat flow from there to a heat sink, to prevent the device from overheating. If the VCSEL's operating temperature is too high, this results in inefficient conversion of electrical energy to photons.

Our solution is to use dielectric materials for the bottom mirror. Options for this include the pairing of AlF_3 and ZnS, which have a very high step in refractive index. With this combination we form a bottom mirror with only 3.5 mirror pairs. To ensure excellent thermal management, we also introduce a very effective heat sink structure, created by deploying a plated gold substrate at the bottom of the wafer (and VCSEL). Thanks to the short distance between the active region and heat sink, the heat that's generated within the quantum wells flows effectively to the heat sink, ensuring excellent thermal performance for the VCSEL.

Last but not least, our long-wavelength VCSELs feature a buried tunnel junction (BTJ). This addition enables sufficient current confinement for realising a high energy density in the active region, which consists of a quaternary InGaAlAs material structure that features around five quantum wells.

There is much to be said for using a BJT, rather than an oxide, the common choice for carrier confinement in GaAs VCSELs. One of the strengths of the BJT is that it can be formed after epitaxial growth by means of dry etching, so there's no need for an oxidation step that threatens to degrade the aluminium-containing active region. While there's a need for high-doping to form a tunnel junction, this is well within the capabilities of MBE. And as the BTJ is formed with a well-defined dry etching process step, there's great control over the dimensions of the active area and thus the optical power capabilities of the device (see Figure 2). If high-powers are required, and multi-modes are acceptable, the diameter of the BJT can reach up to 12 μm; but if single mode is essential, the diameter of this junction is typically just 5 or 6 μm.

We produce both single-mode and multi-mode VCSELs. The former results from an optimised waveguide design and judicious selection of the BTJ diameter. Our 1.3 μm InP-based VCSELs provide

a side-mode suppression ratio of more than 40 dB (see Figure 3).

Delivering data

The key requirements for VCSELs for optical data communication are: a high bandwidth, evaluated in terms of the -3dB point of the S-parameter S21; a low power dissipation; a low threshold current; and sufficient optical power at temperatures of up to 90 °C. We have fulfilled all of these requirements by refining the design of our device. High performance comes from using a threshold current of around just 1 mA and trimming the device's intrinsic parasitics. They are lowered by dry etching a semiconductor mesa for each VCSEL on the wafer. Etching reduces the amount of semiconductor material and minimises the capacitance of the device structure. After this step, we fill the voids with benzo-cyclo-butene (BCB), a polymer with low dielectric characteristics.

With this approach we produce InP VCSELs with a S21 3dB bandwidth of up to 12 GHz, which is more than sufficient for 10 Gbit/s applications. These devices, containing BCB and having a 1.3 µm-matched cavity, provide excellent performance at temperatures of up to 90 °C. Evaluating their capability for optical data transmission with the commonly used 'eye measurement', formed by sampling the output of a laser that's directly modulated with a pseudo-bit-rate sequence, reveals an eye mask margin of 42 percent when transmitting data at 10.3 Gbit/s (see Figure 5).

Even higher levels of performance are realised by shortening the length of the cavity. While doing so, we have reduced the photon lifetime by replacing the top epitaxial DBR with a thinner dielectric DBR. These changes, which have led to a reduction in resonator length by around 30 percent, have enabled an increase in the S21 bandwidth to 18 GHz, and a 26 percent eye-mask margin for a data rate of 25 Gbit/s with direct modulation (non-return to zero). With equalisation, data rates as high as 50 Gbit/s can be realised. Through our participation in the EU project PASSION, we have even played our part in demonstrating a concept 2 Tbit/s dense-wavelength division multiplexing transmitter featuring 40 VCSELs, driver electronics and a SiP chip.

Making arrays

When a higher power is needed, the first option is to increase the active area. However, this leads to a transition from single-mode to multi-mode operation, with the introduction of transverse modes (see, for example, Figure 4, which shows three transversal modes). With a multi-mode VCSEL, more

Key technology milestones of Vertilas InP VCSELs

- 2022: 1.3 µm 2D VCSEL array with 800 emitters and 8 W quasi-CW performance
- 2019: Concept of 2 Tbit/s SiP transmitter with 40 VCSELs at 50 Gbit/s
- 2017: 1.3 µm single mode VCSEL with 40 Gbit/s data transmission (NRZ)
- 2014: 1.55 µm VCSEL with 40 Gbit/s optical data transmission
- 2011: Prototype of wide tuneable 1.55 µm VCSEL with 100 nm tuning range
- 2008: 1.3 µm VCSEL for 12.5 Gbit/s optical data transmission
- 2005: 1.55 µm single mode VCSEL with optical power of 1 mW at 80°C
- 1999 - 2001: BTJ VCSELs at 1.3 µm, 1.55 µm and 2.0 µm

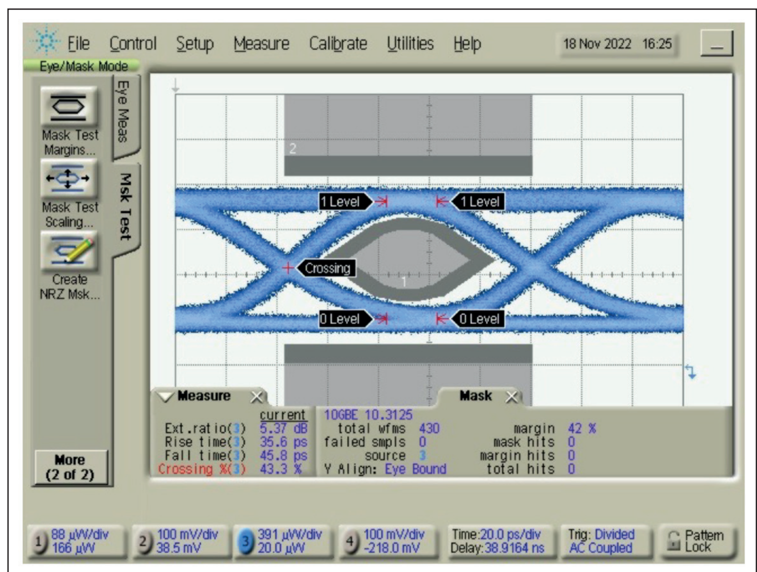


Figure 5. 10 Gbit/s NRZ eye mask margin.

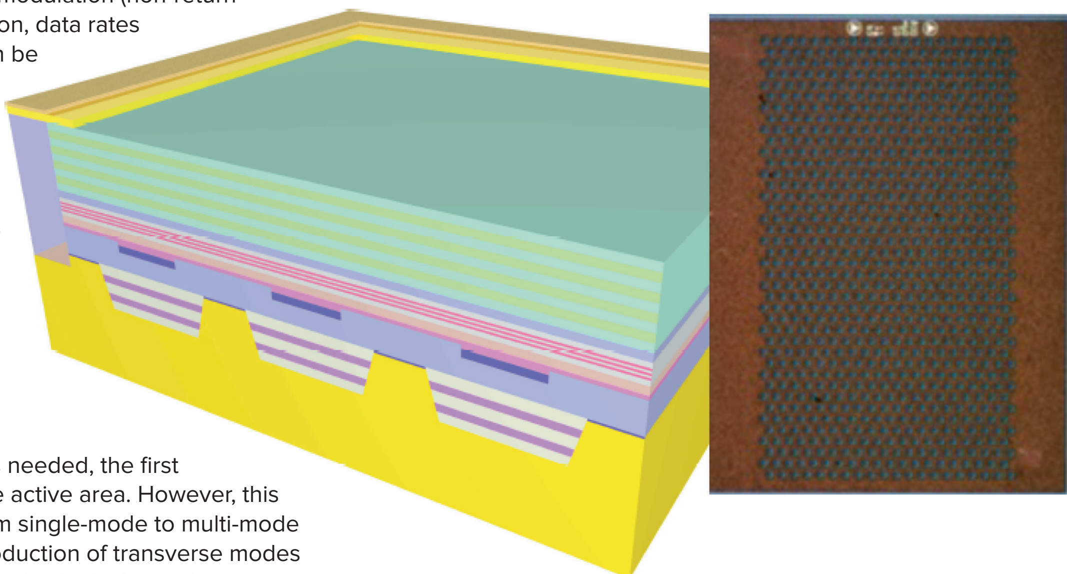
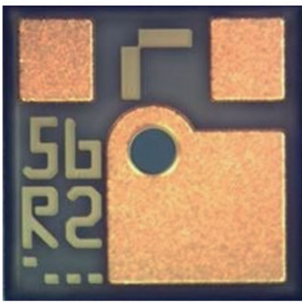
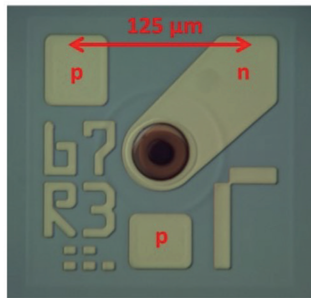


Figure 6. 1.3 µm, 800 emitter InP 2D VCSEL array.



Long Cavity BCB
10 Gbps VCSEL



Short Cavity BCB
25 – 50 Gbps VCSEL

➤ Vertilas' portfolio includes long-cavity BCB 10 Gbit/s VCSELs and short-cavity BCB 25-50 Gbit/s VCSELs.

electrical energy can be pumped into the device before roll-over, a term that describes the post-peak fall in optical power output with increasing current. Compared with our single-mode VCSELs, our multi-mode siblings operate at more than double the bias current for an almost identical voltage. Due to this, our multi-mode lasers with an BTJ diameter of 12 µm generate more than 10 mW of optical power at room temperature.

To accommodate this hike in electrical energy and meet the need for greater power dissipation, we have undertaken additional optimisation of the epitaxial layers of the laser structure, so that they can transfer the heat even more effectively to the gold substrate at the bottom of the device.

To deliver even higher optical output powers of up to several watts, we monolithically integrate many VCSELs into a single 2D array. By taking this approach, we can scale the optical power almost linearly with the number of emitters.

One example of this is a chip that features 800, 1.3 µm emitters (see Figure 6). Operating in quasi-CW mode, this source can deliver more than 8 W of optical power. If higher peak powers are required, the 2D array can be driven with shorter pulses. For pulses in the 200 to 300 µs range, optical peak power can exceed 40 W.

Another avenue that we have pursued, for all our key products, is industrial qualification of their reliability. This may involve stress testing up to 50,000 hours.

While we have come a long way, there's still much more to do. We are now investing in high-volume production capability, to meet the demand for our InP VCSELs in the markets we've discussed. Such efforts will run alongside additional research and development, as we target integration of our VCSELs with silicon photonics, as well as increasing the bandwidth and optical power of our sources. We shall also pursue leading-edge packaging of our VCSELs, and the expansion of their wavelength range beyond 2.3 µm. Without doubt, there's a very exciting future in store for the InP VCSEL.

FURTHER READING

➤ J. Fabrega *et al.* "Experimental Demonstration of a Metro Area Network with Terabit-capable Sliceable Bitrate Variable Transceiver using Direct Modulated VCSELs and Coherent Detection", J. Opt. Commun. Netw., Jan 2023

➤ R. Dohle *et al.* "New Packaging Technology for Disruptive 1- and 2- Dimensional VCSEL Arrays and Their Electro- Optical Performance and Applications", 2022 IEEE 72nd Electronic Components and technology Conference (ECTC), May/June 2022

➤ C. Li *et al.* "Hybrid integration of VCSEL and 3-µm Silicon Waveguide based on a monolithic lens system", IEEE Trans. Compon. Packag. Manuf. **12** 883 (2022)

➤ M. Svaluto Moreolo *et al* "Multi-Tb/s photonic transceivers for metro optical network connectivity evolution", Proc. of SPIE OPTO, Multi-Tb/s photonic transceivers for metro optical network connectivity evolution, 2021 (online)

➤ P. Gatto *et al.* "Beyond 25 Gb/s Directly-Modulated Widely Tunable VCSEL for Next Generation Access Network," 2018 Optical Fiber Communications Conference and Exposition (OFC) Th1E.2.

➤ M. Verplaetse *et al.* "DSP-free and real-time transmission of 50Gb/s NRZ over 15km SSMF and 64Gb/s NRZ B2B with a 1.3 µm VCSEL", OFC 2018, Th4B.7

➤ T. Aalto *et al.* "Transceivers for 400G based on hybrid integrated thick SOI and III/V chips", ECOC 2017

➤ N. Eiselt *et al.* "Experimental Demonstration of 84 Gb/s PAM-4 over up to 1.6 km SSMF Using an 20-GHz VCSEL at 1525 nm", IEEE Journal of Lightwave technology 35 1342 (2017)

➤ A. Dochhan *et al.* "56 Gb/s DMT Transmission with VCSELs in 1.5 µm Wavelength Range over up to 12 km for DWDM Intra-Data Center Connects", ECOC 2016

➤ M. Ortsiefer *et al.* "Long-wavelength VCSELs for TDLS applications", Field Laser Applications in Industry and Research (FLAIR), Garmisch-Partenkirchen, 2009

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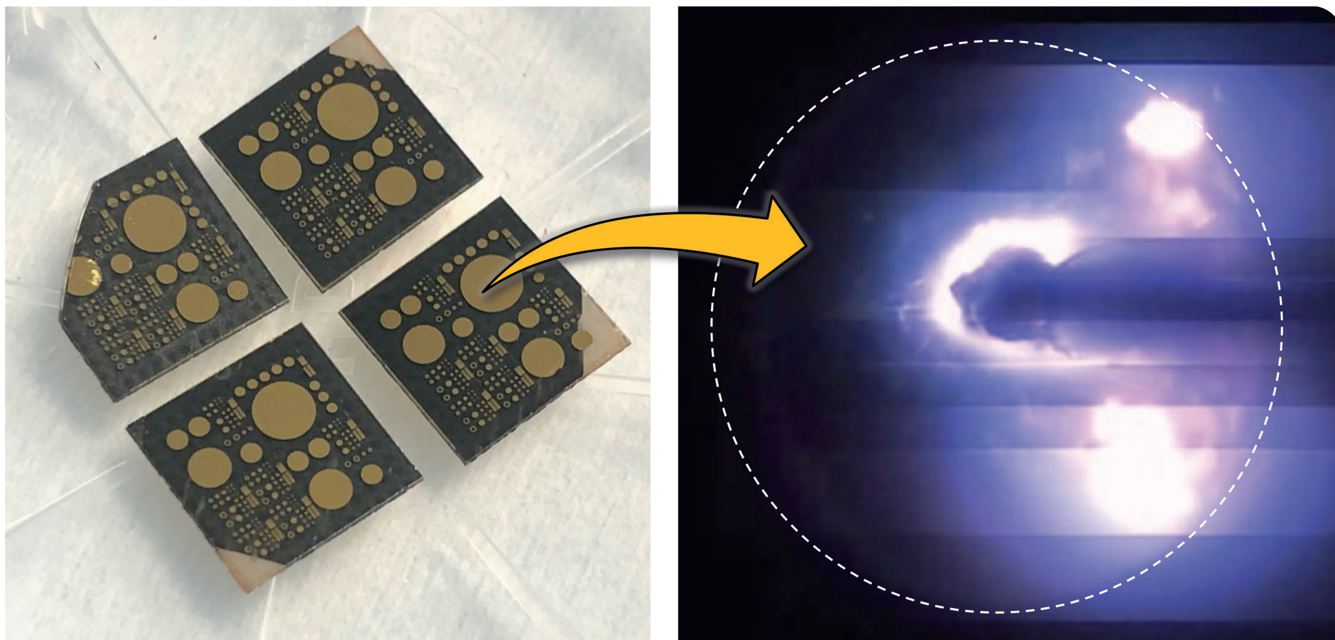


GaN diodes with uniform, robust avalanche

A multi-faceted endeavour, starting with material growth and extending all the way to circuit-level investigation, ensures uniform, robust avalanche in GaN vertical power diodes

BY BHAWANI SHANKAR AND SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY

IN EVERY power electronic system, it is the power devices that provide the building blocks. When these semiconducting devices, often diodes and transistors, are used in power electronic circuits, they are often placed in series with inductive loads, such as a motor or a discrete inductor.

In this configuration, when device switching occurs, there's an interruption to current flow through the series inductor – and this generates a voltage transient, appearing across the device terminals (see Figure 1). If the voltage transient exceeds the breakdown voltage of the device, this poses a threat to damage the device.

To prevent failures from such overvoltage scenarios, device engineers tend to design power devices with extra headroom in the breakdown voltage. But there are penalties to pay: a higher on-resistance, leading to an increase in conduction losses; and a higher device manufacturing cost, stemming from a hike in semiconductor estate associated with the larger drift region volume needed to hold the higher voltage.

Combatting this concern are semiconductor devices with an avalanche capability, which have an inherent overvoltage protection. When such devices face overvoltage transients in a circuit, they undergo avalanche breakdown and generate micro-plasma or current filaments that bypasses the electrical stress and protect the device.

Fortunately, one of the most promising materials for the future of power electronics, GaN, possess avalanche capability. However, despite more than three decades of exploration of this wide bandgap semiconductor as a mainstream device material, reports of its avalanche breakdown are limited to devices that have been grown on native GaN substrates.

Achieving uniform avalanche

This limitation may raise a few eyebrows, given that any GaN-based device with an intrinsic *p-n* junction should show avalanche behaviour, so long as it has been designed correctly. But there are valid reasons why there are so few reports of experimentally realising this phenomenon, and why it took until

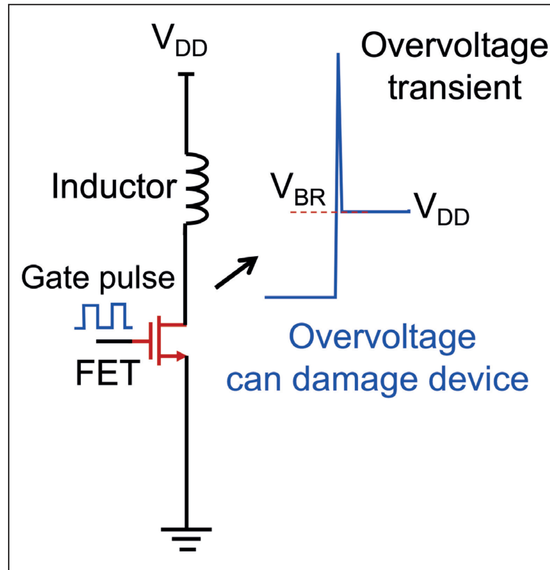
➤ Left: Dies with GaN vertical *p-n* diodes of various diameter, fabricated in the Wide-Bandgap Lab at Stanford University. Diodes of voltage class 1.2 kV and 3 kV with robust avalanche are successfully developed and tested.

2013 to first see this behaviour. The long wait occurred because effort is required on several fronts to realise avalanche breakdown – there's a need for high quality material, very precise device design and well-optimised processing. Regarding the first of these requirements, one pre-requisite for realising avalanche breakdown in GaN devices is a defect density below 10^6 cm^{-2}.

When it comes to device design, as avalanche breakdown is an electric-field-driven phenomenon, electric field management is crucial to realise this mode of operation. However, it is nearly impossible to achieve an avalanche breakdown mode in GaN-based lateral device geometries, such as HEMTs and lateral *p-n* diodes, because they tend to suffer from premature failures, either from corner effects, which cause local field enhancement, or from excessive buffer leakage at high voltages.

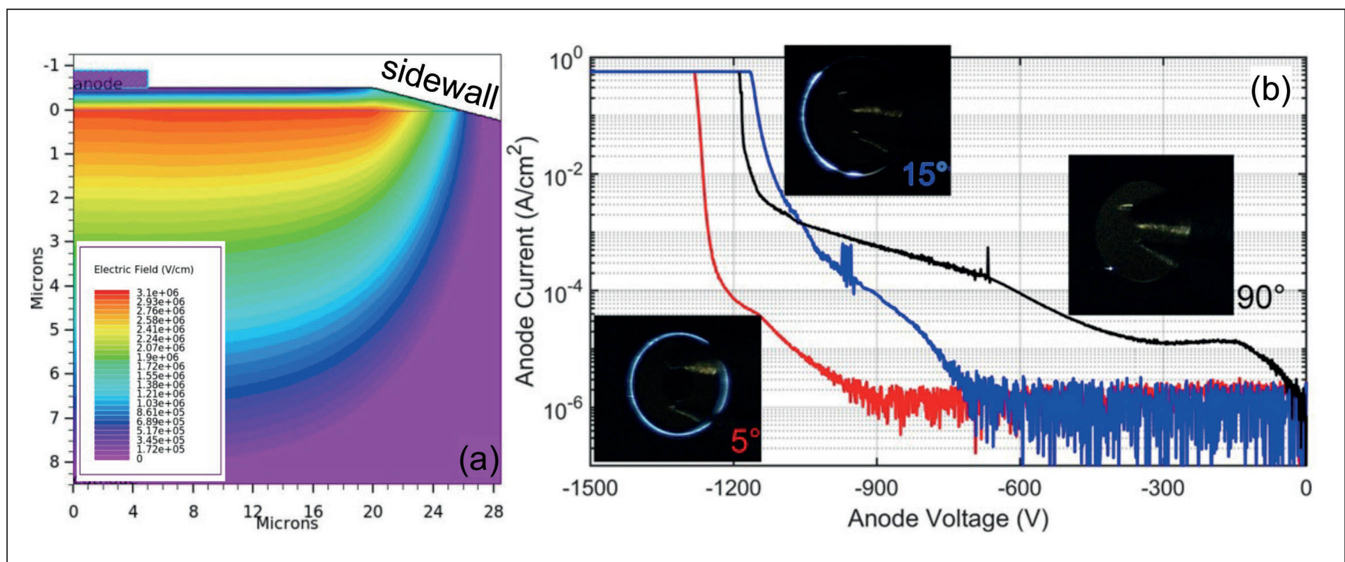
In marked contrast, GaN-based vertical devices offer better field management, higher current density, and a superior area efficiency than their lateral counterparts. These merits are behind the demonstration of GaN vertical *p-n* diodes with an avalanche breakdown voltage of up to 6 kV, reported in 2022.

Given that the development of high-performance avalanche GaN diodes is still a work in progress, it's not surprising that there are relatively few reports

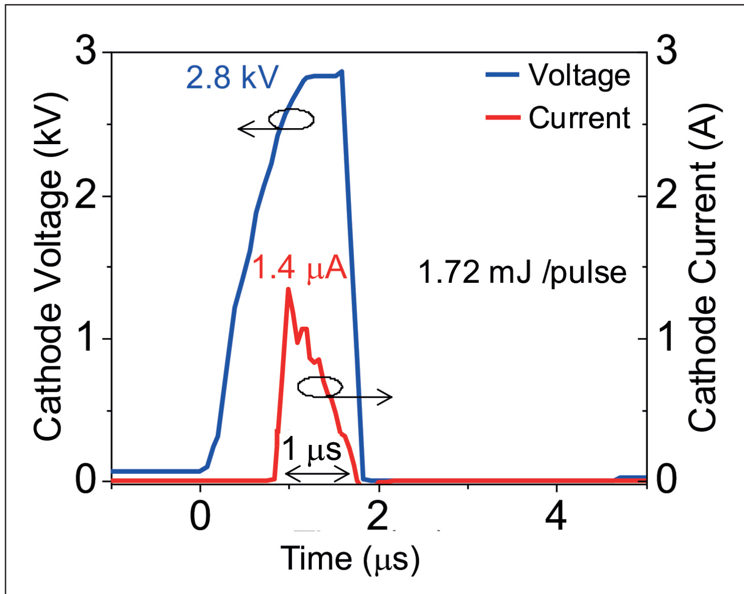


➤ Figure 1. A power MOSFET in series with an inductor experiences voltage overshoot during switching. If the FET is not avalanche capable, the overvoltage can cause device failure. To avoid premature failures, typically the device is overdesigned for a breakdown voltage (V_{BR}) higher than required.

of experimental investigations of this device. Most testing has been undertaken using DC conditions, with studies considering the temperature-dependent reverse characteristics of diodes to verify a positive temperature coefficient of breakdown – this provides proof of avalanche behaviour. However, observing this trait under DC test is no guarantee of reliable, repeatable avalanche operation in a real application.



➤ Figure 2. Avalanche breakdown study for a 1.2 kV GaN vertical *p-n* diode. (a) Bevel termination redistributes the electric field, triggering avalanche mechanism in the bulk GaN. (b) Reverse characteristic of the diode studied at different bevel angles. A uniform electroluminescence (light emission) occurs at breakdown in the diode with a 5° angle, exhibiting 1.2 kV avalanche breakdown voltage.



➤ Figure 3. Current and voltage waveforms of a 3 kV GaN vertical *p-n* diode during avalanche breakdown. The diode voltage clamps and a high current flows from cathode to anode in avalanche mode.

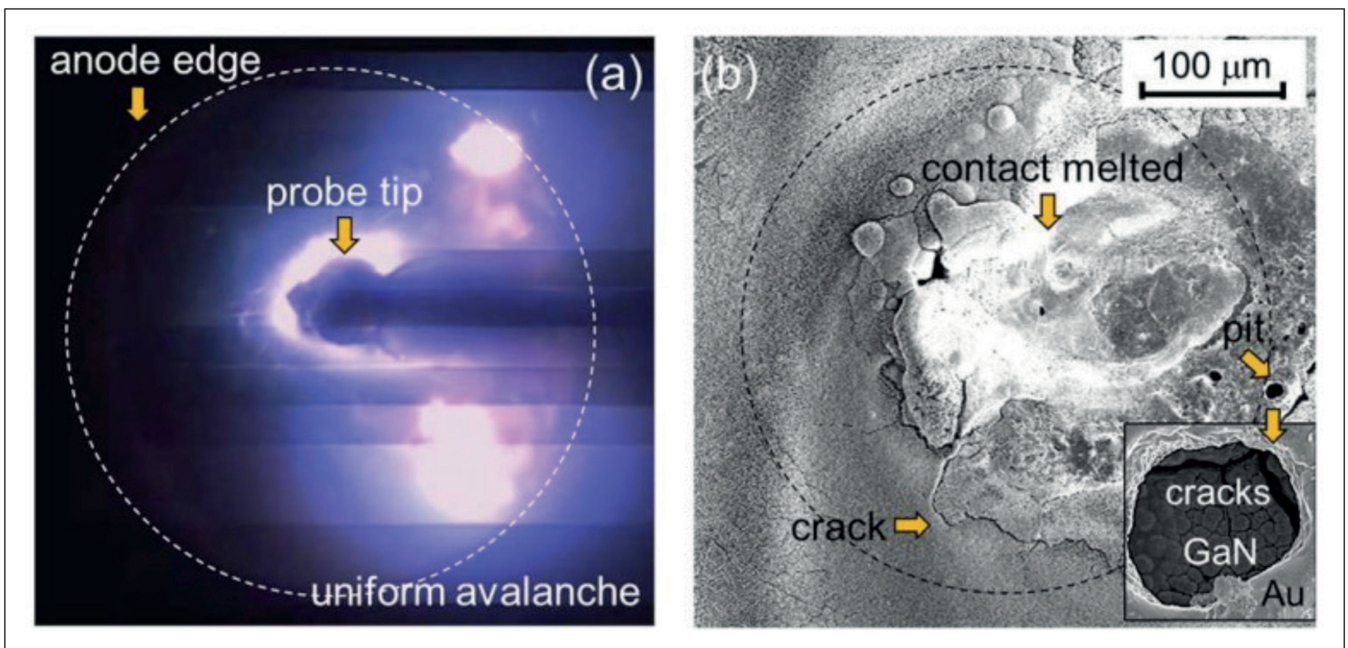
Our group, the Wide-Bandgap Lab at Stanford University, is breaking new ground by investigating the various factors that can guarantee uniform, repeatable avalanche in GaN vertical devices. We have embarked on a multi-faceted endeavour, beginning with material growth and extending all the way to circuit-level characterisation.

Fabrication of our vertical *p-n* diodes starts with the growth of an epi-structure on GaN substrates with an ultra-low defect density – it is less than 10^6 cm^{-2}. We carefully selected the doping profile and its concentration to ensure a uniform electric field distribution in devices, key to a uniform avalanche. Employing optimised *p*-type doping, with a magnesium doping concentration of 3×10^{17} cm^{-3}, resulted in an avalanche breakdown voltage of 1.2 kV.

We have devoted much effort to developing diode designs that avoid the high charge density at device corners and edges, as such features locally enhance the electric field, thereby introducing non-uniformity. To suppress local field peaks and unify the field distribution, we have employed edge-termination techniques, such as bevel and field plate.

Evaluating edge termination efficacy

For this part of our study, we considered a range of bevel angles from 0 ° to 90 °. We found that diodes produced the most uniform avalanche breakdown with a 5° bevel, for a *p*-type doping concentration of 3×10^{17} cm^{-3} (see Figure 2). Higher levels of doping required a higher bevel angle, leading to a lower breakdown voltage in the device. We have found that in general, a bevel is more effective up to 3 kV. It's worth noting that a bevel termination carries an area penalty: the smaller the bevel angle, the shallower the slope, hence the need for a greater area to realise the device. Due to this, a bevel alone cannot offer breakdown voltages higher than 1.2 kV. To overcome this limitation, a bevel should be combined with other edge terminations. Adopting this approach, we fabricated GaN diodes possessing both a bevel and a field plate at the anode and showed an avalanche breakdown voltage of up to 3 kV (see Figure 3).



➤ Figure 4. (a) Uniform electroluminescence, hence uniform avalanche breakdown, observed in a 1.2 kV GaN vertical *p-n* diode under unclamped inductive switching stress. (b) After several thousand avalanche pulses, the diode eventually encountered thermal failure.

A significant difference between the design of our 1.2 kV and 3 kV diodes is that the latter incorporates a spin-on-glass, which passivates the diode surface and acts as a field plate dielectric. For the 1.2 kV diode, it is the SiN that provides passivation at the surface and sidewalls. This form of passivation is unsuitable at voltages above 1.2 kV, as SiN on the bevel sidewalls becomes leaky.

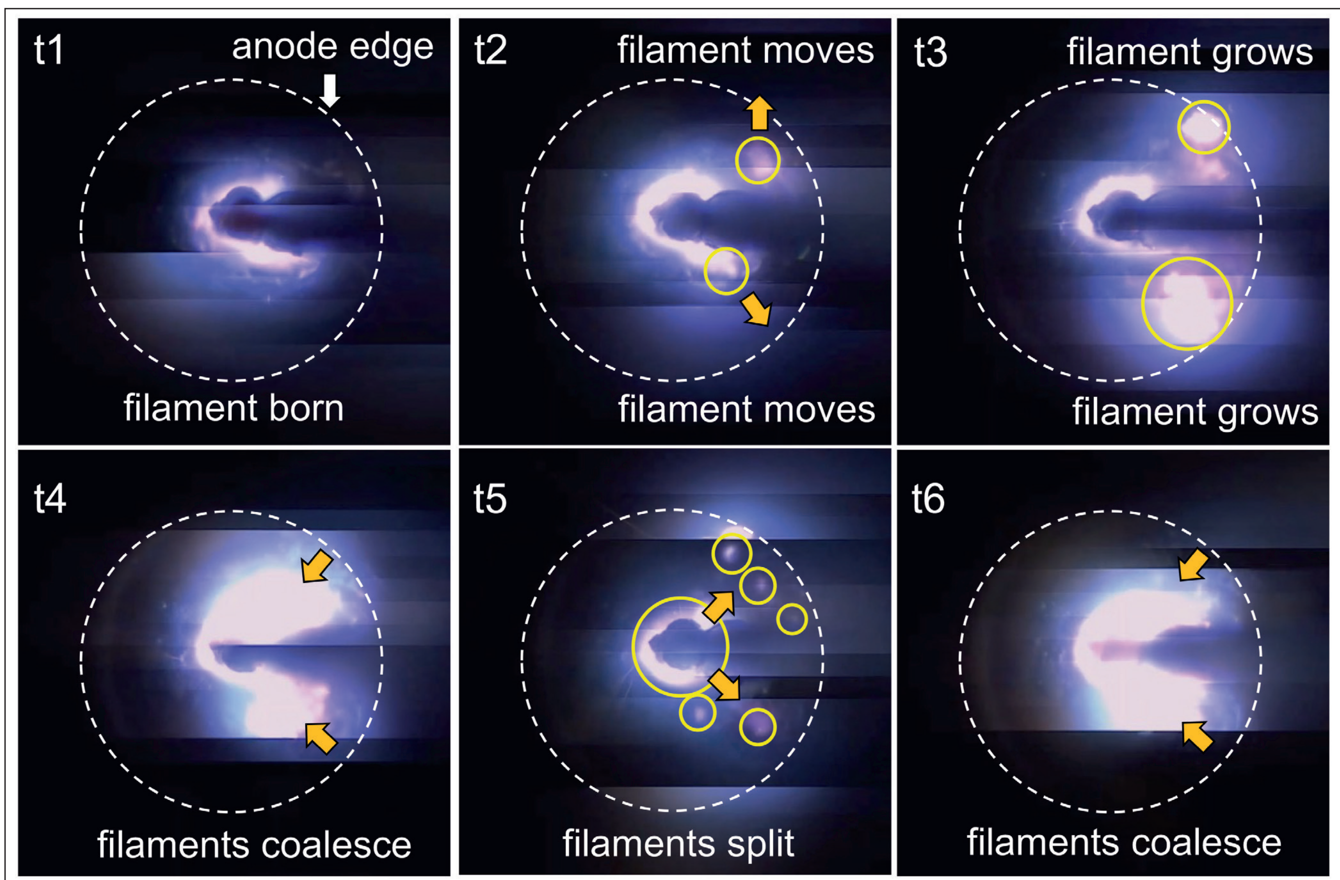
One technique offering great insight into avalanche behaviour is spatially resolved electroluminescence. When avalanche occurs, there is band-to-band and defect-mediated recombination of free electron-hole pairs at breakdown, giving rise to electroluminescence. We have turned to spatially resolved electroluminescence to investigate the efficacy of edge termination in our 3 kV GaN vertical *p-n* diode. We found that electroluminescence emission remained localised at the field plate corner and eventually the diode failed after few avalanche cycles.

Subsequent failure analysis revealed damage to a portion of the field plate under intense heating associated with the avalanche current. This investigation also found that the diode had been compromised by cracking and peeling of the field plate dielectric, due to the thermal stress. On the otherhand, the 1.2 kV diode had more robust bevel termination and the diode could attain uniform avalanche which eventually led to uniform thermal failure (see Figure 4). We have concluded from these observations that there's much need for robust edge termination, which is trustworthy during intense avalanche events involving high currents, high voltages, and tremendous self-heating within the device.

Avalanche robustness?

There is an established approach to evaluating a device's avalanche robustness, involving measurement of the energy-per-cycle that the device can carry without failure during avalanche breakdown. The common approach to determining this value is an unclamped inductive switching test, often involving packaging a device prior to its testing.

Unfortunately, it's challenging to comprehensively investigate the device's avalanche behaviour at the package-level, due to a limited physical and optical access to the die. So, to overcome this issue we have employed a modified test set-up that integrates the unclamped inductive-switching circuit with the wafer-prober. On-wafer tests on devices allow us to perform device-material co-investigations. With this configuration we can undertake on-wafer avalanche tests and electroluminescence measurements simultaneously.



➤ Figure 5. Top view optical images of a GaN vertical *p-n* diode at different instants during an avalanche breakdown. A high voltage, unclamped inductive switching pulse train applied to the diode pushes it into the avalanche breakdown mode. At breakdown, current filaments (or micro-plasma tubes) form which later dynamically move around, spreading the heat across the diode area as the avalanche progresses.

Dynamic filaments improve the diode's reliability and robustness under avalanche breakdown. Filaments may be static in poorly designed devices, causing local burnouts and failures and ultimately limiting device reliability

Such studies show that our 1.2 kV GaN vertical *p-n* diode with optimised *p*-type doping and bevel angle produces uniform electroluminescence. When the diode is operating under avalanche, its cathode voltage clamps to the avalanche voltage and there is a high current flow from the cathode to the anode terminal.

This robustness is highly sought after by circuit designers and power electronics engineers who use power semiconductor devices. What's encouraging is that the degree of avalanche robustness of the GaN *p-n* diode is significant – it exceeds that of a commercial SiC Schottky diode of similar voltage and current rating by 22 percent. Having said this, one might wonder, what contributes to high avalanche robustness in GaN diode? When avalanche occurs in GaN *p-n* diode, this is accompanied by the formation of highly conducting micro-plasma tubes or current filaments across the junction. Due to this, short-circuit paths are momentarily created between cathode and anode terminals. During avalanche, the surge energy from the inductor discharges through these filaments and is later dissipated as heat and light.

We have discovered that the avalanche current filaments in our GaN diodes are not stationary but grow and dynamically move around the diode's active area under switching conditions (see Figure 5). This movement, which is driven by the temperature gradient inside the filament's core, is beneficial, assisting uniform spreading of heat across the device area and suppressing any potential local hotspots. Consequently, these dynamic filaments improve the diode's reliability and robustness under avalanche breakdown. Filaments may be static in poorly designed devices, causing local burnouts and failures and ultimately limiting device reliability.

It is clear that GaN diodes with avalanche capability have great potential to improve the performance of power electronic circuits. There's still a long way to go to understand how to design and optimise these devices for tapping into their full potential using their intrinsic capabilities such as avalanche. But we have shown the benefits of a holistic approach to realise GaN devices with robust avalanche, and how electroluminescence can offer great insight into their avalanche behaviour.

FURTHER READING

- Kizilyalli *et al.* "High Voltage Vertical GaN *p-n* Diodes with Avalanche Capability," IEEE Trans. Electron Devices **60** 3067 (2013)
- Mandal *et al.* "Observation and discussion of avalanche electroluminescence in GaN P-N Diodes Offering a Breakdown Electric Field of 3MV cm^{-1}", Semicond. Sci. Technol. **33** 065013 (2018)
- Li *et al.* "A Study on the Impact of Dislocation Density on Leakage Current in Vertical GaN-on-GaN *p-n* Diodes," IEEE Trans. Electron Devices **69** 4206 (2022)
- L. Yates *et al.* "Demonstration of >6.0-kV Breakdown Voltage in Large Area Vertical GaN p-n Diodes with Step-Etched Junction Termination Extensions," IEEE Trans. Electron Devices **69** 1931 (2022)
- Zeng *et al.* "Designing Beveled Edge Termination in GaN Vertical *p-i-n* Diode-Bevel Angle, Doping, and Passivation," IEEE Trans. Electron Devices **67** 2457 (2020)
- Zeng *et al.* "Study on Avalanche Uniformity in 1.2 kV GaN Vertical PIN Diode with Bevel Edge-Termination," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-4
- B. Shankar *et al.* "On-Wafer Investigation of Avalanche Robustness in 1.3 kV GaN-on-GaN P-N Diode Under Unclamped Inductive Switching Stress," 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2021, pp. 40-43
- B. Shankar *et al.* "Study of Avalanche Behavior in 3 kV GaN Vertical P-N Diode Under UIS Stress for Edge-termination Optimization," 2022 IEEE International Reliability Physics Symposium (IRPS), 2022, pp. 2B.2-1-2B.2-4
- B. Shankar *et al.* "Movement of Current Filaments and its Impact on Avalanche Robustness in Vertical GaN P-N diode under UIS stress," 2022 Device Research Conference (DRC), 2022, pp. 1-2

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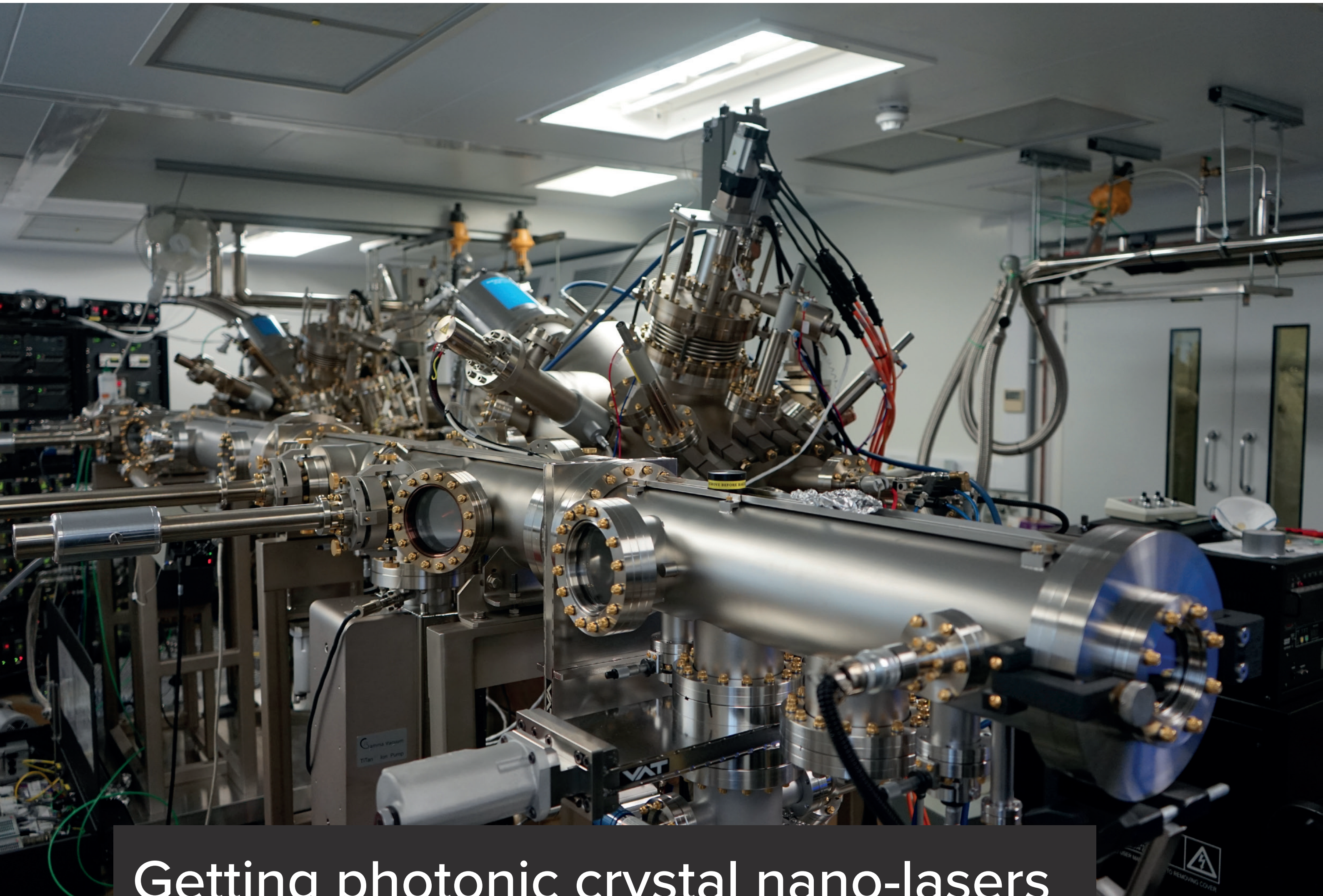


Getting photonic crystal nano-lasers on silicon

Recent demonstrations of photonic crystal lasers on a silicon platform highlight the tremendous potential of these devices for providing efficient light sources for silicon nanophotonic integrated circuits

BY MINGCHU TANG FROM UNIVERSITY COLLEGE LONDON

SEMICONDUCTOR LASERS have come an awfully long way since they emerged from a number of industrial labs in the US in 1962. To realise lasing in those first homostructure devices, the chips would be cooled by liquid nitrogen and electrically pumped with incredibly short, high-current pulses. Fortunately, rapid progress followed the invention of this device, with the introduction of double heterostructures and refinements to the active region improving key characteristics and enabling the production of a practical device.

These advances have spurred the commercialisation of the semiconductor laser and its widespread deployment. Significant successes include miniature sources for reading optical discs, the key technology for CD and DVD players, and the manufacture of countless light engines for various optical networks that underpin communication and the internet.

Now there is much interest in using III-V lasers for silicon photonics. Producing integrated circuits that

route light through waveguides and a number of on-chip devices enables energy savings in many different applications requiring data transfer, such as high-performance computing and data centres, as well as opening up many new markets, including those in healthcare, where miniaturisation is highly valued.

A significant challenge with any silicon photonic integrated circuit is how to incorporate the III-V laser onto the chip. One option is bonding, using the likes of benzocyclobutene (BCB) or oxygen atoms to form a bonding interface. Intel has successfully commercialised this integration method, employing it for the production of silicon optical transceivers operating at 100 Gbit/s. However, the price of these components is at odds with the needs of silicon photonics, which requires a low-cost, high-yield, CMOS-compatible optical communication platform.

A more attractive alternative for bringing laser light to the silicon photonic chip is direct epitaxy. MBE and MOCVD have been used to grow III-Vs on silicon platforms. Recently, this has been shown to be an efficient way to fabricate silicon-based III-V lasers, due to the merits of low cost and large scale. However, despite significant demonstration of conventional Fabry-Pérot and distributed feedback lasers on III-V and silicon platforms, there is still the need for microscale and nanoscale laser devices with far lower energy consumption and optical mode control for silicon-based nanophotonic integrated circuits. Such circuits are promising candidates for next-generation quantum computing and optical microprocessors, and could be used to make microelectronic components for optical/photonic microprocessors.

Helping to lay the foundations for the development of miniature laser sources are the microdisk lasers, a triumph of the 1990s. At the heart of these devices are micro-resonators, a few micrometres in diameter. These structures support whispering-gallery modes, instrumental to single-mode lasing and low operating powers.

Photonic crystal cavities

Building on this concept – and shrinking the footprint of the laser while maintaining its excellent performance – are designs employing a photonic crystal cavity. Thanks to an enhanced light-matter interaction within the photonic cavity, the photonic crystal laser not only benefits from a smaller footprint that is nanoscale in size, but strong optical confinement that comes from the designed photonic bandgap (the primary strengths of the photonic crystal laser, compared with its edge-emitting variant, are listed in Table 1).

One option for integrating a photonic crystal laser with a silicon platform is to bond the light source to a silicon or silicon-on-insulator substrate. Several groups have done just that, including those at the University of Tokyo and the University of Paris-Saclay (see Figure 1 (a)). The greatest advantage of this technique is that it has the potential to couple laser emission to a waveguide, thereby creating a platform for nanophotonic integrated circuits along with other photonic components. However, yields can be very low, hampered by ultra-high requirements for alignment – a challenge that is magnified with micro and nanoscale fabrication.

Our team at UCL is pioneering a more straight-forward approach to fabricating silicon-based photonic crystal lasers, based on the use of direct epitaxy to deposit high-quality III-V materials on silicon (see Figure 1 (b)). This method promises to enable the simultaneous fabrication of many photonic crystal lasers, which significantly increases yield and makes massive production possible.

We have demonstrated the feasibility of massive production of photonic crystal lasers on silicon with our direct growth method by fabricating a nanobeam (one-dimensional photonic crystal) laser array (see Figure 2). Working in partnership with scientists from the Chinese University of Hong Kong and Grenoble Alpes University, we have broken new ground by developing the first III-V two-dimensional and one-dimensional photonic crystal lasers that are directly grown on silicon substrates.

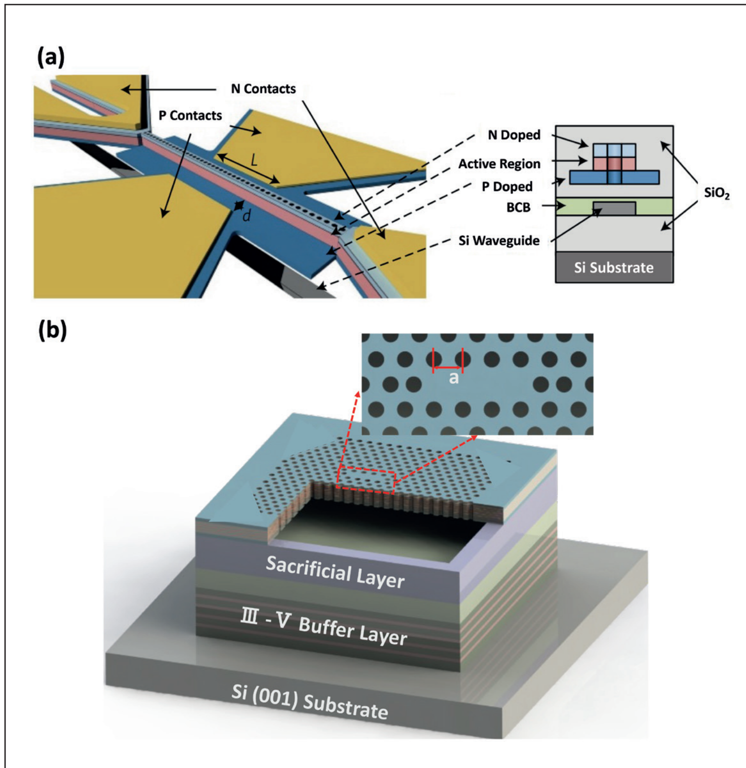
Growing on silicon

It is far from easy to grow high-quality III-V layers on silicon. Barriers to success include dissimilarities in material properties, such as differences in lattice constant, polarity and thermal expansion coefficient. These differences give rise to a high density of crystal defects, which trap numerous carriers, causing additional heating to the chip. Thus, it is crucial to epitaxially grow high-quality III-V materials on a silicon platform, because this is key to realising high-performance III-V lasers on silicon. We have excelled in this regard, growing III-V materials on silicon that have a crystal quality that is very close to that of the III-V native substrate.

To ensure high-crystal-quality III-V materials on silicon, we use a specially designed epitaxial buffer

	Edge-emitting laser	Photonic crystal laser
Footprint	Large	Small
Operating power	Low	Ultra-low
Output power	High	From Low to High
Fabrication cost	Low	Low-medium

➤ Table 1. Comparison of the edge-emitting laser and the photonic crystal laser.



➤ Figure 1. Two different integration methods for photonic crystal lasers on silicon: (a) bonding a III-V nanobeam laser on silicon-on-insulator substrate via BCB material; (b) and direct growth of a III-V photonic crystal laser on a silicon substrate.

layer to prevent: a one-dimensional defect, namely threading dislocations; and a two-dimensional defect, antiphase boundaries. Working with our collaborators at Grenoble Alpes University, we have employed MOCVD to create double silicon atomic steps on the silicon (100) on-axis substrate to avoid formation of antiphase boundaries. The two-dimensional defects, antiphase boundaries, degrade device performance by splitting materials into different domains.

There's a need for this innovation, because prior to treatment, the silicon on-axis (001) surface is covered by single atomic steps. These single steps are to blame for forming antiphase boundaries, which arise when polar III-V materials are directly grown on the non-polar silicon surface.

By switching to a double atomic step, we avoid the formation of antiphase boundary. Evidence of this is provided by the use of hydrogen atoms to destroy the atomic bond between Si-Si atoms under high temperature. Thanks to these double atomic steps, we have grown on silicon a III-V, GaAs, that is free from antiphase boundary defects and has low roughness. Our approach has been widely used with 300 mm silicon substrates, highlighting its potential to slash fabrication costs compared with growth on III-V substrates, as well as the promise of processing our material with state-of-art CMOS fabrication equipment.

Another challenge of growing III-Vs on silicon is accommodating the large lattice mismatch that threatens to introduce a high density of threading dislocations – they could be in the region of 10^{10} cm^{-2} at the interface of III-Vs and silicon. The mismatch is significant: there's a difference of 4 percent between GaAs and silicon, and 7 percent between InP and silicon. Part of the solution is to introduce strained-layer superlattices, which have repeated layers of both tensile and compressive strain. When this is added, threading dislocation density fall to a practicable level for making a device of less than 10^{7} cm^{-2}. This is realised by pushing and pulling the propagation of threading dislocations into the horizontal direction, so they no longer impact the gain materials grown on top.

Additional improvement comes from a high-temperature annealing process, which encourages threading dislocations to move, encounter one another and merge. When annealing is combined with strained-layer superlattices and double atomic steps on silicon, the epitaxial quality of our photonic crystal lasers that are grown on silicon is comparable to heterostructures formed on native III-V substrates.

As well as a high crystal quality, our photonic-crystal lasers need a suitable active region. Over many years, quantum wells have provided gain material in various types of laser, due to their high output power and tremendous optical gain. But they are not ideal in our case, because residual threading dislocations are present in III-V materials grown on a silicon platform, even after careful design of the III-V buffer layer – and as the device operates, the number of threading dislocations grow, degrading device performance. The long-term impact is significant, including diminished output power, a shortened device lifetime and a hike in temperature instability.

➤ Figure 2. A scanning electron microscope image of a fabricated one-dimensional photonic crystal laser array.

Drawing on dots

We have found that a far better alternative for providing gain is the self-assembled quantum dot. When dots are deployed in the active region, they have a high tolerance to threading dislocations – this could lead to threading dislocations forming closed loops, which reduce the extent of device degradation.

Employing the techniques mentioned above, we have produced optically pumped III-V quantum dot lasers on silicon that feature a photonic crystal cavity. These nanobeam lasers have many promising characteristics, including: an ultra-low threshold, with a pumping power below 1 μW; a nanoscale footprint of around 8 μm by 0.53 μm by 0.36 μm, for a one-dimensional photonic crystal cavity; and a high-temperature performance, exceeding 60 °C. These characteristics show that our nanobeam lasers could serve in silicon-based nanophotonic integrated circuits.

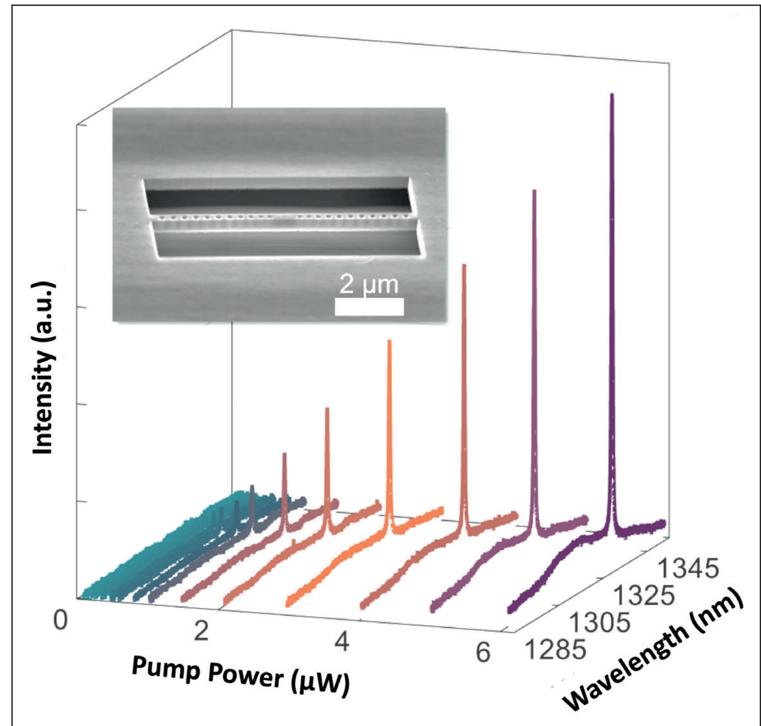
Our next challenge is to realise electrical operation with our photonic-crystal laser on a silicon platform. This can be accomplished by using ion implantation to introduce different *n*-type and *p*-type contact layers on the planar photonic crystal cavity.

It is worth noting that we have the opportunity to turn to some advance types of photonic-crystal cavity. They include the photonic crystal surface emitting laser (PCSEL), which combines the VCSEL's advantages of round beam shape and a high output power of more than 1 W with the high speed and low cost of the edge-emitting laser. Compared with the VCSEL, the PCSEL offers a simpler fabrication process, by using a photonic-crystal cavity to confine light horizontally. This approach avoids the process of oxidation in confining layers.

Another drawback of the VCSEL is that it requires a very high thickness of DBR, so growth of this class of laser on silicon would lead to a large volume of micro cracks, due to incompatible thermal expansion coefficients for the III-Vs and silicon. Turning to PCSELs-on-silicon would offer us a solution for realising high performance III-V surface-emitting lasers on a silicon platform.

When making any semiconductor laser, there are imperfections associated with light scattering at the non-smooth surface. This issue is more severe when using a nanofabrication process, and increases the difficulties of fabricating photonic crystal lasers.

A promising alternative is the topological laser, inspired by the topological insulator in electronics. Topological lasers are capable of guiding light within the designed photonic crystal pattern, and can avoid light scattering associated with imperfections in nanofabrication. Recently, working with colleagues at Grenoble Alpes University and The Chinese University of Hong Kong, we have demonstrated a topological laser with a photonic crystal cavity that's grown on the silicon substrate, thereby showing that this is a robust nanoscale light source for silicon photonics. Even though integrating the photonic crystal laser on a silicon platform is still at an the early stage, we are convinced that this source of light is destined to play a significant role in next-generation, silicon-based nanophotonic integrated circuits.



➤ Figure 3. A nanobeam laser directly grown on silicon substrate with a nanoscale footprint and ultra-low threshold.

FURTHER READING

➤ T. Zhou *et al*. "Monolithically Integrated Ultralow Threshold Topological Corner State Nanolasers on Silicon" ACS Photonics **9** 3824 (2022)

➤ T. Zhou *et al*. "Single-mode photonic crystal nanobeam lasers monolithically grown on Si for dense integration" IEEE J. Sel. Top. Quantum Electron. **28** 1 (2021)

➤ T. Zhou *et al*. "Continuous-wave quantum dot photonic crystal lasers grown on on-axis Si (001)" Nat. Commun. **11** 977 (2020)

➤ G. Crosnier *et al*. "Hybrid indium phosphide-on-silicon nanolaser diode" Nat. Photon. **11** 297 (2017)

➤ B. Ellis *et al*. "Ultralow-threshold electrically pumped quantum dot photonic-crystal nanocavity laser" Nat. Photon. **5** 297 (2011)

➤ K. Hirose *et al*. "Watt-class high-power, high-beam-quality photonic-crystal lasers" Nat. Photon. **8** 406 (2014)

➤ T. Inoue *et al*. "General recipe to realize photonic-crystal surface-emitting lasers with 100-W-to-1-kW single-mode operation" Nat. Commun. **13** 3262 (2022)

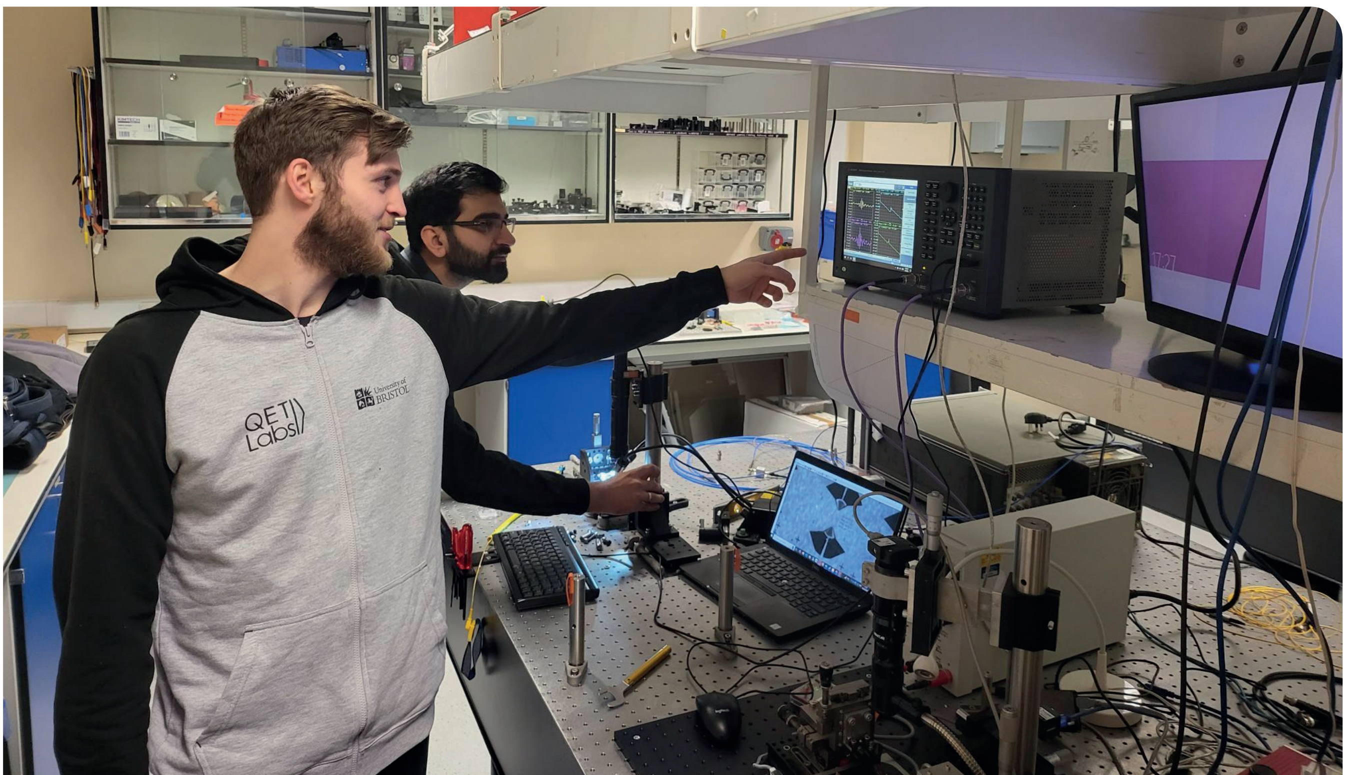
Building phononic integrated circuits with GaN

The ability to guide high-frequency sound around a semiconducting chip positions GaN as a promising platform for producing compact, high-performance acoustic wave devices

BY MAHMUT BICER, STEFANO VALLE, JACOB BROWN, MARTIN KUBALL AND KRISHNA C. BALRAM FROM THE UNIVERSITY OF BRISTOL

A long-standing theme of engineering research is exploring and exploiting the similarities between different wave phenomena. Their similarities, such as reflection, superposition and the creation of standing waves, has been appreciated for decades, thanks in part to excellent demonstrations by the late John Shive, who worked at Bell Labs. Back in 1959 Shive gave a lucid, insightful lecture on this topic that can still be enjoyed via Youtube. In that talk, standing as one of the earliest examples of recognizing the unifying nature of the underlying physics and illustrating how to translate ideas from one field to another, Shive demonstrated his wave generator, a great contribution to teaching this topic.

One modern iteration of exploiting wave phenomena is an extension of silicon integrated photonics, with chips designed to control the propagation of sound waves with frequencies in the gigahertz domain. Such efforts build on progress in silicon photonics over the last decade that spawned a revolution in optical telecommunication, with CMOS foundries now used to build photonic chips. The underlying physics behind this development is the high refractive index contrast provided by a silicon-on-insulator platform – this enables tight confinement of propagating light in wavelength-scale waveguides. For instance, the standard waveguides used to route optical telecommunication signals with wavelengths of



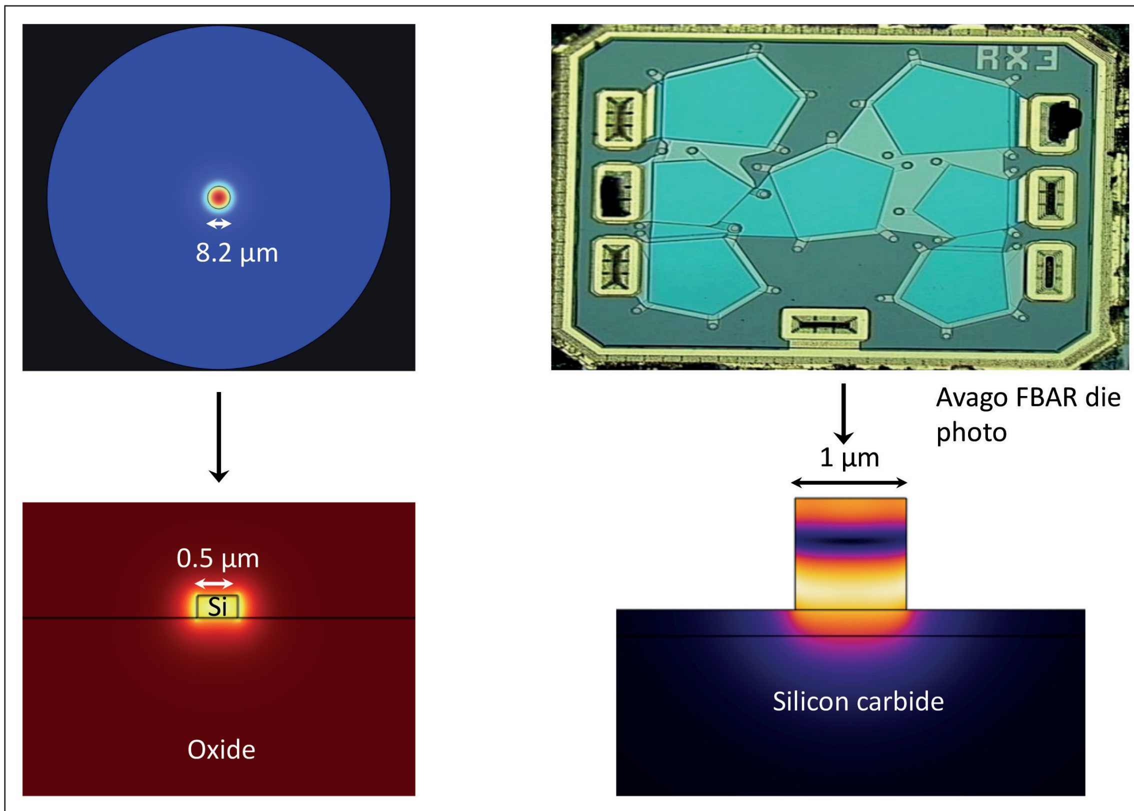


Figure 1. Analogy between photonics and phononics. A strong geometric index contrast leads to an increase in confinement and a reduction in the waveguide cross-section. The rise of silicon photonics is a case in point, with telecom-wavelength silicon waveguides (bottom left) having sub-micron dimensions compared with optical fibres (top left). Bringing these ideas to high-frequency acoustic waves (top right) can lead to the development of compact passive acoustic devices and the prospect of tight active-passive integration on-chip with a view towards integrated RF front-ends. The image of the FBAR Avago die is taken from R. Ruby, "A decade of FBAR success and what is needed for another successful decade," 2011 Symposium on Piezoelectricity, Acoustic Waves and Device Applications (SPAWDA), Shenzhen, China, 2011, pp. 365-369.

around 1550 nm have a cross-section of around just 220 nm by 550 nm. That's substantial miniaturisation compared with an optical fibre: it has a typical core size of 8.2 µm and a cladding diameter of 125 µm, due to its far weaker refractive index contrast.

There are many benefits associated with the extreme confinement that enables compact devices. One great attribute is that a single chip can accommodate various passive and active functions, such as splitting signals, combining them, mode transformation modulation and detection. In addition, there is a low propagation loss that accompanies the strong confinement, resulting in high electric field strengths and associated non-linearities. These properties may be harnessed to implement a variety of functions for quantum information processing, such as single-photon generation using spontaneous four-wave mixing.

As the wavelength of sound waves in the gigahertz range is similar to that of the light used for telecommunication, it is natural to ask how far these ideas from integrated photonics can be extended to gigahertz frequency acoustic waves. One may also wonder what new device paradigms might be enabled. It should be noted that the idea of guiding sound in waveguides is not new – this had been discussed from the very early days of waveguide research. However, this interest has evolved, and is now motivated by considerations related to the acoustic waves that underlie all the filtering in modern smartphones. Today's state-of-the-art smartphones are packed with between 30 and 50 acoustic wave filters, with their number increasing with each successive generation. It is an ever-increasing challenge to accommodate this increasing number of discrete filters into a given area, along with the associated switches, amplifiers and other signal processing circuitry. Current devices are a packaging tour-de-force, but we cannot expect these methods to work well into the future.

The tremendous successes that have come from microelectronics, and more recently silicon photonics, indicate that monolithic integration could be the best solution to this growing problem. Success hinges on figuring out a way to trim the size of traditional acoustic wave devices, and how to implement tight integration between active and passive components on the same die. Much effort has already been directed at accomplishing this, with approaches relying on methods that employ

a CMOS process to integrate existing acoustic-wave devices, such as FBAR and SAW filters, which rely on quasi plane-wave resonators. But at the University of Bristol we are taking a different path, investigating whether acoustic-wave devices can be redesigned around phononic integrated circuits (PnIC), featuring strong geometrical confinement of sound. We are keen to explore the benefits and challenges of this approach.

Computational challenges

Another driver behind the development of PnICs, coming from a very different direction, is the rise of superconducting qubit-based quantum processors – that includes the demonstration of computational quantum supremacy by Google using this platform. A logical next step, following the development of classical information processing technologies, is the development of small quantum networks around these superconducting qubit processors.

This is challenging task, because qubits usually work in a dilution fridge environment that is just a few millikelvin above absolute zero. In addition to this temperature restriction, another issue is that the microwave quantum states cannot be sent over any significant distance, due to loss in the microwave cables.

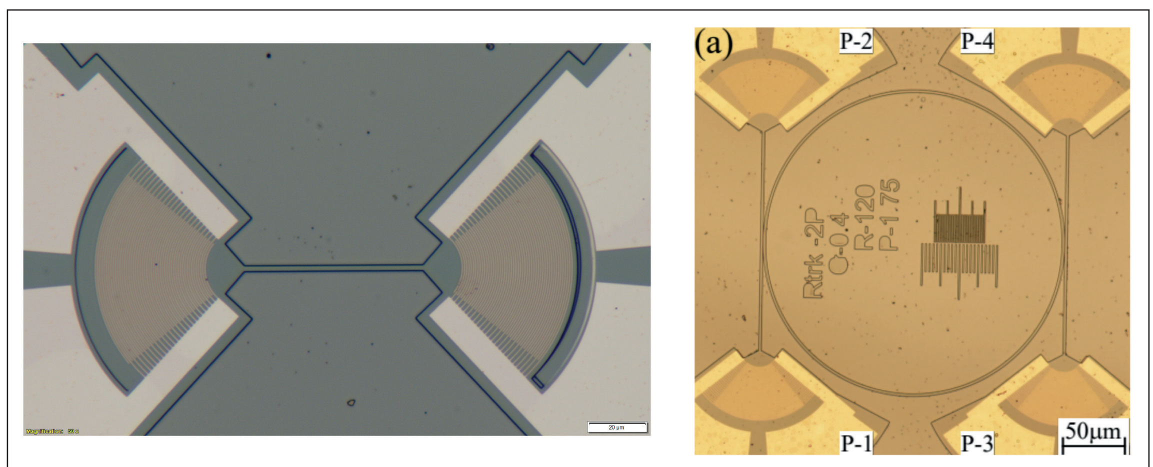
Alternative approaches may offer a better chance of success. One promising pathway is to switch to optical photons, which have been employed in quantum communication from near-earth satellites. This scheme requires quantum transducers, which convert microwave quantum states to light and back with high efficiency. To build such a device, engineers must overcome a massive wavelength mismatch between the fields in the microwave and optical domain. Fortunately, acoustic waves provide a natural way to bridge this, having wavelengths of microns at gigahertz frequencies.

We are pursuing piezoelectric optomechanical platforms that support light and sound propagation on these wavelength scales, and foster strong acousto-optic interactions between resonant optical and mechanical modes. Such piezoelectric optomechanical devices offer one of the most promising routes towards building quantum transducers, with state-of-the-art devices achieving photon transduction efficiencies of around 5 percent.

When developing a PnIC platform, deciding on the material platform is the first and possibly the most critical choice. There's a need for a slow-on-fast platform – in other words, a platform where the acoustic velocity in the waveguiding device layer is far lower than in the substrate – because this offers total internal reflection of sound and the prospect of waveguiding. It's important to satisfy the guiding condition for all potential leakage modes in the substrate, and for all propagation directions simultaneously. The good news is that in practice, this condition is relatively easy to satisfy. There are a wide range of substrate velocities available in different material platforms, and many material platforms are currently being explored, ranging from lithium niobate on sapphire to GaN-on-SiC.

Going with GaN-on-SiC

Out of the many options, which all offer unique advantages and disadvantages, we have selected GaN-on-SiC. Our primary reason for this is that GaN is a moderate piezoelectric semiconductor with a built-in foundry infrastructure that can potentially enable monolithic integration between active and passive components on the same die. By exploiting acousto-electric (electron-phonon) interactions in this platform, it is possible to develop non-reciprocal microwave devices that provide new degrees of freedom to manipulate RF signals on a chip. With alternative, existing technologies, this is only accomplished with the addition of magnetic materials.



➤ Figure 2. Optical microscope images of representative PnIC devices fabricated at the University of Bristol in a GaN-on-SiC platform. The acoustic waves are generated from applied RF signals using interdigitated transducers, whose fingers are curved to focus the sound into the acoustic waveguides. The waves are then routed on-chip using waveguides with cross-sectional dimensions of the order of a wavelength, and high-Q whispering gallery modes in ring resonators, which can be used for resonant devices.

Our PnICs feature an interdigitated transducer, which converts input microwave signals to sound waves (see Figure 2 for an optical microscope image of our device). The periodicity of our interdigitated transducer has been selected to match the acoustic (Lamb) wave frequency in the material. This ensures a periodic perturbation on the surface, due to the piezoelectric effect, and efficient conversion of microwave energy into propagating sound waves. By shaping our electrodes, we can focus sound waves efficiently into wavelength-scale waveguides that have a cross-sectional area of several square microns. Once sound is launched into these waveguides, it can be routed over the surface in an arbitrary fashion, while maintaining tight lateral confinement.

As well as producing straight waveguides, we have the opportunity to construct micro-ring resonators that exploit high-quality-factor, whispering-gallery modes of sound as the resonant building block for filters. Given that whispering-gallery modes rely on the total internal reflection of sound, which is theoretically lossless at a given frequency, resonators based on this technology should demonstrate higher quality factors than traditional SAW and FBAR devices – those incumbents rely on either metal gratings or metal contacts (hard boundaries) for reflection that's always accompanied by excess dissipation and scattering. If we are able to experimentally verify the promise of this micro-ring resonator technology, it would show that in addition to providing compact devices, the PnIC approach can deliver devices with a higher performance than those made with traditional approaches.

The real advantage of the PnIC lies in the realisation that since sound is generated from an RF signal, its manipulation on a chip ultimately provides new degrees of freedom to manipulate RF signals. For instance, if the designer of a PnIC decides to include spiral waveguides with an on-chip footprint of less than 0.25 mm^2, this allows RF signal delays of more than 2 μs, corresponding to electromagnetic delays of at least 600 m.

While our PnIC platform has shown promising initial results, there are a few important problems that we still need to address before our exciting device demonstrations can impact future RF systems. One essential area to work on is the reduction of the overall insertion loss in these platforms. Acoustic waves suffer negligible excess dissipation and scattering once inside the waveguide, but a significant insertion loss at the entrance and exit, coming from the transducer and the transducer-waveguide interface. It is a challenge to develop efficient transducers that are impedance-matched to 50 Ω and mode-matched to wavelength-scale waveguides.

Another issue arises because acoustic platforms are intrinsically multi-moded systems. There's a need to carefully control mode propagation so that sound is efficiently focused into the waveguides without deleterious mode conversion at the interfaces. Note that in this instance the analogy with optics breaks down. For integrated photonics the corresponding problem is much simpler, due to both single-mode operation and the nature of the refractive index profile, which keeps light near the waveguide centre. With sound, especially surface waves, there is a preference for intensity to peak beside the edges of the waveguide.

A second thrust for our research roadmap is to push the PnIC beyond purely passive devices and exert active control on the acoustic waves propagating in these wavelength-scale devices. We would like to move towards tuneable PnICs, engineering acoustoelectric interactions in our GaN platform to provide controllable gain and non-reciprocity. Success on this front will provide new degrees of freedom to the PnIC toolkit from an RF systems perspective. Finally, it goes without saying that there's a need to translate all these research advances to a commercial GaN foundry platform, to enable a full realisation of the system-level benefits.

We are in no doubt that by guiding and manipulating sound on the surface of a chip, wavelength-scale PnICs are providing a promising avenue to re-think passive acoustic devices from an RF systems perspective. As well as trimming the on-chip footprint, building around a waveguide geometry allows natural avenues to route and actively manipulate sound – and by extension the associated RF signal – on a chip in ways that open up new architectures for systems integration and signal processing. To realise the full benefits of this platform in the near-term there's a need to cut insertion loss to levels comparable to current systems and produce devices with a commercial foundry process.

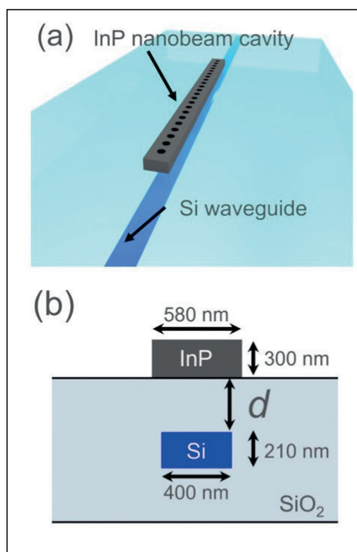
FURTHER READING

- **Smartphones and RF filters issues**: R. Ruby "A Snapshot in Time: The Future in Filters for Cell Phones" IEEE Microwav. **16** 46 (2015)
- **Piezoelectric quantum transducers**: K. Balram *et al.* "Piezoelectric Optomechanical Approaches for Efficient Quantum Microwave-to-Optical Signal Transduction: The Need for Co-Design" Adv. Quantum Technol. **5** 2100095 (2022)
- **Confining sound and light (mechanisms)**: "Controlling phonons and photons at the wavelength scale: integrated photonics meets integrated phononics" A. Safavi-Naeinin *et al*. Optica **6** 213 (2019)
- **GaN acoustics work at Bristol**: M. Bicer *et al.* "Gallium nitride phononic integrated circuits platform for GHz frequency acoustic wave devices" Appl. Phys. Lett **120** 243502 (2022)
- **Acousto-electric interactions for RF signal processing**: L.Hackett *et al.* "Towards single-chip radiofrequency signal processing via acoustoelectric electron–phonon interactions" Nat. Commun. **12** 2769 (2021)

Advancing quantum photonics with transfer printing

Transfer printing produces CMOS-compatible integration of a silicon platform with quantum-dot single-photon sources

A COLLABORATION between researchers in Japan and Germany is claiming to have broken new ground in the integration of single-photon sources and silicon photonic integrated circuits. According to the team, they are the first to unveil hybrid integration of quantum-dot single-photon sources in the telecom band with silicon photonic integrated circuits made in silicon foundries.



➤ (a) InP nanobeam cavities are positioned below the silicon waveguide by transfer printing. (b) Evanescent interaction ensures coupling between the waveguide and the cavity. Calculations indicate a quantum-dot-to-waveguide coupling efficiency of 99.4 percent for a value of *d* of 450 nm.

This advance by engineers from a number of institutions – Toyohashi University of Technology, The University of Tokyo, Keio University, The University of Electro-Communications and the University of Kassel – promises to aid the construction of large-scale quantum photonic integrated circuits. Such circuits could be used for quantum simulation, quantum communication and quantum machine learning.

Options for providing single-photon sources for quantum circuits include III-V quantum dots, colour centres in diamond and SiC, and defects in two-dimensional materials. Of these, there's much merit in InAs/InP quantum dots, according to team spokesman Ryota Katsumi, who is affiliated to Toyohashi University of Technology and The University of Tokyo.

Katsumi told *Compound Semiconductor* that quantum dots are ideal for meeting the requirements for single-photon sources, which include bright single-photon emission, high purity, deterministic operation and high indistinguishability. "It is difficult for other single-photon sources to perform all of these requirements at once."

The team's latest triumph builds on previous successes, including using transfer printing to realise the hybrid integration of InAs/GaAs quantum-dot single-photon sources on a CMOS-processed chip.

REFERENCE
➤ R. Katsumi *et al*. Appl. Phys. Express **16** 012204 (2023)

For that work, the sources produced emission outside conventional communication bands. By now moving to the O and L bands via the switch from dots on GaAs to those on InP, the researchers are benefitting from low loss and low dispersion propagation through optical fibre – this is advantageous for long distance and secure quantum networks.

The latest work began with the growth of InAs quantum dots on an InP substrate via MBE. Using the addition of a hard mask, electron-beam lithography and dry and wet etch etching, photonic-crystal nanobeam cavities were formed from the epiwafers. Transfer printing re-located this structure to a silicon waveguide cladded with glass (see Figure).

Micro-photoluminescence measurements at 13K, using optical excitation from a 785 nm laser, produced a strong quantum-dot emission peak at 1436.9 nm and a fundamental cavity mode at 1436.2 nm. The single-photon coupling efficiency from the dots to the waveguide is 82 percent.

In the nanobeam cavities produced by the team around 10 quantum dots couple to the cavity. Some of these dots are outside the cavity's resonance, leading to background emission and a degradation of a key figure of merit known as g(2), which is a measure of the degree of second-order coherence.

"For purer single-photon emission, it is necessary to employ a single quantum dot," remarked Katsumi, who added that an attractive way to realise this is to produce epiwafers with a much lower quantum-dot density.

As well as improved purity of emission, integrated quantum photonic circuits need single-photon sources that are electrically driven, rather than optically pumped. According to Katsumi, the team's technology offers a way to do this. "Transfer printing could even be used for the implementation of the electrodes for electrical pumping on silicon."

To realise practical quantum photonic information processing, there needs to be efficient, plug-and-play coupling between single photons and fibre – this will ensure long-distance quantum networks. Katsumi and co-workers are targeting this, with efforts directed at making modularize solid-state single-photon sources by transfer printing. "This will enable the efficient and stable supply of single photons for future quantum applications."

Annealed AlN templates aid far-UVC LEDs

Far-UVC LEDs on annealed AlN templates offer increased output powers, thanks to greater strain in the quantum wells

A FORMIDABLE obstacle to realising powerful LEDs emitting in the far UVC is the dominance of transverse magnetic polarisation that inhibits efficient light extraction. But this can be overcome with the introduction of compressively strained AlGaN quantum wells on annealed AlN templates, according to recent work by a team from Berlin.

A partnership between researchers at FBH Berlin and the Technical University Berlin have used this approach to produce LEDs that deliver a CW output of several milliwatts at around 230 nm. Such sources provide an attractive alternative to variants emitting in the deep UV for killing germs.

"Far-UV light does not kill the germs better than 265 nm LEDs. The point is that 265 nm is harmful to the eyes and skin, so cannot be used with people being present," explains Arne Knauer from FBH Berlin. Moving treatment to around 230 nm ensures that light only penetrates the top dead layers of the skin.

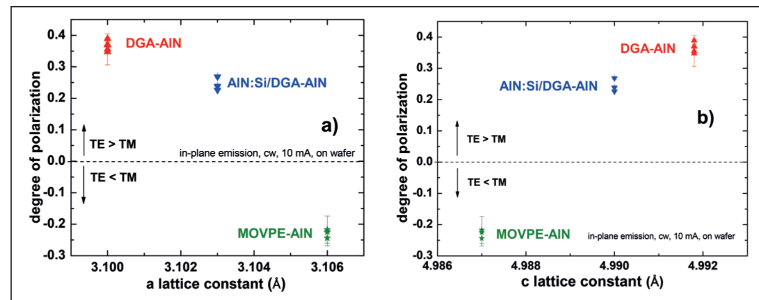
The team from Berlin are not the first to exploit the benefit of strain to enhance the extraction efficiency of far-UVC LEDs. But the use of double-annealed AlN templates is innovative. Knauer says that as well as offering a lower dislocation density – it is just a few 10^8 cm^{-2} – double-annealed AlN templates provide a far smaller *a*-lattice constant, which ensures a substantial increase in the strain in the epilayers, leading to greater light extraction.

The challenge for Knauer and his co-workers has been to incorporate this strain without introducing new dislocations that quench light emission. They have succeeded in this endeavour, with the team claiming an increase in output power to a record level for LEDs formed on double-annealed AlN templates. Devices show an increase in both the light extraction efficiency and internal quantum efficiency.

The team's double-annealed templates were formed by: sputtering a 0.4 μm-thick layer of AlN on 2-inch sapphire substrates; annealing this film at 1720 °C for 3 hours; depositing 1.1 μm of AlN by MOCVD; and annealing the resulting sample at 1720 °C for 5 hours.

Efforts at optimising the double-annealed AlN templates are ongoing, led by Sylvia Hagedorn from FBH Berlin. "The problem is that the process of dislocation reduction is connected with the introduction of oxygen into the AlN," remarks Knauer. "That creates defects, which absorb the light of the LEDs and emit parasitic luminescence."

The researchers have compared the performance



➤ Double-annealed AlN templates provide the most favourable degree of polarisation in both the *a*- and *c*-orientations ((a) and (b), respectively) of far-UVC LEDs.

of far-UV LEDs grown on double-annealed AlN templates with: a variant that combined this with an overgrown layer of 3 μm-thick silicon-doped AlN; and a simpler structure, consisting of just 2 μm-thick AlN grown by MOCVD.

On all three templates, Knauer and co-workers added LED heterostructures featuring a 500 nm-thick AlN buffer, a 875 nm-thick AlGaN *n*-contact layer, an active region with three $Al_{0.76}Ga_{0.24}N$ quantum wells, and a compositionally graded AlGaN layer capped with heavily *p*-doped, 30 nm-thick GaN.

Flip chip mountable, bottom-emitting LEDs were fabricated from all three forms of epiwafer, using plasma etching to define mesa structures with a 0.4 mm^2 emitting area and expose an *n*-type contact layer. After adding platinum-based *p*-contacts and vanadium-aluminium-based *n*-contacts, the team measured on-wafer CW characteristics.

These measurements show that the degree of polarisation – defined as the difference between the intensity in the transverse magnetic and transverse electric orientation, divided by the sum of these two intensities – is most favourable for far-UVC emission in devices with doubled-annealed templates.

This is reflected in the CW output power at 50 mA, which increases from 0.28 mW for the 232-233 nm LED grown on the MOCVD-grown AlN template to 0.44 mW and 0.73 mW for the devices grown on double annealed templates with and without an AlN MOCVD-grown overlayer, respectively.

Knauer says that the team could increase the output power by: replacing the absorbing *p*-side contacts by reflecting contacts; increasing outcoupling, via the introduction of nano-patterned sapphire; and processing arrays of micropixel LEDs.

REFERENCE

➤ A. Knauer *et al*. Appl. Phys. Lett **122** 011102 (2023)

Passivating GaN with ruthenium

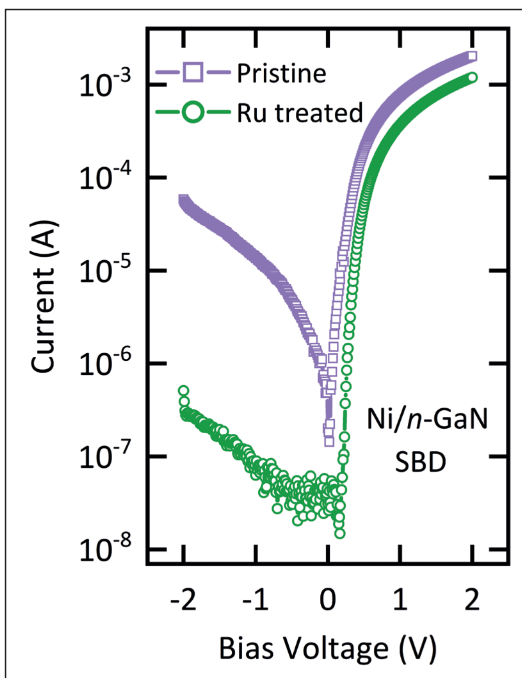
Schottky diodes deliver improved performance when a ruthenium solution is used to passivate the surface of GaN

A TEAM from India is pioneering the use of a ruthenium solution to passivate the surface of GaN.

Effective passivation is crucial to optimising performance of GaN devices, as it eradicates defects such as oxygen impurities and nitrogen vacancies, causes of high gate-leakage currents.

The researchers – from Kurukshetra University, the University of Petroleum and Energy Studies and the Inter-University Accelerator Centre – have demonstrated the benefits of ruthenium treatment with GaN Schottky barrier diodes. Treated devices show considerably better performance, including a significant reduction in leakage current.

Spokesman for the team, Ashish Kumar, who is affiliated to both the University of Petroleum and Energy Studies and the Inter-University Accelerator Centre, told *Compound Semiconductor* that the team has been looking at the impact of ruthenium on GaN for many years. In 2014, they published a paper reporting the results of investigations with X-ray photoelectron spectroscopy; and now they are unveiling the findings of a study involving the use of scanning tunnelling microscopy and photoluminescence.



➤ Current-voltage plots highlight the reduction in the leakage current provided by passivation with ruthenium.

One of the benefits of using ruthenium for passivation is that it has a small atomic radius, which aids chemisorption on the GaN surface. A monolayer of ruthenium results from passivation, preventing atmospheric oxygen from forming bonds with gallium and nitrogen atoms.

"Ruthenium can have positive as well as negative oxidation states, so it can make stable bonds with both anions and cations," explains Kumar, a claim confirmed by X-ray photoelectron spectroscopy, which revealed Ga-Ru and N-Ru bonds.

The latest study involved *n*-type, single-crystalline GaN with a thickness of 500 μm and a carrier concentration of 5.6×10^{17} cm^{-3}, according to Hall effect measurements. Prior to passivation, samples were: ultrasonically cleaned in trichloroethylene, acetone and isopropanol, each for 10 minutes; rinsed with deionised water; dried under nitrogen gas; and etched in hydrochloric acid to remove the native oxide. Passivation resulted from dipping these pristine samples in a solution containing equal volumes of $RuCl_3$ (0.05 M) and HCl (0.1 M).

Photoluminescence measurements on passivated and pristine samples revealed a doubling in the intensity of emission after treatment in ruthenium solution for 1 minute, and a small further enhancement when extending this process to 5 minutes.

Kumar and co-workers also used scanning tunnelling microscopy to compare passivated and pristine samples of GaN. Mapping areas of 62 nm by 62 nm revealed that ruthenium treatment altered the surface features.

Plots of tunnelling spectra – the current as a function of the bias voltage of the tip – showed that after chemical treatment, a dielectric layer is induced on GaN surfaces. This layer reduced tunnelling, and shifted behaviour at negative voltages, possibly due to a neutralising of defect states and the accumulation of charge carriers in the conduction band near the surface. The implication is that the position of the Fermi level changed, turning into the conduction band at the sample surface.

To demonstrate the effectiveness of their passivation process, Kumar and co-workers fabricated Schottky diodes on pristine GaN, as well as that subjected to ruthenium treatment. Measurements showed that passivation increased the Schottky barrier height from 0.78 eV to 0.91 eV, decreased the ideality factor from 1.42 to 1.12, and reduced the leakage current at reverse bias by around two orders of magnitude.

Kumar says that the team plans to continue its studies of passivation, using deep-level transient spectroscopy and time-dependent investigations.

REFERENCE

➤ N. Kumar *et al*. Appl. Phys. Lett **122** 013503 (2023)

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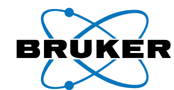
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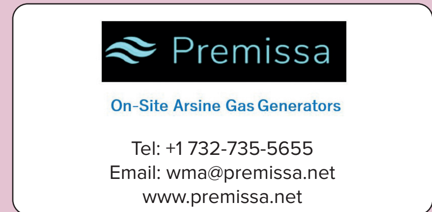

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