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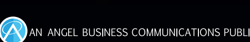
VOLUME 30 ISSUE I 2024



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AlN diodes and transistors deliver high breakdown voltages and operation at incredibly high temperatures

Integrating III-Vs and silicon
To draw on the benefits coming from scaling, silicon and the III-Vs must be united via epitaxy and processing in silicon fabs

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VIEWPOINT

By Richard Stevenson, Editor

The power puzzle

IF YOU ARE a device designer, the material that you'll use is often beyond question. If you are going to design a laser for long-haul optical links, it is incredibly unlikely that you'll look beyond InP; if you are working on the architecture for a powerful RF source, it is sure to revolve around GaN-on-SiC; and if you want a source of emission in the deep-UV, the standout design is an LED based on AlGaN – that's the primary rival to the mercury-based lamp.

But when it comes to power electronics, the situation is far more complex, and evolving. Today GaN-on-silicon dominates at relatively low voltages, thanks to its competitive pricing and its superior performance to the silicon devices it's displacing, and efforts are underway to increase market penetration at higher voltages, such as 650 V and a kilovolt or so. That's a domain where SiC MOSFETs and Schottky barrier diodes are currently having much success.

As well as the battle for this particular domain, efforts are underway to develop devices operating at even higher voltages. In contention are devices based on GaN and SiC, as well as those made from Ga_2O_3 and AlN, with progress on all fronts reported at the most recent International Electron Devices Meeting (IEDM), held in San Francisco in mid-December.

One reason why it's hard to pick a winner at this stage is that all the candidates have significant strengths and weaknesses. For example, extending the SiC MOSFET to higher voltages leads to a much higher on-resistance and ultimately high switching losses.

Much of the progress reported at IEDM has involved innovative device architectures. For example, a team from China and Japan realised 5 kV GaN HEMTs that are free from multiple field plates by introducing an active-passivation design that's based on a thinned *p*-GaN layer.

Of all the novel power devices presented at the most recent IEDM (see pages 28 to 33 for my report), the design that impressed me the most is the first superjunction device made from Ga_2O_3. Superjunction structures demand charge-balancing, a difficult feat with Ga_2O_3, due to its lack of *p*-type doping. To overcome this issue, a US team paired Ga_2O_3 with NiO – the latter offers a far higher level of doping, thereby allowing the use of much thinner layers. Superjunction Schottky rectifiers sporting this design and featuring 1.8 μm-wide Ga_2O_3 pillars wrapped in 120 nm-thick NiO can block 2 kV, and are said to set a new benchmark for the trade-off between blocking voltage and specific on-resistance.

It's impossible to say if this particular device, or the others that I've reported on, will go on to realise great commercial success. But it's going to be fascinating to watch the race unfurl over the coming years, and see which designs kick on to generate substantial sales for the power electronics industry.

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CONTENTS

VOL. 30 ISSUE I 2024

20 Agnitron's new showerhead: Advancing MOCVD technology

A novel showerhead featuring innovative gas injection accelerates MOCVD growth while expanding the palette of epitaxial materials to include AlScN

28 Pushing the power envelope

Novel designs enrich the performance of power devices employing a range of semiconducting materials

34 How to integrate silicon and III-Vs

To draw on all the traditional benefits that come from scaling, silicon and the III-Vs must be united via epitaxy and processing in silicon foundries

40 Nanowires for UVC emission

AlN nanowires with short-period superlattices based on AlN and GaN are trailblazing a path to a new class of UV-emitting devices

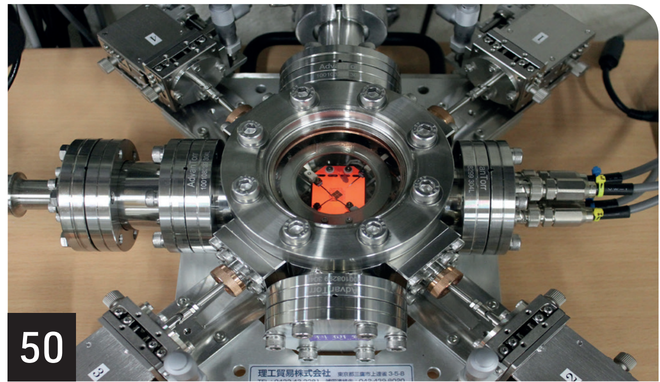
46 Extremely high-power transmitters for access networks

Sources that combine a laser, a modulator and an amplifier in a single device are laying the foundations for high capacity access networks

50 Extreme-temperature devices using AlN

Diodes and transistors with AlN channels deliver high breakdown voltages and operation at incredibly high temperatures

34



50

NEWS & MARKET ANALYSIS

12 A Clas-SiC case of evolution
With a new CEO set on pursuing bold plans for expansion, is Clas-SiC changing course?

14 The world's biggest SiC fab
Infineon's construction of the world's largest SiC fab, in terms of both its footprint and its capacity, remains on track for opening in the third quarter of this year

16 Challenges for high-volume microLED manufacturing
Despite strong momentum, most microLED manufacturers are still experiencing delays in ramping volumes

RESEARCH REVIEW

56 The case for better templates

57 Advancing vertical GaN diodes

58 Accelerating the AlGaN HEMT

NEWS

06 Renesas to acquire Transphorm

07 Acquisitions in power

08 VCSEL research centre opens in Italy

09 Infineon and Wolfspeed extend SiC wafer agreement

10 BluGlass completes GaNWorks acquisition

11 Rohm and Toshiba to collaborate on power devices

Editor Richard Stevenson
richardstevenson@angelbc.com
+44 (0)1291 629640

News Editor Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Director of Logistics Sharon Cowley
sharon.cowley@angelbc.com
+44 (0)1923 690200

Senior Sales Executive
Jacob Caulfield
jacob.caulfield@angelbc.com
+44 (0)2476 718979

Marketing & Logistics Executive
Eve O'Sullivan
+44 (0)2476 823 123
eve.osullivan@angelbc.com

Circulation
Scott Adams
scott.adams@angelbc.com

Publisher Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

USA Representatives
Brun Media
Janice Jenkins
jjenkins@brunmedia.com
+1 724-929-3550

Tom Brun
tbrun@brunmedia.com
+1 724 539-2404

Chief Executive Officer
Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

Chief Technical Officer
Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Directors
Jackie Cannon, Sharon Cowley

Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

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Renesas to acquire Transphorm

Acquisition will provide Renesas with in-house GaN technology

RENESAS will acquire GaN specialist Transphorm for approximately $339 million. The acquisition will provide Renesas with in-house GaN technology, expanding its reach into fast-growing markets such as EVs, computing (data centres, AI, infrastructure), renewable energy, industrial power conversion and fast chargers/adapters.

Renesas has recently announced the establishment of an in-house SiC production line, supported by a 10 year SiC wafer supply agreement. The addition of Transphorm will expand its wide bandgap portfolio with GaN technology and expertise.

Demand for GaN is predicted to grow by more than 50 percent annually, according to an industry study. Renesas says it will implement Transphorm's auto-qualified GaN technology to develop new enhanced power solution offerings, such as X-in-1 powertrain solutions for EVs, along with computing, energy, industrial and consumer applications.

"Transphorm is a company uniquely led by a seasoned team rooted in GaN power and with origins from the University of California at Santa Barbara," said Hidetoshi Shibata, CEO of Renesas. "The addition of Transphorm's GaN technology builds on our momentum in IGBT and SiC. It will fuel and expand our power portfolio as a key pillar of growth, offering our customers the full ability to choose their optimal power solutions."

"Combined with Renesas' world-wide footprint, breadth of solution offerings and customer relationships, we are excited to pave the way for industry-wide adoption of WBG materials and set the stage for significant growth. This transaction will also allow us to offer further expanded services to our customers and deliver significant immediate cash value to our stockholders," said Primit Parikh, co-founder, president and CEO of Transphorm and Umesh Mishra, co-founder and CTO of Transphorm. "Additionally, it will provide a strong platform for our exceptional team to further Transphorm's leading GaN technology and products."

The transaction is expected to close in the second half of calendar year 2024, subject to Transphorm stockholder approval, required regulatory clearances and the satisfaction of other closing conditions.

Pictured above: Transphorm CEO Primit Parikh and Renesas CEO Hidetoshi Shibata.

Kopin and Micledi to collaborate on microLED displays

OPTICAL SYSTEMS firms Kopin Corporation and Imec spin-out Micledi Microdisplays have agreed to work together to design, develop, and manufacture microLED displays to provide a more immersive and information-rich AR experience for use in high-brightness light conditions.

The program will use Micledi's CMOS production flow and Kopin's backplane control and driving capabilities, along with its experience in manufacturing complete display systems, to create full colour microLED displays integrated with advanced CMOS technology for high-performance defence, enterprise, consumer, and medical systems.

"The demand for AR solutions, particularly for defence programmes, has never been higher as users desire more immersive and information-rich experiences," said Bill Maffucci, senior vice president for business development and strategy at Kopin. "Micledi's microLED technology, combined with Kopin's advanced backplane design capabilities, aims to create microLED displays that address the demanding needs of emerging applications without the deficiencies of current technologies."

"We are pleased with Kopin's adoption and co-development of our disruptive AR display technology," said Sean Lord, CEO at Micledi. "To enable optimum microdisplays for AR, we believe Micledi has developed the world's first solution for microLED manufacturing in a 300 mm CMOS line, which allows integrating both a controller ASIC and

an emitter module on a 300 mm wafer in a highly efficient, high volume, and low-cost manufacturing flow."

Lord added: "Unique solutions can be tailored to the particular requirements of each end-use system, making Micledi 's microLEDs manufactured in collaboration with Kopin's backplane and system integration skills, applicable to a variety of specialised AR microdisplay systems."

Acquisitions in power

Interest in GaN technology for cars is driving buyouts, says Yole

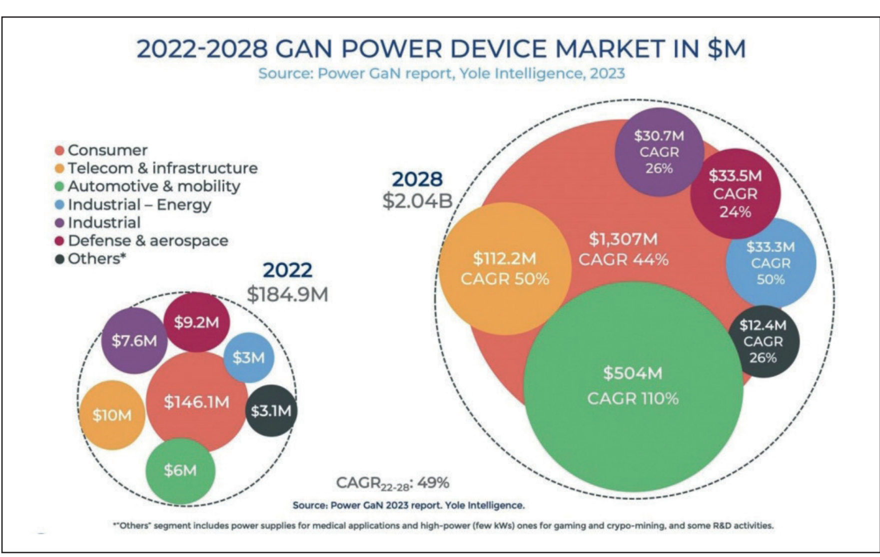
IN THE POWER GaN industry's second major acquisition in a year, following Infineon Technologies' purchase of GaN Systems, US-based Transphorm is to be acquired by a subsidiary of Renesas Electronics Corp of Tokyo, Japan. The acquisition adds to the billions of dollars invested in the power GaN industry since 2019 through partnerships, the construction of facilities, and M&As.

Yole Group's experts Milan Rosina and Taha Ayari say the automotive market is driving this activity. This sector, to be worth $504 million by 2028, is attractive for players such as Renesas and Infineon, because it experiences higher margins and ROIs than the consumer sector.

The trend toward more integrated systems is notable in electric vehicles in particular, where OEMs are moving from today's 3-in-1 unit that integrates an EV drive motor, gearbox and inverter – to 5-in-1 or even 8-in-1 systems that also include power electronics controls such as DC-DC converters and on-board chargers. This is where the major opportunity lies for GaN to offer a high level of perceived value in reducing system costs, weight, volume and power losses.

Transphorm's automotive-qualified GaN technology was mentioned explicitly by Renesas as a reason for its purchase, to enable the development of enhanced power solutions for EVs. This followed Renesas' already strong ambition in targeting integrated power solutions for EVs with a recent partnership with Nidec, which will see the companies develop a 6-in-1 E-Axle.

Like Transphorm, GaN Systems has significant strength in the automotive sector, which was a major reason behind the Infineon acquisition in 2023. However, at $830 million, Infineon paid more than double the $339 million Renesas paid for Transphorm. With the two companies similar in size, with a



comparable market share, and strong GaN expertise and IP – what could be the reason behind the stark difference in value?

Could it be that GaN System's design-win pipeline is more attractive than Transphorm's? In the automotive sector alone, it has partnerships with Hella, Vitesco, Canoo, among others.

Unlike Renesas, Infineon already has in-house GaN capacity, so the upcoming business it could gain through design-wins is likely a big justification. And, thanks to design centres in Canada, the US, China and Taiwan, GaN Systems is in good stead to secure more of this type of business in the coming years. In this way, Infineon is playing the long game to secure a leadership position in the power GaN industry.

In contrast, it is likely that Renesas is satisfied with the in-house IP and GaN device production capacity it will gain (through Transphorm's epitaxy capabilities and its interest in GaNovation's AFSW wafer-fab). It is noteworthy that this AFSW fab is located in Japan, which may be considered as an advantage for Renesas to profit from a local GaN fab ready for high-volume production.

Renesas already has experience on GaN technology, working with EPC and GaN Systems (now an Infineon company) to develop systems like DC-DC converters and even space-grade devices (following the acquisition of Intersil). Upon the completion of Transphorm, Renesas will have a complete power electronics portfolio, with power ICs, silicon power devices, SiC devices – after investing $2 million in Wolfspeed to guarantee a 10-years SiC wafer supply – and Transphorm's GaN products. Renesas is now on track to compete with the leading power electronics players such as Infineon and STMicroelectronics.

Nevertheless, there is still a question as to whether the acquisition, expected to close by mid-2024, will be approved, particularly with Transphorm's work with the US government on several funded projects that can be related to defence.

In the next 5-10 years, IDMs are expected to become the dominant force in the power GaN ecosystem. While some fabless companies will co-exist by expanding into different markets – for example Navitas, which has entered the SiC sector by acquiring GeneSiC – Yole Group's analysts expect to see more M&As.

VCSEL research centre opens in Italy

Centre of excellence will focus on applications in high-speed optical fibre data transmission links and optical sensing

VCSELence Torino, Italy, has been established as a centre of excellence for VCSELs in applications in high-speed optical fibre data transmission links and in optical sensing.

Relying on a well-established physical and technological background of VCSELs, VCSELence targets the experimental exploitation of these devices, pushing the application beyond the current limits. This will be achieved by performing highly sophisticated modelling of the in-laser phenomena supported by in-house experiments, with final tests of the device in the entire system.

VCSELence Torino unites the competences of several participating groups at DET (Department of Electronics and Telecommunication at Polytechnic University of Turin) at LINKS Foundations and at IEIIT-CNR (Institute of Electronics and Information and Telecommunications Engineering of the National Research Council).

All specialise in the fields of optical, electrical and spectral characterisation, modelling and advanced applications of semiconductor lasers covering all wavelengths for optical communication bands and for optical sensing.

The scientific goal is to advance the understanding of the dynamics of the coupled photon-carrier system in these opto-electronic emitters by joint theoretical and experimental investigations.

This will allow the realisation of improved devices designed on-demand, exploiting their ultimate limits and going far beyond the actual state-of-the-art.

VCSELence Torino will also be offering its services in modelling, design,

characterisation and system testing on a worldwide platform, to drive international research, and collaborative opportunities with innovative companies.

VCSELence Torino relies on an already existing large variety of European and world-wide funded projects with universities and companies and it intends extending them to the benefit of society.

VCSELence also builds on the existing photonics infrastructure of Links and Photonext (Interdepartmental Centre for Applied Photonics of Polytechnic University of Turin) where it shares a 300 m^2 lab and expresses the intent to become a significant player in the development of knowledge and expertise in the field of application of semiconductor technologies that will give benefit to Italy's economy.

It is expected that the new centre will also play an important role in advancing quantum physics-based technology.

Pierluigi Debernardi of CNR, with 25-years of experience on VCSELs, added: "Our Center of Excellence will be the research building for all scientists involved in modelling, design, technology and application of these low-cost semiconductor lasers, working together on the advancing of semiconductor optics research and optoelectronics".

Purdue University wins SiC patent lawsuit against ST

PURDUE UNIVERSITY has won its patent infringement lawsuit against STMicroelectronics. US patent 7,498,633 covers technology involving SiC semiconductors invented by Purdue's James Cooper and his graduate student/ postdoctoral researcher Asmita Saha.

On Dec. 4, a jury returned a verdict in Purdue's favour, finding that ST infringed the patent by selling infringing SiC semiconductors. The jury awarded Purdue $32.5 million in past compensatory damages, plus a running royalty on future sales.

"Winning this case is a great victory for Purdue," said Brian Edelman, Purdue Research Foundation (PRF) president. "As the university's tech transfer and commercialisation arm, we take managing and protecting Purdue intellectual property very seriously, and we hold ourselves and others accountable to the highest standards. Our preference is to reach a licensing agreement, but we have a moral obligation to protect Purdue IP, and that includes going to court to defend our rights. The jury recognised this semiconductor research from Purdue researchers, and the decision is great news for the inventors, Purdue University and Purdue Research Foundation."

Under the Bayh-Dole Act, contractors of inventions arising from federal government-funded research, such as US universities, own, patent and commercialise inventions through licensing. At Purdue, revenues from licensing are distributed among the inventors, their affiliated departments and the Purdue Research Foundation, which reinvests back into the commercialisation and innovation ecosystem.

Infineon and Wolfspeed extend SiC wafer agreement

Extended partnership includes a multi-year capacity reservation agreement

INFINEON and Wolfspeed have expanded and extended their existing long-term 150 mm SiC wafer supply agreement, originally signed in February 2018.

The extended partnership includes a multi-year capacity reservation agreement. It contributes to Infineon's general supply chain stability, also with regard to the growing demand for SiC semiconductor products for automotive, solar and EV applications and energy storage systems.

"As the demand for SiC devices continues to increase, we are following a multi-source strategy to secure access to a high-quality, global and long-term supply base of 150 mm and 200 mm SiC wafers. Our prolonged partnership with Wolfspeed further strengthens Infineon's supply chain resilience for the coming years," said Jochen Hanebeck (pictured right), CEO of Infineon Technologies. "We have been working with Wolfspeed for more than 20 years to bring the promise of SiC to the automotive, industrial and energy markets, and to help customers leverage this energy-efficient technology to foster decarbonisation."

The adoption of SiC-based power solutions is rapidly growing across multiple markets. SiC solutions enable smaller, lighter and more cost-effective designs, converting energy more efficiently to unlock new clean energy applications.

To better support these growing markets, Infineon is continuously diversifying its supplier base to secure access to high-quality SiC substrates.

Wolfspeed president and CEO Gregg Lowe said: "Industry estimates indicate demand for SiC devices, as well as the supporting material, will grow substantially through 2030, representing a $20 billion annual opportunity. We are very pleased to continue our partnership with Infineon and to serve as a major supplier of SiC wafers in the years ahead."

BluGlass completes GaNWorks acquisition

Completion follows successful installation and validation of GaN wafer processing equipment at the Silicon Valley fab

BLUGLASS has completed its acquisition of contract manufacturer GaNWorks Foundry, following the successful installation and validation of GaN wafer processing equipment at the company's laser production fab in Silicon Valley.

BluGlass says that testing has confirmed the *n*-side wafer metalisation, wafer thinning, and bar cleave equipment is meeting GaNWorks' operational benchmarks in-house. Product validation of new GaN lasers made at BluGlass' Silicon Valley fab is also underway, and wafer fab vertical integration is now complete.

BluGlass CEO Jim Haden said; "Our acquisition of GaNWorks' specialist wafer processing equipment, manufacturing process transfer, and experienced GaN engineers, will fast-track development and production cycles, and deliver significant cost savings over the long-term.

Haden added: "We have moved quickly to bring these complex processes in-house, having now completed process verification tests, and commenced validation of our first vertically integrated laser lots."

According to Haden, BliuGlass is already seeing the benefits of having all processes in-house under operational control. This enables quick identification of additional process optimisation opportunities, which are expected to significantly enhance production yield, reliability, and throughput.

BluGlass is continuing to refine processes across its manufacturing supply chain to improve laser performance.

Coherent introduces VCSEL-based illumination platform

COHERENT has introduced an illumination module platform for short- and mid-range lidar in automotive safety and robotic vision in industrial applications.

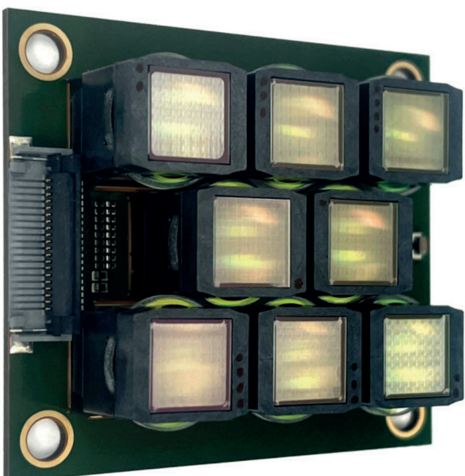
Using eight 940 nm VCSEL modules, the company has demonstrated a solution with several selectively addressable horizontal slices of the field of illumination.

In addition to offering a compact form factor and high power-conversion-efficiency, the module is said to be a much lower-cost alternative than using large addressable VCSEL arrays.

Coherent has a demonstrator available for its customers to explore multiple VCSEL module positioning configurations and scanning algorithms for various depth-sensing modalities and types of scenery.

"A powerful aspect of the module platform is the ability to customise an optimized solution for use cases requiring up to 30 meters of depth sensing in bright daylight. Our illuminators exceed 30 percent total power conversion efficiency and have a compact footprint, only about a third of the size of a credit card," said David Ahmari, VP and general manager, Optoelectronic Devices & Modules Business.

"To achieve this breakthrough in efficiency and size, we are leveraging our state-of-the-art five-junction VCSEL technology that enables each illuminator module to achieve up to 200 W of output power."



Customers of Coherent will be able to adjust the duration of the driving pulses to achieve both short- and mid-range lidar sensing. The FOI slices are dynamically selectable depending on the number of VCSEL modules and the order in which they are scanned. A voltage supply of only 21 V is required, which is much lower, and therefore more efficient, than existing lidar technology.

Rohm and Toshiba to collaborate on power devices

METI recognises joint silicon and SiC production plan as supporting stable, secure supply

AS A MEASURE towards a secure and stable semiconductor supply, Japan's Ministry of Economy, Trade and Industry (METI) has approved a plan by Rohm and Toshiba to collaborate on the manufacture and increased volume production of SiC and silicon power devices.

Current demand for power devices is expected to see continued growth as automotive and industrial applications shift towards greater electrification and efficiency.

For Rohm (one of the first mass producers of SiC MOSFETs), its SiC business is a priority project, with aggressive investment to increase production capacity.

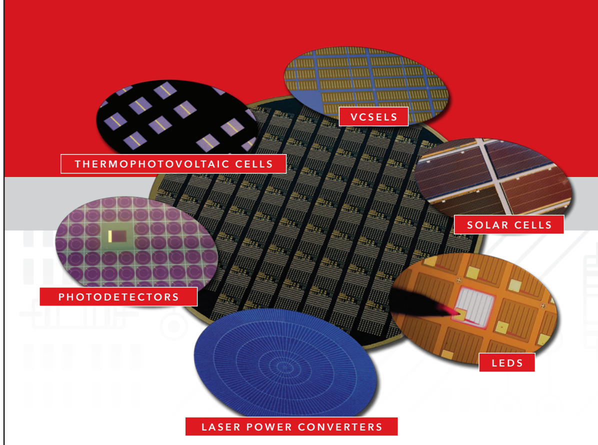
Toshiba Electronic Devices & Storage has for decades supplied silicon power devices, mainly for automotive and industrial markets. The company started production on a 300mm wafer line last year, and is accelerating investment to enhance capacity. It is also advancing development of a wider lineup of SiC power devices, especially for automotive and power transmission and distribution applications.

Under intensifying international competition in the semiconductor industry, Rohm and Toshiba have been considering collaboration in the power device business for some time, and that resulted in the joint application.

Rohm and subsidiary Lapis Semiconductor will invest around $2 billion.

Toshiba Electronic Devices & Storage and its subsidiary Kaga Toshiba will invest around $677 million. The maximum government subsidy is $885 milion, which is one-third of the total investment amount.

Production sites will be Kaga Toshiba for silicon power devices, and Lapis Semiconductor Miyazaki Plant No.2 for SiC power devices and SiC wafers.



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A Clas-SiC case of evolution

With a new CEO set on pursuing bold plans for expansion, is Clas-SiC changing course?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

INITIAL ENCOUNTERS can be misleading. At times first impressions are misguided, to be replaced with a far more informed view after digging a little deeper.

That could be the case for many following the fortunes of Clas-SiC, the Scottish SiC fab. It has just announced the appointment of a new CEO, who only joined the company as chief operations officer in summer 2023; and ambitious plans are now being touted for a major expansion, both in capacity and the technology portfolio.

However, go behind the headlines and what at first glance appears as a couple of major changes is actually a continuation along the same trajectory. The new CEO, Jen Walls, is an old hand, who devoted many years to helping lead Raytheon's SiC foundry services, from which Clas-SiC spawned. And when Walls joined Clas-SiC, her accession to CEO was already part of the company plan, and given that turnover has doubled in the last 12 months, efforts to increase capacity are a logical, natural progression.

Another contributor to continuation, rather than change, is retaining the three major strands of the company. "We have fast turnaround prototyping; low-to-medium volume manufacturing; and we also operate a licencing and royalty arm to the business, to give customers that have more capacity-hungry devices a route to high-volume manufacturing," says Walls.

One strength of this three-pronged approach is that it enables Clas-SiC to work with a wide range of customers from all over the globe. They include those that have gone no further than developing prototypes, and benefit from the reassurance that Clas-SiC can support their entire product lifecycle; and those that have already developed their SiC

➤ Karen Millar, Production Supervisor, and CEO Jen Walls, checking status of the high- temperature annealer.

technology, and want to progress to low rate production.

An engineering pedigree

Walls has devoted most of her career to engineering. As a teenager she won an engineering scholarship at Exxon Chemicals, enabling her to study integrated engineering at the local college on a block release basis while working at the ethylene plant.

"When I graduated, the oil industry was in downturn, but thankfully Scotland's silicon Glen was booming," recollects Walls. "So, my semiconductor journey started with NEC semiconductors, as a photo equipment engineer. I then moved into NEC's new 200 millimetre fab in Livingston, which at the time was the largest, most advanced fab in Europe."

When this fab closed in 2001, Walls moved to Raytheon, where she progressed through the ranks to take management positions while completing an MBA. She views the highlight of her time there as her role as SiC business manager, leading the process development team. However, she could not accomplish all she hoped for, because Raytheon did not give the SiC division the freedom it needed to thrive: "I always wanted the silicon carbide foundry within the defence company to be a standalone business," says Walls.

Seeking a new challenge, she started work as a business manager in the health sector, a role that allowed her to continue to draw on her engineering and manufacturing skills. "However, it never gave me the same fire in my belly. I always knew I would be back in the industry."

And six years later she was, when in July 2023 she joined Clas-SiC and resumed a working relationship with many colleagues from her time in the SiC division at Raytheon.

While preparing to take over from the outgoing CEO, Rae Hyndman, who is moving into retirement, Walls focused on trying to improve operational execution.

"It's worked extremely well," says Walls. "It's allowed me to make sure I fully understand the workings of the operation here at Clas-SiC, and it's allowed me to build a relationship with customers and employees, and importantly as well, the Clas-SiC board."

Viewing the change in CEO as evolutionary rather than revolutionary, Walls has much praise for Hyndman, whom she credits for taking the company from conception back in 2017 to qualification and then rapid growth, including an increase in headcount from 24 to the 80 employees today.

➤ The new CEO, Jen Walls, supporting Senior Equipment Engineer Graeme Dickson.

"Clas-SiC has grown extremely quickly," says Walls. "We're about a year ahead of where we thought we would be under the leadership of Rae."

A legendary supporter

As well as benefitting from the support of the outgoing CEO, Walls is grateful for the guidance of the executive chairman, Carl Johnson, who cut his teeth founding II-VI more than 50 years ago, and led that company for more than 30 years.

"I have weekly goal and mentoring sessions with Carl," says Walls. "He has a wealth of experience and always brings a valued perspective to the table."

Walls is taking over the reins in an enviable position, with 70 percent of the fab capacity for 2024 already allocated. This healthy orderbook is partly behind the decision that now is the right time to expand.

"We're looking for about a £24 million investment," says Walls. "That will take our capacity to 2.5 times where we are today." The funding will be used to expand the clean room space and purchase additional tools for future process development and operational resilience.

Efforts in this direction are already underway. "Just now we are working on our 3.3 kV process design kit for MOSFETs," enthuses Walls.

With the chance to lead a growing company developing exciting new technologies, it's of no surprise that Walls is clearly revelling in her return to an engineering company.

> One strength of this three-pronged approach is that it enables Clas-SiC to work with a wide range of customers from all over the globe

The world's biggest SiC fab

Infineon's construction of the world's largest SiC fab, in terms of both its footprint and its capacity, remains on track for opening in the third quarter of this year

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN the SiC industry, much manufacturing takes place in-house. So, when these chipmakers want to increase production, they tend to boost internal capacity. That's in full flow right now, spurred on by the tremendous ramp in sales of electrical vehicles, which deploy SiC power devices in the on-board charger and DC-DC converter.

One of the companies grabbing the headlines for capacity expansion is the power-electronics giant Infineon, which lays claim to constructing the world's biggest 200 mm SiC fab, in both size and capacity. Initially backed by €2 billion of internal funding, plans for the new fab in Kulim, Malaysia, were bolstered last summer with the injection of a further €5 billion for building and equipment.

Back then the company announced that the completion of the first phase of this fab remained on track for the third quarter of 2024, a deadline that's still on schedule, according to Ng Kok Tiong, Senior Vice President and Managing Director of Infineon Technologies Kulim. Over the next five years the completion of the second phase will proceed. Infineon's new SiC power fab, known as Kulim 3, is being built next to a pair of its 200 mm silicon

Construction of Kulim 3, the world's biggest 200 mm SiC fab, is well underway.

fabs. However, even those fabs, constructed in 2006, were not the beginning of off-shoring of manufacturing by the European powerhouse in Malaysia. Through Siemens, which divested Infineon in 1999, there has been investment in Malaysia for almost 50 years, including the construction of a back-end assembly and test facility in another state, Malacca. The combination of fabs in Malaysia gives Infineon end-to end production within the country. In fact, the investment in semiconductor manufacturing is so strong that Infineon has more employees in Malaysia than any other country, including Germany.

According to Ng, one of the reasons why Infineon decided to expand its SiC production capability by building a third fab at Kulim is that this offers a very fast way to ramp capacity. That's partly because compared with other countries, approval can be granted for construction to take place during more hours of the day, thanks to local labour law.

One difficulty with building any new fab is winning approval for the water and electricity that's supplied to the site. Ng believes that this has been granted quickly for Kulim 3. Building a new fab next to existing ones helps, but in addition to that, Infineon benefits from having a large, welcomed presence in Malaysia.

"We are working very well with the government, with MIDA, which is the government agency for investment," remarks Ng, who adds that they get a lot of attention for any support that's needed.

Ng says that equipment will start being installed in Kulim 3 from April 2024, with production of SiC devices slated for the second half of the year.

Engineers at this fab will carry out all aspects on front-end processing, including production of SiC substrates from boules provided by five suppliers – two from China, two from the US, and one from Japan. Helping increase the margins associated with this process is the Cold Split technology that Infineon acquired from Siltectra in 2018. "With this new technology you can reduce some of the losses of the raw material," says Ng.

Construction of the 200 mm SiC fab is expected to create 900 jobs, with the vast majority taken by local people. To help with the training of Malaysian engineers, many are sent to Infineon's other SiC fab, located in Villach, Austria. In addition, experts from there visit the facility in Kulim.

To help attract the best local talent, the Kulim fab works very closely with local universities and polytechnics by offering placements for internship and final year projects. Ng and his colleagues have found that due to need for very specific expertise, even engineers graduating after a four-year programme can take 8 months of training before they can start making meaningful contributions. So, to avoid this delay, a programme has been

➤ Ng Kok Tiong is Senior Vice President and Managing Director of Infineon Technologies (Kulim) Sdn. Bhd., which is Infineon's first and only wafer fabrication plant in Asia. Ng is also currently the Chairman of the Semiconductor Fabrication Association of Malaysia.

introduced, with students spending time at the facility and having an engineer at the fab as a mentor. "By the time they graduate, they are already effective, because they know SPC, they know how to do the DoE, and things like that," says Ng.

Helping Infineon commit to investing in Kulim 3 are a number of design wins totalling €5 billion. They are roughly a 50-50 split between the electric vehicle and industrial sectors, with the latter a mix of solar and storage industries.

The plan is that by the end of this decade, production at both the Kulim and Villach sites will account for a 30 percent share of the SiC power market, which by then will be worth about €20 billion.

While emphasis is initially on SiC at Kulim 3, efforts are also underway to develop GaN products at this site. The first steps towards this, now underway, involves qualification of the growth process.

Based on all the plans for wide bandgap semiconductors at Kulim, there's no doubt that the long-term relationship between Infineon and Malaysia will only get stronger throughout this decade and beyond.

Helping Infineon commit to investing in Kulim 3 are a number of design wins totalling €5 billion. They are roughly a 50-50 split between the electric vehicle and industrial sectors, with the latter a mix of solar and storage industries

Challenges for high-volume microLED manufacturing

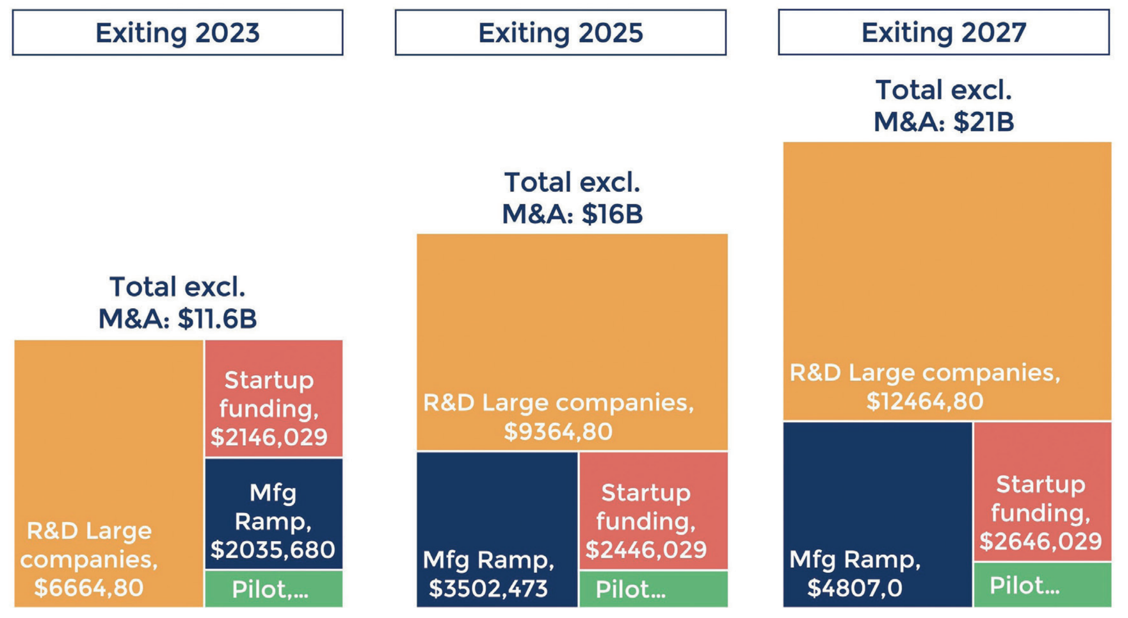
Despite strong momentum, most microLED manufacturers are still experiencing delays in ramping volumes

BY ERIC VIREY FROM YOLE INTELLIGENCE

THERE ARE MANY great attributes of displays based on microLEDs, which are miniature red, green and blue emitters with dimensions typically less than 50 μm. Thanks to independent control of every sub-pixel, displays based on microLEDs combine high-contrast, high-speed, and wide viewing angles – merits also found in OLED displays – with superior colours, better contrast, higher brightness, lower power consumption, longer lifetime, environmental stability and ruggedness. In addition, with microLED-based displays there is the possibility of integrating sensors and circuits, advances that would enable the production of thin displays with embedded sensing capabilities involving fingerprints, an in-display camera, a touch function and gesture control.

Spearheaded by efforts from Apple and others, microLEDs have generated tremendous excitement over the past decade. According to the *MicroLEDs 2023* report by our team at Yole Intelligence, $12 billion has been spent on efforts associated with microLED development and industrialisation, and another $2.4 billion on mergers and acquisitions. While this is dwarfed by the building costs of OLED fabs since the mid-2000s, a expenditure totalling more than $100 billion, it's indicative of strong momentum. All display makers now have sizeable microLED efforts and the first commercial products are on the market, including a number of AR headsets and a TV from Samsung. Expected to join this list in the spring is a luxury watch from Tag Heuer.

More products are sure to follow, as the supply chain shapes up and more companies invest in manufacturing capabilities. Making headlines on this front is Osram, which is spending a billion dollars to build an 8-inch microLED fab in Kulim, Malaysia, to serve Apple's needs for an upcoming smartwatch. As one might expect, this is by no means the only microLED activity in Asia: Taiwanese holding company Ennostar is building a 6-inch fab; most leading display makers in China have aligned



➤ Figure 1. Cumulative investment in microLED development and manufacturing. Taken from *microLEDs report*, Yole Intelligence, 2023. Credit: Yole Intelligence

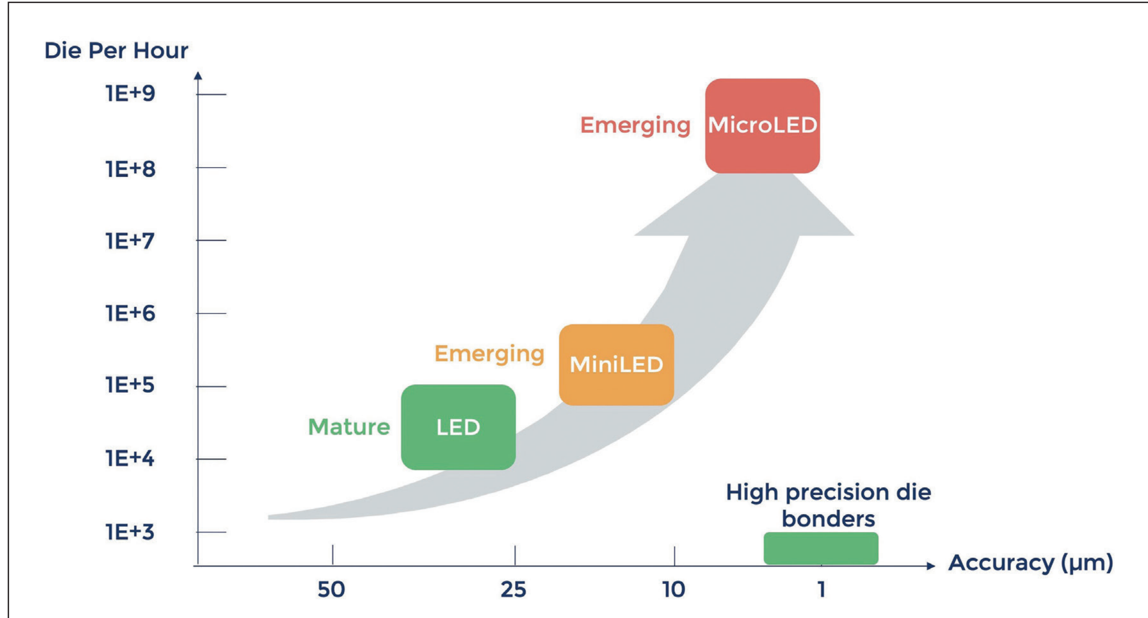


Figure 2. Required die assembly equipment capabilities for microLED vs. existing LED and miniLED solutions. Taken from *microLEDs report*, Yole Intelligence, 2023. Credit: Yole Intelligence

themselves with leading domestic producers of LEDs; and in Taiwan and South Korea, AUO and Samsung have started producing small volumes of smartwatch displays and microLED TVs, respectively. Some investments in microLED capability in China are substantial, with BOE spending $300 million to acquire a controlling stake in HC SemiTek, which is using the entire proceeds to build a 6-inch microLED fab, and Sanan is spending nearly $2 billion on a new fab, with $200 million earmarked for microLEDs. In addition, JBD has completed its construction of a $100 million, vertically integrated microdisplay fab near Shanghai, and Vistar has broken ground on a $413 million microLED display project.

However, progress is not keeping pace with schedules. Osram's fab, initially slated to ramp in 2024, is now expected to start in late 2025; and while Ennostar's first phase is on track for mid-2024, the second phase has been pushed back by one-to-two years, to 2026 or 2027. Note that these are by no means the only projects to experience delays. But why is it taking so long to bring microLEDs to consumers?

Mass transfer: a major hurdle

MicroLEDs are challenging. Making a display involves processing LED epiwafers into arrays of microLED chips, poised for transfer and integration into a heterogeneously integrated system incorporating LEDs, pixel-driving transistors, optics and so on.

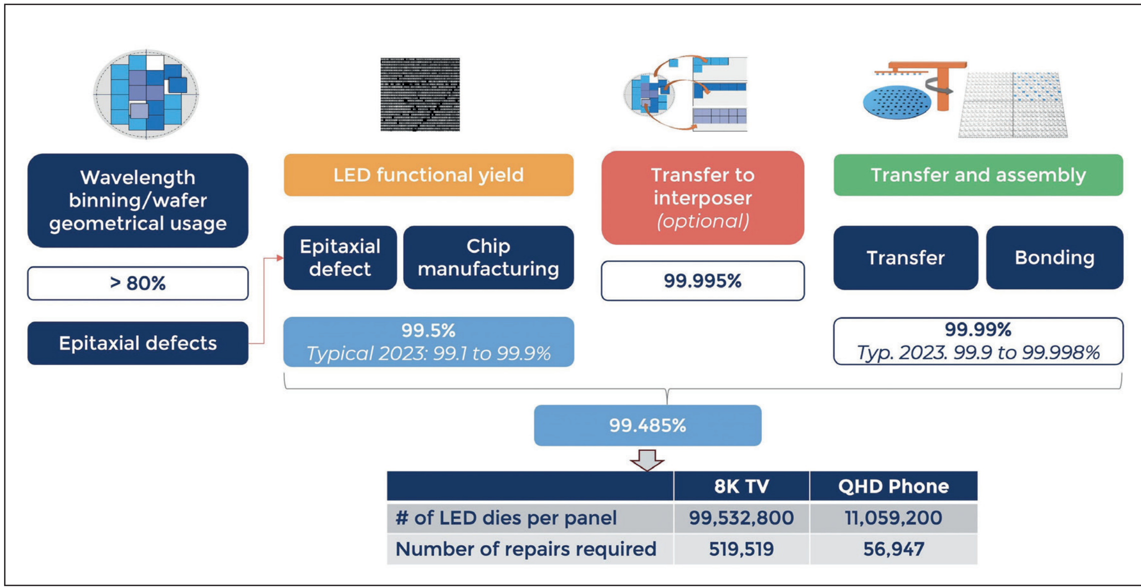
To manufacture a microLED display with an 8K resolution, which is 7680 pixels by 4320 pixels, requires the transfer and assembly of almost 100 million microLEDs with a placement accuracy of ±1 µm – and that must occur in less than 10 minutes to ensure economical viability. Unfortunately, today's LED and die bonders are incapable of manipulating the very small die deployed in high-volume consumer applications, and at the required level of precision their throughput is typically limited to no more than around 1,000 die per hour. At this pace it would take 11 years to manufacture a single 8K TV. Recently developed miniLED transfer equipment trims this time, but it is still longer than a week.

What's needed is a paradigm change: the development of mass transfer technologies that manipulate and assemble far smaller die at a rate five orders of magnitude faster.

The good news is that progress has been spectacular, to the point that many industry players no longer see it as a fundamental roadblock. Only three years ago, a company developing microLED displays had to invent its own mass transfer process and build its equipment. Now, more than a dozen off-the-shelf tools are available from equipment makers. These first-generation tools are suitable for development, pilot lines, and, in some cases, for a first product.

However, to ensure costs meet expectations, the microLED has to be shrunk below 10 µm. For

To manufacture a microLED display with an 8K resolution, which is 7680 pixels by 4320 pixels, requires the transfer and assembly of almost 100 million microLEDs with a placement accuracy of ±1 µm – and that must occur in less than 10 minutes to ensure economically viability



	8K TV	QHD Phone
# of LED dies per panel	99,532,800	11,059,200
Number of repairs required	519,519	56,947

Figure 3. Yield and repair in microLED display manufacturing. Taken from *microLEDs report*, Yole Intelligence, 2023. Credit: Yole Intelligence

example, the microLEDs that Apple will use in its smartwatch will be 6-8 µm. At those sizes, most tools struggle. Another challenge facing equipment makers is that their tools have to operate over large areas – at least 730 mm by 920 mm, and possibly up to 1500 mm by 1850 mm. These challenges associated with mass transfer are thought to be the culprit for Apple's smartwatch manufacturing ramp delay. This tech giant is working with a partner to develop a custom tool based on its proprietary MEMS-based technology.

Yield and repair

Another factor to consider alongside transfer and assembly is yield, which has impact on cost. With microLEDs, bad (dead) pixels can originate from either a faulty die, a missed or misplaced die during transfer, or a defective electrical connection. Today, transfer yields range from 3N (99.9 percent) to 5N+. Meanwhile, microLED chip yields are between 99 percent and 99.5 percent.

While those numbers initially appear impressive, they equate to half a million defective pixels in an 8K TV. As the eye is incredibly sensitive to defects, manufacturers must develop effective yield management strategies that combine pixel redundancies and/or individual pixel repair with chip and pixel testing and binning.

To limit repair needs, it is critical for makers of microLED-based displays to use testing and inspection to remove bad die from the process flow as early as possible. Assisting in this endeavour are multichannel probe-card testing tools, but their workload is daunting, as it will not be long before there are 500 million die on a single 8-inch wafer. Even today's best commercial probers would take more than 40 hours to test one of those wafers. A better option for very small high-density chips is massively parallel, contactless testing. A tool providing this form of testing has been introduced to market in 2023 by the Korean company Top Engineering, but its capability is still to be demonstrated in volume production. Note that in 2020 Apple acquired start-up Tesoro, with the aim of developing an in-house solution.

As well as the need for tools and technologies for microLED mass transfer and massively parallel contactless testing, there are other challenges. They include the driving of the microLED displays, a task that requires innovation, as it is not possible to simply use the drivers of OLED displays. Another hurdle is to improve the external quantum efficiency of the microLED, which can plummet when scaled to very small dimensions.

One may view a microLED display as a new, complex puzzle. While many pieces already exist, some are yet to be perfected – and they need to be brought together, with the last few kinks ironed out, which will take more time. It is only after yields and costs get close to target that the first consumer products will appear. The next two-to-three years are going to be critical, with Apple's smartwatch and Samsung's TV projects acting as incubators for the entire industry. That watch is now expected in 2026, and if it fails, this would be a massive and potentially fatal blow.

Nevertheless, there is very strong momentum for the microLED. However, its innovators cannot let up, because the OLED keeps improving, so there's a sense of urgency to accelerate commercialisation and secure some success before OLEDs get too entrenched in all major target applications.

FURTHER READING / REFERENCE

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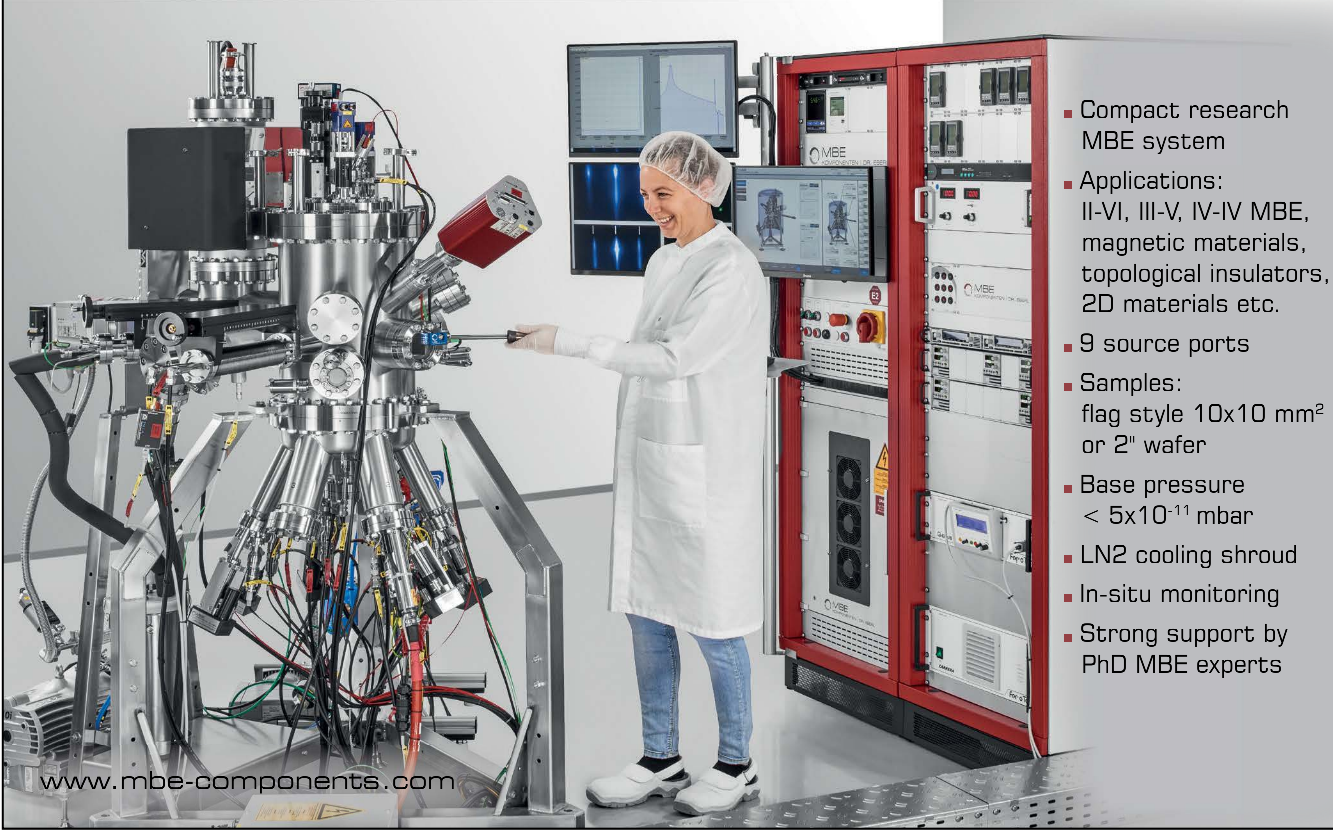
- *MiniLEDs 2023*, Yole Intelligence
- *MiniLED Displays 2023 - Performance and optical construction*, Yole Intelligence
- *Sony MicroLED display*, Yole Intelligence

OCTOPLUS 300
MBE System



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Agnitron's cutting-edge Gen III Close Injection Showerhead unlocks the potential of wide and ultra-wide bandgap materials by realising superior growth rates, unmatched uniformity and exceptional surface quality.

Agnitron's New Showerhead: Advancing MOCVD Technology

A novel showerhead featuring innovative gas injection accelerates MOCVD growth while expanding the palette of epitaxial materials to include AlScN.

BY AARON FINE, FIKADU ALEMA, WILL BRAND, VITALI SOUKHOVEEV, PAUL FABIANO AND ANDREI OSINSKY FROM AGNITRON

POWER ELECTRONICS is undergoing a transformation. Silicon is being replaced with the likes of GaN and SiC, members of a family of wide bandgap materials that are enabling devices to be smaller, more efficient and high-performing. But that's just the beginning, with the focus shifting to the new frontier of ultra-wide bandgap materials, primarily AlN and Ga_2O_3.

Collectively, silicon's superiors are grabbing an increasing share of the power device market, with total sales projected to to exceed $10 billion within just a few years. These high-performance alternatives are finding deployment in many sectors, including the military, electric vehicles, power supplies and photovoltaic inverters.

Playing a pivotal role within this dynamic landscape is our company, Agnitron Technology. We are developing and manufacturing an expanding portfolio of OEM semiconductor growth tools, including but not limited to MOCVD, CVD and HVPE technologies.

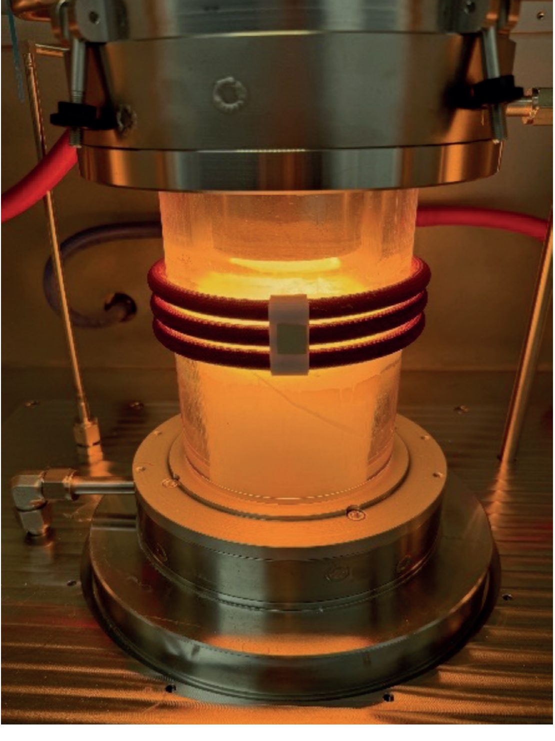
One of these three forms of deposition, MOCVD, is widely used for the manufacture of power electronics, as well as LEDs and lasers. This epitaxial growth technique, involving the deposition of substances onto a surface in a high-temperature chamber, ensures meticulous control of the film's thickness, its composition, and its quality. These assets make MOCVD ideal for crafting high-performance layered structures in various devices.

It's far from trivial to extend the use of MOCVD to the likes of AlN and Ga_2O_3, due to persistent hardware challenges. At Agnitron, we have recognised and started to address these specific challenges.

Gen III CIS

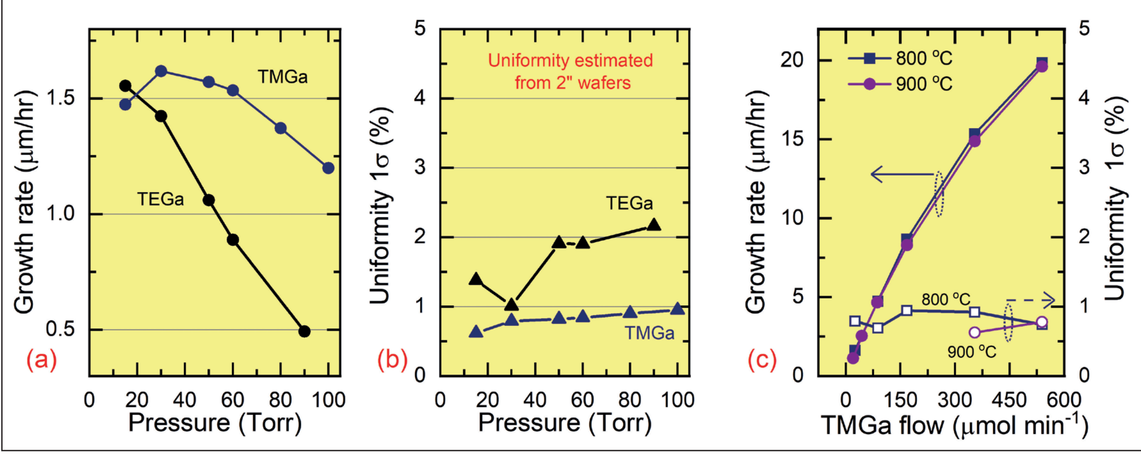
The biggest challenges in hardware design are associated with the showerheads, arguably the most crucial component for epitaxial semiconductor material growth. Traditional showerhead design focuses on facilitating multiple separate, consistent, uniform flows of temperature-regulated gases, by utilising various complex machining methods. Unfortunately, these designs result in expensive, fragile showerheads with a limited lifetime. Success has been held back by traditional manufacturing practices, which hamper efforts to realise faster growth rates, uniform film thickness and smooth surfaces – and the ability to grow films previously not possible with standard commercial MOCVD reactors.

Our team at Agnitron has broken through this impasse with an innovative, patent-pending showerhead technology that we incorporate into our vertical CIS Agilis reactors. Our triumph stems from advances in the initial design of the showerhead based on our previous Gen II CIS. When developing this particular reactor, which features a close injection showerhead (CIS), we focused on exploring a novel method for controlling the well-established hydride and alkyl delivery system. The immediate outcomes, soon discussed, showcase that this design provides precise control over thickness uniformity and surface roughness, as well as enhancing film growth rates and reducing the particle count on the wafer.



➤ The Agnitron Agilis 100 features a Gen III Close Space Injection Showerhead, aiding the growth of an AlN film.

The new showerhead can be applied across different Agilis reactors, for the growth of materials such as GaN, AlN and AlGaN alloys, as well as for oxide-based materials, like Ga_2O_3 and AlGaO alloys. This innovative showerhead offers tremendous versatility, demonstrated by its ability to be heated to temperatures exceeding 150 °C that allow for the pre-heating of ammonia. This attribute also facilitates the growth of films utilising low vapor pressure precursors. An illustrative case is the growth of ternary and quaternary nitrides, including



➤ Figure 1. Ga_2O_3 film growth in an Agilis 100 reactor with the cutting-edge CIS showerhead. The growth rate (a) and uniformity (b) dependencies on chamber pressure for TEGa and TMGa. Growth rate and uniformity versus TMGa molar flow rate (c) for layers grown at substrate temperatures of 800 °C and 900 °C and constant growth pressure of 30 Torr, achieving around 20 μm/hr at 540 μmol/min with less than 1 percent, 1σ uniformity.

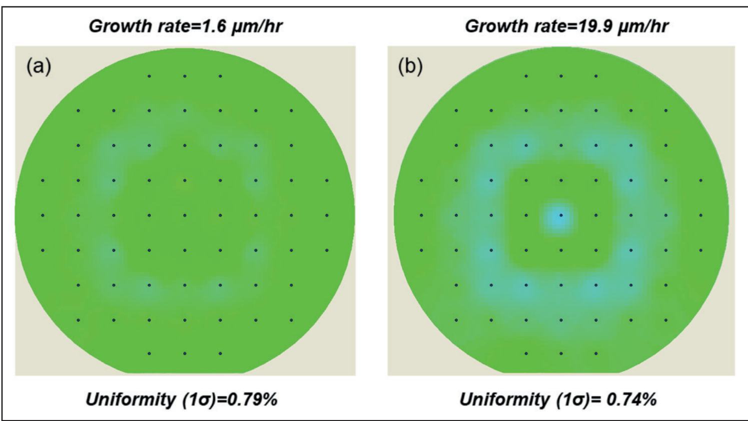


Figure 2. Ga_2O_3 two-dimensional thickness map on a 50 mm sapphire substrate using the CIS. Films grown at 1.6 μm/hr (a) and 20 μm/hr (b). Uniformity remains below 1 percent for both growth rates. A 2 mm edge exclusion has been applied during the thickness map.

ScAlN, and YAlN, which have garnered a lot of interest recently for expanding the application possibilities of AlN.

The Agnitron Agilis 100 MOCVD

One of our most prominent tools, the Agnitron's Agilis 100 MOCVD, is recognised for its compact footprint and outstanding adaptability, and is capable of the growth of an incredibly wide variety of materials. Designed for R&D with smaller substrates but capable of accommodating larger wafers up to 100 mm in diameter, this tool can be used to grow: Ga_2O_3, AlN, AlGaN, GaN, InGaN, III-V As/P alloys, MgZnO, ZnO, II-IV compounds; transition metal dichalcogenides, such as MoS_2, $MoSe_2$, WS_2, WSe_2; phosphorene, two-dimensional hexagonal BN, SiC, ScAlN, and YAlN.

Offering enhanced usability, our Agnitron Agilis 100 integrates optical reflectometry in the UV and blue with Imperium analytical control software to provide real-time measurements of growth rate and thickness. Additionally, the Agilis 100 offers UV light exposure during growth, a feature that ensures effective control of epitaxial film purity by reducing residual carbon incorporation and managing point defects. Moreover, our Agilis 100, along with all our MOCVD/CVD systems, facilitates seamless plug-and-play switching between sources and gas distribution (showerhead) configurations – this is realised within just a few hours of maintenance. Another notable feature of the Agilis 100 is the option to add precursor distribution nozzles. This enables process refinement and wafer carrier cleaning, enhancing the appeal of these tools across a diverse range of applications.

There are two interchangeable configurations associated with the Agilis 100: the remote injection showerhead (RIS), and the CIS. The primary distinction is the placement of the showerhead relative to the wafer carrier. This ensures adaptable film growth options for meeting various research and development requirements.

Our RIS Agilis 100 reactor, capable of temperatures of over 1600 °C, features a distinctive remote injection showerhead that incorporates an optimised hydride or oxygen injector and uniformly distributes around it metalorganic precursors, such as trimethylgallium and trimethylaluminium. Commonly used for Ga_2O_3 growth, this configuration encounters two primary challenges. Firstly, film growth is impeded, due to higher gas-phase reactions, resulting from the increased gap between the showerhead and the wafer carrier. Secondly, it is harder to realise uniform film thickness and doping, due to difficulties in maintaining flow laminarity across the wider showerhead-to-wafer carrier gap.

Despite these limitations, our RIS Agilis 100 MOCVD reactor offers exceptional thickness uniformity within a tight process window. This is accomplished by lowering the reactor pressure and introducing high total gas flows to suppress buoyancy, which threatens to lead to flow instabilities. However, while the RIS Agilis 100 enables uniformity below 2 percent across a 50 mm substrate, process efficiency falls, due to high gas and precursor

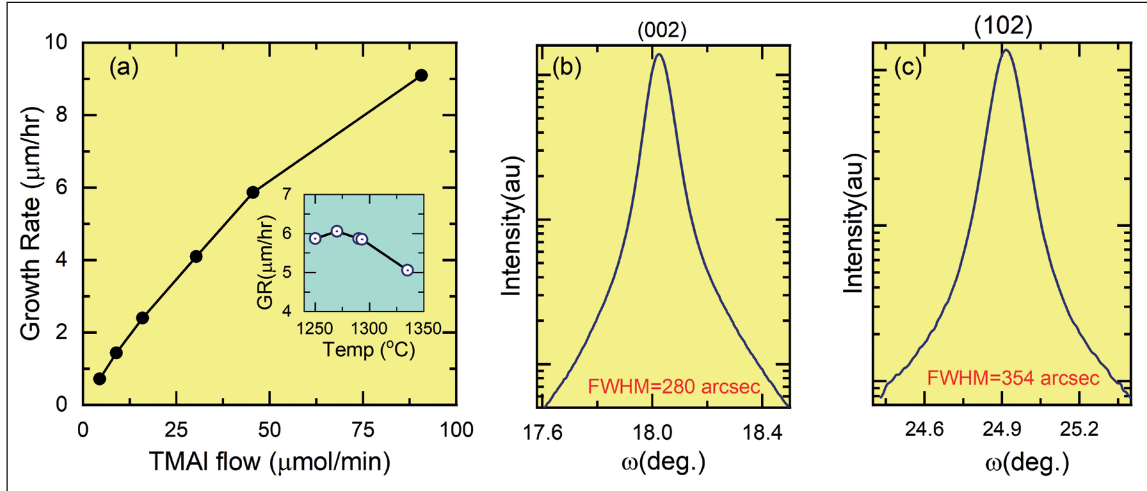


Figure 3. (a) Growth rate as a function of TMAl molar flow rate. The inset in (a) shows the growth rate as a function of substrate temperature. X-ray rocking curves, obtained with 2.4 μm-thick AlN, show values for the full-width at half maximum of 280 arcsecs (002) (b) and 354 arcsecs (102) (c).

consumption, coupled with the narrow process window.

As mentioned earlier, the challenges just discussed can be addressed by equipping the Agilis 100 with the new Gen III CIS showerhead. Note that this is available as an upgrade. We have conducted extensive testing of our Agnitron Agilis 100 reactor for Ga_2O_3 growth, with evaluation showcasing the enhanced performance that comes from introducing the new showerhead. This design overcomes the limitations associated with the RIS configuration.

Agnitron and Ga_2O_3

One of the primary applications for our new Gen III CIS showerhead is the growth of epitaxial layers of β-Ga_2O_3, a pivotal material for advancing power device technology. Positioned to shape the future of the power semiconductor market, Ga_2O_3 possesses fundamental properties that are conducive to the production of superior power devices while maintaining economic viability through the creation of high-quality melt-grown bulk substrates.

Over a decade of dedicated research in device and materials, Ga_2O_3 has demonstrated remarkable progress. Breakthroughs at the device level include a breakdown voltage now exceeding 8 kV and critical breakdown fields of more than 5 MV cm^{-1}, surpassing the theoretical limits of SiC and GaN. Such success has established β-Ga_2O_3 as the most promising candidate for next-generation solid-state power-switching applications.

A critical process in the production of any material is the growth of the epitaxial layers. With β-Ga_2O_3 films, epitaxy has been extensively explored with various methods. Of these growth technologies, MOCVD stands out for its ability to produce high-quality epitaxial films at a rapid growth rate, ensuring uniformity and controllable doping.

Our team at Agnitron Technology is leading many of the breakthroughs in Ga_2O_3 materials – they are spearheaded by the design and building of customised MOCVD reactors and processes for growing high-purity films of this oxide and its related alloys.

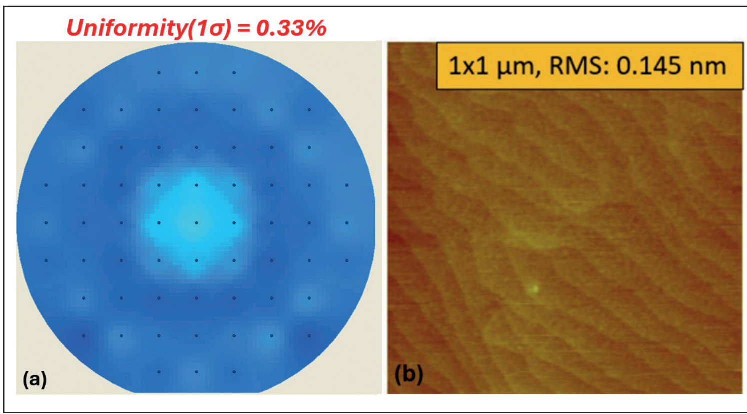
Our renowned Agnitron Agilis MOCVD reactors are widely adopted worldwide, utilised in prestigious institutions that include but are not limited to: the University of California, Santa Barbara (UCSB); Cornell University; US Naval Research Laboratory (NRL); the Ohio State University; Arizona State University; the University of Wisconsin; and Bristol University, UK. Our reactors are being used by research teams at these institutions, with these epitaxial tools behind the growth of high-purity Ga_2O_3 films, including those with impressive electron mobilities of nearly 200 cm^2 V^{-1} s^{-1} at room temperature and over 23,000 cm^2 V^{-1} s^{-1} at low temperatures. Noteworthy results, underpinned by growth using our Agnitron reactors, have featured in previous issues of CS Magazine – see issues 2 and 7 of 2022, and issue 3 and 6 of 2023.

> The results just presented highlight the Agnitron Gen III CIS's remarkable ability to surpass the thickness, doping, and composition uniformity requirements that are essential in production MOCVD, all while maintaining a high growth rate. As well as demonstrating state-of-the-art devices, this new capability offers a cost-effective solution for researchers using MOCVD to make radical breakthroughs in power electronics.

The availability of native Ga_2O_3 substrates, reaching sizes of up to 100 mm in diameter, presents a significant opportunity for commercialising β-Ga_2O_3-based power devices. However, as is often the case with epitaxy, the primary challenge lies in attaining precise thickness and doping uniformity, along with a consistently smooth surface, all while maintaining an industrially feasible growth rate. Our ground breaking Agnitron Gen III CIS showerhead tackles this challenge, offering a solution to elevate film quality. This advance is a critical step towards enhancing film manufacturability, and ultimately positioning β-Ga_2O_3-based power devices for market success.

Gen III CIS: Growing Ga_2O_3

We incorporated the Gen III CIS showerhead into our Agnitron Agilis 100 reactor for the growth of Ga_2O_3. The results accentuate the showerhead's effectiveness in enhancing growth rates and producing exceptional thickness uniformity (see Figure 1 and 2). Using a substrate temperature of 800 °C, we studied the influence of chamber pressure on the growth rate of films produced



➤ Figure 4. (a) Thickness map for a 0.73 μm-thick AlN film and (b) an atomic force microscopy image of a 2 μm-thick AlN layer on a sapphire substrate. Notably, these films showcase exceptional smoothness, with a uniformity of less than 0.33 percent.

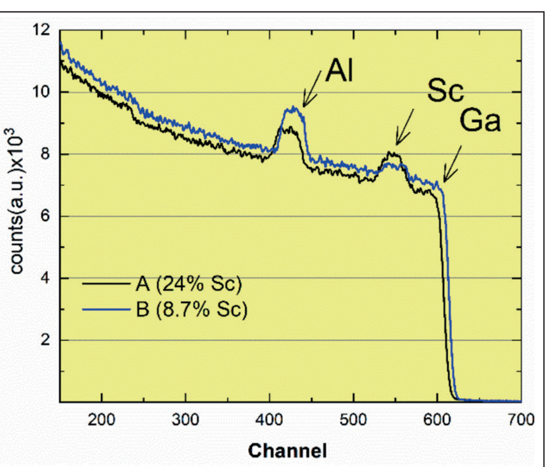


Figure 5. Rutherford backscattering spectroscopy of ScAlN alloys grown on GaN-on-sapphire templates using Agnitron's Agilis 100. The blue trace shows around 9 percent scandium, while the black trace shows 24 percent.

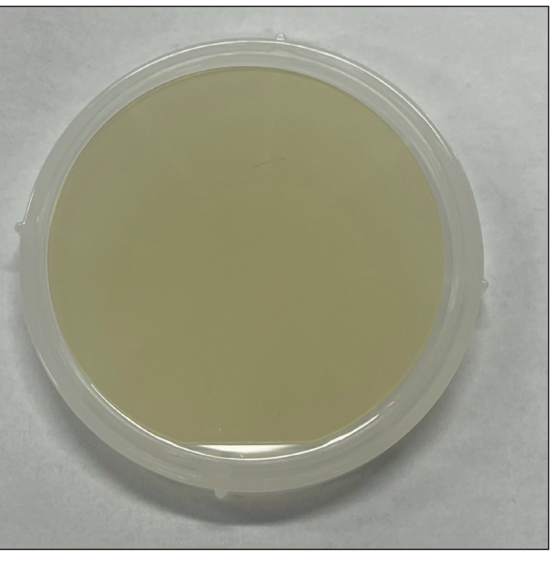


Figure 6. A 0.15 µm-thick film of ScAlN grown on GaN-on-sapphire.

using two different gallium-based precursors: trimethylgallium (TMGa) and triethylgallium (TEGa). When investigating the influence of chamber pressure, we adopted consistent molar flow rates of 46 µmol min^{-1} for TEGa and 25 µmol min^{-1} for TMGa.

At elevated growth pressures, the growth rate falls for both TEGa and TMGa, due to unintended gas-phase reactions. These reactions deplete the precursor before it reaches the substrate, thereby reducing the necessary substrate surface reactions for film growth.

Despite TEGa having a higher molar flow rate, it is the films grown with TMGa that have a higher growth rate, highlighting the efficiency of the TMGa source. The accelerated growth kinetics of TMGa compared with TEGa stem from a pyrolysis process that involves two steps, rather than three. This enables TMGa to react more rapidly with oxidising gases and have a higher growth rate.

Compared with TEGa, the influence of growth pressure on films grown with TMGa is less pronounced, indicating reduced impact of gas-phase reactions for films grown with this precursor. The uniformity of films grown with TMGa is notably superior, consistently measuring below 1 percent, while for TEGa it is below 2.5 percent.

"Unique features like wafer temperatures above 1400 degress C and chamber pressure lower than 50 torr offered by Agilis 100 can help explore optimised process conditions for ultrawide bandgap semiconductors, difficult to achieve with other commercially available reactors." Shubhra S. Pasayat, Assistant Professor, Department of Electrical and Computer Engineering, University of Wisconsin-Madison.

We have also studied the impact of flow rate on the Ga_2O_3 growth rate. For TMGa it's a linear relationship, with the growth rate reaching approximately 20 µm/hr for a TMGa flow of 540 µmol/min (see Figure 1 (c)).

To evaluate film uniformity under different growth rates with TMGa, we produced thickness maps for two films (see Figure 2). These maps highlight the new showerhead's capacity to produce films with less than 1 percent non-uniformity, irrespective of growth rate.

Another encouraging result is that using silane as a dopant, Ga_2O_3 films grown at 4.3 µm/hr with TMGa exhibit an electron mobility of 100 $cm^2 V^{-1} s^{-1}$ and a free carrier concentration of 4.6 x 10^{17} cm^{-3}. This set of results confirms the new showerhead's ability to produce high-quality Ga_2O_3 films.

Gen III CIS: Growing AlN

The significance of AlN cannot be overstated. Blessed with remarkable properties, it is a superb candidate for next-generation high-power electronic and optoelectronic devices. Boasting a substantial bandgap of 6.1 eV, Schottky barriers exceeding 2 eV, an excellent thermal conductivity of more than 150 W $m^{-1} K^{-1}$, and critical breakdown fields surpassing 15 MV/cm, AlN holds promise across various applications. To harness its full potential, high-temperature growth by MOCVD is employed, with temperatures exceeding 1300 °C to ensure a low defect density in the epilayers. Ideal for this task is the Agnitron Gen III CIS. Offering exceptional thermal control capabilities, it stands out by easily withstanding temperatures of over 1350 °C, and operating in close proximity to the susceptor, thanks to its new highly efficient thermal management.

Utilising our innovative CIS showerhead, we've conducted extensive tests, growing AlN on 50 mm

c-plane sapphire substrates. Our results underscore our showerhead's versatility, allowing for adjustable aluminium molar flow rates and, consequently, demonstrating impressive film growth rates, ranging from 0.7 μm/hr to around 9 μm/hr (see Figure 3(a)).

We have explored the growth rate's dependence on substrate temperature, finding a less pronounced effect. However, as substrate temperature increases, the gradual decline in growth rate is evident, a parameter we plan to investigate in more detail. Notably, our Agnitron Gen III CIS allows fine tuning of the distance between the showerhead and the wafer – it can be below 10 mm, and more than 35 mm. This tremendous versatility facilitates diverse precursor allocations and growth scenarios, enhancing the showerhead's adaptability to varied experimental conditions.

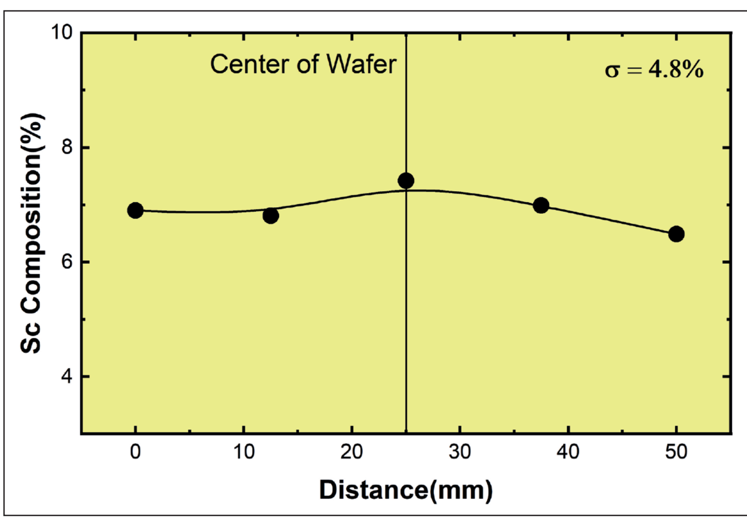


Figure 7. Composition of a ScAlN film measured by Rutherford backscattering spectroscopy across the diameter of a 50 mm wafer. The average composition and coefficient of variation are 7 percent and 4.8 percent, respectively.

Using our novel CIS showerhead reactor, we have grown a 2.4 μm-thick AlN layer on sapphire substrates at a growth rate of around 1.0 μm/hr. X-ray diffraction indicates excellent crystal quality, with values for the full-width at half maximum of the diffraction peak of around 280 arcsecs and 350 arcsecs in the (002) and (102) directions, respectively (see Figure 3(b) and 3(c)). Note that these results are obtained without optimisation of the process conditions. These AlN thin films have a remarkable thickness uniformity and minimal surface roughness, with a uniformity of less than 0.5 percent for a AlN film that's around 0.7 μm thick, grown at about 0.7 μm/hr (see Figure 4(a)). Outstanding smoothness is evidenced by a root-mean-square roughness of just 0.145 nm for a AlN-on-sapphire film that's 2 μm-thick, and grown at 1.3 μm/hr (see Figure 4(b)). These findings underscore the efficacy of our new showerhead in producing high-quality AlN films at a high growth rate that exhibit impressive uniformity and surface characteristics.

Why ScAlN?

High-performance microwave transistors and amplifiers are vital for wireless communication, with GaN-based HEMTs playing a key role. AlGaN serves as a common barrier material, forming a two-dimensional electron gas at the AlGaN/GaN interface. However, the critical thickness of AlN/GaN is insufficient for forming a Schottky gate contact, resulting in devices with high leakage. Emerging as a promising barrier layer is the alloy scandium aluminium nitride (ScAlN). Due to its high polarisation coefficients, its shows superiority over standard AlGaN barriers.

MOCVD is a promising growth technology for the growth of ScAlN on an industrial scale, as there is the potential to produce high-quality, uniform films on large wafers. However, to date, only the group at Fraunhofer IAF, in Freiburg, Germany, has demonstrated the growth of ScAlN by MOCVD. To address this shortcoming and help unleash the substantial market potential for the ScAlN material system, we have been developing a commercial-scale MOCVD process for ScAlN/GaN HEMTs.

Holding back the growth of ScAlN with existing commercial MOCVD reactors is the lack of scandium-based metal-organic precursors with a sufficiently high vapour pressure. The vapour pressure of these particular precursors is very low, and the introduction of a sufficient flux into the reactor chamber requires heating the sources to a relatively high temperature. That's far from trivial, as it demands that all the gas delivery components – including the mass flow controllers, pressure controllers and valves – sustain an even higher temperature to prevent precursor condensation in the delivery network. This necessitates the use of specialised components and assemblies that are capable of withstanding these far high temperatures. Current commercial MOCVD reactors are not designed to deliver such low-vapour-pressure precursors, as they are commonly built to handle the traditional metal organics, which have sufficiently high vapour pressure, even at room temperature.

We have addressed the challenge of gas delivery of scandium-based sources by developing and implementing a specialised high-temperature gas delivery system. We heat the source to 150 °C, and maintain the gas delivery network near 200 °C. By integrating this system with our Agnitron Agilis 100 reactor, we have developed the growth processes for producing high-quality ScAlN thin films on wafers up to 50 mm in diameter using commercially available scandium sources. Our ScAlN alloys have scandium compositions that can exceed 40 percent, despite an unoptimised process.

To evaluate the absorption band edge shift and the crystal quality of our ScAlN films, we have turned to optical transmission and X-ray diffraction. These techniques consistently demonstrate the successful incorporation of scandium into the AlN lattice while preserving the wurtzite structure. We meticulously control scandium integration by adjusting the source temperature, reactor pressure, substrate

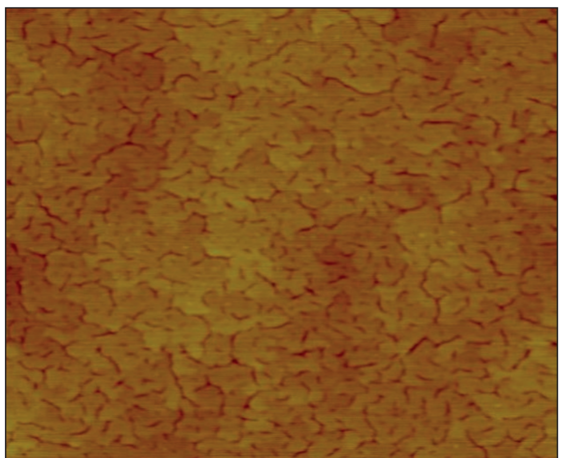


Figure 8. A 2 μm by 2 μm scan of a ScAlN/GaN HEMT structure grown on SiC. The root-mean-square (RMS) roughness is 0.20 nm.

temperature and ammonia flow rate. For accurate determination of the scandium composition in our ScAlN thin films, we utilise both energy-dispersive X-ray spectroscopy and Rutherford backscattering spectroscopy. The results from both techniques are in good agreement (see Figure 5 for Rutherford backscattering spectroscopy results, highlighting peaks for scandium, aluminium and gallium in four films).

Introducing our Gen III showerhead for ScAlN growth delivers a remarkable performance. Consistently, it is capable of producing highly uniform ScAlN films with a thickness uniformity of less than 1 percent. We investigated the scandium compositional uniformity of these films with Rutherford backscattering spectroscopy (see Figure 6). The measurements reveal a uniform scandium content across the entire wafer: the average scandium composition is 7 percent, and the variation is 4.8 percent of the mean value (see Figure 7). These preliminary results show a promising compositional uniformity, and we expect further improvement following the manipulation of showerhead temperature and process flowrates. The root-mean-square (RMS)surface roughness of a ScAlN/AlN/GaN HEMT structure, grown on SiC substrate, is just 0.2 nm (see Figure 8). In the non optimized ScAlN/GaN HEMT structure sheet carrier concentration was measured 1.9 x 10^{13} cm^{-2} and electron mobility about 900 cm^2 V^{-1} s^{-1}.

Success with ScAlN opens the door to the growth of a number of technologically significant nitride materials that have to be grown with low-vapour pressure precursors. They include transition metal nitrides, such as NbN and YAlN.

The results just presented highlight our Agnitron Gen III CIS's remarkable ability to surpass the thickness, doping, and composition uniformity requirements that are essential in production MOCVD, all while maintaining a high growth rate. As well as demonstrating state-of-the-art devices, this new capability offers a cost-effective solution for researchers using MOCVD to make radical breakthroughs in power electronics.

Innovation pedigree

Standing at the forefront of semiconductor innovation, our team at Agnitron Technology is revolutionising the growth of wide and ultra-wide bandgap materials with our ever-advancing portfolio of cutting-edge MOCVD tools. Our focus on overcoming longstanding challenges in showerhead design has spurred the introduction of the Gen III CIS showerhead, showcased in the Agilis 100 reactor. The results obtained with this tool are transformative, enabling us to demonstrate enhanced growth rates, improvements to thickness and alloy composition uniformity, and a film quality exceeding production MOCVD standards. Success on all these fronts comes while maintaining a high growth rate. As well as delivering exceptional performance, the Agnitron Agilis 100 MOCVD system stands out from the crowd for its adaptability and seamless configuration changes. This tremendous versatility enables a spectrum of epitaxial growths, allowing users to explore any imagined possibilities.

As we continue to push the boundaries of materials growth, our tools and growth technologies are paving the way for advancements in power electronics, while solidifying our position as a leader in the semiconductor research equipment manufacturing industry. Our belief is that by focusing on such innovation, we will bolster the future viability of our customers to bring their products to market faster, more reliably, with higher quality and thus make a more meaningful contribution to society at large.

Agnitron would like to acknowledge Greg Haugstad of the University of Minnesota Characterization Facility (UMN CharFac) for conducting RBS measurements and Prof. Chirag Gupta of the University of Wisconsin Madison for XRD measurements.

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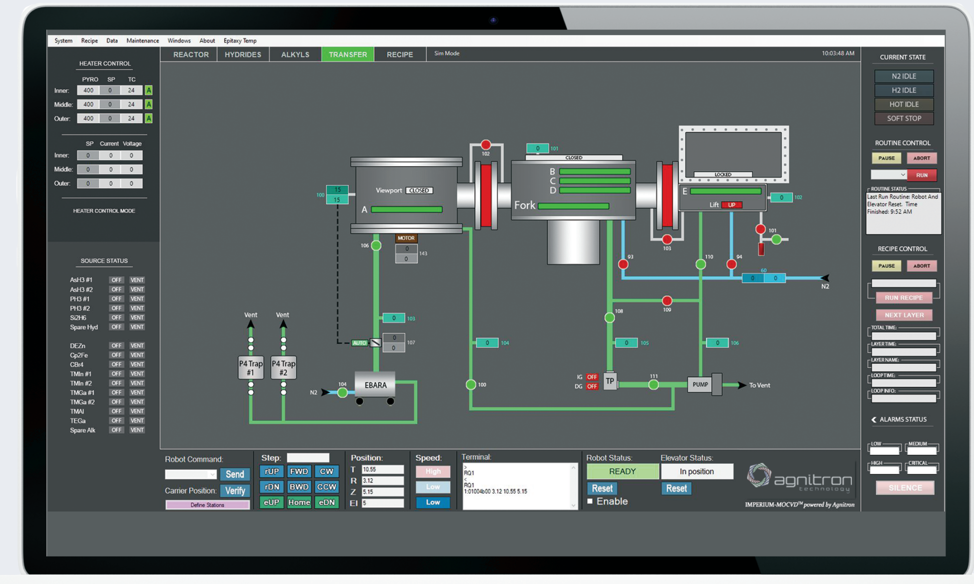

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Pushing the power envelope

Novel designs enrich the performance of power devices employing a range of semiconducting materials

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

LONG GONE are the days when the likes of GaN and SiC were just promising materials. Now they are fulfilling their potential, evidenced by their significant commercial success. Sales of SiC MOSFETs are soaring, thanks to their widespread deployment in electric vehicles, and GaN is now established as the material for making fast chargers for portable devices.

But the revolution in power electronics is by no means over. For operation at a few kilovolts of more, the leading devices are still the silicon IGBT and thyristor. However, looking to replace them are a number of novel alternatives – they may also have a role to play at lower voltages – that are based on compound semiconductor materials.

Several strong examples of these devices featured at the latest IEEE International Electron Devices Meeting (IEDM), held in San Francisco, California, from 9-13 December. Many advances were discussed at that meeting, including: the first demonstration of a trench-shaped 6.5 kV SiC IGBT; GaN HEMTs capable of blocking that voltage while delivering an ultralow dynamic on-resistance; the first vertical superjunction device made from Ga_2O_3, offering a breakdown voltage of 2 kV; and AlN-based vertical *p-n* diodes with dopant-free distributed-polarisation doping that feature a critical electric field almost twice that of reported values for SiC and GaN.

Trench-shaped SiC IGBTs

Efforts at the national level to trim carbon footprints need to include the introduction of smart grids and high-voltage direct-current transmission systems. For both these innovations, the building blocks include

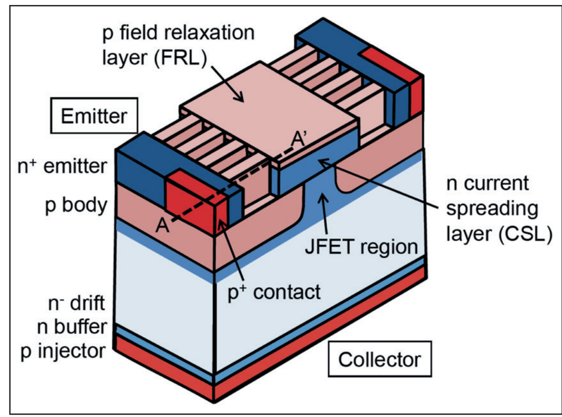
static synchronous compensators and solid-state transformers, components that are formed from power devices capable of blocking high voltages and delivering high currents.

Devices made from SiC are promising candidates for serving in these compensators and transformers. As well as ensuring a high performance at the device level, the capability of SiC to operate at high frequencies opens the door to trimming the size and increasing the efficiency of the compensators and transformers. However, if 6.5 kV SiC MOSFETs are deployed, the on-resistance is a concern, particular at elevated temperatures – at 175 °C, it's 104 mΩ cm^2.

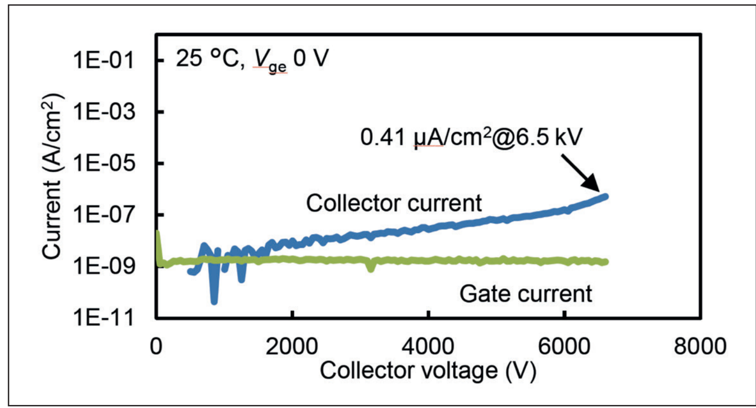
Due to this limitation, a number of research groups have already developed SiC IGBTs. They include those capable of blocking 15 kV by utilising a thick drift layer, and variants pioneered by Hitachi that feature a thinner drift layer to trim switching loss. In 2016 researchers from Hitachi unveiled a 6.5 kV SiC IGBT with a low switching loss that employed an extremely thin drift layer, and at the latest IEDM this team introduced a descendent with a trench-etched double-diffused MOS structure (see Figure 1), designed to address low electron injection from the emitter, due to poor channel mobility.

Describing this device in his IEDM presentation, Naoki Watanabe emphasised a weakness in more conventional SiC trench-gate structures: "At the trench bottom, high electric fields occur in the gate oxide in the off state, due to the high critical electric field of silicon carbide, which is close to the gate oxide. Therefore, electric field relaxation is necessary to realise trench-gate silicon carbide IGBTs."

Addressing this issue is the team's novel form of SiC IGBT, which features a trench-etched double-diffused MOS structure. It is claimed that one of the merits of this design, which utilises a V-shaped structure, is an increased channel density, realised by shrinking the trench pitch. Another strength is that during operation in the off-state, the electric field in the gate oxide is greatly decreased, by burying the trenches in the *p*-body.



➤ Figure 1. The *n*-channel SiC IGBT with a trench-etched double-diffused MOS structure.



➤ Figure 2. A blocking voltage of more than 6.5 kV is realised with the SiC IGBT with a trench-etched double-diffused MOS structure.

To evaluate the capability of the trench-etched double-diffused MOS structure, Watanabe and co-workers produced a test structure of that form, before comparing its electrical characteristics to that of a planar variant. Plotting the gate voltage as a function of drain current revealed a doubling of the current with the trench-etched double-diffused MOS structure, attributed to the fin shape. "Therefore, the electron injection from the emitter can be enhanced by the trench-etched double-diffused MOS structure," argued Watanabe.

Simulations by the team offered an insight into the electric fields within the device in the off-state, thought to peak at 2 MV cm^{-1}. "This is low enough to ensure a high reliability," claimed Watanabe, who added that the trench-etched double-diffused MOS structure suppresses the electric field in the gate oxide.

Fabrication of the team's novel IGBTs began by taking an *n*+ substrate and depositing an epistructure that included a 70 μm-thick drift layer. By using backside grinding as the last process, IGBTs were produced with a thin drift layer.

Measurements of electrical characteristics revealed that the on-voltage, defined as the voltage for a collector current of 200 A cm^{-2}, is 4.8 V for the IGBT with the trench-etched double-diffused MOS structure, compared with 6.7 V for the planar control. At turn-on, the novel IGBT had a differential on-resistance of 6.6 mΩ cm^2, roughly a third of that of the planar device. The blocking capability of the IGBT with the trench-etched double-diffused MOS structure is demonstrated by the collector leakage current of 0.41 mA cm^{-2} at 6.5 kV (see Figure 2).

The switching characteristics of the IGBT with the trench-etched double-diffused MOS structure are also superior to the planar control. Losses for turn-off and turn-on are around 19 percent and 6 percent lower, thanks to a small feedback capacitance and a large electron injection from the emitter.

Active passivation GaN HEMTs

Another device showcased at IEDM that's capable of delivering a 6.5 kV blocking voltages and is targeting tomorrow's electrical grid infrastructure is the E-mode active-passivation *p*-GaN gate HEMT.

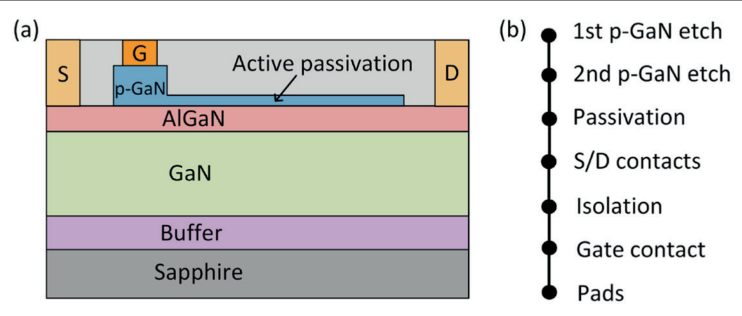


Figure 3. The architecture of the active-passivation HEMT (a) and an outline of its fabrication process (b).

Developed by a partnership between researchers at Peking University, Tsinghua University and Nagoya University, this form of lateral GaN HEMT, which is grown on a sapphire substrate, has merits that include avoiding the need for a thick epitaxial structure and the opportunity to use the same epiwafer for low-voltage and high-voltage devices.

Speaking on behalf of the team, Jiawei Cui from Peking University remarked that two of the challenges faced when developing kilovolt-level GaN power switches are ensuring enhancement-mode operation – that is, the devices are normally off – and the stability of the dynamic on-resistance.

"The *p*-GaN gate HEMT is a mainstream technology for E-mode GaN power transistors," said Cui. "To make full use of the experiences accumulated in the past years, we think it's a good choice to use the *p*-GaN gate structure for high-voltage transistors as well."

To suppress dynamic on-resistance, Cui and co-workers have moved away from the traditional methodology of adding multiple field plates, an approach described as impractical for devices operating at several kilovolts of more.

"As an alternative, we propose the active-passivation *p*-GaN gate HEMT," remarked Cui, who explained that a thinned *p*-GaN layer provides passivation in this transistor (see Figure 3). Additional features of this form of HEMT are the screening of surface trapping by mobile holes, and the use of just a single additional step to provide active passivation.

Fabrication of the team's devices began by taking a conventional epiwafer featuring a high-resistivity buffer layer, a 200 nm-thick undoped GaN channel, a 15 nm-thick $Al_{0.2}Ga_{0.8}N$ barrier and a 20 nm-thick *p*-GaN cap, and selectively etching into this layer with a two-step process. SiO_2 deposition to passivate the device followed, prior to the addition of ohmic contacts, an isolation step, and the formation of a gate contact and probe pad.

Electrical measurements revealed that the active-passivation HEMT has a superior off-state blocking capability than the conventional HEMT, which acts as a control. For both devices, increases in gate length led to a higher blocking voltage, with the activate-passivation HEMT with a 77 μm-long gate capable of blocking 6.573 kV (see Figure 4). The team attributed the higher blocking voltage for the active-passivation HEMT to a shift in the location of the depletion region, so that it no longer sits partially below the gate.

According to measurements of transfer current-voltage characteristics, both forms of HEMT exhibit enhancement-mode operation, with a threshold voltage of 0.8 V.

Measurements of the output current-voltage characteristics revealed that the on-resistance for the HEMT with active passivation is lower that than for the control – the values were 38.2 mW mm and 43.6 mW mm, respectively.

To evaluate the dynamic on-resistance of their devices, Cui and co-workers compared dynamic and static values at a range of drain-source voltages. The ratio is low, with 1.02 reported for measurements at 4.5 kV on enhancement-mode *p*-GaN gate HEMTs with a 77 μm gate length.

The excellent on-resistance characteristics are claimed to result from the screening effect, due to the passivation layer. To validate this attribution, the team produced a pair of devices – with and without active passivation – that included a surface testing electrode.

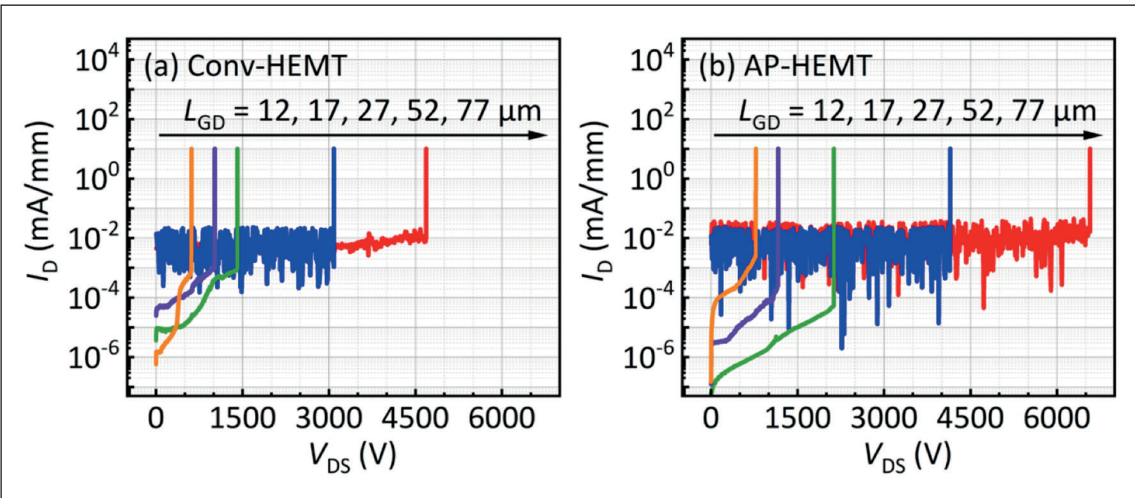


Figure 4. The off-state characteristics of the conventional GaN HEMT (a) are inferior to the variant with the active-passivation design (b).

Applying a negative voltage to this electrode mimicked the negative surface trapping effect. “It is found that the drain current in the conventional HEMT reduces, but the drain current in the active-passivation HEMT remains unchanged,” said Cui. “The result suggests that active passivation can screen the surface effect from influencing the 2DEG channel.”

The researchers also carried out a second test, applying a positive voltage to the electrode to trap electrons at the surface. When this voltage is removed, the drain current in the conventional HEMT reduced, and took a long time to recover. In comparison, the active-passivation HEMT did not produce a change in drain current, providing further evidence of surface screening.

Cui concluded his talk by benchmarking the active-passivation HEMT. He claimed that this device, delivering a performance close to the SiC limit, is the first enhancement-mode *p*-GaN gate HEMT with a blocking voltage of 6.5 kV or more.

Ga_2O_3 superjunction Schottky rectifiers

Another claim of breaking new ground came from a collaboration between researchers in the US and Japan: the first vertical superjunction device made from the ultra-wide bandgap material Ga_2O_3.

This partnership between researchers at Virginia Polytechnic Institute and State University, the University of Southern California, the US Naval Research Laboratory, Novel Crystal Technology, and Oak Ridge National Laboratory, produced a portfolio of devices featuring pillars 1-2 μm wide, wrapped in charge-balanced *p*-type NiO. These devices can block up to 2 kV.

Speaking on behalf of the partnership, Yuan Qin from Virginia Polytechnic Institute and State University, began his presentation by emphasising the strengths of Ga_2O_3. They include a high critical electric field – it is projected to be up to 8 MV cm^{-1} – a high temperature stability, and the possibility for epitaxial growth on large-diameter substrates. Unfortunately, this oxide has two major downsides: a lack of *p*-type doping and a low thermal conductivity.

Qin offered a brief overview of the evolution of all forms of semiconductor device, explaining that the switch from one-dimensional structures to multi-dimensional variants, such as those employing a superjunction, multiple channels and multiple gates, has enabled a higher power density and efficiency at the system level.

For superjunction devices, such as those made by Qin and co-workers, there is a linear increase in on-resistance with blocking voltage, while for one-dimensional variants, the on-resistance scales with the square of the blocking voltage.

“For the ultra-wide bandgap semiconductor gallium oxide there are still some challenges for fabricating superjunction devices,” remarked Qin, who explained that one of them is the development of a deep pillar etch process that produces a vertical sidewall and smooth surfaces.

> Of all the alternatives to silicon, AlN arguably has the greatest promise. Thanks to a bandgap of 6 eV, it has a much higher critical electric field than all its rivals, indicating the potential for an improved trade-off between the blocking voltage and the specific on-resistance.

Due to the lack of *p*-type Ga_2O_3, device development also requires the selection of an alternative *p*-type material that does not lead to excessive interface traps. NiO is an obvious candidate – it has previously been used for fabrication of vertical superjunctions in GaN and lateral superjunctions in Ga_2O_3.

Fabrication of the superjunction devices involved processing a 2-inch Ga_2O_3 epiwafer produced by NCT that has a 10 μm-thick layer of *n*-Ga_2O_3 with a doping level of 2 x 10^{17} cm^{-3}, and a 0.5 μm-thick layer of *n*-Ga_2O_3 with a doping level of 1 x 10^{16} cm^{-3}. Dry etching produced 6.5 μm-deep pillars, wrapped in NiO by conformal sputtering in an atmosphere of argon and oxygen. As the acceptor concentration in the NiO is much higher than the donor concentration in the Ga_2O_3 pillars, NiO with a thickness of 120 nm provides charge balancing with 1-2 μm-wide pillars. The team completed the fabrication of their devices by filling the trenches with a photoresist and adding

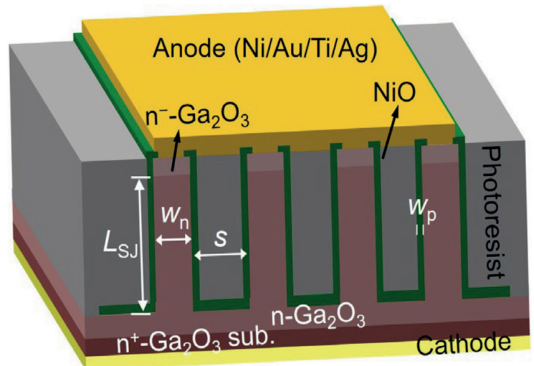


Figure 5. Characteristics of the vertical Ga_2O_3 superjunction Schottky barrier diode are determined by key dimensions, such as the trench depth (L_{SJ}), the trench depth (W_n), the separation distance between the trenches (S), and the thickness of the NiO (W_p).

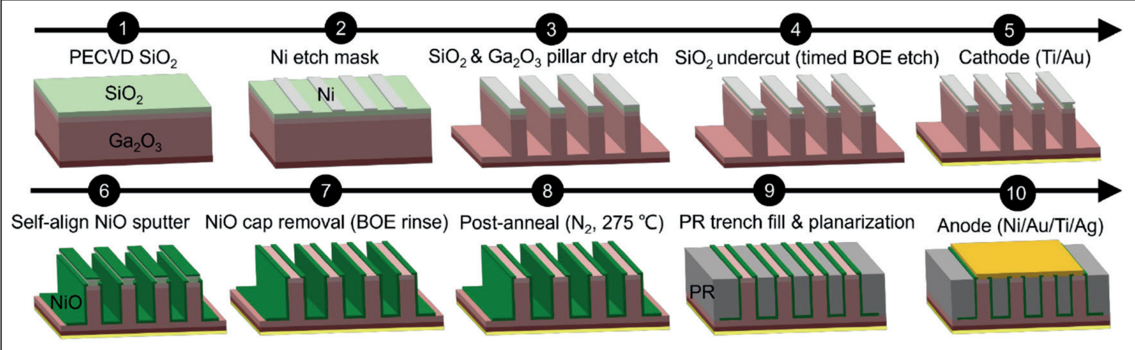


Figure 6. The ten-step process to produce Ga_2O_3 superjunction Schottky barrier diodes.

a Ni/Au/Ti/Ag Schottky contact (see Figure 5 for the device architecture, and Figure 6 for more details of the process flow).

With this design, the 0.5 μm-thick top n-Ga_2O_3 layer serves two purposes: it lowers the tunnelling leakage current of the Schottky contact; and it shifts the position of the peak electric field from the Schottky contact to the bulk superjunction.

Qin and co-workers evaluated the blocking capability of superjunction devices with a range of pillar widths. They found that the breakdown voltage initially increased with pillar width, reaching 2 kV at a width of 1.8 μm, before declining at wider widths. The peak blocking capability results from optimal charge balancing.

As the device temperature increased to 175 °C, the team observed a small reduction in blocking voltage to 1.8 kV. This suggests that the charge balance is preserved at high temperatures.

For the device with the best blocking voltage, at room-temperature turn-on occurred at 1 V, the on-off ratio was around 10^9, and the specific on-resistance just 0.7 mΩ cm^2. At 175 °C, the turn-on voltage fell to 0.8 V, the on-off ratio was around 10^8, and the specific on-resistance 1.3 mΩ cm^2.

Figure 7. Distributed polarisation doping is used to form the AlN-based diode.

Benchmarking this device, Qin remarked that it offers the best trade-off between the specific on-resistance and the breakdown voltage for all Schottky barrier diodes and junction barrier Schottky diodes from 600 V to 4 kV. The performance of the team's device, which offers fast switching, is close to the one-dimensional limit for GaN.

AlN vertical *p-n* diodes

Of all the alternatives to silicon, AlN arguably has the greatest promise. Thanks to a bandgap of 6 eV, it has a much higher critical electric field than all its rivals, indicating the potential for an improved trade-off between the blocking voltage and the specific on-resistance.

For many years, one of the drawbacks of AlN devices has been the lack of native substrates. However, much progress has been made in recent years, with reports from 2022 revealing that threading dislocation densities in this material can be below 10^4 cm^{-2}, and Asahi Kasei announcing 4-inch diameter substrates in 2023.

Another issue with AlN is the difficulty in realising conductive layers. Due to high ionisation energies for the common dopants – for the silicon donor it is 282 meV, and for the magnesium acceptor it is 630 meV – room temperature conductivity via conventional approaches is a challenge.

Offering a solution is distributed polarisation doping, and approach pioneered at the University of California, Santa Barbara, just over 20 years ago. Both *p*-type and *n*-type conductivity can be realised in nitride alloys by using positive or negative fixed space charges that depend on the graded direction.

Building on this approach, a team from Nagoya University and Asahi Kasei has used distributed polarisation doping to produce a *p*-type layer in AlN-based laser diodes. This approach to producing a *p*-type layer is said to increase the injection efficiency and trim series resistance, and ultimately enable the demonstration of a laser with continuous-wave emission in the UVC.

At IEDM that team announced further success with distributed polarisation doping, using this to produce both *p*-type and *n*-type layers in an AlN-based vertical *p-n* diode.

Speaking to the IEDM delegates, Takeru Kumabe from Nagoya University explained that until their team's recent success, AlGaN diodes with an aluminium composition exceeding 30 percent that exhibited ideal electrical characteristics had not been realised.

Kumabe and co-workers produced their devices by taking an AlN substrate and growing a 300 nm-thick $Al_{0.7}Ga_{0.3}N$ contact layer, followed by a 400 nm AlGaN *n*-type layer with distributed polarisation doping, a 120 nm-thick *p*-type layer with distributed polarisation doping, and finally a 20 nm-thick magnesium-doped GaN contact. In the layers with distributed polarisation doping, aluminium content in the AlGaN layers ranged from 70 percent to 95 percent.

Fabrication of the diodes began by activation of magnesium dopants in the capping layer. Etching defined the vertical mesa and plasma-enhanced CVD provided a protecting layer of SiO_2, prior to addition of the cathode, anode and contact pad, and a polyimide surface protection layer to prevent air discharge.

Secondary ion mass spectrometry (SIMS) determined average values for the negative and positive charge concentrations of 1.8×10^{18} cm^{-3} and 2.6×10^{17} cm^{-3}, respectively. "In both distributed polarisation-doped layers, charge concentration was constant along the depth direction, thanks to the linear compositional grading," explained Kumabe, who added that the results from SIMS and X-ray reciprocal spacing mapping indicate that the structure fulfils its intended design.

Electrical measurements at room-temperature on the diodes revealed a turn-on voltage of 6.5 V and a specific on-resistance of 3 mΩ cm^2. According to Kumabe, this is the smallest value for specific on-resistance ever reported for AlN-based *p-n* diodes.

The team have also used electroluminescence (EL) to scrutinise the behaviour of their devices. "The EL emission increased with increasing current, suggesting that both electrons and holes contributed to the conduction of typical *p-n* diodes," remarked Kumabe.

To verify that their device is a true *p-n* diode, Kumabe and co-workers measured the current density as a function of forward bias at temperatures from 323K to 573K, finding that threshold voltage decreased with increasing temperature. Using the recombination current model to describe the electrical behaviour provided further evidence that the team's device behaves as a *p-n* diode, rather than one with a metal-insulator-semiconductor structure (see Figure 8).

Reverse-bias measurements revealed a destructive device breakdown at -283 V, indicating avalanche breakdown did not occur. This led Kumabe and co-workers to calculate an electric field at breakdown of 7.3 MV cm^{-1}.

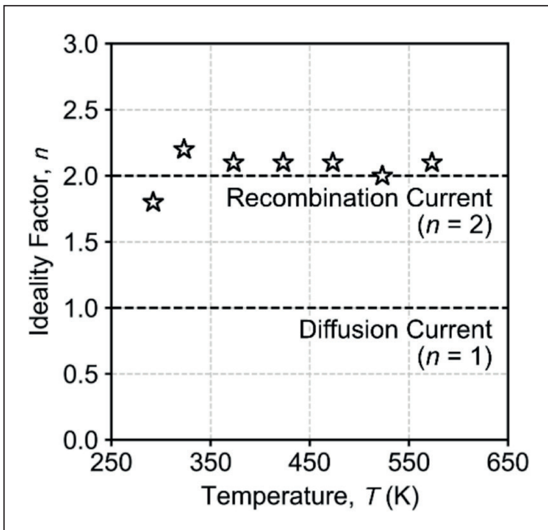


Figure 8. The temperature-dependent ideality factor of the AlN diode is close to 2, indicating that electrons and holes both play a role in device operation.

"The extracted electric field was compared with silicon carbide and gallium nitride electric field limits, as well as previously reported distributed-polarisation-doped GaN *p-n* diodes," said Kumabe. "The value of 7.3 MV cm^{-1} was almost twice as high as the gallium nitride and silicon carbide limit with the same doping concentrations."

Kumabe also noted that their device broke the limit of what could be realised by distributed-polarisation-doped GaN diodes on GaN substrates.

"This result demonstrates the high potential of aluminium nitride and high-aluminium content aluminium gallium nitride in power device applications," concluded Kumabe.

Such work shows that great progress is being made with AlN devices. Alongside advances in SiC, GaN and Ga_2O_3 devices, reported at IEDM and elsewhere, there's no doubt that the revolution in power electronics is well underway – but more is still to come.

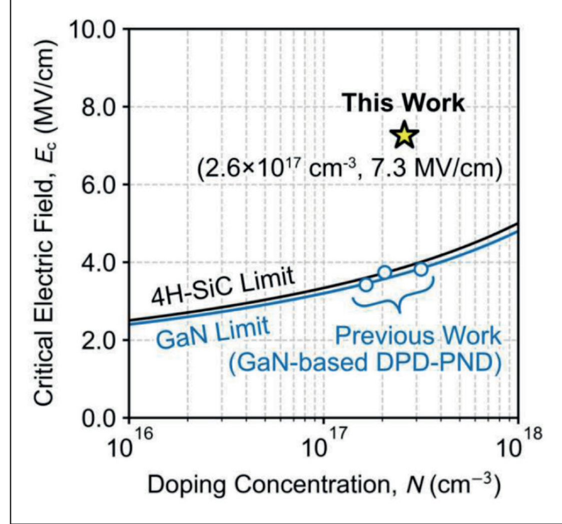


Figure 9. The performance of the AlN-based diode with distributed polarisation doping is well beyond the SiC and GaN limit.

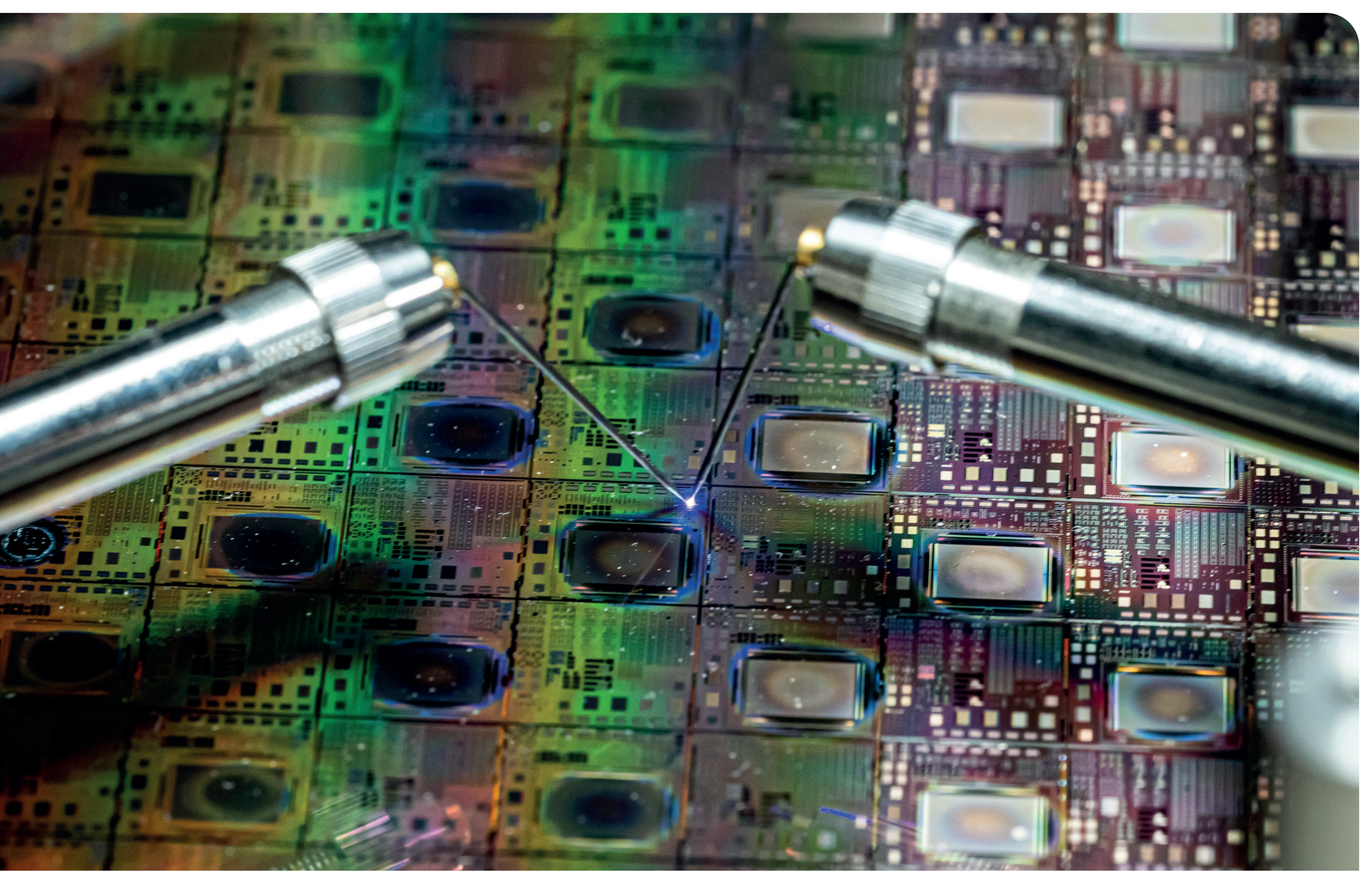
How to integrate silicon and III-Vs

To draw on all the traditional benefits that come from scaling, silicon and the III-Vs must be united via epitaxy and processing in silicon foundries

BY EUGENE FITZGERALD, FAYYAZ SINGAPOREWALA, DANIEL LEPKOWSKI AND JOHANNE CHU FROM NEW SILICON CORPORATION

THE MAINSTREAM semiconductor industry is continuing to head in the same direction. The focus, as always, is the miniaturisation of the silicon transistor. Success on this front today allows more of them to be packed on an IC, making this chip more powerful. It's an approach that enhances the capability of memory and computation but is expected to lead to commoditisation as this industry continues to mature.

In addition to scaling, the silicon industry is exploring other directions. That includes the integration of silicon with compound semiconductors, a marriage that has much promise as it offers the opportunity to draw on the best of both worlds. There is the tantalising prospect of combining the low cost, impressive toolsets and high volumes of the silicon industry with the prowess of the compounds, which include powerful light emission, high blocking



voltages, and efficiency and power in the RF domain.

It is crucial that when the compounds are united with silicon, the strengths associated with the latter technology are retained. Occupying the top spots of this valued list are the need for high-density devices, enhanced performance from scaling, and cost reduction.

Historically, increases in device density have been a major driver behind improvements to microprocessors, multicore processors and silicon memory. In the future, high transistor and LED densities will be needed in augmented-reality displays accommodating millions of pixels, as well as pixelated light sources and highly efficient single-chip phased arrays.

In general, scaling has excelled in increasing the 'bang' while lowering the 'buck'. Miniaturisation can be credited for higher circuit frequencies, lower power consumption, lower parasitics, reduced noise and superior heat removal. It's forecast that these performance enhancement benefits from miniaturisation will continue, with possible new dimensions for the digital control of arrays of high-density devices, such as LEDs and HEMTs.

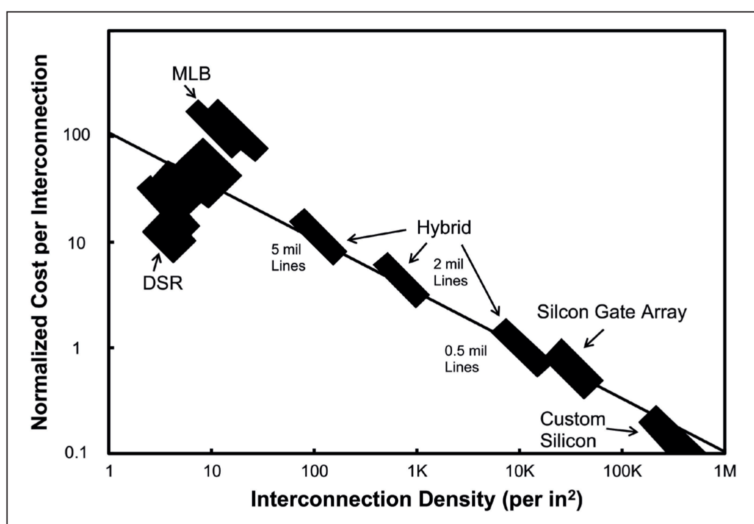


Figure 1. Cost per interconnection versus interconnection density. Custom silicon and silicon gate array are monolithic silicon chips (BEOL of CMOS is interconnecting high-density transistors). When interconnect (and therefore device) density at the chip level decreased to approximately 10,000 per square inch in 1984, costs favoured the fabrication of longer interconnects at the board/package level. [Adapted from W.H. Knausenberger and L.W. Schaper, "Interconnection Costs of Various Substrates- The Myth of Cheap Wire", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. CHMT-7, pp. 261-263, September 1984.]

The trimming of costs that come from scaling are not just due to an increase in the number of circuits per area, ensuring a reduction in the cost to produce each circuit. There is also the average cost for the interconnects between devices to consider – this depends on the interconnect length, with shorter interconnects more cost-effective.

Since the 1980s, the economics of monolithic integration at the chip level have been understood (see Figure 1, which demonstrates the relationship between interconnect density, cost per interconnection, and device density). We have come a long way since 1984, when interconnect density was below 10,000 per square inch and it made economic sense to have interconnects at the board/package level, rather than at the chip level. Over the intervening years, there has been the introduction of more and more wiring levels in chips, and interconnects have migrated from the board or package level to the chip level.

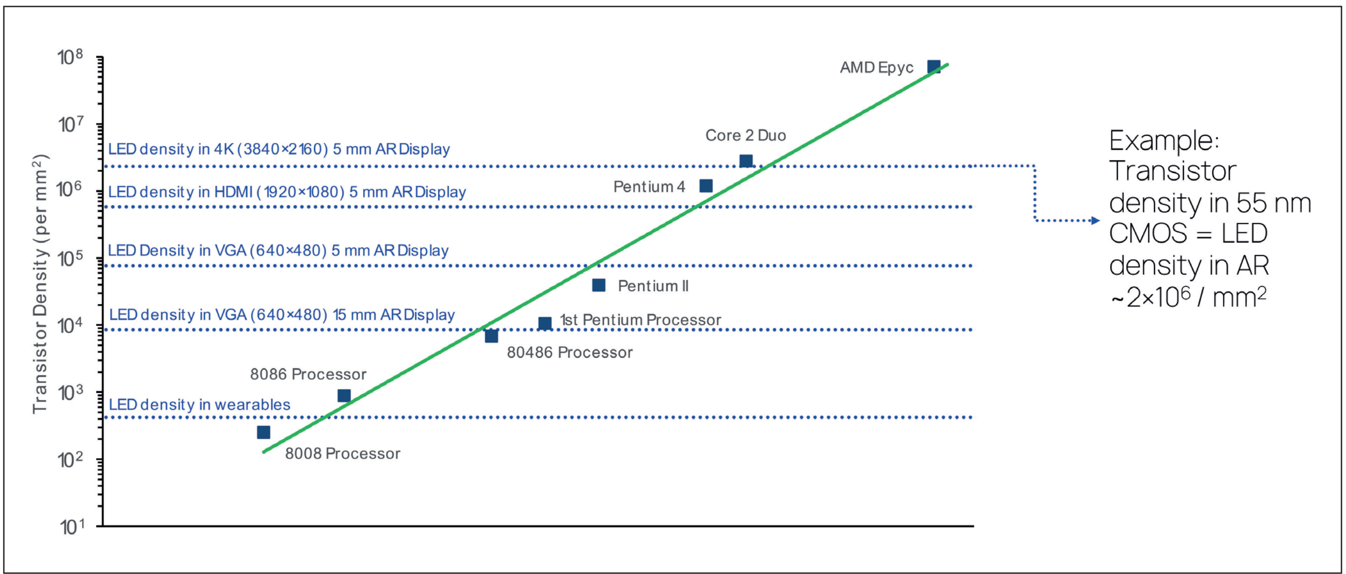
As well as the three strengths just outlined – the new chip possibilities, enhanced performance and cost reduction – there are others associated with silicon manufacturing that should be retained when compound semiconductors are brought onboard. These merits include a high yield, a high level of reliability, and speedy product design cycles. Yield and reliability have undergone steady improvement, due to the use of the same fabrication process for multiple products. A high yield is also aided by low-cost self-diagnostic capabilities for in-line and post-processing measurements – these are features that are facilitated by the integrated design process.

Another asset is the use of a common silicon wafer manufacturing process, which increases the volume of products passing through the process, and drives improvements to yield, reliability, and cost-effectiveness. Crucially, despite the common approach, each customer retains their own design intellectual property.

Integration with LEDs

One attractive opportunity for integration involves the creation of a single-chip LED display, formed by using millions of transistors to drive and address millions of LED pixels. In this case, the LED density in these displays is comparable to the density of transistors in early microprocessors. Due to this, as was the case with those microprocessors, it makes little sense to package all these components together, because it is not feasible to achieve such density, the cost is too high, and such an approach would negate the advantages, in terms of yield and reliability, that come from monolithic integration.

It is possible to compare the density of LEDs in a range of products, including wearables, virtual reality and augmented reality, with historic transistor densities (see Figure 2). This plot shows that the manufacturing of LED displays can be disrupted when LEDs become part of silicon manufacturing and are interconnected with CMOS using the CMOS back-end-of-line (BEOL) approach. Note that arguing against such a trend is as nonsensical as suggesting

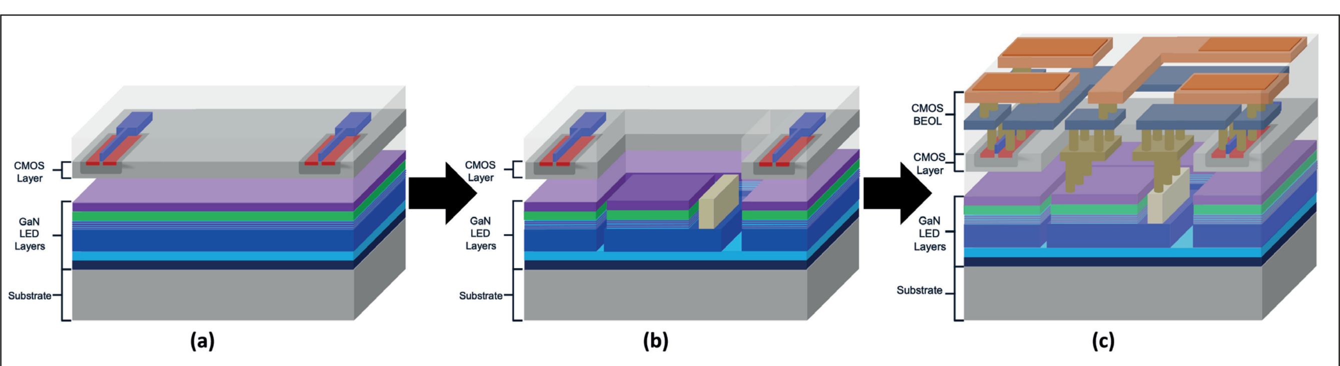


➤ Figure 2. The line across the graph represents the historic increase in the density of transistors over time. Superimposed are LED densities in current and future LED display products. With monolithic silicon integrated circuit manufacturing of CMOS + GaN LEDs, microdisplays will be single-chip and manufactured in silicon fabs.

that the Pentium processor should have been constructed by packaging individual transistors together, such as through mass-transfer or pick-and-place techniques.

To support the advance of single-chip displays, our team at New Silicon Corporation, Singapore, has developed the necessary materials, processes, structures, devices, and software design modules to create integrated circuits using silicon integrated circuit manufacturing that can unite CMOS devices and GaN-based LEDs. Our first set of products will be white or monochrome LEDs, the latter available in red, green and blue. For red and green variants, emission will result from blue light that pumps quantum dots. Further ahead, we plan to produce integrated full-colour displays, with quantum dots present on the red and green pixels.

Our CMOS + III-V process consists of three stages (see Figure 3): CMOS front-end of line (FEOL), new III-V FEOL, and CMOS BEOL. The first and last stages are taken directly from standard silicon CMOS manufacturing, which produces complete circuits by connecting transistors with a FEOL process on silicon wafers using a multi-level metal interconnection network formed in the BEOL. For our CMOS + GaN LED process, we sandwich a GaN FEOL between the CMOS FEOL and BEOL. After GaN LEDs are fabricated, the BEOL's interconnection network connects CMOS transistors and LEDs to create a monolithic integrated circuit. The silicon CMOS BEOL serves as the interconnection network for both silicon and III-V devices. It's an approach that enables an integrated design environment using standard integrated circuit design software.



➤ Figure 3. The monolithic process for creating CMOS + III-V circuits begins by processing III-V devices on the same wafer as the silicon transistors, after the silicon transistors have been processed. With the silicon process strategy of sequential masks, each aligned to the one before it, is critical for a processing platform to gain the benefits of integration and miniaturisation across many product segments. (a) A standard silicon FEOL is fabricated, according to the design, in a foundry and transferred onto a III-V-on-silicon epitaxial wafer. (b) III-V device FEOL is done, automatically aligned to silicon FEOL via sequential masks. (c) Sequential masks form the silicon BEOL, which interconnects the silicon transistors and III-V devices according to circuit design. Diagrams are not to scale or proper aspect ratio.

A tremendous benefit of adopting the silicon front-end and back-end processes for III-V devices is that each mask is aligned to the former one, guaranteeing yield and reliability across the wafer. In addition, this approach eradicates problems that arise when fabricating silicon transistors and III-V devices separately, and then trying to use wafer-scale metallic bonding and alignment to interconnect the devices. When III-V devices are on a separate wafer, realising high-density alignment across the two types of wafers with different materials stacks and thermal expansion coefficients is problematic and low yielding, especially at 200 mm or larger wafer sizes.

Another challenge when uniting III-Vs and silicon is optimising the usable wafer area across both device layers. When wafer bonding is employed to combine silicon die and III-V die, the area occupied by III-V devices is not the same as that occupied by the silicon circuits. Consequently, the unused area on a wafer – often the III-V wafer – is required to spread out circuit components for alignment to the other die on the wafer. This is far from optimal, as it decreases the effective chips per area and increases cost. Unfortunately, this fundamental cost and design constraint is often overlooked, and the limited use cases and higher costs that follow are a headwind to potential wafer sales volumes, further increasing the cost-per-wafer for wafer-bonding approaches.

A far better approach is true monolithic integration. Using sequential masks, as is the case in silicon integrated circuit design and manufacturing, we use integrated circuit designs that intermix silicon and III-V devices. This approach enables the most compact area and the most efficient design, both for circuits and for chips. As all designs employ the same process, wafer volume is maximised, helping to ensure the lowest cost per wafer.

One crucial step in our monolithic process is the transferring of the CMOS FEOL onto a GaN-on-silicon epiwafer. After the transfer, the CMOS FEOL remains on the wafer's surface, resembling a regular CMOS wafer. The GaN LED epitaxy beneath the CMOS FEOL surface is hidden, but the processing of GaN LEDs in specific areas is still possible, by etching through the top thin surface of silicon that hosts the CMOS FEOL.

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With our approach, the areas reserved for LED fabrication must be kept separate from CMOS components. This is accomplished by incorporating III-V device models into the standard CMOS design kit that's provided by the foundries that provide the FEOL and BEOL services. The development of a process design kit (PDK) is crucial for bridging the gap between integrated circuit design and semiconductor foundries for chip fabrication.

We have developed an integrated CMOS + GaN PDK that provides comprehensive solutions for large-scale circuit simulation, design, and layout verification. This PDK allows for circuit design and fabrication on our proprietary integrated CMOS + GaN wafer technology. Our PDK libraries are specifically tailored to our CMOS + GaN offerings, and they cater for unique applications that are outside the scope of the portfolio of conventional CMOS or GaN foundries. Thanks to close collaboration between the process development and IC design teams, we have carefully fine-tuned every aspect, thereby ensuring a robust, reliable bridge between integrated circuit design and fabrication. Our efforts will provide the catalyst to a new era of chip-based solutions for displays, lighting, and wireless systems, overcoming the challenges of III-V-on-silicon integrated circuit design and fabrication (see Figure 4 for an example of a processed 200 mm CMOS + GaN LED circuit).

So far, we have focused on rolling out our initial platform, the CMOS + GaN LED platform. However, our monolithic integrated circuit process can be applied to any CMOS + X platform, where X could be a III-V, or another semiconductor material or device. For integration, it is essential that: there is the capability to produce epitaxial device layers on silicon wafers with an appropriate diameter for silicon line manufacturing; and the defect density in these epitaxial device layers is low enough to ensure and maintain a satisfactory performance in the final integrated devices in the circuit throughout the product lifetime.

As we ramp production of digitally controlled power amplifiers, we are preparing for the introduction of our next product: single-chip phased arrays for 5G/6G. Faster data rates have led to increases in wireless communication frequencies, which has had the downside of higher degrees of absorption in the atmosphere. Due to this, there's a need to focus the transmission of high-frequency wireless signals on the cell recipient station. In the infrastructure of yesteryear, this would have been accomplished with movable dish antennas. However, that's not feasible

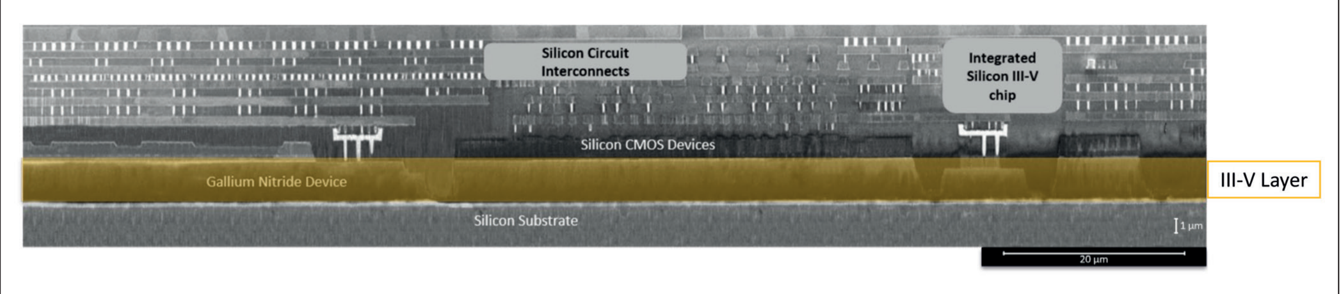

Figure 4: A transmission electron microscopy cross-section of a finished 200 mm wafer processed using silicon foundry manufacturing. The tungsten plug process used for the BEOL is used to also connect to the III-V FEOL.

in consumer devices. In the likes of the smartphone, one way to electronically steer the wireless beam towards the receiver is to use a chip populated with multiple GaN HEMTs, precisely arranged at specific distances from each other on a plane. We view these single-chip phased arrays, manufactured at lower costs in silicon fabs, as crucial for expanding the deployment of high-bandwidth consumer wireless systems.

There is no doubt that the integration of III-V materials and devices into silicon integrated circuits is opening up entirely new market segments for the silicon industry. For that industry, the monolithic integration of new devices into silicon systems will define the next stage of growth, driven by miniaturisation, integration, and scaling of integrated circuits. This will create new high-growth markets, targeted by high-performance systems produced at very competitive costs.

Our immediate focus is the microLED illumination and display market. According to analysis by Spherical Insights and Straits Research, this market had a value of $650 million in 2022, and is forecast to climb at a compound annual growth rate of more than 80 percent through to 2030, when it will be worth $36.5 billion. Demand is driven by the desire for brighter, more powerful display panels for consumer electronic devices, including high-end smartphones and wearable displays, such as head-mounted devices.

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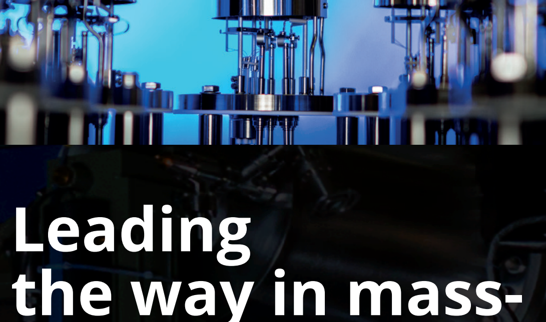

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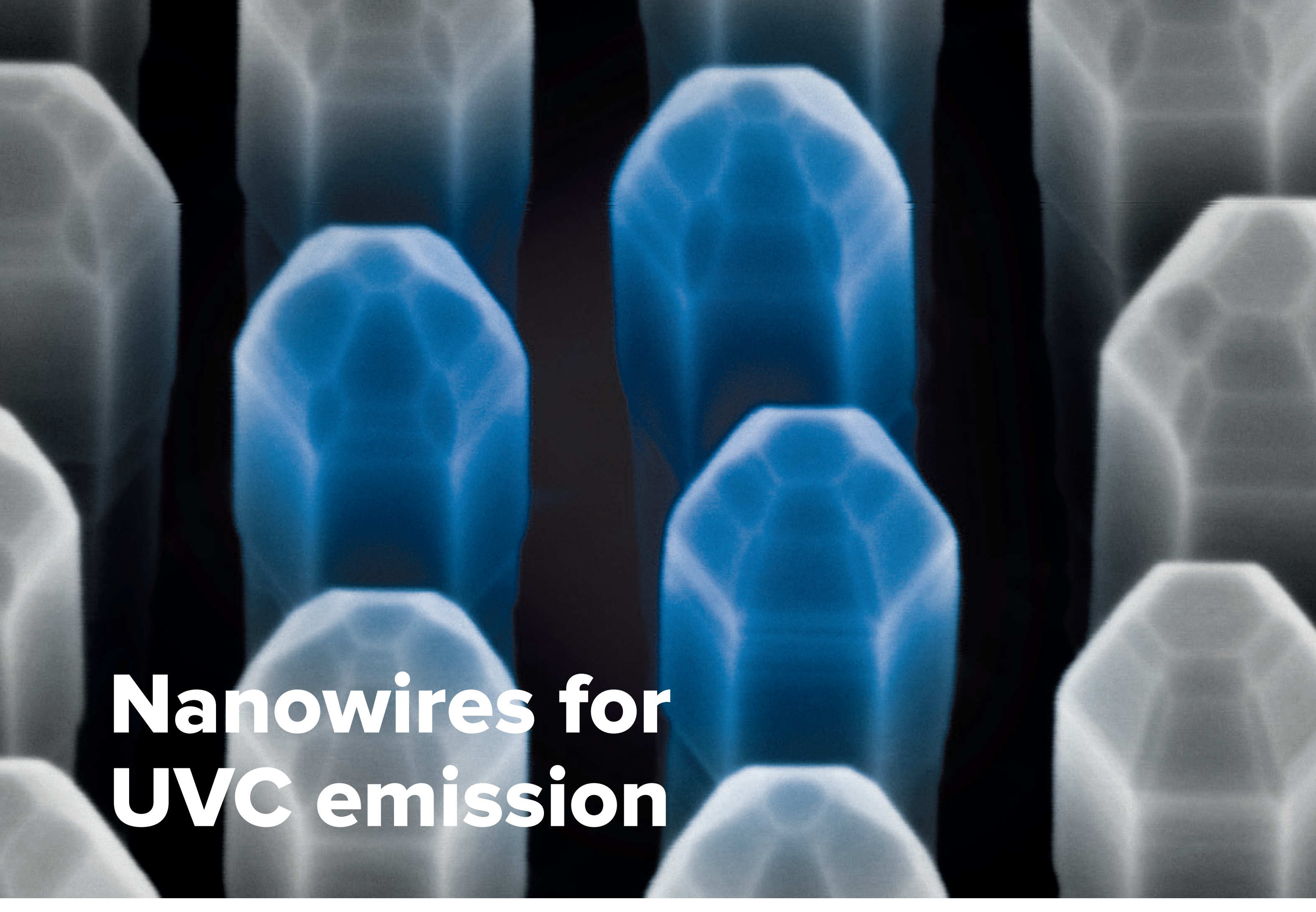


Nanowires for UVC emission

AlN nanowires with short-period superlattices based on AlN and GaN are trailblazing a path to a new class of UVC-emitting devices

BY RÉMY VERMEERSCH AND CORENTIN GUÉRIN, BOTH AFFILATED TO CNRS-GRENOBLE AND CEA-GRENOBLE; GWÉNOLÉ JACOPIN AND JULIEN PERNOT FROM CNRS-GRENOBLE; AND BRUNO DAUDIN FROM CEA-GRENOBLE

IT IS WELL KNOWN that exposure to mercury is not good for our health. It can cause a number of symptoms, including tremors, insomnia, memory loss, neuromuscular effects, headaches and cognitive and motor dysfunction. Due to this, the current implementation of the Minamata convention, signed in 2017 under the auspices of the United Nations, is progressively banning the use of mercury-containing devices for environmental and sanitary reasons.

The phasing out of mercury has major implications for UV lighting. For emission in this spectral range, mercury lamps are the incumbent source, widely used for disinfection. As they will have to be replaced in the short term, the research and development of new UV-emitting devices is on the rise. Hopefully this will address the increasing need for versatile, efficient sources in the UVC range that spans 200 nm to 280 nm.

Optical sources that emit in this spectral domain can serve a variety of applications. That includes disinfection, as UVC light damages DNA (or RNA) chains, thereby preventing the reproduction of viruses and bacteria. However, while highly beneficial for disinfection, the sensitivity of DNA to

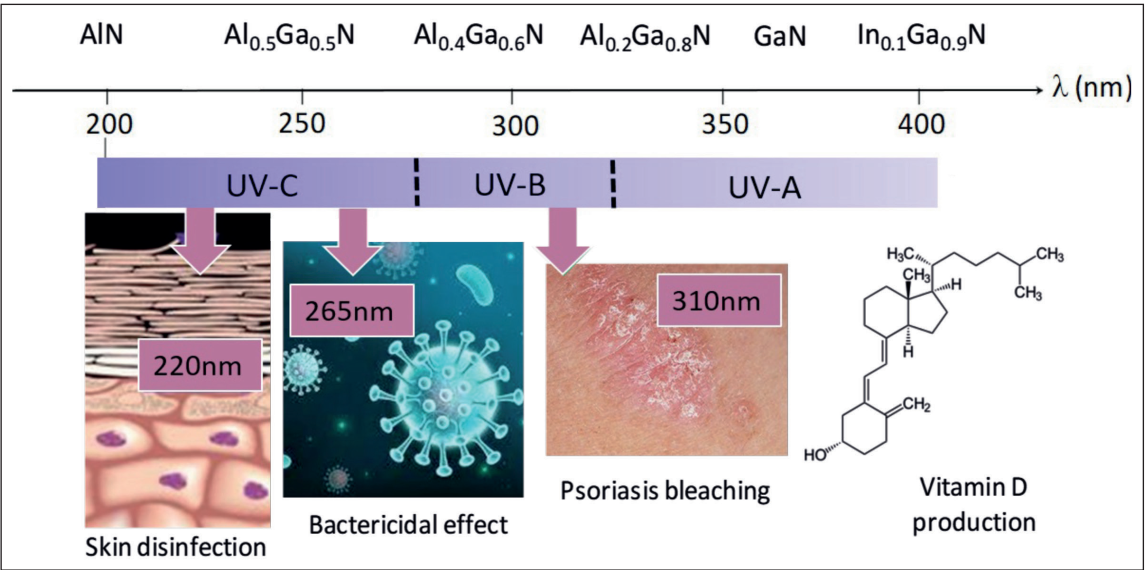


Figure 1. Emission in the UVC (200-280nm) exhibits bactericidal properties, with maximum DNA damage observed at 265 nm. At 220 nm, the reduced depth penetration of UV light prevents damage to eye cornea and skin, opening the path to surface sterilisation of objects. Other medical applications, such as psoriasis treatment, are documented around 312 nm. The stimulated production of vitamin D by exposure to UVA is recognised to have beneficial effects to cure a variety of diseases, including rickets and mood troubles.

UVC sources within this wavelength range is also problematic – it may severely hurt human skin, have long-term effects and cause melanoma. These downsides complicate the practical use of 265 nm UVC sources for the growing market of domestic disinfection applications, such as putting LEDs in a refrigerator, using them for tap water sanitisation and providing air purification.

Fortunately, humanity can enjoy the benefits of UVC sources while avoiding their pitfalls. What's needed is to decrease the wavelength within the UVC to the 220-230 nm range. At such short wavelengths the penetration range in skin is limited to stratum corneum, preventing DNA damage to retina as well as deeper epidermis and dermis layers.

Despite the detrimental effect of UV light with wavelengths above 230 nm to the integrity of dermis, most current research is directed at developing sources emitting in the 260-280 nm range to target disinfection applications.

Incidentally, sources emitting at longer wavelengths than this also have health benefits. Controlled exposure to emission in the UVA (315-400 nm) and UVB (280-315 nm) has been shown to cure various diseases, including psoriasis, lupus vulgaris and rickets, and may even have mood-enhancing effects through stimulated vitamin D production.

Nitrides: Pros and cons

Depicted in Figure 1, III-nitride semiconductors – namely AlN, GaN, InN and their alloys – are well-suited to the realisation of heterostructures spanning the entire UV range. In particular, the bandgaps of AlGaN ternary alloys are capable of fully covering the UVC and UVB bands. This capability has ultimately stimulated wide interest in the scientific community.

Unfortunately, the practical realisation of UV LEDs is far from trivial: III-nitride semiconductors suffer from a significant lattice mismatch with the most common substrates used to grow them, namely sapphire, silicon and SiC. Due to this mismatch, strain accumulation increases with layer thickness until relaxation occurs, which tends to result in the formation of a high density of misfit dislocations. The presence of these dislocations within the epilayers and also of growth-related threading dislocations impairs efficient radiative recombination.

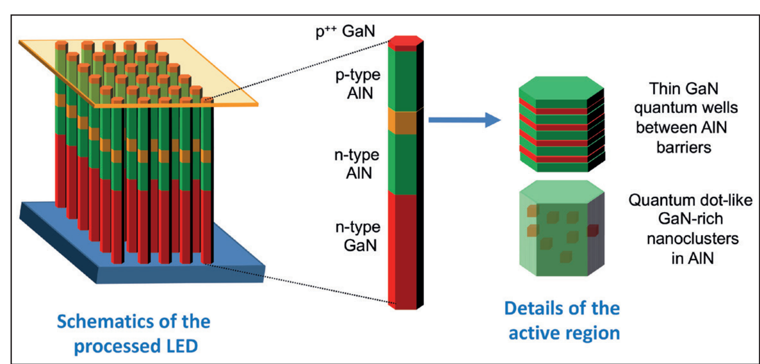
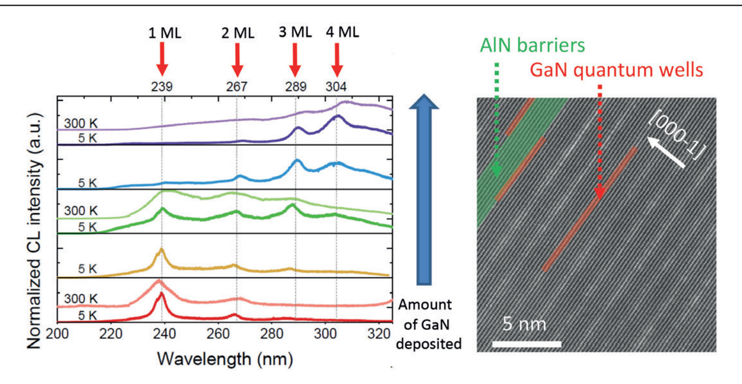


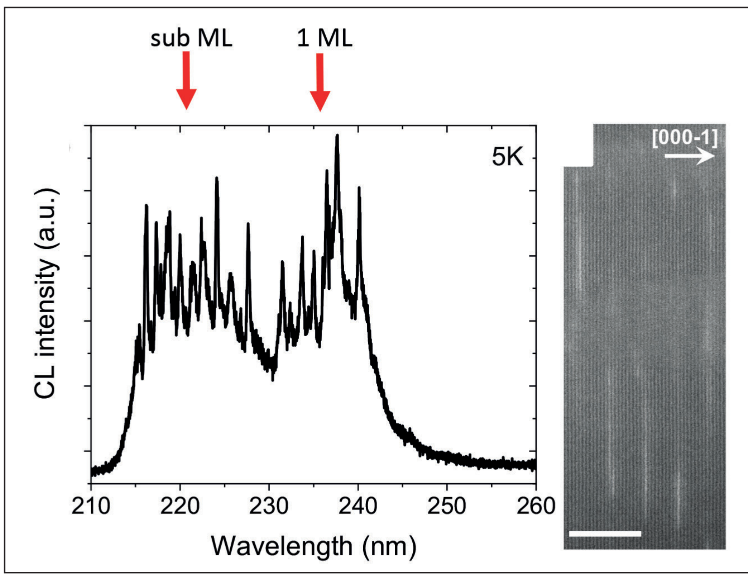
Figure 2. Following the growth of *n*-doped GaN nanowires (NWs) spontaneously nucleated on silicon (111), an *n*-doped AlN NW section is deposited, followed by the growth of an active region consisting of either thin GaN quantum wells separated by AlN barriers or gallium-rich nanoclusters in an undoped AlN section. The top part consists of a *p*-doped AlN NW section covered by a 10 nm thick p^{++} GaN section. This structure is processed using standard lithography techniques and a semi-transparent electrically conducting layer is deposited on top.



➤ Figure 3. Deposition of monolayer (ML)-thick GaN quantum wells (QWs) is easily controlled in MBE. For increasing deposition of GaN, a series of peaks corresponding to QW thickness of one to four MLs is observed at wavelength emission values of 239 nm, 267 nm, 289 nm and 304 nm, respectively. The reduced cathodoluminescence (CL) intensity quenching between 5K and 300K suggests a reduced influence of thermally activated non-radiative defects. The high-resolution, transmission electron microscopy image of one-ML-thick GaN QWs illustrates the interface abruptness and the absence of interdiffusion.

Another challenge with light emitters based on III-nitrides is the realisation of sufficient doping. Electrical doping of a deep-UV LED is not easy, as for *n*-type and *p*-type doping, using silicon and magnesium, respectively, dopant ionisation energy increases with the AlN molar fraction in AlGaN. That means that doping is increasingly challenging at shorter wavelengths. Due to this, current injection is a key issue for UV devices.

As well as issues related to strain and carrier creation and transport, light extraction is far harder in UV devices than their visible cousins. Current-injection layers absorb UV light, and there is a large optical index for these nitrides with respect to air. Due to this, specific packaging strategies are required to prevent light from being trapped within the chip.



➤ Figure 4. The optical signature of monolayer-thick incomplete GaN quantum wells with a limited lateral extension in a single nanowire (NW) consists of a set of sharp lines at wavelengths shorter than 239 nm, corresponding to carrier localisation at the scale of small, flat GaN islands in AlN shown in the high-resolution, transmission electron microscopy image. The scale bar in the inset is 200 nm.

One consequence of all these difficulties is that the external quantum efficiency of today's UV LEDs – that is, the ratio of extracted UV photons to injected electron pairs – is very low. This efficiency is just a few percent at 265 nm, and even lower at 230 nm.

The nanowire revolution

A promising pathway to addressing all performance limitations is the nanowire, a monocrystalline semiconductor structure with at least one nanometric dimension. Nanowires are typically one or more microns in length, and 50 nm to 200 nm in the lateral dimensions. Often exhibiting facets corresponding to low-energy crystallographic planes, these miniature marvels can be grown by various techniques, either using or not using a metallic catalyst (for the former, metal droplets seeded on the substrate act as nanowire nucleation centres).

For catalyst-free formation, specific to III-nitride materials, nanowires may be grown by MBE on virtually any kind of substrate – that includes sapphire, graphene, oxides and metals. Unlike the classical vapour-liquid-solid growth mode, which is a thermodynamic process that is triggered by the precipitation of atomic constituents at the interface between a substrate and a gold catalyst droplet featuring dissolved elementary species, catalyst-free growth of nanowires is governed by kinetics. What this means is that growth is influenced by diffusion of adsorbed atomic species (adatoms) on both the substrate and the nanowire surface.

With catalyst-free growth by MBE, following the spontaneous nucleation process, elongation proceeds through upward diffusion of metallic species, which impinge on the side walls until they reach the top surface. However, depending on the detailed growth parameters and their influence on metal adatom diffusion, it is possible that the nucleation probability on the side walls is not strictly zero. Thanks to a ratio for the longitudinal growth rate to the lateral one of typically 30 for GaN, independent, long and non-coalesced nanowires are formed.

The remarkable properties of these nanowires make them promising candidates to overcome the difficulties that plague the efficiency of conventional UV LEDs, which are based on layer heterostructures.

First, with nanowire heterostructures, the large free surface is very favourable to elastic strain relaxation, which can proceed without producing dislocations detrimental to radiative recombination efficiency.

The second major merit of these miniature structures comes from the higher limit for solubility of electrical dopants in nanowires than layers. With LEDs with a conventional, planar architecture, introducing more foreign atomic species increases the stress in the heterostructure until it reaches a maximum amount, corresponding to the limit of solubility. Beyond this, additional dopants lead to precipitation of this species, as well as mechanical damage, such as crack formation. It's a markedly different state of affairs for nanowires. Thanks to easy elastic relaxation associated with a large surface-to-volume ratio, it is possible to incorporate more electrical doping species –and this favours current injection.

Last but by no means least is the third key advantage of the nanowires – due to their discrete nature, an ensemble of separated nanowires behaves as a medium with an optical index that is intermediate between the index value of bulk III-nitride material and air. Due to this, nanowires offer enhanced light extraction over their planar cousins.

Why use MBE?

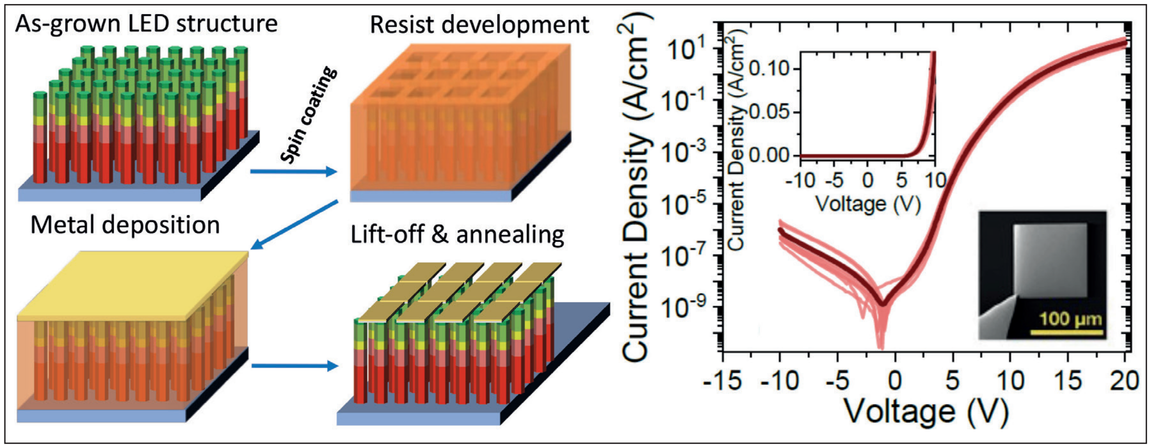
Some question the use of MBE for device production, due to its relatively low growth rate compared with MOCVD. Nevertheless, in our case this apparent drawback turns out to be a decisive advantage, as MBE enables atomic scale control when depositing thin layers. Thanks to this, it is possible to produce the highly confining heterostructures that are needed to make devices emitting at very-short wavelengths.

Our team from Grenoble, France, has used MBE to produce nanowires with GaN quantum wells that have thicknesses of one to four monolayers. Cathodoluminescence measured on these structures features four emission peaks, corresponding to the coexistence of quantum wells with differing numbers of discrete monolayers within a collection of nanowires grown using different experimental conditions (see Figure 3). High-resolution transmission electron microscopy of one sample containing a stacking of the thinnest quantum wells reveals a one-monolayer-thick GaN quantum well in a single nanowire, illustrating the abruptness of the interface between GaN and AlN. There is a fall in cathodoluminescence intensity, a quenching effect, between 5K and 300K. However, the relatively moderate value of this quenching suggests a reduced influence of thermally activated non-radiative defects.

Interestingly, it is also possible to form GaN quantum wells with a sub-monolayer thickness (see Figure 4). In that case, the reduced lateral extension of the monolayer-thick wells results in additional carrier confinement, and leads to the appearance of cathodoluminescence lines at wavelengths shorter than the one corresponding to infinite, one-monolayer-thick quantum wells. The wavelengths provided by the sub-monolayer thickness wells are particularly attractive for surface and skin disinfection, as they are short enough to avoid harmful side effects. Potential applications include replacing hand-sanitising gel in hospitals and other industrial and domestic environments.

Shadow effects

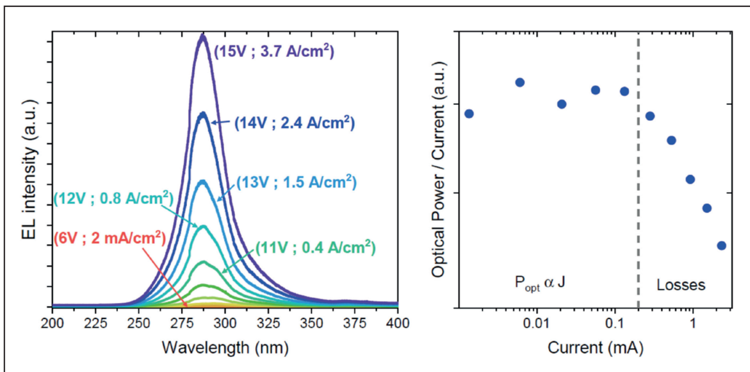
AS MBE is a ballistic process, the aluminium and gallium fluxes produced by the effusion cells will freely travel in straight lines from the cell to the substrate without experiencing collisions. As the directions of these fluxes are never normal to the sample surface, due to geometrical constraints intrinsic to an MBE growth chamber, the metal atoms reach nanowire sidewalls and contribute to growth by diffusing towards the nanowire top surface. The size and spacing of the nanowires influences the amount of metal flux reaching the side wall through the 'shadow effect'.



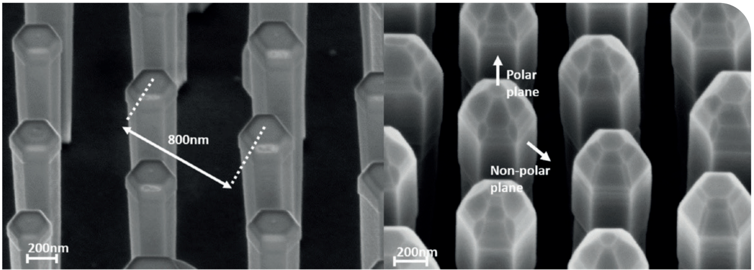
➤ Figure 5. Current-voltage characteristics of AlN nanowire-based LEDs processed using standard lithography techniques. The active region consists of a short section of gallium-doped AlN where the formation of gallium-rich nanoclusters was put in evidence. The inset shows an individual LED and the tip used to contact it. The random measurement of several different LEDs illustrates the reproducibility from LED to LED.

Novel emitters

One difficulty specific to nanowire LEDs is that during the processing of these devices, the space between the nanowires has to be filled with an insulating, UV-transparent material to prevent metal deposition on the base plane or along the side walls. If this action were not taken, there is the possibility of short-circuiting the LED structure. Taking this into account, we have applied standard lithography to process a 280 nm LED (see Figure 5). Electrical measurements reveal a rectifying character for the current-voltage characteristics. Such behaviour underlines the potential of full (Ga)AlN-based nanowire heterostructures, and opens the path to the development of a new generation of devices, assessed by electroluminescence data (see Figure 6).



➤ Figure 6. Electroluminescence spectra of one AlN nanowire LED emitting at 280 nm. The onset of the electroluminescence spectra signal starting at 6 V is consistent with the bandgap of AlN and the LED band structure. Below a current density of 0.2 A cm^{-2}, optical power scales linearly with the current density, which is typically expected for LEDs, as the optical power is the product of current density and external quantum efficiency. Deviation of this behaviour above 0.2 A cm^{-2} is assigned to losses.



➤ Figure 7. AlN nanowire (NW) sections are grown on an array of in-plane ordered GaN pillars, with a pitch of 800 nm. The upper section of the AlN NW section, shown in the right, is enlarged with respect to the GaN pillars, due to non-negligible lateral growth. It exhibits crystallographic facets associated with low surface energy planes. The polar plane corresponds to a (0001) facet and the non-polar plane to a $(1\bar{1}00)$ facet.

FURTHER READING / REFERENCE

➤ R. Vermeersch *et al*. Comprehensive Electro-Optical Investigation of a Ga-Doped AlN Nanowire LED for Applications in the UV-C Range, ACS Appl. Nano Mater. **6** 13945 (2023)

At this stage, it appears that our spontaneously formed nanowires address many of the challenges associated with nitride-based deep-UV emitters. Due to the versatility of their growth – they can be formed on virtually any kind of substrate – and their reduced diameter, generally smaller than 100 nm, they fulfil requirements for increased light extraction while easing strain relaxation and enhancing electrical doping and current injection.

However, that's not to say that all challenges have been overcome. These potential advantages are counterbalanced by a major inconvenience: dispersion in the diameter and the length of the nanowires, variations that are directly related to the spontaneous, random nucleation process. Making matters worse, this dispersion is amplified by 'shadow effects', which modulate the amount of metal reaching each individual nanowire (see the box "Shadow effects" for more details). One of the consequences of the shadow effect, which amplifies differences due to diameter dispersion, is an electrical resistance that varies between a nanowire and it neighbours. An upshot of this is that only a limited number of nanowires contribute to the final device, due to the natural tendency of current to flow along the less resistant path.

Due to this issue that is associated with spontaneously nucleated nanowires, there is now much interest associated with the in-plane ordered growth of homogeneous ensembles of regularly spaced nanowires. Such structures can deliver a superior emission chromaticity and homogeneous current injection, and ultimately aid the introduction of new classes of innovative, efficient LEDs and microLEDs that span the entire UV and visible wavelength range.

Due to this great potential, we are now focusing on the development of deep-UV LEDs via the in-plane ordered approach. Our plan is to exploit the assets of MBE by combining its ability to control the growth of monolayer and sub-monolayer GaN quantum wells with the use of GaN templates grown by selective-area MOCVD (see Figure 7 for an array of such GaN pillars, and the AlN nanowire sections grown on top of them).

We are pleased to see that progress with MBE is popularising the use of 200 mm silicon substrates. Such an advance, drawing on the assets of MBE, in particular controlled growth of GaN quantum wells at the atomic scale, has the potential to change the paradigm of UV LED fabrication. The recent demonstration by Silanna of Brisbane, Australia, of layer-based UVC LEDs grown by MBE with a an impressive external efficiency of 0.8 percent at 235 nm is an illustration of the potential of this epitaxial technique and its capabilities to successfully compete with MOCVD. Our own target is to fulfil the promises of MBE-grown nanowire-based LEDs in the UVC range and take advantage of the fascinating properties of these miniature marvels.

The 14th CS International will see 40 leaders from industry and academia delivering presentations that fall within five key themes: Ensuring SiC's Phenomenal Success; Expanding Horizons for Surface Emitters; Accelerating the Growth of GaN; Taking Power from the Photon; and New Frontiers for the LED.

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Extremely high-power transmitters for access networks

Sources that combine a laser, a modulator and an amplifier in a single device are laying the foundations for high capacity access networks

BY HÉLÈNE DEBRÉGEAS FROM ALMAE TECHNOLOGIES

DUE TO THE PHENOMENAL rise of YouTube and TikTok, many are watching more content on-line. To accommodate this trend, there's been a tremendous rise in internet traffic, with this growth showing no sign of abating. Consequently, capacity has to increase throughout the fibre-optic network, from the long-haul links that span many thousand kilometres to the shorter connections, such as the optical access networks providing the 'last mile' between internet service providers and their customers.

Given this state of affairs, it's not surprising that optical access networks are continuing to be rolled out at great pace. And as well as this additional deployment, throughput is on the up – initially, transmission speeds were 2.5 Gbit/s, recently they climbed to 10 Gbit/s, and sometimes data rates are now as high as 25 Gbit/s and even 50 Gbit/s.

Unfortunately, increasing the capacity of optical access networks is more complex than it appears at first glance. While sources with higher optical modulation rates are essential, they are not the only factor that matters.

In addition, there's a need for a high optical power, because access networks – also known as passive optical networks (PONs) – have no optical amplification, setting them apart from other long-distance networks. This lack of amplification means that the losses resulting from propagation in the fibre and splitting among multiple end users ultimately limit both the network's geographical coverage and the number of its end users.

To optimise the capacity of PON networks, they must include highly sensitive photodiodes that detect the low optical power they receive, and transmitters delivering the highest possible output power. For current applications, such as 10G-PON, 25G-PON and 50G-PON, the modulated power in the fibre needs to be around 4 mW. However, to increase capacity, new access networks are demanding a

modulated power of up to 10 mW in the fibre, with even higher values sure to follow.

For upstream transmissions – that is, transmissions from the end user to the network – O-band wavelengths are used. This spectral domain, which is around 1.3 µm, benefits from an absence of chromatic dispersion in the fibre. A lack of distortion of the optical signal results, enabling implementation of powerful yet low-cost transmitters on the user's premises. In this case, the most suitable source is the directly modulated laser: by simply modulating the electric current injected into the laser, modulation of the emitted power follows.

It's a very different story for downstream transmission, which involves the transfer of data from the network to the end users. Wavelengths used for this task vary, ranging from 1342 nm for 50G-PON to 1577 nm for 10G-PON. However, in all cases, there is significant chromatic dispersion in the fibre.

One troublesome consequence of this dispersion is that the quality of the signal that's emitted by directly modulated lasers is insufficient for transmission with an acceptable degree of errors. Due to this, externally modulated lasers (EMLs) are deployed for downstream transmission in access networks. This class of laser comprises two sections: a laser, powered by an electrical current, that emits a constant optical signal; and an electro-absorption modulator section, which is transparent at zero voltage, but absorbs light under a negative voltage. Through application of a modulated voltage, typically between 0 V and -2 V to the modulator section, successions of bits 0 and 1 can be transmitted at high data rates.

The downside of the EML is that it is more expensive to manufacture than the directly modulated laser. However, the additional cost is acceptable, because the component is only deployed in core network terminals and not on the user's premises. The EML has a high reputation, thanks to its capability to transmit a much higher quality signal: there is a strong power contrast between the 0s and 1s; and there is high spectral purity, ensuring the source is resistant to chromatic dispersion. Following continuous improvements to EMLs for access networks, the modulated power in the fibre now reaches the order of 4mW, meeting today's needs.

However, while the power provided by the EML is adequate for access network coverage, it is still a limiting factor. What's more, this weakness is only going to become more of an issue, as a further power increase is a key differentiator in next-generation high-capacity access networks.

A radical approach is needed to address this concern, because EMLs are getting close to the glass ceiling for their output power. Even if the power of the laser section is increased, it's not possible to maintain the performance of the modulator. That's because there is an intrinsic issue, associated with absorption of photons that create electrical carriers in the modulator. As the injected power increases to a very high value, carrier evacuation cannot keep up, so the carriers accumulate and screen the voltage that's applied to the modulator. Making matters worse, the photogenerated electric current creates an opposing electric voltage in the modulator supply circuit. Both these effects contribute to a distortion of the signal emitted by the EML, and impose modulation voltages that are too high for implementation in the system.

Amplifying concerns

Offering a way forward that allows the realisation of modulated powers of 10 mW or so is the addition of a third section to the EML: a semiconductor optical amplifier (SOA). With this refinement, injection of an electric current into the SOA ensures optical gain in this section through a multiplication of the photons that are passing through it. In theory, the SOA simply boosts the power emitted by the EML.

There are several advantages that come from this approach. First, the EML no longer needs to emit as much power, since there is now optical gain from

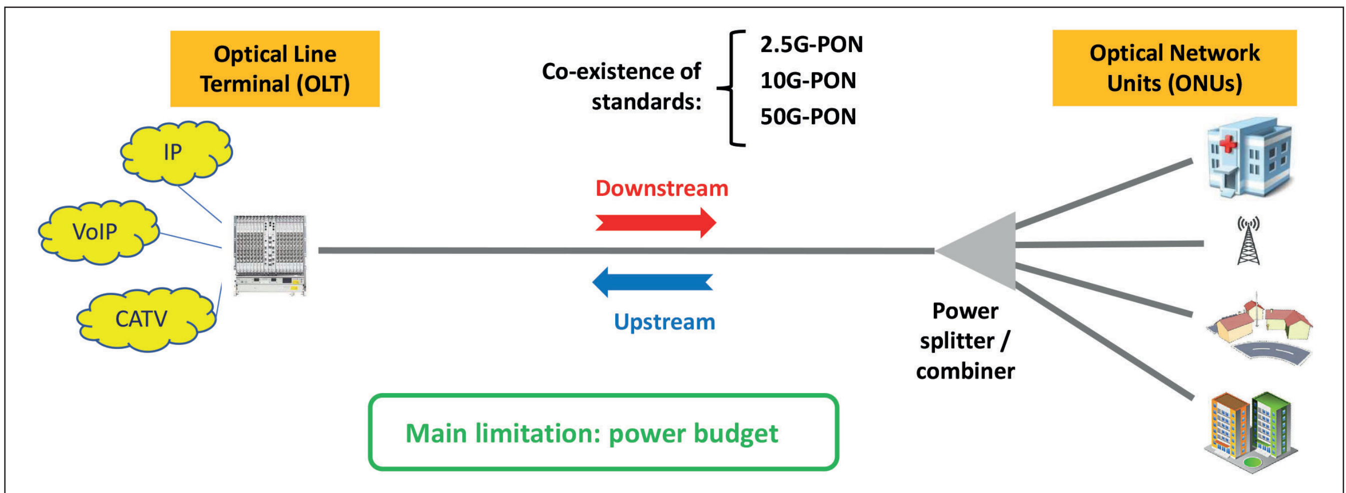


Figure 1. An illustration of a Passive Optical access Network (PON).

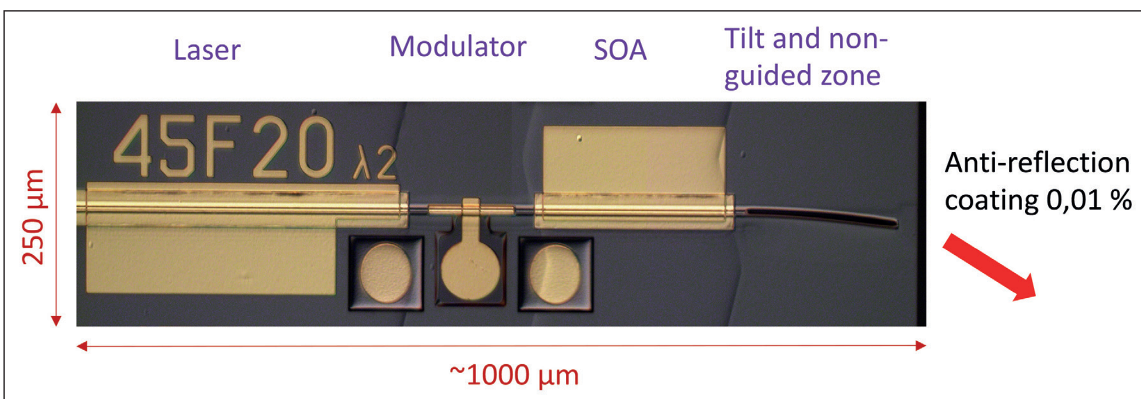


Figure 2. Top view image of a high-power transmitter (EML-SOA), including laser – modulator – amplifier – output passive tilted waveguides.

the SOA that is located after the modulator section. Thanks to this refinement, the problems associated with modulator saturation and the loss of modulation efficiency are eliminated. What's more, as the SOA section is very similar to the laser section, it can be manufactured using the same processing steps. The only noteworthy change is that the surface area of the chip increases. Finally, the SOA section improves the quality of the optical signal through the addition of so-called negative chirp, increasing the capability to combat chromatic dispersion in the fibre.

However, it is far from simple to enjoy all these benefits. That's why the EML-SOA is only starting to be offered as a practical option for the transmitter. Note that great care is needed when taking this approach, because there is the threat that the SOA can severely degrade the performance of the EML.

One of the causes of this is that the SOA suffers from saturation. When too much optical power is injected, the density of photons propagating and multiplying reaches a value that leads to the consumption of all injected electrical carriers. At this point, the SOA fails to provide amplification, a condition described as gain saturation. This is highly problematic, as when the modulated optical signal injected into the SOA goes from a bit 0 to a bit 1, the injected power suddenly increases and the gain saturates in a few hundred nanoseconds. Due to this, the power of bit 1 gradually decreases, resulting in very high noise levels for bit 1s, an issue that prevents data transmission.

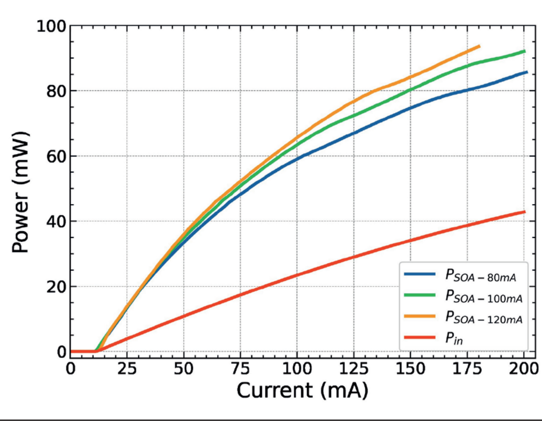
A second concern is that the EML is very sensitive to optical feedback at the output facet. While most modulated light leaves the chip, a small portion is reflected by the facet and excites the laser section, which begins oscillating at a resonance frequency of a few gigahertz. This oscillation totally disrupts the emitted signal, preventing the correct transmission of the information bits. To limit this effect on an EML, an anti-reflection coating of around 0.01 percent is applied to the output facet.

However, with the EML-SOA, optical feedback is amplified by around a factor of ten as light traverses back and forth along the SOA. Due to this, there's the need for a 0.001 percent facet anti-reflection coating, which is not industrially feasible.

Finally, the SOA section requires an additional electrical current. However, this is restricted, because there's a need to limit the power consumption of the transmission modules. It can be assumed that the total for the laser and the SOA should be in the same range as the current for just an EML laser.

Addressing the challenges

At Almae Technologies of Marcoussis, France, we have tackled all these concerns while developing an EML-SOA for emerging high capacity access networks. Our device, suitable for 10G-PON and 50G-PON, targets a very high modulated power in the fibre of around 10 mW. To realise this level of performance we have adapted the design, so it is



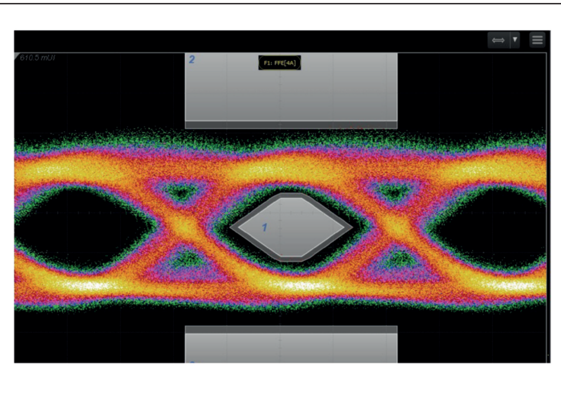


Figure 3. (Left) Output power produced by the semiconductor optical amplifier as a function of input power. (Right) 25 Gbit/s eye diagram with mask margin.

capable of a high-quality modulated signal and a low power consumption.

Our design excels by incorporating a fourth optical waveguiding output section, comprising a bend leading to a 7° output tilt, and a section without a waveguide where light diffracts. Thanks to this architecture, the optical mode is very wide and at an angle of 7° when it encounters the 0.01 percent anti-reflection coated output facet. This ensures that the small portion of reflected light is strongly spread out spatially, forming an angle of 14° with the optical guide. It is a configuration that ensures 99 percent of the reflected light is radiated, while just 1 percent is recoupled into the optical waveguide, where it could possibly disturb the laser section. The combination of the tilt and the unguided zone ensures that despite the SOA section, the device remains compatible with a standard 0.01 percent facet anti-reflection coating, while avoiding laser oscillation.

When designing our EML-SOA, we did not focus on optimising the laser section by placing our emphasis on a high power and low threshold current, but directed our attention to the SOA section. For this part of our device, we placed a premium on realising the highest possible SOA saturation output power. To achieve this, we selected a stack of semiconductor layers that reduced propagation losses, and ensured a less-confined optical mode to avoid too high a photon density. These choices enabled us to more than double the saturation output power of the SOA.

With these optimisations, our EML-SOA operates at record output powers, without any degradation in the quality of the modulated signal. For deployment in 50G-PON networks, our device provides 4 mW modulated in the fibre, for an EML with a laser current of 110 mA; and 10 mW modulated in the fibre, from an EML-SOA with only 135 mA of total laser and SOA current. And for the 10G-PON, we go from 3.5 mW modulated in the fibre with an EML having a laser current of 110 mA to 7 mW modulated in the fibre with an EML-SOA having a total laser and SOA current of just 150 mA. If it seems that there are too many numbers to digest, just note that we have more than doubled the modulated output power for an increase of only 20-30 percent power consumption.

Our EML-SOA results are extremely important for next-generation access networks because in addition to increasing the modulation rate, they open the door to very large capacities, in terms of both geographical coverage and the number of users. Our devices are currently in pre-production phase, with market launch slated for later this year.

It is possible that our technology may also have a role to play in other networks. It is unlikely to be deployed in long-haul networks, as in this case transmission is in the C-band, centred around 1.55 μm, where signals can be amplified by erbium-doped fibre amplifiers. But our EML-SOAs might serve in networks involving O-band transmissions around 1.3 μm, as today they do not have any form of in-line optical amplification. The O-band is used for interconnections between datacentres (400 Gb Ethernet and beyond), with data transmission supported by several very high-speed 100 Gbit/s EMLs. Here the transmission distance is limited by the optical power budget to around 40 km, and the introduction of our high-power EML-SOAs could increase that distance by several tens of kilometres. So it's clear that our device has plenty of promise.

Almae Technologies: A French integrated device manufacturer of InP photonic devices

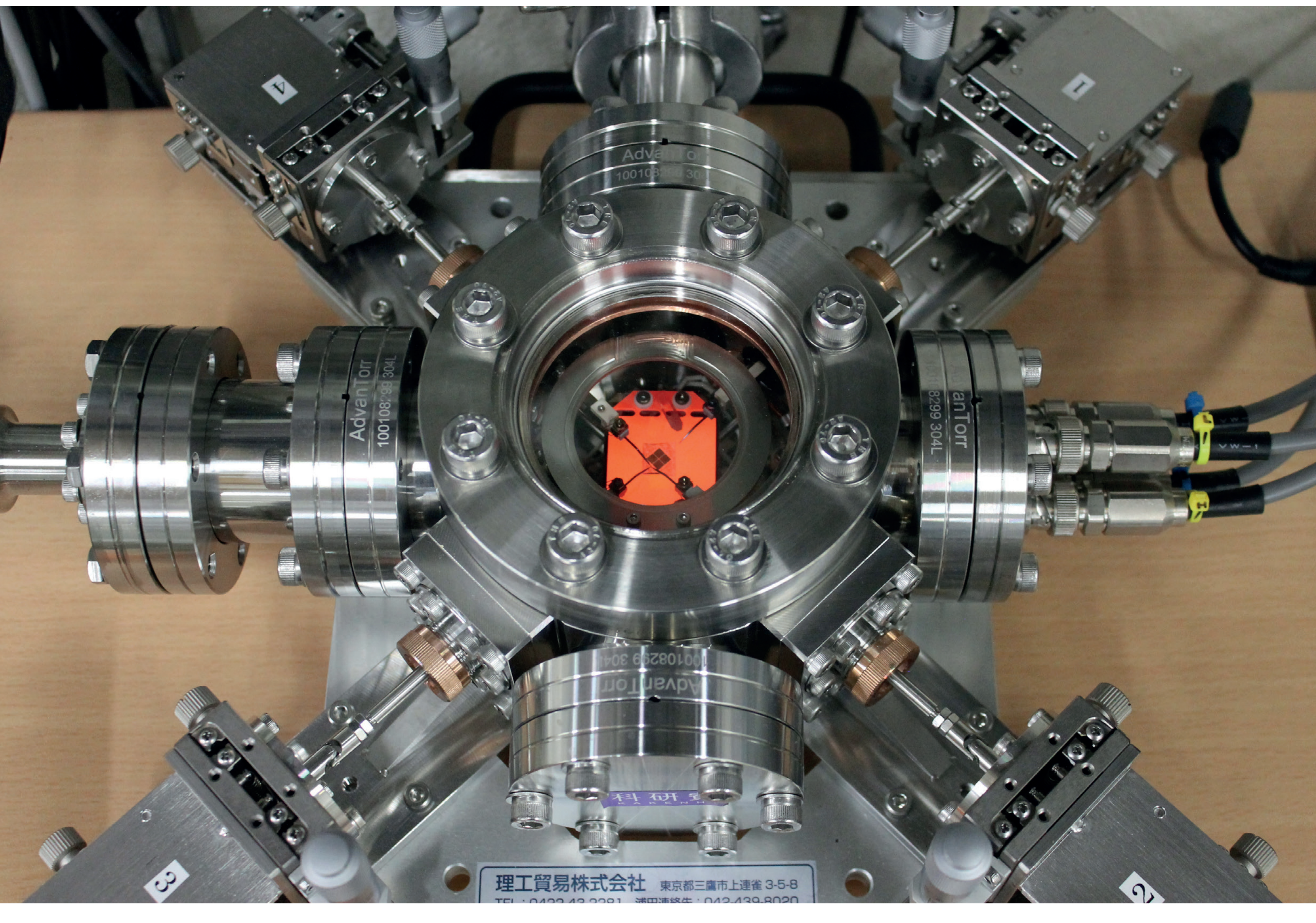
FOUNDED IN 2016, Almae Technologies is a spin-off from III-V Lab, which is a joint research laboratory between Nokia Bell Labs, Thales R&D, and CEA-Leti. The aim of Almae is to build an industrial supply chain for producing and marketing InP components coming from advanced research and development.

Today, Almae has 40 employees, all experts in the field. The company – a well-known Integrated Device Manufacturer (IDM) for advanced InP based photonic chips in Europe – is located south of Paris. From this location, equipped with a 1,700 m^2 clean room, the company undertakes the design, development, and end-to-end manufacturing of InP wafers, including the epitaxial growth of materials, testing and prototyping.

Almae's debut component is a 10 Gbit/s Externally Modulated Laser (EML) for transmission up to 80 km that covers Dense Wavelength Division Multiplexing (DWDM) channels within the C-band, which spans 1530 nm to 1565 nm. This laser, now produced in volume on an in-house production line, is qualified by external customers for field applications.

The team at Almae engages in a great deal of innovation, enabling development of many new products for emerging markets. All these new components, which are based on optimised and specific designs, use exactly the same technology as the 10 Gbit/s EML. This means that these novel components can take advantage of the maturity and efficiency of the production line for design-focused development, to ensure rapid qualification and time-to-market.

New products in Almae's market launch phase include 100 Gbit/s EMLs for datacentre interconnection, 1577 nm EMLs for 10G-PON, and high-power O-band or C-band lasers as sources for silicon photonics modulators, lidar and sensing. EML-SOAs for very high power 10G-PON and 50G-PON (10 mW modulated in the fibre) are in the pre-production phase, with a market launch scheduled for 2024. Another part of Almae's technology involves the integration of laser components or gain sections into silicon platforms using low-cost passive alignment processes.



Extreme-temperature devices using AlN

Diodes and transistors with AlN channels deliver high breakdown voltages and operation at incredibly high temperatures

BY HIRONORI OKUMURA FROM UNIVERSITY OF TSUKUBA

A NUMBER OF human activities are expanding into extreme environments, often motivated by resource exploitation. This has taken exploration in various directions, including deep underground, to great depths at sea and into deep space. In all these environments the temperature is extreme – it exceeds 300 °C on the surface of Venus, in deep-well drilling, and in the space inside an operating engine.

To find out more about all these environments demands the deployment of sensors. But the most obvious ones – that is, those based on silicon – are not up to the task, due to a relatively low operating temperature limit. This means that in order to enrich our lives from these environments, we need to develop extreme-temperature electronics.

When all forms of semiconductor device are operated at extreme temperatures, they face issues associated with materials, electrodes, gate oxides and packaging (see Figure 1). As the temperature increases, numerous electron-hole pairs are generated, due to excitation of electrons from the valence band maximum to the conduction band minimum. These electrons, which increase the intrinsic-carrier concentration (see Figure 2 (a)), are detrimental, as they increase the leakage current of the devices and prevent them from turning off. Options for reducing the leakage current include introducing semiconductor materials with a larger bandgap energy and lower intrinsic carrier concentrations (see Figure 2 (b)), or restricting current diffusion from areas other than the channel. Turning to a channel layer surrounded with high-resistivity layers that have low effective

➤ Left. High-temperature probe station (ExPP Co., Ltd.). The maximum measurement temperature is 1173 K, thanks to tungsten probes, ceramic heaters, a sapphire viewport and a thin-profile sample stage. A type R thermocouple monitors the temperature under the ceramic heater.

donor/acceptor concentrations and low defect concentrations can raise the device's operating temperature. Another approach is to deploy devices with *p-n* junctions, such as JFETs and BJTs. In these cases, it's also important to select refractory metals for the electrodes that have minimal reactivity with base semiconductors. In particular, titanium, vanadium, tantalum, molybdenum, tungsten, and platinum are better for this purpose than aluminium, magnesium, copper, silver, indium, and gold.

Why use AlN?

There are many semiconductor materials with a larger bandgap energy than silicon. They include SiC (3.3 eV), GaN (3.4 eV), Ga_2O_3 (4.7-5.2 eV), diamond (5.5 eV), and AlN (6.1 eV). The team at NASA, led by Philip Neudeck, have reported that SiC JFETs can operate at temperatures over 800 °C. While this is undoubtedly an impressive result, materials with even wider bandgaps promise to reach even higher temperatures. However, quite a few of them have significant drawbacks. GaN suffers from a high effective donor concentration of 10^{16} cm^{-3}; it's not possible to form *p*-type Ga_2O_3 layers; and diamond starts to reacts with oxygen at around 700 °C. In stark contrast, AlN has no obvious flaws, and offers thermal stability and controllable doping. Due to these attributes, our team at the University of Tsukuba has been devoting all our attention to AlN for the development of extreme-temperature devices.

Historically, it's been assumed that AlN is only good as an insulator. However, around 20 years ago Yoshitaka Taniyasu and colleagues at NTT demonstrated that this is not the case by growing electrically conductive AlN layers by MOCVD. This team recorded an electron mobility of 426 cm^2 V^{-1} s^{-1} for silicon-doped AlN layers, for a dopant concentration of 3 x 10^{17} cm^{-3}. Building on this work, they went on to pioneer *p*-type AlN growth and demonstrate the first AlN LEDs with a wavelength of 210 nm and quasi-vertical AlN *p-n* diodes. These successes are to thank for the recent, rapid development of deep-UV LEDs based on AlGaN and AlN.

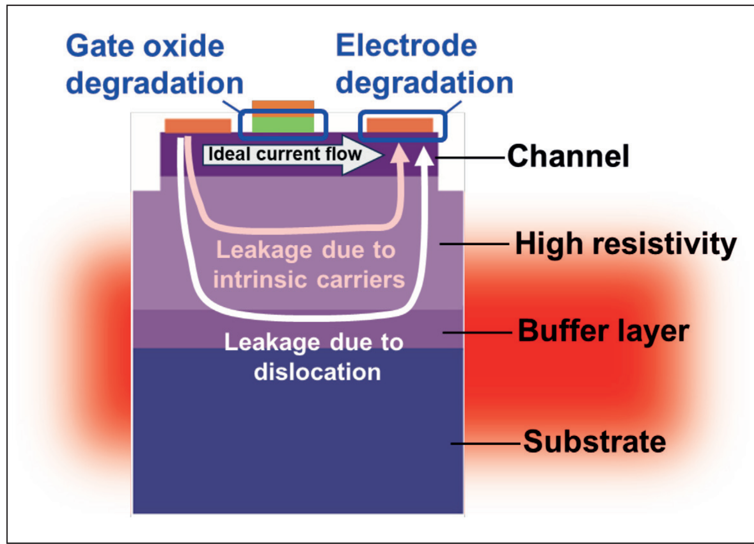
As well as optical devices, the research community has investigated AlN Schottky barrier diodes and AlN/AlGaN HEMTs, to explore the potential benefits of a high critical electric field. Unfortunately, these devices suffer from a low carrier concentration, due to high ionization energies for the donors and acceptors – it is 0.3 eV for silicon and 0.6 eV for magnesium. Due to this, carrier concentrations for both these dopants are around two orders of magnitude lower than their concentrations, causing devices to have very small currents. To overcome this problem, our team, in working in partnership with researchers at MIT and Aalto University, have broken new ground by introducing polarisation-induced doping in N-polar AlGaN/AlN structures. Thanks to spontaneous and piezoelectric polarisations, this form of doping can increase current and lower contact resistivity. Using polarisation-induced doping, we have demonstrated the first N-polar AlN-based PolFETs and HEMTs with drain currents over 100 mA mm^{-1}. Such success has led us to view AlN as a practical semiconductor for optical and electrical devices.

To produce these devices, we have been able to draw on a number of material suppliers. High-quality AlN samples on 2-inch sapphire substrates can be purchased from Dowa Electronics Materials, and 2-inch bulk AlN is commercially available from Stanley and Asahi Kasei.

Doping AlN

Controlling the concentration of dopants in semiconductors is the incorporation of impurities during crystal growth, as well as thermal diffusion and possibly implantation. The latter is an attractive technology, enabling precise dose control and ensuring a high lateral uniformity of the dopant. However, when high-dose implantations are employed, they tend to damage crystal lattices and introduce high concentrations of point defects, which can compensate carriers. Fortunately, most of this damage can be repaired with post-thermal annealing, which we have used when producing a silicon-implanted *n*-type AlN channel.

One of the impressive traits of AlN crystals, including their surfaces, is a robustness at elevated temperatures, with stability under nitrogen gas at up to 1700 °C. This robustness provides a wide window for repairing implantation damage – this process requires temperatures above 1200 °C for electrical activation of the silicon-implanted AlN layer.



➤ Figure 1. The leakage current path and the thermal degradation points in a MESFET with a gate oxide.

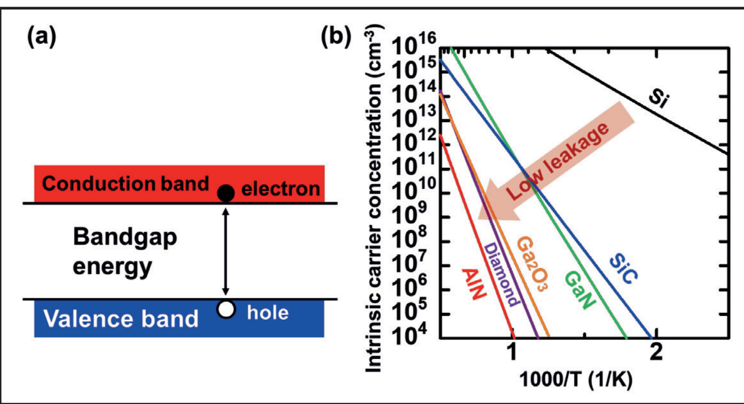


Figure 2. (a) An illustration of electron-hole pair generation at high temperatures. (b) The intrinsic carrier concentration of silicon, SiC, GaN, β-Ga_2O_3, diamond, and AlN as a function of reciprocal temperature.

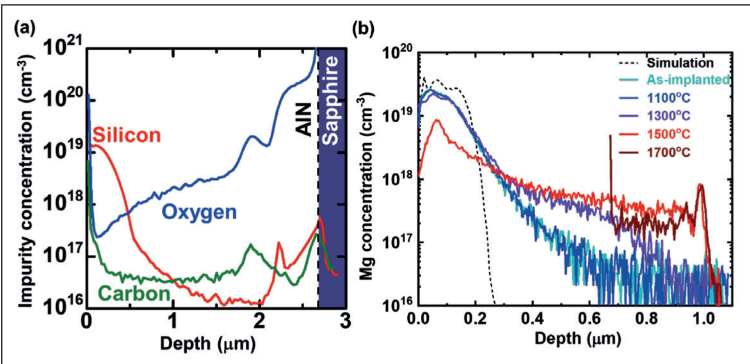


Figure 3. (a) Depth profiles of the impurity concentration of silicon, oxygen, and carbon in a 3 μm-thick silicon-implanted AlN layer after annealing at 1600 °C. (b) Depth profiles of the magnesium concentration in a 1 μm-thick, magnesium-implanted AlN layer after annealing.

Note, though, that much thought is needed when selecting the annealing temperature, as it can drive other changes in the material. Beyond 1400 °C, silicon and oxygen impurities diffuse within the layer above. Due to diffusion of oxygen atoms from the sapphire substrate, which decomposes at 1500 °C under nitrogen gas, a thin AlN layer on a sapphire substrate will have a high oxygen concentration after high-temperature annealing, leading to degraded electrical characteristics.

Through collaboration with MIT, Aalto University, TNSC, and Dowa Electronics Materials, we have investigated the diffusion of silicon, oxygen and magnesium atoms in AlN (see Figure 3). Our investigations revealed that oxygen atoms diffusing from a sapphire substrate cannot reach the channel layer after annealing by using 3 μm-thick AlN layers. This led us to conclude that the preferred annealing temperature ranges for electrically conductive AlN layers with silicon and magnesium implants are 1200-1600 °C and 1400-1500 °C, respectively. This knowledge enabled us to demonstrate the first AlN-channel transistors.

When the fabrication of devices involves conditions close to thermal equilibrium, such as epitaxial growth and high-temperature annealing, the formation of deep states with ionization energies of 250-320 meV is favoured. This tends to lead to self-compensation of the silicon donor, a situation in agreement with our results.

Meanwhile, the use of non-equilibrium processes, such as ion implantation, enables an increase in the population of shallow donors with ionization energies of 64-86 meV. This led Hayden Breckenridge and colleagues at the University of North Carolina and Adroit Materials to produce a highly conductive layer of AlN by silicon implantation and post-annealing at a relatively low temperature of 1200 °C. Another encouraging result, coming from Kyoto University, is that the substitutional magnesium-acceptor binding energy of AlN is only 250-410 meV, a value much smaller than the ionization energy of magnesium acceptors in common MOCVD-grown AlN layers. Taken together, these results indicate that if non-equilibrium process conditions can be reproducibly and easily controlled in AlN that's doped with silicon and magnesium, this could open the door to electronic and optical devices with significantly improved performance.

Electrical properties of AlN

To improve the electrical performance of AlN-based devices, there is more to do than just address the high resistivity of *n*-type and *p*-type AlN layers that are impaired by low carrier concentrations. In addition, there's a need to tackle the high contact resistivity, resulting from the small electron affinity. It is particularly challenging to make an ohmic contact at room temperature in AlN. The voltage drop is governed by the height of the Schottky barrier, which depends on the difference between the metal work function and the semiconductor electron affinity. It is possible to produce ohmic contacts by lowering the potential barrier height through appropriate selection of electrode materials. Options for *n*-type AlN are titanium, aluminium,

> To improve the electrical performance of AlN-based devices, there is more to do than just address the high resistivity of *n*-type and *p*-type AlN layers that are impaired by low carrier concentrations

vanadium and molybdenum, while ohmic contacts to *p*-type AlN can use palladium and NiO.

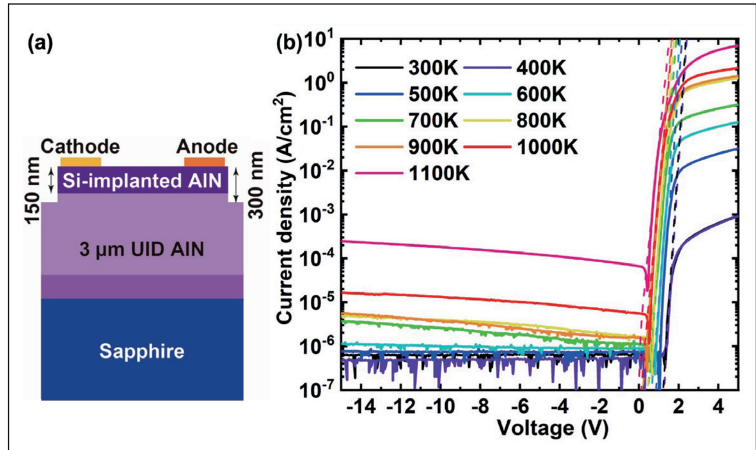
One implication of heavy doping in semiconductor materials is a decrease in the depletion-region width, leading to tunnelling through potential barriers. The heavy doping of the topmost AlN surface is very important for ohmic contacts. However, as the concentration of silicon and magnesium dopants in AlN layers is limited to around 10^{19} cm^{-3}, perhaps due to the formation of compensation defects, there is no prospect for field-emission tunnelling.

To determine the carrier concentration and carrier mobility in semiconducting structures, researchers tend to turn to Hall-effect measurements. As these measurements need ohmic behaviour, some studies have used heavily doped GaN contact layers. This enabled the determination of the electrical properties of AlN, both at room temperature and at elevated temperatures. Along with others, we have evaluated the carrier concentration and carrier mobility at high temperatures, obtaining values for *n*-type and *p*-type AlN at temperatures beyond 200 °C and 500 °C, respectively.

When undertaking this study, we uncovered a new problem associated with high-temperature measurements. We had to use a probe station, as we lacked bonding and package technologies for extreme temperatures. We also found that normal probe tips deteriorate at high temperatures. Note that most reported devices have a maximum operating temperature of no more than 500 °C, implying that measurements of electrical properties are unreliable at temperatures higher than this.

Working with Dowa Electronics Materials, we have evaluated the electrical characteristics of 3 μm-thick AlN layers on sapphire substrates with a high-temperature probe system offering a maximum measurement temperature of 900 °C in high vacuum. For this effort we implanted silicon in the AlN layer at room temperature to obtain *n*-type conductance; the concentration was 2×10^{19} cm^{-3} in a 150 nm-deep box profile. These silicon-implanted AlN layers were subsequently annealed at 1500 °C. We then deposited Ti/Al/Ti/Au electrodes for ohmic contacts, prior to sintering at 950 °C.

Our electrodes deteriorated at 877 °C, possibly due to a reaction between Ti/Al and AlN. This led us to seek suitable metals for ohmic contacts at extreme temperatures. For the temperatures we were able to consider, we observed a current-voltage relationship that's non-linear below 127 °C and almost linear above 227 °C. Evaluating electrical properties between 227 °C and 827 °C revealed that sheet resistance and contact resistivity decreased with increasing temperature. From 227 °C to 627 °C, as the temperature increased electron mobility slightly fell, but the electron concentration increased due to enhanced donor ionization, resulting in a



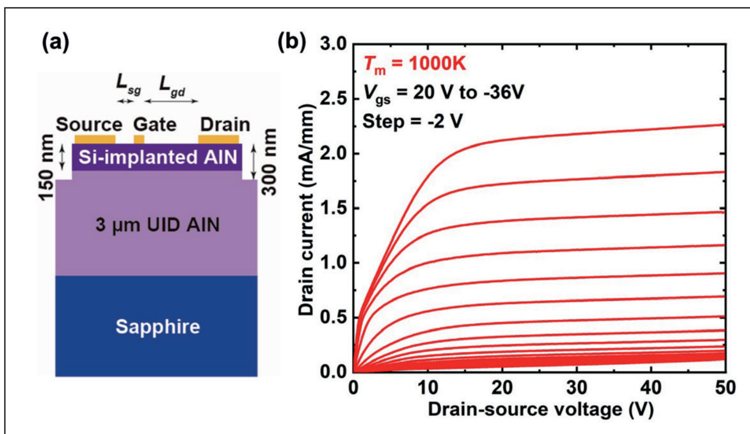
➤ Figure 4. (a) The cross-section of a Schottky barrier diode with a silicon-implanted AlN channel. Ni/Au anode and Ti/Al/Ti/Au cathode. (b) Current density-voltage characteristics of an AlN Schottky barrier diode from 27 °C to 827 °C.

reduction in sheet resistance at high temperatures. This led us to conclude that *n*-type AlN layers exhibit excellent performance at extreme temperatures.

Diodes and transistors

We have fabricated Schottky barrier diodes and MESFETs with silicon-implanted AlN layers on sapphire substrates. Our diodes are capable of operating at 827 °C (see Figure 4), surpassing all previous records, while our transistors can operate at up to 727 °C (see Figure 5). The AlN Schottky barrier diodes have a breakdown voltage of 610 V at room temperature, while the corresponding value for the AlN MESFETs at 727 °C is 176 V. We are keen to point out that these devices are practically feasible, because they have a simple structure, and the AlN layers are grown on large, low-cost sapphire substrates.

To fabricate our Schottky barrier diodes and MESFETs, we used Ni/Au for the anode and gate contacts. We found nickel to be thermally stable, hardly reacting with AlN, even at 827 °C. What's



➤ Figure 5. (a) Schematic cross-section of MESFET with a silicon-implanted AlN channel. (b) DC output characteristics of an AlN MESFET at 727 °C.

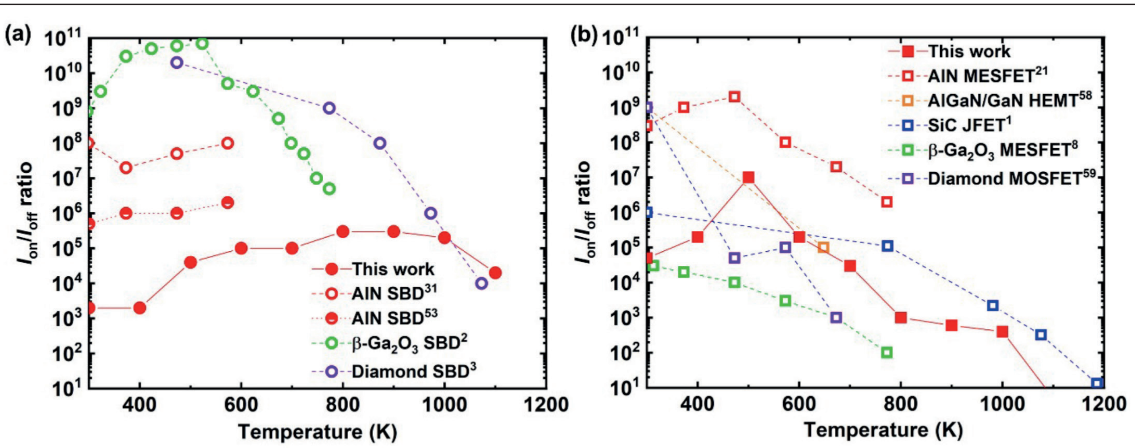


Figure 6. A benchmarking plot, comparing the current on–off ratio versus measurement temperature of AlN devices with the other state-of-art (a) Schottky barrier diodes and (b) FETs.

more, in terms of electrical characteristics, we found little difference between Ni/Au and Pt/Au. For the Schottky barrier diode, the off current is small, even at 827 °C, due to the low intrinsic carrier concentration and the thermally stable Ni/AlN interface. However, the off-state drain current of the AlN MESFET is high at 727 °C, due to leakage through the bottom undoped AlN layers and the high concentration of defects. Unlike the current in silicon devices, which falls at high temperatures due to phonon scattering, we discovered that the forward current of AlN Schottky barrier diodes and MESFETs continues to increase with temperature up to 827 °C. We attribute this to the current in AlN devices at extreme temperatures being dominated by the increase in electron concentration and the reduction in contact resistivity, with the reduction in electron mobility playing a secondary role.

Our development of AlN devices is paving a new way to making semiconductor devices that can operate at extreme temperatures. Although there is a trade-off between the on-off ratio and the temperature of Schottky barrier diodes and FETs (see Figure 6), AlN devices have much potential for improvement. For example, it should be possible to increase the on/off ratio at extreme temperatures through a combination of homoepitaxial growth and the introduction of a JFET structure. Additional improvements could come from the introduction of heat-tolerant ohmic contacts, rather than Ti/Al/Ti/Au, a move that would increase the operating temperature to over 877 °C.

For most extreme-temperature applications, ICs need to operate reliably over long periods. Such circuits are fabricated with complementary technology, with *n*- and *p*-channels. At Kyoto University, engineers have developed a SiC complementary JFET logic gate that operates at 350 °C. We hope to take our work in a similar direction, producing complementary JFETs with homoepitaxial AlN channels that are capable of operating in extreme environments.

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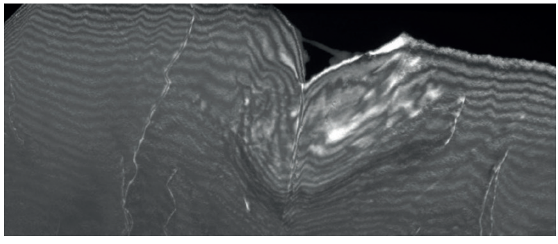
The case for better templates

Higher-quality AlN-on-sapphire templates are need to improve the performance of deep-UV LEDs, according to evidence provided by a range of characterisation techniques

RESEARCHERS at the University of California, Santa Barbara, say that better templates are needed to improve the performance of the deep-UV LED.

A common platform for this light source, which is an attractive option for disinfection applications, is the commercial AlN-on-sapphire template. However, the quality of this template can limit the thickness of the *n*-type AlGaN layer within the LED, thereby impacting the sheet and series resistance and ultimately dragging down the device's wall-plug efficiency.

"With the current threading dislocation densities offered from commercial AlN-on-sapphire templates, thick *n*-AlGaN growth beyond 800 nm is problematic due to threading dislocation inclination," explains team spokesman Michael Wang.



➤ Cross-sectional transmission electron microscopy uncovers cracks in thicker layers of *n*-AlGaN.

He claims that reducing the threading dislocation density of commercial templates by an order of magnitude would enable much thicker *n*-AlGaN films, and thus better voltage efficiency at higher currents.

According to Wang, commercial devices tend to operate at more than 20 A cm^{-2}. "If a thin *n*-AlGaN layer is used, the wall-plug efficiency will be limited at these current densities," remarked Wang.

Yet another benefit of higher-quality templates is that they increase the internal quantum efficiency of the LED, thanks to a reduction in non-radiative recombination in the active region.

The study by Wang and co-workers involved growth by MOCVD of deep-UV epistructures on commercially available AlN-on-sapphire templates. On these templates the team added a 70 nm-thick $Al_{0.85}Ga_{0.15}N$ buffer and a 400 nm-thick silicon-doped $Al_{0.65}Ga_{0.35}N$ layer, using a low III-V ratio to improve conductivity and morphology. These layers were followed by a lightly doped smoothing superlattice, an active region with six 1.5 nm-thick $Al_{0.5}Ga_{0.5}N$ quantum wells, an electron-blocking layer, a *p*-type superlattice and a *p*-contact layer.

The team also produced several *n*-type AlGaN samples, formed by keeping silicon-doping in the $Al_{0.65}Ga_{0.35}N$ layer at 5 x 10^{19} cm^{-3} and increasing the thickness. According to atomic force microscopy scans of 2 μm by 2 μm areas of these samples, increasing the thickness of the $Al_{0.65}Ga_{0.35}N$ layer from 400 nm to 1600 nm led to an increase in root-mean-square roughness from 3.4 nm to 22 nm. This far higher roughness resulted from the presence of large hillocks.

Reciprocal space mapping of the samples using X-ray diffraction revealed that when the $Al_{0.65}Ga_{0.35}N$ layer is 400 nm-thick it is fully strained, but when the thickness is increased to 800 nm and 1600 nm it is 38 percent and 100 percent relaxed, respectively. The X-ray diffraction-based technique also determined that as the thickness of $Al_{0.65}Ga_{0.35}N$ increases, there is a compositional drift to higher gallium content, possibly due to a compositional pulling effect.

The team scrutinised the material quality of their samples with transmission electron microscopy. Those with a thicker $Al_{0.65}Ga_{0.35}N$ layer had cracks that led to the nucleation of new threading dislocations.

Based on the characterisation techniques employed, Wang and co-workers concluded that for today's templates, which have threading dislocation densities between 5 x 10^8 cm^{-2} and 5 x 10^9 cm^{-2}, it's critical to keep the thickness of the *n*-AlGaN layer below the threshold where tensile strain from threading dislocation inclination induces morphological degradation and compositional drift. They point out that templates with a lower threading dislocation density can increase the cracking limit, decrease compositional pulling and the rate of *n*-AlGaN decomposition, and ultimately enable an increase in the thickness of this layer, leading to better devices.

UV LEDs produced during this study are claimed to be comparable to state of the art. Emitting with a peak wavelength of 285 nm, these devices produce a peak external quantum efficiency (EQE) of 10.6 percent at a current density below 1 A cm^{-2}.

"The key limitation to UV LEDs at this point in time is light extraction," says Wang. "Our group, along with many others, is hitting a wall at around 10-20 percent EQE, because the light extraction from AlN on single-side-polished sapphire is around 20 percent at the most."

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Advancing vertical GaN diodes

Optimising doping with a foundry-compatible process produces vertical *p-i-n* diodes with avalanche behaviour

THERE ARE MANY merits of vertical GaN *p-i-n* diodes grown on native substrates, including a simple architecture, low leakage and a high breakdown voltage.

While high-volume production of these devices is hampered by the absence of a foundry process, progress on this front is being made by a collaboration between Vanderbilt University, the Naval Postgraduate School, the Naval Research Laboratory and Sandia National Laboratory. This US team is pursuing a foundry-compatible planar process that controls the electric field and prevents current crowding by managing the dose in the anode extension region. Building on previous work that reported how the dose depends on the thickness of the anode, they are now unveiling the relationship between the dose and the anode doping level.

Commenting on their findings, Mona Ebrish from Vanderbilt University remarks: "The devices with a moderate anode doping have performed the best, and our TCAD simulation shed some light on the reasoning behind our experimental finding."

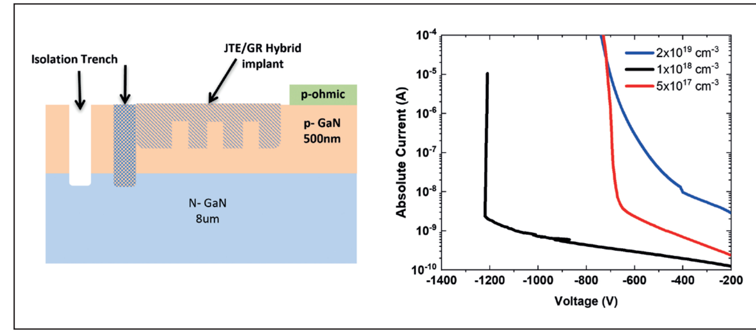
She believes that the approach they have adopted, involving a combination of experimental analysis and simulation, could be extended to other device designs.

A highlight of this study is that in one of the diodes the team recorded avalanche breakdown at different temperatures, a trait indicative of a non-destructive process.

The researchers also found that current increases as function of temperature, leading to a higher breakdown voltage. According to Ebrish, this behaviour suggests successful management of the electric field in the device, an asset not found in all *p-i-n* diodes: "Often devices either do not respond to the increase in temperature, or they experience a surge in current and burn – destructive breakdown."

The team produced their devices by loading non-homogenous GaN substrates into an MOCVD reactor and growing 500 nm-thick anode layers with magnesium doping levels of either 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3} or 2×10^{19} cm^{-3}. For all three samples, which have a 8 μm-thick lightly doped drift layer with a doping concentration of 1-2 x 10^{16} cm^{-3}, thermal annealing at 900 °C activated the anode dopants.

To form devices from the epiwafers, the team employed an edge-termination process that involved: etching a 1 μm-deep trench about 140 nm from the anode edge; applying a nitrogen implant with a box profile, using three different energies and a total depth of 650 nm; and using a nitrogen implant to define the junction termination extension and the guard rings (see figure for the architecture of the device). To completed the fabrication of the diode, the team added a Pd/Pt/Au stack for the *p*-GaN anode and a Ti/Al/Ni/Au stack for the cathode.



➤ The *p-i-n* diodes produced by the team (left) have breakdown characteristics that show a tremendous variation with doping level (right).

Electrical measurements on the three devices uncovered significant differences in breakdown voltage and leakage current, despite the identical drift layer thickness, doping level and edge termination process. The variant with anode doping of 1×10^{18} cm^{-3} exhibits a sharp breakdown at 1.2 kV, implying superior field management in the anode extension region. It is argued that the other two devices do not exhibit the same breakdown behaviour because the extension region is not fully depleted of charges, with the remaining charges to blame for premature breakdown.

The team also carried out avalanche tests, involving temperature-dependent reverse sweeps at 25 °C, 100 °C, 150 °C and 200 °C. They found that devices with doping levels of 5×10^{17} cm^{-3} and 2×10^{19} cm^{-3} struggled to avalanche, due to high leakage and an inconsistent trend with temperature, while the *p-i-n* diode with a doping of 1×10^{18} cm^{-3} avalanched, with an increasing breakdown voltage of 10 V for every 50 °C.

Ebrish says that further improvement to device performance could come from optimising the ion-implantation process.

"We are also evaluating the same process for GaN *p-i-n* diodes that are rated for higher voltages, like 3 kV or 6 kV."

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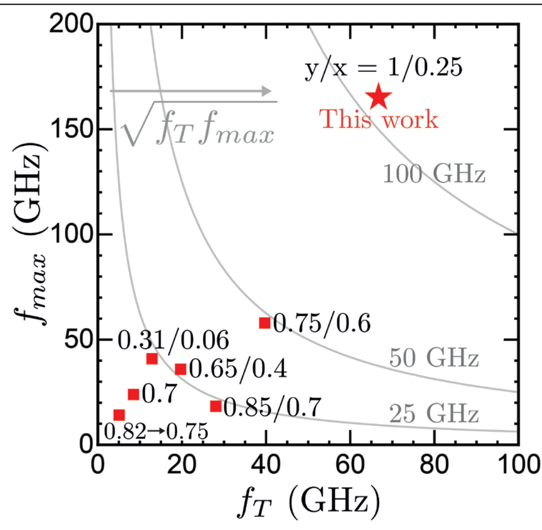
Accelerating the AlGaN HEMT

HEMTs with a $Al_{0.25}Ga_{0.75}N$ channel combine record-breaking speeds with an impressive breakdown voltage

RESEARCHERS from Cornell University are claiming to have broken the speed record for AlGaN-based transistors. The team's HEMTs, which have a T-shaped gate and an $Al_{0.25}Ga_{0.75}N$ channel, have a cut-off frequency, f_T, of 67 GHz, and a maximum oscillation frequency, f_{max}, of 166 GHz.

Another asset of these transistors is an average breakdown field exceeding 2 MV cm^{-1}. This helps to ensure a high value for Johnson's figure of merit – the product of the breakdown voltage and f_T – and highlights the potential of these device for serving in next-generation high-power RF applications.



➤ Researchers at Cornell are breaking new ground for the performance of AlGaN-channel HEMTs. The numbers beside the data points refer to the aluminium content in the top barrier and channel layer, respectively.

Replacing the GaN channel of a HEMT with an AlGaN alloy has much promise, as it has the potential to increase the breakdown voltage due to the higher bandgap, while having no impact on the saturation velocity, so should not impede the speed of the transistor. However, success is not easy – increases in aluminium content in the channel make it harder to realise ohmic contacts, and there is the possibility that the additional aluminium content leads to low-field mobilities, resulting in a higher sheet resistance and parasitic delay, hampering the speed of the device.

To overcome these difficulties, the team applied re-grown ohmic contacts that cover the sidewall of the channel, which had a carefully selected composition to maximise f_T, f_{max}, and the breakdown voltage.

The record-breaking devices produced by the team do not contain a field plate, creating a design with the potential to provide cost savings in high-voltage RF applications.

According to one of the researchers speaking on behalf of the team, Eungkyun Kim, the addition of a field plate would increase the breakdown voltage, reduce the effect of RF dispersion by spreading out the peak electric field near the drain-side gate edge, and ultimately enable a higher output power density in the X-band. "However, due to the extra parasitic capacitance induced by the field plate, power amplification at higher frequencies might become challenging."

Fabrication of the team's HEMTs began by loading a semi-insulating 6H-SiC substrate into a plasma-assisted MBE chamber and depositing a 1 µm-thick AlN layer, followed by a 24 nm-thick $Al_{0.25}Ga_{0.75}N$ channel and a 15 nm-thick AlN buffer layer. Electron-beam lithography defined a T-shaped Ni/Au gate, prior to the addition of a SiN passivation layer that ensures improved dispersion control.

Measurements on devices with a 70 nm gate length and a source-to-drain width of 600 nm revealed a contact resistance for the n^+ GaN non-alloyed ohmic contacts of 0.23 Ω mm, which is claimed to be amongst the lowest values for contact to the two-dimensional electron gas in AlGaN-channel HEMTs.

The value for the DC output conductance exceeds that of previous reports, suggesting the presence of short-channels effects, which could be suppressed by thinning the top AlN barrier.

Biasing at a gate-source voltage of -4 V and a drain-source voltage of 10 V produced a peak transconductance of 0.1 S mm^{-1}. These bias conditions were also used to obtain values for f_T and f_{max}.

For a gate-to-drain distance of 260 nm, the HEMT produced a breakdown voltage of 59 V, equating to an average breakdown field of more than 2 MV cm^{-1}.

Benchmarking their devices revealed that the average geometric mean of f_T and f_{max}, which is 105 GHz, is significantly higher than all previous reported results (see figure).

The team are now considering a switch to nitrogen-polar heterostructures to improve ohmic contacts to their AlGaN-channel HEMTs. This modification would remove the electrically insulating AlN layer on top of the channel, and open up the possibility to make an ohmic contact to AlGaN.

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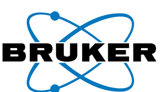

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Fax: +49 8728 911 156
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Email: requestinfo@k-space.com
www.k-space.com

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Tel: +1 949 241 9501
Email: ray@sanan-ic.com
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www.tnsc-innovation.com

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Fax: +1 925 449 4096
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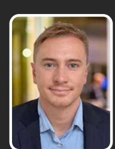

UK, Europe + Rest of the World
Jacob Caulfield
T: +44 (0)2476 719 979
E: jacob.caulfield@angelbc.com

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