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Volume 26 Issue 8 NOVEMBER / DECEMBER 2020 @compoundsemi www.compoundsemiconductor.net

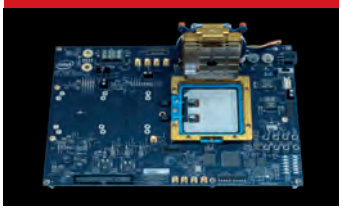
Flying high with concentrating PV

Evaluating new switching technologies

Lasers speed visible light communication

Ditching LEDs to focus on power electronics

Super-fast optical interconnects



Attolight

Scrutinising GaN HEMTs

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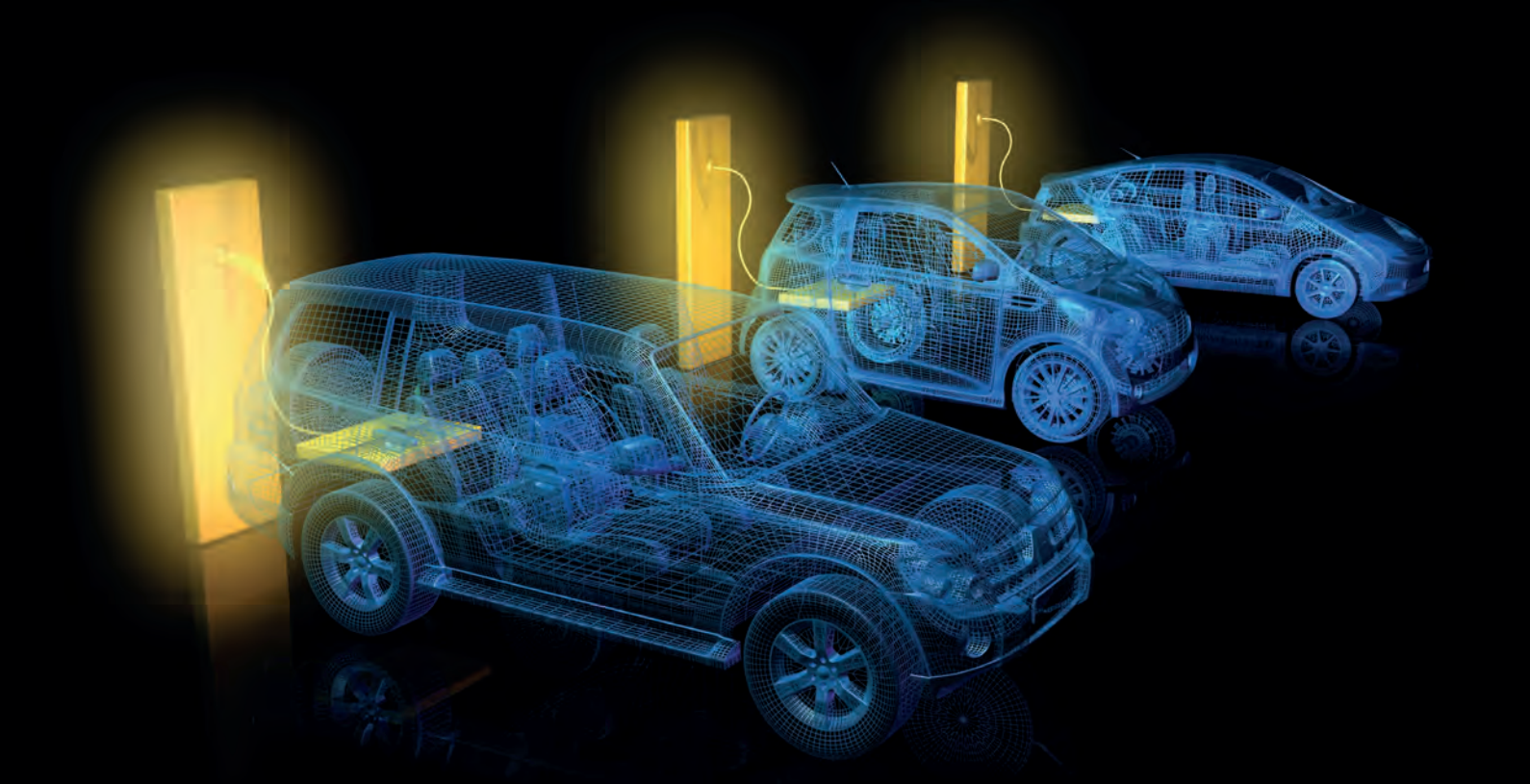

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Viewpoint

By Dr Richard Stevenson, Editor

To space and back ... and out again

IS LIFE ON EARTH deriving much benefit from all the cash poured into numerous space programmes? It's fair to say that space blankets, freeze-dried food and space-aged swimsuits are hardly important breakthroughs in the history of mankind. But there has been a significant pay-off in the form of the silicon solar cell, which is now making a significant contribution to cutting carbon dioxide emissions on this planet.

The silicon solar cell is no longer used by satellite designers. Cells accommodating III-Vs are now the established incumbent, thanks to their combination of higher efficiencies and a greater robustness to radiation.

While the higher efficiencies of III-Vs are valued on earth, their price is far too high to make an impact. Even when lenses or mirrors concentrate sunlight several hundred times to trim power generation costs – a neat solution that also boosts efficiency – commercial success has not followed. Interest in this approach did take-off a decade or so ago, but a credit crunch and tumbling silicon prices pulled the rug from under this nascent industry.

In an interesting turn of events, this concentrating technology could now have a future in space.

Miniaturisation is making this move viable. That is realised by transfer-printing thousands of tiny multi-junction cells to a backplane and adding a vast array of radiation-hardened glass

lenses, used to protect these chips while focusing the sunlight.

Trailblazing this design is US collaboration involving engineers from industry and academia. In this team's design, power is generated from a five-junction cell, created by stacking a triple-junction device based on InP and its associated alloys to a dual-junction device made from InGaP and GaAs (see *Flying High with CPV*, starting on p. 48 for details). To maximise the power, devices are strung together in different configurations to enable the current from both types of material to match. The latest results demonstrate an efficiency in excess of 35 percent, and there is a clear pathway to 38 percent, a figure that surely gives a technology developed for power generation on earth a chance of significant success in space.

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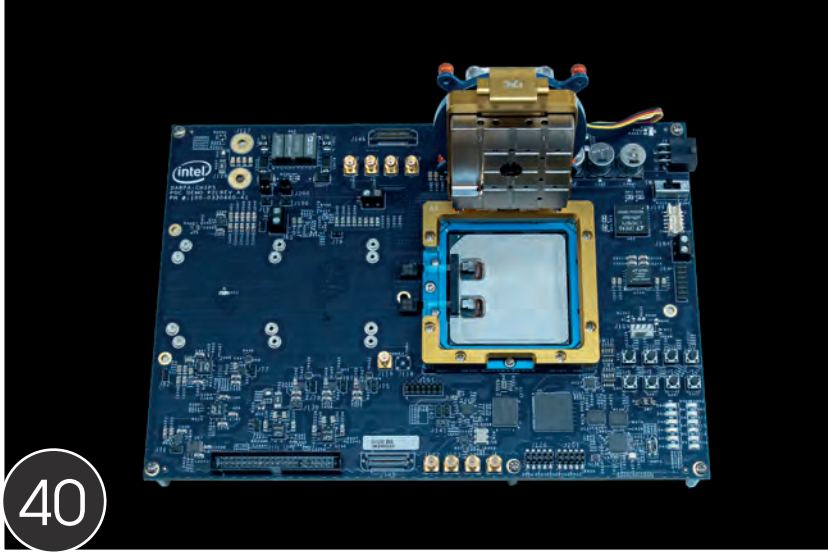


NEWS

NEWS ANALYSIS

RESEARCH REVIEW

IQE develops path for VCSEL growth on silicon

WAFER PRODUCTS firm IQE has announced the successful development of its IQGeVCSEL 150 technology for 6-inch VCSELs on germanium, a critical step in the pathway to 200 mm and 300 mm VCSEL technology.

VCSELs are a key component in telecom and 3D sensing systems. Applications include high-speed data centre infrastructure; facial recognition, proximity sensing and LiDAR time-of-flight sensors on mobile handsets; in-cabin and environmental sensing for autonomous drive vehicles; and 3D image recognition.

As demand for VCSELs grows and technical requirements become more stringent, there is the need to scale to larger wafer diameters and demonstrate a path for integration with CMOS technology.

IQGeVCSEL 150 is a key development milestone in addressing this. Germanium substrates are readily available in diameters up to 200 mm and provide a clear route for VCSEL growth on silicon

substrates (through the use of IQE's world-leading germanium-on-silicon templates) up to 300 mm.

Using this unique, patent pending technology, IQE has demonstrated device performance parity between identical VCSEL structures grown on germanium and conventional GaAs. While the conventional growth of VCSELs on 200 mm GaAs substrates is currently virtually impossible, the use of germanium removes this limitation. This is because germanium substrates allow for optimal strain management, resulting in a VCSEL wafer that is ten times flatter compared to VCSEL on GaAs.

This not only simplifies the subsequent wafer fabrication process but results in a wafer that is up to three times more uniform. The improved wafer flatness provides additional design flexibility for thicker device architectures required to access longer-wavelength VCSELs. Finally, the germanium substrates are available with zero defect density, resulting in higher quality VCSEL epi-material compared with GaAs.

Rodney Pelzel, CTO of IQE, commented: "I am delighted to announce the successful development of IQGeVCSEL 150 technology. Demonstrating device parity with GaAs but with a more uniform VCSEL wafer and improved flatness is a highly significant milestone, and we have begun sampling with partners and customers. In addition, this provides clear line-of-sight to growth on larger diameter wafers as well as VCSEL growth on silicon at 200 mm and 300 mm wafer sizes."

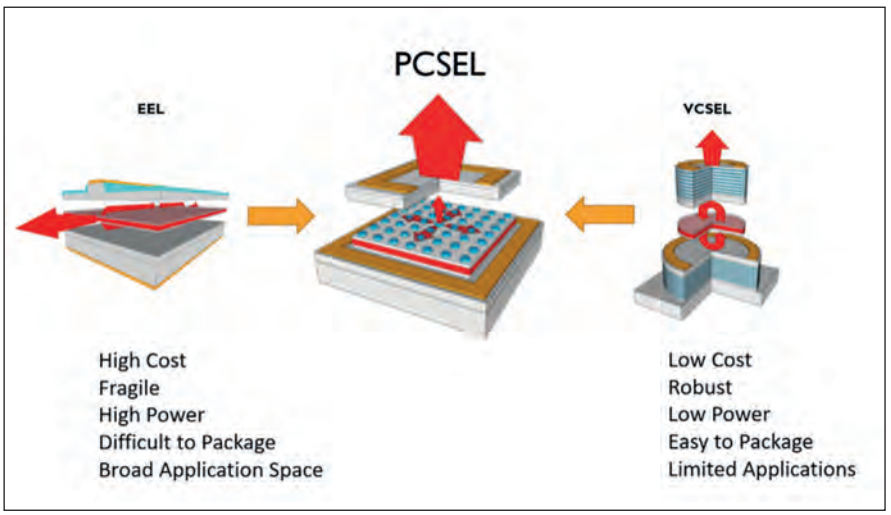
University of Glasgow spin-out to make revolutionary lasers

VECTOR PHOTONICS, a University of Glasgow spin-out, has announced it will commercialise its photonic crystal surface-emitting lasers (PCSELs), which it describes as the most significant innovation in laser design and manufacture for 30 years.

Vector Photonics CEO, Neil Martin, said: "PCSELs are low cost, robust, have a broad wavelength range and high power. This combination of key characteristics gives them a huge advantage over most of the laser technologies used today.

According to Martin, this includes VCSELs, which are robust, but compromise wavelength range and power, and EEL's (edge-emitting lasers), which have broad wavelength range, but are expensive to make and are fragile to handle.

"PCSELs emit light from their top surface, like VCSELs, making them easy to package and incorporate into PCBs



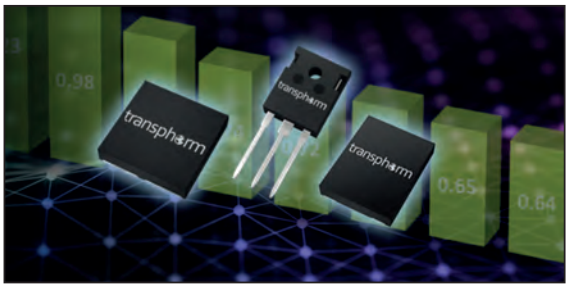
and electronic assemblies. They are also produced in a similar way to EELs, allowing us to draw on existing supply chain expertise and capacity as we grow."

The Vector Photonics' commercial team, comprising Neil Martin and Euan Livingston, has detailed knowledge of the entire photonics supply chain. The technical team includes the inventors of the all-semiconductor PCSEL technology, Richard Taylor, David Childs and Richard Hogg.

Vector Photonics' initial focus is hyperscale data centre applications, however, PCSEL technology brings critical, new functionality to LiDAR, mobile consumer, biometric and sensing markets.

Transphorm releases high-voltage GaN reliability data

TRANSPHORM, a supplier of high-reliability, high-performance GaN power conversion products, has released updated information regarding its GaN technology's quality and reliability.



Currently, Transphorm's GaN platform offers a FIT rate of less than 1 failure per billion hours in real-world applications – indicating very high reliability. The FIT calculation is based on more than 10 billion field hours of operation accumulated from an install base of approximately 250 MW.

Transphorm's devices are in use today across a wide range of applications spanning 65 W to 3 kW. Examples include universal, fast-charging adapters for smartphones and laptops; rugged, broad industrial power modules; and 1.5 to 3.0 kW Titanium class data centre power supplies, which meet the high power efficiency ecodesign requirements mandated by The European Parliament and The Council (ErP: Directive 2009/125/EC).

SiC power devices are an alternative power conversion solution and in a later stage of maturation than power GaN solutions. Although SiC offers more than a trillion hours of field operation compared to Transphorm GaN's 10 billion hours due to being commercially available longer, recent reports indicate that SiC's field failure FIT rate is 4.1. This illustrates the high field reliability achieved to date by Transphorm's GaN with a FIT of less than 1.

Extrinsic reliability, also referred to as early life failure (ELF) or infant mortality, is determined via in-house manufacturer analysis – identifying material, design, and process control defects that may cause parts to fail. Alternatively, field failure measures the number of devices that fail in customer systems in production in relation to the total number of parts sold.

When assessing FIT rate, the above two metrics – ELF and field failure – are studied. The convergence of these two rates means a semiconductor manufacturer's internal reliability assessments are accurate; a customer can have confidence in that reported level of device performance.

In January 2019, Transphorm announced a field failure FIT of 3.1. Later in 2019, the field failure FIT decreased to 2.2. And now Transphorm's field failure FIT of less than 1 aligns closer to its current ELF FIT rate of 0.61.

For customers, knowing the ELF statistics of a technology is essential to controlling warranty claims. Transphorm follows the standard industry practice as defined in JEDEC's JESD74A standard for measuring its early life failure rate. Ensuring conservative results, Transphorm tests its devices to their maximum spike rating at an appropriate use temperature of 85 °C. Despite JEDEC qualification requiring early life failure rate testing, only silicon device manufacturers commonly report it – most GaN and SiC power electronics manufacturers do not.

"To the best of our knowledge, Transphorm is currently the only high voltage GaN semiconductor company to report ELF," said Ron Barr, VP of Quality and Reliability, Transphorm. "We understand that customers require certain information when comparing wide bandgap technologies. So, we aim for transparency here. And accuracy, as we frequently see reliability data being calculated differently or manipulated in uncommon ways yet being reported as the same metric type. Given this trend, our education efforts are focused heavily on explaining the proper methods that must be used to prove business-critical metrics and why."

Mitsubishi to launch 4-terminal 1200 V SiC MOSFETs

MITSUBISHI ELECTRIC has announced the coming launch of a new series of SiC MOSFETs, the N-series of 1200 V devices in a TO-247-4 package, which achieves 30 percent less switching loss compared with the existing TO-247-3 package products.

According to the company, the new series will help to reduce the power consumption and physical size of power-supply systems requiring high-voltage conversion, such as electric vehicle on-board chargers and photovoltaic power systems. Sample shipments will start this November.

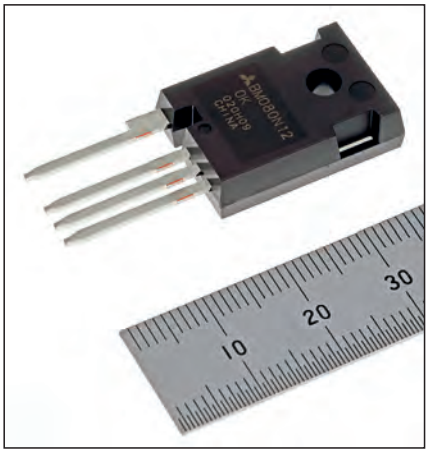
The new series devices come in a four-pin package to help reduce power consumption and physical size of power-supply systems. They feature a figure of merit (FOM3) of 1,450 mΩ-nC and high self-turn-on tolerance. The TO-247-4 package is equipped with an independent driver source terminal as well as a conventional 3-pin package.

The four-pin package is said to help reduce parasitic inductance, a problem in high-speed switching. Eliminating gate-source voltage drops due to current variations helps to reduce switching loss by approximately 30 percent compared with TO-247-3 products.

Using a higher carrier frequency to drive the new power semiconductors helps reduce switching-power loss, enabling smaller, simpler cooling systems as well as smaller reactors and other peripheral components, thereby helping to reduce the power consumption and physical size of overall power-supply systems.

There will be six models for a variety of applications including models compatible with Automotive Electronics Council's AEC-Q101 standards for use not only in industrial applications, such as photovoltaic systems, but also EV applications.

Creepage distance (shortest distance over surface between two conductive parts) between drain terminal and source terminal has been made wider than in TO-247-3 package products for more flexible application, including in outdoor installations where dust and dirt easily accumulate.



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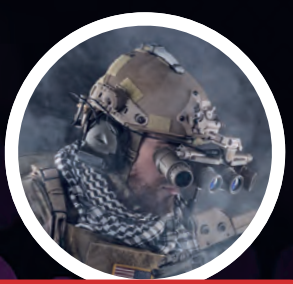

Infrared

Solar

CMOS++

Power

Qorvo to build RF semiconductor packaging centre

QORVO, a US provider of RF semiconductors, has been selected by the US government to create a state-of-the-art heterogeneous integrated packaging (SHIP) RF production and prototyping centre.

The SHIP programme will ensure that microelectronics packaging expertise and leadership is available for both US defence contractors and commercial clients that require design, validation, assembly, test and manufacturing of next-generation RF components.

The exclusive SHIP Other Transaction Agreement (OTA), worth up to $75 million, was awarded to Qorvo by the Naval Surface Warfare centre (NSWC), Crane Division. This program is funded by the Office of the undersecretary of defence for Research and Engineering's Trusted and Assured Microelectronics Program (T&AM), and is administered by the Strategic & Spectrum Missions Advanced Resilient Trusted System (S^2MARTS) Other Transaction Agreement (OTA), managed by National Security Technology Accelerator (NSTXL).

Under the SHIP programme, Qorvo will design and deliver the highest levels of heterogeneous packaging integration. This is essential to meet the size, weight, power and cost (SWAP-C) requirements for next-generation phased array radar systems, unmanned vehicles, electronic warfare platforms and satellite communications.

James Klein, president of Qorvo Infrastructure and Defence Products, said, "We are honoured to be selected to establish state-of-the-art RF packaging capability for the US Department of defence (DoD). This award reflects Qorvo's proven track record as a global leader in RF technology with over 35 years of experience. As part of this collaboration, Qorvo will expand its proven capabilities in Texas to create a SOTA facility that best serves the needs of the US government and commercial customers."

Qorvo's US-based capabilities include manufacturing, packaging and testing for both high- and low-power applications ranging from DC to 100 GHz.

Qorvo holds a defence Microelectronics Activity (DMEA) Category 1A trusted source certification for package assembly, test and wafer foundry services at its Richardson, TX location.

Infineon expands SiC supply base with GTAT

INFINEON TECHNOLOGIES AG and GT Advanced Technologies (GTAT) have signed a supply agreement for SiC boules. The contract has an initial term of five years. With this supply contract, the German semiconductor manufacturer adds a further element to secure its growing base material demand in this area.

Under the brand name CoolSiC, Infineon now already markets a large product portfolio for industrial applications and is rapidly expanding its offerings towards consumer and automotive products.

"We are seeing a steadily increasing demand for SiC-based switches, especially for industrial applications," says Peter Wawer (pictured right), president of Infineon's Industrial Power Control Division. "However, it has become clear that the automotive sector is quickly following suit. With the supply agreement we have now concluded, we ensure that we will be able to meet the rapidly growing demand of our customers with a diversified supplier base."

GTAT's high-quality boules will provide an additional source for competitive SiC. This supports Infineon's ambitious SiC growth plans, making good use of its existing in-house technologies and core competencies in thin-wafer manufacturing.

"We are very excited to enter into a long-term supply agreement with Infineon," says Greg Knight, president and CEO of GT Advanced Technologies.

"GTAT will enable Infineon to achieve a secure high-quality internal SiC wafer supply by applying their proprietary thin-wafer technology to GTAT's crystal. The growth of SiC device adoption is tied largely to the aggressive cost down of the substrate, and this agreement is a significant step towards achieving that goal."

SiC has mainly been used up to now in photovoltaic inverters, industrial power supplies, and the charging infrastructure for electric vehicles. This is where the advantages of SiC at the system level, compared to classical silicon solutions, have already come into play.

Other industrial applications such as uninterruptible power supplies and variable-speed drives are increasingly making use of the new semiconductor technology. In addition, electric vehicles show enormous potential for application options, including the main inverters for the drive train and on-board battery charging units.

IQE announces technology for RF filters

IQE, a manufacturer of advanced semiconductor wafer products, has announced the successful development of its IQepiMo template technology for RF filters and for any application requiring low-resistance buried electrodes.

Built on its cREO technology platform, IQepiMo templates are available in diameters of up to 200 mm and trials are underway with potential customers and partners.

The cREO platform provides a buffer layer to integrate GaAs, InP, GaN and other compound semiconductors with silicon, allowing the potential of producing compound semiconductor epitaxial layers on lower-cost silicon wafers up to 300 mm diameter and opening up the possibility of integrating CS performance and functionality with existing CMOS processing capabilities for true next-generation system-on-chip devices.

Low-resistance contacts are essential for the efficient operation of almost all electronic circuits. As dimensions shrink, the limitations of existing technologies are exposed, resulting in compromised device performance.

This is especially true of RF filters, which are electronic components that allow or prevent the transmission of selected signals or frequencies. As 5G technology

rolls out worldwide, the requirements for RF devices are becoming significantly more demanding.

For RF bulk acoustic wave (BAW) filters, the higher frequencies of 5G translate into an electrical penalty for thinner electrodes that must be accommodated. IQepiMo eliminates this electrical penalty by providing bulk-like metal resistance for very thin layers (down to 50 nm).

In addition, IQepiMo templates enable higher quality piezoelectric layers to be fabricated from customers' current processes, offering a clear path for improved quality AlN piezoelectric materials. As such, IQepiMo extends the capability of existing customer processes for next generation applications.

Rodney Pelzel, CTO of IQE, commented: "I am pleased to announce the successful development of IQepiMo templates based on IQE's patented cREO technology. These templates will mean that customers, while using their existing processes, can fabricate higher quality, better performing BAW filters and eliminate the electrical penalty that had until now been inherent in the application of current technology to higher frequencies."

MicroLED chip revenue to reach $2.3 billion in 2024

SINCE THE INTRODUCTION of Sony's large-sized modular microLED display in 2017, other companies, including Samsung and LG, have successively made advances in microLED development, in turn generating much buzz for the technology's potential in the large-sized display market, according to TrendForce.

Emissive microLED TVs are expected to arrive on the market between 2021 and 2022. Even so, many technological and cost-related challenges are yet to be solved, meaning microLED TVs will remain ultra-high-end luxury products at least during the technology's initial stage of commercialisation.

TrendForce indicates that microLED technology will likely first enter the market in several applications, including small-sized head-mounted AR devices, wearables such as smartwatches, high-margin products such as automotive displays, and niche products such as high-end TVs and large-sized commercial displays.

After this initial wave of products, microLED technology will subsequently see gradual integration in mid-sized tablets, notebook computers, and desktop monitors. In particular, microLED will see the highest potential for growth in the large-sized display market, mainly since these products have a relatively low technological barrier.

MicroLED chip revenue, driven primarily by TV and large-sized display integration, is expected to reach $2.3 billion in 2024.

Taiwanese and Korean manufacturers are working to overcome technological roadblocks. At the present stage, the vast majority of microLED TVs and large-sized displays features a traditional LED architecture of RGB LED chip packages paired with passive matrix (PM) drivers. Not only is PM costly to implement, but it is also limited in terms of how far the pixel pitch of the display can be decreased, making microLED technology viable for only commercial displays currently.

However, various panel manufacturers and display brands have in recent years developed their own active matrix (AM) solutions, which make use of an active pixel addressing scheme and feature TFT glass backplanes.

Furthermore, the IC design for AM, compared to PM, is relatively simpler, meaning AM requires less physical space for routing. All of these advantages make AM the more suitable solution for high-resolution microLED TVs.

Korean companies (Samsung/LG), Taiwanese companies (Innolux/AUO), and Chinese companies (Tianma/CSOT) have all currently demonstrated their respective AM display applications. With regards to the LED light source, Samsung has partnered with Taiwan-based PlayNitride to create a full-colour microLED display manufactured using semi-mass transfer of RGB LED chips.

This process differs from the traditional method of LED display manufacturing, which utilises RGB LED chip packaging technology instead. Conversely, Taiwan-based panel manufacturers AUO and Innolux have pioneered a colour rendering technology that combines blue-light LED chips with quantum dots or LED phosphors.

On the other hand, the cost of microLED displays depends on the display resolution and chip size. As users demand higher resolution displays going forward, microLED chip consumption will also skyrocket. TVs and LED displays in particular will far dwarf other applications in microLED chip consumption. For instance, a 75-inch 4K display requires at least 24 million RGB microLED chips for its subpixel array.

Therefore, the manufacturing cost, which includes technologies such as semi-mass transfer, and material cost of microLED chips will remain sky-high for the time being.

In light of this, TrendForce believes that technological and cost-related issues will remain the greatest challenge to the market availability of microLED TVs and large-sized microLED displays.

As TVs trend toward large sizes and high resolutions in the future, manufacturers must confront increasing difficulties in microLED technologies, including mass transfer, backplanes, drivers, chips, and inspection and repair.

Once these technological bottlenecks have been overcome, whether the cost of microLED manufacturing will undergo a corresponding, rapid drop will then determine microLED's viability as a mainstream display technology.

AngelTech Virtual 2 proves a hit

OVER 1700 DELEGATES took the opportunity to watch, listen and learn as a host of industry luminaries provided some great insight into the latest developments in the compound semiconductor and specialised photonic integrated circuit technology sectors. Angel Business Communications CEO and Event Organiser, Sukhi Bhadal, was delighted with the second AngelTech event, as it brought together the research, vendor and end-user communities for some valuable education and networking opportunities.

"Following on from the continued disruption the Covid-19 pandemic has caused to the events industry, we were disappointed when we had to twice postpone physical Brussels event in March and then again in November. We have been delighted with the continued support the compound semiconductor and photonic integrated circuits community has given us. The second AngelTech event was a fantastic success with over 1700 delegates registered, 25 sponsors signed up and some inspirational speakers. The event, held on our own virtual event platform 'Connect', allowed us to keep the community connected, learning and developing business."

There is a significant overlap between the PIC and the compound semiconductor industry. Some photonic circuits are formed from InP, while others, such as those made from silicon or polymers, depend on III-Vs for the light source. Due to this close working relationship, the CS and PIC summits kicked off with a shared session that included some of the ways that III-Vs play a role in photonic circuits.

One talk by Geza Kurczwell from Hewlett Packard Enterprise focused on this theme, outlining how quantum dots could aid internal communication in supercomputers, while presentations from analysts at Yole Développement and Strategy Analytics detailed the promising outlook for the PIC industry, which has opportunities in many sectors.

This year the compound semiconductor industry has grabbed the headlines in the mainstream press for the role UV LEDs can play in combatting the Covid-19 epidemic. Detailing this opportunity, along with several others, Jennifer Pagan from Aquisense Technologies described how UV LEDs can assist healthcare. While the performance of this device lags behind its light-emitting cousin, Haiding Sun from the University of Science and Technology China, outlined several novel architectures that could help it to catch up.

Advances in visible LEDs continue. The green gap thwarts this sector, but it could be overcome by switching to the cubic form of GaN, argued David Wallis from Kubos Semiconductors. Despite difficulties in making green LEDs, the performance of all forms of visible LED continues to increase, and they are now capable of providing the light source in colour projectors for homes and offices, according to Benjamin Schulz from Osram Opto Semiconductors. Another lucrative opportunity for the LED lies in displays, where arrays of tiny chips provide direct emission. Transferring vast numbers of miniature LED Chips onto a backplane is time-consuming, even with massive parallel-transfer techniques, but microfluidics offers a promising alternative, revealed Paul Schuele from eLux Display.

As well as advancing devices made from established material systems, the AngelTech Online Summit considered the potential of new materials. One is AlScN, offering an opportunity for enhancing the channel in GaN-based HEMTs, claimed Stefano Leone from Fraunhofer IAF; and another is gallium oxide, capable or record-breaking field strengths, explained Andrew Green from the US Air Force Research Laboratory.

- The AngelTech Virtual 2 platform remains live on-demand for the next three months, where you can network with the community, reach out to the exhibitors and watch all presentations.

  You can register for access to the portal or sign in by going to: https://virtual.angel.events/932-858-004/auth

‘Topping off’ ceremony at Cree/Wolfspeed’s SiC fab

GOVERNOR ANDREW CUOMO has announced the ‘topping off’ of Cree/Wolfspeed’s brand new, state-of-the-art, automotive-qualified and 200 mm-capable power and radio frequency SiC wafer fabrication facility at the Marcy Nanocenter, which is located on the SUNY Polytechnic Institute campus near Utica.

Empire State Development’s acting Commissioner, president and CEO Eric Gertler, alongside executive members from Cree/Wolfspeed, Oneida County and Empire State Development, joined distinguished guests in commemorating the placement of the final steel beam atop the new fab. This symbolises a major construction milestone for the project, which remains on schedule for production to begin in 2022.

“This milestone is proof of our commitment to the Mohawk Valley and is another step towards strengthening the research and scientific assets that New York needs to attract high-tech industries and build back better,” Governor Cuomo said. “Cree/Wolfspeed has already proven to be a great partner, and we are proud to have them establish roots in the region as we continue to support and grow the advanced manufacturing infrastructure of New York State.”

“The Mohawk Valley is leading the way in technology and innovation with new investments and opportunities,” Lieutenant Governor Kathy Hochul said. “The progress at the SiC wafer fab at the Marcy Nanocenter will further advance wafer fabrication and production in the state. This significant investment will create hundreds of new jobs and provide internship and research opportunities for students in the area. The construction project is a testament to our efforts to build back better and strengthen the economy in the Mohawk Valley and across the state.”

Cree CEO Gregg Lowe said, “All involved in this project should be proud of where we are today – from Cree/Wolfspeed employees, to our vendors, New York State, generous community partners and the residents who have welcomed us into this amazing community. SiC is at the forefront of green technologies – including electric vehicles, renewable energy and energy storage – that will greatly reduce greenhouse gases. The technology that will be created at this fab – right here in your backyard – will power our customers to build a brighter future that is sustainable for all.”

SUNY chancellor Jim Malatras said, “Today’s ceremony is a symbolization of the foundation and partnership we are continuing to cultivate with Cree, who has been working closely with SUNY Polytechnic Institute to help our students excel in STEM leadership positions through hands-on learning internships. We are proud to collaborate with what will be the world’s largest SiC fabrication facility in Marcy by way of the Wolfspeed project, and know that upon its completion the Mohawk Valley will reap the benefits of this workforce development initiative and added jobs.”

Cree/Wolfspeed has taken many steps forward since announcing it would build its newest facility in New York State. Currently, the company has 40 full-time employees in New York and had 24 interns this past summer from local universities throughout the state.

Cree also has multiple job openings listed for the fab, which include engineering and technician-related positions. Additionally, Cree announced in July that it will establish the “Cree/Wolfspeed Scholarship” program and endowed chairs as part of its ongoing, long-term commitment to the Mohawk Valley to help expand the local economy and develop a pipeline of high-tech professionals.

The programme is designed to educate the next-generation, high-tech workforce by increasing student opportunities in STEM education and graduation rates, as well as by providing access to funds to assist students in advancing their education.

Cree/Wolfspeed has committed to investing at least $1 billion through the construction of the fab, creating over 600 new jobs within eight years and will provide internships and research opportunities for State University of New York students.

SUNY has also committed to match up to $5 million in semiconductor-related research funding from Cree/Wolfspeed for the SUNY system.

New York State is providing $500 million in performance-based, capital grants from Empire State Development to reimburse a portion of Cree/Wolfspeed’s costs of construction and fitting out the new facility and acquiring and installing machinery and equipment, as well as $1 million in Excelsior Jobs tax credits.

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Rivian SUV: the EV startup has won $6 billion to launch its all-electric pickup and SUV.

Cree: Stepping out of the light

As Cree exits the LED industry, its chief executive Gregg Lowe tells *Compound Semiconductor* what will come next

BY REBECCA POOL

WHEN CREE announced plans to sell its LED business to Smart Global Holdings in October for up to $300 million, stock prices leapt by 7 percent. The move followed divestment of Cree's lighting arm in 2019, and comes as China-based manufacturers continue to capture market share from the likes of Lumileds, Osram and Nichia, largely thanks to cheaper production.

With an emphasis on his company now being a 'pure-play semiconductor company', Cree chief executive, Gregg Lowe, is committed to driving revenues in SiC and GaN markets, with electric vehicles currently being the sweet spot. Indeed, according to Lowe, recent meetings with Germany-based car manufacturers indicated that Covid-19 has accelerated electric vehicle adoption.

"With everything around the world shutting down, the skies cleared and these manufacturers have seen a big pull here from consumers," he says. "Europe has a multi-trillion dollar Covid-19 relief fund – 30 percent of this targets green energy initiatives that include electric vehicles and charging stations."

"Also, the EU parliament recently voted to increase its goal of cutting emissions by 40 percent to 60 percent by 2030," he adds. "As horrible as this crisis is, there is this silver lining that's very exciting for compound semiconductors and silicon carbide."

Rising demand

The latest development from Cree is not a surprise. Since the end of 2019, the company has been stacking up power semiconductor contracts with the likes of ABB Power Grids and joining forces with automotive players including Germany-based car parts manufacturer, ZF, and The Volkswagen Group.

Earlier this year Cree also revealed a partnership with Zhengzho Yutong, a Chinese manufacturer of commercial vehicles. Here, Cree's 1200 V SiC devices

will be integrated to Yutong's power modules and used in the powertrain systems of electric buses. And working with long-time distributor, Arrow Electronics, Cree introduced 650 V SiC MOSFETs for electric-vehicle onboard chargers, switched-mode power supplies in industrial applications and more.

"The results that we've got on this platform have just been astounding," says Lowe. "Arrow identified $750 million worth of opportunities across tonnes of different end-products including electric motorcycles, plasma generators and electrosurgical instruments. And when you think about this, we actually launched this platform in April – probably the worst part of the pandemic," he highlights.

Along the way, the company also secured $700 million in design-ins for its power semiconductor arm, Wolfspeed, in quarter one this year, up from $600 million from the fourth quarter of fiscal 2020. Factor in recent financial results which indicate that for the twelve months ending in June 2020, Cree's LED products raised $433 million in sales while Wolfspeed brought in $471 million, and the move makes clear sense.

As Lowe emphasises: "The LED market has certainly got tougher and this really allows us to focus on our [Wolfspeed] business – investors have been pretty happy with this, we received a fair price and we're ready to move forward."

So what next? LED activities will continue at Cree's key fabrication plant in Durham, North Carolina, as Smart Global Holdings rents production space for, as Lowe puts it, 'the time being'. In his words: "Smart's CEO came from Lumileds, he really understands the business so this is a good opportunity for them."

At the same time, Cree has been outsourcing its LED wafer production and processing at Durham, to make more room for SiC capacity. The company intends to continue raising SiC production in Durham, as construction of its New York, Mohawk Valley wafer fab continues.

"We're already working on our pilot line here and we're also hoping to make this facility weather-tight by early 2021," says Lowe. "We'll start installing the first set of tools in the summer of 2021 and then we can also transfer the pilot line to the factory."

Cree intends to increase capacity and SiC crystal growth from a 2017 baseline by 30 percent to 2024. Investments in 200 mm wafer production continue with Lowe anticipating an industry shift to the larger wafer size in 2024. And for the Cree chief executive, the worst of the SiC capacity constraints may be over.

"Capacity is tight but I think the adoption of electric vehicles is accelerating the way that people are thinking about this," he says. "We're going to need to expand beyond our 30 times increase, and we have the capital and ability to modulate our capacity based on what the demand is going to be."

Indeed, it isn't just Europe that appears to have an appetite for more electric vehicles. Over in the US Tesla's cars are shifting faster than most would have imagined; the company surpassed the 1 million production mark this year. EV start-up Rivian has raised some $6 billion, from the likes of Ford and Amazon, ahead of the much awaited launch of its all-electric pickup and SUV. Also, in September this year, Lucid Motors unveiled an all-electric saloon vehicle with a 517 mile range – Tesla's Model S reaches 402 miles.

"At the same time, I see China leap-frogging the internal combustion engine as it's going to be really tough for them to catch up with the West [in this industry] now," points out Lowe. And given that over the last three quarters, more than half of the company's new design-ins came from automotive partners, electric cars look set to be the market to watch for the time being. As Lowe says: "I tell, this is a great time to be a silicon carbide company."

But where does this leave GaN? Following US-China tensions, and the Huawei equipment ban from many nations, including the US, RF GaN activities relating to the roll-out of 5G have dwindled for Cree and competitors in this space.

Lowe says that the present situation makes it 'impossible' for Cree to sell to Huawei, which is one of the world's largest makers of 5G phones and networking equipment. Meanwhile, he reckons the current pandemic has also slowed 5G roll-out across Europe and the US. Still, he is adamant GaN remains important to Cree. "We see opportunities for GaN in aerospace, and 5G is still a pretty good opportunity for us," he says "There's a handful of non-Huawei RF manufacturers out there – we're engaged with all of them and we're winning."

Gregg Lowe with Michael Baecker, Head of Volkswagen Purchasing Connectivity, when Cree was chosen as silicon carbide partner for Volkswagen's FAST programme.

Scrutinising GaN HEMTs

by quantitative cathodoluminescence

Quantitative cathodoluminescence aids development and production of GaN HEMTs by delivering non-destructive measurements for threading dislocations, composition, and doping

BY MATTHEW DAVIES AND CHRISTIAN MONACHON FROM ATTOLIGHT

COMPOUND SEMICONDUCTORS share many of silicon's characteristics. However, there are some notable differences, causing some characterisation techniques for silicon to fail to provide accurate information for compound semiconductors. This state of affairs is most evident with GaN. To ensure competitive pricing, GaN transistors and LEDs are grown on foreign substrates, giving rise to a very high defect density in the epilayers, a situation never found in silicon devices.

Helping to characterise various compound semiconductor devices, including those made from GaN, is a non-destructive technique known as quantitative cathodoluminescence spectroscopy. This is being trailblazed by our team at Attolight of Lausanne, Switzerland, which has launched tools that support this form of metrology.

Previously, our team reported how quantitative cathodoluminescence spectroscopy can assist manufacturers of solar cells, lighting, and display technologies (see, for example, Cathodoluminescence for high-volume manufacturing, from the July 2018 edition of *Compound Semiconductor*). Here we consider how this technique can monitor the quality of the heterostructure of another device, the GaN-on-silicon HEMT (if you are not familiar with this device, take a look at the box "The basics of the GaN HEMT").

For this class of transistor, quantitative cathodoluminescence spectroscopy allows engineers to optimise end-of-line yield by focusing on three key metrics: the threading dislocation density; the aluminium content of the AlGaN layer above the channel; and the magnesium doping content of the *p*-type GaN gate, key to the realisation of a normally-off HEMT.

To ensure optimal process chain management, engineers need to draw on rapid non-destructive feedback from metrology tools at every step of the process chain. This holds true for pilot lines, and for those found in dedicated research and development facilities and high-volume fabs. For those working in research and development, faster feedback accelerates development, while improving its efficiency and trimming costs. In the high-volume fab, faster non-destructive feedback reduces work-in-progress and aids rapid process steering – in an ideal case, the effective work-in-progress is zero for a given process step. This is possible when feedback from a metrology tool is available within the downtime of a process tool between subsequent processes, a situation that occurs, for example, when cleaning an epi-reactor.

Our Säntis platform – for use after the growth of the epiwafers – offers rapid, reliable, non-destructive feedback of various metrics previously only accessible via destructive, time-consuming methods. Armed with this new, high-resolution eye on the epiwafers, fab managers and their engineers are well-positioned to make critical processing decisions. This includes deciding whether certain wafers should proceed to front-end processing, and whether there is a need to tweak the growth recipe, based on immediate feedback on key performance indicators.

In the remainder of this article we describe studies of GaN HEMTs using our Säntis 300 full-wafer quantitative cathodoluminescence platform. These investigations, which include proprietary measurement and analysis methods specifically developed for power HEMTs, represent the current state of development of our technologies for epi process control in GaN manufacturing.

Determining dislocations…

Dragging down the performance of GaN HEMTs are threading dislocations. If they intersect the channel formed by the two-dimensional electron gas, or connect the substrate to the gate contact, they can cause device leakage currents [2] and potentially impair long-term device robustness. Developers of GaN HEMTs have devised several solutions for cutting the leakage current through these channels. However, those working in this field are still to grasp a full understanding of this issue – they don't have a complete picture for what allows current leakage via these dislocations, or how to effectively control leakage, and they don't know the impact of dislocations on device performance and robustness. Consequently, there is a need to analyse threading dislocations in the epilayers, as this will shed more light on this issue and help to control the process, leading to better devices.

As cathodoluminescence has been around for decades, it is often assumed that counting threading dislocations by this technique is trivial. But it's not: it is far more complex than it would first appear to ensure reliable determination of the threading dislocation density to a standard that meets the expectations of process control metrology.

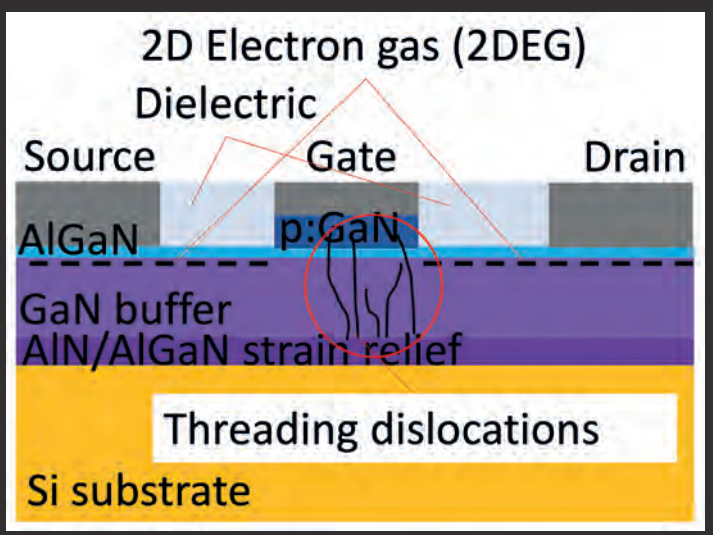
However, quantitative cathodoluminescence is incredibly insightful, combining simple counting of threading dislocations and determining their density with many new metrics. They include the local spatial distribution of threading dislocations; their geometric order and size; and the ability to discriminate between this imperfection and other structural defects, such as V-shaped pits. Thanks to this broad range of capabilities, quantitative cathodoluminescence spectroscopy is a very powerful tool for supporting the development and production of the GaN HEMT.

The basics of the GaN HEMT

At the heart of the junction-gated, normally off HEMT [1] is a two-dimensional electron gas (2DEG), formed at the interface between the large band gap $Al_xGa_{1-x}N$ (with *x* typically 10-20 percent) and regular GaN. To ensure normally-off operation, a *p*-type doped GaN layer is inserted between AlGaN and the gate contact.

For devices with this design, performance is impacted significantly by the:

- Dislocation density. Dislocations are ultimately linked to leakage current [2]
- Magnesium concentration in *p*-type GaN. This affects the Fermi level of GaN underneath the gate, and ultimately the blocking power of the device
- Aluminium concentration in AlGaN. This affects directly the 2DEG concentration [3]



This is the general design of the junction-gated, normally-off HEMT, typically used for power-conversion applications. Threading dislocations are present in the entire sample. This sketch just indicates their presence and direction, especially under the gate, where they have potentially the largest impact.

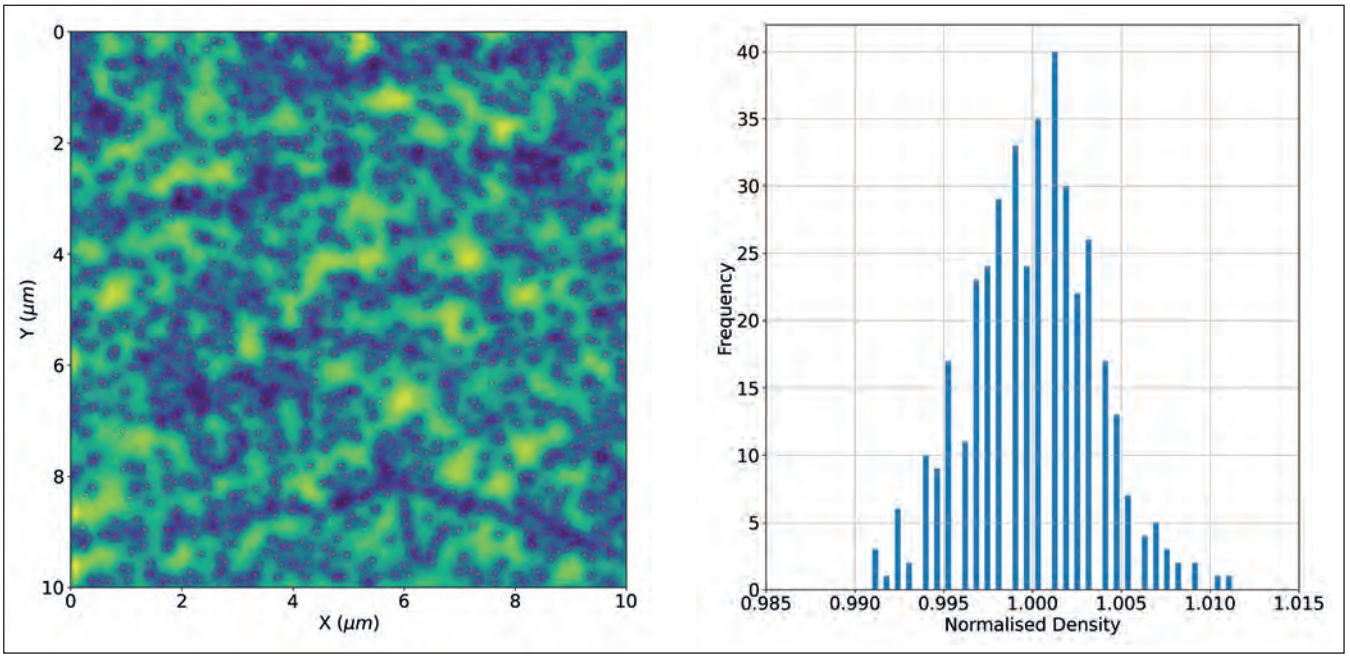


Figure 1. (a). A cathodoluminescence image with threading dislocations identified by the highlighted Attolight image reconstruction solution. (b) Histogram of normalised threading dislocation densities, recorded over several hundred iterations of the image reconstruction algorithm.

One technique with the potential to help quantitative cathodoluminescence is machine vision, which has improved in recent years, leading to widespread implementation in many industries. However, there are pitfalls when applying machine vision to small, densely packed features, such as the clusters of threading dislocations found in the epilayers of GaN-on-silicon HEMTs. In these heterostructures, where on average there are around ten threading dislocations per square micron, traditional feature-detection algorithms can suffer from a drop in accuracy.

We have addressed this weakness with an innovative image reconstruction method that draws on the results of Monte-Carlo and numerical simulations, and material-specific knowledge and assumptions. After investigating hundreds of iterations across different images, we determined a reconstruction reproducibility, evaluated in terms of 3 sigma, of ±1.05 percent (see Figure 1). In addition, our technology resolves up to 40 percent more defects than a benchmark feature-detection solution.

If threading dislocation imaging by quantitative cathodoluminescence is to be employed into process control its capabilities must be more than just accurate counting of these defects in a single image. It may appear that to maximise precision of detection, engineers should record fewer higher-resolution images, each with fewer features. But this can fail to

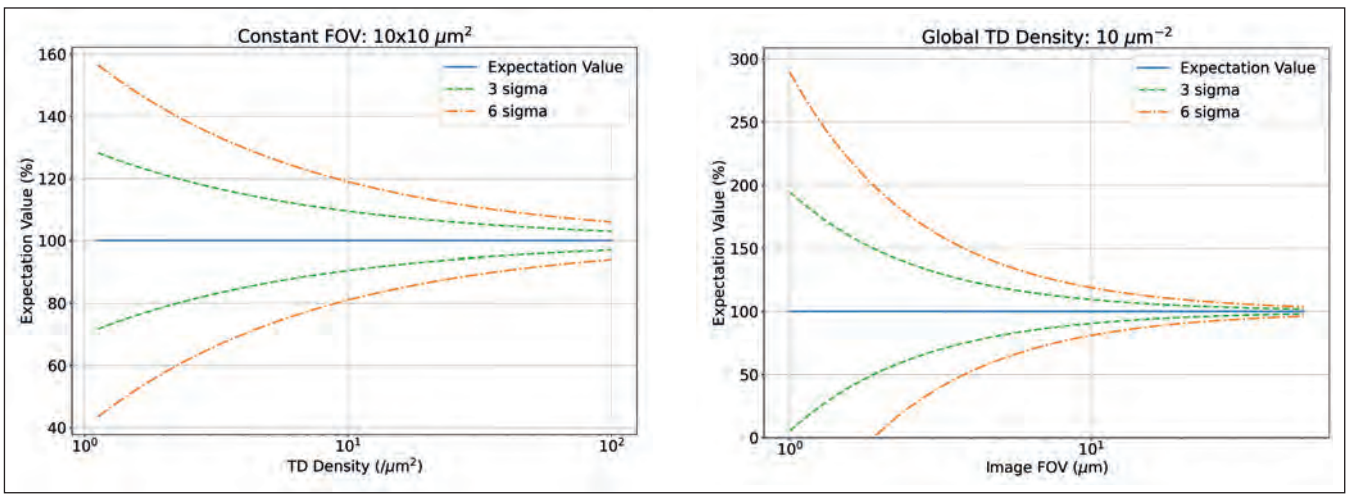


Figure 2. (a) Representative uncertainty (expressed as a percentage of the expectation value) for varying threading dislocation densities when considering a constant image area (FOV) in a single 10 x 10 μm² image. (b) Representative uncertainty (expressed as percentage of the expectation value) for a constant threading dislocation density of 1 x 10^9 cm^{-2}, evaluated for a single image with a varying FOV.

consider both the accuracy and the management of sampling error. This is critical to allowing quantitative cathodoluminescence to play an important role in process control.

As illustrated in Figure 2, when smaller images are used to determine the threading dislocation density, there are fewer features present – and the image is more susceptible to random statistical fluctuation. While an individual image can provide a more precise detection of threading dislocations, in certain circumstances the sampling error overrides this gain, resulting in an inferior accuracy for the result.

Consider, for example, a single image with a small field of view. This can result in an extremely large range of possible values due to random statistical fluctuation, an effect exacerbated by lower threading dislocation densities. In an extreme case, when imaging a sample with a defect density of 1×10^9 cm^{-2} – this equates to an average of ten defects for every square micron – there is a small but non-zero probability of finding no defects in a single 2×2 μm^2 field of view (this is illustrated in Figure 1 (b)).

The solution is to combine a high sampling rate with an optimised field-of-view. Note, however, that it is not possible to process images with an infinitely large field-of-view with high precision, despite the apparent benefits that this would have on minimising sampling error. To realise sampling rates that ensure sufficient repeatability and reproducibility of process control metrology tools, there needs to be excellent, reliable automation, and repeatability of the detection algorithm. We offer this by combining: the automation of the Säntis 300 platform, with due consideration of sampling error and repeatability; with an innovative approach, employing a proprietary image reconstruction method to detect features.

...and epilayer compositions

Situated at the heart of every HEMT, whether it is normally-on or normally-off, is a layer of AlGaN that is integral to the formation of the two-dimensional electron gas channel. By carefully controlling the AlGaN growth, engineers can set the electron gas concentration and ultimately determine key characteristics, such as the threshold voltage and the on-state series resistance.

The growth of the heterostructure for the GaN HEMT is never perfect. Due to epitaxial reactor design, substrate bow, and the kinetics of the growth process, there are radial wafer-level dependences associated with epilayer composition and thickness (see Figure 3). The variations they produce on critical layers – in the case of HEMTs, the AlGaN layer; and in LEDs, the active region – drive down wafer-level homogeneity and device yield. While metrology and monitoring of critical epilayers can't eradicate this, they do play a crucial role in maximising homogeneity and manufacturing yield.

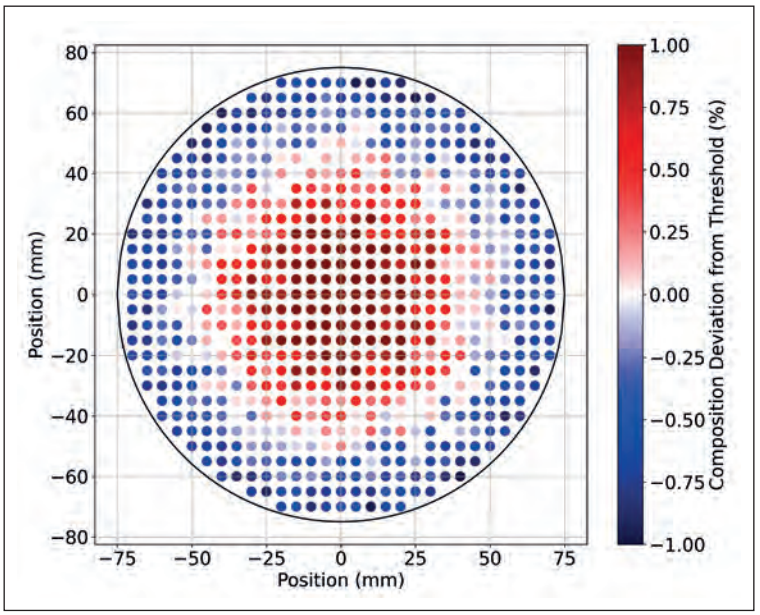


Figure 3. The Säntis 300 platform is capable of producing a wafer map of the aluminium composition of a buried AlGaN layer in a GaN HEMT structure (simulated data).

A very widely adopted, quick approach for determining the composition of epilayers involves measuring the peak of the photoluminescence. However, this is not applicable to all epitaxial structures, including buried AlGaN layers surrounded by GaN cladding. When AlGaN is buried, its energetic state relative to that of the neighbouring GaN layers results in an extremely low emission rate under optical excitation. Compounding matters, the excitation process for the AlGaN layer is inefficient, especially as the layers above it absorb most, if not all, of the incident laser light. Due to these two factors, it is impossible to measure the photoluminescence from a buried AlGaN layer.

Options for overcoming this problem are to either interrupt the growth after deposition of AlGaN, or to expose AlGaN by etching the material above it. Neither are ideal, being destructive processes. Regardless of whether the wafer is etched, or the growth interrupted, material used for photoluminescence measurements cannot be processed into devices. Another limitation is that this approach involves an indirect feedback loop, because measurements are performed on sister wafers.

Our approach offers a superior alternative, adjusting the electron-beam penetration depth to more efficiently and precisely excite the buried AlGaN layer. We have proven the accuracy and reproducibility of our technique by using a nested Gage study to compare equivalent wafers with and without a top *p*-type GaN layer (see Figure 4). This study shows a strong measurement reproducibility, with standard deviations below ± 0.25 percent [of normalised value], based on over 100 repeat measurements.

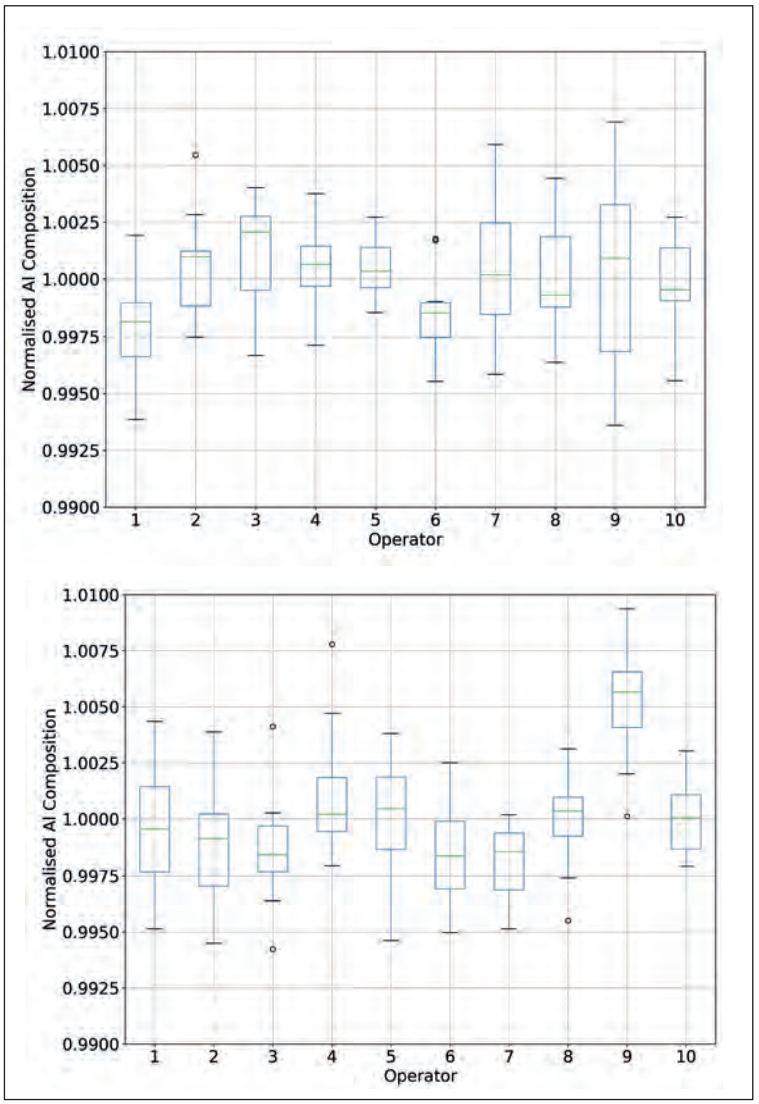


Figure 4. Representative results of a nested Gage reproducibility and reliability study on the determination of aluminium composition in the AlGaN layer of: (a) a full normally-off GaN HEMT structure (buried layer); and (b), the equivalent HEMT structure with the *p*-type GaN cap removed (surface layer).

When assuming a 14 percent specification limit (target ±7 percent), we record a Gage variance below 10 percent for each sample.

Doping control

In normally-off GaN HEMTs magnesium doping influences various device characteristics, including robustness, off-state leakage and threshold voltage. The pioneers of GaN devoted much effort to developing a process for realising magnesium doping, with success in the 1990s allowing GaN to overtake ZnSe and become the best material for making blue and green LEDs and lasers. In the decades that have followed, those working on GaN have made a great deal of progress in understanding magnesium doping, with the self-compensation mechanism investigated and discussed in the research community [5].

Yet despite these advances, magnesium doping in the GaN HEMT still presents complications. Issues include enhanced leakage paths, stemming from an interplay between magnesium acceptors and threading dislocations [6].

The traditional technique for measuring magnesium-doping in GaN is Secondary Ion Mass Spectrometry (SIMS). Used alongside Hall effect measurements, it allows engineers to uncover the ratio of incorporated magnesium to electrically active magnesium. Unfortunately, SIMS and Hall effect measurements are both destructive, with the former sometimes even requiring the shipment of a sample to a specialist lab.

However, long waiting times for both on- and off-site SIMS measurements no longer need to hamper progress, thanks to our proprietary technique for determining the magnesium concentration by quantitative cathodoluminescence. Our approach, based on detailed spectroscopic analyses, draws on a deep understanding of electron-matter interactions and the cathodoluminescence technique, as well as material-specific expertise.

To prove the capability of quantitative cathodoluminescence spectroscopy for determining magnesium doping, we have compared the results it produces to those provided by SIMS. Measurements on multiple samples yields a root-mean-square error of 3.8 percent for the derived relationship between magnesium concentrations determined by SIMS and by quantitative cathodoluminescence. To determine the repeatability of our technique, we have carried out a nested Gage reproducibility and reliability study (see Figure 5). This investigation uncovered good reproducibility, with a standard deviation below ± 1 percent over 100 repeat measurements, when assuming a 60 percent specification limit (target ± 30 percent) and a Gage variance below 10 percent.

Three virtues

One of the great virtues of our approach is that it is non-destructive. This prevents wafers from being periodically sacrificed to determine a property – a particularly welcome asset for determining the magnesium content in GaN HEMTs, as all alternative techniques are destructive. The two other prominent virtues are that this technique is comparatively fast, enabling acquisition from dozens of sites per wafer, and therefore giving a sense of the homogeneity of the properties; and the approach has versatility, providing measurements of threading dislocation density, AlGaN composition and magnesium-doping levels. Although it takes time to move between samples, due to the need to exchange wafers under vacuum, fabs that invest in this tool save space and reduce complexity of their feedback cycle (all these benefits are highlighted in Table 1, which also outlines the pros and cons of other techniques).

Thanks to the virtues of the Säntis 300 platform, it is ideal for process control, providing non-destructive feedback

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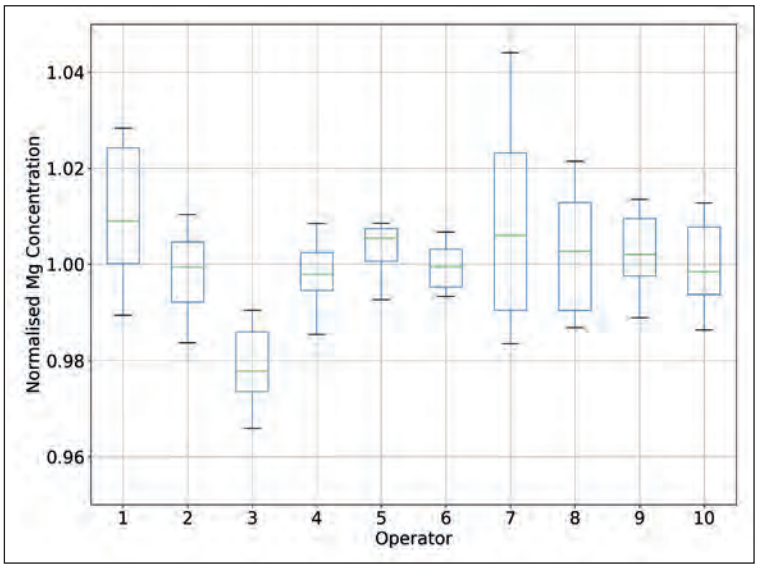

Figure 5. Representative results of a nested Gage reproducibility and reliability study on the determination of the magnesium concentration in the *p*-type GaN layer of a full normally-off GaN HEMT structure.

Use case	Competing techniques	qCL competitive advantage
Threading dislocation density	XRD	- Fast (<1 min/site vs >10 min/site) - Tailored depth sensitivity[7]
	2 photon absorption	- Fast (<1 min/site vs >10 min/site) - Tailored depth sensitivity[4]
	TEM/AFM	- Fast (<1 min/site vs >60 min/site) - Non-destructive - Statistics (see Figure 3.)
Al content in $Al_xGa_{1-x}N$	XRD	- Fast (<1 min/site vs >10 min/site)
	SIMS	- Fast (<1 min/site vs >10 min/site) - Non-destructive
	PL	- Better excitation efficiency, stronger signal, more reliable results
Mg content in p:GaN	SIMS	- Fast (10 min/site vs >60 min/site) - Non-destructive - Measures activated part of dopants
	Hall effect	- Non-destructive - Fast (10 min/site vs >60 min/site)

Table 1. Alternative techniques for analysing GaN HEMT epiwafers highlight the advantage of the Attolight solution.

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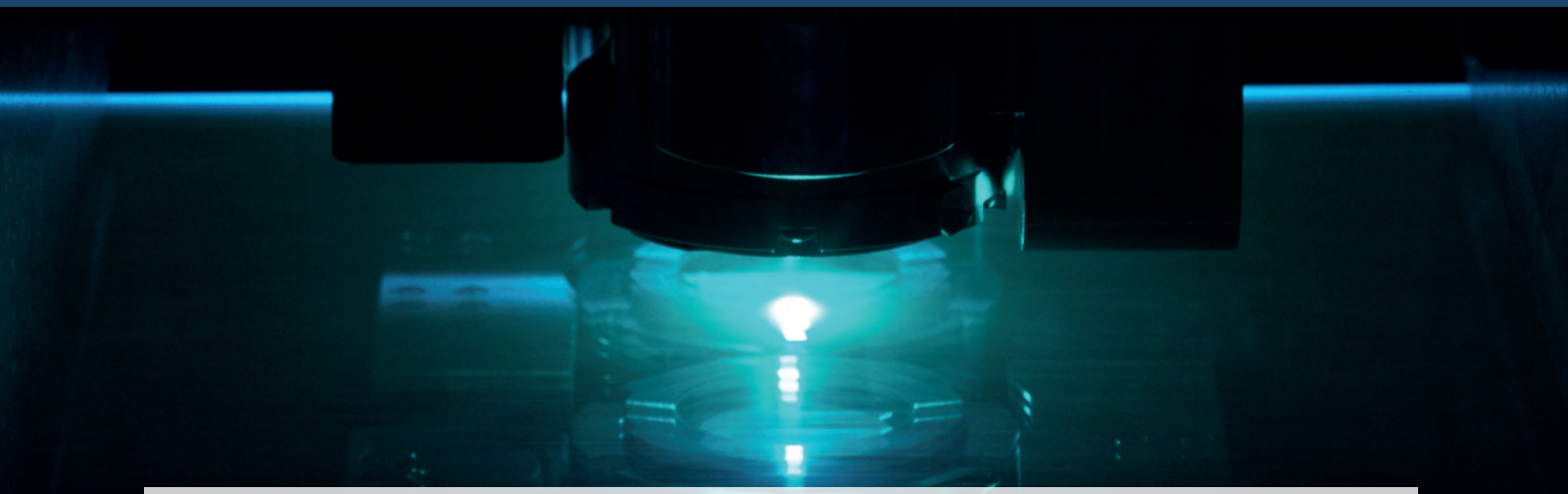

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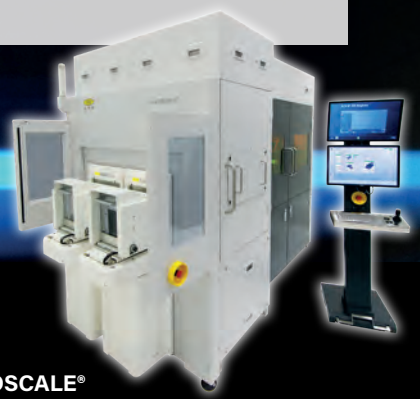

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Enhancing silicon photonics with III-Vs and barium titanate

Heterogeneous co-integration of barium titanate and III-V semiconductors on a silicon photonics platform enables efficient optical transceivers and novel neuromorphic devices

BY PASCAL STARK AND BERT JAN OFFREIN FROM IBM RESEARCH EUROPE AND STEFAN ABEL FROM LUMIPHASE AG

RECENTLY GLOBAL DATA TRAFFIC has been increasing at a compound annual growth rate of more than 25 percent. Due to this exponential rise, worldwide data traffic is tipped to reach 400 Exabytes per month in 2022. To cope with this hike in growth, which shows no sign of slowing, there needs to be a rapid scale-up in data transmission capacity and speed.

The lion's share of the traffic occurs within datacentres, where data is routed through optical fibres over distances from a few metres to a few kilometres. Inserted at the interfaces between optical fibres and the electronic domain, involving computing and routing units, are high-speed optical transceivers (see Figure 1) – they are the most critical element in optical communication links.

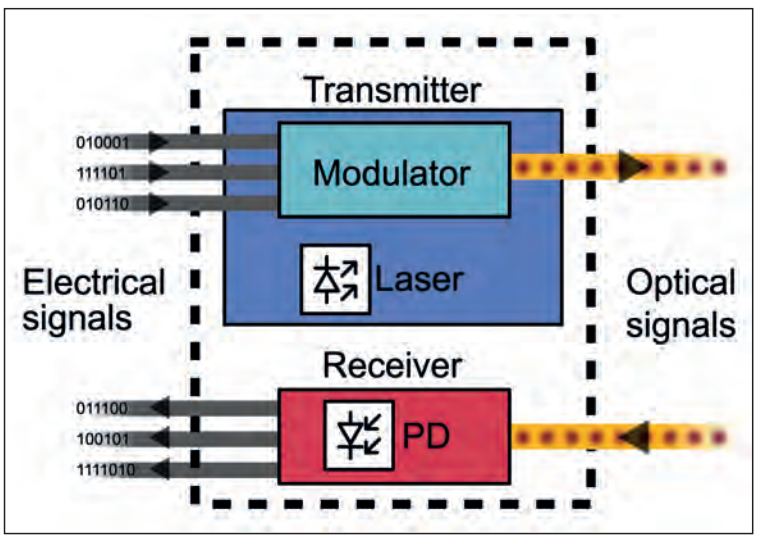

Figure 1. An optical transceiver provides an interface between electrical and optical communication channels. The transmitter converts electrical signals into optical signals. Vice-verse, the receiver is used to convert optical signals into electrical signals.

There are two parts to the optical transceiver: the transmitter and the receiver. The transmitter contains a high-speed electro-optical modulator, which encodes input signals onto an optical carrier by a continuous-wave laser diode. After encoding, the optical signal is transmitted over an optical fibre. When the optical signals reach the transceiver, they are converted from the optical domain to the electrical domain with a photodetector.

Our team at IBM Research Europe has been pioneering a platform that paves the way to compact, high-bandwidth, power-efficient optical transceivers. At the heart of our technology is the co-integration of barium titanate (BTO), selected for its extremely strong electro-optic switching properties, with ultra-thin III-V technology, which provides a gain material for light emission, on a single silicon photonics platform. Lumiphase further develops such efficient switching products based on BTO photonic technology for commercial exploitation.

Here we detail how we integrate these different functional materials onto a silicon photonics platform. To fully unleash the functionality of all the layers, we have taken much care to ensure that we transfer light with low loss between different photonic layers. Efforts have also been directed at developing devices for potential applications such as optical transceivers and novel neuromorphic photonic architectures.

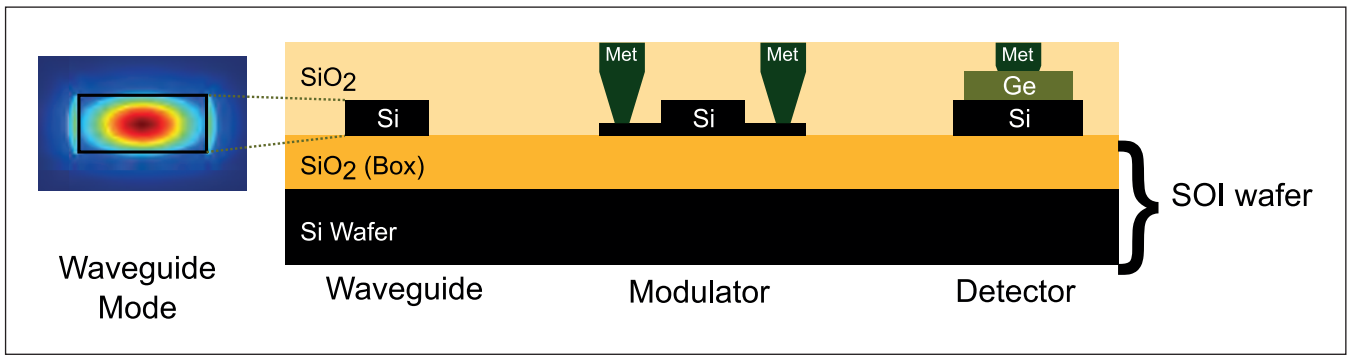

Figure 2. A silicon photonics platform with a waveguide, electro-optic modulator and germanium photodetector. Devices are fabricated on a silicon-on-insulator wafer (SOI). The waveguide mode shows the electric field intensity (red depicts high intensity, blue is for low intensity) in the waveguide (black box).

Silicon photonics: power and flexibility

The foundation for our work is silicon photonics. It offers efficient routing, manipulation, detection and modulation of light at telecommunication wavelengths, which span the range 1.3 μm to 1.55 μm. Today, silicon photonics is a mature photonic integrated circuit (PIC) technology, suitable for high-volume, low-cost production in CMOS foundries. Most commercial platforms are limited to the integration of PICs with optical components, such as waveguides, modulators and detectors, but also approaches to combine electronic and photonic integrated circuits (EPICs) are being developed. These approaches bring on-board electronic circuits, such as drivers, amplifiers, or control electronics, monolithically co-integrated with photonic components. Our technology is compatible with both PIC and EPIC platforms.

Silicon photonics is based on guiding light in silicon waveguides clad by SiO_2. Manufacturing this technology in state-of-the-art processing facilities enables the production of waveguides with propagation losses below 1 dB/cm. Due to the high refractive index contrast between silicon and its native oxide, light is well confined in the waveguides, enabling the realisation of low-loss bends with radii below 10 μm. In addition to waveguides, there are many other passive building blocks in silicon photonic circuits, including: splitters and combiners; low-loss waveguide crossings; tapers; reflectors, which may be based on Bragg gratings; and Echelle gratings. Thanks to many years of research and development, various structures have been established, including passive filters that provide wavelength multiplexing and demultiplexing on photonic chips.

It is also possible to produce some active components with silicon photonics. One example is the electro-optic modulators based on the plasma dispersion effect in silicon. Injecting or depleting carriers creates an electrically induced change in the refractive index. Instead of solely changing the real part of the refractive index, there is also a shift in the imaginary part, due to the plasma dispersion effect. As designers of advanced modulators do not welcome this change in absorption, it must be avoided to boost the performance of future generations of silicon photonic modulators.

Two of the biggest drawbacks of silicon are that it cannot emit light; and that it is transparent at telecommunication wavelengths, making it unsuitable for efficient high-speed photodetectors. To equip circuits with these functionalities, direct-bandgap materials such as III-Vs are co-integrated with silicon. The most common approach for light detection is to add germanium, integrating this on silicon waveguides used for advanced photodetection. Far more challenging is the monolithic integration of the light source.

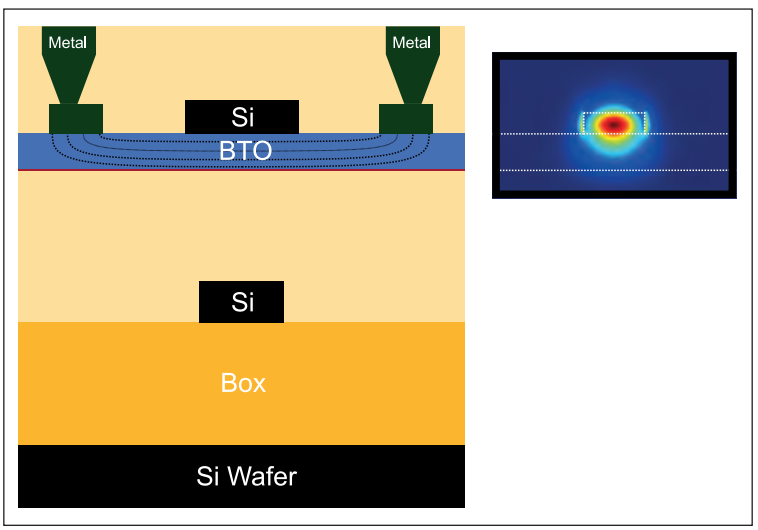

Figure 3. Cross section of a hybrid BTO/silicon device integrated on a silicon photonics platform. The refractive index of the BTO film (blue layer) can be tuned by applying an electric field (dotted lines). The inset shows the electrical field intensity of the optical mode in a hybrid silicon/BTO device. A large fraction of the optical power overlaps with the barium titanate film.

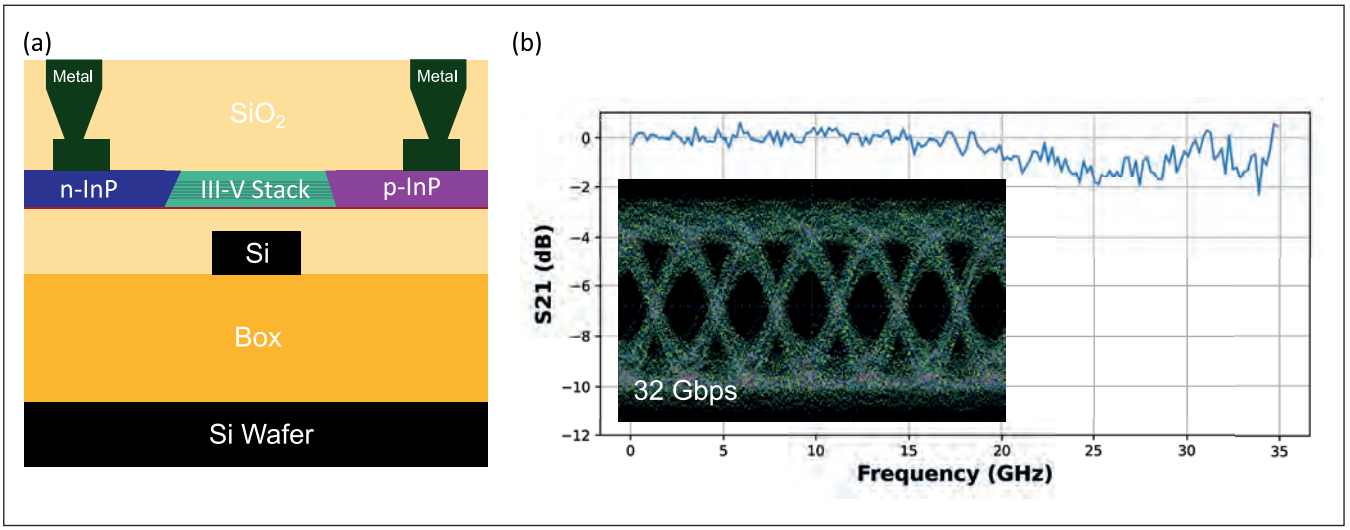

Figure 4. (a) Ultra-thin, CMOS compatible III-V integration on a silicon photonics platform. (b) Frequency response of a III-V photodetector. The inset shows an eye-diagram of the detector operated at 32 Gbit/s (NRZ signal) without using digital signal processing.

Roles for barium titanate and III-Vs

A novel material for improving the performance of silicon photonics is the ferroelectric oxide barium titanate (BTO). It is blessed with one of the largest known Pockels coefficients – this means that it produces one of the most significant changes in refractive index upon application of an electric field. Additional merits of the Pockels effect in BTO are that the refractive index changes are ultra-fast, its static power consumption is extremely low, and it tunes purely the real part of the refractive index, without any absorption.

Exploiting all these strengths enables the construction of ultra-small, energy-efficient, fast modulators, optical switches, and tuning elements, operating by modulating the phase of an optical wave but not its amplitude. Note that there is no Pockels effect in silicon and realizing these functions directly in silicon through the plasma dispersion effect leads to much less favourable properties.

We integrate BTO by loading large silicon-on-insulator (SOI) substrates into an MBE chamber and epitaxially growing a thin film of this oxide. Subsequent low-temperature molecular wafer-bonding allows us to transfer the BTO films to a silicon photonics wafer. By limiting the thermal budget, we ensure that the integration of BTO is compatible with CMOS foundry processes, enabling co-integration with CMOS circuits. That is a major asset for high-speed applications, because monolithic co-integration limits unwanted capacitive effects.

The next step in the fabrication process involves the etching of silicon waveguides into the silicon film on top of the BTO to create hybrid silicon/BTO devices (see Figure 3). The etched silicon waveguide guides the light, while a large fraction of the optical power overlaps with the underlying BTO film. Using this architecture, we have constructed Mach-Zehnder interferometers that offer efficient modulation and provide an excellent value for the figure of merit known as $V_\pi L$– it is 0.2 Vcm, which is about one order of magnitude smaller than a typical silicon photonic modulator based on the plasma dispersion effect. As BTO modulators are field driven, they can also be used as low-loss switches, requiring a switching power of only about 100 nW.

As regular readers of this magazine know, III-Vs have been used for several decades to make high-performance lasers, as well as excellent photodetectors with bandwidths reaching more than 100 GHz. One option for integrating III-Vs with silicon is to employ the wafer bonding technique used to incorporate BTO films. However, today's III-V stacks are often relatively thick, making them incompatible with the CMOS/silicon photonics process.

To use wafer bonding, III-Vs would have to be integrated on a CMOS/silicon photonics wafer in a dedicated fabrication line after completion of CMOS/silicon photonics processing. This effectively rules out direct co-integration with CMOS circuits.

To overcome this limitation we have been exploring the use of an ultra-thin hybrid III-V platform that is fully CMOS compatible. This approach involves lateral injection or collection of carriers in and out of the multi-quantum-well stack. Using ultra-thin stacks, we have built III-V photodetectors with a large bandwidth on a silicon photonics wafer (see Figure 4).

Creating co-integration

Each of the materials that we use has its particular strengths. Silicon holds the key to low-cost photonic circuits, BTO brings efficient modulation, and III-Vs offer efficient light emission and detection. To bring

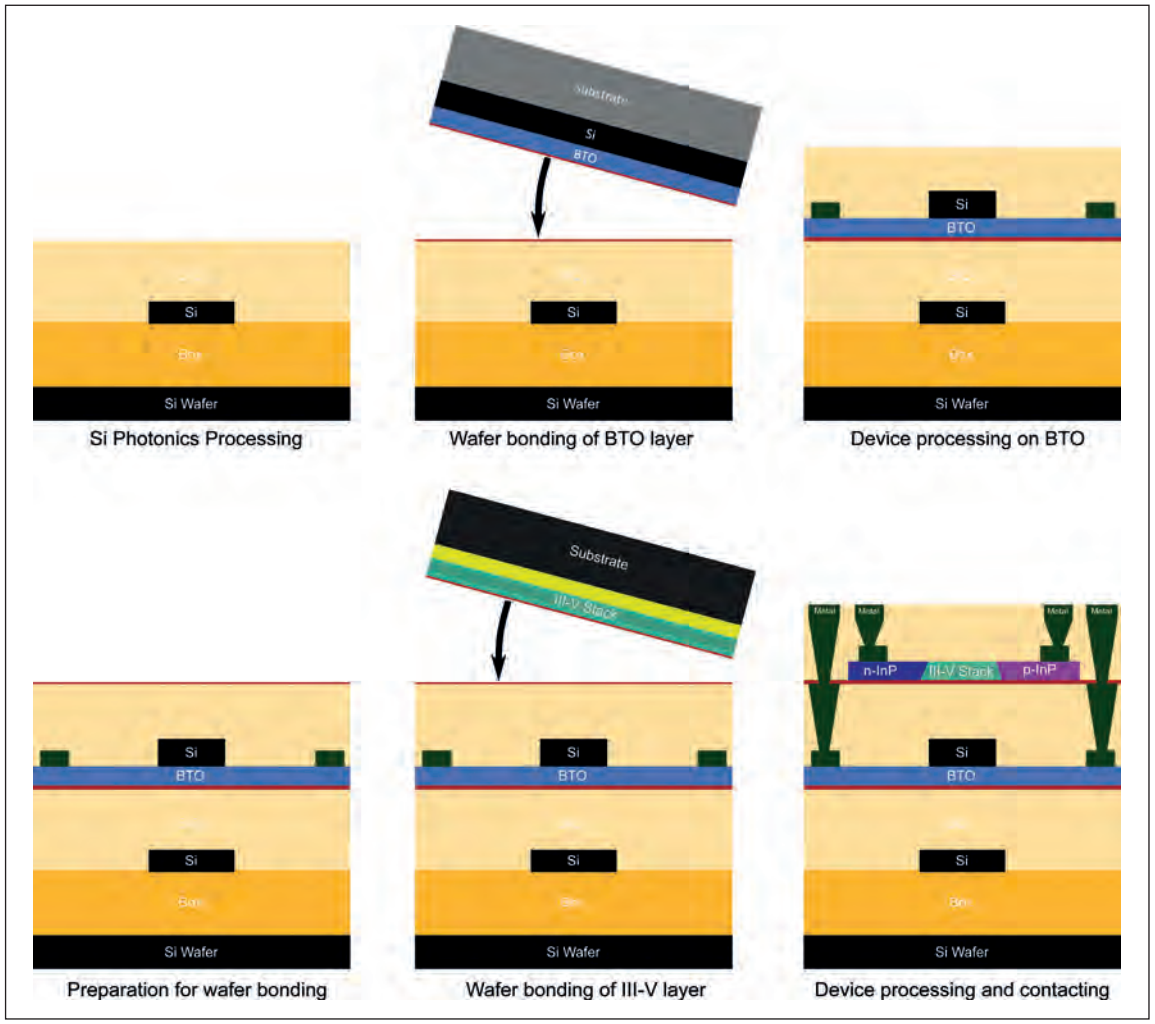

Figure 5. Co-integration of BTO/silicon and III-V technology on a silicon photonics wafer involves the following steps: (1) Processing a silicon photonics wafer and depositing a thin SiO_2 layer on it. Preparing the SiO_2 surface for molecular wafer bonding by chemical mechanical polishing (CMP). (2) Using molecular wafer bonding to integrate a BTO/silicon film on top of the silicon photonics wafer. (3) Defining devices on the BTO/silicon layer. (4) As in step 2, depositing a thin SiO_2 layer and preparing its surface for molecular wafer bonding. (5) Using molecular wafer bonding to integrate a III-V layer on top of the stack. (6) Processing devices in the III-V layer and contacting devices in both co-integrated layers.

them all together in a single photonics platform we begin by fabricating a silicon photonic wafer with a planarized top surface, before transferring a single-crystal BTO layer onto the planarized surface and defining waveguides. Final steps involve bonding a III-V photonic layer, and subsequent processing to create active/passive devices (see Figure 5 for details).

To leverage the benefits from all three classes of material, we use waveguide tapers to ensure a low optical loss when transferring light between the layers. The efficiency of these tapers is enhanced by employing an inverse direction on neighbouring layers. For example, to couple light from the silicon photonics layer to the BTO/silicon layer, we slowly decrease the width of the silicon photonics waveguide (taper down) while increasing the width of the BTO/silicon waveguide width (taper up).

Reducing the silicon waveguide width leads to a decrease in the effective optical mode index and an increase in the mode size along the waveguide taper. This goes hand-in-hand with increasing the width of the BTO/silicon waveguide, which increases the effective mode index in the BTO/silicon waveguide.

As both waveguides are separated by only a thin SiO_2 cladding, there is a small overlap between the silicon and BTO/silicon modes. This overlap propels the optical mode towards the region where the effective mode index is the largest. Consequently, the mode in the silicon waveguide is first converted into a hybrid mode propagating in both the silicon and BTO/silicon waveguides, prior to full transfer to the BTO/silicon layer. This process is incredibly efficient, allowing nearly 100 percent of the light to be transferred from the lower to the upper layer.

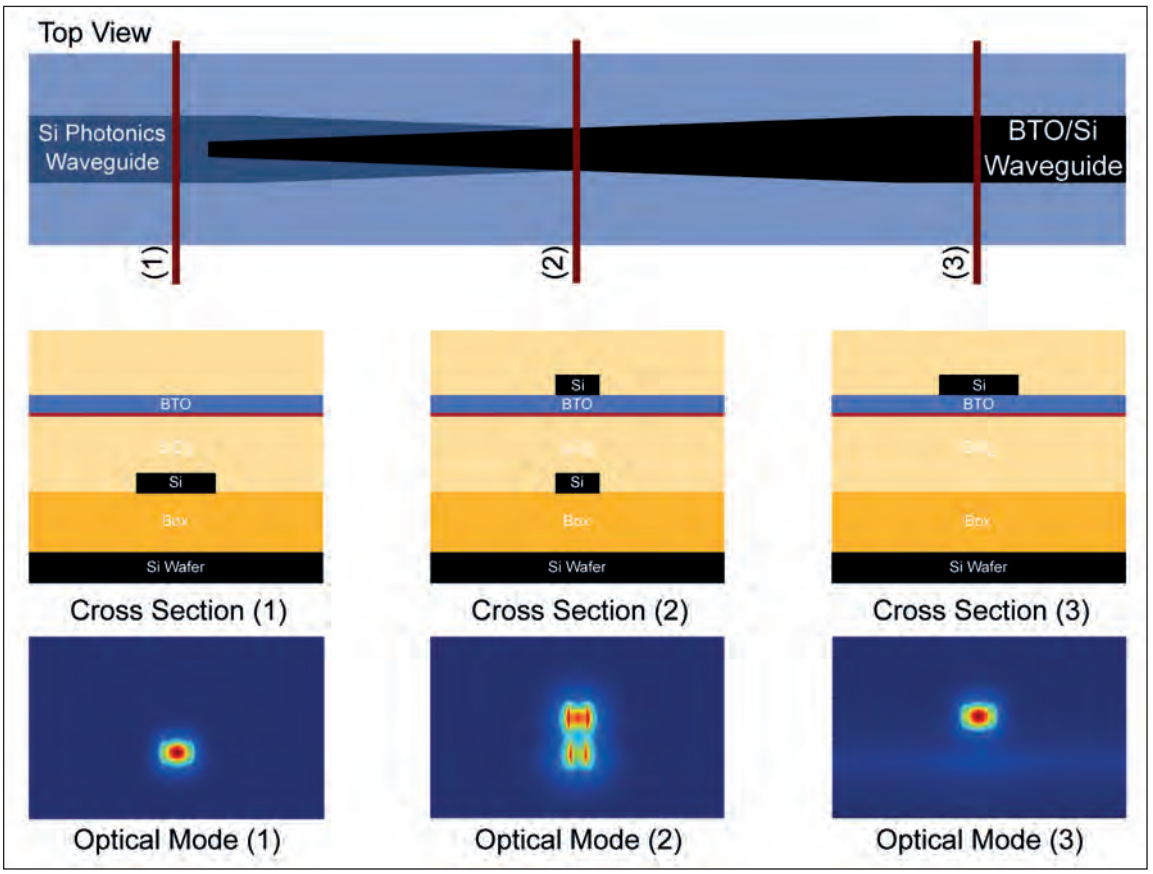

Figure 6. Inverse tapers on consecutive layers couple light between the layers. Shown here is a top view and corresponding cross sections and optical modes along a coupler between silicon and BTO/silicon. The mode is first guided in the silicon photonics waveguide. In the tapered section the mode converts into a hybrid mode, before it transfers to the BTO/silicon waveguide.

We have formed co-integrated structures by combining silicon photonic devices, formed on a 220 nm-thick layer of silicon sitting on 2 μm-thick buried oxide, with a BTO/silicon stack containing 100 nm-thick BTO and an intrinsic 250 nm-thick InP layer. Our entity features passive photonic elements on all photonic layers, demonstrating the simple building blocks of our concept. If we were to include active components, they would be realised with a similar process flow.

Within this structure, a low-loss intrinsic InP layer provides the III-V material stack. InP could act as a potential seed layer for subsequent III-V growth steps required for active III-V devices. This demonstrator, made using the process steps described previously, showcases successful co-integration of all the materials, with separate silicon, BTO/silicon and InP waveguides on different layers (see Figure 7).

We have extracted the coupling loss between the different layers using structures with a varying number of interlayer coupler pairs. To ensure waveguide propagation losses are identical, we kept the total waveguide length in each layer constant for all measurements. That allowed us to extract separate coupling losses for the coupler between silicon and BTO/silicon, and that between BTO/silicon and InP. For these couplers, both based on linear tapers, coupling losses were 0.48 dB and 0.34 dB, respectively. These values equate to power transmissions of 89.5 percent and 92.5 percent (see Figure 8).

Increasing coupling

This level of coupling is good enough for applications that require light to be transferred only a few times between the layers. But it is insufficient for optical transceivers or advanced photonic circuits. So we need to increase the coupling efficiency, a goal that can be met by addressing the two major loss mechanisms: the mode transfer loss, caused by the mode conversion between the waveguides; and propagation loss, attributed primarily to sidewall roughness.

One of the keys to increasing coupling is to optimise the length of the tapers. At first glance, a very long taper is ideal, providing a small mode transfer loss, due to slow mode conversion – in the best case this process can be virtually loss free. However, long tapers are not a panacea, because they lead to a larger propagation loss in the waveguides in the coupling region, and they occupy a larger chip area.

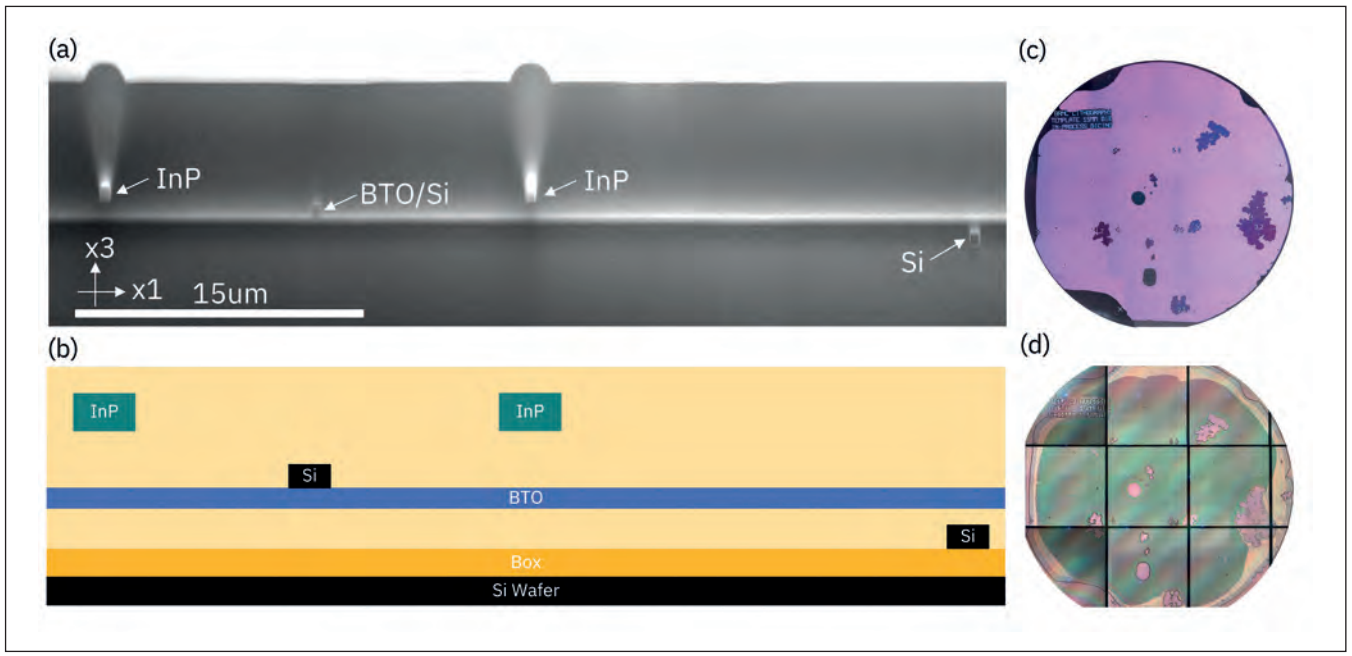

Figure 7. (a) and (b) Co-integrated waveguides in silicon, BTO/silicon and InP. (c) Wafer bonding of BTO/silicon (pink) on the silicon photonics acceptor wafer. Some defects, seen as dark areas, appeared during wafer bonding. (d) Wafer bonding of an InP layer (green colour) on top of the BTO/silicon layer. Defects in the BTO/silicon layer are transferred to the InP layer.

The sweet spot is the use of tapers that are as short as possible, but long enough to ensure that mode conversion is almost loss free. In our experiments, we have found that the coupling loss decreases with increasing coupler length (see Figure 8 (b)). This implies that we are yet to reach a taper length where propagation length dominates over mode transfer loss.

Coupling loss can be reduced even further by optimising the shape of the tapers. We have investigated this through simulation, considering optical modes in many equally distributed cross sections along the coupler structure (see Figure 9 (a)). Our studies consider the mode overlap between consecutive sections. When the mode overlap is large, the mode does not change much. However, when the overlap is small, there is a significant change in the mode field profile.

Based on these insights, mode transfer loss may be minimised by ensuring that the sections with a small mode overlap are longer, so that the mode field profile changes its shape slowly over the section length. On

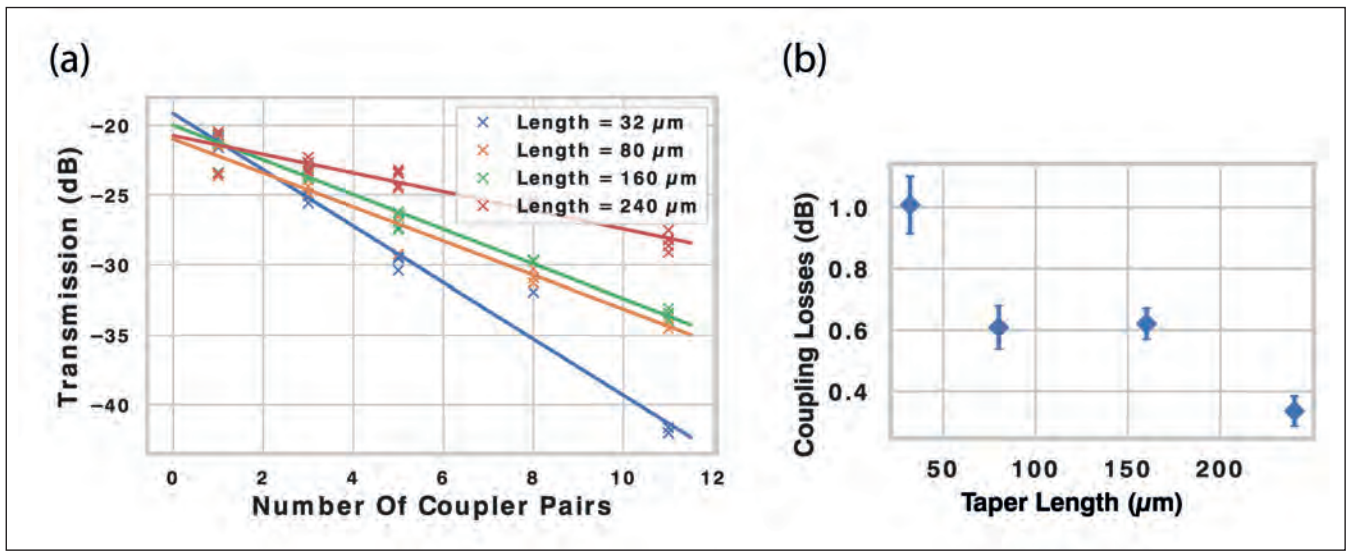

Figure 8. (a) Transmission as a function of the number of coupler pairs for different taper lengths for couplers between BTO/silicon and InP. (b) Coupling loss for BTO/silicon and InP couplers as a function of taper length

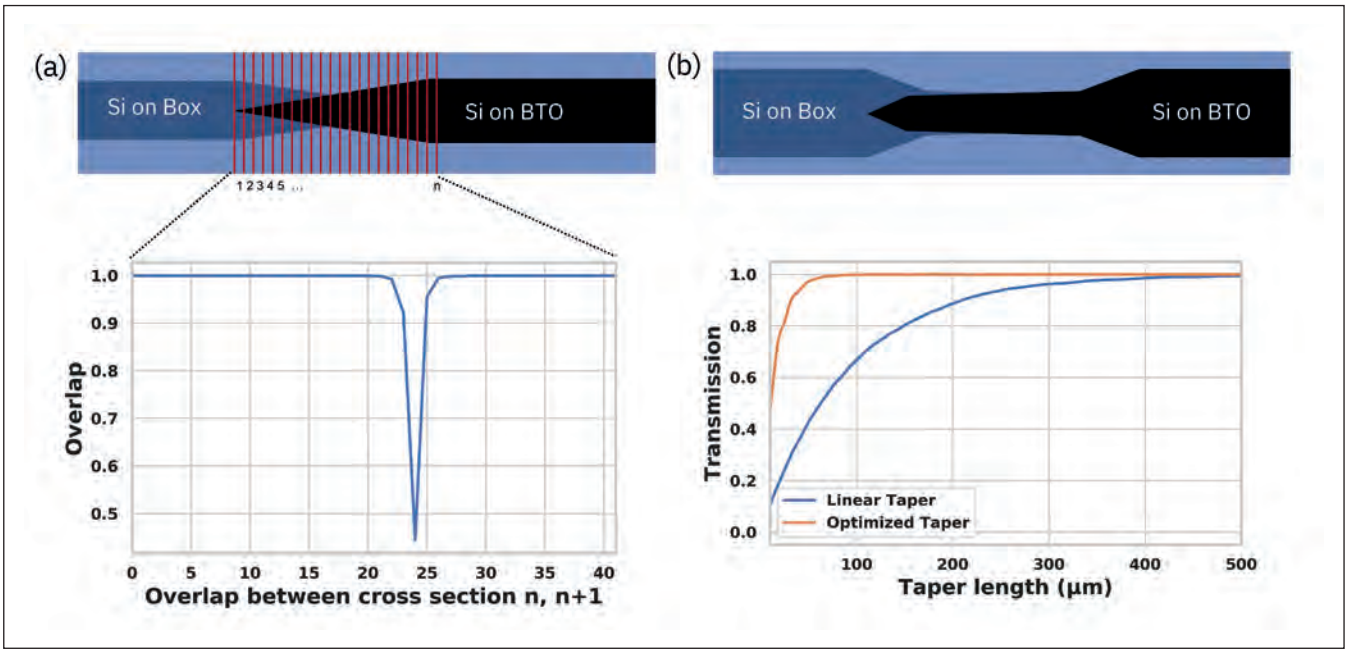

Figure 9.(a) Simulations of optical modes in 42 cross sections (red lines) along the taper. Mode overlap between consecutive sections were computed. (b) Simulated transmission for light coupling from silicon to a BTO/silicon layer as a function of taper length. A transmission value of 1 means that the mode is transferred without any loss. Using the optimised taper shape, a transmission exceeding 99.5 percent is realized for 90 μm-long tapers.

the other hand, sections with a large mode overlap can be shortened, helping to trim propagation loss.

Drawing on mode overlap calculations, we have designed a taper containing three linear sections with different taper slopes. Using Lumerical Mode simulation software, we have found that the mode transfer efficiency exceeds 99.5 percent for 90 μm-long optimised tapers. Switch to a linear taper, and a length of 500 μm is required to deliver a similar performance. Or, to put in another way, by adopting an optimized shape we can slash the length of our taper by a factor of six while maintaining the mode transfer efficiency.

Targeting applications

Data centres and long-haul communication systems are generating strong demand for fast optical transceivers that are power- and cost-efficient. Using our platform, we can form high-performance transceivers from efficient transmitters and receivers. Efficient transceivers are formed by generating continuous-wave optical signals with a III-V laser, subsequent modulation with a BTO/silicon electro-optical device, and turning to a silicon photonics platform to efficiently route, filter and multiplex the signals. If available, we can deploy electronic circuits for the integration of drivers for the laser and modulator. On the receiver side, we use a germanium-silicon photodetector – or, if we require a higher bandwidth, variants made with III-Vs. Here, the roles for silicon photonics circuits could include providing optical filters and demultiplexing circuits. In EPIC platforms, amplifiers and analogue-to-digital converter circuits might also be integrated.

It is clear to see that armed with a platform featuring multiple functional layers, it is possible to combine the strengths of the existing silicon photonic ecosystem with novel functionalities for modulation, emission, and detection. This expansion in functionality also opens the door to radically new fields of applications, such as optical neuromorphic computing. We

It is clear to see that armed with a platform featuring multiple functional layers, it is possible to combine the strengths of the existing silicon photonic ecosystem with novel functionalities for modulation, emission, and detection. This expansion in functionality also opens the door to radically new fields of applications, such as optical neuromorphic computing

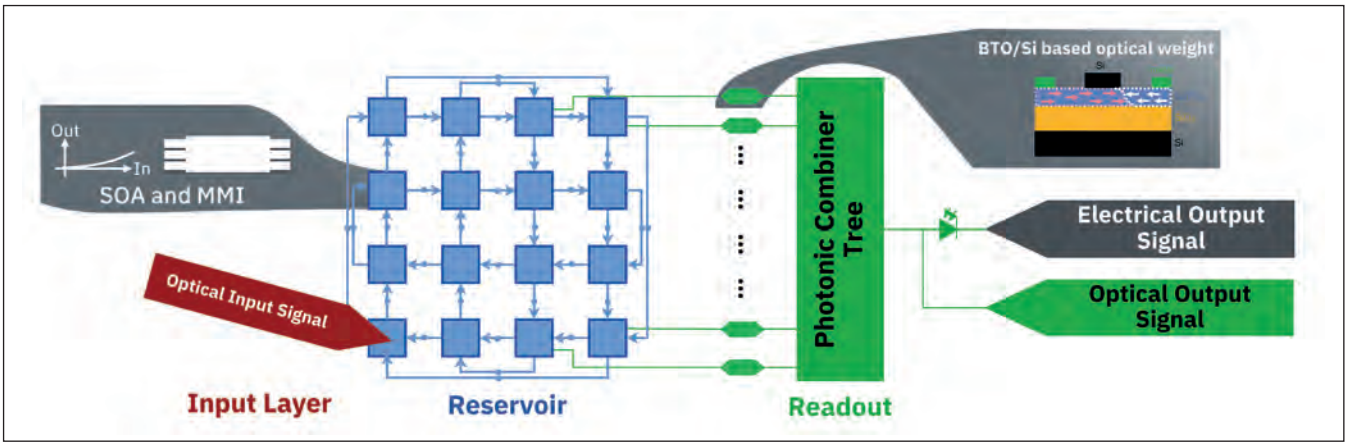

Figure 10. Concept for an all-optical reservoir computing system. Silicon photonics is used to route and mix signals between different nodes (blue squares). Semiconductor optical amplifiers (SOA) based on III-V technology provide a non-linear response at each node. Barium-titanate-based optical weights at the output of the reservoir tune signals, before they are united through a photonic combiner tree. The output signal is converted to the electrical domain using a III-V based photodetector.

have started to consider this opportunity, exploring integrated, all-optical reservoir computing systems based on our co-integration platform (Figure 10). These reservoir computing systems are a special type of neural network, in which only the synaptic weights at the output layer are trained, while weights within the network are random but fixed.

Realising such networks requires the building of various blocks that are not available in standard silicon photonics. They include ultra-compact optical non-linearity or non-volatile optical weights. The good news is that semiconductor optical amplifiers based on III-V technology provide the required non-linear optical response, while BTO/silicon switches, which store their state in the ferroelectric domain configuration of the BTO film, can be used to form non-volatile optical weights. Applying large electric pulses tunes the domain configuration, which is retained for up to several days after the state is set. Uses of optical reservoir computing systems include compensating fibre-optic dispersion and performing Boolean operations, prior to the conversion of optical signals into the electronic domain by a transceiver.

Our efforts have shown that by co-integrating BTO/silicon and III-V technology with silicon photonics we have created a very versatile photonic platform with novel optical building blocks. Results on this platform, featuring low-loss interlayer coupling, demonstrate for the first time the combination of three complementary but powerful technology platforms in a scalable, efficient manner. This multi-functional photonic platform enables not only efficient optical transceivers, but further exciting new applications, such as optical computing and signal processing.

We would like to thank Daniele Caimi, Felix Eltes, Yannick Baumgartner, Youri Popoff and Norbert Meier for their support for the fabrication of the coupling demonstrator. This project has received funding from the EU-H2020 research and innovation program under grants no. 688003 (DIMENSION), 688579 (PHRESCO) and 780997 (plaCMOS).

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Lasers:
Accelerating visible light communication

GaN-based single-mode lasers get ready to revolutionise communication

BY MEIWEI KONG, JORGE HOLGUIN-LERMA, TIEN KHEE NG AND BOON S. OOI FROM KING ABDULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

THERE IS GREAT DEAL going for the use of light for wireless communication. Compared with the standard radio frequency bands employed by mobile devices, the bandwidth is unlicensed and more than a thousand times greater. However, despite these merits, it's not to say that it has to be one technology or the other. Far better is a future that sees light-based wireless communication merge with existing technologies operating in the radio and millimetre-wave regime to spawn a synergic scheme that drives a new era for connectivity.

While the light source for communication can operate in the UV or the IR, it is far better if it is in the visible, as this allows simultaneous illumination and communication. Communicating via visible light is already attracting much commercial interest, thanks to its capability to transmit data at high speeds, its compatibility with large-scale integration, and its freedom from electromagnetic interference.

The conventional light source for visible light communication is the LED. This device is normally in the form of a white emitter, created by coating a blue GaN-based chip with a colour-converting phosphor. Such devices have fuelled the rise of visible light communication, and offered a vision of street lamps providing internet to anyone passing by.

By adopting advanced modulation technologies, researchers have been able to coax data rates of up to several Gbit/s from a single LED. Increased speeds and greater modulation bandwidth have come from miniaturising the device to form a microLED. However, faster speeds come at the expense of output power. Select a conventional LED and you'll get a high optical power and a brightness well-suited for illumination, but the modulation speed is limited; replace this with a microLED and you'll enjoy a very attractive modulation speed, but you'll fall short in illumination.

Fortunately, there is an alternative that eliminates compromise: the laser diode. But is it a good solution? Absolutely, according to our team at the King Abdullah

Photo credit: Yujian Guo

University of Science and Technology. We have been building on the efforts of developers of lasers based on distributed feedback (DFB). These devices can combine lighting levels of brightness with data rates that are higher than those of microLEDs.

Transmitting data wirelessly at high speeds is in much demand. It is needed for emerging applications that include virtual reality, augmented reality, and autonomous driving. This demand has led to new ventures, such as laser-interconnected satellite constellations, such as Starlink, developed by SpaceX. Efforts are also directed at constructing next-generation communication networks known as LiFi. In all these cases, the goal involves establishing a ubiquitous wireless network, unbounded by the limitations of classic infrastructure. The vision is clear; it will not be long before wireless data is burdened by a congested radio-frequency spectrum. Light-based wireless communications in the IR, visible and UV offer a solution, and could make a valuable contribution to 5G networks.

Laser credentials

Laser diodes are well-positioned to make an impact. These energy-efficient sources combine high-brightness illumination with very high-speed data transmissions, and have the potential to replace LEDs in very-high-speed visible light communication applications, such as smart factories, intelligent transportation and large-capacity broadcasting, where data rates need to be at least 10 Gbit/s. Highlighting what is possible are the white-light sources containing blue GaN lasers, which are now appearing in the market, launched by companies such as SaNoor Technologies and SLD Laser. Variants have also been deployed in cars, with laser headlights powered by Osram's chips available in some models from BMW and Audi. And if you take a glance at the scientific literature, you'll see many reports on the impressive properties of lasers for record-breaking visible light communication, leading one to wonder what more is to be done.

One route that we are pursuing, which can lead to far higher date rates than have been seen to date, is to switch to a different laser architecture. Conventional GaN laser diodes feature a Fabry-Pérot cavity that gives rise to longitudinal modes known as Fabry-Pérot cavity modes. These modes, which lead to the emission of a range of closely spaced wavelengths, are fairly acceptable for many applications. However, this architecture is not used in the telecommunication industry, which employs wavelength-division multiplexing to increase the data transmission capacity of optical fibres by a factor of several hundred. The key ingredient for wavelength multiplexing is the single-frequency or single-mode laser. This is the way to go for visible light communication.

It is possible to produce a single-frequency source with a solitary longitudinal mode by modifying the

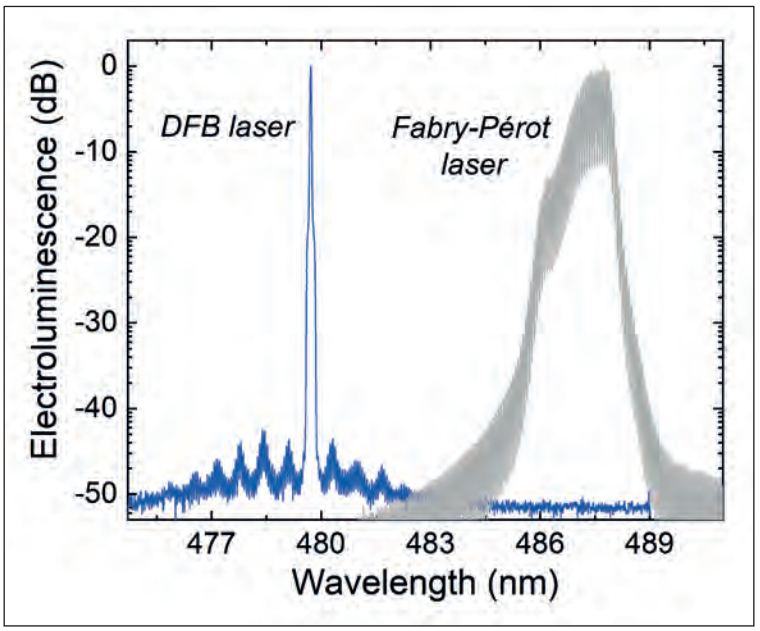


Figure 1. The multiple cavity modes of a Fabry-Pérot laser can be reduced to a single mode by adding a DFB grating. The figure shows a GaN-based sky-blue colour laser.

Fabry-Pérot laser (illustrated in Figure 1). Single-mode operation can be achieved in several ways. One can introduce external elements and external laser cavities, such as prisms, gratings, and mirrors mounted on an optical bench. But it is preferable to avoid moving parts, and create instead a compact source that is immune to vibrations, with the technology for realising a single mode self-contained on a single chip. This type of device, sporting a monolithically integrated distributed-feedback (DFB) grating, uses diffraction to ensure feedback into the laser cavity at a specific frequency. The frequency that becomes the dominant mode is determined by both the material used in the laser and the geometry of the grating.

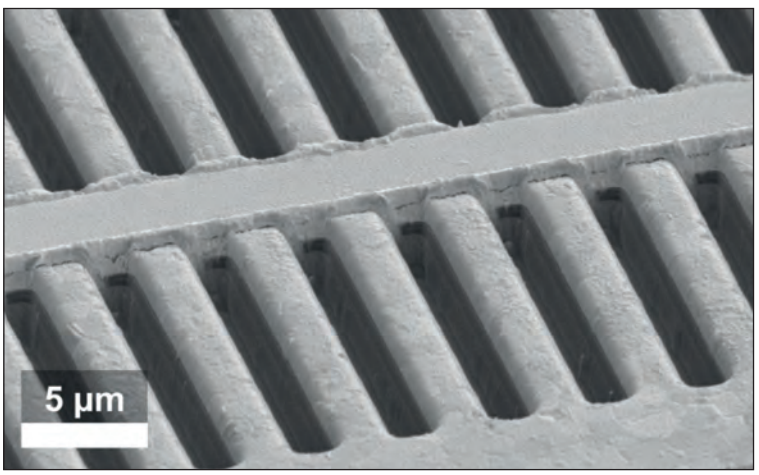


Figure 2. A DFB grating fabricated on the surface of a laser diode from KAUST. Using a surface grating allows a single-mode output without the need for the difficult overgrowth process in GaN lasers.

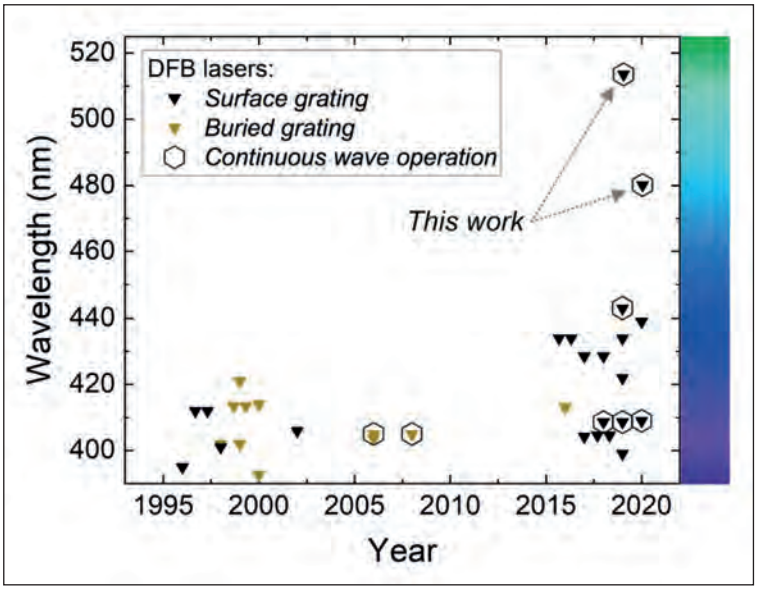


Figure 3. The history of GaN-based DFB lasers at different wavelengths with the rise of surface gratings, including KAUST's contribution to unexplored wavelengths in the blue-to-green regime.

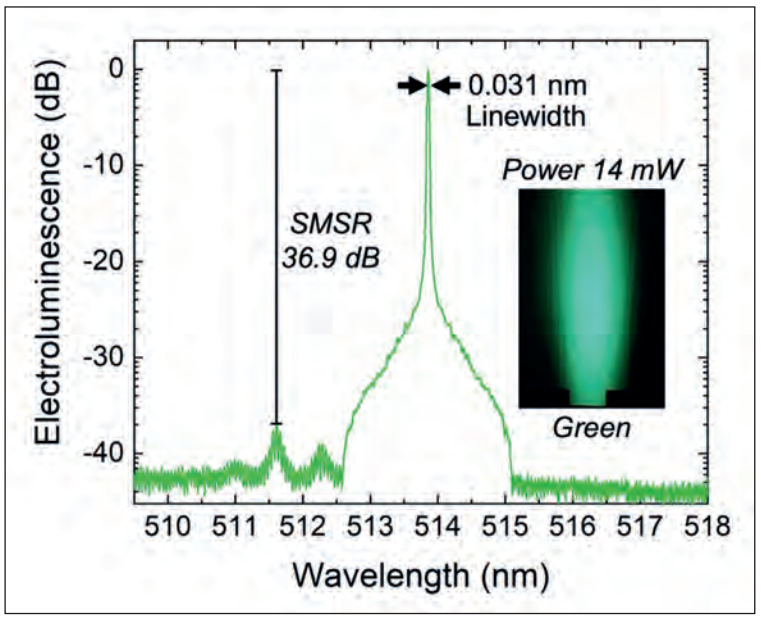


Figure 4. Green DFB laser emission shows a resolution-limited single-mode at around 514 nm. The inset reveals a real-colour image of the laser far-field pattern. The side-mode suppression ratio (SMSR), linewidth, and optical power help to evaluate the quality of the DFB laser.

InP-based DFB lasers are widely available at telecommunication wavelengths, but in the visible spectrum, especially in the blue and green – a domain only reached using GaN materials – they are relatively unexplored. In fact, there are no commercially available GaN-based DFB lasers.

The history of the DFB laser can be traced back to 1996, just a year after the device made its debut. Researchers at the University of Stuttgart, Germany, are to thank for this breaking of new ground – but their aim was not to realise single-mode lasing. Instead, they introduced DFB to address the poor quality of the mirrors in the laser cavity. Back then, the hardness of GaN and its crystal properties hampered efforts to cleave and etch the cavity mirrors.

Problems associated with making mirrors have been addressed, but difficulties in processing GaN remain. These issues need to be understood in order to appreciate the state-of-the-art methods employed for creating modern GaN DFB lasers.

To produce the classical DFB gratings found in InP lasers, engineers embed the grating inside the device. These buried gratings are formed by growing the initial layers of the laser, before etching and subsequent growth of a second stack of materials – the latter process is known as overgrowth.

Producing gratings by this complex approach is particularly demanding for GaN-based materials. Even though buried gratings were used in the first GaN DFB laser diodes producing continuous-wave operation, announced in 2006 by Nichia Corporation, difficulties in processing and overgrowth still present a significant challenge. Illustrating this point, no further work was reported for ten years.

Surface gratings

A radical re-design is to thank for a new era of GaN DFB lasers. Switching from buried to surface gratings has opened the door to the use of highly mature materials, employed to create the latest generation of compact single-frequency DFB lasers at violet and blue wavelengths (see Figure 2). Unlike buried gratings, surface gratings are simply formed on top of the laser, eliminating the need for overgrowth. This makes them easier to fabricate. Look back at the paper detailing the DFB laser from 1996 and you'll find that this was the approach taken back then. But only recently have fabrication and material-growth skills fused together in pursuit of creating GaN-based single-frequency lasers.

Uses for these single-frequency visible DFB lasers extend beyond what one might think of as very-high-speed visible light communication. Two examples are miniaturized atomic clocks, which could soon become a reality; and wireless internet underwater, due to the overlap of the blue-to-green spectral domain with the transparency window of ocean and sea waters.

To increase data rates underwater, and also above ground and in space, systems can be built that match the emission of the DFB laser to one of the low-intensity wavelengths of sunlight, also known as a Fraunhofer line. This provides a boost to the signal-to-noise ratios of communication channels and environmental sensors. As far back as 1986 researchers at the the Jet Propulsion Laboratory were evaluating the use of Fraunhofer channels for data transmission in space; by 1992 scientists at the US Naval Command, Control and Ocean Surveillance Center were exploring this idea for underwater communications; and in 2013 Ocean University of China reported new observations of improved environmental sensing, using sources operating in Fraunhofer lines.

We are building on this work by investigating visible-light DFB lasers that generate single-frequency emission at unexploited wavelengths in the blue and green – we are evaluating a domain from 450 nm to 520 nm (see Figure 3). Producing laser diodes in this spectral range is not easy because material quality falls, driving down efficiency, as emission is propelled from the violet towards the green by increasing the indium content within key layers of the device. This material limitation helps to explain why, until recently, there have been no GaN DFB lasers operating beyond 450 nm.

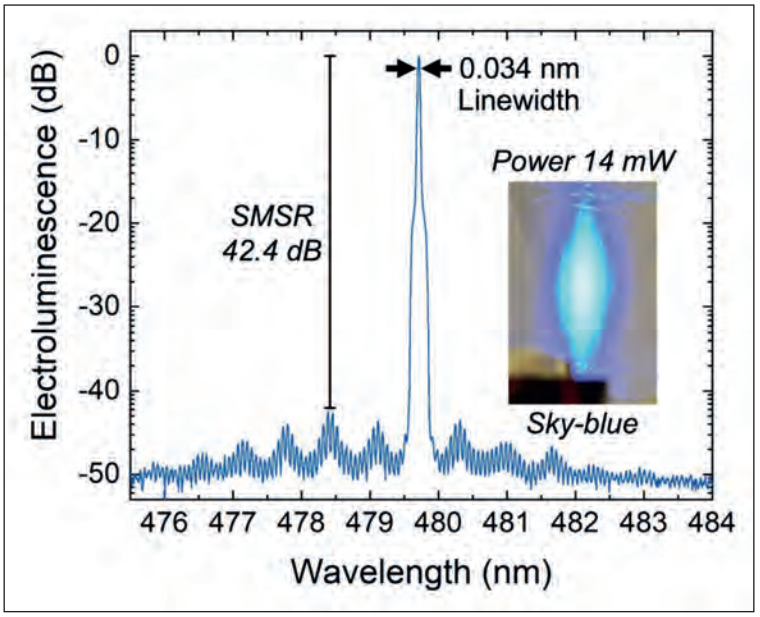


Figure 5. Sky-blue DFB laser emission shows a resolution-limited single-mode at around 480 nm. The inset shows a real-colour image of the laser far-field pattern. The side-mode suppression ratio (SMSR), linewidth, and optical power help to assess the quality of the DFB laser.

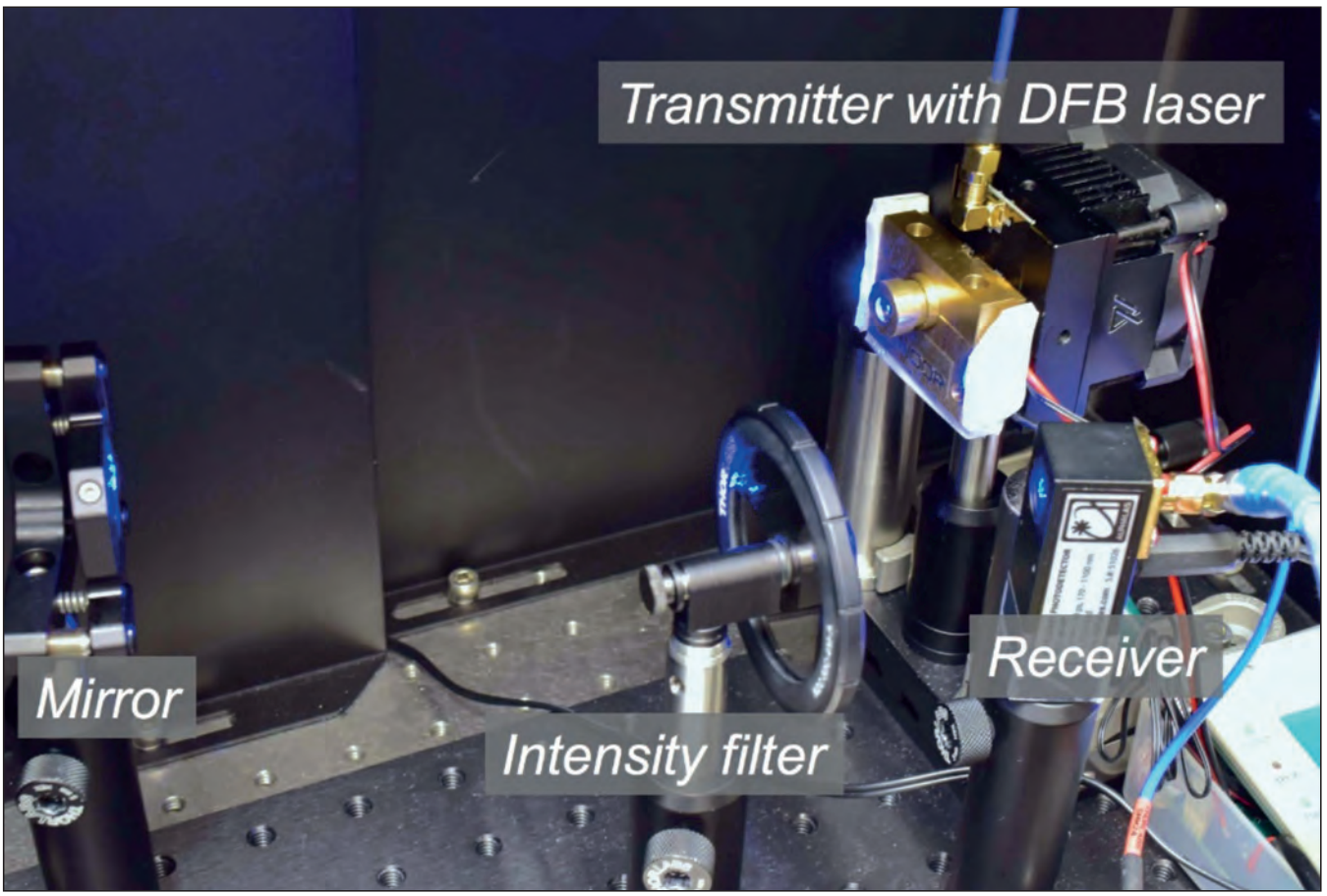


Figure 6. KAUST's testbed for proof of concept. The goal is beyond 10 Gbit/s using a GaN DFB laser.

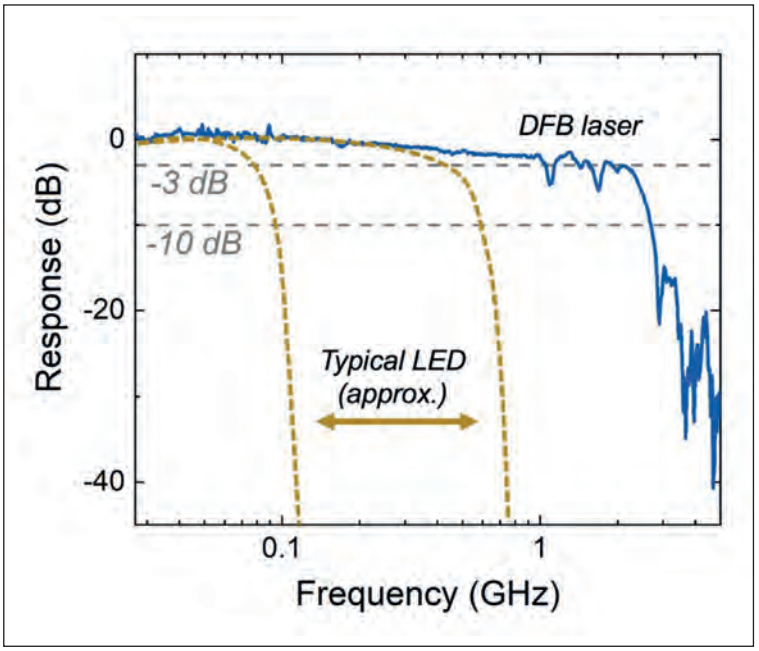


Figure 7. High-speed modulation bandwidth of the sky-blue DFB laser compared with the approximate bandwidth of typical LEDs (ranging from high-power LEDs to faster microLEDs).

To break new ground, we have turned to a microfabrication technique that is suitable for prototyping. We use a focused-ion beam to define a surface grating on the top of laser diodes that are new to the market. These lasers, operating at around 480 nm (sky blue) and 520 nm (green), have much promise for underwater LiFi and low-background noise systems. That's because they are in the vicinity of Fraunhofer lines, particularly the Hydrogen-beta line at 486.13 nm and the Magnesium-b1 line at 518.36 nm.

As the gratings in our lasers are based on the high-order Bragg condition they are spaced relatively far apart, reducing fabrication complexity. If first-order gratings were used for visible lasers, this would require high-end electron-beam lithography, which is relatively expensive and time-consuming.

Although high-order gratings have the potential to introduce diffractive losses, our devices are still able to generate laser light. We have demonstrated a 513.85 nm laser that delivers a 14 mW output at room temperature and has a linewidth of 0.031 nm with a side-mode suppression ratio of 36.9 dB (Figure 4). In comparison, before we introduced the high-order DFB surface grating into the classical multi-mode Fabry-Pérot GaN-based green laser, this device showed a linewidth of 0.540 nm and a side-mode suppression ratio of 0.2 dB. These changes are very promising, with single-mode selectivity improving by a factor of around 5000 and linewidth reducing by nearly 20 times.

We have also produced a variant in the sky-blue with a high-order grating. This 479.7 nm laser produces a continuous-wave optical power of around 14 mW at a slightly cooled room-temperature of 16 °C, has a linewidth of 0.034 nm, and a side-mode suppression ratio of up to 42.4 dB (see Figure 5). This linewidth is narrow enough to enable between 25 and 30 communication channels in the same wavelength window occupied by a single conventional laser, while the side-mode suppression ratio signifies mode selectivity with a factor of around 17,000 – that is, the single-mode of the laser is thousands of times stronger than any other mode in the laser cavity. The superior selectivity of this sky-blue laser compared with its green cousin results from a combination of an optimised fabrication process and a reduction in ridge waveguide width from 4 μm to 2 μm.

Building on these successes, we have investigated the capability of our single-mode lasers for visible light communication, evaluating whether they can operate at more than 10 Gbit/s, a requirement for beyond-5G networks. Using a proof-of-concept testbed with minimal components (see Figure 6), we began by considering how fast the laser can be turned on and off. We recorded a relatively flat modulation response for our sky-blue DFB laser, with values for the –3 dB bandwidth and the –10 dB bandwidth of 1.1 GHz and up to 2.6 GHz, respectively (see Figure 7).

These figures indicate that our single-mode lasers offer a significant amount of practical bandwidth for communications. In sharp contrast, a typical LED has a bandwidth of just a few to hundreds of megahertz. Given this substantial gap in performance, it's of no surprise that lasers are gaining steam in visible light communication.

Using a simplistic non-return-to-zero on-off keying modulation technology, our DFB laser realised a transmission speed of 5 Gbit/s. With this form of modulation, on and off states provide the binary information. We visualise the signal that's received with a plot known as an eye diagram (see Figure 8). In this plot, the upper and lower levels represent the binary nature of the data, and the greater the clarity, the higher the quality of the wireless communication.

To make full use of the modulation bandwidth, we have also turned to a modulation technique called 16-quadrature-amplitude-modulation (QAM) orthogonal frequency-division multiplexing (OFDM). The OFDM technique employs orthogonal and overlapping sub-carriers that adopt the 16-QAM OFDM to improve the spectral efficiency and transmission rate.

We use a constellation diagram to evaluate the quality of the received 16-QAM OFDM signals (see Figure 8). When we see data points that are clearly separated we know that the data has been received with little to no errors. That's the case for our DFB laser, which provides data transmission up to 10.5 Gbit/s. The associated bit error rate is 2.3×10^{-3}, below the forward-error correction limit of 3.8×10^{-3}, an established criterion in the field of digital communications.

This success represents the state-of-the-art for visible DFB lasers for optical communications. But it is only the beginning, providing a small but critical step towards implementing multiple closely adjacent wavelengths. By mimicking the approach adopted in optical fibre communication, we have the potential to multiplex today's 10 Gbit/s transmission rates by a factor of ten or more.

We are now on a journey that could see arrays of single-frequency DFB lasers providing multiple channels of information for wireless internet in underwater sensors and robots, solar-resistant satellite communications, and smart automated factories.

The next step is to scale these results from the level of proof-of-concept up to laser batch-fabrication, which is required for industry adoption. Encouragingly, materials are commercially available with widely accepted process integration, but a stronger market push may be needed.

Another consideration is the verification of the linewidth of GaN DFB lasers. In our work, and in other reports in the scientific literature, optical spectrum analysers are used for this measurement. However, this equipment is limited in its resolution and fails to offer a true telling of the laser linewidth.

Nevertheless, GaN DFB lasers are becoming increasingly mature, and it will not take long before they are deployed in other applications, such as atomic clocks and environmental sensors. What's more, by targeting Fraunhofer lines, there is the opportunity for new endeavours. Our local measurements show operating at these wavelengths removes a few dBs from background radiation. There are also unexplored DFB wavelengths in the vicinity of the sky-blue and green colour regions that could enhance tools such as bathymetry and underwater optical wireless communications. In addition, narrow-line GaN DFB lasers promise to provide live-cell imaging of Förster resonance energy transfer-based biosensors. Clearly, a great future lies ahead for this visible, single-mode laser.

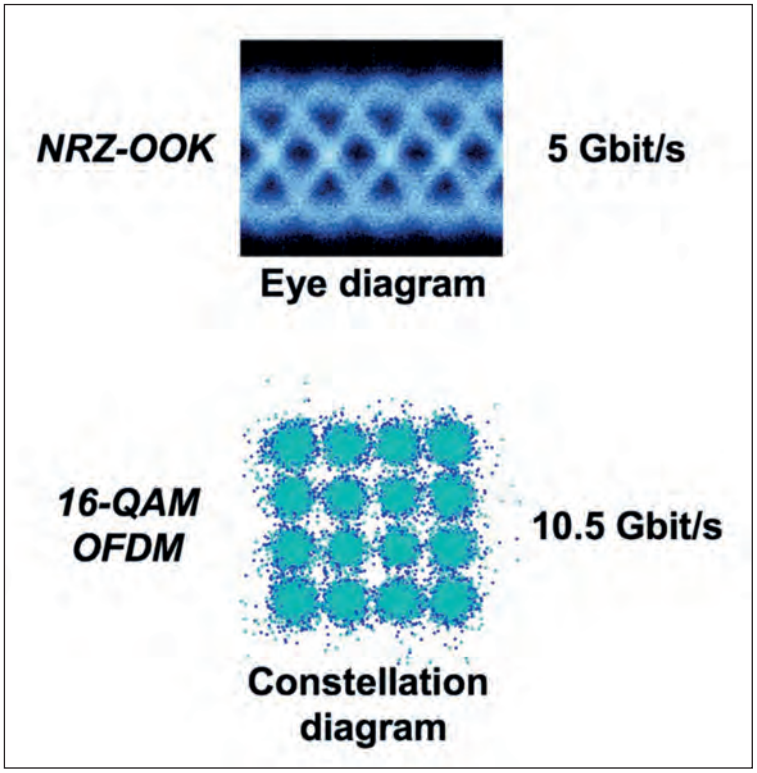


Figure 8. Digital communications can be represented visually depending on their modulation format. The figure shows the eye and constellation diagrams produced by the DFB laser.

Super-fast optical interconnects

Universal chip-to-chip optical interconnects are delivering off-package communication at the bandwidth density and energy cost of in-package electrical incumbents

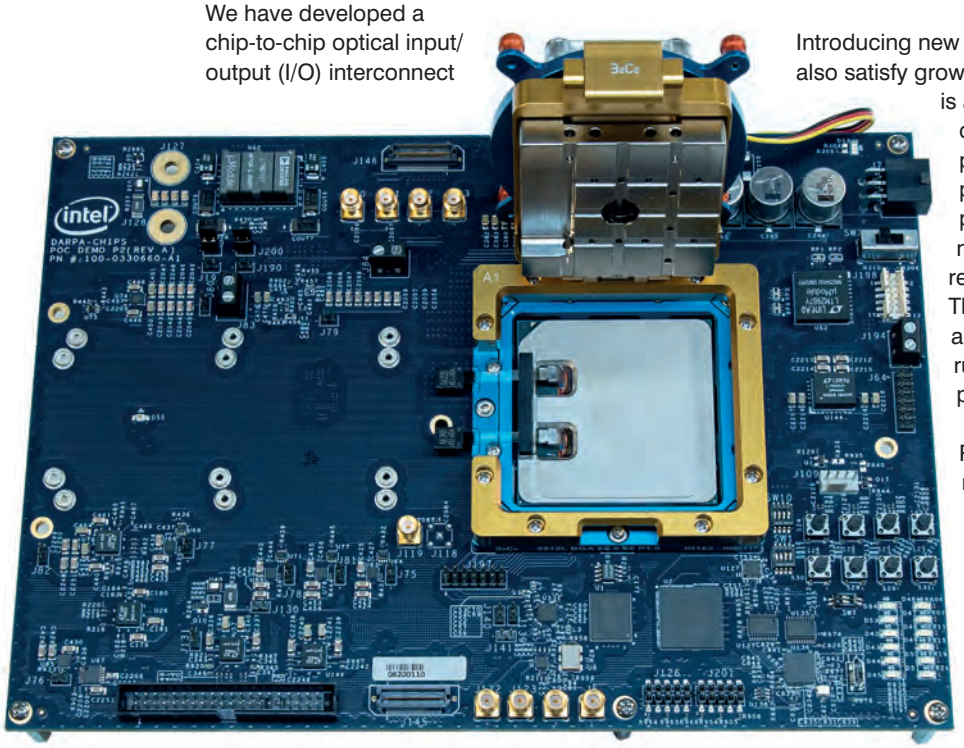
BY VLADIMIR STOJANOVIC FROM AYAR LABS

DATA DASHES through today's optical fibre system networks before it slows to a crawl at copper interconnects. These bottlenecks occur at copper pins and wires on circuit boards, where electrons transmit data at far lower speeds. So great are these delays that there will come a time when copper interconnects will have to be replaced by optical signalling.

Offering a universal solution to this issue is our team from Ayar Labs of Emeryville, CA. Founded in 2015 as a spin-out of three universities – Massachusetts Institute of Technology; University of California, Berkeley; and University of Colorado, Boulder – we are renowned for our pioneering work in micro-ring chip architectures.

We have developed a chip-to-chip optical input/output (I/O) interconnect technology that addresses several weakness associated with electrical interconnects and their scaling limitations. We tackle weaknesses associated with signalling speeds and pin count, which both apply the brakes to electrical I/O connections, and power consumption that is increasing at an unsustainable rate.

The latter concern should not be taken lightly, as it will not be long before the power drawn by the off-chip I/O will account for almost all the power consumption of the package. When this occurs, it will be infeasible to use electrical I/O interconnects, which are primarily made of copper. By then, there will need to have been a shift to chip-to-chip communications based on photonics, a technology that will eliminate electrical I/O bottlenecks.



Introducing new photonic I/O architectures will also satisfy growing throughput demands. There is an emergence of heterogeneous computing, involving central processing units (CPUs), graphic processing units (GPUs), field-programmable gate arrays (FPGAs), neural network accelerators, and resource pooling on the memory side. This trend demands more I/O at the application level, while electrical I/O is running into pin count, signalling and power limitations.

Providing an impetus to act sooner rather than later, the penalties for leaving the chip, package, and board are on the up (Figure 1). This begs the question: will the 112-Gbit/s serializer/deserializer be the last long-range electrical I/O solution? In field deployments, system integrators are already seeing the limitations of 112-Gbit/s long-

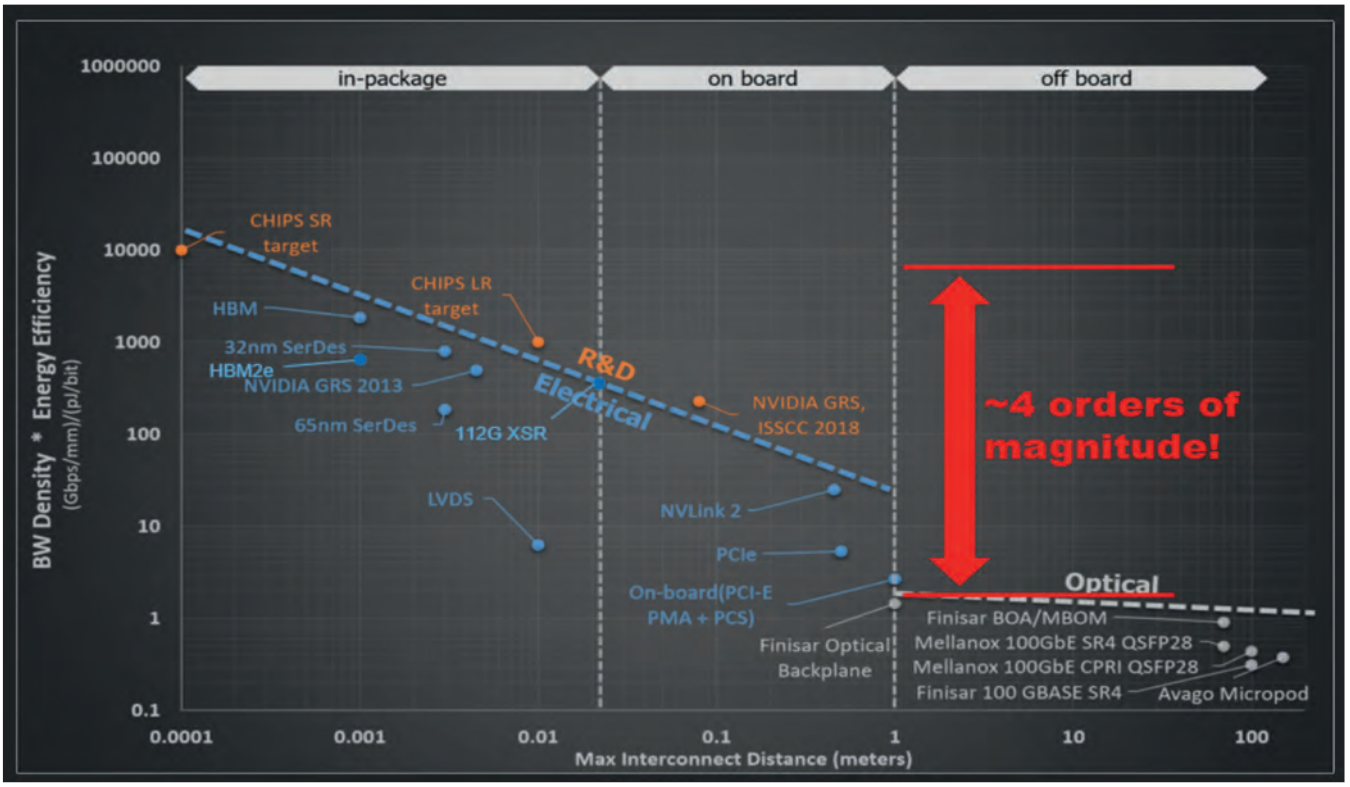


Figure 1. Large penalties will be incurred for leaving the chip, package, and board (Source: Gordon Keeler, DARPA MTO, ERI Summit 2019).

range electrical connections – they are incapable of spanning the signalling lengths required for off-board, rack-scale communication.

To evaluate the performance of the I/O technologies, we use a figure-of-merit involving quite a few terms. It considers the bandwidth density from the edge of the I/O solution, multiplied by its associated energy efficiency. This provides a yardstick that captures the Gbit/s per millimetre per pJ/bit, as a function of distance. When crossing the boundaries from package to board with I/O technologies, this metric plummets – there is a gap of about four orders of magnitude between in-package interconnect solutions and state-of-the-art optical solutions that provide off-board connectivity.

Into this challenging space comes our new optical I/O technology. It delivers a universal I/O solution that provides off-package communication at the bandwidth density and energy cost of in-package electrical incumbents.

An in-package solution

To pull off an optical I/O, certain requirements must be fulfilled (see Figure 2). We meet them with our own optical I/O system architecture. This is a chiplet-based solution that is co-packaged directly with the host system-on-chip (SOC) within a multichip module (MCM) package. By incorporating a monolithic electronic-photonic CMOS chiplet, which we call TeraPHY, we realise a flexible electrical I/O interface adapted to the host SOC, whether the geometry is wide parallel or high-speed serial. Adopting this approach offers flexibility, giving a choice between a silicon interposer and an organic substrate for the package.

One of the merits of our single-chip solution is that it enters a manufacturing ecosystem already established for MCMs. With our architecture, we keep the laser supply outside the module. This simplifies packaging, improves laser reliability, and alleviates issues related to the operational temperature mismatch of SOC packages and laser optical supplies. Due to these advantages, we realise further integration of lasers into a multi-port, multi-wavelength laser module solution, which we refer to as SuperNova.

Several system and technology requirements have to be met for in-package optical I/O to become a reality (see Figure 3). At the system level, the optical I/O requires high-density optical devices and circuits capable of fulfilling the high-bandwidth density demands of future SOCs and applications.

To ensure success, it is critical to draw on existing CMOS processes and manufacturing infrastructure, while complying with I/O standards. And, perhaps most importantly, production must leverage scalable, high-volume manufacturing of the semiconductor technology.

We meet these requirements with wavelength-division-multiplexed (WDM) links that support multiple wavelengths per fibre and allow scaling of the data rate to meet the bandwidth density requirements of future applications. We use closely spaced wavelengths – they are separated by a few hundred GHz – running concurrently on the same fibre. Transmitters and

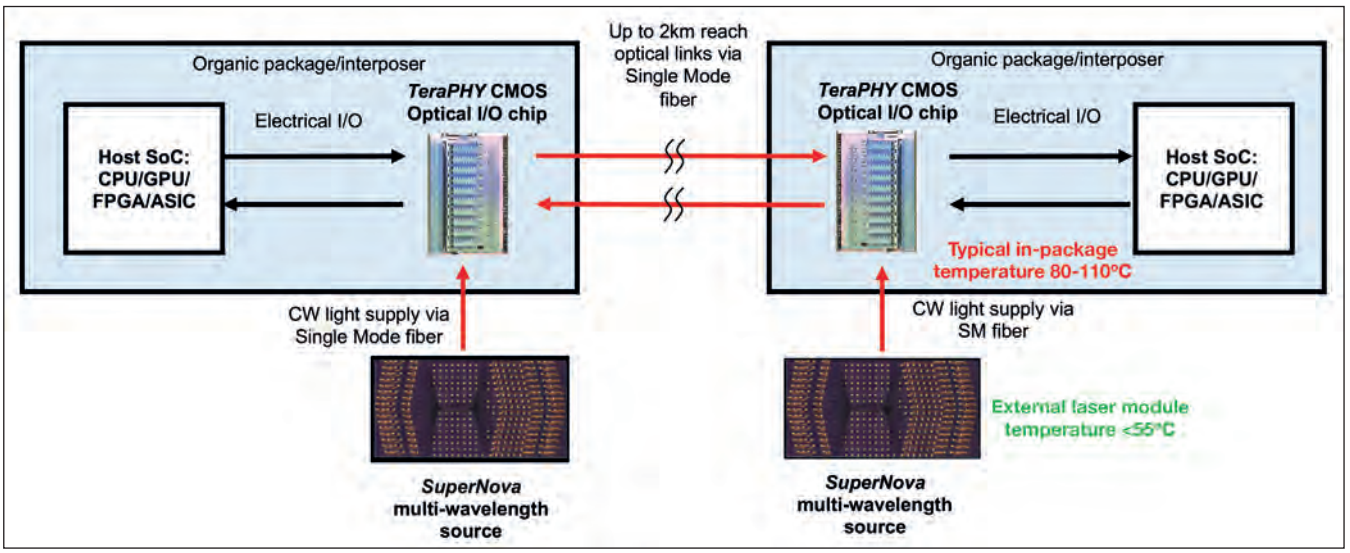


Figure 2. Ayar Labs' in-package optical I/O system architecture (Source: Ayar Labs).

receivers modulate/receive each wavelength separately.

By leveraging monolithic integration and the CMOS process, we create a chiplet-driven technology with tight integration of electronics and photonics while improving bandwidth density and energy metrics. Finally, our monolithic approach taps into the ecosystem of CMOS foundries and scalable high-volume packaging manufacturing of multichip modules. Thanks to this, we have created a compatible solution for advanced packaging and fibre attach.

Optimising the optical architecture

At the heart of our optical I/O architecture lies micro-ring modulator and WDM technology (see Figure 4). At its crux is an off-chip continuous-wave laser, based on non-proprietary standards. This emitter is driven by the Continuous-Wave WDM Multi Source Agreement (CW-WDM MSA), which provides optical power in one or more wavelengths to the TeraPHY chip. Light enters this chip through a coupler and then travels along it in an optical waveguide. The light encounters a micro-ring modulator, which converts data from an electrical domain to the optical domain.

Our micro-ring has a very narrow resonance, typically just 20-40 GHz that is repeated at a much larger period, such as 3.2 THz. With these conditions the micro-ring is wavelength selective. This allows the micro-ring modulator to act as both a modulator and a wavelength division multiplexer, enabling the addition of more wavelengths to the same fibre/waveguide. By making our micro-ring modulators out of silicon, we are employing the same material used to produce all the transistors and optics on the chip.

Output from our chiplets is coupled to the fibre and sent to the receiver chips. Here, micro-ring detectors convert data from the optical domain to the electrical domain. Micro-ring detectors actually perform a dual role, combining the tasks of detector with that of wavelength-division demultiplexer, picking the selected modulated wavelength for the receiver.

We can increase the bandwidth density of our links, alongside the overall throughput of the fibre, by adding wavelengths to the fibre. It's an improvement that we accomplish without increasing strain on backend electronics. Using cascaded micro-rings as independent communication channels, we realise up to

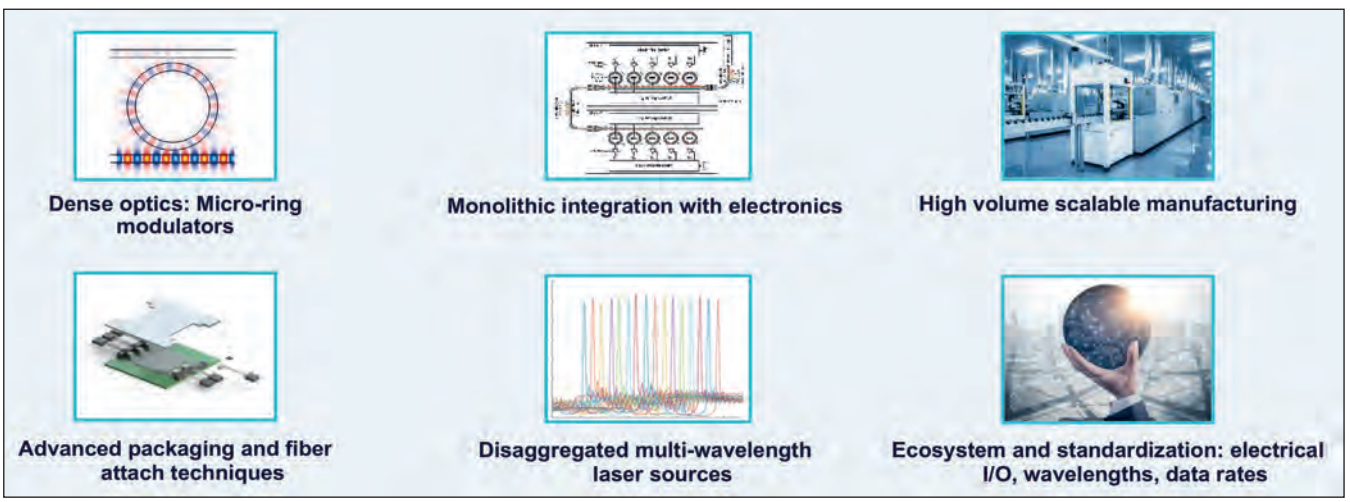


Figure 3. Six areas must be addressed to make in-package optical I/O a reality (Source: Ayar Labs).

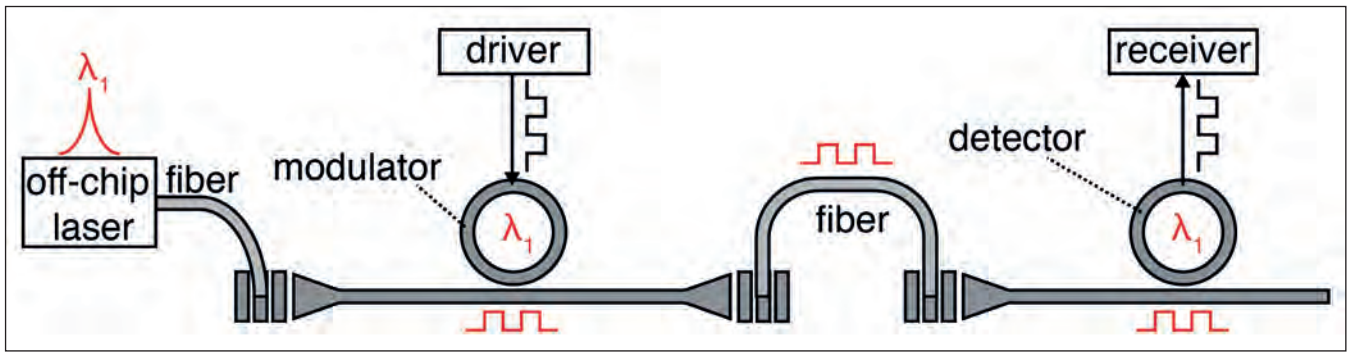


Figure 4. The TeraPHY optical I/O architecture, centred on a micro-ring modulator and WDM (Source: Ayar Labs).

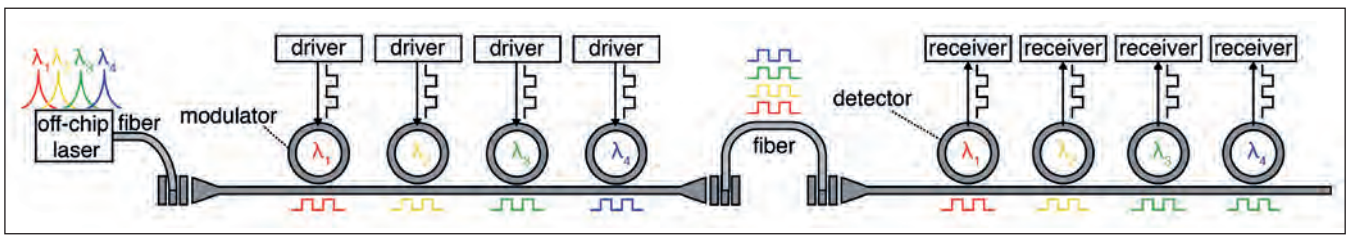


Figure 5. Wavelengths can be added to the fibre – without increasing the strain on the backend electronics – to improve energy-efficiency, bandwidth density and overall throughput of the fibre (Source: Ayar Labs).

64 micro-rings per fibre. This yields a technology that provides up to 6 to 8 Tbit/s per fibre (see Figure 5).

Drawing on this development and others, we have constructed a complete WDM link system, formed by integrating electronic and photonic components. Electronics modulates and receives the data and controls micro-ring resonances through thermal tuning and wavelength locking (see Figure 6). With our technology, transmitter ring modulator resonances are locked to incoming laser wavelengths, prior to locking of the receiver. Working together, locking loops track local and global temperature fluctuations while compensating for process-induced wavelength grid non-idealities that occur in the laser, transmit and receive chips.

Our interconnects excel in bandwidth density and energy efficiency, thanks to miniaturisation of the micro-ring devices, which are integrated with CMOS transistors. The link architecture has enabled us to create TeraPHY, which is essentially a chiplet that provides Tbit/s optical connectivity and offers an alternative to electrical serializer/deserializer chiplets.

The main features of our demonstration chiplet are: a 24 channel advanced interface bus (AIB), providing a total data bandwidth of 906 Gbit/s; ten photonics Tx/Rx macro pairs, configurable to 125 Gbit/s to 256 Gbit/s per macro that equates to 1.28 Tbit/s to 2.56 Tbit/s per chip; a non-return to zero modulation format for the optical channel, eliminating the need for forward-error correction; a reach of up to 2 km; and an all-inclusive estimated energy efficiency of less than 5 pJ/bit.

Our TeraPHY chiplet operates like an electrical chip. To ensure this, we use a variety of pitch bumps – there is a combination of a tight 55 μm-pitch for the AIB interface standard, and a mixed pitch, because our chiplet uses a variant of an embedded multi-die silicon interconnect bridge (see Figure 7). With this arrangement, the main die is connected to others via a piece of silicon. It has been embedded within an organic substrate to provide fine-line connectivity using a 55 μm-pitch for the bump between the die.

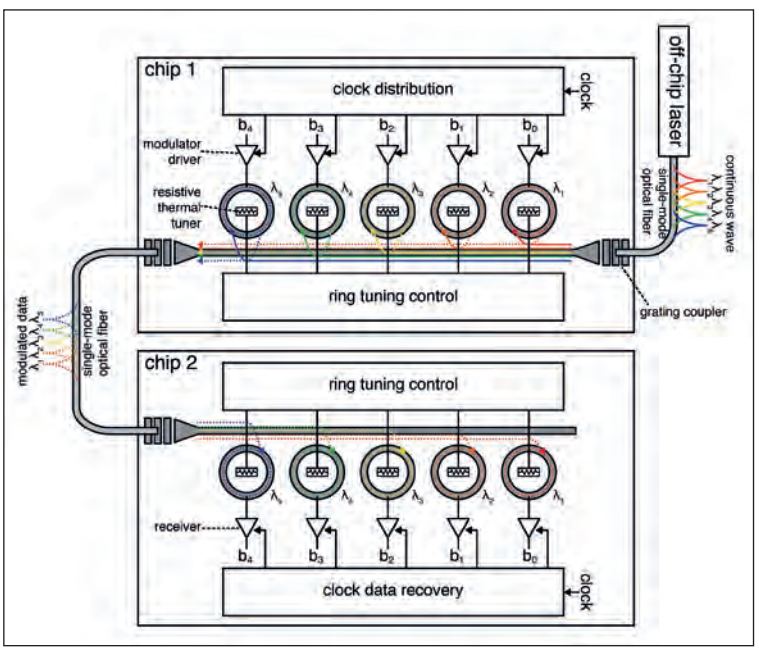


Figure 6. A complete WDM link system that integrates electronics with photonics components (Source: Ayar Labs).

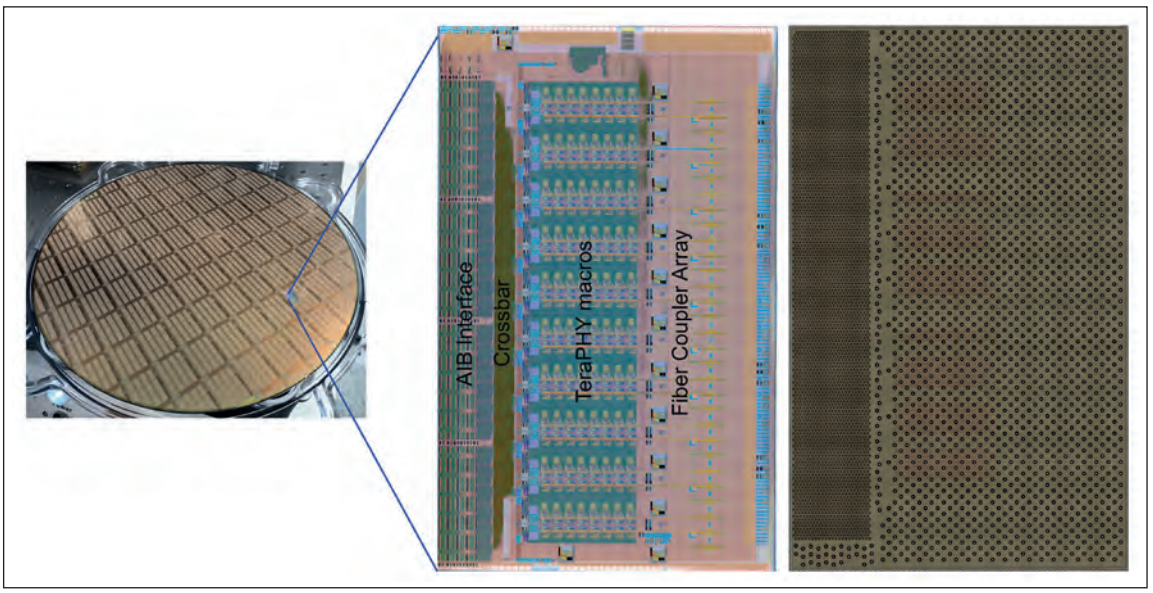


Figure 7. The TeraPHY chiplet with mixed-pitch bumps (Source: Ayar Labs).

This enables fine-pitch 2.5D-type packaging without having to use a silicon interposer. Instead of that we can use an organic substrate, which provides greater flexibility in terms of area and yield.

A major selling point of our in-package chiplet is that it provides a universal off-package interconnect solution for any SOC, including FPGAs, CPUs, GPUs, tensor processing units and switches. Applications include: radar; disaggregated resources for data and high-performance computing racks; 5G connections between front-panel RFIC array and back-end digital beam-forming processors; and artificial intelligence compute scale out, such as GPU to GPU, TPU to TPU, FPGA to FPGA, and CPU to GPU.

Delivering demonstrations

Back in March 2020 we provided a live demonstration of our chiplet technology. Working in partnership with Intel under the US Defense Advanced Research Projects Agency's (DARPA) Photonics in the Package for Extreme Scalability (PIPES) programme, we replaced the traditional electrical I/O of a state-of-the-art FPGA with optical signalling interfaces.

This effort, which drew on Intel's advanced packaging and interconnect technology, involved the integration of TeraPHY optical I/O chiplets and an Intel FPGA core within a single package to create a MCM with in-package optics (see Figure 8). This MCM substantially improves interconnect reach, efficiency, and latency – and ultimately enables high-speed data links featuring single-mode optical lasers coming directly from the FPGA.

The optical waveguides on our chiplet, which are patterned monolithically into the silicon, are the optical equivalents of copper wires. When we bring two waveguides in close proximity, we can transfer photons and power from one waveguide to another to create a coupler. Within the coupler, a 10 μm-diameter micro-ring resonator electrically modulates

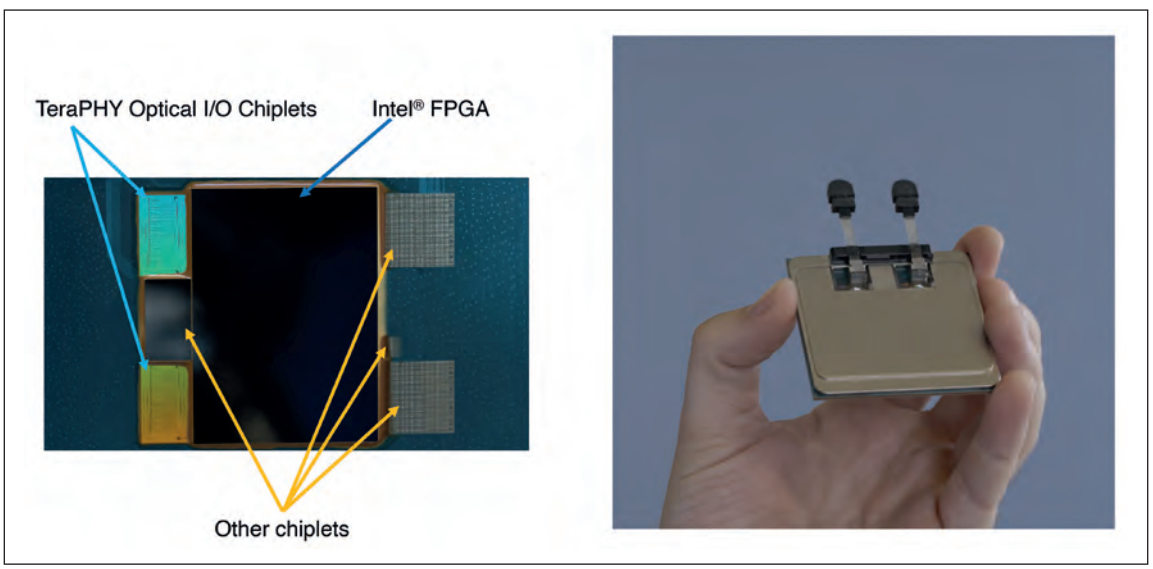


Figure 8. Multi-chip package assembly with in-package optics (Source: Ayar Labs).

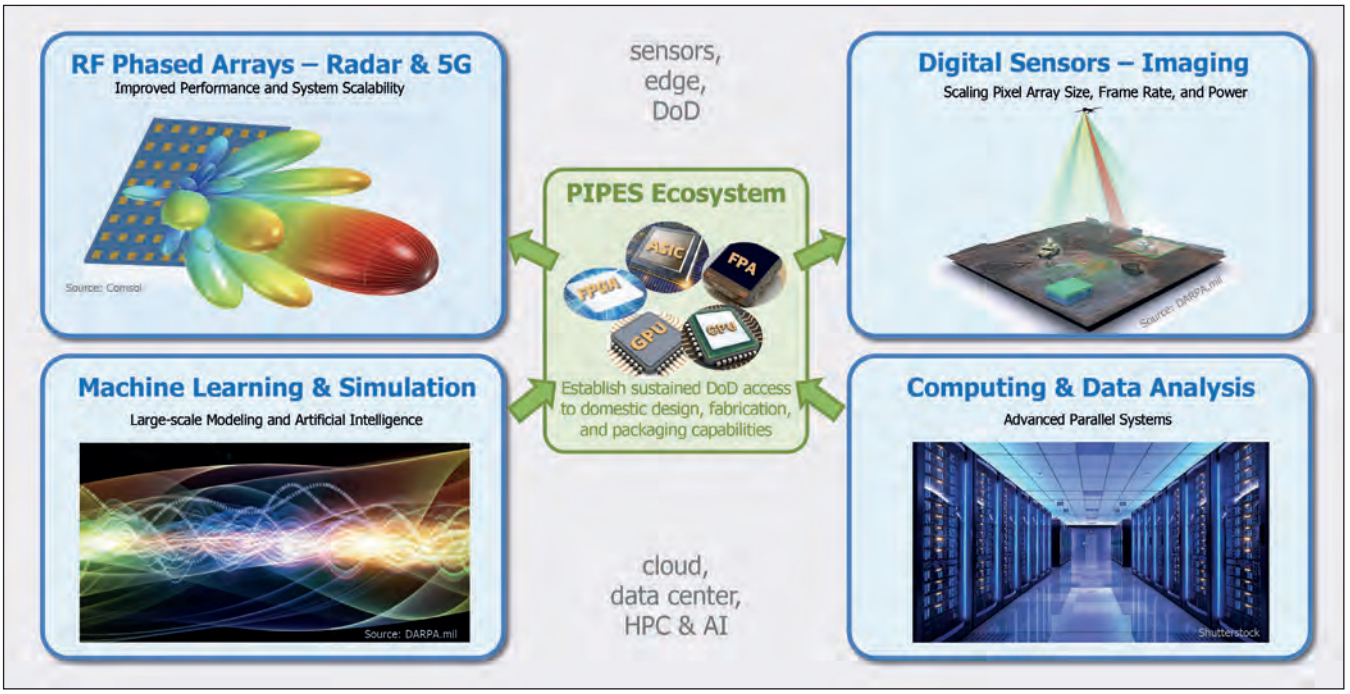


Figure 9. Application areas for advanced integrated circuits with photonic interfaces (Source: Gordon Keeler, DARPA, ERI Summit 2020).

the light's phase and controls its direction. Light is either let through, directed to a drop port, or allowed to dissipate inside the micro-ring.

We use GlobalFoundries' 45 nm-platform for CMOS chip manufacturing. This supports the construction of our co-packaged chiplet that provides an I/O bandwidth of 2 Tbit/s, realised at a small fraction of the power compared with an electrical I/O.

DARPA's PIPES programme is targeting development of advanced integrated circuits that feature photonic interfaces capable of driving bandwidths greater than 100 Tbit/s I/O per package at energies below 1 pJ per bit. Deploying interfaces with this level of performance in FPGAs will improve high-performance computing, AI, large-scale emulation, and US Department of Defense capabilities, such as radio-frequency arrays, advanced radar, and 5G (see Figure 9).

Our demo featured eight wavelength-division-multiplexed channels per macro, using I/O data rates of 16 Gbit/s/wavelength across four optical macros on a single chip. This provided connectivity at 512 Gbit/s.

The demonstration involved low-power signalling standards and chiplet packaging processes developed by Intel for another DARPA programme. This work also used Intel's common interface standard, known as AIB. It is a publicly available, open interface standard that enables us to integrate the MCM and in-package optics.

In production, our single chiplet is expected to reach up to 2 Tbit/s I/O over 64 wavelength channels, at 32 Gbit/s per wavelength. There is no need for forward-error correction, and latency is less than 10 ns. Our chiplet is also designed to work with an off-chip multi-wavelength continuous-wave laser source and integrate with any type of partner system on package – this could be a CPU, GPU, ASIC, or FPGA – to connect switches, servers, and cards over distances up to 2 km.

Beyond our work with DARPA and Intel, we are continuing to advance our in-package optical I/O technology. In a single-die package demonstration this July we took another step forward, highlighting that our micro-ring-based WDM can meet the requirements for next-generation high-performance chip-to-chip I/O. This effort showcased 25 Gbit/s transmitters and 25 Gbit/s receivers, with noteworthy accomplishments including an aggregate bandwidth of 800 Gbit/s on the transmitter side and a bit error rate below 1×10^{-12} on the receiver side (see Figure 10). Combined, energy efficiency came in at just 4.91 pJ/bit.

This demonstration is a milestone on our path towards showcasing the full capabilities of our chiplet. By running each wavelength channel at 32 Gbit/s, our single chiplet can deliver an aggregate bandwidth of 2 Tbit/s for transmit and receive.

We plan to roll out a 2 Tbit/s TeraPHY chiplet. But that is just the beginning of the roadmap for our technology – we will trailblaze a path to 32 Tbit/s per chip, realised at just 1 pJ per bit.

The road ahead

By producing our devices using monolithic in-package optics, we are in a unique position to leverage both the existing chiplet ecosystem and the high-volume manufacturing of MCM assembly approaches. Thanks to the use of the same package for the optics, we

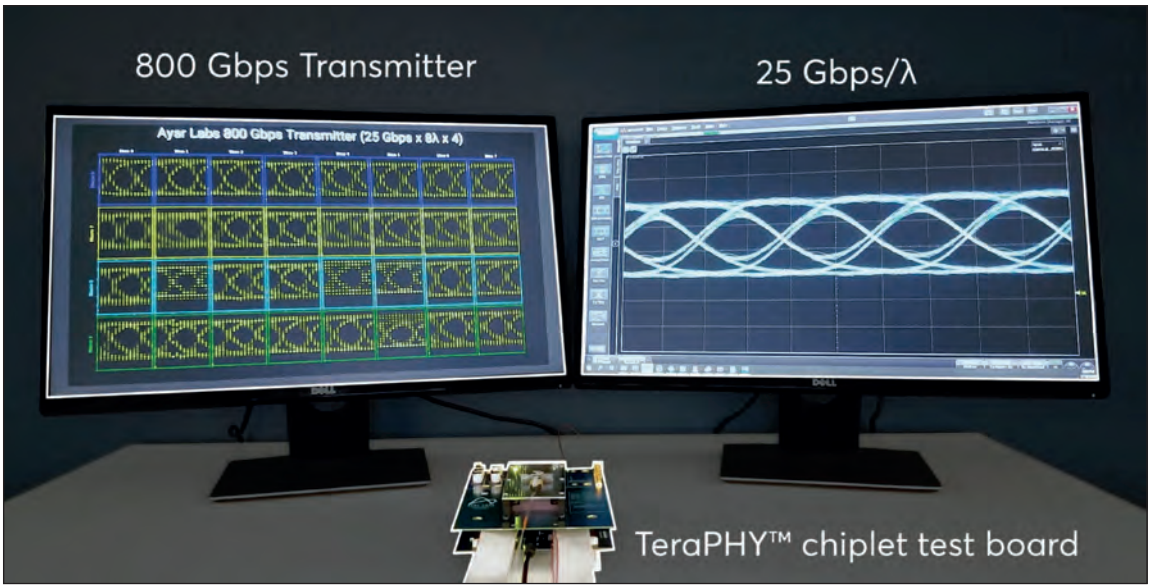


Figure 10. In a single-die package demo, Ayar Labs demonstrated 25 Gbit/s transmitters and 25 Gbit/s receivers with an aggregate bandwidth of 800 Gbit/s on the transmitter side (Source: Ayar Labs).

are not shackled by the traditional distance trade-off in energy efficiency and bandwidth density. This opens the door to new high-performance computer architectures with off-package communication at the cost, energy, and bandwidth density of in-package interconnects.

It is worth emphasizing that the key to realising this chip, featuring integrated photonics and electronics on the same die, is the monolithic integration of photonic components. This approach bore much fruit in the university research that laid the foundations for our company, and through further development, it is now allowing us to make further breakthroughs. We are now refining a technology where photonics components are directly integrated with advanced transistors in a 45 nm process to create complex electronic-photonic systems, such as WDM links.

Using this approach, we can create single CMOS wafers that contain chiplets that integrate photonic components with transistors to support a wide variety of electrical interfaces.

Compare our approach with that of our peers and you'll see that many of the SOC manufacturers have come up with MCM technologies that are driven by the need to realise mixed-die functions on complex applications, such as GPU, CPU, memory, or I/O. One major drawback of that type of approach is that these functions require diverse processes and process nodes – whether it is a DRAM node or a CMOS node in 10 nm or 7 nm technology, and the complexity of MCM assembly is more cost-effective than the development of a process that encompasses all the features required by all the functions. Additionally, even for the same functions, the MCM approach enables significant cost reduction through yield improvement by breaking-up a large die (e.g. 64 core microprocessor) into smaller dies that yield better (e.g. eight 8-core dies).

We are now starting to sample our first TeraPHY chiplet generation with select partners. This is the beginning of a journey, which will continue to new generations of the chiplet. We plan to advance our technology with electrical interface variants that address different host SoC needs and packaging scenarios, and deliver greater throughput by increasing the number of wavelengths and the data rate per wavelength. Target applications exist within artificial intelligence, supercomputing, data centres, aerospace, defence, telecom, and eventually autonomous vehicles.

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the US Government.

Further reading

Ayar Labs Technical Brief: Optical I/O Chiplets Eliminate Bottlenecks to Unleash Innovation (see https://ayarlabs.com/technical-brief-optical-i-o-chiplets-eliminate-bottlenecks-to-unleash-innovation/)

Paradigm Change: Reinventing HPC Architectures with In-Package Optical I/O (see https://ayarlabs.com/paradigm-change-reinventing-hpc-architectures-with-in-package-optical-i-o/)

TeraPHY: A Chiplet Technology for Low-Power, High-Bandwidth In-Package Optical I/O (see https://ayarlabs.com/teraphy-a-chiplet-technology-for-low-power-high-bandwidth-in-package-optical-i-o/

TeraPHY: An O-band WDM Electro-optic Platform for Low Power, Terabit/s Optical I/O (see https://ayarlabs.com/download/teraphy-an-o-band-wdm-electro-optic-platform-for-low-power-terabit-s-optical-i-o/)

Flying high with **CPV**

Operating at almost 100 suns, vast arrays of five-junction micro-concentrator cells promise to set a new benchmark for extra-terrestrial power

BY MATHEW LUMB FROM THE GEORGE WASHINGTON UNIVERSITY

WHILE CONCENTRATOR PHOTOVOLTAICS (CPV) is better known for its potential to deliver outstanding levels of power in sunny climes, it also has a number of compelling performance attributes for generating energy in space. Operating in the range of just ten to a hundred suns, CPV installed on-board a satellite or a space station has the potential to combine a remarkably high specific power, judged in terms of the Watts per kilogram, with a low cost-per-Watt and a high volumetric power density – that is, many Watts per cubic metre.

Thanks to these attractive assets, this form of power generation promises to offset the high launch costs for space deployment. It is well suited to this environment, because the use of a low level of concentration helps to maintain manageable cell operating temperatures and wide optical acceptance angles. And by incorporating focusing optics, there is a tremendous reduction in the impact of one of the harshest environmental aspects of space – particle irradiation. In a concentrator array, lenses made from radiation-hardened glass dramatically slow the degradation of photovoltaics by shielding the epitaxial layers from damaging radiation.

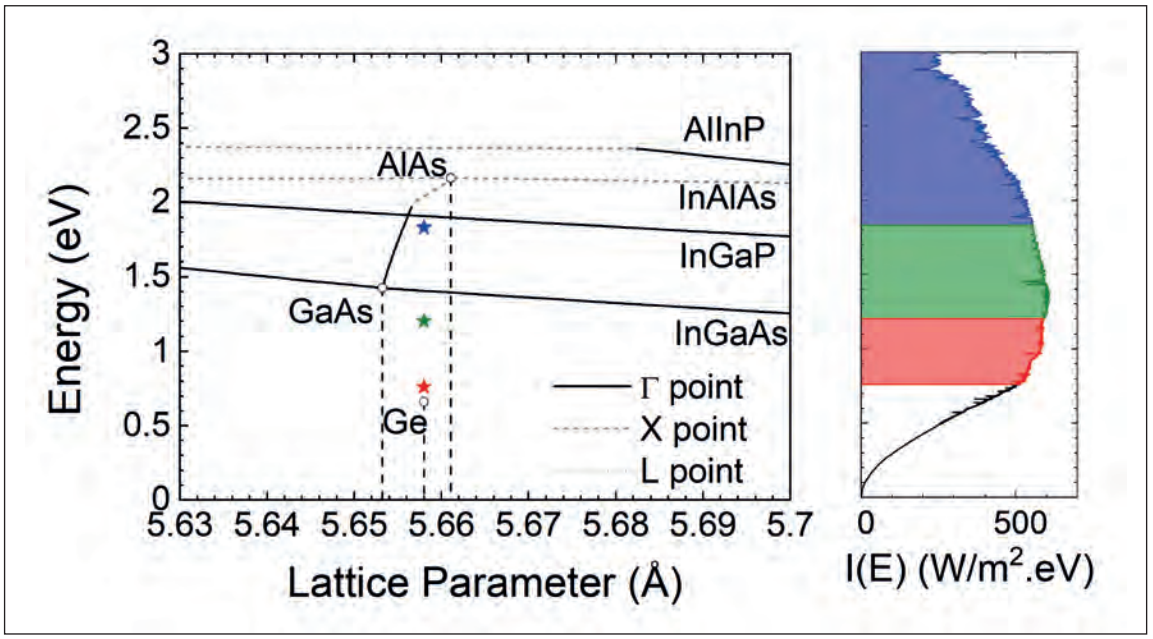


Figure 1. The ideal bandgaps for conversion of AM0 illumination from the detailed balance limit in a triple-junction solar cell, compared with available bandgaps of III-As and III-P alloys on germanium.

A particularly promising form of CPV uses solar cells with dimensions typically just 100-800 μm per side. When well designed, these microcells spread current efficiently across the cell aperture, eliminating the need for metal grid fingers. Another merit of these microcells is that they simplify thermal management, because their diminished dimensions enable effective heat dissipation along interconnect traces and into the backplane, lowering the temperature of these devices and increasing their efficiency. Microcells also permit miniaturised optics, which can be very lightweight and low in profile. Finally, the cells can be spaced close together to realise a micro-concentrator with a very high areal packing fraction and essentially no unusable area. Lengthening cell spacing also reduces the risk of arcing between adjacent cells, while providing a very high degree of flexibility in wiring configurations, which accommodates a large range of output voltages and currents while providing high tolerance to defects.

Building on terrestrial success

Holding the record for the highest efficiency of all photovoltaic technologies are terrestrial concentrator systems. These are usually built around extremely high-performance, monolithic multi-junction solar cells. In these devices the solar spectrum is divided between the sub-cells, ideally in a manner that ensures a similar photocurrent from each, because this maximises efficiency.

For many years the workhorse of space photovoltaics has been a triple-junction cell based on the combination of InGaP, InGaAs and germanium. This architecture, closely related to a terrestrial CPV cell, is generally deployed without concentration thanks to the favourable economics of space power that are governed by high launch costs.

On satellites, power tends to be produced by cells with a footprint of 25 cm^2 to 80 cm^2. Unfortunately, the

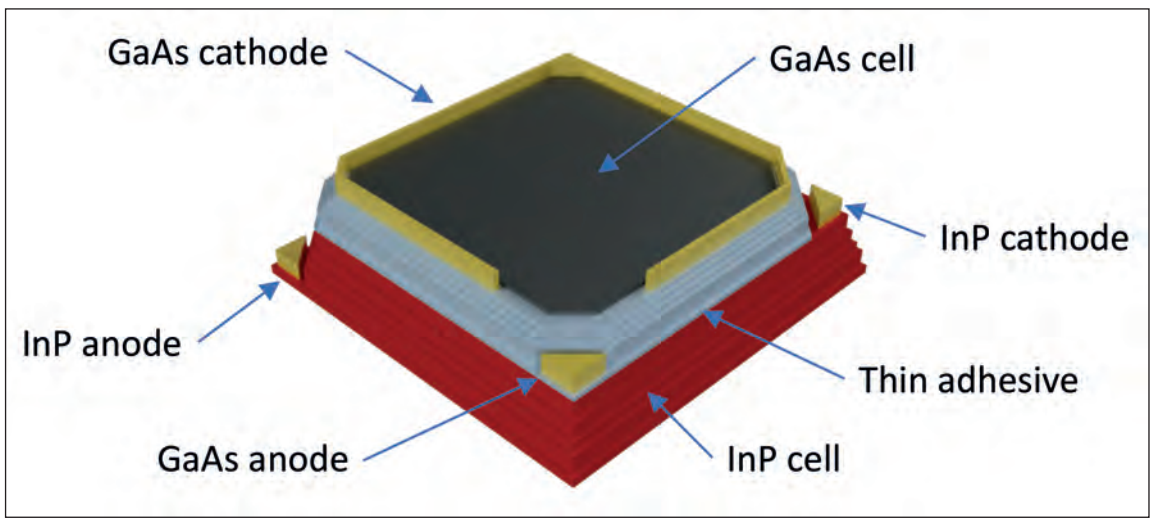


Figure 2. A stacked micro CPV cell, formed from separate GaAs and InP-based multi-junction solar cells, can form a four-terminal device.

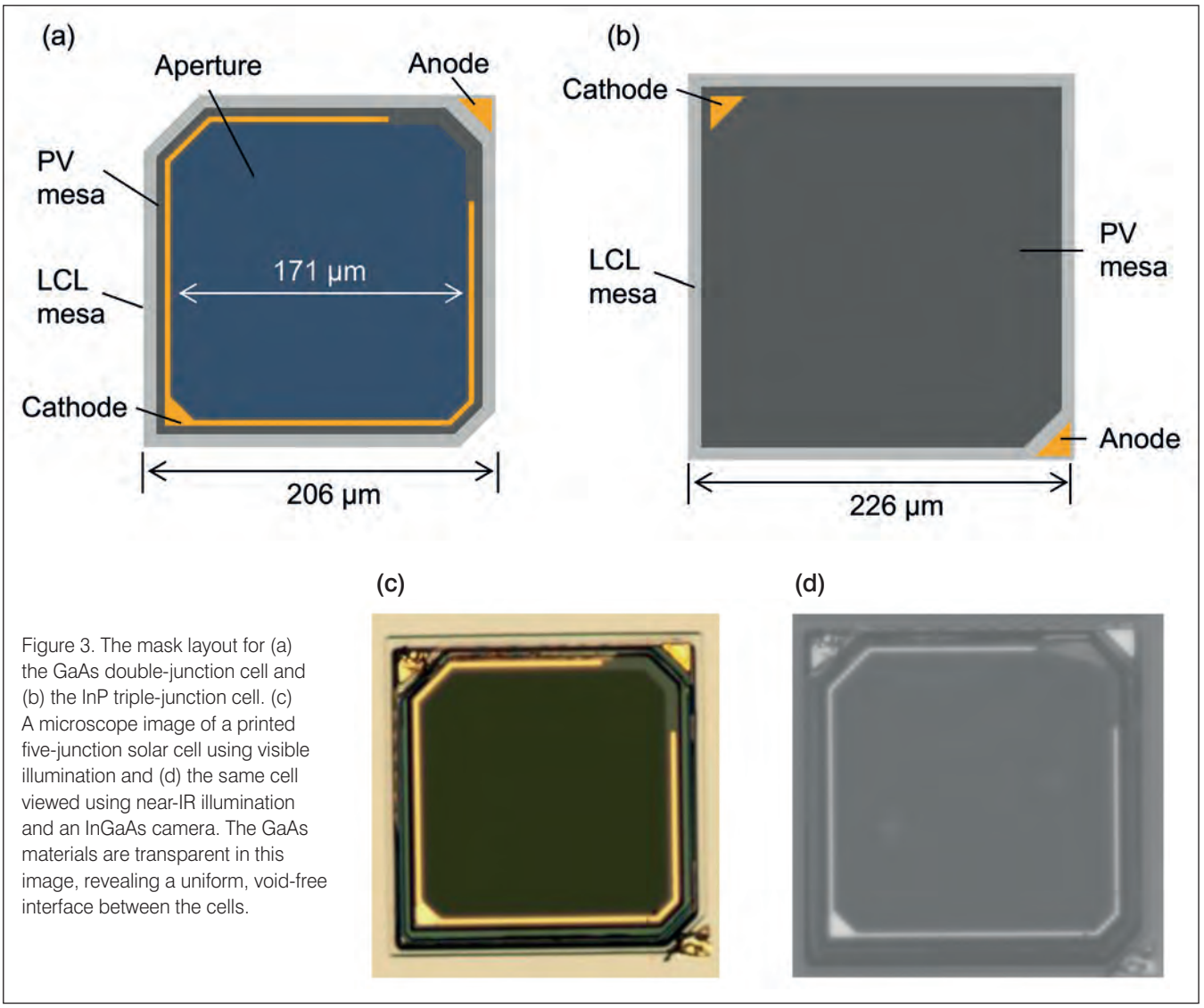


Figure 3. The mask layout for (a) the GaAs double-junction cell and (b) the InP triple-junction cell. (c) A microscope image of a printed five-junction solar cell using visible illumination and (d) the same cell viewed using near-IR illumination and an InGaAs camera. The GaAs materials are transparent in this image, revealing a uniform, void-free interface between the cells.

suite of III-V alloys available on the lattice constant for germanium – the incumbent substrate for triple-junction space cells – fails to provide the ideal bandgaps for spectral splitting (see Figure 1). This has motivated researchers in academia and industry to develop alternative architectures that overcome these limitations. One material with much promise is the dilute nitride InGaAsN – it offers direct-bandgap alloys in the technologically important range of 1.4-0.8 eV that can be lattice-matched to both GaAs and germanium. Strain-balanced quantum wells also offer similar tunability, albeit over a smaller range.

Yet another option is metamorphic epitaxy, which underpins the record-breaking six-junction devices recently developed by scientists at NREL. However, with this class of device, it is very challenging to maintain high crystal quality and a good manufacturing yield.

Today, there are a handful of commercial suppliers of III-V multi-junction solar cells. State of the art efficiencies range from roughly 29 percent for a basic germanium-based triple-junction space cell to around 32 percent for leading metamorphic devices. These efficiencies are for the solar spectrum received outside the Earth's atmosphere, a condition known as air-mass zero, or AM0.

Some of the highest-ever recorded efficiencies for multi-junction solar cells have involved the integration of materials grown on different substrates, such as GaAs, InP and GaSb. Adopting this approach allows III-Vs, which are lattice-matched to their native substrates using close to ideal bandgaps, to be fused into single devices.

Different materials can be united with wafer-bonded approaches. In the devices that result, current conducts across the heterointerface, with each subcell ideally generating a similar current. However, manufacturing devices with this approach is not easy, as high yield, low-resistance wafer bonding is notoriously tricky.

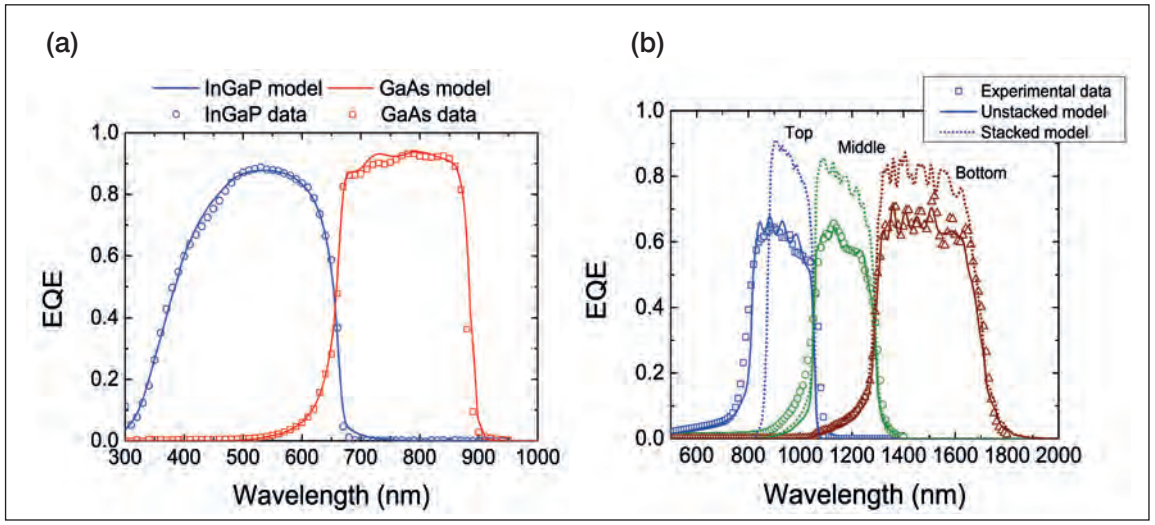


Figure 4. (a) Measured and simulated external quantum efficiency (EQE) for the GaAs double-junction cell. (b) Measured and simulated EQE spectra for the InP triple-junction cell. The implied EQE after stacking is shown by the dotted lines.

An interesting alternative is the heterogeneous integration of electrically isolated devices to form a four-terminal structure. This approach offers much freedom, as current-matching constraints are restricted to only subcells within the separate devices. Eliminating the requirement for electrical conductivity across the heterointerface therefore creates more flexibility in material choices.

Printing cells

Another method for realising heterogeneous integration with a variety of micro-CPV cell material combinations is the highly parallel assembly technique known as micro-transfer printing. This approach for heterogeneous integration, pioneered by researchers at the University of Illinois at Urbana Champaign, has been advanced by our team, which is a collaboration between researchers at George Washington University, NRL, Semprius, X-Celeprint, Veeco, Northwestern, the University of Illinois at Urbana-Champaign and MIT. Our capabilities, refined over several years, include the development of a micro-transfer printing process for placing fully-functional, GaAs-based PV dice (known as chiplets) on top of InP or GaSb-based cousins to make a four-terminal device (see Figure 2).

The printing process begins by using a selective chemical etch to release chiplets from their native substrate, whilst they are temporarily tethered in place with a photoresist. An elastomer stamp picks up the chiplets before adhering them to a non-native substrate, in this case another micro-CPV device. An extremely thin polymer adhesive, less than 20 nm-thick, forms a permanent bond.

We use a tool developed by X-Celeprint to carry out the fully automated printing process. This partner has commercialised transfer printing technology, drawing on experience from a long-time collaboration with former micro-CPV company Semprius. One of the primary merits of the printing process is that it liberates PV devices from their expensive growth substrates, which can be reused.

Our latest solar cells, incorporating both GaAs-based and InP-based devices, were designed using an analytical drift-diffusion model incorporating photon recycling and coherent optical effects. Using a commercial Veeco K475i MOCVD tool we fabricated both devices, presenting results at this year's SPIE Photonics West conference in San Francisco.

The GaAs part of the cell consists of a pair of junctions, made from InGaP and GaAs, separated by an AlGaAs/GaAs tunnel junction. At the bottom of the device we include an AlInP epitaxial release layer. Using a highly selective etch, we remove this layer and release die from their native substrates prior to transfer printing. We produce square-shaped solar cells with sides of around 200 μm, using dry etching in an inductively coupled plasma tool to define mesa dimensions. The front metal pattern forms a roughly square aperture with a width of 171 μm (see Figure 3 (a) and (b)). We improve the efficiency of the cell by applying a three-layer $SiO_2/Si_3N_4/TiO_2$ anti-reflection coating, and we increase the device's robustness by passivation. This involves depositing Si_3N_4/SiO_2 over the sidewalls.

The InP part of the cell is formed from three *n*-on-*p* junctions. The top two junctions consist of lattice-matched layers of InGaAsP, with bandgaps of 1.18 eV and 0.97 eV. The bottom junction is made from InGaAs with a band gap of 0.74 eV. Separating the junctions are p^{++} InGaAs/n^{++} InP tunnel junctions. Dissimilar to the GaAs cells, the InP triple-junction cell does not contain a sacrificial layer for epitaxial lift-off. Due to this, all our measurements are performed on native InP substrates. Note that highly selective etch combinations do exist in the InP family, so there is no barrier to producing printable InP-based triple-junction cells using the same process employed for making the GaAs cell.

Scrutinising our fabrication process using visible and near infrared microscopy reveals precise alignment with a void-free interface between the cells (see Figure

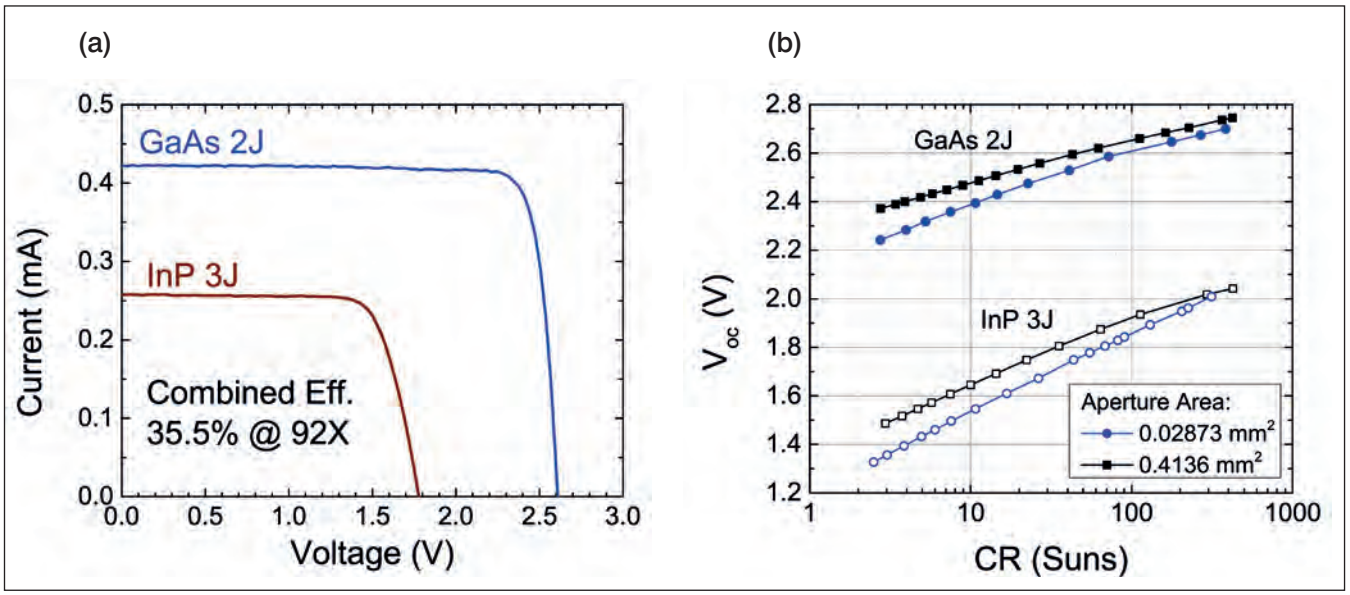


Figure 5. (a) Light current-voltage (I-V) curves for the stacked GaAs- and InP-based multi-junctions, which give a combined efficiency of 35.5 percent under simulated AM0 illumination. (b) Measured open-circuit voltage (Voc) for microcells with different perimeter-to-area ratios, highlighting the losses at low concentration due to perimeter recombination.

3(c) and (d)). Measurements of the external quantum efficiency curve for our devices, using larger area cells from the same wafer, are in good agreement with our simulations (see Figure 4).

Obtaining a reliable figure for the external quantum efficiency of the stacked cells is difficult, due to significant leakage produced by the microcells at the very low light levels employed for this measurement. Our workaround is to deduce the external quantum efficiency of our stacked devices by correcting the experimental data for the transmission through the GaAs heterostructure. While this is not a direct measurement of the external quantum efficiency, it can accurately reproduce the measured light-current-voltage characteristics for stacked and unstacked devices. As expected, the external quantum efficiency of our InP-based cell increases after stacking, because it benefits from the antireflection coating on the GaAs cell. The light that reaches the underlying InP cell has been filtered by absorption in the GaAs layers, which have a cut-off at roughly 870 nm.

We have measured the photocurrents of all five subcells. Values for InGaP and GaAs in the GaAs-based devices are 16.9 mA/cm^2 and 15.8 mA/cm^2, while the top, middle and bottom cells for the InP-based device recorded current densities of 9.5 mA/cm^2, 9.9 mA/cm^2 and 12.5 mA/cm^2, respectively.

To characterise the light, current and voltage performance of our cells, we have used a collimated AM0 solar simulator with a plano-convex lens to focus the light. We determined the incident intensity of the simulated solar spectrum using the ratio of the measured short-circuit current to the equivalent value for 1 sun, as determined from external quantum efficiency curves combined with the AM0 spectrum. This methodology revealed a peak four-terminal efficiency of 35.5 percent at 92 suns.

Greater insight into the performance of our five-junction cell is provided by the current-voltage characteristics of separate InP and GaAs cells operating at 92 suns under AM0 illumination (see Figure 5(a)). Based on these results, our modelling suggests realistic efficiencies in excess of 38 percent at concentrations below 100 suns are within our grasp if we improve current balancing of our subcells, increase the transparency of the tunnel junctions and optimise the material quality of the InGaAsP alloys. When combined with lightweight CPV optics, this high conversion efficiency has the potential to enable extremely high specific-power space arrays which, when combined with the advantages in radiation resistance, areal fill factor, low arcing risk, low cost and high volumetric power density, will provide strong competition to incumbent technologies based on conventional, large-area solar cells.

We are working hard to continue to improve our devices. Current efforts include: developing highly doped C:InAlAs for use in the InP-based tunnel junction, which will improve optical transmission and lower series resistance in the InP triple-junction cell; and tuning subcell thicknesses to optimise the current balancing between the subcells.

A drawback of microcells is their high perimeter-to-area ratio, which creates excessive leakage current at low light intensities. At a very high sun concentration this is not an issue, with leakage effects suppressed by a favourable light-current to dark-current ratio. But

in the relatively low concentration regime, desirable for the space micro-concentrators that we are pioneering, we need to consider perimeter recombination.
To evaluate the extent of this issue, we have compared open-circuit voltages of devices with sides of 200 μm and 700 μm. These measurements, conducted at a range of concentrations, show that there is a reduction in open-circuit voltage in the smaller devices, due to the increased dark current – and this shortfall in performance is exacerbated as the concentration decreases.

It is worth noting that our GaAs devices have a Si_3N_4 dielectric covering their sidewalls, which provides passivating properties, while the InP device sidewalls are bare. This lack of dielectric is behind a drop in open-circuit voltage of 3 percent for the InP-based cells operating at 100 suns, compared with just 1.6 percent for the GaAs-based devices. There is no doubt that trimming sidewall leakage will yield performance improvements in our microcells with sides of around 170 μm. One important goal for us is to address this by developing strategies to minimise perimeter recombination.

Whilst four-terminal stacked cells provide simplifications in assembly, they are not ideal in most practical PV array scenarios. That's because operating two separate strings of multi-junction solar cells at their respective maximum power points is impractical, due to the additional complexity and hardware required. Our solution is to combine separate devices into a small-integer series or parallel string combinations which, when combined, match the photocurrents of the GaAs and InP cell strings. This results is an efficient, two-terminal output.
We are able to implement this approach by drawing on the interconnection degrees of freedom afforded by the micro-CPV architecture. Consider, for example, an array of our 170 μm CPV cells with a geometric concentration ratio of 92. This has a density of almost 380,000 cell-and-lens units per square metre, providing tremendous flexibility in wiring options.
To realise a roughly current-matched string for our five-junction cell we connect five series-connected groups of three GaAs double-junction cells, arranged in parallel, to three series-connected groups of five InP triple-junctions, configured in parallel. We calculate that the 15 stacked cells arranged in this manner will deliver more than a milliamp, with an associated output voltage of more than 15 V (see Figure 6 (a) for a diagram of the stacked cell arrangement, and Figure 6 (b) for the calculated light, current and voltage characteristics, using measured current-voltage curves at 92 suns).

By combining groups of this 15-cell unit in series or parallel as part of a larger array, we can provide flexibility in output voltage and current whilst retaining two terminals. There is also the option to use different photocurrent ratios by adapting cell design; for instance, in previous work we explored a terrestrial design for a stacked five-junction solar cell with a ratio of photocurrents between the GaAs and the

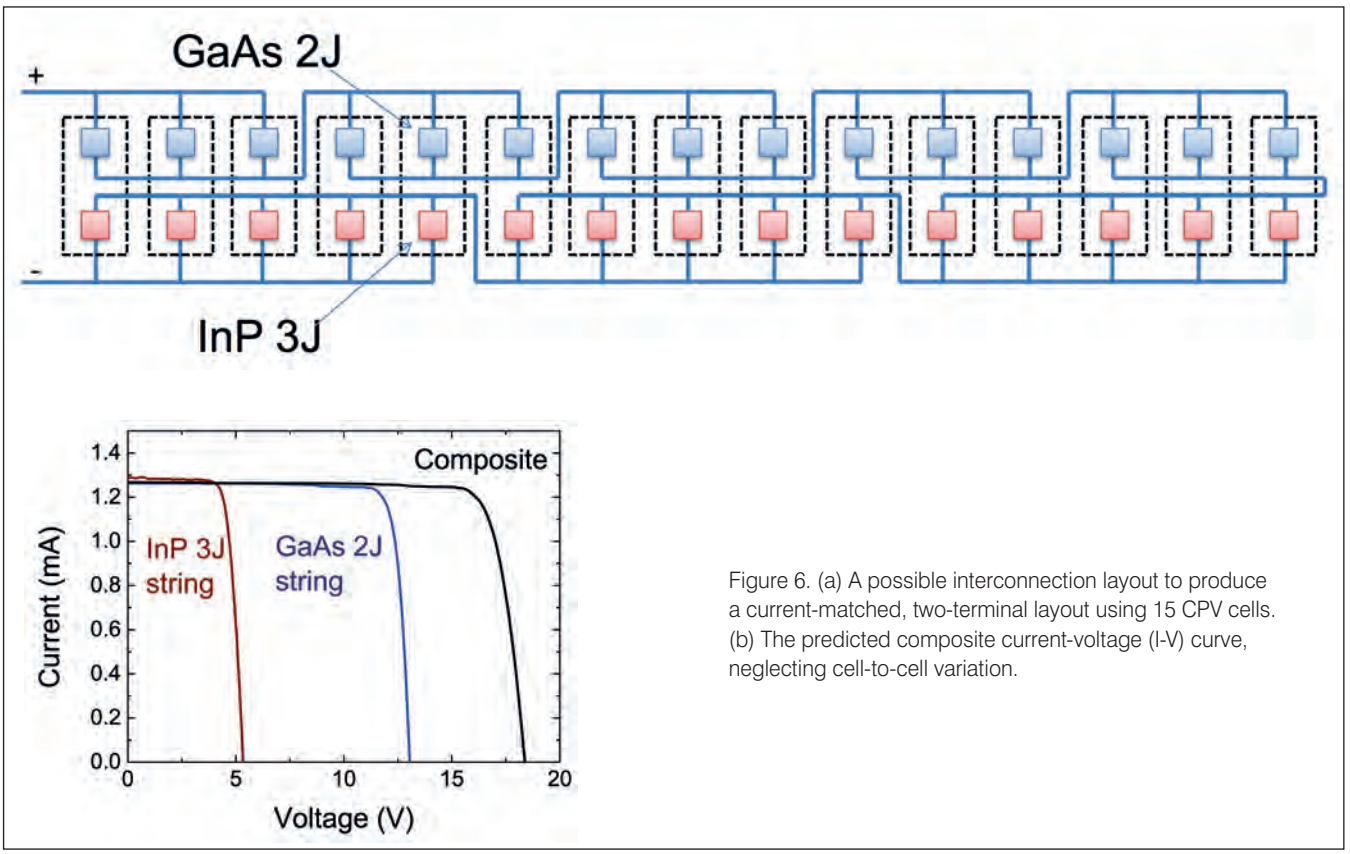


Figure 6. (a) A possible interconnection layout to produce a current-matched, two-terminal layout using 15 CPV cells. (b) The predicted composite current-voltage (I-V) curve, neglecting cell-to-cell variation.

InP cells of 2:1. Our work showcases some of the compelling advantages of micro-CPV over incumbent space photovoltaic technologies. By employing micro-transfer printing for assembly, we have a well-considered manufacturable route to high-efficiency heterogeneously integrated CPV cells. Our latest results demonstrate a conversion efficiency of 35.5 percent under concentrated AM0 illumination, and we have set out a clear pathway to efficiencies in excess of 38 percent. Realising this with lightweight, low-profile optics gives us the opportunity to break new ground in the key metrics of specific power, end-of-life efficiency and cost. We are well on our way to disrupting the long-established technological approaches for space power.

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Building better solar cells

Better-performing solar cells result from the introduction of dilute nitrides, novel separation layers and germanium-on-silicon templates

BY RICHARD STEVENSON

WHAT DO WE LOOK FOR from a solar cell? Many seek a high efficiency, especially if they need to generate a lot of power from a small plot. Cost is also crucial, as the return-on-investment is a big factor in determining whether a power-generation project gets the go-ahead. And depending on the application, flexibility of the cells may be essential; as can the ability to deliver plenty of power after continual bombardment from high levels of radiation.

Excelling on some of these fronts while struggling on cost are multi-junction cells involving III-Vs. By combining record-breaking efficiencies with a relatively high radiation hardness, they can reign supreme in the space market, where cost is not a major consideration. For the emerging market of powering light-weight unnamed aircraft they also show much promise, because they can cover a curved surface and produce a lot of power. But they have failed to make an impact in generating electricity for the grid because they are too pricey, even when deployed in concentrating photovoltaic systems.

If the cost of making multi-junction cells were to fall, this would increase margins, and could lead to a growth in sales across the board. Success in this regard might result in a significant reduction in the cost-per-Watt, which could also fall through increases in efficiency – an improvement that is welcome in all applications. It is also a good idea to devote some effort to refining the fabrication and performance of flexible cells, given that this is a potentially lucrative application where this class of device can shine.

Efforts to increase efficiency, cut costs and develop processes for making flexible cells were discussed at the *37th European PV Solar Conference and Exhibition (EU PVSEC)*, held online between 7th and 11th of September 2020. Speaking in a session entitled *III-V and Related Compound Semiconductor Solar Cell Devices*, Ivan Garcia from The Technical University of Madrid outlined efforts to trim the cost of multi-junction solar cells by switching to growth on silicon substrates; Arto Aho from Tampere University, Finland, presented results related to the development

of dilute nitride cells that could boost multi-junction cell efficiency; Nobuaki Kojima from the Toyota Technological Institute in Nagoya, Japan, detailed the use of a GaSe buffer for epitaxial lift-off of GaAs cells from a silicon substrate; and Christina Honsberg from Arizona State University spoke about the addition of GaPN top cells to form devices based on silicon that feature three terminals.

Cutting costs with silicon

Historically, germanium substrates have been used for manufacturing III-V cells, primarily because this foundation is cheaper and stronger than GaAs. Building on this approach, Garcia and co-workers from The Technical University of Madrid, working with engineers from the global epiwafer provider IQE, are pioneering germanium virtual substrates, created by the direct growth of germanium films on silicon. Merits of this approach include low cost, minimal germanium consumption, an absence of graded buffers, and the realisation of very low threading dislocation densities – values of just 5 x 10^5 cm^{-2} are possible.

However, success with this approach is not easy. When Garcia and co-workers started to use this foundation for the growth of multi-junction heterostructures, they found cracks in the epiwafers. This issue stemmed from the thickness of the epi-stack, with layers of germanium and the III-Vs totalling a thickness of around 10 μm. The critical thickness for the propagation of cracks is around half this value.

Garcia's explained that the team is addressing this issue by trimming the thickness of the epi-stack to 5.5 μm. This goes below the critical thickness, trading a far better material quality for a slight reduction in efficiency. The germanium layer that forms the bottom sub-cell is reduced from 5.5 μm to just 3 μm, and the middle sub-cell that is made from GaInAs is decreased from 3.5 μm to 1 μm (see Figure 1).

The team turned to modelling to assess the impact of the new design and investigate whether they needed a different composition to optimise performance. Based on considerations of the short-circuit current and the open-circuit voltage of the InGaAs sub-cell, they decided to employ an indium content of 8 percent in this 1 μm-thick layer.

Another finding from this theoretical study is that the thinning of the cell reduces efficiency by 2-3 percent. Under concentration, the efficiency of this new design could still be as high as 39-40 percent.

By fabricating the two designs, the researchers found that thinning the epistructure reduced cracks from more than 5 per millimetre to less than 1 per millimetre.

The team also studied a device with just the bottom two cells. This revealed that thinning InGaAs increases carrier collection efficiency. However, the external quantum efficiency still lags that of devices made on germanium substrates.

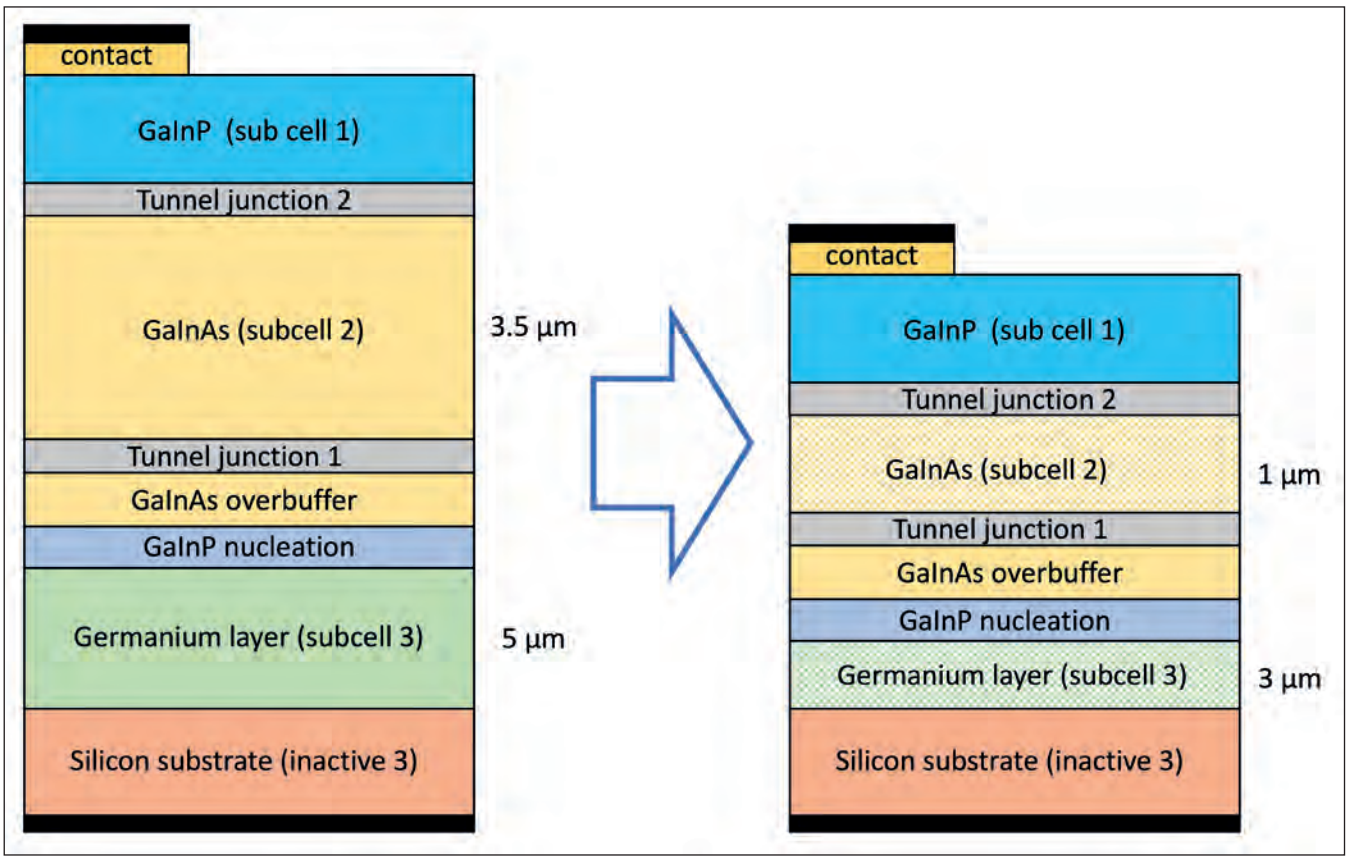

Figure 1. Reducing the thickness of the multi-junction cell that is grown on silicon leads to a reduction in the density of cracks in the epistructure.

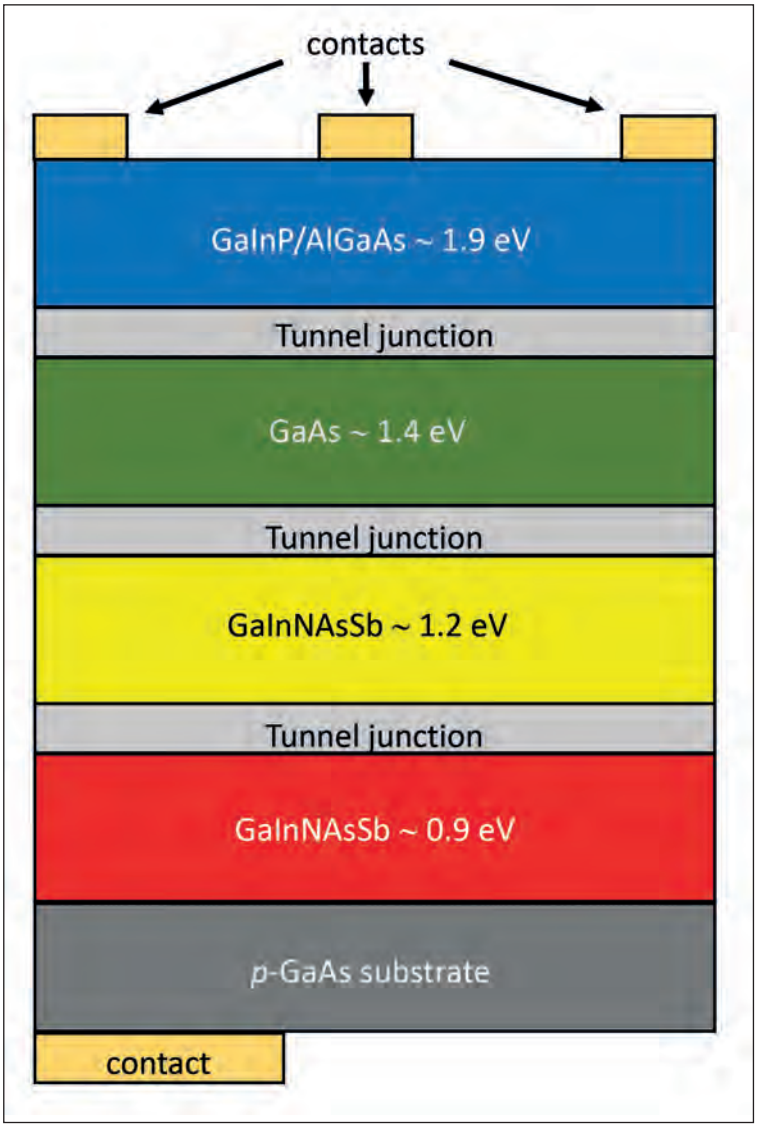

Figure 2. Researchers involved in the EU project AMETIST – Advanced III-V Materials and Processes Enabling Ultrahigh-efficiency Photovoltaics – are laying the foundations for devices with six or more sub-cells that involve dilute nitrides.

For the team's triple-junction cell, measurements under a 1 sun concentration showed that trimming the thickness led to an increase in current density, while the drop in open-circuit voltage is smaller than anticipated. However, performance is still significantly behind that of the standard III-V cells grown on silicon substrates, due to inferior material quality.

Goals for the future include investigating cells produced on higher-quality germanium-on-silicon templates and introducing current-matching in designs with thinned layers of GaInP and/or AlGaInP. Efforts may also be directed at evaluating residual tensile strain in thinned structures and considering the implications of this.

Delivering with dilute nitrides

One of the most effective ways to increase the efficiency of multi-junction photovoltaics is to replace the germanium sub-cell with multiple variants formed from dilute nitrides. This alternative design helped NREL to raise the record for efficiency to 47 percent, using a six-junction device; and it is also being pursued through a European project running from 2017 to 2022 entitled *AMETIST: Advanced III-V Materials and Processes Enabling Ultrahigh-efficiency Photovoltaics*. The latter aims to realise an efficiency of 55 percent with a monolithic cell featuring GaInNAsSb and GaNAsBi layers and nanophotonic structures for light-trapping.

Aho, who is working on this project, told those tuning in to EU PVSEC that the team's devices have their pros and cons compared with those formed by wafer fusion and mechanical stacking. Approaches of this ilk, which have produced efficiencies as high as 46 percent, are complex and expensive, with two wafers needed to form a device; but designs are free from material compromises. For developers of monolithic devices, decisions have to be made between upright and inverted designs, and lattice-matched and metamorphic architectures. The lattice-matched upright design adopted in the AMETIST project is simple to process and allows the use of the same tunnel junction throughout, but epitaxy is not easy to master.

Simulations by the team highlight the promise of their dilute nitrides. Triple-junction cells should be capable of efficiencies of 49 percent, rising to values of 52 percent and 55 percent for variants with six and eight junctions.

Updating delegates of progress made during the first few years of the project, Aho presented results of efforts at producing four-junction cells with two dilute nitride sub-cells (see Figure 2). Measurements on cells with a size of 2 mm by 2 mm show an efficiency of 39.3 percent at 564 suns, falling to 36.9 percent at 946 suns.

Analysis revealed total losses of 15 percent. Of this, 6 percent came from grid and shadowing losses, with the team believing there is only room for marginal improvements; just 1 percent was associated with transmission losses from the upper tunnel junction; and 8 percent came from transmission and/or collection losses in the bottom cell – this is where there is an opportunity for the biggest gains.

The team have started to develop sub-cells that could be added to the device to increase efficiency. Work has been directed at a sub-cell with a bandgap of more than 1.9 eV, and another below 0.9 eV. During the project the team developed techniques to increase the nitrogen content in GaInNAsSb layers, and fabricated AlGaInP devices with a bandgap of up to 2.18 eV that have an efficiency up to 26 percent. "We have the building blocks for six-junction solar cells," remarked Aho.

Flexible photovoltaics

Production of flexible thin-film photovoltaics has much to offer, combining the opportunity to cover curved surfaces with the potential for substrate re-use. This technology has been developed by inserting an AlAs

buffer between a GaAs substrate and a cell made with the same material, with HF etching removing the sacrificial layer. However, etching is time consuming and substrates are expensive.

Addressing these weaknesses, Kojima and co-workers are trailblazing the use of a two-dimensional metal selenide layer that allows mechanical cleavage and re-use of the silicon substrate. To ensure success, the two-dimensional structure has to be thermally stable under the growth conditions used for GaAs.

Promising materials for the two-dimensional metal selenide layer are In_2Se_3 and GaSe, materials with lattice constants relatively close to that of GaAs. Using diffraction patterns generated during MBE of III-Vs on silicon, the team observed how the growth of In_2Se_3, followed by GaAs, created a layer of Ga_2Se_3. Although the direct growth of Ga_2Se_3 on silicon is possible, it yields films with inferior material quality.

To separate the GaAs-based epilayers from the silicon substrate, Kojima and colleagues bonded the top of the wafer to a polymer sheet with an adhesive, before dipping the resulting structure in liquid nitrogen. A homogeneous thermal stress resulted, separating the substrate from the GaAs layers.

Inspecting the silicon substrate with a scanning electron microscope uncovered flaky remains on its surface, while optical microscopy revealed plenty of wrinkles in the GaAs film produced by the peeling process. This suggests more progress is needed before this technology can realise its full potential.

Supplementing silicon

While III-Vs can't compete with silicon on price, they will always hold the ascendancy on efficiency. The best value for silicon is now just shy of 27 percent, with any gains modest and hard to come by. But what about adding a III-V to silicon to try and enjoy the best of both worlds? That's the approach adopted by Honsberg and her team from Arizona State University.

She told the on-line attendees at EU PVSEC that a major impediment to this approach is the lack of a conventional III-V that is latticed matched to silicon and has a suitable bandgap – ideally, it needs to be around 1.7 eV. Her solution is a three-terminal solar cell that incorporates a lattice-matched dilute nitride (see Figure 3). By turning to a three-junction solar cell, the current-matching constraint is alleviated while allowing monolithic integration. Honsberg explained that the three-terminal tandem is relatively unsensitive to optimisation of the bandgap, allowing the use of higher bandgaps that result in a greater proportion of energy from the silicon cell. She also pointed out that to get the best output from the tandem, the bandgap of the top cell needs to be higher when working with imperfect material.

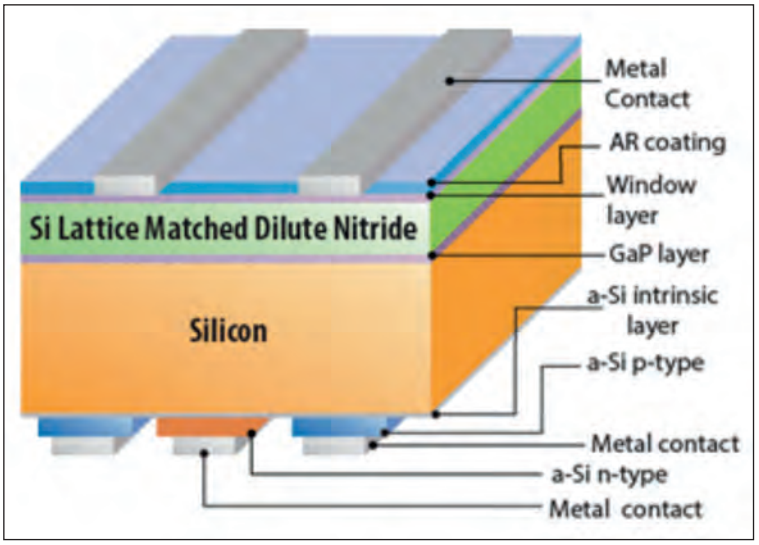

Figure 3. A team from Arizona State University is developing a three-terminal solar cell that incorporates a lattice-matched dilute nitride.

To prevent damage from the nitrogen plasma, as well as deleterious effects of nitrogen at the silicon interface, Honsberg and co-workers employ a GaP buffer layer. Growing this on silicon can lead to anti-phase domains, misfit dislocations, stacking faults and pit formation, with the team from Arizona finding that they get their best results when using off-cut substrates. Working with an off-cut of 4° increased crystal quality, according to X-ray diffraction measurements, and improved minority carrier lifetimes.

Measurements on unoptimised layers of GaPN grown on silicon show a minority carrier lifetime of 28 ns at 78K. Based on external quantum efficiency fitting of an experimental device, the minority carrier lifetime at room-temperature is estimated to be 0.5 ns – it needs to be 1-2 ns for an efficiency of more than 35 percent. This is an encouraging result, as is an external quantum efficiency of an initial device of 25 percent. Efforts will now be directed at defect annealing for different growth conditions as this could lead to better material quality, and ultimately more efficient devices.

Progress made by Honsberg and her team – as well as the recent research at The Technical University of Madrid, Tampere University and the Toyota Technological Institute – highlight the value that III-Vs can bring to solar technology. It's hard to see III-V cells replicating their success in space on earth any time soon, but progress in the lab could spark commercial ventures and the emergence of sales.

While III-Vs can't compete with silicon on price, they will always hold the ascendancy on efficiency

Evaluating new switching technologies

It takes more than a change in part number to move to a wide bandgap technology; what's required is a systemic approach, considering all aspects of design

BY STEFAN OBERSRIEBNIG FROM INFINEON TECHNOLOGIES

TRANSISTORS ARE EVERYWHERE. They are in our mobiles, tablets and PCs, providing the key ingredient in integrated circuits, with each device tuned for a specific function, such as fast switching or a low operating voltage. Transistors also appear in a discrete form, serving in power switching applications. Here there is also a need for optimisation, a task made more challenging by an ever-growing range of products. But select the right one and the rewards are greater than ever.

This expansion in the range of power transistors has taken place against a backdrop of 'More than Moore', an era where the use of new materials offers a route

to improved performance. During this time, we have learnt that the latest fabrication node may not provide the most optimal solution; instead, it may be more prudent to choose the appropriate node for each function and integrate at a modular level.

When it comes to discrete transistor technologies, particularly for high-power applications, the expansion in choice comes from the introduction of new materials. It may be perceived that the technologies on offer, namely silicon, SiC and GaN, follow a path comparable to integrated digital transistors; that each new step is a linear improvement on the last, and should be adopted without question as the right replacement. But this is a misconception. The reality is more nuanced, with the optimal solution hinging on adopting the lessons learned through the development of More than Moore to the power domain. One must not simply view the newest technology as the best, without first giving it closer inspection. When engineers do this, they need to consider many aspects associated with design, so that they select the technology that is best for the respective application.

For makers of silicon, SiC and GaN power electronic devices, two of the biggest applications are power conversion and power management. Many devices are deployed in conversion topologies, based on variations of the common switched-mode power supply. The basic switched-mode power supply takes advantage of a transistor's ability to turn on and off rapidly and precisely, with variants manipulating specific features to deliver higher efficiency under specific conditions. New wide bandgap technologies are enabling innovative ways to exploit these topologies through faster switching and higher power capabilities.

It is often overlooked that even without changes to switching frequencies and turn-off/turn-on timings, the replacement of silicon devices with those with a wider bandgap can still deliver improvements. These gains relate to specific features, such as the integrated body diodes of SiC MOSFETs that allow them to take the place of conventional diodes in synchronous rectification designs. Merits of the body diode of the SiC MOSFET include a negligible reverse recovery charge and a high forward-voltage drop when

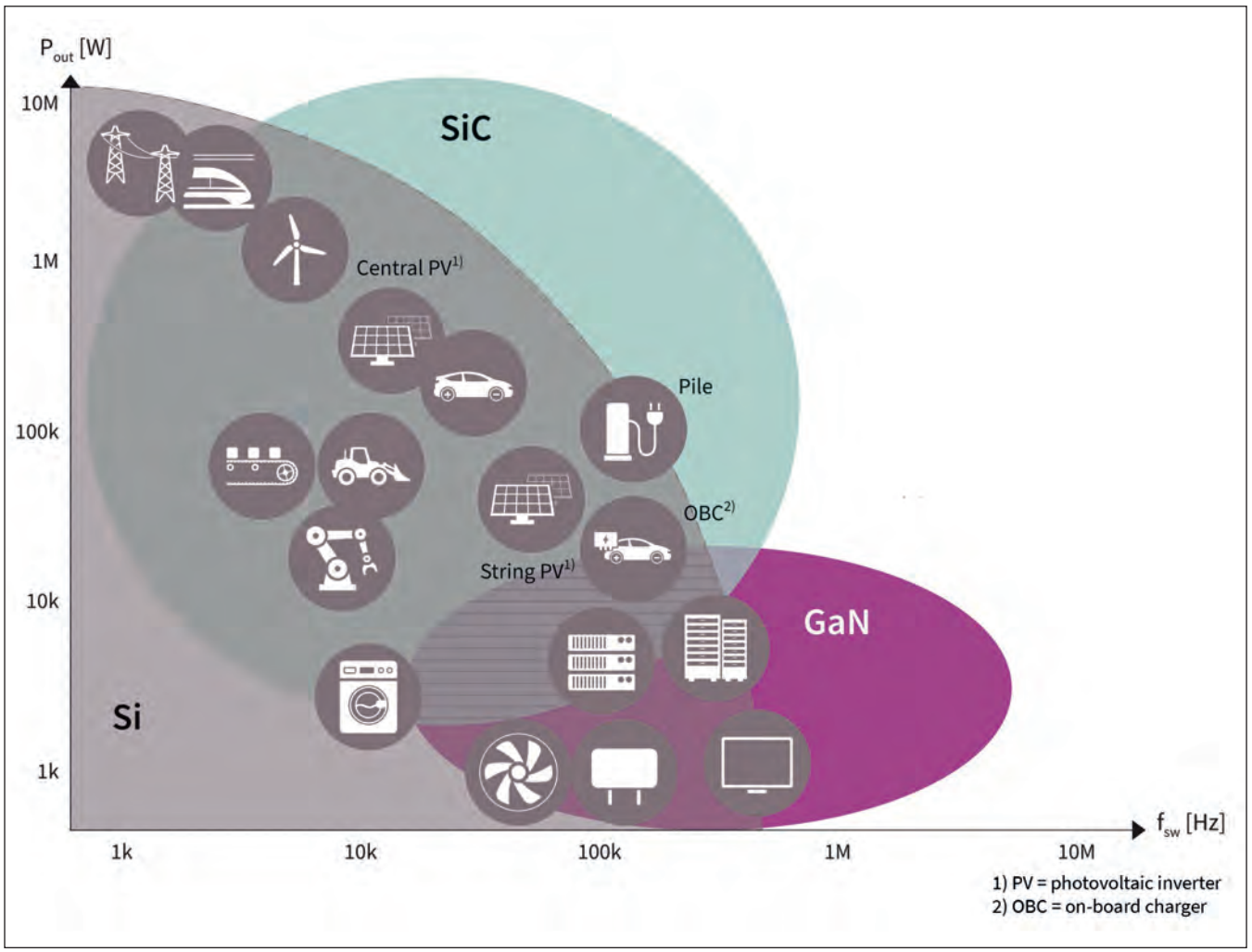

Figure 1: Mainstream silicon, complemented by SiC and GaN, delivers increased efficiency and a higher power density.

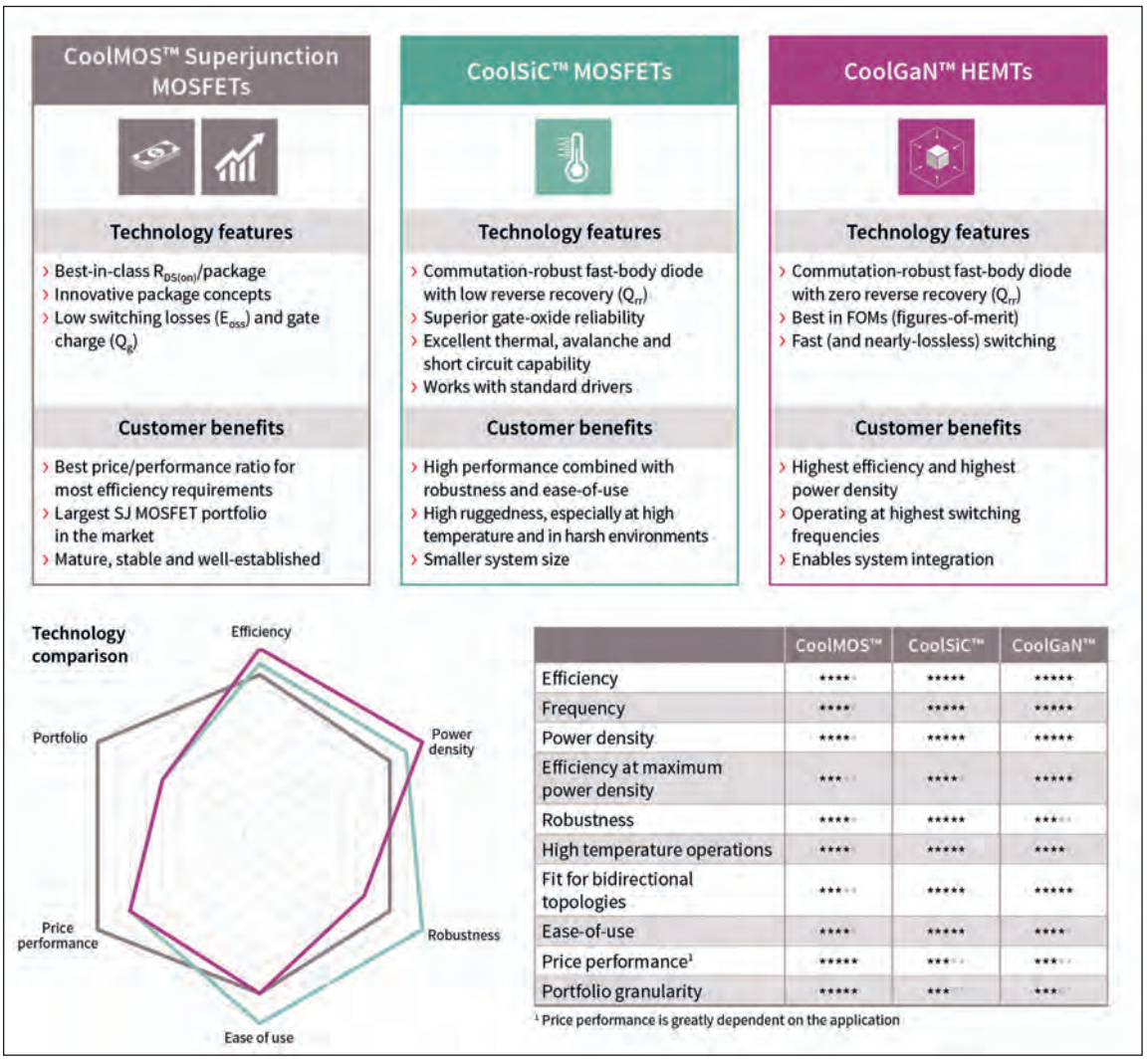

Figure 2: Different power switching technologies and application areas.

conducting, which dissipates the energy build-up that limits the switching frequency of silicon devices. It is the switching characteristics of SiC that are behind its capability to deliver higher efficiency.

Many different types of switching topology are in use today, including inverters, active clamp flyback converters and phase-shifted bridge topologies. This diversity is unlikely to change, as each topology has its own merits.

When designers select a topology, their decision tends to be governed by the requirements of the application rather than the ideal substrate. Due to this hierarchy within the decision-making process, GaN is not always the best option for applications requiring high voltages and currents. The reasoning is that although GaN is better than silicon in half-bridge topologies when implementing hard-switching, SiC has the upper hand for soft- and resonant-switching topologies (see Figure 1 for an evaluation of the suitability of today's available semiconductor technologies to several key applications).

As new applications emerge, such as electric vehicles and renewable energy, and existing applications evolve, like data centres and cellular telecommunications, the requirement isn't simply for more power. Instead, there is a need for more power, delivered in the same or a smaller form factor, using different voltage levels, currents, stability and response times. This list of requirements puts pressure on power supply developers, who may need to explore new topologies. However, the demands also create an opportunity to evaluate new transistor technologies for fulfilling these needs.

At a high level there is much to be garnered by considering the characteristics of all the classes of transistor technology. Taking this approach provides a snapshot of their respective merits and goes some way to explaining why the industry is pursuing their development.

Transistor characteristics

At Infineon Technologies, a multi-national device manufacturer operating in the power electronic industry, we have devoted much time and effort to developing a range of technologies based on silicon, SiC and GaN, as well as the corresponding drivers needed to maximize the potential of each technology.

We can advise what will provide the best cost-to-performance ratio – it may be silicon; in some high-power applications it could be SiC; and in other scenarios – for instance for high frequency designs, GaN might deliver the best performance, making it the right option.

We have a rich history of innovation, including invention of Superjunction technology and the launch of the world's first SiC Schottky barrier diode (in Figure 2 we offer a graphical representation of where each semiconductor technology fits in terms of power transistors).

Our experience is that the demand for silicon-based power devices remains strong. It is still the best technology for many applications, and it has reached a level of maturity that makes it highly cost-competitive. Although at one stage regular silicon appeared to be running out of steam, the introduction of superjunction technology injected a new lease of life, reducing the on-resistance. This led to a trimming of switching losses, allowing this class of device to serve in high-voltage, high-power applications.

When SiC launched, it lowered the on-resistance of the transistor for a given area by a factor of three. Another advantage, also coming from its wider bandgap, is that it enabled devices to handle far higher voltages without failure.

Recently, GaN has entered the fray, sporting a very similar bandgap to SiC. However, its transistor architecture is markedly different from that of SiC MOSFETs and superjunction devices. GaN FETs feature an undoped layer that increases electron mobility and results in an even lower on-resistance.

At first glance, the reductions in on-resistance associated with moving from silicon to SiC and then on to GaN suggest that the latter is always the preferred solution for power switching. However, while the material used for the transistor determines its strengths, the characteristics of each class of device differ under the same operating conditions. Due to this, when GaN is employed in a topology implementing a continuous conduction mode, it only delivers a superior efficiency to a silicon MOSFET under certain load conditions. So, when designers make a decision, they must take into account how the technology behaves under all operating conditions; they should not view any two technologies as drop-in replacements for one another.

With these factors at play, designers must evaluate the difference in the performance of SiC, of GaN and of silicon MOSFETs and superjunction devices in different types of power-converter circuits – the right approach for one application is not necessarily the right one for another. Due to this, the best results do not come from simply standardizing on one wide

bandgap technology, as this will not lead to efficiency gains across all applications.

We are in an enviable position of offering industry-leading devices made from silicon, SiC and GaN; and we can draw on our system expertise to support our customers through every generation of their application. This allows us to supply the best technology for the most appropriate topology, whether that is silicon, SiC or GaN, making us a great power-design partner. We can advise what will provide the best cost-to-performance ratio – it may be silicon; in some high-power applications it could be SiC; and in other scenarios – for instance for high frequency designs, GaN might deliver the best performance, making it the right option.

Note that the right decision is not set in stone. SiC and GaN are still evolving, and it is also crucial to consider the driver technology used for power switching, as matching the best transistors with the best drivers plays a big part in optimising design.

Power integration

Each application comes with its own requirements, which dictate the right topology and in turn the most appropriate semiconductor technology. However, there is also a trend towards more integrated solutions, which combine transistors and drivers into modular solutions. In much the same way as More than Moore is bringing together the most appropriate nodes for given functions, power modules are starting to simplify power supply design for various applications with similar requirements.

The semiconductor industry is moving towards greater integration at a modular level. This is already apparent in the wireless communication sector, where entire radio systems are being integrated closely alongside controllers, allowing the end device to pass certification with less effort. In many cases, wireless modules are supplied pre-certified, making them a 'plug and play' solution.

Within the power systems sector, a similar trend is underway and set to continue. We are well-positioned to respond, thanks to a portfolio of products and the experience required to develop and bring to market high-quality integrated power modules.

Merits of power modules are not limited to simplifying the design process for the customer. By optimising the design, we also provide two major performance benefits: a reduction in size compared with discrete components, resulting in higher power density at 'no extra cost'; and a higher efficiency, which is an overriding requirement in power conversion and one of the key drivers behind the development of wide bandgap technology.

Using a module also has practical benefits. It is not easy for an engineering team to realise a high level of efficiency, because they need to understand how the power supply will behave under all possible modes of operation when selecting the design that delivers a performance curve that best fits their objectives. With discrete devices this could be an iterative process, with no guarantee that the results deliver the best efficiency under all operating conditions. By turning instead to a power module, complexity is eliminated, allowing an out-of-the-box solution to deliver a superior efficiency while increasing ease of use.

There is no doubt that the introduction of wide bandgap semiconductor technologies improves the power conversion landscape. They are complementing silicon-based technology by extending power and switching frequencies to support new applications with improved topologies. However, they must not be seen as a drop-in replacement for existing technologies. It is also critical that the underlying requirements of the application define the switching topology used and in turn guide engineers in their selection of the best transistor technology for meeting power efficiency goals.

We have an incredibly strong track record in the power semiconductor industry, having more than 40 years of power MOSFET know-how at our hand. Our portfolio includes silicon, SiC and GaN power devices, plus optimised complementary drivers. We continue to expand our offering, with recent steps in this direction including the acquisition of Cypress Semiconductor, which will increase our offering at the system level. By putting all of this experience into practice, we are uniquely positioned as a trusted advisor and partner within the semiconductor industry.

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Supercritical carbon dioxide spawns superior MOSFETs

A low-temperature treatment with supercritical CO_2 improves the interface between SiC and SiO_2

THE PERFORMANCE of the SiC MOSFET is held back by the quality of the interface between SiC and SiO_2. But this weakness can be addressed with a supercritical CO_2 treatment that slashes the density of interface states, claims a partnership between researchers at Xi'an Jiaotong University and Xidian University.

Spokesman for the team, Weihua Liu from Xi'an Jiaotong University, told *Compound Semiconductor* that in conventional SiC MOSFETs the interface is not optimised by high-temperature annealing, because this can create carbon clusters and other defects.

Formation of these imperfections is quashed with a lower temperature supercritical CO_2 treatment that promises higher carrier mobility, a lower leakage current and a hike in the critical breakdown field of the gate oxide.

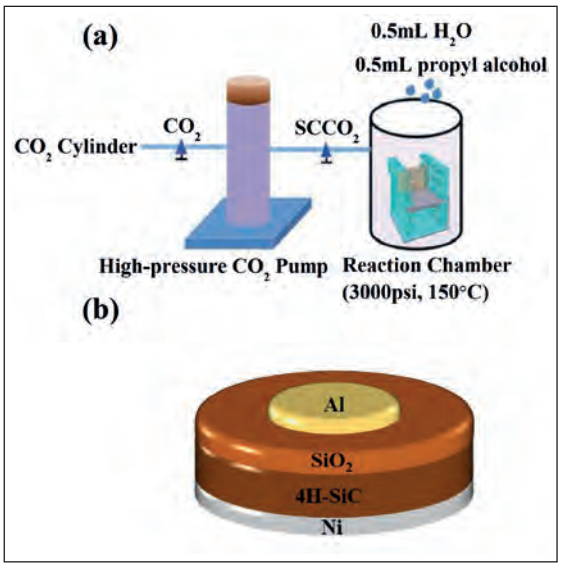
In a supercritical fluid there is a co-existence of liquid and gas phases. Thanks to this, supercritical CO_2 combines gas-like solubility with liquid-like penetration, enabling damage-free diffusion into nanoscale structures.

The use of supercritical CO_2 to improve interfaces in semiconductor devices is not new. Back in 2007, reports appeared describing the benefits this can bring to thin-film transistors made from amorphous silicon.

When supercritical CO_2 treatment is applied to SiC MOSFETs at temperatures as low as 150 °C, it is thought to terminate traps at the oxide-semiconductor interface and supress the interfacial parasitic oxide.

To assess the benefits of the supercritical CO_2 process, the team began by producing MOS structures. They took epiwafers with an *n*-type layer that has a doping concentration of 3.5 x 10^{15} cm^{-3} and, after applying a standard cleaning process, used dry oxidation to create SiO_2 films with a thickness of 55-60 nm.

Some sample were treated in supercritical CO_2 at 150 °C for 60 minutes, using a pressure of 20 MPa (see Figure). To the process chamber the team added 0.5 ml of water and 0.5 ml of propyl alcohol. The latter acts as a surfactant between non-polar CO_2 molecules and polar water molecules, enabling water to be uniformly distributed in supercritical CO_2.



Treatment with supercritical CO_2 (a) is applied to MOS structures (b).

To benchmark results, the team did not treat some samples and processed others in a pure water vapour at 150 °C for 60 minutes.

Fabrication of MOS structures, featuring aluminium electrodes with a diameter of 300 μm, allowed the team to evaluate the density of near-interfacial oxide traps. Using capacitance-voltage measurements, they found a near-interfacial oxide trap density of 1.62 x 10^{11} cm^{-2} in the untreated sample, while samples treated in water vapour and supercritical CO_2 produced values of 6.63 x 10^{10} cm^{-2} and 1.84 x 10^{10} cm^{-2}, respectively. The lowest value is claimed to result from the termination of traps in SiO_2 through the creation of Si-O-Si feature bonds.

Additional benefits of the supercritical CO_2 treatment are a reduction in leakage current and an increase in breakdown field.

Measurements of the interface state density also revealed the benefit of supercritical CO_2 treatment.

Liu says that one of the next tasks for the team is to optimise the experimental conditions, in order to further reduce the interface state density. Another goal is to verify that the supercritical fluid process delivers benefits to 4H-SiC MOSFETs by applying this treatment to those devices.

Reference

M. Wang *et al*. Appl. Phys. Express **13** 111002 (2020)

Building better Ga_2O_3 transistors

Wrapping modulation-doped Ga_2O_3 FETs in highly conductive materials addresses concerns related to thermal management and carrier transport

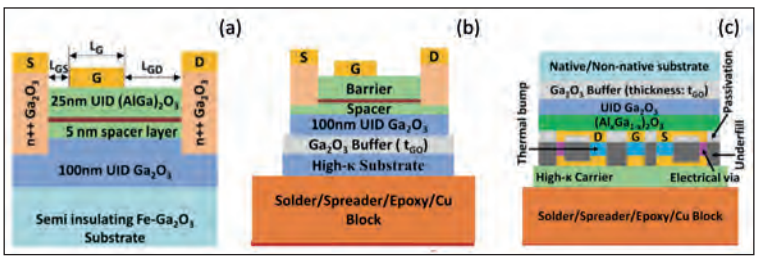
IF Ga_2O_3 transistors are to fulfil their potential in RF and power electronics, issues must be addressed that relate to a low electron carrier mobility and heat extraction.

Offering promising solutions to both these concerns is a US collaboration between engineers from The Pennsylvania State University, The Ohio State University, Kyma Technologies, Modern Microsystems and the University of Utah. This team is making the case for replacing the MOSFET with a FET featuring modulated silicon δ-doping – a class of transistor known as the MODFET – and incorporating materials with a high thermal conductivity, to allow the device to run harder without overheating. Using the most capable architecture for heat extraction enables a five-fold increase in power handling.

Investigations by the team involved experimental studies and simulations. They included the use of thermo-reflectance thermal imaging to determine the surface temperature of the MODFET under various operating conditions. To validate those results, the engineers turned to nanoparticle-assisted Raman thermometry. Both techniques, which probed the temperature rise of the gate metal, gave excellent agreement. Values were replicated in simulations produced by Synopsys Sentaurus and COMSOL Multiphysics software.

Simulations were employed to consider the impact of changes to gate-to-drain distance in MODFETs with a gate-to-source separation of 1 μm and a gate length of 3 μm (see Figure (a)). To increase the breakdown voltage in power FETs, designers tend to employ a gate-to-drain spacing that exceeds the gate-to-source separation. According to simulations, by increasing the gate-to-drain spacing from 3 μm – the distance used in the devices produced for the thermal measurements – to 20 μm slashed the peak electric field by an order of magnitude. In turn, the rise in peak temperature fell by almost 40 percent.

The engineers have also used simulations to consider the impact on power handling of the insertion of high thermal conductivity substrates underneath the MODFET. For a MODFET with a 10 μm-thick Ga_2O_3 buffer (see Figure (b)), mounting this device on a 4H-SiC wafer led to a reduction of 46 percent in the rise in maximum temperature. Replacing 4H-SiC with diamond, which has a thermal conductivity around four times higher, delivered further improvement. However, gains were modest, delivering just a 5 percent decrease in the maximum temperature,



The thermal management of a Ga_2O_3 MODFET (a) can improve by inserting a high thermal conductivity substrate (b). Even better results are possible with a double-sided cooling design (c).

because the 10 μm-thick Ga_2O_3 buffer dominates the thermal dissipation of this device.

To evaluate the role that the buffer has on device heating when switching from 4H-SiC to diamond, the team also simulated MODFETs with Ga_2O_3 buffer thicknesses of 100 μm and 1 μm. For the former, diamond delivers only a 1 percent gain over 4H-SiC, but for the latter it is an improvement of 14 percent. However, the team is quick to point out that the feasibility of thinning a Ga_2O_3 buffer to just 1 μm is yet to be established.

Experimental verification of these trends came from infrared thermography measurements, supported by finite-element thermal modelling. The engineers demonstrated that the addition of a 500 μm-thick 4H-SiC wafer to MODFETs with a 10 μm-thick Ga_2O_3 buffer provided a 66 percent reduction in the peak temperature.

Further reductions in peak temperature can result from a double-sided cooling design. With this architecture, the best results come from a combination of: depositing nanocrystalline diamond over the FETs; using gold bumps, rather than those made from indium; and mounting the transistor on polycrystalline diamond.

Simulations suggest that for MODFETs operating with a channel temperature of 200 °C, moving from the conventional homo-epitaxial design to an optimum double-sided design enables a hike in power density from 1.7 W/mm to 9.5 W/mm.

Reference

B. Chatterjee *et al.* Appl. Phys. Lett **117** 153501 (2020)

AlPN enlarges the nitride family

Growth of AlPN epilayers promises better HEMTs and VCSELs

A PARTNERSHIP between researchers at Nagoya University and Japan's Institute for Material Systems for Sustainability claims to have broken new ground by producing the first epilayers of AlPN. This ternary, latticed-matched to GaN, promises to improve the performance of GaN HEMTs and VCSELs.

Latticed-matched AlPN could transform HEMTs by introducing a very high polarisation that leads to a high carrier concentration in the channel. Early results are very encouraging, with an unoptimised sample producing a sheet resistance of just 150 ± 50 Ω/square.

For GaN VCSELs, AlPN could be a game-changer, simplifying and improving the fabrication of the mirrors. Prior to the work of the Japanese team, GaN and AlInN provided the only pair of nitrides that could be used for growing mirrors. With this duo, the growth of a mirror takes 12 hours or more, due to drawbacks on three fronts: there is a need for many mirror pairs; the ternary has a slow growth rate; and temperature ramping is needed between GaN and AlIN, which must be grown using a temperature deviation below 3 °C.

Those issues are to blame for a growth time that is far too long for the production of VCSELs incorporating two GaN-based mirrors. Instead, devices tend to combine one GaN-based mirror with another made from a dielectric.

Switching to mirrors made from AlPN and GaN promises to slash the growth time to 2-3 hours, says the spokesman for the team that is pioneering this novel alloy, Markus Pristovsek from Nagoya University. According to him, the substantial time saving stems from the faster growth rate for the ternary and the reduction in the number of mirror pairs, realised thanks to a much larger difference in refractive index between the two nitrides.

The development of ternary nitrides has a long history, with efforts between 1996 and 2005 directed at a cousin of AlPN, GaPN. During those years researchers discovered that when the phosphor content exceeded 3-4 percent, phosphor atoms head for gallium sites, due to the shorter bond length and smaller size. Adding aluminium offered a solution.

In 1999 Panasonic filed a patent for AlPN and AlGaPN. "However, there was never a publication," points out Pristovsek, who reasons that either attempts failed or the patent was filed simply to expand an intellectual property portfolio.

Pristovsek started to actively pursue AlPN in 2012. "A first attempt to patent it at TU Berlin failed, because they thought there is absolutely no commercial value and the patent would not earn its fee."

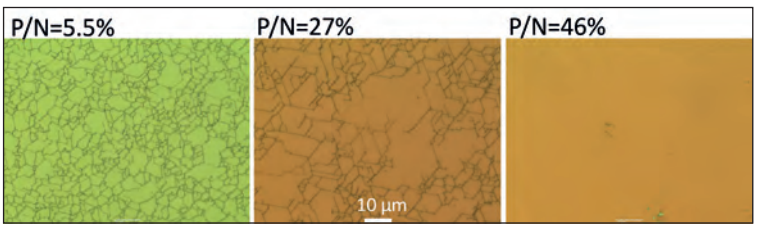
A move to the University of Cambridge enabled Pristovsek to secure funding for AlPN research. However, by the time an order had been placed for a tertiary-butylphosphine (tBP) bubbler that would provide a source of phosphor – phosphine is toxic, so forbidden in many labs – Pristovsek had an offer of a professorship at Nagoya University.

Taking that up in 2016, he took some time to find an underused reactor for his experiments and convert a metal-organic line to tBP. The first epiwafers were riddled with cracks, but cranking up the tBP flow addressed this issue.

Pristovsek and co-workers turned to X-ray diffraction to investigate the crystalline structure of a 60 nm-thick layer of AlPN, grown on a GaN-on-sapphire template. Measurements produced reflections only from GaN, sapphire, and strained $AlP_{0.103}N_{0.897}$, revealing that the ternary is pure wurtzite AlPN. Based on the position of the diffraction peak for this alloy, to ensure lattice-matching the composition of this ternary needs to be $AlP_{0.106}N_{0.894}$.

Ellipsometry measurements on samples with AlPN thicknesses of 180 nm, 315 nm and 665 nm indicate that the refractive index of this ternary, when lattice-matched to GaN, is around 1.95 to 2.05. There are Fabry-Perot oscillations associated with the 655 nm-thick sample that suggest that the bandgap for this alloy is around 5.5 eV.

One of the next goals for the team is to develop GaN HEMTs with an AlPN layer.



Cranking up the flow of tertiary-butylphosphine increases the ratio of phosphor-to-nitrogen and reduces the density of cracks in the AlPN layer.

Reference
M. Pristovsek *et al.* Appl. Phys. Express **13** 111001 (2020)

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