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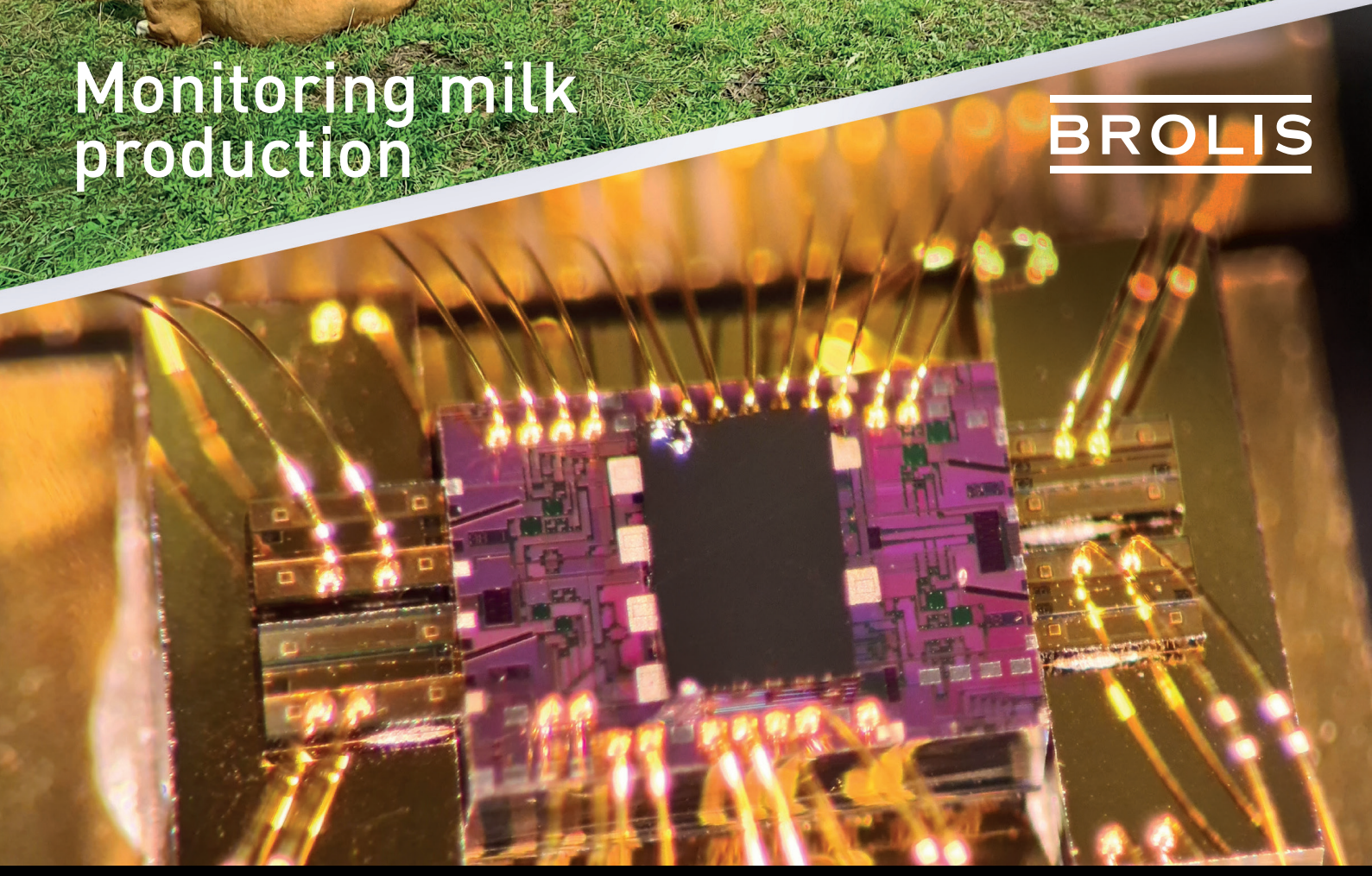

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VIEWPOINT

By Dr Richard Stevenson, Editor

WHILE MANY PEOPLE have never heard of compound semiconductors, we know that they are all around us. When speaking to the uninitiated we can offer many examples of their uses, pointing to the LEDs that light our homes, offices and displays; lasers that underpin the internet; and power electronics that lies at the heart of the leading electric vehicles.

When we rattle off all these examples, it's easy to forget the role that III-Vs play in space. Since the turn of the millennium they have dominated power generation on satellites, thanks to a higher efficiency than the previous incumbent, silicon, and a tremendous resilience to radiation.

That's not the only use of compound semiconductor is space. They are also being deployed in communication systems, where GaN devices are rising to the fore, due to a wonderful set of attributes that include a capability to operate at an incredibly high power density, handle substantial voltages, and run at high temperatures.

However, there are concerns relating to the use of GaN RF devices in space. One issue relates to the efficiency of GaN MMICs, but efforts are underway to increase this through a project called Kassiopeia that is funded by the European Space Agency. This initiative will combine the excellent thermal management provided by SweGaN's novel buffer design with FBH's iridium sputter-gate technology that reduces dynamic losses (see p. 50 for more details). Another key player in Kassiopeia is the University of Bristol, responsible for assessing the temperature distribution within the devices.

Much thought and care must be devoted to assessing the reliability of GaN devices for space and setting appropriate standards. For more than fifty years standards have been developed, but what was right for assessing the leading devices of the 1960s and 1970s is not necessarily suitable for today's GaN.

To help bring these standards up to date so that they offer valuable insights when evaluating GaN, John Scarpulla from The Aerospace Corporation has led efforts to produce guidelines for specifying, testing and qualifying devices based on the GaN HEMT. This body of work, concerned with the use of GaN on lengthy missions that demand an incredibly high level of reliability, focuses on intrinsic and extrinsic reliability, electrical robustness, environmental factors, mechanical integrity and radiation effects. You can read an overview of this guideline on pages 28 to 33, and if this piques your interest, you can get hold of a copy – it is available to the general public upon request.

Arming engineers with this information will give GaN devices an even better chance of being a major success story in space, and in turn provide yet another example of what compound semiconductors are doing for all of us.

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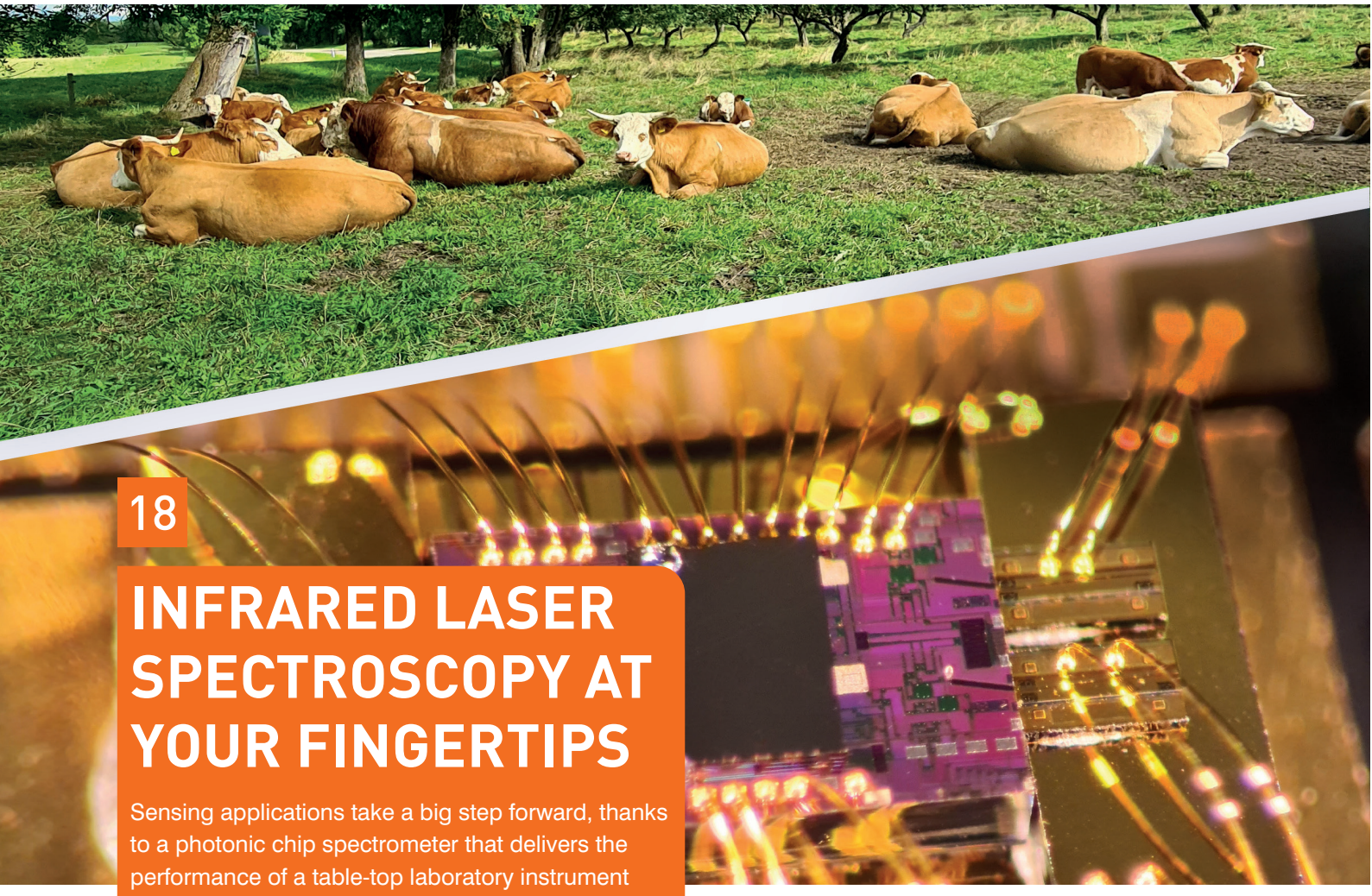

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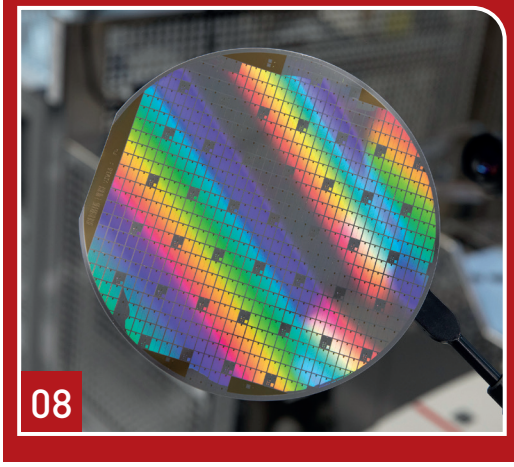

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NTU Singapore launches Quantum Science and Engineering Centre

NANYANG TECHNOLOGICAL UNIVERSITY, SINGAPORE (NTU Singapore) has launched the Quantum Science and Engineering Centre (QSec), which aims to develop devices and technologies powered by quantum science – the study of how particles behave at the atomic level.

The centre, the first of its kind in Singapore, will conduct research on developing and producing quantum chips using semiconductor fabrication technologies. These chips form the backbone of quantum devices such as quantum chip processors, networks, and sensors. They hold important applications in many areas such as quantum computing, communication, cryptography, cybersecurity, and sensor technology.

The opening ceremony for QSec was witnessed by Chan Chun Sing, Minister for Education and NTU President Subra Suresh.

The Centre aims to train skilled manpower for quantum engineering, the application of quantum science to real-world scenarios, and to promote and develop Singapore's quantum industry. It will collaborate with the Centre for Quantum Technologies (CQT), a Research Centre of Excellence established in 2007, on quantum technology research and engineering application, and look at establishing an international platform to collaborate with other overseas partners.

NTU President Subra Suresh said: "The Quantum Science and Engineering Centre aims to conduct ground-breaking research in several areas: quantum key distribution chips, quantum computation, quantum and classical neural networks, cluster state computation and quantum sensing. NTU's focus in these areas is part of our strategy to be a key enabler in the development of quantum science technologies to support Singapore's efforts in quantum engineering for the benefit of industry and society."

Housed at NTU's College of Engineering, the cutting-edge research centre's current projects include research into quantum chip processors, quantum chip networks, and quantum chip sensors.

Centre co-director Liu Ai Qun from NTU's School of Electrical and Electronic Engineering said: "The Quantum Science and Engineering Centre aims to not only take up a key role in supporting the local quantum industry, but to also build up strong international collaboration in quantum technologies which will benefit Singapore."

Creating light-based quantum chips

One of the QSec's main research projects is the development of a quantum computing chip that can perform quantum calculations using an integrated photonic chip, which can be made with semiconductor materials such as silicon wafers.

QSec researchers are exploring how photonics engineering can be used in a quantum context. By using lasers and beam splitters within a chip circuit, researchers can manipulate individual photons as qubits. This method, called boson sampling, uses light to perform quantum calculations which can far exceed the performance of supercomputers. Creating such a quantum photonic chip that can do this will open the possibility of bringing quantum computers into mainstream, real-world use.

Keeping communications secure

As cyberattacks become more sophisticated and hacking tools become more powerful, quantum cryptography offers an alternative to secure sensitive information against future cyber-attacks and unforeseen technological advances.

The most well-known developed application of quantum cryptography is quantum key distribution (QKD), a method that allows two remote users – who are embedded in an untrusted network such as the internet – to exchange secret keys in the presence of an attacker who may own unlimited computing resources.

By taking advantage of the sensitivity of quantum signals, QKD chips can detect when an attacker attempts to eavesdrop on communication. The secret keys, which are transmitted as a series of quantum signals, become disturbed and will scatter if an attacker intercepts, rendering them useless.

QSec researchers have managed to develop a quantum communication chips small enough to fit into everyday devices, such as laptops or smartphones, which could lead to highly secure, encrypted communication.

Foundry-ready silicon photonics process integrates III-V lasers

TOWER SEMICONDUCTOR and Juniper Networks have announced the world's first silicon photonics foundry-ready process with integrated III-V lasers, amplifiers, modulators and detectors. This integrated laser process addresses optical connectivity in datacentres and telecom networks, as well as new emerging applications in artificial intelligence (AI), LiDAR and other sensors.

According to the market research firm Yole, the silicon photonics transceiver market for datacenters is expected to grow rapidly at a CAGR of 40 percent to reach over $5 billion in 2025.

The new platform co-integrates III-V lasers, semiconductor optical amplifiers, electro-absorption modulators and photodetectors with silicon photonics devices, all monolithically on a single chip. This enables smaller, higher-channel count and more power-efficient optical architectures and solutions.

Foundry availability will enable a broad array of product developers to create highly integrated photonic integrated circuits (PICs) for diverse markets.

Process design kits are soon to be available and the first open multi-project wafer run is expected to be offered early this year.

First samples of full 400 Gbit/s and 800 Gbit/s PIC reference designs with integrated laser are expected to be available in the second quarter of 2022.

"Our mutual development work with Tower has been extraordinarily successful in qualifying this innovative silicon photonics technology in a high-volume manufacturing facility," said Rami Rahim, CEO of Juniper Networks. "By offering this capability to the entire industry, Juniper offers the potential to radically reduce the cost of optics while lowering the barrier to entry for customers".

"Our partnership with Juniper on silicon photonics is bringing a paradigm shift for product development across our industry," said Russell Ellwanger, CEO of Tower Semiconductor.

"It is now possible to mix the advantages of III-V semiconductors with high-volume silicon photonics manufacturing. Being the singular open market, integrated laser silicon photonics platform, and having a multi-year advantage over any potential foundry competitor, we are jointly creating breakthrough products with truly unique value for our industry and for society as a whole".

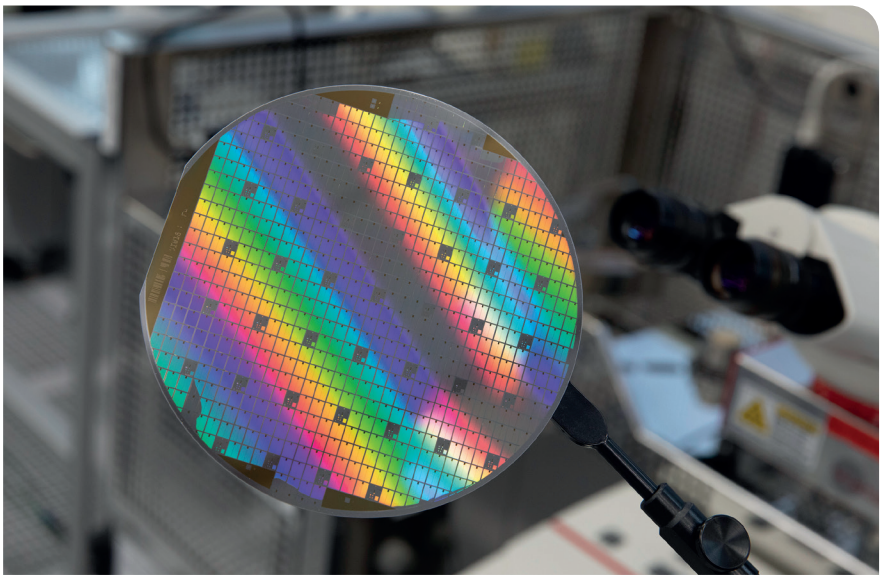
Bosch gives go-ahead for volume production of SiC chips

AFTER several years of development, Bosch is now starting volume production of SiC power semiconductors. “The future for silicon carbide semiconductors is bright. We want to become a global leader in the production of silicon carbide chips for electromobility,” says Harald Kroeger, member of the board of management of Robert Bosch.

Two years ago, this supplier of technology and services had announced that it would push ahead with the development of SiC chips and enter production. For this, Bosch developed its own manufacturing processes, which it has been using since the beginning of 2021 – initially as samples for customer validation. “Our order books are full, thanks to the boom in electromobility,” Kroeger says.

In the future, Bosch intends to expand its production capacity for SiC power semiconductors to a unit volume running into the hundreds of millions. With this in mind, the company has already started expanding the clean-room space at its Reutlingen plant. In parallel, work is also being done on the second-generation of SiC chips, which will be even more efficient and should be ready for volume production as of this year.

Bosch is receiving support for the development of these innovative manufacturing processes for SiC semiconductors from the German Federal Ministry for Economic Affairs and Energy as part of the *Important Project of Common European Interest Microelectronics* programme.



“For several years now, we have been providing support to help establish semiconductor production in Germany. Bosch’s highly innovative semiconductor production strengthens the microelectronics ecosystem in Europe and is a further step toward greater independence in this key field of digitalisation,” says Peter Altmaier, Germany’s Federal Minister for Economic Affairs.

In order to meet steadily increasing demand for SiC, Bosch added an extra 1,000 m^2 to the clean-room space at its wafer fab in Reutlingen in 2021. Another 3,000 m^2 will be added by the end of 2023. The new space will house state-of-the-art production facilities for manufacturing SiC semiconductors using processes developed in-house. To achieve this, Bosch’s semiconductor experts are building on their decades of expertise in chip manufacturing.

In the future, the company plans to manufacture the semiconductors on 200 mm wafers. Compared with today’s 150 mm wafers, this will deliver sizeable economies of scale. After all, it takes several months for a single wafer to pass through several hundred process steps in countless machines. “By producing on larger wafers, we can manufacture significantly more chips in one production run and thus supply more customers,” Kroeger says.

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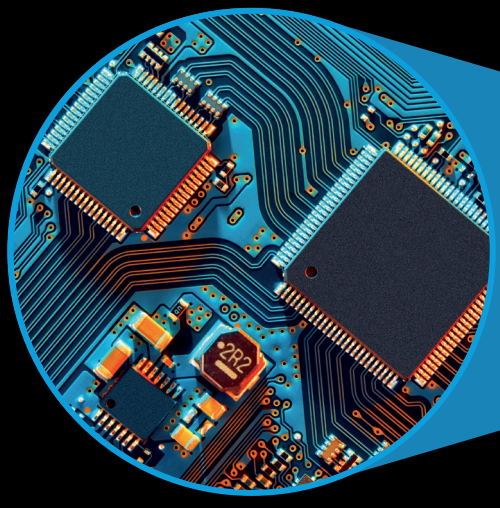

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ANGEL EVENTS

AMS Osram unveils brightest LED for car front lights

Last month, Ams Osram unveiled what it believes is the brightest LED currently available on the market for automotive front lighting.

The Oslon Black Flat X offers 460 lumens at 1 A and is available in a 1-chip and 2-chip variant. In mid-2022, the family will expand to include various multichip variants, enabling headlamp manufacturers to create cost-effective LED headlamp designs

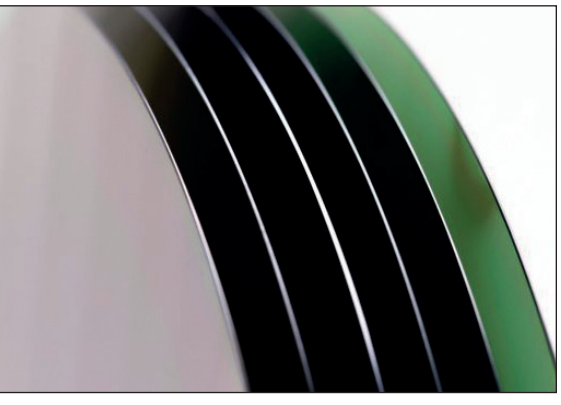
"The Oslon Black Flat product family has been an ideal solution for high-quality and at the same time cost-optimized headlamp designs for many years," said Philipp Puchinger, marketing manager Automotive Exterior at Ams Osram. "With the two new products in the Oslon Black Flat X line, Ams Osram is once again underlining its innovation leadership in automotive lighting."

The surface-mountable components can be processed easily in manufacturers' standardised production processes. In addition to its brightness , the 1-chip variant is characterised by its compact dimensions of 3.75 mm by 3.75 mm. The special QFN platform of the LEDs enables customers to perform simple thermal management. Depending on the system, heat sinks can be significantly reduced in size or even eliminated altogether. The Oslon Black Flat X family's leadframe package also achieves a lower thermal resistance than the leading ceramic packages in this context to date. Together with a special TiO_2 encapsulation, the black package of the LEDs delivers high contrasts of 1:200. In addition, the new components are characterised by a very homogenic colour over angle radiation.

A*STAR and Soitec announce SiC research collaboration

The Institute of Microelectronics (IME) at the Agency for Science, Technology and Research (A*STAR) and the semiconductor materials firm Soitec have announced a research collaboration to develop next-generation SiC semiconductor devices to power electric vehicles and advanced high-voltage electronic devices.

Under the collaboration, the parties will leverage Soitec's proprietary technologies such as Smart Cut and IME's pilot production line to create 200 mm diameter SiC semiconductor substrates.



The joint research will contribute towards developing a holistic SiC ecosystem and boost semiconductor manufacturing capabilities in Singapore and the region. The research collaboration is planned to run until mid-2024, and aims to achieve the following outcomes: first, to develop SiC epitaxy and MOSFET fabrication processes for Smart Cut SiC substrates to produce higher quality microchip transistors with less defects and enhanced yield during the manufacturing process; and second, to establish a benchmark for SiC power MOSFET devices fabricated on Smart Cut SiC substrates and demonstrate the advantages of the process with conventional bulk substrates.

"This joint research between A*STAR's Institute of Microelectronics and Soitec to develop next-generation semiconductor devices using innovative technologies is made possible by both organisations' deep capabilities in R&D," said Terence Gan, executive director of IME. "We look forward to working together with Soitec to add value to the local R&D ecosystem and the growing pool of SiC players in the semiconductor industry," he added.

"This is a great opportunity for us to partner with Singapore's Institute of Microelectronics and demonstrate SmartSiC substrate's scalability to 200 millimetre," said Christophe Maleville, CTO and senior executive VP at Soitec.

"The collaboration paves the way for the development of advanced epitaxy solutions to produce higher quality silicon carbide wafers with energy-efficient characteristics, given the exciting potential of this material. As the main beneficiaries of this new process, the semiconductor ecosystem in Singapore will be given the opportunity to validate the superior energy efficiency of the silicon carbide wafers produced through our collaboration."

Soitec acquires Novasic to strengthen SiC wafer tech

Grenoble-based Soitec has acquired Novasic, a French company specialised in polishing and reclaiming wafers on SiC. The acquisition allows Soitec to drive the development of semiconductors for power supply systems in electromobility and industrial applications. In a strategic move to address the need of the automotive and industrial markets for performance and energy efficiency, Soitec is expanding its product portfolio beyond silicon-on-insulator (SOI) with SiC. This crystal material unlocks greater performance, optimized design and lower environmental impact for power electronics, making it a perfect fit in particular for electric vehicles and other power efficient applications.

SmartSiC substrates, resulting from the application of Soitec's patented proprietary technology SmartCut to SiC, will enable new levels of performance and energy efficiency compared with traditional bulk SiC, through higher donor wafer re-usability, improved yields and lower die sizes.

In addition to reducing SiC's environmental impact in its production process, SmartSiC will be a catalyst to accelerate the adoption of electric vehicles. SmartSiC is currently at the prototyping level for devices with several key partners.

Established in 1995, Novasic provides state of the art wafering, reclaiming and polishing services for high performance semiconductors and industrial crystals to laboratories and industrial customers, with a particular focus on SiC.

The company has developed innovative polishing processes allowing enhanced device performance with a scratch free, low roughness, ultra-clean epiready surface, and no damaged layers.

With the acquisition, Didier Marsan, CEO of Novasic and international expert will become senior technical advisor for Soitec.

"Soitec's SmartSiC substrates will be the backbone of energy-efficient electromobility," said Bernard Aspar, COO of Soitec.

"The acquisition of Novasic and the integration of its expertise in wafering, polishing and reclaiming brings the latest technology building block for Soitec to deliver an optimal final product and prepare the industrialisation phase of our SmartSiC product line. The expertise of Novasic will help us further accelerate the go-to-market and adoption of our smart SiC applications in the promising and demanding automotive and industrial markets."

EPC demo boards for rad hard GaN

EPC SPACE has announced the availability of a family of easy-to-use demonstration boards to help designers quickly and easily implement radiation hardened (rad hard) GaN power devices into their high reliability and aerospace applications.

The new family of demonstration boards is said to offer fast prototyping and evaluation of the features and capabilities of EPC Space Rad Hard eGaN power devices.

The offering includes three low-side driver demo boards, EPC7C001, EPC7C002, EPC7C003, which use the EPC Space's eGaN gate driver modules to drive a corresponding 40 V, 100 V, or 200 V discrete eGaN FET.

There is also the EPC7C005 demonstration board that allows evaluation of the switching operation and conversion efficiency performance of the FBS-GAM02-P-C50 Rad Hard power module connected as a half-bridge point-of-load (POL) output stage.

Finally, there the EPC7C006 demo board, which is a three-phase motor demonstration board that uses the FBS-GAM02-P-R50 module.

"Radiation Hardened eGaN FETs and ICs offer designers improved performance, lower cost, and shorter delivery times compared to rad hard silicon-based devices," said Bel Lazar, CEO of EPC Space. "We are happy to provide an easy-to-use evaluation platform to assist designers looking to convert their rad hard silicon designs to take advantage of the higher power densities, higher efficiencies, and better cost and delivery that GaN offers."

Navitas GaN IC powers new Vivo smartphone

Navitas has announced that its next-generation GaNFast power IC drives the 120 W ultra-fast charger supplied 'in-box' with Vivo's iQOO-brand flagship iQOO 9 Pro mobile phone.

The 9 Pro's 4,700 mAhr battery charges from 0-100 percent in 19 minutes, and at 60.5 mm by 52.5 by 28.8 mm, the charger is 26 percent smaller than the previous generation, reaching 1.3 W/cm^3 power density. It weights 135 g.

Vivo's director of charger development, Xiaohong Zhang, commented on the release of the product: "We are excited to use Navitas Semiconductor's autonomous, next-generation GaN power ICs in the new 120 W ultra-fast mini charger to power Vivo's iQOO-brand flagship model, the iQOO 9 Pro. By successfully integrating Navitas' new GaNFast technology into this mobile phone charger, we will bring a lighter and faster charging experience to iQOO consumers and enhance the consumer experience in all aspects."

Navitas' GaNSense technology integrates real-time fast sensing of system parameters, including current and temperature, and achieves patent-pending lossless current-sensing. Integrated GaNSense products are said to be six times faster than discrete GaN power chips, and take only 30 ns from detection to protection.

"Navitas is honoured to help Vivo's iQOO 9 Pro launch with this 120 watt super mini ultra-fast charger. GaNFast power ICs with GaNSense technology enable significant upgrades in speed, weight and power density," said Gene Sheridan, Navitas' CEO and co-founder.

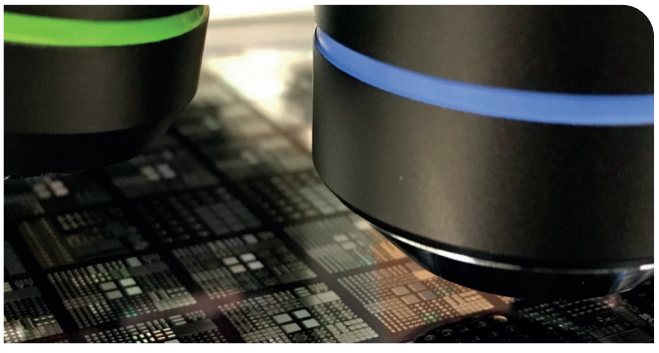
Aixtron says YESvGaN

EPITAXY SPECIALIST Aixtron has announced that it is a partner in the EU 'YESvGaN' (Vertical GaN on Silicon: Wide Band Gap Power at Silicon Cost) research project, which aims to develop highly efficient power transistors based on a novel process technology for large-scale industrial production.

The 'YESvGaN' consortium estimates the potential electricity savings by the consistent use of such YESvGaN vertical membrane GaN transistors in the EU in 2030 to be equivalent to the power output of seven nuclear power plants or ten coal-fired power plants.

For the development of vertical GaN power transistors with silicon as substrate, the consortium will be relying on the epitaxy expertise of Aixtron SE. This is because for this newly developed power device, GaN must grow over a large area in the form of crystalline layers on a suitable substrate such as a silicon wafer.

In order to further drive the market penetration of GaN-based devices, Aixtron is also testing epitaxial growth on epi-wafers with 300 mm diameter as part of the 'YESvGaN' research project; currently, MOCVD technology is primarily used for crystalline growth on 150 mm to 200 mm wafers. For the deposition of GaN layers on 300 mm silicon substrates, the deposition systems specialist is developing the required equipment.



"GaN power transistors on silicon wafers provide us with the intriguing opportunity to combine about 15 percent higher power density in GaN compared to silicon with the cost advantages of the established silicon technology. The performance is thus expected to exceed that of modern silicon carbide MOSFETs at chip costs rivalling those of silicon IGBTs," says Michael Heuken, VP Advanced Technologies at Aixtron SE.

'YESvGaN' partners include Bosch, Ferdinand-Braun-Institut, Leibnitz Institute for Highest Frequency Technology, Fraunhofer Institute for Integrated Systems and Device Technology, Finepower, X-FAB, NanoWired and Siltronic, Centre national de la recherche scientifique CNRS, Ion Beam Services, STMicroelectronics, EpiGan, Universiteit Gent, EV Group, Materials Center Leoben Forschung, Hexagam, Linkopings Universitet, Smart Induction Converter Technologies, Universitat de Valènciam Aurel, Consorzio nazionale interuniversitario per la nanoelettronica, and Raw Power.

UV LEDs post pandemic?

THERE WILL BE a 'before' and 'after' the Covid-19 pandemic for the UV lighting industry according to Joël Thomé, CEO of Piseo, which has combined its expertise with Yole to look at trends in the UV LED industry.

"The health crisis due to the SARS-CoV-2 virus has generated unprecedented demand for the design and manufacture of disinfection systems using optical UV rays. LED manufacturers have seized this opportunity, and we are currently seeing an explosion in UVC LED products," said Thomé.

The UV LEDs and UV Lamps – Market and Technology Trends 2021 report from Yole is a survey of UV light sources and the overall UV LED industry. In parallel, the *UVC LEDs in the Time of Covid-19 - Update November 2021* from Piseo discusses the technical state-of-the-art of UVC LEDs and possibilities for further development of performance and price. This technical analysis offers a comparative overview of the products of the 27 leading UVC LED manufacturers.

UV lamps are historic, established, and mature technologies in the UV lighting market. Business before the Covid-19 pandemic was driven mostly by polymer curing with UVA wavelength light and water disinfection with UVC light. On the other hand, UV LED technologies are still emerging. Until recently, business was mostly driven by UVA LEDs. It was only a few years ago that UVC LEDs reached the performance and cost specifications of early adopters and started generating revenue.

According to Pierrick Boulay, senior technology and market analyst, solid-state lighting at Yole: "Both technologies will benefit, but on different timelines. In the very short term, UV lamps might dominate end-systems because they are already established and easy to integrate. However, this proliferation of applications is a catalyst for the UV LED industry that will further push the technology and its performance forward. In the middle-to-long term, several end-systems might further adopt UV LED technology".

Pandemic demand

The UV lighting market overall was worth around $400 million in 2008. By 2015 UV LEDs alone were worth $100 million. In 2019, the total market reached $1 billion as UV LEDs spread into UV curing and disinfection. The Covid-19 pandemic has then driven demand, increasing total revenues by 30 percent in just one year. In this context, Yole's analysts expect the UV lighting market to be worth $1.5 billion in 2021 and $3.5 billion in 2026, with a 17.8 percent CAGR from 2021 to 2026.

Numerous industries and players supply UV lamps and UV LEDs. Signify, Light Sources, Heraeus, and Xylem/Wedeco are the top four UVC lamp players, while Seoul Viosys and NKFG are currently leading the UVC LED industry. There are few overlaps between the two industries. Yole's analysts expect this to remain the case even though some UVC lamp players, such as Stanley and Osram, are diversifying their activities into the UVC LED field.

Overall, the UVC LED industry is likely to be the most transformed by recent trends. The industry has waited for more than 10 years for this moment to happen. All the players are now ready to grab a piece of this booming market.

UVC LED-related patents

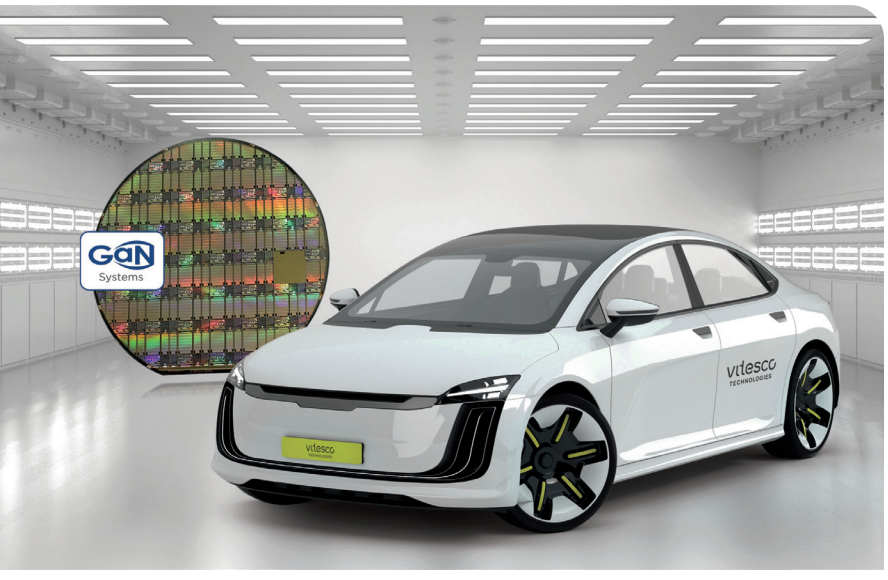
The number of UVC LED-related patents filed in the last two years has exploded, thereby illustrating the dynamism of research in this area, states Piseo. In its new UVC LED report, Piseo offers a particular focus on key patents of four LED manufacturers. This selection highlights the main challenges of the rollout of this technology: intrinsic efficacy and cost. Yole also offers a complementary analysis of the patent landscape. The need for disinfection and the opportunity to use small light sources enabled the creation of increasingly compact systems. This evolution, including new form factors, has clearly generated renewed interest on the part of LED manufacturers.

GaN Systems:
Ready for volume production

With its sights set on EVs, device chargers and data centres, GaN Systems is primed for mass markets, reports **REBECCA POOL**

FOR JIM WITHAM, chief executive of Canada-based GaN Systems, one of the biggest success stories of 2021 centred on electric vehicles. As the pandemic gathered momentum and global car sales plummeted, the electric vehicle market proved to be remarkably resilient. Policy support relating to emissions cuts remained strong while battery costs fell. And as Witham puts it: "Eighteen months ago, many were dabbling in electric vehicles but now the OEMs are saying, '100 percent of my cars are going to be electric by this year'. The world was really gone for electric vehicles."

This spells good news for manufacturers of both GaN and SiC devices, as industry developments indicate. For example, in late 2020, Cree, now Wolfspeed, stepped out of the LED light and is now churning out SiC components and systems for electric vehicles, as well as GaN RF products for defense and communications applications. At the time, Chief executive, Gregg Lowe, told *Compound Semiconductor*: 'I have to say, this is a great time to be a silicon carbide company'. Since this time, Wolfspeed and other players – including SananIC, Rohm, II-VI and Infineon – have been signing deals with auto-OEMs and investing millions to billions of dollars in SiC capacity to snare their share of this burgeoning market.



Likewise, GaN manufacturers have been busy in this sector. GaN power devices from Innoscience of China are being used in EV wireless chargers, US-based Navitas is working with Switzerland-based EV subsystem supplier, Brusa, and recently opened a GaN IC design centre dedicated to EVs, while Power Integrations, US, has been releasing auto-qualified high-voltage GaN ICs for EVs.

Along the way, GaN Systems has received investment funds and amassed contracts from auto-makers and EV-related firms, including BMW, Toyota, Canada's GaN powertrain developer, FTEX, and EV powertrain systems supplier, Vitesco Technologies, Germany. A recent $150 million investment comes from BMW i Ventures, Vitesco and other players.

Witham asserts there is space for both GaN and SiC technologies in the EV market, but believes GaN will lead in high frequency applications, such as onboard charging and DC-to-DC conversion, while both GaN and SiC could well come into their own in the traction inverter.

"Silicon carbide is great with very high voltages and powers, and preferred in, say, electric buses, trucks and muscle cars, while GaN is the favoured option in sedans and the vehicles you drive around town," he adds.

However, Witham also believes that GaN production hasn't been facing the same capacity constraints as SiC. When GaN Systems signed its capacity agreement with BMW in September 2021, the company's guaranteed volumes were cited as a key draw to the contract. Indeed, after shipping its 20 millionth transistor in February 2021, the company revealed its goal to complete a 40-fold capacity expansion by the end of the year, which it has now met.

"Capacity has been a huge issue for silicon carbide, but less so for gallium nitride, as we can increase capacity in increments with smaller capital expenditures," says Witham. "In the world of LEDs, you will literally see thousands of MOCVDs from companies like Aixtron and Veeco in factories in Asia."

"We use the same equipment and are repeating the expansion in Power GaN – TSMC is our primary and long-time foundry partner, and through our joint plans, we put more machines in place, expand our capacity and keep our lead times short," he adds. "We've already proven we can ramp up production and supply the demand of our customers, and there's much more to come."

Meeting market standards

But what about the nagging issue of reliability? In line with other industry players, Witham says GaN device reliability is well and truly proven, and highlights his company's test and qualification methodology, AutoQual+, that ensures transistors meet stringent market standards.

Pointing to data supplied by some companies in the SiC market, he also highlights: "Some [firms] co-mingle their reliability data from a silicon carbide diode, which has been shipping for a long time, with that from a [silicon carbide] transistor, which hasn't shipped for so long. [These devices] are very different beasts with very different failure modes."

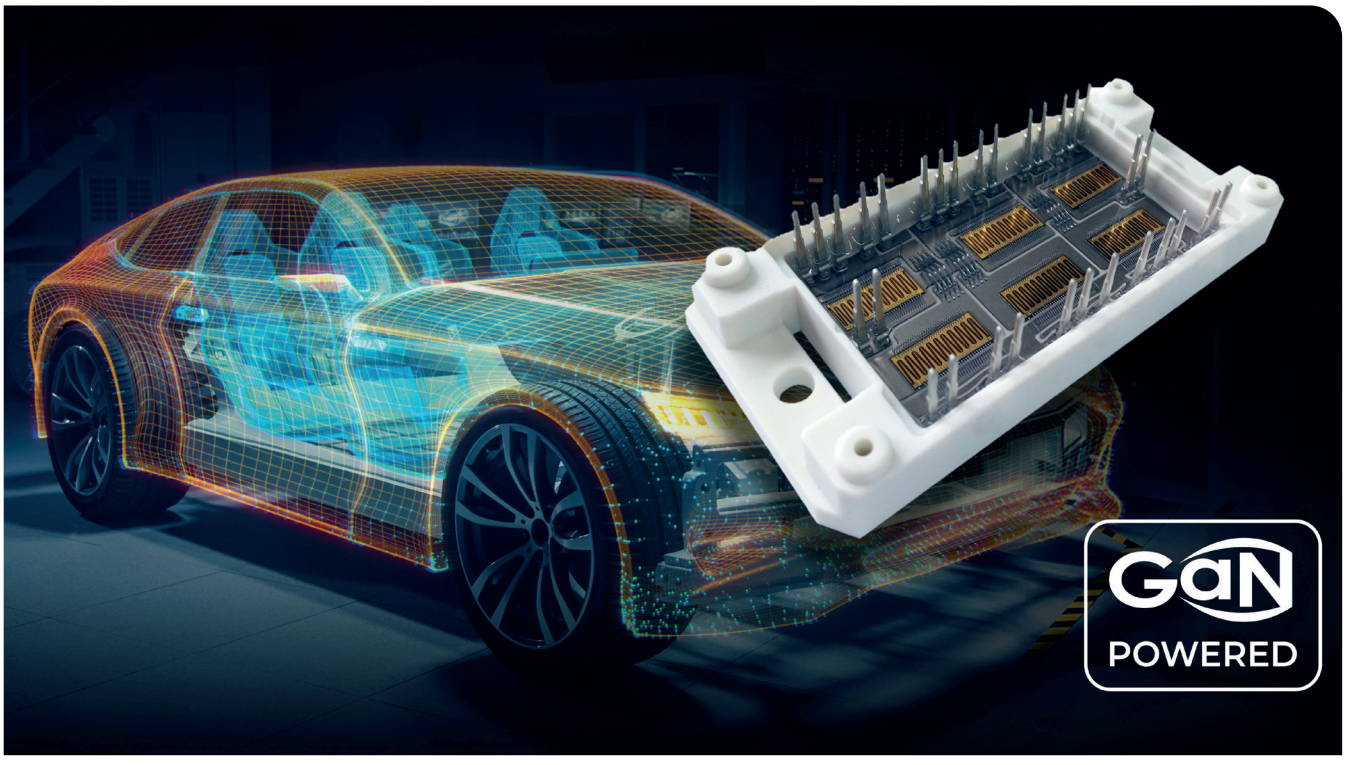
"I challenge the silicon carbide transistor companies to publish their transistor-only lifetime data and show that it can compete with the outstanding reliability of GaN Systems transistors," he adds.

With capacity in place and customer confidence high, GaN Systems now plans to hire more employees to fulfil its growth plans – according to Witham, office space will triple in Ottawa and Taiwan. At the same time, more products are in the pipeline for mobile device chargers, audio amplifiers and data centre power supplies.

In January 2022 alone, the company released a 250 W AC/DC GaN charger reference design for consumer electronics devices as well as its Generation 2 audio amplifier and power supply reference design. "Today revenues are driven by these markets but come 2024 to 2026 we'll also see an explosion of GaN inside vehicles," says Witham.

"A long time ago I built a team of power electronics veterans that came from many of the big power semiconductor companies and knew how to satisfy the big customers," he adds.

"In the next decade, we're going to see GaN becoming the major player and the major transistor in power systems - we're now going to make sure that more than the fair share of those transistors are from GaN Systems."



Navitas:
Plans for GaN dominance

Recent analysis indicates that Navitas is now the market leader of GaN power devices. **REBECCA POOL** talks to Stephen Oliver, Vice President of Investor Relations, about the company's progress, products and plans.

Q *Tell us how it's been to work with GaN so far.*

A I would say that 2021 is the year when the world really 'got' gallium nitride. We're a young company – only 7 years old – but we're also a bunch of 'old engineers'. A lot of us worked together at International Rectifier back in the 80s, 90s and 2000s before it went its different ways to Vishay and then Infineon.

GaN certainly went through a troubled adolescence but by the late-2000s, Alex Lidow, who had left International Rectifier and launched EPC in 2007, was pioneering low-voltage, enhancement-mode discrete gallium-nitride-on-silicon FETs, using Episil, Taiwan, as the foundry supplier. He did a lot of heavy-lifting with quality and reliability proof-points, so when Navitas delivered high-voltage gallium nitride power IC prototypes in 2014, and went into mass production in 2018, the enhancement-mode platform was already accepted.

➤ Stephen Oliver (centre) with Dan Kinzer, Co-Founder and Chief Technology Officer/Chief Operating Officer (left), and Gene Sheridan, Co-Founder and Chief Executive Officer, at Navitas Semiconductor, US.

Q *Your GaN power ICs combine several power electronics functions onto a single GaN chip – why take an integrated approach?*

A GaN is awesome, but it has its Achilles heel – the weak gate structure. This requires external silicon-based drive and control, which increases costs, [device] size, energy losses and also inhibits gallium nitride's high-speed performance. So, we set out to deliver an easy-to-use, 'digital-in, power-out' gallium nitride power IC which fully protects the gallium nitride gate, and optimizes the system for performance and reliability. I would say the majority of power designers struggled with discretes, but then tried the Navitas 'Lego brick' approach and liked it.

Q *You recently signed a strategic deal with Anker to co-develop next-generation chargers. How has your partnership helped to drive gallium nitride power ICs forward?*

A We've been working with Anker since 2017, with our GaNFast power ICs being used in Anker's PowerCore Fusion PD combination charger and portable power bank from 2019. This was certainly a turning point for Navitas, and the first GaN device to appear in the Apple Store.

Our latest partnership is a formalisation of the relationship, and we will second Navitas-badged engineers to Anker, and this will decrease the time-to-prototype and increase the chance of 'right-first-time'. Anker will be in the first wave to sample new prototypes – it's a great two-way relationship, and we believe Anker is one of the most technically-aggressive of the aftermarket charger companies.

Q *Your winning market right now is mobile fast chargers – how is this going?*

A We went into production in 2018 and our technology is now in 160 different charging products from different companies. We've got another 150 chargers in the pipeline and these will come out by the end of 2022. We announced our third generation GaNFast power ICs with GaNSense technology a month ago – it was already in mass production 'undercover' with Lenovo and Xiaomi. We also have partnerships with Dell, OPPO, LG, Amazon, and others – overall we're working with more than 90 percent of OEMs that are supplying phones, laptops and tablets. When it comes to gallium nitride, we don't have to 'handhold' now, designer engineers are just running with the technology.

Q *What markets are next?*

A We expect that the majority of revenues to 2023 will come from fast charging. But this month, we're sampling another 'next-generation' of gallium nitride power ICs into solar, datacentre and electric-vehicle applications. They each have a slightly different gestation period centred around qualification time, but by the end of 2023 we expect to see revenues from datacentre and solar applications kicking in. We're looking for our first electric vehicle revenues for model-year 2025, and by 2027, electric vehicles applications will probably provide our fastest, growing revenues.

Q *TrendForce indicates Navitas holds the greatest market share of GaN power device suppliers in 2021 – is this thanks to the fast-charging market?*

A The trend in smartphones is for higher power so this means that legacy companies with lower-power charger designs are struggling to provide devices that operate at higher frequencies and powers. The 5-to-10 watt low-power market won't disappear completely, but most companies such as Xiaomi, Oppo, Vivo, and Realme are more aggressive on charging speeds, which increases the power requirement [of a device]. Around 2 billion chargers are sold every year for phones, laptops and tablets, and the average price for one of our chips to go into one of these chargers is about $1. This means there's a $2 billion market today just in fast mobile chargers. Right now, gallium nitride has around 2 percet market share with the rest belonging to legacy silicon chips. This is going to give us a lot of growth in fast charging.

Q *What are your thoughts on competition from InnoScience and other China-based players?*

A In total, there are probably a dozen companies with gallium nitride programs right now, with a few of those from China. These market-entrants validate gallium nitride's maturity and value to markets. This is the Wild West and it's kind of a land grab for market share right now – we estimate the gallium nitride market could be worth more than $2 billion by 2026, so there's a lot of room for a multiple companies to be profitable.

Q *Do you think Navitas can retain market dominance?*

A Obviously we want to do this, and we have a three-prong approach to maintaining and extending our lead; a strong, 130 plus patent 'wall', a proprietary process design kit, and a very fast innovation rate. We have twin IC design centres in El Segundo and Shanghai, as well as application design centres, including our new centre in Hangzhou, China. Today, the majority of our revenue comes from China, so being close to customers is critical. We're introducing a new generation of GaN power IC every 10 or 12 months and have a multi-year lead. We've also gone from being around 100 people at the start of 2021 to some 170 people – so yes, we think we can maintain our market dominance.

This is the Wild West and it's kind of a land grab for market share right now - we estimate the gallium nitride market could be worth more than $2 billion by 2026

Q *You process wafers with TSMC – what wafer sizes are you working with?*

A Gallium nitride is an extremely advanced material, yet can be processed on old, low-cost, 350 nanometre equipment. We use TSMC's 'Fab 2' in Hsinchu, Taiwan, for wafers. This is the oldest fab that TSMC still has running, and has plenty of capacity. We're working on six-inch wafers, and will do until 2022 – we will transition to larger wafer sizes at the right time. Even pre-Covid, we went to TSMC and said "Here's our aggressive forecast," and they said, "OK, we'll match that plus extra capacity on top." We have high capacity and high yields, and can provide new gallium nitride technology with only 12-week lead-times, way less than the 30-, 40- and 50-week extended lead-times for silicon devices.

Q *Can gallium nitride compete with silicon carbide?*

A Silicon carbide is great for extreme high-power, high-voltage applications and is 10 to 15 years more mature than gallium nitride, and therefore more accepted. But take a look at our recent partnership with Swiss electric-vehicle-subsystem supplier, Brusa, to accelerate electric-vehicle adoption. The company has publicly said that it was using silicon, is now using silicon carbide, but will move togallium nitride for its onboard chargers. Silicon carbide switches are great for high-power, high-voltage, relatively slow-switching speed applications like a wind turbine or electric locomotive. But if you have a four-passenger vehicle, with in-wheel, four-wheel-drive, then that's a great application for gallium nitride. So the real battleground for gallium nitride and silicon carbide is going to be with traction inverters and motor drives.

Infrared laser spectroscopy at your fingertips

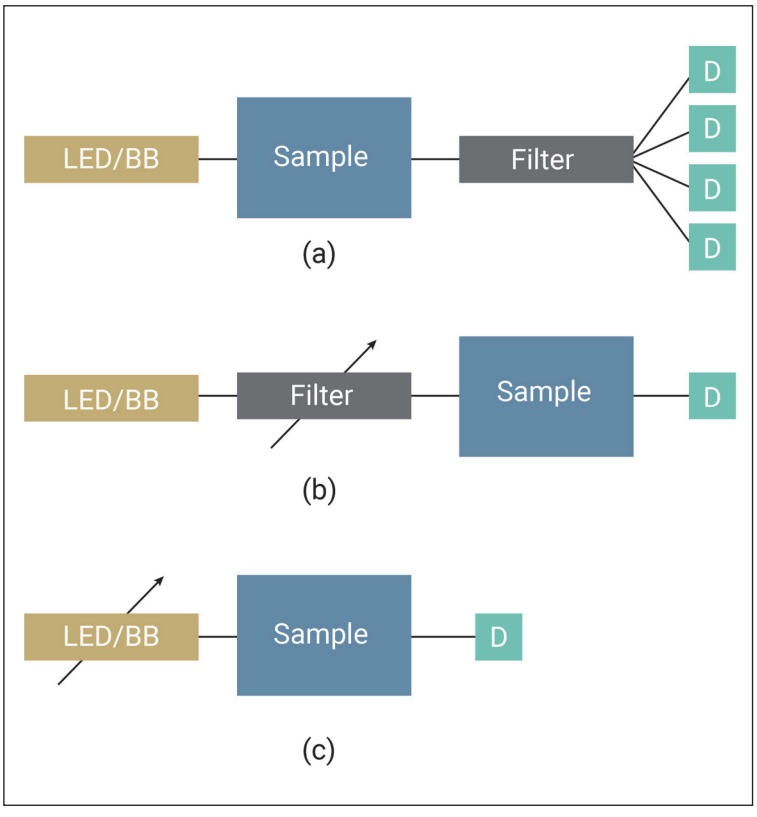
Sensing applications take a big step forward, thanks to a photonic chip spectrometer that delivers the performance of a table-top laboratory instrument

BY AUGUSTINAS VIZBARAS FROM BROLIS SENSOR TECHNOLOGY

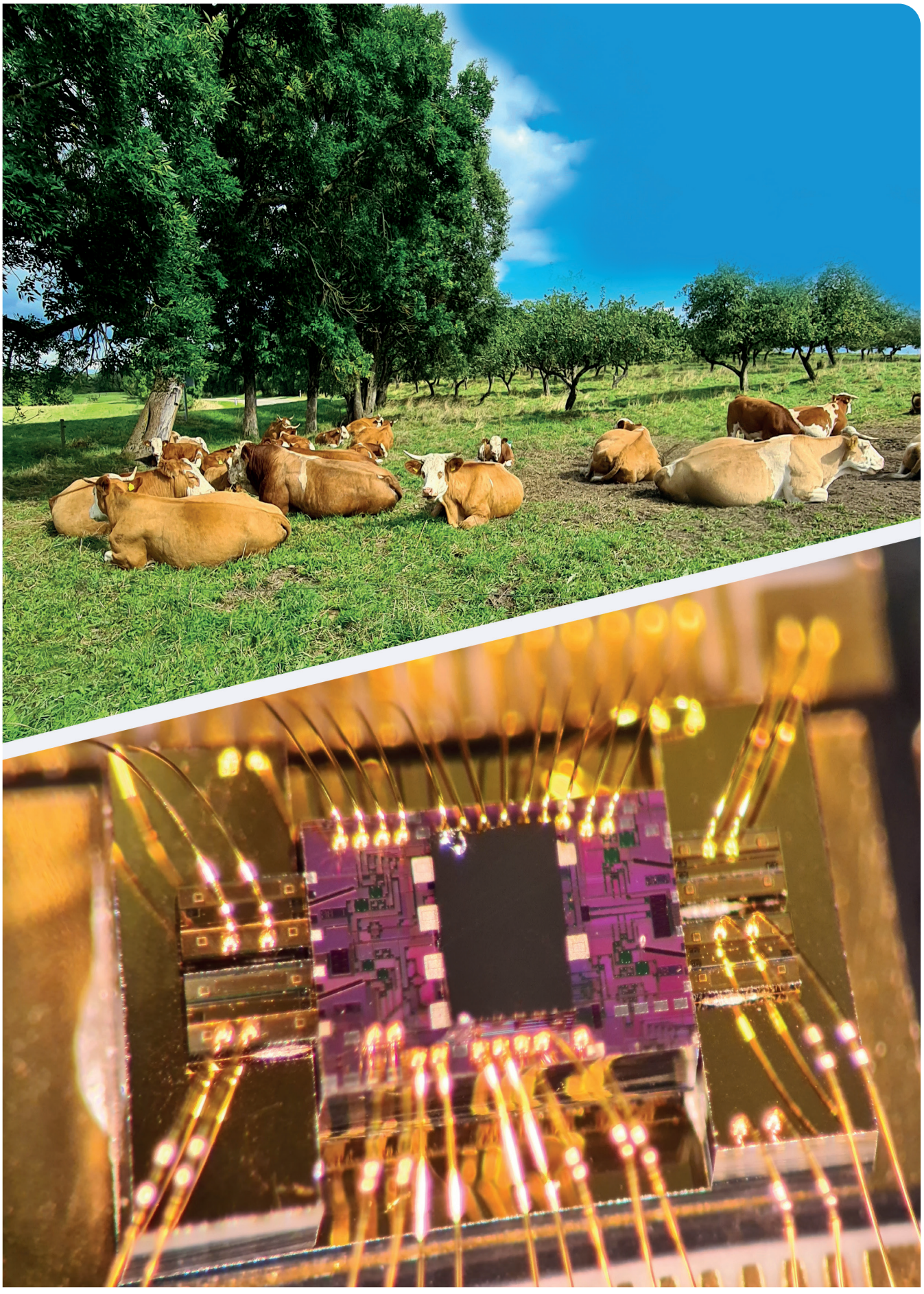
DEVELOPED during the first half of the twentieth century, infrared spectroscopy has established itself as an effective, widely adopted laboratory technique for analysing organic and inorganic compounds. By measuring the interaction of matter with infrared radiation, this form of spectroscopy can identify compositions of substances, determine the presence and absence of chemical species, and offer quantitative and qualitative analysis. When radiation is directed at a substance, the photons that are absorbed have energies coinciding with vibrational frequencies that are molecule specific. Since every different molecule has a unique molecule-specific absorption spectrum, it is possible to identify species and measure their concentrations within a sample.

The tremendous insight garnered from infrared spectroscopy has led to the use of spectrometers in numerous applications. This technique is serving in the biomedical sphere, where it is used to analyse biological fluid, tissue and pharmaceuticals; it is deployed in industrial sectors, such as those involving chemicals, bioreactors, petrochemicals and polymer technology; it is valued in environmental settings, providing the likes of gas analysis and pollution monitoring; it is found in the food industry, where it provides trace element detection and unveils composition; and it also serves in agriculture and veterinary applications.

So common is infrared spectroscopy that it is found in every governmental, regulatory or industrial laboratory, providing a gold standard. Note that instrumentation takes many forms, from the universal



➤ Figure 1. The basic principles of infrared spectroscopy, when measuring a sample in a transmission configuration. Orientations include: (a) a broadband light source and a static filter, (b) a broadband light source with a tuneable filter, and (c) a tuneable light source. BB short for the broadband light source, Sample is the object under investigation, Filter is the spectral filter/wavelength discriminator, and D is the detector of radiation.



	Light Source	Remarks
Type	GaSb/Si widely tunable laser	Hybrid external cavity laser, all electronic tuning. No moving parts
Wafer Size	3-inch, transition to 4-inch	Brolis is moving to 4-inch platform in the next 2 years
Growth Technology	MBE	Lattice-matched, mainly bulk layers
Spectral Bandwidth	~120-140 nm/channel	Currently limitation on the silicon side. GaSb chips provide over 400 nm of accessible bandwidth. Future developments should lead to extend the bandwidth on silicon
Wavelength Span*	1850 – 2450 nm	GaSb can efficiently cover from 1700 nm to 3000+ nm. Standard silicon works well up to 2500 nm
Threshold current	20-50 mA	–
Input threshold power	~50 mW	–
Operating power @ 0.2 mW output	~ 120 mW	Includes gain-chip, and thermal tuner power
Output power	1-5+ mW CW	Free-space, off-chip.
SMSR	50 dB+	Limited by test instrumentation noise floor
Tuning Speed	kHz range	–

*Current BROLIS design. Upon need, can be extended.

➤ Table 1 (a). The light source, a laser, for a GaSb/silicon spectrometer-on-chip.

table-top Fourier-transform infrared spectrometer (FTIR), to different designs of laser spectrometer and Raman spectrometer.

Unfortunately, all these high-end tools are bulky and expensive, restricting their use to the lab. It would be far better to deploy them directly at sites, providing in-line, *in-situ* monitoring. However, this is too expensive, preventing the opportunity to provide better control over processing and the identification of deviations from intended processes in real-time. Instead, when infrared spectroscopy is used today, it provides results that are offline – and often off-site.

Gathering results in real-time is hugely beneficial. As well as providing immediate feedback, it unveils dynamics – that is, trends over a given period of time. Rarely or never can a trend be deducted from a single data point.

Another attractive feature of spectroscopy is its generality. This technique is capable of identifying and quantifying many different molecules. While it's crucial to adapt data algorithms for every molecule, from a hardware perspective the technology is the same and thus generic. Thanks to this, technology can be scaled, costs driven down and adoption increased. It is the choice of hardware that defines the cost, form-factor and performance. An additional decision facing the designers of spectrometers is the configuration that is used (several are shown in Figure 1).

One of the key differences between the various classes of infrared spectrometer is the technique employed for wavelength discrimination. This can be static, dynamic, or a combination of both. Which approach is taken has significant ramifications, impacting a number of system properties, including the spectral power density, the number of components, the power consumption and the footprint. The value for them may limit the level of miniaturization.

Typical state-of-the-art FTIR spectrometers command price tags between €20,000 and €70,000, have dimensions of around 1 m by 0.6 m by 0.2 m, and weigh about 30 kg. These table-top instruments feature one or more broadband light emitters, such as incandescent lamps or blackbody radiators. Such sources provide a broad emission spectrum, but this comes at the expense of a low total output power and thus a low power density. A moving-mirror interferometer ensures wavelength discrimination or filtering, while detection is performed by a single photodetector.

Another attractive feature of spectroscopy is its generality. This technique is capable of identifying and quantifying many different molecules. While it's crucial to adapt data algorithms for every molecule, from a hardware perspective the technology is the same and thus generic.

For static filtering, instrument designers may turn to prisms or arrayed waveguide gratings. These optical elements spatially separate different wavelengths, which are detected with a separate photodetector.

An alternative approach is to undertake wavelength discrimination on the laser side, using a wavelength tuneable laser. Merits of this methodology are minimising the number of components and employing the highest possible spectral power density, but there is complexity, associated with the tuneable laser. This can be in the form of an external cavity tuneable laser, which serves in the most advanced spectroscopic applications, such as cold atoms to gas sensing, and the detection of explosives and drugs. However, up until now the downsides of this approach have been the high cost and complexity of the laser, preventing this precision instrument from being deployed in many applications.

Spectrometers on a chip

At Brolis Sensors Technology of Vilnius, Lithuania, we are changing this state-of-affairs with our GaSb-based chips – they promise to revolutionize the sensing market. A year ago, in the first edition of this magazine, 2021, we detailed our path towards the realization of a spectrometer-on-a-chip with the potential to drive a paradigm shift in the sensing application domain. Twelve months on we are now in a position to share our latest advances that have propelled our technology to the doorstep of multiple markets.

Semiconductor technology is renowned for its capability to scale. This enables widespread adoption, driven by strengths that include a highly parallel technology, a low-cost potential, and an extremely small form factor. All these attributes hold for infrared spectroscopy – it has huge potential to be deployed in a wide range of applications, and drive a transformation from what is today an offsite laboratory test, directly in the field, to a real-time measurement capability. To enable this to happen, all functional blocks of the spectrometer – including the light source, the wavelength discriminator or filter, and the detector – need to be semiconductor-based technologies that can be drawn together.

When it comes to the infrared, III-Vs are ideal for producing the light source and the photodetector technologies, with different materials better suited to different spectral regions. GaAs and InP are well established in markets from consumer to datacom, while GaSb is still either overlooked or largely unexplored when it comes to real market applications. However, GaSb has the largest potential for spectroscopy and sensing applications.

Our approach involves using a widely tuneable laser, realized by the hybrid integration of a GaSb-based gain-chip with a silicon photonic integrated circuit that houses all the wavelength tuning, filtering and locking blocks. Optical signals are sent to the object under test, prior to collection by either a discrete

	Detector	Remarks
Type	GaSb based bulk type detector. *p-i-n*, *n*B*n*, or *p*B*p*	Very high quantum efficiency, lattice matched
Wafer Size	3-inch, transition to 4-inch	Brolis is moving to 4-inch platform in the next 2 years
Growth Technology	MBE	Lattice-matched, mainly bulk layers
Spectral Bandwidth	Broadband	Bulk absorber
Cut-off Wavelength	1500 – 4000 nm	By design
Responsivity	1 – 1.5 A/W	–
Detectivity	~10^{10} cm*$Hz^{0.5}$/W	For 2600 nm cut-off
Noise Equivalent Power	~10^{-12} W/$Hz^{0.5}$	For 2600 nm cut-off
On Wafer Yield	95%+	For single pixel

➤ Table 1 (b). The detector technology for a GaSb/silicon spectrometer-on-chip.

	Photonic Integrated Circuit	Remarks
Type	Silicon-on-insulator*	Standard telecom platform
Wafer Size	8-inch (200 mm) and 300 mm	Available at least in several industrial PIC foundries
Spectral Bandwidth	Up to 2500 nm at least	For SOI, as tested at BROLIS
Node	160 nm	Depends on the exact platform used

➤ Table 1 (c). The photonic integrated circuit technology for a GaSb/silicon spectrometer-on-chip.

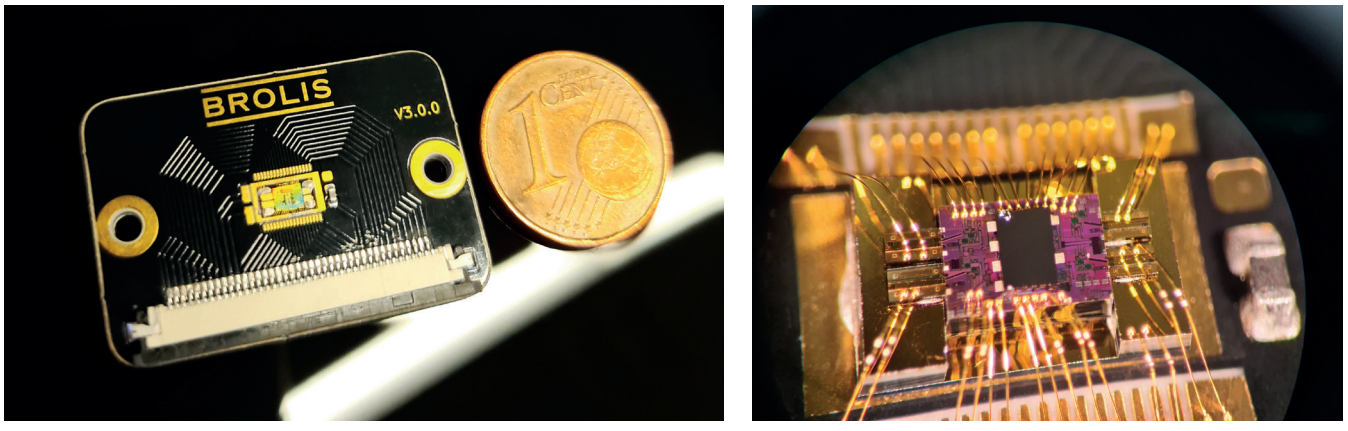
➤ Brolis runs all in-house hardware infrastructure in Vilnius, Lithuania and Ghent, Belgium.

GaSb-based photodetector or an array of them. The response of these photodetectors is optimised for the spectrum of the laser spectrometer (see Table 1 for the main technical features of the technology platform, including the necessary semiconductor-based ingredients).

One of the features of our spectrometer-on-chip is the edge-coupling of GaSb gain-chips to mode-converters on the PIC side. Optimising this coupling is not easy, demanding alignment tolerances better than 0.5 μm. We meet this requirement with integration by glue or a solder, such as AuSn. A linear array of flip-chip integrated photodiodes monitors internal signals, such as the laser output and the degree of wavelength locking.

For our initial prototype, we produced a 4-channel chip with a footprint of just 5.6 mm^2. This device provides spectral coverage greater than 400 nm (see Figure 2). It is easy to increase or reduce the number of channels so that they are suited to the final application.

We selected a 4-channel configuration to demonstrate the promise of our technology, because this provides



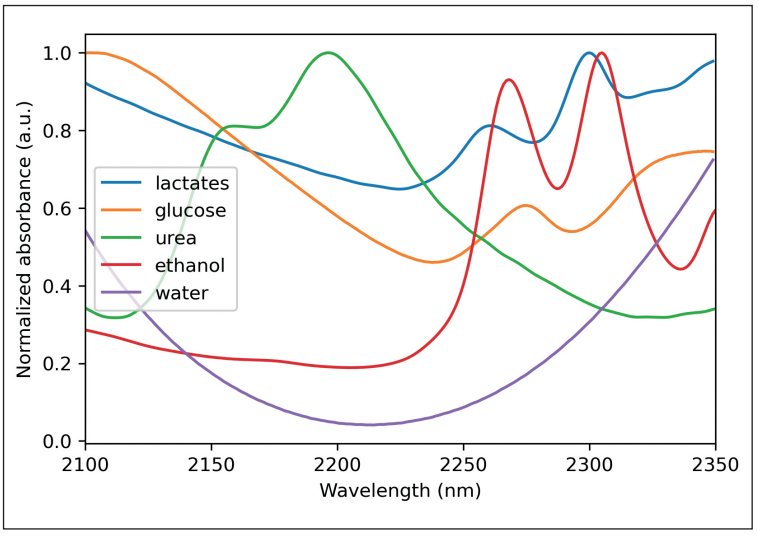
➤ Figure 2. (a) Brolis has all its in-house hardware infrastructure in Vilnius, Lithuania and Ghent, Belgium. (b) Brolis 4-channel laser spectrometer-on-chip on a PCB next to a 1 Euro cent coin (left), and a close-up of the system-on-a-chip (right). The optical output is surface-normal to the chip surface.

a spectrometer that is suitable for many applications. For instance, applications involving the sensing of liquid-phase objects, such as fluids or tissue, require a large spectral bandwidth. Typically, a bandwidth between 200 nm and 300 nm is sufficient for monitoring one or more molecules with absorption in the same spectral region. With our spectral region of choice, spanning 1850 nm to 2450 nm, we can cover various molecules, including glucose, lactate, urea, ethanol, lactose, albumin, cholesterol, milk fat and milk protein.

What's more, we can identify and monitor large-molecule compounds, as they have a specific spectral shape. This includes the likes of collagen and carotene (see Figure 3, which illustrates several different molecules falling within the spectral bandwidth of our chip). Note that by using two channels, we can sense molecules that are spectrally close together (see Figure 4).

For applications that involve spectroscopic sensing, there is a need to consider: mode purity, the scan speed or rate, how stable the wavelength is, and the power stability at a given wavelength. In addition, for handheld, wearable or battery-operated products, the output power and input power also matter.

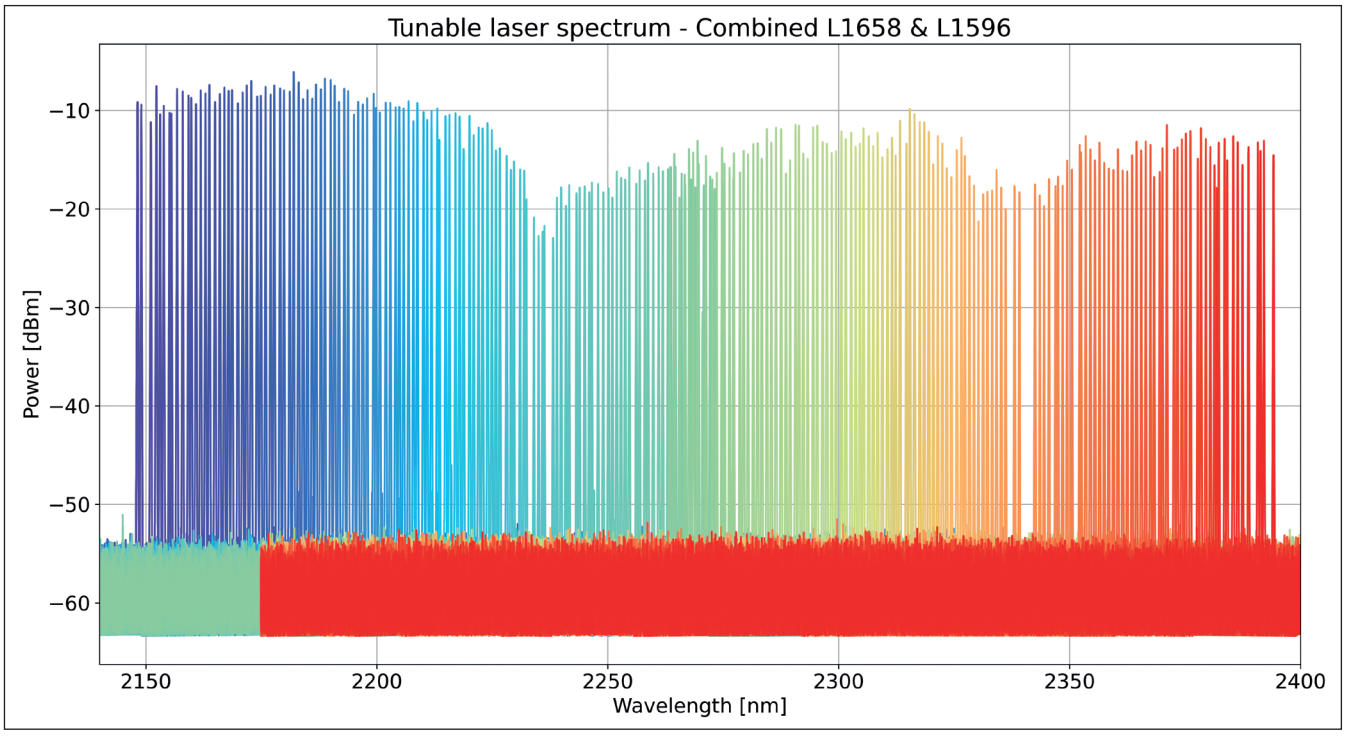
Back at the beginning of last year we were unable to offer firm answers to questions related to these considerations, because what can be accomplished hinges on the optimisation and successful combination of all layers of our technology – from the chip to the photonic integrated circuit and integration. It is only in the last few months that we have finally been able to shed some light on what those answers might be.



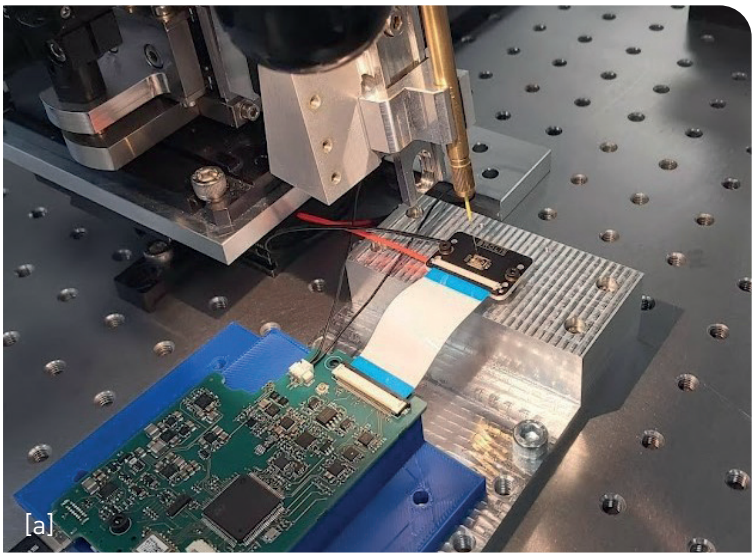
➤ Figure 3. Normalized absorbance for different molecules that fall into the Brolis spectrometer-on-chip bandwidth.

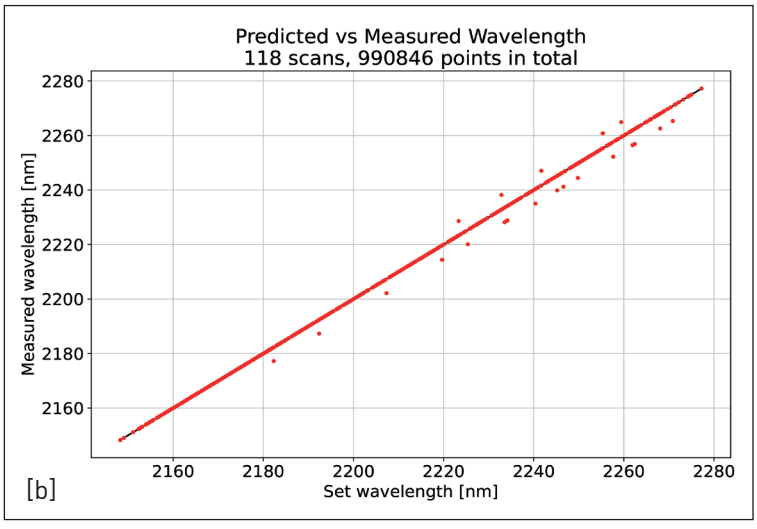
Our latest integrated spectrometer-on-a-chip provides pure single-mode operation at every wavelength. When providing fast sweeping, it takes around just 12 ms to record around 300 nm, realised with a resolution of at least 0.3 nm. By compromising speed, it is possible to provide fully continuous tuning with an additional phase control – this may be desirable for liquid or multi-gas sensing, or both.

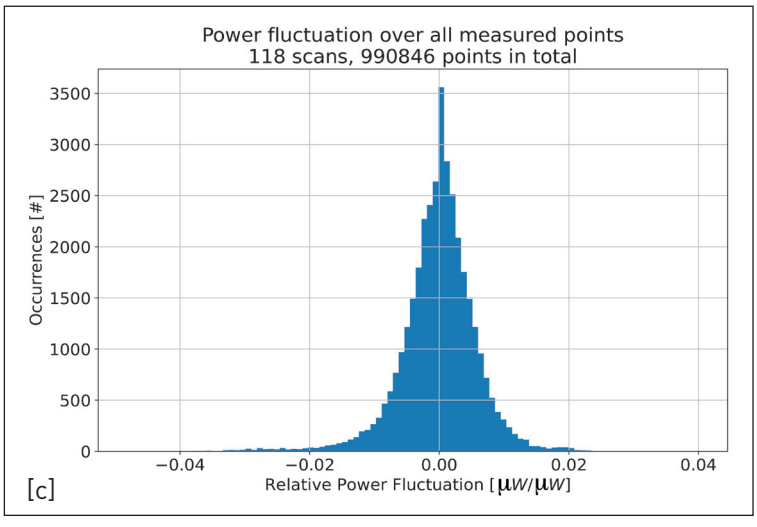
Two striking features of our spectrometer-on-chip are its stability and mode purity. The sidemode suppression ratio is maintained above 50 dB for the entire operation across a 265 nm bandwidth (see Figure 4). This is hard to beat by any table-top system or instrument.



➤ Figure 4. The spectral output of a 2-channel laser spectrometer-on-chip with a resolution of 0.3 nm.







➤ Figure 5. (a) A Brolis spectrometer-on-chip under test. (b) Spectrometer-on-chip wavelength accuracy, determined during uninterrupted sweeps for nearly a million wavelengths and 14 hours of sweeping. Accuracy without any outlier correction is at least 97 percent. (c) The relative power of a spectrometer-on-chip at wavelength fluctuation during uninterrupted sweeps for nearly a million wavelengths and 14 hours of sweeping. Power stability is better than 99 percent.

Additional attributes of our patented technology are its excellent wavelength and power stability across an extended period of uninterrupted operation (see Figure 5). Without the aid of any outlier correcting software, we achieve a relative power stability of over 99 percent at a set wavelength. During an extended period of uninterrupted operation, wavelength stability – that is, the accuracy between set and actual wavelengths – is 97 percent. Again, such a high level of performance is hard-to reach with most table-top lab instruments. But in our case it comes from just a tiny chip. This highlights that we have a great technology with a real potential for advancing spectroscopy, through an expanded product range that will serve a vast number of applications.

Another strength of our technology is its power ratings – primarily the power output and the power consumption. It is important to point out that there is no universal output power level that separates what is and is not acceptable for all applications. Instead, criteria must be established on a case by case basis. However, having said that, some numbers are possible to define. Based on our own internal work we have identified that most *in-vitro* applications need around 0.1-0.2 mW of CW laser power when using our GaSb detector. Note that this is the level for a single-mode laser, and does not correspond to the total power of a broadband emitter, but should rather be compared with a spectral power density, which is usually expressed in power/nm.

Governing the power consumption of our spectrometer-on-chip is its laser. To minimise what it draws, its threshold current should be as low as possible, as this ensures that the operational output power is realised at the lowest possible drive current. As we routinely achieve thresholds between 20 mA and 50 mA, we can operate at currents in the 100 mA to 150 mA range, and use input powers of around 100 mW. Such powers are very promising for a very broad range of applications – from implantable biosensors to wearables, handhelds and remote-operation sensors. By combining a low power consumption with a small form factor and a monolithic design, our spectrometer offers stabilization and simple, reliable operation over an extended period of time.

The road ahead

We are pursuing parallel paths for the development of our products, and the applications that they will serve (see Table 2). Essentially, our products are ‘simple engines’ plus data. For every new application, every new molecule requires a dedicated application development experimental campaign. As this places a cost on resources, we must decide carefully what to pursue, based on considerations such as the demands of resource, the market opportunity and strategic interest.

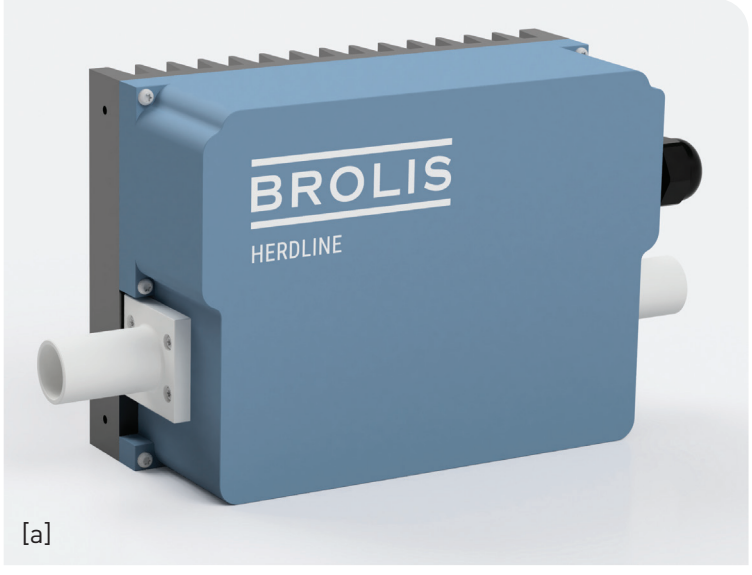
On dairy farms, spectroscopic sensing allows individual cow monitoring for critical molecular data. This can include the monitoring of lactose, fats, and

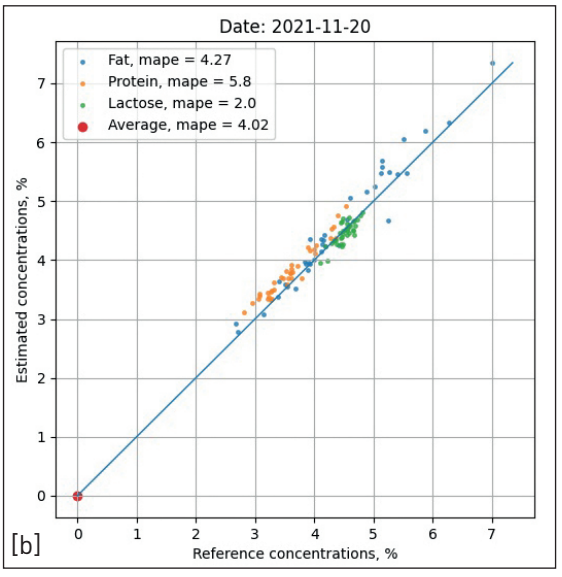
PRODUCT/APPLICATION	TYPE	SENSING OBJECT	MARKET READINESS
OEM spectrometer-on-chip	OEM	–	End of 2022
Dairy farm milk analyzer	Industrial hardware +data	Fat, protein, lactose, blood, milk volume, etc.	First sales 2022
***In-vitro* blood**	OEM biomedical / end-user	Glucose, lactate, urea, cholesterol, ethanol	End of 2023
***In-vivo* blood**	End-user	Ethanol, lactate, glucose, cholesterol	2025
In-line industrial (not disclosed)	Industrial hardware +data	Multiple molecules	2023

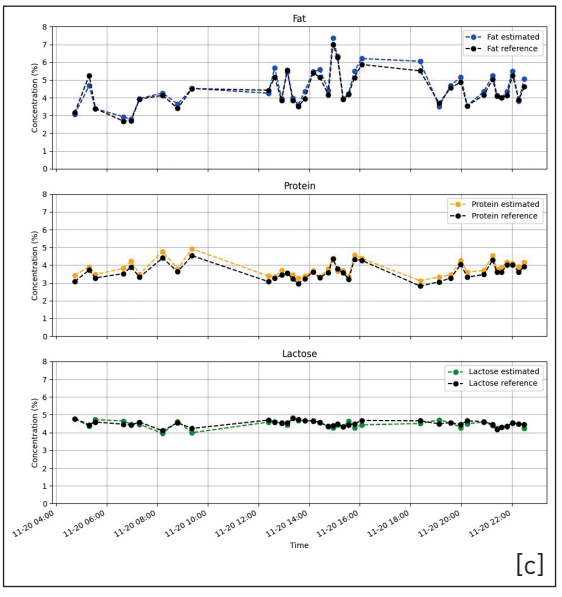
➤ Table 2. Brolis spectroscopic sensor product list and market readiness.

proteins, and provide insight into productivity and herd health status. By drawing on accumulated data models, farmers can foresee the onset of health issues such as ketosis, mastitis and acidosis. This information may lead to antibiotic-free treatment and minimise off-line losses. Additional key metrics for those running dairy farms are the total volume of milk and how rich it is in proteins and fats. Individual animal data monitoring can capture all of this and enable efficient herd selection, and ultimately enhance the profitability of the business (see Figure 6 for performance data provided by our in-line dairy farm sensor).

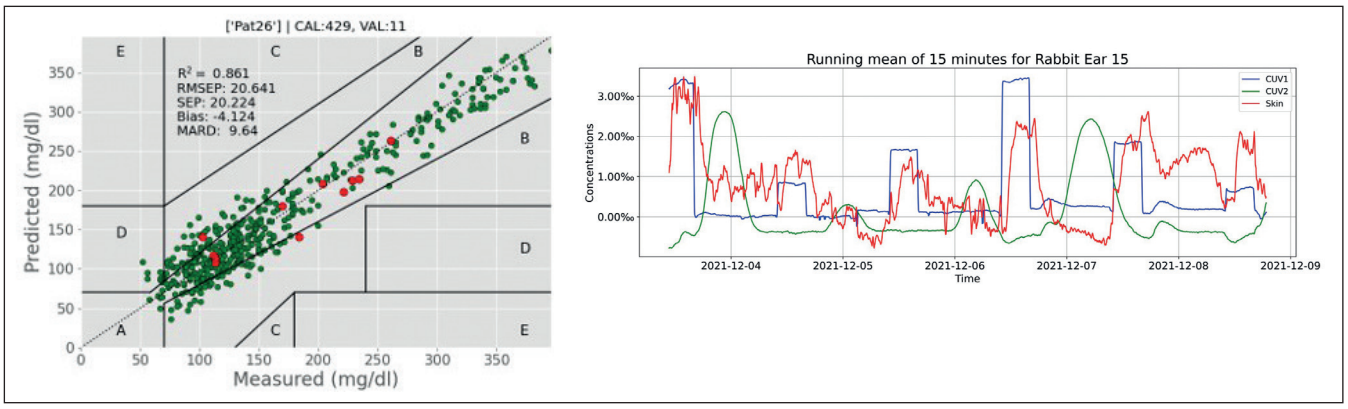
There are also important, challenging, high-potential applications involving blood. We are targeting an *in-vitro* handheld blood spectrometer, by working







➤ Figure 6. (a) A Brolis in-line milk analyser. A spectrometer-on-chip measures the composition of milk during milking in-flow and real-time. (b) Accuracy of the in-line, in-flow, real-time milk analyser for milk fat, lactose and protein. (c) A one-day milk analyser trend data compared with a laboratory reference for milk fat, protein and lactose.



➤ Figure 7. (a) *In-vitro* prediction of blood glucose for a diabetic patient with an accuracy of slightly above 1 mmol/l or 20 mg/dl. (b) *In-vivo* trend for a 5-day transdermal blood ethanol detection in animal study. 1 permil blood ethanol is visible and detected through the skin.

towards a sensor for detecting multiple molecules, such as glucose, lactate, cholesterol and urea. This combination provides valuable insight into diet, kidney function, fatigue and metabolism in general. We are intending to have a pre-market prototype ready by the end of 2023 that will be suitable for at least several molecules. Further ahead, we have plans for *in-vivo* or non-invasive sensing. Our first product will be a non-invasive blood alcohol (ethanol) sensor. We hope to follow this with devices that detect and monitor additional molecules (see Figure 7 for details of our *in-vitro* and *in-vivo* developments.

The spectroscopic sensing of milk and blood provide just a couple of illustrations of the capability of our chip technology. We have no doubt that many more products will follow – and in that light, we believe that over the next few years we will demonstrate some very exciting products, breaking new ground in functionality, form-factor and applicability.

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Artist rendering of a GPS III satellite deployed in a medium-earth orbit (MEO). Credit: The Aerospace Corporation.

Are GaN RF devices reliable enough for space missions?

Can concerns over the likes of intrinsic and extrinsic reliability, mechanical integrity and radiation hardness scupper the chances of GaN HEMTs from being deployed on lengthy satellite missions?

BY JOHN SCARPULLA FROM THE AEROSPACE CORPORATION

IT IS NOW BEYOND QUESTION that GaN-based microwave devices, that is transistors and MMICs, offer a high enough level of maturity to be deployed in many terrestrial and airborne applications. However, they are have yet to be incorporated in space satellite missions lasting up to 15 years, where ultra-reliability is paramount.

A lack of deployment in these space missions is certainly not due to any issue associated with performance. When GaN HEMT-based devices are used to construct power amplifiers, they outpace the GaAs HEMTs of the previous era by a substantial margin, delivering far higher power densities while operating at higher temperatures and voltages. Hunt for the details and you'll find that when judged by those crucial metrics, GaN HEMTs offer about a ten-fold hike in the current-per-unit-gate-width when compared with their GaAs equivalents, while running at a channel temperature of 200°C or more

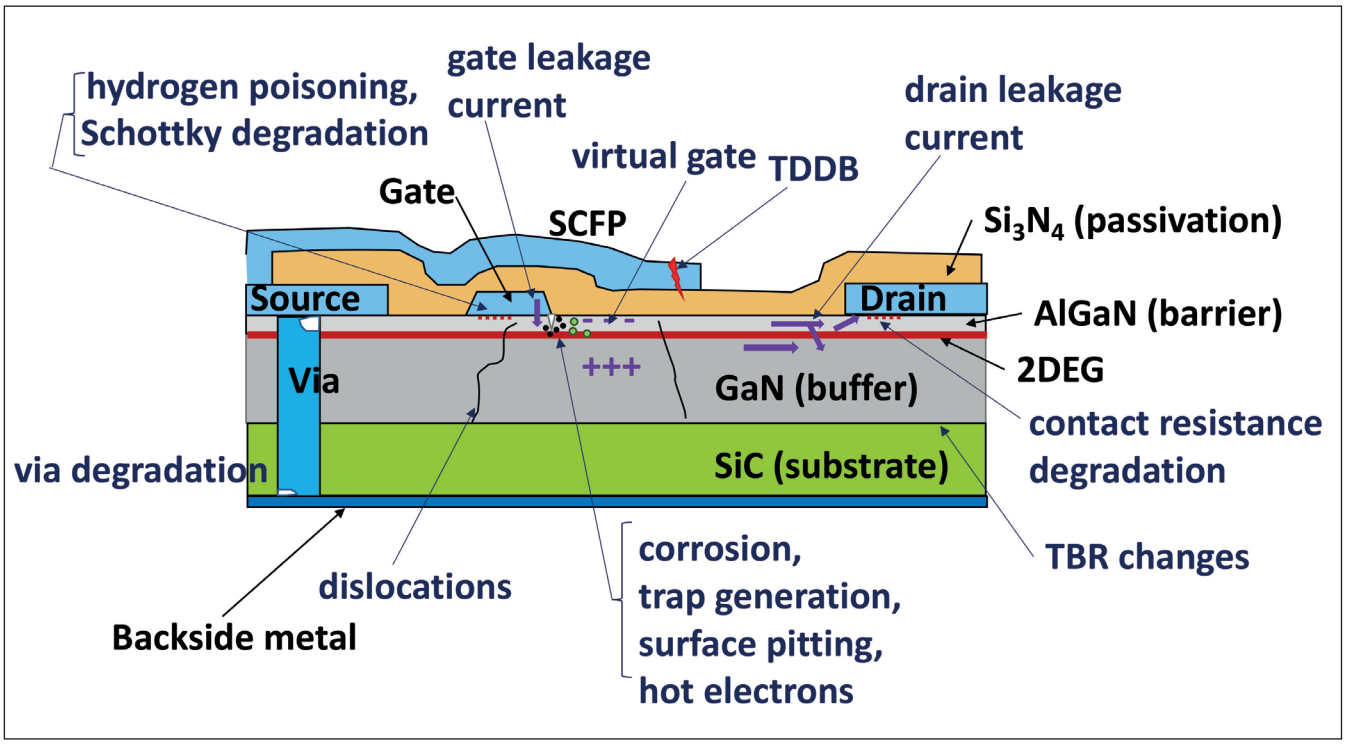
and handling higher RF peak voltages – currently ranging from 50-100 V, and rising. And given that the overriding goal for satellite designers is to minimise size, weight and power, it would appear that GaN-based HEMT devices would be a shoe-in. But it is still a struggle to infuse high-reliability satellites with this technology. Why?

Based on my experience in working in the aerospace industry – my current role is Technical Fellow of The Aerospace Corporation – I have concluded that part of the reason why GaN is not as successful as it should be is that the existing crop of military and industry standards are not up to snuff. When specifying and acquiring high reliability semiconductor devices, the entire set of standards that's employed are inappropriate, having been developed over the last 50 years.

Back in the 1960s and 1970s, when these standards were conceived, silicon bipolar transistors were the RF power device of choice. Since then several alternatives have emerged, including LDMOS, Si-Ge CMOS, GaAs HBTs, GaAs MESFETs, GaAs pHEMTs and now GaN-based HEMTs. Over that timeframe GaAs and InP HEMTs have rose to prominence in low-noise amplifiers, and for a GaN HEMT and MMIC, the power amplifier is now seen by many as the 'killer app'. Failing to keep pace are the semiconductor device testing and quality standards – and compounding the issue are the additional stringent requirements for high-reliability space missions, such as radiation exposure, temperature cycling, RF multipaction, hermeticity and long mission durations. The upshot is that the problem has become even more intractable.

To try to bridge this gap I have worked with colleagues at The Aerospace Corporation – plus a working group consisting of industry, government, space contractors, GaN fab houses and academia – to develop a guideline to aid in the specification, testing and qualification of GaN HEMT-based devices for high reliability space applications. This effort has culminated in the publishing of a 205-page document, available to the general public upon request, that covers six main areas: intrinsic reliability, focusing on the identification of wearout failure modes intrinsic to all devices; extrinsic reliability, involving the characterization of defect densities affecting reliability; electrical robustness, considering the safe operating area for the gate and drain; environmental factors unique to space, such as multipaction and hydrogen poisoning; mechanical integrity issues, such as bondwires operating at higher than traditional temperatures; and radiation effects, involving considerations of radiation test plans for various environments.

In the remainder of this feature I present some highlights and key topics from this guideline. But just before we get there, I wish to emphasize that in general, to assess the reliability of an electron device one has to generate failures in a controlled and accelerated stress environment, because this allows a distribution of failure times to be extrapolated to more benign usage conditions. While tests that



➤ Figure 1. GaN HEMTs suffer from many different failure mechanisms. The more common ones are depicted here, with current arrows showing electron currents. Positive and negative charges may accumulate as well as surface traps. Abbreviations used are: SCFP for source-connected field plate, TDDB for time dependent dielectric breakdown, 2DEG for two-dimensional electron gas, and TBR for thermal barrier resistance.

produce no failures may at first glance appear to be a positive result, they are not especially useful in determining the physics of failure. It is this philosophy that has been adopted for considering the qualification of GaN HEMTs.

Intrinsic and extrinsic reliabilities

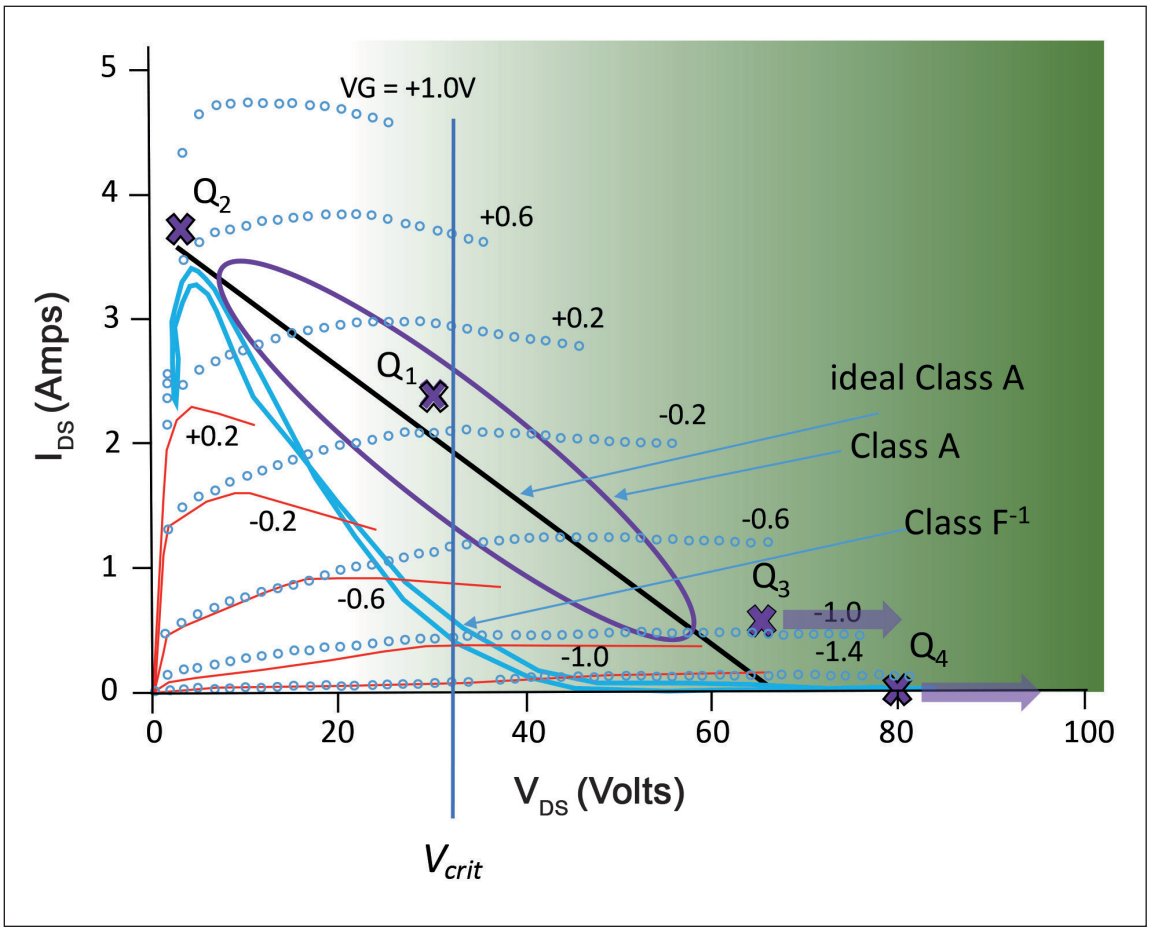
To improve the reliability of the GaN HEMT, many designers add a field plate to reduce the peak electric field on the device's drain side (see Figure 1 for such a design, plus a list of many failure mechanisms). While this type of device could fail for many different reasons, it will not exhibit all of these traits, because they are activated under different usage or stressing conditions. The trick is to identify the mechanism, or mechanisms, that will govern wearout reliability in any given space mission scenario.

Engineers tend to operate RF power amplifiers into compression, as this increases the power-added efficiency. Depending on whether the amplifier operates in Class A, AB, F^{-1} or another mode, there can be a dramatic variation in the 'load figure' (a generalization of the load line) on the IV-plane (see Figure 2, which depicts typical load figures and illustrates how the IV plane is traversed differently depending upon the amplifier design).

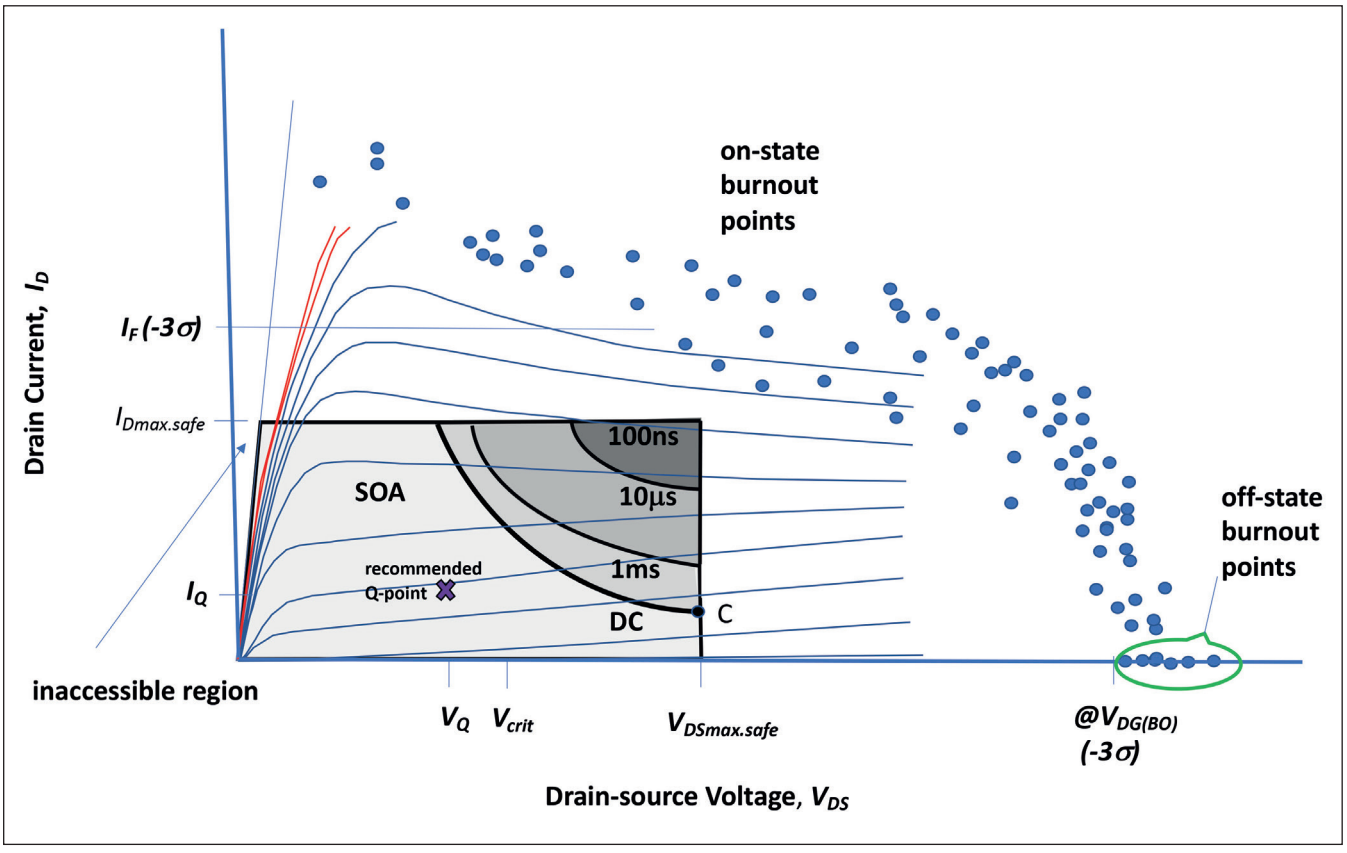
It is now understood that failure modes are different at different locations on the IV plane. Our working tenet is that DC stressing at the different quiescent points (or 'Q-points') shown in Figure 2 uncovers different failure modes. One example of this is the off-state, zero current, high-voltage condition (Q-point #4 in the figure) – this leads to voltage or piezoelectric strain-driven failure modes that cause surface pitting and trap generation.

In comparison, an on-state, low-voltage, high-current condition (Q-point #2) engenders current-driven failure modes, such as contact voiding or electromigration. The other two Q-points are 'semi-on' (Q-point #3), and the traditional central point in the IV-plane (Q-point #1). That's traditional in the sense that 20 years' worth of reliability testing of GaAs low-noise amplifiers has been performed there – an effective strategy for small-signal GaAs low-noise amplifiers, where gate sinking has been the dominant failure mode.

With GaN, there's a need to broaden thinking to include many more failure modes. My view, and that of my collaborators, is that it is best to use DC testing: we advocate beginning with step-stress testing, before turning to constant-stress testing, to uncover multiple GaN failure modes. We also recommend 'test-like-you-fly' RF-driven life-testing, as this helps to



➤ Figure 2. DC (lines) and pulsed IV (points) characteristics of an RF power GaN HEMT, and representative loadlines, with four proposed operating Q-points for DC reliability testing. The shaded region above critical voltage V_{crit} may exhibit quite different electric field-driven failure modes than the region below it, where thermally driven mechanisms may prevail.



➤ Figure 3. An example of drain IV plane and common-source characteristics of a GaN HEMT showing the safe operating area (SOA), which must be extremely conservatively defined for high-reliability space missions. The dots show the burnout points that must lie well outside the drain SOA. The critical voltage V_{crit} defines the onset of time-dependent degradation. A possible amplifier Q-point is shown, and Point C shows a recommended stressing condition in the guideline for power cycling tests.

correlate DC results with actual RF usage conditions. Note that more details on qualification test plan recommendations are provided in our guidelines. Extrinsic failure modes represent the other side of the coin, producing early failures in a subset of the device population. According to JEDEC standard JESD65B, an extrinsic mode is 'a failure mechanism that is directly attributable to a defect created during manufacturing'. Examples of such defects include particles, voids, and lithography errors.

The good news is that many of these failure modes may be screened out with appropriate tests, such as those recommended in our guideline. For example, if a particle or an irregularity is in the gate-drain recess region, this can lead to a premature breakdown of the device at the peak RF voltage – and screening HEMTs with a combination of an elevated drain voltage and temperature offers an effective solution.

It is also possible to screen the metal-insulator-metal capacitors (MIMCAPs) that are present in MMICs. Some have argued that the reliability of a large GaN MMIC could be dominated by MIMCAP extrinsic failures rather than the HEMTs themselves. Detailed in our guideline are methods involving the use of test structures, such as large-area MIMCAPs and wide HEMTs, to estimate defect densities and their associated reliability.

Safe operating areas

When deployed on space missions that demand that all devices have a high level of reliability, it is crucial to conservatively define the safe operating area of a power GaN HEMT. In Figure 3, which shows the typical drain safe-operating-area for a GaN HEMT, plotted points depict where the device burns out abruptly as the voltage or current is raised.

One of the common characteristics of the RF GaN HEMT is that it lacks a well-defined sustaining avalanche breakdown voltage. Instead, the voltage breakdown tends to be abrupt and catastrophic. Due to this, our guidelines recommend selecting a value for the maximum safe peak drain voltage of no more than one-half to one-third of the burn-out voltage. Similarly, for conservatism, we advise adopting a similar constraint for the maximum drain current.

Those that employ GaN HEMTs should be aware that a critical voltage may exist for this class of transistor, where time-to-failure begins to be controlled by a voltage or an electric field rather than by the temperature alone. If this is the case, as well as elevated temperatures providing an accelerator for

failure times, drain voltages have this effect. In our guideline we propose various models for estimating reliability, based on both temperature and voltage.

Hermetic or not?

Traditionally, it has been the case that electronic modules, and certainly RF amplifiers, are packaged hermetically for space. There are many reasons for this, including avoiding moisture effects, preventing possible solvent incursions during payload integration, and ruling out contamination from the dirty launch environment.

For GaN HEMT based RF amplifiers, the benefits of hermeticity may be dwindling. Take the maximum permissible water vapour content within a hermetic module, a figure of 5,000 parts-per-million-volume (ppmV). This requirement is designed to prevent condensation of liquid water on die surfaces. The dewpoint of internal gas that contains 5000 ppmV of moisture at 1 atmosphere lies below the freezing temperature of water, reducing the possibility that a film of liquid water might form on a die surface.

It was hoped that would prevent corrosion mechanisms in the poorly passivated silicon die of yesteryear. Now, in the era of GaN RF amplifiers, that level of moisture may not be acceptable. The issue is that GaN, as well as its family of related alloys, can react with water vapour to produce ammonia. If this reaction proceeds to produce gallium oxide and ammonia, 5,000 ppmV of water can be converted into as much as 3,333 ppmV of ammonia gas.

Note that this is not just a theoretical concern. In sealed microwave modules containing GaN devices high levels of ammonia have been found. This gives rise to two open questions: Is it acceptable to trap moisture that converts to ammonia inside a hermetic microwave module? And are the present requirements unsuitable for GaN HEMTs?

There is the possibility that vented modules containing GaN die are more reliable for space missions. One argument in favour of this relates to multipaction and ionization breakdown. All hermetic modules leak to some extent, and when launched into space, internal gas will slowly leak away. This will produce a drop in internal gas pressure and an alarming reduction in the Paschen gap – this is the distance between two electrodes needed to induce electrical breakdown by gas ionization at a particular voltage. When this gap gets too low, breakdown may take place, either between two adjacent bondpads or two adjacent bondwires acting as electrodes. This catastrophic ionization breakdown tends to occur late in a mission when the gas is leaked away.

To avoid this difficulty, the gas can be removed altogether, leading to the flying of a fully vented module resulting in vacuum after launch. But care is needed, as there is the threat of the multipactor effect: it occurs in vacuum when electrons emitted from metal surfaces, either thermionically or via field emission, resonate with an RF field, leading to electron avalanche and catastrophic damage. The cure is the combination of a well-chosen geometry and the suppression of surface electron emission by coatings or foams. In our view, a reasonable approach for space missions might be to use a high-reliability vented microwave module that is free of ionization breakdown and ammonia build-up, and features multipaction mitigation.

Radiation effects

One commonly held view is that GaN HEMTs and MMICs are 'intrinsically' rad-hard. This position stems from the fact that current conduction is via minority-carrier only in the two-dimensional electron gas (2DEG). Minority carrier (hole) lifetime that may be degraded by radiation is of little consequence in a GaN HEMT.What's more, there are no gate oxides or field oxides to trap charges, like there are in silicon devices. GaN or AlGaN surfaces are Fermi-level pinned by large surface trap densities, so the radiation-induced charges in adjacent passivation layers have little effect. The upshot is that in GaN, the usual total ionizing dose of radiation and displacement damage effects are usually fairly inconsequential.

However, for those that are considering using GaN HEMTs in space, concerns should be directed at single-event effects caused by trapped electrons and protons in the Van Allen belts, and cosmic rays emanating from deep space, which are nuclei stripped of all electrons. There is plenty to consider, now that that GaN RF power devices are being propelled to higher and higher peak RF voltages.

When an ion strike occurs, it leaves behind an ionized track of semiconductor atoms. The electrons thus freed by this are capable of causing burnout, coming from the generation of current under a sufficient electric field. This 'single-event burnout' is now a significant concern in GaN RF power devices.

To determine how susceptible these devices may be to this form of burnout, they can be assessed using cyclotron particle accelerators. Qualification testing in this manner has shown that for a GaN device to be usable in some space radiation environments, it

GUIDELINES FOR SPACE QUALIFICATION OF GAN HEMT TECHNOLOGIES

- *Guidelines for Space Qualification of GaN HEMT Technologies* by J. Scarpulla and C. Gee, The Aerospace Corporation, TOR-2018-00691-A, was published on March 5, 2020. This publicly available document, with 205 pages, 200 references and 8 appendices, covers many aspects regarding space qualification of GaN RF HEMTs and MMICs. An ongoing working group continues to improve this document.
- **Contact: J. Scarpulla (john.scarpulla@aero.org) to request the document and/or to participate in the working group.**

must be severely derated. The burnout-free operating voltage must fall to 30 percent or less of the rated voltage in some cases. To help shine more light on this major source of concern at the system level, in our guidelines we have detailed prototype radiation test plans that are suitable for space-qualifying GaN HEMTs and MMICs.

While there are concerns related to intrinsic and extrinsic reliability, electrical robustness, environmental factors, mechanical integrity and radiation, we believe that RF GaN HEMT-based devices can be qualified for high reliability in space. Addressing a combination of absence and inappropriateness surrounding space qualification tests and methodologies for GaN RF HEMTs and MMICs in existing electronic device specifications is our published guideline.

We believe that this document will help to speed the adoption of RF GaN HEMTs and MMICs for space. While new GaN standards and requirements are now being discussed by standards agencies, such as JEDEC, IEEE, ASTM, AEC and NASA, their focus is not necessarily on ensuring high-reliability in space.

Trying to fill this void, manufacturers have stepped in, developing their own test methods and qualification. But this leads to a lack of standardization, slowing the adoption of RF GaN for high-reliability space systems. It is our hope that our guidelines will help to alleviate this situation and spark the development of an industry standard for qualification of GaN RF HEMTs and MMICs for high-reliability space missions.

ADDITIONAL QUALIFICATION TOPICS

There are so many qualification topics that it's not possible to mention them all in this article. Many more are covered in *Guidelines for Space Qualification of GaN HEMT Technologies*.

Detailed within the pages of that document are:

- The reasons behind the need for a complete re-think regarding electromigration occurring in the metallization lines in GaN. This is needed because the traditional current density safe limits found in existing silicon-based standards have been grounded in operation at 125°C, while for GaN HEMTs, especially at gate feeds where the current density is high, temperatures can far exceed this.
- An explanation of why microscopic visual inspection of GaN die cannot always be performed according to existing criteria. As GaN (and the typical SiC substrate) are optically transparent, the microscope 'sees' only the back surface of any non-metallized die regions.
- An entire section devoted to a ratings and de-rating philosophy consistent with high-reliability operation, and a standardized ratings data sheet.
- Many measurement techniques for estimating HEMT channel temperature.
- Recommendations for qualification methods to determine the reliability of passive devices, such as thin-film resistors, MIMCAPs and backside vias.
- A checklist for qualification testing, as well as '50 questions' to consider when choosing a GaN HEMT vendor or process, as a guide to the space community.

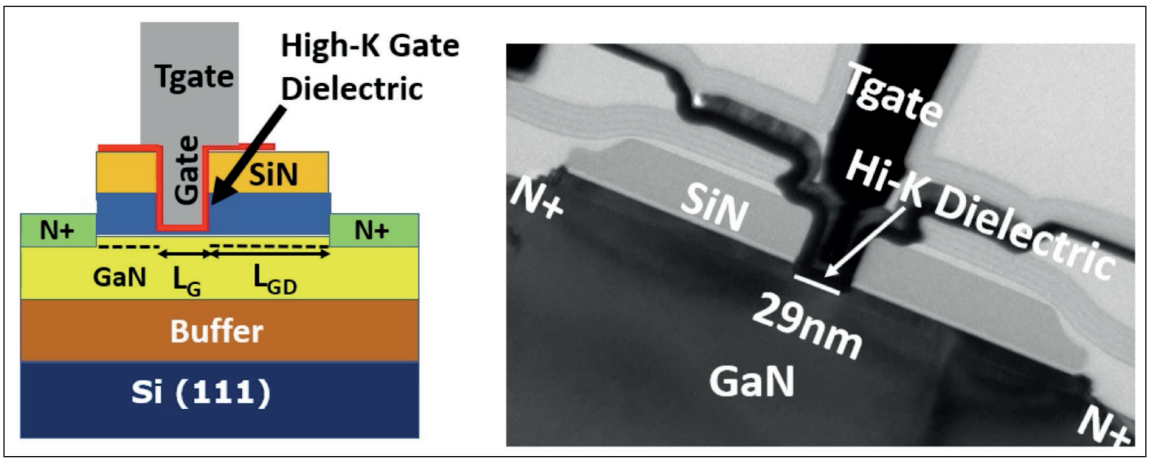
Turbo-charging the transistor

At a session at the International Electron Devices Meeting devoted to 6G and terahertz applications, engineers unveiled new strategies for increasing the operating frequency of the transistor

BY RICHARD STEVENSON, EDITOR, COMPOUND SEMICONDUCTOR

As the roll-out of 5G gathers pace, engineers in academia and industry are considering what might follow. Towards the end of this decade and beyond, wireless communications is tipped to move to higher frequencies – almost certainly beyond 100 GHz, and possibly encroaching the terahertz domain.

While the next step on the wireless roadmap, 6G, is yet to be defined, it is expected that initial research into this communication standard will focus on the D-band, which spans 110 GHz to 175 GHz. However, when 6G is actually deployed, it is likely to operate within the 300 GHz to 450 GHz frequency range.



➤ Figure 1. (a) Intel's E-mode GaN transistor has an f_T of 300 GHz and an f_{MAX} of 400 GHz. (b) A transmission electron microscopy image shows the gate length is just 29 nm.

Circuits operating at such high speeds will need to combine high frequencies with a high power efficiency and multi-functionality, a set of conditions that is hard to satisfy with silicon CMOS. Offering more promise are heterogeneous technologies that marry the merits of silicon, such as maturity and high-volume manufacture, with the superior speeds of the III-Vs.

Efforts in this direction were discussed in session at the 2021 International Electron Devices Meeting (IEDM) entitled *Microwave, Millimetre Wave and Analog – III-V technologies and their application to terahertz/6G*. In that session, taking place in San Francisco in early December, Intel championed its record-breaking enhancement-mode GaN transistors produced on 300 mm silicon, and a team led by KAIST claimed to break new ground with InGaAs HEMTs on silicon. Other teams reported their successes with III-V transistors on native substrates, potentially providing a stepping-stone to triumphs on a silicon foundation. A partnership between engineers in South Korea and NTT detailed InGaAs-on-InP HEMTs with record-breaking frequencies, while researchers at ETH Zurich unveiled terahertz transistors based on GaAsSb and InP that are fabricated with a new process that provides optimisation of the base-emitter access distance.

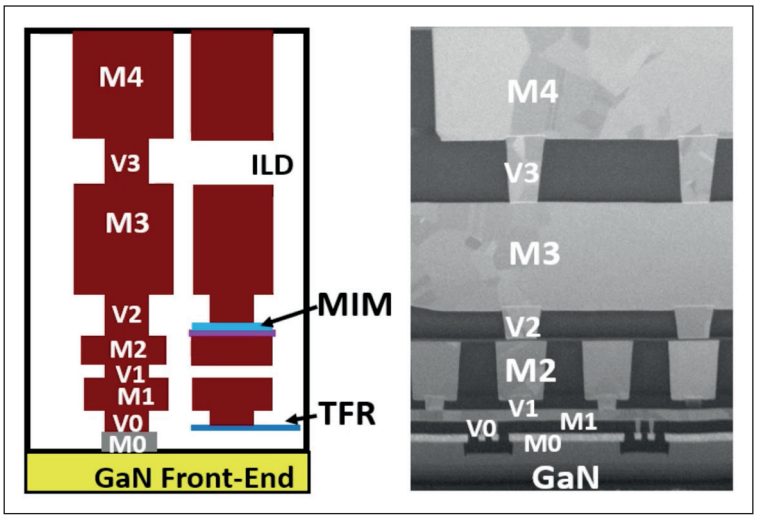
Intel integration

At IEDM Intel made many record-breaking claims for its GaN-on-silicon transistors, including new benchmarks for the cut-frequency (f_T) and maximum oscillation frequency (f_{MAX}), two key figures-of-merits. Further firsts included: the highest transconductance, attributed to device scaling and the incorporation of a material with a high dielectric constant; a record-breaking drain-source voltage for this class of transistor; and the fabrication of the first truly E-mode GaN transistor that delivers a full on-current, realised with a record low-gate drive of just 1.8 V (typically, E-mode GaN HEMTs need a gate drive of at least 6 V). In addition, Intel's GaN-on-silicon transistors were said to provide an outstanding RF performance.

According to Han Wui Then, spokesman for the Intel team from Hillsboro, Oregon, their successes have come from insights provided by Moore's law and Dennard MOSFET scaling. To draw on this, they developed a process for producing E-mode transistors with gate lengths down to 30 nm. Their fabrication involves the use of a high-κ dielectric technology, an atomic layer etch, and GaN buffer technology.

Intel's spokesman is in no doubt that the best material system for such efforts is GaN, describing this as "the technology of choice for ultra-fast switching and for producing compact integrated power electronics and RF millimetre-wave".

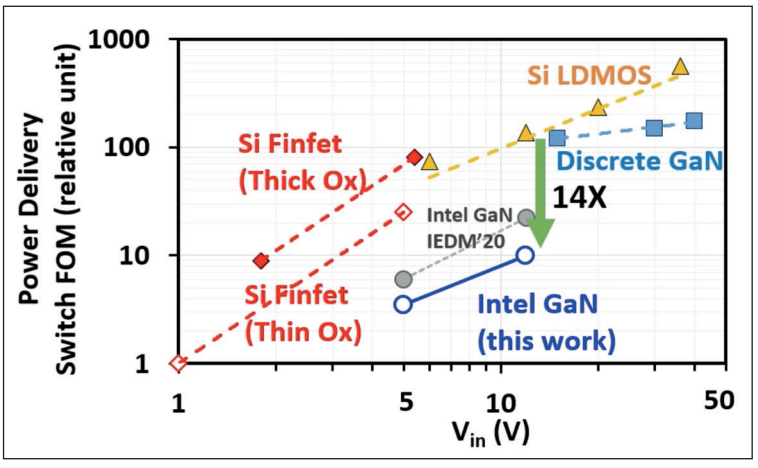
The team's GaN transistors, formed on silicon (111) substrates, feature a recessed gate and low-resistance re-grown source and drain contacts (see Figure 1 for a device diagram). Circuits that incorporate these devices are formed with a four-level copper backend interconnect process that can produce thin-film resistors and metal-insulator-metal capacitors (see Figure 2).



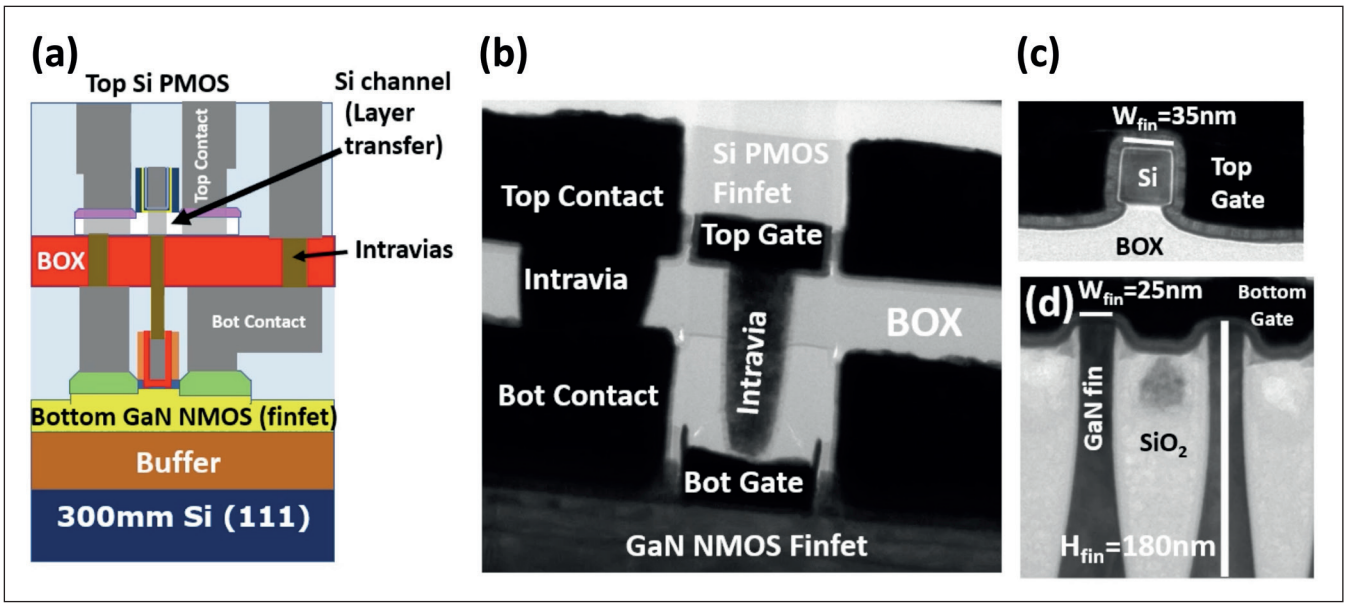
➤ Figure 2. (a) Intel's high-speed ICs are formed using a four-layer copper back-end stack that includes metal-insulator-metal capacitors and thin-film resistors. (b) A scanning electron microscopy image, showing the fabricated copper backend interconnect over E-mode high-κ dielectric GaN transistors fabricated on 300 mm silicon.

"Our 300 millimetre process is highly uniform," argued Then, who pointed out that the one-sigma variation in threshold voltage is just 38 mV. He added: "This enabled us to fabricate and integrate a large number of gates". He gave an example of a power GaN die with a total width of 880 mm and an area of just 4 mm^2. This chip is capable of a power density of 9 A mm^{-2}.

Attributes of Intel's GaN transistors include a very low leakage current, a high drive current, a low on-resistance, and a capability to withstand a drain-source voltage up to 65 V. A common figure-of-merit for power



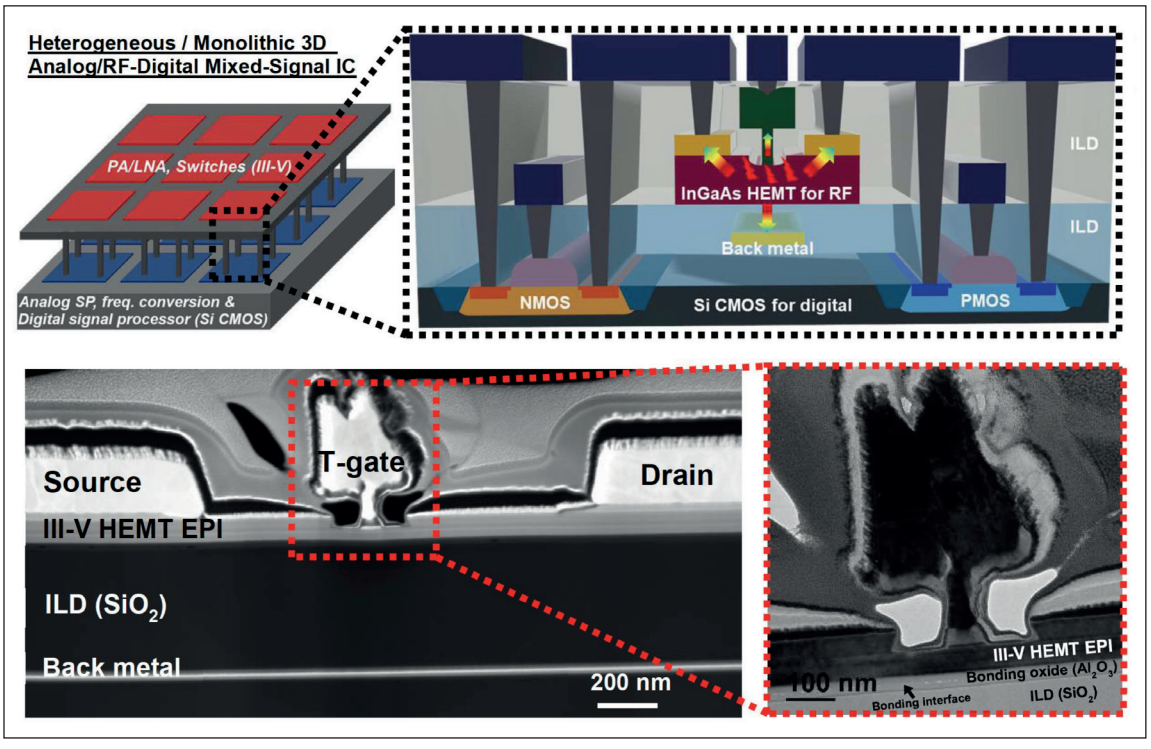
➤ Figure 3. Channel length scaling improves the power delivery switch, according to a figure-of-merit that is defined as the product of on-resistance and the gate charge. One of the benefits of scaling is that it allows the construction of faster, more compact power electronics.



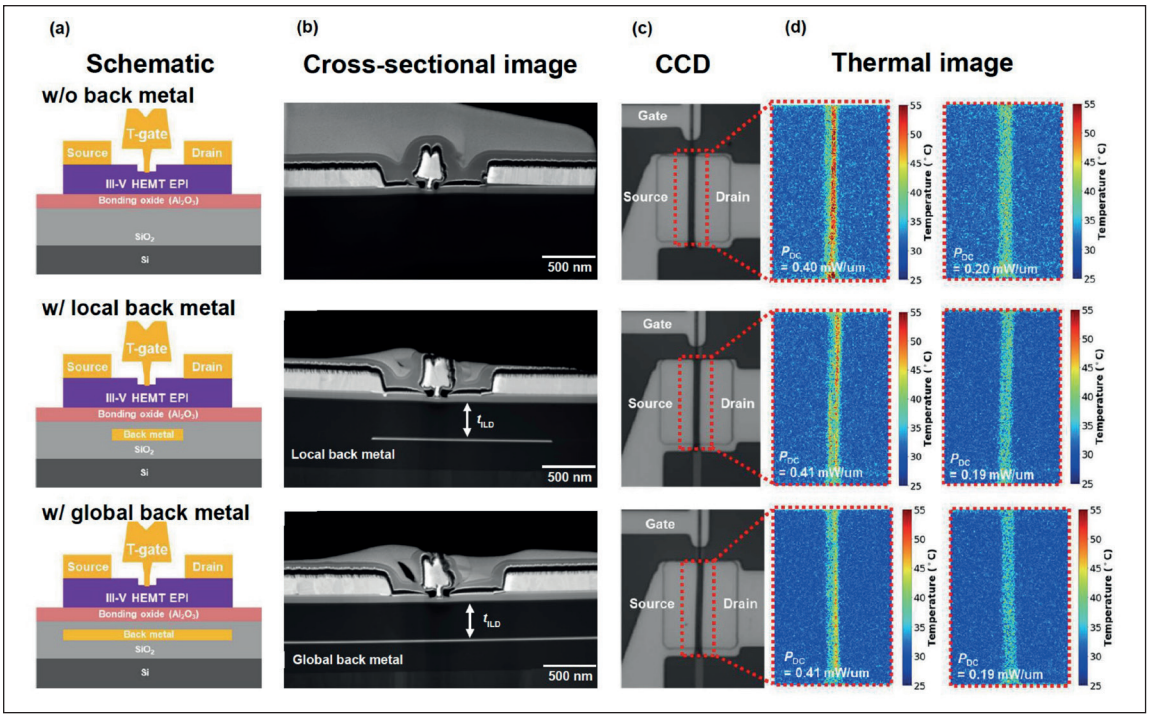
➤ Figure 4. (a) Using wafer bonding, a team from Intel produced a 3D-stacked GaN-silicon CMOS inverter. Transmission electron microscopy images show: (b) the stacked inverter, comprising a bottom GaN E-mode high-κ NMOS finFET and a top silicon PMOS finFET; (c) a 35 nm-wide silicon fin, which forms the top PMOS channel; and (d), a 25 nm-wide GaN fin for the bottom NMOS channel.

electronics – the product of on-resistance and the gate charge – suggests that Intel's GaN transistors are 14 times better than discrete GaN and silicon LDMOS devices (see Figure 3). "This gain truly shows the power of scaling when applied to high-κ gate dielectric gallium nitride transistors," claimed Then.
Intel's GaN transistors combine an impressive performance with a high level of reliability. Operating at 90 °C with a drain-to-source voltage of 10.5 V, time to failure – defined as a degradation in the drain current by 10 percent – is 10 years.

Studies by Then and colleagues have shown that shrinking device dimensions leads to a hike in



➤ Figure 5. Engineers at KAIST are pioneering a heterogeneous, monolithic 3D analogue/RF-digital mixed-signal platform. (top) A back metal is included to reduce self-heating. (bottom) Cross-sectional transmission electron microscopy images show the global back metal, the III-V HEMT, and the SiO_2 interlayer dielectric.

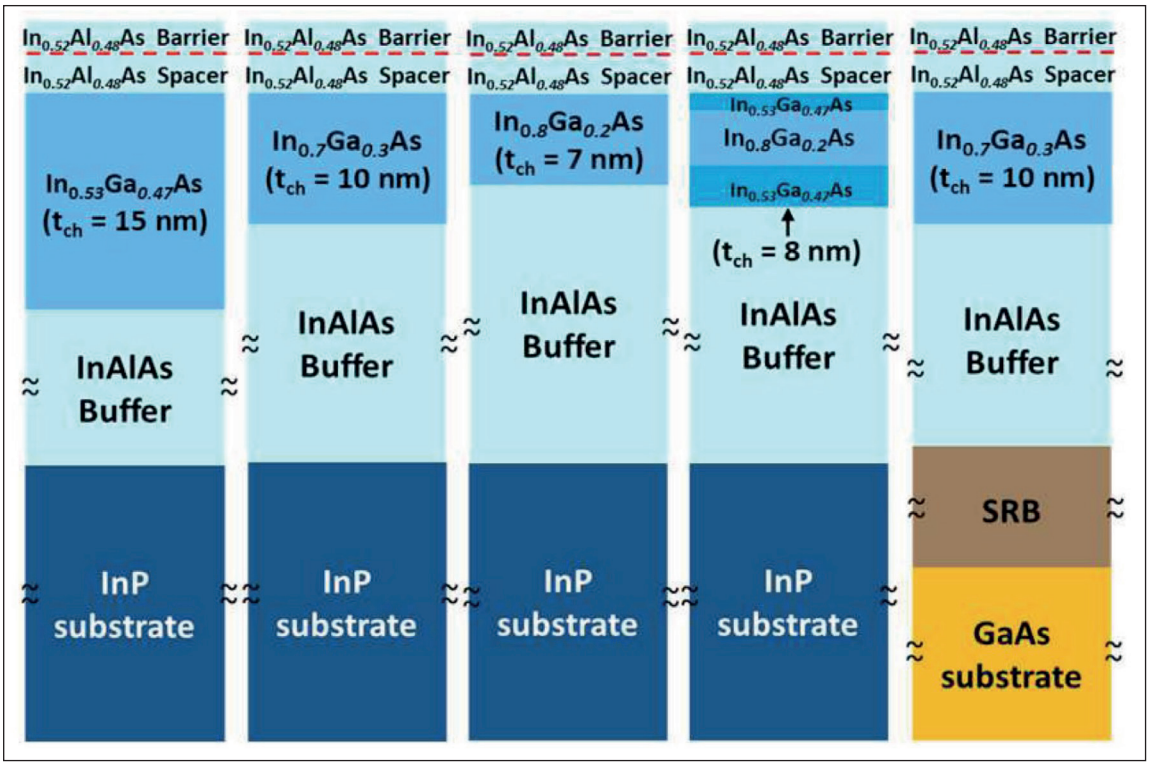


➤ Figure 6. (a) Engineers at KAIST produced a variety of monolithic 3D RF transistors with different back metal structures. (b) Cross-sectional scanning transmission electron microscopy images and (c) CCD images of these back metal structures. (d) Thermal images of these different structures reveal that the architecture has an significant impact on self-heating.

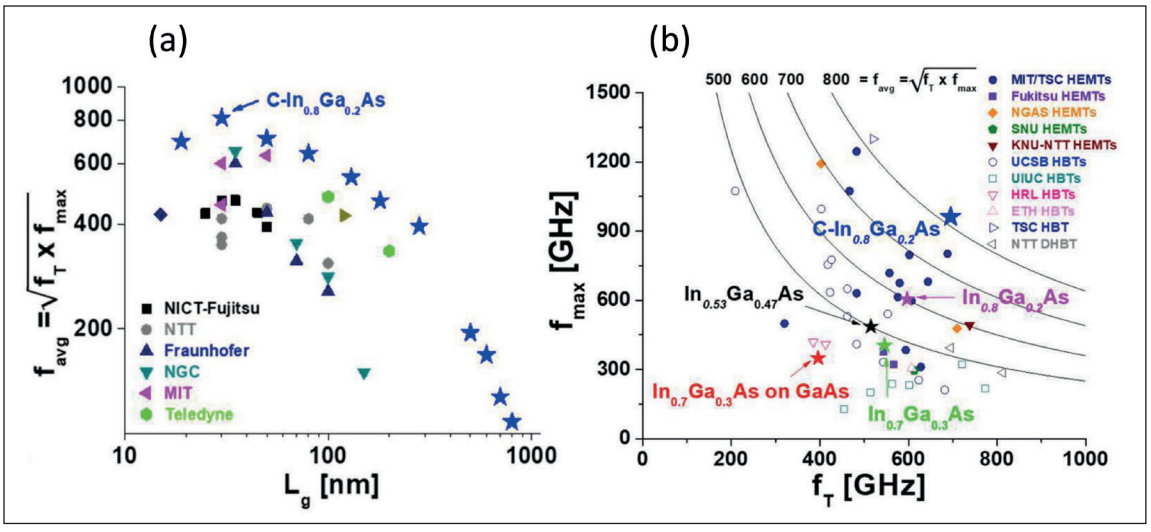
transconductance. Decreasing the gate length from just over 2 μm to 30 nm led to a rise in transconductance from just over 1200 μS/μm to 2100 μS/μm.

Transistors with a 30 nm gate length and a gate-to-drain distance of 160 nm have an f_T of 300 GHz and an f_{MAX} of 400 GHz. For this device, the RF switch figure of merit – the product of the on-resistance and off-capacitance – is 70 fs. This as an "excellent number," said Then.

He and his co-workers have also carried out load-pull measurements, considering a range of frequencies



➤ Figure 7. A collaboration between researchers in Korea and Japan has produced a portfolio of devices with different hetero-structures and gate lengths.

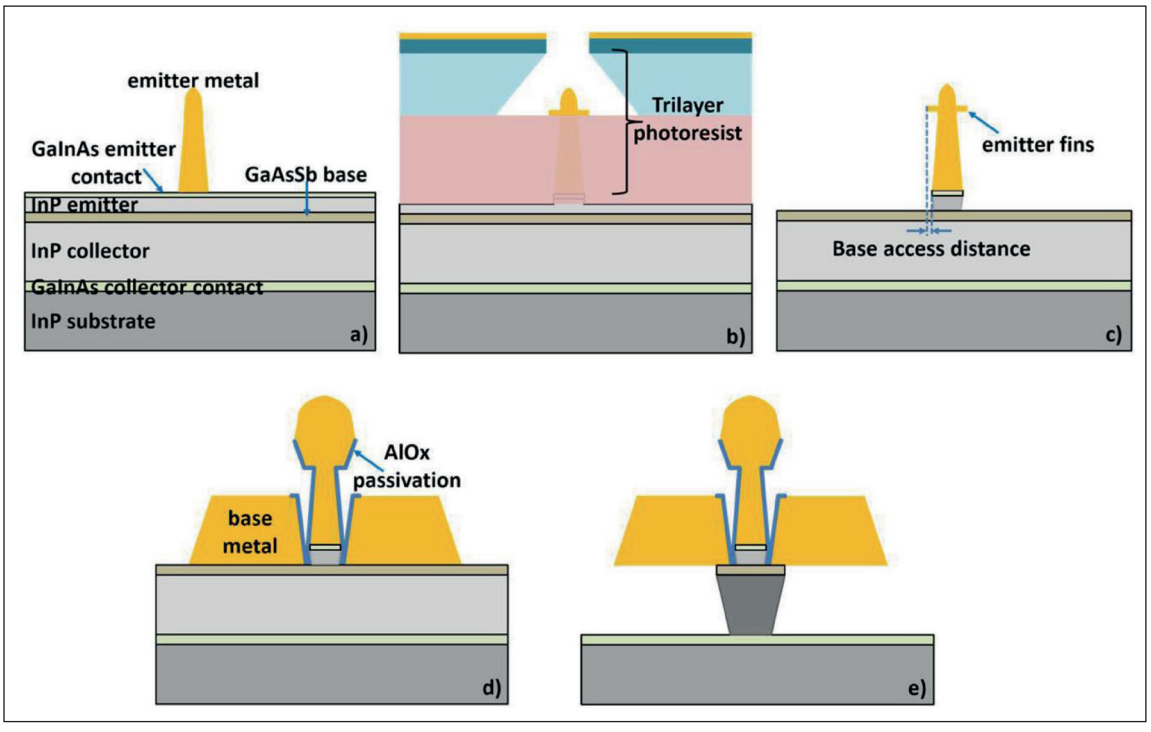


➤ Figure 8. The collaboration between researchers in Korea and Japan has produced InGaAs quantum-well HEMTs with impressive values for the average of f_T and f_{MAX} (a) and for f_{MAX} (b).

and various gate lengths. Results included a device with a 90 nm gate length producing an output power of 23.4 dB at 28 GHz, alongside a power density of 2.7 W/mm and a power-added efficiency of 50 percent. Increasing the frequency led to a reduction in output power and efficiency, with a saturated output power falling to 0.4 W/mm at 90 GHz, and power-added efficiency down to 10.5 percent.

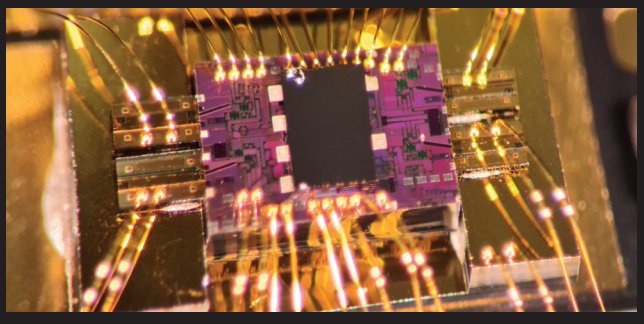
The team from Intel are expecting GaN finFET architectures and 3D layer transfer technologies to play a significant role in the scaling of GaN transistors and the integration of more functionalities. According to Then, this could include a marriage of GaN and CMOS, to enhance the capabilities and reach of GaN technology.

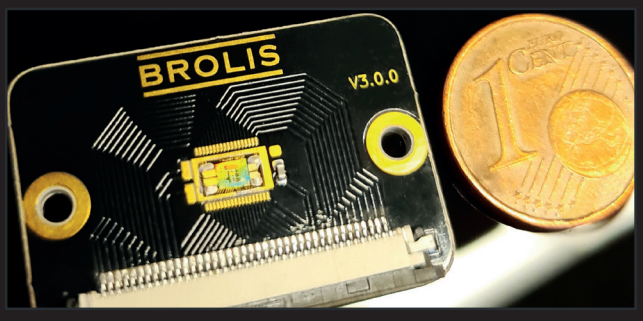
He and his co-workers have already started to explore this possibility, using 3D layer transfer technology to unite silicon PMOS and GaN NMOS devices (see Figure 4). The latter, having finFET widths of just 35 nm, are claimed to feature the narrowest GaN fins ever produced. Device fabrication involved the bonding, cleaving and transfer of a thin layer of single-crystalline silicon onto a GaN transistor wafer, prior to completing the fabrication steps required to



➤ Figure 9. The team at EPFL forms it record-breaking double HBTs with a process that allows an optimal choice of base-emitter access distance down to 10 nm, the use of thick base contact metals, and minimization of parasitic capacitances and resistances via precise lateral wet etching of the base-collector mesa. The steps used are the formation of: (a) the emitter metal; (b) the emitter fins, using a trilayer photoresist; (c) the emitter mesa; (d) the self-aligned base contacts, and AlO_x passivation; and (e), the narrow base-collector mesa.

BROLIS LASER SPECTROMETER-ON-CHIP





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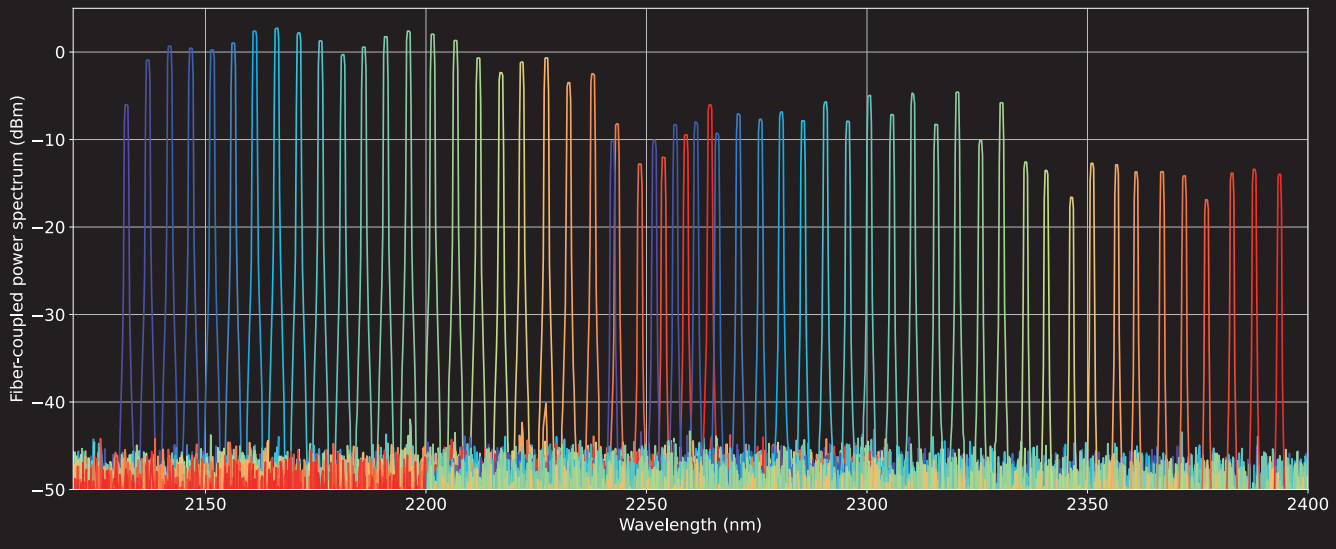
- Lactate
- Cholesterol
- Urea
- Ethanol



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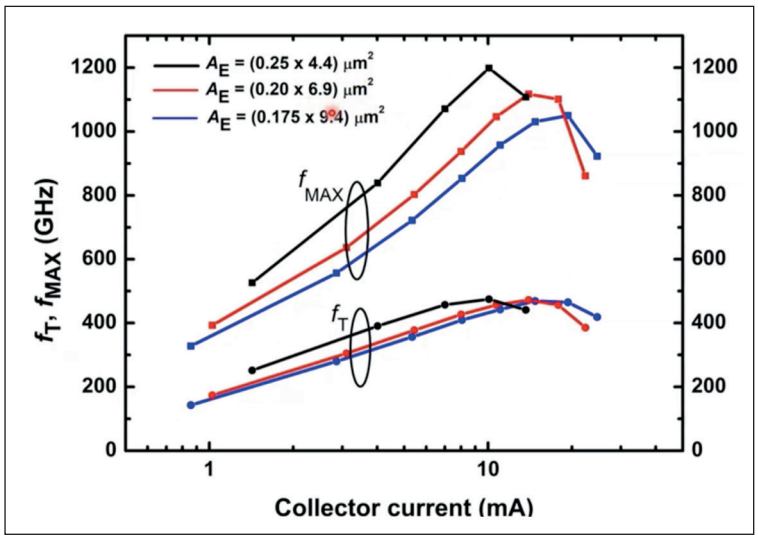


➤ Figure 10. Engineers at EPFL have shown that even for an emitter mesa length as long as 9.4 μm, f_{MAX} can exceed 1 THz. This result is claimed to emphasize a breakthrough in scalability.

form the top silicon devices over the bottom GaN transistors.

According to Then, initial results are promising, with the hybrid structure producing low leakage currents, a pre-requisite for logic applications. Another attribute is a well-matched threshold voltage between the finFETs of silicon PMOS and GaN NMOS.

InGaAs attributes

Heterogenous 3D integration also featured in a presentation from Jaeyong Jeong from KAIST, who argued that there is still work to do before this technology can target 6G applications. When discussing the improvements that are needed, he honed in on the need to increase f_T and f_{MAX} and to minimise self-heating. "We need new monolithic 3D structures for relaxing self-heating of top devices."

To address these issues, the team from KAIST improved the f_{MAX} of their transistor by gate scaling and process optimisation, and introduced a novel monolithic 3D structure with a back metal that quashes self-heating. Success came from using indium-rich InGaAs HEMTs – they offered the best balance of f_T and f_{MAX} to date, as well as the lowest noise figures.

The team's latest triumphs have built on previous work, reported in 2021, that resulted in an f_T of around 450 GHz. However, the accompanying f_{MAX} of 210 GHz, attributed to a lack of optimisation, needed to increase. The team also identified a need to address the impact of heat dissipation by an inter-layer dielectric. This could degrade performance and reliability.

Jeong and co-workers tackled all these concerns by fabricating a monolithic 3D structure that did not suffer from a substantial degradation in RF performance when inserting a metal backside on top of the RF devices (see Figure 5) .

To form this superior structure, the team loaded InP substrates into an MBE reactor and grew an inverted HEMT heterostructure featuring a channel comprising a 3 nm-thick layer of InAs, sandwiched between a pair of 3 nm-thick $In_{0.53}Ga_{0.47}As$ layers. The next steps involved depositing a 40 nm-thick layer of SiO_2 on the silicon wafer, adding a patterned 40 nm-thick back metal, and covering this in a 600 nm-thick interlayer dielectric. Subsequent chemical mechanical polishing eliminated the step height and ensured the desired thickness for this dielectric layer.

A wafer-bonding process followed, involving the addition of 20 nm-thick layers of Al_2O_3 to both silicon and InP wafers. Once they were brought together, highly selective wet etching removed the InP substrate and the etch-stop layer, before molybdenum-based source and drain contacts were added and double-exposure e-beam lithography formed a 95 nm gate foot opening and a wide head. The final steps involved the use of citric acid to etch the n^+ $In_{0.53}Ga_{0.47}As$ layer, forming a T-gate by a deposition and lift-off process, and annealing the structure at 300 °C for 5 minutes.

Measurements on a device with a gate length of 95 nm and a gate width of 2 x 20 μm revealed an f_T of 301 GHz and an f_{MAX} of 716 GHz – the latter is claimed to be a record for monolithic 3D transistors. The researchers found that increasing back gate bias led to a slightly higher f_{MAX}, thereby providing enhanced flexibility to circuit design.

Thermal analysis revealed that self-heating is asymmetric, with more heat generated by the drain side (see Figure 6). According to high-resolution thermoreflectance microscopy, despite the poor thermal conductivity of the InGaAs channel compared with that made from silicon, the former has a 1.8 times smaller thermal resistance, thanks to the Al_2O_3 layer.

By comparing different device designs, Jeong and co-workers discovered that the addition of a local

An attractive alternative to transistors made from GaN and from GaInAs is the combination of InP and GaAsSb. This pairing can unite to form a type-II double HBT that is free from electron blocking and provides a conduction band offset of around 150 meV between the GaAsSb-base and the InP collector.

back metal decreased the thermal resistance by 19 percent compared with a device without a back metal. Turning to a global back metal provided a 31 percent improvement.

Although the insertion of a back metal introduced additional parasitic capacitance, this did not have a significant impact on f_T and f_{MAX}. As the reduction in these values is less than 7 percent, the slight reduction in RF performance can be compensated by adjusting the back gate bias.

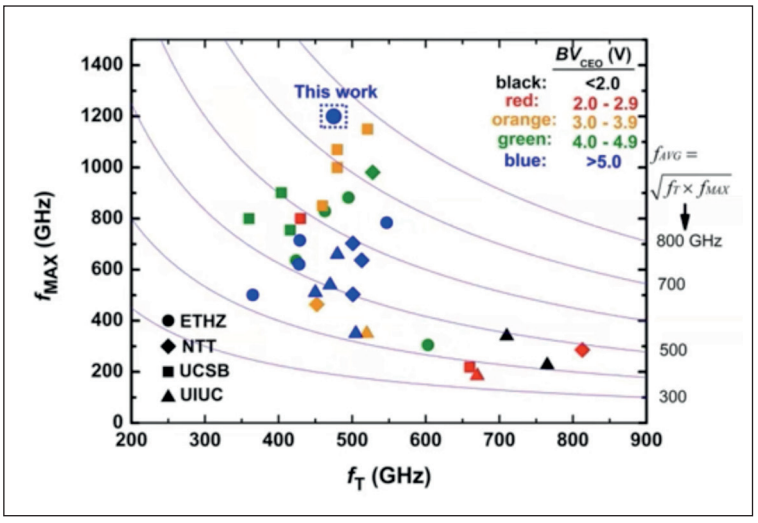
Efforts to improve InGaAs quantum well HEMT technology have also been undertaken by a collaboration between engineers at NTT, Japan, and three institutions in South Koera – Kyungpook National University, the University of Ulsan and Quantum Semiconductor Incorporation (QSI). This partnership has combined the fabrication of record-breaking HEMT designs with the development of accurate mathematical models, which have been lacking. The team's new physics-based models can predict f_T and f_{MAX} using just the physical and geometrical parameters of apparent mobility, saturation velocity and aspect ratio.

The portfolio of devices for this work included those with a cap recess etched, to accommodate transfer-length-method measurements; and those with gate lengths from 10 μm to below 30 nm, a range spanning the mobility relevant regime to the ballistic regime. An i-line stepper defined longer gates, while shorter variants were formed with electron-beam lithography. Most epilayer designs were produced on InP. They included devices with a 15 nm-thick $In_{0.53}Ga_{0.47}As$ quantum well, a 10 nm-thick $In_{0.7}Ga_{0.3}As$ quantum well, a 7 nm-thick $In_{0.8}Ga_{0.2}As$ quantum well, and an $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ quantum well with a thickness of 8 nm. In addition, the team used a GaAs substrate to produce a HEMT with a 10 nm-thick $In_{0.7}Ga_{0.3}As$ quantum well (Figure 7 details all the epistructures).

Speaking on behalf of the team at IEDM, Hyeon-Bhin Jo from Kyungpook National University detailed the record-breaking results, as well as providing an overview of progress in the performance of f_T and f_{MAX}. He pointed out that up until the early 1990s, increases in the f_T and f_{MAX} of III-V HEMTs were driven by scaling the gate length to below 100 nm, while from the mid 1990s to 2010, further increases in f_T came from enhanced transport, using indium-rich quantum-well channels.

"From 2010 to now, reductions in parasitics, such as series resistance and parasitic capacitance, have increased f_T, whereas there has been no further improvement in f_{MAX} – it has actually degraded."

Addressing this weakness, HEMTs produced by the team combine a high f_T with a high f_{MAX}, with both values benefitting from gate scaling. Plots presented by Jo show that the composite HEMT produced the best results, thanks to a superior average velocity in the $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ channel.



➤ Figure 11. Benchmarking double HBTs, with colour-coded breakdown voltages. The team from EPFL is claiming a new milestone for a f_{MAX} x V_{CEO} of 6.48 THz V.

For that design, a device with a 30 nm gate length combined an f_T of 706 GHz with an f_{MAX} of 962 GHz. "f_T continues to increase with gate length decrease," added Jo. "Contrarily, f_{MAX} shows its peak at a gate length of 30 nanometres, and decreases." According to him, the reason for this is the intrinsic output transconductance, which plays a more critical role for gate lengths less than 100 nm.

Jo and co-workers have benchmarked their results, considering f_T, f_{MAX}, and the average of these two figures of merit (see Figure 8). "The result for the composite channel HEMT shows the best balance and the highest average frequency for any transistor technology for all gate lengths."

Type-II triumphs

An attractive alternative to transistors made from GaN and from GaInAs is the combination of InP and GaAsSb. This pairing can unite to form a type-II double HBT that is free from electron blocking and provides a conduction band offset of around 150 meV between the GaAsSb-base and the InP collector.

Driving recent improvements to this particular device is a team at ETH-Zurich headed by Colombo Bolognesi. At IEDM, Akshay Mahadev Arabhavi spoke on behalf of this group, outlining a new fabrication technique that has led to record-breaking performances, including an f_{MAX} of 1.2 THz and a very high figure for the open base common-emitter breakdown voltage.

The latest work builds on previous results, which included an f_T of more than 450 GHz, an f_{MAX} in excess of 800 GHz, and a breakdown greater than 4.5 V. "In addition, and more importantly, these devices [from before] have a very good power performance," remarked Arabhavi, giving the example of an output power of more than 1 mW/mm at 94 GHz, alongside 12 dB of linear power gain and a maximum power-added efficiency of 30 percent.

The team's latest devices employ a new architecture that features a fin emitter and ensures a reduction in extrinsic base-collector parasitics. This comes from a reduction in the emitter-base access gap, realised without having to reduce the base metal thickness. "In fact, we have an even thicker base metal contact than before," argued Arabhavi, who added that the new design also offers control over the base metal contact width. This allows a reduction in the area of the junction and ultimately the extrinsic capacitance.

The team from ETH used MOCVD to grow the heterostructure for the HBT. Compared with the previous design, the thickness of the InGaAs emitter contact has been reduced from 35 nm to 10 nm and the heavily doped InP emitter thinned from 130 nm to 20 nm. Due to these changes, the total emitter thickness has been slashed from 185 nm to 50 nm. Note that the base and collector dimensions have not been changed.

Fabrication of the emitter-fin double HBT involved e-beam lithography and deposition to form an emitter metal structure, followed by argon sputtering, which simultaneously etched the GaInAs contact layer and smoothed the emitter metal edge roughness. A trilayer photo resist process followed, to form fins and set the base access distance, thanks to self-alignment (see Figure 9 for details). The final steps involved: the addition of a passivation layer; wet etching, to create a base-collector mesa; and a low-temperature etch-back planarization process, to support the electron-beam evaporated probe pads.

Arabhavi and co-workers made DC measurements on devices with a 35 nm base access distance and an emitter area of 0.25 μm by 4.4 μm. For collector currents of 1 kA cm^{-2} and 10 kA cm^{-2} – two common values for benchmarking – the common-emitter breakdown voltages were 5.4 V and more than 6.5 V.

For RF measurements on double HBTs, the team found that a variation in collector current produced changes to values for f_T and f_{MAX}. Using a collector-emitter voltage of 1 V, both frequencies peaked at a collector current density of around 9.2 mA mm^{-2}, with f_{MAX} hitting 1.2 THz and f_T climbing to 475 GHz.

The team also studied the values of f_T and f_{MAX} for a range of collector currents and emitter sizes (see Figure 10). Even devices with a 9.4 μm-long emitter had an f_{MAX} of more than 1 THz.

"This is a significant breakthrough in HBT scalability," argued Arabhavi, who believes these high values for f_T and f_{MAX}, along with the high breakdown voltage, make the ETH devices very promising (see Figure 11).

Thanks to this breakthrough, and those unveiled by other teams developing ultrafast transistors and ICs, foundations are being laid for communication at 6G and beyond. While it may be difficult to know quite what will follow with such fast data communication rates, we can be sure to expect that life in the virtual world has an exciting future ahead – and one that we will hopefully benefit from.

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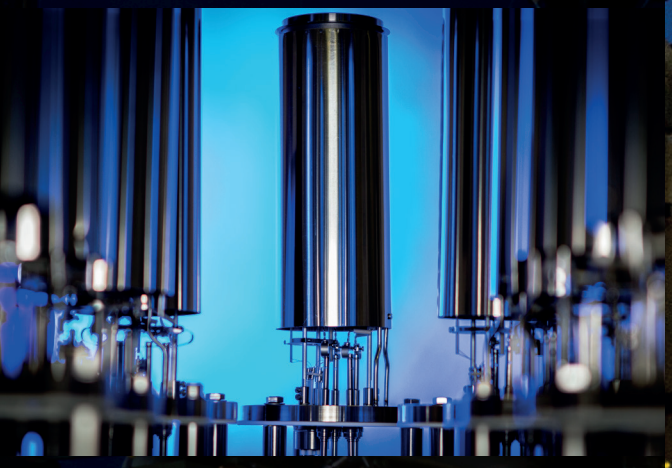

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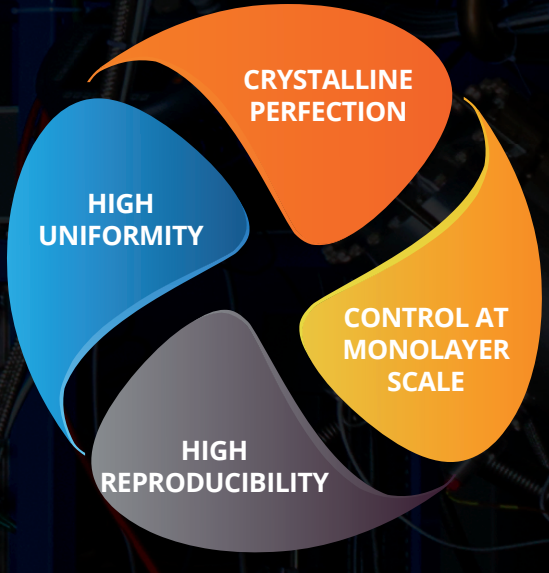

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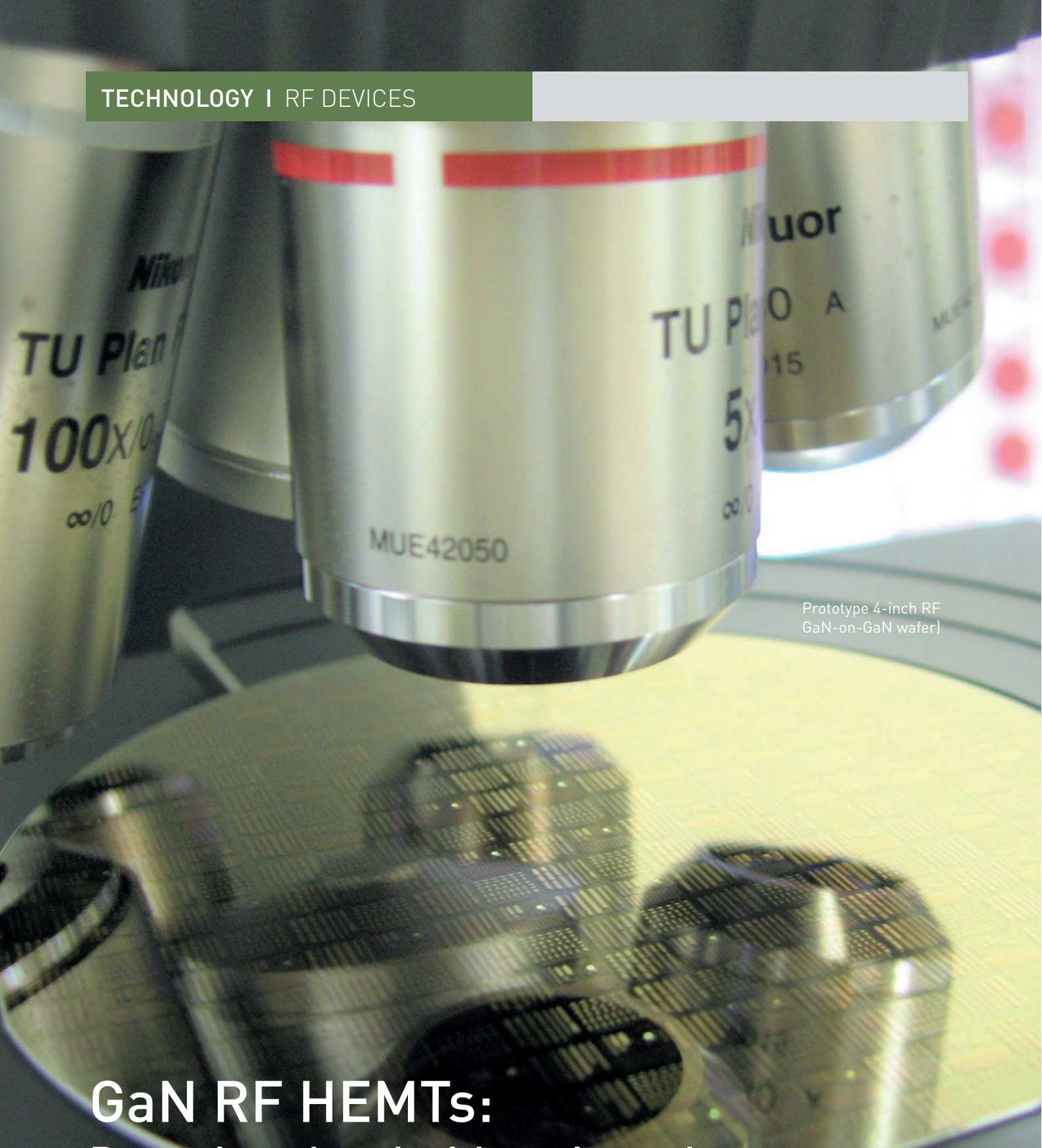


Prototype 4-inch RF GaN-on-GaN wafer)

GaN RF HEMTs:
Powering ahead with native substrates

GaN-on-GaN high-power amplifiers with through-substrate vias are delivering record-breaking power-added efficiencies and continuous-wave operation

BY NAOYA OKAMOTO AND YUSUKE KUMAZAKI FROM FUJITSU LIMITED

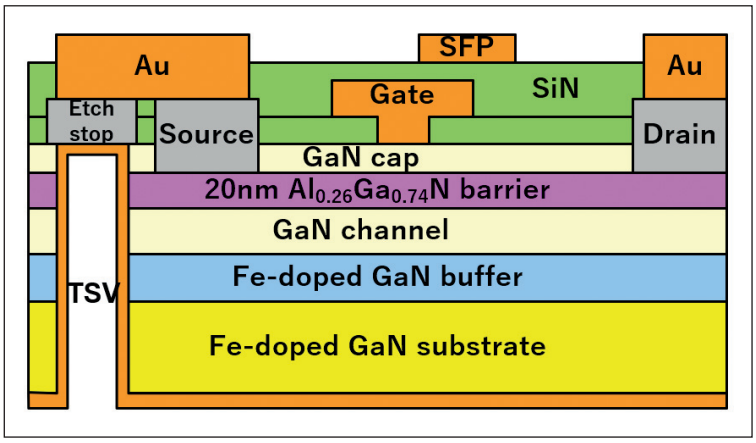
Electronic devices make our lives richer and more convenient. They are now taking us towards an advanced society, formed through the fusion of cyberspace and physical space. On entering this era, we will benefit from vast numbers of sensors in physical space collecting big data, quantitatively analysed by artificial intelligence in cyberspace. New value will be created from this, including the provision of high-quality services. Underpinning this new world order will be an increase in the use of radio waves above the microwave band to sense and collect data, alongside networks that exchange huge amounts of data, as well as sectors within industry that manufacture substances that bring new value. Supporting this introduction of a higher sensing resolution and a roll-out of a higher network capacity will be an increase in the frequency of solid-state power amplifiers deployed in radio equipment. A shift from microwaves to millimetre waves is already underway, and migration to the terahertz domain will follow.

Moving to higher frequencies is not trivial. Challenges are not limited to simply ensuring that devices can operate at higher speeds – there is also the issue of a reduction in the power conversion efficiency of solid-state power amplifiers at higher frequencies, leading to greater power consumption. This is at odds with a sustainable society, as to curb the carbon footprint of the communication sector, the power consumption of radio equipment must fall as the number of units increases.

The most efficient, powerful solid-state power amplifiers are based on GaN HEMTs. These RF transistors are typically fabricated on non-native substrates, such as SiC or silicon. However, the power and the efficiency of these devices are held back by electron traps that form in the GaN epilayers – mainly the buffer layer – and lead to current collapse.

Our team from Fujitsu, Japan, is tackling this issue head-on by switching the substrate to free-standing GaN. It is a solution we have been working on for many years. About ten years ago, when characterising the metal-insulator-semiconductor interface and the Schottky junction of GaN-based epitaxial layers grown on GaN substrates, we observed excellent crystal quality in this GaN-on-GaN heterostructure. But at this time only *n*-type, rectangular GaN substrates that were small in size were available. This restricted our development to the basic research phase.

Around 2017, when the availability of semi-insulating 2-inch GaN substrates began, we embarked on full-fledged work on RF GaN-on-GaN HEMTs. Initially, we directed our efforts at developing RF GaN-on-GaN HEMT power amplifiers for microwave heating. This project, supported by the Japan Ministry of the Environment, required transistors to run under severe conditions of high-power, continuous-wave operation. Realising success on these fronts would create a device that could serve in other applications, such as radar and wireless communication. However, progress would not be easy, due to the lower thermal conductivity of the GaN substrate compared with that made from SiC.

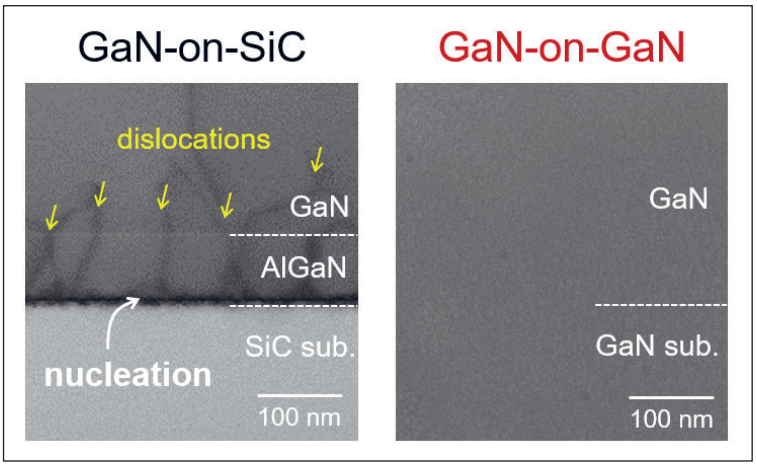


➤ Figure 1. Fujitsu is a pioneer of the RF GaN-on-GaN HEMT power amplifier.

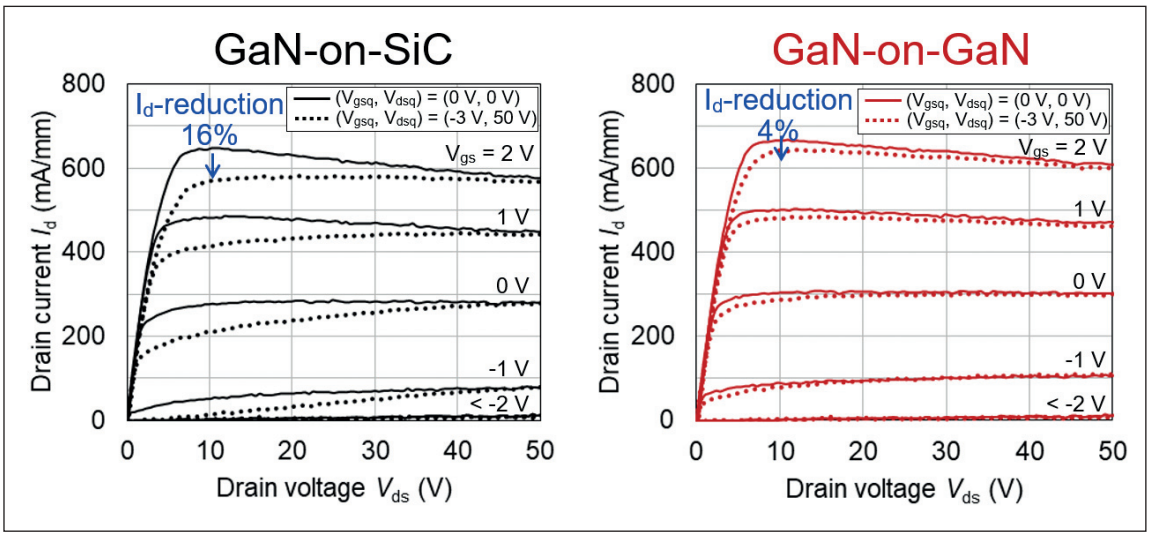
Recently, we have shown that this concern can be overcome by: increasing the power-added efficiency, through improvements to the GaN substrate/epilayer interface; and developing GaN through-substrate vias that reduce the source inductance (see Figure 1).

Targeting record-breaking efficiencies

As more efficient devices minimise self-heating, we decided to aim for a record-breaking power-added efficiency. Young researchers within our team spearheaded in this effort, leading the development of front-side devices for RF GaN-on-GaN. This project kicked off by comparing the quality of GaN epitaxial crystals grown on a conventional SiC substrate and on a GaN substrate (see Figure 2). Scrutinising these materials revealed a dislocation density in the GaN grown on SiC of 2×10^8 cm^{-2}, compared with less than 10^6 cm^{-2} for GaN grown on a native substrate. In addition, HEMTs were fabricated from these epiwafers to obtain basic device characteristics. Results confirmed that GaN-on-GaN transistors have diminished current collapse compared with their GaN-on-SiC counterparts, due to superior crystal quality (see Figure 3). However, measurements of the power



➤ Figure 2. Transmission electron microscopy underscores the superior material quality of GaN-on-GaN compared with GaN-on-SiC.

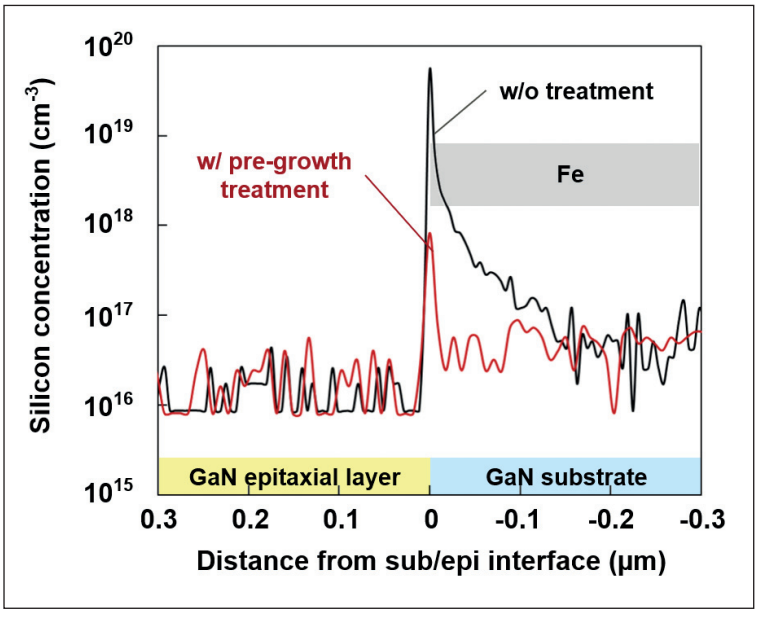


➤ Figure 3. Pulsed current-voltage characteristics show that GaN-on-GaN RF HEMTs suffer from less current collapse than those based on GaN-on-SiC.

output at high frequencies were disappointing, with the power-added efficiency for GaN-on-GaN HEMTs buried within conventional GaN-on-SiC data.

How can it be that despite a far better crystal quality, the power produced by this native device is no better than that for a GaN-on-SiC HEMT?

Investigations eventually revealed a conductive layer at the GaN substrate/epitaxial interface, stemming from silicon contamination. The level of silicon is not insignificant, having a concentration more than an order of magnitude higher than that of the iron concentration within the GaN substrate (see Figure 4). Note that a quarter of a century ago, a similar problem plagued GaAs substrates. Their surfaces can be riddled with the likes of silicon, carbon and oxygen, impurities activated by improvement of crystal quality through homoepitaxy. The young researchers in our team were unaware of this issue, as it had not been a problem when growing GaN epilayers, due to the use of non-native substrates.



➤ Figure 4. Secondary ion mass spectrometry (SIMS) showed that pre-treatment of the GaN substrate can prevent high levels of silicon contamination.

To address this issue, we turned to wet processing the substrate surface prior to epitaxial growth (see Figure 4). This approach reduced the silicon concentration to below that for iron, leading to suppression of the high-frequency leakage path. Thanks to this, we could realise a record-breaking power-added efficiency of more than 80 percent in the 2.45 GHz ISM-band (see Figure 5).

The virtue of vias

Another important technique for improving the performance of power amplifiers based on the RF GaN-on-GaN HEMT is to add GaN through-substrate vias, as this reduces the source inductance. Taking this approach is not a novel – it is already applied to commercially available GaN-on-SiC devices. We have been working on this for some time, having started to develop through-substrate vias for GaN when we began device development.

Our efforts began by investigating GaN etching. Employing inductively coupled plasma etching, using a mix of chlorine and boron trichloride gases, we targeted an etching rate of at least 1 µm/min and an etching selection ratio of 30 or more, using a nickel metal mask. While success came relatively quickly, we still had challenges associated with the formation of pillars (see Figure 6).

Previous experience associated with SiC via hole etching had taught us that inclusions contained in the SiC substrate could impact pillar formation. To see if this issue remained with GaN, we scrutinised the bottom surface of these substrates with a scanning electron microscope. However, we failed to find any inclusions on GaN substrates grown by HVPE with void-assisted separation. Note that this might not be the case with GaN substrates grown by other methods, such as ammonothermal and sodium-flux – we simply don't know.

We then focused on the wafer surface temperature during etching. Using almost identical plasma power conditions, we found that etching SiC involved a wafer

surface temperature of 200 °C or more. In comparison, for GaN the temperature could be as low as 90 °C, making the etching by-product difficult to remove. To address this concern by promoting the desorption of the etching by-product, we increased the wafer surface temperature by dialling back the cooling helium pressure. This action immediately solved the pillar problem (see Figure 6). With optimized etching conditions, we could successfully form a GaN via hole with a depth of 91 μm, using a GaN etching rate of 1.5 μm/min and a selectivity to the nickel metal mask of 35.

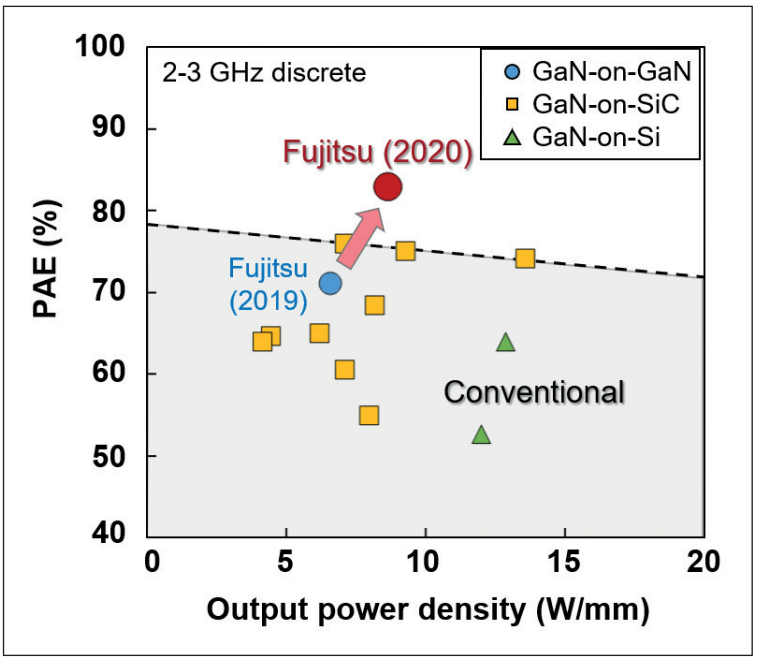
However, another issue emerged: etching selectivity fell to one-third of that for conventional SiC etching, falling from a value of around 100 to about 35. The reduced selectivity impacted the thickness and the process for the front-side etch stop. Compounding matters, the remaining metal mask for via etching interfered with the stealth dicing of the GaN substrate. To overcome these problems, we refined our process for forming vias in GaN (see Figure 7).

Upping the power

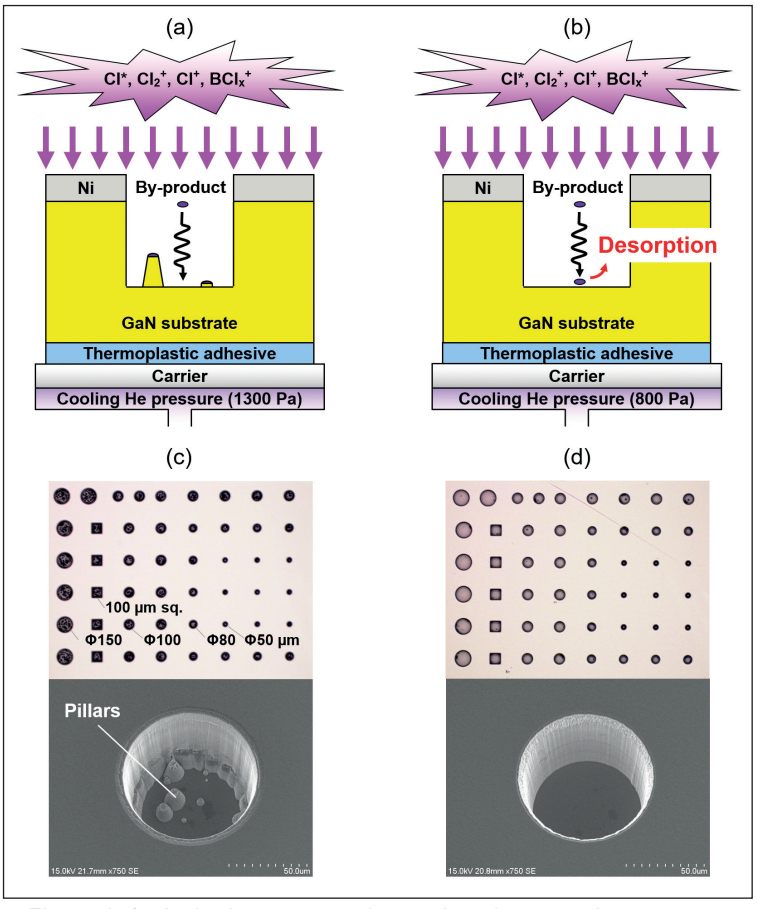
Thanks to this progress, we were now in a position to draw on all our development and integrate our technologies. Due to the lower thermal conductivity of GaN than SiC, we had concerns relating to heat radiation characteristics. Encouragingly, we could realise heat dissipation characteristics comparable to those for GaN-on-SiC by drawing on thermal simulation and introducing backside processing (see *Compound Semiconductor* **25** Issue 7, October, 2019, p32). But we were still to demonstrate GaN-on-GaN high-power amplifiers with output powers greater than 50 W.

Now this value has been exceeded with a GaN-on-GaN high-power amplifier featuring a through-substrate via, 36 gate fingers, a gate length of 0.5 μm, a unit gate width (W_{gu}) of 300 μm, a gate-to-gate spacing (L_{gg}) of 30 μm, and a total gate periphery of 10.8 mm. This chip has a W_{gu}/L_{gg} aspect ratio of 10, creating a very severe condition for heat dissipation.

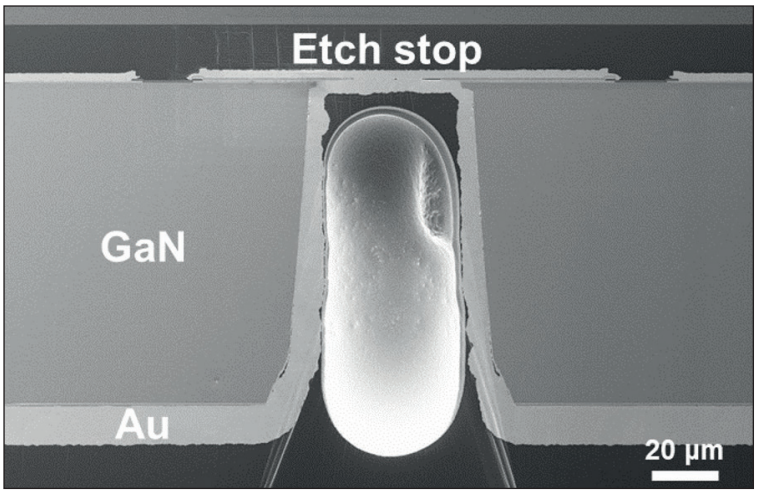
After mounting our chip on an evaluation board, we carried out large-signal measurements that produced an excellent set of results (see Figure 8). Driven in pulsed mode, using 10 μs pulses and a 1 percent duty cycle, our amplifier delivered a maximum output power of 64.3 W and a peak power-added efficiency of 71.1 percent at 2.6 GHz. Running in continuous-wave mode produced a slight reduction in performance, due to self-heating, with values of maximum output power and power-added efficiency falling to 54.6 W and 63.3 percent. According to the simulated transient response, we think that the difference in channel temperature between continuous-wave and pulsed operation can be as high as 100 °C. However, the realisation of continuous-wave operation indicates that our GaN-on-GaN HEMT power amplifier has suitable heat dissipation characteristics, and eliminates concerns regarding this particular technology.



➤ Figure 5. Supressing silicon contamination leads to a hike in the power-added efficiency of discrete GaN HEMTs operating at 2-3 GHz.



➤ Figure 6. Optical microscopy and scanning electron microscopy images (c) and (d) show that switching from conventional conditions (a) to optimum conditions (b) improves the etching of by-products.



➤ Figure 7. A cross-sectional scanning electron microscopy image of a GaN through-substrate via of a GaN-on-GaN HEMT.

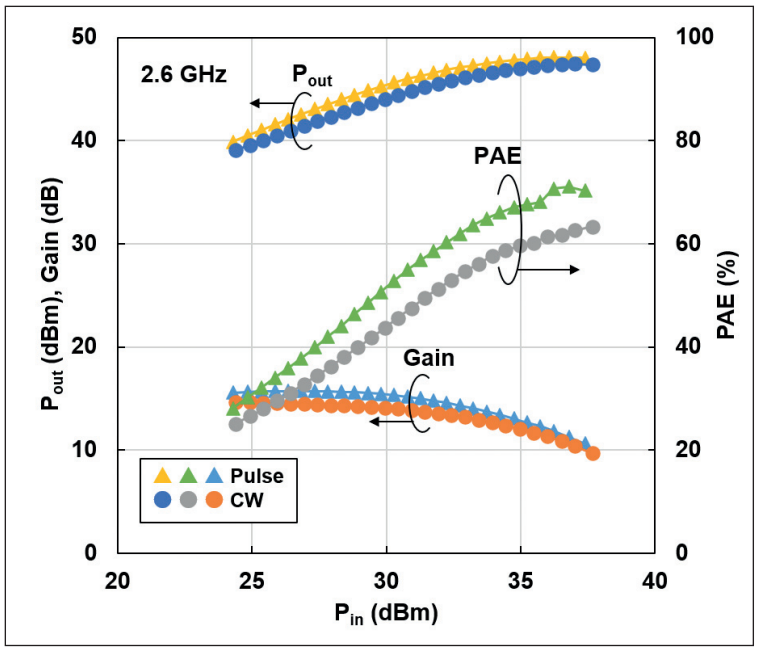
Looking ahead

Two of the biggest issues facing RF GaN-on-GaN HEMTs are the cost of these devices and the size of the substrate. Progress is being made with the latter: a 4-inch iron-doped GaN substrate has already been commercialized, and a 6-inch GaN substrate will soon be realized. Even so, prices are still quite high, and need to fall to at least the same level as SiC to enable the commercial launch of RF GaN-on-GaN HEMTs. Ensuring that this happens requires not only the efforts of substrate manufacturers, but also demand for power and optical devices, as well as RF devices.

It is also anticipated that problems will arise in device manufacturing, along with the enlargement of the diameter. Our team is playing its part in addressing these important issues by starting to fabricate 4-inch RF GaN-on-GaN epiwafers. While the efficiency of the GaN devices decreases with increasing frequency, we expect that this decline can be suppressed with high-quality crystalline material. Devices featuring such epilayers are tipped to ensure ultra-high data rates for beyond 5G and 6G, realised by using GaN-on-GaN with ultrafine gates.

Another opportunity for improving device performance is to introduce architectures that combine the high crystal quality of GaN-on-GaN with materials with great thermal conductivity. Options for high-performing heat spreaders include diamond. However, its addition would need to be cost-competitive, just like the introduction of GaN substrates.

This research was partially supported by the Japan Ministry of the Environment, as part of the Project of GaN technology innovation for enabling decarbonized society and lifestyle.



➤ Figure 8. Power characteristics of a GaN-on-GaN HEMT power amplifier in pulsed (closed triangles) and continuous-wave (closed circles) operation.

FURTHER READING

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Photo Credit: Matthias Baumbach

Towards efficient spaceborne millimetre-wave transmitters

Through the project Kassiopeia, a European team is developing highly-efficient microwave and millimetre-wave amplifiers based on an iridium-sputter gate technology and a novel buffer

BY JOACHIM WÜRFL FROM THE FERDINAND-BRAUN-INSTITUT, BERLIN

OVER THE LAST DECADE and more, there has been a significant increase in the maturity of GaN transistors and MMICs for microwave applications. Improvements in this regard, reflected in the technology readiness level, are allowing engineers to now implement these devices into mission critical systems.

One example of this is the deployment of decentralised microwave power sources in space applications. In this case, using GaN opens the door to light-weight, electronically controlled beam-steering systems, powered with many pixels of active antennas.

Designers of such systems need to consider the pros and cons of using GaN, which majors on flexibility and low weight, but is compromised by its efficiency. To address this shortcoming, it is incredibly important to bundle existing technologies and optimize them along the whole value-added chain – from the semiconductor substrate to epitaxy, processing, circuit design and system implementation.

Our team is taking this approach through a project that commenced on 1 March 2021 entitled Kassiopeia – an acronym for Ka-band MMICs using novel epitaxy, processing and circuit concepts towards highly efficient GaN and AlN devices. We are supported by the European Space Agency, in the frame of the ARTES Advanced Technology initiative on European Ka-band high-power solid-state technology for active antennas.

➤ Automatic processing facilities in new FBH clean room

To meet our project's goals, we are drawing on the expertise of several European partners. It is only through collaboration and the ensuing optimization of devices that incorporate many different technologies that we are able to develop highly-efficient microwave and millimetre-wave amplifiers. Together we are aiming to address self-heating, as well as static and dynamic loss mechanisms, as they are known to adversely influence power amplifier efficiency.

Varying roles

A key partner in our project is the epitaxial wafer provider SweGaN. This company is renowned for its fabrication of GaN epitaxial stacks for millimetre-wave transistors. These stacks feature a significantly reduced thermal impedance between the heat source in the device and the heat sink, together with minimized dispersive dynamic effects due to the proprietary epitaxial structure. It is a virtue that comes from the proprietary buffer-free epitaxial approach, which ensures an efficient heat drain to the semi-insulating SiC substrate.

Also playing an important role in Kassiopeia is the Ferdinand-Braun-Institut (FBH). When it comes to GaN RF devices, its unique selling point is its iridium sputter-gate technology, which reduces dynamic losses – that is, gate lagging – to typically just 5 percent. This value is at least half of that of competing institutional and industrial technologies. Additional attributes include a high level of reliability, which is especially important for spaceborne devices. What's more, FBH has a proven track record in GaN MMIC design, processing and circuit characterization, undertaken in one of the best equipped labs in Europe.

Another key player in the Kassiopeia project is the team at the University of Bristol. They have extensive experience of thermal simulations, combined with direct measurements of the heat source temperature distribution in active GaN FETs.

The over-arching goal of Kassiopeia is to holistically improve Ka-band MMIC efficiency, power density, linearity and reliability. Success will come through a systematic analysis of current technology, with respect to parameters that increase device efficiency, linearity and millimetre-wave power density.

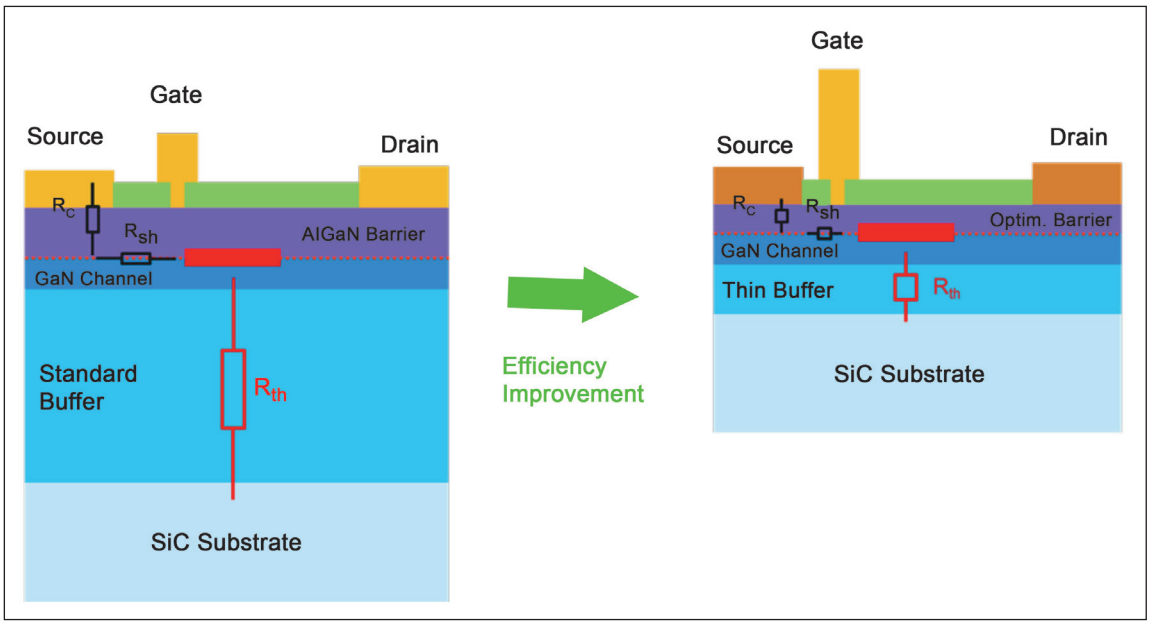
Chasing targets

Several parasitic elements are still limiting the performance of GaN-based MMICs (see Figure 1 for an overview of the most important parasitic elements). Through Kassiopeia, we will be developing and refining innovative technological concepts to reduce parasitic elements and incorporate them with novel MMIC design concepts. Our target is to demonstrate GaN MMICs, operating in the frequency band spanning 17.3 GHz to 20.2 GHz, at a power level of up to 43 dBm, while delivering a power-added efficiency of 50 percent and a noise-power ratio of 15 dB.

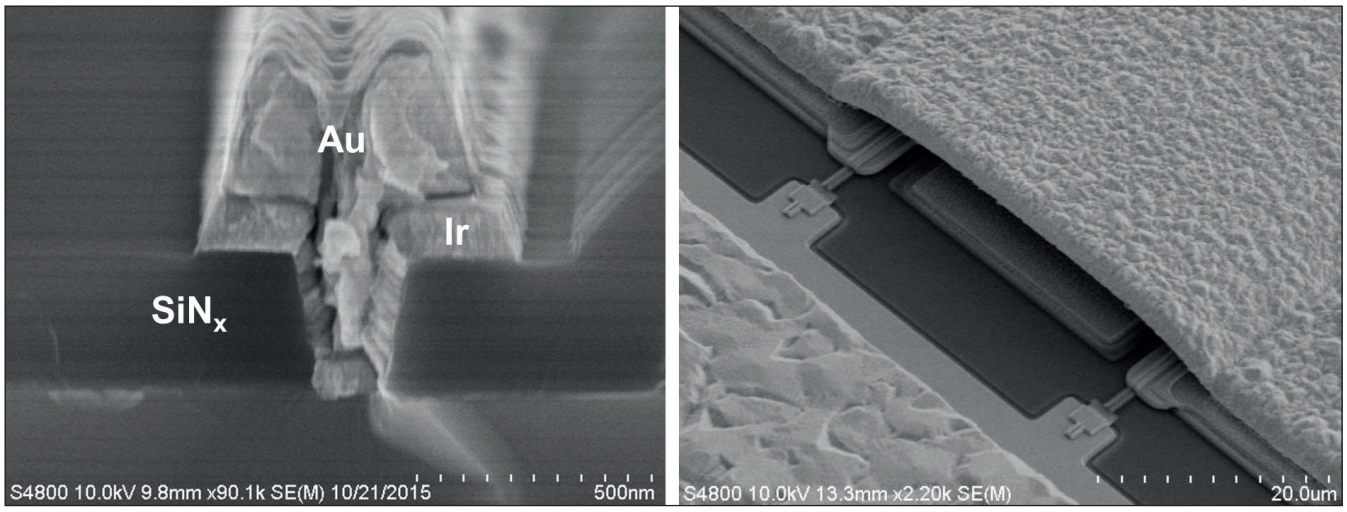
Our development is supported by innovative processing equipment and characterization tools, available at FBH thanks to funding within the framework of the Research Fab Microelectronics Germany – FMD. When making these developments, much consideration is given to the possible transfer of our technology to one of Europe's GaN foundries.

Substantial technological efforts are being made within Kassiopeia to trim parasitic resistances and increase thermal coupling between the heat source, located in the device's channel region, and the SiC substrate. All optimisation involves FBH's 4-inch GaN Ka-band process line, featuring iridium-sputter gate technology (see Figure 2).

When developing high-performance microwave power amplifiers, it is crucial to reduce the transistor knee-voltage, because this ensures efficient use of the load-line offered by the device. With highly scaled millimetre-wave devices, total on-resistance may be dominated by the transfer resistance of the source



➤ Figure 1. Through the Kassiopeia project, a European collaboration is pursuing holistic technology improvements that aim to enable high power, efficient Ka-band transistors and amplifiers.



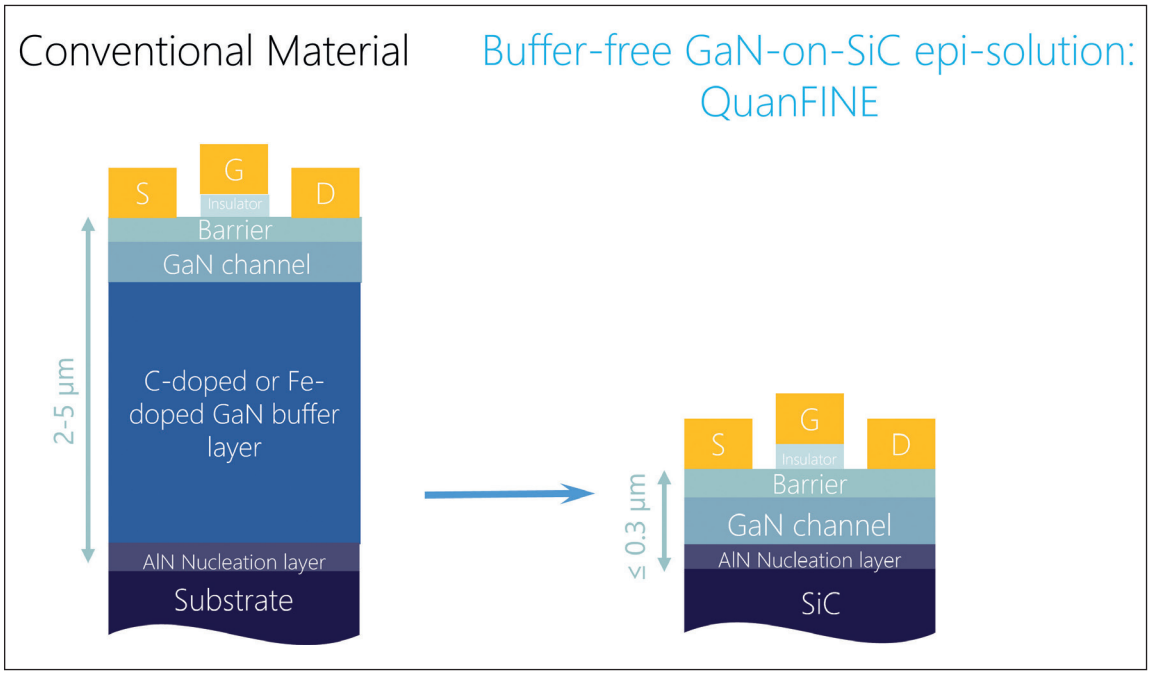
➤ Figure 2. FBH baseline technology for X and Ka-band MMICs: (left) 150 nm gate using iridium-sputter technology to fully conformally coat the gate trench; (right) an air-bridged X-band power cell using source-connected field plates.

and drain ohmic contacts. To minimise this, there is a need to drive down the ohmic contact resistance, the sheet resistance between source and drain, and the total sheet resistance (see Figure 1).

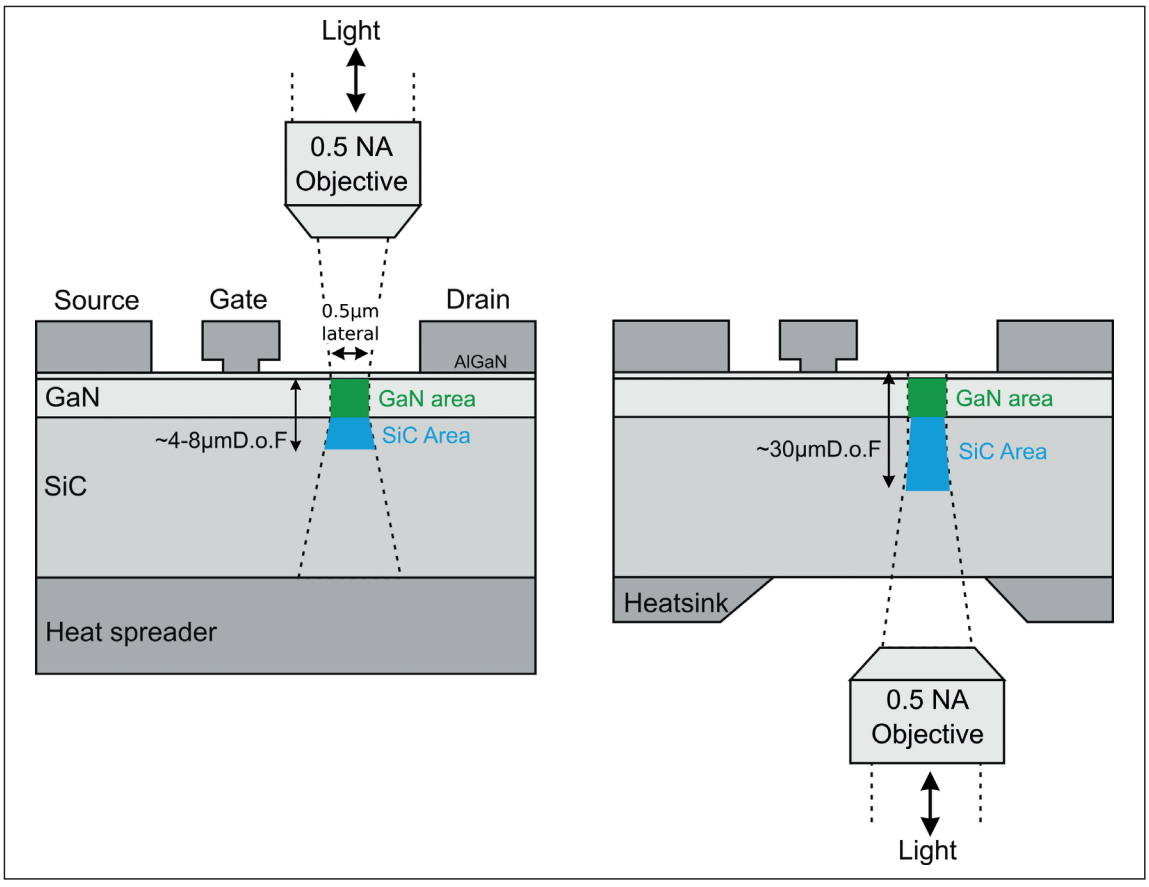
Factors that influence the contact resistance include the metallurgy of the contacts, as well as the quality, doping and bandgap energy of the semiconducting material underneath it. To try and trim the contact resistance, we are investigating the impact of increasing the AlGaN barrier doping by local ion-implantation. After implantation, we deposit and activate a refractory ohmic contact, which has the hallmark of an extremely precise edge acuity. Thanks to this attribute, we drive down the contribution of the channel sheet resistance to the total source resistance, and thus deliver a further reduction in the knee voltage.

Improvement is also been pursued in the metallic gate strip. Efforts are being directed at increasing its electrical conductivity, because this will enable a more flexible and efficient design of millmetre-wave power cells. Success could come from introducing longer gate fingers per cell – this trims taper losses for more extended power cells. To explore this possibility, we are developing a high-aspect-ratio gate metallization with a comparably low contribution of parasitic capacitances. Key to this is innovative electroplating techniques, utilising FBH's sputtered iridium gate process to temporarily provide a plating base.

Ensuring efficient power amplification and reliable device operation hinges on a reduction in the thermal impedance between the transistor's heat source and the SiC substrate. To optimise heat transfer from the device to the substrate, we employ SweGaN's QuanFINE buffer technology. This platform enables direct growth of a high crystalline quality epitaxial stack, featuring a GaN channel on top of a thin AlN nucleation layer (see Figure 3 for a comparison between this approach and the conventional method). Merits of the use of the QuanFINE buffer technology



➤ Figure 3. Comparison of standard epitaxial approaches for GaN microwave transistors and the QuanFINE concept proposed by SweGaN.



➤ Figure 4. Scanning the internal heat source of transistors by micro-Raman technology. The technique can be applied from the top of the device, and also from the underside, through an opened backside metallization.

extend beyond very good thermal coupling. The AlN back-barrier efficiently confines electrons to the channel, thereby enhancing the breakdown voltage for a given gate-drain distance. The upshot, as we'll soon see, is higher power-density transistor designs.

Putting it all together

We will use all the technologies discussed to enable innovative power-cell designs. This will enable us to integrate larger gate peripheries into one transistor cell, and in turn increase the respective power level and power density. Ultimately, this will lead to a higher total amplifier power, alongside greater linearity and bandwidth.

One downside of a higher power density is that it exacerbates confined heat generation. Consequently, it is indispensable to undertake thermal considerations. In the Kassiopeia project we are doing this, with those at Bristol University taking the lead and offering much insight into the thermal designs of power cells. Efforts involve thermal simulations, and correlation of these results with thermal characterizations using micro-Raman techniques that provide a sub-micron spatial resolution (see Figure 4).

The team at Bristol uses a focused laser beam to scan the device, either from the top, or from the bottom through window openings in the backside metal. The latter orientation enables thermal device characterization of field-plated devices. Whichever geometry is employed for this measurement, micro-Raman characterization provides a precise mapping of the transistor's heat source. This enables the thermal fingerprint of any modification in device technology and layout to be directly revealed. By adopting this approach, the thermal modelling base is iteratively improved, ultimately leading to well-engineered Ka-band power cells.

To optimize targeted-power MMICs at the circuit level, our collaboration is focusing on low-loss combining, alongside the implementation of highly efficient, harmonically tuned amplifier concepts such as class-F, class-F^{-1}, and Class-J. These concepts provide proper termination of harmonics and significantly reduce transistor losses by establishing zero-voltage crossing conditions in the transistor. Once these new power cells have been optimised, they will be modelled and implemented into the final MMICs, with all improvements realized, tested and characterized on FBH's professional 4-inch process and testing environment.

Through these endeavours Kassiopeia will tackle the most important aspects of Ka-band device improvement. When success follows, it will provide a pathway to high-efficiency spaceborne millimetre-wave communication systems that are especially suited for future beam steering applications.

The European Space Agency (ESA) supports Kassiopeia in frame of the ARTES Advanced Technology initiative on European Ka-band high-power solid-state technology for active antennas (https://artes.esa.int/news/artes-advanced-technology-workplan).

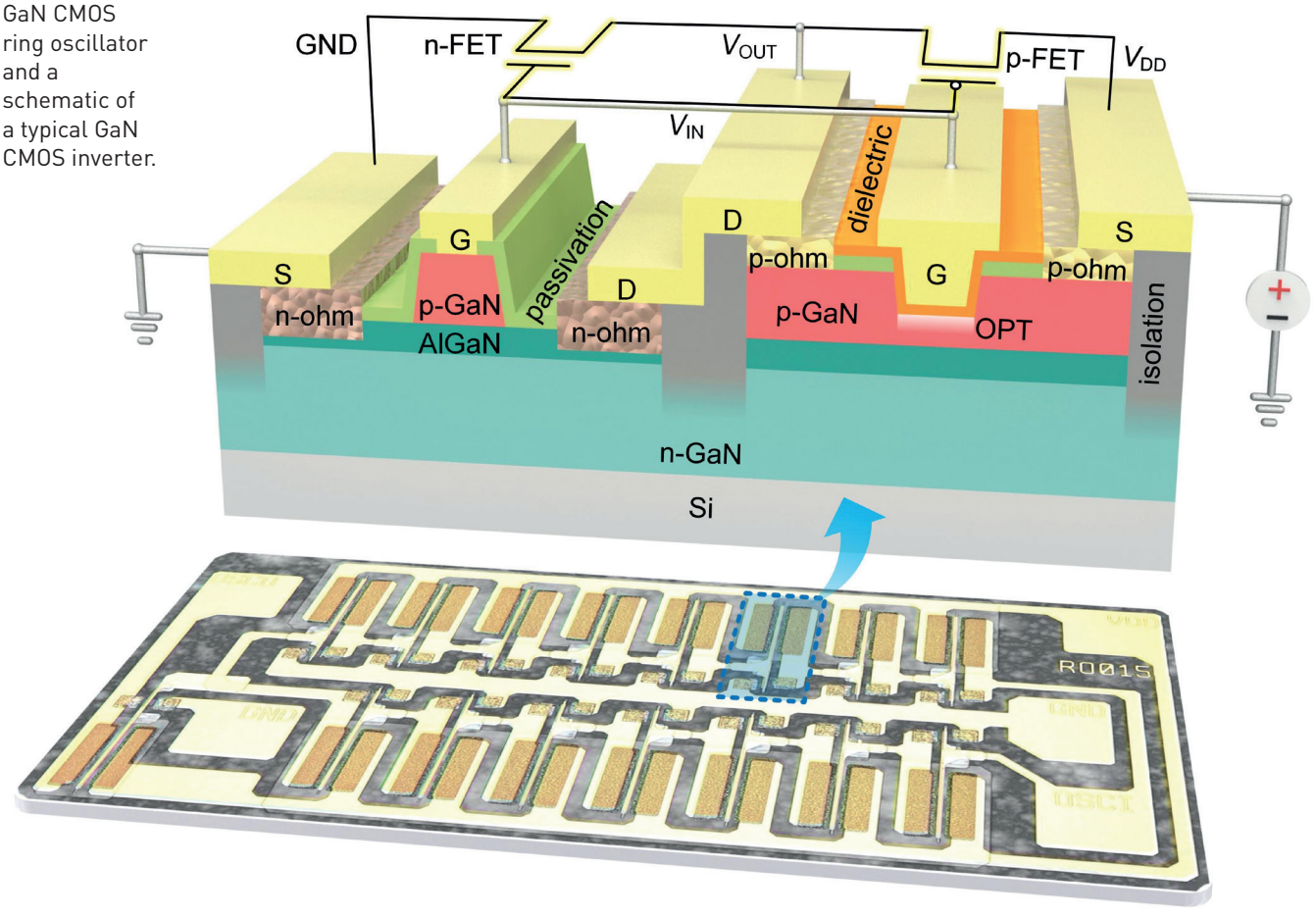
Taking GaN CMOS to the IC

Forming logic circuits with a power HEMT platform that features a *p*-GaN gate provides a significant step towards unlocking the full potential of GaN integration

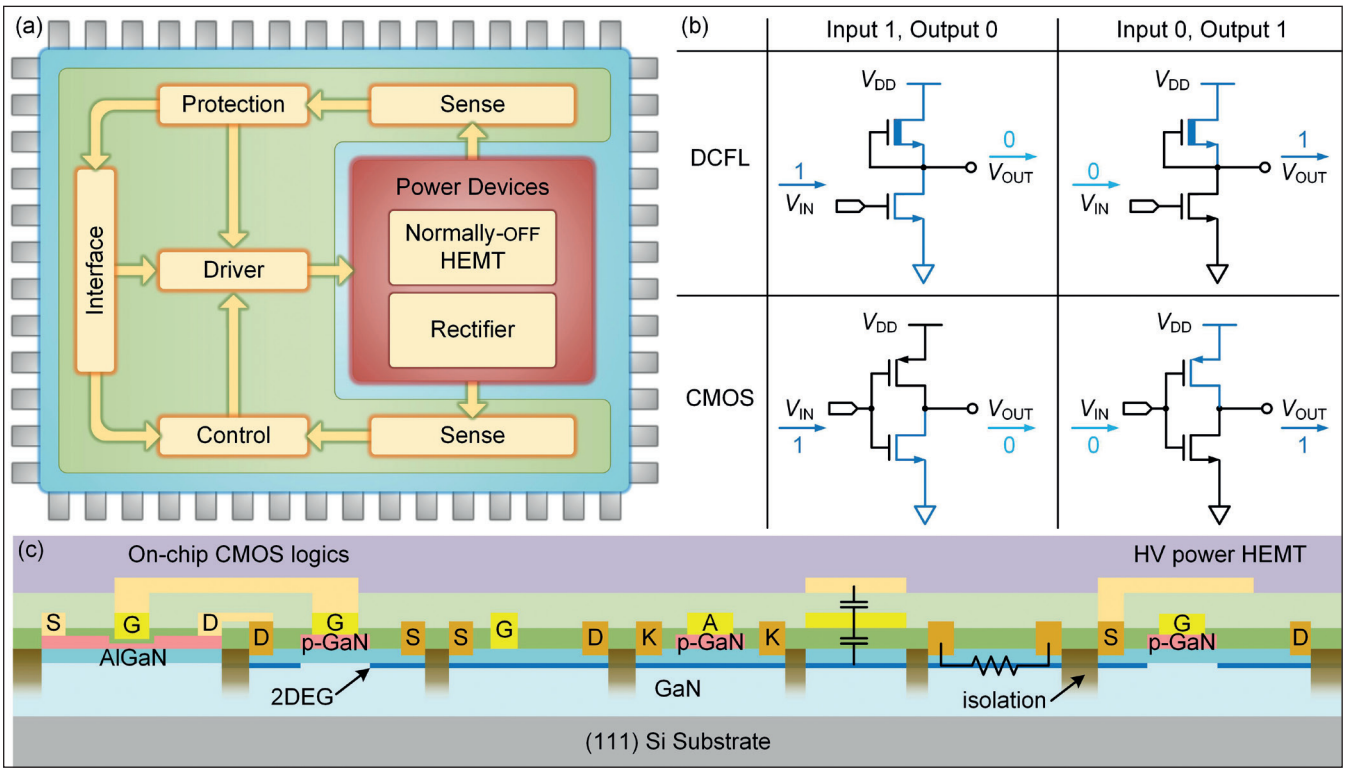
BY ZHEYANG ZHENG, LI ZHANG AND KEVIN CHEN FROM
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

CMOS TECHNOLOGY continues to prevail in very large-scale and mixed-signal ICs. In these forms of circuit, CMOS has dominated for the past four decades, thanks to topping the list of the most energy-efficient circuit topologies. Whenever new electronic devices are explored in other semiconductor materials, there is a hunt for complementary devices, to see whether this could lead to a superior successor to silicon CMOS. However, such a pursuit tends to be full of obstacles, with GaN providing a typical example.

This wide-bandgap semiconductor, blessed with an inherent capability to form a very high-mobility two-dimensional electron gas (2DEG) channel, has many attractive attributes. This has driven widespread



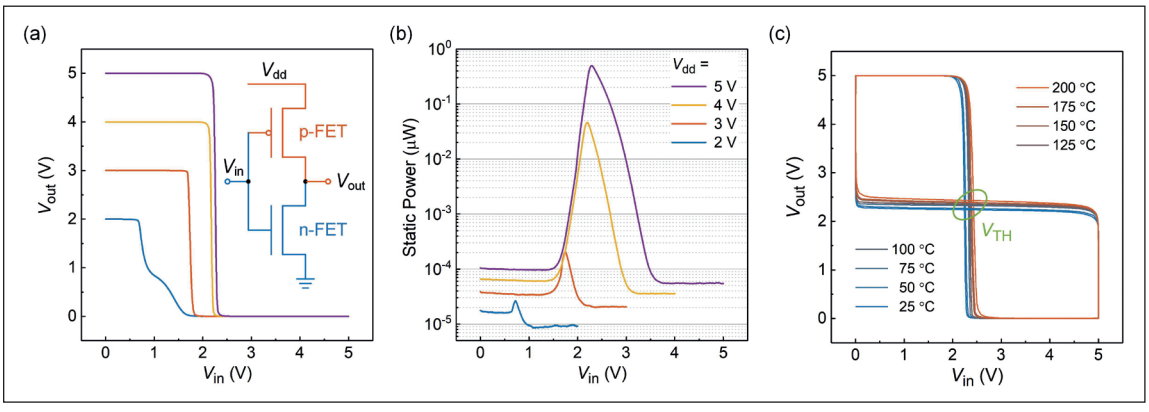
➤ A 15-stage GaN CMOS ring oscillator and a schematic of a typical GaN CMOS inverter.



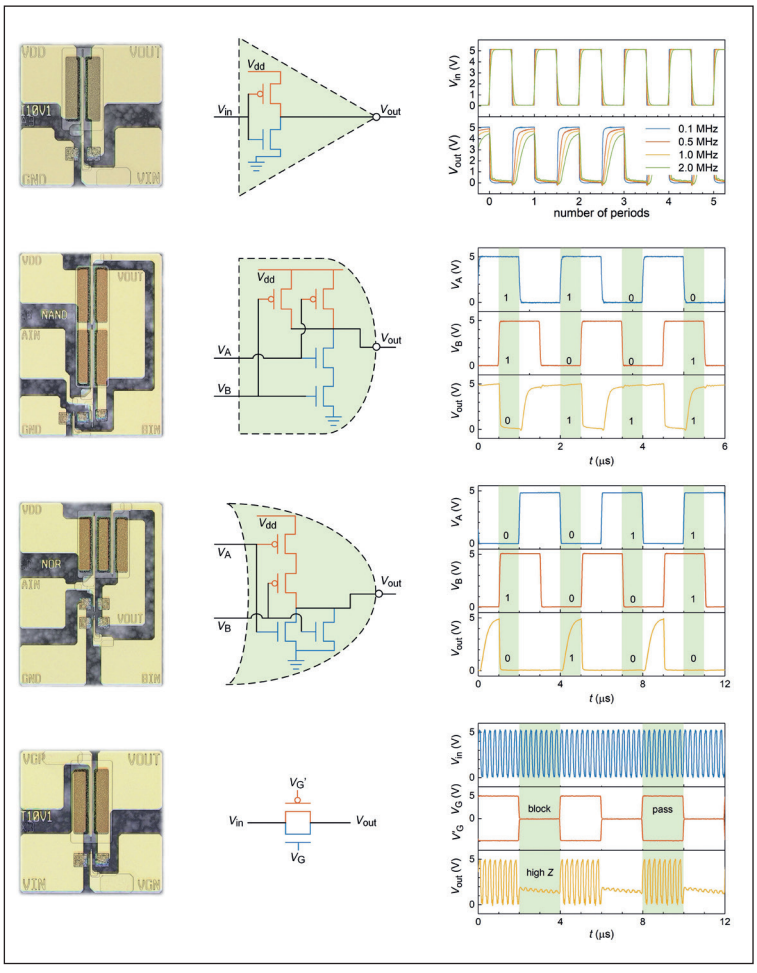
➤ Figure 1. One attractive approach to fully unlocking the potential of GaN in power electronics is the monolithic integration of the entire power conversion system. (a) depicts a GaN-based smart power platform. (b) illustrates that when a logic inverter is made of *n*-FET-based topologies, such as directly-coupled-FET-logic (DCFL), there would be one logic state when the gate has significant static power dissipation. Using the CMOS topology instead could guarantee the suppression of static power dissipation at both states; (c) is a cross-section view of available components on the *p*-GaN gate power HEMT platform. The on-chip CMOS logics would be inducted onto this platform.

deployment of *n*-channel GaN HEMTs in 5G base stations, as well as ultra-compact power adaptors and supplies for mobile devices. In the near-term, more exciting applications are sure to emerge that are power-hungry, yet demand ultra-compactness in power supplies. This will create an appreciable market for GaN. However, much is still to be done when it comes to GaN CMOS. Efforts have been held back by undesirable material properties for implementing *p*-channel FETs and a lack of essential applications that would spur development.

Part of the problem with *p*-channel devices is the very low hole mobility in GaN. It is typically just 20 $cm^2 V^{-1} s^{-1}$, compared with around 2000 $cm^2 V^{-1} s^{-1}$ for the electron mobility in the 2DEG channel. Such a low value dampens the interest of many researchers. What's more, there doesn't appear to be a need for GaN CMOS in power amplifiers and power switches. GaN HEMTs tend to act as powerful discrete devices, usually incorporating a very large gate width for regulating high currents and handling high powers. Consequently, despite the rapid development of GaN



➤ Figure 2. A GaN CMOS logic inverter shows impressive quasi-static performances, including rail-to-rail operation, V_{DD}-adaptive and well-placed transition thresholds, substantially suppressed static power dissipation, broad noise margins, and high thermal stability.



➤ Figure 3. HKUST has demonstrated a full family of elementary logic gates with GaN CMOS. This figure shows their photos, circuit diagrams, and operating waveforms with sub-megahertz frequencies.

HEMTs, demonstrations of GaN *p*-FETs are few and far between, with efforts related to CMOS logic inverters even rarer.

Now the situation has started to change. With GaN power HEMTs intensively advanced, peripheral circuitry is starting to become a non-negligible performance-limiting factor for the entire power conversion system. Parasitic inductances are the most undesirable but inevitable issue – they are induced by interconnections between power HEMTs and other off-chip functional blocks, such as the gate driver and miscellaneous sensing modules. By hampering the continuous push towards higher operating frequencies, these inductances are compromising the superiority of the GaN HEMT. One promising solution is monolithic integration – that is, the deployment of as many peripherals as possible on the same chip as the GaN HEMTs.

Our team at The Hong Kong University of Science and Technology (HKUST) have been developing integrated GaN technology for many years. The planar structure for this class of device inherently favours high-density monolithic integration (see Figure 1).

Back in 2009 we proposed the concept of 'GaN smart power systems', and since then we have kept on advancing this technique, working in partnership with colleagues in academia and industry.

As more and more functional blocks have been demonstrated, and entire systems have got more and more complicated, there has been a significant increase in the use of logic circuits. In fact, it is these logic circuits that make the power system 'smarter' and more intelligent. For GaN, logic circuits are still constructed from just *n*-channel FETs. Due to this, as the number of logic gates increases, power consumption has become a concern. It is this state-of-affairs that hampered the silicon-based ICs of the late 1970s. Back then, NMOS logic circuits consumed too much power, giving rise to CMOS.

With a potential beneficiary in mind, we wanted to develop GaN CMOS. Due to the low mobility of holes, we knew that this technology would never be deployed in cutting-edge ultra-high-speed/low-power logic ICs. However, it could deliver on-chip logic services for specific applications, such as power electronics, thanks to its high energy efficiency. We were also intrigued in how much we could benefit from the *p*-GaN epi-layer that is readily available in the *p*-GaN gate power HEMT technology, a dominant platform for commercial GaN power electronics.

The GaN CMOS family

Three immediate benefits come from using the commercial *p*-GaN gate HEMT epi-structure to produce GaN CMOS ICs. First, this enables straightforward integration with the power HEMT. This is most welcome, given the commercial opportunity associated with the monolithic integration of high-energy-efficiency peripheral logic gates with power switches. Second, owing to the maturity of power HEMT technology on this platform, GaN *n*-FETs for CMOS ICs are naturally ready. All that's required to move from power to CMOS is to make some simple changes in the physical layout, because *n*-FETs for both applications share exactly the same device structure and fabrication steps. Third, the *p*-GaN layer is designed to deplete the 2DEG channel underneath, which could only be restored by removing the *p*-GaN layer above. This enables the *p*-channel and *n*-channel to be naturally de-coupled, suppressing crosstalk.

Drawing on the commercial *p*-GaN gate HEMT platform, our team has fabricated a large set of elementary CMOS logic gates. They include the inverter, which clearly shows almost all desired 'CMOS properties', such as: rail-to-rail output; adaptively varied transition thresholds, roughly following half of the supply voltage (V_{DD}); substantially suppressed static power; a very high voltage gain; and broad noise margins. More importantly, thanks to the use of a wide bandgap material, our CMOS logic inverter demonstrates satisfactory thermal stability (see Figure 2). When considering static characteristics, the presented GaN CMOS inverter is almost perfect for use.

We have also demonstrated a NAND gate, a NOR gate, and a transmission gate. All three exhibit rail-to-rail outputs and deliver correct functions at megahertz-level frequencies (see Figure 3). By demonstrating this logic gate family, we have shown that, in theory,

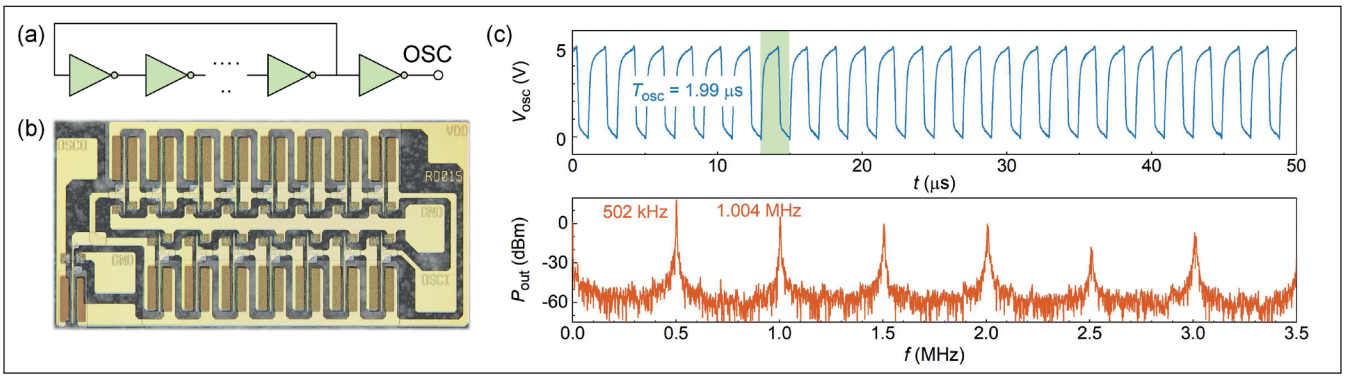


Figure 4. Demonstration of multistage GaN CMOS logic ICs. The team at HKUST uses a 15-stage ring oscillator composed of GaN CMOS logic inverters as an example, showing its oscillating waveform and power spectrum.

the essential building blocks of any logic function can be readily designed and implemented. From this foundation we have gone on to show that by cascading these blocks in certain ways to form more complex logic circuits, it is possible to construct multi-stage logic circuits, such as a monolithic 15-stage ring oscillator oscillating at a sub-megahertz frequency (see Figure 4).

Realising E-mode *p*-FETs

The key to realising GaN CMOS ICs is to produce satisfactory GaN *p*-FETs on the selected platform. With our commercial *p*-GaN gate HEMT epi-structure, we enjoy appreciable benefits, but they come with stringent restrictions. For example, to ensure a sufficiently E-mode operation of the power HEMT, the *p*-GaN must be heavily doped and sufficiently thick to prevent punch-through at a high gate bias.

It is essential to include a recess in the design. Otherwise, the *p*-GaN, which is thick and heavily doped, could never be depleted by the gate, as the electric field would become dramatically high and induce a catastrophic breakdown. Once only a moderate portion of *p*-GaN is removed – for example, by still retaining 30 nm of *p*-GaN – the channel can be turned off with a positive gate voltage. Operating in this manner, the *p*-FET works in a depletion mode.

However, a more significant modification to the design is needed to form E-mode FETs, which are mandatory for realizing ICs with truly 'CMOS-like' behaviour (especially, completely suppressed power dissipation at static states). One option is further thinning of the channel. However, while this drives the device into E-mode, this comes at the expense of a significantly reduced on-state current, because the channel for current conduction is too thin. Of greater concern, though, is the poor-quality of the etched *p*-GaN surface that introduces strong scattering to holes in the very thin *p*-channel.

By adopting a novel approach to solve this dilemma, we have maintained a reasonable on-state current density while realizing E-mode operation. This is accomplished with an architecture that combines a moderate recess with an oxygen plasma treatment to the recessed *p*-GaN surface. With this approach, we realise E-mode operation in a 'gentler' way (see

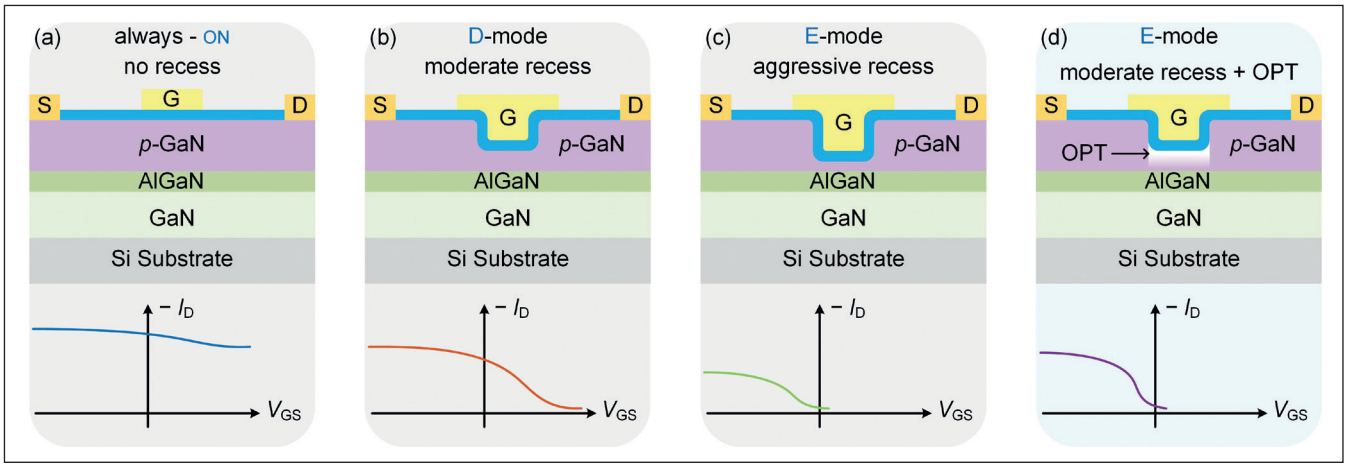
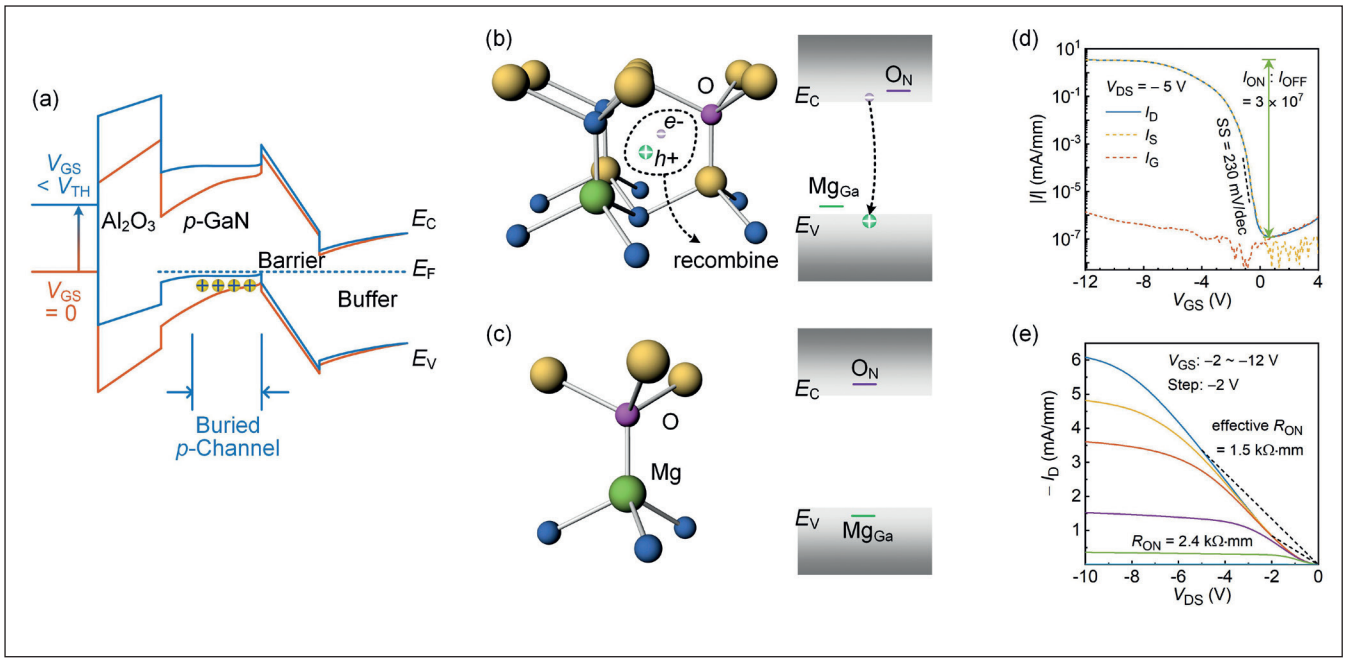


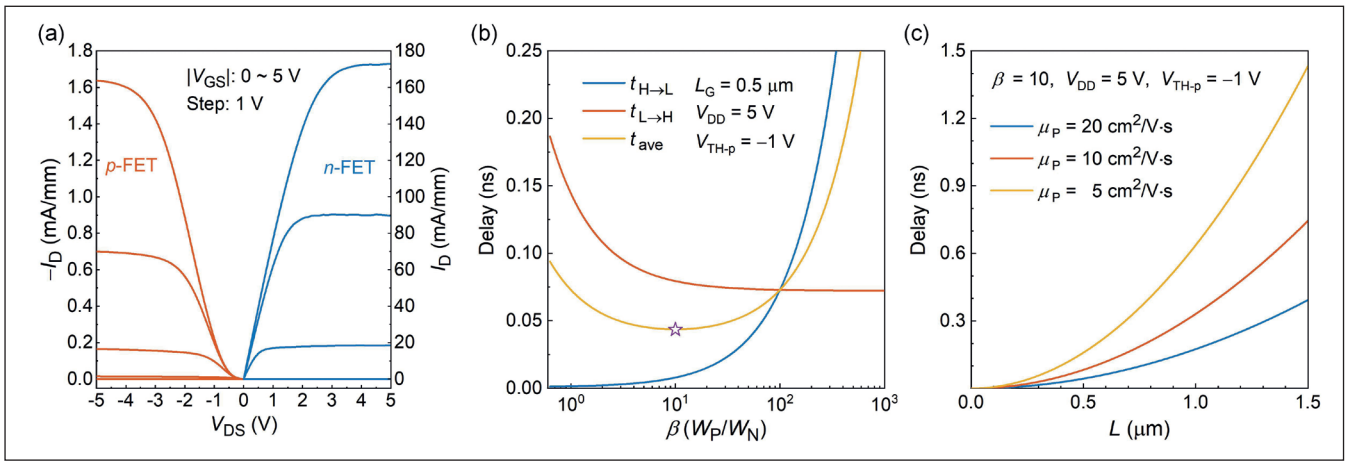
Figure 5. Approaches to realising E-mode *p*-FETs on the *p*-GaN gate HEMT platform. One option is to gradually thin down the gated region to drive the device from always-on to D-mode and then E-mode. However, the aggressive etching would significantly reduce the on-state current. The team at HKUST has taken a different approach, adopting a 'moderate gate recess + oxygen plasma treatment (OPT)' to realize E-mode operation while maintaining reasonable on-current.



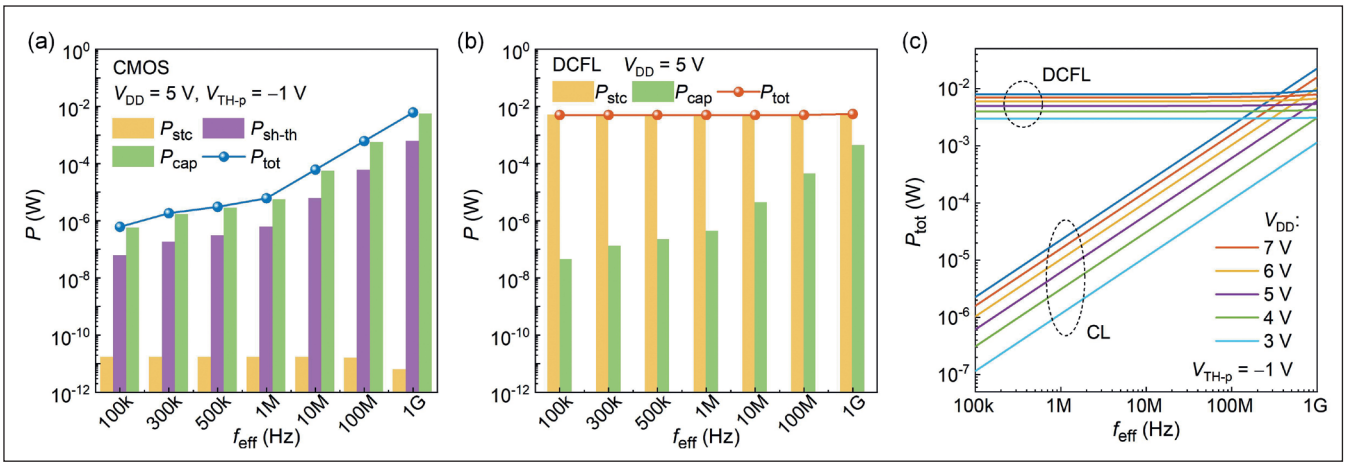
➤ Figure 6. Working principle and device performance of a buried channel GaN *p*-FET formed using an oxygen plasma treatment. (a) shows energy band diagrams of the off-state (with V_{GS} = 0 V) and the on-state (with V_{GS} < V_{TH}); (b) and (c) conceptually show possible mechanisms of why oxygen plasma treatment could convert the *p*-GaN surfaces to free-of-holes. (b) shows that oxygen acts a donor to ionize electrons to compensate holes. (c) shows that oxygen forms a Mg-O complex to directly passivate the acceptor. (d) and (e) plot transfer and output characteristics of the *p*-FET, respectively. The *p*-FET exhibits stringent E-mode operation, reasonable on-state current density, and a high on-off ratio.

Figure 5 for a comparison between our device and the conventional alternative). We use an oxygen plasma treatment to convert the top layer of retained *p*-GaN free-of-holes, thereby facilitating depletion of the *p*-channel buried below. It is possible that oxygen appearing in the *p*-GaN could act as a shallow donor, ionising electrons to recombine with holes; or it could form Mg-O complexes, passivating the magnesium acceptor directly (see Figure 6).

Operating with a negative gate bias, the holes in our E-mode FETs can be restored to the buried *p*-channel. This maintains a high hole mobility, because it is separated from the plasma-etched problematic interface between the oxide and *p*-GaN by the region treated by the oxygen plasma. Thanks to this, the buried-channel GaN *p*-FET exhibits decent electrical characteristics. The threshold voltage is stringently negative, and the on-state current density reasonable,



➤ Figure 7. The performance of the *n*-FET and *p*-FET on the *p*-GaN gate platform determine the optimization of the propagation delay at the circuit level. (a) Given the significant mobility mismatch between electrons and holes, the *n*-FET and *p*-FET exhibit a two-orders-of-magnitude difference in current density. (b) With device ratio, β, increasing, the average propagation delay firstly drops and then rises. Thus, there is an optimum value of β, which is around the inverse of the square root of the mobility ratio. (c) Reducing the gate length could reduce the delay in a quadratic way. Overall, it is achievable to realize a sub-nanosecond delay for GaN CMOS logic gates, which could satisfy the requirement of current GaN-based power conversion systems.



➤ Figure 8. By replacing the DCFL logic circuits with CMOS logic circuits, the power loss induced by logic blocks would be greatly reduced, because the static power dissipation (P_{stc}) in CMOS circuits is negligible. (a) shows that for a CMOS logic gate, dominating power dissipation components are contributed by the shoot-through current (P_{sh-th}) and the capacitance charging/discharging current (P_{cap}). Both arise at transition states and thus the total power dissipation (P_{tot}) increases with frequency. (b) shows that for a DCFL logic gate, the dominating component is P_{stc} (in this case P_{sh-th} is included in P_{stc}). (c) shows that when the switching frequency is lower than 100 MHz, CMOS circuits have significantly lower power loss than DCFL circuits.

exceeding 6 mA/mm. Overall, the on/off-state current ratio can reach seven orders of magnitude. We believe that the well-suppressed off-state leakage current could be attributed to a combination of: an insulating gate structure that guarantees a very low gate leakage; a stringent E-mode operation, which ensures a fully depleted channel; and a fluorine ion-based planar isolation technique that eradicates detrimental leaky sidewalls.

While there is still much room for further optimization, the performance delivered by this commercial platform-based *p*-FET is already impressive, and shows that developing CMOS ICs on exactly this platform is highly feasible. Building on this start, we had the motivation to construct CMOS ICs, and produce the first GaN CMOS IC family.

Performance projections

There are two aspects to evaluating the potential and the utility of GaN CMOS. One is the limit of its operating speed, given restrictions related to material properties and fabrication capabilities, and the other is the extent of energy savings associated with replacing *n*-FET-based logics with CMOS logics.

Right now it is not that practical to build circuit models for simulation-based studies, because the currently available devices have not been intensively optimized. So to gauge the potential of GaN CMOS, we have conducted an analysis using reasonable simplifications. This revealed that the operating speed of GaN CMOS will comfortably satisfy the requirement of GaN-based power systems and, as expected, that GaN CMOS is capable of significantly reducing power loss in the interested frequency regime.

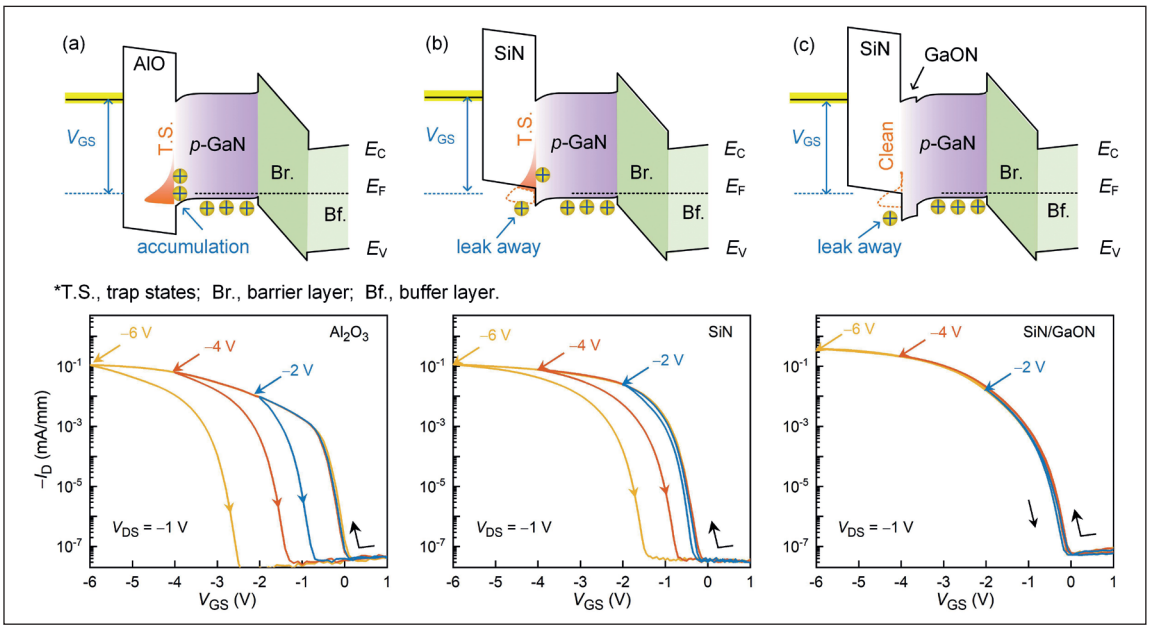
A sufficient operating speed may come as a surprise, given the massive mismatch between the mobilities of electrons and holes that leads to a two-orders-of-magnitude difference in the current density of *n*-FETs and *p*-FETs (see Figure 7 (a)). Due to this, GaN CMOS logic gates inevitably exhibit asymmetric rising and falling edges. However, it is the average delay time that determines the speed of the circuit.

At the circuit level, what matters is to optimise the device ratio between the *p*-FET and the *n*-FET. When there is a hole mobility of 20 $cm^2 V^{-1} s^{-1}$, using a gate length of 0.5 μm enables an optimum delay time that's less than 50 ps (see Figure 7 (b)) – that is sufficiently fast.

When judged in terms of energy efficiency, there is no doubt that CMOS outperforms *n*-FET-based logics, such as DCFL, which is short for direct-coupled FET logic (see Figure 8). In CMOS circuits static power dissipation is negligible, with power loss mainly coming from the shoot-through current and a charging and discharging of the capacitor during transition states. But for DCFL circuits, static power dissipation dominates. Note also that as the operating frequency increases, so does the power dissipation of GaN CMOS. However, despite these concerns, in the interested frequency regime of a power system – it has a typical operating frequency ranging from 100 kHz to 10 MHz – CMOS has the potential to dramatically reduce power loss.

Toward real applications

Based on constraints associated with material properties and fabrication, we believe that GaN CMOS will deliver a promising performance when used for power integration. To facilitate an actual application, in addition to the need for substantial downscaling and process optimization that would boost up the current density of *p*-FETs, there is another critical issue: examining and improving stability at the device and circuit levels. On this mature platform it will come as no surprise that the stability and reliability of the *n*-FET has been substantially studied and enhanced. So what's needed is to focus on the *p*-FET.

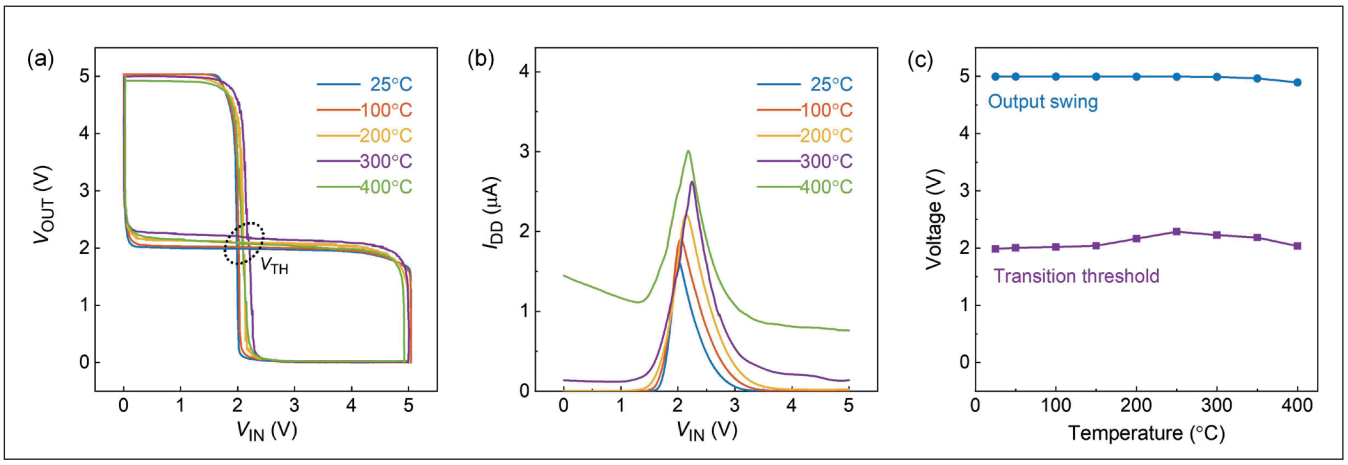


➤ Figure 9. The unoptimized gate stack results in pronounced hysteresis loops in dual-sweep transfer curves. Such an instability in the threshold voltage (V_{TH}) is very likely induced by the problematic dielectric/*p*-GaN interface. Utilizing the buried-channel structure of this *p*-FET, the team at HKUST replaced Al_2O_3 with SiN_x, which exhibits no hole barrier to GaN, and found that the V_{TH} shift induced by highly negative V_{GS} has been effectively suppressed. The V_{TH} shift induced by a small V_{GS} is eventually suppressed by converting the OPT-treated *p*-GaN surface to GaON, which eliminates high-density interface traps.

One option for mitigating the strong scattering within the *p*-FET is to use oxygen plasma treatment to separate the conducting channel from the troublesome etched interface. However, the downside is a sub-standard quality for the etched interface. Due to this weakness, when a large gate bias is applied, holes traversing the device get trapped at the interface, leading to a variation in the threshold voltage.

We tackle this problem with a two-step strategy. Our first move is to replace the Al_2O_3 gate dielectric with SiN_x. As the latter aligns with GaN in a type-II manner, it presents no barrier to holes in GaN. According to the disorder-induced-gap-states model, which can generally describe the interface between GaN and oxides, there is an appreciable trap density near the band edge of the former structure. Our switch to SiN_x introduces a hole evacuator, automatically nullifying the high-density hole traps near the valence band edge. The upshot is the prevention of successive shifts in threshold voltage at highly negative gate biases (see Figure 9 (a) and (b)).

However, this in itself is not a great solution, as there is still notable hysteresis, attributed to deeper trap states that align with the bandgap of SiN_x and are thus



➤ Figure 10. With the stability of *p*-FETs greatly enhanced, the GaN CMOS logic inverter exhibits remarkable thermal stability up to 400 °C. The transition threshold only varies slightly, whereas the rail-to-rail output is well preserved until the temperature reaches 400 °C to induce notable leakage. These results show that GaN CMOS is very promising for use in harsh environments.

not easy to evacuate. To tackle this issue, we take a second step in gate stack engineering, converting the region that we have treated with an oxygen plasma into crystalline nano-phase, gallium oxynitride (GaON). Previously, we used GaON to improve the gate reliability of a *p*-GaN gate HEMT. Through that effort, we learnt that GaON possesses a much better thermodynamic stability and a higher material quality than GaN subjected to an oxygen plasma treatment. Introducing GaON has had a profound effect, completely eliminating hysteresis (see Figure 9 (c)).

Our staggered gate stack differs from the conventional metal-insulator-semiconductor stack. In our case, the dielectric does not provide a barrier for blocking carriers when the device is in its on-state. Due to this, we need to include a buried-channel structure. When operating in the on-state, the holes in the channel are confined by the built-in potential in *p*-GaN, enabling the gate leakage to remain at a very low level if the gate bias does not exceed -6 V. Yet, the SiN_x is indispensable. It effectively blocks the gate leakage at the off-state under a positive gate bias; and it serves as a voltage divider, expanding the allowed input swing to fit the *p*-GaN gate HEMT platform, where typically 5-6 V are usually used to drive *n*-FETs.

By turning to our SiN_x/GaON gate structure, we are able to extend the operating temperature of GaN CMOS ICs to 400 °C (see Figure 10). With a 5 V voltage supply, the logic transition threshold fluctuates within only 0.4 V. At this supply voltage, the rail-to-rail output swing is well maintained, degrading only slightly at 400 °C, due to an increase in leakage that could be further suppressed with process optimization. These results underscore the superiority of GaN as a wide-bandgap semiconductor, indicating possible applications of GaN in extreme environments.

We have made major strides with GaN CMOS, demonstrating the first family of ICs and also projecting performance in power integration and substantially improving stability. Our next steps, hopefully taken in collaboration with industry partners, are to undertake device downscaling, silicon-compatible process development and yield/uniformity improvement. There is no doubt that GaN CMOS is marching toward practical applications.

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Refining the quantum dot laser

Increasing the density of dots by at least an order of magnitude promises faster lasers with a lower threshold current

A TEAM FROM JAPAN claims to have broken new ground by cranking up the density of quantum dots in lasers that could serve in optical networks and biomedical measurement systems.

By increasing the density of dots by at least an order of magnitude, the engineers at The University of Electro-Communications in Tokyo have slashed the number of active layers in the device. According to team spokesman Koichi Yamaguchi, while conventional quantum-dot lasers have around ten active layers, their devices can have just one or two of them.

Yamaguchi revealed that one of the merits of trimming the thickness of the active region is enhanced carrier recombination.

"In addition, the in-plane ultra-high-density quantum-dot layer is expected to not only reduce the threshold current, but increase the carrier incorporation rate into the quantum-dots and enhance high-speed modulation."

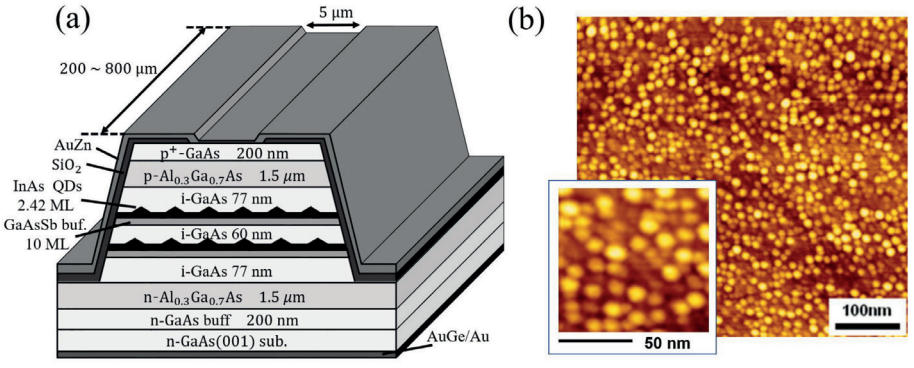
Fabrication of the team's lasers began by loading an n^+ GaAs (001) substrate into an MBE reactor and depositing an epitaxial stack consisting of a 200 nm-thick *n*-type GaAs buffer layer, a 1.5 μm-thick *n*-type $Al_{0.3}Ga_{0.7}As$ bottom cladding layer and a 220 nm-thick undoped GaAs-based waveguide. The latter features a pair of layers containing an ultra-high density of in-plane InAs quantum dots, deposited at 470 °C and formed on a GaAsSb buffer layer using the Stranski-Krastanov growth mode.

X-ray diffraction measurements of this heterostructure indicated that the antinomy content in the buffer is between 12 and 14 percent. According to atomic force microscopy, the density of the dots is 5 x 10^{11} cm^{-2}. The team attributes an antinomy surfactant effect to suppressed coalescence of the dots, which are typically 1.4 nm high and 14 nm wide.

To complete the fabrication of the lasers, the engineers added a 1.5 μm-thick *p*-type $Al_{0.3}Ga_{0.7}As$ top cladding layer and a 200 nm-thick p^+ GaAs contact layer. Subsequent photolithography and wet-etching created a 20 μm-wide ridge-waveguide structure. Magnetron sputtering of a 200 nm-thick SiO_2 film followed, prior to defining 5 μm-wide or 7 μm-wide windows and then adding a pair of electrodes – one to the substrate and another to the p^+ GaAs contact layer. Finally, the team cleaved the patterned substrate into laser chips to create cavity lengths ranging from 200 μm to 800 μm.

These lasers, which could deliver an even better performance by forming high-reflectivity coatings on their facets, have a threshold current density of 1-10 kA cm^{-2}. While continuous-wave lasing at room-temperature occurs at just 1021 nm, emission could be shifted to the 1.2 μm to 1.3 μm range by adding a GaAsSb capping layer.

The researchers claim that when their lasers operate at room temperature, there is a strong coupling of the wavefunction between neighbouring quantum dots. This gives rise to a miniband in the conduction band that results in a characteristic temperature that the team describes as "not so high".



➤ Ridge waveguide lasers produced by the team from The University of Electro-Communications, Japan, have just two quantum dot layers (a), thanks to the high density of dots, seen in atomic force microscopy images (b).

Based on an analysis of the dependence of the cavity length on threshold current density, Yamaguchi and co-workers have concluded that their devices have a comparable crystal quality to other quantum-dot lasers. What's more, they have said that by increasing the length and reflectivity of the cavity, their lasers realise a lower threshold current density.

By comparing the threshold current of the team's laser with another design, the researchers estimate that just 41 percent of the dots in the latest design contributed to lasing. They attribute this weakness to inhomogeneous broadening.

"The uniformity of the in-plane ultra-high-density quantum dots is still insufficient," argued Yamaguchi. "So, it is necessary to promote high uniformity in future."

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Realising a high UV efficiency on sapphire

AlN templates with a face-to-face anneal enhance deep-UV LED efficiency

THE INTERNAL QUANTUM EFFICIENCY of active regions that emit in the deep-UV can now be almost as high on AlN templates as they are on native bulk substrates, claims a team from Japan.

By minimising light-quenching dislocations with a templates formed with sputtering and annealing, the team – a partnership between Yamaguchi University, the National Institute of Technology and Mie University – has fabricated multi-quantum-well heterostructures with an internal quantum efficiency of 90 percent.

Spokesman for these researchers, Yoichi Yamada from Yamaguchi University, told *Compound Semiconductor* that the collaboration expected a very high quantum efficiency from its samples because calculations predicted a value of more than 80 percent for a dislocation density of 2 x 10^8 cm^{-2}. "Our study has shown that [efficiency] experimentally for the first time."

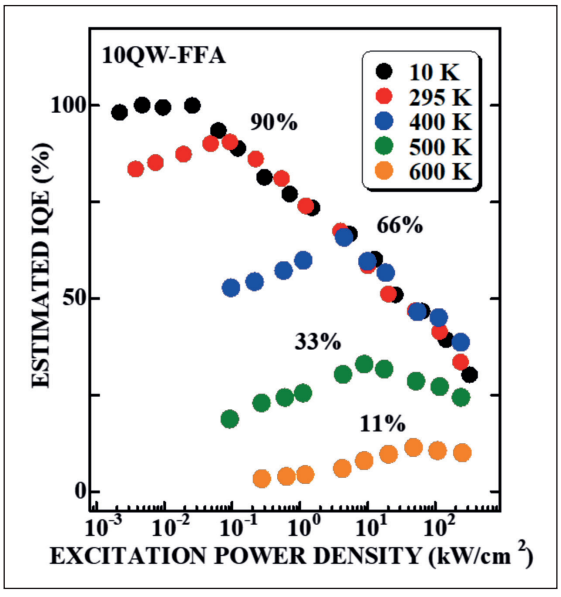
This success could underpin an increase in the bang-per-buck of commercial deep-UV LEDs. Those built on a bulk AlN foundation have an excellent internal quantum efficiency, but are high in cost, due to the expense of the substrate.

As well as cutting costs, using a sapphire substrates for this class of emitter aids process development and improves reliability, as demonstrated by the progress of the blue-emitting LED.

"In addition, the refractive index of sapphire is close to that of silicon dioxide, making it advantageous in light-extraction structures", remarked Yamada.

He and his co-workers have fabricated light-emitting active regions on templates that are formed by sputter-depositing AlN films on *c*-plane sapphire substrates, which are off-cut by 0.2 ° toward the *m*-axis. To improve material quality prior to MOCVD growth, the researchers put faces of pairs of AlN templates together before annealing them under nitrogen, typically for several hours. According to X-ray diffraction measurements, this process reduced the screw and edge components of dislocations in the AlN film to just 1.2 x 10^6 cm^{-2} and 3.3 x 10^8 cm^{-2}, respectively.

On this foundation the team added an active region, formed from ten $Al_{0.50}Ga_{0.50}N$ quantum wells with a thickness of 2 nm, separated by 6 nm-thick $Al_{0.75}Ga_{0.25}N$ barriers. Doping the wells and barriers with silicon decreased the density of non-radiative recombination centres consisting of cation vacancies. To provide a benchmark for evaluating that light-emitting structure, the team replicated the active region on an MOCVD-grown AlN template that had screw and edge dislocation densities of 2.9 x 10^7 cm^{-2} and 9.1 x 10^8 cm^{-2}, respectively.



➤ AlN templates formed with a face-to-face anneal provide a foundation for deep-UV active regions that realise high efficiencies at elevated temperatures.

Internal quantum efficiencies were deduced by making photoluminescence measurements at various temperatures, and assuming that this efficiency is 100 percent at absolute zero. This methodology determined a value of 90 percent for the room-temperature internal quantum efficiency of the sample with a foundation formed by sputtering, compared with just 58 percent for the control.

By considering the internal quantum efficiency at a range of excitation densities, the team uncovered an efficiency plateau at 10 K in the sample containing a sputtered template. This feature revealed that at low excitation densities, non-radiative recombination centres are either fully saturated or completely frozen. In comparison, at that same temperature the non-radiative recombination centres in the control sample are active. Based on this finding, the researchers have concluded that using of face-to-face-annealed AlN templates decreases the density of non-radiative recombination centres in the active region.

By cranking up the temperature of the sample, Yamada and colleagues determined that the internal quantum efficiency is as high as 66 percent at 400 K and 33 percent at 500 K (see Figure). They attribute such high values to insignificant thermal activation of non-radiative recombination centres below 400 K.

The team is now planning to fabricate and design LED light extraction structures, and to optimize quantum well structures.

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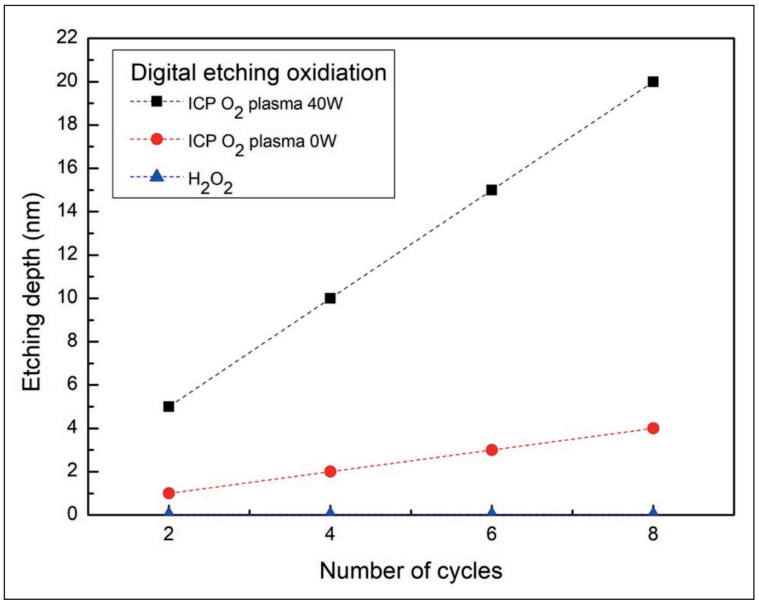
Producing normally-off RF HEMTs

Plasma treatment and wet etching yields RF GaN HEMTs

A TEAM from National Yang Ming Chiao University, Taiwan, claims to have produced the first normally-off GaN HEMTs using a digital etching technique.

According to spokesman for the team, Ping-Yu Tsai, RF devices benefit from normally-off operation because they can then be driven with just a single positive voltage. "This can reduce the complexity of IC design and save power consumption of the system modules, since the device does not consume energy when it is not operating," added Tsai.

There are several reports of using a digital etch to recess the gate of power HEMTs, which have larger dimensions. Tsia and co-workers believe that they are breaking new ground by being the first team to apply this technique to RF HEMTs.



➤ Digital etching is linear, with a high RF power speeding the process.

"We used this method to control the gate recess for RF HEMTs with a small gate length," explained Tsai. By providing good control of the etch depth, the team demonstrated E-mode devices and RF characteristics.

Realising high-quality gate etching is not easy, demanding precise control of the etching depth while ensuring a low surface damage and good uniformity. Gate etching tends to involve the use of a plasma formed from either chlorine gas or BCl_3, but both options promote damage on the surface of the gate, and ultimately impair the device's performance and reliability.

To improve gate etching quality, Tsai and co-workers turned to a two-step digital etch. To optimise that approach prior to device production, they began by studying the impact of surface chemistry and etch rate on an AlGaN/GaN heterostructure comprising a buffer layer, an un-doped GaN channel, a 1 nm-thick AlN spacer and a 22 nm-thick $Al_{0.22}Ga_{0.78}N$ barrier layer.

After adding a SiN hard mask to this heterostructure and patterning it by photolithography and fluorine-based inductively coupled plasma etching, the team oxidized the wafer with two different techniques: exposure to hydrogen peroxide for 5 minutes; and oxidation of the wafer in an oxygen plasma, using an inductively coupled plasma system operating at a range of RF powers. Both approaches were followed with an identical second step: a 90 s digital etch in diluted HCl to remove the oxide products.

Atomic force microscopy measurements revealed good linearity in the etch depth per cycle (see Figure). Using RF powers of 40 W and 0 W, the average etch rates with the oxygen plasma treatment were 2.5 nm per cycle and 0.5 nm per cycle, respectively. The process involving hydrogen peroxide produced an etch depth per cycle close to 0 nm. Based on these findings, further studies were restricted to the use of oxygen plasma treatments.

X-ray photoelectron spectroscopy uncovered the presence of a strong peak associated with oxygen in samples subjected to plasma treatment. This peak's strength plummeted after dipping the sample in HCl, demonstrating that this step provided good oxide removal.

Atomic force microscopy on 1 μm by 1 μm areas revealed that after three digital etch cycles, the AlGaN surface had a root-mean-square roughness of 0.10 nm and 0.09 nm for 40 W and 0 W treatments, respectively. Etching with a chlorine plasma increased the rougness to typically 0.49 nm.

The team produced HEMTs with a 110 nm gate length using three etching processes: one cycle, 0 W bias; six cycles, 40 W bias; and eight cycles, 40 W bias. Measurements with a 5 V drain bias showed that increasing the number of cycles, and thus the amount of material etched, led to a decrease in drain current and transconductance, along with a shift in the threshold voltage – it increased from -2.7 V to 0 V and then 0.4 V. The positive threshold voltage, crucial for normally off operation, came at the expense of drain current and transconductance, due to the creation of a very thin AlGaN barrier layer that almost ensured depletion of the two-dimensional electron gas.

Tsai said that the team might now refine its technique for use on larger wafers, so that it could be applied to high-volume production of RF devices with good uniformity.

REFERENCE
➤ P. -Y. Tsai *et al*. Appl. Phys. Express **14** 126501 (2021)

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