COMPOUND SEMICONDUCTOR
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

G10-AsP brings microLEDs to high-volume production

VOLUME 29 ISSUE I 2023
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
COMPOUNDSEMICONDUCTOR.NET

INSIDE

GALLIUM NITRIDE POWERS AHEAD

Researchers at the International Electron Devices Meeting unveil record-breaking devices featuring superior architectures

VIABLE DIAMOND SUBSTRATES

Diamond is set to serve in more applications, thanks to a heteroepitaxial growth process for fabricating 2-inch substrates

OPPORTUNITIES FOR THE VCSEL

Mirrors that incorporate porous layers of GaN will drive the commercialisation of blue and green VCSELs

Global mega trends require best performance III-V materials

AIX 2800G4-TM

- 3D sensing
- Augmented reality
- Autonomous driving
- Cloud computing
- Internet of things
- Next generation displays

Discover the MOCVD tool of record for AsP-based applications

Made in Germany

AIXTRON

info@aixtron.com
www.aixtron.com

VIEWPOINT

By Dr Richard Stevenson, Editor

GaN's formidable reach

GaN, WITHOUT DOUBT the most important material in our industry, is continuing to extend its reach. Having cemented its commercial prowess in the LED industry, where it is netting billions of dollars every year from backlighting our screens and illuminating our surroundings, sales are now surging from new products in the optoelectronic and electronic domain – a trend that is sure to continue throughout this decade.

There's now renewed interest in GaN lasers. They are certainly not new, having been invented back in 1995, when this magazine made its debut. But high-volume, commercial production of the VCSEL – that much-vaunted class of laser, cherished for its circular beam profile, efficiency, fast switching speed and on-wafer testing – has remained elusive, due to difficulties associated with the growth of the mirrors.

Now that problem may be consigned to the history books, thanks to the efforts of a little-know start up from Wilmington, DE. Going by the name Ganvix, this trailblazer, which is partnering with the Industrial Technology Research Institute (ITRI) in Taiwan, is producing VCSELs with alternating layers of porous and non-porous GaN (see p. 16 for details). Sampling these VCSELs, sporting output powers of around 5 mW, should soon be underway.

While it may take a few more years before GaN VCSELs are netting substantial sales, 2023 will mark the inflection point for GaN power electronics, according to GaN Systems.

In our recent interview with company CEO Jim Witham (see p. 16), he argued that sales of GaN power devices will soon smash through

the billion-dollar barrier, driven by increased penetration in several sectors. GaN is already renowned as the go-to material for fast chargers for mobile devices, and it is tipped to see greater deployment in audio amplifiers, power supplies for data centres, inverters for renewables, and in chargers and power trains in electric vehicles.

Although GaN power devices have made great strides over the last few years, there is still much more to come, according to those presenting at the 68th IEEE Electron Devices Meeting, held in San Francisco last December. At that gathering Intel championed its progress in scaled GaN HEMTs with field plates; Transphorm showcased the capabilities of 1200 V GaN switches produced on sapphire substrates; and academics unveiled devices with a hybrid gate that bolster threshold voltage stability, and the world's first GaN superjunction device (see p. 22 for details).

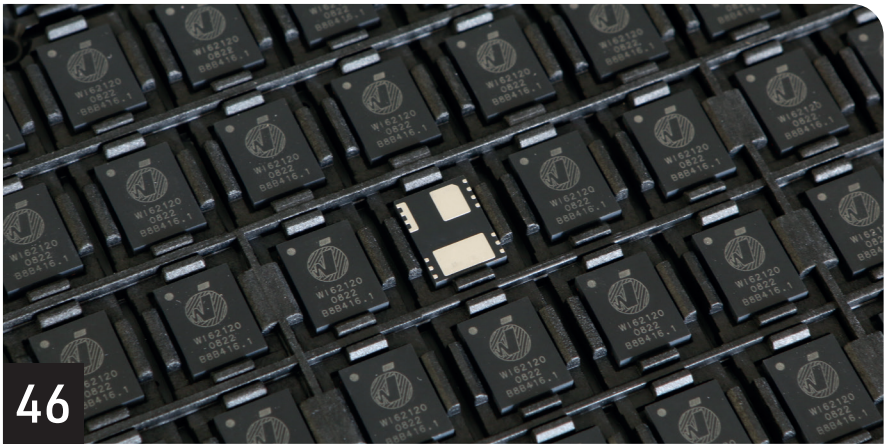
Particularly for the breakthroughs at universities, it could be some time before revenues result. But they will, ensuring increasing diversity of GaN devices, along with their reach into ever more applications.

Free weekly e-news roundup go to: compoundsemiconductor.net

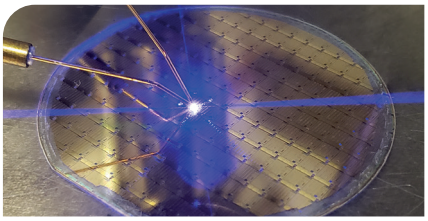
CONTENTS

VOL. 29 ISSUE I 2023

COMPOUND SEMICONDUCTOR
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

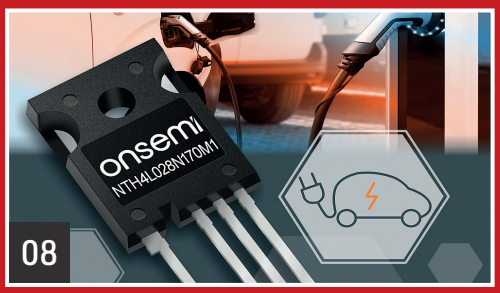


NEWS ANALYSIS



RESEARCH REVIEW

NEWS



Editor Richard Stevenson
richardstevenson@angelbc.com
+44 (0)1291 629640

News Editor Christine Evans-Pughe
chrise-p@dircon.co.uk

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Director of Logistics Sharon Cowley
sharon.cowley@angelbc.com
+44 (0)1923 690200

Sales Executive
Jacob Caulfield
jacob.caulfield@angelbc.com
+44 (0)2476 718979

Circulation
Scott Adams
scott.adams@angelbc.com

Publisher Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

USA Representatives
Brun Media
Janice Jenkins
jjenkins@brunmedia.com
+1 724-929-3550
Tom Brun
tbrun@brunmedia.com
+1 724 539-2404

Chief Executive Officer
Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

Chief Technical Officer
Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Directors
Jackie Cannon, Sharon Cowley

Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

Silanna UV introduces TO-packaged UVC LEDs

High-performance, hermetically sealed packages ideal for sensing applications

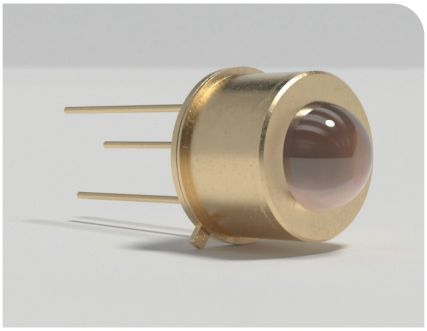
AUSTRALIAN UV-LED company Silanna UV has released two new products in its SF1 235 nm and SN3 255 nm series of UVC LEDs.

The new UVC LEDs, the SF1-3T9B5L1 and the SN3-5T9B5L1, feature the TO-can package format, which consists of a header and a cap that together form a hermetically sealed package. This innovative design protects sensitive semiconductor components within the package. The header supplies power to the encapsulated components, while the cap enables the transmission of optical signals. The strong weld between the cap and the header provides hermetic protection to the die, and the ball lens offers a narrow viewing angle for the high irradiance required in most sensing applications.

The industrial standard TO-39 footprint uses a steel header with a gold coating. These devices have ESD protection and contain no mercury. The TO-39 package has an 18° viewing angle, enhancing radiant intensity and measurement resolution.

The SF1-3T9B5L1 is a far-UVC emitting device with a peak wavelength of 235 nm, making it effective for water quality detection of nitrate (NO_3) and nitrite (NO_2), gas detection of carbon dioxide (CO_2), and liquid chromatography.

The SN3-5T9B5L1 is a powerful deep-UVC LED with a peak wavelength of 255 nm, making it effective for water quality detection of chemical oxygen demand and total organic carbon, as well as gas detection for ozone and medical analysers. It has a high optical output power, making it suitable for a range of applications, including chemical and biological analysis, water



quality monitoring, gas sensing, and liquid chromatography.

Both the SF1-3T9B5L1 and SN3-5T9B5L1 offer excellent stability and performance, with less than 0.5 percent drift and fluctuation in a steady state.

They are also compatible with off-the-shelf optical systems, making them a convenient and reliable choice for sensing applications.

Wolfspeed SiC to power Mercedes Benz EVs

WOLFSPEED will be supplying SiC devices to power future Mercedes-Benz electric vehicle (EV) platforms, to enable greater efficiency in the powertrain.

“Coming from a long-term technical collaboration history between our companies, we have now chosen Wolfspeed as one of our key partners for future SiC devices, thus securing preferred long-term supply, technology and quality of this decisive semiconductor component for our electrification offensive,” said Gunnar Güthenke, head of procurement and supplier quality for Mercedes-Benz.

“We are pleased to be supporting Mercedes-Benz, an organisation with a long, successful history of providing world-class performance and luxury vehicles, as they introduce next-generation EVs to the market with highly efficient power systems,” said Gregg Lowe, CEO of Wolfspeed.

The SiC power devices for Mercedes-Benz will be produced at Wolfspeed’s facilities in Durham, North Carolina and its new 200 mm Mohawk Valley Fab in Marcy, New York. This Mohawk Valley Fab is the world’s largest SiC fabrication facility.

In 2022 Wolfspeed announced it was beginning construction on a new SiC materials facility in North Carolina, which will expand its SiC capacity by more than ten times.

First monolithic microLED display using organic TFTs

SmartKem uses semiconductor inks to process transistors directly on top of GaN LEDs

SMARTKEM, a company based in Manchester, UK, has announced the world's first monolithic microLED display using organic thin-film transistors (OTFTs). It says this new method of processing a thin-film transistor backplane on top of GaN LEDs has the potential to accelerate the commercialisation of microLED displays.

Consumer electronics companies are developing microLED displays since they promise higher brightness, lower power consumption and longer lifetime. This is particularly important for portable powered displays, such as smartwatches and AR/VR displays, which cannot accommodate large batteries.

Today's existing VR & AR headsets use LCD and OLED displays, lacking brightness, resolution, power efficiency and lifetime.

Existing efforts at establishing microLED manufacturing use physical transfer of LEDs from the wafer upon which they are manufactured to the TFT display backplane, where they must be laser welded to the contact pad of the transistor to make an electrical connection. Since, for high-resolution displays, millions of tiny LEDs need to be transferred from one place to another, then the potential for placement error is large. If a 99.9 percent placement yield is achieved, then a full HD colour display will have over 6,000 faulty sub-pixel LEDs that would need to be identified, removed, and re-attached.

Once the 6,000 faulty LEDs have been replaced, a 99.9 percent yield will still mean six of these will be faulty, so the job of manufacturing a perfect display is not yet finished. It is the process of seeking out the faults and then replacing them one by one which is slowing down commercialisation of this new type of display. SmartKem's patented core chemistry allows its semiconductor inks to be processed at the low temperature of 80°C. With this lower temperature, one can process transistors directly on top of the microLEDs. This eliminates the mass transfer and laser welding processes, and the fabrication of OTFTs can use existing low-cost manufacturing tools currently used for LCD backplane manufacturing.

This approach cannot be carried out with other types of thin-film transistors as they are processed at the much higher temperature of 300°C, which damages the microLEDs, and is why you need to make them separately and then laboriously join them together one by one.

Onsemi announces EliteSiC family

New 1700 V EliteSiC devices provide reliable, high-efficiency operation in energy infrastructure and industrial drive applications

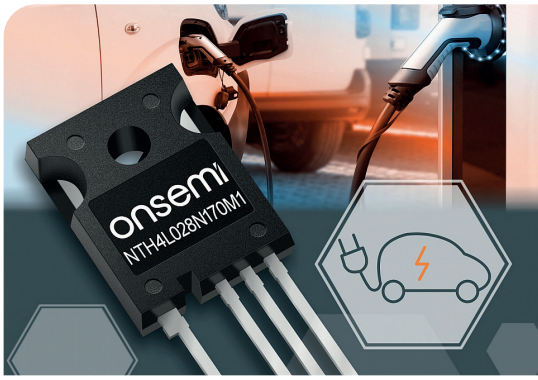
ONSEMI has introduced EliteSiC as the name of its SiC family. It exhibited three new members of the family – the 1700 V EliteSiC MOSFET and two 1700 V avalanche-rated EliteSiC Schottky diodes – at the Consumer Electronics Show (CES) in Las Vegas.

With the 1700 V EliteSiC MOSFET (NTH4L028N170M1), Onsemi delivers higher breakdown-voltage SiC solutions, required for high-power industrial applications. The two 1700 V avalanche-rated EliteSiC Schottky diodes (NDSH25170A, NDSH10170A) allow designers to achieve stable high-voltage operation at elevated temperatures while offering high efficiency enabled by SiC.

"By providing best-in-class efficiency with reduced power losses, the new 1700 V EliteSiC devices reinforce the high standards of superior performance and quality for products in our EliteSiC family, as well as further expand the depth and breadth of Onsemi's EliteSiC," said Simon Keeton, executive vice president and general manager, Power Solutions Group, Onsemi. "Together with our end-to-end SiC manufacturing capabilities, Onsemi offers the technology and supply assurance to meet the needs of industrial energy infrastructure and industrial drive providers."

Renewable energy applications are consistently moving to higher voltages with solar systems from 1100 V to 1500 V DC Buses. To support this change, customers require MOSFETs with a higher breakdown voltage. The new 1700 V EliteSiC MOSFET offers a maximum V_{gs} range of -15 V/25 V, making it suitable for fast switching applications where gate voltages are increasing to -10 V, delivering increased system reliability.

At a test condition of 1200 V at 40 A, the 1700 V EliteSiC MOSFET achieves a gate charge of 200 nC – which is said to be market-leading compared to equivalent competitive devices that are



closer to 300 nC. A low gate charge is critical to achieving high efficiency in fast switching, high-power renewable energy applications.

With a breakdown voltage rating of 1700 V, the EliteSiC Schottky diode devices offer improved margin between the maximum reverse voltage and the peak repetitive reverse voltage of the diode. The new devices also provide excellent reverse leakage performance, with a maximum reverse current of just 40 µA at 25°C and 100 µA at 175°C.

Infineon and Resonac expand SiC cooperation

INFINEON TECHNOLOGIES has signed a new multi-year-supply and cooperation agreement with Resonac Corporation (formerly Showa Denko), complementing and expanding the announcement of 2021. According to the agreement, Resonac will supply Infineon with SiC materials for the production of SiC semiconductors, covering a double-digit share of the forecasted demand for the next decade.

While the initial phase focuses on 6-inch SiC material supply, Resonac will also support Infineon's transition to 8-inch wafer-diameter during the later years of the agreement. As part of the cooperation, Infineon will provide Resonac with intellectual property relating to SiC material technologies.

"The demand for SiC is growing rapidly and we are preparing for this development with a significant expansion of our manufacturing capacities," said Angelique van der Burg, chief procurement officer at Infineon.

"We are pleased to deepen our collaboration with Resonac and strengthen the partnership between our two companies."

"The business opportunities in the area of renewable energy generation and storage, electromobility and infrastructure are enormous for the years to come. Infineon is doubling down on its investments into SiC technology and product portfolio, to proliferate the most

comprehensive product offering to its customers. We are very happy that our partnership with Resonac will strongly support our market-leading position," said Peter Wawer (pictured above), president of Infineon's Industrial Power Control division.

ClassOne TECHNOLOGY

All Systems. GO

Your advanced microelectronics make the world go.

Our advanced manufacturing systems get you there.

SOLSTICE®

Advanced Single-wafer Electroplating and Surface Preparation

OUR FLAGSHIP SOLSTICE PLATFORM delivers best-in-class performance at an unmatched price/performance ratio. Our highly flexible platform can be customized for a comprehensive range of semiconductor packaging applications for advanced device manufacturing including VCSELs, microLEDs, RF and power semiconductors.

GO NOW, GO SOLSTICE

- Advanced performance with maximum throughput and wafer uniformity
- Flexible, scalable platform for multiple applications on a single, compact system
- Elegant and simple design, easier to use, operate and maintain
- Engineered for reliability and uptime
- Unparalleled cost-efficiency and ROI

YOU SEEK WORLD-CLASS MANUFACTURING EQUIPMENT TO MAKE YOUR FAB GO. WE CREATED SOLSTICE TO MAKE YOUR DECISION EASY.

REACH OUT - WE'RE READY.

TEL: +1 406 407 7814
info@ClassOne.com

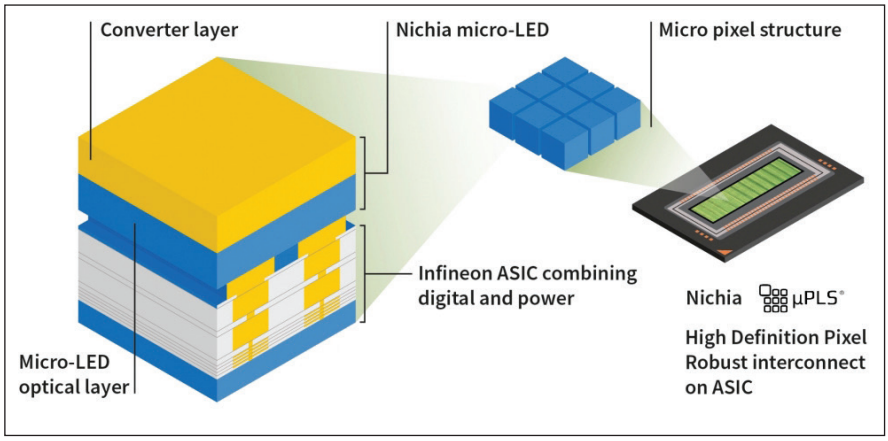
Nichia and Infineon launch industry's first HD microLED matrix solution

Companies to premier first fully integrated microLED light engine for HD adaptive driving beam applications

THREE YEARS AGO Nichia and Infineon announced the joint development of a high-definition (HD) light engine with more than 16,000 microLEDs for headlight applications. Now, both companies are launching the industry's first fully integrated microLED light engine for HD adaptive driving beam applications. The microLED matrix solution will be seen in a German premium vehicle in 2023.

"The new 16,384 pixel micro-pixelated light solution is our latest addition to Nichia's portfolio of high-class automotive lighting solutions," said Yusuke Yamazaki, head of sales and marketing automotive, Nichia Europe GmbH. "It combines high-definition resolution with industry's highest light output. This solution enables a new automotive lighting experience by providing four-times wider field-of-view with significantly higher light output than any other current micro-mirror based HD matrix-light solution. For this reason, the advanced HD light can warn drivers of hazards by highlighting people or objects on or by the side of the road. It can also project markings on the road to guide the driver through a construction site or intersection. In addition, functions such as the glare-free high beam or bending light work more precisely and smoothly compared to current adaptive driving beam solutions. This takes the driver's road safety and driving comfort to a new level."

Andreas Doll, Infineon's SVP and general manager of the business Unit Body Power of Infineon's Automotive Division commented: "The µPLS is industry's first fully integrated matrix LED driver capable of driving 16,384 LEDs, combining all required microLED driver circuitry with extensive diagnostics and high-speed video and control interfaces."



"Our innovative µPLS is much more energy efficient than current HD matrix lighting solutions, contributing to saving global CO_2 emissions and extending the range of electric driven vehicles. Furthermore, we enable the vision of our customers to deploy fully digital light on the road, saving them overall system cost at a very small form factor at the size of a single semiconductor chip."

The new HD light engine uses Nichia's microLED technology and an integrated LED driver IC from Infineon that can drive all 16,384 microLEDs individually using pulse-width modulation (PWM) control. Additionally, the driver IC monitors each microLED separately and provides on-chip temperature monitoring, allowing for optimal thermal control. Integrated video interfaces enable high-speed transmission of the video signal from the light pattern generator unit.

Unlike current HD matrix solutions, Infineon's driver IC only activates the LEDs that are actually needed for a light pattern. This dramatically increases the energy efficiency of the µPLS light engine at much smaller form factor compared with micro-mirror-based HD matrix solutions in the market.

This allows for smaller and slimmer headlamp designs in the future. In addition, the new HD light engine enables adjustments that can be digitally programmed at the factory or activated by the vehicle manufacturer or driver on demand. For example, the different requirements of left- and right-handed drivers can be considered, significantly increasing user-friendliness.

With all these features, the new HD light is said to significantly reduce design and production complexity for vehicle manufacturers.

The new HD light engine enables adjustments that can be digitally programmed at the factory or activated by the vehicle manufacturer or driver on demand

UK start-up secures £4 million for antimony-based lidar chip

New architecture is 10 times more sensitive and with 50 percent more range compared to equivalent sensors

PHLUX TECHNOLOGY, a University of Sheffield spin-out based in one of the world's leading centres for III-V semiconductor research, has secured £4 million in seed funding to bring its antimony-based infrared sensors to the mass market.

The round was led by Octopus Ventures and included Northern Gritstone, the Foresight Williams Technology Funds and the Innovation Fund, as well as receiving funding from Innovate UK.

Phlux' patented approach to infrared sensors is said to dramatically improve performance in lidar. The new architecture is 10 ten times more sensitive and with 50 percent more range compared to equivalent sensors, reducing the cost of manufacture of lidar sensors and opening up mass market adoption.

Phlux Technology was founded by Ben White, CEO, Jo Shien Ng and Chee Hing Tan, who met at Sheffield University where they researched novel semiconductor materials and devices for infrared detection.

Unlike Moore's Law for semiconductors, which predicts performance improvement every 18 months, infrared sensors (InGaAs) have reached a plateau in terms of performance.

Having studied alternatives for more than 10 years, the founders identified antimony as a material capable of revolutionising the lidar sensor market. It opens access to the 1550 nm infrared space, offering higher sensitivity and capacity as it operates in the 'eye safe' region of the electromagnetic spectrum.

Well over 1,000 times more photons can safely be launched compared to silicon-compatible emitters, enabling antimony-based sensors to see further, with greater pixel density at a mass market cost.

"Our ambition is to become the Nvidia of the sensor market, starting off with delivering the world's first lidar sensor chip using antimony," said Ben White, CEO and co-founder. "Industry will never achieve full autonomy with lidar if it relies on silicon-based sensors, so our approach will reshape the sensor market for robotics and self-driving machines."

CrayoNano UVC LED lasts over 10,000 hours

Company releases preliminary results of CrayoLED CLH-N3S lifetime results

CRAYONANO has released the preliminary results of the CrayoLED CLH-N3S H-Series UVC LED room-temperature operating-life (RTOL) test conducted by an independent, accredited third-party testing and qualification lab.

The lifetime testing aims to demonstrate the quality and reliability of the CrayoLED and generate data to predict the LED's lifetime until it reaches 70 percent of its original power output, based on the TM-21 modelling.

The RTOL testing follows the EIAJ-ED-4701/100(101) standard, an industry accepted test method to measure output power maintenance of LED packages.

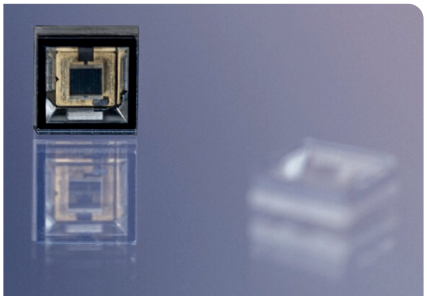
The CrayoLED CLH-N3S LEDs are tested at the standard forward driving current, 350 mA per LED, under continuous operation for a minimum of 6,000 hours.

The test condition and set-up consist of the CLH-N3S LED mounted on an aluminium metal core printed circuit board, attached to an aluminium heatsink for thermal management, and running inside a temperature-controlled chamber.

CrayoNano has demonstrated that after 3,000 hours (approximately 4 months), the CLH-N3S UVC LED at 350 mA maintained an average performance output of 79.3 percent. This preliminary test data is extrapolated, based on the TM-21 model, and predicts an estimated lifetime of more than 10,000 hours. It is claimed that this unprecedented lifetime in a small footprint, high-power-density UVC LED will enable solutions in challenging applications requiring better performance and where maintenance is difficult— reducing customers' total cost of ownership.

"We have taken great care in creating the CrayoLED – optimising our LED package design and assembly technology using higher quality materials, combined with our understanding of the thermal efficiencies and performance of LEDs," says chief product officer, Alejandro Basauri.

The CrayoLED is optimised for disinfection with a typical peak



wavelength of 275 nm. Its small package footprint (3.5 mm x 3.5 mm) and high-power performance (typical 80 mW optical power at 350 mA) are said to easily integrate into systems for residential, commercial, and industrial applications.

CrayoNano will continue testing until the results have reached 6,000 hours to complete the TM-21 testing criteria. Alejandro Basauri continues, "We are immensely proud of the results. Quality and reliability are key factors for solutions towards automated disinfection solutions."

CrayoLED H-series (CLH-N3S) is available in both sample quantities and in stock for volume production.

Nexperia engages US law firm to fight wafer fab decision

NEXPERIA has engaged the US law firm Akin Gump to fight the UK government's decision that it should sell at least 86 percent of the Newport Wafer fab.

Nexperia, which is owned by the Chinese company Wingtech, was instructed in November 2022 to sell its majority stake due to national security risks.

The Secretary of State's order said the risks relate to technology and know-how that could result from a potential reintroduction of compound semiconductor activities at the Newport site, and the potential for those activities to undermine the UK's own capabilities. In addition, the location of the site could facilitate access to technological expertise and know-how in the South Wales Compound Semiconductor Cluster, and the links between the site and the Cluster may prevent the Cluster being engaged in future projects relevant to national security.

The Welsh Government says its immediate priority is to safeguard the future of the hundreds of highly skilled jobs in Newport. A spokesperson said: "We remain fully committed to ensuring the continued development of our compound semiconductor cluster in south-east Wales and the role it plays on a wider UK scale. In light of the UK Government's decision, UK Ministers now clearly view the compound semiconductor sector in Wales as a strategic national asset as well as being internationally recognised. We therefore call on the UK Government to invest in the sector to safeguard its future."

GaN expert Tomás Palacios to direct MIT lab

Co-founder of Finwave Semiconductor to take over directorship of MTL

GaN expert Tomás Palacios will be the new director MIT's Microsystems Technology Laboratories (MTL). He succeeds Hae-Seung (Harry) Lee, who has been the director of MTL since 2019.

"MTL is a very unique place," said Palacios in his email to the lab's community. "The research being done here is second to none, and MTL's commitment to developing innovative technologies at all levels of the stack, from materials to devices, circuits and systems is an example to all. We just need to browse the internet, make a phone call, or recharge our electric vehicle to see how technologies that came out of MTL have found their place in applications all around us."

Palacios joined MTL in 2006, after receiving his PhD from the University of California, Santa Barbara, and his undergraduate degree in Telecommunication Engineering from the University Polytechnic of Madrid, Spain. A world expert in GaN electronics for both RF and power applications, Palacios and his group have also made seminal contributions to 2D materials and devices, and heterogeneous integration with silicon electronics.

Palacios is the founding director of the MTL Center for Graphene Devices and 2D Systems, as well as the co-founder of Finwave Semiconductor, an spin-off company commercialising GaN power amplifiers for 5G communications.

Palacios is a Fellow of the IEEE and has served the microelectronics community in many roles. His work has been recognised with multiple awards, including the Presidential Early Career Award for Scientists and Engineers, the 2012 and 2019 IEEE George Smith Award, and the National Science Foundation, Office of Naval Research, and the Defense Advanced Research Projects Agency Young Faculty Awards, among many others.

Palacios follows in the footsteps of Hae-Sung (Harry) Lee, whose guidance of MTL throughout the pandemic Palacios praised, saying, "his amazing leadership during [....] arguably the most difficult times I have ever seen, has been both inspiring, and key to position MTL in the amazing place we are today."

The lab will continue to build upon its long history of innovation, Palacios promised: "Semiconductors and microsystems have never been more important. It is not only about their tremendous implications to computing and communication, but also that they are the key to solving the climate crisis, transforming healthcare and, even, the future of education. We have a-once-in-a-generation opportunity to set the foundation for the future of semiconductors and microsystems, and everything that means for the future of our society. I am convinced that the MTL community will play a vital role in setting this foundation."

GaN's inflection point

Thanks to surging sales in several sectors, including EVs, data centres and industrial motors, the GaN device has now reached an inflection point, argues Jim Witham, CEO of GaN Systems

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THROUGHOUT the last few years SiC has grabbed the headlines, due to a tremendous ramp in device shipments, alongside several vast capacity expansions from chipmakers. But despite this frenetic activity, SiC is not the fastest growing wide bandgap semiconductor. That accolade actually belongs to GaN, which is now at an inflection point, according to Jim Witham, CEO of fabless Canadian firm GaN Systems.

Backing up this claim is a forecast from Yole Intelligence. "They're showing $200 million today in GaN power transistor sales. In four years, that goes to $2 billion. It's ten-X type growth, which is an inflection point," remarks Witham.

He says that in terms of the market size and the opportunity for GaN, it is the EV industry that is topping the list. In this sector, GaN Systems is out in front, having the only production programme. The second biggest opportunity for GaN electronics is consumer charges – where there's competition from the likes of Power Integrations and Navitas – followed by audio and data centres. "We are far and away the leader [in data centres]," says Witham, who claims that the company's shipments to many different sectors makes it the biggest and broadest GaN electronics provider in the industry.

Success for any supplier to the EV industry is hard won, due to the conservative nature of this sector. Due to an awareness of this, during the early days of the company Witham instructed engineers to develop both low-voltage, low-current parts and high-voltage, high-current parts, so that GaN Systems would be in a good position to generate sales when the EV market started taking off. "We sat down with a couple of our customers five or six years ago and defined a programme called AutoQual+, which builds on AECQ 101, the automotive spec for transistors," explains Witham.

As part of that effort, GaN Systems introduced tests to specifically address failure mechanisms for GaN

➤ As the world becomes increasingly electrified – from our homes to our factories to our transportation systems – our demands for electricity are growing at unprecedented rates. A single high-power GaN transistor can eliminate the need for paralleling multiple transistors to achieve a higher power level and thereby reduces a system's complexity and validation time.

devices. This move paid off, convincing customers that the company's devices had sufficient reliability for deployment in EVs.

"Doing that puts us five or six years ahead of other GaN companies," remarks Witham. "We've already put in the hard work."

Parts produced by the Canadian chipmaker include one that delivers up to 150 A, switches up to 650 V, and is suitable for traction inverters operating at up to 250 kW. GaN Systems also offers solutions at higher voltages, giving it opportunities for deployment in both smaller EVs running at 400 V, and more powerful variants at 800 V, where more designs are emerging.

For much of humanity, any awareness of GaN power devices is likely to have come through the role it's playing in fast-charging consumer electronics.

"There's a new term spawned, and that term is GaN charger," enthuses Witham. "People either have a charger or they have a GaN charger."

He argues that this terminology offers further evidence for an inflection point: "People want a GaN charger. They don't want to lug around big old bricks from the silicon age."

This miniaturisation, wrought by a switch from silicon to GaN, is also found in audio – but in that case, this benefit is only part of the appeal. In addition, there's better fidelity, argues Witham. He appreciated this attribute when sitting in sound rooms with customers, where side-by-side comparisons were conducted using the same recordings of the same music, played through amplifiers powered by either GaN or silicon. "I was worried I wouldn't be able to tell the difference," admits Witham, who confesses to owning a tin ear. But he was blown away. "It's just amazing."

The prowess of GaN has not escaped some of the biggest names in data centres, with Intel and HP adopting power supplies incorporating this material.

"The number one item on their operating expense list is the energy to run the servers, so they value high efficiency," says Witham. However, that's not the only advantage of GaN. Revenue for these companies comes from compute and memory power, and this is increased when introducing GaN, because the space it saves allows more processors or more memory to be installed in the server.

Another area where GaN is playing a role is in the renewable energy sector, where it's deployed to ramp voltages up and down and switch between AC and DC waveforms. SiC also competes in this space – it, and GaN, are taking market share from silicon by offering high efficiencies, and the capability of operating at higher frequencies, leading to a trimming of the size and weight of the converters, along with increasing their power density.

➤ To ensure customer acceptance in the very high reliability applications, GaN Systems collaborated directly with customers in the automotive, industrial, and high-reliability industries to develop the very first qualification strategy and process for GaN power semiconductors, named the AutoQual+ qualification criterion.

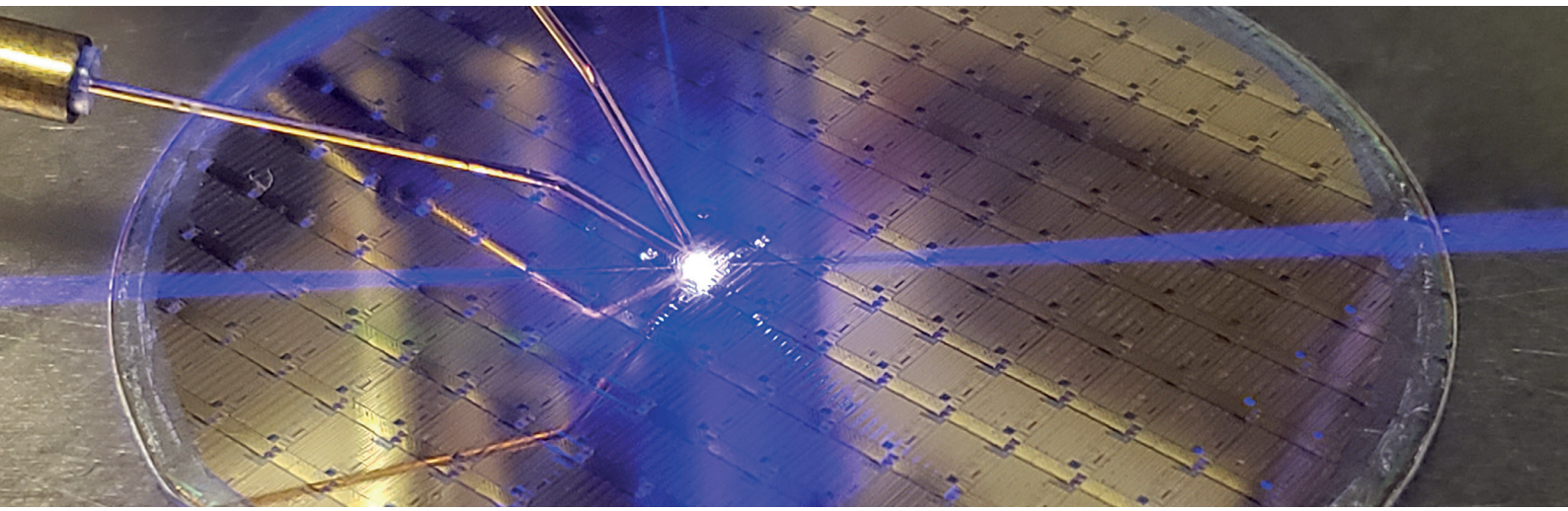
Witham argues that the increase in frequency resulting from the migration from silicon to SiC is relatively modest, shifting from typically 100 kHz to 200 kHz. With GaN, it's an entirely new ballpark, with customers able to use it at 1, 10, even 100 MHz.

These far, far higher frequencies have obvious benefits. "With a silicon carbide system, you can make it half the size, half the weight; and with a GaN system, you can make it a fourth the size, a fourth of weight. Silicon carbide does beat silicon, but GaN beats silicon carbide in terms of power, density and efficiency."

That's not to say that SiC is dead in the water in the renewable sector. There is still a role for this rival, says Witham: "Silicon carbide tends to be good in very high-voltage, very high-power situations."

The biggest recent development within the semiconductor industry has been the injection of substantial government funding, via the 2022 CHIPS and Science Act in the US and the EU Chips Act. This could have at least as big an impact on the compound semiconductor industry as the silicon industry, according to Witham. He points out that due to the vast sums required to build a fab for producing cutting-edge ICs operating at the latest nodes, funding is more likely to support the expansion of facilities requiring less capital expenditure that can churn out chips for analogue and power applications. More fabs with GaN capability may result, a development that would delight Witham, by enabling the company to shine even brighter through this inflection point and beyond.

"Our customers would like to see us making our parts in multiple geographies, so that there's some supply chain resilience. These sources of funds are going to help that."



Getting GaN VCSELs to market

Mirrors formed by alternating conventional layers of GaN with porous equivalents are set to drive the commercialisation of blue and green VCSELs

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

OVER THE LAST FEW YEARS the GaN VCSEL has come on in leaps and bounds, enjoying substantial gains in lifetime, efficiency and output power. Thanks to all this great progress, blue and green VCSELs are now standing on the brink of commercialisation.

Taking this next step is far from easy, but the chances are now better than ever, thanks to a significant breakthrough from a little-known start-up that's located far away from the centre of the action. While much of the early running has come from big names in Japan, such as Nichia, Sony and Stanley Electric, the driver of GaN VCSEL commercialisation is Ganvix of Wilmington, DE.

What distinguishes this trailblazer from its peers is the approach it takes to form the bottom mirror of the VCSEL. Rather than making a distributed Bragg reflector (DBR) from interlacing layers of GaN and a ternary nitride – a pairing that is slow to grow, and, due to a lack of lattice-matching, introduces light-quenching defects into the active region – Ganvix combines conventional layers of GaN with porous variants, produced by electrochemical etching.

Company CEO John Fijol told *Compound Semiconductor* that the start-up is planning to sample VCSELs to its customers in early 2023, targeting output powers of 5mW or more. "We see a lot of nascent opportunities in markets like consumer electronics, communications, industrial devices, sensors. There's a lot of overlap with markets where the gallium arsenide VCSELs have seen success, but with applications in those markets that require blue or green wavelengths."

Bringing together all three colours of VCSEL to form a light-engine for pico-projectors and other projection systems is another opportunity for these lasers, which are valued for their small size and colour purity.

Like their infrared cousins, blue and green VCSELs could also server in communication – but rather than transmitting through a glass fibre, light would be directed through a polymer fibre or free space.

For the next year or so, Ganvix intends to be very selective about the customers it works with, directing its focus on an initial product entry. "We're not in stealth mode by any means, but we're also not at the point where we want to do broad marketing activities and fish for customers," says Fijol.

The output powers of today's Ganvix VCSELs are not as high as the hero devices that have come out of Japan, such as the 22.2 mW laser from Stanley Electric. However, rather than seeing this shortfall as a gap to bridge, Fijol takes encouragement from these higher figures, showing what's possible.

Right now, breaking power and efficiency records is not at the top of Ganvix's agenda. "Our focus for the last year has been more on developing manufacturing," remarks Fijol, revealing that the emphasis has been on improving production through the development of robust designs, advancing cost-effective processing and introducing superior metrology techniques. Thanks to progress on all these fronts, Ganvix has what Fijol describes as "very solid processes for the building blocks".

There's proficiency for producing the DBR, the active region, and the optical cavity.

To form the DBRs, engineers grow a GaN stack that features layers with different doping concentrations. A subsequent electrochemical etch that takes place after device fabrication introduces the porous structure that creates the mirrors.

"The density and size of the nanopores can be very precisely controlled, by adjusting current and voltage settings during the process," reveals Fijol. "This allows us not only to create the porosity, but tailor the optical properties of those layers."

Ganvix combines a partially porous GaN mirror, which typically needs fewer layer pairs than a traditional GaN-based mirror, with a dielectric top mirror. "We could create a very high quality top DBR [with our porous technology], but from a process standpoint it's easier for us to use the dielectric DBR."

For those considering whether to adopt a Ganvix VCSEL, one possible concern might be the threat of contamination entering the porous structure. "But that doesn't happen because of the passivation," explains Fijol, who points out that these structures are inherently stable. He says that another strength of the Ganvix design is that it eliminates the possibility of lower electrical and thermal connectivity near the active region.

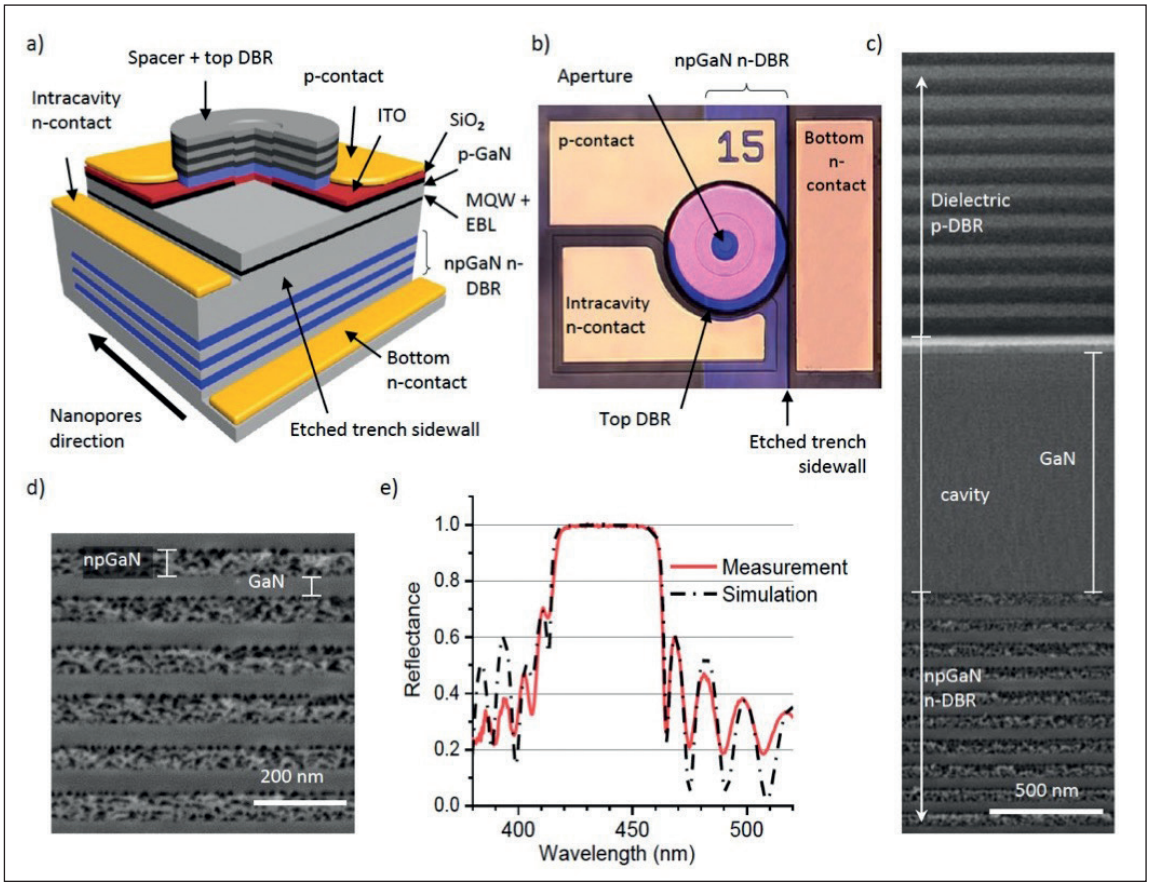
Working with ITRI

Ganvix has teamed up with the Industrial Technology Research Institute (ITRI) in Taiwan to accelerate technology development and speed time to market. Fijol explains that the are many reasons why Ganvix has chosen to work with ITRI. Part of the motivation is the large, active electro-optics community in Taiwan; and another factor is the long-established relationship between ITRI and key personal at Ganvix.

To manufacture its VCSELs, Ganvix needs a line that has tools to produce the porous DBR and assess its quality. "But other than that, we've worked very hard to develop a process that is compatible with standard gallium nitride processing," remarks Fisol. This approach should help the US start-up expand from establishing an initial product to building a broad portfolio that will pave the way for a catalogue-type business.

Another possible goal for Ganvix is to bring light engines to market that are based on red, green and blue VCSELs. "We're working on building the partnerships with existing manufacturers of red devices that will enable us to provide a complete solution for customers."

With a foundation for volume production in place, and a compelling roadmap for the VCSEL, there's good reason to believe that commercial products based on this class of laser will soon be spanning the visible domain.



➤ (a), (b), (c) and (d) The architecture of the Ganvix VCSEL includes a nanoporous bottom DBR and a dielectric top DBR. (e) The measured reflectivity profile of the DBR is in excellent agreement with the results of simulation.

Enhancing volume production of microLEDs and lasers

Aixtron's new fully automated G10-AsP platform, the largest 200 mm AsP batch reactor released to the market, will initiate the end of the wafer binning era

BY VINCENT MERIC, THOMAS KORST AND ARTHUR BECKERS FROM AIXTRON SE

COMPOUND SEMICONDUCTOR devices have come a long way from the first transistors and lasers used in the 1990s for telecommunication or from the replacement of incandescent light bulbs at the beginning of the millennium. They are now extending the roadmap of many applications from power electronics to advanced photonics devices, opening up one opportunity after another: while VCSELs and edge-emitting lasers have a bright future in lidar for autonomous vehicles, microLEDs have the potential to disrupt the market for displays.

Fast growing demand from multiple applications drives chipmakers to employ high-volume, mass production processes. These processes must be tailored to the specific requirements of each device type and be robust enough to ensure high yields in a manufacturing chain with growing complexity. To address all these needs, Aixtron has launched a new MOCVD platform for arsenide-phosphide epiwafers for microLEDs and lasers.

➤ G10-AsP reactor including cassette-to-cassette automation

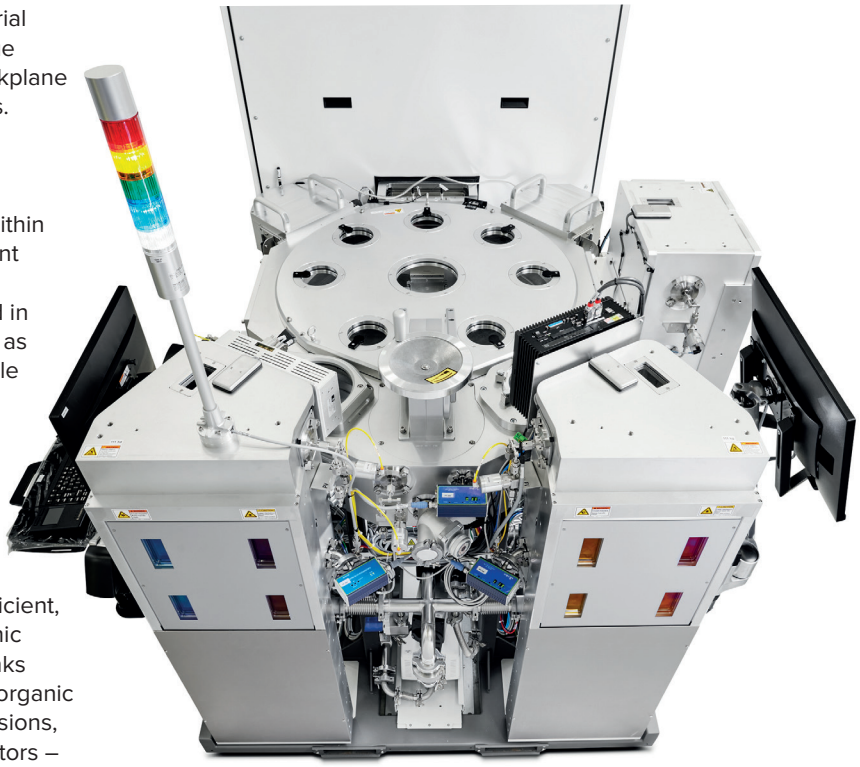
This new MOCVD platform AIX G10-AsP brings full automation, automated cassette-to-cassette wafer loading and *in-situ* etching for the first time to the epitaxy of arsenide-phosphides. These features will help to ensure reliable, efficient production of high-quality microLEDs, VCSELs and InP lasers with enhanced uniformity, reduced particles and optimised yield.

MicroLEDs are on the verge of revolutionising the display industry

Since the emergence of the solid-state lighting era a decade ago, LEDs have found their way into several other applications, including the head and tail lights of automobiles and the backlighting units for displays. In

addition, LEDs have been deployed in industrial displays and signage, with red, green and blue pixels mounted onto a thin-film transistor backplane to deliver very bright, high-resolution displays. These displays are used for advertising, both indoors and outdoors.

Recently, one of the most exciting activities within the LED community has been the development of the microLED, a miniaturised form of this device. It is no more than 50 μm in width, and in some devices this dimension can be as small as 600 nm, according to a recent report from Yole Intelligence.

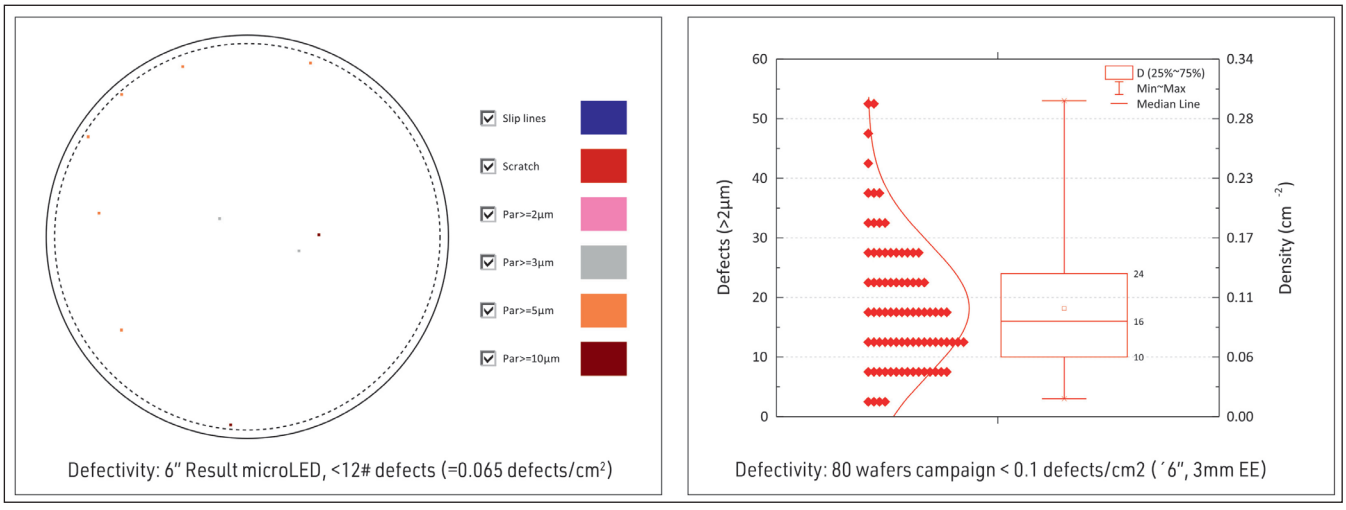


MicroLEDs are seen as the future of displays. Compared with organic LEDs, these inorganic siblings are renowned for their durability, their long lifetime, and their absence of burn-in effects. What's more, microLEDs promise to be far more energy efficient, brighter, and able to offer a wider high dynamic rate and a more extensive colour gamut, thanks mostly to their intrinsic, superior quality over organic material. In addition, due to diminutive dimensions, microLEDs are expected to enable low fill factors – less than 10 percent for larger displays – opening the door to integrate new sensors between the pixels.

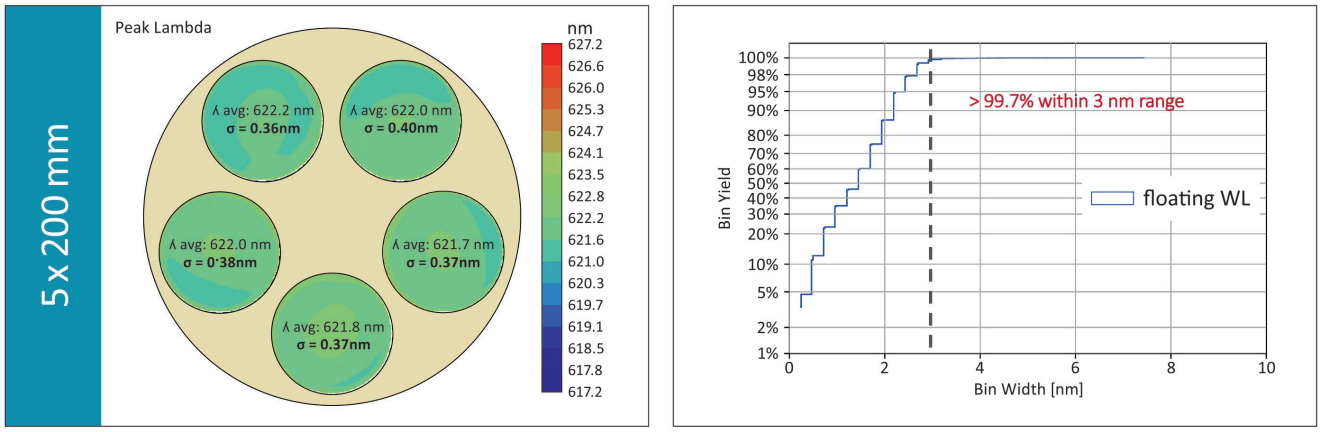
Due to their tremendous promise, the last few years have witnessed a great deal of research and development of the microLED. This miniature marvel is seen as a very promising light source for smart watches, smartphones, TV displays, augmented-reality projection displays and automotive displays. With so many lucrative opportunities on the horizon, the microLED has the potential to become the biggest market opportunity for the LED over the next decade.

Fulfilling the commercial promise of the microLED hinges on overcoming several challenges, both related to quality of the pixels and their transfer to backplanes. To enable a very high pixel resolution and a low manufacturing cost, chipmakers will have to produce very small pixels and transfer them to the final display. It is anticipated that pixel sizes of not much more than 10 μm are needed for first-generation volume products addressing mid-size and larger displays, and variants with a width of less than 3 μm – and possibly sub-micron – may be required for very high-resolution AR applications. Manufacturing pixels that are this small is challenging. It is crucial to break new ground for the defect density at the epitaxy level, not only to ensure a high chip yield, but because this matters for the final display.

➤ G10-AsP fully automated processes with cassette-to-cassette handling and optional standard mechanical interface port



➤ Figure 1. G10-AsP demonstrated defectivity level, on-wafer and in 10-run marathon mode (R-E-R).



PL Plot – Fully Loaded microLED Run (5 wafers)

Bin Yield (%) for all wafer area (21 x 200mm wafers)

➤ Figure 2. Wavelength uniformity yield for microLED wafers (5 x 200 mm).

One downside of the miniaturisation of the LED is that it impairs binning, with small pixel sizes preventing any sorting of this device. It may be possible to introduce techniques that repair pixels or deal with redundancy – both are under development – however, this is undesirable in the long run because any such solution will increase production costs.

Another substantial challenge for making displays from microLEDs is that it requires the transfer of a vast number of devices. For example, to produce a 4K TV, there needs to be a transfer of around 25 million sub-pixels, which is too many for traditional pick and place. Superior techniques may come from new transfer methods, such as elastomer stamps and even microfluidic or laser transfer. Another option, suitable when a very high density of pixels is needed for a small display area, is the direct bonding of microLEDs to a CMOS wafer. Ultimately, all the approaches advocate for a leapfrogging improvement in wafer-level uniformities and cleanliness.

Advanced photonics requirements

In contrast to microLEDs, photonic devices are well established, having served in several applications for many years. For example, infrared compound semiconductor lasers and detectors are the building blocks of telecom and datacom transceivers supporting the world's hunger for data, year after year.

For telecommunication, an increase in data rates will come from a hike in bandwidth, realised by increasing the number of different wavelengths transmitted simultaneously through an optical fibre.

To ensure denser packing of distinct frequencies, engineers have been trying to increase the tightness of the wavelength tolerances, to prevent overlap between a signal at one wavelength and a signal at another. Fabrication of these photonic devices is a highly complex process, often requiring several growths in an MOCVD reactor.

This complex manufacturing calls for refined control of the epitaxial process, in terms of material accuracy and defects. If any yield loss occurs during one of the earlier steps, it is particularly detrimental, having a multiplier effect on any subsequent step.

The new G10-AsP: World's first fully automated AsP MOCVD reactor

Aixtron is releasing the first fully automated AsP platform, the G10-AsP. Engineered to serve the most demanding microLED and advanced photonics requirements, this system features a cluster of two process modules, each embedding a mini-batch reactor that accommodates up to twelve 4-inch, eight 6-inch or five 8-inch wafers. The platform inherits some of the AIXG5+ C DNA and architecture, such as its level of automation and *in-situ* cleaning.

MicroLEDs will revolutionise the world of displays as they offer better durability, higher lifetime, a better picture quality and a very low energy consumption. However, this innovative technology challenges the production processes as we know them today.

Equipped with automated, high-temperature, cassette-to-cassette loading of wafer, the G10-AsP can undertake up to ten process runs – that is, for example, the production of fifty 200 mm epiwafers – before there's any need for operator assistance to load new wafers. This exceptional degree of automation enables a reduction in the number of technicians required to provide support around the clock, day after day.

For the first time, the front-end of the MOCVD system can be equipped with standard mechanical interface pods to minimise the exposure of epitaxial wafers to the room environment. Aided by this and *in-situ* cleaning, particle densities can plummet as low as never before for MOCVD processes. For example, the G10-AsP has demonstrated an average defectivity below 0.1 defects/cm^2 with a particles size greater than 2 µm in a 80-wafers marathon campaign (see Figure 1).

With on-board *in-situ* cleaning, users can reset chamber conditions on demand. They may decide to do this after every process run, if they need to cater for the most demanding requirements; or they may do so after completing a production campaign, so they benefit from the highest throughput.

Note that the benefits of *in-situ* cleaning minimise imperfections in the epiwafers. Another benefit of the cleaning process is that it can replace the regular preventive maintenance for any AsP MOCVD system – this is required to remove contaminated material from the chamber on a regular basis. Eliminating preventive maintenance on the process chamber ensures a significantly longer, more stable production campaign for all types of MOCVD process.

The G10-AsP also inherits the advanced wafer-level temperature control that has been a reliable component of Aixtron reactors for growing nitride wafers. This enables individual control of wafer temperature, ensuring improved reproducibility in campaign mode.

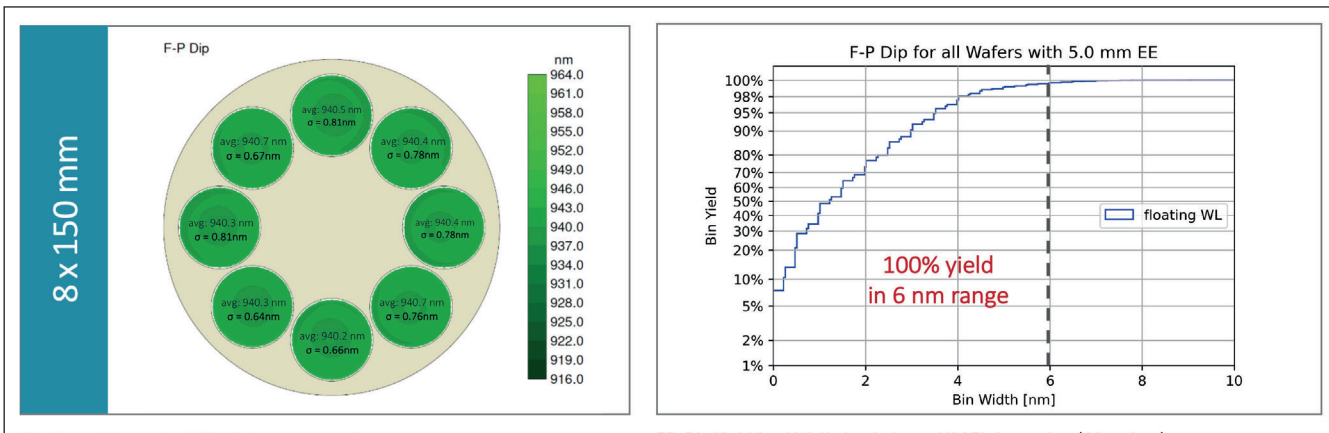
Another feature of the G10-AsP is a new central gas injector that provides the highest metalorganic and hydride utilization. With this refinement, chemical efficacy is improved by more than 40 percent. Therefore, purification and scrubbing costs are trimmed to the lowest ever seen for such materials.

What's more, the tuning capability of the new injector enables new levels of uniformity for multi-quantum wells, and for quaternary materials used for advanced lasers. For example, trials have demonstrated exceptional uniformity of the platform, with close to 100 percent of the surface area within a 3 nm-wide bin (see Figure 2) over a campaign of twenty-one 200 mm wafers (fully and partially load combined).

Equally impressive results have come from 150 mm VCSEL epiwafers. In this case the uniformity is as low as 0.7 nm standard deviation within wafer, translating into yields as high as 100 percent for a 6 nm-wide bin in a 80 wafers marathon campaign (see Figure 3).

For both microLEDs and today's advanced photonics, the era of wafer binning is now over. The high volume of compound semiconductor devices needed for markets demands scalable, reliable MOCVD processes. Offering just this is the G10-AsP: it can provide the production of microLEDs with sizes of 10 µm or less; and accommodate the complex requirements for high-volume production of InP edge-emitters and GaAs-based VCSELs, with the controllability of regrowth only MBE could reach today.

The G10-ASP is the largest 200 mm AsP batch reactor released to market, enabling the highest throughput of its class to maximise cleanroom utilisation. As chipmakers undertake a rapid adoption of the G10-AsP system, they will fulfil the tightened market requirements for microLEDs and lasers and enable the production of high performance, predictable devices while realising significant cost savings.



FP-Dip – Fully Loaded VCSEL Run 6 inch wafer

FP-Dip Yield for 10 fully loaded runs VCSEL Campaign (80 wafers)

➤ Figure 3. Wavelength uniformity yield for processed VCSEL wafers (8 x 150 mm).

GaN powers ahead

Researchers at the recent International Electron Devices Meeting unveiled record-breaking GaN devices featuring superior architectures

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN OUR INDUSTRY, the standing of GaN continues on its upward trajectory. This wide bandgap semiconductor is entrenched as the ultimate material for making blue, green and white LEDs, and is now strengthening its case for the transmission of RF signals and starting to enjoy a tremendous sales ramp in the power domain. In the later sector, revenue is tipped to soon break the $1 billion barrier, driven by advances in device performance that will ensure energy savings in various consumer and industrial applications.

Underpinning this surge in sales are efforts of researchers in academia and industry – this community is improving established devices and developing new ones. Some of their recent, major breakthroughs were detailed at the 68th IEEE International Electron Devices Meeting (IEDM), held from 3-7 December, 2022, at the Hilton San Francisco Union Square. At that gathering, engineers unveiled new records in power integration, success with high-voltage switches on sapphire substrates, the introduction of a hybrid gate that bolsters threshold-voltage stability, and a debut for the vertical GaN superjunction device.

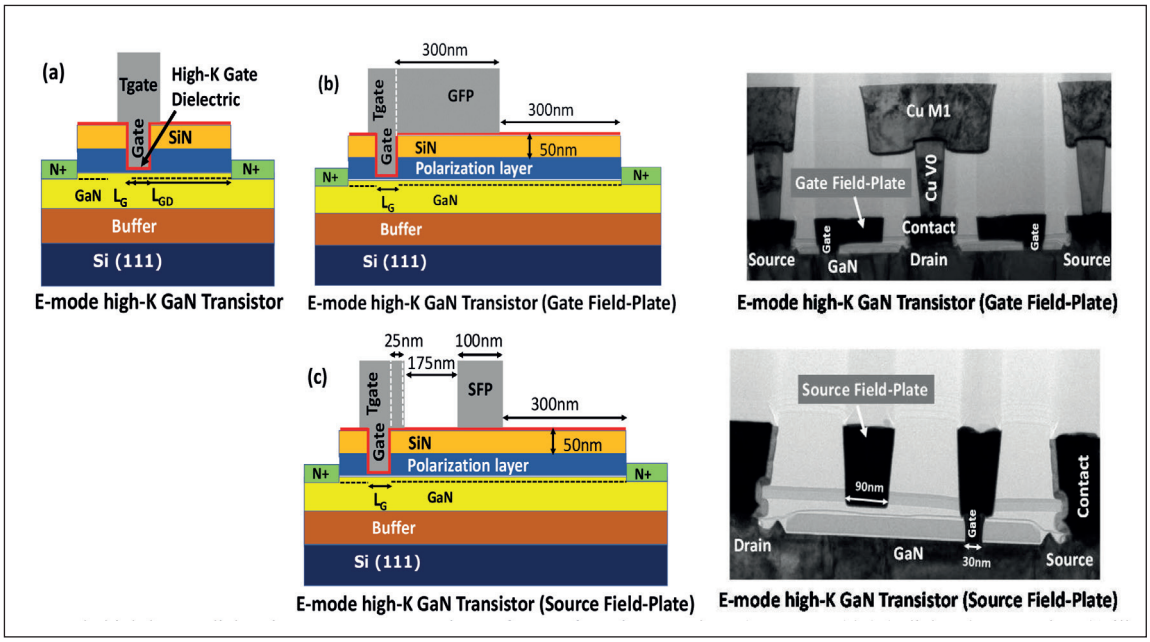
➤ San Francisco, California, hosted the 68th IEDM

Optimising field plates

Speaking at the latest IEDM, Intel Components Research Engineer Han Wui Then claimed new records in power integration, accompanied by a new benchmark in the RF. He and his colleagues have been working to improve the performance of GaN devices on a 300 mm silicon (111) platform through the introduction of a pair of scaled field plates.

Intel's latest success builds on its previous breakthroughs in GaN-on-silicon technology. Back in 2019, the company's Components Division reported the first industry process for 300 mm GaN-on-silicon, motivated by a desire to better the performance, efficiency and density beyond what is capable with established technologies, such as SOI, CMOS, SiGe, BiCMOS and GaAs/InP HBT/HEMT. The GaN-on-silicon technology they have developed, promising high data rates and the ability to aid 5G communication systems, has already led to claims of best-in-class performance. Previous presentations by Then and his co-workers championed the capability of this technology for voltages of 12 V or below, where it could be used for battery-powered RF front-end modules. That ceiling on the voltage has now been raised, with Then announcing at the latest IEDM that with the introduction of field plates, performance is now far, far better than that of incumbent technologies at up to 40 V.

These field plates are added to a platform that is bringing Moore's law to GaN, with fabrication of devices with dimensions on the nanoscale involving the use of atomic layer etching, as well as the



➤ Figure 1. Intel Component Research has progressed its high-κ GaN transistor (a) to designs with a gate-field plate (b) and a source-field plate (c).

atomic layer deposition of a dielectric gate. These processes are key to producing two devices: the enhancement-mode high-κ gate dielectric GaN transistor, and the D-mode Schottky GaN HEMT. The two types of transistor can be incorporated into circuits with an interconnect process that features four copper layers and enables tight integration of passives. There is also the opportunity for monolithic integration of GaN and CMOS technologies, using advanced chemical-mechanical polishing and cleaving processes.

For their latest work, Then and colleagues have investigated two different field plate architectures for enhancing device performance at higher drain voltages. One involves a gate field-plated and the other a source field-plate (see Figure 1 for details).

"What we conclude from our research is that the source-connected field plate can achieve the extension of the drain voltage to higher drain voltages, bringing the field plate closer to the 2D electron gas to exert control on the 2D electron gas, and finally scale the source field plate in order to minimise parasitics," remarked Then.

With the source-field-plate device, which has a 30 nm gate length, a 600 nm gate drain and a 100 nm source field plate, a drain-source breakdown voltage of 70 V is realised, based on a breakdown current of 1 mA/mm. Increasing the gate length of this device boosted breakdown to 92 V. "These are really excellent devices: short channel and high voltages," claimed Then.

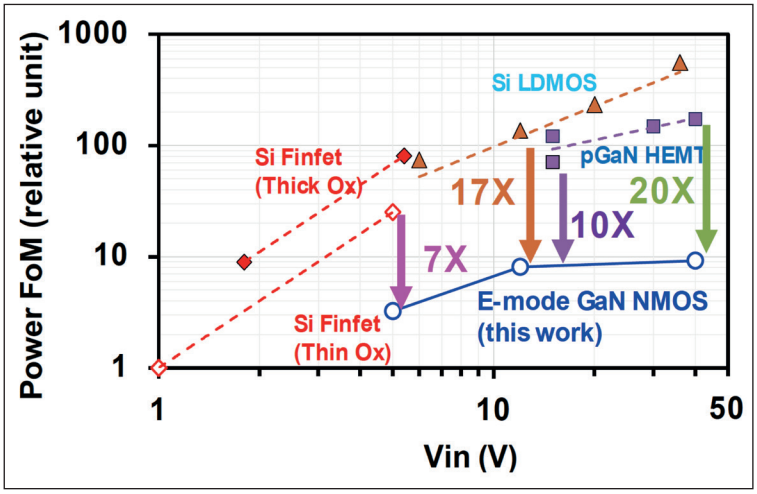
The team from Intel's Components Division have also considered a figure-of-merit for power: the product of on-resistance and gate charge, which reflects the amount of charge switched in and out of the transistor. Measurement gave values for this figure-of-merit of less than 4 mΩ nC – that's so low that they are best-on-class for power electronics, according to Then. He added that this value improves with scaling of the channel length.

Additional plots show the true enhancement-mode operation of the devices, with the drain leakage below 0.3 pA/mm at 40 V, for a gate voltage of 0 V; and just 2 V required to turn the MOS gate fully on.

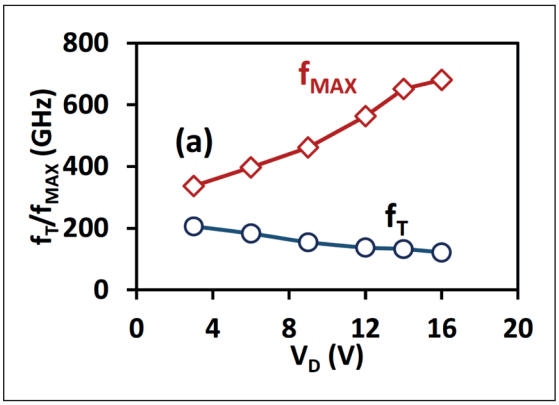
"That really contrasts with what is needed to turn on a discrete GaN pHEMT device," explained Then. "You will need 5-6 volts in order to turn on those devices."

Due to this lower voltage, it is possible to integrate a GaN MOSHEMT with a high-κ gate dielectric with CMOS. Even the latter, in the form of a 1.8 V technology, is capable of driving the gate of the GaN transistor.

The engineers from Intel have also investigated the lifetime of their GaN devices. Experiments, showing the benefit of a field-plate, indicate a lifetime for this



➤ Figure 2. Intel's latest GaN devices that incorporate a field plate have a far better figure of merit, in terms of the product of on-resistance and gate charge, than all the incumbent technologies.



➤ Figure 3. Intel's field-plated GaN NMOS devices show an increase in fmax and a slight reduction in f_T with drain voltage.

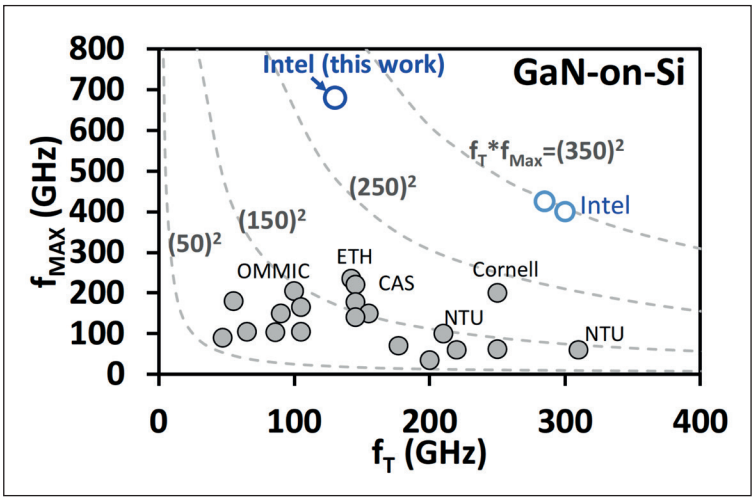
type of device of 10 years, based on a 10 percent degradation in the on-resistance under a 41 V drain-source stress.

Using a figure of merit that is the product of on-resistance and gate charge, the team benchmarked its device (see Figure 2). "What we see is fantastic figure-of-merit gains over incumbent technologies, such as silicon finFET, silicon LDMOS and *p*GaN HEMT," remarked Then. "The figure of merit can be ten times to twenty time higher than all these technologies."

As well as considering the capability of their devices for power, Then and colleagues have considered RF capabilities. The maximum cut-off frequency (f_{max}) increases with drain voltage, to hit what is claimed to be a record-breaking 680 GHz at 16 V for the source-field plate transistor. The cut-off frequency, f_T, shows a slight decline with voltage, falling to 130 GHz at 16 V (see Figure 3). Benchmarking these results shows that this level of performance far exceeds that for other GaN-on-silicon devices (see Figure 4).

Supported by sapphire

For GaN power devices, by far the most common substrate is silicon. However, there's a very strong case for using sapphire, a platform championed at IEDM by Geetak Gupta, a Senior Member of Technical Staff at Transphorm. In his talk he made a strong case for the merits of using GaN-on-sapphire for the production of 1200 GaN switches.



➤ Figure 4. Benchmarking Intel's latest GaN-on-silicon devices reveals a record f_{max}.

Transphorm's motivation for developing this particular product is partly driven by the opportunities in the electric vehicle market, which will increase its production of automobiles running on an 800 V supply over the next few years. The chipmaker could target the deployment of its 1200 V GaN FET on on-board chargers and the driver inverter. Additional markets where this power device might serve include those that require uninterruptable power supplies, the aerospace and defence sectors, server farms and the photovoltaic industry.

For lower voltages, Transphorm has launched five generations of 650 V transistors on silicon substrates, plus three generations of 900 V variants. According to Gupta, the company is unique in providing the market with a product capable of handling this higher voltage.

To extend the portfolio to 1200 V, it makes much sense to switch the substrate from silicon to sapphire, argued Gupta, as this widely available alternative enables far lower epitaxial costs. "This is because the high voltage is held vertically across the buffer, and as a result, greater than ten microns of epitaxy growth is required to build a 1200-volt device [on silicon]." With sapphire, its insulating nature allows 1200 V GaN FETs to be produced with a very thin buffer layer, trimming epitaxial growth costs and also improving material quality, thanks to less stress in the material.

Processing of GaN-on-sapphire is well established, due to the success of the LED industry. Gupta advocates running 150 mm or 200 mm wafers through a CMOS-compatible fab, followed by further processing using grinding and dicing tools that serve in the GaN LED industry.

Fabrication of Transphorm's 1200 V devices begins with the growth of a GaN heterostructure that is said to have very good crystal quality, a low dislocation density near the active layers and excellent sheet resistance uniformity. Epiwafers are processed into lateral GaN HEMTs that feature a high-mobility two-dimensional electron gas and a field plate to optimise the electric field profile. Low-voltage silicon MOSFETs with a threshold of around 4 V are attached to these HEMTs to create normally-off switches. To ensure low thermal resistance, the GaN die is directly bonded to the package leadframe with a low void fraction.

Electrical measurements on this switch reveal that off-state leakage is below 2 mA for voltages up to 1200 V, with hard breakdown occurring above 2 kV (see Figure 5). "This gives us an adequate

voltage margin for a 1200 volt device," said Gupta, who added that the switch shows very good output characteristics. Pulsed current in the on-state exceeds 200 A, indicting high-current capability.

Gupta and his co-workers have used a three-dimensional model to evaluate the performance of their switch in a TO-247 leadframe on a copper heatsink. Modelling indicates that thinning the sapphire to 200 μm, a relative conservative value, should ensure a low thermal resistance. Measurements on such a device showed good agreement with the model, giving a thermal resistance of 0.78 °C/W, which is said to be sufficient for high-power applications.

"There is room for further improvement, as substrate thinning to 100 microns is well within the range offered by commercial vendors," added Gupta.

To evaluate the switching performance of their device, Gupta and colleagues investigated inductive switching in a half-bridge circuit, using 720 V and 28 A. This study revealed a rise time of around 14 ns – the value for SiC is 25 percent higher, even for a much smaller gate resistance; and for the silicon IGBT the value is 140 percent higher. Note that the fall time for the 1200 V GaN switch is just 13 ns.

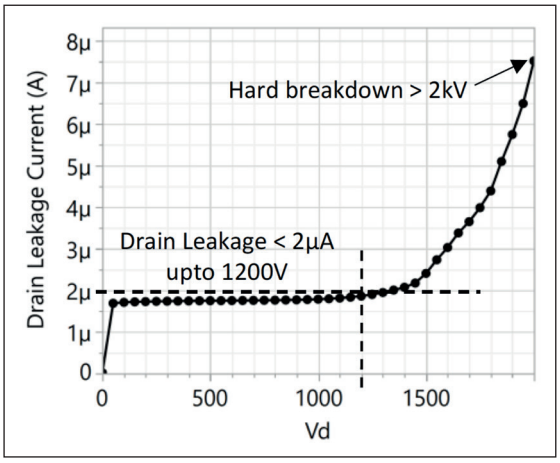
Thanks to fast rise and fall times, switching loss of the half-bridge circuit operating at 720 V and 24 A is just 510 mJ per cycle. According to Gupta, this value is half that for a state-of-the-art SiC MOSFET.

"We also built a buck converter, to test the efficiency of 1200 volt GaN switches," added Gupta. Using a pair of 1200 V, 70 mW devices and 50 kHz switching, the efficiency of this converter is above 99 percent. This drops to 98.7 percent at 100 kHz.

"Lastly, we benchmarked our devices against state-of-the-art silicon carbide," said Gupta, who pointed out that the GaN-on-sapphire variants have a superior figures of merit. "This is reflected in the buck converter efficiency of 1200 V GaN being higher than silicon carbide state-of-the-art MOSFETs." The extent of this superiority is shown in Figure 6.

Hybrid gates

A decision facing every designer of a GaN HEMT is whether to use a Schottky-type gate for their device, or one based on an ohmic contact. The Schottky-type variant is often preferred, because it offers a lower gate leakage and an enlarged operation voltage swing.



➤ Figure 5. Transphorm's GaN-on-silicon switches are capable of handling more than 1200 V.

However, the Schottky-type gate does have its weaknesses. In a presentation delivered by Chi Zhang from Southeast University, China, he explained that a drawback of the Schottky-type gate is that it can lead to charge storage, stemming from the use of back-to-back diodes.

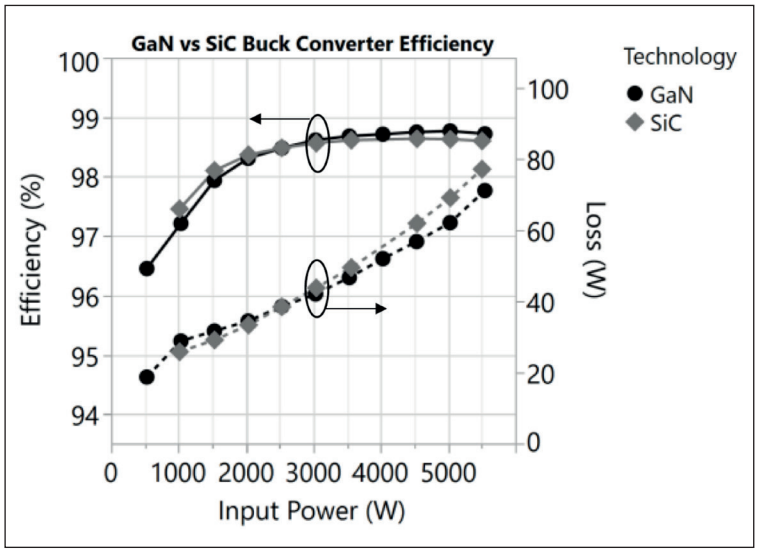
The reason for this, according to Zhang, is that the depletion region in the Schottky-type gate can result in a "floating *p*-GaN layer", sandwiched between the gate and the channel. It is difficult to remove charges in this layer, induced by a drain bias, and these carriers lead to a shift in the threshold voltage – in a commercial Schottky-type GaN HEMT, this shift is typically as high as 0.42 V. This increase in threshold voltage is undesirable, leading to a higher on-state resistance and reduced system efficiency.

While an ohmic gate can combat these issues, it also results in a large gate leakage. What's more, there's a need for a higher continuous gate current to maintain an on-state operation voltage.

A far better option, argues Zhang – who has been working with colleagues at Southeast University and at Nanjing Electronic Devices Institute – is to introduce a new, hybrid gate architecture that ensures a low gate leakage current and a small threshold voltage shift.

To fabricate the transistors, the team began by loading a 2-inch silicon substrate into an MOCVD chamber and depositing a 5 μm-thick buffer layer, followed by a 300 nm-thick undoped GaN channel, a 15 nm-thick $Al_{0.23}GaN_{0.77}N$ barrier and a 70 nm-thick *p*-GaN layer with a magnesium doping concentration of around 2 x 10^{19} cm^{-3}.

Another highlight in the development of GaN power devices at IEDM came from the unveiling of the first vertical superjunction device in this material. Yuhao Zhang from Virginia Tech made that claim



➤ Figure 6. In a buck converter, state-of-the-art SiC switches have a loss that is 8-9 percent higher than GaN-on-silicon variants made by Transphorm.

These engineers formed the hybrid gate (see Figure 7) by using an e-beam evaporator to deposit 20 nm of titanium, followed by 80 nm of gold. Lift-off followed, before forming the Schottky contact on the *p*-GaN layer and the top ohmic regions by depositing 100 nm of tungsten and then undertaking patterned lift-off. Using the Schottky gate metal as the hard mask, they etched a *p*-GaN region with a self-aligned process. Source and drain contacts were created by depositing a metal stack with an e-beam evaporator, prior to thermal annealing under nitrogen gas for 45 s at 840 °C.

Transmission line measurements on the hybrid-gate HEMT revealed a contact resistance of 101 Ω mm and a resistivity of 0.003 Ω cm^2.

"In order to verify the reliability of the hybrid gate HEMT, Schottky HEMTs fabricated by the same production line on the same wafer were also investigated as a comparison," remarked Zhang. "The results indicate that the hybrid-gate structure has no impact on the concentration of the *p*-GaN layer. The hybrid-gate structure only adjusts the Schottky diode formed by the gate metal and the *p*-GaN layer. The *p-i-n* diode – consisting of the *p*-GaN layer, barrier layer, and channel layer – is not affected, due to the same process steps."

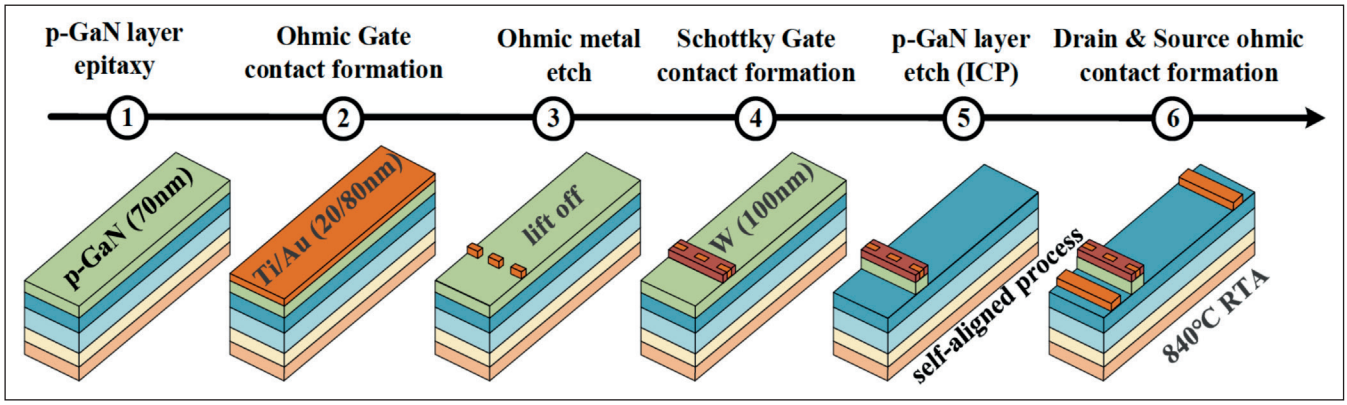
Zhang and co-workers have also considered the change in the performance of their devices at elevated temperatures. Increasing the temperature from 300 K to 400 K shifted the threshold voltage by less than 0.3 V.

Measurements on a conventional Schottky diode HEMT showed a long-term shift in the threshold voltage of around 0.2 V (see Figure 8). During DC gate bias stress, the emitted holes accumulated in the *p*-GaN layer, and after removal of the bias, holes could not exit this region, causing the threshold voltage to decrease. "Significant advantages can be observed in hybrid-gate HEMTs, where almost no threshold voltage shifts happen after 1200 seconds DC gate bias stress," added Zhang.

The hybrid gate structure also ensures a superior performance under drain bias. For the conventional Schottky diode HEMT, the threshold voltage shifted by 0.7 V, compared with a shift of less than 0.03 V for the hybrid device.

To evaluate reliability, Zhang and colleagues measured the breakdown voltage of HEMTs with a Schottky gate, an ohmic gate and a hybrid gate. All three variants exhibited a very similar breakdown of around 10.6 V, indicating that the breakdown mechanism is independent of the junction between the metal and *p*-GaN. Using a drain-source voltage of 9 V, current-transient measurements unveiled energies for the traps of 0.69 eV and 0.59 eV, for the HEMTs with the Schottky gate and the hybrid gate, respectively. "This information indicates that hybrid-gate HEMTs own shallower traps, leading to easier discharge of the induced stored charges," concluded Zhang.

The team have also investigated the performance of their novel HEMTs in a circuit producing unclamped



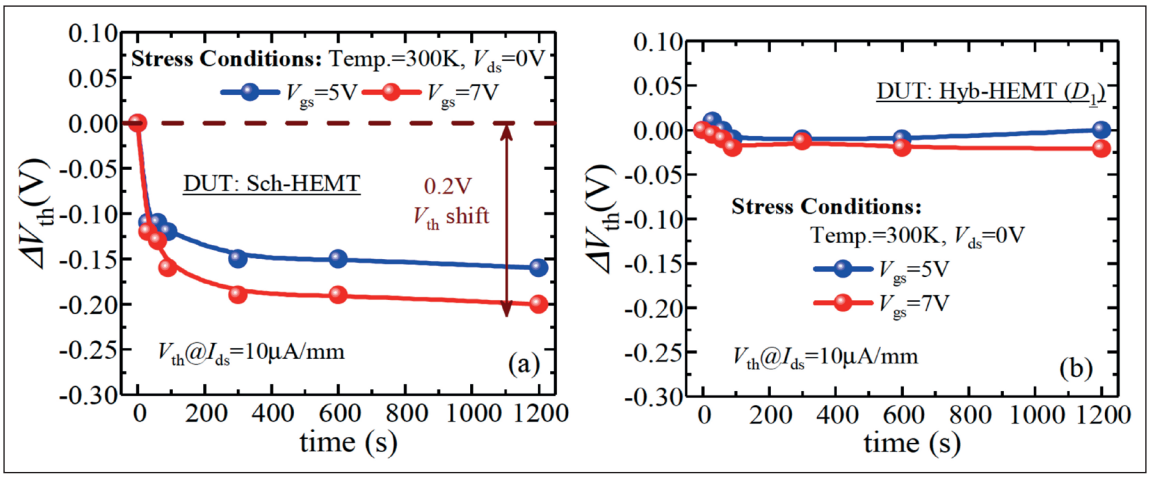
➤ Figure 7. A team led by researchers from Southeast University, China, are pioneering GaN HEMTs with a hybrid gate. The fabrication of these transistors involves the deposition of a Ti/Au (20 nm/80 nm) metal stack, followed by the formation of a Schottky contact on the *p*-GaN layer and top ohmic contact regions by the addition of 100 nm of tungsten.

The NSER is here.

With the passing of the CHIPS Act, a blueprint to advance US semiconductor manufacturing competitiveness is needed now more than ever. More than 80 industry leaders, educational institutions and public sector leaders from states around the nation came together to collaborate and develop the **National Semiconductor Economic Roadmap**. The first-of-its-kind roadmap identifies goals and objectives across four critical pillars: infrastructure, supply chain, workforce, and entrepreneurship to ensure global competitiveness. Now, it's yours.

Download it now at **azcommerce.com/NSER**

ARIZONA
COMMERCE AUTHORITY



➤ Figure 8. Stress tests reveal the superiority of the hybrid HEMT, in terms of a reduced voltage shift.

inductive switching. Subjecting the equivalent circuit with a Schottky gate HEMTs to 2 million unclamped inductive switching cycles produced a shift in the threshold voltage. This shift is not observed in the circuit with the hybrid-gate HEMT, underlining the promise of this device.

A related study considered the repetitive reverse freewheeling stress, with measurements of gate capacitance. "After 1000 cycles stress, the measured gate capacitance indicates that no gate charge storage mechanism occurs in the *p*-GaN layer for hybrid gate HEMTs," remarked Zhang, adding that this helped to ensure gate reliability.

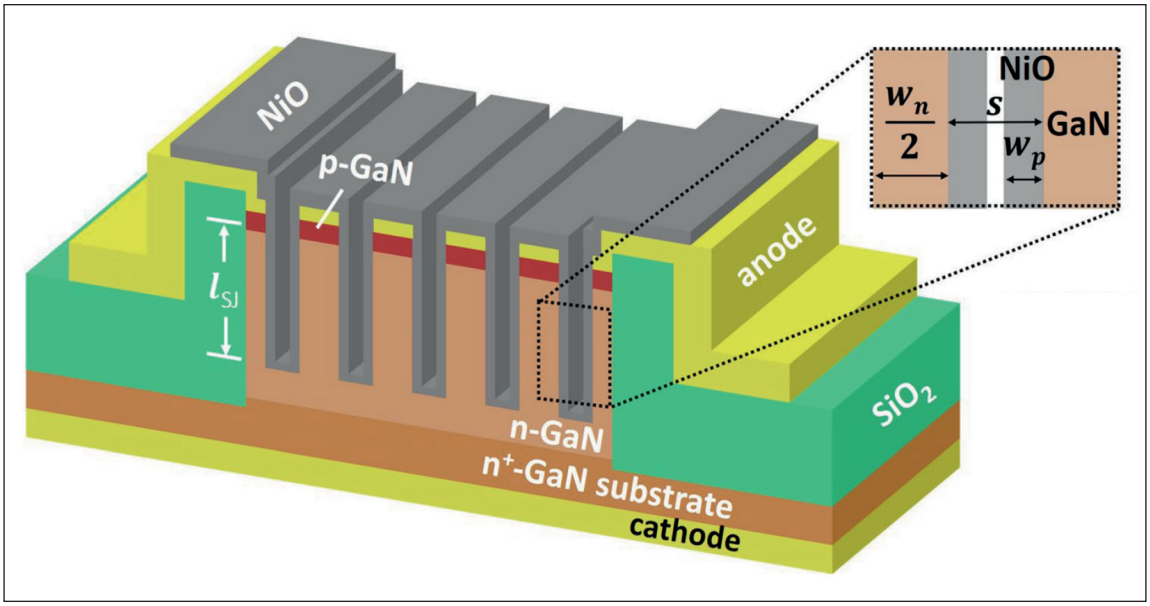
A debut for the superjunction

Another highlight in the development of GaN power devices at IEDM came from the unveiling of the first vertical superjunction device in this material. Yuhao Zhang from Virginia Tech made that claim, describing work accomplished through a collaboration between his group and researchers at the University of Southern California, Enkris Semiconductor, the University of Cambridge, Qorvo and the US Naval Research Laboratory.

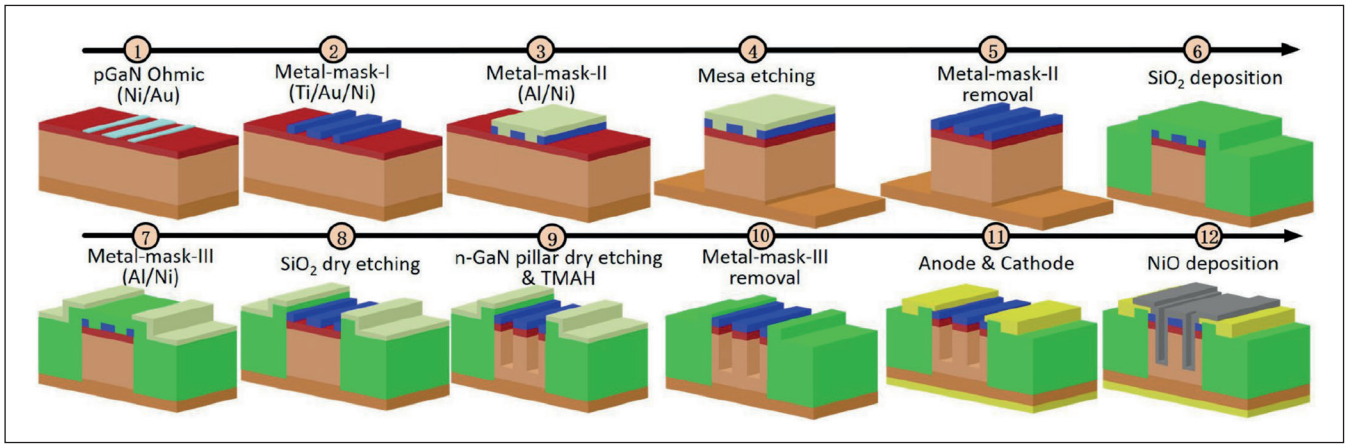
The attraction of any superjunction is that it can overcome the trade-off between the blocking voltage and the on-resistance that limits the performance of one-dimensional devices. Silicon super-junction devices are already well-established, netting billion-dollar revenues per annum, while those made from SiC were first unveiled in 2016. Now GaN has joined the ranks, delivering impressive results.

"To make the superjunction in GaN is very challenging," remarked Zhang. He explained that one of the two standard approaches, the creation of trenches that are subsequently filled, is susceptible to interfacial impurities and high leakage currents. Meanwhile, the alternative, involving multiple epitaxial steps and ion implantation, requires high-pressures and temperatures for activation – and re-growth can result in re-passivation.

Zhang and co-workers have pursued a novel trench-filling approach that avoids the issues associated with standard methods. Their solution is to fill the trenches with a layer of NiO – it has previously been shown to provide a conformal coating on GaN,



➤ Figure 9. A collaboration led by Yuhao Zhang and co-workers at Virginia Tech has produced the first GaN device featuring a superjunction.



➤ Figure 10. Many steps are required to produce the GaN superjunction diode.

handle high electric fields and offer good thermal stability. NiO has a bandgap of around 3.4-4.0 eV, a critical electric field of up to 5 MV/cm, and a dielectric constant of 11.9, which is higher than that for GaN.

Before fabricating devices, the team modelled the performance of the superjunction. Efforts began by considering the dimensions of the GaN pillars, with calculations revealing that they should be around 2-3 μm wide, and have a donor density of the order of 10^{17} cm^{-3}. After this, they thought about the NiO filling.

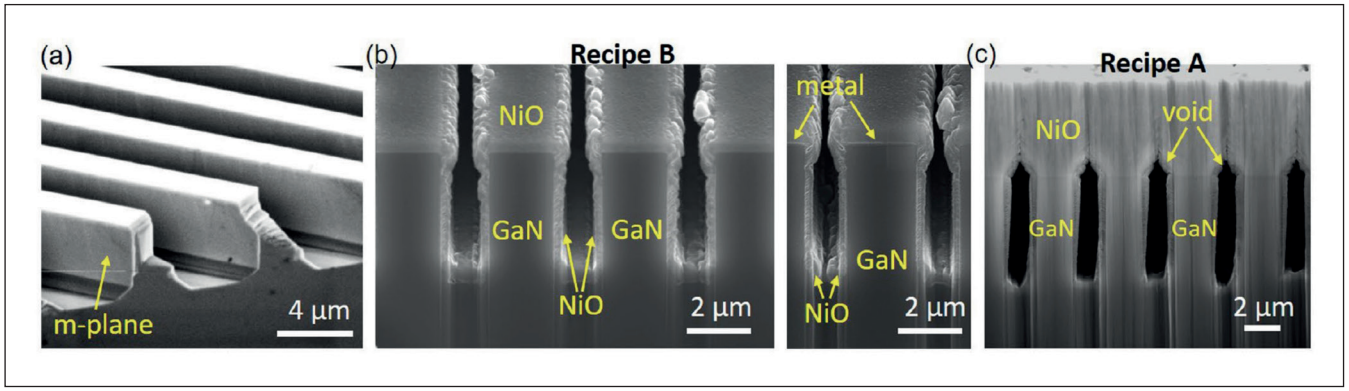
"We wanted to explore the possibility of not having the trench fully filled by the *p*-type material," said Zhang. "In this way we can use the *p*-type material with a much higher acceptor concentration. This may essentially make the sputtering process easier."

Modelling supported this approach, with the electric field distribution having a similar profile for trenches that are completed filled with NiO, and those that are just partially filled.

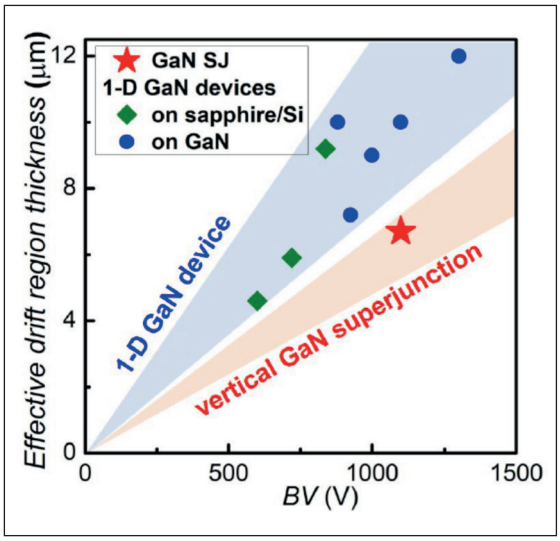
Armed with this insight, the researchers investigated the growth conditions for sputtering NiO with an appropriate doping concentration. They considered three recipes: just argon, a mix of argon to oxygen in the ratio 20 to 1, and a mix of argon to oxygen in the ratio 2 to 1. The later produced a very high hole concentration, exceeding 1 x 10^{19} cm^{-3}, according to Hall measurements. More suitable concentrations resulted from other recipes, with just argon resulting in a value of 5-6 x 10^{16} cm^{-3} and the mix of argon to oxygen in the ratio of 20 to 1 producing a value of 4-5 x 10^{17} cm^{-3} – both approaches were used in device fabrication, with prior modelling employed to optimise dimensions.

Fabrication of the devices began by loading a 2-inch GaN substrate in an MOCVD reactor and depositing: a 0.8 μm-thick layer of GaN, doped with silicon at a concentration of 2 x 10^{18} cm^{-3}; an 8 μm-thick layer of GaN, doped with silicon at a concentration of 9 x 10^{16} cm^{-3}; a 300 nm-thick layer of GaN, doped with magnesium at a concentration of 1 x 10^{19} cm^{-3}; and finally a 40 nm-thick layer of GaN, doped with magnesium at a concentration of 1 x 10^{20} cm^{-3}. To provide a comparison, the team deposited an identical structure on sapphire, apart from the initial growth of heavily doped *n*-type GaN layer around 4 μm-thick, designed to trim current crowding in the quasi-vertical device.

Processing the epiwafers into devices began by adding a *p*-GaN ohmic contact, in the form of Ni/Au stripes, and then a thick layer of nickel (see Figure 9, which also details the processing steps). The addition of a mask followed, before etching



➤ Figure 11. Focussed-ion beam, scanning electron microscopy images (a), (b) and (c) of the trench of a GaN superjunction diode show that growth in just argon leads to coalescence of NiO at the top of the trenches. Growth with an argon-to oxygen ration of 20 to 1 avoided coalescence.



➤ Figure 12. The vertical super-junction device delivers a superior performance to one-dimensional equivalents.

created a mesa. Removal of this mask followed, prior to deposition of SiO_2 that surrounds the mesa. Pillars were then etched, and the sidewalls treated with tetramethylammonium hydroxide to improve surface quality. To compete device fabrication, the researchers added the anode and cathode, and filled the trenches with NiO.

Focussed-ion beam, scanning electron microscopy images of the trench region showed that the growth in just argon led to coalescence of NiO at the top of the trenches (see Figure 11). This does not take place in the other device, which is the only type that the team characterised with electrical measurements.

These investigations revealed a breakdown voltage of more than 1100 V for the superjunction diodes formed on both silicon and sapphire.

Benchmarking devices against other vertical GaN diodes, considering the blocking voltage and differential on-resistance, indicated that the team's device is amongst the best for GaN-on-GaN diodes. "If we look at the effective drift region thickness with breakdown voltage, you see that the gallium nitride super-junction compared with the one-dimensional devices allows for the more efficient utilisation of the epi-thickness to boost the breakdown voltage," commented Zhang (see Figure 12).

Zhang also compared the performance of his team's superjunction device with those made from silicon and SiC, pointing out that despite the wider pillar width, the GaN device has a much lower specific on-resistance. "This suggests a good potential for out-performing the silicon carbide superjunction with a further scaling of the pillar width."

Efforts such as this, and the other breakthroughs reported in GaN at IEDM, suggest that the performance of commercial GaN devices will continue to improve. This should help to drive up sales of GaN power devices and increase the reach of this material system throughout our world.

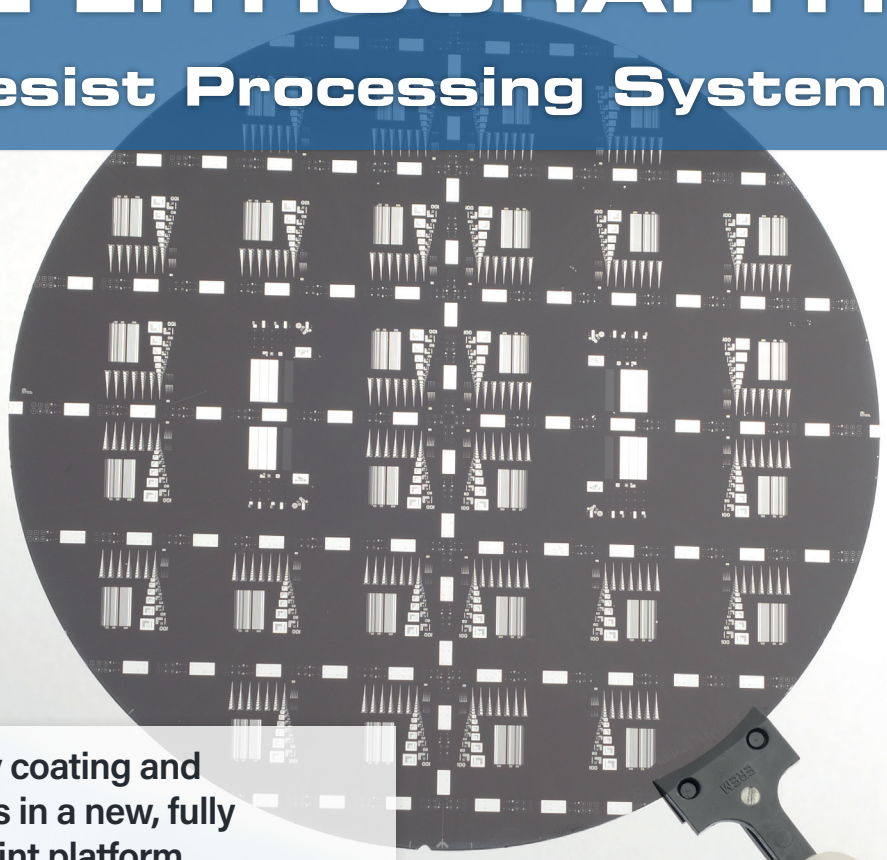
EVG®

invent
innovate
implement

www.EVGroup.com

NEXT-GENERATION OPTICAL LITHOGRAPHY

EVG®150 Resist Processing System



- Automated spin / spray coating and development processes in a new, fully modular, smaller footprint platform.
- Outstanding throughput for HVM processes using a high-speed, high-accuracy robot and advanced scheduler algorithms.
- Guarantees highly uniform coats ranging from demanding thick resist applications down to sub-micron layers.

EVG® 150 (200 mm)

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

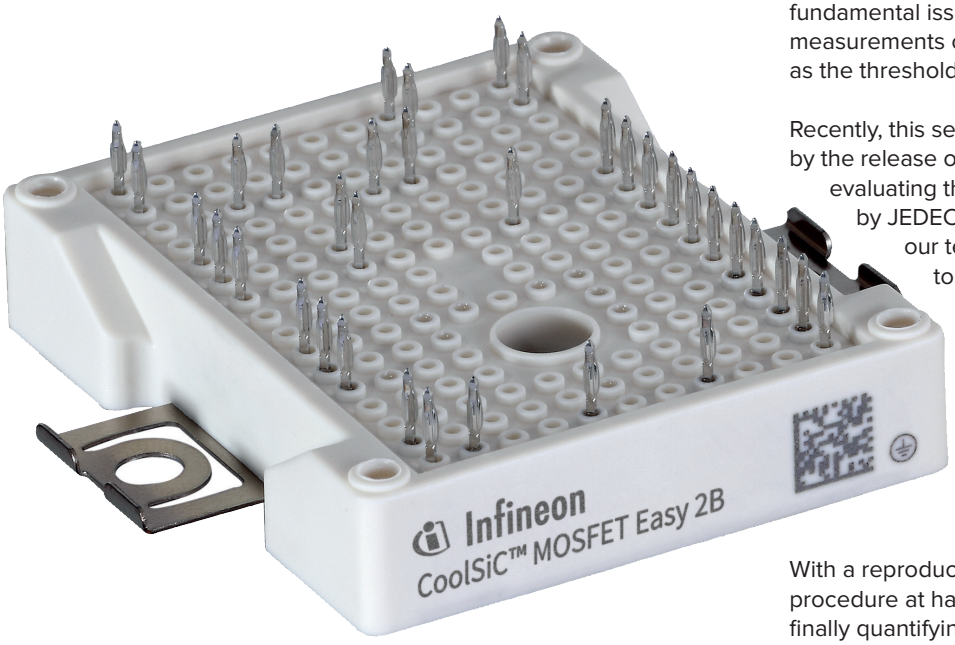
Controlling threshold voltage instabilities in SiC MOSFETs

System designers can now benefit from new test and stress procedures for SiC MOSFETs that realistically determine their worst-case threshold voltage variations

BY THOMAS AICHINGER FROM INFINEON TECHNOLOGIES

ONE OF THE GREATEST strengths of the SiC power MOSFET over its silicon-based equivalent is its capability to operate at much higher switching frequencies and lower losses. Thanks to this, engineers can build advanced power electronic circuits that feature smaller cooling units and smaller passive components. These gains are so highly valued that as well as opening up new applications, they are enabling SiC MOSFETs to replace silicon counterparts in existing applications, where new ground is being broken for lighter, more efficient system design.

When engineers design circuits with SiC components, they expect that as well as exploiting the performance benefits, they will not be held back by any compromise in quality compared with silicon counterparts. There is an expectation from these engineers of a predictable electrical parameter stability over lifetime.



Unfortunately, until fairly recently the initial general impressions of these engineers had been that SiC technologies are not quite there. There were concerns, for instance, regarding so-far-unknown threshold voltage (V_{TH}) peculiarities, and their extraordinary electrical parameter drifts during reliability investigations. Scientific papers had shown large V_{TH} variations within short periods of stress, raising concerns that critical electrical parameters of SiC MOSFETs were highly variable, threatening to get out of control during operation in the field, sooner or later.

Until recently, the origin and the application relevance of these short-term V_{TH} instabilities in SiC MOSFETs had not been fully understood, with literature reporting a wide range of parameter variations. Various possible reasons have been proposed. One is that first-generation products had varied levels of quality; and a second is that fundamental issues hampered stable, reproducible measurements of crucial electrical parameters, such as the threshold voltage.

Recently, this second issue has been addressed by the release of new measurement guidelines for evaluating the V_{TH} in SiC MOSFETs, published by JEDEC and drawing on contributions from our team at Infineon. We have gone on to develop a deeper understanding of the trapping dynamics at the metal-oxide semiconductor (MOS) interface. Outlined in this first section of this article, this insight has helped us to adapt V_{TH} measurement routines so that they resolve the issue of undefined and non-reproducible measurements.

With a reproducible and reliable V_{TH} measurement procedure at hand, we have made further strides, finally quantifying the effect of electrical stress on

the condition of a device in a standardised way. This has been most valuable in dispelling major doubts surrounding the overall stability and controllability of SiC MOSFET technology. Our findings include the revelation that the mysterious short-term V_{TH} variations are fully reversible and recur in every single switching cycle. Note that this effect, found in all SiC MOSFETs in the market and already present in pristine devices, is not a cause for alarm: it is an inherent device characteristic, rather than a reliability-critical degradation mechanism.

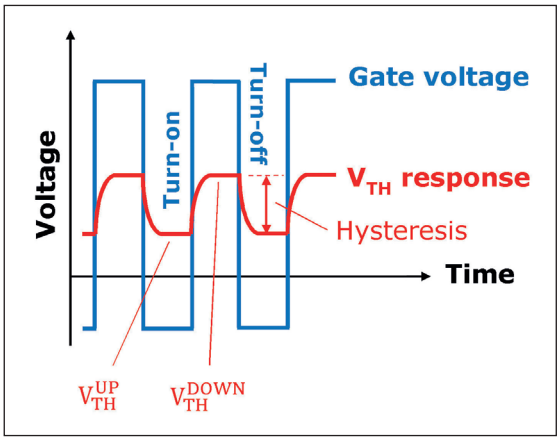
Our next important step has been to discover how to stress SiC devices in the most realistic way, so that we can determine worst-case V_{TH} variations after the MOSFET has been used in an application for its intended lifetime. Historically, the approach that's been applied to silicon power MOSFETs to check for systematic V_{TH} variations is to raise these devices to an elevated temperature and perform static stress tests at a constant positive or negative gate bias. For high-temperature gate-bias tests, one would tend to select a stress temperature and bias higher than the use conditions, in order to cover the chip's entire lifetime within a 1000-hour (typical) qualification test. The result produced by this test has always been considered to be the worst-case scenario. It has been assumed that a common alternative – the more application-near, gate-switching stress test – is less critical, because it may involve some compensating drift effects and recovery phases in between. We question that assumption with work showing that these factors do not apply to SiC MOSFETs. These findings are described in the second section of this article, along with our completely new stress procedure.

Threshold voltage peculiarities

A stable and reproducible measurement of V_{TH} is important. It's needed to define the datasheet values of pristine devices and it's mandatory for assessing V_{TH} evolution in a stress experiment. In silicon MOSFETs this task is straightforward – it does not require any particular precaution. Pristine silicon power transistors always show the same V_{TH}.

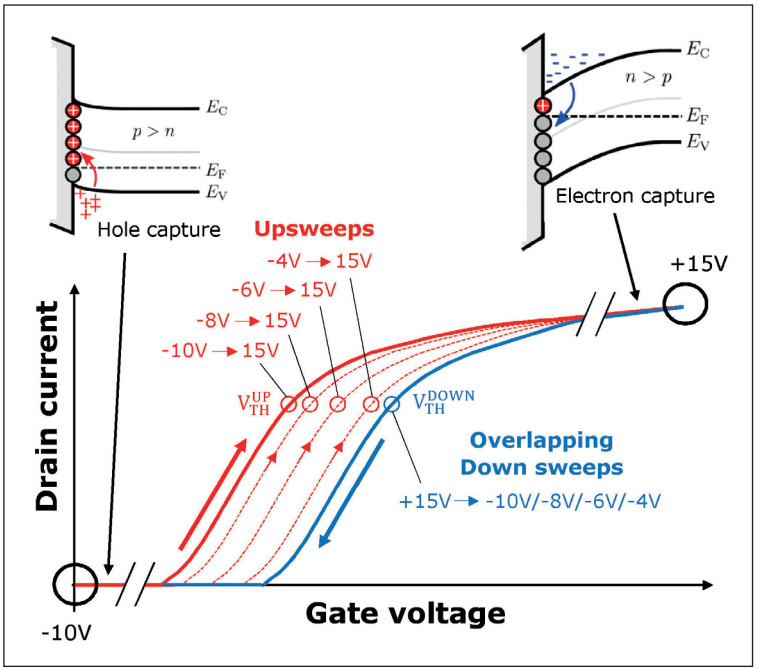
That's not the case, though, in SiC MOSFETs, which have a V_{TH} that's not constant. According to our measurements, the V_{TH} shows different values when the transistor turns on, coming from a negative gate voltage; and when it turns off, coming from a positive gate voltage (see Figure 1). This indicates that there's a need to define the V_{TH} hysteresis: it is the difference between the V_{TH} during turn-on, the so-called upsweep V_{TH} (V_{TH}^{UP}); and V_{TH} during turn-off, the so-called down sweep V_{TH} (V_{TH}^{DOWN}).

Hysteresis is at its largest when sweeping the gate between deep accumulation and deep inversion, for example, between -10 V and +15 V (this is illustrated in Figure 2, which shows typical transfer characteristics of SiC MOSFETs for fast upsweeps and downsweeps of the gate voltage). Hysteresis reduces when the upsweep starts at voltages closer to 0 V, and when sweeping is slower.

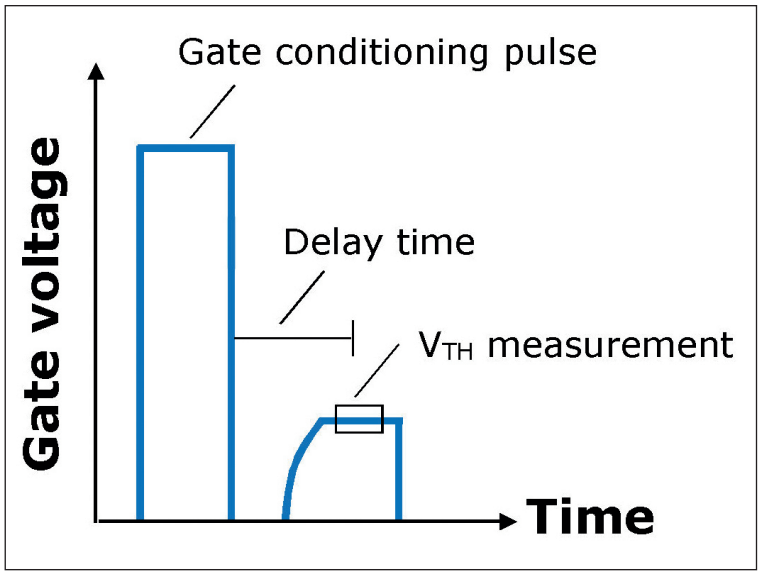


➤ Figure 1. An illustration of threshold voltage dynamics of a SiC MOSFET when switching the gate of a pristine SiC MOSFET in bipolar mode.

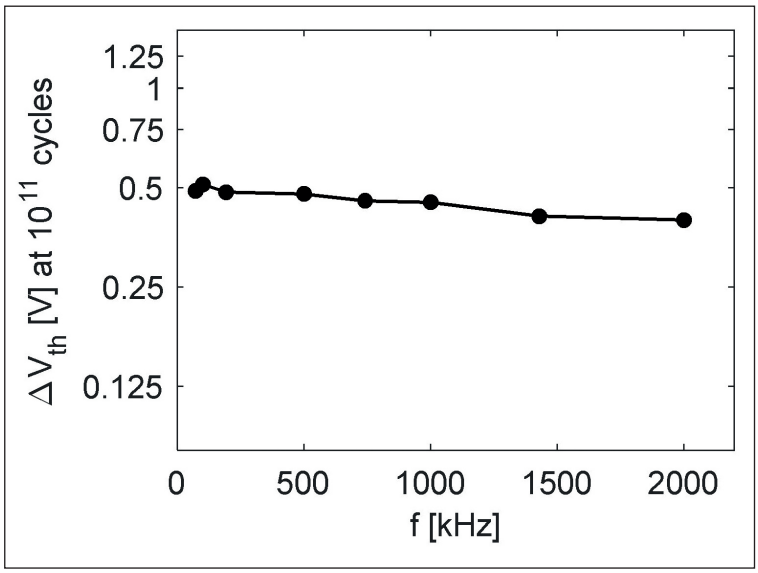
Our investigations suggest that these effects are due to short-term charging and discharging of pre-existing traps located near to or directly at the SiC/gate-oxide interface. We have determined that the upsweep V_{TH} is always lower, because the interface is charged positively in the negative half period of the gate pulse, due to holes captured from the valance band. Meanwhile, the down sweep V_{TH} is always larger, because the interface is charged neutrally or even negatively in the positive half period of the gate pulse, due to electrons captured from the conduction band. There is actually a continuum of possible V_{TH} values within the



➤ Figure 2. Transfer characteristics vary during turn-on and turn-off. V_{TH} is lower during turn-on due to holes captured at negative gate bias. During turn-off, V_{TH} is higher due to electrons captured at positive gate bias. Hysteresis reduces when the upsweep starts at gate voltage levels closer to 0 V, because fewer holes are trapped during the negative gate voltage period.



➤ Figure 3. An example of gate conditioning. Before measuring the V_{TH}, a positive gate pulse is applied for several milliseconds to bring the MOS interface to a defined charged state. Afterwards, a V_{TH} spot measurement is performed using, for instance, a gated-diode biasing scheme. To ensure reproducible results, there must be a constant time delay between the conditioning pulse and the V_{TH} measurement.



➤ Figure 4. An exemplary threshold voltage drift after 10^{11} switching cycles, using stress frequencies between 70 kHz and 2 MHz. The resulting V_{TH} drift after the same number of switching cycles is virtually identical despite the different total stress times.

hysteresis envelope, arising from the large variety of capture and emission time constants for trapped charges in the virtually continuous defect band.

One consequence of these findings is that the 'gate biasing history' of the MOSFET can impact V_{TH} measurements for a very long time. For instance, when the device is either floating, or biased at V_{GS} = 0 V after the application of a positive or negative gate pulse, charges that are trapped near the mid-gap may be 'stored' at the interface for hours, days or even longer – this keeps the device in a state of non-equilibrium. This is a consequence of large thermal emission barriers, associated with the large bandgap of SiC. There's no similar effect in silicon MOSFETs, because they have a lower density of interface traps and a narrower band gap.

Based on these findings, we knew that the key to accomplishing a reproducible V_{TH} measurement with a SiC MOSFET was to begin by defining a 'gate biasing history'. One option is to apply a short positive gate pulse to the device, using gate voltages between the recommended use voltage and the maximum allowed voltage in the datasheet (see Figure 3). We call this technique gate conditioning. Once undertaken, V_{TH} must be measured with a constant time delay.

An easy way to accomplish fast, well-timed V_{TH} spot measurements is to use a gated-diode measurement scheme. Here, the gate and drain terminals of the device are shorted, the source terminal grounded, and a threshold current, for example 1 mA, forced. Eventually, this gate conditioning procedure creates a defined, reproducible charge state at the SiC/gate-oxide interface, and enables a defined, reproducible V_{TH} measurement. Our own research that is consistent with recent guidelines published by JEDEC has shown that more complex conditioning procedures, involving negative and positive gate conditioning pulses, also allow for reproducible measurements of hysteresis.

Having crossed the hurdle of measuring V_{TH} in an accurate and reproducible manner, we took on the next challenge: controlling and assessing V_{TH} instabilities in SiC MOSFET operations, by developing a stress procedure for determining worst-case V_{TH} drifts for different application profiles.

Worst-case threshold voltage drifts

Quality is the ability to deliver what is promised. It follows that to realise the highest quality levels and secure reliable operation of SiC MOSFETs in different applications and/or mission profiles, it is crucial to know the worst-case change in V_{TH} and other related electrical parameters over lifetime. Armed with such insight, system design engineers can consider potential variations in electrical parameters.

The most direct way to determine the variation in electrical parameters during real operation is to run full application tests and measure the condition of devices within their specified lifetimes. However, this is impractical in most cases. That's because it would be too time consuming to come to a final result, and the variety of possible applications would be far too large to be checked in individual long-lasting application tests.

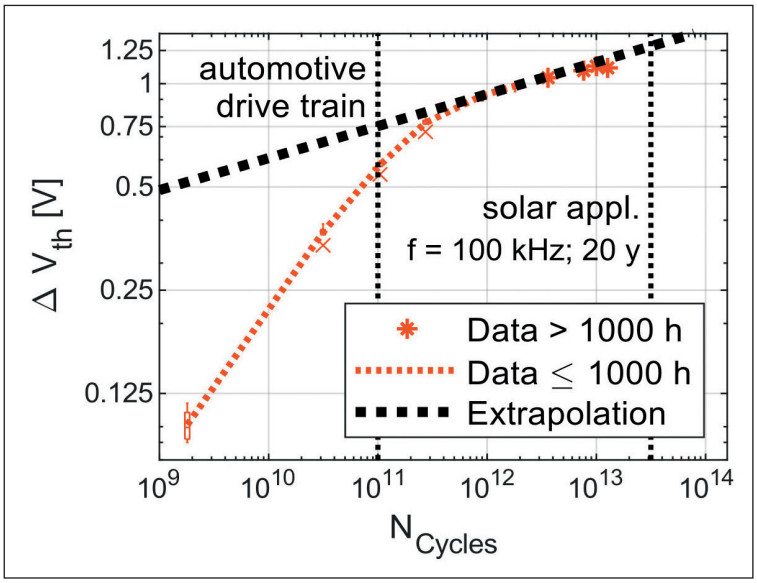
To ensure quality management while employing a practical approach, best practice is to select worst-case stress conditions and strive for stress procedures that are simplified but do not alter the degradation mechanism of interest. One of the merits of this is that all allowed application conditions are covered by one stress test. There may also be an opportunity to turn to simplified stress procedures, which might offer some potential for acceleration and parallelization.

Another way to look at this is that the ideal stress procedure should encompass all important stressors addressing a certain application-relevant degradation mechanism, but at the same time be devoid of application conditions that do not impact the final drift result, or hinder upscaling of sample size and acceleration of stress. To uncover such a unified stress procedure, we have found that it's been useful to look at common aspects of different SiC MOSFET applications and identify the main stressors.

When SiC MOSFETs are used in switching applications, they are typically running at frequencies between 5 kHz and 500 kHz. As well as fast switching, there is often the need for a wide and flexible gate drive operation window, including margins for overshoots, undershoots, and negative gate turn-off voltages to allow safe turn-off. Due to this, over the lifetime of a SiC MOSFET, it is often exposed to a large number of bipolar gate switching events.

Based on the typical characteristics for a SiC MOSFET, it is expedient to stress this device in pulsed gate mode rather than DC mode when aiming to trigger the same degradation mechanisms that determine V_{TH} instabilities in this transistor, when it's deployed in real applications. Underlining this point are recent discoveries by our team, and also academic researchers working independently in China, that SiC MOSFETs show different and even enhanced parameter instabilities under bipolar gate switching conditions compared with static gate stress. This mechanism is called the gate switching instability.

Another key finding from this body of work is that for any given gate switching condition, the resultant threshold voltage drift depends predominantly on the number of gate switching events (see Figure 4). Consistent with our findings, a team in China has later independently confirmed that the total stress time and the frequency of the duty cycle is of minor or even of no importance. Drawing on this finding, it has been revealed that it is possible to determine the time evolution of V_{TH}, for a given application profile, by simply stressing devices up to their maximum number of gate switching cycles. We have shown that this can be accomplished using elevated stress frequencies of up to 2 MHz for acceleration.



➤ Figure 5. Example of worst-case V_{TH} drift evolution curve due to gate switching stress. This measurement has been made at the maximum data sheet conditions and 500 kHz. The bold dashed line (black) indicates the power law fit of data points in the saturation regime, but within 1000 hours of total stress time, corresponding to around 2 x 10^{12} cycles. Additional data points recorded up to 7000 hours of stress time (> 10^{13} cycles) confirm the validity of the power law fit.

To cover all possible applications, devices must be stressed to their worst-case conditions, using the most critical operating conditions allowed in the datasheet. This means using $V_{GS,max}$ and $V_{GS,min}$. Taking this approach also exposes overshoots and undershoots in the gate signal that may occur in the application and influence gate switching instability.

We have found that devices from different manufacturers behave differently when stressed at different temperatures. Some SiC MOSFETs drift more at lower temperatures while others drift more at higher temperatures. Due to these variations, it is far from obvious which temperature is really the worst-case for devices from different manufactures.

Through collaborative efforts, we have tested two more potentially application-relevant stressors: the drain voltage and the load current. This study revealed that neither led to altered V_{TH} instabilities. It's a negative result that is extremely beneficial, because it allows a drastic simplification of the stress procedure without neglecting any important V_{TH} stressor present in real applications.

Using a stress frequency of 500 kHz and maximum data sheet conditions for gate voltage and temperature, we have undertaken measurements that led to the plotting of an exemplary V_{TH} drift evolution curve (see Figure 5). The total stress time is 7000 hours, with stress interrupted multiple times to record the V_{TH} using the gate conditioning approach described previously. The slope of this V_{TH} drift evolution curve is higher for fewer switching cycles (< 10^{11} cycles), and tends to saturate when exceeding 10^{11} – 10^{12} switching cycles.

To assess the worst-case drift at the end of an arbitrary application profile, one must calculate the total number of gate-switching events, before either interpolating or extrapolating the V_{TH} drift evolution curve. This curve can also be used to calculate variations in other related electrical parameters, such as the on-resistance. In that case, it's worth noting that changes in V_{TH} predominantly affect the channel resistance as a component of the total on-resistance of a power device. Other components of resistance, such as those associated with the JFET, the drift zone and the substrate, are not affected by V_{TH} instabilities.

In application notes, our company has published parameter drift evolution curves that are similar to those shown in Figure 5. Drawing on this information, our customers are able to directly extract the maximum drift that can be expected for a given technology during a specific application. For instance, for automotive drive applications, the total number of switching cycles until the end-of-application profile is relatively low, typically around 10^{11} cycles. This allows the maximum V_{TH} drift to be directly read from raw data, shown in Figure 5.

However, for solar applications, which feature operation under frequencies of typically 70–100 kHz during daylight hours for 20 years or more, data must be extrapolated, because a real end-of-application profile test would lead to an unreasonably long stress time. The curve to be used for this power law extrapolation is shown in Figure 5.

In short, drawing on our efforts to increase our understanding of trapping dynamics at the SiC/gate-oxide interface, we have gone on to develop new characterisation and stress procedures that are tailored to the characteristics of the SiC MOSFET.

These new methods provide standardized, reproducible measurements, as well as realistic assessments of time-dependent parameter variations in real applications. In turn, this allows engineers to predict how device characteristics will evolve during an application, and paves the way for SiC MOSFETs to reach their next level of quality excellence.

FURTHER READING

- T. Aichinger *et al*. "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs" Microelectron. Reliab. **80** 68 (2018)
- K. Puschkarsky *et al*. "Understanding BTI in SiC MOSFETs and Its Impact on Circuit Operation," IEEE Trans. Device Mater. Reliab. **18** 144 (2018)
- JAP183, "Guidelines for measuring the threshold voltage (VT) of SiC MOSFETs", www.jedec.org
- JAP184, "Guideline for Evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion", www.jedec.org
- P. Salmen *et al*. "A new test procedure to realistically estimate end-of-life electrical parameter stability of SiC MOSFETs in switching operation", IEEE International Reliability Physics Symposium (IRPS) (2021)
- H. Jiang *et al*. "Dynamic gate stress induced threshold voltage drift of silicon carbide MOSFET", IEEE Electron Dev. Lett. **41** 1284 (2020)
- X. Zhong *et al*. "Bias Temperature Instability of Silicon Carbide Power MOSFET Under AC Gate Stresses," IEEE Trans. Power Electron. **37** 1998 (2022)
- M.W. Feil *et al*. "On the Frequency Dependence of the Gate Switching Instability in Silicon Carbide MOSFETs", Proceedings ICSCRM, Davos, 2022
- M. Sievers *et al*, "Monitoring of parameter stability of SiC MOSFETs in real application tests", Microelectron. Reliab. **114** 113731 (2020)
- Infineon Application Note 2018-09

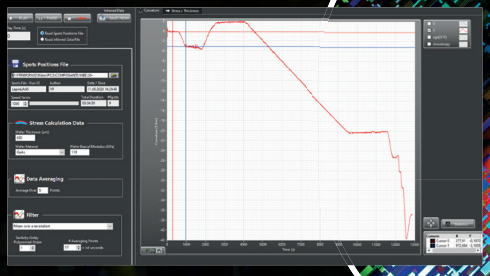
Solutions for Compound **semiconductor epitaxy**

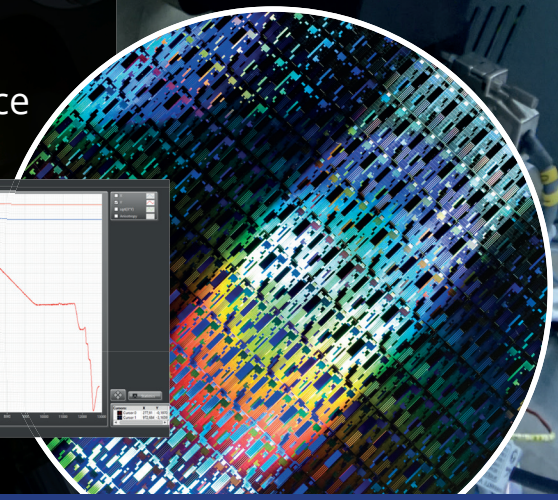
In situ real time curvature

RIBER
EZ-CURVE®

Tool for process monitoring: yield enhancer

- In situ measurements of bow, stress and curvature
- Real time detection of growth events
- Comparison with reference curve





RIBER

INNOVATIVE SOLUTIONS FOR SEMICONDUCTOR INDUSTRY

info@riber.com
www.riber.com

ANGELTECH
CS INTERNATIONAL CONFERENCE

18-19 April 2023

Join us in Brussels at CS International to hear from more than 40 influential innovators

The 13th CS International Conference building on the strengths of its predecessors, will bring 40 leaders from industry and academia delivering presentations that fall within five key themes:

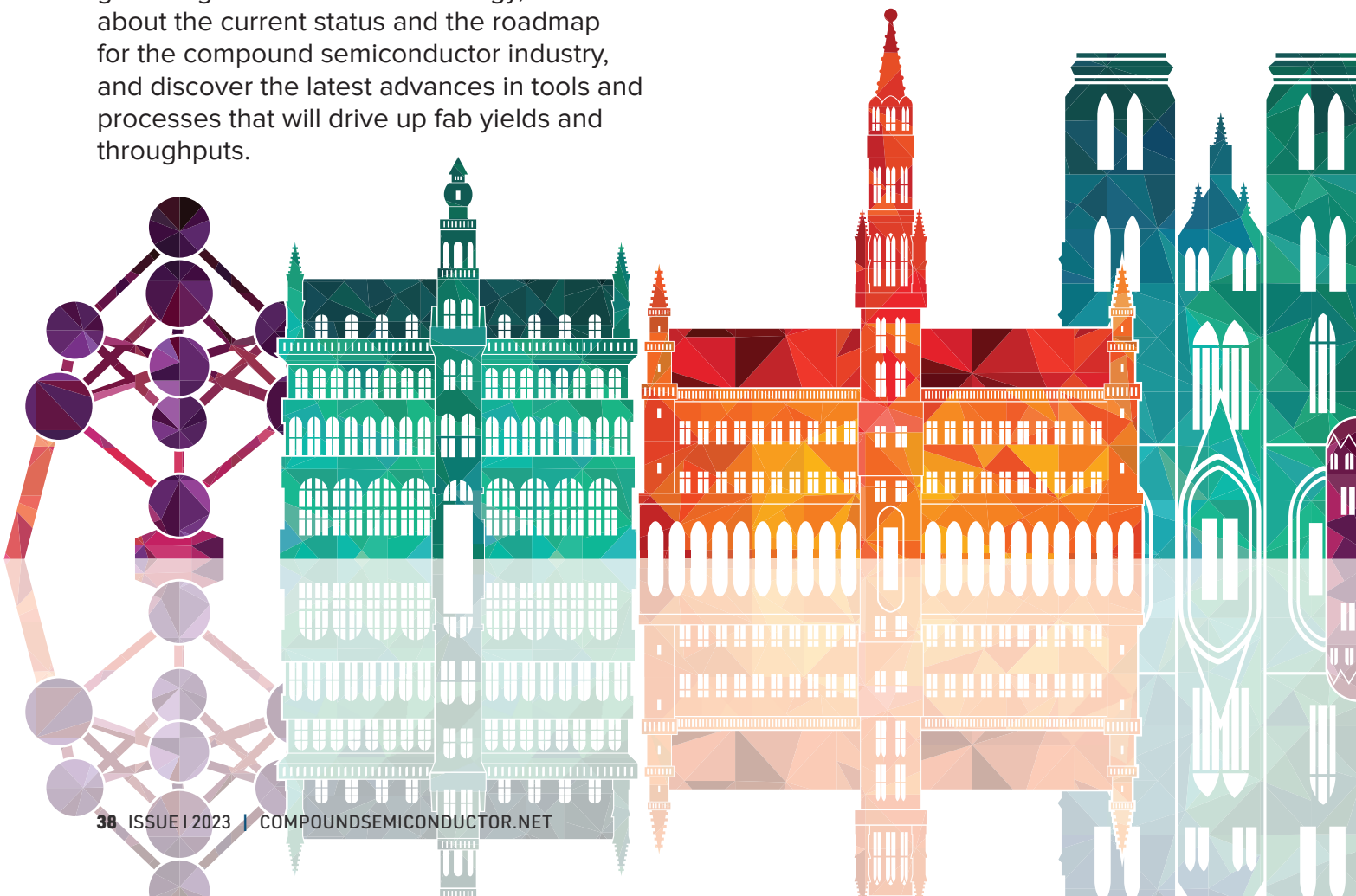
- Ultrafast Communication
- Making Headway with the MicroLED
- Taking the Power from Silicon
- New Vectors for the VCSEL
- Ultra-wide Bandgap Devices

Delegates attending these sessions will gain insight into device technology, find out about the current status and the roadmap for the compound semiconductor industry, and discover the latest advances in tools and processes that will drive up fab yields and throughputs.

Attendees at this two-day conference will also get the opportunity to meet many other key players within the community.

Registration to **AngelTech** allows you to access both days of **CS International** and the co-located **PIC International** and **Power Electronics International**.

Contact to speak, sponsor or attend:
https://csinternational.net/contact



2023 Sponsors so far include:

AIXTRON
ANNEALSYS
APPLIED MATERIALS make possible
BelGaN
BRUKER
C&D SEMICONDUCTOR SERVICES, INC.
CS connected
DISCO
ELEMENT 3 5
EPIC EUROPEAN PHOTONICS INDUSTRY CONSORTIUM
evatec process systems
EVG
FerroTec
FORGE NANO
HARDINGE
htt GROUP.
KLA
GO Photonics
Lam RESEARCH
LAYTEC MEMBER OF THE NYNOMIC GROUP
Masimo SEMICONDUCTOR
nanotronics
onto innovation
Optiwave
OXFORD INSTRUMENTS
Panasonic CONNECT
PFL
RIBER
SEMILAB
soitec
SENTECH
ThermoFisher SCIENTIFIC
umicore
Veeco
vistec Electron Beam
YES
YOLE Group

A national treasure: The UK's central growth facility

Director of the UK's national epitaxial facility, Jon Heffernan, discusses its remit, its proficiencies and its contributions to the research and development of compound semiconductor materials and devices

INTERVIEW BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

RS: *Why and when was the national facility founded?*

JH: It started in 1979, so we've been going for over 40 years. The purpose of the facility is to provide epitaxial materials to researchers across the UK, primarily for UK-funded research grants, but we do work with industries as well.

The idea is that there are many people doing semiconductor research in the UK, but they don't all have epitaxy facilities. Epitaxy is an expensive technique and it requires significant experience to operate at the highest level and produce semiconductors of the highest quality. Therefore, the EPSRC [Engineering and Physical Sciences Research Council] have funded this facility for many years. It's part of a network of national research facilities – there are about ten of them – that are centres of excellence.

We're renewed on a five-year basis. As part of the renewal, there's what's called statement-of-need consultations. We go and speak to the community in the UK and ask them what they need from a facility like this. We draw that together, and then it is reviewed by the EPSRC. There's a competitive call for somebody to run a facility like this and to deliver what the community needs. So we're very much integrated with what the community is looking for.

➤ Left: One recent addition to the EPSRC National Epitaxial Facility is an MBE tool from DCA Instruments. Credit: Sort of Films.

RS: *The facility is more than just the capabilities in Sheffield?*

JH: We have two partner universities, Cambridge and UCL. The partners provide specialised materials. We provide a broad range of III-V materials: arsenides, phosphides, antimonides; Cambridge provides gallium nitride material; and UCL provide group IVs and III-Vs-on-silicon.

We also have a pump priming facility, to provide a small amount of initial material to help in supporting grant proposals. In particular we want to support new lecturers. This will help them get their first grants.

We're now expanding materials to a much wider range, such as 2D materials, gallium oxide. It's not something that Sheffield could specifically do on its own, because to explore all of these new materials would require many more new reactors, or would require potentially incompatible materials on an existing reactor.

RS: *What are some of the biggest highlights over the years?*

JH: We've tracked and supported the growth of many different technological areas. We're strongly involved in work on lasers for telecommunications and the internet.

Quantum Technologies is a very big area globally and a big focus in the UK, with the National Quantum Technology Programme. Sheffield has been pioneering many aspects of semiconductor quantum photonics over the last 20 years or so. We have been at the forefront of developing quantum dots to the point where they can be used in quantum technology applications. We have produced some very pioneering results with Toshiba, using quantum-dot-based entangled-photon emitters for quantum communications. We've also recently spun out of Sheffield a company working on single-photon sources called Aegiq.

Another interesting emerging area is environmental sensing; in particular using devices in the mid-infrared, including lasers. These types of lasers, particularly quantum cascade lasers, are very challenging to produce. Sheffield was the first group in the world to demonstrate the growth of these type of quantum cascade lasers by MOCVD. That's quite a big breakthrough in terms of making these types of devices for industrial applications.

We've got a number of large projects looking at applications for mid-infrared spectroscopy, using both lasers and detectors. We're core partners in the EPSRC Future Photonics Manufacturing Hub with the University of Southampton. Funded by EPSRC, it has over 40 companies working with us. Again, we've been looking at the manufacturability of devices for mid-infrared applications.

Our partners have done very pioneering work in the growth of III-V lasers on silicon. They've demonstrated long lifetimes, compatible with commercialisation.

Cambridge has been working on gallium nitride for many years and has had many breakthroughs. Most recently, they've been working on a technology called porous gallium nitride. This is very interesting for display technology, for instance for virtual-reality displays. They've spun out a company called Porotech, which has attracted a lot of investment.

RS: *How much time do you spend working for academia, and how much time for industry?*

JH: It's difficult to say what the split is as it has varied over the years. I might say about 20 percent industry, 80 percent academia.

Our primary function is to support academic research. The way it works is that somebody applies for a grant to the EPSRC, and if they don't have their own epitaxy facilities, they come to us and discuss their needs. If the grant is funded, we will supply the epitaxy into that grant.

We work with industry because essentially the capacity of the facility is not taken up entirely with academic research. We also have a remit to work with industry, because of the impact agenda. It's very important for the UK that publicly funded research does have impact, and that means an impact on the existing industrial sector or starting new companies.

RS: *Epitaxial growth technologies are getting more mature, and the systems are getting easier to use. So is the case for a central facility diminishing?*

JH: Definitely not. It's actually the opposite.

At the moment the UK government is looking very closely at investing in the semiconductor industry, and has been consulting very widely over the last year and a half, including with us. It's now clear to many governments how important semiconductors are – that's been highlighted by supply chain problems and various geopolitical problems. The US government has just announced the CHIPS act, a $280 billion investment in semiconductor technology. Europe has got its own CHIPS act, and the UK government is expected to announce its intentions fairly soon.

It's been recognised that semiconductors are extremely important, from an economic impact point-of-view. Semiconductors in general, but III-Vs

in particular, are a gift that just keeps on giving. If you track the work that we've been doing over the last 40 years, you can see new technologies coming along all the time. There are so many physical properties we can exploit.

Epitaxy is not static, and not really very mature. It still remains very challenging, even classic III-Vs, like indium phosphide, gallium arsenide and the antimonides. We have a very strong expertise in antimonides, which are mainly grown by MBE. Antimonides by MOCVD for production is very immature, but we're developing it. There's a long way to go. There are still many areas in III-Vs and in group IV epitaxy where the field is almost completely open.

We continue to get people needing everything from us. EPSRC wouldn't fund us unless there was an actual demand. Also, if you look more broadly, what is happening in the semiconductor industry, demands and opportunities are just growing by the day.

RS: *There are some UK universities, such as Lancaster and Nottingham, that have their own epitaxial tools. For some areas of research – possibly detailed studies of esoteric heterostructures– does it make sense for a research group to have its own tool?*

JH: Definitely. The facility that we have is not meant to be the only epitaxy facility in the UK. The reason our facility is set up this way is because there are groups who have their own epitaxy and are pursuing new materials or pursuing epitaxial techniques.

Some of those universities will have invested a significant amount of money to pursue epitaxy. It is an expensive technique and there needs to be a real commitment to this.

➤ Two key members of the EPSRC National Epitaxial Facility in Sheffield are: Ian Farrer (left), Senior Lecturer in Semiconductor Epitaxy and Materials; and Edmund Clarke (right), Head of MBE Group. Credit: Laure Divisia.

If you're a researcher in another part of the UK and have an interesting idea for a new laser, for instance, it's actually difficult for you to go to universities and ask them to do that kind of work, especially on a supply basis. If you want to do that, you really need to collaborate with those groups, which means that you have to write joint grants, *et cetera*, and have to be properly involved in the epitaxy side.

The idea of the facility is that researchers can come to the facility and obtain epitaxial material as a research service. We obviously advise them and work with them on what they want to do, but they can obtain their material without needing to formulate long term collaborations, write joint grants, and be involved in the strategic agenda of the epitaxy itself. That's the value of the facility.

If you look at the numbers, you'll see that there are a lot of people interested in semiconductor devices across the UK. Those existing epitaxy groups are not able to cater for that demand, and certainly not able to provide a research service like we just described.

We have a very complementary role with the epitaxy groups in the UK. They're part of the community. We often help them, and we often advise them – and also people who want to work with them. What we described earlier, in terms of pump priming, is a good example. We've now got about six or seven groups that will provide material through the facility and pump priming. They could do that themselves, but the facility has got very good networks in the community. We've got long experience of how to manage effectively pump-priming activities that lead to good results.

RS: *Is this model of a central facility replicated in other countries?*

JH: No. There are probably a handful of big groups with multiple epitaxial tools for producing multiple materials. There's a few in the US, in places like Santa Barbara, and there's a few around Europe. But this model for epitaxy, in which we provide materials to a broad range of academics, that's unique.

We've got a steering group that has a number of international members. They are consistently saying that this model is very valuable. They've talked a lot about how they're interested in implementing it in their own countries. It is actually a very good model that the EPSRC has been running over many years.

RS: *Do you ever ship material overseas?*

JH: Sometimes. Again, it's the capacity question: do we have capacity to provide material outside of the core function? Generally speaking, we tend to work with UK companies on that front. We often have inquiries, most typically from Europe, and, for example, we've done some work for Fraunhofer in Germany. There's also a Fraunhofer in Strathclyde that we work with on some grants.

RS: *Could you explain how the facility is funded?*

JH: There's essentially a block grant from the EPSRC. We are funded on what's called an 80-20 model, which means that 80 percent of the funding is designed to fund the existence of the facility – the staff employed and keeping the facility available. The rest of the costs of the facility, the 20 percent, is provided through user grants.

It's actually a good model. It stimulates us to go out and work very closely with the community, in order to have users.

We're supporting a lot of grants. We typically work with around 25 universities across the UK. We are ISO9001 qualified. That helps us work very closely with industry.

RS: *The tools you have include those for MOCVD and MBE?*

JH: Yes. In Sheffield, we have three MBEs – we could call it four, because we've got one multi-chamber system – and three MOCVD reactors. Cambridge have two MOCVD reactors for nitrides, and UCL has three MBE reactors. So overall it is twelve reactors. We don't have HVPE.

RS: *Amongst those twelve, is there any material system you can't grow?*

JH: Our focus across the consortium is III-Vs and group IV. We can do basically all the III-Vs; in Sheffield we can do arsenides, phosphides, antimonides, and things like dilute nitrides and bismides – novel materials. Cambridge does gallium nitrides, that's the other III-Vs; UCL is doing the group IV materials. We don't do materials such as silicon carbide or gallium oxide, but these can be provided through our pump-priming partners. This also includes a whole range of 2D materials that you could explore.

Why don't we do those materials? One reason is that when we do the community consultation, most people are looking for the III-Vs or group IV. That's where the biggest need is. Of course, people are interested in other materials, and there are groups now growing them within the UK, but they are not at the point where it should be really provided through a facility model. New materials take a lot of effort. You end up going down a lot of blind alleys before you can make breakthroughs in materials, so it would be very difficult and very expensive for a central facility like ours to offer all kinds of new materials. Typically, you also need dedicated reactors, because you've got all kinds of material incompatibilities. Where would be the users to support those reactors?

We have had discussions with the community, the epitaxy groups involved, the EPSRC, and our steering group. In terms of new materials, the facility

Recent research highlights involving contributions from the UK's National Epitaxial Facility

- **"A prototype AlInP electron spectrometer", M.D.C. Whitaker *et al.* Planetary and Space Science 205 105584, (2021)**
  Development of a particle counting electron spectrometer using an AlInP photodiode, useful for space science missions where the instruments would be subject to high temperatures and intense radiation.

- **"Continuous-wave quantum dot photonic crystal lasers grown on on-axis Si (001)", T. Zhou *et al.* Nature Communications, 11 977 (2020)**
  III-V membrane photonic crystal lasers monolithically grown on CMOS-compatible on-axis silicon substrates, for applications in on-chip photonic networks.

- **"Quantum interface of an electron and a nuclear ensemble", D A Gangloff *et al.* Science 364 (2019)**
  Coherent manipulation of nuclear spins in a quantum dot, using interactions with an electron, forming the basis for development of an interface to a long-lived solid-state quantum memory.

- **"High Purcell factor generation of indistinguishable on-chip single photons". F Liu *et al.* Nature Nanotechnology 13 835 (2018)**
  Generating single photons with high indistinguishability by placing a quantum dot in a photonic crystal cavity that considerably shortens the radiative lifetime of carriers in the dot, enabling on-chip single photon sources with very high repetition rates.

- **"A quantum LED for the standard telecom window around 1550 nm", T. Müller *et al.* Nature Communications 9 862 (2018)**
  Demonstration of a light emitting diode emitting single photons and entangled photon pairs around the 1550 nm telecom window, for long-distance fibre-based quantum communications and cryptography.

- **"Wafer-scale Fabrication of Non-Polar Mesoporous GaN Distributed Bragg Reflectors via Electrochemical Porosification", T. Zhu *et al.* Scientific Reports 7 45344 (2017)**
  Demonstration of non-polar GaN distributed Bragg reflectors formed from layers of non-porous and porous GaN using a novel electrochemical porosification step that allows realisation of DBR structures on a wafer scale.

- **"Phase-locked indistinguishable photons with synthesized waveforms from a solid-state source" C. Matthiesen *et al.* Nature Commun. 4 1600 (2013)**
  Showing how the waveforms of indistinguishable single photons from a quantum dot may be controlled using resonance fluorescence techniques. Enables a variety of quantum technology applications.

Having the equipment is one thing. We've got 40 years' experience characterising materials as well. That's a big part of the facility.

has a role to play: to support the development of those new materials until they reach a point of maturity where there's enough users in the UK that may want the central facility for that.

For materials like gallium oxide, silicon carbide, or some of these II-VI materials, it may be that in five years' time there are so many people working on this technology within the UK that to deliver it through a central facility makes sense, both academically and financially. But we're not at that point with those materials. There's a risk of investing in a central facility to provide a huge range of materials, some of which there won't be the users to actually develop the research.

RS: *How do you characterise the material you ship?*

JH: We've got extensive characterisation facilities within each of the three organisations. There's a core set of characterisation techniques that are actually part of our ISO9001, which ensures that what we deliver meets the specifications of the user. For instance, we will always do X-ray measurements on material to check that the material quality is good. We always do Normarski to check that the surface quality is good. These are indications of whether the growth has worked or not. With optical devices, we will do the photoluminescence, because we need to see that light actually comes out. We have all kinds of characterisation techniques that we need for basic materials.

➤ While the EPSRC National Epitaxial Facility may be renowned for its growth via MBE, it also has MOCVD tools, including two Aixtron reactors. Credit: Zofia Bishop

What we don't have is some of the more advanced, specialised, expensive characterisation, like advanced transmission microscopy, for instance. But we outsource that kind of work.

Having the equipment is one thing. We've got 40 years' experience characterising materials as well. That's a big part of the facility. It's not just our epitaxy capability; it's our knowledge of materials and our knowledge of how to characterise and understand them that is very valuable. We often get users who have a fairly poor understanding of what they're asking for. People may want to combine materials, for instance, but they haven't even thought about lattice matching. So our knowledge of the materials is also very important for users.

RS: *How long does it take you to ship material?*

JH: It depends on the complexity of the material. We primarily support people on grants, so all of our work is peer reviewed. People come to us looking for material, we then supply them with essentially a quote, which goes on to their grant. We will provide the material if the grant is funded.

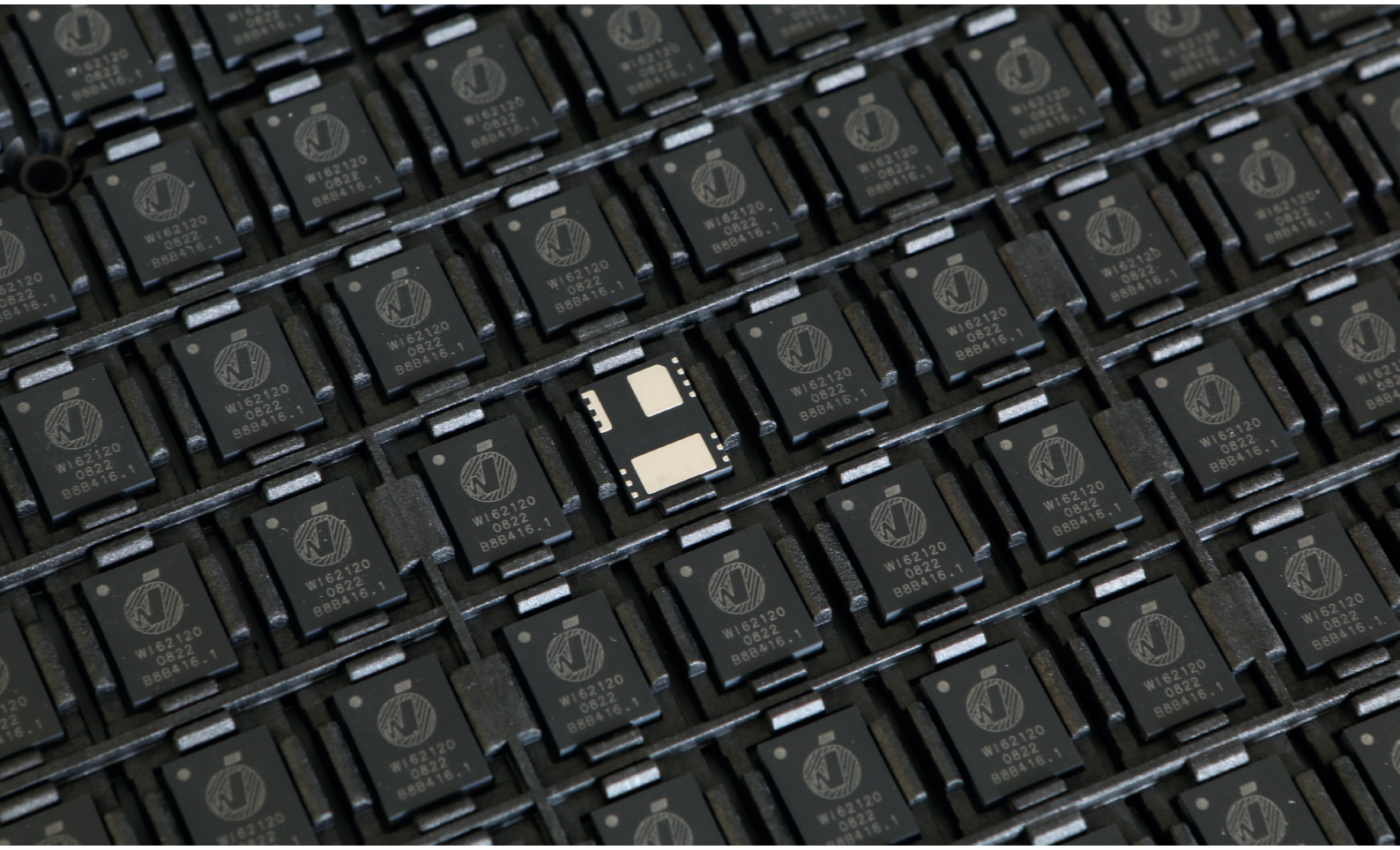
We're doing new research; we're not providing off-the-shelf material because that's not our role. If somebody looks for off-the-shelf material, we will encourage them to find commercial suppliers. Typically, we have to deliver requested wafers within a three-month period.

Some other projects are really pushing materials development or pushing the device concept. That can take longer, typically several iterative cycles. Although we're a research service, we effectively work collaboratively. Users need to work with us, understand the limitations, the constraints, *et cetera*. We will do quite a lot of characterisation before delivering the final product to the user.

RS: *For wafers that are used by industry, can you support up to prototype production?*

JH: We can, but our main constraint on that front is volume. We don't produce wafers in any kind of volume. We could, but it would take the capacity of the facility.

We can produce wafers up to a high TRL, if that's what you mean, in terms of prototyping. We have certainly produced lasers that have been used in the field, deployed in systems for various companies. But our primary role is to deliver to academic researchers.



Now's the time to commercialise the GaN IC

Power ICs that combine several power electronics functions in a single GaN chip are set to play a major role in worldwide electrification

BY GERALD AUGUSTONI, PLINIO BAU, DOMINIQUE BERGOGNE, FLORIAN COUVIN AND RYM HAMOUMOU FROM WISE INTEGRATION

POWER CONVERSION SYSTEMS are at the heart of most electronic equipment, from home appliances and laptops to data centres and electric vehicles. In some of these applications GaN technologies will soon be essential, because silicon has hit its physical limits as a power-conversion platform.

As well as increasing the efficiency of power conversion stages, GaN has other virtues. They stem from its great physical properties, such as: a bandgap of 3.2 eV, nearly three times that of silicon; and a breakdown field of 3.3 MV/cm, which is around ten times that of silicon. These strengths contribute to excellent values for both the on-resistance and the key figure of merit – the product of the on-resistance and the surface area of the chip. GaN devices can deliver high currents, a high breakdown voltage and a high switching frequency, and are competing with current MOSFETs and super junction MOSFETs in power applications operating at voltages of up to 650 V.

Traditionally, power designers build half-bridge circuits that serve in power conversion systems from discrete transistors and a number of external components, such as drivers, level shifters, sensors, bootstraps and peripherals. Improvements can be realised by combining discrete GaN devices, rather than those made from silicon, with other components. However, there is a better approach than this – one that we are pursuing at Wise Integration, which is based in France. Founded in 2020, our team is pioneering the GaN power IC, which combines several power electronics functions in a single GaN chip. Through integration, we are improving speed, efficiency, reliability and cost-effectiveness.

More agile adapters

Over the past decade, major OEMs have devoted much effort into making the most powerful smartphones, the thinnest notebooks and the largest TVs. The common factor in this trend is the growing demand for power, to enable sharing of a massive amount of data every second.

Unfortunately, OEMs have not been paying much attention to the adapters placed next to their products. This has resulted in bulky, heavy, inefficient power supplies that rely on silicon transistors. But that is starting to change.

Back in 2019, GaN technology penetrated the consumer market, initially in 30-100 W adapters. Since then this wide bandgap technology has spread widely, evolving as a next-generation power-conversion option. Today, most makers of mobile devices acknowledge that adapters are part of the equation, with mobility requiring them to be compact and lightweight, in tune with their main product strategy. Power supplies are now becoming an integral part of the product.

Power density is the main 'driver' for GaN, while efficiency is becoming increasingly important to meet new demand for AC-DC/DC-DC power supplies from 100 W to 3 kW, especially for the data-centre industry. For this specific market, higher power is required in the same form factor to reach high levels of efficiency.

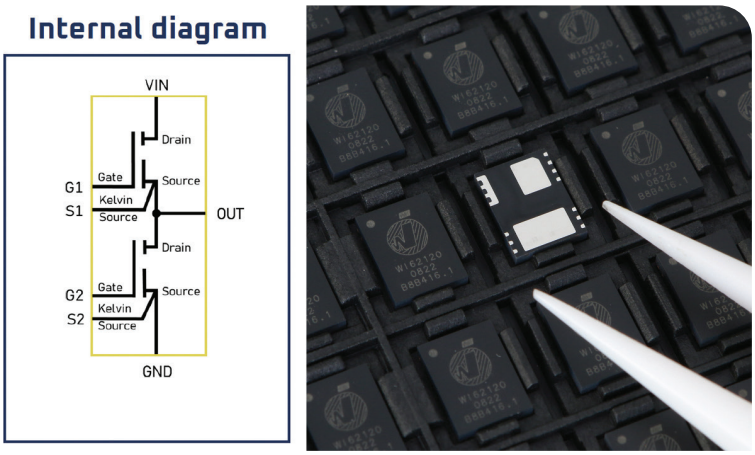
GaN had a great year in 2022. Along with its growing popularity it became cost competitive, with expanding demand prompting several global foundries to add GaN lines. At the system level, it will not be long before AC-DC analogue controllers are 'GaN compatible'. However, their GaN capabilities will not be fully utilised, because they are still switching at low frequencies.

Now is the time for the GaN industry to start overcoming this limitation and deliver the next big energy and power boost. This can come from a move from discrete GaN devices to GaN ICs that deliver a hike in efficiency at the system level, and lead to material costs that are more competitive than traditional silicon-based power supplies.

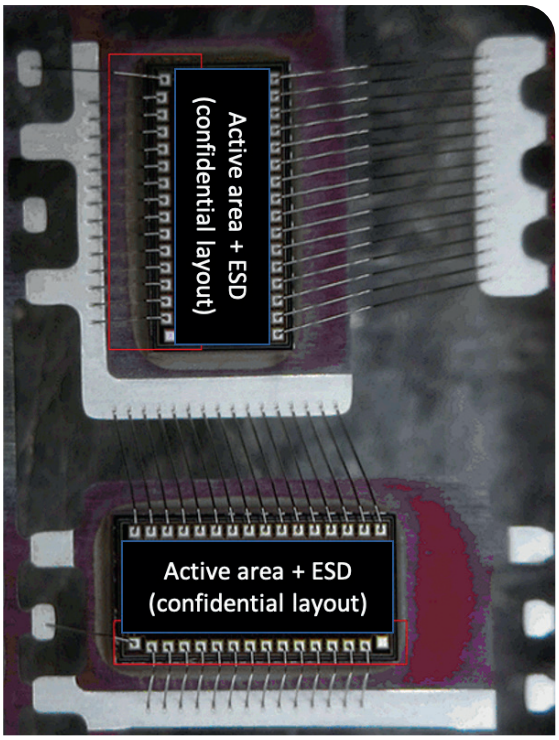
GaN IC design

To see this vision fulfilled, we have been prototyping different HEMTs, using different form-factor and metallisation strategies. Our efforts have involved the modelling and design of GaN transistors for 100 W to 1 kV applications using multi-project wafers. These investigations have drawn on expertise at CEA-Leti, the French microelectronics research institute. Through this collaboration we have obtained a solid basis for mass production.

Among all the multi-project wafers and prototypes we have built, we have undertaken R&D projects that are focused on power transistor layout topologies. From matrix metallisation to comb metallisation, we have uncovered parasitic contributions from the metal paths that affect performance parameters, leading to different values for parasitic capacitance, on-resistance and gate internal resistance. We have found that the pad positioning in the floorplan diagrams impacts the parasitic on-resistance caused by the bonding wires, as well as the distribution of current and metal resistance calculated by metal squares. Changing the bonding wires' position in the power IC floorplan impacts the final on-resistance in two ways: post-layout simulation and performance parameters change, due to variation in current distribution inside the metallisation; and the addition of bonding wires in parallel impacts the final resistance. Over the past two years we have built hundreds of prototypes, selecting the best ones. We have also performed electrostatic discharge (ESD) tests on: prototypes for different circuit strategies, circuits with diodes, digital input/output clamp and power clamp circuits.



➤ Figure 1. WiseGan half-bridge.



➤ Figure 2. Integrated half-bridge transistors composed of a low-side and a high-side power switch in the same package.

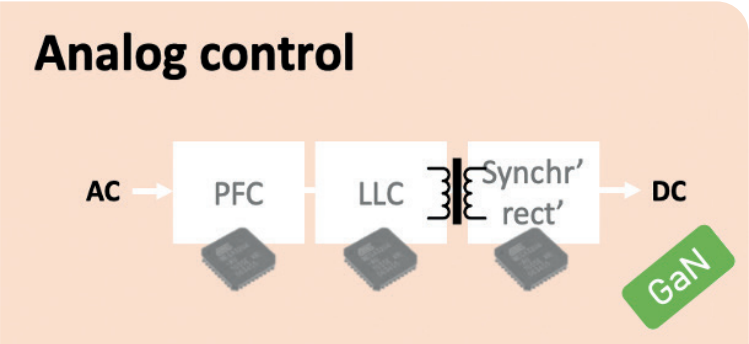


Figure 3. Typical GaN-based power supply with analogue control.

When our community gathers at international conferences, along with discussions of power transistors, there are conversations related to analogue circuits for GaN power integration. To obtain high-performance circuits, it is clear that there's a need to overcome fabrication-corner dispersion and a charge-trapping effect. Another impediment is the absence of *p*-type transistors for pull-up circuits. However, designers can overcome these challenges by adapting their circuit topologies. Many have demonstrated analogue circuit blocks, such as voltage reference, under-voltage lock-out, ESD circuits, comparators and operational amplifiers, with high switching frequencies of up to 10 MHz. These blocks are also compatible with voltages up to 650 V and powers of up to 1 kW.

System-level benefits

An entrenched factor that limits the performance of systems that employ silicon MOSFETs is the figure of merit for this transistor – it is the product of its on-resistance and the combination of its internal gate-to-source and gate-to-drain capacitance. Moving from silicon to GaN allows designers to enjoy a far better figure-of-merit. There's no longer a limit to the operating frequency, which can be ten times that of silicon.

However, it's not as simple as it first appears, as there's another obstacle to raising the system frequency. If the GaN transistor in the converter is not operating in a soft switching condition – that's the situation where the voltage at every turn-on of the transistor is close to zero, or otherwise limited – the energy stored due to the capacitance of transistor, as well as the system capacitance, has to be dissipated in GaN, causing the transistor to quickly overheat. While this may be acceptable for systems operating at 100 kHz or below, it is not for frequencies from 500 kHz to 2 MHz, the typical operating frequencies of our systems.

Our solution is to constantly operate in a soft switching condition, accomplished by specific control and topologies. To ensure that this is possible for everyone, we have launched WiseWare controllers (see Figure 4).

Driving forces

The GaN IC is destined to be the next step on the road to high power density and system integration, two of the key drivers behind the historical success of semiconductors. But power electronics, and power transistors in particular, have lagged in integration, held back by the complicated processes employed for forming vertical architectures.

We are in no doubt that the integration offered by our GaN lateral process will deliver benefits at the system level. Realising integration is a crucial step forward, as it always enables a reduction in system dimensions and an increase in complexity, which improves reliability and performance.

Our GaN ICs will bring benefits to market, because they enable: a shrinking of system dimensions, by reducing the number of components and minimising power losses, which leads to practical packaging for heat transfer; increased complexity, which can lead to optimised system performance, including better shaping of the power signal; improved reliability, thanks to fewer components on the board, and additional system protection that

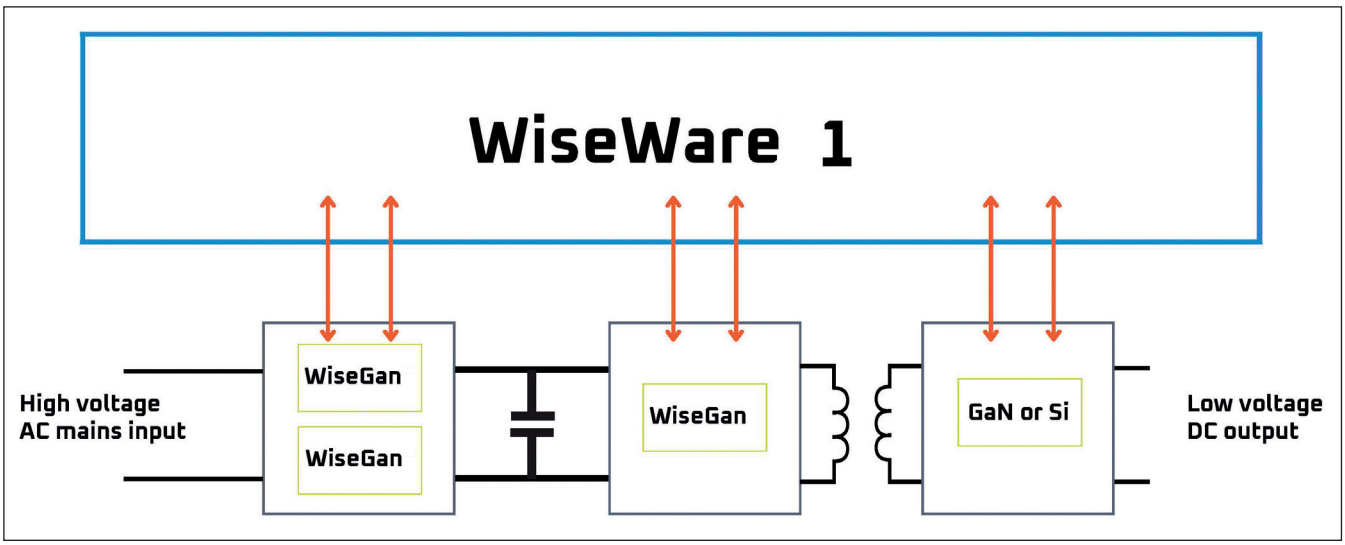
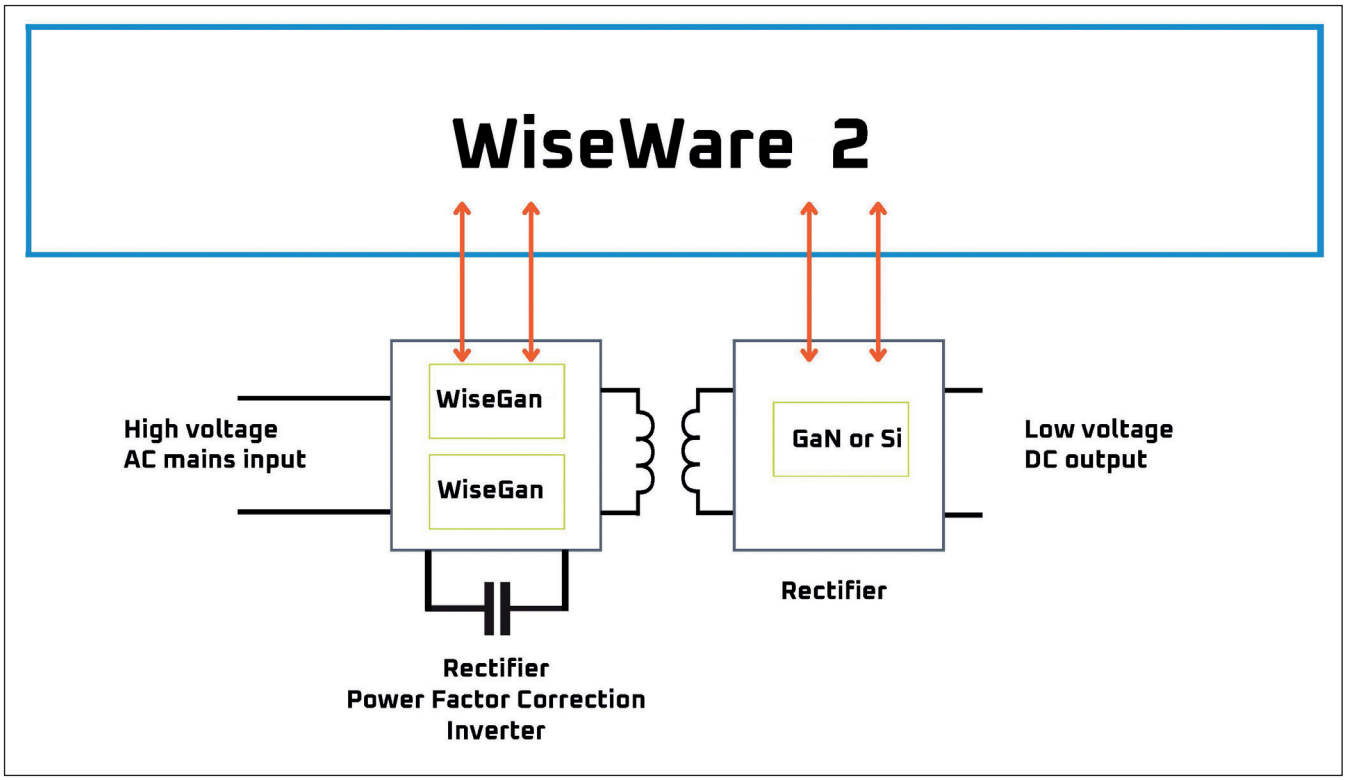


Figure 4. WiseWare 1 digital control.



➤ Figure 5: WiseWare 2 digital control.

includes early detection of abnormal conditions; and better performance with faster switching devices, thanks to driver integration. The latter enables a higher operating frequency, by reducing parasitic components and ensuring better switching behaviour. In addition, there is the opportunity to introduce 'in-power sensing', to feed the true status of the converter back to the controller through sensors integrated on the power transistor die.

Of course, this evolution requires several steps. However, such efforts are worthwhile, as they provide the main driving force to the future of the GaN market. While progress may span several decades, the result will be a revolution in system design, so that it delivers unmatched performance at low cost.

Digital control

Digital GaN is a promising option for realising great performance with GaN ICs. It is a disruptive approach to digital control. No longer are analogue signal blocks 'translated' into digital blocs, while the functions of the GaN IC and digital GaN controllers are partitioned in such a way that each part boosts the other part's performance. Current sensing is usually complex to achieve, but the digital GaN solution makes the analytical estimation of the current possible, thus creating a virtual current sensor. Such a sensor, which costs only lines of code, prevents losses, saves PCB area, reduces the bill of materials and eliminates analogue sensor problems (see Figure 5).

Another advantage of digital GaN is that it elevates high resolution pulse-width modulation to a level that cannot be reached with analogue controllers. By opening up the opportunity for a precise sub-nanosecond timing resolution, combined with high-performance microcontroller units (MCU), new solutions are introduced for zero-voltage switching – this is a technique that reaches extreme high switching frequencies without increasing switching losses, thanks to what is called 'soft switching'. By computing exact switching times, a digital GaN controller can perform zero-voltage switching using

Digital GaN is a promising option for realising great performance with GaN ICs. It is a disruptive approach to digital control. No longer are analogue signal blocks 'translated' into digital blocs, while the functions of the GaN IC and digital GaN controllers are partitioned in such a way that each part boosts the other part's performance

low-bandwidth hungry sensors and a model of the switching device.

Note that the high-frequency, switched-voltage waveforms are not measured or sensed. Instead, slow-changing variables are fed to the MCU analogue-to-digital conversion peripheral.

Digital GaN opens new pathways from the power stage to the cloud, helping to combat climate change by drastically reducing the amount of data exchanged. Sitting at the heart of power supply units and power converters, digital GaN can aggregate performance data from the power circuits to compute health-and-usage data. An ultralow bandwidth data flow can be generated by processing the data onboard: it requires just a few kilo-bytes per day to provide optimal information for monitoring huge installations using a massive quantity of power supply units.

By providing an intelligent link between the world of data and the world of electrical power, digital GaN enables remote-firmware updating, as well as feature activation over the internet. This possibility is common in many computing devices, such as internet boxes, TVs and computer mainboards. There is also the opportunity to deliver power and data to EVs.

For power supply systems that serve data-hungry needs that are as diverse as consumer electronics, e-mobility, data centres and industrial applications, there will be increasing pressure to deliver the vast amounts of power required to transmit that data. Helping to meet that demand are our GaN ICs that combines several power electronics functions in a single GaN chip. The payoff: improved speed, higher efficiency, greater reliability and cost-effectiveness, alongside a digital control that opens new paths from the power stage to the cloud, while respecting the environment by drastically reducing the amount of data exchanged.

FURTHER READING

- P. Bau *et al.* "Static and dynamic measurements for GaN integrated switches", International Exhibition and Conference for Power Electronics (PCIM 2022)
- D. Bergogne *et al.* "Integrated GaN ICs, development and performance" 21st European Conference on Power Electronics and Applications (EPE'2019)

A webinar without the right audience is worthless!

Dedicated webinars for the compound semiconductor industry:

Using our 30+ years' experience in B2B vertical technical markets, and as the publisher of Compound Semiconductor portfolio, we now offer effective webinars, webcasts and virtual events. We help you get your message, to your desired audience, by marketing to over 53,000 power electronics professionals.

We offer access to the right audience at the right time.

In addition to organising and managing your webinar, we can also market your webinar to our specialist Compound Semiconductor database.

We deliver the audience!

In a dedicated 6 week program we will promote through our magazine, newsletters, LinkedIn group and website.

We can also provide the webinar moderator, from our team of highly respected editors and researchers.

Not sure what to say? Let our editors work with you and help you with the content.

Harness the power of a webinar

- **Brand Awareness**
  Increase global awareness by running sponsored webinars, webcasts and virtual events which also have the possibility of generating revenue
- **Lead Generation**
  Generate and mature leads through the use of online events. Then analyse, qualify, and understand their buying behaviour
- **Thought Leadership**
  Become the voice of knowledge by generating compelling content via online events

COMPOUND SEMICONDUCTOR
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

Find out how Angel Webinar can help you organise and run a webinar within the power electronics industry, contact:

jackie.cannon@angelbc.com **+44 (0)1923 690 205**

angelwebinar.co.uk

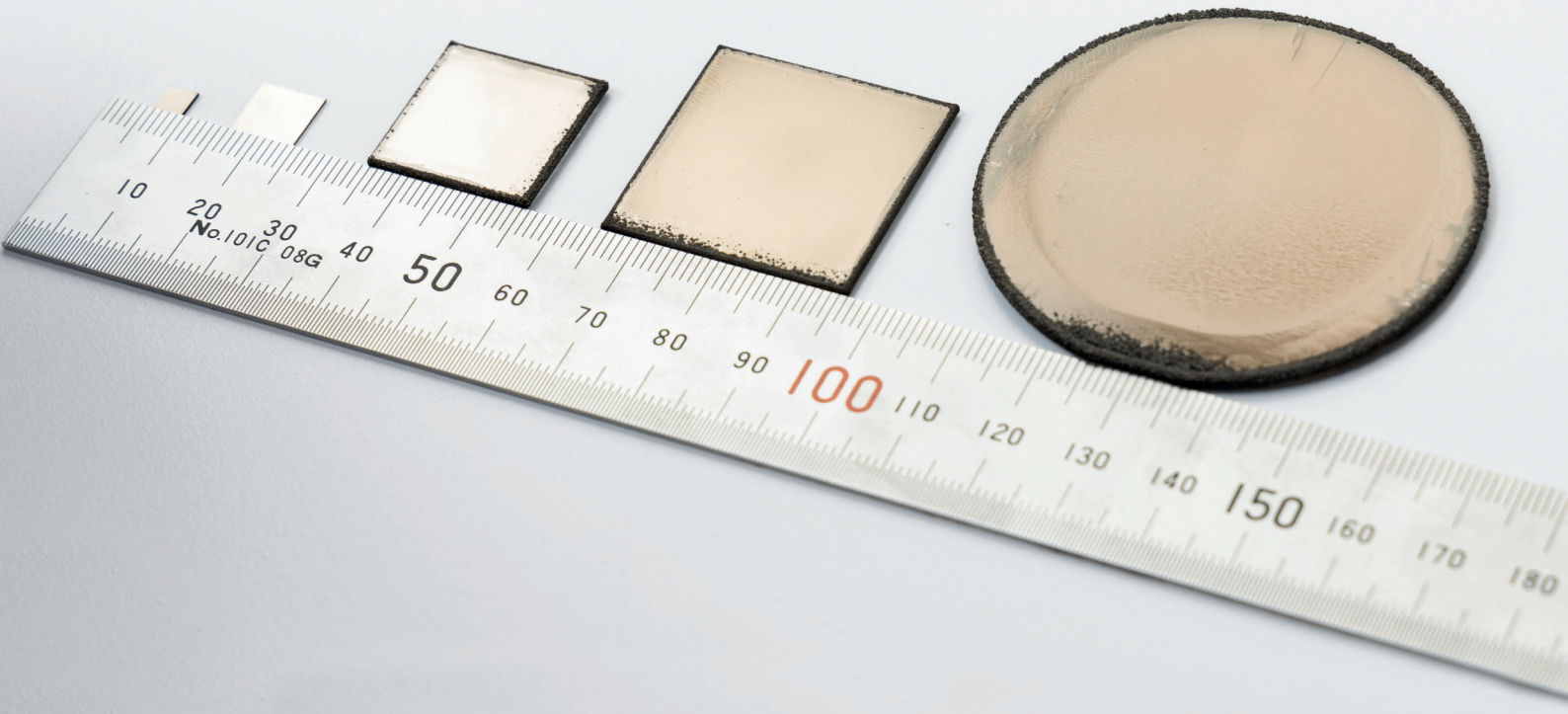
Creating commercially viable diamond substrates

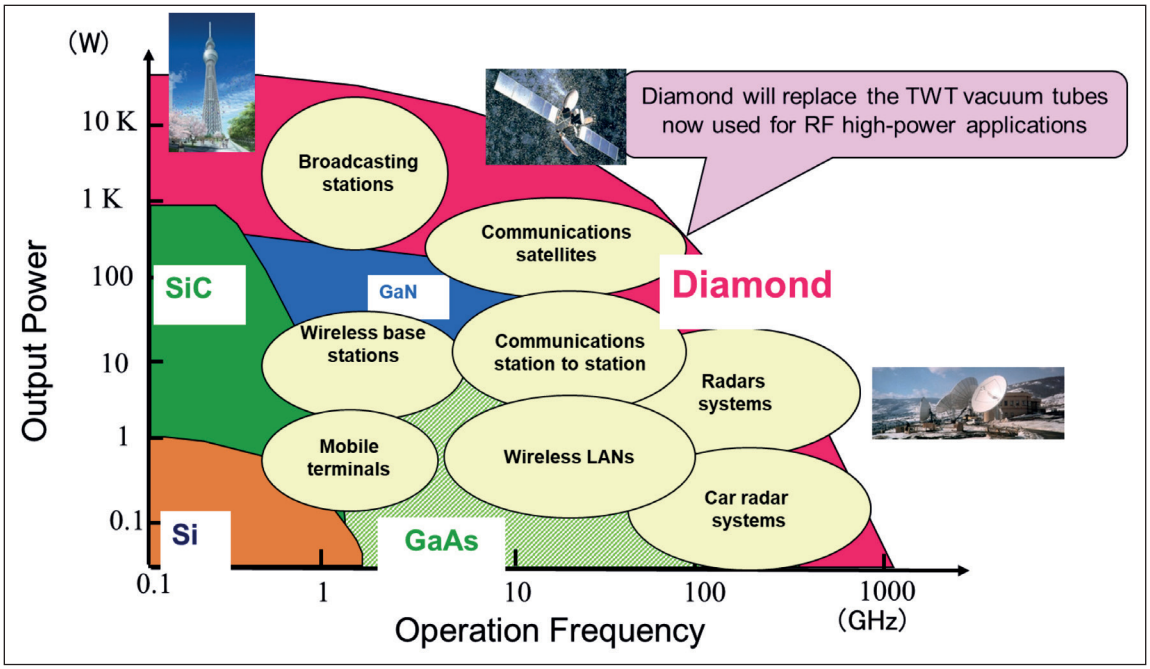
Diamond is set to serve in many more high-end applications, thanks to the development of a heteroepitaxial growth process for fabricating 2-inch substrates

BY SEONG-WOO KIM AND KOJI KOYAMA FROM ORBRAY COMPANY (FORMERLY ADAMANT NAMIKI PRECISION JEWEL)

CRYSTALLINE DIAMOND is the ultimate semiconductor. It combines an outstanding degree of crystallinity with an extremely high breakdown voltage, excellent electrical properties and exceptionally high thermal conductivity (see Table 1). Once this allotrope of carbon is put to practical use, it will enable devices that are vastly superior to those incorporating currently available materials, setting far higher benchmarks for voltages, output powers, and efficiencies. What's more, thanks to the nitrogen vacancy centre that's unique to diamond, this material has tremendous promise for making sensors.

By far the biggest challenge to commercialising these 'super-devices' is the lack of industrial-size diamond wafers. Up until now, development has been restricted to diamond wafers that are typically just 4 mm by 4 mm in size. Such wafers, made using high-temperature, high-pressure methods, are simply too small for the semiconductor industry. It is possible to scale-up by laying out small wafers as if they are tiles and growing a film across them – but this leads to an unacceptably high density of defects at the wafer boundaries, arising from slight misorientations between aligned substrates. That said, the main reasons why large uniform





➤ Figure 1. Semiconductor power device applications in terms of operating frequency and output power for wireless communication.

wafers cannot be produced are two-fold: it is almost impossible to create sufficiently large seed crystals, and separating seed crystals from the diamond crystals that are grown on them is extremely difficult.

At Orbray, formerly Adamant Namiki Precision Jewel, of Tokyo, Japan, we have broken new ground by developing 2-inch diamond wafers via microneedle growth and step-flow growth methods. It's important to note that these methods are already deployed in mass production and further scaling is possible. Read on to discover what we have achieved, and learn of the range of devices that could benefit from crystalline diamond wafers.

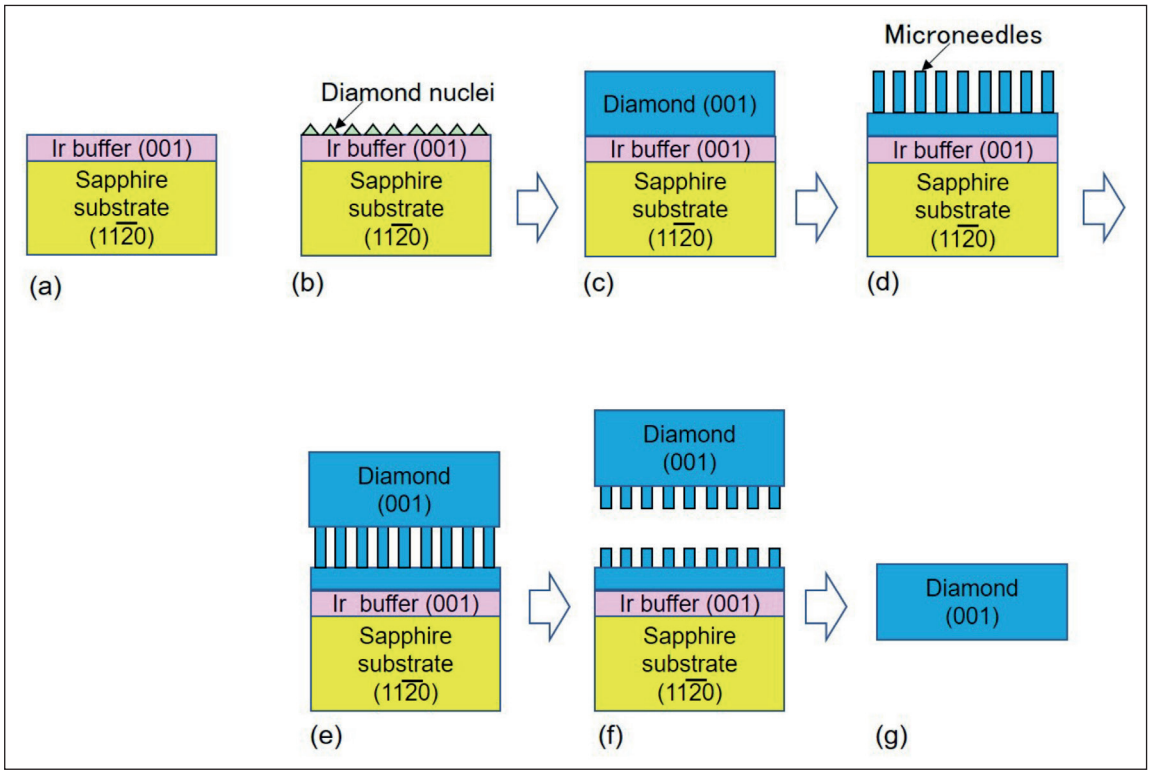
Providing some numbers to the virtues of diamond, we can site a breakdown field that reaches to 10 MV cm^{-1}, a thermal conductivity of 22 W cm^{-1} K^{-1} – the highest of any material – and carrier mobilities for electrons and holes of 4500 and 3800 cm^2 $V^{-1}s^{-1}$, respectively. These figures indicate that diamond devices promise to be not just a little bit better than today's most impressive equivalents, made from SiC and GaN, but substantially better (see Figure 1, which illustrates the output power against operating frequency for various semiconductors, along with their common applications). Note that broadcasting stations, communications satellites and radar devices require devices that operate at high speeds and deliver extremely high output powers, requirements that are only met today by vacuum tube amplifiers. Diamond is the only semiconductor with the characteristics needed to meet such extreme requirements. Once diamond devices replace vacuum tubes, this will trim power consumption and in turn enable downsizing.

As well as great potential for RF and power devices, diamond has outstanding properties that can be used in radiation detectors. For this reason, detectors utilizing the very high radiation hardness of diamond have been developed for use at Japan's Fukushima nuclear power plant. There are also opportunities in medicine and healthcare, where diamond detectors are attractive, because they don't need a correction factor, as carbon is a human tissue equivalent.

Yet another potential application for diamond is in quantum computing, thanks to nitrogen vacancy (NV) centres in this material. These centres consist of a nitrogen atom and a corresponding vacancy in the diamond lattice, which has an independent spin (NV-). This NV-centre can form a minute magnetic force at the atomic level. While it is possible to achieve electron spin in other materials, in those

	Si	SiC	GaN	Diamond
Band Gap (eV)	1.1	3.2	3.3	5.4
Hardness (GPa)	12	23	10	100
Mobility (cm^2/Vs)	1350 (e)	1000 (e)	2000 (e)	4500 (e) 3800 (h)
Breakdown voltage (MV/cm)	0.3	2.8	3.0	9.9
Thermal conductivity (W/cm·K)	1.5	5.7	1.8	22

➤ Table 1. A material property comparison of various semiconductor materials.

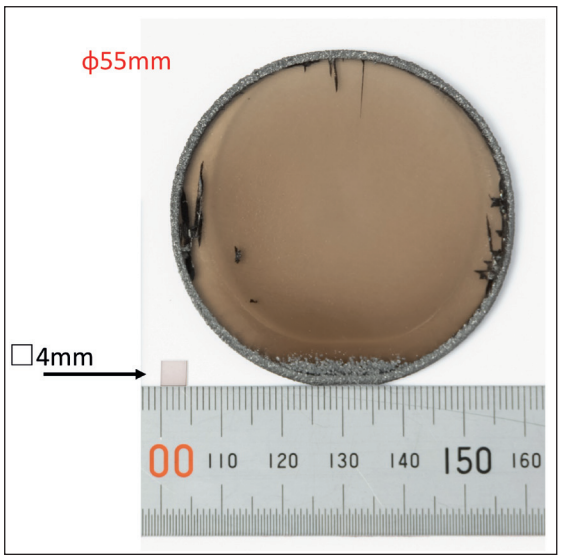


➤ Figure 2. The production process for heteroepitaxial diamond.

cases the direction of the spin cannot be stabilised at room temperature. Diamond is markedly different, providing a room-temperature electron spin that is reliable enough for the semiconductor industry.

Overcoming size limitations

Limiting the size of today's diamond substrates is the dimensions of the anvil employed in high-temperature, high-pressure growth. We avoid this issue with our heteroepitaxial approach, involving the growth of diamond on a non-native substrate. Following investigations that considered silicon, SiC, TiC, nickel, platinum, cobalt and iridium as potential substrates, we found that the latter is best. It is the element that's blessed with the highest nucleation density, exceeding 1×10^8 cm^{-2}. Unfortunately, single-crystal iridium substrates with a large surface area are not available, so the likes of iridium-on-MgO, YSZ-on-silicon and STO-on-silicon has been investigated.



➤ Figure 3. A free-standing diamond substrate with diameter 55 mm.

A growth study with these composites revealed that the best material quality for diamond, according to X-ray diffraction, comes from growth on the iridium-on-MgO composite. This platform produced full-width at half-maximum values for peaks in the diffraction spectra of 281 arcsec and 534 arcsec in the (004) and (311) planes, respectively. The X-ray rocking curve full-width at half-maximum of the (004) symmetrical diffraction indicates a tilt component, while that of (311) asymmetrical diffraction reveals a twist component.

To improve crystal quality, we have introduced diamond micropatterns and microneedles in early-stage growth. These micropatterns lead to epitaxial lateral overgrowth, which reduces the density of dislocations; while the microneedles release heteroepitaxial strain, leading to a natural delamination that creates free-standing diamond crystals without breakage.

Sapphire is renowned for its high quality, low cost, and availability in relatively large sizes, attributes that have led to its use as a foundation for growing nitrides. Due to these strengths, we have adopted it for the growth of diamond, with iridium providing an intermediary layer. This also makes sense from a coefficient of thermal expansion perspective: values for sapphire along the *a*-axis and *c*-axis are 4.2×10^{-6} K^{-1} and 5.3×10^{-6} K^{-1}, respectively, which

are higher than the 1.5 × 10^{-6} K^{-1} for diamond, but still much less than that for MgO, of 12.8 × 10^{-6} K^{-1}.

Controlling the stress

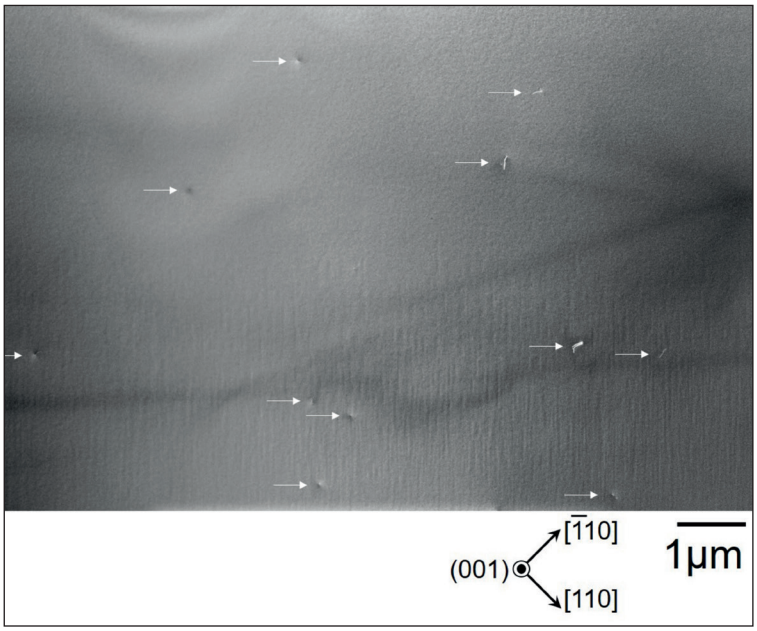
Initially our fabrication of our heteroepitaxial diamond, realised by what we refer to as the microneedle growth method, began with the sputtering of an iridium buffer layer on the (110) orientation of sapphire (see Figure 2 for an overview of the process flow). After this, diamond nuclei were created by applying bias-enhanced nucleation to the iridium buffer. We then grew the first diamond layer on the iridium buffer, using micro-wave plasma assisted CVD (MPCVD), with CH_4 and H_2 providing the source gases.

Our next step involved the fabrication of microneedles on this first diamond layer. To do this, we began by depositing a nickel film on top of the first layer of diamond, before defining an array of through-holes that are 2 μm in diameter and separated with a 10 μm pitch. Annealing this structure in a hydrogen atmosphere at 1000 °C drove the migration of carbon atoms that are in contact with the nickel film towards the surface, where they reacted with hydrogen to produce methane. This caused the diamond that's in contact with the nickel film to be etched away, resulting in formation of diamond microneedles.

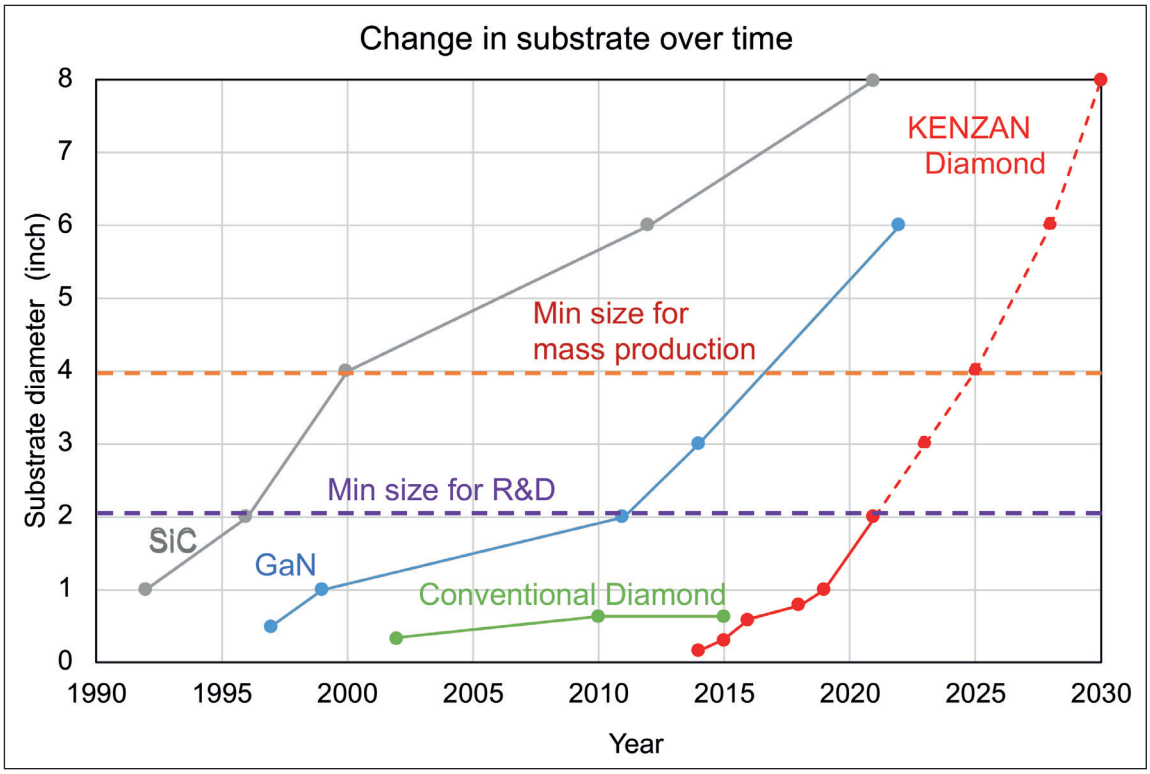
Using MPCVD, we grew a second diamond layer on top of the microneedles. This is much thicker than the first, typically 800-1000 μm. During cooling after diamond growth, the microneedles broke, due to stress that stems from difference in thermal expansion coefficients. Polishing the front and back surfaces of the liberated diamond removed the microneedles to create an atomically flat front surface. The final thickness of the free-standing diamond is 500-600 μm.

To succeed with our microneedle growth, we addressed several issues. One potential pitfall is that the microneedle fabrication process causes a bottleneck, hindering efforts to reduce production costs.

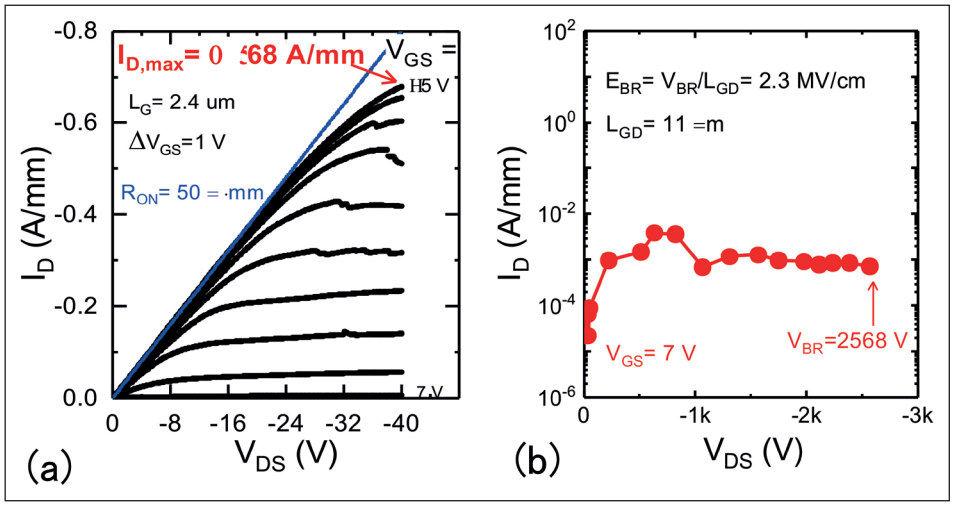
Our novel solution is to induce diamond step-flow growth on the misoriented iridium-on-sapphire



➤ Figure 4. Transmission electron microscopy image of (001) heteroepitaxial diamond.



➤ Figure 5. For all wide bandgap semiconductors, substrate size has increased over time.



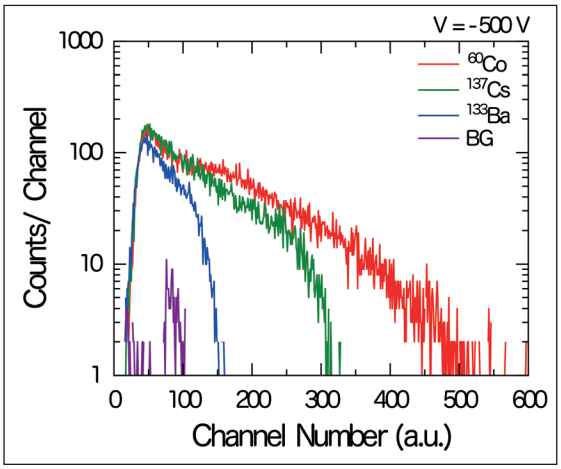
➤ Figure 6. (a) DC output characteristics and (b) maximum off-state breakdown voltage characteristics of a diamond MOSFET with a gate length of 2.4 µm. During the fabrication of this transistor, to perform NO_2 *p*-type doping, the H-terminated diamond substrate was subjected to 2 percent NO_2 gas diluted in N_2. Ohmic contacts were formed with a 50-nm thick gold layer. A 16 nm-thick Al_2O_3 bi-layer was deposited as a gate insulator layer, which also provided the diamond channel with passivation. Gold formed the gate.

substrates, because this drastically reduces the stress in the diamond film. Step flow growth enlarges the substrate size without the complicated microneedle process, and has enabled us to successfully create a 2-inch diameter diamond substrate, the minimum size required for the semiconductor industry.

We have also developed a process to reduce nitrogen contamination to less than 3 parts per billion, according to electron spin resonance. We have given this form of diamond, which we fabricate using stress-released heteroepitaxial growth, the commercial name Kenzan Diamond.

Our 2-inch diameter diamond substrates with low nitrogen contamination are transparent (see Figure 3). X-ray pole figure measurements of this material have identified that epitaxial relationship of diamond/iridium/sapphire is diamond (001) [110]// iridium (001) [110] // sapphire (11$\bar{2}$0) [0001]. Another insight provided by this measurement is that the heteroepitaxial diamond free-standing substrate is free from twins.

X-ray rocking curve full-width at half-maximum values for the (004) and (311) diffraction peaks are 98.35 arcsec and 175.3 arcsec, respectively. These values, the lowest for heteroepitaxial diamond ever reported, have been obtained across the entire substrate. The curvature of our substrate can be determined by the values for the X-ray rocking curve peak angle of diamond (004). This reveals that the substrate is concave, with a curvature of 90.6 cm, caused by the significant difference in the coefficients of thermal expansion of sapphire and diamond.



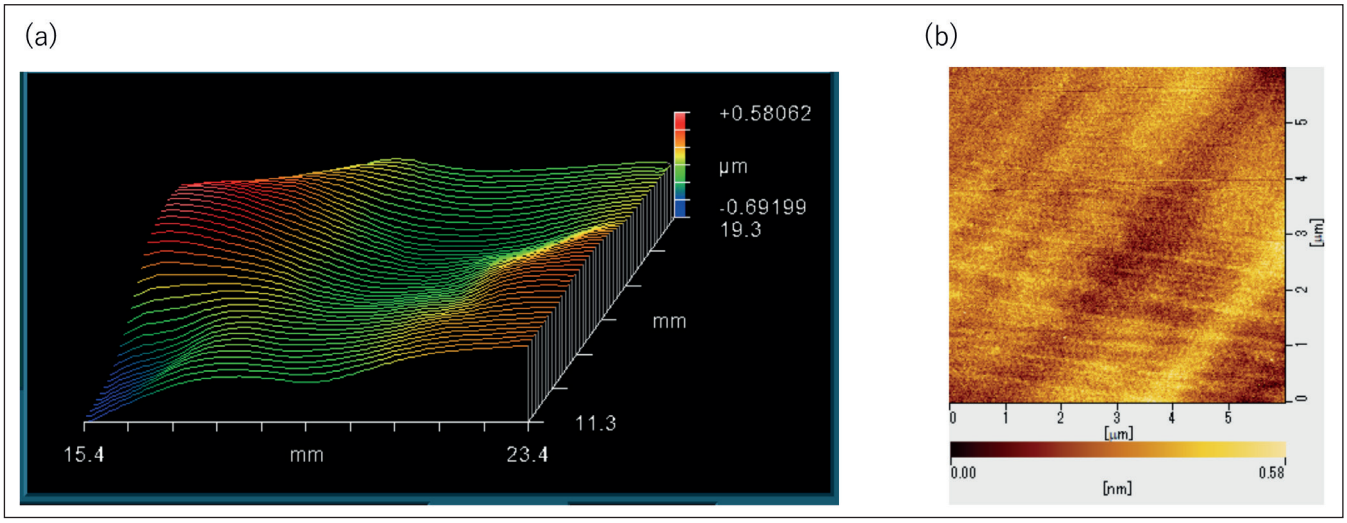
➤ Figure 7. Radiation detection results for 60Co, 137Cs, and 133Ba.

Additional characterisation of our material is provided by transmission electron microscopy (see Figure 4). Using the diffraction vector **g** = 2$\bar{2}$0, which uncovers all dislocations, we have determined a threading dislocation density of 1.4 × 10^7 cm^{-2}. This result is in good agreement with the etch pits density, obtained by dry etching.

With nitride semiconductors, to ensure laser oscillation in an InGaN layer grown on a sapphire substrate, the dislocation density should be below 1 × 10^7 cm^{-2}, while the X-ray rocking curve full-width at half-maximum for (004) needs to be less than 100 arcsec. We believe these targets are applicable to the development of heteroepitaxial diamond. As we try to meet these specifications, we will search for an explanation for the stress reduction mechanism that occurs during the step flow method. Another goal is to produce diamond substrates with larger diameters and improved quality.

Over the last three decades there has been an increase in the available substrate sizes of common wide bandgap materials. We have set ourselves the goals of producing a 4-inch diamond substrate in 2025 and an 8-inch one in 2030. In parallel with this increase in diameter, there must be a reduction in cost if the diamond substrate is to become widespread.

High production costs are mainly due to the expense that's associated with polishing diamond, which is an extremely hard material. While there's not space to discuss the details of polishing technology, we are confident that there will be



➤ Figure 8. Surface morphology of Kenzan Diamond for surface-activated bonding, as revealed by (a) laser interferometer and (b) atomic force microscopy. Interferometry reveals bowing below 2 µm and a thickness variation, based on 5 points, of less than 2 µm. According to atomic force microscopy, surface roughness is below 0.1 nm.

advances that trim costs. By 2030, we intend to produce 2-inch diamond substrates with the same level of price as currently available 2-inch GaN substrates.

Making devices

Working in partnership with researchers at Saga University, Japan, we have fabricated NO_2-doped *p*-channel diamond MOSFETs on a Kenzan Diamond, formed by the growth of (001) diamond on a (110) sapphire substrate misoriented by 5° in the [0001] *c*-direction. These transistors exhibit a breakdown voltage of 2568 V, the highest value for a diamond MOSFET (see Figure 6, which includes details of device fabrication). We have also evaluated DC output characteristics, recording a maximum drain current of -0.68 A/mm and an on-resistance of 7.54 mΩ cm^2. The maximum experimental Baliga Figure of Merit of 874.6 MW cm^{-2} was demonstrated. We have our sights set on breaking the record for a GaN device of 2093 MW cm^{-2}.

We have also investigated opportunities for our technology to be applied to the detection of radiation. Already on the market are conventional diamond radiation detectors, made from either very high-quality natural diamond or CVD homoepitaxially grown diamond. Both provide high performance, thanks to diamond's extreme radiation hardness and its excellent thermal conductivity. However, widespread commercialisation is hampered by size limitations. The introduction of Kenzan Diamond promises to overcome this, thereby diversifying diamond's applications.

Through a collaboration with Saga and Tohoku Universities, Japan, we have built a radiation detector that incorporates Kenzan Diamond. The nitrogen concentration in the substrate is below 3 parts per billion, in order to prevent carrier trapping. Characterisation of the device's capacity for radiation detection involved the use of three different sources: ^{60}Co (1.17 and 1.33 MeV), ^{137}Cs (662 keV), and ^{133}Ba (356 keV). We recorded the output voltage associated with the electron and hole charges induced by radiation, and plotted of the energy spectrum for the three different types of γ radiation source (see Figure 7). Based on these results, it is clear to see that Kenzan Diamond can be used to discriminate between nuclides. This is an encouraging result for developing applications for diamond.

Established high-power devices are encroaching performance limitations, due to overheating. One promising way forward is to integrate GaN with diamond. It is challenging to realise the epitaxial growth of GaN on diamond, due to mismatches in lattice constants and thermal coefficients of expansion. But progress can be made with a different approach – working with Osaka City University, Japan, we have fabricated a GaN/diamond heterointerface using room-temperature, surface activated bonding. We prepared Kenzan Diamond substrates with variations in bowing, thickness, and surface roughness (see Figure 8 for details), and used surface-activated bonding to successfully adhere them to GaN.

Our development of 2-inch crystalline diamond, and our efforts with others at demonstrating devices that incorporate this material, are showcasing its great promise. While there's still a long way to go, there's good reason to believe that in time, the world will benefit from the deployment of the ultimate semiconductor.

FURTHER READING

➤ S.W. Kim *et al*. Appl. Phys. Express. **14** 115501 (2021)
➤ S.W. Kim *et al*. Appl. Phys. Lett. **117** 202102 (2020)

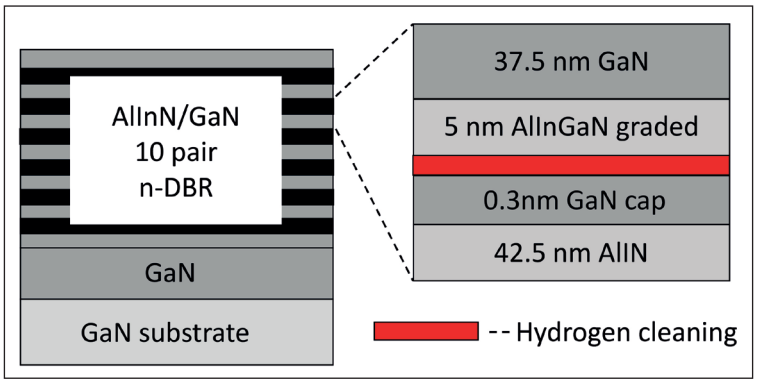
Hydrogen cleaning ensures high-quality mirrors for GaN VCSELs

A flow of hydrogen gas during the growth of distributed Bragg reflectors reduces pits and threading dislocations

A JAPANESE COLLABORATION is claiming to have made significant progress in the growth of the mirrors for GaN VCSELs. This success could aid efforts to commercialise blue and green VCSELs, which are promising sources for compact and lightweight mobile displays and adaptive headlights with controllable illumination.

The researchers from Meijo University and the National Institute of Advanced Industrial Science and Technology have produced high-quality, *n*-type AlInN/GaN distributed Bragg reflectors (DBRs) via hydrogen cleaning.

This effort builds on the team's previous successes in fabricating GaN VCSELs, including the production of variants with non-conductive and conductive AlInN/GaN DBRs that have maximum output powers of 4.4 mW and 2.6 mW, respectively. The addition of doping simplified device design, but degraded morphology, with a rougher surface contributing to a lower output power.



➤ Hydrogen cleaning removes pits in the *n*-type DBR.

The rougher surface is attributed to a higher dislocation density in the DBR. These imperfections are avoided in the undoped DBR by adding a GaN cap less than 1 nm-thick on the AlInN, prior to an increase in temperature. For the doped DBR there's a need to introduce a 5 nm-thick AlGaInN compositionally graded layer with a silicon concentration of 6×10^{19} cm^{-3} to neutralise negative polarisation charges – this must be grown at a lower temperature, leading to a high density of threading dislocations.

As it is not possible to use a higher temperature to reduce the density of threading dislocations, the researchers have tried to supress them by eliminating indium-indium bonds.

"Indium atoms are very volatile," remarked team spokesman Tetsuya Takeuchi from Meijo University. "If we use hydrogen, it is quite possible to remove indium atoms on the surface."

Takeuchi and co-workers began their trials by producing six samples with a 10-period DBR, each grown with different hydrogen flow conditions. The growth of every period of the mirror began with a 42.5 nm AlInN layer and a 0.3 nm GaN cap. Hydrogen cleaning followed during a growth interruption, prior to the addition of a 5 nm-thick AlInGaN layer and a 37.5 nm-thick GaN layer. The growth of the first three layers took place at 840 °C under nitrogen gas; while the 32.5 nm GaN layer was grown at 1100 °C under hydrogen gas.

Variations in hydrogen conditions came from applying a hydrogen flow of 31 standard litres per minute (slm), and varying ammonia flow from 0.5 slm to 4 slm. Assessing material quality by atomic force microscopy (AFM) revealed a minimum pit density of 1.3×10^5 cm^{-2} for an ammonia flow of 0.65 slm.

The team used this condition to produce a 40-pair, silicon-doped DBR, alongside variants that were undoped and had no hydrogen cleaning.

No pits were observed in the undoped DBR, while doped variants with and without hydrogen cleaning had pit densities of 1×10^7 cm^{-2} and less than 10^6 cm^{-2}, respectively. It is even possible that the sample with hydrogen cleaning has no pits.

Additional measurements on the superior doped sample revealed a peak reflectivity of 99.8 percent at 399 nm, and a vertical resistance of 15 Ω.

These promising results prompt the question of whether it is worth pursuing the growth of GaN VCSELs with two *n*-type DBRs, plus a tunnel junction that provides a switch from *n*-type to *p*-type conduction. However, Takeuchi warns that long growth at a high temperature – it takes 12 hours to grow one DBR – could damage the quantum wells in the active region.

The team are now growing and fabricating GaN-based VCSELs with conducting DBRs, produced using hydrogen cleaning. Takeuchi expects these lasers to exhibit improved performance, due to superior current injection uniformity and a lower device resistance.

REFERENCE

➤ K. Shibata *et. al.* Appl. Phys. Lett. **15** 112007 (2022)

Enhancing the credentials of Ga_2O_3 with a novel MOSFET

A vertical Ga_2O_3 MOSFET with a U-shaped gate trench and a current-blocking layer combines promising performance with E-mode operation

ENGINEERS FROM CHINA are claiming to have broken new ground by unveiling the first β-Ga_2O_3 MOSFET with a U-shaped gate trench.

This vertical MOSFET has key advantages over those with a lateral geometry, according to Guangwei Xu from the University of Science and Technology of China, who is the spokesman for a team that includes departmental colleagues and Yongjian Ma from the Suzhou Institute of Nano-Tech and Nano-Bionics. "For Ga_2O_3 lateral MOSFETs, channel thickness is limited to hundreds of nanometers," commented Xu, who added that in this class of device the substrate tends to just provide structural support, and does not contribute to device performance.

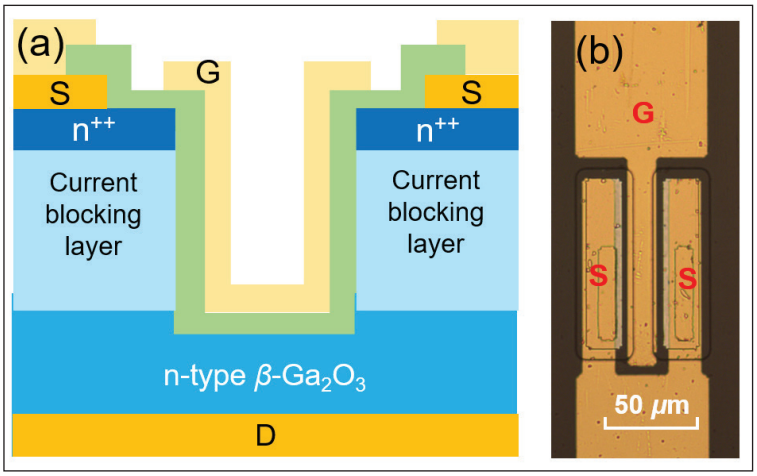
"Therefore, the drain-to-source current cross-section for a lateral MOSFET is much smaller than a vertical MOSFET, which means that a much larger current density is needed for a lateral MOSFET to achieve the same current level as a vertical MOSFET."

Another advantage of the vertical MOSFET is that its breakdown voltage can be increased without sacrificing chip area, because the breakdown voltage scales with drift-layer thickness. Vertical transistors also benefit from a more uniform heat distribution, as well as burying the peak electric field in the bulk – this prevents premature device failure caused by surface flashover, and alleviates performance instabilities induced by surface states.

Xu and co-workers are not the first to produce a vertical β-Ga_2O_3 MOSFET. There are reports of vertical fin-channel FETs, vertical diffused-barrier FETs and vertical current-aperture FETs – but all of these have their weaknesses. The fin-channel FETs, which have realised a breakdown voltage of more than a kilovolt, are produced using a complex, costly fabrication process. Meanwhile, unlike the U-shaped trench MOSFET, the vertical diffused-barrier FET and the current-aperture FET feature a JFET region, leading to a higher internal resistance.

Of all the variants, the cell pitch for the U-MOSFET can be made much smaller, enabling a higher packing density, according to Xu.

Realising a U-shaped trench β-Ga_2O_3 MOSFET is not easy, because it is a challenge to form an effective current-blocking layer. Drawing on work that shows how thermal annealing can create a high-resistivity layer, Xu and colleagues have introduced current blocking by thermal oxidation. This has led to the formation of an enhancement-mode MOSFET with an on-off ratio of 6 x 10^4.



➤ (a) U-shaped trench β-Ga_2O_3 MOSFETs feature an effective current blocking layer, formed by oxygen annealing. (b) An optical image of this device.

To produce the team's U-shaped trench β-Ga_2O_3 MOSFETs, the researchers began by taking a (201)-orientated substrate with a doping concentration of around 3 x 10^{17} cm^{-3} an annealing it under oxygen for 6 hours at 1200 °C to form a current blocking layer. Implanting oxygen with a concentration of around 3 x 10^{19} cm^{-3} introduced an n^{++} layer, activated by thermal annealing for 5 minutes at 950 °C. Mechanical grinding of the backside of the wafer removed the high-resistivity layer, before etching defined the trench and mesa. Electron-beam evaporation enabled the addition of source and drain contacts, prior to atomic layer deposition of the gate dielectric and the formation of the gate, using magnetron sputter deposition.

Electrical measurements on the devices revealed an off-current below 10^{-4} A cm^{-2} at a gate-source voltage of 0 V, suggesting normally off operation. The threshold voltage is 11.5 V, a high value that is attributed to the thick dielectric. Trimming this layer could realise a more preferable threshold voltage.

Xu revealed that one of the team's next goals is to reproduced their results via HVPE. The breakdown voltage of the latest devices is limited by the small depletion width of relatively highly doped substrates. "To improve both the on-state and the off-state performances, future work will focus on the highly doped substrate with a lightly doped epitaxy layer."

REFERENCE

➤ X. Zhou *et. al.* Appl. Phys. Lett. **121** 223501 (2022)

Eradicating dark-line defects in deep-UV laser diodes

A sloped mesa geometry promises superior deep-UV laser diodes by banishing dark-line defects

A TEAM FROM JAPAN has eliminated dark-line defects in aluminium-rich, AlGaN-based lasers by introducing a sloped mesa geometry. Eradicating these defects should enable the production of more reliable, higher efficiency laser diodes emitting within the UVC, which spans 100 nm to 280 nm.

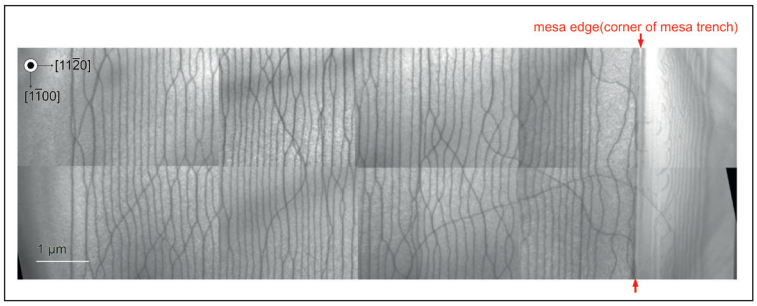
According to the engineers from Nagoya University and Asahi Kasei Corporation, today's AlGaN UVC lasers are impractical, due to their low efficiency, short lifetime and lack of reliability.

Contributing to these weaknesses are dark-line defects, which deteriorate the active area at the edge of the mesa. One workaround is to place the *p*-type electrode away from the mesa edge, so the current path avoids this area – but this leads to a higher resistance, and in turn device heating and a hike in threshold current.

Adopting this approach, the team recently produced a 272 nm laser delivering CW operation at 5 °C. For this 600 μm-long laser, every 5 μm increase in distance from the mesa corner increased the resistance between the *n*- and *p*-electrodes by 2.6 Ω. The high resistance that resulted led to Joule heating, which prevented room-temperature lasing. The engineers could not reduce this resistance by thickening the $Al_{0.75}Ga_{0.25}N$ *n*-type cladding layer or decreasing its aluminium content due to constraints associated with pseudomorphic growth. Breaking these rules would lead to a higher defect density in the active region, quashing radiative recombination.

One of the weaknesses of the team's 272 nm laser is that it is riddled with dark-line defects. To investigate their origin, the team's latest work involved MOCVD growth of a laser structure on a single-crystal AlN substrate. This heterostructure consisted of: a 350 nm-thick *n*-type $Al_{0.7}Ga_{0.3}N$ cladding; a 100 nm-thick $Al_{0.63}Ga_{0.37}N$ waveguide with multiple quantum wells; a 320 nm-thick *p*-type cladding layer, with distributed polarization doping and an average aluminium content of 85 percent; and a *p*-contact layer. Dry etching isolated the *p*-contact layer and defined a mesa stripe along the [1$\bar{1}$00] direction.

To aid analysis, the team avoided adding metal electrodes to their device. However, they still applied thermal treatments that would be used during the fabrication of metal electrodes to their epistructure, in case this influenced its material quality.



Plan-view transmission electron microscopy images of this structure clearly show dark-line defects (see figure), observed as far at 12 μm inside the mesa edge. Inspection of these images reveal an absence of partial dislocations and stacking faults, providing strong evidence that the dislocations stem from slip, resulting from forces perpendicular to the mesa stripe.

➤ Plan-view transmission electron microscopy reveals dark line defects in AlGaN laser diodes with a conventional geometry.

These dislocations occur in other material systems, such as InGaN/GaN and AlN/SiC heterostructures, where there is a large strain due to lattice mismatch, with symmetry of the plane stress broken by the mesa trench.

Finite-element modelling by the team revealed the forces acting within the structure, and indicated that reducing the mesa slope angle to less than 50° could provide a significant reduction to the shear stress concentration at the corner of the mesa trench.

The team have put this finding to the test. "AlGaN has a slow etching rate, so we were worried whether we could obtain the desired shape," admitted team spokesman Maki Kushimoto. "However, after trying several resist and reflow conditions, it is clear that we can form the mesa stably."

According to plan-view transmission electron microscopy, structures with a slope inclination of 15° to the surface are free from dark-line defects.

Goals for the team include further studies of dislocations. "I would like to clarify the mechanism of dislocation propagation to the active layer, the effect of thermal expansion, and the effect of crystal plane orientation," revealed Kushimoto.

REFERENCE

➤ M. Kushimoto *et al.* Appl. Phys. Lett. **121** 222101 (2022)

ONLINE ROUNDTABLE

Connecting Leaders & Experts in the Compound Semiconductor Field

- Based around a hot topic for your company, this 60-minute recorded, moderated zoom roundtable would be a platform for debate and discussion
- Moderated by an editor, Richard Stevenson, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the Compound Semiconductor homepage for 8 weeks
- 4x weekly dedicated HTMLs
- 4x news pieces which would also appear on the weekly e-newsletters
- Promoted through our social media platforms for 8 weeks (pre and post event)
- Available as an on-demand asset through all mediums
- All registered attendees' details would be made available to you

Cost: €4995 / $4995

COMPOUND SEMICONDUCTOR
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

Contact: Jackie Cannon
jackie.cannon@angelbc.com

ANGEL EVENTS

INDUSTRY SERVICES DIRECTORY

To promote your products and services contact:

UK, Europe + Rest of the World
Jacob Caulfield
T: +44 (0)2476 719 979
E: jacob.caulfield@angelbc.com

USA:
Janice Jenkins
T: + 1 724-929-3550
E: jjenkins@brunmedia.com

agnitron technology
Tel: +1 952 937 7505
Email: sales@agnitron.com
www.agnitron.com

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

APPLIED ENERGY SYSTEMS
Tel: +001 610-647-8744
info@appliedenergysystems.com
www.appliedenergysystems.com

APPLIED MATERIALS®
make possible
Tel: +1 408 727 5555
www.appliedmaterials.com

ARM PURIFICATION
BY APPLIED ENERGY SYSTEMS
Tel: 1 610-647-8744
purification@appliedenergysystems.com
www.armpurification.com

BRUKER
Tel: +44 (0)191 332 4700
Fax: +44 (0)191 332 4800
sales.semi@bruker.com
www.bruker.com

CS CLEAN SOLUTIONS
Tel No: +49 (89) 96 24 00-0
Fax No: +49 (89) 96 24 00-122
Email: sales@csclean.com
www.csclean.com

MBE KOMPONENTEN | DR. EBERL
Tel: +49 7033 6937-0
info@mbe-components.com
www.mbe-components.com

Efab
Tel: +886 4 2534-7800
Fax:+886 4 2534-8869
Email: sales@efab.com.tw
www.efab.com.tw

GATAN AMETEK®
info-gatan@ametek.com
www.gatan.com

HORIBA Scientific
Tel: +1 732 494 8660
joanne.lowy@horiba.com
www.horiba.com/scientific

INNOVION
FOUNDRY ION IMPLANTATION
Tel: +1 408 501 9100
Fax: +1 408 501 9110
Email: sales@innovioncorp.com
www.innovioncorp.com

evatec
process systems
Tel: + 41 81 403 8000
Fax: + 41 81 403 8001
www.evatecnet.com

III/V-Reclaim
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.com

Non Contact Measurements
Resistance, Resistivity
Wafer Thickness

KITEC
microelectronic technologie

Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

kSA k-Space Associates, Inc.
Tel: +1 734-426-7977
Email: requestinfo@k-space.com
www.k-space.com

Masimo semiconductor
Tel: +1 603 595 8900
Email: sales@masimosemi.com
www.masimosemiconductor.com

nel®
Tel: + 1 203 949 8697
Email: info@nelhydrogen.com
www.nelhydrogen.com

Experience the Power of **Connected Thinking**
onto innovation
ontoinnovation.com | info@ontoinnovation.com

Pegasus
Tel: +44 (0)1244 521869
Email: info@pegasuschemicals.com
www.pegasuschemicals.com

PerkinElmer
For the Better
Tel: +1-203-944-2418
Email: michele.pacelli@perkinelmer.com
www.perkinelmer.com

Premissa
On-Site Arsine Gas Generators
Tel: +1 732-735-5655
Email: wma@premissa.net
www.premissa.net

Sanan Integrated Circuit Co., Ltd.
Tel: +1 949 241 9501
Email: ray@sanan-ic.com
www.sanan-ic.com/en

SEMILAB
Tel: +36 1 505 4690
sales.support@semilab.com
https://semilab.com

soitec
info.epigan@soitec.com
www.soitec.com

Temescal
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

TAIYO NIPPON SANSO
Tel: + 1 908-403-3304
Email: info@tnsc-innovation.com
www.tnsc-innovation.com

Trymax®
PLASMA TECHNOLOGY SOLUTIONS
Tel: +31 24 350 0809
info@trymax-semiconductor.com
www.trymax-semiconductor.com

TYSiC
1st SiC-epi Foundry in China
Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

ULVAC
Tel: +49-89-96090900
Email: ulvac@ulvac.de
www.ulvac.eu

UMC UNITED MINERAL & CHEMICAL CORP.
MBE Specialists
Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

UNILOK
Tel: +82 10 8531 2724
overseas@unilok.com
http://unilok.com

VACUUM BARRIER CORPORATION VBC
Tel: +1-781-933-3570
Email: sales@vacuumbarrier.com
www.vacuumbarrier.com

Veeco
Tel: 516-677-0200-1222
Email: info@veeco.com
www.veeco.com

VIGO PHOTONICS
Tel: +4822 733 54 10
Email: info@vigo.com.pl
www.vigo.com.pl

vistec
Electron Beam
Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

Ysystems Ltd. 有限会社 ワイ・システムズ
Optical Metrology for Wafer Mapping and in Situ Monitoring
Tel: +81(0)88-660-7633
sales@ysystems.jp
www.ysystems.jp

Showcase your presence to the global Compound Semiconductor industry for the next 12 months

COMPOUND SEMICONDUCTOR MAGAZINE is the primary information resource for professionals working with compound semiconductor materials and devices.

Each issue of the magazine is distributed in print and digitally to over 60,000 professionals worldwide. With the largest and most diverse global audience of qualified buyers served by any compound semiconductor focused magazine, secure a corporate partnership and buyers guide entry and receive 12 months of promotion and exposure to the compound semiconductor industry across the magazine portfolio including:

- 12 months of promotion in nine issues of the print and digital versions of Compound Semiconductor featuring your company logo and company details
- 12 months of promotion and exposure on the Compound Semiconductor website **compoundsemiconductor.net** featuring a Buyers Guide entry and hyperlinked company logo
- Sponsorship of one e-news alerts sent out to over 60,000 industry professionals with text and a standard web banner.

To find out more, contact:
Jacob Caulfield
Senior B2B Event & Media Sales Executive
E: jacob.caulfield@angelbc.com
T: +44 (0)2476 719 979

USA:
Janice Jenkins
Sales Executive
E: jjenkins@brunmedia.com
T: +1 724-929-3550

200mm Process Has Arrived

Introducing the Temescal Systems UEFC-6100

Welcome to your production future. Our UEFC-6100 is the first compound semiconductor production tool designed for 200mm lift-off processing. The world's leading manufacturers are welcoming our Auratus™ enhanced line of Temescal electron beam deposition systems, and you won't want to be left behind. We vaporize metals more efficiently. We deliver uniformity. We return unmatched savings. The results are overwhelming.

With a line of tools optimized for a range of production environments, whether 150mm or 200mm, small-batch or high-volume, this invasion could be coming your way.

Find out more before you take us to your leader. Contact Ferrotec at 1-925-371-4170 or visit temescal.ferrotec.com/200mm.

UEFC-6100
25 Wafers (200mm)

UEFC-5700
42 Wafers (150mm)
18 Wafers (200mm)

UEFC-4900
25 Wafers (150mm)

FerroTec