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30 YEARS ANNIVERSARY

VOLUME 31 ISSUE I 2025

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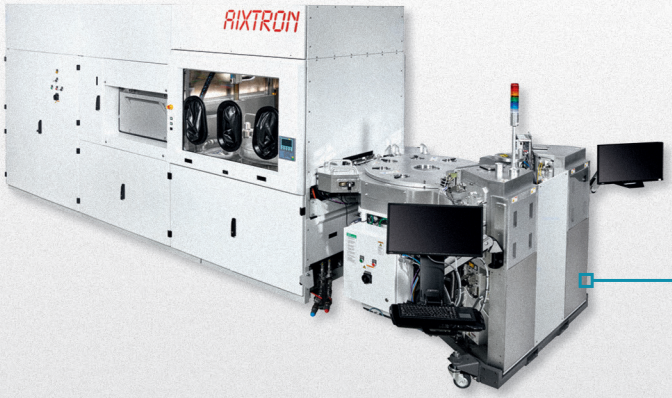
AIXTRON

THE NEW G10 SERIES

Your Productivity Solution for All Advanced Epitaxy Materials



G10-SiC

- 9x150 mm (6") or 6x200 mm (8")
- New hardware & process surpassing Single Wafer Reactor uniformities
- +50 % productivity per fab area with large batch technology & small footprint

End Markets/Products:
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G10-GaN

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated compact GaN MOCVD cluster designed 100 % for Si Power fabs
- Novel hardware solution for unmatched barrier uniformities and device yields

End Markets/Products:
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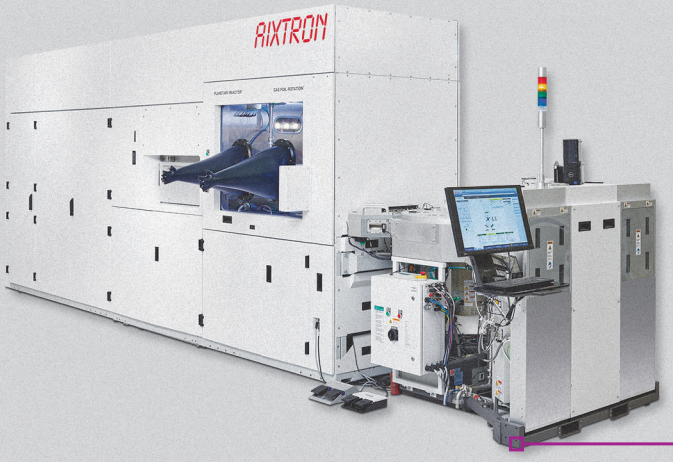

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AIXTRON SE · Dornkaulstr. 2 · 52134 Herzogenrath · Germany · Phone: +49 2407 9030 0 · **www.aixtron.com**

VIEWPOINT

BY RICHARD STEVENSON, EDITOR

New beginnings

The ending of one year and the beginning of another always offers the opportunity to make a fresh start. For some of us, this will take the form of a handful of New Year resolutions, or a to-do list – but for others, it's simply a chance to leave behind what's gone wrong and embark on a new chapter of our lives.

At the start of a new year, it's not only you and I that can strike out in a different direction with renewed vigour. Companies can do it too. This may come from the top and permeate down. But it can also be inspired by employees, returning recharged and enthused from a break over the Christmas holidays to devise and implement new plans in January that promise greater growth and profitability.

Two of the stalwarts of our industry, Wolfspeed and IQE, will certainly be keen to put their recent past behind them and blaze a new path. Both parted ways with their CEOs in the final quarter of 2024, a year that saw their share prices plummet – in the case of the SiC pioneer, by 80 percent.

While Wolfspeed has not excelled in recent times under the leadership of its ex-CEO, Greg Lowe, history may view him kindly – he led the re-direction of the company from the production of LEDs to a more promising future.

Whoever succeeds Lowe will not find it easy to turn Wolfspeed's fortunes around. Growth in the EV market has been more sluggish than hoped, and this maker of SiC substrates and devices has had to shelve plans to build a new fab in Germany, and is closing a facility at its Durham headquarters. Wolfspeed is also in the process of shedding 20 percent of its workforce, a painful move that will lead to a loss of hard-won expertise.

It's also going to be a challenge to replace IQE's recent leader, Americo Lemos. He had a tough ask, having to take

over from the company's charismatic founder, Drew Nelson, who understand both the technology and the business inside out.

What should concern anyone willing to have a crack at leading this global leader of epiwafer manufacturing is that whether our industry is booming or going through tougher times, IQE is yet to deliver a financial performance that has led to lucrative dividends for its shareholders. While it is clear that the outsourcing model can generate business within our industry, one may wonder if it can ever provide a healthy financial return to investors over many years.

There's no doubt that when the new leaders of IQE and Wolfspeed are appointed, they will initially face some difficult decisions. But at least they are working in an industry that is sure to grow, as compound semiconductors continue to play an ever-increasing role in all of our lives, throughout 2025 and beyond.

Free weekly e-news roundup go to: compoundsemiconductor.net

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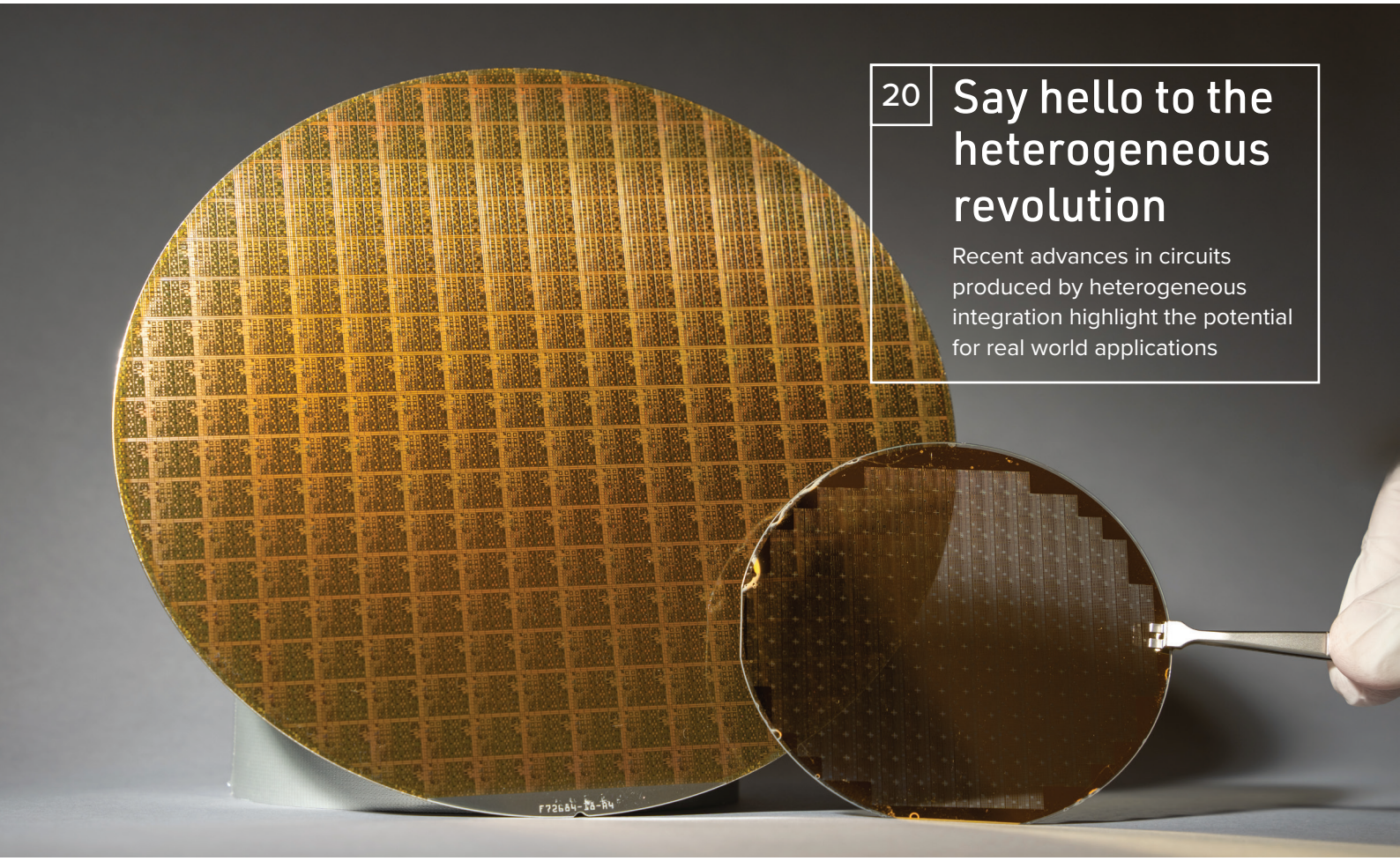

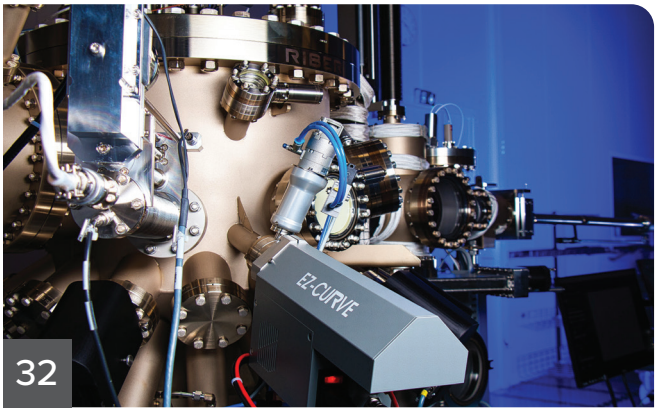

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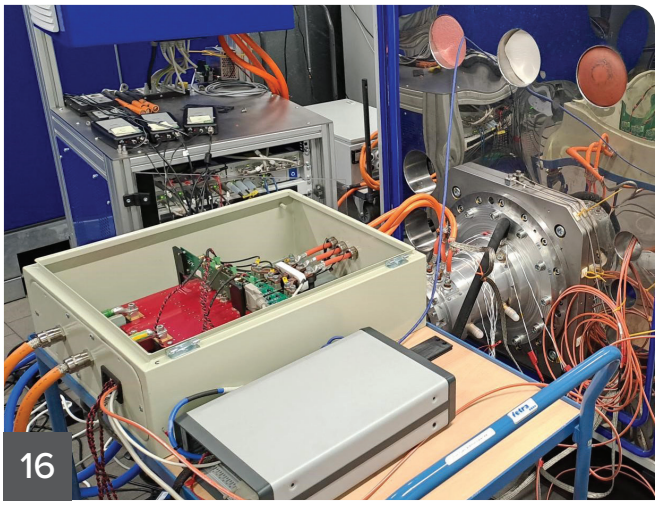

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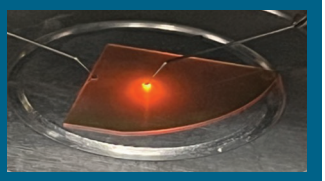

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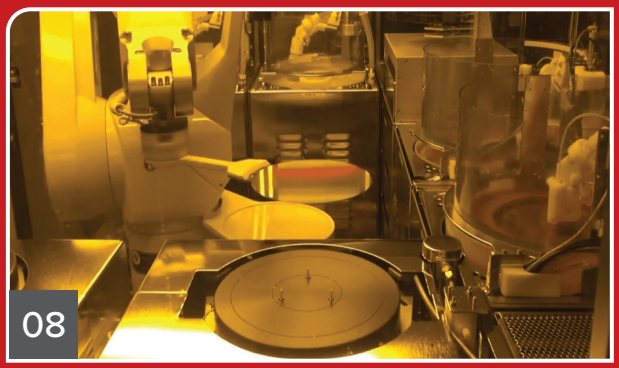

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Editor Richard Stevenson
richardstevenson@angelbc.com
+44 (0)1291 629640

News Editor Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Director of Logistics Sharon Cowley
sharon.cowley@angelbc.com
+44 (0)1923 690200

Senior Sales Executive
Jacob Caulfield
jacob.caulfield@angelbc.com
+44 (0)2476 718979

Senior Logistics Executive
Eve O'Sullivan
+44 (0)2476 823 123
eve.osullivan@angelbc.com

Circulation
Scott Adams
scott.adams@angelbc.com

Publisher Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

Chief Executive Officer
Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

Chief Technical Officer
Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Directors
Jackie Cannon
Sharon Cowley

Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

Bosch nets $225 million for US SiC fab

Proposed project could comprise more than 40 percent of all US-based SiC device manufacturing capacity

THE Department of Commerce has signed a preliminary memorandum of terms with Bosch to provide proposed funding of $225 million to expand the company's SiC, factory in Roseville, California.

Under the agreement, the United States would support Bosch's investment of $1.9 billion to modernise its SiC manufacturing facility under the CHIPS and Science Act, enabling the company to produce chips on 200 mm wafers starting in 2026, the Commerce Department said.

This funding would support the expansion of Bosch's largest SiC device factory globally, which would significantly increase the company's production capacity and create up to 1,000 construction jobs and up to 700 manufacturing, engineering, and research and development jobs in California.

When at full capacity, the project is expected to produce the majority of Bosch's total capacity of SiC semiconductors and could comprise more than 40 percent of all US-based SiC device manufacturing capacity.

Bosch, a tier 1 automotive supplier, is differentiated by having specialised semiconductor business within its portfolio. In addition, Bosch is a leading provider of trench gate SiC semiconductors for the car industry.

"The Roseville investment enables Bosch to locally produce SiC semiconductors, supporting US consumers on the path to electrification," said Paul Thomas, president of Bosch in North America and Bosch Mobility Americas. "Producing this key technology in the US underscores our leadership in the mobility market."

Bosch expects to produce its first chips on 200 mm wafers in its Roseville facility starting in 2026. The facility will perform both front-end device manufacturing and backend testing, sorting and dicing processes.

Imec makes breakthrough with GaAs lasers on silicon

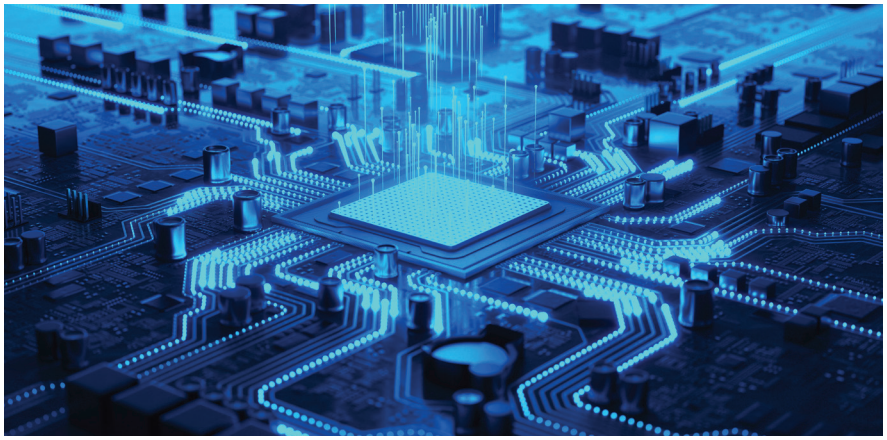
Fabrication of electrically-pumped nano-ridge lasers on 300 mm wafers highlights the potential of direct epitaxial growth of III-V materials on silicon

BELGIAN research organisation Imec has announced a significant milestone in silicon photonics with the successful demonstration of electrically-driven GaAs-based multi-quantum-well nano-ridge laser diodes fully, monolithically fabricated on 300 mm silicon wafers in its CMOS pilot prototyping line.

Achieving room-temperature continuous-wave lasing with threshold currents as low as 5 mA and output powers exceeding 1 mW, the results, detailed in *Nature*, demonstrate the potential of direct epitaxial growth of high-quality III-V materials on silicon. This breakthrough provides a pathway to the development of cost-effective, high-performance optical devices for applications in data communications, machine learning and artificial intelligence, according to Imec.

The lack of highly scalable, native CMOS-integrated light sources has been a major roadblock for the widespread adoption of silicon photonics. Hybrid or heterogeneous integration solutions, such as flip-chip, micro-transfer printing or die-to-wafer bonding, involve complex bonding processes or the need for expensive III-V substrates, which are often discarded after processing. This not only increases costs but also raises concerns about sustainability and resource efficiency. For that reason, the direct epitaxial growth of high-quality III-V optical gain materials selectively on large-size silicon photonics wafers remains a highly sought-after objective.

The large mismatch in crystal lattice parameters and thermal expansion coefficients between III-V and silicon materials inevitably initiates the formation of crystal misfit defects, which are known to deteriorate laser performance and reliability. Selective-area growth (SAG) combined with aspect-ratio trapping (ART) significantly reduces defects in III-V materials integrated on silicon by confining misfit dislocations within narrow trenches etched in a dielectric mask.



"Over the past years, Imec has pioneered nano-ridge engineering, a technique that builds on SAG and ART to grow low-defectivity III-V nano-ridges outside the trenches. This approach not only further reduces defects, but also enables precise control over material dimensions and composition. Our optimised nano-ridge structures typically feature threading dislocation densities well below 10^5 cm^{-2}. Now, Imec exploited the III-V nano-ridge engineering concept to demonstrate the first full wafer-scale fabrication of electrically pumped GaAs-based lasers on standard 300 mm silicon wafers, entirely within a CMOS pilot manufacturing line," says Bernardette Kunert, scientific director at Imec.

Leveraging the low-defectivity GaAs nano-ridge structures, the lasers integrate InGaAs multiple quantum wells as the optical gain region, embedded in an *in-situ* doped *p-i-n* diode and passivated with an InGaP capping layer. Achieving room-temperature, continuous-wave operation with electrical injection is a major advancement, overcoming challenges in current delivery and interface engineering. The devices show lasing at around 1020 nm with threshold currents as low as 5 mA, slope efficiencies up to 0.5 W A^{-1}, and optical powers reaching 1.75 mW, showcasing a scalable pathway for high-performance silicon-integrated light sources.

"The cost-effective integration of high-quality III-V gain materials on large-diameter silicon wafers is a key enabler for next-generation silicon photonics applications. These exciting nano-ridge laser results represent a significant milestone in using direct epitaxial growth for monolithic III-V integration," said Joris Van Campenhout, fellow Silicon Photonics and director of the industry-affiliation R&D program on Optical I/O at Imec.

This project is part of a larger pathfinding mission at Imec to advance III-V integration processes towards higher technological readiness, from flip-chip and transfer-printing hybrid techniques in the near term, over heterogeneous wafer- and die-bonding technologies and eventually direct epitaxial growth in the longer term.

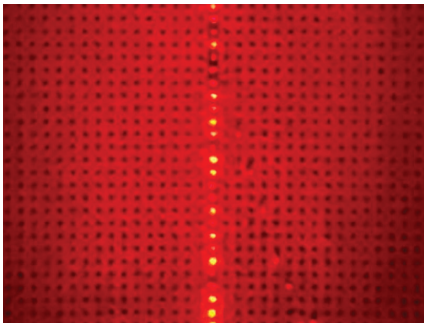
Polar Light Tech makes microLED breakthrough

Red pyramidal microLED is based on the same material as green and blue

SWEDEN-BASED Polar Light Technologies has realised red light of 625 nm based on its non-etching bottom-up concept. This means the company has built red, green, and blue pyramidal microLEDs using the same material compound.

The pyramidal design has the ability to be manufacturable while maintaining excellent microLED performance, laying the foundation for monolithic RGB displays, according to Polar.

Blue and green microLEDs have been in the market for years, but reaching a red colour has been difficult, due to fundamental challenges in the material properties. There are several workarounds or alternatives for reaching a red colour, but they all come with some compromises, such as efficiency, manufacturability, or the need to integrate with other material systems.



"Pursuing Polar Lights' innovative pyramidal LED concept has been about overcoming those challenges without compromises. Thanks to a great tech team, we have succeeded in realizing the red-emitting microLEDs based on our innovative pyramidal structure", says Lisa Rullik, CTO of Polar Light Technologies.

Polar Light Technologies' microLED is composed of pyramid shapes that are built with a novel bottom-up approach, a technology that has a number of benefits, according to the company.

One is that the inevitable strain in the lattice-mismatched InGaN/GaN structures is reduced, which is important to be able to manufacture blue, green, and red microLEDs with the same material system, that is, to build monolithic RGB.

The approach also makes it possible to integrate the frontplane with a backplane.

In addition, no etching is needed, which means performance is maintained for smaller dimensions, since no etching damages occur.

Other benefits are that it enables nanoLEDs, it is easier to manufacture and integrate with CMOS and TFT, and it there is a narrow emission cone, which is important for microprojectors.

Rohm develops 1 kW class infrared laser diode

ROHM has developed a high output infrared laser diode – RLD8BQAB3 – for use in Advanced Driver Assistance Systems (ADAS) equipped with lidar for distance measurement and spatial recognition.

The 125 W, 8 channel (1 kW class) array-type product is the latest in a range of devices based on patented technology to achieve the narrow emission width of lasers, enhancing long-distance, high accuracy lidar.

Rohm will initially start supplying samples for consumer and industrial applications, such as drones, robot vacuum cleaners, automated guided vehicles, and service robots.

Lidar is seeing growing adoption in recent years across a variety of applications that require automation.

But to detect information at greater distances with more accuracy, there is a need for laser diodes that serve as light sources to achieve high kilowatt-level output while allowing multiple light sources to emit light at close intervals.

The RLD8BQAB3 is an ultra-compact surface mount device designed for lidar applications that use 3D time-of-flight systems to carry out distance measurement and spatial recognition. The optimised design features eight emission areas (each 300 μm wide) per element, installed on a submount affixed to a high heat dissipation substrate.

The package's emitting surface incorporates a clear glass cap – an industry first for a surface mount laser diode – eliminating the risk of light scattering caused by scratches during dicing that tends to occur with resin-encapsulated products, ensuring high beam quality.

Each emission area is wired with a common cathode, enabling the selection of the irradiation method based on application needs – ranging from individual emission that increases the number of light-emitting points to industry-leading simultaneous emission at ultra-high outputs of 1 kW class.

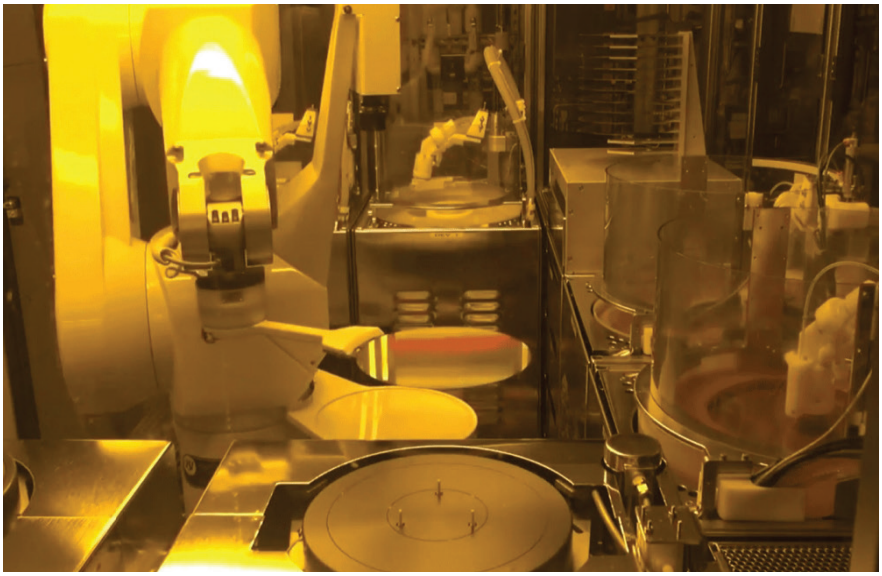
The new product retains the key features of Rohm's conventional laser diodes, including uniform emission intensity across the emission width.

On top of that, the array configuration narrows the regions of reduced emission intensity between channels, while the bandpass filter minimises the effects of ambient light noise from the sun and other sources.

GF gets $9.5million for GaN chip production

Funding moves GF closer to large-scale production of next-gen GaN chips for RF and high-power applications

GLOBALFOUNDRIES (GF) has received an additional $9.5 million in federal funding from the US government to advance the manufacturing of GF's essential GaN-on-silicon semiconductors at its facility in Essex Junction, Vermont.



The funding moves GF closer to large-scale production of GaN chips.

With the award, GF will continue to add new tools, equipment and prototyping capabilities to its market-leading GaN IP portfolio and reliability testing as the company moves closer to full-scale manufacturing of its 200 mm GaN chips in Vermont.

"GF is proud of its leadership in GaN chip technology, which is positioned to make game-changing advances across multiple end-markets and enable new generations of devices with more energy-efficient RF performance and faster-charging, longer-lasting batteries," said Nicholas Sergeant, VP of IoT and aerospace and defence at GF.

"We appreciate the US government's partnership and ongoing support of our GaN programme. Realising full-scale GaN chip manufacturing will be a catalyst for innovation, for both our commercial and government partners, and will add resilience and strengthen the semiconductor supply chain."

The new funding, awarded by the US Department of defence's Trusted Access Program Office (TAPO), represents the latest federal investment to support GF's GaN programme in Vermont.

"This strategic investment in critical technologies strengthens our domestic ecosystem and national security, and ensures these assets are readily available and secure for DoD utilisation.

In concert with key partners, this approach fortifies defence systems, empowering resilience and responsiveness," said Nicholas Martin, director at defence Microelectronics Activity. In total, including the new award, GF has received more than $80 million since 2020 from the US government to support research, development and advancements to pave the way to full-scale GaN chip manufacturing.

EU project to develop high-voltage DC WBG tech

‘MoWiLife’ project to produce SiC and ultra-wide-bandgap devices for DC wind and solar energy applications

A NEW three-year multi-partner Horizon Europe funded project, called MoWiLife (Condition Monitoring and Wide Bandgap Power Electronics – Leading Innovations for the European Energy Sector), will be working on technology for DC wind and solar energy applications.

This includes the development of a 2.3 kV SiC MOSFET with temperature sensing and self-protection features. Additionally, the project explores the potential of ultra-high voltage and ultra-wide bandgap semiconductors, including diamonds as semiconductor materials, for energy savings.

The project features two wind energy converter pilots and two university-developed pilots: a TRL 5 DC-DC converter and a TRL 5 DC circuit breaker.

The basis for the four pilots is the 2.3 kV SiC MOSFET, which will be developed by project partner Infineon. It includes a source-gate *p-i-n* diode, whose on-state voltage has a strong temperature dependence and can be read out by the gate drive, which will be developed by Rostock University. In addition, self-protection features will be integrated into the SiC chip for robustness and direct water cooling will be realised for higher output power.

The two wind energy converter pilots are being realised by two industrial partners. A leader in wind energy, Vestas – supported by University of Aalborg – will develop a TRL 6 SiC converter with +20 percent power density and digital-twin Condition and Health Monitoring. The start-up RKL, together with Rostock University, will develop a TRL 5 wind energy power stack with Condition and Health Monitoring based on online chip temperature and on-state voltage measurement.

Solar medium-voltage DC collection grids and meshed high-voltage transmission grids will play an important role in the future. As third and fourth pilots, a TRL 5 DC-DC converter and a TRL 5 DC circuit breaker, including condition monitoring, are being developed by the MoWiLife university partners KTH Stockholm and the University of Aberdeen.

The Aberdeen HVDC research team will be responsible for developing and validating a functional SiC MOSFET hybrid high-voltage DC circuit breaker, which builds on previous research projects at Aberdeen.

Jovcic said: “DC electrical systems have not been much utilised since AC systems have been preferred with traditional overland power transmission and conventional electricity generation. However, AC power can only be transmitted over relatively short distances with subsea cables, and as we look increasingly to offshore wind or tidal technology to meet growing demand, solutions are needed to create high-voltage DC connections and to eventually develop an HVDC grid.”

US ITC says Innoscience infringed EPC GaN patent

EFFICIENT POWER CONVERSION (EPC) has announced the conclusion of the Presidential review period for the US International Trade Commission’s (ITC) final determination, affirming that Chinese GaN firm Innoscience infringed EPC’s foundational patent for GaN technology.

The ITC’s decision is now final, implementing an import and sales ban on Innoscience products in the United States without a license from EPC. “This ruling marks a milestone for EPC and fair competition in GaN technology,” said Alex Lidow, CEO and co-Founder of EPC. “We will safeguard our IP to drive innovation and support our customers in shaping the future of power electronics.”

EPC’s case against Innoscience began in May 2023, culminating in the ITC’s final determination issued in July 2024. EPC’s intellectual property has been consistently upheld across multiple jurisdictions, including the China National Intellectual Property Administration’s decisions in April and May 2024.

EPC says this decision opens new pathways for it to expand access to its technology through licensing agreements, fostering collaboration and innovation with global partners.

Aixtron opens innovation centre

Company prepares for transition to 300 mm wafers for GaN and other compound semiconductor applications

MONA NEUBAUR, Minister for Economic Affairs of the State of North Rhine-Westphalia, Germany, has opened Aixtron's new Innovation Centre at the company's headquarters in Herzogenrath.

The high-tech building is designed for the next big step in compound semiconductor technology: the transition to 300 mm wafers for GaN and other compound semiconductor applications.

The larger wafer size offers customers the productivity gain of 2.25 times more wafer area compared with the currently used 200 mm wafers.

Furthermore, customers can use their 300 mm fabs and processing equipment for the first time for compound semiconductors. This will make the production of GaN semiconductor devices not only more cost-effective, but offer opportunities to technology performance gains in the future.

"With the new 300 mm-capable cleanroom at the Innovation Centre, we will further expand our technological market leadership," said Aixtron CEO Felix Grawert. "We already have the first 300 mm GaN prototype systems, which have also been integrated into pilot lines at several customers. And this is precisely where Aixtron's innovative strength and DNA come into play."

"With 300 mm wafer technology, we are bringing compound semiconductors for the first time into the mainstream of the semiconductor fabrication. The Innovation Center is a major element of our strategy, providing space and capabilities for next-generation technologies. The step towards 300 mm in compound semiconductors is a landmark milestone, that is set to trigger numerous growth options for the industry in the years to come." explains Michael Heuken, VP of Advanced Technologies at Aixtron.

Neubaur said: "Aixtron's new innovation centre is an impressive example of the innovative strength and future viability of the semiconductor industry in North Rhine-Westphalia. The launch of 300 mm wafer technology is a milestone for the energy efficiency and competitiveness of our region. Our global competitiveness benefits enormously from robust domestic semiconductor production, because semiconductors are essential for the transformation towards climate neutrality: without them, no computer would run, no car would drive, and neither wind nor solar plants could produce energy."

Pictured from left to right: Benjamin Fadavian, Felix Grawert, Mona Neubaur, Christian Danninger

XDC and Lumileds develop novel 140 pixel-per-inch microLED display

High assembly yield of 13 x 20 μm^2 LEDs and microICs demonstrate readiness for volume production

X DISPLAY COMPANY (XDC), a developer of semiconductor devices for displays, and LED company Lumileds, have developed a 140 pixels-per-inch (ppi) microIC-driven microLED prototype display.

MicroICs are an XDC innovation that integrate the display driver with the emitters, replacing the traditional TFT backplane to bring benefits in power consumption and visual performance.

The companies describe the novel display technology as a milestone for microLED displays in mobile consumer applications including smartwatches, smartphones, tablets, and PCs.

“We see a lot of potential for microLED displays in mobile consumer electronic devices” said Ross Young, CEO of DSCC. “This XDC and Lumileds breakthrough will improve the cost, power, and brightness display profile significantly and help accelerate adoption of these technologies.”

The new microLED display has an architecture based on a cluster drive system combined with microLEDs that measure 13x20 μm^2. The result is a peak brightness of 2360 cd m^{-2}. Notably, the mass transfer process employed in the development of these prototypes achieves 99.9998 percent microLED sub-pixel yield and a 99.992 percent percent microIC transfer yield, according to the partners. The processes used to manufacture the prototype are mass-production ready.

“XDC’s mass transfer, bonding, and display driving technologies have created new opportunities to transform the world of displays,” said Brendan Moran, senior director of Display Technology at Lumileds. “Lumileds has successfully implemented XDC’s transfer-ready microLED technology into our volume production LED fabrication facilities. Together, we are setting new standards in the microLED industry and advancing mobile display technology.”

“This milestone is made possible by Lumileds’s device expertise and manufacturing process discipline applied from the very start. The result is repeatable, high-quality microLED displays,” said Matt Meitl, EVP and co-founder of XDC. “Our long collaboration has resulted in microLED displays sought by customers in the mobile device space.”

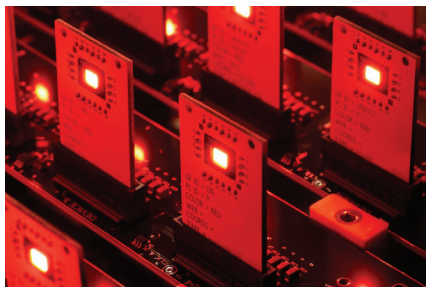
The microICs, microLEDs, and the transfer equipment used in this prototype can be deployed for interested customers.

Plessey and Meta announce brightest red microLED display

PLESSEY SEMICONDUCTORS and Meta Platforms have announced the development of what they claim is the world’s brightest red microLED display suitable for augmented reality (AR) glasses.

The display offers a brightness up to 6 milion nits at high resolution (<5 μm) with low power consumption – overcoming critical technical challenges that will help pave the way for the next computing platform.

This achievement follows Meta’s recent announcement of the Orion AR glasses prototype. Orion combines the look and feel of a regular pair of glasses with the immersive capabilities of AR due to its 70-degree field of view, SiC



high-performance waveguides, custom silicon, microLED projectors, integrated input system, and more.

As part of its long-term agreement, Plessey is continuing to work with Meta by dedicating its manufacturing operations to support the development of prototypes and new technologies for potential use in the XR category.

Jason Hartlove, VP of Display and Optics, Meta’s Reality Labs, said: “Our work with Plessey has pushed the boundaries of what’s previously been possible, and it’s only the beginning – the future is starting to look up.”

Keith Strickland, CEO of Plessey added: “Plessey is proud to be working alongside Meta to drive the development of microLED display technology. The collaboration between Meta and Plessey has delivered a major breakthrough in the development of AR technology, and we are excited to see the impact that this innovation will have on the industry. With the world’s brightest red microLED display, we are one major step closer to making AR glasses a mainstream reality.”

IQE and Quintessent partner on QD lasers for AI

Partners establish commercial quantum dot epitaxial wafer supply chain for AI optical interconnects

COMPOUND SEMICONDUCTOR wafer company IQE has strengthened its partnership with Quintessent, a pioneer in quantum dot laser technology and heterogeneous silicon photonics, to establish the world's first large-scale quantum dot laser (QDL) and semiconductor optical amplifier (SOA) epitaxial wafer supply chain.

This milestone is backed by an initial purchase order of $0.5m for delivery of production wafers to Quintessent through 2025.

The rapid expansion of AI-driven applications has placed significant requirement in data centres power consumption driving the migration from copper chip to chip connectivity to silicon photonics. This has created an increasing demand for high-bandwidth, low-latency, energy-efficient and highly reliable optical interconnects.

Traditional laser technologies struggle to meet these requirements, making QDLs and SOAs a critical innovation for future AI infrastructure which offer superior performance, including extended lifetimes, improved efficiency, lower noise and greater resilience to environmental fluctuations.

IQE and Quintessent have collaborated for over a decade to transition QDL technology from research to large-scale production. Building on research breakthroughs from John Bower's laboratory at the University of California, Santa Barbara, the partnership has successfully developed highly optimised and high performing gain GaAs-based quantum dot epitaxial wafers on 6-inch substrates versus state of the art 4-inch art InP lasers.

This achievement enables the production of hundreds of millions of high-performance edge-emitting lasers annually, according to the companies. Jutta Meier, Interim CEO and CFO of IQE, commented: "IQE is proud to strengthen our long-standing partnership with Quintessent, driving the commercialisation of QDL technology. This commitment highlights our expertise in high-volume epitaxial wafer manufacturing and our proven ability to scale innovative semiconductor solutions into production. Our collaboration, spanning commercial products and DoD programs has delivered QDL wafers with exceptional reproducibility and lasing performance"

Alan Liu, CEO and co-founder, Quintessent, said: "The performance, cost, and reliability advantages that quantum dot-based lasers and amplifiers enable over their quantum well counterparts are exactly what our customers are demanding to address the soaring need for optical connectivity in AI driven compute. Through our partnership with IQE, we have brought this transformative technology to scale, positioning us to be the leader in delivering solutions leveraging quantum dot laser and SOA technology."

'Game-changing' VCSEL system targets clinical imaging

TRUMPF PHOTONIC COMPONENTS, a maker of VCSELs for industrial and consumer sensing, and iThera Medical are introducing a solution for optoacoustic imaging for clinical applications, which they will demo at Photonics West in San Francisco, 28 – 30 January 2025.

The photonic subsystem presented is based on a compact set-up of high power VCSEL arrays and bare ToF CMOS driver chips. The heat dissipation can be buffered in a small copper block, so the subsystem can be directly mounted within a medical handheld device with no active cooling.

According to Trumpf, the subsystem can replace current photonic systems and is described as a "game changer for routine clinical use", starting with soft tissue perfusion and oxygenation measurements, applicable to a wide range of diseases.

"The power-efficient and compact photonic solution of Trumpf and iThera is scalable and paves the way towards future patch and sensor optoacoustic applications. The VCSEL technology, with its benefits like precision, compact structure, energy efficiency and wide range of wavelengths is perfect for this application," said Alexander Weigl, head of product management at Trumpf Photonic Components. "At Trumpf Photonic Components, we view the medical technology and life sciences sector as a growth area for numerous VCSEL wavelengths and applications," he added.
"Using VCSELs will allow us to cut light-source-related costs, volume and power consumption of our market-leading optoacoustic imaging devices by a factor of 100," explained Patrick Leisching, CTO at iThera Medical GmbH.

"Additionally, compared with the currently used tunable solid-state lasers, the VCSEL subsystem results in a downgrade of the laser safety classification from its current Class 4 to Class 1, eliminating the need for special safety measures, and it will provide a substantially improved operating stability," he commented. "These game-changing improvements will facilitate the translation of our technology from research into routine diagnostic use and also enable future sensing applications, making optoacoustic technology widely accessible across different care settings," he said.

300 mm SiC: A format for when?

Is the unveiling of a 300 mm SiC substrate by SICC going to drive a relatively rapid shift to high-volume production with this format?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THOSE in our industry will probably remember the recent *Electronica* for the unveiling of the world's first 300 mm SiC substrate. This breakthrough, showcased to the world in mid-November from Munich, Germany, is undoubtedly a great demonstration of technical prowess. But is it going to have an impact in an industry that is only just starting to make the transition from 150 mm to 200 mm SiC lines?

Some may argue that this triumph, realised by one of the world's biggest manufacturers of SiC, SICC of Jinan, China, is of little relevance in the near term, but the trailblazer sees the situation differently.

Speaking of its behalf, Chairman Yanming Zong told *Compound Semiconductor* that one of the purposes behind this demonstration is the promotion of industrialisation of 300 mm SiC. While the rate of technical progress and the level of demand for this new format will influence the precise timing of SICC's commercialisation of 300 mm *n*-type SiC substrates, the anticipation is that small production volumes will begin in 2027.

At this stage, it's unclear which chipmakers will be keen to buy this new format. However, Zong believes that some of the leading makers of SiC devices may be willing to invest in upgrading their lines to trim costs, and he points out that some start-ups may see the benefit of beginning with larger wafers.

For all those making SiC devices, weighing on production costs is the slow growth rate of the boules, which are sliced to form substrates.

"We want to continuously reduce the cost of material per unit area by expanding the substrate size," remarks Zong, who hopes that one of the consequences of introducing larger wafers will be an increase in the bang-per-buck of SiC devices.

Swift scaling

Founded in 2010, SICC, which focuses on the R&D, production and sales of SiC substrate material, used equipment designed and installed by its R&D team to produce the record-breaking substrates. This multicultural, highly qualified team took just

18 months to enlarge its *n*-type boules from 200 mm to 300 mm.

The ground-breaking enlarged boule, produced using the same axial growth rate employed for manufacturing of 200 mm material, has a thickness of around 20 mm. From this ingot, it is possible to slice around 25 to 35 wafers with a thickness of 500 μm. And as the team refines its process, it will be possible to produce thicker boules that yield more wafers.

Historically, SiC substrates have been plagued with a variety of imperfections that degrade and even kill devices. However, those issues have now been addressed by many companies, and as the process that's used to fabricate the 300 mm substrate is the same as that used to produce smaller wafers, there is no major barrier to realising state-of-the-art quality with the larger format.

Encouragingly, one of the critical defects, the micropipe, is not a significant issue in SICC's *n*-type 300 mm substrate. With further development, micropipe density is forecast to fall to below 0.2 cm^{-2}, which is a degree of prevalence found in the company's 200 mm *n*-type SiC.

Of more concern are basal plane dislocations. However, while this class of defect needs to be reduced, the company is confident it can replicate the density found on its 200 mm *n*-type substrates.

Efforts will not have to be directed at improving surface roughness. SICC's 300 mm substrate has a roughness of just 0.2 nm, a figure comparable to that for the company's 200 mm wafers.

One of the next steps on the road to commercialisation is the verification of the quality of the epilayers produced on 300 mm substrates. Today, none of the suppliers of MOCVD reactors have tools designed to accommodate this size. However, Zong argues that they will have anticipated the unveiling of this format, and he does not expect tool availability to hold back progress.

The *n*-type 300 mm format that SICC is pioneering is suitable for producing power devices that operate at high voltages and high frequencies and are deployed in inverters and electric vehicles.

As well as being the world's second biggest producer of *n*-type SiC, SICC has other SiC-related products in its portfolio, including a heat dissipation SiC bare product that is said to combine exceptional thermal stability with ultra-high thermal conductivity.

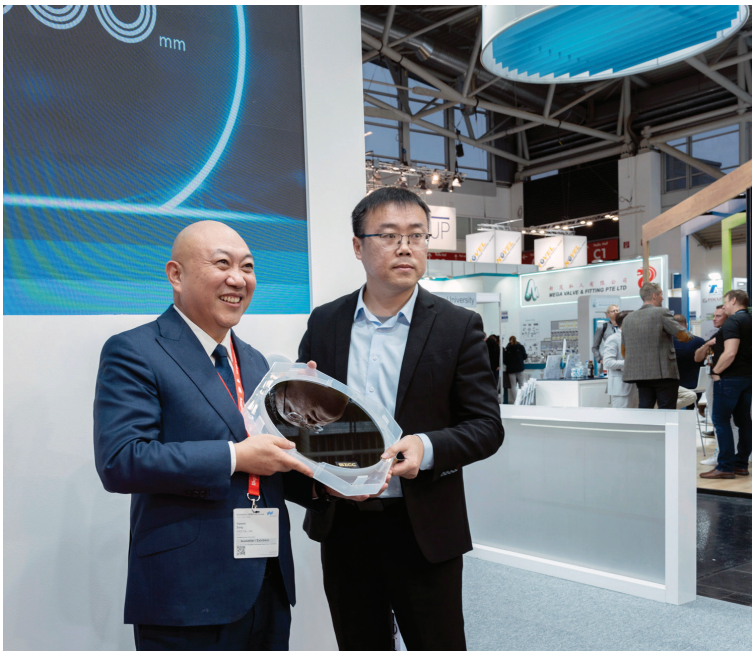
For the last five years SICC has been the third largest producer of semi-insulating SiC, a popular platform for RF products. It also offers *p*-type SiC, the ideal platform for producing bipolar SiC IGBTs, which are attractive candidates for deployment in high-power electronic systems, such as smart grids – they require devices than can handle 10 kV or more.

SICC also offers *p*-type SiC, the ideal platform for producing bipolar SiC IGBTs, which are attractive candidates for deployment in high-power electronic systems, such as smart grids – they require devices than can handle 10 kV or more

A novel growth process

To address concerns related to cost, high resistivity and defect control with *p*-type SiC, SICC has pursued and mastered an alternative growth technology to the standard approach, physical vapour transport. By turning to top-seeded solution growth, the company has been able to produced *p*-type substrates with low threading dislocations, zero stacking faults, and a uniform resistivity that's below 200 mΩ cm. These substrates have an off-cut of 4°.

To increase its capacity for producing 200 mm SiC wafers, SICC is now investing in its facility in Shanghai. This will help to satisfy the global demand for 200 mm SiC substrates. That's clearly going to be the leading format for the next few years, but beyond then there may be the introduction of 300 mm variants, thanks to the recent efforts of SICC.



➤ SICC unveiled its record-breaking 300 mm SiC *n*-type substrate at Electronica, held in Munich, Germany, in mid-November. On the left is the company's Chairman Yanming Zong, and on the right its CTO, Chao Gao.

Going through the gears with gallium nitride

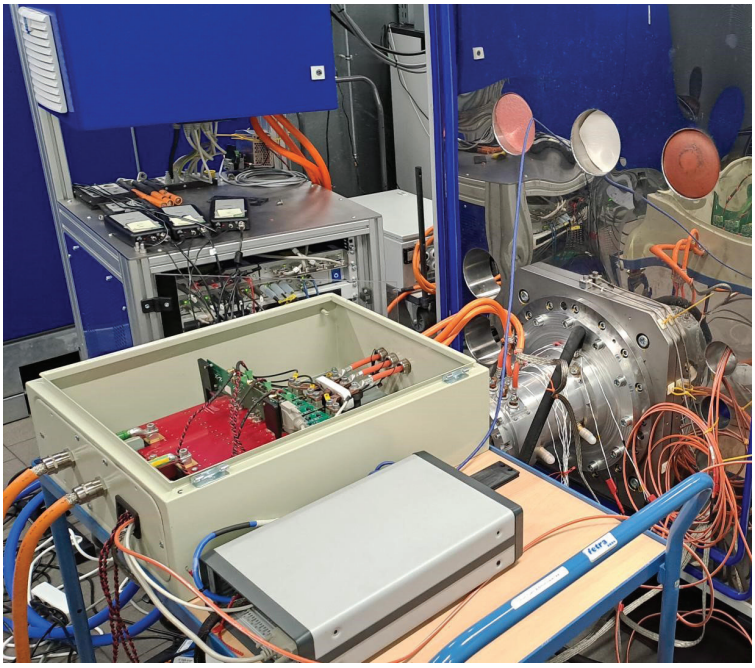
VisIC plans to ramp production of its GaN depletion-mode HEMTs for electric vehicle inverters before the end of this decade

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

DESIGNERS of electric vehicles are facing a dilemma when selecting the power electronics for their drive trains. To trim the bill of materials, they favour the use of the silicon IGBT. But this transistor fails to offer the efficiency of the pricier SiC MOSFET, which ensures a greater driving range for the automobile, an attribute that has spurred the commercial success of this class of transistor.

Due to these awkward trade-offs, designers of EVs will be enthralled by the tantalising prospect of a power transistor that delivers a performance on par with that of the SiC MOSFET, but for a price comparable with that of the silicon IGBT.

Preparing to offer just that in significant volume within the next few years is the Israeli-based producer of GaN power devices, VisIC Technologies, which is working in partnership with AVL, one of the leading developers, simulators and testers of many forms of green transportation.



AVL Dyno test setup with a VisIC D3GAN power inverter.

"We can really push the boundaries and technology with AVL," enthuses Dieter Liesabeths, Senior Vice President of Product at VisIC. He says that this partner excels in software knowledge and hardware experience, and will provide great support in the development of highly integrated inverters. "They also have the capability to go to a very high RPM with their motors, up to 30,000 RPM, which is really benefiting the GaN technology."

In December 2024, VisIC and AVL reported efficiencies for their inverter of 99.67 percent and 99.8 percent at 10 kHz and 5 kHz, respectively. These values for efficiency are said to be up to 0.5 percent higher than those for SiC inverters, an improvement that ensures a trimming of energy loss by more than 60 percent.

The partnership between VisIC and AVL determined these efficiencies by testing their inverter under 400 V, a voltage that's used in many city-type cars, as well as those made by Tesla.

Despite much interest is moving EVs to 800 V, these results are incredibly relevant, argues Liesabeths: "The majority of cars that will come out in the future will be 400 volts, because these are typical city-cycle cars, which are having smaller batteries."

For these EVs, most driving is in urban areas, where the typical average speed is around just 25 km hr^{-1}. At these modest speeds, the load condition on the inverter is relatively low, and this drags down the efficiency of inverters with VisIC's HEMTs to 99.2 percent. However, that's still better than that for inverters based on SiC operating at higher loads, thanks in part to the vanishingly small switching losses for GaN.

The GaN HEMT also has the upper hand in terms of price, costing about half that of the SiC MOSFET. The GaN HEMT is still about 20 percent more expensive than the silicon IGBT, but if the former were to be produced using 300 mm wafers, cost-parity with silicon might be within reach, thanks to the smaller size of the die.

Note that lower chip costs are a big deal for makers of EVs. “If you can replace silicon carbide, which is around 55 to 60 percent of the cost of the invertor, with gallium nitride, you’re cutting your cost almost by half,” says Liesabeths.

In addition, replacing SiC MOSFETs with GaN HEMTs ensures a substantial reduction in carbon footprint, as producing the former involves very high temperatures.

Depletion-mode devices

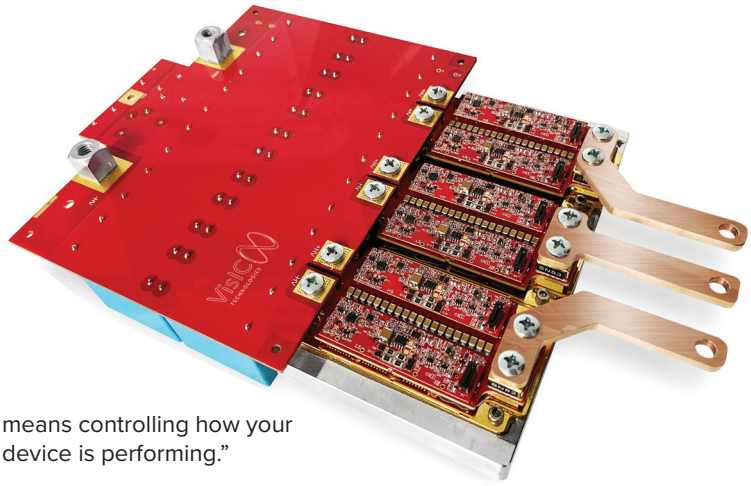
VisIC differentiates itself from its rivals with a patented D-mode HEMT technology, pairing its depletion-mode GaN transistor in series with a silicon MOSFET.

It’s a novel configuration that enables direct driving of the GaN transistor, thereby avoiding losses that come from switching the silicon MOSFET; and it allows control over the slew rate, leading to greater robustness at the system level. What’s more, the company’s D-Mode technology offers a superior dollar-per-amp, as this form of HEMT can be smaller than its enhancement-mode cousin.

Many producers of GaN HEMTs partner with 200 mm foundries, which were in very high demand during the pandemic. However, this constraint has now eased, says Liesabeths, who can’t see any difficulties or bottlenecks in the future for GaN. He points out that foundries offering GaN power electronic technologies are increasing their capacity, and those dedicated to silicon are branching out into GaN.

Initially, VisIC partnered with TSMC, which can handle all steps of production, by producing GaN-on-silicon epiwafers and process them into HEMTs. But now VisIC is also starting to investigate an alternative supply chain, involving independent epiwafer specialists, as well as foundries that process this material into devices.

“Working with dedicated epi-partners means that we have better control, and more influence about the design itself,” says Liesabeths. “The quality is the key differentiator here, because controlling epi means controlling how your device is performing.”



➤ VisIC D3GAN 3-phase VM022 Gen 1 Power Core system.

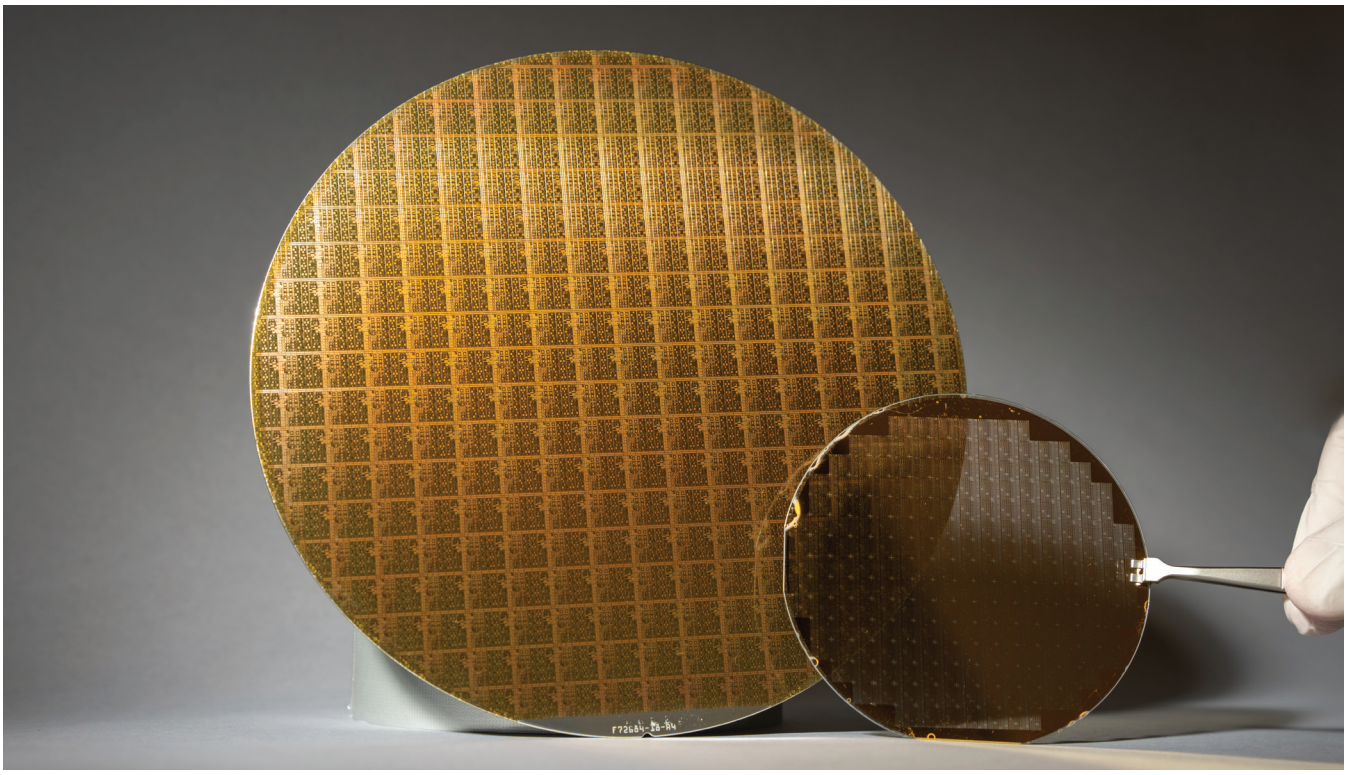
Power modules based on ViSIC’s HEMTs are now undergoing full qualification, under the AEC-Q101 and AQG-324 criteria used in the automotive industry to verify reliability.

“We are confident that we are passing this qualification and even exceeding some of the requirements,” says Liesabeths.

Looking ahead, plans for the partnership include developing very high-power inverters, operating in the 300 kW range, and demonstrating variants around 100-120 kW, suitable for city cars. Liesabeths says that accomplishing all of this will show that GaN is viable for “both ends of the spectrum”.

For VisIC, another target is to produce GaN HEMTs for EVs in high-volume by 2028-29. “We are confident that by this time frame, we will see the first cars on the road,” says Liesabeths, who is helping to lay the foundations for this success, via ongoing work with OEMs and tier ones.

If and when the EV industry moves to higher voltages, VisIC is well-prepared with its patented multi-channel devices that can handle up to 3.3 kV. “We were not utilising [this technology] so far, because we first want to demonstrate a viable solution for 400 volts,” says Liesabeths. But his co-workers are developing 800 V devices for market, slated for release within the next two years.

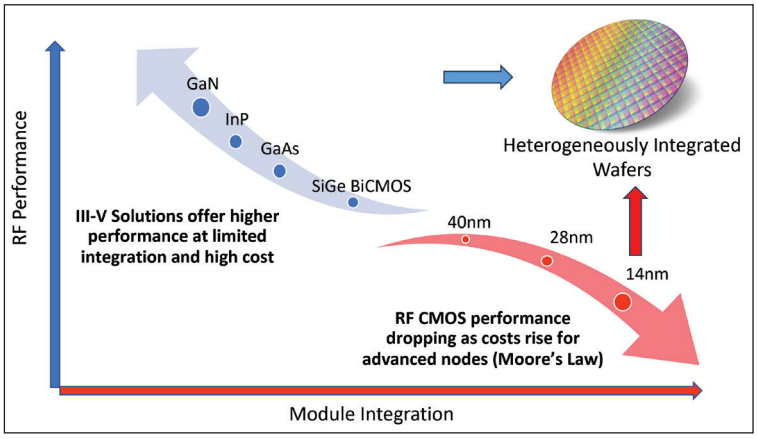


Say hello to the heterogeneous revolution

Recent advances in circuits produced by heterogeneous integration highlight the potential for real world applications

BY CHRISTOPHER MAXEY, JUSTIN KIM, DAVE HODGE, MARK SOLER, BENNETT COY, DAN GREEN, JAMES BUCKWALTER AND FLORIAN HERRAULT FROM PSEUDOLITHIC INC.

SINCE the advent of VLSI silicon CMOS, this technology's RF and millimetre-wave performance has taken a back seat during the inexorable drive towards smaller gate dimensions and higher device density. Stepping up to fill this gap have been a number of compound semiconductors, such as GaAs, GaN, and InP, providing high gain and high output powers at ever higher frequencies. Thanks to these devices, it has been possible to construct solid-state phased-array radars, 5G/6G base-stations and quantum computers. However, these applications pay a significant price in an ecosystem where many may see 'exotic' materials as an issue that slows and restricts adoption. Compared to silicon CMOS, it typically takes twice as long to fabricate compound semiconductor devices, which are 5 to 10 times as expensive per unit area, because they lack the fundamental economic benefits of high-volume manufacturing.



➤ Figure 1. Silicon CMOS and compound semiconductors provide unique benefits, while heterogeneous integration promises to deliver the best of both worlds.

One attractive solution to addressing this issue is heterogeneous integration. Many are now investigating this approach that combines the disparate benefits of multiple technologies into a single integrated circuit (see Figure 1). Here, we review the rise in interest in heterogeneous integration, its progress in the context of the historical evolution of semiconductor technologies, and the potential inflection it offers to accelerate deployment of new devices into the marketplace. We also describe the contribution that our company,

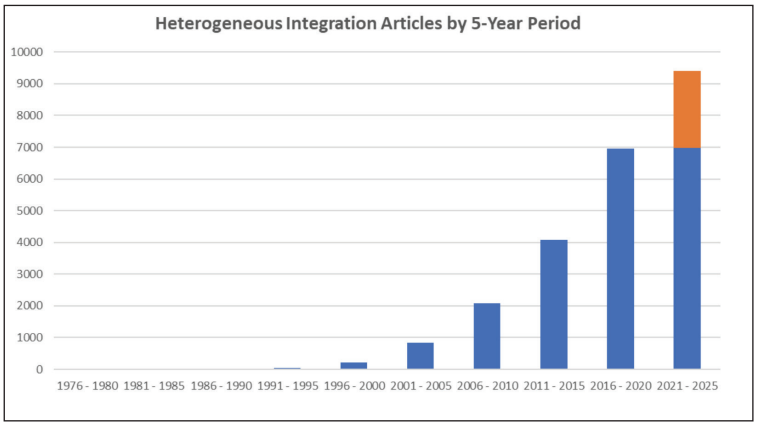
PseudolithIC, is making – we are the pioneers of a number of 'first-ever' prototype designs, including the world's first millimetre-wave amplifier based on InP and GaN devices.

HI primed for impact

Evidence of accelerating interest in heterogeneous integration is found in increases in journal articles and patent filings over the last three decades (see Figure 2). At the turn of the millennium heterogeneous integration started to take shape as a *bone fide* topic, and since then there has been a steady rise in publications continuing to the present day. Alongside this trend, there has been a multiplication in both the number of potential approaches to realising integrated solutions, and the potential applications for heterogeneous integration. For example, integration of varying digitally focused chiplets has spawned multiple conferences and consortia, including the recent Universal Chiplet Interconnect Express consortium. Supporting and spurring on much of this activity are federally funded efforts, such as the DARPA CHIPS programme. There are also many efforts driven by government research programmes that focus on mixing optical technologies at the chip scale to trim the cost and improve the performance of photonic integrated circuits.

Looking more broadly at the history of semiconductor innovation, the timeline from a technology's first results to its commercial deployment has consistently been on the order of two decades. The time that it takes to develop a compound semiconductor device technology, such as that based on GaAs or GaN, is very similar to that for silicon (see Figure 3), with initial device results preceding deployment in commercial applications by about 20 years.

For both GaAs and GaN, development has been facilitated by significant industrial investment, underwritten in part by the US Government. Development of GaAs devices has been supported by the DARPA MIMIC programme, while advances in GaN have been aided by the DARPA WBGS programme. Heterogeneous integration is now on the cusp of commercial employment, and has benefitted from similar developmental investment.



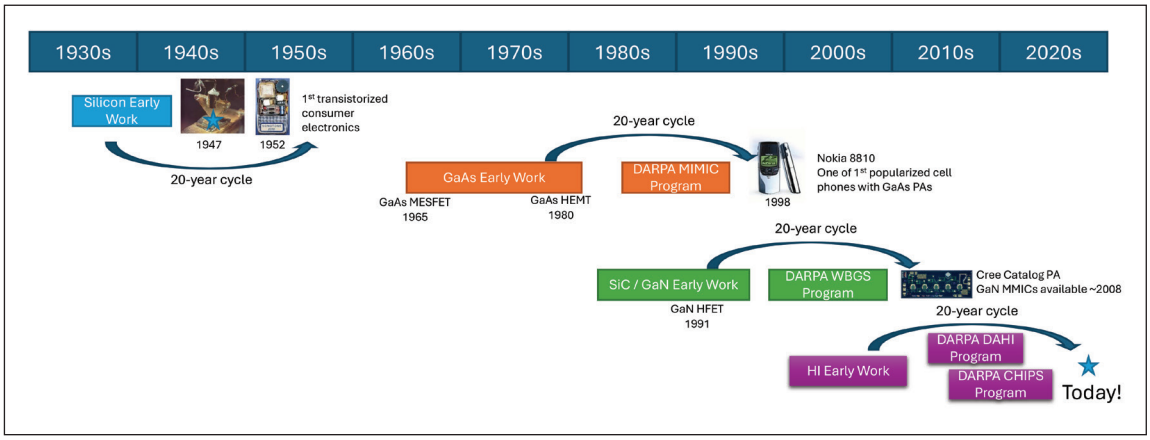
➤ Figure 2. Articles and patents referencing heterogeneous integration over five-year periods spanning the 1970s to today. The final period includes a linear extrapolation for the remainder of the current period (courtesy Google Scholar).

Based on historic rates of progress, we can conclude that heterogeneous integration is primed to realise its commercial impact.

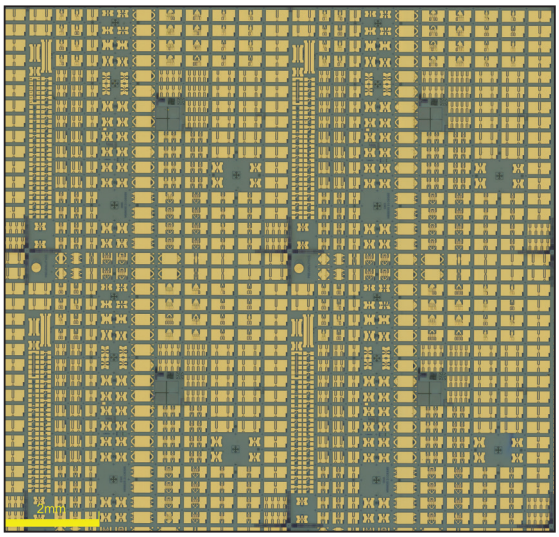
Merits of the PseudolithIC approach

A number of research groups are focusing on RF applications, and exploring several approaches. We are involved in this area, but taking the technology much further, by commercialising a chip-scale 2.5D integration approach that leverages existing RF silicon and compound semiconductor ecosystems.

Our approach offers three critical value propositions over monolithic processes, which concentrate on a single material. First, we accelerate the design and fabrication process for a high-performance RF circuit. An example of this is designing new circuits and integrating exotic materials, such as N-polar GaN, faster than a traditional foundry, because we just require chiplets of the material, rather than an entire MMIC. Consequently, several thousand chiplets can be procured from a single tape-out (see Figure 4). Once we have sourced our chiplets and built up an inventory, our designers only need to design the interposer to produce a new pseudolithic IC, which we refer to as simply a PLIC. Second, our approach

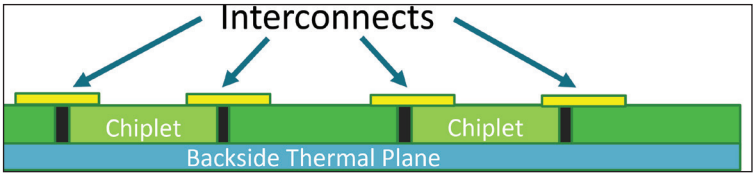


➤ Figure 3. A timeline illustrating the evolution of silicon, GaAs, GaN and heterogeneous integration as semiconductor technologies.

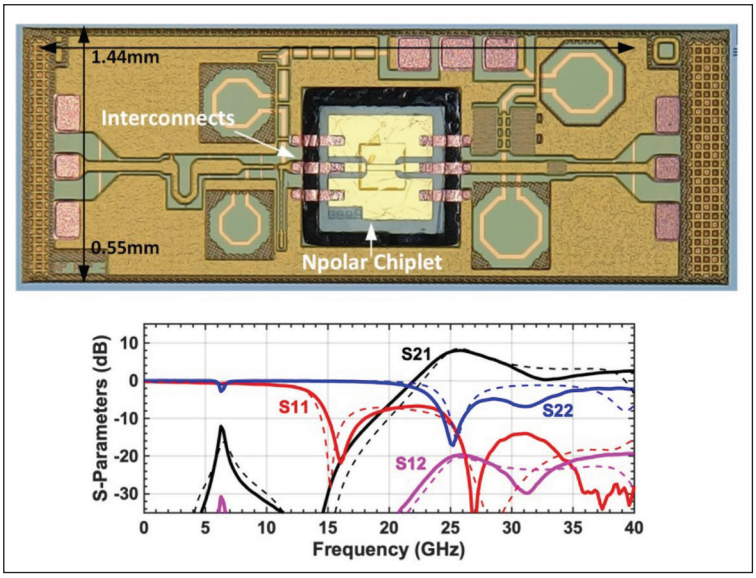


➤ Figure 4. Micrograph of an example 'sea of transistors' wafer used for N-polar GaN chiplet fabrication.

enables a true 'mix-and-match' of different devices, such as InP and GaN, in a single PLIC. This enables optimal architectures that are free from multi-chip modules. Finally, as the interposer is built on wafers with a diameter of at least 8 inches, they have at least four times the area of the 4-inch wafers used in typical III-V processes, leading to significant fab throughput and cost advantages.



➤ Figure 5. Cross section of a completed PseudolithIC PLIC with a chiplet embedded in a silicon interposer.



➤ Figure 6. (top) Chip microphotograph of the 26 GHz heterogeneously integrated amplifier illustrating the compact implementation of the input and output matching networks. For clarity, the HEMT chiplet and interconnect are highlighted. (bottom) Simulated (dashed) and measured (solid) S-parameters of the heterogeneously integrated amplifier. A peak gain of 8.0 dB occurs at 26 GHz.

To enjoy all these benefits, we employ an approach that begins by sourcing individual active III-V transistors – or even more complex integrated circuits – from either an established defence industrial base or a commercial foundry. After dicing these devices into singulated 'chiplets', they are embedded into a separately designed and fabricated silicon substrate interposer, which may feature passive networks, such as transformers, and active CMOS control circuity. By adopting a low-temperature process, we maintain the integrity of the chiplets and the *in-situ* CMOS devices. Our final step, completing integration at the wafer scale, is the fabrication of copper coplanar waveguide interconnects between the chiplet and interposer.

The finished product, a PLIC, is completely planar and compatible with commercial die attach, packaging, and chip-on-board processes, aiding downstream integration in higher-level systems. Critically, the PLIC is nearly indistinguishable from a single technology IC (see Figure 5, which shows a cross section of a PLIC after the chiplets are embedded in the interposer, and highlights the thermal advantages that result from direct access to the backside of the high-power chips).

First pass successes

Our unique process, which capitalises on the maturity and reliability of silicon to simplify the millimetre-wave and microwave MMIC design processes, results in an exceptionally high first-pass success rate. Exemplifying the advantages of our process are recent publications outlining how our technology can be used to produce an N-polar GaN power amplifier, an InP power amplifier, and a two-stage amplifier that features both InP and GaN technology.

Recent research shows that N-polar GaN HEMTs offer high-efficiency, high-power density, and excellent linearity for microwave and millimetre-wave applications. However, transitioning emerging GaN HEMT technologies into commercial applications is impeded by the lengthy foundry development cycle for a full MMIC process – this involves device maturation and qualification, and incurs a high cost, due to the specialised 4-inch epitaxial wafers. Our approach addresses some of these delays, with an acceleration of material to viability, thanks to the introduction of a heterogeneous design that embeds an N-polar transistor in a silicon interposer.

For the amplifier we have fabricated, we use a HEMT chiplet with: an 80 nm gate length; 500 nm gate-drain separation; and two fingers of 37.5 μm width, for a total gate periphery of 75 μm. Measurements of S-parameters for this amplifier suggest a peak output power of 150 mW (see Figure 6). Despite designing across two processes, there is excellent agreement between 20 GHz and 40 GHz, thanks to the maturity of our custom design environment that is adept at uniting silicon and

III-V technologies. The peak gain of our amplifier reaches 8.0 dB at 26 GHz. At this frequency, the input and output return loss exceed 16 dB and 12 dB, respectively. The reverse isolation, S12, is better than 20 dB across the frequency band. The measured amplifier is unconditionally stable from 0 to 40 GHz.

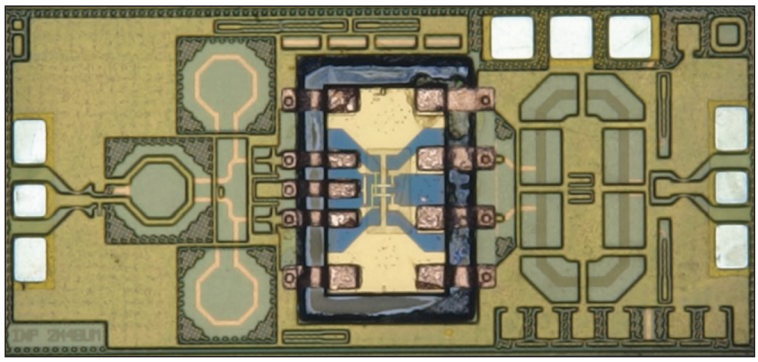
We have also demonstrated similar first-pass success with more mature process technologies, including a 250 nm InP HBT process reported in early 2024. This process offers a 2.5 V supply with a maximum oscillation frequency (f_{max}) approaching 650 GHz. The high value for f_{max}, and also for the cut-off frequency (f_T), ensures that this technology is attractive for high-gain and high-efficiency blocks.

Additional attributes are a low supply voltage and a high collector current density of 2 mA μm^{-1}, strengths that support matching that is closer to a desired 50 Ω. Due to this, a lower impedance matching quality factor (Q) is required to match to the device, leading to wideband amplifier designs.

Our heterogeneously-integrated InP amplifier, shown in Figure 6, has differential-mode stabilisation included on the chiplet. To allow supply of the base voltage through the common mode node, a transformer with capacitive isolation is used on the input. The differential signals on the collector are combined through a sub-quarter-wavelength balun on the output. Using this configuration, our amplifier exhibits 10.6 dB of gain at 24 GHz, with a total power consumption of only 45.3 mW.

Combining GaN and InP

Building on our foundation that has established that single III-V technology heterogeneous integration is viable and commercially competitive, we have gone on to prove that our technology can mix and match different III-V device types in the same integration process. For this demonstration, we have drawn on the success of our previous two circuit designs, by designing and fabricating a two-stage amplifier that has an InP first stage and a GaN second stage. The motivation for making this single PLIC is that no single technology is best suited for all RF functions. In our Ka-band amplifier, we need an InP first stage to maximise gain and a GaN second stage to maximise output power (see Figure 8 for a die micrograph of the fabricated PLIC and a top-level schematic of the two stages).

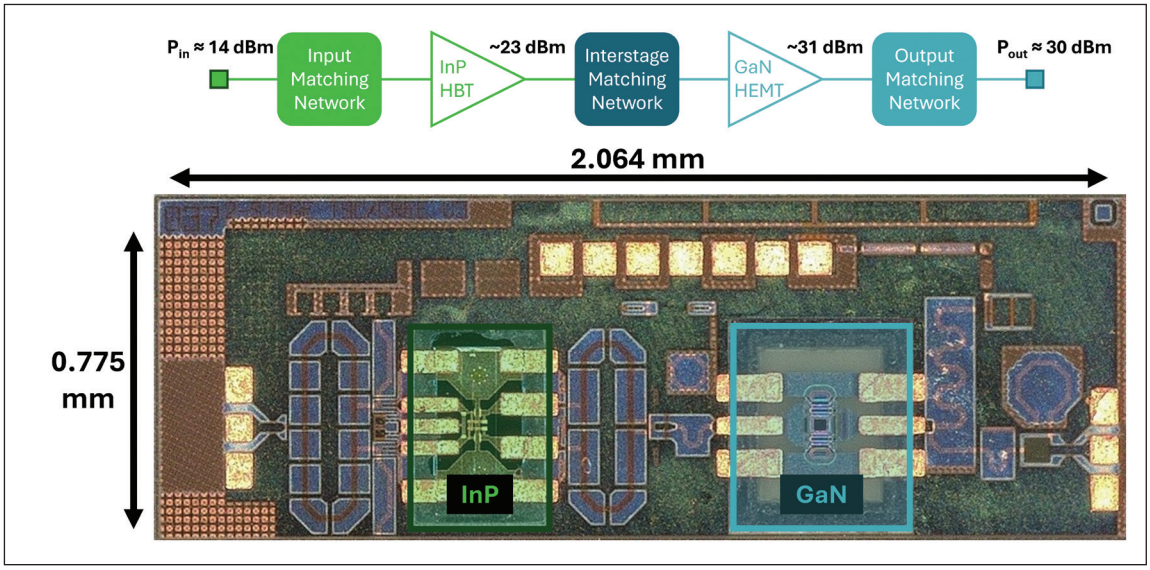


➤ Figure 7. Chip micrograph of the Ka-Band heterogeneously integrated InP amplifier.

As we had previously built and tested each stage independently prior to this design, we concentrated our efforts on a new interstage matching network and making slight adjustments to the previous input and output matching networks. This again demonstrates how we can accelerate the adoption of heretofore impossible circuit topologies through our unique process. Our combined amplifier measures over 20 dB of gain at 25.7 GHz, validating our approach of merging the two technologies.

Higher levels of integration

Transmit/receive modules are ubiquitous in commercial and defence electronics. Here there is an ever-present demand for higher performance, realised at a lower cost and at higher frequencies. Defence electronics is tending to migrate to the



➤ Figure 8. High level schematic of the two-stage amplifier (top) and a die micrograph of the fabricated device (bottom).

Our triumphs include the world's first millimetre-wave amplifier that combines InP and GaN devices, a demonstration that underscores the extreme flexibility associated with combining different technologies. Another significant success is our dense transmit/receive module designs that combine InP, GaN and CMOS to deliver higher performance and lower cost

Component	Ideal Qualities	Candidate Technologies
T/R switch	Fast Switching Time High Off/On Isolation Low Insertion Loss	Si SOI CMOS GaN HEMT
Low-Noise Amplifier	Low Noise Figure Wide Bandwidth Low Power Consumption	InP HEMT GaAs pHEMT
Power Amplifier	High Output Power High Efficiency Ease of Matching	GaN HEMT

➤ Table 1. Design considerations for a Ka-Band T/R module.

V- and W-band to gain both bandwidth and a spectrum access advantage over potential adversaries. Similarly, commercial electronics are moving to higher frequencies, in this instance to satiate the growing demand for bandwidth in cellular and satellite communications networks. Heterogeneous integration is ideally suited to meet all these application requirements, providing an optimised performance in small form factors.

Conventionally, transmit/receive modules are constructed from multiple die, and packaged and interconnected with traditional PCB-style manufacturing techniques. This approach is adopted because no single monolithic process is ideal for each of the transmit/receive functions (see Table 1 for some of the design considerations for a typical transmit/receive module, including devices that best meet those requirements).

Building on our success with our multi-stage, multi-technology amplifier, we have designed and fabricated several generations of transmit/receive modules that mix different devices to achieve optimal performance in a very small form factor, typically around just 5 mm^2. According to our latest simulations, our technology can deliver an output power of 2 W from the transmit path of the module. The receive path can deliver 12 dB of gain at 28 GHz while maintaining a total noise figure below 2.5 dB for the module when accounting for switch loss. There is no doubt that heterogeneous integration holds the key to realising an optimal technology combination, and enabling great performance from a small form.

Following 20 years of public and private investment and research activity, it appears that heterogeneous integration is now poised for commercial adoption, thanks to continued maturation and evolution of the foundational manufacturing techniques. We have contributed to this development with a proprietary process that has yielded several 'first-ever' prototype designs, highlighting the key benefits of heterogeneous integration for RF and millimetre-wave circuits.

Our triumphs include the world's first millimetre-wave amplifier that combines InP and GaN devices, a demonstration that underscores the extreme flexibility associated with combining different technologies. Another significant success is our dense transmit/receive module designs that combine InP, GaN and CMOS to deliver higher performance and lower cost. While this demonstration has targeted Ka-band applications, the approach extends readily to frequencies at W-band and beyond. These results highlight that the moment has now arrived to transition heterogeneous integration to various applications, from commercial 5G/6G telecommunications to defence electronics and beyond.

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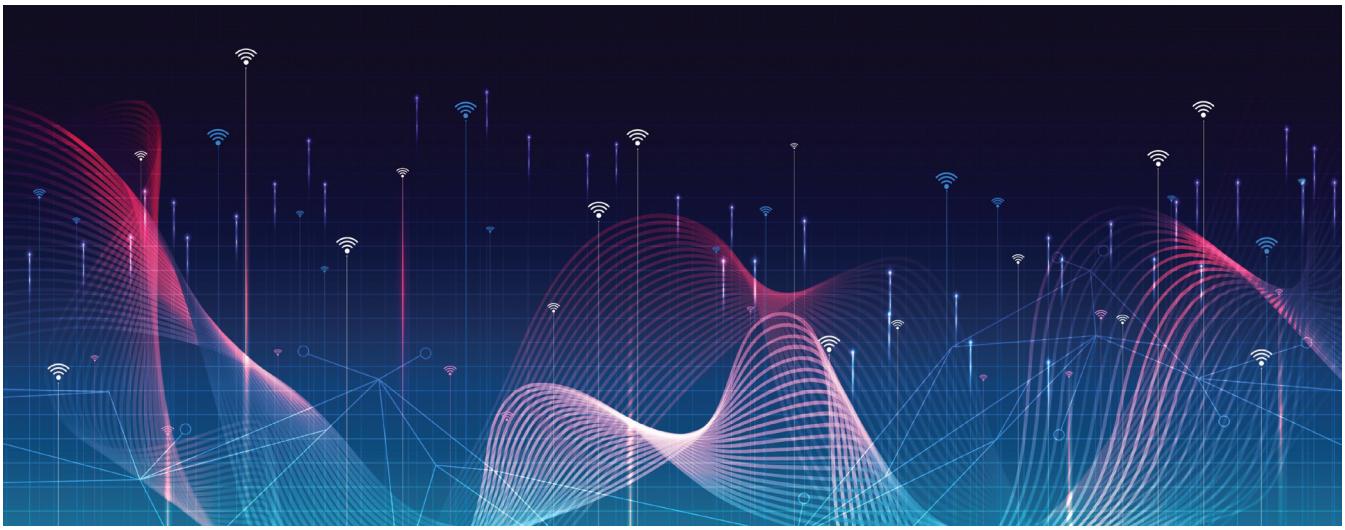


Multiple materials vie for RF success

Researchers at the recent International Electron Devices Meeting reported breakthroughs in RF devices made from many different materials

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN the optoelectronic domain, the most suitable material for producing a particular device is pretty obvious. If you want to make a blue LED, use GaN; for a red variant, InGaP; and if you are to make a laser that's targeting the low-absorption windows of a fibre, use InP. Selecting the best material for light emitters is easy, because the leading contender is identified by its bandgap.

The waters get a little murkier in the power electronics arena. From a theoretical standpoint, the best semiconductor is the one with the widest bandgap, so AlN. But that's not the standout candidate when practical considerations are accounted for, such as the ease of doping, how hard it is to form an ohmic contact, and the availability and cost of suitable substrates.

When it comes to RF devices, it is even harder to determine what material to select. In part, that's because one must consider more figures of merit, and determine their prioritisation on a case-by-case basis. Practical considerations are also challenging, with decisions needing to reflect how difficult it is to miniaturise a particular device and improve its high-frequency performance. So, given all these complications, it is helpful to know the state-of-the-art capabilities of RF transistors produced with a wide range of material systems.

An opportunity to get exactly that insight was given to delegates attending the most recent International Electron Devices Meeting (IEDM), held in San Francisco between 7th and 11th December.

At that conference, and in the on-demand talks that followed, attendees could hear presentations on record-breaking RF devices made from a wide variety of material systems, including InP, GaN, AlScN, Ga_2O_3 and diamond.

Marrying InP and silicon CMOS

Amongst the many materials that are suitable for producing RF transistors, InP offers a strong case as the leading option. By delivering an impressive performance, in terms of both gain and power efficiency, devices based on this III-V are compelling candidates for a number of millimetre-wave and sub-terahertz applications.

However, there is literally a high price to pay for the great performance of InP transistors. Their manufacture is costly, due to use of electron-beam lithography processes, and production on substrates that are at most 100 mm in diameter.

One application for InP transistors is phased arrays for radar systems. When these systems operate above 100 GHz, the antenna array pitch, which is governed by the operating wavelength, is of the order of 1 mm. This length scale necessitates the dense integration of InP power amplifiers and silicon CMOS beamformers.

An attractive approach to realising this integration, pioneered by the European microelectronics centre imec, is to position InP chiplets providing power amplification at precise positions on a fine-pitch carrier.

The capabilities of this approach, using an RF silicon interposer platform developed in house, were highlighted at IEDM by imec's Siddartha Sinha.

There is a significant financial benefit that comes from combining InP and silicon CMOS in this way. "If you are able to restrict the III-V content in your design to less than 20 percent of your area, there is a drastic reduction in cost," remarked Sinha, who added that these savings can be as large as a factor of five to ten. "We use InP only where it is needed, for RF power amplification, and everything else is built using standard CMOS technology."

Sinha pointed out that there are four significant packaging challenges to overcome when producing platforms operating above 100 GHz: realising sufficiently dense integration; dealing with the fall in transistor performance that comes from scaling, overcome by introducing more stages or new materials; addressing high interconnect losses; and managing the increase in thermal density.

"At imec we have developed a unique interposer-based solution that addresses these four issues," argued Sinha. He explained that he and his co-workers are able to realise dense integration with a 1 mm pitch for the arrays by using redistribution layers and a via pitch of 30 μm, and they tackle the decline in device performance with miniaturisation with a CMOS beamformer and InP power amplifiers. To reduce interconnect loss, imec's engineers use smooth films of copper and low-loss polymers, and for thermal management they benefit from the use of silicon that has a much higher thermal conductivity than glass interposers.

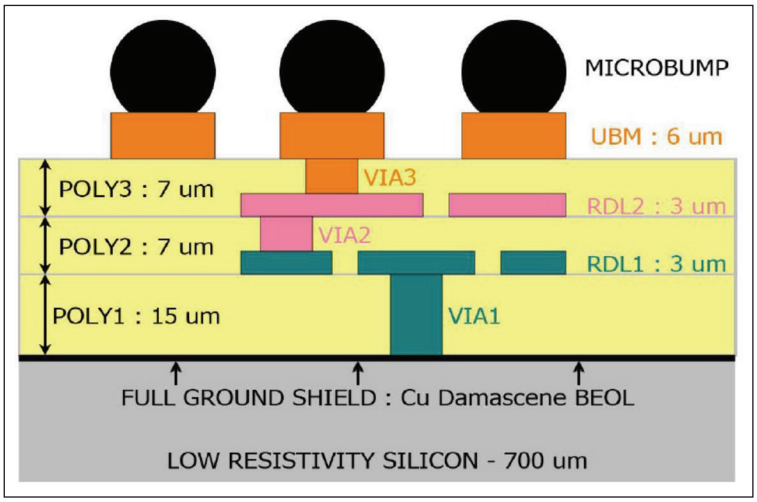
To assess the capability of their technology, Sinha and co-workers have produced RF interposer stacks featuring: spin-coated layers on RF-friendly polymers, thick layers of copper that reduce low-frequency and DC losses, and interconnects that can operate up to 200 GHz (see Figure 1).

Transmission measurements on these interposers reveal line losses of 0.3 dB mm^{-1} and 0.23 dB mm^{-1} at 140 GHz for structures with polymer thicknesses of 15 μm and 22 μm, respectively. Broadband performance is realised, spanning 20 GHz to 170 GHz.

"These numbers are comparable to what you have in PCB or glass interposers, but with much higher integration densities – that is, much thinner substrate sizes," remarked Sinha.

Additional investigations have considered the combination of the interposer and InP transistors. To assess this, the team from imec flip-chip bonded a Teledyne 250 nm InP stack to its interposer with an in-plane alignment accuracy of 3 μm.

Passive measurements of losses with this flip-chip architecture determined values of 0.9 dB mm^{-1} and 0.3 dB mm^{-1} at 140 GHz for the InP backend



➤ Figure 1. Engineers at imec have highlighted the potential of InP chiplets on a silicon interposer for millimetre-wave applications by demonstrating the low losses of this particular system.

microstrip and interposer microstrip, and an insertion loss of around 0.1 dB for one flip-chip transition over 20 GHz to 170 GHz.

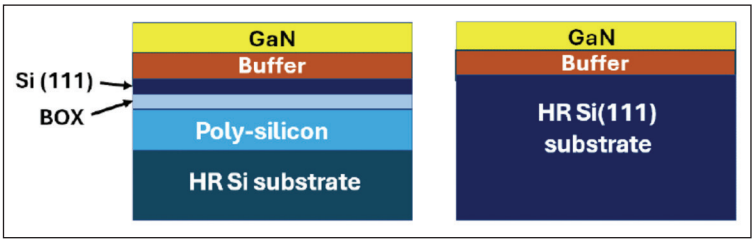
"The interposer microstrip is about three times better than what you could get in an indium phosphide die back-end," said Sinha, who added, "keep in mind that CMOS back-ends are even more lossy than this, because they are not millimetre-wave optimised."

The engineers from imec have also investigated the active performance of the InP power amplifier on the interposer, recording a peak small-signal gain of 16.3 dB and a 3 dB bandwidth spanning 116 GHz to 148 GHz. "These are state-of-the-art numbers, compared to even standalone PAs," claimed Sinha.

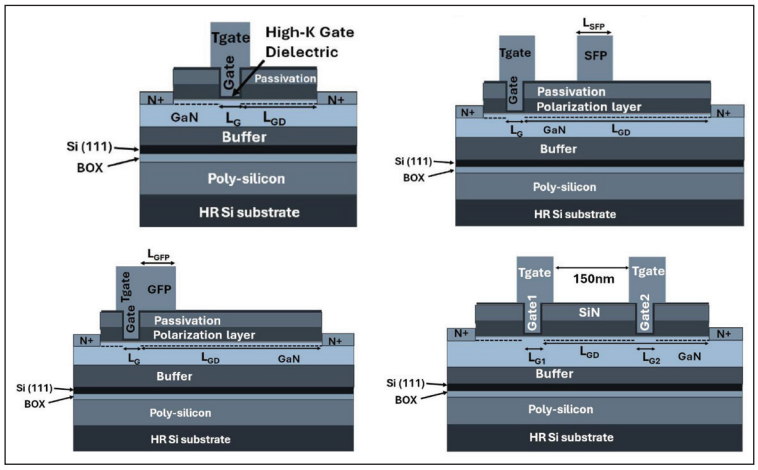
GaN on 300 mm silicon

Another material with a proven pedigree for providing RF amplification is GaN.

One of the leading developers of this technology is Intel. Back in 2019 this chipmaker unveiled the industry's first 300 mm GaN-on-silicon process for scaled enhancement-mode high-κ gate dielectric GaN MOSHEMTs for power delivery and



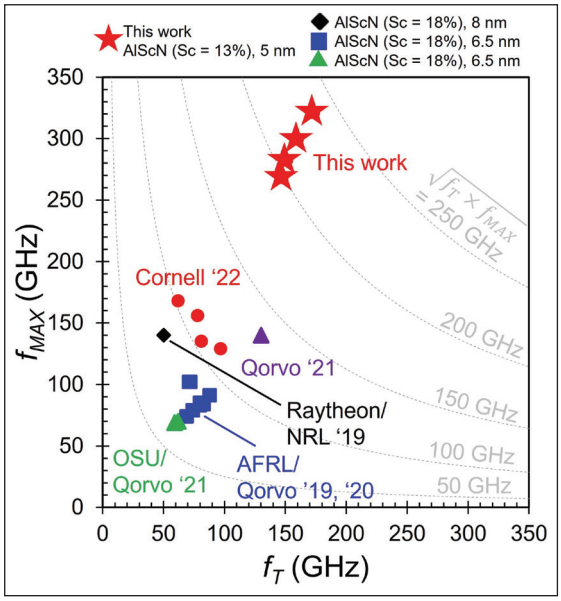
➤ Figure 2. (a) Intel has used 300 mm trap-rich SOI as a foundation for producing GaN MOSHEMTs on 300 mm silicon wafers. The thin silicon (111) layer serves as a crystalline template for GaN epigrowth. Beneath this is an underlying insulating buried oxide (BOX), and below that a trap-rich polysilicon layer that eliminates stray charges at the interface to the BOX, as well as a high-resistivity silicon substrate.



➤ Figure 3. On 300 mm trap-rich SOI substrates, Intel has fabricated four variants of the enhancement-mode high-κ dielectric MOSHEMT. As well as the standard form of MOSHEMT, there are those with a source field plate, a gate field plate, and multi field plates.

RF electronics, and at IEDM 2024 it revealed that it had extended this technology with the introduction of a low-loss, high-resistivity engineered substrate. On this new platform, produced by Shin-Etsu Handotai and featuring a 'trap-rich' silicon-on-insulator architecture (see Figure 2 for details), Intel's engineers have produced GaN MOSHEMTs with a 30 nm channel length that deliver a superior level of performance to those produced on a conventional silicon substrate.

Spokesman for the team from Intel, Han Wui Then, told delegates at IEDM that engineered substates are important for the future of GaN. He explained that turning to a trap-tich poly-silicon layer ensures the elimination of stray charges at the interfaces to the buried oxide and to the high-resistivity silicon substrate. "This enables lower RF losses and better signal linearity; decoupling of the crystalline silicon (111) template from the silicon substrate; and acts as a clear separating or isolating layer that enables backside processing to realise advanced integration schemes that are chiplet-based, for example," remarked Then.



➤ Figure 4. Using a strain-balanced design, engineers at Cornell have broken the record for the frequency performance of AlScN/GaN HEMTs.

Measurements by the team show that switching from a high-resistivity substrate to the engineered one made by Shin-Etsu Handotai for growth of a GaN epilayer leads to a four-fold increase in effective electrical resistivity, along with superior linearity – there is 10 dB suppression of the second harmonic.

Using the novel trap-rich substrate, engineers from Intel have produced four variants of the enhancement-mode GaN MOSHEMT with a high-κ dielectric at the company's advanced CMOS fab in Oregon. As well as fabricating a standard form of MOSHEMT, they have produced another with a source field plate, a third with a gate field plate, and also a variant with a multi-gate architecture. All forms were fabricated using a 300 mm gate-last integrated process flow involving the epitaxy of GaN layers by MOCVD, the deposition of a high-κ dielectric, epitaxial re-growth of source and drain contacts, and the addition of a copper backend interconnect.

Measurements on variants of the standard form of the GaN MOSHEMT with channel lengths of 30 nm, 90 nm, and 180 nm, show that these devices deliver enhancement-mode operation, have drive currents as high as 1 mA μm^{-1}, and have an on-off ratio that exceeds 10^{10}. These devices are said to have a good figure-of-merit for the RF switch – the product of the on-resistance and off-capacitance is 80 fs for a 30 nm channel length – and a good drain breakdown voltage, with a healthy breakdown slope of 1.3 MV cm^{-1}.

The variant with the source-field plate is capable of drive currents exceeding 1 mA μm^{-1} and can handle drain voltage swings as high as 12 V. The cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) are 190 GHz and 532 GHz, respectively. Note that the product of f_T and f_{MAX} is similar to that for Intel's GaN-on-silicon MOSHEMTs on high-resistivity silicon.

For the gate-field MOSHEMT, current-voltage plots are similar to those of the source-field variant.

MOSHEMTs with two gates, separated by 150 nm, are less susceptible to short-channel effects, while maintaining a high drive current – it can be as high as 1.2 mA μm^{-1}.

Improving the RF switch

The two primary choices of substrate for a GaN HEMT are SiC and silicon. GaN-on-SiC HEMTs offer a higher power-handling capability, but those with a silicon foundation are catching up, and offer the advantages of greater flexibility and superior economies of scale.

In this context, the downsides of the silicon substrate include degradation to devices and active components. A key circuit element that's highly sensitive to the substrate is the RF switch, which

must combine high linearity with a low insertion loss. To mitigate problematic substrate-induced surface losses, GaN-on-silicon devices tend to be produced using high-resistivity silicon substrates. However, while much effort has been devoted to studying the effects of GaN-on-silicon stacks on transmission-line RF loss and non-linearity, there have been very few investigations on active devices and RF switch circuits.

Helping to address this lack of knowledge is work at CEA-Leti involving the characterisation of GaN HEMT switches integrated on 200 mm high-resistivity silicon. This investigation, detailed at IEDM 2024 by Luca Lucci, is claimed to show that the GaN-on-silicon HEMT is approaching that of RFSOI, in terms of the metric that's the product of on-resistance and off-capacitance, while offering linearity and power-handling capability previously only possible with GaN-on-SiC.

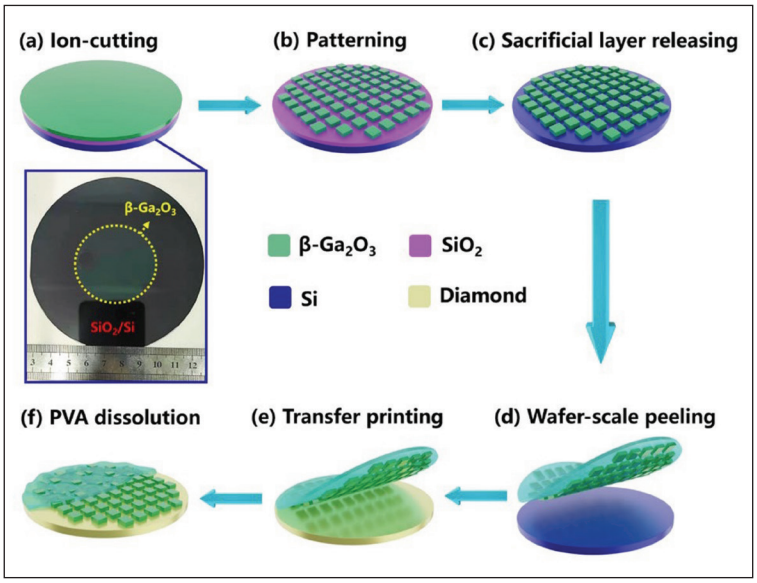
For this work, researchers at CEA-Leti have employed their own GaN-on-silicon process technology that involves processing epiwafers that feature an AlN nucleation layer, a GaN buffer layer, a 150 nm-thick GaN channel, a 700 nm-thick AlN spacer, a 20 nm-thick AlGaN barrier and a 7 nm-thick SiN cap, added *in situ*. HEMTs are produced from the epiwafers by using argon implants to realise isolation, prior to the addition of ohmic source and drain contacts annealed at just 590°C. A T-shaped Schottky gate is then defined, before the addition of interconnects that are fully CMOS compatible.

Lucci presented measurements for losses from 0 GHz to 40 GHz for two different wafers. The more recent devices, associated with lower processing temperatures, had losses below 0.15 dB mm^{-1}. "Our long-term target is to succeed in keeping these 30 gigahertz losses below 0.1 dB per millimetre, as is already feasible in gallium nitride on silicon carbide technologies," remarked Lucci.

Small-signal measurements show that by trimming the size of the access region, the engineers at CEA-Leti are able to decrease the on-resistance while having just a very small impact in the off-capacitance. It's also possible to reduce the off-capacitance while having a minimal impact on the on-resistance by reducing the width of the ohmic regions.

Showing a benchmarking plot of off-capacitance and on-resistance, Lucci remarked: "Our experimental points represent all the best of on-resistance, off-capacitance extracted so far from GaN-on-silicon technology, apart from data which has been published by Intel with a much, much shorter channel length of 40 nanometres."

Lucci and co-workers have also carried out large-signal characterisation, determining that this technology can handle 36 dBm in a shunt configuration.



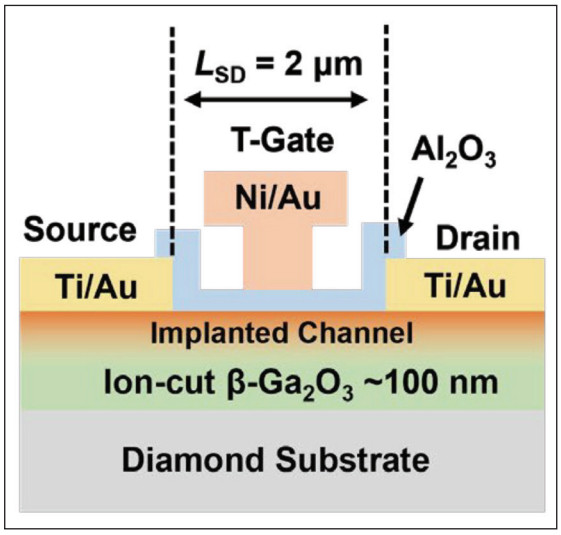
➤ Figure 5. A collaboration from China has improved the performance of β-Ga_2O_3 MOSFETs by transferring chiplets of β-Ga_2O_3 to diamond using transfer printing.

A benchmarking of all results led Lucci to conclude that his team's technology still falls short of RFSOI, when judged on the product of on-resistance and off-capacitance. "But if we also put power handling in the picture – so the maximum power that the device can handle without requiring stacking in the design – that makes the GaN solution very attractive." While GaN-on-SiC accommodates even higher powers, it requires gate voltages that are higher than preferable in many applications, according to Lucci.

Strain-balanced AlScN

For those believing that the AlGaN/GaN HEMT is starting to encroach its limits, switching the AlGaN barrier with another material has much appeal. Options include tensile-strained AlN, the lattice-matched ternary AlInN, and AlScN, which has a wider bandgap. The latter is a compelling candidate: it's not impeded by a 6 nm strained-related thickness limitation that impairs AlN, or restricted to a two-dimensional electron gas density of no more than 2 x 10^{13} cm^{-2}, a limitation that holds back AlInN.

To mitigate problematic substrate-induced surface losses, GaN-on-silicon devices tend to be produced using high-resistivity silicon substrates. However, while much effort has been devoted to studying the effects of GaN-on-silicon stacks on transmission-line RF loss and non-linearity, there have been very few investigations on active devices and RF switch circuits



➤ Figure 6. The β-Ga_2O_3 MOSFETs formed on diamond using transfer printing feature an implanted channel and a T-shaped gate.

Development of the AlScN/GaN HEMT is in its infancy. Early reports provided a value for f_{MAX} of no more than 156 GHz, but far higher values are possible, according to recent research from Cornell University that pairs compressively strained AlScN with tensile strained AlN.

Unveiling this breakthrough at IEDM 2024, Cornell's Thai-Son Nguyen explained that these record-breaking HEMTs were produced by loading high-resistivity 4H-SiC substrates into a MBE reactor and depositing a 100 nm-thick AlN nucleation layer, followed by a unintentionally doped 600 nm-thick layer of GaN, a 1.5 nm-thick layer of AlN, a 5 nm-thick layer of $Al_{0.87}Sc_{0.13}N$, and a 2 nm-thick GaN cap, added to prevent oxidation of the aluminium-containing epilayers.

According to Hall effect measurements on this epistructure, the sheet charge is 2.46 x 10^{13} cm^{-2}, the mobility 755 cm^2 V^{-1} s^{-1}, and the sheet resistance 337 Ω/sq.

To produce HEMTs from epiwafers, Nguyen and co-workers employed hard mask patterning and etching, followed by the addition of MBE-regrown source and drain n^+ contacts. Processing continued with device isolation, ohmic metallisation of source and drain contacts, and the use of electron-beam lithography to construct T-shaped gates with a length of 40 nm.

Electrical measurements determined a contact resistance for the ohmic contacts of 0.09 Ω mm. "This is the lowest contact resistance reported for AlScN/GaN HEMTs, and is in line with some of the best contact resistances for GaN HEMTs in general," remarked Nguyen.

He and his colleagues have compared the performance of AlScN/GaN HEMTs with gate lengths of 800 nm, 120 nm and 40 nm. They found that the maximum drain current increases with scaling, to exceed 2.5 A mm^{-1}, and on-resistance can be as low as 0.83 Ω mm.

Small-signal RF results on the HEMT with the shortest gate length determined values for f_T and f_{MAX} of 173 GHz and 321 GHz, respectively. "These are the highest f_T and f_{MAX} reported for AlScN HEMTs," remarked Nguyen (see Figure 4 for values of f_T and f_{MAX} at various gate lengths). He predicts that even higher values are possible with more extreme scaling, such as a 20 nm gate length.

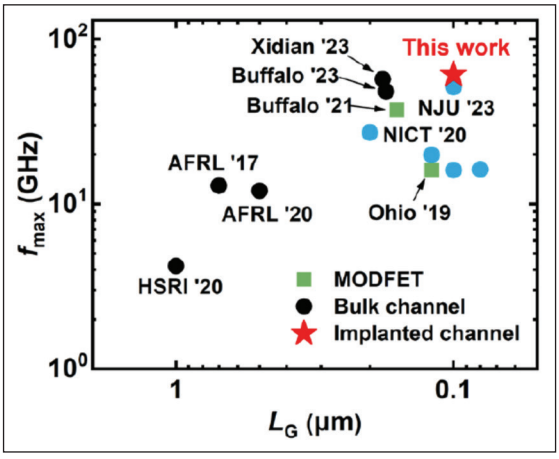
Combining Ga_2O_3 with diamond

Over the last few years interest in Ga_2O_3 power devices has rocketed, driven by this oxide's high breakdown field, as well as the promise of low-cost, high-quality native substrates. Note, though, that Ga_2O_3 also has much promise in the RF domain – it is three times better than GaN, according to a Johnson figure of merit that characterises power-frequency capability.

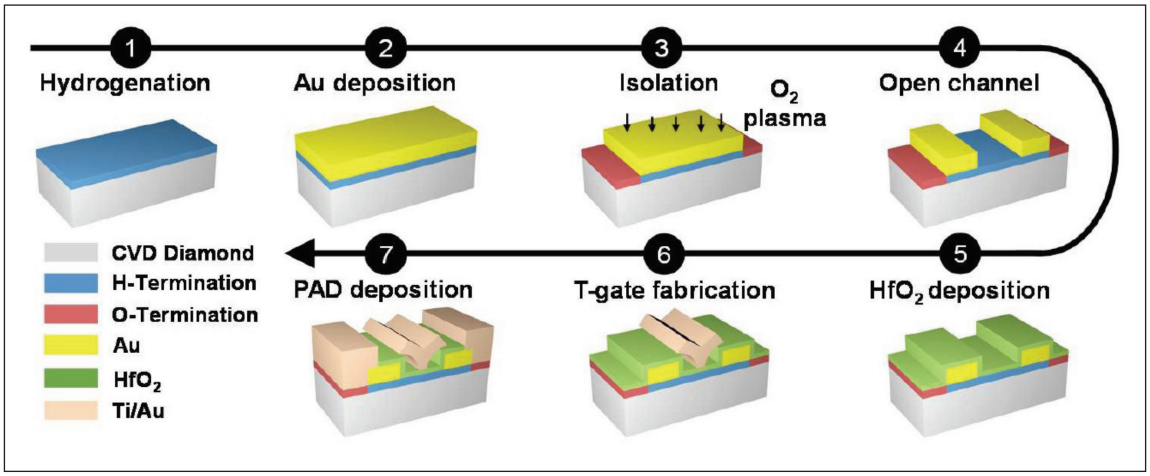
The Achilles heel of Ga_2O_3 is its incredibly poor heat dissipation. This can be addressed by pairing this oxide with materials that are far better in this regard, such as diamond, well-known for its exceptional thermal conductivity. However, combining Ga_2O_3 and diamond is far from easy. Severe lattice mismatch between them hinders direct epitaxial growth, and direct wafer bonding is problematic, due to dangling bonds created during the activation process.

Offering a far more promising alternative, unveiled at IEDM 2024 by a collaboration from China, is a transfer printing process that forms arrays of β-Ga_2O_3 thin films and MOSFETs on diamond. Triumphs by this team from Shanghai Institute of Microsystems and Information Technology, Nanjing Electronics Devices Institute, the National Key Laboratory of Solid-Sate Microwave Devices and Circuits, and Harbin Institute of Technology, include record-breaking frequencies for their devices.

To produce their arrays, this partnership begins by using its novel ion-cutting technology to fabricate



➤ Figure 7. β-Ga_2O_3 MOSFETs that feature a diamond foundation and are produced using transfer printing are setting new benchmarks for f_T and f_{MAX} for MOSFETs made with this ultra-wide bandgap oxide.



➤ Figure 8. A partnership between engineers in Japan and the US has produced diamond MOSFETs with a Al_2O_3 high-κ dielectric that operate at record-breaking frequencies.

a 2-inch β-Ga_2O_3/SiO_2/silicon wafer. After using inductively coupled plasma to etch a square pattern into the β-Ga_2O_3 layer with dimensions of 200 μm by 200 μm, these engineers remove the exposed SiO_2 layer by etching in HF acid for 4 hours to ensure a direct contact between β-Ga_2O_3 and the silicon substrate. Coating the whole wafer with polyvinyl alcohol follows, before transfer printing exploits the weak van der Waals interaction between β-Ga_2O_3 and silicon, and unites the β-Ga_2O_3 chiplets with a 1-inch diamond substrate. Deionised water then dissolves the polyvinyl alcohol, prior to annealing at 900°C for 30 minutes, to strengthen the bond between β-Ga_2O_3 and diamond (see Figure 6 for an illustration of the process).

Spokesman for the team, Tiancheng Zhao from the Shanghai Institute of Microsystems and Information Technology, told delegates at IEDM that the team confirmed the quality of the transferred film using X-ray diffraction and atomic force microscopy. There is an X-ray diffraction peak around just 78 asrcec wide, highlighting the lack of stress in the film.

Zhao explained that HF acid etching damages the surface of the films, with a root-mean-square value for roughness, according to atomic force microscopy, of 0.59 nm. However, planarization via an inductively coupled plasma improves surface quality, reducing the root-mean-square roughness to just 0.36 nm.

Further evidence for the high-quality of the transfer process comes from cross-sectional transmission electron microscopy. This technique reveals a well-organised lattice arrangement for the β-Ga_2O_3 thin film, and a well-defined, sharp heterointerface – the amorphous layer between β-Ga_2O_3 and diamond is less than 2 nm-thick. "This is beneficial for the transport of interface phonons," remarked Zhao.

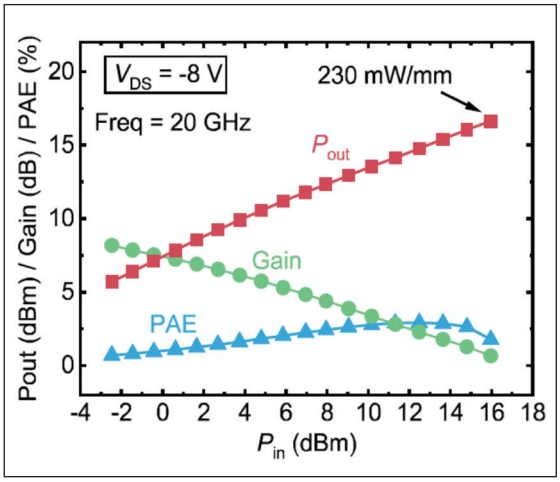
He and his co-workers have benchmarked the thermal boundary resistance of their process for uniting β-Ga_2O_3 and diamond. The value they have obtained, 21.7 m^2 K^{-1} GW^{-1}, is significantly better than that for a number of alternatives, including mechanical exfoliation.

To produce devices from the array of β-Ga_2O_3 films on diamond, Zhao and colleagues thin down the β-Ga_2O_3 and smooth its surface, before isolating the mesa, using ion implantation to form a channel, and adding source and drain ohmic contacts, followed by a 15 nm-thick film of Al_2O_3 gate dielectric and a T-shaped gate (see Figure 6).

Electrical measurement on the β-Ga_2O_3 MOSFETs have revealed a maximum drain current of 810 mA mm^{-1}, a value more than three times that of a bulk variant. Values for f_T and f_{MAX} are 34 GHz and 61 GHz, respectively, with the latter breaking new ground for β-Ga_2O_3 MOSFETs (see Figure 7). This success is attributed to the combination of an undamaged β-Ga_2O_3 film, a high-quality interface, and the diamond substrate's high thermal conductivity and low parasitic effects.

Diamond devices

The exceptional thermal conductivity of diamond, alongside its high breakdown field and high thermal conductivity, make this ultra-wide bandgap semiconductor a very promising candidate for producing high-frequency devices. Conventional bulk doping is far from ideal, due to the high activation energy, but it is possible to form a two-dimensional hole gas near the surface of this allotrope of carbon.



➤ Figure 9. At IEDM 2024 a partnership between engineers in Japan and the US unveiled the world's first diamond MMIC.

For several decades, researchers have been developing diamonds transistors. These efforts have identified that the performance of the diamond RF MOSFET falls far short of the limitations of this material, and that device performance hinges on transconductance, which can be improved with high-κ dielectrics. Recent work has identified the benefits of an Al_2O_3 gate, and variants with a higher permittivity, such as HfO_2, have much promise.

At IDEM 2024 a partnership between researchers in China and the US revealed that diamond devices with a HfO_2 dielectric can fulfil their potential. This team from Nanjing Electronics Devices Institute, the National Key Laboratory of Solid-Sate Microwave Devices and Circuits, Nanjing University and Virginia Tech, reported that diamond MOSFETs with a HfO_2 dielectric deliver record-breaking values for f_T and f_{MAX}. The team have used them to produce the first ever diamond MMIC.

Record-breaking devices were formed by depositing a 50 nm-thick gold film on a hydrogen-terminated diamond surface by electron-beam evaporation, before removing the gold outside the active regions by chemical treatment, and using oxygen plasma to provide electrical isolation. Following electron-beam lithography, channels were opened by wet etching gold, before using atomic layer deposition to add a 10 nm-thick film of HfO_2, employed as both the gate insulator and passivation dielectric. To complete the MOSFET, the team added a T-shaped gate (see Figure 8 for an overview of the process).

Electrical measurements revealed that the two-dimensional hole gas has a density of 8.9×10^{12} cm^{-2} at room temperature, rising to 9.2×10^{12} cm^{-2} at 200°C. Mobility decreases by just 34.5 percent over this temperature range. In comparison, for a GaN HEMT, the mobility of its two-dimensional electron gas falls by 70 percent between room temperature and 200°C.

Diamond MOSFETs with a gate length of 80 nm produce a peak drain current of 1.05 A mm^{-1} and a transconductance of 251 mS mm^{-1}. Measurements of small-signal characteristics determined values for f_T and f_{MAX} of 90 GHz and 164 GHz, respectively, and large-signal characteristics at 20 GHz revealed an output power density of 230 mW mm^{-1}.

The engineers have produced a diamond MMIC for operation in the X-band that has dimensions of 1.7 mm by 0.8 mm. Small-signal gain peaks at 6.25 dB at 7 GHz. At 10 GHz, this MMIC produces a small-signal gain of 6.25 dB, and an output power of 117 mW (see Figure 9).

This work, and that of the other team's presenting at IEDM, highlights improvements in RF performance realised by devices made from many material systems. All offer promise, but will they kick on to commercial success over the coming decades? Only time will tell.

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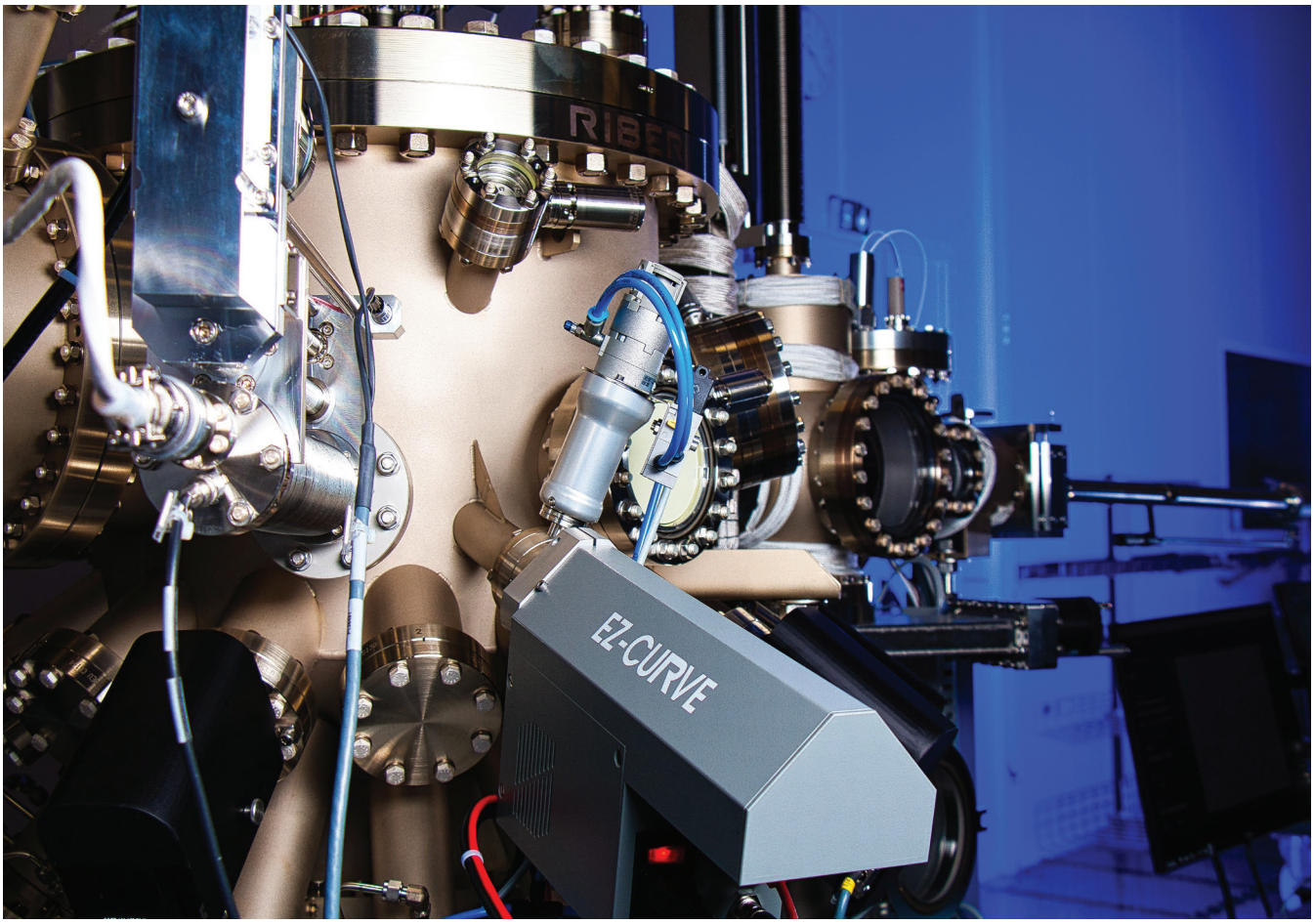


Gaining greater insight into the epitaxial process

A new generation of *in-situ* tools enables engineers to delve far deeper into the details of their epitaxial processes

BY ROMAIN BRUDER, YOURI ROUSSEAU AND ALEXANDRE ARNOULT FROM EPICENTRE, A JOINT LABORATORY BETWEEN LAAS-CNRS AND RIBER

THE LAST 50 years has witnessed a substantial development in semiconductor thin-films technology. At times this advance has been gradual, and other times it's been disruptive – but regardless of the rate of progress, there has been a continuous improvement in the equipment employed to grow these films. Thanks to this progress, epitaxial tools now have a high level of maturity, essential for supporting today's semiconductor ecosystem, which is one of the most important industrial markets worldwide.

There is also a strategic aspect to this sector, highlighted by recent, ongoing geopolitical events. Within the global semiconductor industry, a number of ambitious industrial plans are underway, designed to create or strengthen local production capacities and improve supply chain resilience. Against this backdrop, a high production yield is critical to realising a good financial return for these new ventures.

Another trend, occurring over several decades, is a tightening of product specifications, in some cases by orders of magnitude. This reflects ever-more-demanding customer requirements that are behind the need for greater process control.

Some may argue that mastering the fabrication process and decreasing the risk of product non-conformity has always been a pre-requisite for a sustainable business model. However, for many working within the semiconductor industry, these requirements are more important than ever.

Over the years, *operando* and *in-situ* instrumentation have emerged in parallel in a variety of industrial fields. Both are increasingly deployed when producing thin films, to enhance the fabrication equipment and 'augment' them.

For the growth of thin films, the introduction of instrumentation began with 'traditional' pressure and temperature measurement sensors. This has now expanded to include optical techniques – both imaging and spectroscopic – a move that enables the monitoring of more parameters, to improve the performance and the consistency of the final device.

Among the various steps necessary to process a raw wafer into a final device, epitaxy and deposition techniques at the wafer scale are critical: being at the beginning of the fabrication process, their success often determines process yield. At this stage, undetected flaws are seeds to future device failure; and any not-detected faulty epi-wafer that's used in subsequent process steps squanders the production time of the corresponding equipment. Due to this, our company, MBE equipment manufacturer Riber, is an advocate of techniques that will enable 'Smart Epitaxy' equipment with advanced capabilities.

Of all the optical technologies that can probe thin films growth, one is particularly linked to the epitaxy of compound semiconductor materials onto substrates of a different nature: the curvature measurement. By quantifying the stress that is generated by a layer deposited onto a substrate, due to dissimilarities in crystalline lattice constants, the curvature measurement provides an accurate indication of a process' dynamics and its stability. But that's not all – curvature measurements indirectly reveal information associated with the composition and the thickness of the deposited layer.

Curvature tools have been on the market for several years. However, they have tended to be held back by an intrinsic difficulty linked to their sensitivity, which has often limited their application to highly strained material systems.

Overcoming this limitation is our curvature instrument that features innovative concepts. By improving the sensitivity of the measurement, our novel instrument is a game changer in *in-situ* real-time curvature measurements, for both epitaxy and a variety of other thin films processes.

Our tool is a culmination of fruitful, patented, collaborative work, undertaken in the joint laboratory project Epicentre, involving our team and researchers at the CNRS-LAAS laboratory in Toulouse. One of the goals of the Epicentre is to accelerate the development of *in-situ* instruments on MBE reactors to enable machine learning approaches for the epitaxy process.

Magnification inferred curvature

During the growth of epiwafers, stress and strain are introduced, due to differences in lattice constants and thermal expansion coefficients. These differences result in a deformation of the wafer, which can be measured with our instrument that is based on a simple optical phenomenon known as magnification inferred curvature. For this measurement, the wafer acts as a deforming mirror, with its curvature altering the image of a bright object made of white light spots. A camera collects the distorted image, with the spacing of spots measured in real time.

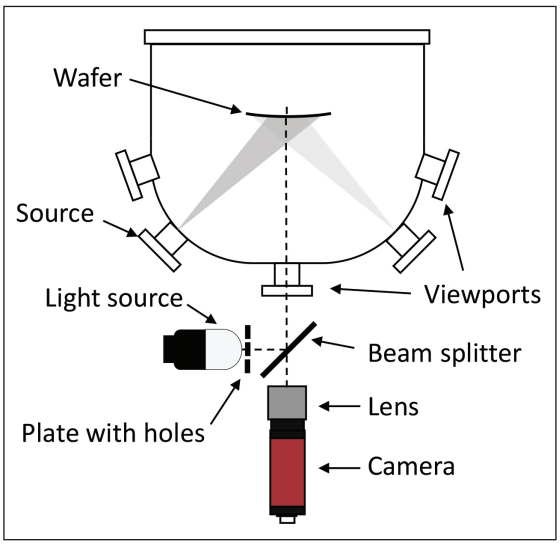
By comparing spacings in the initial image and the distorted image, our instrument determines the curvature change – that is, the amount of deformation. This figure is related to the stress associated with the film that's been added to the substrate (see Figure 1).

Applying this technique *in situ*, and monitoring the curvature of the wafer in real time, allows us to track this characteristic on a second-by-second basis. Note that while the magnification inferred curvature equipment has been designed for epitaxy, it is also applicable to other thin-films processes, such as PVD, CVD, and various vacuum treatment processes, such as plasma etching and annealing.

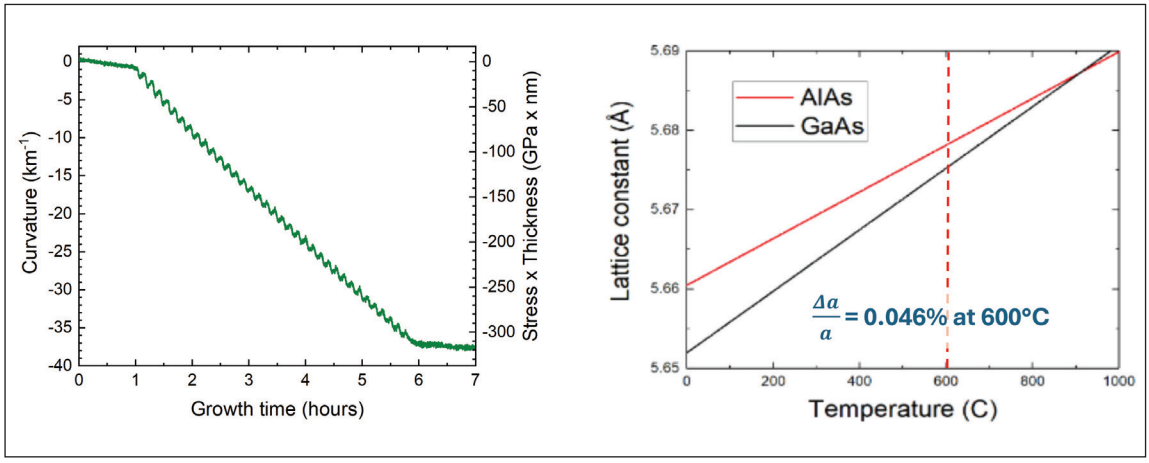
We are keen to emphasise the following point: when using this monitoring tool, the curvature measurement need not be a goal in itself, and can rather be a means to follow, in real time, what is happening at the wafer surface. Monitoring may be useful, even when there is no specification related to the curvature of the epiwafer.

Proven results

One of the greatest benefits of our magnification inferred curvature instrument is its sensitivity. We are certainly not the first to use curvature to monitor a process, but we offer far greater sensitivity than the previous techniques employed for the likes of highly



➤ Figure 1. The magnification inferred curvature principle.

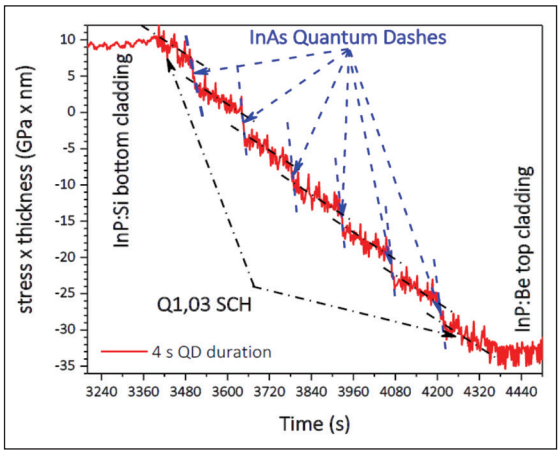


➤ Figure 2. Curvature measurement during the growth of an AlGaAs/GaAs superlattice on a GaAs substrate, to form a distributed Bragg reflector. A lattice mismatch as low as just 0.046 percent can be detected.

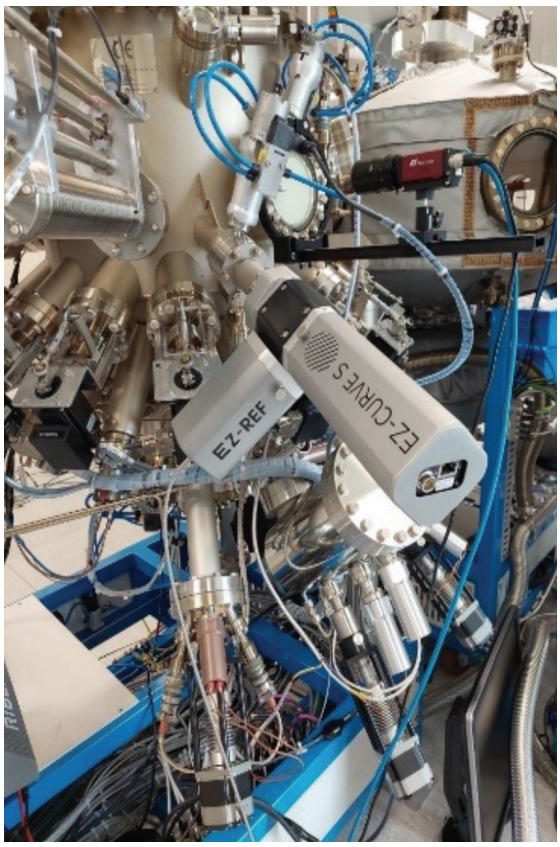
strained films and high-speed processes, where the curvature may vary significantly.

Our solution, emerging from the Epicentre laboratory, offers greatly enhanced sensitivity, thanks to its superior design. Armed with this attribute, our tool is capable of detecting incredibly low levels of lattice mismatch and very subtle phenomena (see Figures 2 and 3).

There are a variety of situations where our instrument has proved successful to monitor a process, even if it has not been purposely deployed to meet a curvature specification. One example is flux calibrations for MBE growth, which have been performed within 30 minutes. That's far faster than the traditional approach of using successive *ex situ* calibrations via X-ray diffraction, a process that can last several days. The upshot is significant savings in time and money, when MBE is used for high-volume production.

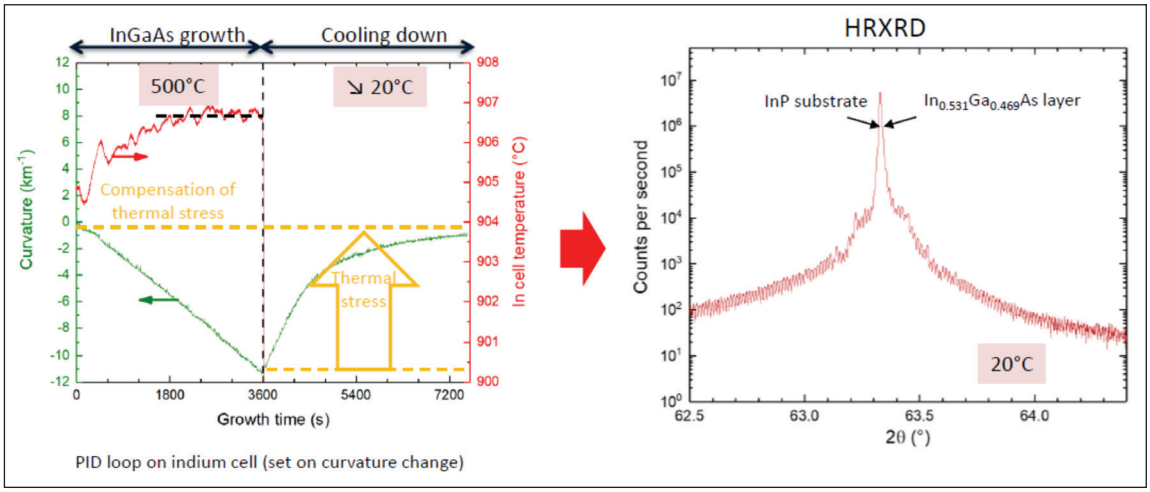


➤ Figure 3. Growth of InGaAs quantum dash in an InGaAsP barrier. The growth of each quantum dash lasts just 4 s, and leads to a modification of the curvature, clearly seen as steps in the signal. Courtesy of A. Wilk, III-V Lab.



Another example is associated with automatic lattice-matching during MBE growth. This provides control of the composition of a ternary or quaternary alloy in real time to match the substrate lattice. By using the curvature signal as an input parameter, process engineers can instigate closed loop feedback on a cell temperature or a valve position to ensure that the grown layer always matches the underlying substrate. Taking this approach to growth minimises dislocations and enhances material quality.

The same approach can be adopted for stress engineering. When differences in thermal coefficients between the substrate and the film induce stress, it may be best to grow a layer with a controlled and desired curvature, a task aided by our instrument. Thanks to its exceptional sensitivity,



➤ Figure 4. Stress engineering thanks to a curvature measurement. The growth process is carried out at a high temperature, with a fixed curvature slope that is calibrated with reference data and used as a PID input to enslave the indium cell temperature. When the process stops and the wafer cools down, the curvature signal enables monitoring of the wafer's thermal relaxation, which gets back to its initial curvature at room temperature. The processed wafer is then as flat as it was before the process, with no added bowing. The X-ray diffraction plot shows a single peak for the substrate and the film, indicating a perfect match of lattice parameters.

once growth is over and the wafer cools down to room temperature, its curvature returns to its initial, pre-process level. This ensures that when the wafer's removed from the deposition tool, it's free from any additional bowing. That's a great asset when subsequent processing steps demand flat, non-bowed wafers (see Figure 4).

Our tool has already seen widespread deployment. It has supported MBE with various substrates, including GaAs, silicon, GaSb and InP, and it has aided the growth of III-Vs, II-VIs, and oxides. In addition, it has been used during studies of the nitridation of silver films, realised by PVD.

Curvature is just the beginning

One of the features of our instrument is its communication module. Users can interface this with a lab management system, and integrate curvature in a large-scale monitoring approach. It's also possible to use the curvature data for machine learning purposes.

We are developing specific software modules to compare traces to reference data, and to simulate, *a priori*, the trace of a theoretical structure. These modules will help to get good structures from the outset, and will accelerate growth recipe optimisation.

Efforts at our Epicentre are now being directed at coupling our new curvature instrument to reflectivity or temperature monitoring. The promise of combining these different technologies in one platform is that it will offer great insight into non-equilibrium phenomena involved during growth. It is expected that the collected signal will help to finely tune the process and optimise the overall yield. In this scenario, it's possible that *ex situ* characterisation will only be required for periodical control.

We are confident that this new generation of instruments will inject new life into the capabilities of *in-situ* instruments, by introducing new concepts that enhance sensitivity and flexibility. Thanks to advanced integration into the manufacturing equipment software, our new instrument can revolutionise growth tools, by augmenting their capacity to monitor and correct themselves. As the process is controlled in real time, deviations will be eliminated, leading to a dramatic hike in yield and far more efficient use of manufacturing equipment.

While the magnification inferred curvature is only a first building block towards smarter monitoring of growth processes, it will definitely open a new era for compound semiconductor manufacturing equipment.

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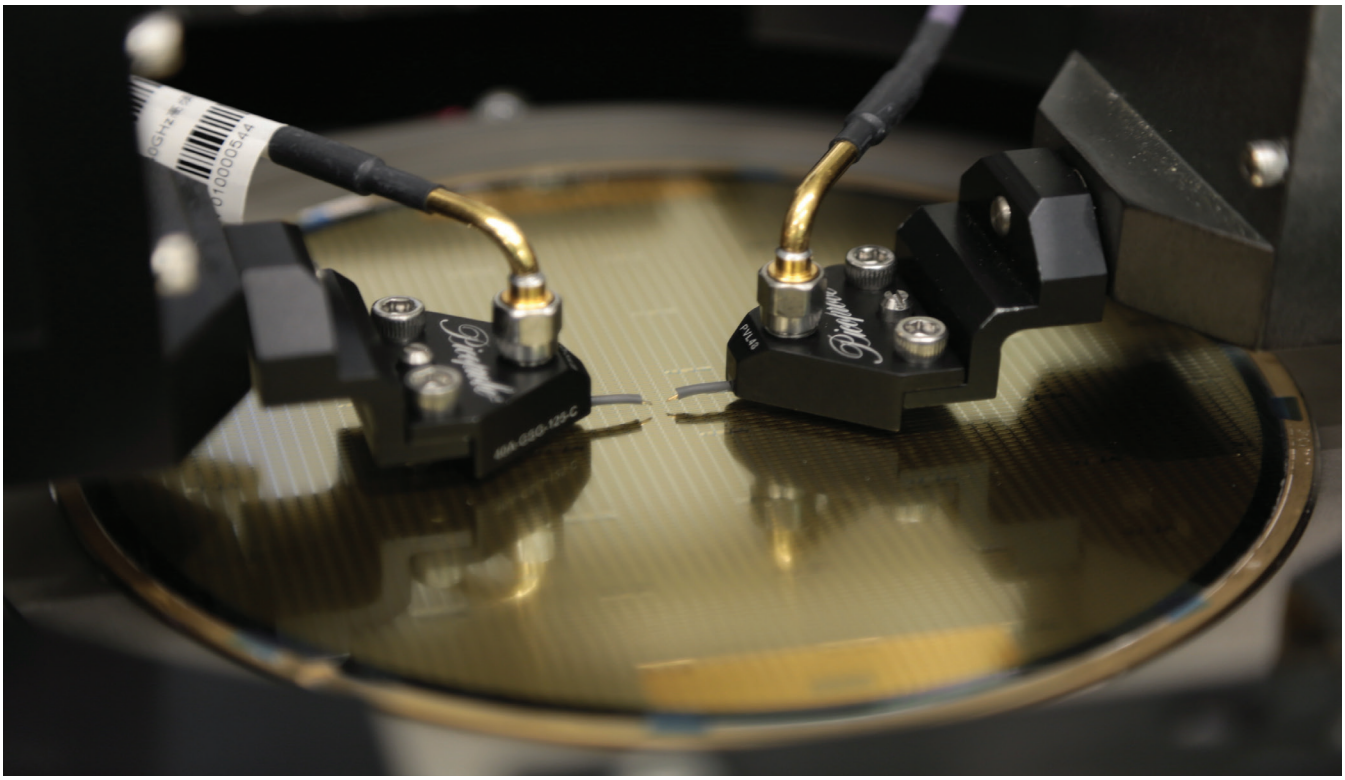


Manufacturing miniaturised GaAs power amplifiers

Introducing a foundry service for 70 nm GaAs pHEMTs supports the production of power amplifiers operating at frequencies up to hundreds of gigahertz

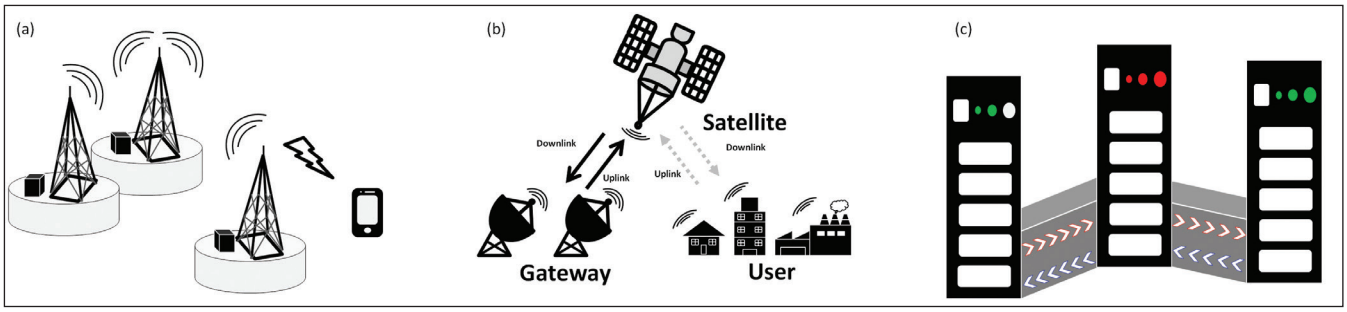
BY LUNG-YI TSENG, LI-CHENG CHANG, JUNG-TAO CHUNG, HSI-TSUNG LIN, SHU-HSIAO TSAI, CHENG-KUO LIN AND DAVID DANZILIO FROM WIN SEMICONDUCTORS

COMPOUND SEMICONDUCTORS are widely used in RF applications. In millimetre-wave front-ends, the GaAs pseudomorphic HEMT, known simply as the pHEMT, combines exceptional performance with an adequate breakdown voltage, strengths that ensure it's long been used in wireless backhaul amplification in the E-band. GaAs pHEMT power amplifiers (PAs) are also widely deployed in aerospace/defence systems, optical transceivers and low earth-orbit satellites (see Figure 1).

Due to the increasing popularity of massive data transmission, there is increasing demand for an expansion in spectral resource that can satisfy this explosive traffic growth. This has already led to the exploration of opportunities in both the W-band, which spans 75 GHz to 110 GHz, and the higher frequency D-band, at around 130 GHz to 175 GHz.

One prominent example of the commercial pursuit of using such bands is Nokia's construction of the world's first live full duplex D-band link, for mobile backhaul, announced in 2024. There are also low earth orbit applications, such as SpaceX's Starlink. This company has been granted permission by the Federal Communications Commission to upgrade its constellation to 12,000 second-generation satellites equipped with W-band technology. However, despite enjoying market dominance in the past, the GaAs pHEMT is not the leading candidate for these commercial applications.

The biggest barrier to the adoption of GaAs pHEMTs in W and D-band applications is the gain of these transistors. According to current research, only a few GaAs pHEMTs are being used in the D-band, due to the rapid degradation of gain with increasing operating frequency. Moreover, InP HBTs and GaAs metamorphic HEMTs (mHEMTs) are more compelling, due to higher maximum available gain in the D-band region. However, both these rivals are held back by a relatively low operating voltage, due to the inherently low breakdown voltage, which limits output power and reliability. To fulfil these requirements related to gain, to output power and to reliability, our team at WIN Semiconductors



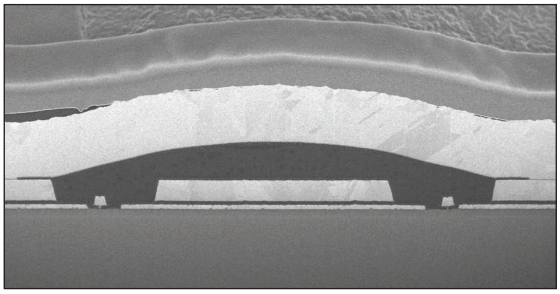
➤ Figure 1. Communication transmission application architecture of (a) mobile wireless backhaul, (b) a low-earth orbit satellite, and (c) optical transceivers in a data centre.

Corporation has developed a 70 nm GaAs pHEMT for W- and D-band PA applications.

Device fabrication...

Our latest generation of GaAs pHEMT technology employs a gate length of 70 nm, a significant reduction over its predecessor, which had a 100 nm gate length. For both classes of device, epiwafers are produced by loading 6-inch GaAs substrates in an MOCVD reactor. Growth in this chamber begins with a buffer, and is followed with an InGaAs channel, an AlGaAs Schottky layer, an AlAs etching stop layer, and an *n*-type doped GaAs cap layer. Subsequent processing requires a more complicated manufacturing process flow for the pHEMTs with a shorter gate length.

For these devices, fabrication begins by forming Ohmic source and drain contacts. Ion implantation follows, enabling device isolation. The next step is the most critical – using electron-beam lithography to define a 70 nm T-shaped gate, which has an asymmetric gate-to-drain recess length. After this, we undertake back-end-of-line processing, which includes the addition of two interconnect metal layers and a SiN_x film to fabricate the capacitors. To minimise the parasitic capacitance between two metal layers, we form air-bridge crossovers with a top metal layer with a thickness of 4 μm. Our final step is to thin the substrate down to 50 μm and then add a backside via and a backside plating metal (see Figure 2 for a cross-sectional diagram of the active and passive components).

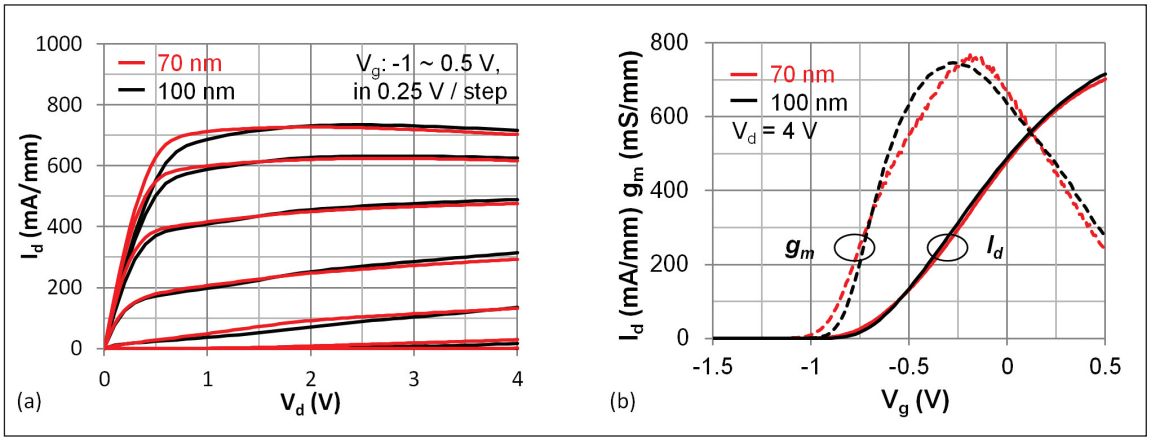


➤ Figure 2. Cross-section diagram of both active and passive components of technology.

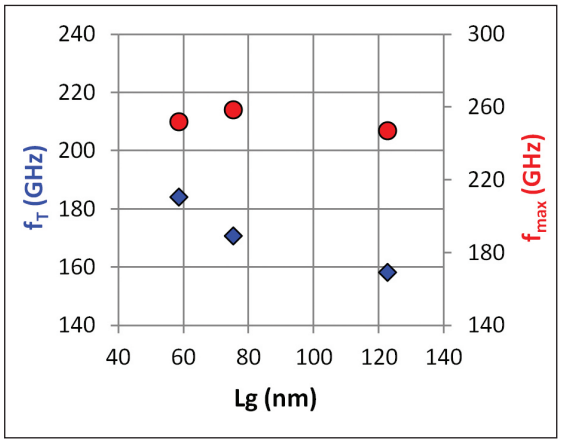
... and characteristics

Device characteristics determine whether our 70 nm GaAs pHEMT technology can be used for W- and D-band operation, and in particular whether these devices deliver sufficient gain and output power. The major aim of our 70 nm GaAs pHEMT development programme has been to enhance gain performance, while maintaining the output power provided by 100 nm GaAs pHEMTs.

According to DC characteristics, shrinking the gate length from 100 nm to 70 nm trims the on-state resistance by 21.6 percent, falling from 0.83 Ω mm to 0.65 Ω mm (see Figures 3 (a)). Transfer characteristics, using a drain voltage of 4 V, determine that our 70 nm GaAs pHEMT produces a maximum drain current of 701 mA mm^{-1} at a 0.5 V gate voltage, and has a D-mode threshold voltage of -0.97 V (see Figure 3 (b)). Peak transconductance is 760 mS mm^{-1} at a -0.16 V gate voltage, implying that the device is behaving in an appropriate manner, and can operate with a



➤ Figure 3. DC characteristics of (a) output and (b) transfer characteristics for 70 nm GaAs pHEMT.



➤ Figure 4. Correlation between the cut-off frequency (f_t), and the maximum oscillation frequency (f_{max}) and the gate length (L_g), based on a device with symmetric gate recess.

negative gate voltage. This is an attractive feature, reducing design complexity for circuit designers, who can simply use a different negative bias voltage to turn-on and to turn-off the transistor. As our 70 nm HEMT has similar values for the maximum drain current, threshold voltage and peak transconductance as its cousin with the 100 nm gate length, we expect the scaled device to deliver a similar output power.

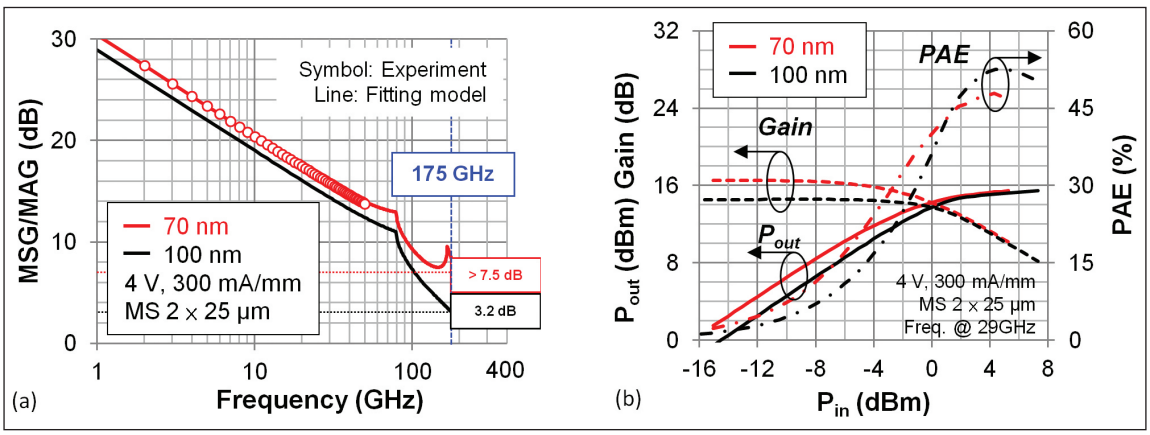
For millimetre-wave PA applications, the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) are great metrics for predicting the current gain and power gain, respectively, of the pHEMT. We use our pHEMT with a symmetric gate recess undercut to evaluate the relationship between the gate length, and both the cut-off frequency and the maximum oscillation frequency (see Figure 4). Scaling the gate length from 120 nm to 70 nm increases the cut-off frequency by more than 10 percent, but only delivers a slight increase in the maximum oscillation frequency, due to an increase in device access resistance. As power gain is a key characteristic for PA applications, it makes sense for us to slightly reduce the recess undercut on the source side, a modification that trims resistance and increases the maximum oscillation frequency.

We have also evaluated the maximum available gain and the output power of our 70 nm pHEMTs, using a drain voltage of 4 V, a drain current of 300 mA mm^{-1}, and a 2 × 25 µm device with a microstrip waveguide (see Figure 5). Compared with its cousin with a 100 nm gate length, our 70 nm pHEMT produces a higher maximum available gain across the D-band, with a minimum gain of 7.5 dB at 145 GHz, and 8 dB at 175 GHz. There is an increase in maximum available gain of 4.8 dB at 175 GHz, enabling the 70 nm GaAs pHEMT to support D-band PA applications

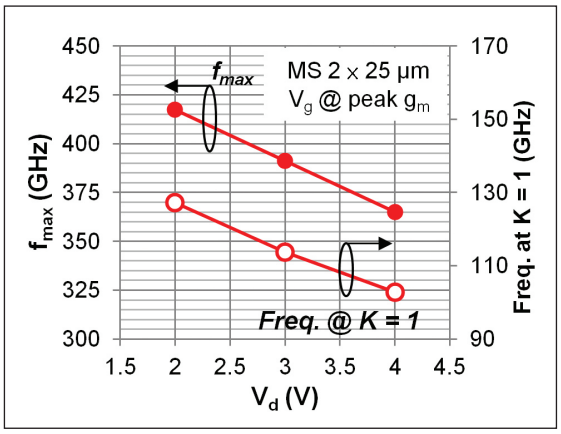
It's possible to adjust the operating voltage to trade one characteristic against another, and optimise amplifier design for a particular application. For example, when pHEMTs are used in optical transceivers, the operating bias is lower than mobile backhaul PAs, and the maximum available gain can be further increased by reducing drain bias. This point is illustrated in Figure 6, which plots the maximum oscillation frequency, and the frequency at a stability factor of 1, for our 70 nm GaAs pHEMT under different values for the drain bias. Lowering this bias to 2 V enhances the maximum oscillation frequency to 417 GHz, and should ensure a higher maximum available gain.

After this analysis of the small signal performance, we measured the large signal characteristic of our 70 nm device. According to a preliminary load-pull test, using a drain voltage of 4 V and a drain current of 300 mA mm^{-1}, our device produces an output power of 15.44 dBm (700 mW mm^{-1}) and a power-added efficiency of 47.8 percent at 29 GHz. These values are similar to those for the 100 nm pHEMT, a finding we attribute to similar figures for the maximum drain current and the threshold voltage. Our view is that the slight reduction in power-added efficiency for the 70 nm device is due to the matching impedance we employed. The conclusion we would draw from these results is that reducing the gate length of the pHEMT to 70 nm improves high-frequency operation, with higher gain realised, without detriment to the output power.

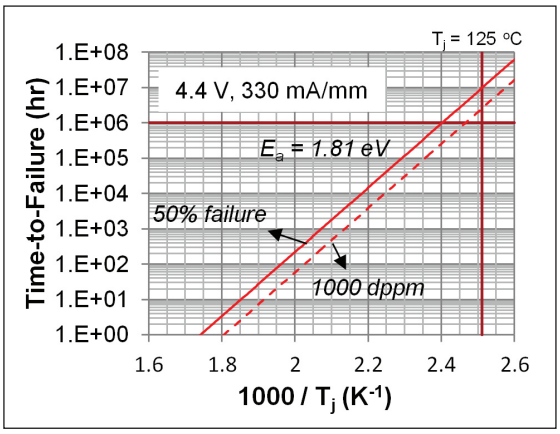
As well as impressive performance figures, a high level of reliability is crucial for commercialisation.



➤ Figure 5. RF characteristics. (a) The ratio of maximum stable gain (MSG) to maximum available gain (MAG), and (b) load-pull test for 70 nm GaAs pHEMT.



➤ Figure 6. Correlation of the maximum oscillation frequency (fmax) and frequency for a stability factor, K, of 1, as a function of the drain voltage.



➤ Figure 7. Reliability test result of 70 nm pHEMT.

We have evaluated this aspect of our device with an Arrhenius plot of time-to-failure, using a drain bias of 4.4 V and a drain current of 330 mA mm^{-1}, which is 10 percent higher than the maximum operation bias condition (see Figure 7). Defining device failure as a 20 percent degradation in drain current at a gate voltage of 0.4 V, values for the mean-time-to-failure and 1,000 defect-parts-per-million are 6.76 × 10^6 hrs and 2.70 × 10^6 hrs, respectively, at a junction temperature of 125°C. Activation energy is 1.81 eV.

Based on our characterisation, there is much to like about our 70 nm GaAs pHEMT, which combines a high maximum available gain with a high output power when operating at a drain bias of 4 V. We attribute these exceptional characteristics primarily to the short gate length and the asymmetric structure. While yield control is very challenging for manufacturing a device with a narrow gate length, it's an obstacle we've overcome, realising robust gate yields of more than 97 percent for 70 nm pHEMTs produced from 6-inch GaAs wafers. These strengths, alongside impressive device lifetimes, provide the proof that we are offering an attractive foundry service for W- and D-band PAs with our new 70 nm GaAs pHEMT technology.

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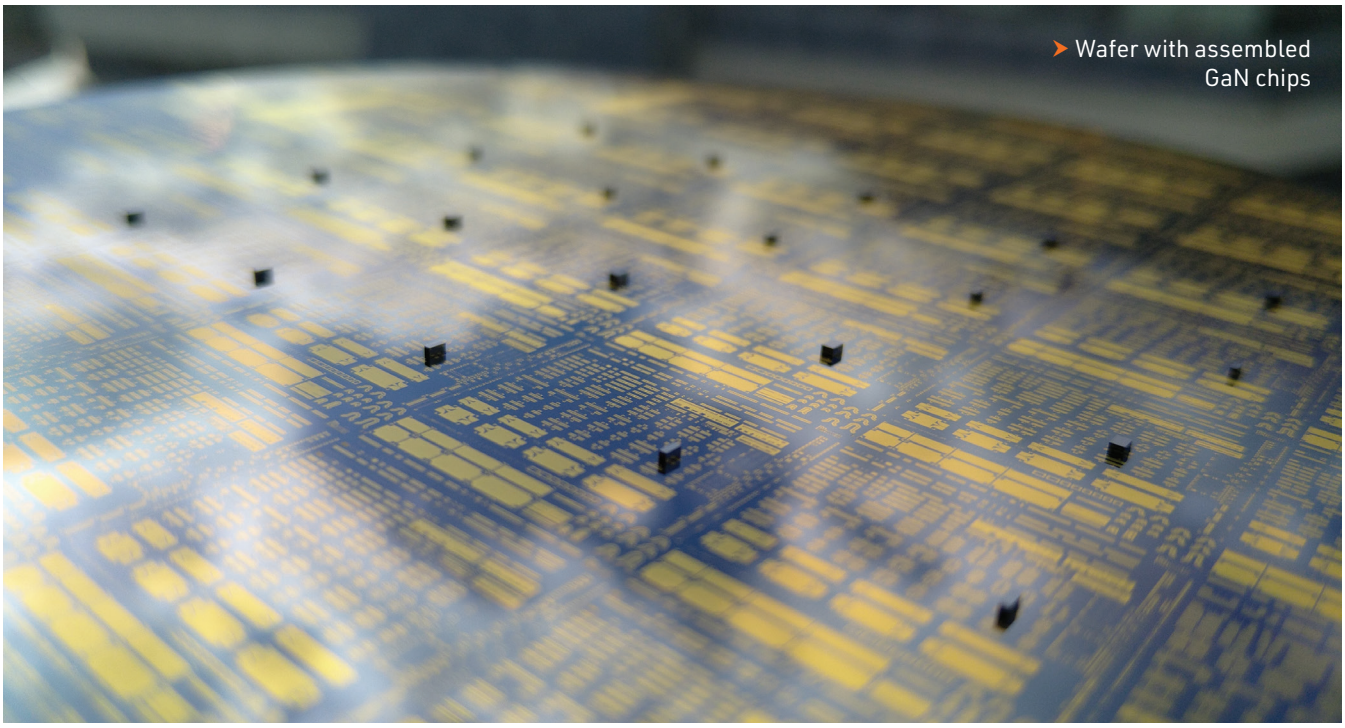


Wafer with assembled GaN chips

Boosting the bang-per-buck with RF integration

The hybrid integration of GaN and silicon paves the way for high-efficiency, cost-effective 5G and millimetre-wave RF systems that provide a cutting-edge power density and scalability

BY ALEXIS DIVAY FROM CEA-LETI

AS DEMAND for data skyrockets, telecommunication infrastructure is being pushed to its limits. To keep up with this growing demand, networks must evolve, not only by increasing their capacity, but by also reducing latency and enhancing global energy efficiency.

One promising solution to improving network performance is to boost data rates by moving to higher-frequency bands. They include the FR3 band, spanning 6 GHz to 24 GHz, and millimetre-wave frequencies between 24 GHz to 40 GHz, a band for 5G applications. However, while these higher frequency bands have the potential to provide faster data transmission and greater bandwidth, they come with a number of new challenges: realising a high energy efficiency; maintaining linearity, key to low distortion; and delivering a robust output power for better coverage and reliable communication.

In this context, the GaN HEMT has emerged as a key contender. It's a class of transistor that combines a cutting-edge power density with a high power-added efficiency, even at millimetre-wave frequencies, making it ideal for next-generation communication systems. However, hampering the deployment of the GaN HEMT in the communication sector is its lack of linearity. This metric is crucial for ensuring that amplified signals remain clean and undistorted. The degree of linearity directly impacts communication reliability, especially in high-frequency systems and those operating with very high modulation complexity.

To address these linearity challenges, engineers tend to turn to techniques such as digital pre-distortion, which compensates for amplifier non-linearities by pre-processing the signal. However, digital pre-distortion requires digital-to-analogue converters, which are not easy to integrate with compound semiconductors, such as GaN. This difficulty causes designs to be more complicated and complex.

Avoiding these pitfalls are silicon technologies – particularly CMOS and BiCMOS. They are well-

regarded for their ability to integrate digital and RF functionalities on the same chip. Valuing their integration are engineers, who benefit from another degree of freedom at the system level, and are able to design products that feature the co-existence of front-end RF modules and digital processing circuits. However, silicon-based RF devices are not a panacea. While highly integrated, they suffer from limitations in output power and efficiency compared with GaN HEMTs. This trade-off between power and integration leaves a gap that neither technology alone can fully bridge.

Merging silicon and GaN

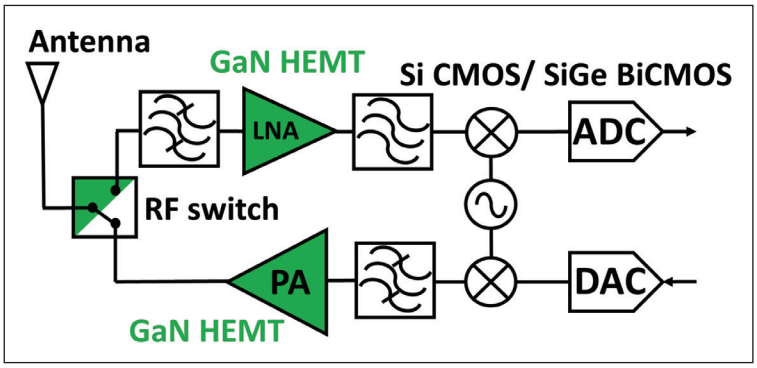
The solution lies in the hybrid integration of GaN and either CMOS or BiCMOS. By combining GaN RF transistors and silicon-based technologies, designers leverage the best of both worlds: the high power and efficiency of GaN for RF applications; and the advanced digital, analogue, and mixed-signal capabilities of CMOS/BiCMOS. Adopting this hybrid approach opens the door to more efficient, compact, and powerful systems that can serve a wide range of applications, from 5G infrastructure and satellite communication to radar systems and the Internet of Things (IoT).

Moreover, hybrid integration offers a cost-effective path forward. By stacking GaN RF transistors only on top of silicon RF and digital circuits, manufacturers can avoid high costs associated with large-area GaN chips. GaN die are significantly more expensive than silicon, so reducing the amount of GaN material while still benefiting from its performance can lead to significant cost savings. However, assembling these technologies in a tight space presents its own set of challenges, particularly at high frequencies.

When working at frequencies of several gigahertz or more, traditional assembly methods like wire bonding are inefficient, introducing signal losses that degrade performance. However, it's now possible to eliminate these connections, thanks to recent advances in 3D integration technologies that enable high-density integration of CMOS and III-V (GaN) transistors on the same chip. The upshot is lower parasitic losses, improved signal integrity, and faster signal transfer – all critical for high-performance RF systems.

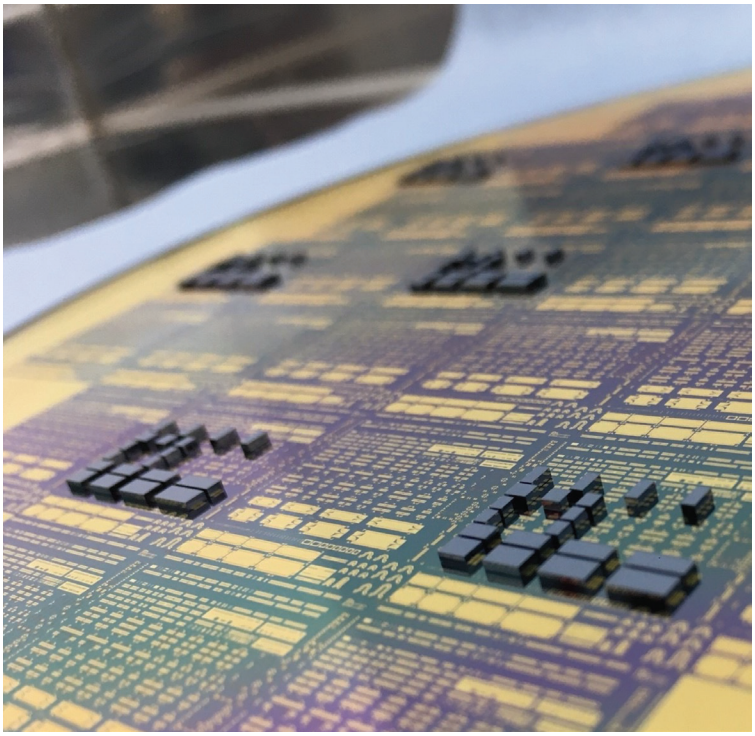
Several solutions have been developed for integrating GaN and silicon technologies, with copper pillars and hybrid bonding offering the most promise. The latter, which involves bonding at the wafer level, requires a back-end process that is fully compatible with CMOS technology, limiting its use to CMOS-compatible GaN processes. Meanwhile, copper pillars offer greater versatility, but their use with GaN-on-SiC technologies remains challenging, due to material and process complexities.

Recently, a variety of heterogeneous integration schemes have been proposed and tested, often involving sophisticated and unconventional processes. Looking to improve on this, our team at CEA-Leti has developed a simpler, more cost-effective approach. We begin by processing a GaN HEMT on a large-format silicon substrate using industrial processes and copper pillar growth, before dicing and stacking GaN devices on a silicon interposer. These steps ensure a performance that is close to the state of the art, crucially realised with a more scalable and economical process.

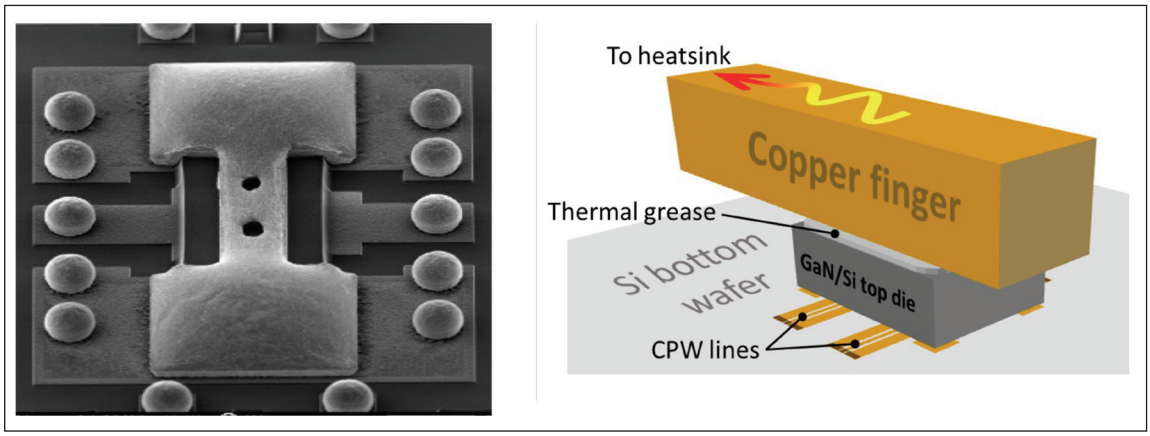


➤ Figure 1. An example of a heterogenous front-end module: RF amplifiers benefit from the figures-of-merit of GaN. RF signal generation and digital parts are in CMOS/BiCMOS.

Our hybrid integration of GaN and silicon opens up exciting possibilities for the future of RF communication systems. By combining the strengths of both these technologies, we create systems that not only excel in power and efficiency, but are cost-effective and scalable. This makes our approach to hybrid integration of GaN and silicon an ideal one for meeting the growing demands of 5G, satellite communication, and serving in applications beyond that.



➤ Figure 2. GaN dies stacked on 200 mm silicon RF interposer.



➤ Figure 3. (left) Transistor ready for pick and place assembly (right). Future package heatsink emulation using a copper finger, allowing higher electrical performance.

Cutting-edge RF technology

For more than a decade, scientists around the world have been striving to advance GaN-on-silicon technologies. Their motivation includes lower chip costs, increased volume, and the advantages that come from using 200 mm and 300 mm cleanroom tools. Offering enhanced process control, these more modern machines significantly reduce chip-to-chip variability and enable more reliable and efficient semiconductor devices. Our institution is a leader in this field, developing cutting-edge power and RF GaN HEMTs on 200 mm silicon substrates. These devices hold great promise for the next generation of high-frequency and high-power applications.

At the heart of this development is an RF GaN device, based on AlGaN/GaN epilayers grown on a high-resistivity 200 mm silicon <111> substrate. This high-resistivity substrate minimises RF losses to 0.27 dB mm^{-1} at 30 GHz, measured using coplanar waveguides at the final stage of the HEMT process. These minimal RF losses are critical for ensuring the overall efficiency of the amplifier, making this technology a strong contender for the future of RF systems. The relationship between RF losses and amplifier efficiency is well-known, as lower losses directly contribute to higher overall performance in high-frequency circuits.

The fabrication process for making these GaN HEMTs is fully CMOS-compatible and gold-free, ensuring integration with standard silicon manufacturing processes. Multi-finger transistors with coplanar access are produced using a TiN Schottky gate with a 150 nm gate length. The specific device discussed here has four fingers and a 50 μm gate width.

For this GaN-on-silicon transistor, operating at a current density of 1.35 A mm^{-1}, the cut-off frequency (f_T) is 83 GHz and the maximum oscillation frequency (f_{MAX}) 220 GHz. These are very encouraging frequencies for millimetre-wave applications, particularly those at 30 GHz, because the value for the maximum oscillation frequency is more than five times higher than the target operating frequency. This substantial margin ensures that the device offers high gain and excellent efficiency at millimetre-wave frequencies, making it ideal for 5G millimetre-wave and beyond-5G applications.

We have measured this device's large-signal performance at 28 GHz – a key frequency for 5G millimetre-wave communications – testing the GaN transistor in class AB operation. Under these conditions, and a nominal bias of 10 V, our device delivers an output power of 26.5 dBm at a power-added efficiency of 43 percent. When we double the initial bias to push the device harder, the power density climbs to 4 W mm^{-1}, translating to nearly 1 W of output power (29 dBm). This high power-density underscores the strength of GaN-on-silicon technology in handling the demands of high-frequency, high-power applications while maintaining efficiency.

For ease of testing, and to demonstrate the potential of 3D integration, we have stacked our GaN chiplets on a silicon substrate. We left our bottom silicon substrate as a passive interposer, featuring RF pads and coplanar waveguides, to facilitate connections to the flip-chipped GaN chiplet, which we bonded using copper pillars. We built the RF passive interposer, developed specifically for 3D RF system characterisation, on a trap-rich high-resistivity (2 kΩ cm) silicon wafer that's designed to minimise RF losses.

This high-resistivity silicon substrate helps us to address a common issue in silicon-on-insulator processes: parasitic surface conduction. With our configuration, the trap-rich design slashes this conduction, leading to lower losses and superior linearity of passive devices on the substrate. These benefits are critical for maintaining the high performance needed for RF systems, particularly at millimetre-wave frequencies.

To ensure precise measurement and calibration, our interposer design includes multiple thru-reflect-line calibration kits. These kits, along with various footprints designed to accommodate 3D GaN dies with widths ranging from 500 μm to 1 mm, ensures that our system can support future developments in GaN technology. The interposer's access lines have

RF losses of less than 0.25 dB mm^{-1} at 28 GHz.

Interconnect performance

To ensure optimal performance in high-frequency GaN devices, interconnections between the GaN chip and the interposer have to strike a delicate balance. On the one hand, these connections must be short enough to minimise parasitic effects – specifically resistance and inductance. These parasitics threaten to degrade signal quality and impair overall system efficiency, especially at higher frequencies. However, on the other hand, it's essential to position the GaN chip far enough from the interposer to prevent electromagnetic compatibility issues, which can disrupt signal integrity.

For our demonstrator, we employed copper pillars to realise the ideal interconnection height, while addressing both parasitics and electromagnetic compatibility concerns. We fabricated our pillars by electrochemical deposition on both the silicon substrate and the GaN wafer. To ensure robust electrical connections, we finished the GaN wafer with a tin-silver coating, a standard material for solder joints in advanced packaging. After growing our pillars, we carried out a solder reflow process on the GaN wafer to prepare the bumps for assembly. We then diced the GaN wafer into individual chips, which we precisely positioned using a pick-and-place machine. Finally, we used a second solder reflow to complete the 3D assembly. This process led to an interconnect height of 25 μm, with a pitch (the spacing between pillars) matching the same dimension, ensuring compact yet efficient connections between the GaN chip and the interposer.

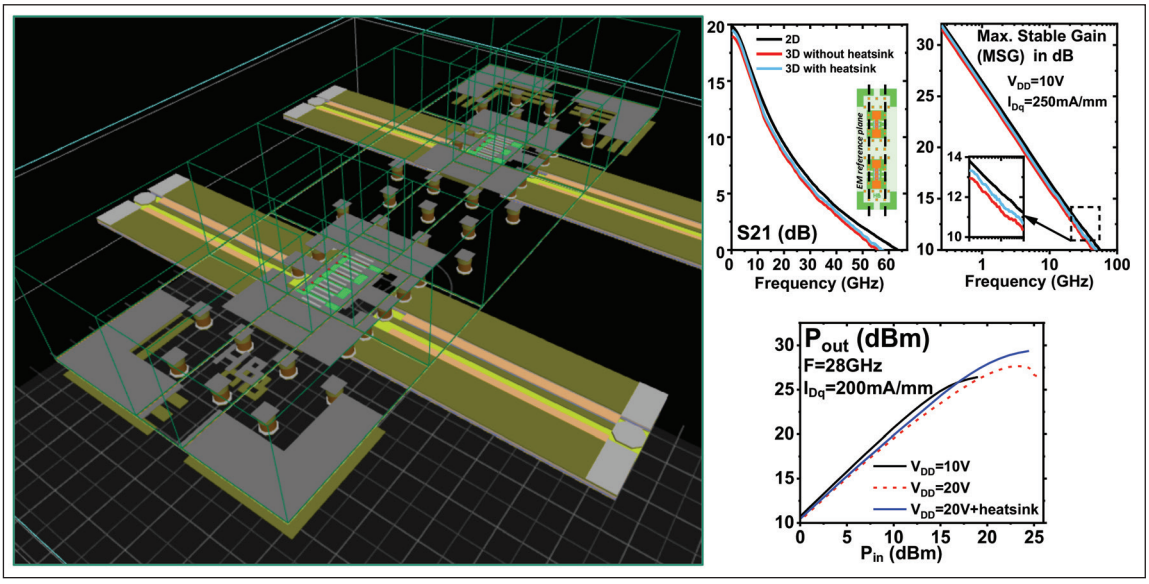
A key aspect of our development process has been the rigorous testing of the copper pillar interconnects under millimetre-wave conditions. We performed several RF measurements, considering both standard 2D transmission lines and daisy chains featuring copper pillars. These tests confirm the low-loss characteristics of the interconnects, showcasing insertion losses below 0.05 dB per 3D transition at 28 GHz using coplanar waveguides. Such minimal losses are significant at millimetre-wave frequencies. This level of performance ensures that multiple transitions – such as those at a transistor's input and output – can be incorporated without a substantial degradation in efficiency or signal quality. In practical terms, this opens the door to a higher degree of integration in GaN-based systems, allowing for more compact designs that do not compromise performance.

3D-GaN RF performance

When a GaN transistor is integrated atop a silicon interposer, it does not behave in the way it does in its native 2D configuration. While interconnect height and placement are optimised to reduce electromagnetic interference and minimise signal losses, thermal management becomes a critical challenge, especially when the transistor operates in power amplifier mode.

One of the first noticeable differences in resulting from the stacking of the GaN transistor is its higher thermal resistance compared with the 2D version. According to DC characterisation, current levels fall by around 20 percent when the device is handling a high dissipated power, a clear sign of thermal limitations. Under small-signal conditions – with S-parameter measurements taken up to 67 GHz – the device suffers from self-heating. Even at modest bias points, the transistor's temperature is higher by at least 75°C than the chuck temperature. This substantial increase in temperature stems from the relatively high junction-to-chuck thermal resistance in the 3D configuration, which restricts heat dissipation to through just the copper pillars that connect the GaN chip to the silicon interposer.

Despite these thermal limitations, our GaN transistor delivers a solid RF performance. At 28 GHz under large signal operation, it produces a power density



➤ Figure 4. (left) Schematic of the demonstrator's architecture, featuring two GaN transistors stacked on co-planar waveguide transmission lines through 25 μm height and width copper pillars. (right) RF performance of the stacked transistor. Thermal dissipation is mandatory for higher voltages/power densities.

of 2.2 W mm^{-1} at nominal voltage with a 41 percent power-added efficiency, showing minimal gain degradation. However, as the voltage increases, the self-heating effect becomes so severe that it causes the amplifier's performance to deteriorate significantly.

To tackle these thermal challenges, we have implemented an innovative but straightforward solution. This involves placing a copper finger that's coated with thermal grease on the backside of the GaN chip, emulating a future package with a dedicated thermal sink. This addition allows heat to dissipate more effectively by conduction, improving the RF performance and bringing it much closer to its original efficiency.

Turning to this heatsink has enabled us to halve DC performance degradation and recover almost 90 percent of the performance seen in the ideal 2D configuration, which operates on a thermal chuck. Small-signal gain shows only a 0.32 dB drop compared with the ideal case, and large-signal performance improves dramatically. Once again, our device delivers a power density of 4 W mm^{-1}, matching its performance in the 2D configuration, with no observed degradation during testing. We conclude that this simple thermal management strategy is highly effective, allowing nearly 1 W of output power to flow through the interconnects without performance loss.

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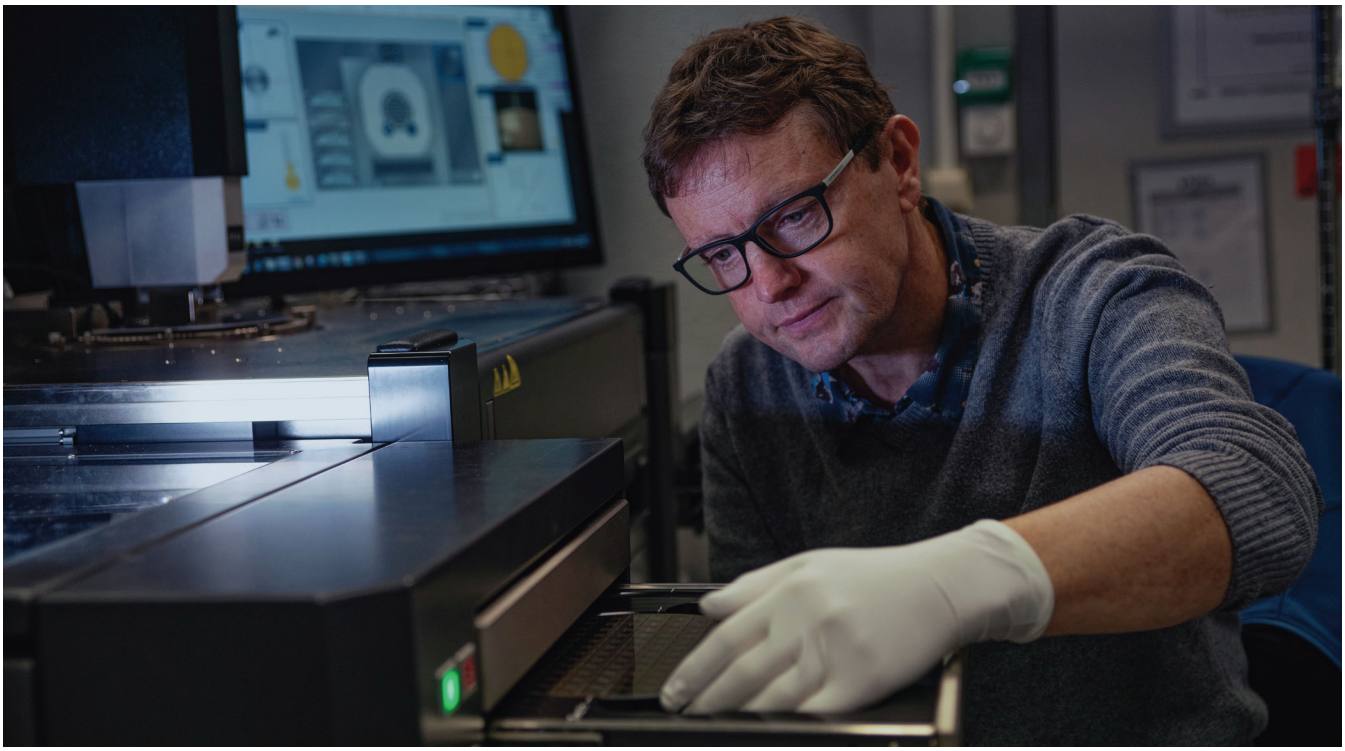
In addition to addressing thermal concerns, our chiplet integration of GaN with silicon offers several key benefits. One of them is that by employing a die-to-wafer bonding process, manufacturers can implement a 'known good die' approach, significantly boosting system yield. This merit has much value, given the lower yields typically associated with GaN technologies compared with high-volume 300 mm silicon CMOS/BiCMOS processes. Another advantage of our approach to integration is that it uses only the necessary GaN components, rather than an entire GaN-on-SiC MMIC, enabling a reduction in the overall GaN footprint used in a given front-end module or RF system, leading to substantial cost savings.

However, there are still challenges. Amongst them, one of the most significant is the low pick-and-place machine assembly speed for small dies – that is those with a width below 1 mm. Our colleagues at CEA-Leti are currently working on this issue, which must be resolved to obtain a competitive solution.

Looking ahead, our plan is to introduce additional design improvements that will focus on minimising impedance mismatches in the 3D configuration to ensure optimal RF performance. We are also aiming to undertake advanced 3D thermal simulations to refine the design guidelines for heterogeneous GaN-CMOS/BiCMOS power amplifiers utilising copper pillar technology.

In parallel, we will continue to develop new GaN demonstrators delivering an enhanced performance. These future designs will feature advanced AlN barriers and MIS gates that push power density even further, to exceed 6 W mm^{-1} – a level previously only realised with GaN-on-SiC devices. By leveraging these innovations, our GaN-on-silicon technology is poised to bridge the performance gap with SiC, while offering the cost and integration benefits of silicon. It's an approach that's paving the way for next-generation high-efficiency RF systems.



Scrutinising traps in GaN MOS-HEMTs

Experiments expose the physical and energetic locations of defects that are impairing the performance and reliability of GaN MOS-HEMTs operating in 5G millimetre-wave bands

BY BARRY O'SULLIVAN FROM IMEC

TODAY'S mobile technology bears little resemblance to that of the 1980s. Long gone are the days when the only capabilities of the handsets were to make calls and send texts limited to 160 characters. Now mobiles combine the capabilities of a computer with an impressive camera for stills and video, and provide great communication almost everywhere, a benefit that is realised by uploading and downloading a tremendous amount of data at high speeds.

The latest generations of smartphones, and how they are used, account for the explosive growth in data traffic and an unabating need for higher bandwidth. Both show no signs of slowing, and are more likely to accelerate, due to the onset of a new era that will incorporate artificial intelligence and virtual reality.

Helping to support the eye-watering ramp in data traffic is the steady upgrade to wireless infrastructure. Now being rolled out in its fifth-generation format, known simply as 5G, the latest technology is offering a significant leap in capabilities. When operating today at sub-6 GHz frequencies, 5G combines unprecedented data rates with ultra-low latency and the capacity to connect a massive number of devices simultaneously. This wonderful set of attributes is paving the way for a number of new applications, including smart cities, autonomous vehicles, and the Internet of Things (IoT).

The sub-6 GHz devices that are currently available are based on silicon-on-insulator technologies that utilise the scalability of the silicon microelectronics industry. However, this particular material system is held back by fundamental limitations in speed, an impediment that's opening the door to compound semiconductor materials, which have the potential to supplant silicon-based devices as the primary foundation for next-generation RF technologies.

This promising family of alternatives includes SiGe, InP and GaN. The latter is the stand out candidate, due to its superior electron mobility, high breakdown voltage, and its capacity to operate at higher frequencies and powers. Drawing on these strengths, allied to excellent thermal stability and efficiency, ensures that GaN-based devices are ideal for RF and microwave applications, including 5G infrastructure, radar, and satellite communications.

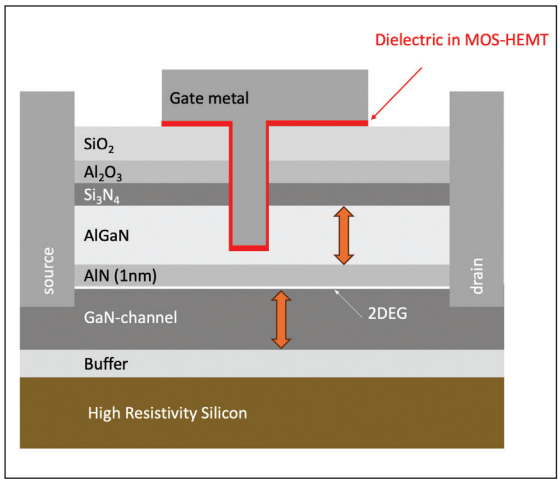
GaN-on-silicon technologies

At imec, we are currently investigating the potential of GaN-on-silicon technologies for millimetre-wave RF applications in the FR3 frequency range, which spans around 7 GHz through to 25 GHz. Our decision to work with GaN power amplifiers stems from their superior output power over other technologies at millimetre-wave frequencies, and when fabricated on silicon, their cost benefits. For this class of power amplifier, the core transistors are AlGaN/GaN HEMTs – they are renowned for their high-frequency performance and their ability to handle high power.

Scaling is a crucial lever for optimising the performance of RF transistors in applications for 5G and beyond. This miniaturisation can be lateral, involving a trimming of the width and length of the transistor, or vertical, realised by reducing the thickness of the layers. Benefits of lateral scaling include enhancing the speed and frequency response, while concomitant vertical scaling is required to tackle short-channel effects that threaten to degrade transistor performance. However, continued vertical scaling is a concern, as it can lead to an increase in leakage currents, particularly when the transistor is in the on-state.

One option for combating a scaling-induced hike in leakage current is to insert a high-κ dielectric between the gate metal and the AlGaN barrier. It's a move that creates a metal-oxide-semiconductor HEMT (MOS-HEMT) structure.

High-κ dielectrics are well-stablished, having been used in silicon technologies for the same purpose – to reduce leakage in ultra-scaled transistors – for the last 20 years. But their widespread application does not guarantee success, as they are notoriously defective materials. Due to reliability challenges faced when incorporating them in silicon-based logic devices, it is critical to study the impact that they have in MOS-HEMTs.



➤ Figure 1. A design of MOS-HEMT devices with a gate dielectric deposited in a partially recessed AlGaN layer.

Here we present the key findings of one of the first reliability studies for GaN-on-silicon MOS-HEMTs for power amplifiers, an investigation that we first reported at the 2024 IEEE International Reliability Physics Symposium (IRPS) and published in its proceedings.

An important finding from our study is that there is charge trapping and emission in the HEMT-structures with high-κ dielectrics. During our investigations, we successfully isolated the physical and energetic location of the responsible defects. We found that trapping and emission occur when charge carriers in the device are confined in, or released from, certain defects in the semiconductor or dielectric material. These processes impact the performance and the reliability of the HEMT, especially in high-frequency and high-power applications. Another outcome of our research is that it has identified the best material combinations and layer thicknesses for overall device process optimisation.

Capturing electrons from the dielectric

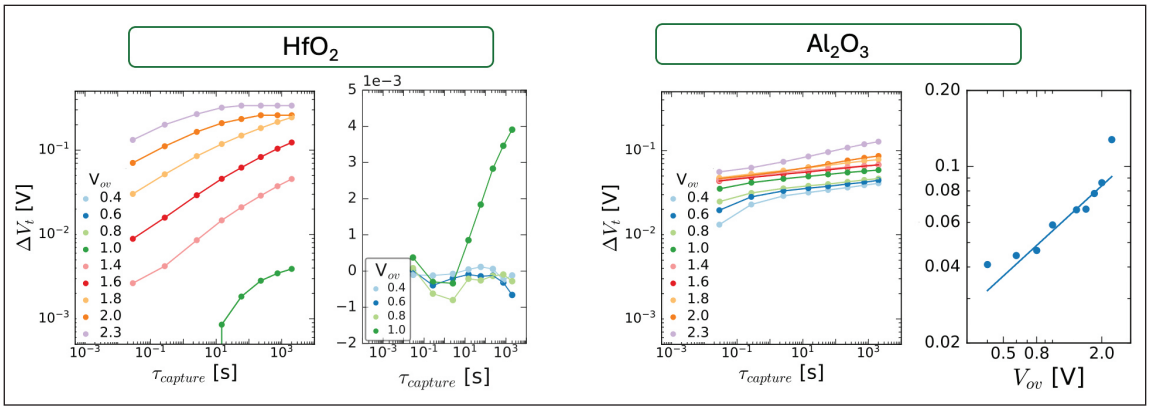
A primary reliability concern affecting the MOS-HEMT is bias temperature instability (BTI), an affliction that leads to device degradation over time, due to prolonged exposure to electrical stress (bias) at elevated temperatures. The root cause of this issue is a trapping of electrons, either in the dielectric or at the interface between the dielectric and the semiconductor layers. One consequence of BTI is a gradual shift in threshold voltage. Due to this shift, transistors require more voltage to switch on, and ultimately circuits are slower and less efficient.

We have mimicked BTI by applying a DC voltage or 'stress' to MOS-HEMTs with HfO_2 and Al_2O_3 high-κ dielectrics and monitoring the shift in threshold voltage. For variants with Al_2O_3-stacks, the threshold voltage increases with time and bias, indicative of defects present over a wide bias and energy range. In the case of HfO_2, we observe two modes of degradation. At lower voltages the plots show HEMT-like time-independent and negligible charge trapping, while at higher stress bias we see significant threshold voltage shifts, with a power law increase with time and bias until saturation at around 300 mV. This high degree of bias dependence suggests a relatively narrow defect type in this stress range.

A key question is this: Are charges trapped in the bulk dielectric or at the interface? We are able to differentiate between these two locations by observing how the shift in threshold voltage responds to changes in thickness of the high-κ dielectric, using capacitance measurements and simulations. This approach has determined that most of charge trapping happens in the bulk dielectric.

Emission behaviour: 3 types of defect?

Switching off the stress that's applied to MOS-HEMTs can lead to the release or emission of trapped charges. By analysing these emission

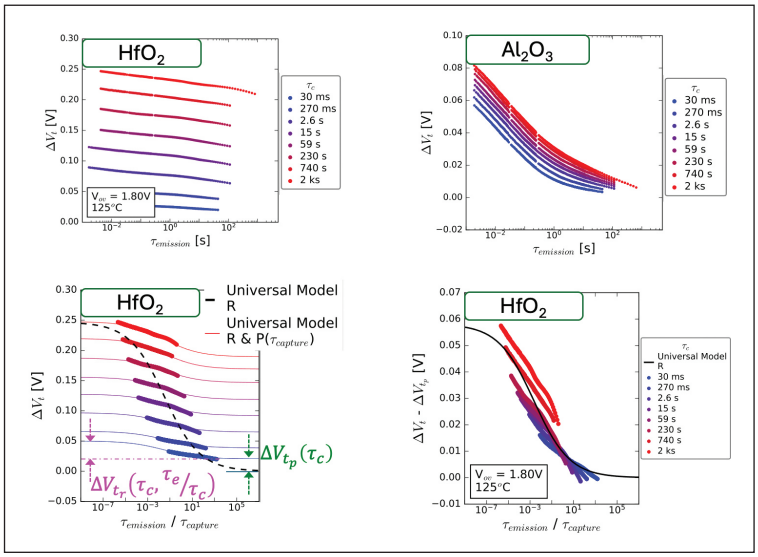


➤ Figure 2. The charge trapping characteristics of MOS-HEMT structures with HfO_2 or Al_2O_3 high-κ layers. Al_2O_3 results shows the threshold voltage, V_t, increasing as function of time and bias, suggesting defect types with a wide energy range. HfO_2, on the other hand, shows negligible trapping at low biases but, there are significant V_t shifts at higher bias. This points to a relatively narrow defect type in this bias range. Figure based on O'Sullivan *et al*. IRPS 2024.

dynamics, it's possible to gain insight into the reliability of the device, by looking at the recovery of the threshold voltage, and the origin of the defects.

Our results reveal that the defects responsible for the shift in threshold voltage in Al_2O_3 MOS-HEMTs release their charges quickly and completely. In comparison, devices with HfO_2 emit charges more slowly, and this process remains incomplete. Based on these findings, there is a difference in the nature of the defects responsible for charge trapping on changing the dielectric material.

To determine how many types of defects are present in our HfO_2 MOS-HEMTs, we fitted our experimental results to the universal relaxation model. This model assumes that for every type of defect present, the individual defects of that nature have their own characteristic energy, following a certain distribution.



➤ Figure 3. (Top) Emission kinetics of (left) HfO_2 and (right) Al_2O_3 MOS-HEMTs after stressing for increasing times. Note the difference in emission behaviour between Al_2O_3 and HfO_2, which only partially emits. (Bottom) Fitting data to the universal relaxation model shows that HfO_2 emission is described by (left) a recoverable component, (right) a permanent component and a third component, as the data doesn't match the fit well. Figure based on O'Sullivan *et al*. IRPS 2024.

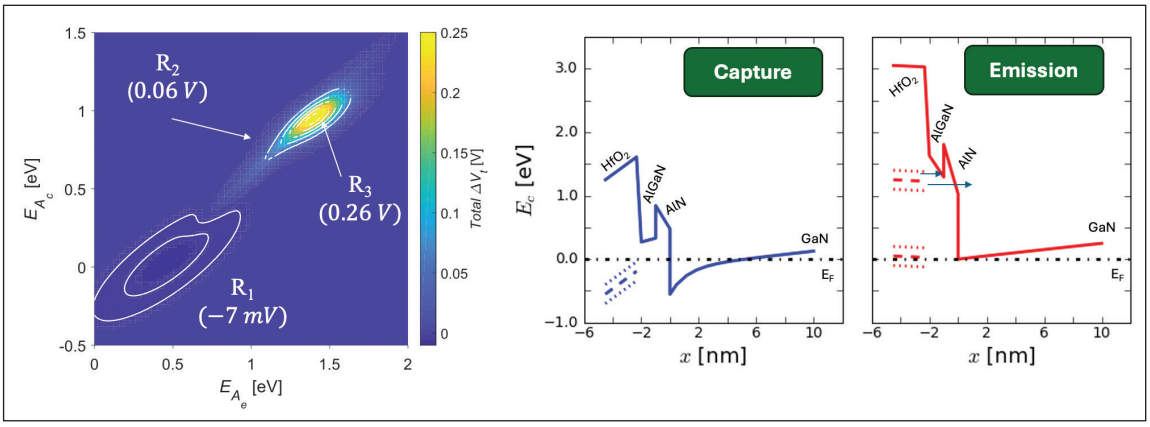
Fitting this model to our HfO_2 data clearly shows that more than one defect level is at play; the emission data is not overlapping the model. Our simulation only considered defects that display complete emission, a situation that occurs when the threshold voltage is recovered. However, in some cases the trapped charges do not emit from the defect, and the change in threshold voltage is permanent. When this permanent component is added to the model, it aligns more closely to the experimental data. Note, though, that the fit is not perfect. While the difference might only be 10 mV, this suggests that there are a total of three different defect types present in the HfO_2 MOS-HEMTs.

This finding differs from previous studies on Al_2O_3 dielectrics. According to these reports published in the literature, only two defect types contribute to the charge trapping in Al_2O_3 dielectrics. However, there is a wide distribution of defects in Al_2O_3 that complicates further detailed analysis.

Scrutinising HfO_2 devices

The next step in our study involved investigating how the defects in HfO_2 MOS-HEMTs contribute to the threshold voltage shift. Armed with this knowledge, we gained greater insight into device stability.

By calculating the activation energy that's needed for defects to capture and release charges, we have mapped out three different defect types for HfO_2. They are: a low thermally-activated defect, which we name as R1, that captures and emits electrons quickly; and a pair of higher activation-energy defects, denoted R2 and R3, that have similar charge capture rates but emit charges differently. According to the band diagram for our HfO_2 MOS-HEMTs, during application of the bias voltage,



➤ Figure 4. (Left) The activation energy map for HfO_2 MOS-HEMT showing the three defect types modelled to explain the measured BTI behaviour. (Right) Simulated band diagram of HfO_2 MOS-HEMT, showing electrons filling the shallow defect during capture and emission from 3 defect types. Emission from the shallow defect can be either to the channel (recoverable) or the AlGaN conduction band (non-recoverable), while simultaneously the deep HfO_2 level can be charged, explaining the increasing threshold voltage, V_t, seen at low temperatures. Figure based on O'Sullivan *et al*. IRPS 2024.

electrons are captured into a shallow defect in the dielectric, located about 2 eV below the conduction band of HfO_2. As this defect level is not accessible energetically at a low stress bias, charge trapping becomes more pronounced at higher voltages.

The band diagram also helps explain why the removal of the bias causes some of the captured electrons to be emitted back into the GaN channel, leading to a recoverable threshold voltage shift (R2). That's not the case for all electrons, with some still trapped in the energy barrier between the HfO_2 and AlGaN layers, a situation that results in a permanent threshold voltage shift (R3). This difference in emission behaviour reveals that while the same defect type is behind the threshold voltage shift, it must be modelled as two separate defects, due to the two emission pathways.

We have also identified a deeper defect, about 3 eV below the conduction band, that contributes to the negative threshold voltage shift (R1). These electrons are trapped during the recovery phase.

Improving reliability

This study of ours provides crucial insights into how different high-κ dielectric materials, particularly HfO_2 and Al_2O_3, affect the performance and reliability of MOS-HEMT devices. By identifying multiple defect types in HfO_2, with varying charge capture and emission characteristics, we highlighted how these materials respond differently under electrical stress.

Based on our findings, we would argue that Al_2O_3, with its faster charge recovery, probably offers better stability for applications requiring rapid switching. Meanwhile, HfO_2 shows more persistent threshold voltage shifts due to slower emission, which could impact long-term device reliability. Additionally, HfO_2 has higher defect densities, but they are energetically distributed across narrow energy ranges, whereas Al_2O_3 has a lower density of defects, but the responsible defects are distributed over a broader energy range. These insights are invaluable for optimising material combinations and layer thickness choices in high-frequency, high-power devices, allowing for improved designs that balance performance and durability across a range of applications.

Our next step is to compare our results with those for enhancement-mode HEMTs, which are devices that have a threshold voltage that's greater than 0 V. Intrinsically, HEMT-structures are depletion-mode devices – that is, the device is switched on at 0 V – but enhancement-mode operation is preferred for RF applications, as it reduces power consumption and increases reliability. Another benefit of enhancement-mode operation is that it simplifies circuit design, eliminating the need for either: voltage shifters, which create the negative voltage to switch off depletion-mode transistors; or for a multi-step device turn-on, which prevents short-circuits and power surges in depletion-mode devices.

Looking further ahead, we plan to study the RF performance of MOS-HEMTs with these dielectric layers, as well as the interaction between defect levels.

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Maintaining Momentum for the microLED

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Optimising Opportunities for SiC success

As sales of electric vehicles stutter, SiC revenues could face some bumps in the road ahead. So, what's the best approach to optimising returns in these uncertain times?

Expanding the Emission Envelope

What strategies will extract an even better performance from the various classes of lasers and LEDs? And what applications could benefit from these superior sources?

Ultra-wide Bandgap Materials: The Ultimate Devices

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Expanding the Emission Envelope

- Expanding the Spectral Range of GaN-based SLEDs
- Perfecting GaN VCSEL Production Process
- The Power of Pseudomorphic Nitrides

GaN: Going Beyond Fast Charging

- Achieving Avalanche in GaN-on-silicon Diodes
- Advancements in X-ray Metrology for GaN and Compound Semiconductors Presented by AIXTRON
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- Harnessing the Underestimated Potential of GaN in the Digitalization Revolution: A Catalyst for Unforeseen Innovation in Energy Efficiency
- Enhancing Analytical Accuracy of Active Epilayers in Compound Semiconductors by Multi-ion Species Plasma-FIB and Novel STEM Techniques
- Yole Group Presentation

Maintaining Momentum for the microLED

- Perfecting the Polychromatic Pixel
- MicroSolid Printing: Redefining the Future of MicroLED Displays
- Leveraging NIL for µLED Lens Packaging
- Pioneering Mass Production and Commercialisation of MicroLED Microdisplays for AR
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Optimising Opportunities for SiC Success

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ANGEL EVENTS

Xiuling Li group members working in the cleanroom: from left to right: Aadil Waseem, Henry Roberts, Moriah Weiss, and Gavin Latham.

Revolutionising semiconductor etching

Metal-assisted chemical etching is a damage-free process that produces trenches with an unprecedented aspect ratio

BY XIULING LI FROM THE UNIVERSITY OF TEXAS AT AUSTIN

IN THE RAPIDLY advancing world of semiconductor technology there's a relentless drive to scale device dimensions. Motivating this miniaturisation is a combination of enhancing performance, reducing power consumption, and increasing density across a wide range of applications – from logic and memory, to RF, photonics, and sensing. However, shrinking feature sizes and moving integration in the third dimension creates significant challenges for traditional etching techniques, which struggle to realise ultra-high aspect ratio vertical structures while preserving material integrity.

Offering much promise in this regard is metal-assisted chemical etching. This groundbreaking technique, also referred to as MacEtch or MACE, provides ultra-high anisotropy etching that's free from damage. It is an innovative approach that effectively addresses the limitations of conventional methods, and enables aggressive scaling of semiconductor devices and integration.

Here we explore the principles, applications, and future prospects of MacEtch. It's a technique that we are advancing at the University of Texas at Austin that has the potential to reshape the landscape of semiconductor manufacturing.

Detrimental damage

One of the most widely used techniques in semiconductor manufacturing, inductively coupled plasma reactive ion etching (ICP-RIE), offers high etching rates and excellent control over anisotropy. However, the presence of high-energy ions in the plasma tends to result in surface and sidewall damage, which becomes increasingly detrimental at reduced feature sizes. The damage manifests

as lattice defects, such as vacancies, interstitials, dangling bonds, surface roughness, and impurity accumulation.

An unwanted consequence of this damage is that it drags down device performance. Electronic devices may suffer from increased leakage currents, reduced speed, and lower breakdown voltages, issues that stem from the introduction of traps and degraded mobility; while optoelectronic devices can be impaired by a reduced efficiency, due to surface scattering and non-radiative recombination.

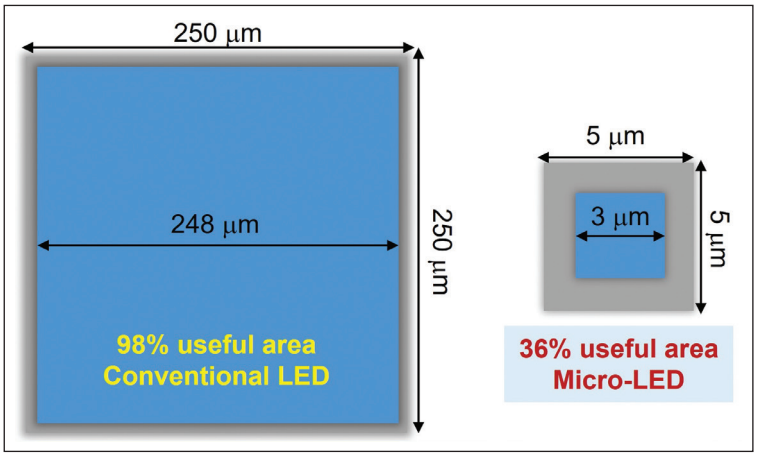
An example of the downside of RIE is that when it's used to process LEDs, device efficiency falls, primarily due to sidewall damage during etching. It's an issue that's particularly acute in microLEDs – as damage does not scale, the proportion of luminous area reduces significantly with device size (see Figure 1). Due to this damage, the external quantum efficiency of a blue-emitting microLED with dimensions of 5–10 μm is usually no more than 20 percent, a figure that falls far short of 70 percent, which can be realised with a broad-area blue LED.

When working with silicon, etch damage can mostly be repaired by thermal annealing if the thermal budget allows. But that's not the case for compound semiconductors – they are limited by different requirements for each element in the compound to restore lattice crystallinity and stoichiometry; the damage is extremely difficult to repair completely; and, in some cases, damage is irreversible. These problems are exacerbated when device or circuit dimensions or densities are of the order of tens of nanometres, a length scale where surface damage is detrimental. Due to these concerns, it is paramount to find a solution that allows precise, damage-free etching, a crucial requirement for continued scaling of semiconductor technologies.

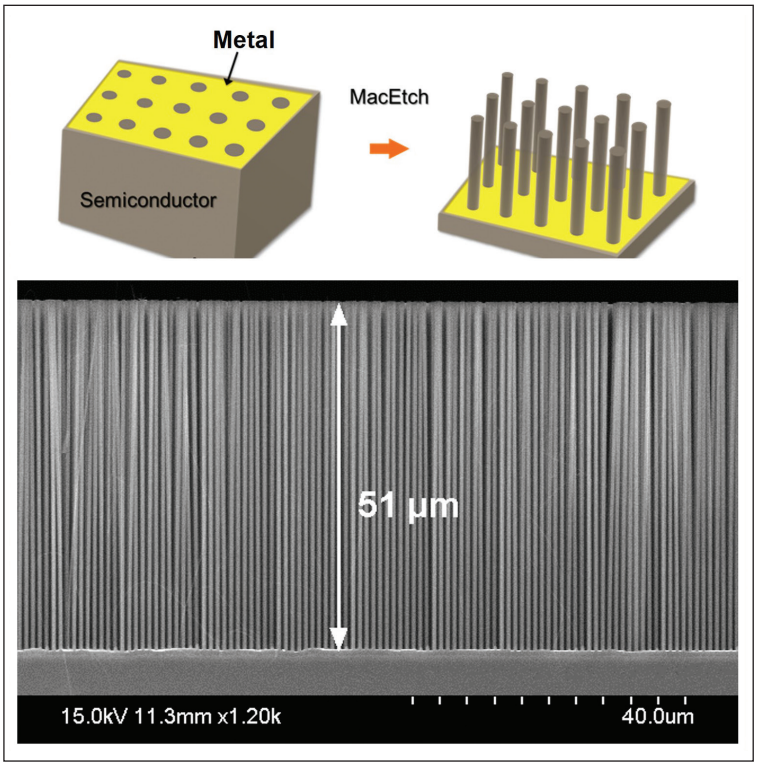
The conventional strategies for mitigating the damage caused by traditional ICP-RIE involve process optimisation. It's a task that demands the careful tuning of etching parameters, such as RF power, pressure, and gas flows, while maintaining etch rates and anisotropy; and it also requires the application of post-etch treatments, such as annealing or wet chemical treatments. However, these approaches often compromise the etch rate, anisotropy, or feature density, making ICP-RIE less suitable for high-throughput manufacturing. What's needed is a fundamentally different approach that is not held back by these limitations.

Not your ordinary etching

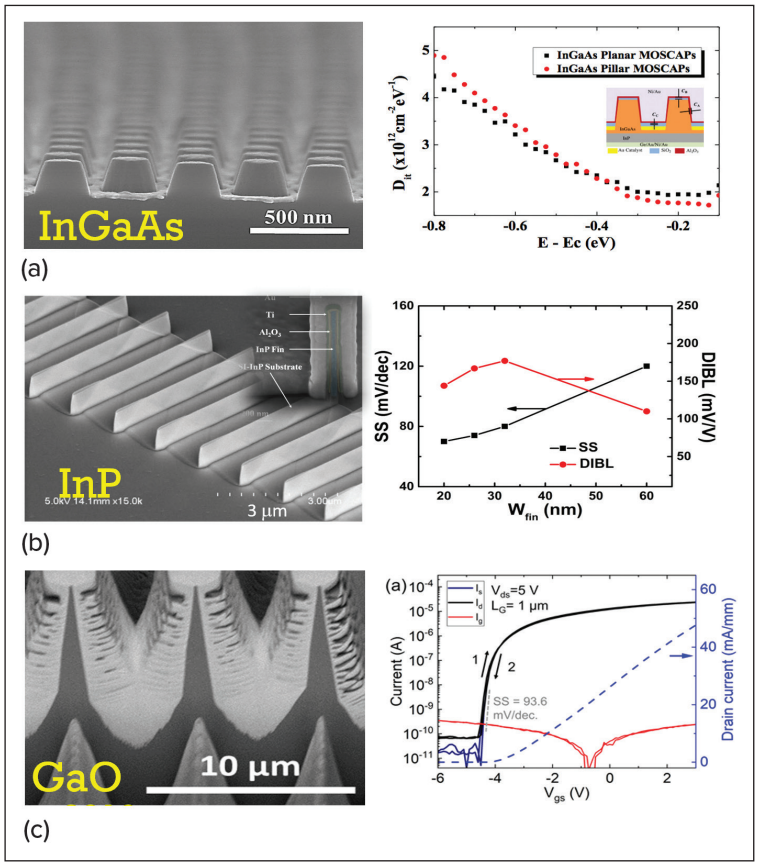
Defying the isotropic nature of the conventional chemical etch, MacEtch is an open-circuit, anisotropic etching method that is plasma-free, causes no damage and can take place at near-room temperature. Thanks to these strengths, MacEtch promises to transform the production of three-dimensional device structures for various electronics, photonics, energy, quantum, and



➤ Figure 1. Illustration (not to scale) of the effect of sidewall damage (assuming 1 μm depth) with microLED device size scaling – the damage does not scale and hence the percentage of luminous area reduces significantly with size.



➤ Figure 2. MacEtch process illustration and a scanning electron microscopy image of an array of silicon nanowires (diameter = 550 nm, depth = 51 μm) produced by gold-MacEtch. For more details, see X. Li., Curr. Opin. Solid State Materi. Sci. **16** 71 (2012) and K. Balasundaram *et al*. Nanotech. **23** 305304 (2012).



➤ Figure 3 (a). A scanning electron microscopy image of an InGaAs MOSCAP produced by MacEtch, showing nearly the same interface trap density (D_{it}) as that from the planar counterpart. For more details, see L. Kong *et al*. ACS Nano **11** 10193 (2017). (b). A scanning electron microscopy image of a InP FinFET structure (14 nm gate width and 50:1 aspect ratio) fabricated by MacEtch, with the cross section showing in the inset, demonstrating record subthreshold slope (SS). For more details, see Y. Song *et al*. IEEE Electron Dev. Lett. **37** 970 (2016). (c). A scanning electron microscopy image of a Ga_2O_3 FinFET structure fabricated by MacEtch, showing near-zero hysteresis in the transfer characteristic curves. For more details, see H.-C. Huang *et al*. Appl. Phys. Lett. **121** 052102 (2022).

sensing applications, and three-dimensional heterogeneous integration.

MacEtch relies on a local catalysis and an electron-transfer effect to enable site-controlled semiconductor nanostructure fabrication (see Figure 2 for a silicon MacEtch example). For this form of etching, a metal-patterned semiconductor is immersed in an acid (or base) and an oxidant mixture; and a metal catalyst is employed to provide anisotropic selectivity, by lowering the activation potential of the etching reaction locally. During this process, the semiconductor functions as the anode and the metal serves as the cathode. A local electrochemical cell under open circuit is created by the metal/semiconductor contact, working in tandem with the semiconductor/MacEtch-solution. The operation of this circuit dictates the direction of carrier transport during etching, thereby enabling anisotropic wet etching. Depending on the requirements of the structure, or the device, a number of metal catalysts can be employed, including: well-known noble metals, such as silver, gold, and platinum; CMOS-compatible ruthenium and TiN; as well as metal stacks.

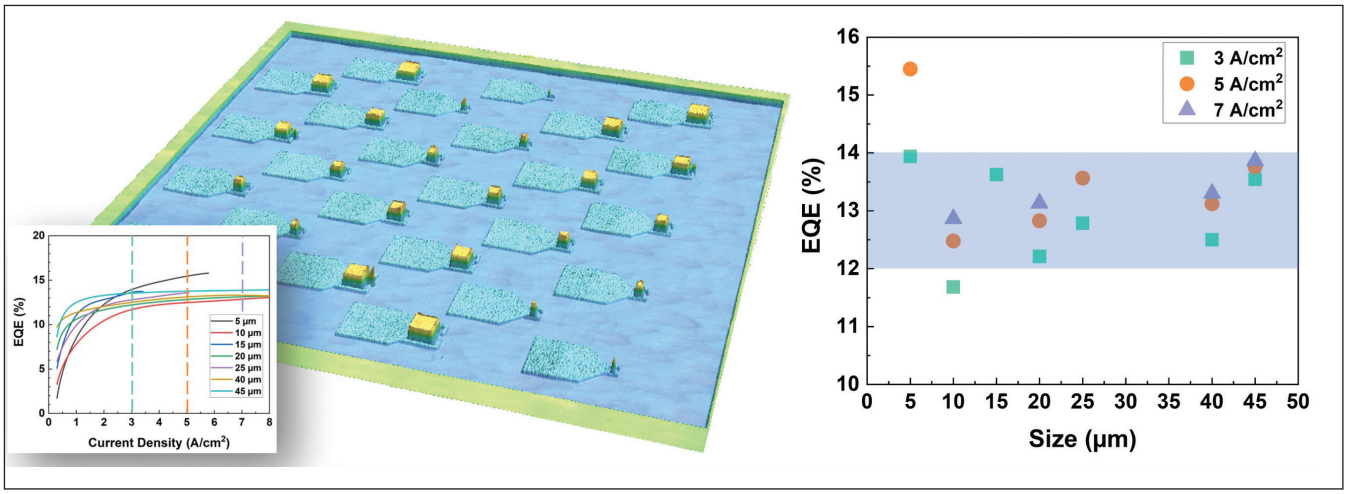
Our work on MacEtch began at University of Illinois, by using this technology as a method to generate porous silicon. This involved having a discontinuous layer of a noble metal catalyst metal film under open circuit in a solution of hydrofluoric acid and peroxide.

Since then, we have gone on to advance this technology, demonstrating the anisotropic MacEtch across a variety of semiconductor materials, and also opportunities at the device level. In addition, we have reported variations of MacEtch, such as inverse-MacEtch, magnetic field guided h-MacEtch, and self-anchored catalyst MacEtch.

What's more, we have demonstrated that MacEtch can be programmed fully in vapour phase, with independent control of flow rates, injection and synchronous or asynchronous pulse, and pressure. This form of MacEtch is a major milestone in the development of MacEtch nanotechnology, holding the promise for better uniformity and scalability.

Using MacEtch to process silicon, we have realised an ultra-high aspect ratio of more than 300:1 and an etch rate that's faster than 3 µm min^{-1}. We have also applied this etching technology to a wide range of semiconductors, including silicon, germanium, III-As, III-P, III-N, SiC, and Ga_2O_3.

Thanks to the combination of the readily achievable extraordinary aspect ratio, and the inherent absence of high-energy ion-induced damage, this innovative etching method has a profound impact on semiconductor fabrication. In our lab, we have championed this possibility, providing a number of examples of compound semiconductor structures produced by MacEtch that have device



➤ Figure 4. *hν*-MacEtch enabled external quantum efficiency (EQE) scaling of III-N microLEDs. Left: Three-dimensional profilometry (with *z* axis magnified for visual clarity, and actual height 780 nm) of an array of fully fabricated InGaN/GaN/AlGaN based microLEDs of 5 - 45 μm in pixel size, with the multi-quantum well region and the *n*-side etched by *hν*-MacEtch. Inset shows the EQE as a function of injection current density. Right: Plot of EQE as a function of LED size, showing only ±1 percent variation from 5 – 45 μm size. For more details see C. Y. Chan *et al*. Adv. Opt. Mater. **12** 2302957 (2024).

characteristics that are only possible with damage-free sidewalls. These examples, shown in Figure 3, include: an InGaAs pillar metal-oxide-semiconductor capacitor with no degradation of interface charge density; an InP finFET with record-high aspect ratio, and a near-ideal sub-threshold slope; and a Ga_2O_3 finFET with near-zero hysteresis.

Successful scaling of microLEDs

For wide and ultra-wide bandgap semiconductors, such as GaN, SiC, and Ga_2O_3, there is a limited carrier mobility that applies the brakes to the MacEtch rate. To address this, we are turning to above bandgap photons, which generate free electron-hole pairs. For this form of etching, which we refer to as *hν*-MacEtch, the redox reaction extracts electrons from the semiconductor, driving a charge imbalance, with holes left at the surface to oxidize the semiconductor. This process is an inherently inverse-MacEtch, because the UV light does not penetrate the metal catalyst film. However, there is an additional degree of freedom, the photon energy, that enables selective etching based on the bandgap energy of the semiconductor. This feature allows *hν*-MacEtch to be used to release heterostructures laterally.

Note that simply illuminating samples with an above bandgap light source in the absence of an oxidant does not induce directional etching. It is possible to induce a photocurrent by applying an external bias under illumination – these are the conditions for the well-known photoelectrochemical etching. However, in that case there is a need for an externally applied anodic bias, a requirement that might be challenging to scale, in terms of current density uniformity, when the feature size is aggressively reduced to produce microLEDs with dimensions of just a few microns. In contrast, the positioning of the metal catalyst in *hν*-MacEtch defines the etching pattern and resolution, and can be readily removed after etching. Thanks in part to this, *hν*-MacEtch has the simplicity and versatility to produce damage-free anisotropic structures of III-N multi-heterojunctions with a desired profile in a single step under open-circuit.

We have created an array of InGaN/GaN/AlGaN blue microLEDs that are 5 μm to 45 μm in size, with MacEtching employed to define the mesa of the multi-quantum well active region. While MacEtch does not cause damage, as no additional defects are generated, optimal device performance still demands the passivation of surface dangling bonds. However, even without optimisation of surface passivation and the metal contact, the microLEDs produced using MacEtch show improved performance. Gains include: reaching a peak external quantum efficiency at a lower current density of around 1 – 2 A cm^{-2}; producing a level of performance that is much less dependent on size than that for microLEDs produced using conventional RIE, an absence of efficiency droop, and with values almost converging at a higher current density.

MacEtch is particularly well suited to defining deep trenches or pillars with high aspect ratios, forming periodic or random arrays of patterns, or providing shallow surface texturing. These strengths will enable MacEtch to have a disruptive and lasting impact on many fronts

While these observations highlight that *h*ν-MacEtch holds extreme promise for unlocking the potential of scaling the high-pixel-density of microLEDs, significant barriers still remain in the way of realising industry metrics for pixel density, brightness, and cost. In addition to detailed process optimisation, there are a number areas for improvement for MacEtch to unleash its full potential in microLED display manufacturing. They include: overcoming band-bending in the *p*-side of III-nitride structures; transitioning to vapour-phase *h*ν-MacEtch for better etchant delivery and manufacturability; and tuning the sidewall profile, surface termination, and passivation of microLED dies to enhance readout efficiency and reduce surface states. On top of this, there is a need to extend the capabilities of MacEtch to III-N green and red microLEDs, as well as AlInGaP-based cousins, to advance high-pixel-density full-colour display capability, as well as high modulation bandwidth optical communications.

This is a long list, but working through it will bring significant rewards. Triumphs could include breaking size limits and unlocking high-pixel-density microLED arrays for cost-effective high-resolution displays in AR/MR/VR, and addressing the data transmission bottleneck in computing and communication by enabling high-speed, low power, chip-to-chip interconnects.

Transformative potential

To conclude, MacEtch is not just an incremental improvement – it represents a paradigm shift in semiconductor fabrication. The simplicity of the MacEtch process, along with its versatility, manufacturability and its plasma-free damage-free nature, make it highly promising to supplement and enhance the well-known reactive-ion etching methods. In this regard, MacEtch is particularly well suited to defining deep trenches or pillars with high aspect ratios, forming periodic or random arrays of patterns, providing shallow surface texturing. These strengths will enable MacEtch to have a disruptive and lasting impact on many fronts, with an impact in various electronics, photonics, energy, quantum and bio-sensing applications, as well as three-dimensional heterogeneous integration.

As the semiconductor industry pushes toward even smaller feature sizes and more complex architectures, we have no doubt that MacEtch's role will expand, offering a pathway to the next generation of high-performance, low-power electronic and photonic devices, and potentially bio-medical sensing and detection. While the groundwork has been laid through successful device-level demonstrations and detailed mechanism studies, the true test lies ahead: manufacturability. The journey from lab to fab is underway, and the destination promises to redefine the limits of what's possible in semiconductor etching technology.

The author is deeply indebted to her current and past students and postdocs, who contributed to the ideas and implementations of various aspects of the MacEtch technology, especially Clarence Chan, Lukas Janavicius, Hsien-Chih Huang, Zhongjie Ren, Henry Roberts, Xihang Wu, Gavin Latham, Julian Michaels, J.D. Kim, Yi Song, Karthick Balasundaram, Parsian Mohseni, S.H. Kim, Matthew Dejarld, Lingyu Kong, Wen Huang, Jae Cheol Shin, and Munho Kim, as well as many long-term collaborators, especially James Coleman, Paul Bohn, Ilesanmi Adesida, John Rogers, Placid Ferreira, Weidong Zhou, Paul Braun, Zetian Mi, and Dane Sievers. Financial support from NSF (including NSF #2200651 and #2329107), ARO (MURI #W911NF2110337), the Welch Foundation, and various industry gifts are greatly appreciated.

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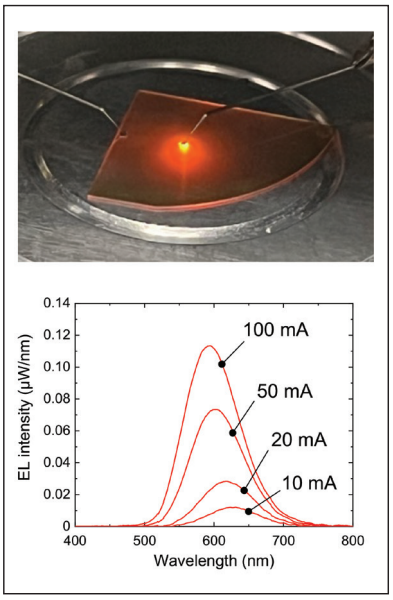
Realising red LEDs on $ScAlMgO_4$ substrates

$ScAlMgO_4$ substrates provide a foundation for producing LEDs with lattice-matched, indium-rich quantum wells

A COLLABORATION between engineers based in Saudi Arabia and Japan is claiming to have broken new ground by producing the first red-emitting LEDs on $ScAlMgO_4$ substrates.

According to this team from King Abdullah University of Technology, Saudi Arabia, and Aichi Institute of Technology, Japan, the $ScAlMgO_4$ substrate is a promising platform for growing nitride emitters in the red, green and blue. Success on that front would pave the way for the production of pixels with a single material system that emit all three primary colours, which is an attractive option for display applications.

A significant challenge for traditional red-emitting GaN-based LEDs is that their high indium content needed to propel emission to a relatively long wavelength leads to a large lattice mismatch, degrading material quality and impairing radiative recombination. To reduce in-plane stress during InGaN growth, many research groups from around the world have pursued a number of novel approaches – they involve the likes of porous GaN, InGaN pseudo-substrates, InGaN decomposition layers and sputtered AlN layers. This body of work highlights the benefits from increasing the InGaN growth temperature, key to higher crystalline quality.



➤ Significant indium compositional fluctuations in the quantum well account for broad electroluminescence.

Building on this promise, the partnership between researchers in Saudi Arabia and Japan has shown that it's possible to produce red-emitting LEDs on $ScAlMgO_4$, a foundation that provides lattice matching with $In_{0.17}Ga_{0.83}N$.

While these engineers are not the first to grow InGaN layers on $ScAlMgO_4$, the epilayers produced by other groups are plagued by poor material quality, high levels of impurities, and surface roughness.

Avoiding these issues, the team from Saudi Arabia and Japan have produced their red LEDs on a low-temperature buffer layer with a Ga-polar structure that helps to reduce residual electron concentrations and realise an effective *p*-type InGaN layer.

Devices grown on this foundation and featuring a 4 nm-thick InGaN quantum well have an emission peak at 629 nm when driven at 20 mA. Spectral width of this electroluminescence is relatively broad, with a signature that's similar to that for InGaN quantum dot structures, suggesting that the wells have significant compositional fluctuations in indium content.

Cross-sectional bright-field scanning tunnelling electron microscopy of the red LEDs reveals a high density of V-pits, generated through threading dislocations. This sub-optimal growth is attributed to insufficient recrystallisation of low-temperature buffer layers.

Another drawback of producing red LEDs on $ScAlMgO_4$ is the high cost of the substrate. Team spokesman Kazuhiro Ohkawa told *Compound Semiconductor* that the price of this substrate, limited to just 2 inches in diameter, is more than two orders of magnitude higher than that of sapphire.

While such a high cost could prohibit the commercialisation of red LEDs on this foundation, it is not a barrier to producing lasers – and that's the primary target of this team.

Working towards this long-term objective, Ohkawa and co-workers have already produced highly efficient InGaN-based red LEDs on sapphire, a result that is claimed to suggest that it will be possible to produce InGaN-based red lasers.

Ohkawa says that red LED structures on sapphire are complicated by strain-relaxing layers and defect-stopping layers – both eradicate the space that's needed for the waveguides. It's possible to avoid this issue by turning to $ScAlMgO_4$ substrates, thanks to better lattice-matching.

Crucial to the team's success is its home-built MOCVD tool that is capable of higher growth temperatures. This asset is key to higher crystal quality that enables a lower background electron concentration and ultimately *p*-type InGaN.

Before the team can try to produce InGaN red laser diodes, they will need to realise additional improvements in the crystalline quality of their epilayers. "Adding the waveguide layers will be the next step," remarks Ohkawa.

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SiC MOSFETs: Understanding the benefits of plasma nitridation

Annealing interfaces of SiC and SiO_2 formed by a process based on plasma nitridation reduces interface states and increases immunity to positive gate bias stress

ENGINEERS from Osaka University are offering new insights into the benefits of their novel approach to forming the key interface for SiC MOSFETs. The team has just determined that its approach – involving plasma nitridation of the SiC surface, sputter deposition of SiO_2, and post-deposition annealing – reduces the interface state density near the conduction band edge by more than an order of magnitude and delivers a substantial increase in immunity to positive gate bias stress.

These valuable findings highlight the benefits of moving away from standard approaches to making SiC MOSFETs, which despite significant commercial success suffer from a high on-resistance and poor reliability, according to the team from Osaka. This team attributes those weaknesses to a high interface state density and near-interface traps.

The Osaka University researchers say that interface nitridation with NO is widely used to reduce the interface state density and passivate defects. However, this approach is far from perfect: the reduction in the density of interface states is limited, probably due to saturation of nitrogen content at the interface; and there are reliability issues, such as a strong drift in threshold voltage with gate bias stress.

To address these concerns, the engineers from Osaka are pioneering an approach that suppresses nitrogen incorporation into SiO_2 while minimising oxidation of SiC. Their three-step process involves: plasma nitridation of the SiC surface; sputter deposition of SiO_2; and post-deposition annealing under CO_2.

According to the team, one of the benefits of this approach is that SiC is directly nitrided by a high-density plasma, enabling a high proportion of nitrogen atoms to be incorporated at the SiC surface. Additional merits of their approach include sputter deposition of SiO_2 in a pure argon atmosphere to minimise SiC oxidation, and a post-deposition anneal that reduces the density of defects in the SiO_2 dielectric.

The researchers previously established that their process trebled the density of nitrogen atoms incorporated at the SiC side of the interface, lowering the density of interface states to 1×10^{11} eV^{-1} cm^{-2}. However, they had not investigated the impact of post-deposition annealing on device characteristics.

They have just addressed this issue with a thorough investigation of the roles played by the particular gas employed and the temperature that's adopted for the post-deposition anneal. For this work, they produced SiC metal-oxide-semiconductor capacitors, using *n*-type SiC (0001) epilayers with a donor density of 1×10^{16} cm^{-3}. Following wet cleaning, they nitrided the surface of SiC for 30 minutes at 350°C with a high-density nitrogen plasma at 1.4×10^3 Pa, before sputtering a 30 nm-thick film of SiO_2 in a pure argon atmosphere. The final step involved a post-deposition anneal for 30 minutes under either CO_2 or argon at a temperature between 1050°C and 1250°C.

Comparing capacitance-voltage curves for annealing under CO_2 at different temperatures showed that carrying out this process at 1050°C ensured sufficient electron accumulation. However, this technique led to hysteresis and stretch-out due to interface traps. Both concerns were not found in capacitance-voltage plots for devices with a 1250°C anneal, suggesting a significant reduction in interface traps.

The researchers also observed a negative shift in the capacitance-voltage curve with increasing anneal temperature, indicating the presence of positive fixed charges at the interface.

Additional investigations by the team considered the trapped charge density and the energy distributions of interface states. For annealing under CO_2, the trapped charge density plumets with increasing annealing temperature. Under argon, the fall in trapped charge density is notably smaller, leading the team to conclude that the reduction in charge density is not simply an annealing effect, and involves a reaction of CO_2 molecules with interface traps.

Studying the energy distribution of the interface state density revealed that this fell with increasing temperature when annealing under CO_2. Switching to argon led to an insufficient reduction in interface state density, showing that the benefits of the team's process are not just plasma nitridation and minimised oxidation – they also include defect passivation by a CO_2 post-deposition anneal.

The team have also carried out stress tests, applying a positive stress bias for up to 2000 s at field strength of 5-8 MV cm^{-1}. This investigation revealed that a higher annealing temperature under CO_2 increases the immunity of the device.

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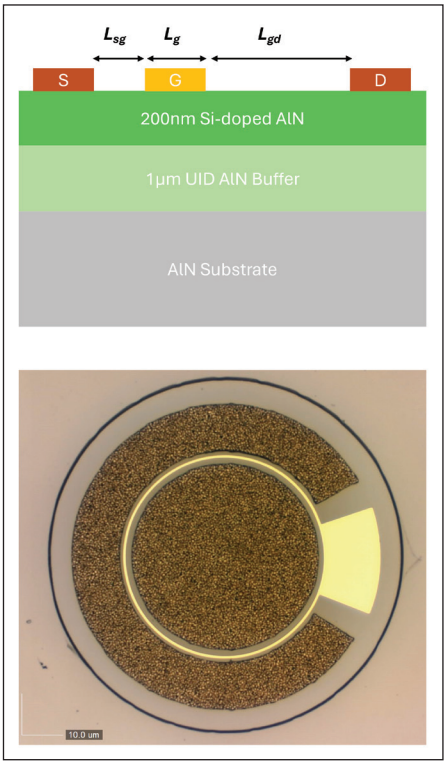
A debut for the native AlN transistor

AlN metal-semiconductor transistors grown on 2-inch AlN substrates provide a breakdown voltage of more than 2 kV

Researchers from Arizona State University are claiming to have fabricated the first AlN transistor that's grown on a native substrate. The team's metal-semiconductor FET (MESFET) has a breakdown voltage of more than 2 kV, alongside what's said to be 'decent' values for drain saturation current and the on-off ratio.

Spokesman for the team, Houqiang Fu, told *Compound Semiconductor* that there are opportunities for AlN MESFETs in power electronics and RF electronics, due to the potential of these transistors to operate at high voltages, high breakdown fields and high-power densities.



➤ AlN-on-AlN MESFETs have much promise as power and RF devices.

AlN, a member of the family of ultra-wide bandgap semiconductors that includes Ga_2O_3 and diamond, boasts the highest bandgap of 6.2 eV and the highest breakdown electric field of 12 MV cm^{-1}. It is these strengths have spurred interest in AlN devices, which need to overcome issues related to defects, doping and contacts. Examples of these challenges include an ionisation energy for silicon, the common *n*-type dopant, of more than 200 meV, and the tendency for metals to form Schottky-like contacts rather than ohmic ones.

The success of Fu and co-workers comes after reports from a number of groups of the fabrication of AlN Schottky barrier diodes on AlN substrates, and AlN MESFETs on foreign substrates.

Breaking new ground, the team from Arizona State University has produced the first AlN-on-AlN MESFETs by loading 2-inch AlN substrates from Hexatech into an MOCVD reactor and depositing: a 1 µm-thick AlN buffer layer; a 200 nm-thick *n*-type channel layer with a silicon doping concentration of 1 x 10^{19} cm^{-3}; and a 2 nm-thick GaN capping layer, added to protect the AlN layers from oxidation.

Characterisation of these epiwafers reveals a surface roughness, according to atomic force microscopy, of around 0.4 nm, and a dislocation density as low as 10^4 cm^{-2}, based on X-ray diffraction. As this dislocation density is at least three orders of magnitude lower than that for AlN-on-sapphire structures, there is the promise of improved device performance.

Device fabrication began by cleaning the surface of the epiwafer, before turning to conventional photolithography and lift-off processes to form isolated mesas by etching to a depth of around 700 nm into the resistive buffer layer. Electron-beam deposition added all three contacts, with the source and drain formed first, with annealing under nitrogen at 950°C for 30 s.

Electrical characterisation of the MESFETs revealed that the AlN ohmic contact is non-linear, a trait that is said to be typical for AlN and high aluminium content AlGaN, due to the high potential barrier at the metal-semiconductor interface. The team found that the resistivity of the contact falls at higher temperatures, thanks to an easier passage for the thermally excited electrons through the metal/AlN interface, attributed to tunnelling through an effectively thinner potential barrier and/or thermionic emission.

Measurements of output characteristics determined normally-on operation and effective modulation of the drain current by the gate-source voltage. Drain current peaks at 56 µA mm^{-1}, a value six times higher than that reported for AlN-on-sapphire MESFETs. Fu and colleagues believe that this improvement stems from the lower sheet resistance in the homoepitaxial AlN layer.

Off-state breakdown of the team's devices increases from 442 V to 2010 V as the drain-to-gate-spacing increases from 2 µm to 15 µm.

Fu says that his team's transitors are still inferior to state-of-the-art SiC and GaN power devices, in terms of on-resistance and forward-current capabilities. "This is mainly caused by low electron carrier concentration and poor ohmic contacts in AlN devices."

The team is now working on improving the doping efficiency and the ohmic contacts of its AlN MESFETs, to reduce on-resistance and increase on-state current. "And we are also developing AlN-based MOSFETs to realise more robust gate control," added Fu.

REFERENCE
➤ B. Da *et al.* Appl. Phys. Express **17** 104002 (2024)

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