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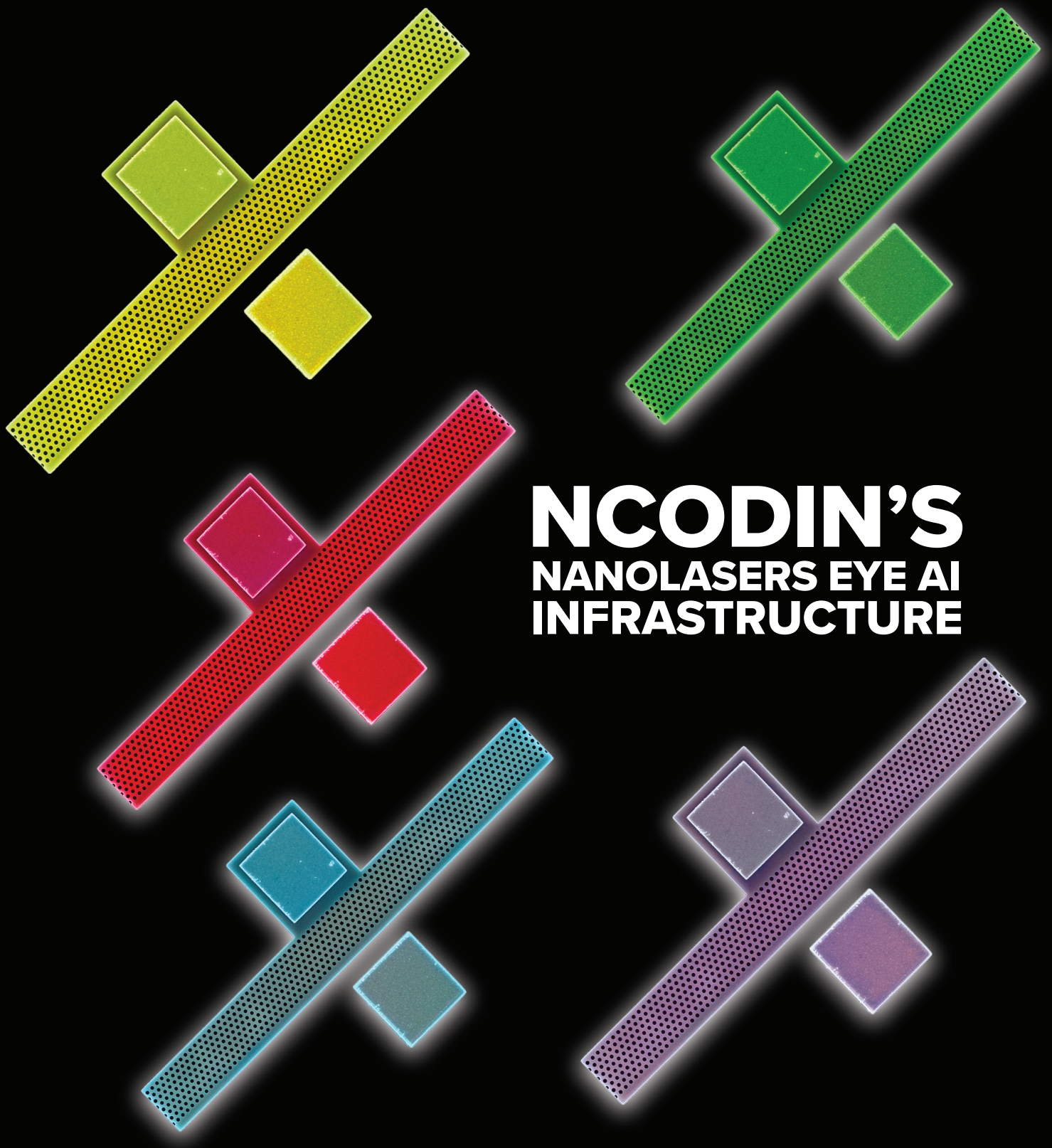

NCODIN'S NANOLASERS EYE AI INFRASTRUCTURE

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

Optoelectronic opportunities in an AI-driven world

GIVEN that Nvidia has a market capitalisation of $4 trillion, you might find it surprising to hear that the data centre market is only worth around half a billion dollars a year. But even so, that's still a substantial market to target by any company promoting a revolutionary technology to improve the performance of tomorrow's data centres, needed to support the growth of AI.

Within our industry, many companies see an opportunity here. They include makers of wide bandgap power devices that are championing the capability of their products to improve electrical efficiency while handling incredibly high power densities. And there are also the producers of optoelectronics, marketing lasers for data transfer.

Over short distances, copper is viewed as the ultimate solution for data transfer, thanks to its resiliency, robustness, and capability to facilitate high bandwidths. But once it's employed to transmit data over a few centimetres or more, losses rise and bandwidths fall – and optical-based links are more attractive.

There are plenty of optical-link technologies vying for success. They include a couple of options promoted by French researchers that are outlined in this issue.

One of these approaches, which is being pursued by CEA-Leti – and shares similarities with that of US company Avicena – is to use vast arrays of microLEDs. These tiny emitters are coupled to fibre bundles to transfer data between chips, which could be on the same board, on different boards, or even on different racks or servers.

Strengths of this approach include an opportunity for redundancy and the promise of an energy efficiency of only 0.5 picojoules-per-bit. While it's ten times this figure today, lower values will be realised during a three-year project that will draw on expertise from the lighting, semiconductor and fibre industries (for more details, see p. 16).

An even lower figure for this key metric of just 0.1 picojoules-per-bit has been realised by the French start-up Ncodin, which has just announced that it has secured funding totalling €16 million. Its core technology is InP-based nanolasers, which are attached to silicon-based waveguides, another approach that allows for redundancy (for more details, see p. 14).

Today Ncodin is working with a partner on the industrialisation of its technology. When success follows, a foundry will produce Ncodin's wafers, which will be marketed to some of the biggest names in the tech industry, such as Nvidia, Qualcomm, AMD and Intel. The expectation is that these giants will employ a third party to test, assemble and package systems that combine Ncodin's wafers with a variety of chips, such as those for memory and processing.

It could be a number of years before datacom infrastructure benefits from Ncodin's nanolasers or microLED technology promoted by CEA Leti. But AI is not going away – surely it's only going to get more pervasive – so there's a lot to be said for pursuing this promising opportunity.

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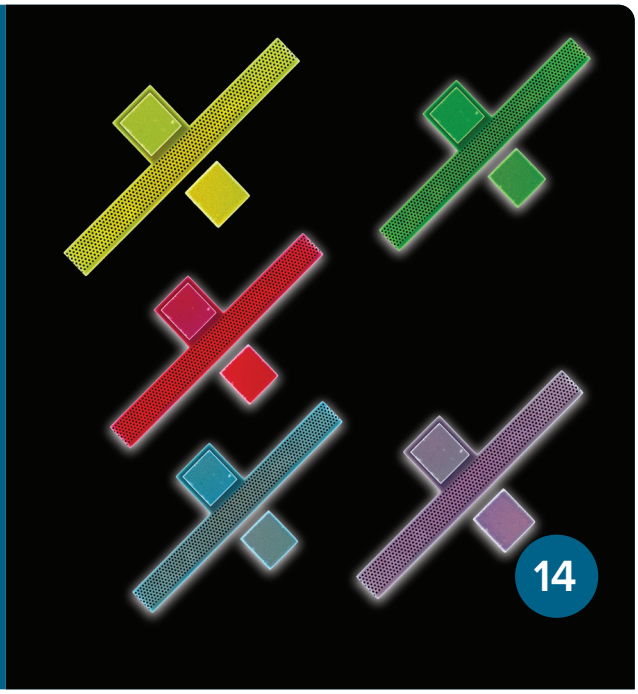
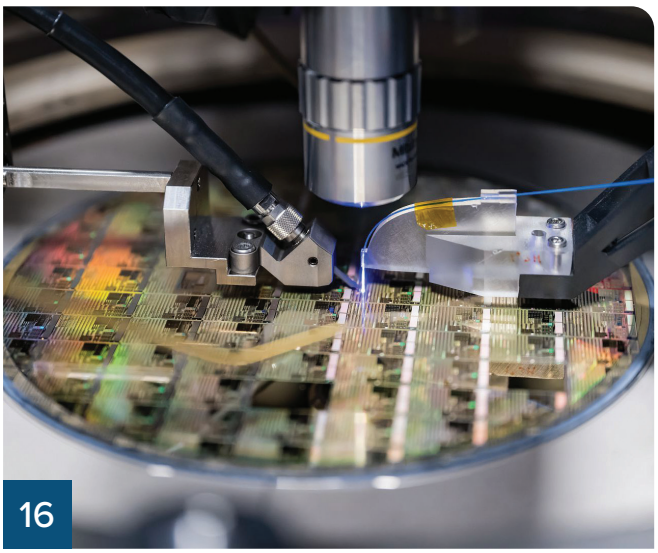
COVER STORY

Ncodin's nanolasers eye AI infrastructure

Delivering a revolutionary energy-per-bit, the French start-up's nanolasers are a compelling source for on-chip communication in tomorrow's data centres





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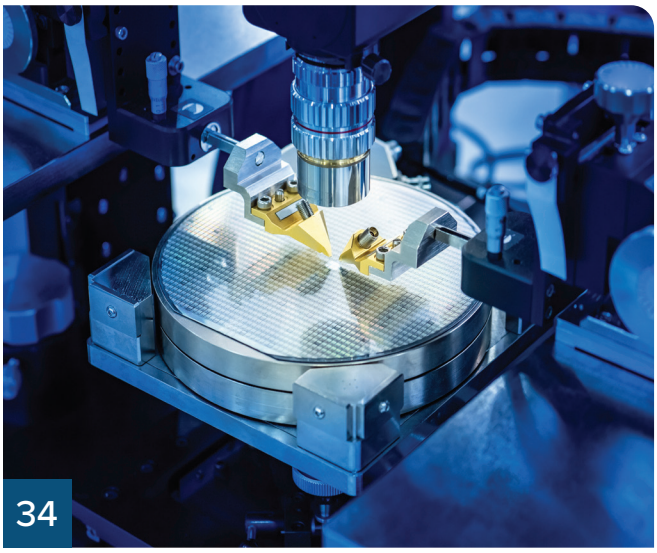

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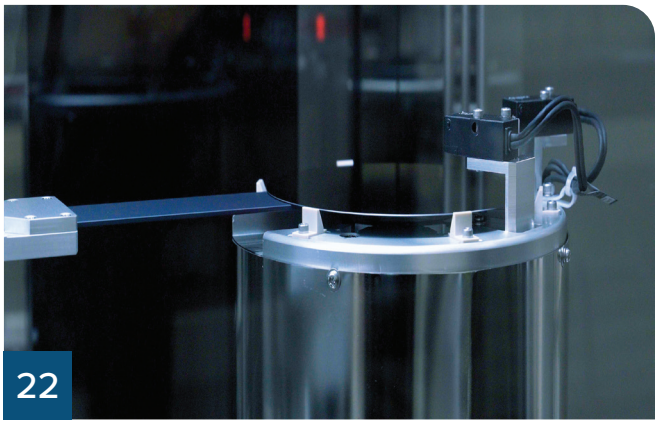

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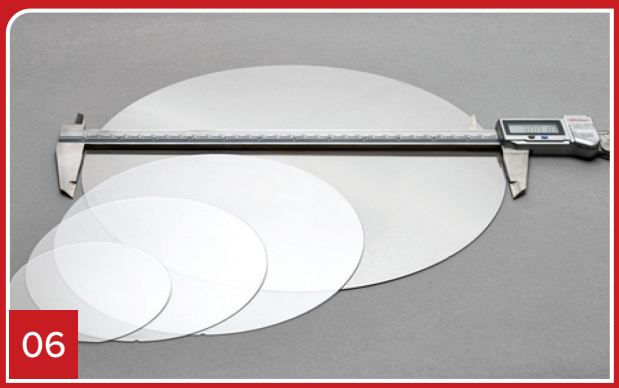
NEWS



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Wolfspeed makes 300 mm SiC breakthrough

300 mm technology, enabling scalable platforms for AI, AR/VR, and advanced power devices

WOLFSPEED has announced a significant industry milestone with the successful demonstration of a single-crystal 300 mm SiC wafer.

This represents a major step forward for next-generation computing platforms, immersive AR/VR systems, and high-efficiency, advanced power devices, according to the company.

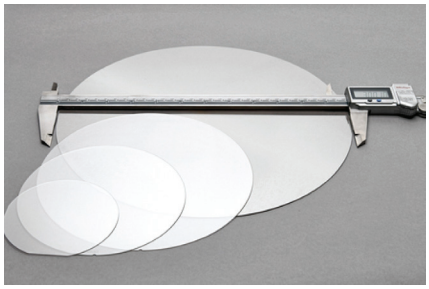
“Producing a 300 mm single crystal SiC wafer is a significant technical achievement and the result of years of focused innovation in crystal growth, boule growth, and wafer processing,” said Wolfspeed CTO Elif Balkas.

“It positions Wolfspeed to support the industry’s most transformative technologies, especially critical elements of the AI ecosystem, immersive virtual and virtual-reality systems, and other high-voltage device applications.”

Wolfspeed says its 300 mm platform will unify high-volume SiC manufacturing for power electronics with advanced capabilities in semi-insulating substrates used in optical and RF systems. This convergence will support a new class of wafer-scale integration across optical, photonic, thermal, and power domains.

As AI workloads push data centers to their power limits, the demand for improved power density, thermal performance, and energy efficiency will continue to accelerate. Wolfspeed says its 300 mm SiC will enable integration of high-voltage power delivery systems, advanced thermal solutions, and photonic interconnects at wafer scale, extending system performance beyond traditional transistor scaling.

Next-generation AR/VR systems require compact, lightweight configurations that integrate high-brightness displays with expansive fields of view and effective



thermal management. SiC’s material properties – including mechanical strength, thermal conductivity, and optical refractive control – suits it to multifunctional optical architectures.

Beyond AI infrastructure and AR/VR, moving SiC to a 300 mm platform could unlock a broader range of advanced power devices to support applications such as high-voltage energy transmission at the grid level and next-generation industrial systems that enable smaller, high-performance components that generate less heat.

Onsemi to develop next-gen GaN power with GlobalFoundries

ONSEMI has signed a collaboration agreement with GlobalFoundries to develop and manufacture advanced GaN power products using GF’s latest 200 mm eMode GaN-on-silicon process, starting with 650 V. This collaboration will speed up Onsemi’s roadmap for high-performance GaN devices and integrated power stages, expanding its portfolio with high-voltage products to meet the growing power demands of AI data centres, electric vehicles, renewable energy, industrial systems, and aerospace, defence and security.

“This collaboration brings together Onsemi’s system and product expertise with GlobalFoundries’ advanced GaN process to deliver new 650 V power devices for high-growth markets. Paired with our silicon drivers and controllers, these GaN products will enable customers to innovate and build smaller, more-efficient power systems for AI data centres, EVs, space applications, and beyond. We are on track to begin providing samples to customers in the first half of 2026, and scale rapidly to volume production,” said Dinesh Ramanathan, SVP of corporate strategy, Onsemi.

“By combining our 200 mm GaN-on-silicon platform and US-based manufacturing with Onsemi’s deep system and product expertise, we’re accelerating high-efficiency solutions and building resilient supply chains for data centres, automotive, industrial, aerospace and defence, and other critical markets. With Onsemi as a key partner, we will continue to advance GaN semiconductors that meet the evolving demands of AI, electrification, and sustainable energy,” says Mike Hogan, chief business officer, GlobalFoundries.

Onsemi will pair its silicon drivers, controllers, and thermally enhanced packages with GF’s 650 V GaN technology platform to deliver GaN devices with higher power density and efficiency. These include power supplies and DC-DC converters for AI data centres, onboard chargers and DC-DC converters for electric vehicles, solar microinverters and energy storage systems, motor drives and DC-DC converters, for industrial and aerospace, defence, and security applications. This effort means Onsemi’s power semiconductor portfolio now includes the full spectrum of GaN technologies – from low-, medium- and high-voltage lateral GaN to ultra high-voltage vertical GaN.

Polar Light unveils the first nanoLEDs

Swedish company says InGaN LEDs measuring 500 nm and smaller pave the way to monolithic RGB displays

POLAR LIGHT TECHNOLOGIES AB, a Swedish microLED company, has unveiled a breakthrough at SPIE Photonics West 2026, with the first series of nano-scale LEDs.

The company says it's achievement illustrates the extraordinary flexibility of its patented pyramidal architecture, developed without requiring the traditional etching process.

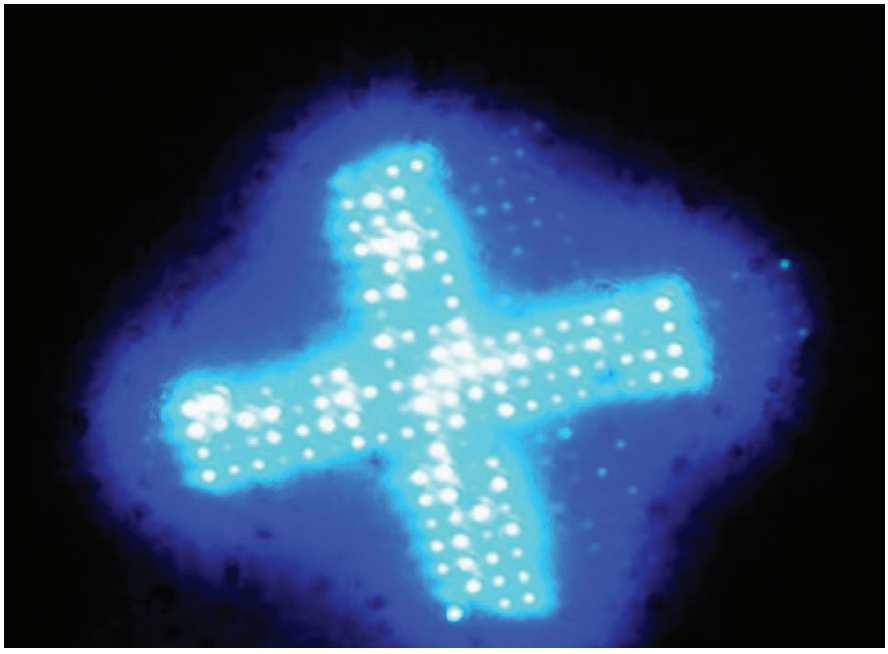
Over the last several months, Polar Light has produced a series of electrically excited InGaN nanoLEDs, measuring 500 nm and smaller, which are built using the same monolithic architecture as Polar Light's existing microLED platform.

This new process makes it possible to scale the technology to significantly smaller dimensions without compromising performance or efficiency, according to the company.

"Reaching nanoLED scale without sacrificing LED performance or production capability is a major milestone for the industry," said Oskar Fajerson, CEO, Polar Light Technologies. "NanoLEDs, in combination with our roadmap toward monolithic RGB, will enable the next generation of ultra-small, monolithic full-colour displays."

MicroLED is widely regarded as the next display technology, due to its unparalleled brightness and low power consumption, making it possible to create whole new categories of display types for a wide variety of novel use cases.

In spring 2025, Polar Light demonstrated its first public prototype at Display Week. In January 2026, Polar Light announced a new €5 million+ funding round that will enable the company to bring its first products to market in late 2026.



Mitsubishi samples new SiC-MOSFET bare dies

MITSUBISHI ELECTRIC has announced that it will shortly start shipping samples of four new trench SiC-MOSFET bare dies designed for use in power electronics equipment, such as electric vehicle (EV) traction inverters, onboard chargers, and power supply systems for renewable energy sources, including solar power.

These new power semiconductor bare dies will contribute to efforts to embed advanced bare dies in various power electronics equipment to lower power consumption while maintaining performance, according to the company.

Mitsubishi Electric exhibited the new trench SiC-MOSFET bare dies at the 40th Nepcon Japan R&D and Manufacturing show in Tokyo from January 21 to 23, as well as exhibitions in North America, Europe, China, India and elsewhere.

The four new trench SiC-MOSFET bare dies are similar to the company's existing trench SiC-MOSFET bare dies, but use a proprietary trench SiC-MOSFET structure to reduce power loss by approximately 50 percent compared to planar SiC-MOSFETs.

Furthermore, manufacturing processes including Mitsubishi Electric's proprietary gate oxide film manufacturing method suppress variations in power loss and on-resistance to ensure stable quality over a long period of use.

Allos and Ennostar forge microLED partnership

Collaboration to establish silicon fab-compatible supply chain for microLED products

ALLOS SEMICONDUCTORS of Germany and Ennostar of Taiwan have announced a partnership to bring 200 mm GaN-on-silicon LED epiwafers for microLED applications into volume production. This collaboration represents a key milestone in establishing a silicon fab-compatible supply chain for microLED products.

Through this partnership, Allos will be able to deliver its GaN-on-silicon epiwafers at the volumes required by its customers, supporting their transition into microLED volume production. Ennostar takes on the role of Allos' manufacturing partner for 200 mm GaN-on-silicon LED epiwafers.

Ennostar has one of the world's largest LED manufacturing infrastructures and expertise in high-end LED technologies, including microLEDs. In addition to manufacturing, Ennostar will also contribute its advanced LED-related technologies to further enhance the product performance.

"With Ennostar we work with the best possible partner to provide our customers with a high quality and scalable supply of epiwafers. Together we can offer the industry's best combination of highest LED efficiency and superior on-wafer and wafer-to-wafer yields for microLED chip manufacturing," said Burkhard Slischka, co-founder and CEO of Allos.

"This partnership delivers competitive GaN-on-silicon microLED solutions and provides a scalable production pathway compatible with standard silicon foundry processes," said Terry Tang, president of Ennostar Corporation. "By partnering with Allos, we can now address the 200 mm GaN-on-silicon LED epiwafer segment alongside our existing market-leading microLED solutions, offering a uniquely

comprehensive value proposition to the rapidly evolving microLED industry."

Designed for compatibility with standard silicon fabs, Allos' epiwafers are available in a thickness of 725 μm and conform to silicon industry cleanliness and contamination standards.

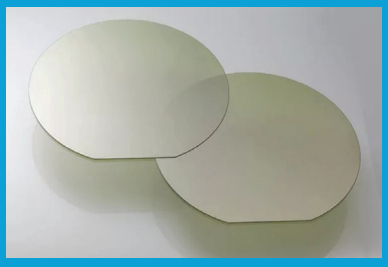
"We share our customers' vision that using standard silicon fabs for microLED manufacturing will unlock the yield and cost efficiencies needed to make mass production of microLEDs economically viable," explained Slischka. He added: "Through our partnership with Ennostar, we can now quickly scale up epiwafer production with increasing demand for microLED products."

The partnership also paves the way for 300 mm GaN-on-silicon LED epiwafers, enabling efficient integration with 300 mm logic wafers – essential, for example, to enable ultra-fast and energy-efficient optical interconnects between AI processors and memory chips using microLED light sources. Allos has already demonstrated 300 mm capability since 2020 and continues to refine the technology with lead customers.

Coherent 300 mm SiC platform addresses AI needs

COHERENT has announced that its next-generation 300 mm SiC platform will address the increasing higher power density, faster switching, and thermal efficiency demands in AI data centre infrastructure.

"AI is transforming the thermal-management landscape in data centres, and SiC is emerging as one of the foundational materials enabling this scalability," said Gary Ruland, SVP and general manager at Coherent. "Our 300 mm platform, which we plan to ramp in high volumes, delivers new levels of thermal efficiency that translate directly into faster, more power-efficient AI data centres."



The platform's conductive SiC substrates provide low resistivity, low defect density, and high homogeneity, enabling low-dissipation, high-frequency, and good thermal stability.

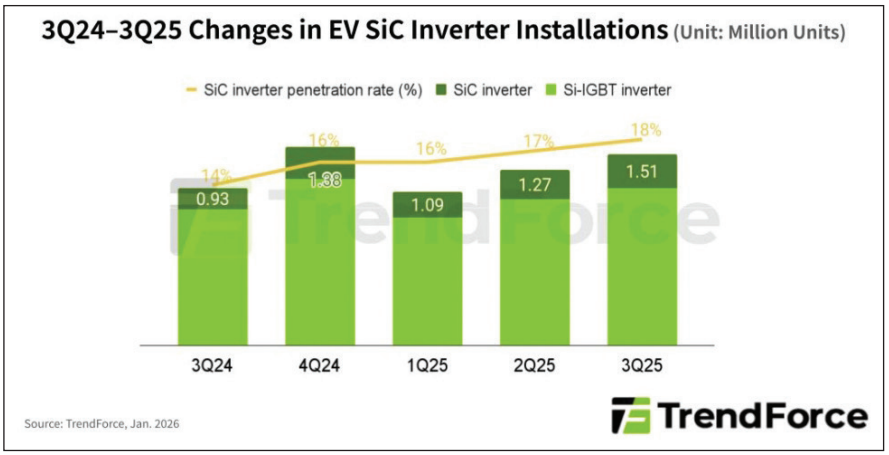
In AI and data infrastructure, these properties boost energy efficiency and thermal performance in next-generation data centre systems.

In addition, the company says the technology brings benefits for AR/VR devices, enabling thinner and more efficient waveguides for AR smart glasses and VR headsets, improving reliability in compact immersive display modules.

Global EV SiC inverter installations hit record high

Traction inverter installations for EVs reached 8.35 million units in 3Q25, says TrendForce

TRENDFORCE'S latest investigations indicate that total global traction inverter installations for EVs reached 8.35 million units in 3Q25, representing a 22 percent increase YoY, driven by ongoing growth in the new energy vehicles market. Battery EVs (BEVs) and plug-in hybrid EVs (PHEVs) were the main contributors to this expansion, with installation increases of 36 percent and 13.6 percent, respectively.



Automakers are progressively enhancing the integration of chassis electric drive systems to achieve goals for smarter and more efficient EVs. This aims to reduce wiring and hardware costs while bolstering communication efficiency and increasing driving range.

In 3Q25, over 70 percent of inverter installations were part of '3-in-1' or greater configurations, including components like reducers and motors. The adoption of '4-in-1' or higher integrated systems increased from 16 percent in the same period of 2024 to 23 percent.

TrendForce highlights that SiC power semiconductors, due to their compact size and higher voltage capacity, are now crucial for advanced electric-drive systems. In 3Q25, worldwide SiC inverter installations reached a record high, surpassing 1.5 million units. The adoption rate in EVs rose from 14 percent in the same period of 2024 to 18 percent, and when focusing solely on new energy vehicles, it reached 22 percent.

A detailed analysis of vehicle models fitted with SiC inverters reveals that 84 percent of these installations are in BEVs, with the remainder in PHEVs and range-extended EVs. China remains the leading market, accounting for approximately 75 percent of all SiC inverter installations, whereas demand in Europe and the US is declining. Against a backdrop of geopolitically driven global dynamics, this structural concentration poses a risk that is difficult for IDM suppliers to mitigate or relocate.

While inverter installation volumes keep rising with the overall vehicle market, the total market value in 3Q25 dropped by 10 percent YoY. This suggests that despite market growth, automakers are exerting greater pricing pressure on the supply chain.

MicroLED reaches a make-or-break phase, says Yole

MicroLED on TFT enters a decisive phase in 2025, with the first low-volume commercial products ramping at AUO

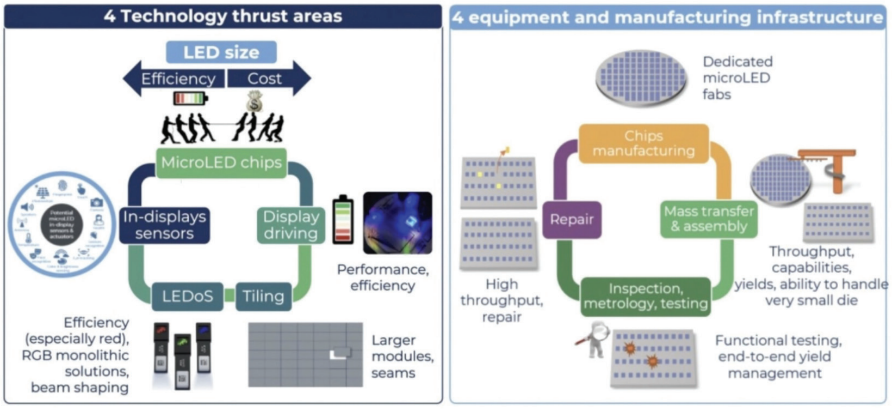
THE microLED industry is transitioning from hype to reality according to Yole's latest two reports: *MicroLED Markets, Applications, and Competitive Landscape 2025* and *MicroLED Technologies, Equipment, and Manufacturing 2025*.

After years of development, the first commercial displays, Garmin's smartwatch and Sony-Honda Afeela's automotive exterior display, entered low-volume production in 2025, manufactured on AUO's G4.5 line. Yole says this moment represents a critical test: the industry must prove that yields, manufacturability, and costs can converge toward a viable commercial path beyond niche B2B and LED-on-silicon applications.

Raphaël Mermet-Lyaudoz, technology and market analyst in photonics and display at Yole Group, commented: "MicroLED has progressed enough to exist without depending on a single flagship product. The momentum returned in 2025, supported by a clearer understanding of strengths, limitations, and realistic timelines."

Yet, the challenges remain significant. MicroLEDs must match OLED's cost while delivering differentiating performance, a demanding requirement that intensifies pressure on die efficiency at small pixel sizes, mass-transfer yields and throughput, repair strategies, and TFT-backplane limitations. Although investments in fabs and pilot lines continue, decision-makers remain cautious as processes and tools are still maturing.

The industry also faces a structural bottleneck: a lack of process standardisation. Today, most microLED display makers pursue unique architectures that require customised



equipment that is costly and complex. While some equipment suppliers, including Hardram, Coherent, Contrel, and PlayNitride, continue developing new generations of tools, others have stepped back due to uncertain prospects and daunting development challenges.

According to Eric Virey, principal analyst, display at Yole Group: "MicroLED supply chains are becoming clearer, with stronger alignment between chipmakers and panel makers. However, strategic questions remain, particularly around foundry models, assembly distribution, and the maturity of large-stage, high-throughput tools."

After years of development, the first commercial displays, Garmin's smartwatch and Sony-Honda Afeela's automotive exterior display, will enter low-volume production in 2025, manufactured on AUO's G4.5 line

Meanwhile, LED-on-silicon is emerging as the most promising volume driver, fueled by AI-accelerated demand for AR glasses and high-performance microdisplays. China leads the charge with JBD as the only player shipping in volume, while Sitan, Saphlux, Hongshi, Innovision and Raysolve scale new fabs. Outside China, alliances are forming around Porotech, PlayNitride, Micledi, Mojo Vision, Aledia, and others, each pursuing distinct architectures, materials, and manufacturing strategies.

MicroLED is also attracting growing interest for optical interconnects in data centers and high-performance computing, supported by major stakeholders such as TSMC, Intel, Nvidia, and Microsoft. Startups, including Avicena and Hyperlume, have raised significant funding to accelerate development in this emerging field.

The microLED is entering a decisive phase, one defined by cautious investment, advancing supply-chain alignment, and a growing focus on manufacturability over the long term.

CGD appoints new CEO

Appointment of Onsemi's Fabio Necco kickstarts next phase of growth for Cambridge company

CAMBRIDGE GaN DEVICES (CGD) has announced the appointment of Fabio Necco as CEO. The move is designed to drive forward CGD's entry into key markets.

Necco takes over as CEO from CGD co-founder, Giorgia Longobardi, who made the announcement, saying, "I am delighted to welcome Fabio to CGD and hand over the day-to-day leadership of the company while I channel my energy into my passion for bringing advanced, sustainable and energy-efficient power electronics solutions to market. Fabio is the right person with the right skill set to take CGD into its next growth phase, and I shall do all I can to support his initiatives as I transition into my new role as CMO at CGD."

Necco comes to CGD from Onsemi, the US-based semiconductor company specialised in delivering industry-leading intelligent power and intelligent sensing solutions, where he was vice president and division general manager with more than 25 years' experience in power electronics, application engineering, vehicle electrification, and data centres, all primary market focus points of CGD.

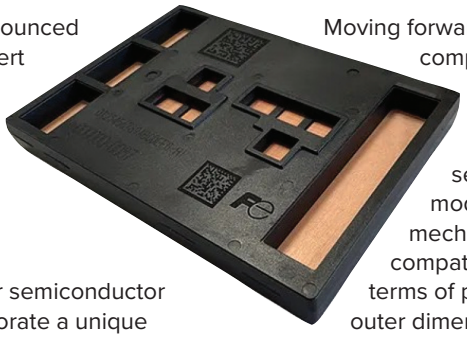
Necco said: "CGD is at an exciting juncture in its history. I have known CGD and Giorgia for years, and have long been impressed with its success under her leadership. I am very excited about CGD's unique technology, and to have been chosen to lead our entire team to the next stages of product development, as well as substantially increasing our presence in key markets."

Unlike many other GaN solutions, CGD's ICeGaN technology uses a monolithic, single-chip approach that integrates all necessary components onto a single die, which substantially improves efficiency and performance.

As for CGD Co-founder, Giorgia Longobardi, in addition to her continuing role as CMO at CGD, she will continue to serve as a Director on CGD's Board and on the Advisory Board of the International Semiconductor Industry Group.

Fuji and Robert Bosch collaborate on SiC modules

Companies to work on EV SiC power modules with mechanical compatibility



FUJI ELECTRIC has announced an agreement with Robert Bosch GmbH to collaborate on SiC power semiconductor modules for electric vehicles that feature package compatibility.

Fuji Electric's SiC power semiconductor modules for EVs incorporate a unique packaging technology, designed to allow high power density in inverters. By modifying the size and number of mounted chips, the modules can accommodate a wide range of power requirements and circuit configurations from automotive manufacturer customers.

Moving forward, both companies intend to develop SiC power semiconductor modules with mechanical compatibility in terms of package outer dimensions and terminal positions. This will enable either module to be integrated into an inverter system without additional mechanical modifications, minimising the adjustment effort required for customers when using both module options in their systems.

This collaboration aims to shorten design periods and contribute to diversifying procurement sources.

As a result, customers will be able to use SiC power semiconductor modules from both companies without altering their inverter system specifications, leading to reduced design time and diversified procurement.

Both also companies plan to jointly develop user application technologies related to cooler design and various terminal connections when integrating SiC power semiconductor modules into inverter systems, and plan to provide technical support to customers.

Atalco to establish large scale gallium plant

ATALCO, the only operating alumina refinery in the United States, has announced a partnership with the US Government to sustain and increase domestic alumina production and establish the country's first and only large scale primary gallium production circuit in Gramercy, Louisiana.

The company expects to produce over one million metric tonnes of alumina per year and up to 50 tonnes of gallium per year in Gramercy, Louisiana.

Both alumina and gallium are essential minerals for production of aerospace and defence systems, catalysts, semiconductors, and next-generation energy technology.

The partnership also involves Concord Resources Holdings in conjunction with Concord's majority shareholder, a fund managed by Pinnacle Asset Management, a leading commodities investment firm.

Atalco said: "Aligning this essential public sector support with private sector investment will secure onshore supply of alumina and gallium, which are contested commodity market segments currently dominated by China. This deal shows how quickly and decisively America can act to ensure long-term national security and economic resilience."

America's Department of War's Industrial Base Analysis and Sustainment programme has invested $150 million of preferred equity in Atalco. Additional funding from the US Government is expected to close within 30 days of the equity closing. Pinnacle's fund, as the majority shareholder in Atalco via Concord, has invested more than $300 million in private capital.

"For the past decade, our investment philosophy has centered on bolstering the US supply chain for critical minerals and other commodities," said Jason Kellman, chief investment officer,

Pinnacle Asset Management. "This strategic partnership plays an important role in strengthening our country's critical minerals supply."

"In addition to the core expansion of the Atalco facility, this investment unlocks significant growth potential, including increasing the site's mineral processing and power generation capabilities, all of which contributes to the long-term security of America's materials supply chain." said Scott Kellman, managing partner, Pinnacle Asset Management.

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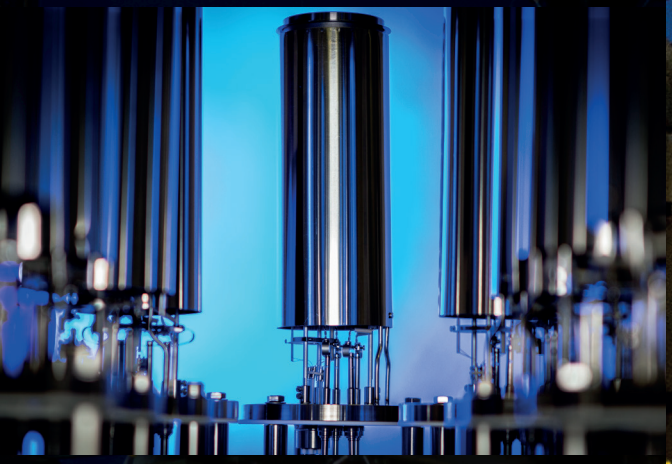

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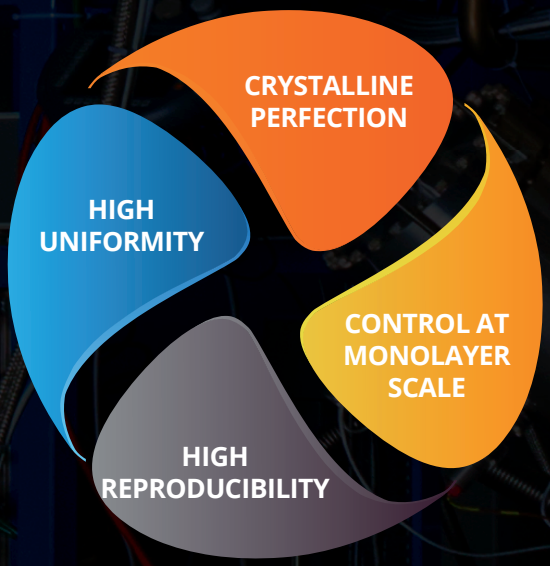

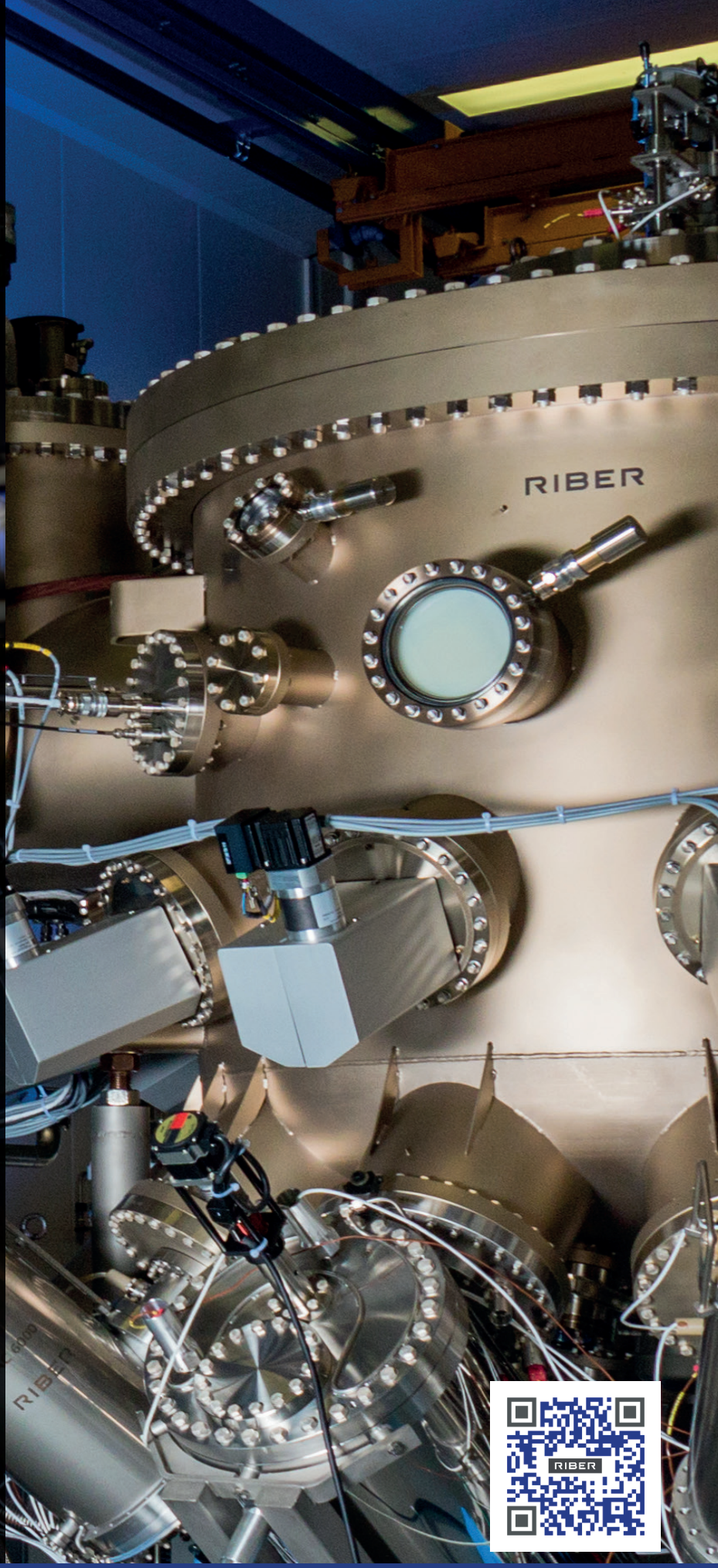

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Ncodin's nanolasers eye AI infrastructure

Delivering a revolutionary energy-per-bit, the French start-up's nanolasers are a compelling source for on-chip communication in tomorrow's data centres

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

SUPPORTING increasing adoption of AI is the building of more and more data centres. This roll-out of essential power-hungry infrastructure already accounts for hundreds of billions of dollars per annum, and total costs are forecast to exceed a trillion dollars a year by the middle of the next decade.

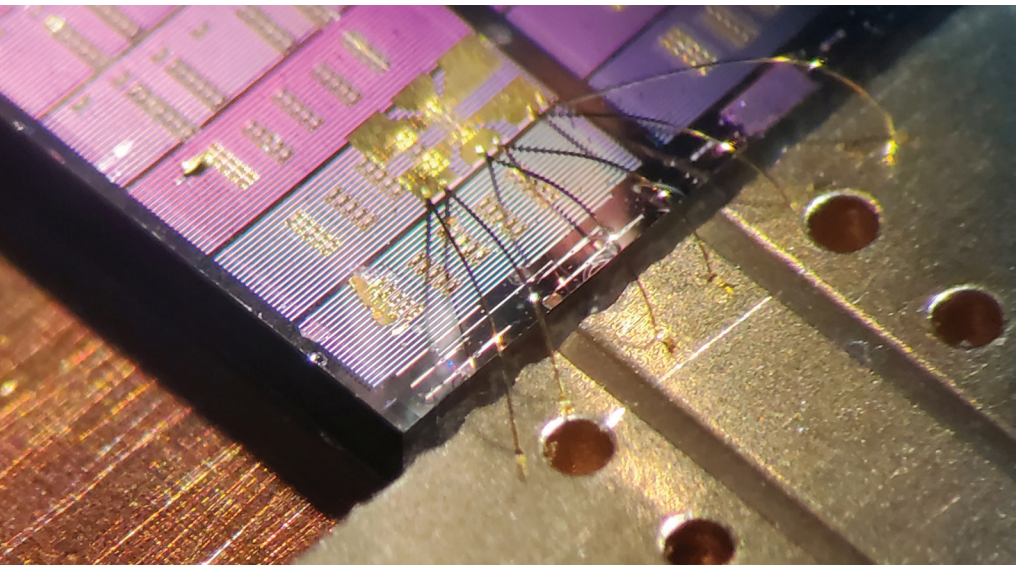
These eye-watering sums offer a fantastic opportunity for companies with technologies that can enhance critical hardware, especially if these products deliver breakthroughs in performance and efficiency.

One of the biggest issues in today's datacentres surrounds the transfer of data between chips. Although widely deployed for decades, copper is a bottleneck to higher speeds. And that's not its only downside, with other significant weaknesses including a limited reach and losses that lead to a significant contribution to overall energy consumption.

Offering attractive alternatives that address all these issues are various forms of optical links. There are a number of options for the light source – including edge-emitting lasers, VCSELs and microLEDs – and photons can be routed through optical fibres or waveguides in wafers.

Amongst these competing solutions, French start-up Ncodin, which has just raised €16 million, believes it has the winning formulation: miniature lasers that launch their emission into waveguides in silicon-based wafers.

Optical interposers formed by this approach, featuring incredibly small lasers and photodetectors – both are created by bonding InP epiwafers to silicon substrates and subsequent photolithography – are claimed to deliver unrivalled efficiencies. Data transfer is incredibly fugal, at less than 0.1 pJ/bit, and integration can exceed 10,000 mm^{-2}, enabling breakthroughs in performance on two fronts – what is possible per Watt, and per dollar.



➤ Ncodin's silicon photonic chip integrating nanolasers, the core technology showing record energy efficiency below 0.1pJ/bit. The wires provide a connection between the controller (an FPGA) and the nanolasers.

A pioneering PhD

The origins of Ncodin can be traced back to the labs at the Centre for Nanosciences and Nanotechnologies, located in the southern suburbs of Paris, where co-founding CEO, Francesco Manegatti, developed these nanolasers during his PhD days.

Enthused by the emergence of a start-up ecosystem – in 2017, colleagues from this lab founded the quantum computing spin-off Quandela – Manegatti shifted his post-graduation plans from joining a big company to trying to commercialise the nanolaser technology he'd developed, a vision shared by his supervisor, now chief scientific officer and co-founder Fabrice Raineri.

Efforts in this direction began in late 2019 and continued during the pandemic, when these entrepreneurial partners started to try and secure initial funding and develop a first roadmap towards commercialisation.

The next steps involved: working with the support of CNRS on an R&D project; establishing a business plan; and bringing in third co-founder, Bruno Garbin, who switched roles from a postdoc in the laboratory to Ncodin's CTO.

Founding of the start-up followed in 2023, with Ncodin raising €3.5 million in a pre-seed funding round that closed in March 2024. Since then, headcount has mushroomed from four to 30 employees, and the company has established its own headquarters.

"We still exploit the facilities of CNRS, because this lab has the largest

academic clean room of France. It's a 3,000-squared-metre clean room, where they have a lot of collaboration with private entities," explained Manegatti.

Ncodin uses this facility to develop its chip technology, and make proof-of concept devices that are shared with partners.

"In parallel, we are working on the industrialisation of our technology, to reproduce it in a CMOS pilot line on 300 millimetre [wafers]."

The start-up has always focused on optical interconnects. Neuromorphic architectures initially garnered consideration, but the primary goal is to complement copper and aid the scaling of infrastructure and process architecture.

"For extremely short reach, copper is best," argues Manegatti. "It's super resilient, it's super robust, you can deliver a high bandwidth."

But for connections beyond a few centimetres, links should switch to the optical domain, where Ncodin's solution addresses the challenge of transferring tens of terabits per second of bandwidth while consuming just a fraction of a picojoule per bit.

This is an attractive option for AI workloads, which are fulfilled through continuous communication between the compute element, which could be a GPU or an ASIC, and the high-bandwidth memory. For these tasks, nano-lasers promise to play a role in fulfilling demands for extremely fast retrieval of data, as well as the writing of data in the memory.

Numerous nano-lasers

To produce its devices, the French start-up draws on external expertise for the growth of its epiwafers. Multiple coupons are crafted in these epiwafers, prior to hybrid bonding to silicon-based wafers. Subsequent lithography and patterning define the dimensions of lasers and photodetectors, both operating at telecom wavelengths. The emission from the lasers, which have a footprint that is 500 times smaller than their conventional cousins, evanescently couples into the waveguides in the underlying silicon wafers.

➤ Since it's founding in 2023, headcount at Ncodin has increased to 30 employees.

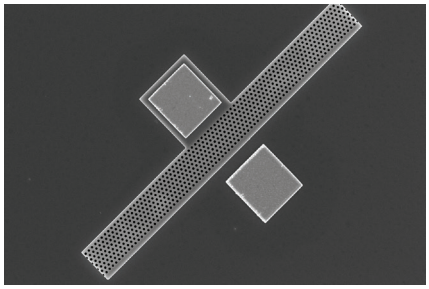
Nanolasers produced by this process have an output of up to a few hundred microwatts – that's more than enough for the intended task – and an efficiency of around 15 percent. These low emitting powers prevent self-heating issues for these miniature sources, which are capable of delivering robust operation at temperatures approaching 100°C.

Thanks to the incredibly high density that can be realised with Ncodin's technology, the intention is to connect every input and output pin of every ASIC and every high-bandwidth memory to a nanolaser.

"Our goal is, of course, to add redundancy, to extend even further the lifetime and essentially the reliability of our chip," adds Manegatti.

The nanolasers are directly modulated, as it's not critical to have a high data rate per channel, thanks to the use of so many channels.

According to modelling by Ncodin, it's possible to realise data rates of up to 64 Gbit s^{-1}. However, the nanolasers currently operate at 16 Gbit s^{-1}.



➤ Ncodin's core technology is the production of telecom lasers with a footprint that is 500 times smaller than their conventional cousins.

"This is more than enough," argues Manegatti. "High-bandwidth memory, for example, is driven at 8 gigabits-per-second today."

Before Ncodin's optical interposers are deployed in data centres, they need to have proven reliability. Efforts in this direction are on-going, according to Manegatti, who remarks: "We are industrialising the solution, so the most important KPIs will be extracted during this project." Note, though, that his team have already demonstrated lifetimes that are well beyond a few thousand hours.

The business plan

To produce its technology in volume, Ncodin will partner with a dedicated foundry to manufacture wafers packed with optical interposers.

"We'll sell the wafers to our customers, so chipmakers like Nvidia, Qualcomm, AMD, Intel, *et cetera*," says Manegatti. These household names will employ partners to test, assemble and package entire systems that combine Ncodin's wafers with a variety of chips, such as those for memory and processing.

Manegatti says that the main goal for now is to finish the industrialisation project, undertaken with a partner, and start qualification of its product.

"We're going to open an office in Silicon Valley, to be closer to our customers and partners, and to be able to engage in an even deeper relationship with them."

These plans, which make a lot of sense, promise to enable III-Vs to play yet another role in tomorrow's technology infrastructure.

Aiding AI with the microLED

Promising to provide the most efficient links for tomorrow's energy-hungry data centres are links formed from vast arrays of microLEDs, employed alongside optical fibres and photodetectors

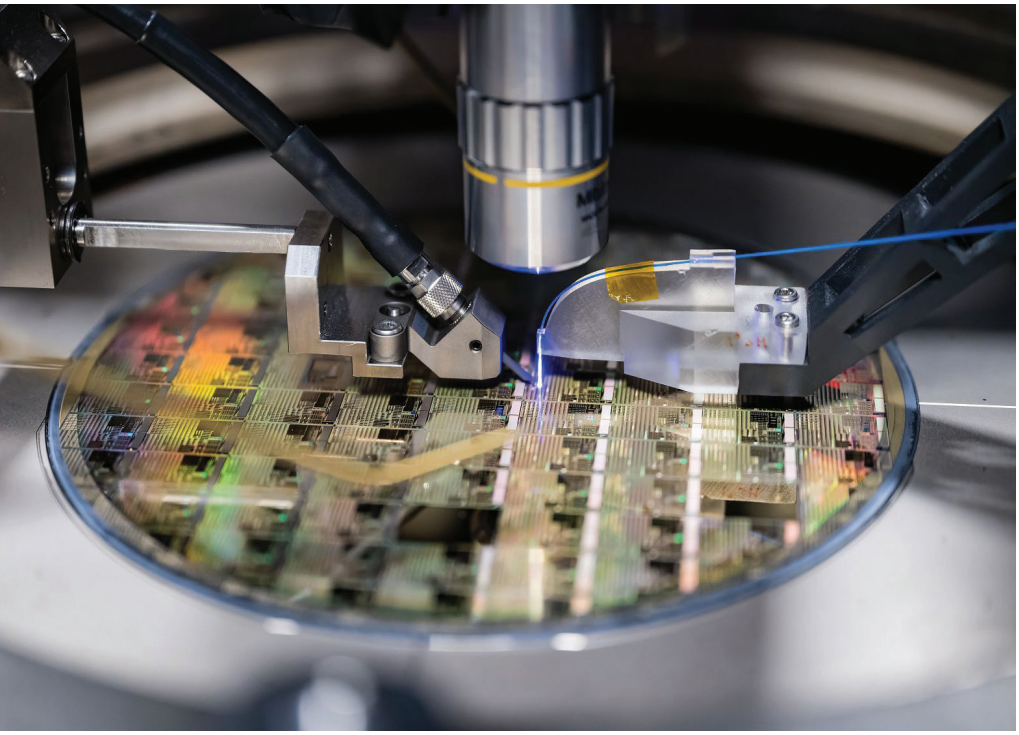
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AROUND the turn of the millennium many bought their first mobile phone, a purchase that helped to swell revenues for our industry on two different fronts. Sales created the first 'killer' application for the LED, coming from backlighting the displays and keypads of these handsets, and it led to rocketing revenue of GaAs HBTs and pHEMTs, with these devices deployed in RF amplifiers and switches.

Since then, there's not been another application that's delivered multi-billion-dollar sales for more than one class of device within the compound semiconductor industry. But that could change, thanks to AI, which is fuelling a hike in the roll-out of data centres.

Many makers of wide bandgap power devices are saying that they are aiming to exploit growth in data centres – efforts are directed at securing contracts for discrete components and modules for electrical infrastructure that combine exceptional efficiencies with the handling of high power densities. But there's also an opportunity within the optoelectronics sector, for sources and detectors that can form short-reach optical links that overcome a data transfer bottleneck while minimising the energy-per-bit.

Focusing on the latter is a three-year project starting this January. Led by French technology research institute CEA-Leti, this effort aims to drive the development of optical links formed by combining arrays of GaN-on-silicon microLEDs with fibres that have a relatively wide core and photodetectors. It is intended that this project will involve all the key players in the supply chain, including manufacturers of microLEDs, optical fibres, photodiodes and interconnects, as well as chipmakers, system integrators, and hyperscalers.



According to Jankus Vygintas, CEA-Leti Partnership Manager and spokesman for this three-year project – it's referred to as the *Multilateral MicroLED Data Link Program* – the proposed optical links could be deployed to transfer data from one chip to another within a board, or from one chip on one board to one chip on another board. Chip-to-chip transfer could even go from server to server or rack to rack, as the technology offers much appeal for links spanning 10 cm to 10 m.

Note that Vygintas is not suggesting the complete elimination of copper in data centres, arguing that this is the best choice for distances of just a few centimetres. But this should be the upper limit, as the longer these wires get, the more energy they consume.

Giving the success VCSELs have had in datacomms, they are another candidate for chip-to-chip links.

"For pluggables and so on, for longer distance links, it's probably the best developed technology" claims Vygintas, who explains that this surface-emitting laser can be viewed as a 'Ferrari' for short links, from both a cost and an efficiency perspective.

Providing a starting point for the project is the significant body of microLED work conducted by CEA-Leti that's led to the generation of around 100 patents. The well-renowned French research institute has been developing microLEDs since at least 2015, and around six years ago its efforts started to involve the modulation of these devices, initially to gauge their potential as sources for LiFi.

More recently, the focus has shifted to coupling the emission from microLEDs into fibres, and evaluating a key metric, the picojoules-per-bit.

"Nowadays, we are at around 5 picojoules-per-bit," reveals Vygintas, who adds that a primary objective of the project is to slash this critical figure to just 0.5 picojoules-per-bit.

"The other target is, of course, data density. In the long term, we aim to reach 10 terabit-per-second per millimetre."

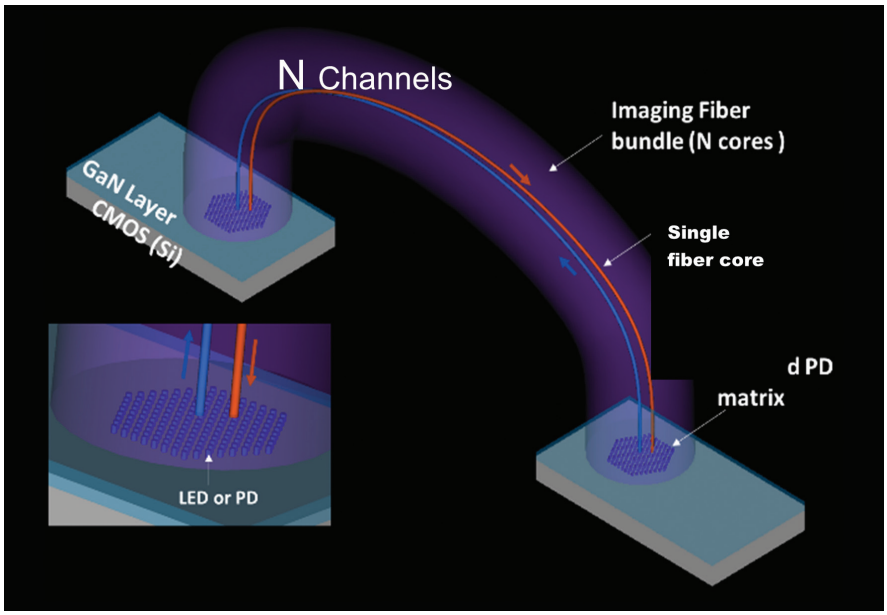
In CEA-Leti's 11,000 m^2 cleanroom researchers have developed a process for producing GaN-on-silicon LEDs on 200 mm substrates. Note, though, that the process can be scaled to 300 mm.

The team can shrink the size of its microLEDs to just a few microns – dimensions that are ideal for augmented reality, but a level of miniaturisation that introduce issues, including quenching at the edges of these emitters. For short-reach data links, Vygintas recommends using microLEDs with a size of around 10 μm, with emission coupled into fibres with a core of around 50 μm.

"We work on emission in the blue, but in principle, emission in green or red would be possible," says Vygintas.

While at first glance shifting emission to longer wavelengths is deleterious, driving a decline in efficiency that stems from an increase in indium content in the quantum wells, this view fails to grasp the bigger picture. That's because many more factors are at play, such as modulation bandwidth, fibre coupling and losses, and the efficiency of the detector – all contribute to the key metrics.

For data links, the emission from arrays of microLEDs is coupled into fibre bundles, a technology already employed for imaging in medical applications.



Credit: Patrick Le Maitre, CEA

➤ Working principle of a microLED-based data link.

"We are testing all type of fibres, including plastic fibres," reveals Vygintas. "Some manufacturers provide glass multi-core fibres."

A key advantage coming from combining arrays of microLEDs with fibre bundles is a built-in redundancy at the system level.

"The VCSEL has to be well aligned, but in our case, we can afford some loss," claims Vygintas. The team at CEA-Leti tackles this task with partners that fabricate alignment and attach tools for the silicon photonics industry. These collaborators can use their technology to attach fibres to microLEDs.

Vygintas believes that an even better approach involves refining the design of the microLED so that it includes a resonant cavity that creates an emission profile tailored to coupling into a fibre. Such a device demands the introduction of Bragg mirrors made from dielectrics.

One of the options for the detector that's positioned at the other end of the fibre is a silicon-based diode, which is a well-established device; and the other contender is a GaN photodetector. While the latter is inferior today, it has a reasonable responsivity, and would simplify device integration. To try and improve performance, the team at CEA-Leti are aiming to optimise the epitaxial process for producing these devices.

Thanks to the fabrication of devices on silicon, drivers for these microLEDs can be added by bonding to the backplane. Over the last four years Vygintas and co-workers have adopted this approach when they've been comparing various modulation schemes. While the more complicated ones may have greater promise, the team has concluded that the best solution is a basic on-off modulation scheme that simplifies amplification and photodetection.

"It should also be more efficient, because higher modulations can consume more energy," adds Vygintas.

He believes that CEA-Leti's status as a research institute ensures that it's in a great position to nurture the formation of an ecosystem for producing microLED-based short-reach optical links. Over the next three years, they will be bringing together those working in the lighting, semiconductor and fibre industries from all around the world. Some of these companies are already on-board – but their names cannot be revealed, due to non-disclosure agreements – and many more are expected to join.

"We occupy very special place in the whole ecosystem to provide prototypes. We are open to discussions with everybody," says Vygintas.

By adopting such a collaborative stance, CEA-Leti is giving the microLED a great opportunity to find its first killer application, and increase compound semiconductor content in the data centres of tomorrow.

Polymatech: Propelling Indian optoelectronics

The launch of powerful UV LEDs for industrial curing helps to strengthen the emerging compound semiconductor industry in India

DECADE after decade, our industry goes from strength to strength. This is evident in growing revenues that are now totalling many tens of billions of dollars per annum, and the expanding reach of our devices – they are now powering EVs, charging mobiles and illuminating our world in numerous ways, to name but a few applications.

As well as increases in sales and applications, our growth is highlighted by the range of locations producing these chips. Back in the twentieth century, makers of compound semiconductor devices were found predominantly in North America, Europe, Japan and South Korea. But in more recent times you can add Taiwan and China to that list, and now India.

Entry of the latter is gathering pace, spurred on by a desire by the Indian government to make in India for India – that's an ambition that goes back well before the introduction of tariffs by Washington. Success is already underway, evident through: SiCSem, building India's first fab for manufacturing SiC chips; Navitas, providing a catalyst for the country to establish a GaN supply chain; and the efforts of Indian-based optoelectronics firm Polymatech Electronics, which has just expanded its portfolio of LED products. Its latest addition is a 'world-class' UV LED for curing applications, promoted at the recent Consumer Electronics Show (CES) in Las Vegas.

This UVA LED, emitting at around 400 nm, is said to deliver an industry-leading photon flux density that ensures sub-one-second curing.

Discussing this product with *Compound Semiconductor*, CEO and Managing Director of Polymatech, Eswara Rao Nandam, says that his company's UV-LED platform can compete globally on three primary metrics: "One is electrical efficiency, second is operating lifetime, and third is optical power density."

For the latter, viewed by Nandam as actually the most important, the CW optical power density for the UVA LED is around 150 W cm^{-2}. As the chip size is typically a few millimetres squared, output is several watts.

Polymatech's UVA LEDs feature a chip-on-board architecture, selected for its superior thermal dissipation that stems from the aluminium substrates. Additional benefits of this particular design are uniform optical emission, an absence of interconnect losses, and a very high packaging density.

External quantum efficiency is 11.5 percent, notably higher than that for its siblings emitting in the UVC – they have values of 2-2.5 percent.

For the LEDs emitting at around 400 nm, lifetime is beyond 50,000 hours, based on defined operating conditions. This figure, defined by the time it takes for output to fall to 70 percent of its initial value, has been determined with the commonly adopted approach within industry that involves accelerated performance tests conducted at an elevated temperature and current.

According to Nandam, commercial opportunities for LEDs emitting in the UVA go well beyond what many

➤ Polymatech's key facility at Oragadam is used for advanced semiconductor packaging, R&D, ingot growth, wafer slicing, 3D printing and rapid prototyping.

imagine. As well as being employed for the curing of printing and packaging, these LEDs can provide a source for UV-cured coatings and finishes of automotive parts. There are also opportunities for very fast curing, found in electronics assembly, semiconductor assembly and 3D printing. Taken together, these applications create a global market for UV curing that's already worth many billions of dollars, and is growing fast. "I will not say [the market is] expanding, I will say it is exploding," enthuses Nandam.

A family business

After graduating with an electrical and electronics degree from the Birla Institute of Technology and Science in Pilani, and gaining a doctorate in Electrical Engineering & Computer Sciences (EECS) from the University of California, Berkley, Nandam held positions in the compound semiconductor sector for several decades. During that time he has worked for various companies, including Nokia.

A key juncture came in 2011, when the tsunami in Fukushima sparked substantial losses for Japanese company Polymatech Electronics, a supplier of keypads for mobiles to the likes of Nokia, Ericsson, Sony and Motorola. Following that colossal and devastating tidal wave, Polymatech struggled for profitability for several years, ending up in arbitration. In 2018, the Nandam family purchased the company, revitalised it, and today its two key leaders are Eswara Rao Nandam and his son.

Under the leadership of this duo, Polymatech is expanding, in terms of its capacity, manufacturing sites, and where it plays within supply chains.

Initially starting with the packaging of chips for the automotive industry, Polymatech has expanded in many directions, drawing on sites it owns all over the world. There's a factory in Grenoble, France, that produces sapphire ingots and wafers; a site in the US that makes semiconductor testing and failure-analysis equipment; and there are advanced packaging facilities in India and Singapore. And recently Polymatech has purchased a company in Estonia that produces printed circuit boards.

This expansion is helping reposition Polymatech from a packaging company to one that makes products. Within the optoelectronics domain, as well as UVA LEDs that have just been announced, there are products emitting in the near infrared that help to diagnose issues beneath the skin, and those in the UVC for water purification

In India, for India

In addition to overseas expansion, Polymatech is investing in its capabilities at home.

The key facility is at Oragadam, near Chennai. Here there's advanced semiconductor packaging, R&D, ingot growth, wafer slicing, 3D printing and rapid prototyping.

"We make everything here, and we give it to other places in Singapore, or in the USA, or in Estonia, *et cetera*," says Nandam, who adds that they are seeking permission from government for more land for this key site.

The two additional sites in India are located in Nava Raipur, which is home to a Polymatech industrial park that has facilities for ingot growth, wafer manufacturing, epitaxy, packaging, and product assembly; and Bannihalli, Krishnagiri, a site currently under construction that will be dedicated to manufacturing products for the Domestic Tariff Area (DTA).

All these efforts are helping to equip India with what Nandam views as "real manufacturing", rather than assembly services for other companies.

"We, Polymatech, are proudly building compound semiconductor expertise and developing skilled-engineer talent, anchoring India's high-value global chains."

This lofty goal is pursued while maintaining efforts overseas, an approach that makes strategic sense.

➤ Polymatech's UVA LED has an output of 150 W cm^{-2}, an external quantum efficiency of 11.5 percent, and a lifetime is beyond 50,000 hours.

"Singapore serves as a global customer interface," says Nandam, describing this facility as a bridge between Indian manufacturing and international markets.

Nandam believes that Polymatech started 2026 strongly, with attendance at CES generating enquiries related to system adoption that could be worth billions of dollars.

Goals for the rest of the year include stabilising the plant in Singapore, expanding the facility in Estonia, scaling the output power of its LEDs and driving their adoption.

And in addition, Nandam has another aim, which promises to leave a legacy: "I wish to establish India as a credible source of advanced semiconductor technology."

CEO and Managing Director of Polymatech, Eswara Rao Nandam, previously worked for Nichia and holds a PhD from the University of California, Berkley.

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Key Themes for 2026

Growing revenues in GaN Power Electronics
Sales of GaN transistors are tipped for tremendous growth throughout this decade and beyond. But what are the optimum strategies for exploiting this opportunity?

microLEDs: How to gain market traction
The potential of the microLED is beyond question. But what's needed to ensure that this miniature marvel starts to generate significant sales?

Revitalising the SiC industry
With profit margins shrinking, makers of SiC devices cannot rest on their laurels. But what are the key innovations to ensure success, in terms of production processes, fab operations and new device architectures?

Advancing surface-emitting optoelectronics
What's needed to increase the spectral range and speed of the VCSEL, so it can target new applications? And how can the performance of PCSELs and UV LEDs improve, to drive their commercial success

Unlocking the potential of ultra-wide bandgap materials
Offering some tremendous characteristics, ultra-wide bandgap materials are poised for success. But which one is going to have the biggest impact? Will it be AlN? Or diamond? Or one of the oxides?

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Clas-SiC: A thriving three-pronged attack

The Scottish SiC specialist is excelling on the three fronts – alongside rising demand for prototyping, the manufacture of SiC devices at low-to-medium volumes is on the up, and the licensing side of the business is booming

RICHARD STEVENSON, EDITOR OF CS MAGAZINE, INTERVIEWS JEN WALLS, CEO OF CLAS-SIC WAFER FAB

RS: *What's your view on the current state of play in the SiC industry?*

JW: It's changed a lot in the last 12 to 18 months. The number of players coming into the market has driven costs down, because capacity has been there. This has opened up new markets.

The cost of the substrate has reduced, bolstered by Chinese government subsidies. There has also been dramatic increases in quality for substrates, epitaxy, device performance and reliability.

Devices are more readily available than they were even a couple of years ago. Voltages are being pushed up in more applications, because device performance has increased. This wouldn't have happened before, because silicon carbide was so expensive.

Price reductions have opened up markets for silicon carbide where it would not have played before, especially at lower voltages. Silicon carbide can now compete in consumer products, where GaN may have been the device of choice. Some of our customers are supplying makers of consumer products, like LG. That's been a huge change.

RS: *A great deal of excitement in SiC has come from the EV market, which is suffering from some softness. Do you think that's a big issue?*

JW: The compound annual growth rate of the EV market hasn't been at the levels suggested by Yole Group and all the other market predictors. However, it's growing. You can see that yourself – you can see more EVs on the road.

Here at Clas-SiC, our customers aren't solely based on the EV market. I think the EV market is an absolute enabler to drive quality and device performance, but it's not all about the EV market.

Silicon carbide is now seen as a major enabler for data centres. The power systems for large data centres needed for the future of AI are going to need silicon carbide.

RS: *When Clas-SiC founded in 2017, I'd argue that the world was a different place. While co-operation still exists, there's a move away from global supply chains towards sovereign capability. And there's also the rise in vertical integration. How do these trends impact the progress of Clas-SiC?*

JW: Sovereign capability and silicon carbide supply chains are great opportunities for Clas-SiC.

We are licencing our technology to SiCSem, to build a fab in India for India. India's sovereign capability is driving that. It's an extremely high-profile project for the Indian government. This will be the first time that they have backed a compound semiconductor fab to this level.

Clas-SiC benefits, not just through the licence fee and the royalty payments, but through the capacity we will get in that fab. Part of the agreement is that we get 15 percent capacity in that high-

➤ Routine facilities pressure checks are vital to ensuring no unplanned downtime to the wafer fab.

volume fab. We access high-volume, lower-cost production, but without the associated CapEx.

It's very similar to the model we've already carried out in China. The Chinese fab is now up and running. It's qualified for diodes and it's going through MOSFET qualification.

For Clas-SiC, that's come at the right time. Here in the UK, manufacturing is expensive, electricity is expensive, and labour rates are high. To allow Clas-SiC to compete, that's very key for us.

For supply chains needing a route outside Asia, right now there are not many options available. That's good for us.

We've also signed an early engagement with a fab to be built in Bulgaria. It'll be good to have a high-volume route in Europe.

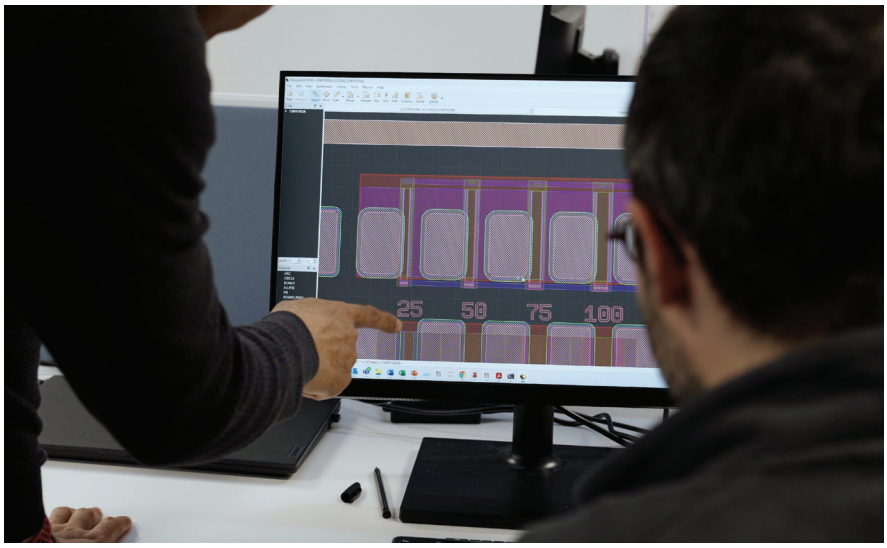
Our customers and others are nervous about US tariffs and where that's going to go. Again, that has put Clas-SiC in a good position.

RS: *Go back a few years and SiC substrate supply struggled to meet demand. Today, what's your view on SiC substrate and epiwafer supply, in terms of quality, quantity and pricing?*

JW: Chinese quality is still the best out there. That's what we are seeing, anyway. On our baseline MOSFET process, yields increased by 7 percent over the last year or so. That's huge.

Now there's overcapacity, so pricing's low. I don't think it's going to drop much more.

In the future, AR goggles will use silicon carbide for lenses. Our suppliers are already telling us that they're predicting 80 percent of their capacity will go for that type of material, rather than for device material. So, capacity could be an issue again in a few years if some companies can't survive without subsidies, and if a lot of capacity is taken up by AR goggles. I think the prediction is that in the next 3-5 years, everyone over the age of 18 will own at least one pair. That's going to take up a huge amount of capacity, so there's no way that the price is going to continue to drop as it has over the last 12 months.



➤ Device scientists reviewing layout prior to mask making- an important step in device manufacture.

RS: *Are you happy to process epiwafers from all vendors? And do you offer recommendations to those seeking an epiwafer supplier?*

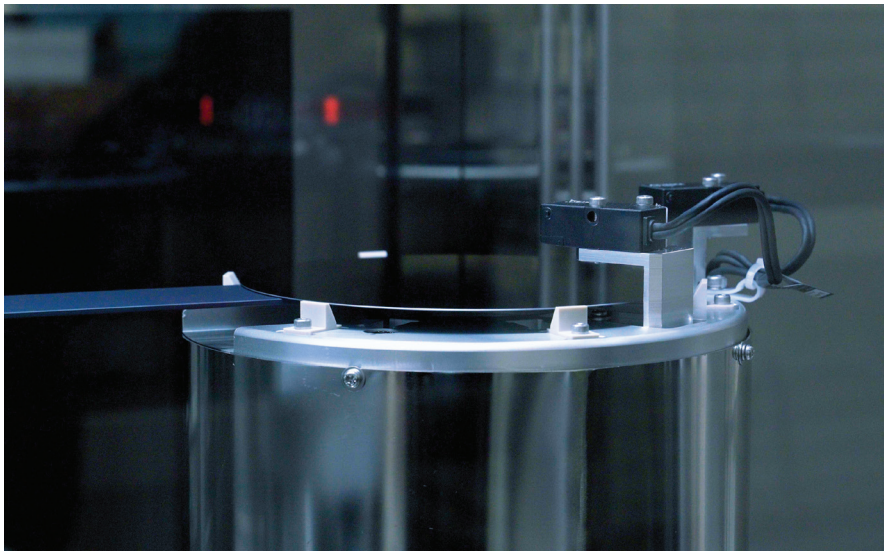
JW: We run a mixed model. Some of our customers supply wafers to us; others, we procure wafers on their behalf.

Normally, in production, we procure wafers on behalf of the customer, but at R&D, prototype-level, customers normally supply wafers to us.
We now have PDKs for engineered substrates, plus *p*-type wafers. Having *p*-type wafers in the fab is a great leap forward, because if we can get a silicon carbide IGBT that would be amazing.

RS: *Around this time last year you secured £10 million of funding from Archean of India. Why did it invest, what's its return, and what's that funding been used for?*

JW: Actually, we received £10 million, and there was also a shareholder-to-shareholder arrangement, because Carl Johnson gave up equity in the company.

As well as being a sound business decision, it was a strategic decision for them, because they are the financial backers behind SiCSem Private Limited, who are building the fab in India. As part of that investment they get a seat on our board.



➤ A rapid-thermal-anneal tool loading station. Devices visit these tools at least twice during fabrication.

➤ Clas-SiC CEO Jen Walls at the SiCSEM fab groundbreaking ceremony in November 2025, attended by the Indian Government and dignitaries.

Ranjit Pendurthi, who's the Managing Director of Archean Chemical, sits on the Clas-SiC board now. Archean has brought a different perspective to our board, a really welcome perspective from my behalf.

RS: *Earlier this year, you signed a deal to set up a power fab in mainland Europe. What's Clas-SiC's role in this project, how much progress has been realised, and what is still to do?*

JW: Our role in the Bulgarian project will be the same as the Chinese and Indian licence agreements. We've signed an early engagement commitment to help them build a business plan to attract further investment.

We've been working in partnership with Wafer Fab Solutions, to help them to work on a toolset, and to help them build an OpEx and CapEx plan to feed into their business plan. The idea is that we will then help them set up the fab in Bulgaria and transfer our technology, whatever the generation of technology is at that point in time.

RS: *The founder of II-VI, Carl Johnson, is Clas-SiC's executive chairman. How much of a role is he playing in the direction of your company?*

JW: I personally value his mentorship over the years. He's a lot of experience. It's not just the technical side – he's run a huge company that's had varied revenue streams, the same as Clas-SiC does. We have our R&D revenue stream, our tech revenue stream, our production revenue stream, and our licencing revenue stream.

I have a weekly one-to-one with Carl that lasts an hour. That's the only input he has into the day-to-day running of Clas-SiC. The conversations are led by me. They can cover blue-sky thinking, a current issue we're having, or sometimes just how life's going for us.

I've been in the CEO role here at Clas-SiC for over two years. Clas-SiC has changed a lot over that time because the market has changed. Thankfully, Carl and the rest of the board have been extremely supportive to allow us to do that.

RS: *You have process design kits for 1200 V, 1700 V and 3300 V, and another for 2,300 V in development. How much interest is there in the higher voltages within this range?*

JW: There's a lot of interest. Electric cars require longer ranges and faster charging. Also, as governments are looking to improve grid infrastructure, devices that work at higher powers are required. We have customers prototyping as high as 6.5 kV with us. We even have others talking to us about 10 kV.

Our design kit is pretty flexible. We're really willing to get our customers to design and own the reliability of the device termination. We can adapt processes as much as we can. What the customer is doing is leveraging Clas-SiC's experience and processing of silicon carbide to push voltages higher. We're small and flexible enough that we're willing to do that.

These products at extremely high voltages, they'll never be high volume. They're probably quite niche. However, that's where Clas-SiC fits. So, it's a good part of our business.

RS: *In addition, you have a process design kit for diodes. Does this account for a significant proportion of your business?*

JW: Two years ago, I think diodes accounted for about 10 percent of the business. Last year it increased. This year it has decreased again.

One of the main drivers is that the licenced fab in China was mainly a diode customer. Now they've got their own fab. They're producing in their own fab. We get the benefit of royalties, but the diodes are not produced here at Clas-SiC.

Recently, we have attracted a few customers at an R&D level that are looking at a more bespoke-type diode technology. But I would say it's probably back down to 10 percent of our business.

RS: *There are two types of MOSFET: planar and trench. You offer the former, but are developing the latter. What's the motivation behind extending into trench MOSFETs?*

JW: Our customers have driven us towards developing a trench process. We have processed trench MOSFETs before, but it's been a customer-owned process. Now we are developing our own trench PDK, so customers will be able to design on our own process. The aim is to have a trench PDK by mid-year.

We also have super-junction on the horizon. The new kit we're bringing in is to help serve that technology roadmap. That's where the £ 10 million investment came in for technology advancement.

RS: *You offer both prototyping and low-to-medium volumes of production. Which of these accounts for most of Clas-SiC's day-to-day activity?*

JW: It's mixed. Having just come from the morning meeting, about 60 percent of the work-in-progress in the fab today is technology and 40 percent is production.

Most of the technology work is extremely engineering-intensive. We work with some major players in the industry that use us at an R&D level, because they're trying to leverage our expertise. I would hope in future that we will be able to licence parts of the process and black-box solutions.

Just now, for these people, we may use our gate-oxide process or our backside annealing process, but that's owned by Clas-SiC. They send us wafers just for that process. I hope in future we could licence these parts.

We also have long-standing, fab-less design companies.

RS: *You also offer licensing of technology. How does that work in practice, and is it a significant part of your business?*

JW: It's quite unique, as there are not many silicon carbide companies that will licence their technology and know-how right now.

While licensing is a key revenue stream for us, it's not only the revenue that's key – it's having capacity in these high-volume fabs. That's very much part of our business model and strategy. In practise, we assist these fabs to get up and running by transferring our processes.

I think if I was to ask the owner of the Chinese fab, she would say that we've saved about three-to-four years in time-to-market because they qualified, prototyped and ran product here on our process while their fab was being built. They were able to sample customers. It became a process transfer, rather than a full qualification for their customers.

It's an ongoing relationship with our licenced customers. As we develop our technology, they will come back to licence the next generation. That's actually already happened with the Chinese fab.

At the ICSCRM Conference in 2025, Professor Anant Agawal stood up on stage and said that to make silicon carbide a success, it's going to take a village. And that is so, so true. I think collaboration is absolutely key.

RS: *When transferring licenced technology and supporting these companies, do you send engineers to these fabs?*

In November 2025 Clas-SiC CEO Jen Walls addressed an audience of around 600 at the SiCSEM fab groundbreaking ceremony at Odish.

JW: If I think back to China, our engineers were out there for about three months. Not the same engineers, because we would concentrate on one part of the process and set that up, and then another set of engineers would go.

That was an absolutely amazing experience for a lot of the guys and girls here at Clas-SiC. We sent graduate apprentices, we sent modern apprentices, as well as senior engineers, principal engineers.

We still support these fabs through a consulting-type basis, and we'll continue to do that. It's an ongoing relationship.

We've been running this process for so many years, and developing it and improving it. Any problem they see, we have probably seen before. Where it's maybe taken them three weeks to get the root of a problem, we can fix it overnight.

RS: *The SiC industry is shifting to 200 mm wafers. As I understand it, you are still working with the 150 mm platform. Do you have plans to move over?*

JW: It would be too much investment right now. There's no immediate plan. However, when we're procuring equipment, we make sure that it's 200-millimetre-compatible.

Our licenced fabs are very much a route to 200 millimetre, because they are setting up as 200 millimetre.

We can compete at a low production level because of our varied revenue streams. In low-rate production, we can offer similar pricing to what these fabs can offer in China. However, that won't remain forever, so we do need to get our licenced fabs at 200 millimetre up and running.

RS: *With SiC, doping may be realised through both ion implantation and epitaxial growth with dopants. What do you see as the pros and cons of both approaches?*

JW: For me the jury's out. It's very early days. I think only time will tell.

We work with customers looking at and evaluating both methods. Implant is obviously an expensive process, and planters are costly CapEx investment. They're an expensive tool to manage in production. However, control is extremely good.

RS: *One area for improvement of the SiC MOSFET is its channel mobility. Many employ nitridation to address this issue, and there are reports of alternative, promising processes. Does Clas-SiC have a nitridation process, and if so, is it advancing?*

JW: We are always advancing, and what we have available right now is the best our customers have seen. Right now, there's ongoing work with Purdue University.

> "Electric cars require longer ranges and faster charging. Also, as governments are looking to improve grid infrastructure, devices that work at higher powers are required. We have customers prototyping as high as 6.5 kV with us. We even have others talking to us about 10 kV"

RS: *Within the UK community, is their much effort on SiC? And which research groups and companies are you collaborating with?*

JW: Specific silicon carbide activity within the UK is pretty limited. We have one commercial customer in the UK on silicon carbide that we're working with at a device level.

We work extremely closely with academia, with Warwick, the University of Glasgow, Strathclyde, and other universities around the UK.

We also work with some of the Catapults, NMS (the National Microelectronics Manufacturing Centre), and with partners that are looking to develop advanced module packaging or advanced packaging methods.

RS: *A company is only as good as its people. Carl Johnson definitely believes in that. What are you doing to recruit the best staff, from technicians to experienced engineers?*

JW: I'm glad that you mentioned Carl, because that ethos absolutely carries down into Clas-SiC. People are absolutely our main asset.

Because we've grown quickly, bringing new people in to Clas-SiC is always on our watch. Carl and I very much share that vision that growing our own talent is always a valuable route. 10 percent of our workforce are graduate and modern apprentices. The modern apprentices have all been promoted from within.

Graduate apprentices have all been linked to the company in some way, whether they've been here on work experience, or whether they were a friend or family member of an employee. We've promoted one of our operators into a quality role and another into a facilities technician role.

We look where we can to bring people on to be the best they can possibly be. This benefits not only the employee, as it allows us to bring in new blood and see where that goes.

Professional engineering roles are obviously harder to fill because of the skills gap in the UK. We have had to bring in people from overseas. I sit on the technology Scotland Skills Group, and I'm part of TechWorks UK, looking at skills for women in technology. Keeping the talent pipeline filling in the UK is extremely important.

To retain talent here at Clas-SiC we've had to be as flexible as we can. We definitely had an ageing workforce, looking to retire. We have some engineers who would normally have retired that we're managing to retain because they're working on reduced days to give a better work-life balance. They enjoy it, and want Clas-SiC to be a success, so they're happy to stay. Some of these engineers I've personally worked with for almost 30 years.

RS: *What are the goals for Clas-SiC for 2026?*

Our absolute main goal for 2026 is to achieve IATF 16949 accreditation – that's automotive accreditation. It's imperative for us, for working with customers that work in the automotive supply chain. We've got our stage-one audit in January, followed by our stage-two audit. So hopefully by the middle of 2026 we'll be IETF 16949 qualified.

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New directions for GaN electronics

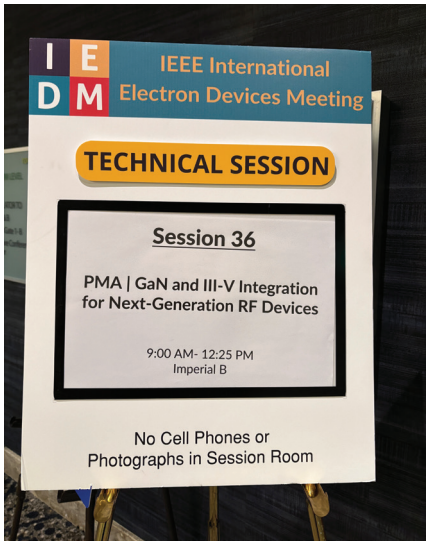
Advances in epitaxy and processing are opening up new opportunities for GaN in handsets, computation, and the delivery of RF signals in the X-band

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

GaN is, without doubt, the most important and pervasive material within the family of compound semiconductors. It's initially enjoyed tremendous success within the optoelectronics domain, where it's been used for several decades to produce countless LEDs, as well as blue and green lasers that are deployed for a variety of tasks, including material processing and colour projection.

While some may argue that the best days of GaN optoelectronics are now behind us, the same cannot be said for the electronics sector. Here GaN is increasingly employed for RF power amplification and fast-charging, with sales sure to increase with improved performance – and there are also lucrative opportunities in handsets and computation.

Key to fulfilling all these promises are technological breakthroughs, which may take the form of improvements in device design or processing. Many advances on these fronts are reported at global conferences, and at the most recent *International Electron Devices Meeting* held in early December in San Franscico three significant milestones were unveiled: the first integration of a GaN low-voltage power amplifier into a handset, where a three-stage III-N MMIC provided an efficiency of over 50 percent; the development of a GaN chiplet technology based on 300 mm GaN-on-silicon that has much appeal for high-performance, high-density efficient power and high-speed/RF electronics; and the fabrication of an X-band GaN-on-SiC-based HEMT that delivers



a substantial hike in power density, realising 41 W mm^{-1}.

Handsets: From GaAs to GaN?

Since the mass adoption of the mobile phone at the turn of the millennium, the critical task of RF amplification has been performed with a GaAs-based device, typically a HBT. One of its strengths is that it's well-suited to being driven by a battery, which provides just a few volts.

Offering an attractive alternative on several fronts is the GaN-on-silicon PA. This technology delivers a superior power performance from a smaller form factor, a key advantage, given the limited space in smartphones. What's more, GaN-on-silicon HEMTs have the potential to be integrated with on-chip power supplies, and can be manufactured in high volume in silicon lines, ensuring cost-competitive chip production.

However, for deployment in handsets, the GaN-based PA has an Achilles heel – its high operating voltage, with devices typically driven at 28 V. But there is no longer a need to target a reduction to just a few volts to develop a handset-friendly solution, thanks to the introduction of higher supply voltages of up to 10 V, realised with the introduction of advanced power management ICs.

Taking advantage of this and delivering a step-change in the performance of PAs that can serve in handsets is a collaboration led by Dynax Semiconductor and involving engineers at Xiaomi Communications and The Hong Kong University of Science and Technology.

Speaking on behalf of this partnership at IEDM, Haochen Zhang from Dynax highlighted a HEMT efficiency of over 80 percent at a drain voltage below 10 V, and a three-stage GaN MMIC evaluated in the main board of a smartphone with a power-added efficiency of more than 50 percent.

"We believe that this marks the dawn of a wireless communication era defined by gallium-nitride-based radio-frequency technologies," remarked Zhang.

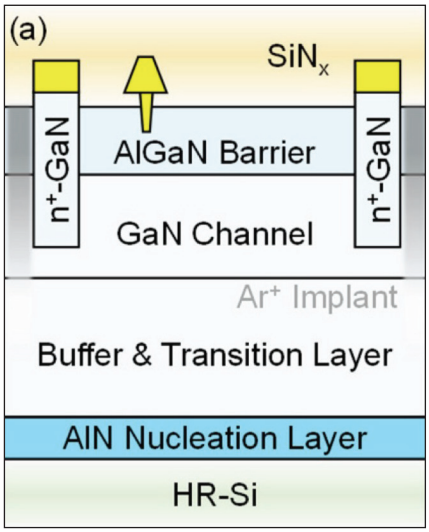
Dynax, which has constructed an advanced GaN manufacturing centre that includes a 4,500 m^2 cleanroom, has devoted many years to pursuing the deployment of GaN in handsets. Efforts have been supported by an R&D team with over 150 staff that has helped to file over 500 patent applications, both domestically and internationally.

Zhang explained that one of the three key challenges the collaboration faced in developing a GaN PA technology for mobile phones was to ensure that the knee-voltage is as small as possible. "Secondly, gallium nitride devices suffer from gain soft-compression, which undermines linearity. Thirdly, unlike gallium arsenide HBTs, which are voltage-driven D-mode devices and work comfortably at 4.5 volts, gallium nitride devices are voltage-driven D-mode devices with a relatively high operating drain voltage."

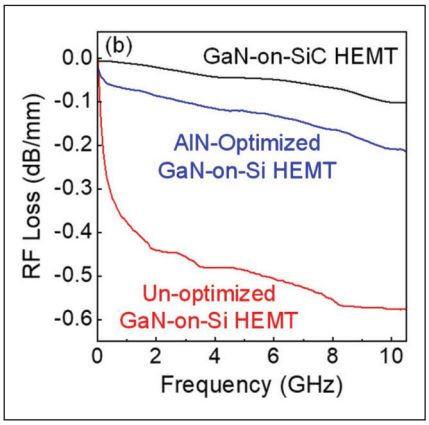
To address the latter concern, Zhang and co-workers introduced a power-management IC, and considered the voltage supply to both the gate and the drain.

Fabrication of the collaboration's devices (see Figure 1) began by loading high-resistivity silicon substrates into an MOCVD reactor, applying an *in-situ* substrate treatment, and adding an AlN nucleation layer with an optimised thermal budget to regulate the distribution of impurity atoms at the AlN-silicon interface. This approach is claimed to reduce aluminium diffusion into the silicon substrate and suppress the formation of a parasitic channel in silicon, which would lead to an RF loss associated with the substrate.

"The substrate loss and interface loss is optimised, to be around 0.2 dB at



➤ Figure 1. Engineers at Dynax Semiconductor, Xiaomi Communications and The Hong Kong University of Science and Technology have developed a GaN HEMT for providing RF amplification in handsets.



➤ Figure 2. Substrate loss for III-N-on-silicon heterostructures is reduced with an AlN nucleation layer that has an optimised thermal budget and regulates the distribution of impurity atoms at the AlN-silicon interface.

10 gigahertz, which is a level comparable to gallium-nitride-on-silicon-carbide devices," remarked Zhang.

Using these epiwafers, the team deposited a hard mask for re-growth of heavily doped GaN. Dry etching removed the SiO_x/SiN_x hard mask prior to GaN re-growth, involving a pre-dose of indium atoms that acted as a surfactant, improving interface morphology and promoting doping efficiency through the suppression of silicon self-compensation. Fabrication of the HEMTs was completed with hard mask removal, surface passivation through low-pressure CVD of SiN_x, and the addition of source and drain electrodes and a T-shaped gate. Resulting devices have a contact resistance of 0.09 Ω mm and a sheet resistance 251 Ω/sq.

Measurements of the DC characteristics of these devices – which have a gate length of 0.25 μm, and gate-to-source and gate-to-drain distances of 0.4 μm and 0.8 μm, respectively – determined an on-resistance of 0.76 Ω mm^{-1}, a knee voltage of 1.6 V, and a saturated drain-source current of 1.5 A mm^{-1}. It is said that these impressive figures provide the foundation for the high performance of the GaN HEMTs.

The breakdown voltage for these transistors is 98 V, a value claimed to fully guarantee device performance, ruggedness and reliability.

Small-signal characteristics at a drain-source voltage of 5 V revealed a peak cut-off frequency (f_T) of 31.2 GHz and a maximum oscillation frequency (f_{max}) of 66.2 GHz, and large-signal power sweeps determined a power-added efficiency of 84.2 percent and a maximum output power of 2.84 W mm^{-1}.

Zhang pointed out that even higher output powers have been realised by other teams, using devices with an InAlN barrier layer. "However, the reliability of such indium-incorporated devices remains an issue."

To determine the reliability of their devices, Zhang and co-workers subjected 15 devices to high-temperature reverse bias tests (HTRB) and high-temperature operating lifetime (HTOL) tests.

"After the HTRB and HTOL stress, the devices show negligible performance degradation," said Zhang. For example, the change in output power is below 0.1 dB.

The engineers also determined a mean-time-to-failure of 2,500 years at a junction temperature of 225°C.

These GaN HEMTs provided the key building block for a three-stage PA MMIC that features a shunt power structure with high-pass and low-pass networks to increase bandwidth and linearity.

Zhang told delegates that to optimise linearity, it is critical to consider the inter-stage matching network between the driver PA and the final-stage PA.

> "We demonstrate, for the first time, a library of fully functional integrated on-die CMOS digital circuits – from inverters, logic gates, multiplexers and flip-flops to ring oscillators – all implemented with a monolithically integrated gallium nitride and silicon PMOS process"

Reference	IEDM 2025			[1]	RF7205	[2]
Freq. (GHz)	1.6	1.8	2.0	0.814~0.915	1.85 ~ 1.91	2.3 ~ 2.6
V_{DD} (V)	10			3.5	3.4	5
P_{sat} (dBm)	41.6	40.9	40.3	30 ~ 31.5	30	32.8
P_{rated} (dBm)	39.8	38.3	38.4	29	28	32.1 ~ 32.8
PAE (%)	57.7	52.1	54.5	33 ~ 36	41 (Typ.)	34.6 ~ 37.5
Gain (dB)	40.3	44.0	40.4	29 ~ 32.5	26 ~ 31	31.7
ACPR (dBc)	–34.6	–33.6	–34.2	-35	–36	–33.2
FBW (%)	22.2			11.7	3.2	12
Technology	GaN-on-Si HEMT			GaAs HBT	GaAs HBT	GaAs HBT

➤ Table 1. A comparison of the performance of the III-N-on-silicon low-voltage MMIC produced by engineers at Dynax Semiconductor, Xiaomi Communications and The Hong Kong University of Science and Technology: [1] W. Y. Refai et al. IEEE Trans. Microw. Theory Tech. **68** 3519 (2020); a commercial product, the RF7205; [2] M. Liu, et al., IEEE Microw. Wireless Tech. Lett. **33** 1305 (2023).

And he revealed: "To counteract gain compression, the gain curve of the driver stage was deliberately designed to expand at power saturation, and thereby enhance gain flatness over the entire bandwidth."

Measurements of this MMIC under modulated signals at 2 GHz revealed a gain of 39.3 dB and a power-added efficiency of 60.1 percent. Benchmarking against GaAs HBTs, using values in publications and for a commercial product (see Table 1), led Zhang to claim: "This work demonstrates significantly higher output powers, due to a higher supply voltage, and especially optimised device fabrication and epi processes."

The team's three-stage MMIC has been evaluated on a smartphone mainboard using a radio communication tester, connected to the antenna connector by a coaxial cable. The phone battery powers the system, and is paired with an external power management IC that integrates logic control, boost conversion and negative-voltage generation for MMIC biasing. Thanks to the introduction of the power management IC, the smartphone battery voltage increases from 3.8 V to 10 V, with this voltage applied to the drain bias.

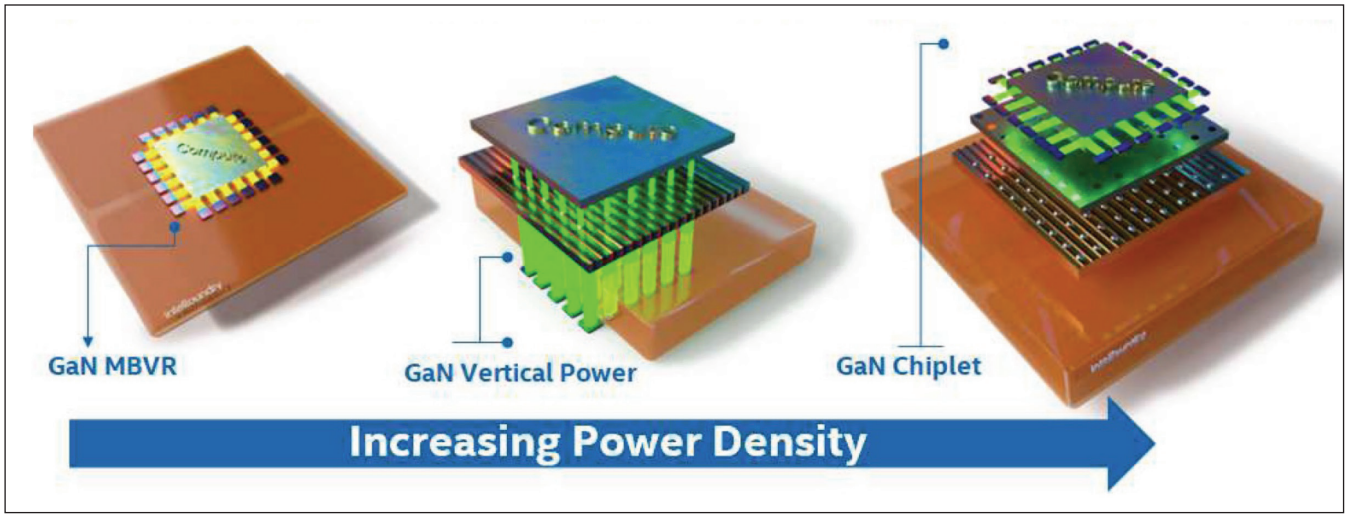
Using π/4-QPSK modulation with a 20 percent duty cycle and a frequency of 2 GHz, the power amplifier produced an output power of 38 dB at a power-added efficiency of 51.4 percent.

"In future work further device linearity is required, especially for high-order modulation," remarked Zhang, who commented that there is also the opportunity to shrink dimensions, via system-in-package designs, such as those based on flip-chip bonding.

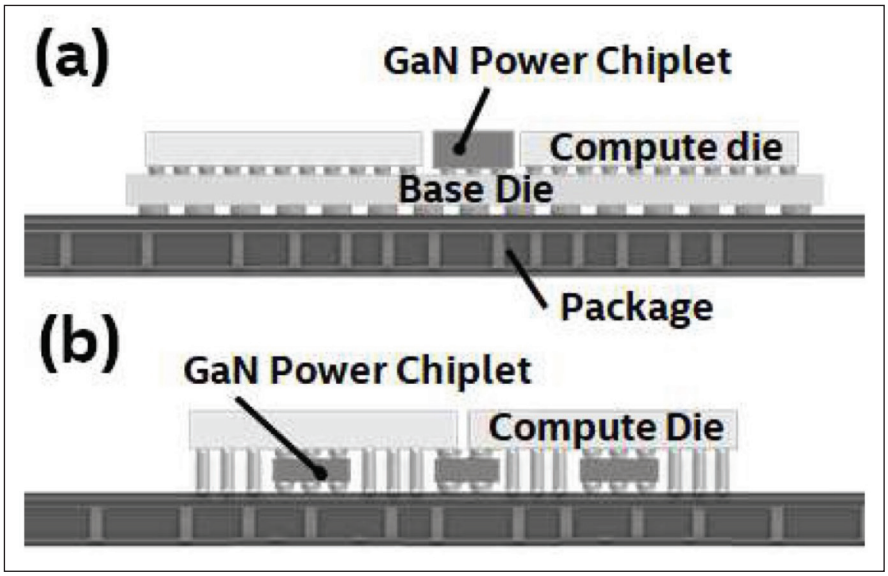
GaN chiplets

In computing, it is expected that over time discrete silicon components powering motherboard voltage regulators will be replaced with GaN technologies – initially GaN discrete modules; and then approaches where GaN power modules are still on the board, but situated directly below the compute package; and finally, a transition to chiplet integration, with GaN power chips integrated with other die in the same compute complex (see Figure 3). For the latter, options include what is described as Foveros integration and next-generation 3D chiplet integration (see Figure 4).

Efforts to develop these new technologies, needed to address demands for higher power densities, superior efficiencies and tighter integration, are underway at Intel – and at the recent IEDM meeting Han Wui Then detailed this company's development of GaN chiplets, as well as the industry's first library of fully integrated on-die CMOS digital circuits, produced using a monolithically integrated GaN *n*-type MOSHEMT and silicon PMOS process.



➤ Figure 3. As demand increases for higher power density and efficiency increases, there will be an evolution in GaN point-of-load power solutions from discrete motherboard voltage-regulators (MBVR) to GaN vertical power, and then to chiplet integration with GaN power chiplets.



➤ Figure 4. Examples of chiplet integration with GaN power chiplets: (a) Foveros integration, (b) next-generation 3D chiplet integration.

According to Then, as there is little room in any direction to house the chiplets in the complex, it's critical that the GaN transistor technology has a high density, a high performance, and is capable of delivering current densities of at least 10 A mm^{-2}.

In addition to these requirements, the GaN chiplets need to be ultra-thin – their thickness must be well below 50 µm – as this will enable short (low aspect-ratio), low-resistance through-silicon vias that ensure low resistive losses and acceptable thermal dissipation.

While ticking these boxes, it's important to note that there is no room in the complex to accommodate more chiplets, such as CMOS companion dies.

"It is crucial that the gallium nitride chiplets are as complete as possible, with the required functionalities, such as CMOS controllers, low-leakage drivers, PMOS current mirrors, telemetry circuit tees, etcetera," remarked Then, who added that functionalities, such as integrated CMOS drivers and date time controllers, are essential for achieving optimal efficiencies and fast-switching to minimise passives.

"To this end, we demonstrate, for the first time, a library of fully functional integrated on-die CMOS digital circuits – from inverters, logic gates, multiplexers and flip-flops to ring oscillators – all implemented with a monolithically integrated gallium nitride and silicon PMOS process that's achieved by layer transfer and designed using a process design kit."

Fabrication of the chiplets involves what's described as a 'stealth dicing before grinding' process that produces a thinned, singulated 300 mm GaN-on-silicon wafer. Following this process, the underlying silicon substrate is just 19 µm thick, leading Then and co-workers to claim that they have produced the industry's thinnest fully processed 300 mm GaN wafer.

According to Then, characterisation of GaN transistors with a 30 nm gate length has determined: an excellent on-resistance; a low gate leakage, below 3 pA μm^{-1}; a breakdown voltage of up to 80 V; and values for f_T and f_{max} of 212 GHz and 304 GHz, respectively. For gate lengths up to 130 nm, f_{max} remains above 200 GHz.

It's claimed that this RF data bodes well for RF and high-speed applications, such as photonics. According to the research team behind this work, their GaN chiplet technology could have potential use in these applications.

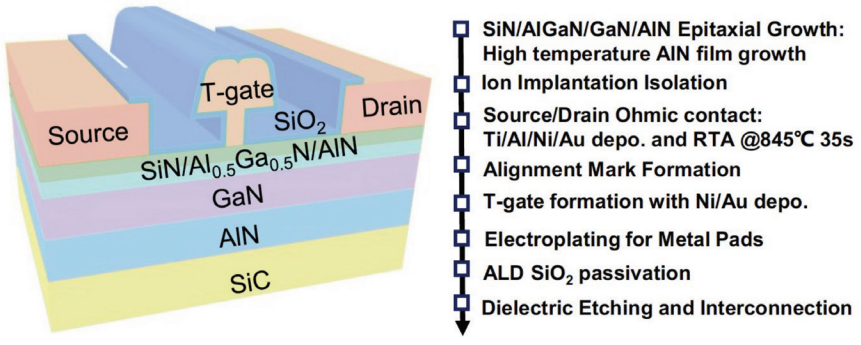
Then and co-workers have undertaken an extensive reliability study of their GaN MOSHEMTs, with investigations considering time-dependent dielectric breakdown, positive-bias temperature instability, HTRB and hot-carrier injection.

It's claimed that these studies demonstrate promising results towards meeting the reliability metrics for 300 nm GaN MOSHEMT technology.

Hiking power in the X-band

GaN HEMTs operating in the RF domain are widely deployed in satellite communication, radar and 5G base stations. They are valued in all these applications for their high-power density, peaking at around 31-33 W mm^{-1}.

While this figure is far better than that for RF transistors produced with traditional III-V technologies, it has not improved significantly for around two decades – until now, thanks to work by a Chinese partnership that's led by engineers at Xidian University, and also involves researchers at Dynax Semiconductor, Chengdu

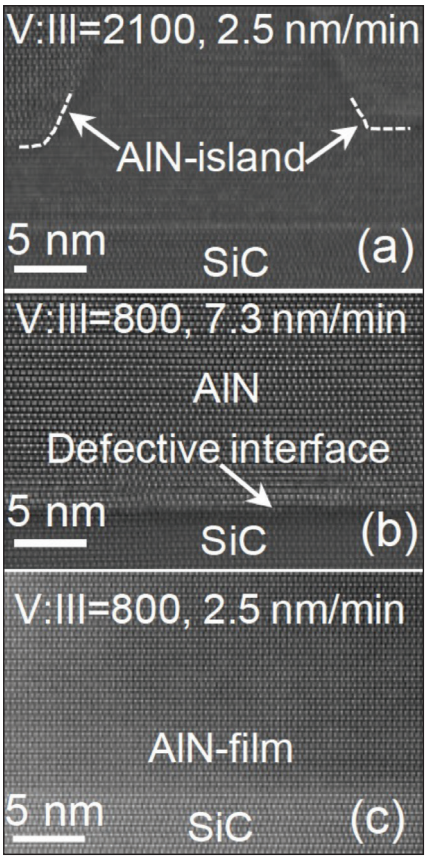


➤ Figure 5. A passivated AlGaN/GaN/AlN RF power HEMT on a SiC substrate produced by a partnership between Xidian University, Dynax Semiconductor, Chengdu Aerospace Bomu Electronic Science and Technology Company and Wuhan University. Key elements of this work include a film-like AlN buffer and a thin GaN channel.

Aerospace Bomu Electronic Science and Technology Company and Wuhan University.

Speaking on behalf of this partnership at IEDM, Hong Zhou from Xidian University remarked: "The achieved device performance sets several new records for gallium nitride RF power transistors." They include a record maximum output power density of 41 W mm^{-1} and a value for the product of f_T and breakdown voltage of 31 THz V (see Figure 5 for device and processing details).

According to Zhou, the hike in performance comes from optimisation of the heterostructure, including an abrupt interface between AlN and SiC.



➤ Figure 6. High-resolution transmission electron microscopy image of AlN/SiC interfaces with different growth conditions reveal the benefits of a relatively low growth rate and V-III ratio. (a) V-III ratio of 2100 and growth rate of 2.5 nm min^{-1}, (b) V-III ratio of 800 and growth rate of 7.3 nm min^{-1}, and (c) V-III ratio of 800 and growth rate of 2.5 nm min^{-1}. With an optimised V-III ratio of 800 and a growth rate of 2.5 nm min^{-1}, an atomically abrupt interface between a high-quality AlN buffer and SiC substrate can be formed.

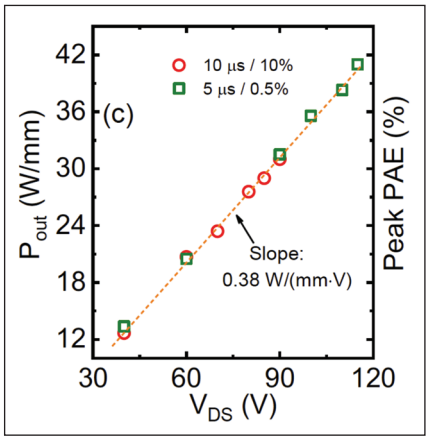
Zhou and co-workers attribute the lack in progress prior to their work to issues associated with the growth of GaN-based epistructures on foreign substrates, typically SiC. The island-like AlN nucleation layer that's often employed creates a high thermal boundary resistance between AlN and SiC; and another common downside is a GaN buffer with a thickness of a micron or more, which provides a much-needed reduction in dislocation density, at the expense of an additional compromise in thermal conductivity.

These issues are addressed with a film-like AlN buffer, providing an abrupt AlN/SiC interface that reduces the thermal boundary resistance and the dislocation density.

Success has come from the growth of an AlN buffer layer, using the following conditions to enhance aluminium adatom surface migration: a V-III ratio of just 800; a growth temperature of 1300°C; and a growth rate of only 2.5 nm min^{-1} (see Figure 5). On this buffer, just 190 nm-thick, the team added a 210 nm-thick GaN channel that has a defect density of just 1.67 x 10^{8} cm^{-2}, according to cathodoluminescence mapping.

The superior heat dissipation of the thinner structure is highlighted in laser-based transient thermoreflectance measurements. This technique shows that for a conventional power device with an AlN nucleation-island and a 1.2 μm-thick GaN buffer layer, device temperature increased by 98 K when operating at 13 W mm^{-1}. In comparison, there is an increase in temperature of just 47 K for the thinner device, when operating at the significantly higher power density of 24 W mm^{-1}.

Additional measurements have determined a sub-threshold swing of 77 mV dec^{-1} and an on-off ratio of 10^{9}, results indicative of a high-quality interface. For a device with a gate-to-drain distance of 1.2 μm, the maximum blocking voltage is 161 V – that's claimed to be higher than that in traditional GaN RF devices, an increase attributed to the effectiveness of the ultra-wide bandgap AlN barrier in boosting the blocking field.



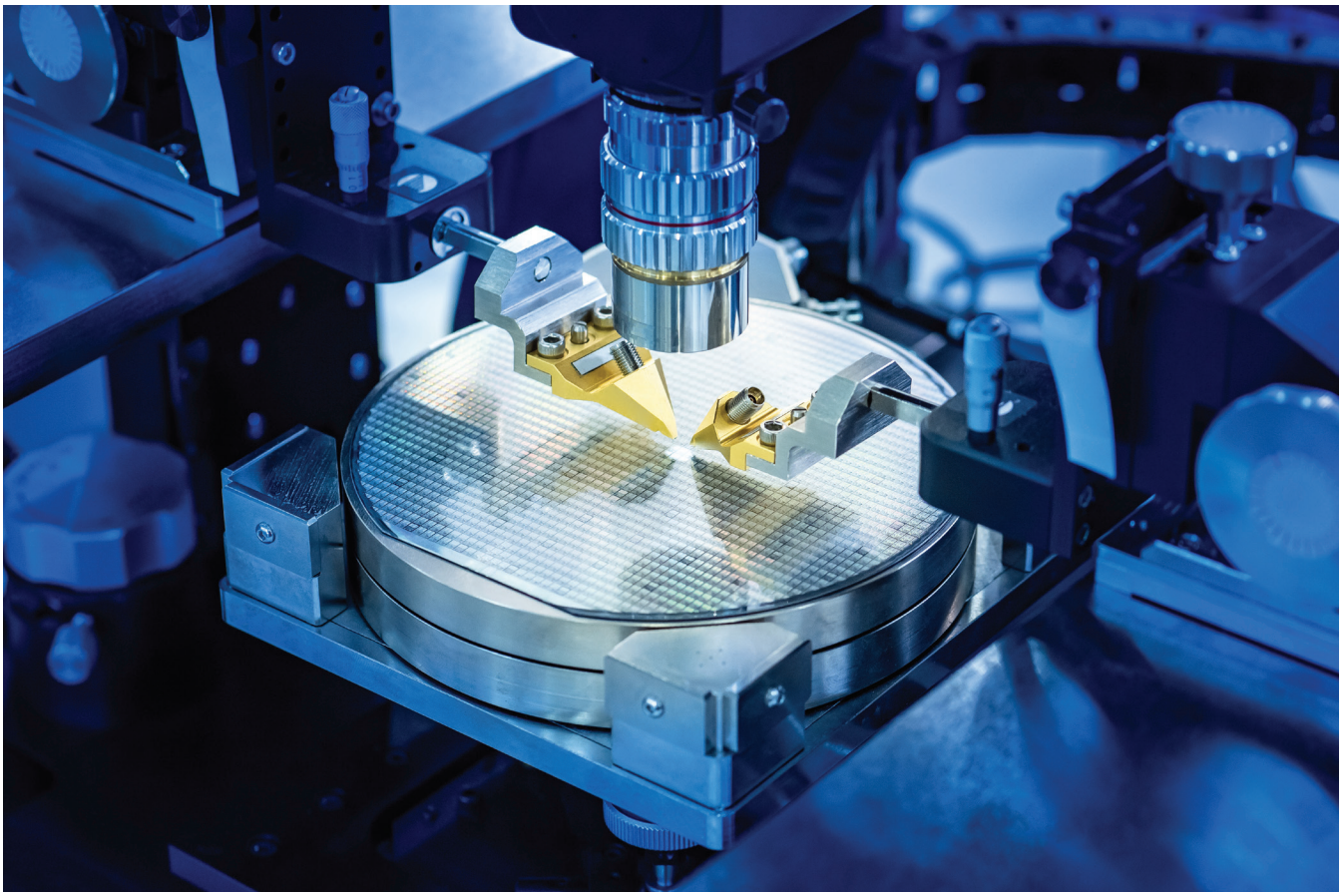
➤ Figure 7. Peak power-added efficiency (PAE) versus drain-source voltage V_{DS} at two pulse conditions: a pulse width of 10 μs, duty cycle of 10 percent and V_{DS} of 90 V; and a pulse width of 5 μs, a duty cycle of 0.5 percent and V_{DS} of 115 V. A smaller duty cycle at the higher V_{DS} is used to protect the RF probe tips, since each measurement lasts for more than 10 minutes with maximum output power of 40 dBm.

Zhou and co-workers are also encouraged by the results of gate- and drain-lag measurements, which show a dispersion of less than 8 percent and validate the suppression of self-heating and current collapse effects.

Values for f_T and f_{max} are 72 GHz and 134 GHz, respectively, for their novel HEMT with a 230 nm gate length and a drain-to-source spacing of 2.2 μm. Increasing this spacing to 8.6 μm produced a fall in f_T and f_{max} to 56 GHz and 104 GHz, respectively.

Using a device with a drain-to-source spacing of 5.6 μm and a 230 nm gate length, at a source-to-drain voltage of 90 V and a gate width equal to 240 μm (2 x 120 μm), a 10 GHz input signal with a pulse width of 10 μs and a duty cycle of 10 percent produced an output power of 31 W mm^{-1} at a power-added efficiency of 51 percent. Increasing the drain-source voltage to 115 V, and moving to 5 μs pulses and a duty cycle of 0.5 percent, increased the output power to a record 41 W mm^{-1} without reducing the power-added efficiency (see Figure 7).

This breakthrough, and those related to GaN chiplets and GaN HEMTs for handset PAs, highlight that while much has already been accomplished with this nitride, there's more to come.



HEMTs: InAlGaN raises the ceiling

Thermal CVD equips next-generation InAlGaN/GaN HEMTs with high frequencies, exceptional powers and high reliability

BY ATSUSHI YAMADA FROM FUJITSU LIMITED

EXTENSIVELY deployed in defence and communication systems, GaN-based semiconductors are held in high regard as optimal materials for high-power and high-frequency applications. However, due to decades of intense development, conventional AlGaN/GaN HEMTs are now encroaching the fundamental limits of this particular material system, making further improvements in output performance increasingly difficult. To overcome this plateau, innovative approaches are needed for next-generation device technologies that will sustain progress in advanced electronics.

A particularly promising candidate for raising the ceiling that limits what's possible is a variant of the nitride-based HEMT that utilises indium-based nitride semiconductors in the barrier layer – it's an alternative that is commonly referred to as the InAlGaN/GaN HEMT. Compared to its conventional cousin, the pairing of InAlGaN and GaN creates a two-dimensional electron gas (2DEG) with a higher density, an advantage that positions this material combination as a strong contender for next-generation devices optimised for the delivery of high powers.

Unfortunately, it not easy to unleash the full potential of InAlGaN materials. The issue is that this quaternary introduces a fundamental challenge, rooted in its chemical structure. There's a relatively weak bond between indium and nitrogen that renders this class of material particularly vulnerable to damage during fabrication processes, especially those involving exposure to a plasma. Issues arising from the intrinsic fragility include the introduction of non-uniform surface potentials and a reduction in electron mobility – both adversely affect overall device performance.

One consequence of these drawbacks is that the InAlGaN/GaN HEMT is yet to demonstrate RF output characteristics that exceed those of the conventional AlGaN/GaN HEMT. It's a state of affairs that highlights the ongoing need for innovation in

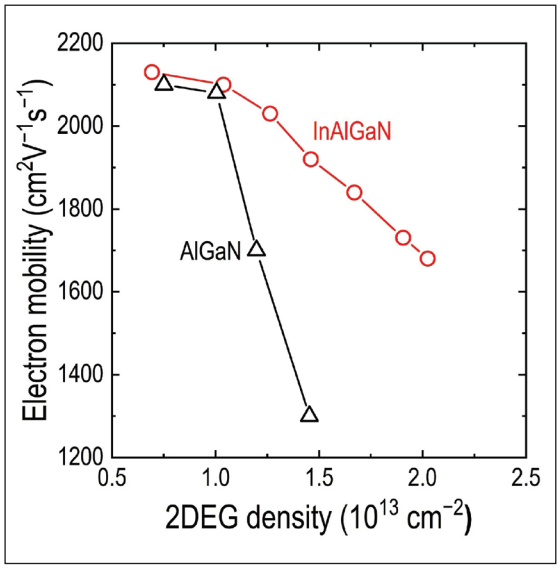
epitaxial growth and process optimisation. Growth is held back by the adoption of epitaxial and process techniques originally developed for the traditional duo of AlGaN and GaN. Despite InAlGaN exhibiting distinct physical properties, conventional methods are employed without sufficient adaptation, obstructing this alloy from fully realising its potential.

To address this issue, our team at Fujitsu has undertaken a comprehensive re-evaluation of epitaxial growth conditions and process technologies, while focusing on the objective of developing device structures optimised for high-frequency, high-power operation. During this exercise, we directed our attention at the deposition conditions of the SiN_x passivation layer, which plays a critical role in suppressing surface damage. Adopting this optimisation strategy enhanced electron mobility, and ultimately realised an output performance exceeding that of conventional AlGaN/GaN HEMTs.

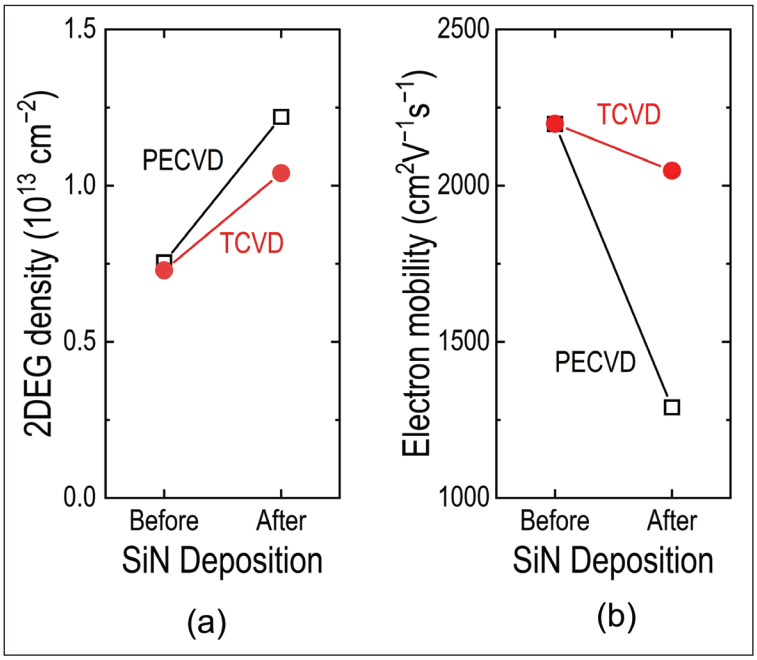
Why InAlGaN?

The primary benefit of employing an InAlGaN barrier layer is not limited to simply attaining a high 2DEG density; rather, it is the simultaneous realisation of a high electron mobility and a high 2DEG density. One strength of InAlGaN is that it consistently exhibits a higher electron mobility than AlGaN at equivalent 2DEG densities, rendering it a compelling candidate for utilisation in next-generation devices (see Figure 1).

In conventional AlGaN barriers, increasing the aluminium content enhances the 2DEG density, but at the expense of adding strain in the material. The downside of strain is an increase in the effective mass of the electrons, impairing their mobility and limiting device performance. Conversely, InAlGaN incorporates indium, a material that relaxes strain and boosts mobility, even at elevated 2DEG densities. This renders InAlGaN a well-optimised material system for maximising output power.



➤ Figure 1. Dependence of the electron mobility on the 2DEG density in the InAlGaN/GaN and AlGaN/GaN HEMT.



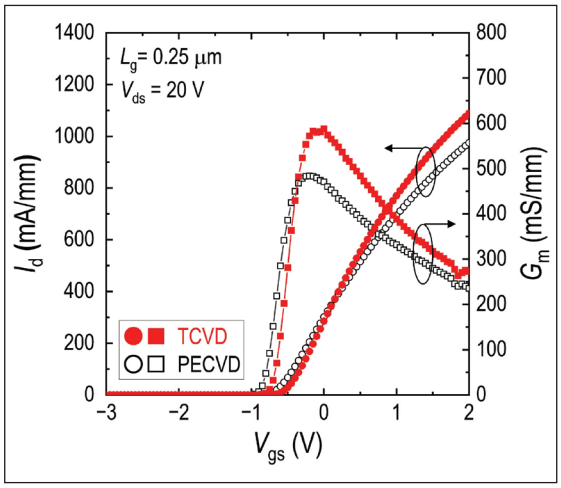
➤ Figure 2. Changes in (a) 2DEG density and (b) electron mobility before and after SiN passivation using thermal CVD and plasma-enhanced CVD techniques.

However, there are still drawbacks with InAlGaN barriers. While extremely high 2DEG densities are beneficial for increasing current, they can significantly reduce breakdown voltage, an essential parameter for high-power operation. Consequently, it is imperative for engineers to be meticulous in their material and device design, as this is critical to ensuring the optimal balance between 2DEG density and mobility.

In our work at Fujitsu, we excel in this regard, prioritising the enhancement of electron mobility as a key strategy for improving output power. By optimising the material structure and growth conditions, we have targeted the full exploitation of the intrinsic advantages of InAlGaN for high-performance HEMTs.

Optimising the epitaxial structure

Early research into InAlGaN-based HEMTs investigated the utilisation of the ternary InAlN as the barrier layer, because this alloy can be precisely lattice-matched to GaN at an indium composition of about 18 percent. Lattice-matched InAlN effectively suppresses crystal strain, and the substantial spontaneous polarisation difference between InAlN and GaN delivers a hike in the 2DEG density compared with that of conventional AlGaN/GaN HEMTs – it's two-to-three times higher. Thanks to these combined strengths, InAlN/GaN structures are highly attractive for high-power applications.



➤ Figure 3. Transfer characteristics of InAlGaN/GaN HEMTs with SiN passivation using thermal CVD and plasma-enhanced CVD techniques.

However, there's a price to pay for this lattice matching – a high indium content, which demands low-temperature growth. This compromise hampers thermal robustness and limits process compatibility, creating challenges for device reliability.

To tackle these issues, we have turned to the quaternary alloy InAlGaN. By fine-tuning the gallium, indium and aluminium content, we precisely control lattice parameters and polarisation characteristics. It's possible to produce a heterostructure with the desired electrical properties while employing a reduced indium content that opens the door to elevated growth temperatures, key to enhancing thermal stability and reliability.

When adopting this approach, one must be mindful that InAlGaN is susceptible to significant alloy scattering, which threatens to degrade electron mobility. Crucial to mitigating this effect is the incorporation of a spacer layer. Often AlN is employed for this task. However, it's hard to form a smooth AlN layer, due to the low thermal stability of underlying GaN, which complicates high-temperature growth. Another issue is that the growth of InAlGaN occurs at relatively low temperatures, hindering surface smoothing and even promoting roughness. Consequently, InAlGaN-based structures necessitate an even greater degree of surface flatness for AlN than conventional AlGaN/GaN HEMTs.

To address this challenge, we have undertaken a comprehensive optimisation of the growth rate, and an augmentation of ammonia supply. This has led to successful formation of a flat AlN spacer layer, and ultimately a higher electron mobility and an enhanced performance for the InAlGaN/GaN HEMTs.

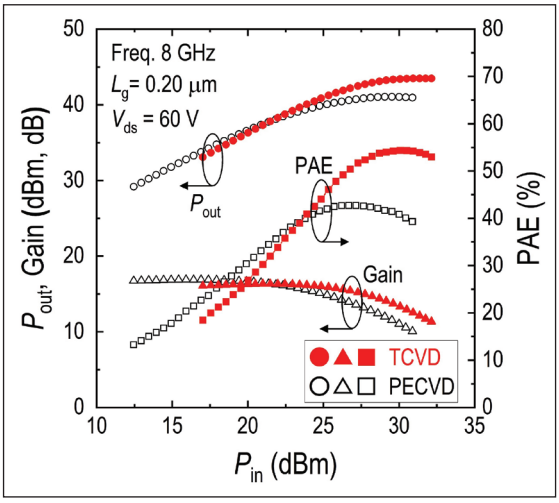
Critical passivation

High-quality epitaxial layers are essential for enhancing the performance of InAlGaN-based HEMTs. However, it's critical to not ignore the role played by the passivation layer – this must protect the device surface. One weakness of nitride semiconductors is their sensitivity to plasma processes, a vulnerability particularly pronounced in InAlGaN materials.

We address this issue with a thermal CVD method that eliminates plasma exposure during formation of the SiN_x passivation layer. This approach has the objective of enhancing output power.

To produce our InAlGaN/GaN HEMTs we load substrates into a horizontal-flow MOCVD reactor and grow a heterostructure featuring a 6 nm-thick $In_{0.05}Al_{0.39}Ga_{0.56}N$ barrier layer and a 2 nm-thick AlN spacer. In this reactor, we then add a SiN_x passivation layer by thermal CVD at 730°C using silane and ammonia. To provide a comparative reference, we also produce a sample using plasma-enhanced CVD of SiN_x at 250°C – this is a form of passivation widely employed in the fabrication of AlGaN/GaN HEMTs.

Electrical measurements reveal alterations to 2DEG density and electron mobility following SiN_x deposition by thermal and plasma-enhanced CVD (see Figure 2). Both forms of CVD increase the 2DEG density. With thermal CVD, density of the 2DEG increases from 0.73 x 10^{13} cm^{-2} to 1.04 x 10^{13} cm^{-2}; and with plasma-enhanced CVD, it increases it from 7.54 x 10^{12} cm^{-2} to 1.22 x 10^{13} cm^{-2}. The extent of these changes is far smaller than that for electron mobility, which exhibits markedly divergent behaviour. Plasma-enhanced CVD induces a precipitous decline in mobility, falling from 2197 $cm^2 V^{-1} s^{-1}$ to 1290 $cm^2 V^{-1} s^{-1}$ – likely attributable to plasma-induced surface damage. In contrast, thermal CVD cause only a slight decrease in mobility – from 2198 $cm^2 V^{-1} s^{-1}$ to 2048 $cm^2 V^{-1} s^{-1}$ – indicating that the plasma-free process minimises surface damage and maintains uniformity. Taken together, the high electron mobility and the high



➤ Figure 4. RF power characteristics of the InAlGaN/GaN HEMT with SiN passivation using thermal CVD and plasma-enhanced CVD techniques. Load-pull measurements were conducted at 8 GHz under pulsed operation, employing a pulse width of 10 µs and a duty cycle of 1 percent to mitigate the effects of self-heating. Measurements involved a bias current of 10 mA mm^{-1} and a total gate width of 1 mm.

2DEG concentration realised by thermal CVD SiN_x passivation yield a sheet resistance of just 293 Ω/sq. Another encouraging finding is that InAlGaN remains thermally stable, even at 730°C.

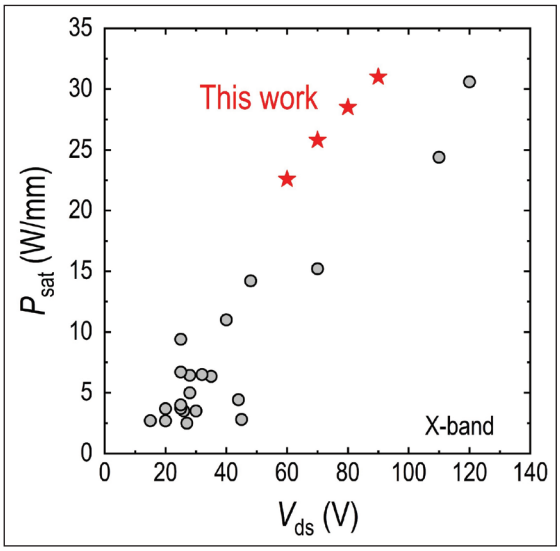
We have compared the transfer characteristics of our devices produced with different forms of CVD SiN_x passivation (see Figure 3). Threshold voltages are similar: -0.69 V for thermal CVD, versus -0.86 V for plasma-enhanced CVD. The maximum transconductance of our HEMTs produced using thermal CVD, rather than plasma-enhanced CVD, is higher – 600 mS mm^{-1}, compared with 504 mS mm^{-1} – and the maximum drain current is higher. We presume that this superiority is associated with a higher maximum drain current, due to a reduced on-resistance that results from enhanced mobility.

Another advantage of thermal CVD over its plasma-enhanced variant is that it provides a significant enhancement in breakdown performance, with the breakdown field increasing from 3.6 MV cm^{-1} to 5.9 MV cm^{-1}. The three-terminal off-state breakdown voltage also increases, rising from 169 V to 227 V. These findings demonstrate the efficacy of thermal CVD SiN_x passivation for enhancing the surface properties of InAlGaN/GaN HEMTs, and significantly improving their performance.

For practical devices, a strong performance must by accompanied by reliability. Judged on this font, our HEMTs excel, with thermal-CVD-based SiN_x passivation providing a substantial enhancement in device reliability

Outstanding RF output

As one would expect, the benefits of thermal CVD are also observed in the RF output characteristics of InAlGaN/GaN HEMTs. Measurements at 8 GHz show that switching from plasma-enhanced CVD to thermal CVD delivers a significant increase in output power and power-added efficiency (see Figure 4). At a drain voltage of 60 V, the device with thermal CVD SiN_x passivation realises a peak power-added efficiency of 53.9 percent, a linear gain of 12.1 dB, and a peak output power of 43.49 dBm. It is noteworthy that this device also supports high-voltage operation up to 90 V, significantly higher than the 60 V limit observed in the sample produced by plasma-enhanced CVD. As the drain-source voltage increases, the RF saturated output power density climbs steadily, ultimately attaining a power-added efficiency of 52.6 percent, a linear gain of 12.7 dB, and an output power of 44.91 dBm. This corresponds to an impressive power density of 31.0 W mm^{-1}, among the highest reported values for this category of device.



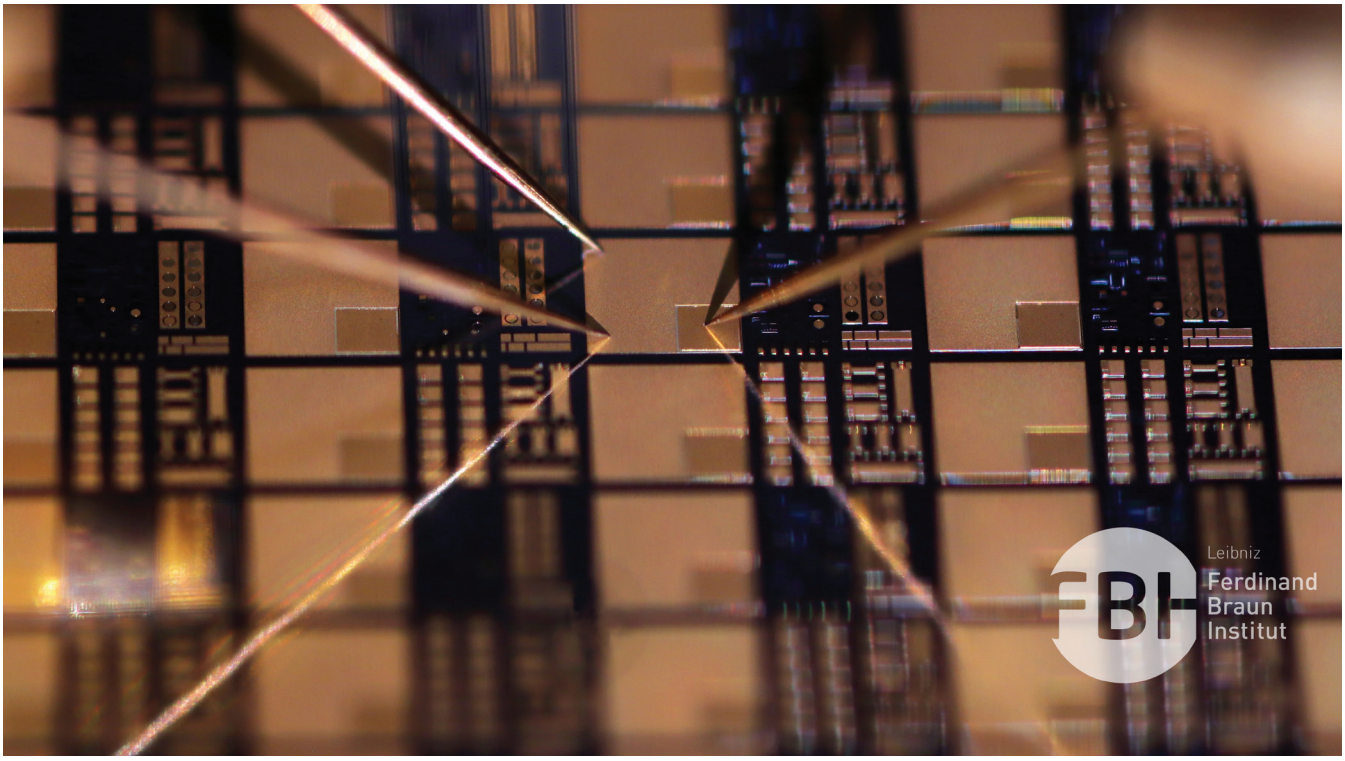
➤ Figure 5. Benchmark of the RF saturated output power densities (P_{sat}) versus the drain-source voltage (V_{ds}) of GaN-based HEMTs in the X-band.

For practical devices, a strong performance must by accompanied by reliability. Judged on this font, our HEMTs excel, with thermal-CVD-based SiN_x passivation providing a substantial enhancement in device reliability. Early-stage tests have determined that InAlGaN/GaN HEMTs produced with plasma-enhanced CVD SiN_x fail at a junction temperature of 307°C. In sharp contrast, devices protected with thermal-CVD SiN_x passivation demonstrate stable operation for over 900 hours under identical conditions. These findings indicate that InAlGaN/GaN HEMTs, produced using optimised thermal CVD SiN_x passivation, exceed conventional AlGaN/GaN devices in both performance and reliability, making them compelling candidates for broad commercial adoption and long-term implementation in demanding applications.

Moving forward, we will continue to refine our InAlGaN/GaN HEMT technology, which will be essential in meeting the demands of next-generation power and communication systems. These efforts will include further research into thermal stability and reliability under extreme conditions, work that will help accelerate commercial adoption of these devices. As our fabrication techniques continue to evolve, the potential for InAlGaN to redefine high-frequency electronics is becoming increasingly tangible.

FURTHER READING

- A. Yamada *et al.* "Electron mobility enhancement in metalorganic-vapor-phase-epitaxy-grown InAlN high-electron-mobility transistors by control of surface morphology of spacer layer," Jpn. J. Appl. Phys. **57** 01AD01 (2018).
- A. Yamada *et al.* "31 W/mm at 8 GHz in InAlGaN/GaN HEMT With Thermal CVD SiNx Passivation," IEEE Electron Device Lett. **45** 324 (2024).



HfO_2 for better GaN transistors

Introducing a HfO_2 gate dielectric improves the vertical GaN transistor, boosting its drain current density and its breakdown voltage

BY ENRICO BRUSATERRA, ELDAD BAHAT TREIDEL, PALLABI PAUL, MARTIN DAMIAN CUALLO, FRANK BRUNNER, INA OSTERMAY AND OLIVER HILT FROM THE FERDINAND-BRAUN-INSTITUT, BERLIN

THE LATERAL GaN HEMT is without doubt a great success, generating significant sales that will continue to climb to billions of dollars per annum by the end of this decade. But despite the ramping revenues, it's not the best geometry for this higher class of power device. The vertical architecture has the upper hand on a number of fronts, promising a higher breakdown voltage, a higher on-state current, a reduced resistance and a lower thermal impedance for a given chip size.

In addition to all these advantages, the vertical device has another valuable asset – it provides a normally-off behaviour, with a positive threshold voltage required to turn the transistor on. This characteristic is a mandatory requirement for safe, high-power operation.

Developers of vertical transistors tend to use gates that are either based on metal-oxide-semiconductors or junctions. Of these two, it's only a variant of the former, the inversion-type MOSFET, that provides a sufficiently high positive threshold voltage required for fail-safe normally-off operation, alongside a low gate leakage current necessary for stable operation in a noisy power-electronic environment.

Within the family of vertical GaN MOSFETs, those with a trench-gate architecture are the most common. A key merit of this design is that it allows the *p*-type GaN channel-layer to be formed by epitaxial growth, thereby avoiding the need for ion implantation of magnesium, followed by successive activation during the fabrication process. Such activation is not ideal, demanding lengthy annealing above 1300°C, a temperature so high that it already decomposes the GaN crystal. What's more, as the processing of the trench MOSFET does not require particularly high-resolution lithography, these transistors can be produced with a higher yield and a lower cost than other architectures, such as FinFETs.

One of the requirements for the gate module is that it has an electrical connection to all three epitaxial layers: drift, channel and source. To fulfil this requirement, a trench is etched into the epitaxial

stack prior to deposition of the gate dielectric and the gate metal.

When operating the trench MOSFET, electrons in the *p*-GaN layer, induced by a positive gate bias, form the transistor inversion-channel. During device processing, trench-etching damage may occur, slowing electron transport. Causes include interface roughness and the formation of defect states at the interface of the GaN and the gate dielectric at the trench side-walls. Due to this, channel electron mobility can be quite low.

An undesirable consequence of this state of affairs is that it's hard for trench MOSFETs to achieve channel mobilities and switching speeds as high as those in planar gate devices.

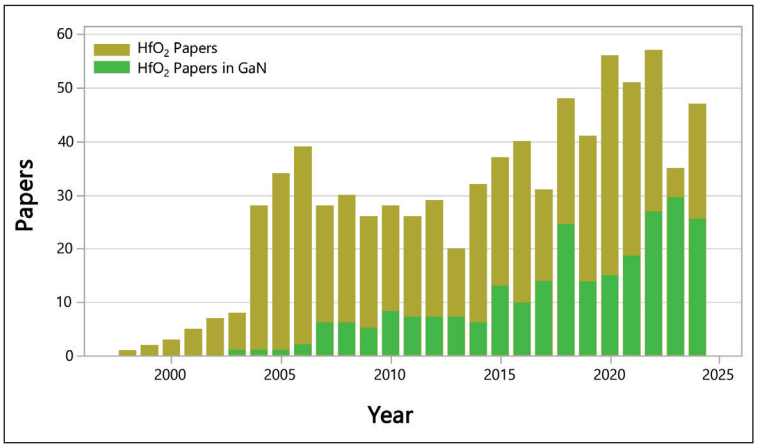
For engineers employing modern GaN-based semiconductor technology, there are two primary options for the gate dielectric of the trench MOSFET. For production purposes, SiO_2 is preferred, due to the higher throughput of low-pressure CVD machines; and for research and development, Al_2O_3 is the standard, as high-quality thin layers can be deposited with atomic layer deposition, and this oxide is a well-established high-κ dielectric in the semiconductor industry.

To improve the performance of the trench MOSFET, our team at Ferdinand-Braun-Institut, Berlin, is pioneering a new gate dielectric, consisting of a stack formed from HfO_2 and Al_2O_3. This pairing is designed to combine a high relative dielectric constant with a low interface trap density and the realisation of a small threshold voltage shift, as typically observed for pure Al_2O_3 layers. A high dielectric constant is very desirable, as it increases inversion charges in the *p*-type channel, as well as helping manage the electric field inside the gate trenches.

Selecting HfO_2 is not a surprising choice, given that this oxide has gained a growing popularity for GaN-based transistors (see Figure 1). Merits of HfO_2 include a very high relative dielectric constant of around 20, while still maintaining a high enough bandgap – it is around 5.4 eV – and, more importantly, a good band offset to both the GaN conduction (1.1 eV) and the valence (1.6 eV) band. HfO_2 is also a tried and tested material in the semiconductor industry, having been developed for silicon-based applications in DRAMs since 2007.

To ensure that we can work with this oxide in our standard trench MOSFET process line, we tested the material properties of HfO_2, and its stability to other process steps. This investigation determined that HfO_2 is stable up to 350°C, shows signs of decomposition at 500°C, and starts to crystallise at 550°C.

Based on these findings, we know the extent of the temperature budget available for all the process

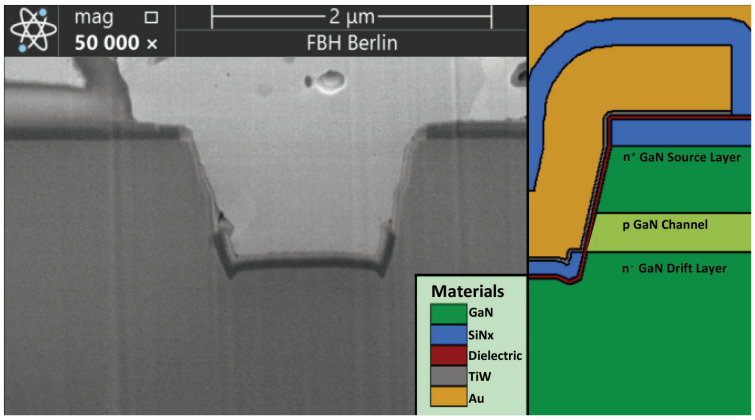


➤ Figure 1. Publication trend of the last 20 years on HfO_2 in general, and in combination with GaN.

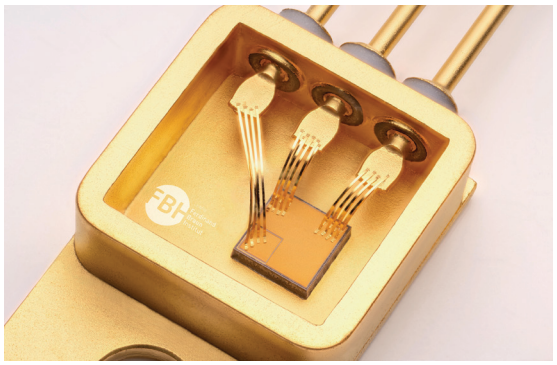
steps for transistor fabrication after oxide deposition. Another factor influencing oxide stability is the surface quality of GaN. We discovered that ammonia plasma-treated surfaces are more stable overall. In addition, plasma cleaning helps reduce oxygen impurities at the GaN surface, leading to improved electrical performance for the dielectric.

We have compared our new dual material dielectric with our standard gate technology that's based on just Al_2O_3. Our stacked oxide consists of 60 percent hafnium and 40 percent aluminium, a combination that provides a relative dielectric constant above 15 while maintaining a low interface trap density associated with the Al_2O_3 component of below 4×10^{12} cm^{-2}, and a high breakdown field provided by HfO_2 of 6.6 MV cm^{-1}. Another encouraging finding is that our combined oxide is more than twice as stable to voltage-induce stress as either just Al_2O_3 or just HfO_2. This robustness is especially beneficial for transistors, as exposing the gate to voltage stress may induce a shift in threshold voltage and ultimately instability during operation.

Our newly developed dielectric stack has been implemented in our standard trench-MOSFET process line. We have produced devices on 2-inch ammonothermally-grown bulk GaN substrates provided by the Institute of High-Pressure Physics of



➤ Figure 2. (left) An image of a multi-cell trench-MOSFET cross-section taken using focused ion beam (FIB). (Right) A device schematic diagram.



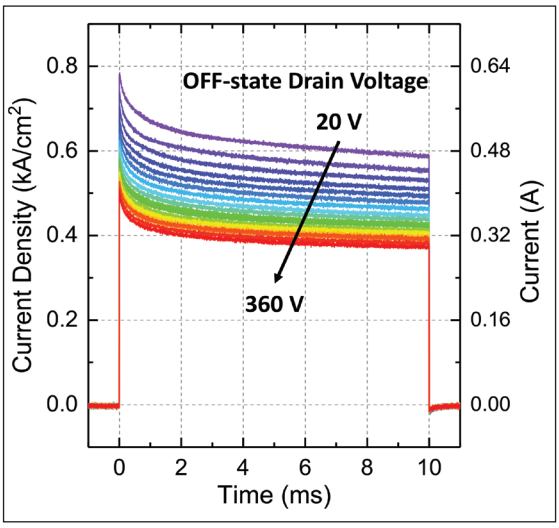
➤ Figure 3. Photo of a packaged trench MOSFET with 1800 mm gate periphery processed by the Ferdinand-Braun-Institut (FBH).

the Polish Academy of Science (for more details, see the papers listed in 'Further Reading'). The design of this trench MOSFET and details related to epitaxy are provided in Figure 2.

Electrical measurements on our trench MOSFETs with the novel stacked gate dielectric reveal that compared to that with a standard Al_2O_3 gate dielectric, forward current is up to three times higher, and there is a substantial reduction in the threshold-voltage shift induced by positive gate-bias stress. Another strength is the much higher channel mobility of 11.1 $cm^2 V^{-1} s^{-1}$. Thanks to this, on-state resistance falls by a factor of three, despite no apparent difference in accumulation capacitance or threshold voltage.

We explain these phenomena by considering that, for the same gate capacitance, the two different dielectrics are exposed to very different electric fields, given the different oxide thicknesses of 25 nm and 50 nm needed to maintain the same input capacitance. A lower electric field inevitably reduces trapping effects in the oxide. The diminished electric field that reduces interface trapping accounts for the superiority of our trench MOSFET with a gate that features both HfO_2 and Al_2O_3.

Incorporating HfO_2 into the gate stack increases the breakdown voltage of the gate modules. With HfO_2, a 50 nm-thick dielectric can handle up to 250 V, while the standard Al_2O_3-based dielectric only withstands 50 V over 25 nm. Our measurements have determined that the breakdown voltage of transistors that incorporate HfO_2 are 410 V. Testing our trench MOSFETs with the new gate dielectric under high-voltage switching conditions produces promising results (a photo one of these transistors, which have a large gate periphery of 1800 mm that's designed to deliver high currents, is shown in Figure 3). When stressing these devices under a high voltage in their off-state for 10 ms, we monitored the drain current after turn-on for another 10 ms (results are shown in Figure 4). Operating at an off-state drain bias of 360 V, on-state resistance degraded by only 50 percent, increasing from 16.7 mΩ cm^2 to 25.6 mΩ cm^2. Note that the correlation between the dynamic on-state resistance and off-state drain voltage is not typical degradation due to hot electrons (this is common in lateral GaN HEMTs, where current flows close to the surface and is sensitive to the presence of localised charges and defects).



➤ Figure 4. Dynamic switching characteristic of a trench MOSFET with HfO_2 gate dielectric. After 10 ms off-state stress with 20-360 V drain bias, the transistor is turned on by switching the gate bias from 0 V to 15 V. The on-state drain current is monitored for 10 ms at 10 V drain bias.

Following in-depth analysis, based on the degradation of the on-state resistance over time, we concluded that for low stress biases, the non-depleted part of the drift region interacts with the gate trench, showing a wide range of traps and defects. This situation differs for high stress biases. In this case, the portion of the drift region close to the trench is fully depleted, making interaction less likely. This suggests that the degradation of on-state resistance is related to the gate trench itself, and suggests that improving the dielectric interface to the GaN inside the trench can advance the switching performance of the trench MOSFET.

With interest in GaN power electronics increasing, and efforts at launching commercial vertical GaN transistors underway by both start-ups and established chipmakers, our efforts provide a timely development on how to improve the performance of these most promising of devices.

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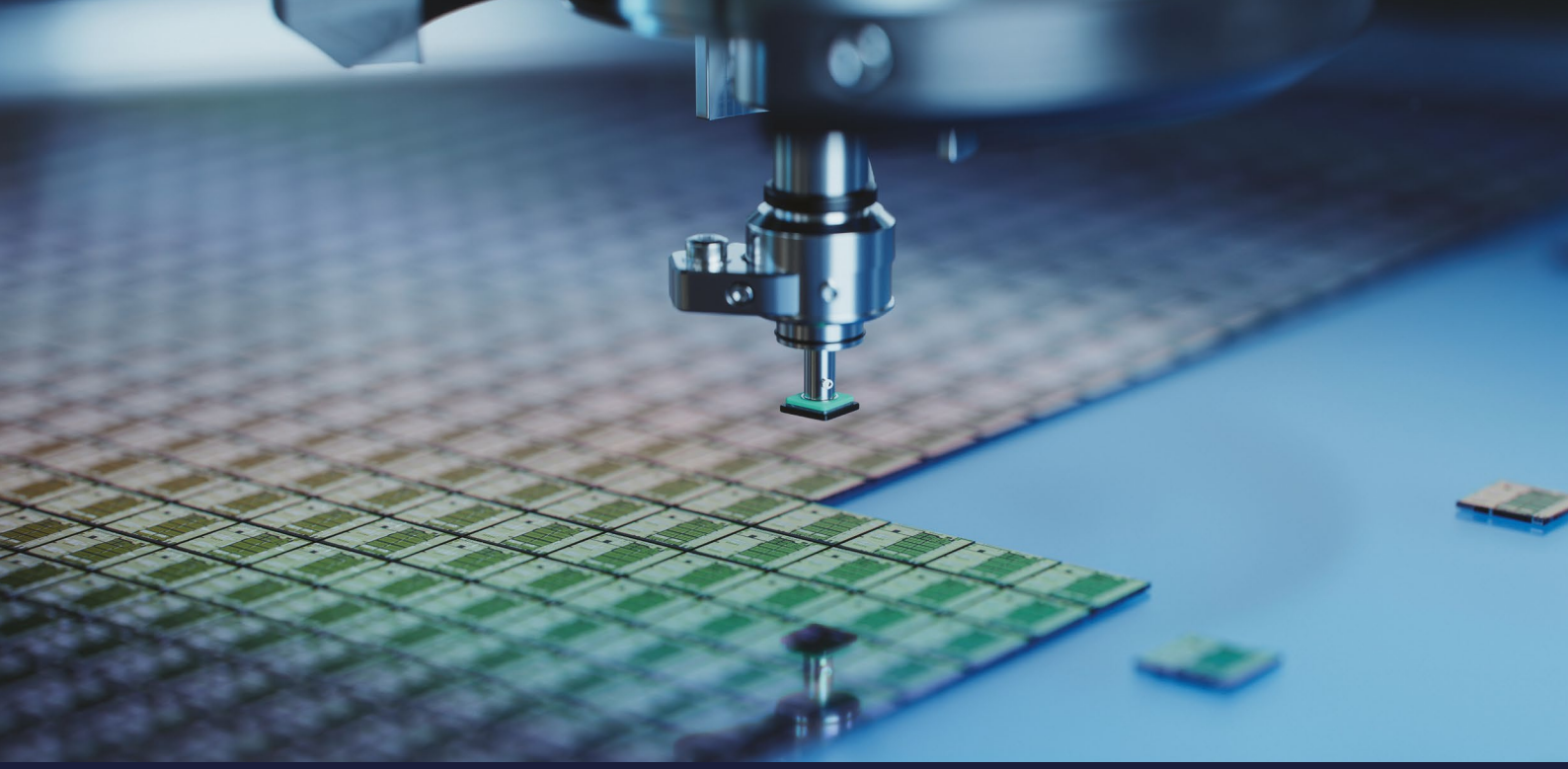

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Engineered substrates enhance high-voltage GaN power electronics

Substrates with a ceramic AlN core and a silicon top surface provide a promising platform for the production of high-voltage, fast-switching GaN devices and ICs

BY KAREN GEENS AND BENOIT BAKEROOT FROM IMEC

THINK of an application for SiC power electronics and you'll probably think of electric vehicles (EVs). After all, it's the battery-powered automobile that's driving the growth in sales of SiC MOSFETs, a trend that's forecast to continue throughout this decade and beyond. Employed in the traction inverter, these transistors tend to operate in systems operating at 400 V – but higher voltages, particularly 800 V, will be introduced over the coming years, a shift that moves towards the sweet spot of SiC. Commercial products associated with of this class of transistor span several hundred volts to a few kilovolts, with the well-established 1.2 kV MOSFET offering ideal headroom for EVs operating with 800 V power systems.

However, SiC is not the only wide-bandgap semiconductor with the attributes needed to make a compelling case for deployment in EVs. There's also GaN, which many are overlooking today for this application. This attractive alternative is already enjoying tremendous success at lower voltages, and is now the key component in fast chargers. Increasing the blocking voltage to 1 kV or beyond remains a challenge for fabrication of devices on large-area substrates. A possible route to success is turning to engineered substrates, an approach we are pioneering at the European microelectronics research centre, imec. Alternatives such as bulk GaN exist, though they come with smaller wafer diameters and significantly higher cost.

The GaN HEMT has a number of strengths, including a high critical-electric-field and a high electron-mobility, the latter realised in combination with very high density for the two-dimensional electron (2DEG) that's created at hetero-interfaces with other III-nitrides, such as AlGaN. In recent years, there has been significant improvement in the leading forms of this device, which include the enhancement-mode

(E-mode) lateral *p*-GaN gate HEMT and the cascode depletion-mode (D-mode) HEMT.

To realise high power levels in D-mode devices in a cascode configuration, engineers tend to direct their efforts at lowering the 2DEG channel resistance and increasing the electron channel mobility, steps that result in a very low on-resistance.

In comparison, the E-mode *p*-GaN gate HEMT has a higher 2DEG channel sheet resistance and thus a higher on-state resistance. However, this weakness must be weighed against a device architecture that allows a higher level of monolithic integration, thanks to the E-mode transistor ensuring a safe stand-alone operation and a simpler gate driving circuitry in many applications.

In addition to these advantages, the *p*-GaN gate HEMT stands out for its maturity and performance. That's why we have selected this particular device architecture for the first demonstrator for a 1200 V GaN switch, while exploring the potential of vertical GaN structures for future high-voltage applications.

Engineered foundations

To produce a switch that operates at such a high voltage demands a thicker epitaxial layer, which presents challenges in manufacturing. This is where Qromis Substrate Technology, often referred to as just QST, comes into play.

Qromis' commercially available, engineered substrates feature a ceramic AlN core that combines a high mechanical strength with close matching of the coefficient of thermal expansion of GaN and AlGaN layers. In addition to these features, the seed layer for the epitaxial growth of the GaN and Al(Ga)N layers remains well-known silicon, with a (111) crystal orientation.

This engineered platform provides a great foundation for the growth of thick, crack-free GaN stacks, significantly reducing the risk of wafer breakage, a common issue when using silicon substrates for growing thicker stacks targeting 1200 V, especially at larger diameters, such as 200 mm.

Using these proprietary substrates, we have fabricated lateral GaN power HEMTs with 9 μm-thick AlGaN buffer stacks that deliver excellent electrical performance. These devices have a hard breakdown voltage of over 1800 V, and a specific on-resistance of around just 5.8 mΩ cm^2.

Another asset of QST is its scalability. Applicable to 300 mm wafers, this technology is a major step forward for cost-effective, high-volume production. Migrating to larger wafers allows more devices per batch, helping to drive down manufacturing costs and accelerate the adoption of GaN in high-voltage markets.

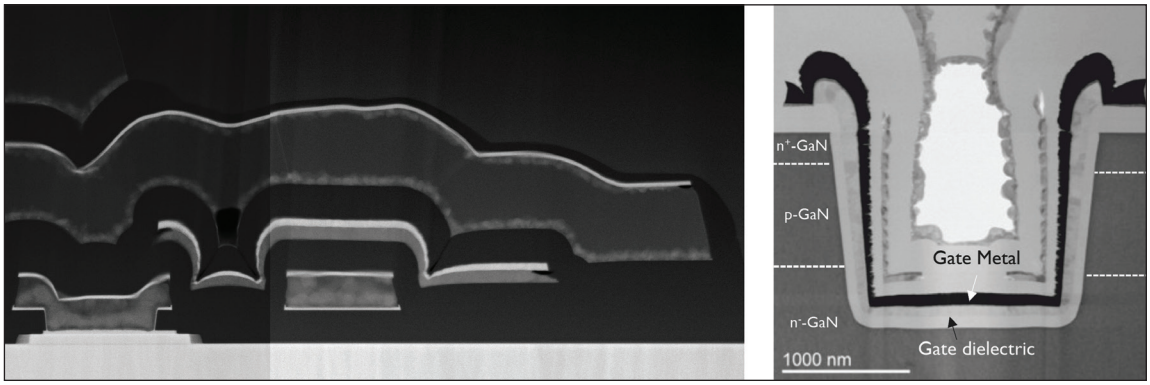
Vertical or lateral?

One key question when pursuing higher voltages, such as 1200 V or more, is this: which architecture, vertical or lateral, will offer a superior performance? With lateral GaN devices, all connections – that's the gate, the source, and the drain – are made to the front side. With this geometry, as voltage targets rise, the gate-to-drain distance has to increase to maintain safe operation. In addition, it's critical to lengthen the field plates – they are employed to distribute the high-voltage in the off-state, with source-connected field plates used to optimise the electric-field distribution (see Figure 1 (a)). Due to these requirements, the introduction of higher blocking voltages requires a larger footprint, and leads to a higher specific on-state resistance and larger capacitance, limiting efficiency and scalability.

To address these issues, a number of researchers, including ourselves, are investigating vertical GaN architectures. Unlike lateral devices, vertical structures distribute the high off-state voltage throughout the thickness of the epitaxial stack, rather than across its surface. Thanks to this, the device footprint remains compact, regardless of voltage rating – a noteworthy asset for high-voltage devices.

A key challenge associated with the development of vertical GaN devices is realising low defect densities in the epilayers. In GaN-based epitaxial stacks grown on foreign substrates – including silicon, employed in all commercially available GaN devices – the most common defects are one-dimensional (1D) dislocation lines perpendicular to the surface. In lateral devices, it appears that these dislocation lines do not have a significant impact on device operation and reliability. However, that's not the case for vertical devices, where current flow is inherently from bottom to top, and 1D defects interfere with vertical current flow. Due to this limitation, it's preferable to produce vertical devices using homoepitaxial growth on GaN substrates. But GaN substrates are expensive and limited in size, restricting commercial scalability. One possible avenue for further research involves investigations to understand the full extent of these 1D defects on the operation of vertical GaN devices, as well as determining what 1D defect level may be acceptable regarding device performance and reliability.

Using QST substrates for vertical device development, we have grown thick, high-quality *n*-type GaN drift layers on 200 mm wafers, paving the way for manufacturable vertical GaN devices.



➤ Figure 1: Cross-section STEM of (a) the *p*-GaN gate architecture used in lateral devices and (b) the trench gate MOS architecture used in vertical devices.

We have produced epitaxial stacks with a thickness exceeding 11 µm on this engineered foundation, enabling robust device performance.

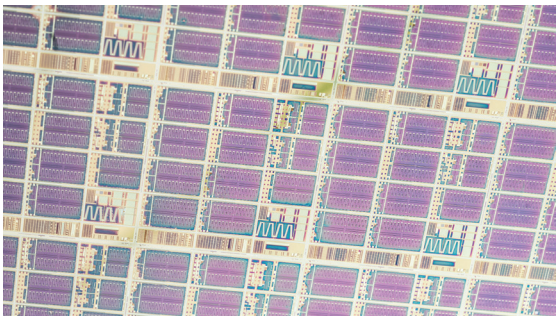
We have processed these epiwafers into semi-vertical trench gate MOSFETs. When these devices are in the on-state there's an electron inversion channel in a *p*-type GaN layer, similar to traditional MOSFETs, albeit at the sidewall of the trench MOS gate. During device operation, electrons flow from the source n^+-GaN layer through the electron inversion channel towards the deeper drift layer, before they are transported into a buried n^+ layer at the bottom of the structure. We use a drain metal contact from the frontside towards the buried n^+-GaN layer to collect these electrons.

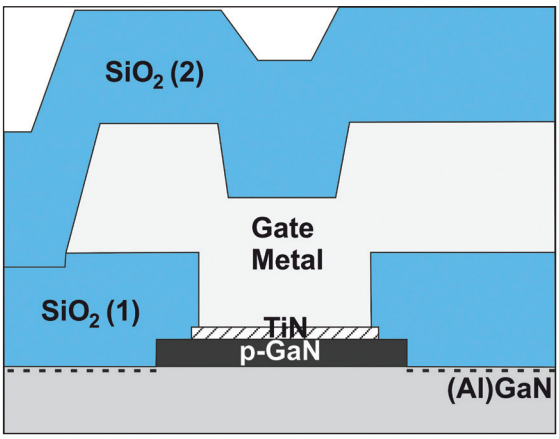
Vertical GaN devices are emerging as a promising direction for future high-voltage power electronics, attracting significant research interest worldwide. Although still in an exploratory stage, this technology holds potential to overcome key limitations of conventional lateral architectures.

GaN ICs on chip

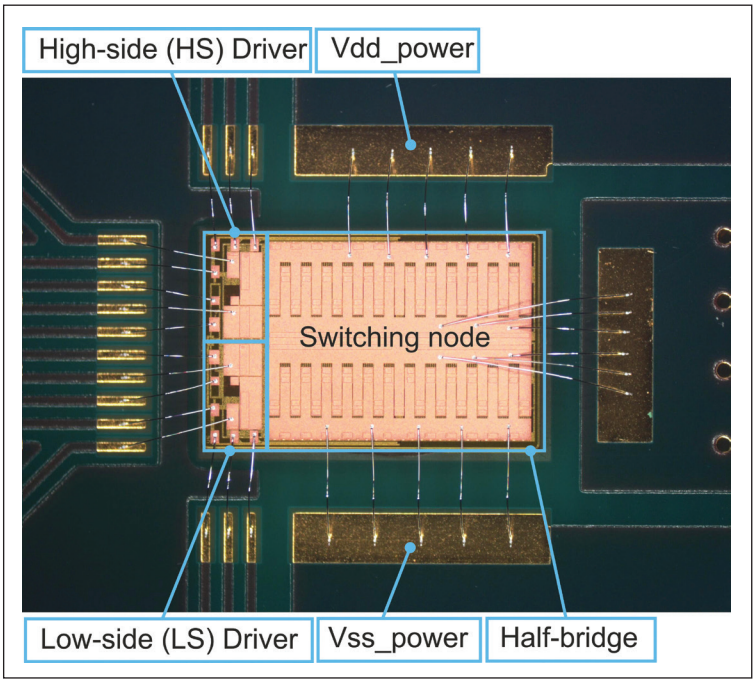
Today, most GaN-based power systems are built from multiple discrete chips, assembled on a printed circuit board. While this modular approach is effective, it introduces parasitic inductances – they are unwanted electrical effects that can degrade performance, especially in fast-switching applications.

A promising route to truly harnessing the speed and efficiency of GaN is monolithic integration – that's the bringing together of multiple power devices and control circuits on a single chip. GaN power ICs are already finding their way into power supplies, motor drives, and converters, offering compact, high-performance solutions.





➤ Figure 3: Image of fabricated GaN-ICs, along with test structures, on 200 mm QST substrate.



➤ Figure 2: Example of 650 V GaN-on-QST monolithic IC, depicting a symmetrical 140 mm half-bridge with integrated driver and level shifters.

One of the key advantages that comes from forming a GaN IC through the on-chip integration of multiple GaN power HEMTs and accompanying control circuitry is a dramatically reduction in parasitic inductance. This enables faster, more-efficient switching. At the heart of these ICs are lateral *p*-GaN HEMT power arrays, serving as core switching elements.

To further enhance performance and reliability, we are combining a GaN-on-SOI (silicon-on-insulator) technology with trench isolation to ensure galvanic isolation between switches on the same chip. This design helps prevent electrical interference and enables stable operation at high voltages.

One of our critical innovations is the use of a local deep contact to the top silicon layer in the SOI substrate, which is connected (shorted on chip) to the source. This prevents back-gating effects – a condition that threatens to disrupt switch performance, especially in integrated half-bridge configurations, where the high-side switch might otherwise fail.

It's worth noting that QST substrates, which share similarities with SOI in terms of structure and

insulation, also support this technology platform. We have successfully demonstrated monolithically integrated GaN ICs on both SOI and QST substrates, with voltage ratings up to 650 V.

These integrated circuits are not limited to just power switches, and can also include gate drivers, control and protection logic, and even sensing functions, such as temperature monitoring – all on the same chip. This level of integration paves the way for smarter, more compact, and more efficient power systems, ideal for everything from consumer electronics to industrial automation.

The work on the fabrication of GaN ICs both on SOI and QST received funding from the ECSEL Joint Undertaking (JU) HiEFFICIENT project under grant agreement no. 101007281. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Spain, Belgium, Germany, Slovakia, Italy, Netherlands, and Slovenia. This work also received funding from the ALL2GaN Project for the development of lateral HEMT devices on QST for 1200 V (Grant Agreement No 101111890), and has been supported by the Chips Joint Undertaking and its members including the top-up funding by Austria, Belgium, Czech Republic, Denmark, Germany, Greece, Netherlands, Norway, Slovakia, Spain, Sweden and Switzerland. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the national granting authorities. Neither the European Union nor the national granting authorities can be held responsible for them.

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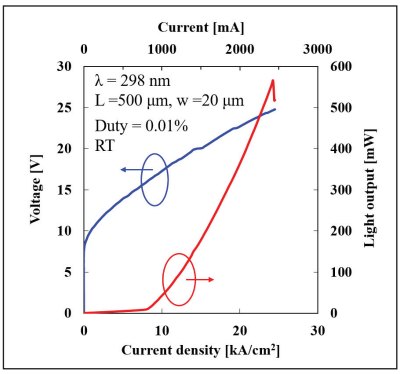
Building better UVB lasers

Superior carrier injection and an aluminium-content-drop architecture improve the performance of lasers operating at around 300 nm

A JAPANESE collaboration dominated by engineers from Meijo University claims to have delivered significances advances in the performance of lasers operating in the UVB.

Strengths of the team's devices, which span 298 nm to 319 nm, include an injection efficiency between 42 percent and 52 percent – that's more than a threefold increase over previous polarisation-doped UV laser diodes – and a peak optical output power of 570 mW.

According to lead author of the paper detailing this work, Takumu Saito, this level of performance is close to that required for some applications employing lasers operating in pulsed mode, such as spectroscopy and fluorescence excitation. "In addition, we have recently achieved continuous-wave lasing in a closely related UVB laser diode structure," says Saito. These results, currently under review, are regarded as another important milestone toward real-world applications.



➤ Operating in pulsed mode, UVB lasers deliver an output power of more than 500 mW.

However, Saito says that further improvements to the performance of UVB lasers are needed if these sources are to serve in a broader range of applications. Internal optical loss must fall to just 30–50 cm^{-1}, the lasers must not exceed a catastrophic optical damage threshold, and there's need to address challenges associated with thermal management, continuous-wave stability, device lifetime, and process yield.

The performance of deep-UV laser diodes is held back by the aluminium-rich cladding layers, which fail to combine a low resistivity with a high hole concentration. Due to this, it's extremely difficult to realise efficient carrier injection, and thus stable laser operation.

To address this weakness, many developers of UVB and UVC lasers turn to polarisation doping, with linear grading of the AlN molar fraction in the *p*-type cladding facilitating a supply of holes. However, this benefit comes at the expense of a lower carrier injection efficiency – it is typically around just 15 percent for UVB laser diodes. Behind the low carrier-injection efficiency is excessive electron leakage, stemming from strong fixed polarisation charges formed at the AlN molar fraction discontinuity between the electron-blocking layer and the *p*-side waveguide layer. These charges are a menace, diminishing the effective electron barrier height and leading to electron overflow that hampers the electron injection efficiency.

A promising solution to this issue is an 'aluminium-content-drop' scheme, involving an intentional reduction in the AlN mole fraction of the *p*-AlGaN layer next to the electron-blocking layer. However, the success of this approach can be thwarted by unintentional diffusion of aluminium and gallium atoms at heterointerfaces, leading to compositional smearing and degraded interfacial abruptness.

Simulations and material studies suggest that low-temperature MBE can tackle these concerns. Building on this, Saito and co-workers have taken the next step, producing four UVB laser diodes with multiple cavity lengths that demonstrate that breakthroughs can result from this approach.

Efforts began sputtering an AlN buffer layer onto sapphire, improving crystallinity with face-to-face annealing, adding an AlN template by MOCVD, and defining AlN nanopillars by nanoimprint lithography and etching. Overgrowth of unintentionally doped $Al_{0.68}Ga_{0.32}N$ created a high-quality, relaxed AlGaN template. On this platform the team added an MBE-grown laser structure featuring a first *p*-type AlGaN cladding layer using unintentional polarisation doping and a second *p*-type AlGaN layer that combines magnesium and polarisation doping. All epilayers from the *n*-side waveguide onwards were grown at 800°C or less, to preserve abrupt heterointerfaces and ensure high optical gain at low excitation carrier densities.

Saito and co-workers produced lasers with cavity lengths from 100 μm to 1000 μm and optical losses ranging from 49 cm^{-1} to 29 cm^{-1}. These high values are expected to stem from crystal imperfections, impurity incorporation and scattering from dislocations induced during low-temperature growth.

Goals for the future include optimising crystal quality and reducing optical loss by improving layer thickness control.

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Advancing Ga_2O_3 diodes with copper anodes

Copper anodes are enabling Schottky diodes to deliver an impressive performance while offering robust thermal reliability

ENGINEERS from China are claiming to have delivered a significant advancement in the performance of β-Ga_2O_3 power rectifiers through the introduction of copper anodes.

According to the spokesman for the team, Xiaohui Wang from Southern University of Science and Technology, by integrating a Cu_2O/Ga_2O_3 heterojunction with a low work-function copper anode, this collaboration has produced a diode that combines a turn-on voltage of less than a volt with a breakdown voltage beyond 2 kV. The result is a leading figure-of-merit for power devices.

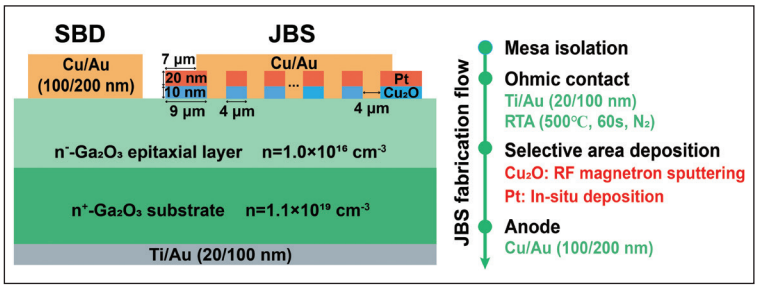
Another feature of this device, produced by a partnership involving researchers at Southern University of Science and Technology, Peng Chen Laboratory, The University of Hong Kong and Shenzhen Polytechnic University, is its enhanced field control. It is said that the highly doped *p*-Cu_2O layer and the Cu_2O-based junction termination extension effectively redistribute the electric field and suppress peak electric field crowding. According to Wang, these breakthroughs have played a key role in establishing a new material platform and design strategy beyond conventional NiO/Ga_2O_3 heterojunction barrier Schottky diode structures.

Wang and co-workers are not the first to try and improve NiO/Ga_2O_3 by turning to Cu_2O, an alternative that helps to excel on two key fronts: a high blocking voltage and a low forward voltage. Previous success has been reported by engineers at NCT, producing an ampere-class large-area diode that's optimised for high current density and switching performance.

"Our work introduces a low work-function copper anode with an *in-situ* platinum layer to form an optimised *p*-contact to copper oxide," explains Wang, who points out that the device from NCT, featuring nickel contacts and produced using a lift-off trench-filling Cu_2O process, has significantly higher values for on-voltage and specific on-resistance.

Another strength of the device produced by the team from China is a result of its optimised planar *p*-Cu_2O ring, which suppresses electric-field crowding and shifts the peak electric field into the drift region.

Efforts by Wang and co-workers have not been restricted to device design, and include the fabrication process: "Our device benefits from rigorous interface engineering, including copper oxide with a high hole concentration, an *in-situ* platinum contact and surface preparation. These processes lead to lower leakage, a more uniform electric field distribution, and superior thermal/electrical reliability."



➤ Schottky barrier diodes (SBDs) and heterojunction barrier Schottky diodes (JBSs) benefit from a highly doped *p*-Cu_2O layer and a Cu_2O-based junction termination extension.

Devices have been produced by processing epiwafers, featuring a 10 μm-thick silicon-doped drift layer on a heavily tin-doped native substrate, into Schottky barrier diodes and heterojunction barrier Schottky diodes (see Figure for details). Characterisation of the latter determined a turn-on voltage of 0.83 V, a breakdown voltage of 2345 V, and a figure-of-merit for power of 1.22 GW cm^{-2}.

Efforts have also been directed at evaluating long-term reliability. Operating under a 200 V reverse-bias stress at 425 K for 10,000 s produced negligible degradation in dynamic on-resistance and on-voltage. "Combined with a trap-related mechanism analysis, these results offer critical experimental evidence for the practical deployment of gallium oxide devices in high-temperature, high-voltage applications," argues Wang.

One of the team's goals is to improve heterojunction quality through a combination of controlled oxidation, refined surface treatment, and alternative deposition strategies.

"These efforts are expected to suppress interface trap density, enhance carrier transport uniformity, and further reduce leakage and barrier inhomogeneity," says Wang.

There are also plans to: increase the breakdown voltage while maintaining the low specific on-resistance of 4.5 mΩ cm^2, a goal that will be pursued by introducing either multi-zone junction termination extension, field plates, or hybrid termination structures; and to explore the on-chip integration of the team's diodes, by using surge-protection devices, field-control components, and high-voltage rectifiers.

REFERENCE
➤ X. Wang *et al*. Appl. Phys. Lett. **127** 212102 (2025)

Improving MBE for GaN power devices

Dividing the growth of a channel into a dozen layers boosts the blocking voltage of MBE-grown GaN HEMTs

A TEAM from China has strengthened the case for manufacturing GaN HEMTs by plasma-assisted MBE by producing simple devices that can block more than 2.5 kV.

While MOCVD dominates the manufacture of GaN HEMTs for power electronics, there are a number of benefits associated with plasma-assisted MBE.

One of the strengths of this class of epitaxy is that it is capable of producing an insulating buffer without the need for doping. Avoiding doping is a significant asset, as it eliminates current collapse when switching GaN HEMTs between their on and off states.

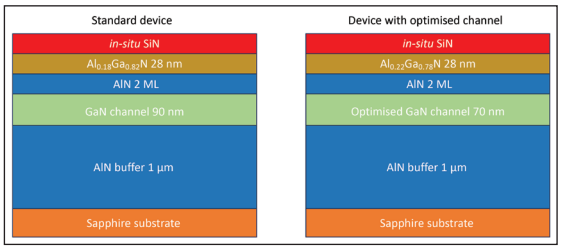
Another advantage of plasma-assisted MBE is the suppression of background impurities and defects, thanks to growth under ultra-high vacuum.

Exploiting these assets, the team from Massphoton, Suzhou Powerhouse Electronics Technology, and Suzhou Institute of Nano-Tech and Nano-Bionics, have produced GaN HEMTs that feature a 70 nm-thick channel produced with a novel growth scheme.

To form this device, the team divides the growth of the channel into 12 layers and employs a gallium droplet depletion treatment. This approach is said to enhance the quality of the GaN channel, due to fewer defect states and a lower pore defect density.

Fabrication of the HEMTs began by loading a 3-inch sapphire substrate with a 2° off-cut into a plasma-assisted MBE chamber and depositing a 1000 nm-thick AlN buffer at 920°C, followed by growth of the 70 nm-thick GaN channel, two monolayers of AlN and a 28 nm-thick layer of $Al_{0.22}Ga_{0.78}N$, all at 815°C. After growing this III-N stack, the team added, *in situ*, a 10 nm-thick SiN passivation layer. In addition, the team produced a control device with a slightly thicker channel (see Figure for details).

Processing these epiwafers into devices began with the deposition of a 30 nm-thick SiN layer by low-pressure CVD, followed by nitrogen implantation to realise mesa isolation, and the addition and annealing of source and drain ohmic contacts. After the growth of a 150 nm-thick layer of SiN, gate windows with a recess depth of 120 nm were defined, to leave 30 nm of SiN as the gate insulator. Deposition of Ti/Al/Ti followed, creating a gate metal and field plate, prior to the addition of interconnects and deposition of a 2 μm-thick SiN top passivation layer.



➤ A superior channel improves the HEMT's blocking voltage, leakage current and on-off ratio.

Electrical measurements using the transmission line method determined a contact resistance of 3.6 Ω mm and a sheet resistance for the wafer of 491 Ω sq^{-1}. Meanwhile, Hall measurements provided values for the two-dimensional electron gas density of 1.07 x 10^{13} cm^{-2} and the field-effect mobility of 884 cm^2 V^{-1} s^{-1}, suggesting a sheet resistance of 660 Ω sq^{-1}. The engineers attribute a discrepancy between values for sheet resistance obtained from different measurements to a buffer layer below the GaN channel that's not sufficiently insulating and leads to parasitic conduction.

It's claimed that improving the growth conditions of the buffer layer would reduce the sheet resistance and enable a thicker channel layer.

Transfer measurements of the GaN HEMT featuring modified channel growth show current saturation in the output characteristics. This characteristic, not observed in a control device with a conventional channel, is attributed to the superior channel produced with subdivided layers.

Additional benefits associated with the superior channel include an increase in the on-off ratio to 10^7 and a reduction in the drain leakage current at a drain bias of 0.5 V to 1 nA mm^{-1} – in both cases, there is an order-of magnitude improvement over the HEMT with the conventional channel.

Both forms of HEMT have a relatively high on-resistance, due to the thin GaN channel thickness.

According to the team, increasing the channel thickness will help to reduce the on-resistance, which can also fall by introducing a graded layer and improving the growth process.

The control device breaks down at 1000 V, while the HEMT with the superior channel can withstand around 2500 V. The team speculates that the far higher value stems from the superior insulating properties of the GaN channel.

REFERENCE
➤ Z. Yang *et al*. Appl. Phys. Express **18** 114001 (2025)

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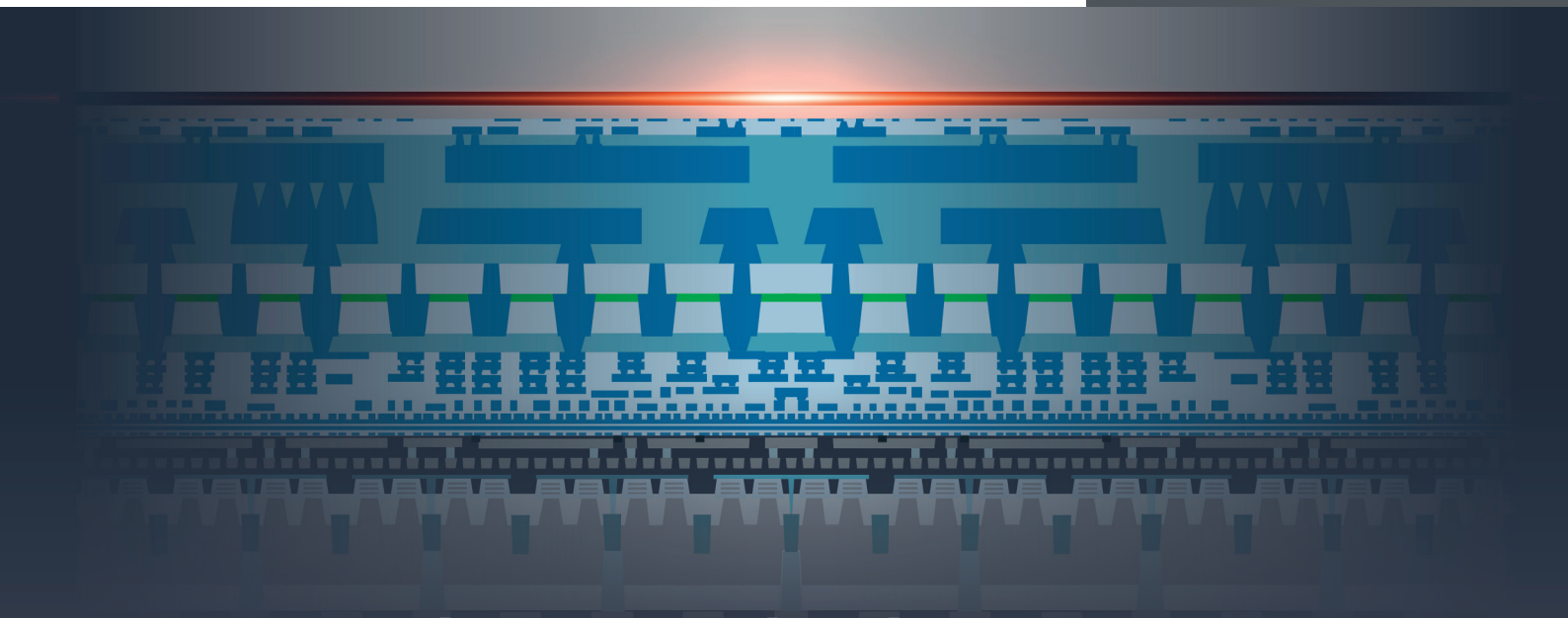

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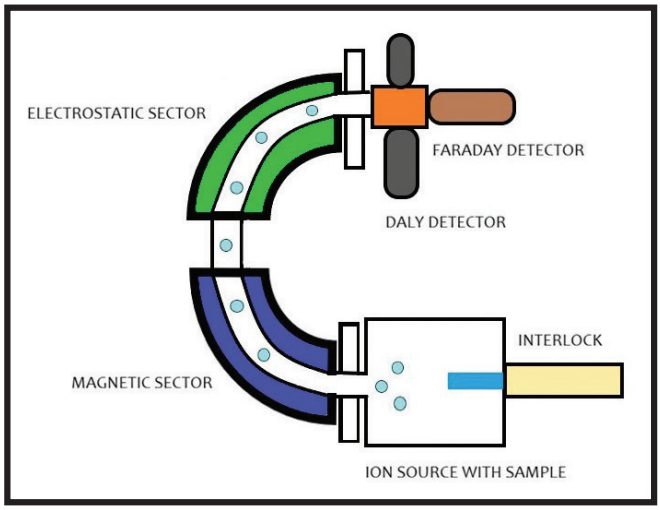

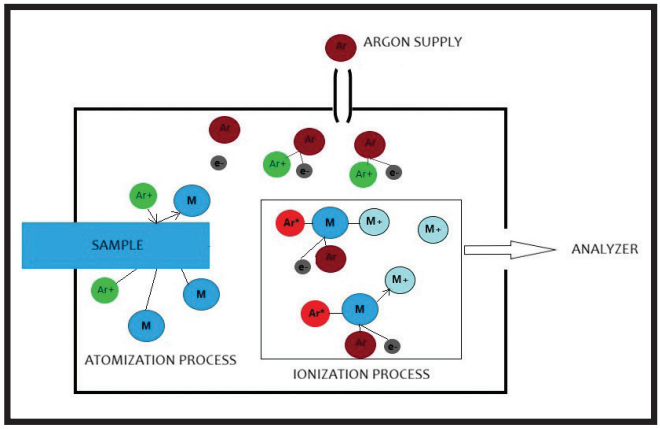

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