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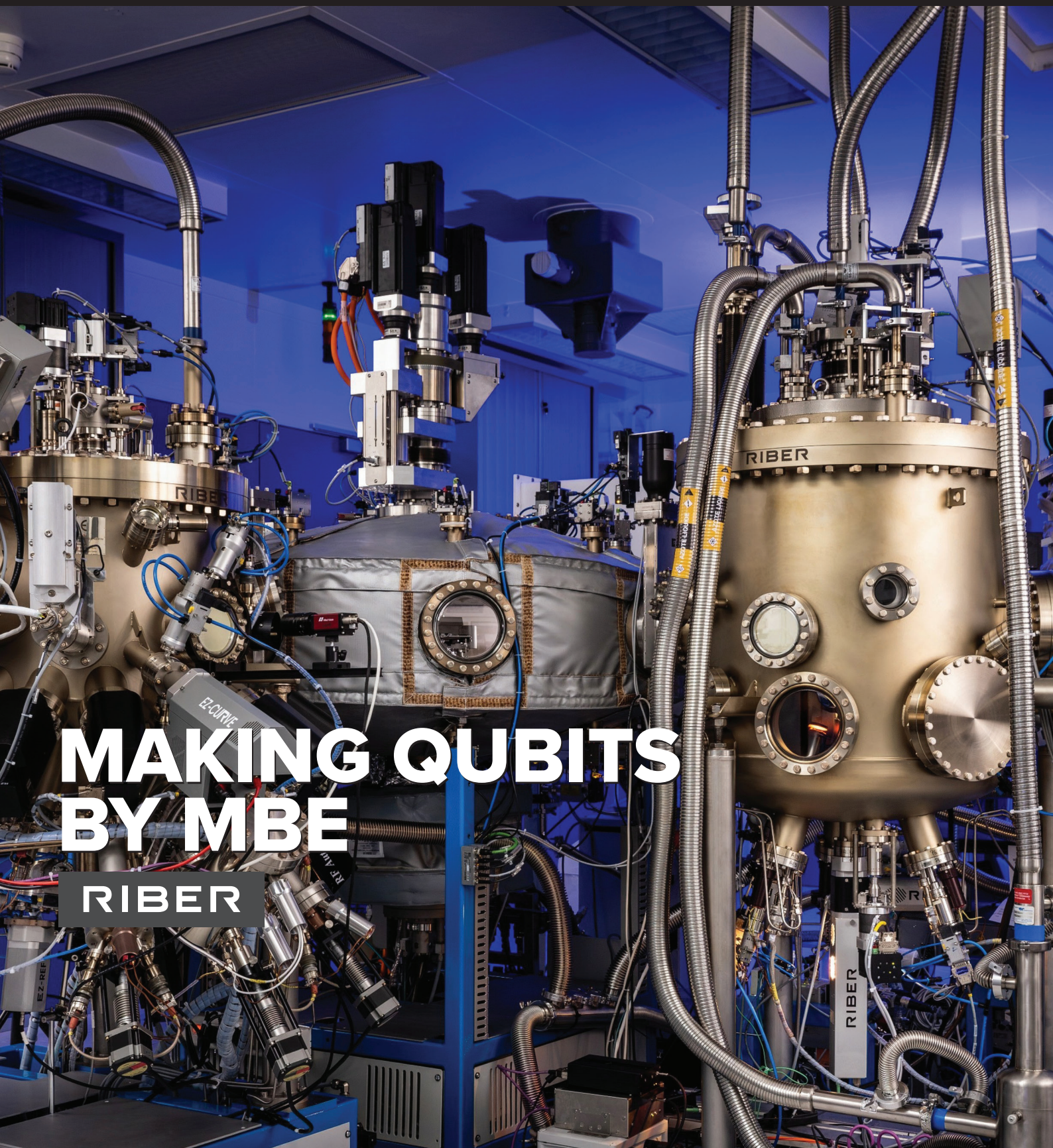

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

The best stories

AS EDITOR of *Compound Semiconductor,* I perform a number of enjoyable roles.

Most of my time is spent commissioning and editing features. This offers the opportunity to delve into the details of new technologies, and to work with authors on producing informative, engaging copy.

Another regular task is to pick papers for each issue's Research Review, before asking a handful of questions to the researchers, and then trying to provide an accurate, enjoyable synopsis of their breakthroughs.

While both these elements of my work are pleasurable, nothing beats writing up an interview. Ideally this involves a visit to a company or a lab, but it's more common to have a conversation over a virtual platform.

Of all the interviews I've been conducting over the last twenty years and more, the highlights are those with start-ups. The obvious attraction is the chance to hear a first-hand account of a fascinating, potentially ground-breaking technology. But there's also the personal story: Who invented this novel tech? How did the founders meet? And how did they get to where they are today?

Start-ups tend to emerge from university research groups, with entrepreneurial post-graduates founding companies, enthused by the chance to create great tech and make a mark. Often, they'll be joined be an industry veteran, who has the contacts and knowhow to raise funds, and a strong background in navigating the challenging transition from promising lab devices to a commercial product.

But that's not the only way that start-ups emerge. In this edition, you can read about a notably different beginning, based on a consultant with idea for cooling all forms of chip.

This is the story of the founding of CoolSem, a Dutch start-up led by CEO and CTO André van Geelen (see p. 14). After completing his PhD in the 1990s at Radboud University, where he developed the knowhow for wafer-scale removal of a substrate from its epilayers, van Geelen went into industry, working for a number high-profile companies. Then, in 2015, he switched to offering consultancy services to start-ups.

During this time, van Geelen devised a novel, elegant solution to chip heating. His idea is to remove the substrate, either by epitaxial lift-off or grinding and polishing, and in its place add a composite with an exceptionally low thermal resistance.

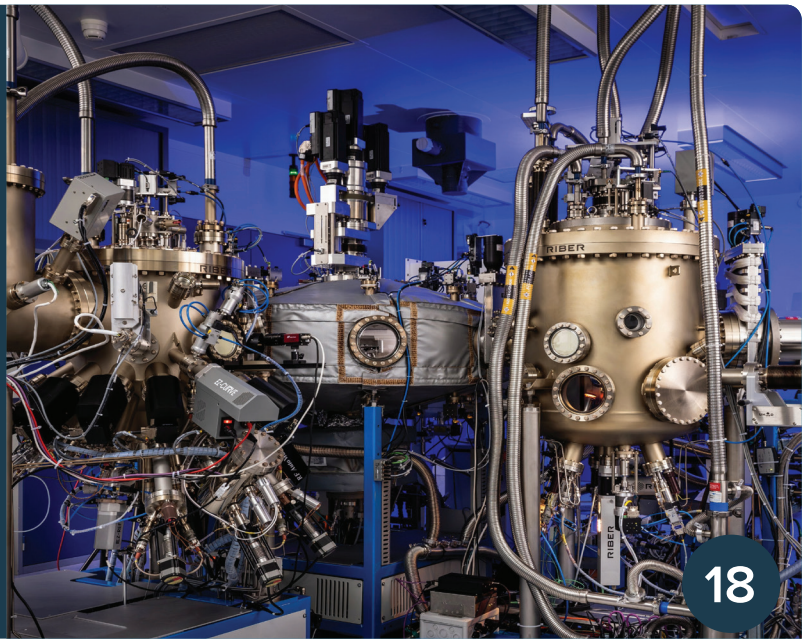
Pursuing this goal is a team that's grown to around ten, and plans to demonstrate this technology to customers this June. It's the start of a fascinating journey that could aid the performance of lasers, and RF and power devices, so we'll definitely be tracking the progress of CoolSem through the pages of this magazine.

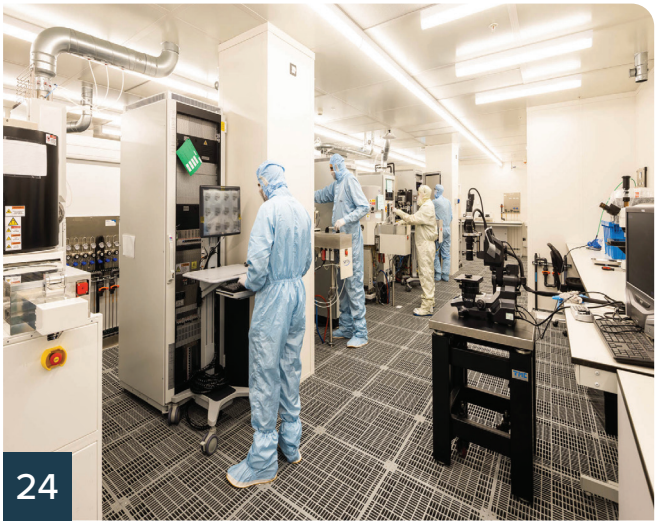
CS COMPOUND SEMICONDUCTOR

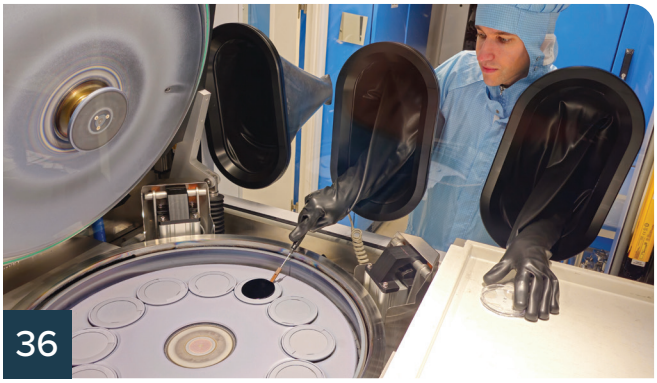
COVER STORY

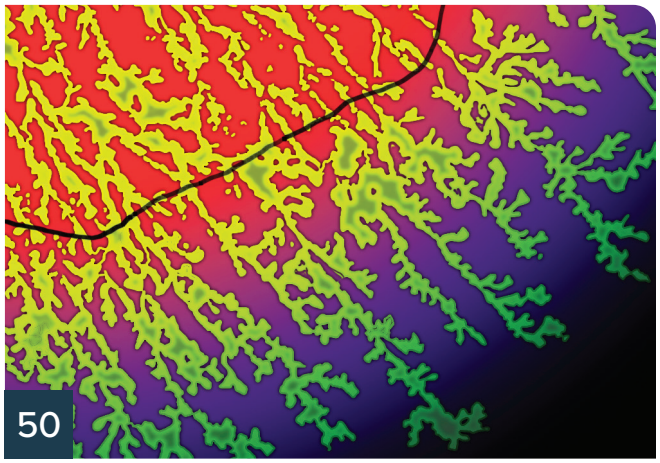
Making qubits by MBE

MBE excels in the growth of structures for quantum computing that combine layers of semiconductors and superconductors

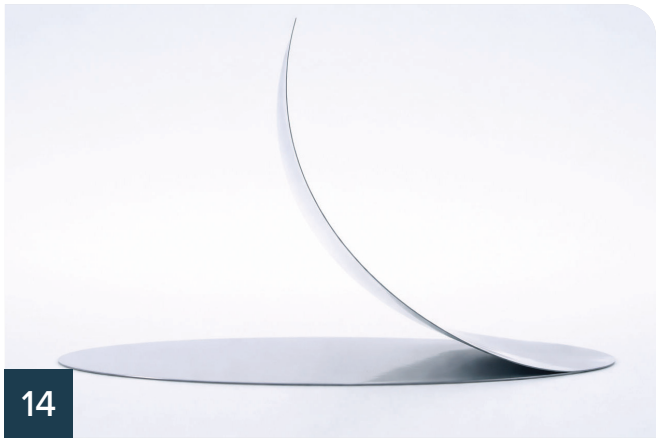






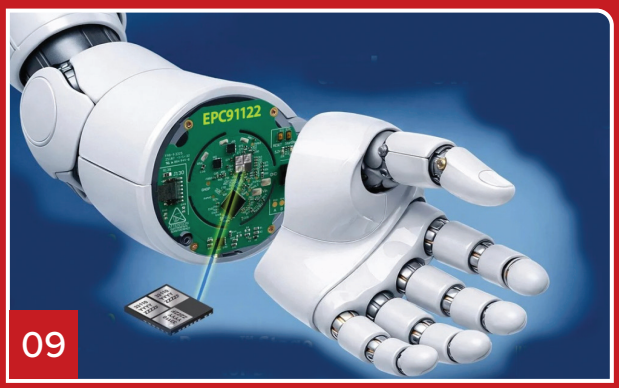


NEWS ANALYSIS



RESEARCH REVIEW

NEWS



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Compound semis enter new growth phase

With 14 percent CAGR through 2031, compound semis are becoming the core to power electronics, photonics, and AI infrastructure, says Yole

YOLE GROUP has announced the release of its annual market & technology report, *Status of the Compound Semiconductor Industry 2026 – Focus on Substrates and Epiwafers*, highlighting sustained structural growth through 2031.

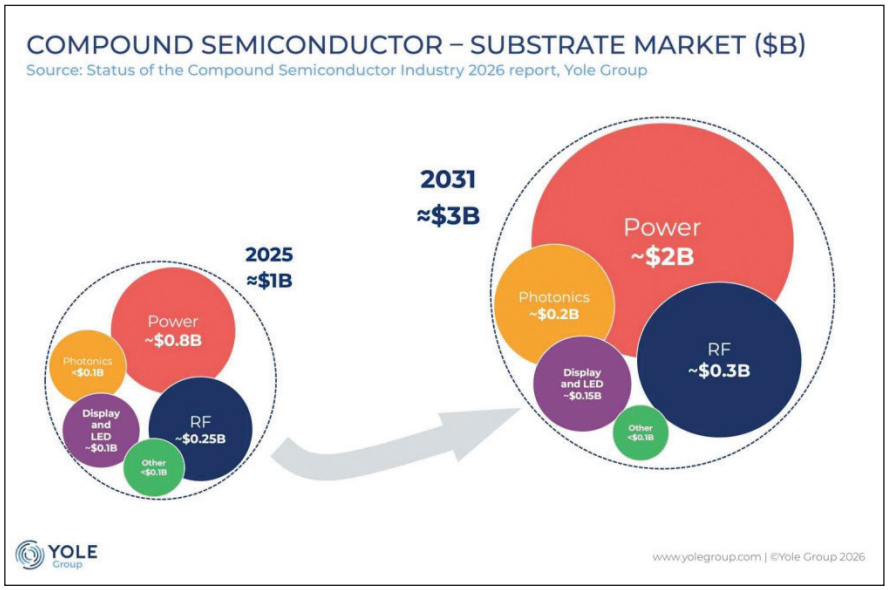
The report says that despite short-term pricing pressure in certain segments, electrification, AI infrastructure expansion and next-generation connectivity are reinforcing long-term demand for compound semiconductor materials, including SiC, GaN, GaAs, and InP.

The combined compound semiconductor substrate and open epiwafer markets are projected to grow to more than $5 billion in 2031, reflecting a CAGR of about 14 percent between 2025 and 2031.

Ahmad Abbas, technology and market analyst for compound semiconductors at Yole Group, said: “Power SiC continues to anchor market expansion. What is particularly notable is the diversification of growth. In this new edition, we see this industry becoming structurally stronger and more balanced.”

Poshun Chiu, principal analyst for compound semiconductors at Yole Group commented: “In this edition, we would also like to highlight the key role of AI. Without doubt, AI is reshaping the overall compound semiconductor supply chain: from SiC enabling efficient power delivery in data centres to InP supporting high-speed optical interconnects, compound materials are becoming essential to scalable AI infrastructure.”

The adoption of compound semiconductors is accelerating thanks to their clear performance advantages. At Yole Group, analysts are closely monitoring this shift across diverse market segments.



Power electronics remains the dominant growth engine. *n*-type SiC substrates alone are expected to surpass $2 billion by 2031, supported by electric vehicle adoption, 800 V architectures, onboard chargers, renewable energy systems, and industrial electrification. The transition from 6-inch to 8-inch wafers is accelerating cost reduction and scaling efforts, reinforcing SiC’s long-term competitiveness despite recent pricing pressure linked to overcapacity and the normalisation of automotive demand.

Power GaN continues expanding beyond consumer fast charging into automotive and data-centre applications, strengthening its strategic position as a complementary power technology.

> *n*-type SiC substrates alone are expected to surpass $2 billion by 2031

In RF markets, GaAs maintains leadership in handset front-end modules, while GaN progresses in telecom infrastructure and defense applications, with long-term prospects in 6G deployment.

Photonics represents the most dynamic segment. InP substrates are forecast to grow at more than 18 percent CAGR through 2031, driven by AI data centres, high-speed optical transceivers, and co-packaged optics architectures. The transition to 6-inch InP platforms supports both performance scaling and manufacturing efficiency. Meanwhile, LEDs remain mature, and microLED adoption progresses gradually, beginning with high-end wearable and display applications.

To explore these market and technology dynamics, Yole Group will address compound semiconductor trends during briefing sessions at upcoming industry events including OFC and Semicon China.

UK-Bulgaria partnership to deliver SiC factory

£350 million project will use the expertise of Scottish SiC specialist Clas-SiC

THE UK Government's Science and Technology Network (STN) has facilitated the development of a €350 million investment Green SiC wafer factory in Bulgaria, delivering £10.5 million UK export wins and advancing next-generation materials.

Scottish SiC specialist Clas-SiC has signed an early engagement with the project.

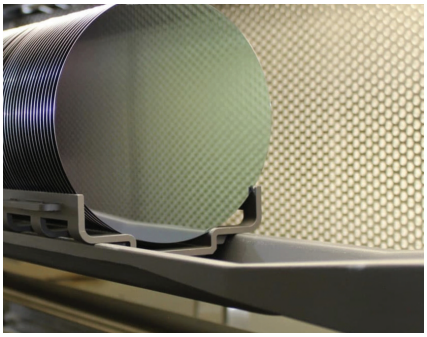
This announcement follows discussions over the last two years to link UK semiconductor expertise with Bulgaria's ambitions under the EU Chips Act 2023 and its fast-growing auto electronics sector.

Bulgaria is a gateway to Eastern markets and a key manufacturing hub in Southeast Europe. The country now produces about 80 percent of sensors used in European cars and hosts state-of-the-art R&D centres and smart factories (for example, Melexis in Sofia, Sensata and Schneider Electric in Plovdiv).

In 2024, a roundtable in Sofia hosted by British Embassy Sofia brought together UK and Bulgarian government, academia, and industry leaders to discuss opportunities. STN followed this up by organising a study visit to Scotland in March 2025, where Bulgarian stakeholders experienced the UK's world-class factories and training models first-hand.

Finally, a UK trade mission to Bulgaria in November 2025 showcased the country's growing semiconductor ecosystem, including both Bulgarian innovators and global players investing in the Bulgarian market, attracting UK innovators to explore partnerships.

The launch of the Green Silicon Carbide factory in Bulgaria aims to deepen R&D partnerships and expand skills



initiatives by linking UK compound semiconductor expertise with Bulgaria's manufacturing capacity.

The UK-Bulgaria Strategic Partnership has resulted in a series of other activities including a research MoU between Glasgow and Sofia Universities, enabling joint projects and talent exchange; and an industry MoU between TechWorks UK and Bulgaria's Association of Electrical Engineering and Electronics.

VIS signs GaN licensing agreement with TSMC

TAIWANESE foundry Vanguard International Semiconductor (VIS) has signed a technology licensing agreement with TSMC for high-voltage (650 V) and low-voltage (80 V) GaN technologies.

Through this licensing agreement, VIS will expand its GaN-on-silicon technology into high-voltage applications and offer a comprehensive GaN-on-silicon platform for power applications. Combined with its existing GaN-on-QST technology platform, VIS will become the only foundry in the world capable of offering power GaN technologies on both silicon and QST substrates.

VIS will support complete product solutions covering low voltage (less than 200 V), high voltage (650 V) and ultra-high voltage (1200 V), further strengthening its technology roadmap for high-efficiency power conversion.

The aim is to accelerate the development and expansion of next-generation GaN power technologies for applications such as data centres, automotive electronics, industrial control, and energy management, which are key areas that demand high-efficiency power conversion.

The technology will be validated on VIS' mature 8-inch manufacturing line to ensure process stability and high yield. Development activities are expected to commence in early 2026, with production scheduled for the first half of 2028.

"This technology licensing agreement not only underscores the engagement and ongoing collaborative efforts between VIS and TSMC, but also represents our continued commitment to advancing a comprehensive power GaN product portfolio and strengthening our strategic position in compound semiconductors," said John Wei, President of VIS.

"Through this collaboration, we will accelerate our support for customers in high-performance power conversion applications, enabling the semiconductor power technology to move into the next generation and helping realise a future of green energy and intelligent technologies."

IFW Dresden chooses Agnitron tools

Institute to use Agilis 100 MOCVD tools for its ScAlN roadmap and to test new chemistries for Ga_2O_3 thin films

THE MOCVD and ALD Competence Centre at the IFW Dresden, Germany, has selected the Agilis 100 MOCVD system to support its research on precursor chemistry and development of MOCVD and ALD processes.

IFW Dresden is developing innovative chemistries for a variety of new semiconductor device categories. Selecting the Agnitron tool enabled IFW Dresden to solve the challenges of deploying newly synthesised, unique, low-vapour-pressure precursors in a flexible R&D MOCVD platform.

Anjana Devi (pictured right), director of the Institute for Materials Chemistry at IFW Dresden, recognised this unique version of the Agnitron Agilis 100, which combines a newly developed apparatus for thermally

controlling the special precursors from the ampule to the wafer via a patented showerhead in this equipment.

"We found partnering with Agnitron provided us with the flexibility we need and the support required to execute our plan to synthesise and test new precursors in a commercial reactor," she said.

HexaTech launches 3-inch AlN substrate product

HEXATECH, a subsidiary of the Japanese firm Stanley Electric, has announced the immediate production release of its new 3-inch diameter single-crystal AlN substrate product.

Three-inch diameter substrates are seen as a key transition milestone toward the realisation of 100 mm diameter material, supporting future high-volume production of AlN-based high-voltage and high-frequency electronic devices.

"With this 3-inch launch, HexaTech continues to build on its history of delivering AlN material with industry-leading structural and surface quality, retaining the same macroscopic defect-free performance we have been producing for many years with

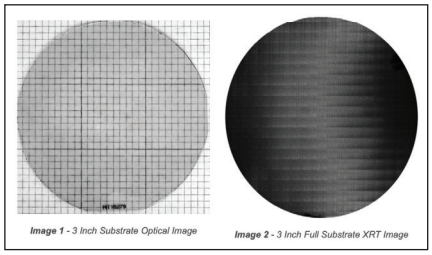


Image 1 - 3 Inch Substrate Optical Image

Image 2 - 3 Inch Full Substrate XRT Image

our existing 2-inch platform," remarked HexaTech manager of research and development Rafael Dalmau.

Gregory Mills, HexaTech VP of business development noted: "HexaTech continues to drive increased value by delivering superior quality alongside reduced price-per-unit-area to our customers. This accelerating trend will enable our customers to quickly transition from device research into production."

Nuburu to ramp high-power blue laser systems

NUBURU has announced the production ramp of blue lasers throught its Italian subsidiary Lyocon, following a previously awarded contract valued at approximately $850,000.

The order consists of 40 high-power 450 nm blue laser systems for Dutch agritech automation company Trabotyx, including: 24 units of 100 W systems, and 16 units of 200 W systems. The principal manufacturing and delivery cycle is scheduled for the first quarter of 2026.

The company says the order provides operational validation of Lyocon's scalable 450 nm high-power laser architecture.

Paola Zanzola, executive director of Lyocon, said: "Following a rigorous validation phase with the customer in 2025, we are now executing under a defined production programme. The flexibility between 100 W and 200 W configurations underscores the modularity of our architecture and its suitability for advanced automated systems. This delivery cycle represents an important operational milestone for Lyocon."

EPC releases GaN-based design for robot joints

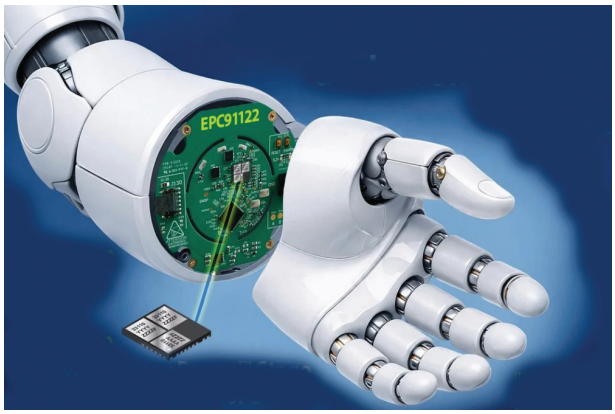
Motor drive inverter board features highly integrated 3-phase ePower Stage module

Efficient Power Conversion (EPC) has released the EPC91122, a 3-phase BLDC motor drive inverter evaluation board engineered for humanoid robot joint applications.

Featuring EPC's highly integrated EPC33110 3-phase ePower Stage module, the EPC91122 delivers up to 20 A_{RMS} (28 A_{peak}) phase current in an ultra-compact form factor optimised for space-constrained robotic joints, integrating all key functions of a complete motor drive inverter, including a microcontroller, motor shaft angular sensor, housekeeping power supplies, accurate voltage and current sense.

"The EPC91122 highlights how GaN-based power stages enable unprecedented integration and power density in humanoid robotics," said Marco Palma, director, Motor Drives Systems and Applications at EPC.

The EPC91122 is mechanically optimised to fit directly inside humanoid joint motors. The complete GaN inverter occupies a 32 mm diameter inner circle, surrounded by a 55 mm external frame that supports mechanical mounting and lab connectivity. This design lets the inverter fit inside the motor chassis, which lowers loop inductance and makes the power density and dynamic performance higher.



The EPC33110 is the main part of the system. It is a three-phase co-packaged module with a maximum voltage of 100 V. It has three monolithic GaN half-bridges with built-in gate drivers, bootstrap circuits, and level shifters.

The device has an $R_{DS(on)}$ of 11.7 + 13 mΩ and can switch at frequencies of up to 150 kHz, which means it may use smaller passive components and respond quickly to changes.

The board operates from a wide input range, making it well-suited for battery-powered robotic systems. It integrates all critical subsystems required for a complete motor drive inverter, according to EPC.

The EPC91122 comes preprogrammed to operate at 100 kHz PWM with 50 ns dead time, showcasing the high-speed switching capability enabled by GaN technology. Thermal testing under real-world operating conditions confirms the board's capability for continuous and pulsed operation.

As well as humanoid robot joints, the EPC91122 is suitable for compact servo drives, robotics, drones, and eMobility platforms. Complete design support files, including schematic, bill of materials (BOM), and Gerber files, are available.

Northrop Grumman to fast-track US microelectronics

The company is ready to deliver advanced semiconductor solutions over a ten-year period

NORTHROP GRUMMAN is one of the companies selected to receive an award from the Defense Microelectronics Activity (DMEA) for a contracting resource. This tool has an award ceiling of $25 billion and can speed up the delivery of military-grade semiconductor technology to get solutions into the hands of warfighters faster.

Under the Advanced Technology Support Program V (ATSP5), Northrop Grumman can: respond to requests for proposals within 30 days (the ATSP5 enables an 80 to 90-day turnaround time from proposal to award); and continue to advance solutions in next-generation manufacturing and packaging techniques as well as emerging semiconductor materials engineering.

Lori Manley, program manager, ATSP5, Northrop Grumman: “The government demands swift action, and we’re ready to deliver speed with this solution.

ATSP5 is an ‘Indefinite Delivery, Indefinite Quantity’ (IDIQ) contract used to ensure military systems have access to the most advanced microelectronics embedded within, replacing chips that are generations behind those available from commercial companies to deliver weapons systems readiness

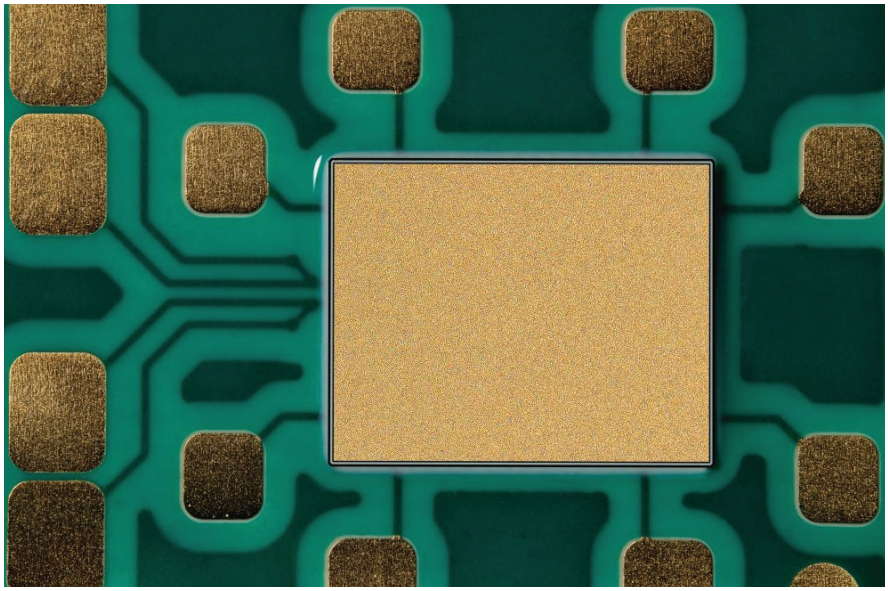


Photo Credit: Northrop Grumman

After years of using this process to complete more than 200 task orders across Northrop Grumman, the award of the ATSP5 contract proves our ability to rapidly integrate American-made microelectronics solutions and strengthen the US supply chain by ensuring speedy deployment of reliable systems for the warfighters who need them.”

Programme details

ATSP5 is an ‘Indefinite Delivery, Indefinite Quantity’ (IDIQ) contract used to ensure military systems have access to the most advanced microelectronics embedded within, replacing chips that are generations behind those available from commercial companies to deliver weapons systems readiness.

Aligned with the Secretary of War’s priorities, this award will enable improved responsiveness, defines both short and long-term goals and ensuring that teams remain focused on delivering solutions with speed to supercharge those providing technology to US military.

Northrop Grumman designs, manufactures, assembles, tests and packages millions of microelectronics annually to support next-generation defence and commercial systems in the United States, ensuring the American supply chain is protected and sustainable to strengthen national defence infrastructure.

From design, fabrication, to field, the company’s mission-tailored microelectronics serve as the crucial intelligence powering next-generation military and commercial systems and are foundational to mission success.

Northrop Grumman describes itself as a leading global aerospace and defense technology company. According to the company, its pioneering solutions equip its customers with the capabilities they need to connect and protect the world, and push the boundaries of human exploration across the universe.

The US firm says that its driven by a shared purpose to solve its customers’ toughest problems.

RF GaN: geopolitics fuel sustained growth

Sustained growth in high-power RF GaN is supported by 5G evolution and increasing adoption across defence and satellite communications.

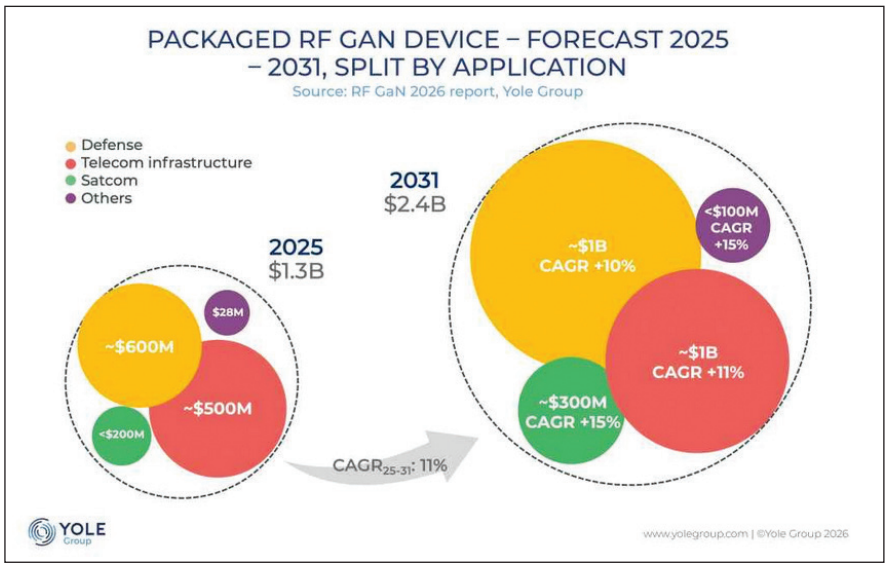
ACCORDING to Yole Group's latest report on the RF GaN market, GaN devices play a critical role in high-power RF signal generation and amplification, with growing adoption across telecom infrastructure, defence, and satellite communications.

The market is expected to reach $2.4 billion by 2031, growing at a 11 percent CAGR between 2025 and 2031, up from about $1.3 billion in 2025. After a downturn starting in 2023, due to weaker demand for telecom infrastructure, the market is now rebounding, driven by rising defence spending and supported by renewed momentum in satcom applications.

Yole Group's report, *RF GaN market*, analyses market dynamics in the context of 5G network evolution, growing defence requirements, and long-term preparation for 6G systems. As telecom architectures shift toward active antenna systems and defence platforms continue to transition to solid-state RF solutions, GaN is gaining share over legacy technologies. GaN-on-SiC remains the dominant platform, while GaN-on-silicon is being increasingly adopted in specific applications.

Defence and aerospace represent the second major pillar of the RF GaN market, characterised by high-performance requirements, long qualification cycles, and stable demand. In parallel, satellite communications increasingly rely on GaN for high-power uplinks in ground gateways and satellite terminals as operating frequencies expand from K/Ka up to E/W band applications.

The RF GaN defence market, valued at $592 million in 2025, is expected to reach $1 billion by 2031, growing at a 10 percent CAGR. Growth is driven by the increasing deployment of GaN-based solid-state RF technologies across radar, EW, and military satellite communications, with the United States remaining the leading adopter.



In radar systems, GaN RF technology has become a core enabler of AESA architecture operating across the S- to X-bands. Airborne radar represents the largest application segment, supported by the transition from TWT technologies to GaN-based transmit/receive modules that deliver higher output power, improved resolution, reduced weight, and greater scalability.

Adoption of GaN has also increased significantly in ground-based radar systems, while naval radar modernisation is progressing more gradually as innovation efforts focus on sensor integration and multifunction apertures.

Beyond radar, electronic warfare is among the fastest-growing RF GaN segments, as wideband, high-efficiency GaN power amplifiers enable compact jamming systems for counter-UAS applications, next-generation tactical radios, and high-data-rate military communications.

Beyond radar, electronic warfare is among the fastest-growing RF GaN segments, as wideband, high-efficiency GaN power amplifiers enable compact jamming systems for counter-UAS applications, next-generation tactical radios, and high-data-rate military communications.

Navitas unveils fifth-gen SiC technology

Latest trench-assisted planar technology delivers improvements for AI data centres, grid and energy infrastructure, and industrial electrification

NAVITAS has launched its 5th-generation GeneSiC technology platform. The high-voltage SiC trench-assisted planar (TAP) MOSFET technology is claimed to represent a significant technological leap over previous generations.

The technology, which will be used to make 1200 V devices, complements Navitas' ultra-high voltage (UHV) 2300 V and 3300 V technologies from the 4th generation GeneSiC platform.

The 5th generation MOSFET platform features Navitas' most compact TAP architecture yet, combining the ruggedness of a planar gate with high performance enabled by a trench structure in the source region, while also elevating the efficiency and life-time reliability for high-voltage power electronics.

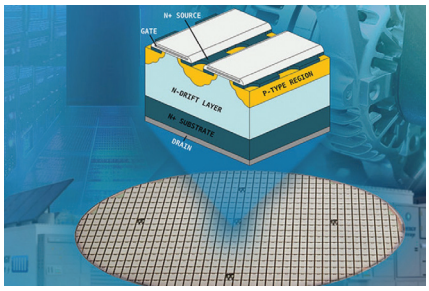
The 5th generation platform is said to achieve a new benchmark in power conversion through a 35 percent improved $R_{DS,ON} \times Q_{GD}$ figure of merit, as compared to the previous generation 1200 V technology. This improvement slashes switching losses, allowing for cooler operation and higher frequency of operation in demanding power stages.

High-speed switching is further fortified by a 25 percent improvement to the Q_{GD} / Q_{GS} ratio. When paired with a stable high-threshold-voltage specification ($V_{GS,TH} \geq 3$ V), this technology ensures immunity against parasitic turn-on, providing a robust and predictable gate drive, even in high-noise environments.

The 5th generation technology delivers improvement in dynamic performance by optimising the $R_{DS(ON)} \times E_{OSS}$ characteristic while also integrating a 'Soft Body-Diode' technology to further enhance system stability by minimising electromagnetic interference and ensuring smoother commutation during high-speed switching cycles.

AEC-Plus grade qualification of this generation ensures long-term stability and durability for AI data centres, energy and grid infrastructure applications.

> Our customers are redefining the boundaries of power conversion in AI data centres and energy infrastructure, and Navitas is marching along with them in every step of the way



Key reliability benchmarks include: 3 times longer duration for static high-temperature, high-voltage testing (HTRB, HTGB, and HTGB-R); dynamic reverse bias and dynamic gate switching to represent stringent fast-switching application mission-profiles; and an extrapolated gate-oxide failure time exceeding 1 million years at a V_{GS} of 18 V and 175°C. The technology also has enhanced cosmic ray resilience with low Failure-in-Time rates, ensuring mission-critical reliability in high-altitude and high-uptime environments.

"Our customers are redefining the boundaries of power conversion in AI data centres and energy infrastructure, and Navitas is marching along with them in every step of the way," said Paul Wheeler, VP & GM of Navitas' SiC Business Unit.

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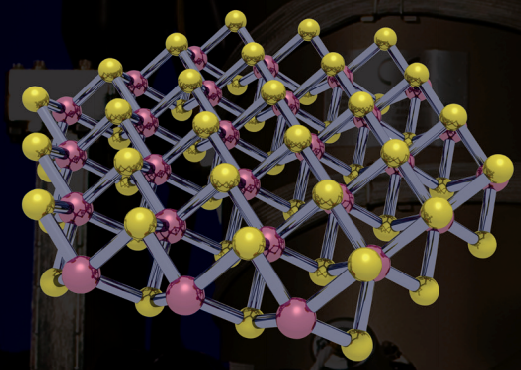

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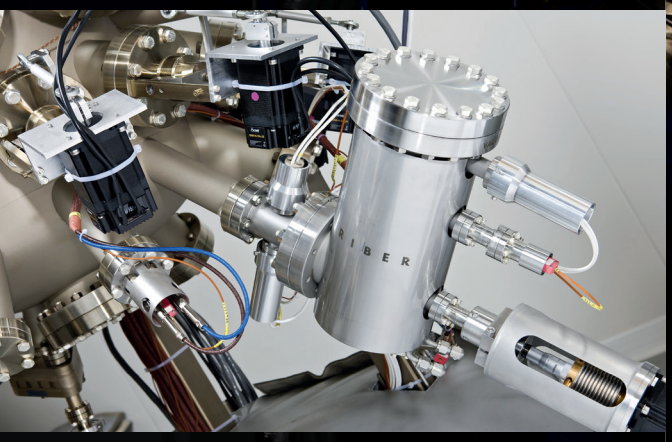

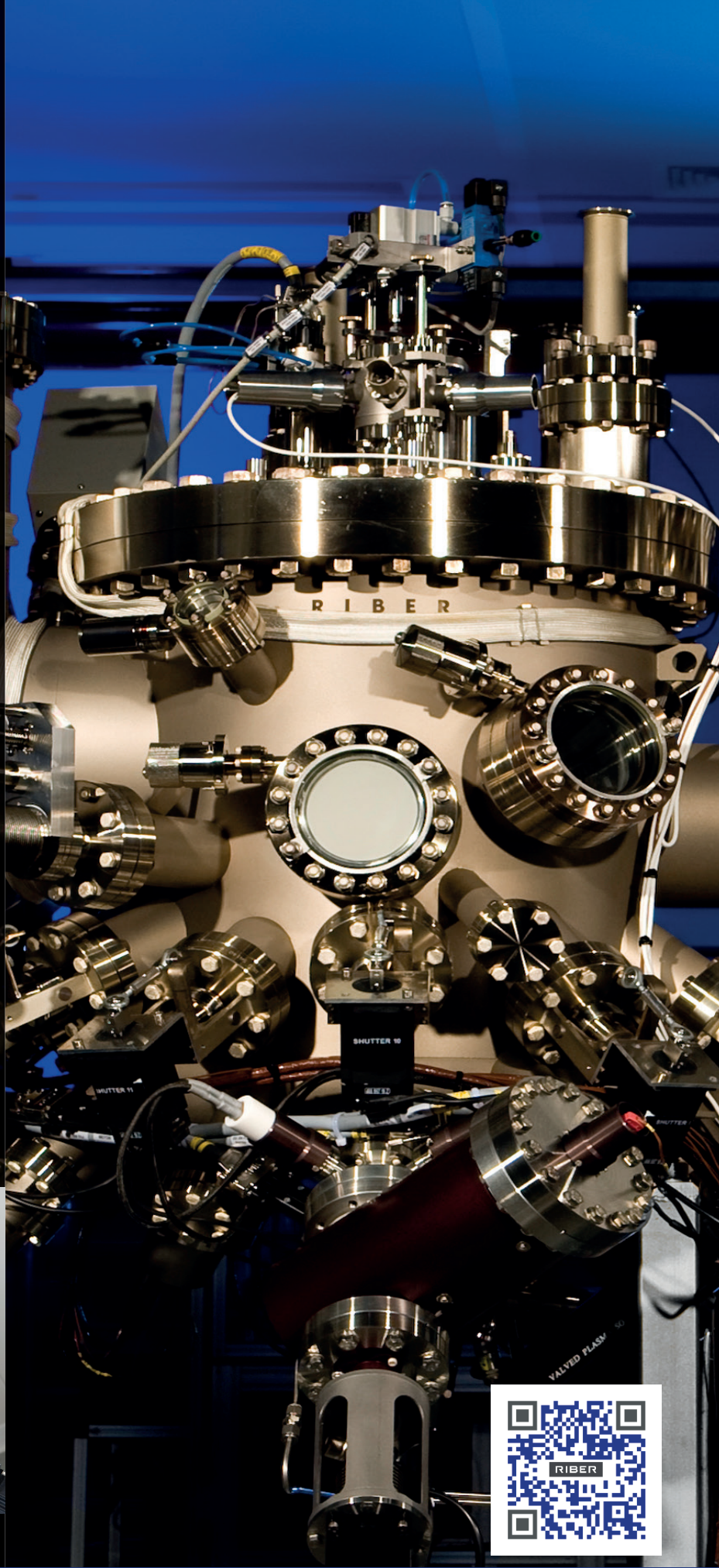

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A universal solution for chip heating

More powerful, more reliable devices may be realised by replacing the substrate with a composite that provides an exceptionally low thermal resistance

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AT TIMES, our industry appears a disparate entity. The high-power GaAs lasers diodes that cut and weld metals operate in a different sphere from their InP cousins that underpin the internet – and both these emitters occupy different domains from the RF devices deployed in defence, and the wide bandgap diodes and transistors that are improving the efficiency of power delivery.

But there are common threads running through these various classes of compound semiconductor devices. One is that they are united by epitaxial growth, with gains on this front having far-reaching ramifications. And another, of high importance but not discussed as much, is that the performance of all these devices derives substantial benefits from better thermal management. Gains include higher output powers, greater efficiencies, and longer lifetimes.

A new, exciting and universal solution to this critical thermal management issue is now being pioneered by Dutch start-up CoolSem. It has just secured a pre-seed financing round that will support the commercialisation of its chip-cooling technology, involving removal of a substrate, which is replaced by a composite structure with a vastly superior thermal conductivity.

The trailblazer of this technology is CoolSem CEO and CTO, André van Geelen. Back in the early 1990s, during his time as a PhD student at Radboud University, he developed a key element of the start-up's core technology – wafer-scale removal of a substrate from its epilayers via epitaxial lift-off, a proven process already in use for the formation of large, flexible III-V solar cells.

Since then, van Geelen has spent his entire career within the semiconductor industry, initially working for a number of high-profile companies – Philips, JDSU, ThreeFive Photonics, and NXP – where he gained insight into the issues associated with device heating, and how this limits performance.

For the last 10 years, most of his time has been devoted to consulting start-ups and working on the board of UK start-up Forefront RF. But recently he has also been mulling over his idea for superior thermal chip management, with his entrepreneurial side nagging away and eventually getting the better of him. "Basically, I stopped most of my consultancy and went for it," remarks van Geelen.

➤ A key element in CoolSem's technology is substrate removal, accomplished by either epitaxial lift-off on grinding and polishing.

A classy composite

There are essentially two parts to the CoolSem technology, which provides a more elegant solution to chip heating than existing approaches based on attaching a cooler to either the chip or the package. Substrate removal is the first step, followed by the addition of a heat-sinking composite.

For III-V structures, substrates may be removed and re-used by epitaxial lift-off, a process that involves the etching of a sacrificial layer. That's not an option for devices grown on silicon, but in this case a grinding-and-polishing approach is available, a technique widely used on 200 mm and 300 mm wafers.

To determine the composition of the composite that delivers the best results,

van Geelen has undertaken one- and two-dimensional simulations of various material combinations, considering mechanical and thermomechanical stresses.

"One of our customers actually put the key parameters that we provided in their device and found a clear improvement. In this case, this was on a power amplifier for Satcom."

This verification of CoolSem's technology underscores the potential of the proprietary composite, which features a wide bandgap material beside the chip, a central compliance layer and a base metal. This trio, referred to as WaLTIS – that's short for Wafer-Level Thermal Interface Stack – has a thermal-resistance-per-mm^2 of just 0.2 K W^{-1}. That's far lower than a typical device with a Au/Sn solder, which would have a value of 3 K W^{-1}. Thanks to the thermal superiority, chips run at far lower operating temperatures, with differences between the device and its foundation falling from between 30°C and 60°C to just 4°C.

As well as tremendous thermal properties, WaLTIS provides excellent mechanical support and avoids RF losses, crucial when used with power amplifiers.

One of the strengths of this technology is the generality of the solution, as WaLTIS is compatible with all semiconductor materials. The only change that might be applied from one device to another is the thickness of the compliance layer: "If you have extremely large die, you can imagine that the stresses in the stack become larger, so we need a little bit more compliance there," says van Geelen.

To take his idea from the drawing board to commercial success, he hand-picked three co-founders, all known to him from previous projects. They are: Commercial Officer Pieter Heersink, who van Geelen worked with on a previous start-up; Strategic Officer Robbert van der Waal, a co-worker at NXP; and Operational Officer Kees Steenbergen, who was a colleague at ThreeFive Photonics.

Following the coming together of these four in autumn 2025, the team has expanded with the addition of four engineers, plus two-to-three external contributors. Together they are supported by an undisclosed level of funding: roughly half of this is equity; one-quarter loans; and the other quarter a grant from the Dutch Future Network Services Programme, which focuses on future RF technologies.

➤ The founder of CoolSem are: CEO and CTO André van Geelen (front right), Operational Officer Kees Steenbergen (front left), Commercial Officer Pieter Heersink (back left), and Strategic Officer Robbert van der Waal (back left).

A hands-on approach

CoolSem's business plan is to provide a 'mid-end' foundry service. This involves receiving processed epiwafers, followed by the application of CoolSem technology and the dispatching of chips on a plastic thin-film backing to packaging houses.

To begin with, CoolSem will carry out its processes with local external partners, based in The Netherlands and Germany. "Some provide facilities as well. It's not just services," says van Geelen, who reveals that these relationships have provided CoolSem with access to a cleanroom, which can be used for prototyping and initial engineering.

Looking further ahead, CoolSem plans to carry out its processes in-house. Accomplishing this only requires a few tools, an investment totalling €5-10 million.

One of the benefits of this is that it will help CoolSem advance its technology. And in addition, it will reduce the risk that potential customers will take.

"We plan to bring up to pilot volumes, which could be 30,000 wafers a year. Anything beyond that, I think most customers we're working with would feel quite comfortable bringing that over to their own environment," says van Geelen, explaining that this transition involves a licensing model.

If makers of VCSELs and other forms of laser adopt CoolSem's technology, it could have a big impact – van Geelen suggests increases in efficiency from around 25 percent to twice that. Substantial gains are also possible in RF devices. In power devices, increases in efficiency are more modest, but given emphasis on minimising electrical consumption, such savings will still have much value.

To transition CoolSem's technology from promise to reality, the aim is to demonstrate its capabilities to customers this summer. "That's also the point where we will engage with two or three customers, to demonstrate the technology in their applications."

The hope is that success with the latter will occur in summer 2027, paving the way for new generations of chips that run cooler, while performing better.

UltraRAM: A viable solution for post-silicon memory?

While UltraRAM has much promise, will long-standing challenges with interfaces, variability and manufacturability scupper commercial success?

BY DOMINIC LANE FROM THE UNIVERSITY OF ADELAIDE (ADJUNCT)

IF YOU could construct the ultimate form of computational memory, what form would it be? While opinions will differ on the details, many will concur that it will combine the non-volatility of a data-storage memory, such as flash, with the speed, energy-efficiency and endurance of a working memory, like DRAM.

Offering much potential on all these fronts is an emerging technology, known as UltraRAM. It's an elegant, intellectually compelling memory concept that draws on a carefully engineered III-V heterostructure to combine fast access with non-volatility. Early laboratory demonstrations are offering much encouragement, demonstrating that underlying device physics functions as intended – and this success is helping UltraRAM to attract attention as a potential alternative to established memory technologies.

However, commercial success is by no means a certainty for UltraRAM. Anyone that has spent much time within the semiconductor industry knows that the transition from a working laboratory device to a manufacturable memory platform is rarely a stroll in the park – instead, it's often where the most serious challenges arise. It is in this context that UltraRAM's longer-term prospects must be assessed.

Demonstration versus deployment

During development of semiconductor device technologies, early progress tends to focus on proof-of-concept demonstrations that validate a physical mechanism. Such milestones are essential and exciting. But they do not, on their own, determine whether a technology can be scaled to the densities, yields and reliability required for commercial success.

For ultraRAM, data in the public domain is largely confined to micron-scale devices characterised under controlled laboratory conditions. Retention and endurance behaviour are commonly inferred through extrapolation, rather than through demonstrations across statistically meaningful device populations. In the open literature little is said on advanced CMOS metrics that ultimately govern memory viability – they include wafer-level yield, array-level uniformity, threshold-voltage distributions and integration compatibility.

This gap between demonstration and deployment is not unusual in early-stage technologies, but it has become increasingly important as claims of maturity begin to circulate.

An enduring interface challenge

Unfortunately, UltraRAM inherits a difficulty that's been plaguing III-V devices for decades: realising stable, low-defect interfaces. This challenge has thwarted efforts to displace silicon in logic applications with materials such as GaAs and

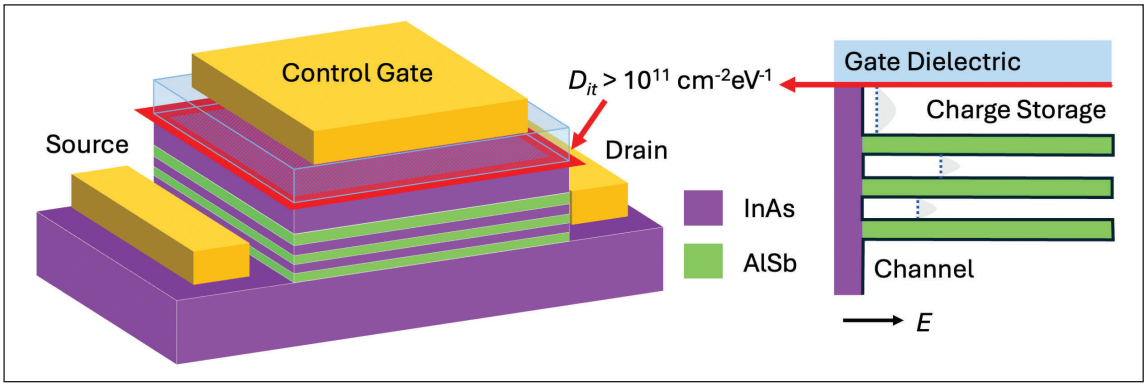


Figure 1. The structure of ultraRAM includes a heterostructure based on alternating layers of InAs and AlSb, an InAs floating gate, and a dielectric.

InGaAs, which have superior transport properties. It's a limitation still relevant today for memory concepts based on similar material systems.

In devices based on UltraRAM, the stored charge resides in a quantum-confined region with an electron density on the order of 10^{12} cm^{-2}. Note that this signal level is dictated by the physics of the heterostructure rather than by design margin. As reported interface-trap densities in relevant III–V systems are typically 10^{12}-10^{13} cm^{-2} eV^{-1}, they are comparable to, or even exceed, the stored charge itself.

Under such conditions, trap occupancy plays a prominent role in device behaviour. Due to this weakness, interface quality needs to improve substantially – otherwise variability, drift and retention degradation will remain central considerations, rather than secondary effects.

Variability kills memory

It's tempting to draw parallels between emerging memory concepts and development trajectories for UltraRAM and other post-silicon semiconductor technologies. But that's a questionable rationale, as memory devices operate under constraints that are fundamentally different to those governing power and RF electronics.

For example, power devices derive value from the performance of relatively small numbers of components, so yield loss and parameter spread tends to be mitigated through design margin, redundancy or binning. In sharp contrast, memory demands the correct operation of numerous nominally identical cells. Memory chips may contain billions of devices, and each must function within extremely narrow voltage margins.

In this statistical regime, variability is not merely a yield concern – it is a functional one. Failure mechanisms with low probability at the device level are a killer when myriads are deployed across large arrays. Due to this, interface-related fluctuations that might be tolerable in other device classes are to blame for unacceptable bit-error rates in dense-memory architectures.

This distinction places particularly stringent demands on material quality and uniformity.

Integration realities

Some of the proposed development paths for computational hardware envision combining memory and logic within III-V material platforms. While this is a conceptually appealing architecture, similar approaches have been explored extensively in the past, without much success. Large industrial efforts, investing decades in the development of III-V CMOS, encountered a combination of technical and economic challenges. Among these, the realisation of sufficiently stable and low-defect oxide/semiconductor interfaces has been a persistent hurdle.

Until stable, CMOS-compatible interfaces between III-Vs and their native oxides yield interfaces with trap densities approaching around 10^{9} cm^{-2} eV^{-1} – the benchmark that enabled Flash memory to scale – UltraRAM should be seen as important research, rather than a near-term manufacturing solution

Much effort has been devoted to retaining silicon substrates. It's an approach that accommodates the vast investment in silicon manufacturing lines. However, when silicon substrates are retained, there are challenges associated with large-area III-V heterostructures, related to dislocations, wafer bow and thermal mismatch. Controlling these issues at the full wafer scale is critical to viable manufacturing. While isolated device demonstrations offer encouragement, they do not address system-level requirements.

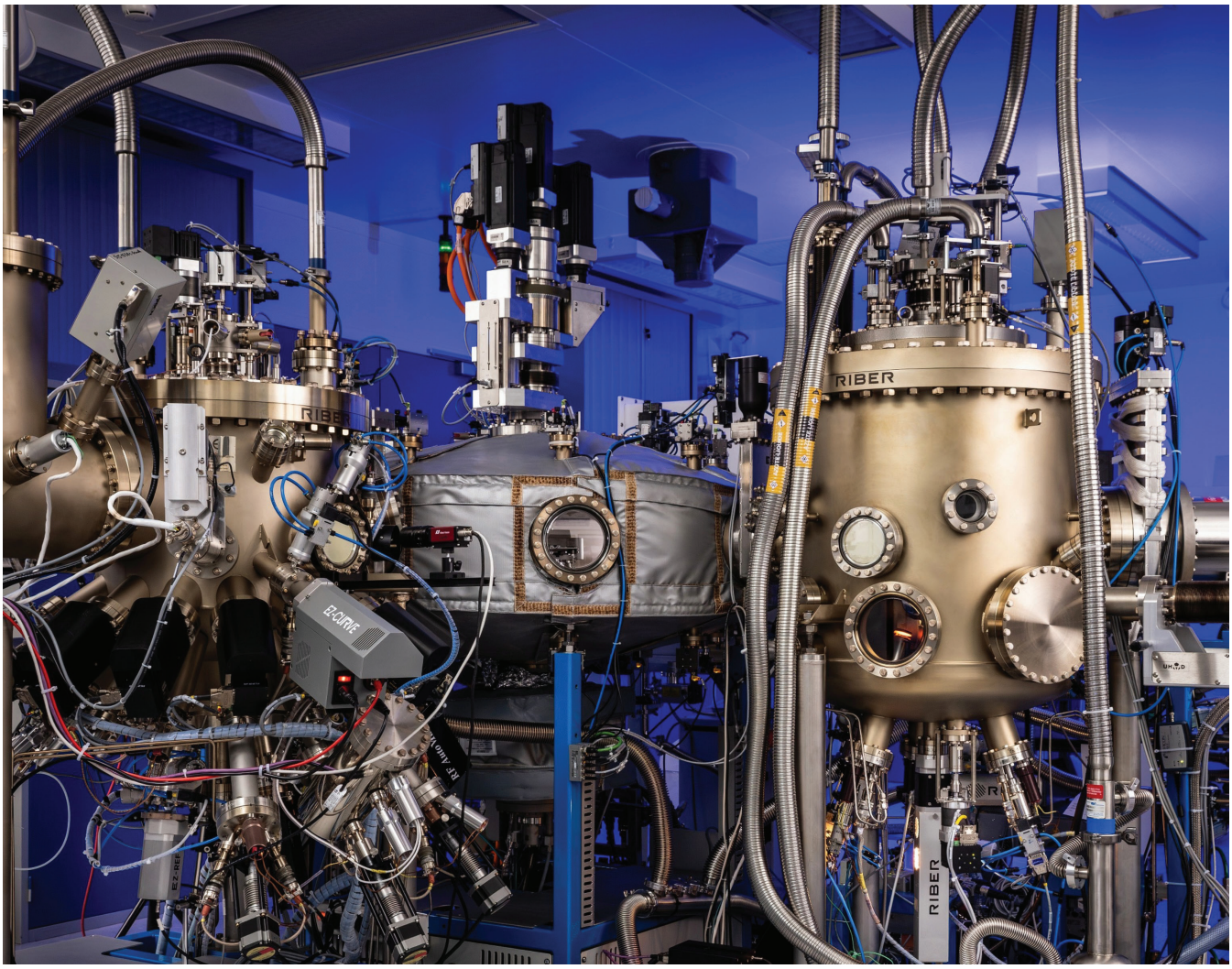
Another cause for concern is recent modelling studies, which extend UltraRAM concepts into areas such as neuromorphic computing, often assuming ideal integration, negligible variability and multi-bit precision across large arrays. While such simulations are valuable exploratory tools, they do not replace experimentally demonstrated margin.

When undertaking these investigations, it's imperative to consider fabricated arrays operating under realistic conditions. Ignoring this risks drawing conclusions from models that obscure practical constraints, which ultimately determine feasibility.

A call for measured expectations

There's no doubt that UltraRAM is an impressive scientific achievement, and one that provides a valuable platform for exploring III-V interface physics. And it is possible that breakthroughs in interface passivation could enable new classes of memory devices based on similar principles. However, for now, the technology should be viewed through the lens of what has been demonstrated, rather than what is hoped for. Until stable, CMOS-compatible interfaces between III-Vs and their native oxides yield interfaces with trap densities approaching around 10^{9} cm^{-2} eV^{-1} – the benchmark that enabled Flash memory to scale – UltraRAM should be seen as important research, rather than a near-term manufacturing solution.

UltraRAM's future will be determined by progress in materials science and interface engineering, rather than narrative momentum. If long-standing interface challenges are resolved, this could allow UltraRAM to influence future memory architectures. But if that's not the case, let's keep our feet on the floor, and allow experimental evidence to guide our discussions and evaluations of this technology.



Making qubits by MBE

MBE excels in the growth of structures for quantum computing that combine layers of semiconductors and superconductors

BY CLAUDINE PAYEN, YOURI ROUSSEAU, ROMAIN RICHARD FROM RIBER AND ALEXANDRE ARNOULT, SÉBASTIEN PLISSARD, QUENTIN GRAVELIER AND HUGUES GRANIER FROM LAAS-CNRS

THE FIRST quantum revolution, associated with the birth of quantum theory, took place at the start of the twentieth century. Humanity is now building on this as we enter the second quantum revolution, which is characterised by the manipulation, control and exploitation of quantum phenomena, with the objective of creating new technological objects. A key part of this era is the introduction of quantum computing.

This particular breakthrough is so exciting that it's not just being reported in the technical press – stories of quantum computing are also appearing in mainstream media. An ever-growing number of laboratories are driving progress, along with the major research centres of the five big tech companies, collectively referred to as GAFAM: Google (Alphabet), Amazon, Meta (formerly Facebook), Apple, and Microsoft. Efforts by these institutions are directed at providing innovative, high-performance solutions in areas such as simulation, particularly in chemistry and pharmacology, as well as encrypted data exchange, and flux movement optimisation – the latter relates to the likes of car traffic and logistics.

The goal of a quantum computer is not limited to using quantum physics for its operation. The aim is to also ensure

that computations are quantum, that is, the way calculations are performed is also quantum related. To accomplish this, computation must involve two key quantum properties: the superposition of states and quantum entanglement.

Engineers that are working towards this have several options for building a quantum computer. To transport information, they can employ trapped ions, photons, electron spins, nitrogen-doped diamond cavities, Josephson-effect superconductors, or Majorana fermions (fermions that are their own antiparticles, and appear in certain materials, including hybrid systems of superconductors (Al, Nb...) and topological insulators (BiSe, BiTe..)). All these particles are known as quantum bits or, for short, qubits. Only time will tell which of these approaches prove successful, and as of today nothing has been definitively established.

Among the different ways to create a qubit, three may benefit from MBE: Majorama fermions, Josephson junction superconductors and photons.

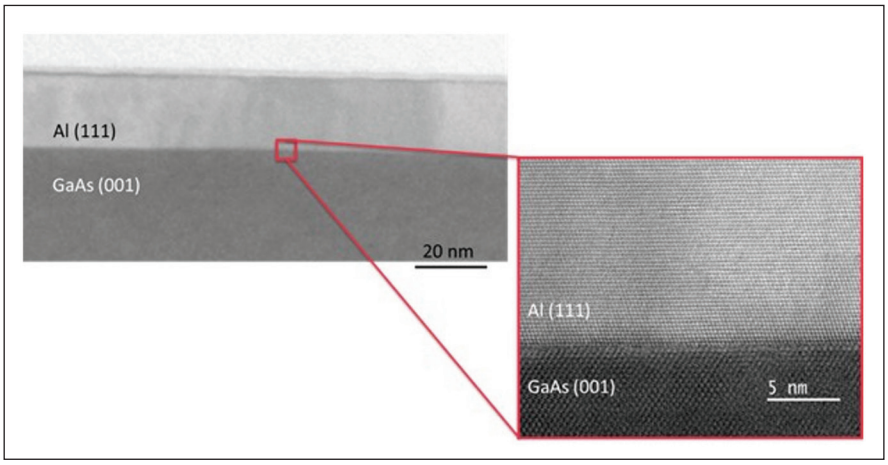
The key strengths of MBE are its ultra-clean ultra-high vacuum environment, the use of high-purity material that enables the growth of perfectly defect-free interfaces, and exceptional control that ensures monolayer precision and crystalline perfection.

To support the development of quantum computing, our company, Riber, which has been making MBE systems for more than 45 years, has recently launched a new platform with the capability to produce semiconductor-superconductor structures within a single ultra-high vacuum environment.

The Supra hybrid platform

Our hybrid platform called Supra – derived from the French word for superconductor, 'supraconducteur', is a fully automated ultra-high vacuum system that's dedicated to the growth of semiconductor–superconductor heterostructures. Developed in close collaboration with LAAS-CNRS Toulouse within the joint laboratory Epicentre, it provides unprecedented control over epitaxial interfaces, opening new pathways for producing higher-performance qubits.

When developing our Supra hybrid platform, we have drawn on our long-standing expertise in the MBE of III–V semiconductors. Within this new platform is a primary III-V growth chamber that's optimised for the fabrication of high-purity heterostructures of compound semiconductors.



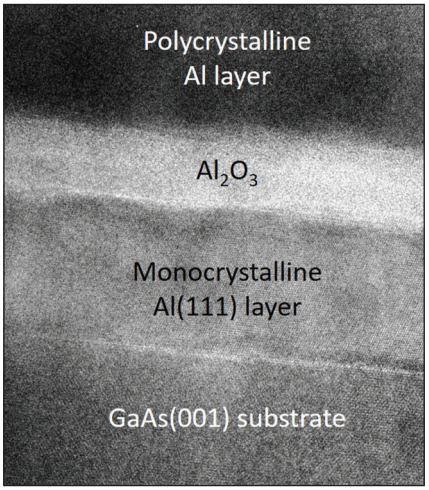
➤ Transmission electron microscopy image, showing the perfect interface of 20 nm-thick aluminium (111) grown on a GaAs (001) substrate. Results from Epicentre.

This chamber is directly connected, under ultra-high vacuum, to a new, patented cryogenic metal growth reactor that's dedicated to superconducting materials. In this chamber engineers can deposit thin superconducting films, such as aluminium, tin, lead and specific alloys, directly onto semiconductor surfaces at temperatures below 100 K. Thanks to full-wafer *in-situ* deposition on rotating substrates, our platform provides excellent thickness uniformity on wafers with diameters up to 100 mm, while in-vacuum transfer guarantees oxide-free, contamination-free interfaces.

Critical cryogenic growth

For superconductors, shifting from conventional deposition temperatures to the cryogenic realm delivers decisive advantages. Cryogenic temperatures suppress the surface diffusion of metal adatoms, leading to smooth, continuous films with reduced grain boundaries and structural disorder. What's more, this growth regime minimises thickness inhomogeneities to yield ultra-flat superconducting layers with low dissipation. Equally important, deposition at cryogenic temperatures strongly suppresses interdiffusion and chemical reactions at semiconductor-superconductor interfaces. By preventing alloy formation and interface roughening, our system preserves atomically abrupt, chemically intact interfaces. This exceptional interface quality ensures high transparency and strong superconducting proximity effects – they are key requirements for high-performance Josephson junctions and hybrid quantum devices.

For aluminium in particular, a low growth temperature enables the stabilisation of specific crystalline orientations and epitaxial relationships, requirements that are difficult to obtain at higher temperatures. Structurally coherent films are crucial, translating directly into improved device uniformity, narrower distributions of critical current, and reduced leakage in Josephson



➤ First Josephson junction achieved in the framework of Epicentre by Sébastien Plissard and his team.

junctions. All three are essential for scalable quantum circuits.

Benefits of cryogenic growth are also seen when viewed from a quantum device perspective. There's reduced structural disorder and pristine interfaces, two valued characteristics that lead to a lower quasiparticle density, reduced noise sources, and improved coherence times – central metrics for qubit performance.

Our platform also provides dedicated oxidation capabilities, either within the cryogenic chamber or in a specific oxidation module. This allows precise, reproducible formation of ultra-thin tunnel barriers under controlled conditions.

By maintaining the entire semiconductor-superconductor growth and oxidation sequence under ultra-high vacuum, we eliminate uncontrolled oxidation and contamination that's typically associated with *ex-situ* processing.

One of the weaknesses of traditional fabrication methods is that they often expose the superconducting film to air during processing, leading to uncontrolled oxidation and interface contamination. By contrast, our hybrid platform maintains the entire semiconductor-superconductor growth sequence under ultra-high vacuum, to ensure epitaxial interfaces with superior transparency and stability.

We have evaluated the capabilities of our Supra hybrid platform by growing and characterising a structure on a GaAs (001) substrate that consists of a thin epitaxial aluminium (111) layer, a thin Al_2O_3 tunnel barrier, and a polycrystalline aluminium top electrode. For the growth of the aluminium layer, deposition took place at 90 K, a low temperature that strongly reduced the surface mobility of aluminium adatoms, supressed long-range diffusion, and limited the formation of misoriented nuclei. Due to this, aluminium grows epitaxially on GaAs (001) with a well-defined (111) orientation.

Inspecting this structure using cross-sectional electron microscopy provides images with uniform contrast and an absence of visible grain boundaries. This form of microscopy also confirms the single-crystalline nature of the aluminium (111) layer.

During the growth of this superconductor-semiconductor stack, the thin Al_2O_3 layer is formed by controlled oxidation of the epitaxial aluminium surface. There is a lack of long-range order in the oxide, indicating an amorphous structure. This leads to an aluminium (111) epitaxial/Al_2O_3 amorphous/aluminium polycrystalline stack that combines a high-quality superconducting base electrode with a robust tunnel barrier. It's a combination that's well-suited to Josephson junctions integrated on semiconductor platforms. This technology is a candidate for superconducting electronics and quantum devices.

Beyond semiconductor-superconductor fabrication, our platform is a contender for producing Josephson junctions, thanks to a chamber that can grow superconducting material at a low temperature. It should be noted that the Supra chamber allows growth with wafer rotation, to ensure high uniformity across the whole wafer.

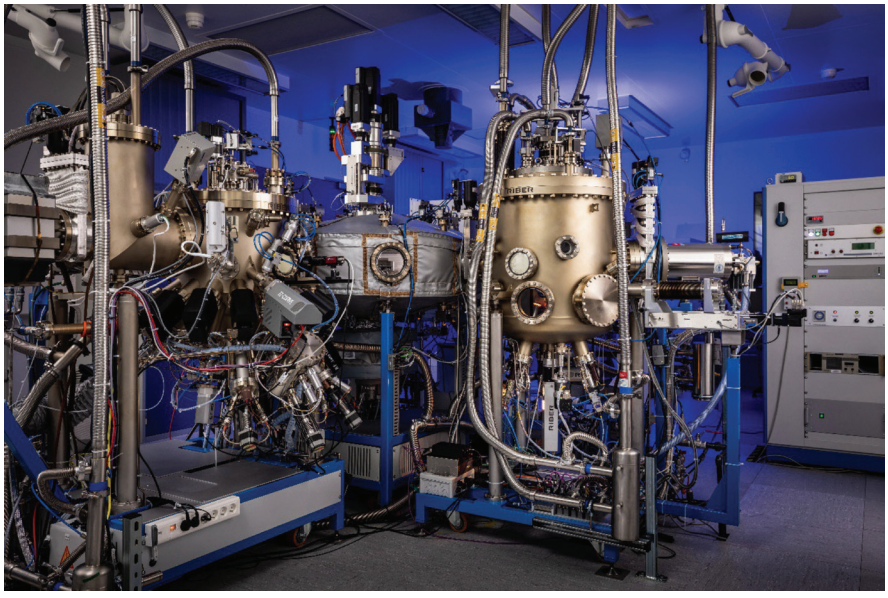
Towards early industrialisation

With a combination of ultra-high vacuum integrity, full automation, recipe-based process control, and real-time *in-situ* monitoring instruments that are based on optical measurements and, our Supra platform provides a level of reproducibility suited not only to academic research but also the early-stage industrialisation of quantum technologies. As this emerging field moves toward scalable architectures, the ability to fabricate uniform hybrid interfaces and Josephson junctions across full wafers will become indispensable.

By integrating III-V semiconductor growth, cryogenic superconductor deposition and controlled oxidation in a single ultra-high vacuum environment, our hybrid platform minimises contamination, increases uniformity and simplifies workflow – they are three key requirements when transitioning from laboratory-scale demonstrations to manufacturable quantum devices.

Supporting our development of quantum-related technologies is the Epicentre, a joint laboratory between Riber and the CNRS Laboratory for Analysis and Architecture of Systems (LAAS-CNRS) in Toulouse – it's one of the largest in-house units of the French National Centre for Scientific Research (CNRS). Working together, we have already used the Supra chamber to demonstrate high-quality aluminium growth on GaAs substrates, with monocrystalline aluminium films grown below 100 K for several hours, atomically sharp interfaces confirmed by transmission electron microscopy, and the realisation of the first Josephson junctions, developed by Sébastien Plissard and his team at LAAS-CNRS.

Beyond device validation, the Epicentre is playing a central role in addressing key technological barriers that have



➤ Supra Platform at Epicentre, a joint laboratory between Riber and LAAS-CNRS member of Renatech network.

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previously limited the integration of cryogenic superconductor growth within an MBE environment. One major challenge that we have tackled through the development of the Supra chamber is the design of a cryogenic metal growth chamber that's compatible with ultra-high vacuum and full-wafer MBE standards, while maintaining precise thermal stability below 100 K over extended deposition times. To realise such stability, we had to develop a dedicated cryogenic architecture that ensures uniform cooling, controlled thermal gradients, and mechanical stability compatible with wafer rotation.

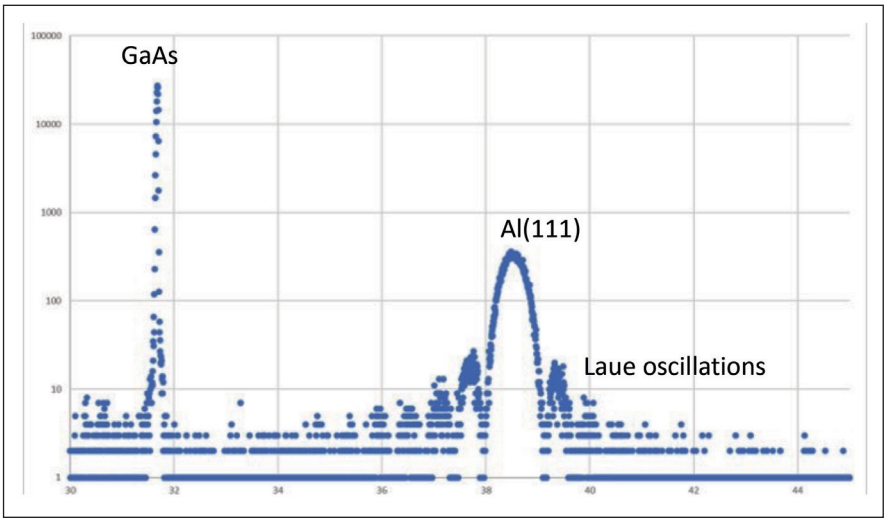
Another critical hurdle that we've overcome is the preservation of interface purity during cryogenic deposition. At low temperature, conventional effusion and shutter designs could induce parasitic condensation, flux instabilities, and uncontrolled background deposition. Our Supra chamber architecture overcomes these limitations through a patented source-to-substrate geometry and thermal management scheme, enabling a stable metal flux, reproducible growth rates, and the suppression of unwanted condensation on cold surfaces.

An equally important challenge is enabling *in-situ*, contamination-free transfer between semiconductor growth, cryogenic metal deposition, and controlled oxidation. Our Supra hybrid platform, which integrates an ultra-high-vacuum-connected cluster design, ensures that the semiconductor–superconductor interface is never exposed to ambient conditions. This capability is essential for maintaining chemically abrupt interfaces and forming reproducible tunnel barriers.

Strengths of the Supra hybrid platform

The Supra hybrid platform enables:

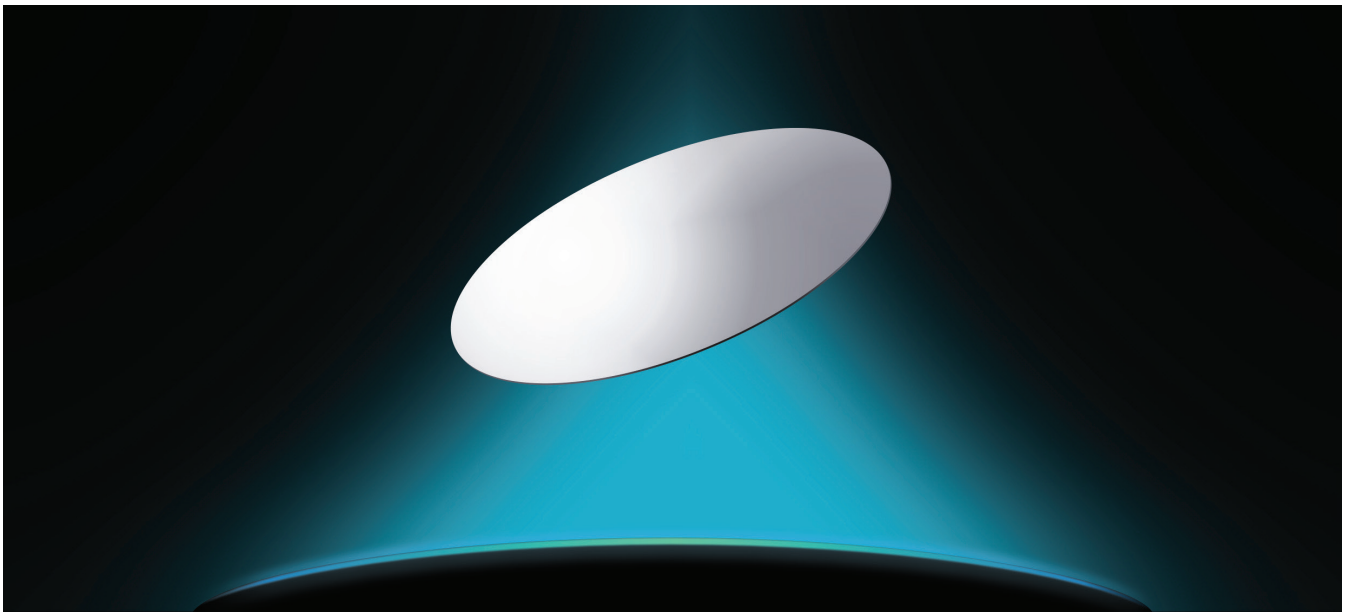
- **III-V semiconductor growth** with precise control over thickness, doping, and interface sharpness.
- **In-vacuum transfer** to a cryogenic deposition chamber for Aluminum or other superconducting materials, ensuring perfect, oxide-free interfaces.
- **Rotating-wafer metal deposition** for uniform superconductor films.
- **Up to 100 mm wafers capability**
- **Dedicated oxidation chamber** allowing controlled and reproducible oxidation of superconducting layers—crucial for tunnel barriers in Josephson devices.
- **Real-time *in-situ* monitoring,** enabling automated process control



➤ Aluminium deposition on a GaAs substrate with 2D morphology and monocrystalline phase. X-ray diffraction measurement of a 18 nm-thick aluminium film grown at 92K on a GaAs (001) substrate. Epicentre was able to maintain substrate temperature below 100K during aluminium growth for more than 3 hours.

We will continue to advance the capabilities of our hybrid platform and share our results.

Efforts related to the latter including a presentation by Sébastien Plissard at the International Workshop on Superconductor-Semiconductor Hybrids 2026 that will highlight Supra's role as a key enabling platform in next-generation hybrid quantum technologies.



Towards in-space crystal growth

Could the answer to how to produce the next-generation of reliable, high-quality semiconductor crystals lie in space?

BY ALASTAIR MCGIBBON AND NEIL MONTEIRO FROM SPACE FORGE

COMPOUND SEMICONDUCTORS have successfully established themselves in market applications where their superior properties over silicon give them a clear advantage. However, for classes of material such as wide and ultra-wide bandgap semiconductors, bulk defect densities can limit the performance and reliability of the systems, which in turn can slow or limit the rate of adoption into markets.

Examples of this are seen in the wide- and ultra-wide bandgap semiconductors GaN, SiC, AlN and diamond. With these materials, high levels of bulk defectivity threaten to seriously curtail power performance, as well as the quality of the crystal, which is critical to high-coherence quantum applications. SiC and GaN are clearly making an impact in power RF and power electronics markets, but there remains the persistent challenge of crystal quality, reliability and yield, particularly for very high power-density and voltage applications.

Progress continues, with crystal quality slowly improving, particularly in epilayer and two-dimensional material development. But it's still not possible to reliably grow inorganic crystal ingots with bulk defectivities on a par with silicon. This puts up barriers to market adoption.

Space Forge's approach

At Space Forge, we are taking an entirely new approach in the search for reliable, high-quality semiconductor crystals, by posing this question: What if there could be a way to produce CVD seed wafers with a quality that's at least two-to-three orders of magnitude better than what's currently available?

A promising answer to this question lies in a broad, but disparate body of evidence that shows that the conditions found in low earth orbits (LEOs) and beyond have a reliable, positive effect on the quality of crystal growth. Broadly, these conditions are: microgravity, very low temperatures and a high-quality vacuum. Of these three, microgravity is a driving factor – it has been shown to greatly reduce convection, and hence nucleation points, in gas-phase crystallisation in orbit. Also aiding inorganic crystal growth is the high-quality vacuum found in a LEO, ensuring very low levels of nitrogen. At typical LEO altitudes, the density of N_2 particles is less than 1×10^{12} m^{-3}, and even lower in the wake of satellites, as seen in the epitaxial demonstrations of the Wake Shield Facility flights.

Our mission is to establish the quality of material that can be produced in an LEO, when optimising the design and operation of the growth tool, so that this makes the most out of the benefits of these conditions in space.

The concept of conducting CVD growth in space gives rise to a series of complex engineering, manufacturing and cost challenges – so it's

important to focus on a relatively simple strategy for proof-of-concept and early scale-up. Based on these considerations, we are prioritising the in-space element of semiconductor growth to be as conservative as possible. Our motto is this: do only in space what only space can do. Consequently, our focus is on the quality of the crystal that can be grown in an LEO, and not the scale. Once that's accomplished, efforts will only be directed at conventional terrestrial semiconductor scale-up, exploiting returned high-quality space seeds.

Pursuing this approach, we have already sent a pilot semiconductor growth tool into space, which is currently orbiting the Earth in a free-flying satellite. Our ForgeStar-1, launched last June, is now carrying out initial feasibility tests of the pilot plasma-enhanced CVD system in the payload. Although our tool is small scale, designed to grow only a few millimetres of material, it is a first significant step in space, proving that we are capable of using our semiconductor growth tool in orbit. Once we have completed this stage, we will embark on a series of missions that involve scaling up our tool and beginning to fully understand the physics of inorganic crystal nucleation and growth in orbit.

The next step

The challenges of in-space crystal growth and return are considerable – not least optimisation of the size, weight and power within the payload, so that it is practical to reliably and repeatably grow inorganic crystals in space. Energy requirements for most types of in-space manufacturing are very much the 'elephant in the room', providing a barrier for embarking upon such ventures. Tackling this issue head-on, we are developing one of the highest energy-density satellites in the market, to enable the growth of in-orbit seeds. Our next iteration of spacecraft will feature a magnitude of power-generation that's normally reserved for telecommunication satellites, combined with the capability of returning from orbital velocities, something rarely seen outside crewed vehicles.

While working towards these goals, we will optimise the size, weight and power of our plasma-enhanced CVD tool. Our improvements in this regard are already leading to a significant innovation in energy efficiency that could even have an impact on purely terrestrial systems.

We are developing a tool capability that's flexible, and does not have to be on our satellite to work – it can be hosted in future systems, and be adapted to meet material or experimental needs of other customers.

Design for space

Within the space industry, the International Space Station (ISS) provides the principal platform for developing in-space manufacturing. Unfortunately, as well as being a highly problematic venue for growing compound semiconductors, it is

➤ The successful integration of ForgeStar-1 onto the SpaceX Transporter 14 mission.

decommissioning. This means that industry is moving to a private model, involving Commercial LEO Destinations that are expected to replace much of the functionality of the ISS. Due to this, we are working with a number of partners to host our systems on their platforms – a mutually beneficial arrangement as commercial platforms need viable commercial routes to be able to function, as long as they have the power density capabilities to be able to do so.

After growing our seed crystals in a LEO, we must return them to Earth. That's not necessarily as challenging as it may first appear, thanks to the highly competitive nature of space transport. Recently, a number of companies have emerged, such as Varda Space Industries in the US and Atmos Space Cargo in Germany. Both are individually developing ways to return satellites to Earth – although for these companies, the focus is on a low power density for pharmaceutical crystal growth. At present, we are working on an integrated approach with our own satellites, deploying a heat shield that acts as an aerostable means of return through the Earth's atmosphere, with the ability to predict and track low-impact landing zones.

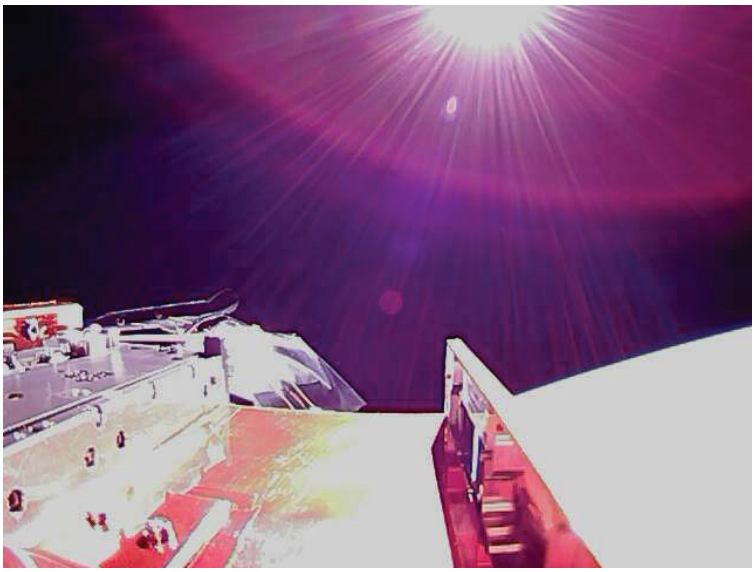
As the barriers to in-space manufacturing are overcome, the benefits of the orbital environment – and the technological developments required to exploit it – promise to help to solve challenges in terrestrial inorganic crystal growth.

➤ Space Forge is using the clean room at Centre for Integrative Semiconductor Materials at Swansea University.

Scaling up

The crux of our proposition – and that of any inorganic-crystal in-space manufacturing – is that the quality of our crystals is high enough that, when returned to Earth, provide seeds for significant high-quality scale up into a wafer stock. How good does this stock have to be? Well, good enough to displace terrestrially-seeded material in the market.

Based on these factors, we are involved in a number of needle-moving activities related to in-space metrology and growth control, investigating some of the key questions we can already anticipate. These questions are: What techniques and data are needed to understand *in-situ* and in-space measurement and optimisation? How do you achieve controllable and repeatable manufacturing with no real-time intervention? How do you model in-space microgravity growth, in order to reduce development cost and increase reliability? All these questions are being addressed.



➤ A view from ForgeStar-1's onboard camera in a low-Earth orbit.

On the ground we are tackling all the technical and business challenges that every compound semiconductor supplier has to meet. It is pointless producing high-quality seeds in an LEO unless this is followed with a terrestrial growth process that maintains initial crystal quality for as long as possible. We are currently incubating with the Centre for Integrative Semiconductor Materials (CISM) in Swansea to develop that capability. In addition, we are directing efforts at post-processing grown material, which provides the heart of engineered substrates, with an appropriate surface treatment that enables competitive products in the marketplace.

Given the challenges of growing wide- and ultra-wide bandgap materials on Earth, that's our initial target. Similar to the challenges faced by all materials providers in the compound semiconductor industry – both past and future – success is not as simple as just providing a high-quality solution with disruptive theoretical properties. What's needed to generate significant sales, is the adoption of our material in the supply chain, so that it is eventually part of a co-designed end-user system that justifies the cost and effort involved. To this end, we are already actively involved as a conventional materials supplier into power, RF, photonic and quantum projects.

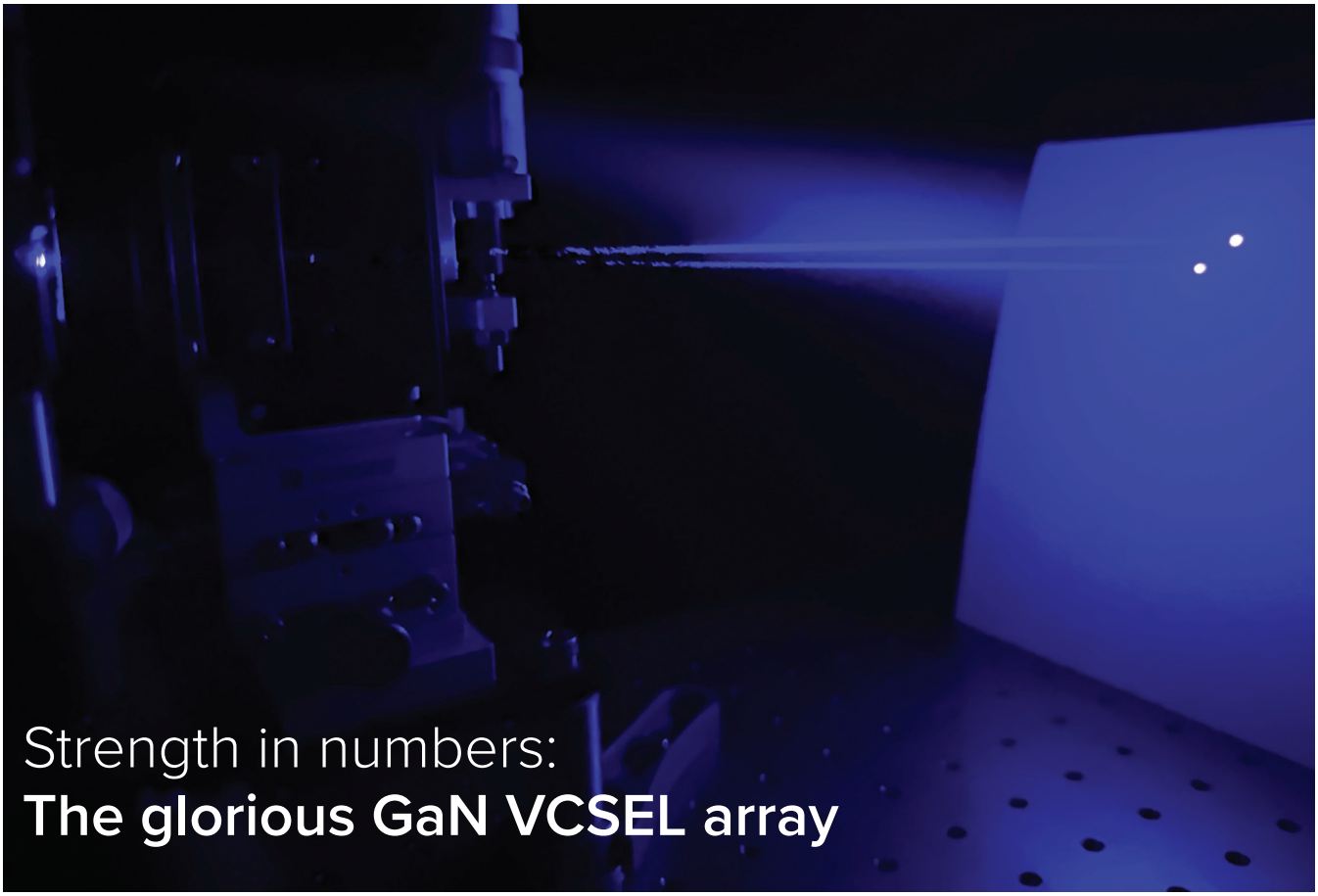
Into the future

If our approach to in-space manufacturing succeeds, what comes next? It's likely that our attention will turn to the development of new markets and applications that will be enabled by high-quality wide- and ultra-wide bandgap materials.

For example, once we have established ourselves in our initial target market of materials to assist with thermal management and integration at the package level, we could gradually move towards producing materials for active devices at the fab-level. Alternatively, we can begin to explore how our materials can support quantum applications.

We may also diversify our activities to other growth processes and materials, while maintaining our focus on systems where the quality of the bulk crystal drives end performance. Efforts on this front are already in their infancy, as we are involved in early discussions on the feasibility of non-linear optical crystal growth in orbit. Similarly, although alternatives to CdTe are being deployed as a material for solar cells, data on good growth of this material in orbit already exists and may be possible to expand once in-space manufacturing capability is in place.

However the future path of development unfolds, what's clear is that as the barriers to in-space manufacturing are overcome, the benefits of the orbital environment – and the technological developments required to exploit it – promise to help to solve challenges in terrestrial inorganic crystal growth.



Strength in numbers: **The glorious GaN VCSEL array**

GaN-based VCSEL arrays are emerging as a disruptive platform for next-generation displays, sensing, and optical communications, offering a unique combination of high brightness, spectral purity and scalability

BY KENTARO HAYASHI FROM SONY SEMICONDUCTOR SOLUTIONS

THE VCSEL is an indispensable source in modern optoelectronics, where it is valued for its high beam quality, low threshold current, and compatibility with wafer-level processing.

Unfortunately, today's commercial VCSELs tend to be restricted to the GaAs and InP material systems, confining their operation to the infrared. It is a limitation that holds back the number of applications where they can serve, and prevents their uptake in situations where a compact source emitting in the visible or ultraviolet is essential.

Overcoming this issue is the GaN-based VCSEL, which extends the spectral domain of this source into the visible and even the ultraviolet. Reaching these shorter wavelengths enables multiple GaN VCSELs, in the form of arrays, to be a disruptive technology – they can push boundaries in displays, sensing, lighting, and communications.

While commercial adoption of the GaN VCSEL is still in its early stages, rapid research breakthroughs are accelerating progress, bringing practical devices closer to reality.

Producing VCSELs with the GaN material system is challenging. Difficulties stem from the inherent complexities of GaN crystal growth and, in particular, the fabrication of mirrors – in this class of laser, they take the form of distributed Bragg reflectors (DBRs), providing the optical confinement necessary for lasing. Today it is relatively straightforward to manufacture the AlGaAs/GaAs DBRs deployed in infrared VCSELs, but it is far more challenging to construct those made from AlInN/GaN multilayers, the obvious candidate for GaN-based VCSELs. Here, there are significant hurdles to overcome when producing mirrors that combine a high reflectivity with a low defect density.

Helping to overcome these barriers are recent advances in epitaxial growth techniques, heterostructure design, and strain management. Researchers have demonstrated GaN VCSELs that deliver stable operation in the blue-violet, blue and

green, with output powers and lifetimes rapidly approaching practical levels. These milestones have established GaN VCSELs as not only a pathway to compact visible lasers, but as a foundation for entirely new device architectures.

Why arrays matter

While single GaN-VCSEL devices are already promising, their disruptive potential emerges when they are integrated into dense two-dimensional arrays, an approach we are pursuing at Sony Semiconductor Solutions Corporation, where we draw on our novel long-cavity GaN-based VCSEL technology.

Employing battalions of VCSELs in arrays enables a scalable output power, spatial beam shaping and multi-wavelength integration. These are much-valued advantages that extend well beyond the capabilities of individual emitters. For applications in microdisplays, adaptive lighting, optical communications and underwater sensing, array-level integration provides a versatile platform for next-generation light engines.

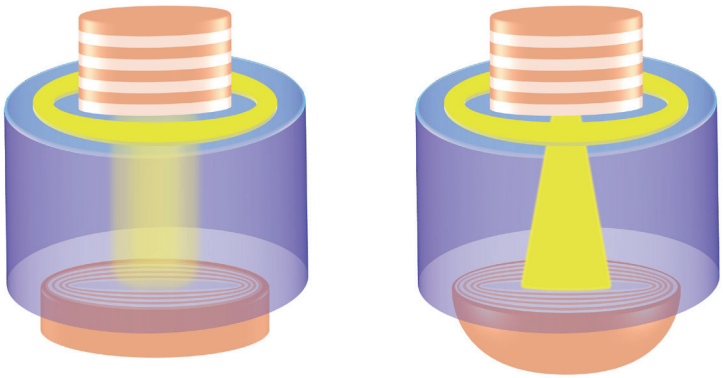
Unfortunately, scaling VCSELs into large arrays introduces new challenges, foremost among them thermal management. Despite the relatively high thermal conductivity of GaN substrates, densely packed arrays of VCSELs are prone to localised heating and thermal crosstalk. These issues impair efficiency, shift emission wavelength, and ultimately curtail device lifetime. Exacerbating these weaknesses are the epitaxial DBRs deployed in GaN-VCSELs – often based on AlInN/GaN multilayers – that are renowned for relatively high thermal resistances that magnify heat-dissipation issues.

To address these concerns, some researchers are exploring novel cavity architectures, alternative reflector designs and advanced packaging strategies aimed at trimming thermal resistance and ensuring stable operation under high drive currents. Such innovations are crucial to unlocking the full potential of GaN-VCSEL arrays, so that they can function as reliable, energy-efficient light sources across a wide spectrum of applications.

Fabricating arrays

A typical GaN-VCSEL array consists of: an *n*-type GaN layer, grown on a GaN substrate; an active region composed of multiple quantum wells (MQWs); a *p*-type GaN layer; and two high-reflectivity DBR mirrors.

One of the weaknesses of conventional VCSELs is their planar mirrors, which are to blame for significant diffraction losses as the cavity length increases. To address this, our design incorporates a concave mirror on one side of the cavity. The primary advantage of the concave-mirror cavity is its ability to effectively suppress diffraction losses. As illustrated in Figure 1, planar mirror structures ensure that optical modes spread outward, especially in long cavities, resulting in increased losses. In contrast, our design confines the optical mode tightly within the cavity, using a concave geometry that significantly reduces diffraction losses. With our design, we can extend the cavity length substantially without compromising performance.

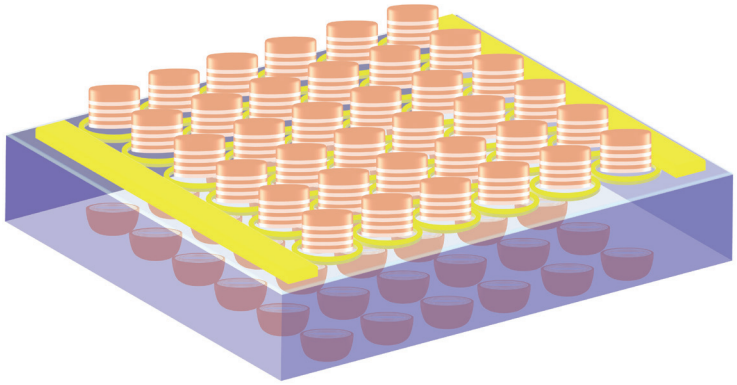


➤ Figure 1. Comparison of optical mode confinement in planar-mirror and concave-mirror VCSEL cavity structures. In the planar configuration, the optical mode tends to spread outward, especially in longer cavities, resulting in increased diffraction losses. In contrast, the concave-mirror design effectively confines the mode within the cavity, significantly reducing losses and enabling extended cavity lengths without performance degradation.

Our focus is on long-cavity designs. That's a noteworthy difference from the architecture of the conventional planar-mirror VCSEL, which typically employs a short cavity to prevent diffraction losses. The major downside of short cavities is that they lead to a wide longitudinal-mode spacing, which poses several challenges. For instance, the gain spectrum of InGaN MQWs is relatively narrow, with a value for the full-width at half-maximum below 20 nm, and even slight variations in cavity thickness can cause the longitudinal mode to deviate from the gain peak. This results in an increased threshold current and a lower yield. For a GaN VCSEL with a 2 μm cavity, engineers must ensure a thickness control within ±10 nm, an extremely difficult requirement when employing chemical-mechanical polishing on GaN substrates.

Adopting a concave mirror structure is a game changer. This allows the cavity length to be extended beyond 20 μm, and narrows the mode spacing to approximately 1 nm. With these changes, it is much easier to align the mode with the gain peak, an advantage that increases design tolerance and improves device yield. The opportunity to extend cavity length without sacrificing performance also enables each emitter in the array to deliver sufficient optical output, maximising the overall performance of the array.

Another advantage of our concave-mirror structures, with cavity lengths exceeding 20 μm, is that they have around half the thermal resistance of the



➤ Figure 2. Sony has produced a 456-emitter GaN-VCSEL array structure. Each emitter consists of a concave-mirror vertical cavity with an InGaN/GaN MQW active region, current confinement via B^+ ion implantation, and transparent ITO electrodes. The array is fabricated on a conductive GaN substrate with a device pitch of approximately 70 μm, enabling high-density integration and a uniform layout.

more common planar-mirror structures. Thanks to the superior thermal characteristics of the concave design, we enjoy structural advantages for high-power operation in array configurations.

Fabrication of our concave mirrors begins by forming a photoresist pattern on the back side of a GaN substrate. Subsequent heating transforms this resist into a spherical shape, thanks to surface tension. This spherical resist provides a mask for reactive ion etching, which transfers the desired curvature directly onto the GaN surface. We deposit a dielectric DBR multilayer directly onto the lens-shaped GaN surface to create a lens with a root-mean-square roughness of just 0.3 nm – this low value minimises scattering losses.

Our concave-mirror GaN-VCSEL includes an InGaN/GaN MQW active region for efficient blue emission. We then form a current-confining layer via B^+ ion implantation, a step that enables the fabrication of devices with a designed aperture diameter of 4 μm. The addition of indium tin oxide provides a transparent electrode, and ensures efficient *p*-side light extraction and lateral current spreading. Our DBR, consisting of 14 pairs of SiO_2/Ta_2O_5 on the *n*-side and 7.5 pairs on the *p*-side, provides high reflectivity. The *n*-side DBR is selectively removed by dry etching, except at the lens apex, prior to *n*-electrode deposition that optimises optical and electrical performance. With this design, light is primarily extracted from the *p*-side. Using this VCSEL architecture, we have fabricated arrays with 456 emitters and a device pitch of approximately 70 μm, an architecture providing a uniform layout and a high integration density (see Figure 2).

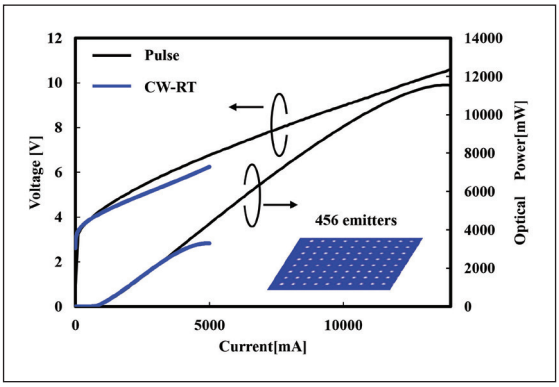
Measurements of this VCSEL-based 456-emitter array reveal that we can produce 2.8 W under CW operation and 11 W using pulsed conditions – that's with pulses with a duration of 5 μs, and a 5 percent duty cycle. These results demonstrate the scalability and high-power capability of our concave-mirror VCSEL architecture (see Figure 3).

Addressing the individual

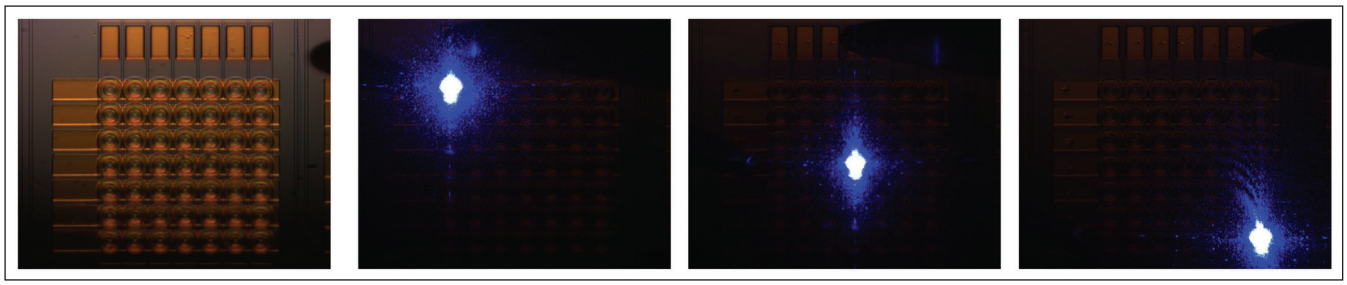
In lighting and displays, VCSELs offer a significant advantage over conventional LEDs, thanks to their narrow beam profiles, high output power and high-frequency operation. It's possible to produce compact lighting systems by combining blue light from a GaN-based VCSEL array with a yellow phosphor. One of the promises of this VCSEL-based lighting technology is that it could serve as a light source for optical communications in areas where Wi-Fi cannot be used. Meanwhile, if GaN-based VCSELs are deployed in displays, they could enable a wide colour gamut and high brightness, making these sources suitable for outdoor signage and advanced display systems. Critical to the realisation of both these applications is pixel-level light control via addressable arrays.

To achieve individual addressing, we employ passive matrix technology. This is a type of display technology where a grid that's defined by a vertical and horizontal metal line provides pixel control. By activating each VCSEL at the intersection of row (*p*-electrode) and column (*n*-electrode) lines, we ensure efficient wiring and scalability.

One requirement for applying passive matrix technology is electrical isolation. We accomplished this by inserting a semi-insulating layer beneath the VCSEL structure to provide vertical isolation, and by introducing mesa structures to ensure lateral isolation between pixels. Using this technology, alongside our grid with metal lines, we fabricated a 7 x 7 VCSEL array with individually addressable elements that demonstrates selective pixel activation.



➤ Figure 3. Current-voltage-output power characteristics of the GaN-VCSEL array measured at room temperature. The array exhibits threshold currents and slope efficiencies comparable to single-emitter devices. A total optical output of 11 W is achieved under pulsed operation (pulse: on 5 μs, off 95 μs, duty 5 percent), and 2.8 W under CW operation, demonstrating the high-power scalability of the array architecture.

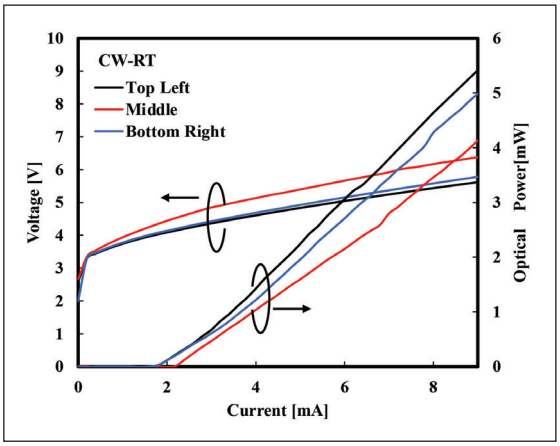


➤ Figure 4. Passive matrix wiring structure is employed in the VCSEL arrays. Here is shown the emission mode for individual VCSEL driving. Current injection is 3 mA, under room-temperature CW operation.

Operation of our VCSEL array involves current injection at the intersection of selected row and column electrodes, corresponding to the *p*- and *n*-electrodes of each VCSEL, respectively. Under room-temperature CW operation with an injection current of 3 mA – that's less than 1.5 times the threshold current – we have produced selective emission, confirming the feasibility of passive matrix addressing (see Figure 4).

After packaging our full 7 x 7 array, we recorded current-voltage and current-output power characteristics, far-field patterns, and emission spectra under CW operation at room temperature. Although measurements were performed for all 49 emitters, here we share the results from just three locations within the matrix to illustrate performance variation across the array (see Figure 4, which shows the results from the VCSELs positioned at the top-left, centre, and bottom-right. Note that the top-left emitter is positioned closest to the probe contact pad, while the bottom-right is the farthest away from this pad).

Measurements on these three particular VCSELs have threshold currents of around 2 mA; and at 4 mA injection, optical outputs of 1 mW for operating voltages between 4.6 and 5.1 V (see Figure 5). Slope efficiency is 0.67-0.8 W/A. These results confirm a uniform electrical and optical performance across the array. To evaluate the emission profile, we have considered the far-field pattern. Its full-width at half-maximum ranges from 6.5° to 7.6°, with



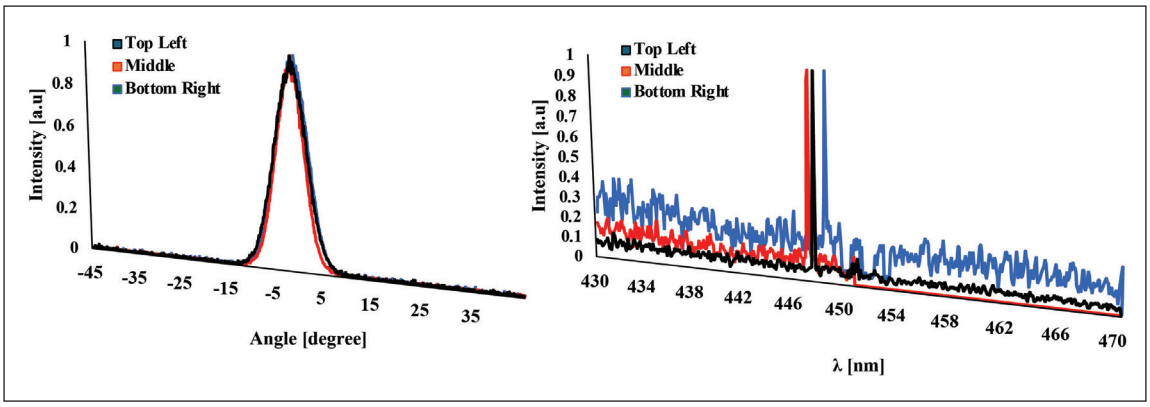
variation attributed to differences in the radius of curvature of the fabricated concave mirrors. Emission wavelengths are consistently centred around 447 nm across all emitters, demonstrating excellent spectral uniformity and mode control (see Figure 6).

Our efforts will now focus on producing high-output arrays, capable of delivering more than 1 W per illumination zone, as well as high-resolution, energy-efficient arrays with more than 100 individually addressable channels.

Next-generation light sources

Given the great promise of GaN-VCSEL arrays, it's not surprising that they are strong candidates for next-generation light sources, as they offer

➤ Figure 5. Current-voltage-output power characteristics of individually addressable GaN-VCSEL array elements measured at room temperature. Each emitter shows a threshold current and slope efficiency comparable to single-emitter devices, confirming uniform electrical and optical performance across the array.



➤ Figure 6. (left) Far-field emission pattern of selected VCSEL elements, showing beam divergence angles (FWHM) between 6.5° and 7.5°, attributed to the variation in radius-of-curvature among devices. (right) Emission spectra of array elements, with peak wavelengths consistently centered around 447 nm, demonstrating excellent spectral uniformity and mode control.

advantages in brightness, spectral purity and energy efficiency over conventional LEDs and laser projectors. In particular, these arrays are attractive contenders for compact, high-performance light engines in microdisplays and AR/VR devices, where it is critical to deliver high luminance and efficiency within limited volumes. There are significant concerns surrounding today's mainstream approach based on microLEDs and waveguide optics – this technology faces a number of inherent challenges, including Lambertian emission profiles and broad spectral bandwidths, which can reduce optical coupling efficiency and give rise to colour dispersion artifacts, such as rainbow effects.

Another significant impediment of the microLED is that its performance plumets when its pixel size shrinks below around 10 µm, due to enhanced non-radiative recombination at etched sidewalls that drags down the external quantum efficiency. Thanks to their vertical cavity geometry, VCSELs are less sensitive to sidewall effects, equipping them with the potential to maintain high efficiency, even when the pixel pitch is below 10 µm. This attribute enhances the appeal of GaN VCSELs for future high-resolution AR displays.

There are a number of products that combine MEMS scanners with infrared VCSELs, including AR display modules, lidar, and compact projection systems. Offering an alternative source is the GaN-based VCSEL array. While this is yet to be realised in practical MEMS-scanned light engines, it offers several unique advantages. Unlike its edge-emitting siblings, which are inherently one-dimensional emitters requiring additional optics for two-dimensional scanning, the VCSEL can be fabricated as two-dimensional arrays with high uniformity and addressability.

The circular, low-divergence beam produced by the VCSEL is well-suited for efficient coupling into MEMS scanners, and wafer-level fabrication enables integration with photonic and micro-mechanical components. These attributes suggest that GaN-VCSEL arrays may provide compact, scalable, high-resolution light sources for future AR glasses, head-mounted displays, and compact lidar systems.

Furthermore, the GaN material system is capable of realising blue and green VCSELs, creating opportunities for multi-wavelength light engines – although realising full-colour emission still requires integration with red-emitting devices from another material platform.

Another opportunity for the GaN-based VCSEL is in underwater lidar, where efficient emission in the blue-green is highly valued, due to the low absorption of water in this spectral domain. When combined with MEMS scanning, such sources promise to provide compact, wide-angle underwater sensing systems for marine exploration and robotics.

Yet another potential application for the GaN-VCSEL array is visible light communication. Thanks to high-speed modulation and narrow spectral linewidths, GaN VCSELs could serve as efficient transmitters, with potential applications in short-range optical links, such as data centre interconnects, smart home networks, and IoT devices.

There is no doubt that the GaN-VCSEL arrays holds significant promise for next-generation light sources, with the potential to drive innovation across displays, sensing, lighting, and communication. The evolution of this attractive source along three key axes – high output power, multi-wavelength integration, and dense array scalability – equips it with the opportunity to fundamentally reshape optoelectronic systems.

As this class of laser technology matures, progress will depend on close collaboration across materials science, device engineering and system integration. With advances in efficiency, miniaturisation and addressable control, GaN-VCSEL arrays are poised to underpin future high-resolution AR displays, adaptive lighting, underwater sensing and high-speed optical communication, demonstrating not only their technical impact but also their broader societal value.

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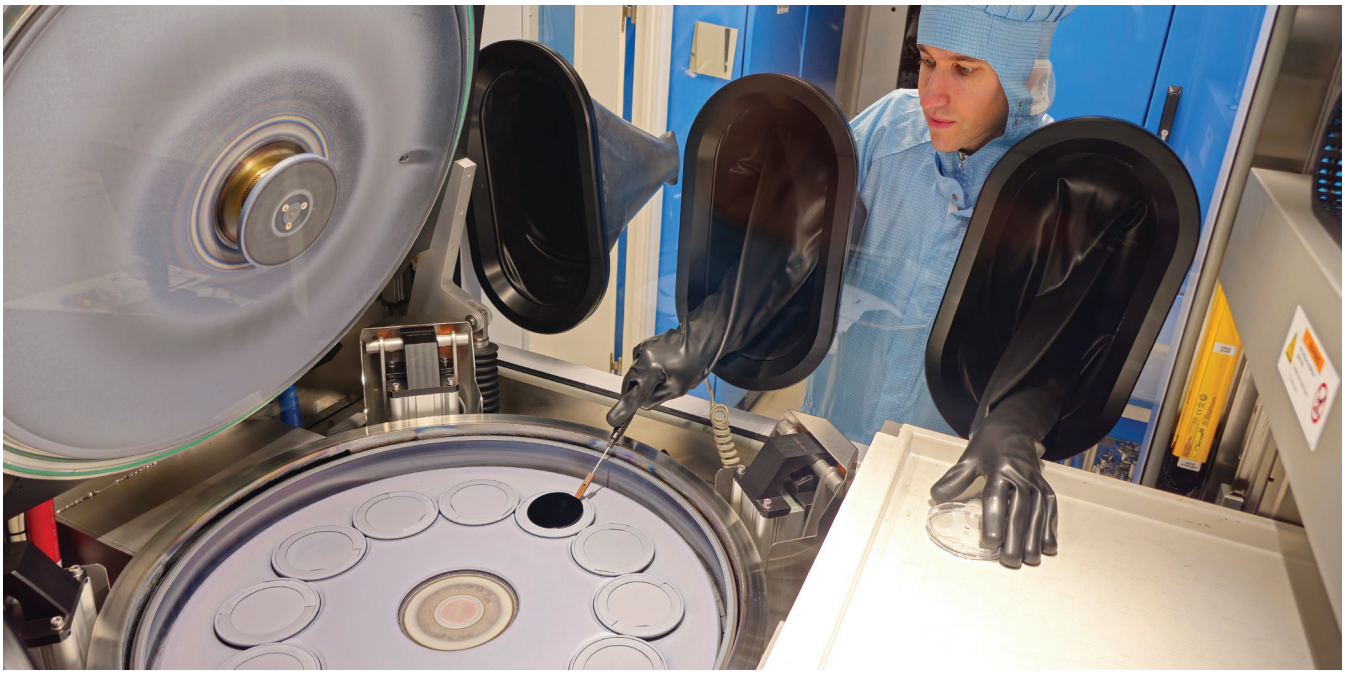


Optical metrology in VCSEL processing

By drawing on optical metrology data across the entire VCSEL manufacturing process chain engineers improve their capability to target precise wavelengths and boost yield

BY ANDRE MAAßDORF, MORITZ BRENDEL, ANDREAS RENKEWITZ, RALPH-STEPHAN UNGER AND MARKUS WEYERS FROM FERDINAND-BRAUN-INSTITUTE (FBH) AND JOHANNES ZETTLER AND KOLJA HABERLAND FROM LAYTEC

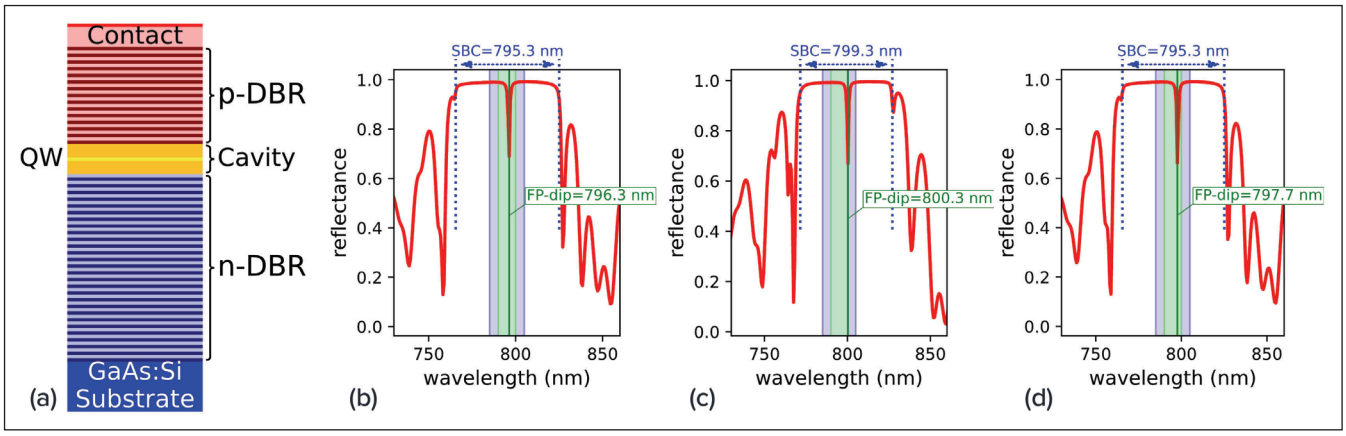
THE VCSEL, a well-established class of laser that's generating substantial sales, is enjoying success in an increasing number of applications. Most of this revenue comes from providing a light source for facial recognition in smartphones, and in datacoms, where it's valued for its high-modulation rate.

In both these applications, the wavelength of the emission is not that critical – but that's not the case in space applications, like highly sensitive nuclear magnetic resonance gyroscopes. Critical to the operation of these gyroscopes are single-mode lasers emitting at exactly 795 nm, a wavelength that ensures pumping and probing of a rubidium gas cell. This cell is key to sensing rotation and ensuring accurate altitude control in small CubeSats, capabilities that are not possible with today's state-of-the-art technology.

To ensure that the pump/probe configuration works, the VCSEL's operating wavelength must be within a ±1 nm tolerance window, centred around the central wavelength of 795 nm. This requirement dictates that the VCSEL cavity resonance wavelength, also called Fabry-Pérot or FP wavelength, must be precisely within this window. Note that the FP wavelength is a result of the etalon effect – and it's essentially defined by details surrounding the round trip that light takes inside the cavity, formed by bottom and top mirrors separated by a distance of a few hundred nanometres. So, to be able to meet demanding wavelength accuracy requirements, epitaxial engineers must fulfil a thickness accuracy requirement, and ultimately grow a stack of epilayers with sub-nanometre-precision.

Our partnership between the Ferdinand-Braun-Institute and LayTec has been considering these requirements, along with their implications. This has led us to consider this important question: what does sub-nanometre-precision actually mean, and how can we get there by using and combining the different optical metrology systems available across the production chain? In the remainder of this article we offer an answer to this key question.

Let's begin by illustrating the precision requirements, by looking at a simulated white-light reflectance spectrum of a typical top-emitting VCSEL layer sequence, illustrated in Figure 1. We can simulate



➤ Figure 1. Simulated white light reflectance (WLR) response in normal incidence for the VCSEL layer sequence (a), consisting of the lower *n*-type doped DBR (blue layers), the cavity layers including the quantum wells (QWs, yellow) and a *p*-type doped top DBR (red layers). (b) Reference spectrum. (c) *n*-DBR layers detuned by +1 nm. (d) Upper cavity layers detuned +3 nm.

the white-light reflectance response for the VCSEL layer sequence, considering normal incidence from the top surface.

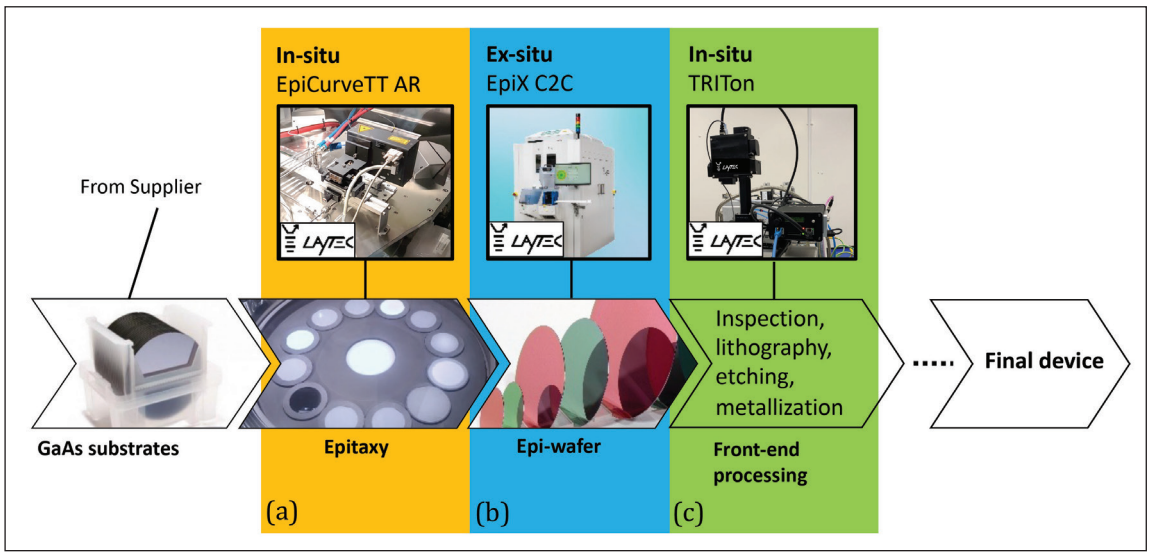
There are two characteristic features in this response: the spectral position of the stop band centre wavelength (SBC), and the so-called FP-dip wavelength. When thicknesses within the VCSEL structure change, the SBC and the FP-dip are shifted. For example, if we increase the *n*-DBR period thickness by 1 nm (see Figure 1(c)), we red-shift the FP-dip by 4 nm. Less impactful, but nonetheless similarly important, is what happens when we increase the cavity thickness above the quantum well by 3 nm (see Figure 1 (d)). With this change the FP-dip red-shifts by only about 1 nm. These results make the point that to ensure a FP-dip sits well inside the ±1 nm target window, the layer thicknesses in the DBRs must be grown with sub-nanometre precision.

So far, we have focused on precision requirements. Now let's delve into the implications, considering the case of growing the VCSEL structure shown in Figure 1 by MOCVD. According to our experience, we can expect the precision associated with growth rates to usually be in range of ±1 percent. Imagine we want to grow a 6000 nm-thick GaAs layer. Based on knowledge of the growth rate from a previous, sufficiently recent growth process, we will be able to grow a GaAs layer with a thickness of around (6000 ± 60) nm. For a VCSEL with a total thickness of 6 μm and a distributed Bragg reflector with around 60 periods in total, each period would be off by 1 nm at worst.

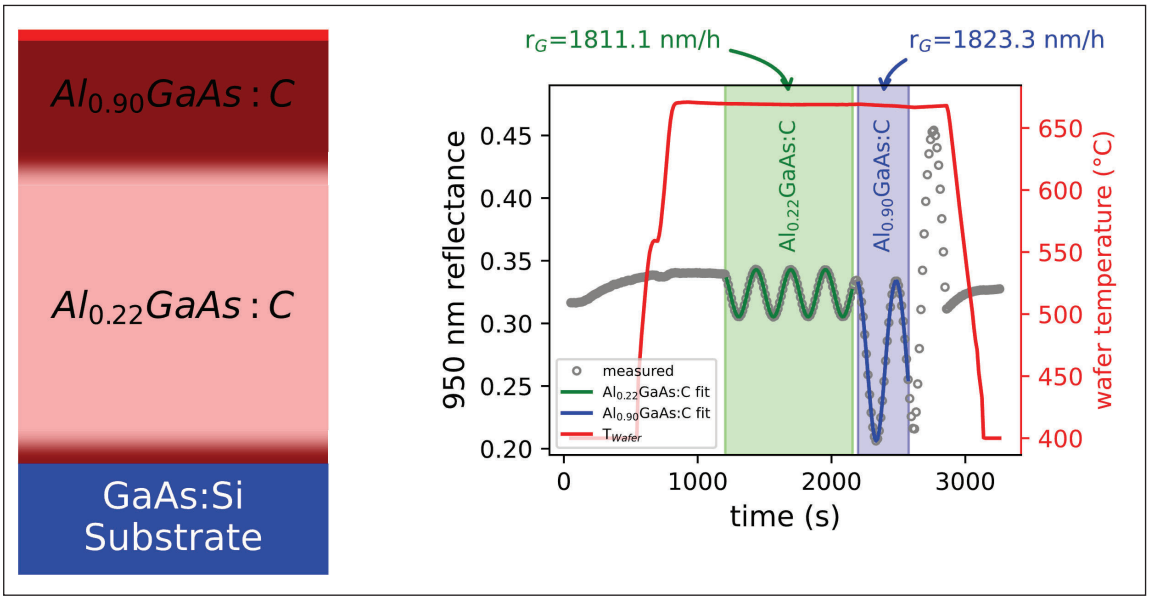
Unfortunately, our simulations show that a 1 nm detuning in thickness for just the n-DBR periods produces a 4 nm detuning in the FP-dip (Figure 1(c)). So, we must have a growth rate accuracy that's far better than ±1 percent. We accomplish this challenging requirement by heavily relying on optical metrology during (*in-situ*) and after (*ex-situ*) the growth process.

Combining metrology systems

We have several optical metrology systems employed for our VCSEL fabrication process (see Figure 2).



➤ Figure 2. Different metrology systems across the VCSEL production chain: (a) *In-situ* reflectance, temperature and curvature during growth; (b) *Ex-situ* WLR mapping after growth; (c) *In-situ* reflectance during plasma etch.



➤ Figure 3. *In-situ* growth rate determination from reflectance transients: (left) Schematic layer sequence showing a two-layer stack on a silicon-doped GaAs substrate; (right) oscillating 950 nm reflectance transient (symbols), with the oscillations caused by the layer thickness steadily increasing during epitaxial growth.

One of these systems gathers *in-situ* reflectance data during growth (see Figure 2 (a)). We have tracked the 950 nm transient during the growth of two layers that subsequently provide the quarter-wave layers in the superlattice periods that form the DBRs in our VCSELs: $Al_{0.22}Ga_{0.78}As$ and $Al_{0.90}Ga_{0.10}As$.

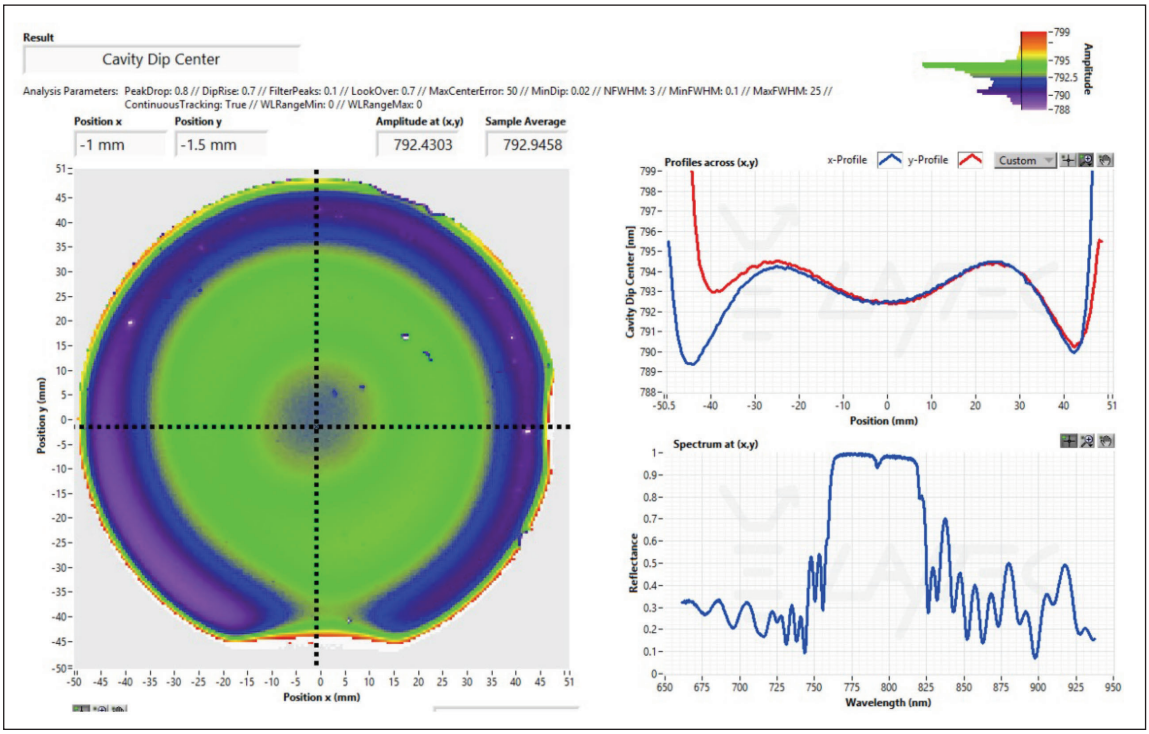
Information buried within the Fabry-Pérot oscillations of the reflectance profile reveals the speed each layer thickness is increasing. By using a virtual interface approach to model these oscillations, we calculate this speed, usually referred to as the growth rate. Values for two determined growth rates are provided at the top in the viewgraph on the right in Figure 3.

Within Figure 2, also shown is the *ex-situ* WLR mapping instrument – it's part (b). Used after epitaxial growth, this tool records the optical response at each position on the wafer, following illumination with white light at normal incidence (see Figure 4).

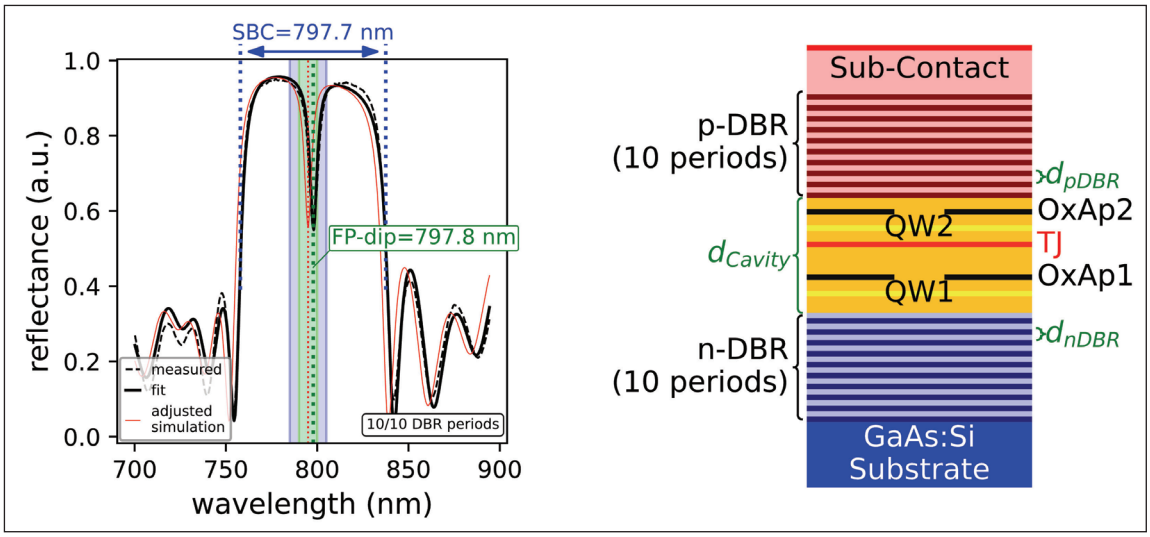
Calibration scheme

Our WLR mapping data is incredibly useful. As well as helping to evaluate and optimise the homogeneity of the SBC and FP-dip, it plays an important role in our calibration scheme, which begins with the growth of a shorter version of the full VCSEL layer sequence. For this trimmed-down epistructure, the number of superlattice periods for both the top and the bottom DBR is decreased to just 10 periods (see the right of Figure 5).

This alteration trims the epitaxial growth time from



➤ Figure 4. White-light reflectance mapping providing a full spectrum (bottom right) at each position on the wafer.



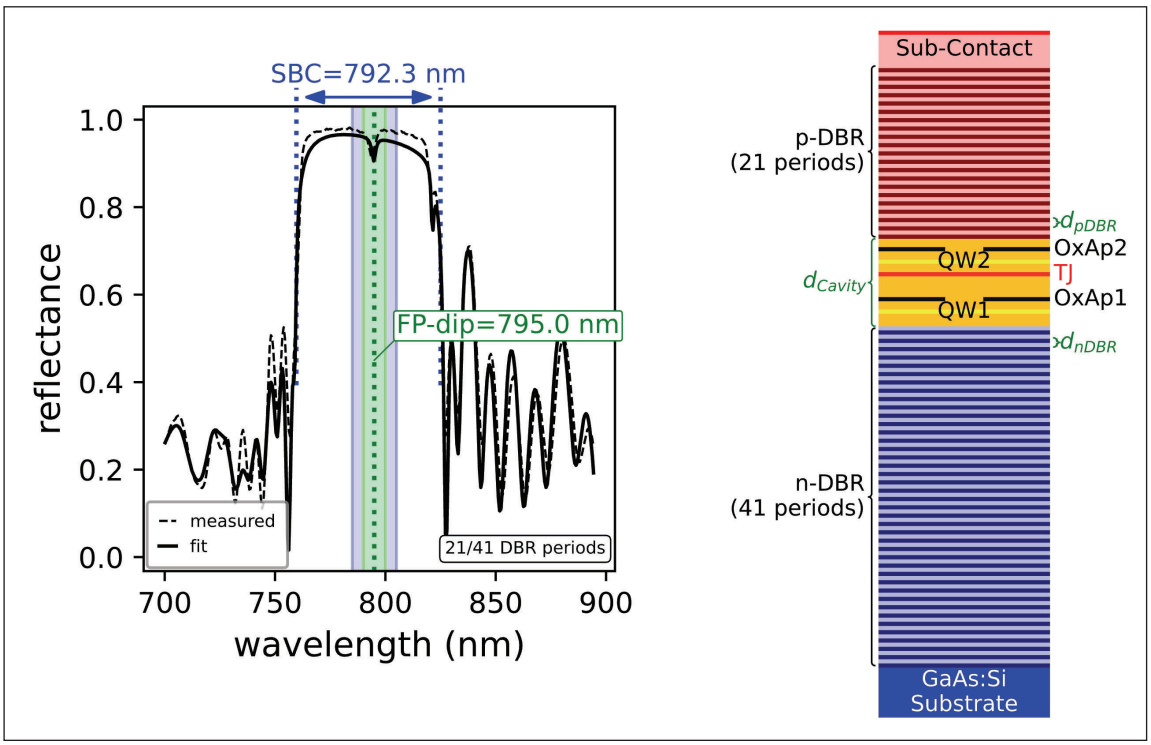
➤ Figure 5. Measured (dashed) and modelled (solid) WLR spectra of the shortened VCSEL layer sequence, as shown in the schematic on the right.

6 hours or so to less than 3 hours, while maintaining the strong features in the WLR spectrum (see the left of Figure 5).

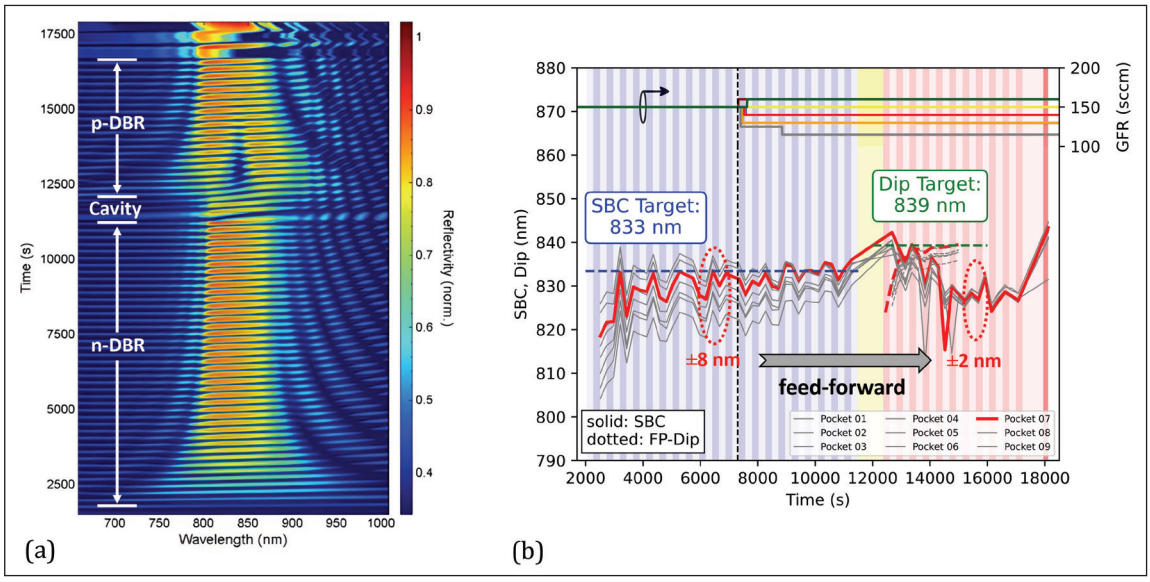
We use the measured WLR spectrum to fit the modelled counterpart, varying the DBR period thicknesses for top and bottom DBRs individually, as well as the cavity thickness. With this method we are unable to accurately determine the two quarter-wave layer thicknesses individually, as they are not represented by a strong feature in the WLR spectrum. Due to this limitation, we draw on previous values for growth rates (see Figure 3). This involves assuming that the ratio of the two quarter-wave layers is equal to the ratio of the two growth rates – it is a reasonable claim, so long as we use exactly same growth conditions for the two-layer sample described in Figure 3, and the DBR layers in the shortened VCSEL layer sequence, detailed in Figure 5.

Using this fitting to the model, we have determined cavity and DBR thicknesses. In the example we are sharing, the SBC and FP-dip wavelengths are about 3 nm above the target wavelength of 795 nm. So, we change the model parameters, adjusting the DBR thicknesses by -0.5 nm, equally distributed across the two quarter-wave layers, as well as the cavity thickness by -3.2 nm, also equally distributed across the individual layers around the quantum wells. We obtained these values by gradual adjustment and simulation, closing in until the simulated spectral profile is exactly centred around the target wavelength.

Following this, we applied changes to the growth recipe, along with an increase in the number of



➤ Figure 6. Measured (dashed) and modelled (solid) WLR spectra of the full VCSEL layer sequence, shown in the schematic on the right, with the delta changes applied to the growth recipe, as determined from the model in Figure 5.



➤ Figure 7. *In-situ* feed-forward procedure based on spectral WLR VCSEL analysis during growth and per-satellite adjustment of the gas-foil rotation flow rate in order to homogenize the wafer to wafer spread for SBC and FP-dip.

repeats for top and bottom DBRs, to 21 and 41, respectively. The measured WLR spectrum of this full VCSEL structure is nicely centred around the target wavelength (see Figure 6).

This completes the procedure that we use to nail the target wavelength for one wafer.

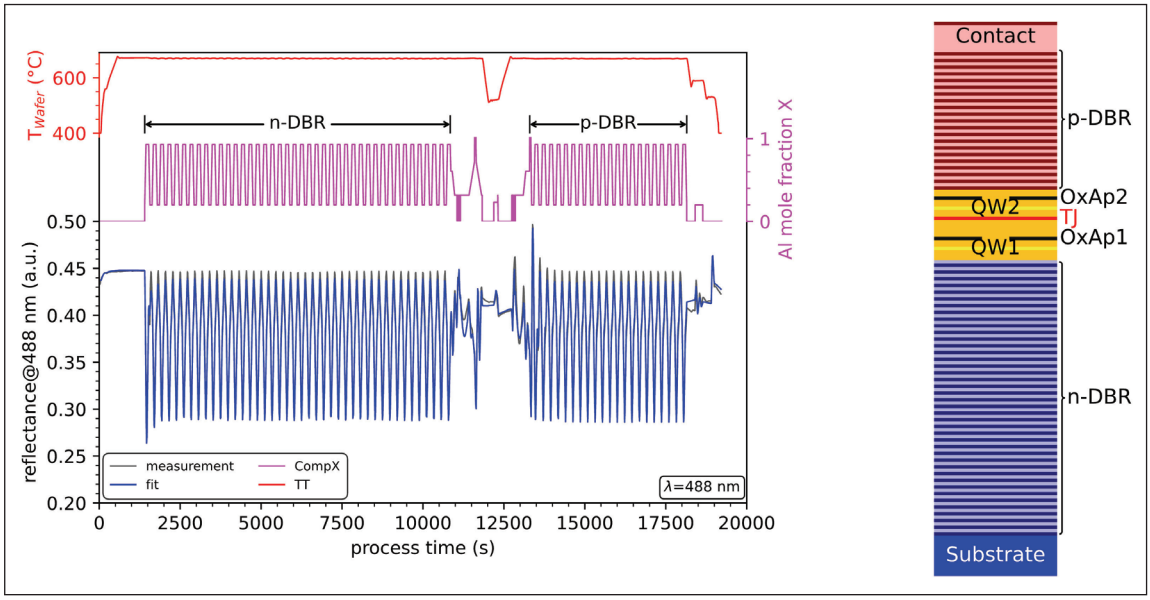
In-situ feed-forward

As our MOCVD has the capacity to accommodate 12 wafers in one process, we must ensure that all the wafers are on target.

We have shown that we can accomplish this goal. This is possible because reflectance data is measured for each wafer individually. Figure 7 (a) shows the colour-coded reflectance data for one wafer as an example. In these kinds of plots, wavelength-resolved reflectance is represented by horizontal lines, stacked along the vertical time axis to provide transient information for those spectra. Inspection of these plots reveals unique signatures during *n*-DBR, cavity and *p*-DBR growth. Analysing these signatures in real-time yields transient data lines (see Figure 7 (b)) for the SBC (solid) and the FP-dip (dashed) for each wafer.

Based on *in-situ* analysis (not shown) of the shortened VCSEL growth as part of the calibration scheme explained earlier, we know the target wavelengths for SBC and FP-dip at the growth temperature (this is indicated by the blue and green dashed lines in Figure 7 (b)). Due to a technical limitation of our metrology set-up, we are only able to monitor 9 of the 12 wafers with full spectral transient analysis. Now, if any of the SBC transients of our wafers is offset from this target during *n*-DBR growth, we can make online adjustments. The changes provide corrections to the subsequently grown layers and the FP-dip, with success revealed once the *p*-DBR starts growing.

To carry out our online adjustments, we make use of the so-called gas-foil rotation (GFR). Within our



➤ Figure 8. Measured (grey) and simulated (blue) 488 nm reflectance transient during growth of the VCSEL layer sequence already shown in Figure 6.

Another opportunity that's open to us is to draw on the full reflectance transient recorded during growth of the VCSEL layer sequence and undertake a full-stack simulation and fit. This exercise allows us to determine all the layer stack parameters

MOCVD system, there are 12 graphite wafer carriers – also known as satellites – all put into rotation by hydrogen gas, spirally flowing in a gap below the carrier, from the centre to the outside. As well as causing the carrier to rotate, the spiral motion of the gas produces partial mixing and dilution of the main process gasses flowing on top of the carrier across the wafer. This dilution slightly affects growth rate. That can be to our advantage, as by varying the GFR flow rate, we can fine-tune the growth rate.

The benefits of individual GFR flow rates are evident in Figure 7 (b), which includes GFR profiles (top right). By comparing the SBC spread during *n*-DBR growth, and before and during *p*-DBR growth, one can see that by applying adjustments to the GFR flow rates during growth of the *n*-DBR, we decrease the spread from ±8 nm to ±2 nm – that's a significant improvement.

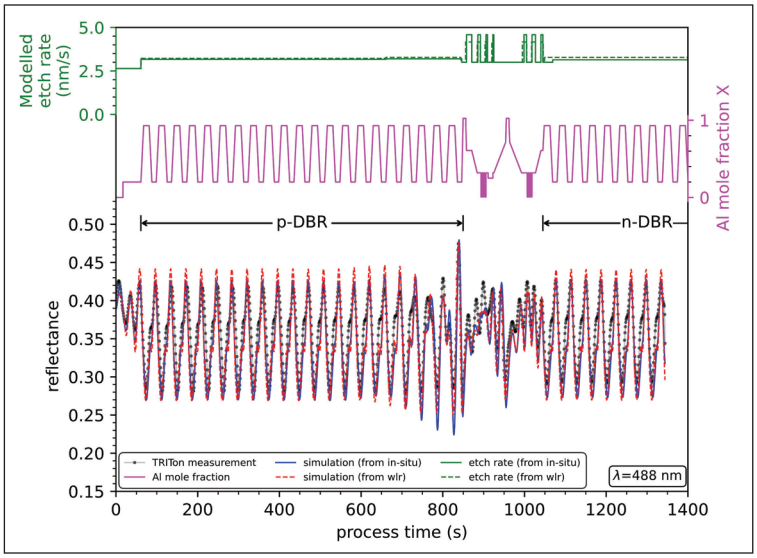
Another opportunity that's open to us is to draw on the full reflectance transient recorded during growth of the VCSEL layer sequence (see Figure 6), and undertake a full-stack simulation and fit. This exercise allows us to determine all the layer stack parameters. The result of this model fit is shown in Figure 8. You can see that the fit provides a good representation of the measured transient. One can benefit from this knowledge when undertaking front-end processes on the grown wafers.

Connecting growth and etch

One of the critical steps in VCSEL processing is the formation of a mesa, defined by etching down to the bottom DBR and precisely stopping below the active region. This step takes place before forming a current aperture by wet oxidation of a layer with high aluminium content. Again, optical *in-situ* metrology is used to monitor and control the plasma etching process.

Based on full-stack simulation, we can use that layer stack, remove all growth interruptions and calculate the transient in the reverse direction – now starting at the surface and progressing towards the substrate. Similarly, we can do the same with the layer stack obtained with WLR analysis (see Figure 6), and calculate an expected transient.

Shown in Figure 9 is a comparison of two predicted 488 nm transients. One is from the *in-situ* transient analysis (Figure 8); and the other from *ex-situ* WLR analysis in Figure 6, shown together with the actually measured 488 nm transient during plasma etch of the VCSEL mesa.



As you can see, both approaches produce a reasonably good agreement with the measured etch transient. The implication is that by using the knowledge gathered during epitaxial growth, it's possible to implement feature-based end-pointing in plasma etching. For non-periodic layer sequences, such as those found in edge-emitting lasers, this approach is even more powerful, as there are far fewer interfaces from which one could deduce the approximate depth. Note also that for these non-VCSEL-like structures, such as the layer structures found in edge-emitting lasers and devices with similar layer sequences, the WLR profile tends to be devoid of any strong features. Due to this, the only viable way to deduce the layer stack parameters is full-stack transient reflectance analysis (see Figure 8). Thus, this connected way of utilising metrology is currently expanded to non-VCSEL-like structures.

➤ Figure 9. Measured (grey symbols) and modelled 488 nm transients during plasma etch of the VCSEL layer sequence shown in Figure 8.

FURTHER READING

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- E.A. Donley, "Nuclear Magnetic Resonance Gyroscopes", IEEE Sensors Conference, 2010
- W. G. Breiland *et al*. "A virtual interface method for extracting growth rates and high temperature optical constants from thin semiconductor films using in situ normal incidence reflectance" J. Appl. Phys. **78** 6726 (1995)

Nitrides below the tip of the iceberg

Discoveries of new nitride materials are expanding the semiconductor landscape beyond the GaN family

BY ANDRIY ZAKUTAYEV FROM THE NATIONAL LABORATORY OF THE ROCKIES

BY NOW, you have likely heard of AlScN. If not, it is worth paying attention: it is a ferroelectric nitride that has become a prominent topic in compound semiconductor research. Yet, if one asks the community to provide an overview of nitride semiconductors, most would immediately point to GaN, the material that revolutionised LEDs and is now transforming telecom and defence applications.

However, whether the focus remains on GaN or expands to include AlScN, the discussion may still be confined to only the tip of the nitride iceberg. That is my perspective – and the one that I hope may resonate with other researchers as community interest in emerging nitride materials grows. What follows is an overview of the broader and still-developing landscape of novel nitride semiconductors.

For many decades, GaN and its semiconductor alloys have dominated nitride device research. In 2014, InGaN was recognised with the Nobel Prize in Physics for its role in LED development, helping to drive an energy-efficient lighting revolution. Since then, AlGaN HEMTs have played a crucial role in defence and telecom industries and are now expanding into other applications. However, despite continued advances in these GaN-based materials, there is growing recognition that they represent only a fraction of the broader nitride semiconductor materials space.

More recently, AlScN has risen to prominence in semiconductor research. Ferroelectric switching in this polar nitride was reported a few years ago in Germany and has since attracted significant attention around the world. Device engineers are now exploring its potential as a dielectric barrier layer in HEMTs to increase channel charge density, as well as in switchable ferroelectric field-effect

transistors for non-volatile memory applications. Notably, although AlScN is considered a relatively new ferroelectric nitride for semiconductor devices, it has been used for more than a decade as a piezoelectric material in tunable RF filter applications in the telecom industry. Despite this long-term piezoelectric history and the recent ferroelectric breakthrough, it is unlikely that AlScN represents the final stage of nitride semiconductor materials development.

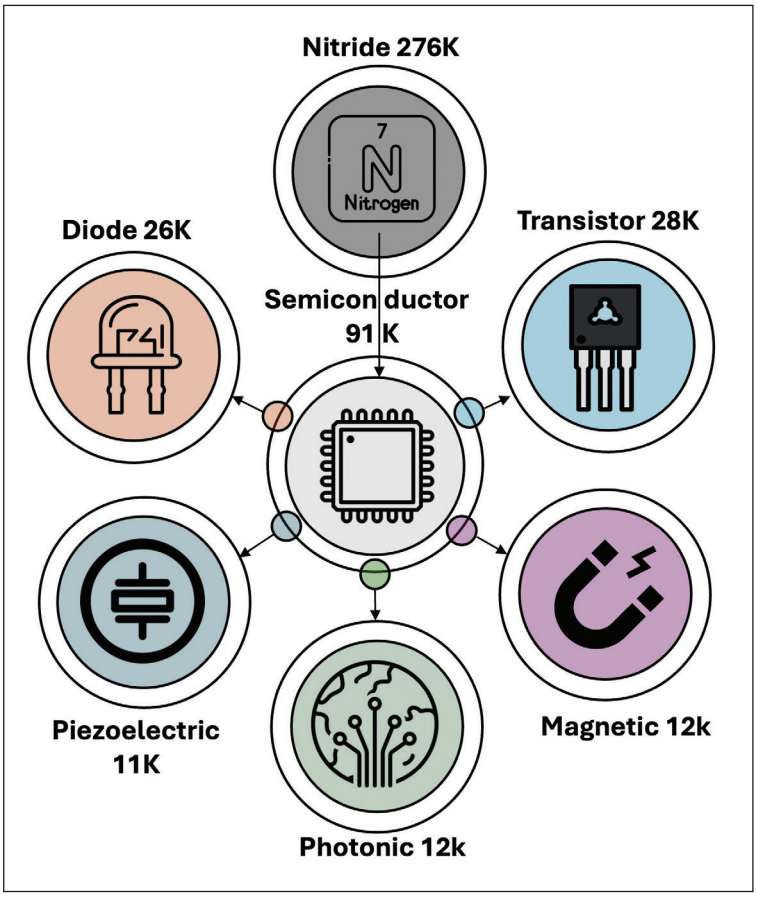
Less visible, but equally important, are advances in fundamental materials chemistry that are laying the groundwork for a wide range of new nitride discoveries. Researchers in this area have predicted and synthesized numerous novel nitride compositions and structures, some exhibiting highly tunable electronic, and even quantum, properties. This raises an important question: what lies beneath the GaN tip of the nitride iceberg?

Below the tip of the iceberg

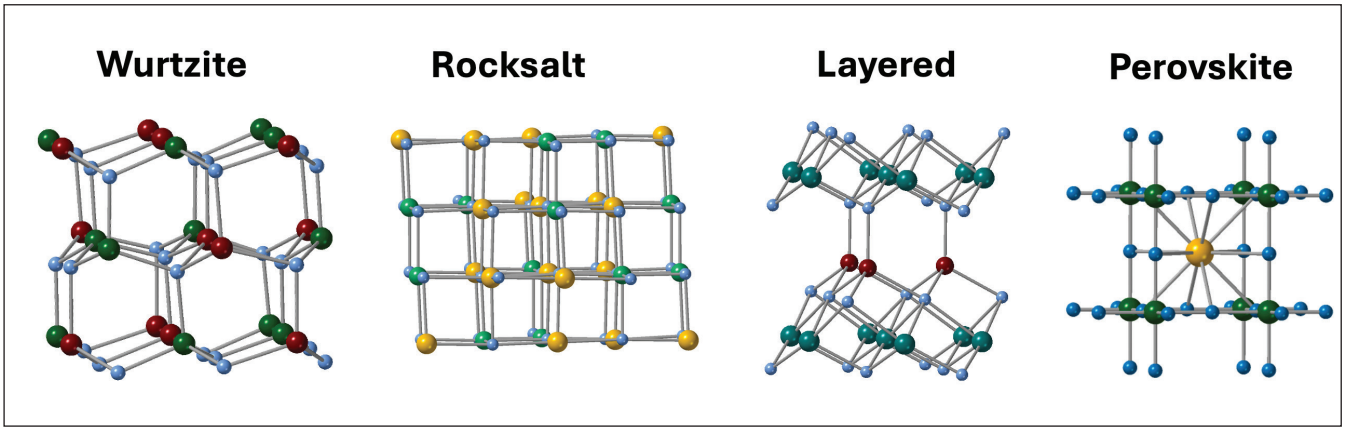
Contrary to common perception, nitride semiconductors are not limited to III-N compositions such as GaN. For example, $ZnGeN_2$, part of the II-IV-N_2 family, offers the potential for bandgap tunability through cation ordering at a fixed lattice constant. This approach may provide a pathway to addressing the miscibility gap challenges encountered in InGaN for green and amber LEDs.

The II-IV-N_2 family extends beyond $ZnGeN_2$ to include compounds such as $MgSiN_2$, $ZnTiN_2$, Mg_2SbN_3, Zn_2NbN_3 and Zn_3MoN_4, all of which show potential for tunable optical performance.

While nitride semiconductors are often associated with wurtzite structures, this is not their only crystallographic form. Recently, rocksalt nitrides such as $MgZrN_2$ and Mg_2NbN_3 have emerged as wide-bandgap semiconductors. Despite possessing indirect bandgaps and non-polar structures, unlike the wurtzite nitrides, these materials may find roles as barrier layers in



➤ The research on nitrides already extends beyond diodes and transistors to include their piezoelectric, magnetic and photonic applications. The number next to each icon corresponds to the number of research articles with the word 'nitride' and the corresponding application keywords, in the title/abstract/keywords of the papers. For example, 276,000 (276K) is the number of papers mentioning the word 'nitride', the middle number of 91K is the number of papers talking about nitride semiconductors, the number of papers about nitride diodes or LEDs is 26K, on so on.



➤ Beyond the well-known wurtzite-derived structures of AlGaN or InGaN, nitride semiconductors feature other crystal structures under research, including rocksalt-derived, layered (such as wurtsalt, nickeline), and most recently perovskite. Each of these structures contains two distinct metal atoms with different charge marked by orange or red, and a nitrogen atom marked blue.

quantum devices, including Josephson junction qubits. Although rocksalt nitrides have historically been associated with superconductivity, such as in NbN, new semiconducting variants are broadening the scope for future device design and fabrication.

Bridging the structural space between wurtzite and rocksalt are layered nitrides. These include materials such as $ZnZrN_2$, sometimes termed 'wurtsalt', which consist of alternating wurtzite and rocksalt layers, and are predicted to exhibit very low hole effective masses.

Although wurtsalt structures remain challenging to synthesize, the related layered 'rockseline' structure (combining rocksalt and nickeline motifs), exemplified by $MgMoN_2$, has recently been realised in thin-film form. There is cautious optimism that the epitaxial growth of rockseline materials, together with their predicted topological properties, could contribute to the development of next-generation nitride-based quantum electronics.

FURTHER READING

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- A. Zakutayev *et al*. "Experimental synthesis of theoretically predicted multivalent ternary nitride materials." Chem. Mater. **34** 1418 (2022)
- S. Choi *et al*. "A single-phase epitaxially grown ferroelectric perovskite nitride." Sci. Adv. **11** eadu6698 (2025)

Another emerging area involves nitride semiconductors with non-stoichiometric metal-to-nitrogen ratios, such as nitride perovskites with the general formula ABN_3. Following theoretical predictions a decade ago, recent synthesis advances have enabled the development of oxygen-free nitride perovskites. Examples include $LaWN_3$ exhibiting high piezoelectric coefficients, and $CeTaN_3$, demonstrating switchable ferroelectricity. Admittedly, compared with halide perovskites, progress in nitride variants has been more gradual. Nevertheless, these materials may significantly influence the future direction of electronic device research.

Taken together, these research developments suggest that the nitride semiconductor field extends well beyond GaN and its close relatives. Advances in materials chemistry are revealing a diverse family of nitride material systems, ranging from tunable-bandgap wurtzites and emerging rocksalt semiconductors, to layered nitrides and nitride perovskites. It is conceivable that one of these compositions could follow a trajectory similar to AlScN, rapidly gaining prominence due to distinctive functional properties.

From the perspective of a materials scientist, it is my opinion that continued evolution in electronic devices presents an opportunity.

Broadening the materials palette to include the wider family of nitrides may enable new functionalities and device concepts drawn from what lies beneath the tip of the GaN iceberg.

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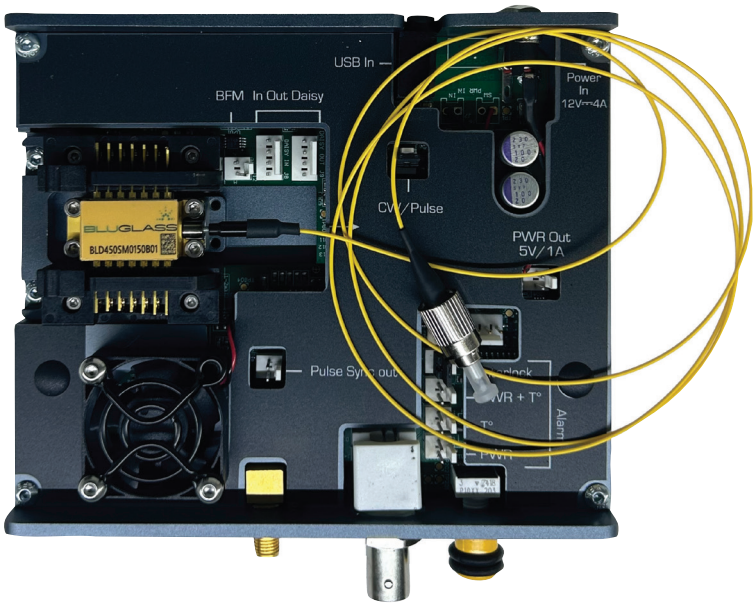
GaN-based lasers for quantum applications

Blue lasers with surface gratings are delivering quantum precision from millimetre footprints

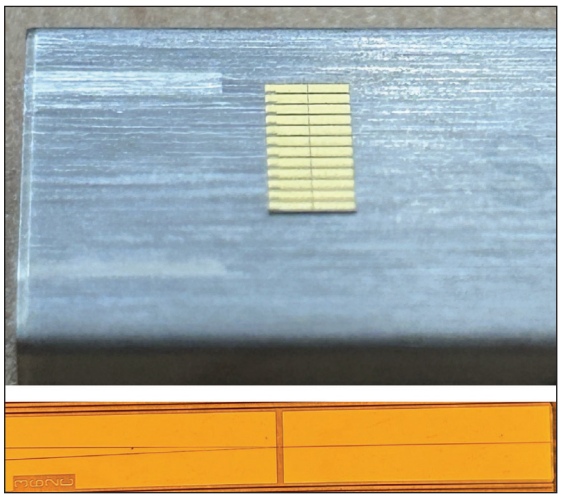
BY RYAN ANDERSON FROM BLUGLASS



THE VISIBLE SPECTRUM is an exciting frontier for laser diode technology. Here emerging applications exist, demanding sources with a small size, low power consumption and high-fidelity.

Addressing this need are narrow-linewidth lasers. Capable of single-frequency emission, these emitters enable breakthroughs in quantum computing, quantum sensing, and secure communications.

For those in search of a narrow-linewidth laser, an attractive candidate is the GaN-based distributed feedback (DFB) laser, a device we have developed at BluGlass. We view this source as a significant step in the progress of narrow-linewidth lasers, because our device combines a compact form with a relatively straightforward manufacturing process and a level of performance that promises to drive innovation in visible photonics.



➤ A bar with 12 high power GaN laser chips on a USB stick for size comparison. The optical microscope image is a higher magnification of a single chip.

Precision emission

For every laser, its spectral linewidth has a profound impact on how it interacts with its environment. When the linewidth is narrow, nearly all emitted energy is concentrated into a useful optical frequency. That's a massive asset when serving in an atomic system, as this exactness makes the difference between realising the resonance for laser cooling or missing the absorption line entirely.

Quantum technologies, which depend on a high degree of accuracy and precision, rely on the excitation of sensitive atomic transitions by lasers emitting at specific wavelengths. Within this sector, Rydberg sensors are emerging as power detectors for electric fields. These sensors, requiring visible light with linewidths of hundreds of kilohertz, can target many applications, ranging from high-resolution RF imaging and communication and surveillance to quantum computing and networks for defence and aerospace.

In addition to quantum applications, lasers emitting in the blue and green are compelling candidates for underwater communications and lidar, thanks to operation in the spectral sweet spot for water penetration. Similarly, these wavelengths can

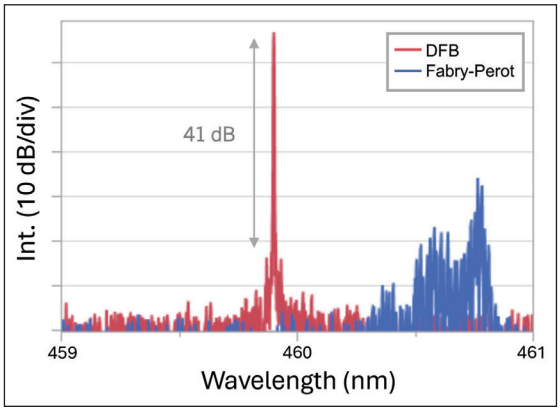
provide the optical source for remote detection of aerosols, gases, and clear-air turbulence, helping scientists understand weather patterns and pilots avoid dangerous flightpaths in otherwise impossible-to-detect conditions.

In all these applications, one theme is clear: there's a need for compact, stable, scalable narrow-linewidth sources in the visible regime.

Comparing options

The narrow-linewidth laser can take various forms, all involving significant trade-offs between performance, complexity and practicality.

In general, external cavity diode lasers are a well-established source with an excellent linewidth. Incorporating tuneable optical cavities outside the laser medium, this class of laser requires quite sophisticated precision optics. This often results in bulky but delicate benchtop systems, needing alignment, isolation, and complex packaging.



➤ The difference between a single-frequency laser and typical Fabry-Pérot laser diode are starkly evident when comparing the spectral characteristics measured in an optical spectrum analyser. The width of the DFB laser is less than 3 picometers and limited by the resolution of the measurement system, while the Fabry-Perot laser is approximately 0.5 nm.

Another promising approach for compact visible lasers are photonic integrated circuits (PICs) featuring GaN emitters. In this configuration, a laser gain section is fabricated on a chip that couples the optical output into waveguides, with external resonators or filters controlling the emission frequency. GaN-based lasers featuring a ring resonator as a PIC have produced impressively narrow linewidths, but at the expense of complex wafer bonding and multi-step processing. Each additional layer of integration may double or triple fabrication complexity.

We are trailblazing a third route: the GaN distributed feedback (DFB) laser. This design, already well-established in lasers made from traditional III-Vs, uses a precisely defined grating that's built into the optical cavity to select and stabilise a single-emission wavelength. While DFBs are yet match the sub-100 kHz linewidths of the most advanced PIC-based systems, they offer a balance of performance, size, and manufacturability practical for large-scale deployment.

In our view, all three classes of narrow-linewidth laser have a role to play in the application landscape. Here, the GaN DFBs occupy the critical middle ground, as they are simpler than external-cavity diode lasers and cheaper than heterogeneous PICs, while still delivering narrow linewidths and a stability sufficient for most quantum and sensing applications.

GaN DFB challenges

Replicating the processes employed for making III-V DFB lasers with a GaN-based material systems is far from trivial. The primary challenge stems from difficult epitaxial layer growth in the III-nitride hexagonal material system. With conventional III-V DFB lasers, fabrication involves overgrowth of patterned semiconductor layers, a step that's typically straightforward in a cubic material system. In stark contrast, regrowing GaN over etched gratings tends to introduce defects or roughness, compromising optical and electrical performance. To address this concern, some groups turn to porous GaN layers or laterally etched gratings. However, impressive results are realised with methods that add complexity or introduce new limitations.

We have developed a different approach that avoids deep etching and regrowth entirely. Instead, we form embedded surface gratings in the transparent, conductive material indium tin oxide (ITO).

With our approach, after epitaxial growth of our GaN laser structure, we deposit ITO as a transparent *p*-contact. We then define nanoscale gratings in this oxide by electron-beam lithography. After writing them, they are directly embedded under another thin ITO layer to preserve a smooth, conductive surface for current spreading.

This design, originally developed at the University of California, Santa Barbara (UCSB), and refined through our ongoing collaboration, avoids the most challenging aspects of GaN fabrication. It minimises damage to the *p*-GaN layer, maintains optical quality, and integrates the feedback mechanism directly within the device's current-spreading layer.

Record-breaking linewidths

Over the last few years our team has made significant strides in optimising the epitaxial structure and the embedded grating design. By refining the optical mode overlap and the coupling strength, we've realised side-mode suppression ratios (SMSRs) exceeding 40 dB, a clear indication of single-mode operation.

An even more impressive result is a linewidth of just 680 kHz, recorded when UCSB researchers measured the fundamental linewidth of our embedded-grating GaN DFB laser using a correlated self-heterodyne setup. To our knowledge, this is the narrowest fundamental linewidth reported for a nitride-based DFB laser.

Thanks to this result, we know that our GaN DFBs are within the performance range for laser cooling, atomic sensing and visible lidar applications – and they are within striking distance of 100 kHz, which could open the door to even more demanding quantum technologies.

Wavelength tuning

Linewidth is not the only critical characteristic for a single-frequency laser. It's also essential that accuracy and precision hit a bullseye regarding the target wavelength of a particular application; and the laser runs at a stable wavelength under a wide range of operating conditions.

To consider these criteria, we've compared our DFBs against Fabry-Pérot lasers from the same wafer, operating under varying temperatures and currents. Under those conditions, our lasers maintain single-mode operation and shift by only 17 picometers per degree Celsius. This is a remarkably low sensitivity to temperature compared with traditional III-V lasers. Our DFBs also exhibit a very low wavelength drift during current sweep. This robustness makes our sources ideal for portable applications, where environmental control isn't perfect.

For some applications it's essential to provide a modest tunability, on the order of a few nanometres – this feature enables locking to atomic transitions. It is challenging to meet this need with GaN, due to a relatively stable refractive index with temperature; and it's also not easy to take the well-trodden path of adding regrown passive phase sections, to create a device that's similar to an external cavity.

As a first step towards coarse tunability, we have explored prototypes with two cavities resembling distributed Bragg reflector lasers. While these devices undergo mode hops during current adjustment, we are optimistic that clever design will enable pathways for realising controlled tuning in multi-section lasers. Through ongoing work, we are aiming to refine these structures and explore three-section architectures that combine stability with electronic control.

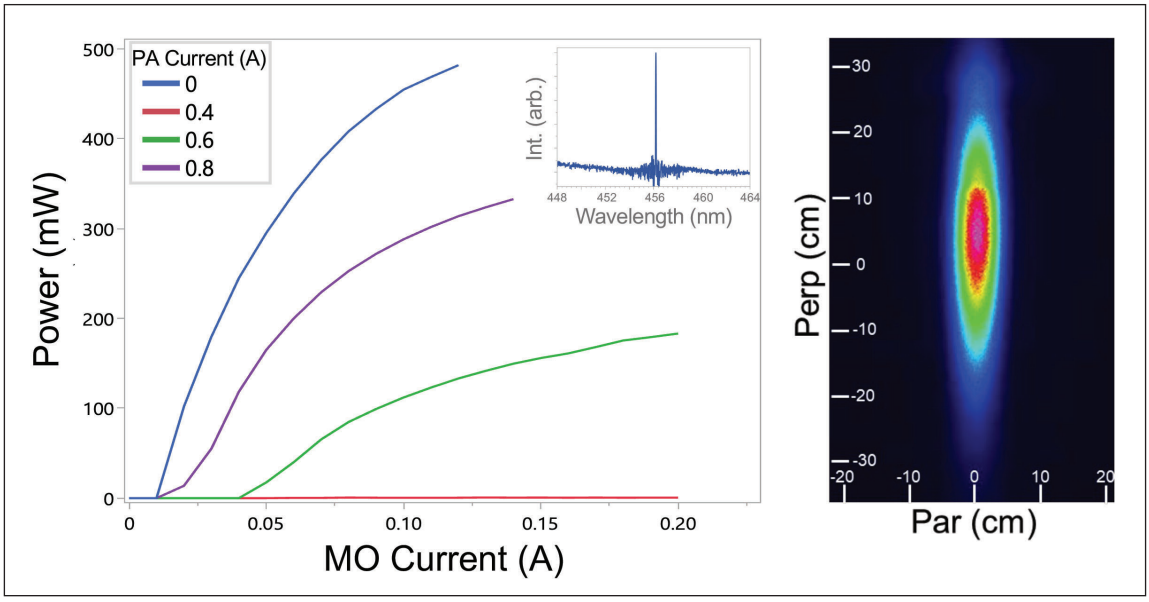
Scaling-up power

Many applications require not just stable light, but a lot of it. We have already demonstrated DFBs with up to 100 mW of single-frequency emission, and we are pushing toward hundreds of milliwatts and beyond, via the introduction of semiconductor optical amplifiers and configurations that include master oscillator power amplifiers.

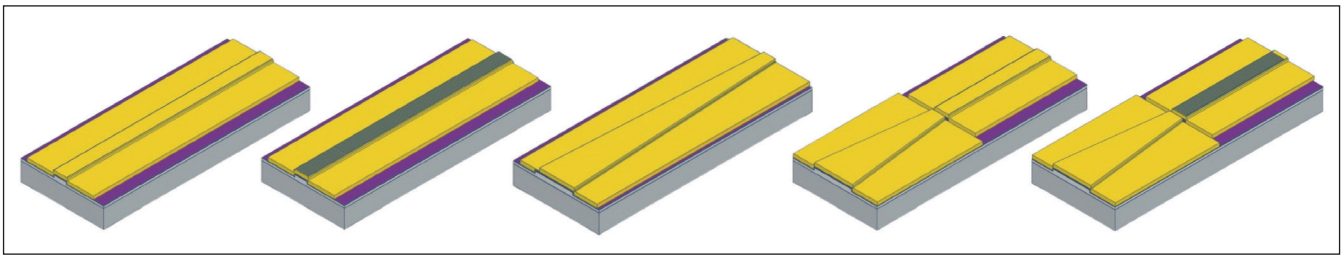
To create efficient amplifiers, we've developed anti-reflective coatings that have a reflectivity of less than 0.1 percent at 450 nm. According to initial tests, amplifiers with these coatings, which prevent unwanted feedback and lasing modes in the external cavity, provide up to 15 dB of optical gain with minimal optimisation.

We have also fabricated integrated devices with master oscillator power amplifiers that combine a Fabry-Pérot or DFB seed section with a tapered amplifier. By carefully controlling amplifier geometry and current drive, we have produced more than 400 mW of power under quasi-CW operation while maintaining a single spatial mode in the far-field.

Following additional refinements in epitaxy, facet coatings, and thermal design, we expect to propel output powers towards 1 W without compromising



➤ Light output for a master-oscillator and power amplifier configured laser diode. The inset exhibits the narrow linewidth spectral peak and the associated far-field mode profile at 400 mW of output power. The test is performed under quasi-continuous wave electrical injection.



➤ Chip types manufactured by BluGlass from left to right including basic Fabry-Pérot lasers, DFBs, semi-conductor optical amplifiers, single spatial mode MOPAs, and high-power single-frequency lasers.

linewidth or mode quality. That's a level of performance that could unlock new boundaries in visible-light sensing and communication systems.

Ensuring consistency

Equally important to achieving narrow linewidths is consistency across wafers and manufacturing batches. To succeed in this regard, we have partnered with Fred Kish's group at North Carolina State University, carrying out simulations that lead to improved laser diode performance. Their team's modelling combines band-structure calculations with carrier transport, cavity mode analysis and coupled-wave theory to elicit a model for fabricated devices.

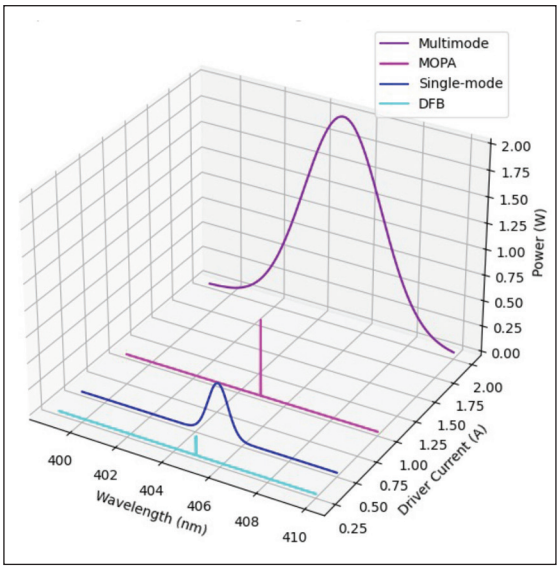
Using our data for a lower-performing 442 nm DFB laser, their model pinpointed two causes for poor performance: a low coupling coefficient, and a mismatch between the grating peak and gain peak. Modelling also determined that increases in the coupling coefficient produce a dramatic increase in the predicted side-mode suppression ratio and the threshold current, even with a slight detuning of the grating wavelength to the gain peak. These insights are guiding our epitaxial layer design, and enabling us to systematically realise higher-performing, more repeatable DFB lasers.

Looking forward

The promise of GaN DFB lasers lies not only in their performance, but in their scalability and versatility. Unlike high-end laser technologies that are confined to research labs, DFBs are chip-scale, manufacturable, and integrable. With careful design, they can be arrayed, wavelength-locked, or coupled to amplifiers – advances that create a platform for diverse applications, ranging from quantum networks to compact lidar sensors.

Our roadmap includes reducing linewidths to 100 kHz or less, increasing yield and reproducibility across wafers, enhancing tunability without sacrificing mode purity, and scaling output power to the watt range.

We view visible-light GaN DFBs as a foundational technology for the next generation of photonics in quantum systems. By combining materials innovation and optical engineering, while collaborating with leading academic partners, we are advancing practical, scalable solutions that will power the quantum and sensing systems of tomorrow.



➤ The relative peaks and magnitudes of various devices manufactured by BluGlass under current in the violet wavelength regime.

The ability to generate blue light that's precise and stable is transforming what's possible in science and technology. Our GaN-based DFB lasers are compelling candidates for meeting the demand for a manufacturable platform that delivers narrow linewidths and high power in a compact form.

As our research continues, we have no doubt that the innovations provided by us, and our partners, will play a pivotal role in shaping the visible photonics landscape.

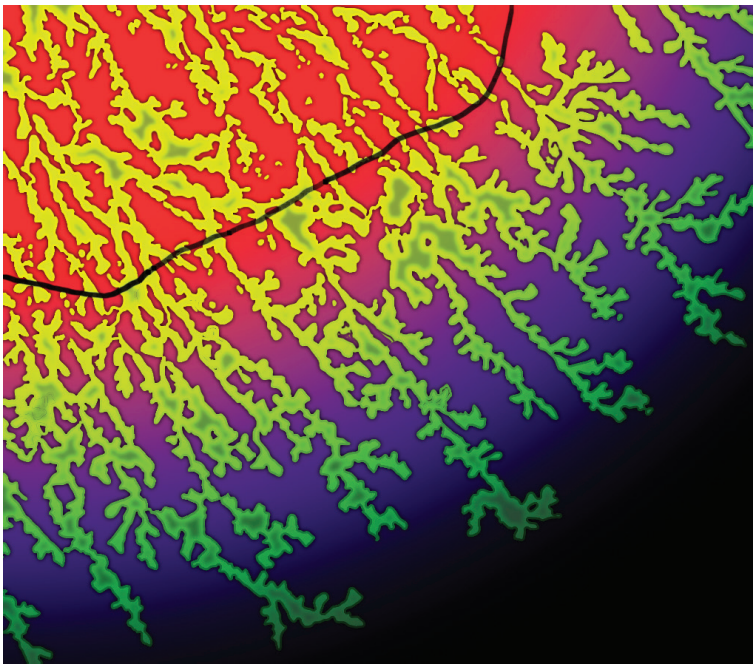
FURTHER READING

➤ R. Anderson *et al*. Advancements in GaN DFBs with embedded gratings and a path to higher power", Proc. SPIE 13345, High-Power Diode Laser Technology XXIII, 1334510 (21 March 2025)

Paths to improved laser reliability

Implementing strategies that slash laser diode failure rates by at least two orders of magnitude can banish reliability-related delays in the deployment of co-packaged optics

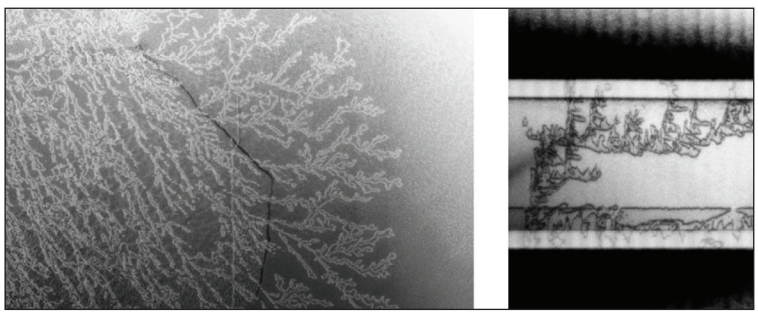
BY ROBERT HERRICK FROM ROBERT HERRICK CONSULTING



OVER the last two decades, fibre-optic transceivers have played an increasingly critical role in modern data centres. However, as these data centres have scaled up, concerns have escalated surrounding energy consumption. For more than ten years there's been a proven solution, 'co-packaged optics' – it's an architecture that is capable of power savings of 30-70 percent – but industry is reluctant to adopt this approach, held back by concerns associated with reliability and maintainability.

A number of issues have hampered laser reliability in transceivers for the last 30 years, a situation that's not helped by poor design choices. The emphasis has been on ease-of-fabrication, cost, performance, and supply chain diversity – an agenda that's neglected reliability.

This has led to a number of high-profile failures, that have made transceiver reliability the source of a lot of apprehension amongst buyers. The earliest of these failures occurred on the first 'low-cost' (sub-$1,000) transceiver, known as the Gigabit Link Module, or for short, GLM. In this case, failure of the entire population started after just a few years of deployment, and the product had to be recalled.



➤ Figure 1. Dark Line Defects (DLDs) are dislocation networks that grow in lasers from crystallographic or mechanical defects, increasing optical loss and reducing laser output power. These have been responsible for most transceiver reliability failures. Examples can be seen from a failed GaAs 850nm VCSEL (left) and an AlGaInAs 1310 nm cleaved-facet laser (right).

A few years later, makers of VCSELs had challenges deploying the first generation of parallel optical links. The first parallel-optic module based on this class of laser never made it to product release, while the second had to pulled off the market and the product line permanently cancelled, only a year or so after initial deployment. It then took a few more years for engineers to figure out how to solve the problem of dark-line defects (see Figure 1) that propagate from the edge of the die.

Despite these woes, one could argue that lessons have not been learned, with reliability issues continuing to plague lasers. Recently, chipmakers deployed low-cost AlGaInAs edge-emitters with failure rates ten times higher than the target. This oversight had severe ramifications, including significant delays and cost over-runs during data-centre bring-ups.

There are concerns even among typical transceivers. The key metric for reliability is FIT, which is the number of failures-in-time per billion operating hours. For an 'average' transceiver the FIT is around 200-300, implying that engineers can expect a typical switch with 32 transceivers to need maintenance during its deployment lifetime 10-40 percent of the time. For this reason, to ensure easy maintenance most switches are currently designed with front-panel pluggable transceivers. This allows failing transceivers to be quickly removed and replaced. However, according to data centre operators, there's a significant cost associated with identifying failed links and performing maintenance.

The desire for embedded optics

Another consideration is that as data rates increase, it is more difficult to maintain signal integrity over links of just a few centimetres. To address this matter, engineers are adding 're-timer' circuits that clean up signals after they propagate the 20 cm required by front-panel pluggable designs (see Figure 2 (a)). That's an imperfect solution, as the power consumption of these re-timers is significant. To trim this, one can mount smaller fibre-optic transceivers that don't require re-timers right next to the switch ASIC (see Figure 2 (b)). Note, though, that these miniaturised transceivers are usually not pluggable, and certainly not accessible from the front panel. Thus, repair cost and repair time are expected to increase by around an order of magnitude, hikes previously viewed as unacceptable with the fibre optic transceivers currently available.

A potential solution could be the uptake of co-packaged optics. Based on industry consensus, the adoption of this technology will commence with next-generation switches, introduced this year. A number of providers have showcased systems based on co-packaged optics that are not just 'technology demos', but expected to be mainstream products.

The need for greater reliability

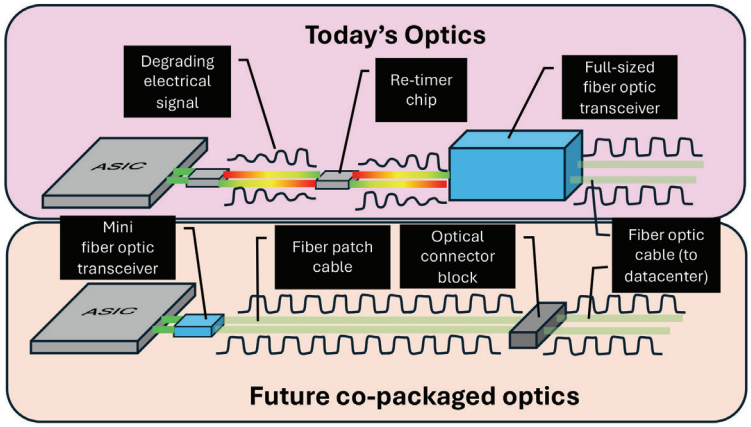
Laser reliability levels that have been 'good enough' during the past few decades are unlikely to be acceptable for future applications. In this context, it's worth considering an application beyond co-packaged optics – future AI clusters, involving hundreds of thousands or even millions of links. In the case of one million transceivers with a typical 200 FIT failure rate – that equates to an annual failure rate of about 0.2 percent – existing transceivers would be responsible for a link failure every 5 hours, on average. This is unacceptable. An improvement by a factor of at least 100 is needed to support next-generation million-link AI clusters.

Another application demanding consideration is lidar photonic integrated circuits (PICs). As lidar is a safety-critical component for autonomous driving and robotaxis, the automotive industry has failure-rate expectations that are typically multiple orders-of-magnitude lower than today's state-of-the-art.

Five solutions

There are five existing solutions that provide significant improvements in reliability: External Laser Small Form-Factor Pluggable (ELSFP) products, heterogeneous lasers, redundancy, improved materials and improved screening. Now we will consider these approaches, one by one. Note that some are starting to be used, but most have only limited adoption.

Enjoying the widest adoption is the ELSFP. Its popularity stems from retaining the laser that provides the light to the photonics in a 'front-panel-pluggable' position, where it can easily be replaced if it fails. With this technology light is routed in with

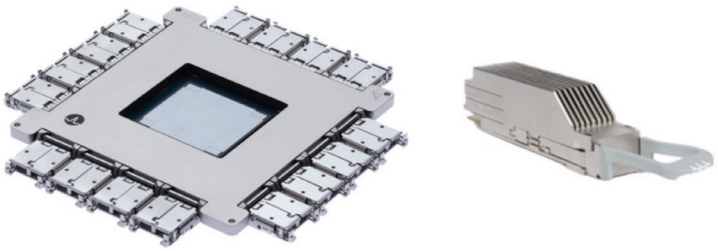


➤ Figure 2. Today's optics (upper diagram) rely on power-hungry retimer chips to recover rapidly degrading electrical signals that are far from the switch ASIC. New co-packaged optics (lower diagram) place mini fiber-optic transceivers much closer to the switch ASIC, to where retimers can be eliminated.

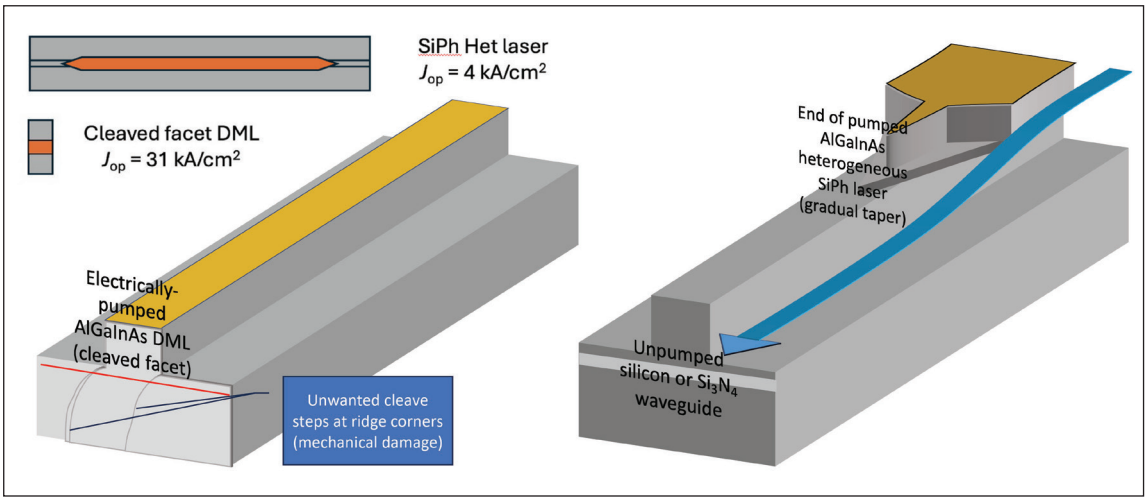
fibre optics (see Figure 3). In addition to moving the laser to a more maintainable location, this product employs a more expensive, more reliable laser. The light source has a number of costly-to-fabricate features that quash the failure rate by orders of magnitude over low-cost ridge lasers, which were previously used for most data communication.

The second solution, heterogeneously-integrated lasers, has been used by Intel. With this approach Intel obtained some of the lowest failure rates ever reported, with a FIT laser failure rate of just 0.09 – that's 0.8 parts per million per year. It is thought that the superior reliability stems from elimination of cleaved facets (a modification that provides many of the benefits of 'window' lasers), as well as a current density 8-10 times lower than that of direct-modulated-lasers (see Figure 4). In addition, many of these designs are also used in tandem with redundancy.

Redundancy, the third solution, has much appeal. Rather than straining to improve reliability by orders of magnitude, engineers include backup channels that allow the use of conventional lasers. This redundancy-related approach boosts system



➤ Figure 3. Co-packaged optics (or 'CPO', left) using front-panel pluggable ELSFP laser module (right) powering the optics (courtesy of Broadcom). The lasers are accessible from the front panel, and can be easily replaced in case of failure, while the electrical-to-optical conversions can be close to the switch ASIC.



➤ Figure 4. Heterogenous laser (right) benefits from not having a cleaved and pumped facet like the directly-modulate laser (DML) does (left). The heterogeneous laser also benefits from having its gain spread among a larger area, with current density less than 1/8th the level of the DML.

availability by 100-fold or more. If there's monitoring of the performance degradation in the link, it's possible to predict failure hours or even months before it happens, allowing software repair to be proactive and a graceful switch-over to take place.

Two types of redundancy are being proposed for future systems (see Figure 5). One option is to provide a spare for every channel (a condition known as 1:1 sparing); and the second is having a pool of lasers with some spares ('*m* of *n* sparing'). While gains in reliability depend on failure rates, and whether failures are correlated or fully random, it is relatively straightforward to obtain improvement by a factor of 100 in redundant systems. However, there's still the need for 'software repairs' that switch to the backup channel once failure has been forecast or observed.

The fourth pathway for improving reliability is associated with gains in material quality. Unfortunately, most laser material used in data communication systems is not selected with reliability in mind, so it is vulnerable to 'dark line defects' (DLDs). These imperfections are implicated in the failures found in 850 nm GaAs VCSELs, and in the cleaved 1310 nm AlGaInAs directly modulated lasers mentioned earlier and shown in Figure 1. But other laser materials exist. They can be adopted, especially if industry standards committees are flexible about wavelength, or less demanding about requirements relating to uncooled operation. Today there are requirements for operation at very high-temperatures, often greatly exceeding what is actually present in data centres.

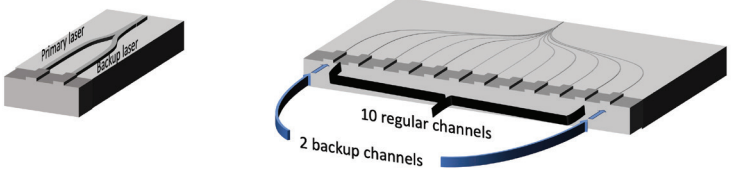
Options based on this line of thinking include replacing unstrained 850 nm GaAs quantum well VCSELs with variants that emit at 980 nm, and are based on strained InGaAs. The standards committees could have supported this move in the mid 1990s, but shied away, preferring an 850 nm standard, due to wider availability of low-cost GaAs and silicon photodetectors. However, with the benefit of hindsight it's clear that retaining the 850 nm standard has only delivered minimal cost savings associated with photodiodes, and this upside is overshadowed by problems coming from DLDs. Now, at least on proprietary links, 980 nm VCSELs are being adopted. Their merits are not limited to a lack of vulnerability to sudden DLD failures, and include a much higher modulation bandwidth under direct modulation.

Another option for improving reliability via the introduction of better materials is to turn to quantum-dot lasers. Due to the high strain of the dots, DLDs do not grow in them, instead appearing to be tangled around these nanostructures. With normal quantum-well material, the presence of just a single threading dislocation leads to growth of a DLD network during laser operation, prior to causing device failure. In sharp contrast, despite being surrounded by hundreds or thousands of threading dislocations in the III-V, quantum-dot lasers grown on silicon substrates pass reliability tests, with no DLDs observed during their aging. This class of laser has been developed or commercialised by a number of companies, with efforts targeting deployment in industrial and data-communications applications.

A third example of a more robust material is that of InGaN, which is used in lasers and LEDs. These sources, not vulnerable to DLDs, are also being explored for use in co-packaged optics by companies like Avicena.

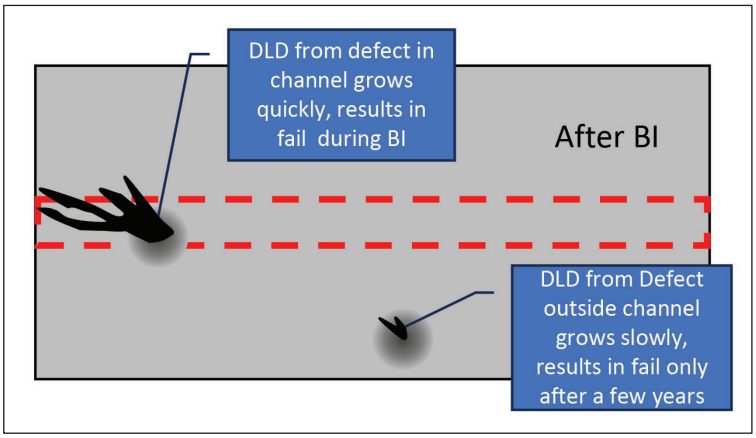
Finally, while prior techniques are probably preferred for improving reliability, there may be times where redundancy cannot be added to the design – for example, in many lidar PICs. And there can be instances where performance or wavelength is critical to the application, creating a compelling reason for

➤ Figure 5. 1-to-1 sparing (left) has a spare backup laser for each channel; '*m* of *n*' sparing (right) has a pool of spares lasers, switched in if any of the original channels fail.



using materials that are vulnerable to DLDs. In such cases, our company, Robert Herrick Consulting, is working on implementing the first known application of a new generation of high-speed inspection tools. These tools, capable of detecting small and isolated defects in devices prior to deployment, are slated for pilot roll-out later this year.

One of the significant weaknesses of traditional laser screening methods that use burn-in is that they only provide a single indicator of performance. With that approach, lasers tend to be rejected if they degrade by more than 5 percent by the end of the burn-in aging period. However, in many cases, lasers occupy thousands of square micrometres, but the defects only impact performance in a few square microns of the device – less than 1 percent of the area. What this means is that defects have minimal impact on performance and are hard to detect. By imaging through transparent substrates, one can obtain thousands of data points for the device, and megabytes of information (see Figure 6), rather than a single indicator, allowing defects to be detected long before they impact overall device performance. A reliability improvement by a factor between 20 and 100 is expected for many failure modes, although this depends on laser design and the quality of the inspection system.



➤ Figure 6. Backside inspection breaks the device down into hundreds or thousands of 1 μm^2 pixels, where each one can be examined for uniformity, and subtle mechanical or crystal defects identified prior to aging. Most lasers will appear featureless and uniform in this type of inspection, but lasers with latent defects can be identified and removed from the shipping population.

A call for change

Unfortunately, since the turn of the millennium, there has not been a significant improvement in laser reliability. That's not surprising, given that there has only been minimal change in the methods for manufacturing and screening them. But the substantial improvement that industry is demanding from suppliers – a factor of 100 to 1000 – is unlikely to materialise without a more proactive role from research agencies and/or the customer base.

Another impediment to progress is an absence of an industrial reliability improvement roadmap. To avoid supply chain shocks and allow for price negotiation, hyper-scale cloud service providers only buy compatible transceivers through a 'multi-source agreement', where at least three suppliers are available. These providers pursue aggressive cost targets, tending to leave almost no margin for suppliers – and that hampers efforts directed at fundamental research into novel materials, or many of the other potential solutions listed above. Even if some of the more advanced suppliers could set aside millions of dollars required to demonstrate one of the solutions, industry will not shift over to supporting that technology unless multiple suppliers provide it. A transition would require low-cost licensing of competitive advantages that one firm might develop, meaning they couldn't recoup much of the investment through increased market share.

It's not all doom and gloom, though. There is an opportunity for industry-funded consortiums that are comparable to the SEMI global industry organisation. In this model, highly profitable hyper-scale cloud infrastructure providers – that's the main customer base – would fund research, either at universities, research institutes such as imec or Sandia, or at multiple suppliers, based on competing research proposals. This would create IP and licenses not owned by the suppliers, but by the industry organisation, and licensed to suppliers. With this model, consortium researchers would assist suppliers in bringing chosen technology improvements into production, and getting through the qualification process.

There's also a more traditional path available, involving government-funding agencies. However, these agencies often think that laser development is 'mature', and argue that further development must be funded by industry. But that's not the reality. Many details of laser degradation are not understood at the fundamental level, including those as simple as why the addition of indium to a GaAs

Another impediment to progress is an absence of an industrial reliability improvement roadmap. To avoid supply chain shocks and allow for price negotiation, hyper-scale cloud service providers only buy compatible transceivers through a 'multi-source agreement', where at least three suppliers are available

quantum-well laser diodes 'pins' DLDs and stops their growth, or how to make a AlGaInAs laser diode that's DLD-resistant.

Another example of a lack of understanding relates to nature of the DLD. It's is a planar structure with an additional interstitial half-plane – think of it like a structure that keeps adding more 'bricks' as it grows. As the number of interstitials required is quite large, it is not understood how those are generated and transported – and debates dating back to the 1970s are still to be resolved by experimental evidence today.

Key questions remain: If we want to make a new generation of 'DLD-resistant lasers', what principles should we use to predict which materials are most likely to succeed? And would the most promising approach involve strain engineering, or instead modelling the band structure of optimised alloys compositions? Government research agencies should fund projects to answer these key questions, if they want to help to enable the next generation of reliable lasers for power AI clusters and lidar PICs.

Within industry, laser reliability is viewed along similar lines to the weather – something you complain about, but have little control of. But that's not the case: there are many potential paths for improvement, even if few are aware of the options. The reality is that the real obstacles for the simplest fixes are the cost of implementation, and support of industry standards bodies that drive multi-source agreements.

For more powerful, fundamental improvements, one should consider that more than 80 percent of the semiconductor lasers manufactured to date have unfortunately been those that are vulnerable to DLDs, and in many cases have fallen far short of their reliability targets. Government research agencies could change that, ushering in an era where laser reliability is a given, rather than one subject to a number of uncontrollable unknowns.

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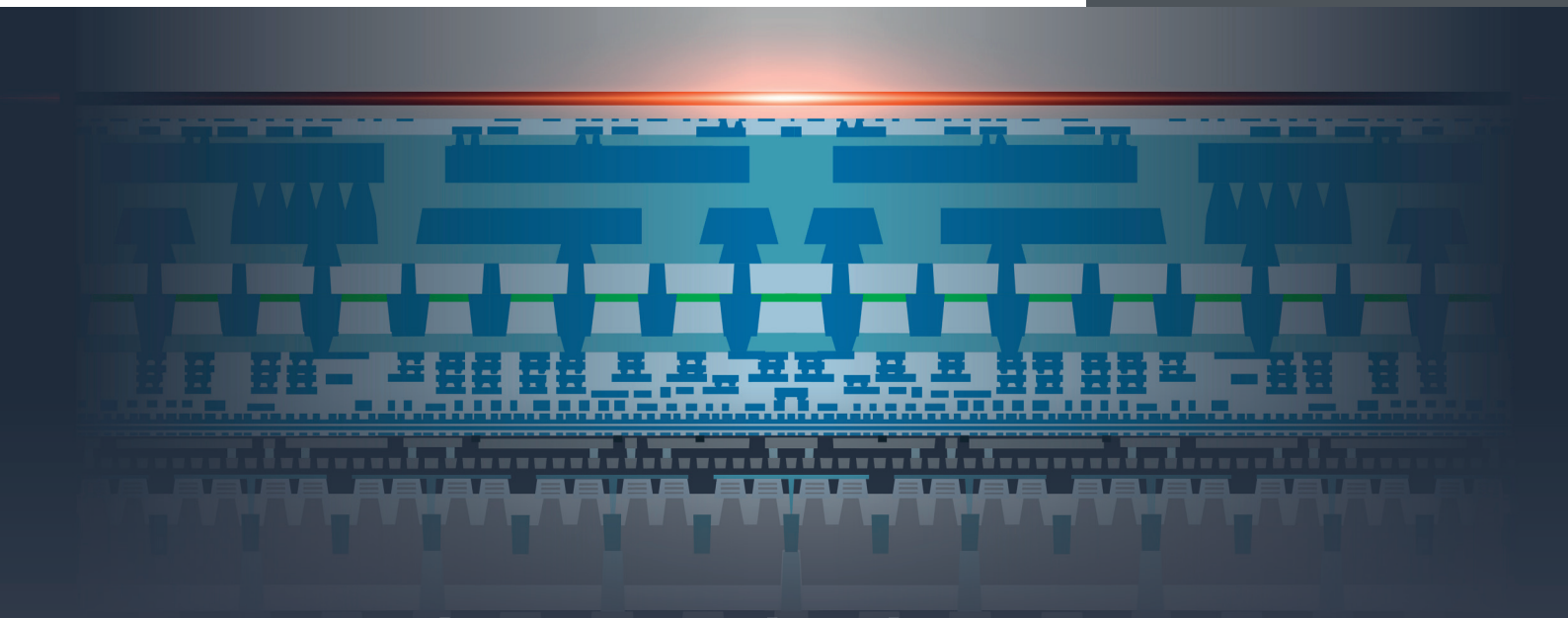

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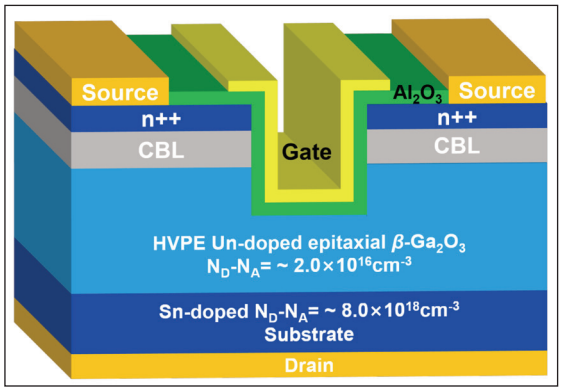
HF treatment aids Ga_2O_3 MOSFETs

When the sidewalls of U-shaped trenches are treated with HF acid, Ga_2O_3 MOSFETs combine high blocking-voltages with improved forward conduction

A TEAM from China claims to have been the first to use HF treatment to enhance the conduction of β-Ga_2O_3 MOSFETs with U-shaped trenches.

This particular FET architecture, known as the UMOSFET, has a number of assets: thanks to its vertical geometry, engineers can scale the blocking voltage by increasing drift-layer thickness, an approach that avoids an increase in footprint; and there's the opportunity to incorporate a current-blocking layer, an addition that provides a pathway to improving the forward-voltage characteristics of these devices.



➤ Fluorine treatment is claimed to dramatically improve channel transport in vertical β-Ga_2O_3 UMOSFETs with current-blocking layers.

However, often the performance of UMOSFETs is held back by deep-level defects in trench sidewalls – those imperfections trap free electrons. Overcoming this drawback is HF treatment pioneered by the Chinese collaboration, a partnership between researchers at the University of Science and Technology of China, Suzhou Institute of Nano-tech and Nano-Bionics, and the Jiangxi Institute of Nanotechnology.

According to team spokesman Xiaodong Zhang – who is affiliated to both the University of Science and Technology of China, and Suzhou Institute of Nano-tech and Nano-Bionics – their work demonstrates that a simple, low-cost HF-based sidewall treatment can preserve the blocking of kilovolts, while dramatically improving channel transport in vertical β-Ga_2O_3 UMOSFETs with a current-blocking layer.

The team is not the first to modify the surface of β-Ga_2O_3 with HF acid. Previous work has shown that incorporating fluorine creates shallow donors, and/or passivation of oxygen-vacancy-related defects, leading to improved conductivity in planar and lateral Ga_2O_3 devices.

Commenting on this, Zhang remarks: "These studies clarified the fundamental role of fluorine in modulating the near-surface electronic properties of gallium oxide, and motivated us to explore whether a similar concept could be extended to vertical power devices."

He points out that a key difference between his team's work, and that of others, is the use of HF treatment, rather than plasma-based fluorine doping.

"HF treatment provides a unique combination of selective fluorine incorporation, defect passivation, and mild surface polishing along the trench sidewalls," explains Zhang. "This is particularly critical for UMOSFETs, where channel conductivity is strongly influenced by implantation-induced deep acceptor states and etching-related sidewall damage."

The team produced their UMOSFETs by processing epiwafers with a 10 μm-thick layer of *n*-type β-Ga_2O_3. Device fabrication began with implantation of nitrogen ions at a depth of 650 nm with a box-shaped profile and a peak concentration of 2 x 10^{19} cm^{-3}, followed by annealing, which activated dopants and formed a current-blocking layer. To create the ohmic contact layer, silicon implantation and annealing followed, prior to etching, to define trenches 100 μm wide and 2 μm long.

To mitigate etching-induced damage, Zhang and co-workers treated their devices in 85 percent phosphoric acid and then 40 percent HF acid – a step not applied to the control. Atomic layer deposition added a 40 nm-thick Al_2O_3 layer to provide the gate dielectric, before the addition of source and drain contacts to the backside of the UMOSFET and the formation of the gate contact through deposition of a Ni/Au stack.

Electrical measurements determined a specific on-resistance of 6.0 mΩ cm^2, a maximum field-effect mobility of 19.1 cm^2 V^{-1} s^{-1}, and a breakdown voltage of 1132 V; and a figure-of-merit for these power devices of 0.214 GW cm^{-2} (defined by the square of the breakdown voltage, divided by the on-resistance). According to Zhang, this value is one of the highest for β-Ga_2O_3-based power transistors.

The next goals for the team are to: quantify and optimise fluorine's near-surface profile; integrate surface and sidewall engineering with advanced electric-field management techniques, including field plates and termination structures; and develop UMOSFETs that combine kilovolt blocking voltages with ampere-level operation.

REFERENCE
➤ A. Luo *et al*. Appl. Phys. Let. **128** 022107 (2026)

InP lasers: Breaking the 10 W barrier

High-efficiency carrier injection and a low-loss optical cavity drive the output power of 1470 nm diode lasers beyond 10 W

RESEARCHERS from China are claiming to have raised the bar for the output power of InP lasers to more than 10 W.

The 1470 nm laser produced by this team – a collaboration between researchers at Changchun Institute of Optics, the University of Chinese Academy of Sciences, and Jlight Semiconductor Technology Company – will help address the demand for low-cost, compact InP-based laser modules that are capable of delivering several hundred watts of CW output power. There is much interest in these modules for: welding; edge-banding; material processing; and medical applications, related to cosmetics and surgery.

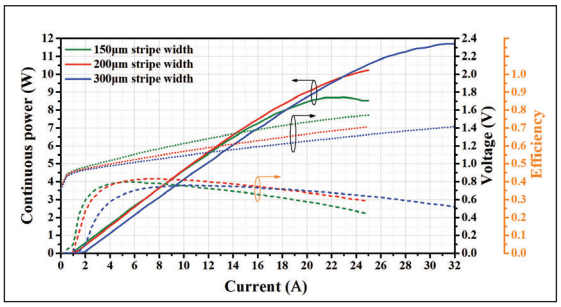
According to team spokesperson Lijie Wang, who is affiliated to both Changchun Institute of Optics and Jlight, their 1470 nm laser features a systematically optimised epitaxial structure that combines high-efficiency carrier injection with a low-loss large optical cavity design.

"By optimising the placement of the electron-blocking layer and employing an extremely asymmetric waveguide structure, reduced electron leakage and a high characteristic temperature of the slope efficiency are achieved," claims Wang.

He says that the team have grown hundreds of wafers, with devices exhibiting excellent consistency and stability and offering the potential to meet the desired performance for practical applications.

Development of the team's 1470 nm sources, which trim carrier loss from Auger-Meitner recombination, began with simulations that calculated the gain spectrum of the quantum wells, the electrical band profile, and optical mode distribution. Based on these insights, Wang and co-workers decided to employ an active region with a pair of 7 nm-thick InAlGaAs quantum wells with a compressive strain of more than 1.2 percent, surrounded by barriers with a tensile strain of 0.5 percent. It's argued that the strain-balanced design improves material quality and quantum efficiency.

Fabrication of the high-power lasers began by loading *n*-type InP substrates into an Aixtron MOCVD tool and growing an InP-based epistucture that includes an active region, an InAlAs electron-blocking layer and an *p*-type InGaAs contact layer. Lithography masks created stripe widths of 150 μm, 200 μm and 300 μm, prior to chemical etching, which defined ridge waveguides with a depth of 1 μm.



➤ For stripe widths of 200 μm and beyond, lasers emitting at 1470 nm deliver peak output powers of more than 10 W.

To complete device fabrication, the team: etched grooves with a depth of 5.5 μm between adjacent emitters to suppress lateral optical resonance; deposited a 200 nm-thick SiO_2 electrical insulating layer; opened a contact window by wet-etching; added a Ti/Pt/Au *p*-electrode and Ni/Au/AuGe/Au *n*-electrode; thinned the substrate; and used cleaving to form cavities with a length of 3 μm. Coating front and rear facets provided reflectivities of 1 percent and 98 percent, respectively.

Characterisation of these lasers, bonded *p*-side down to sub-mounts to minimise device heating, revealed that the 200 μm-wide variant produces a maximum output power of over 10.2 W and has a peak efficiency of 42 percent. The engineers observed no degradation after operating this device for over 1000 hours at a drive current of 8 A. The 300 μm-wide sibling delivered an even higher output power of more than 11.7 W, realised at an efficiency above 26 percent.

Far-field measurements determined that prior to thermal roll-over, 95 percent of the optical power falls within vertical and lateral divergence angles of 60° and 10°, respectively. "Though its beam quality is inferior to that of fibre lasers, it is comparable to that of GaAs-based diode lasers," remarks Wang, adding: "The fibre coupling issue is not significant."

The team's next goals include: further optimisation of the carrier confinement in the laser epitaxial structure, to enhance its output power and wall-plug efficiency; and developing high-power InP-based lasers operating at various wavelengths. Efforts will also be directed at expanding reliability testing to output powers beyond 10 W, using lasers with larger stripe widths.

"Additionally, we will implement advanced lateral-mode control techniques to improve beam quality and brightness," remarks Wang.

REFERENCE

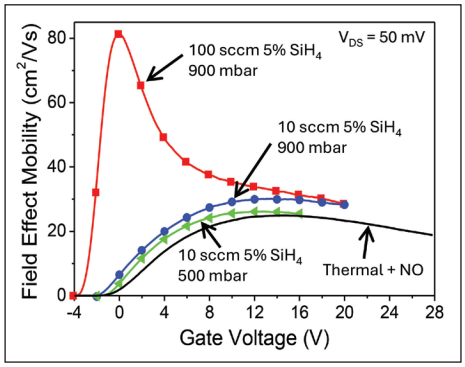
➤ R. Zhao. *et al.* Apply. Phys. Express **19** 012001 (2026)

Minimal oxidation boosts mobility of SiC MOSFETs

Silane delivers a substantial hike in the channel mobility of SiC MOSFETs

ONE of the biggest weaknesses of the SiC MOSFET is its low channel mobility. For commercial devices, it is typically around just 5 percent of that for bulk SiC.

Due to this drawback, much effort has been devoted to increasing channel mobility, with success coming from a variety of novel approaches, such as the use of sublimation-grown epilayers. But these methods don't always align with high-volume production – a criticism that cannot be levelled at the SiC MOSFETs just produced at Purdue University. They boast an increase in mobility over commercial devices by a factor of 4.5.



➤ Optimising the flow of silane leads to a hike in the mobility of SiC MOSFETs.

According to the team spokesman Koushik Ramadoss, critical to obtaining their high channel mobility is silane treatment. "Though it is not fully understood at present, we believe the inclusion of silane during the hydrogen anneal prevents excessive loss of silicon from the surface, which could lead to carbon-related defects at the oxide/SiC interface."

Fabrication of the team's devices involved implantation, a technique that's widely used in the SiC device industry for the selective introduction of dopants.

"Since SiC power MOSFETs typically use an implanted channel region, it was important to include this in our experiment to ensure the results could be replicated in production," remarked Ramadoss.

Planar long-channel MOSFETs were formed on an *n*-type 4H-SiC epilayer with a doping concentration of 9×10^{15} cm^{-3}. Implantation with aluminium at a surface concentration of 1.6×10^{16} cm^{-3} created a *p*-type body region, and source and drain regions were defined by heavy-dose nitrogen implantation.

Formation of the gate oxides began with a chemical clean of the surface, followed by hydrogen etching at 1300°C for 3 minutes in an Epigress VP-508 hot-wall CVD reactor, using pressures between 500 mbar and 900 mbar and a flow rate of 10 slm. Etching concluded by adding 5 percent silane, diluted in hydrogen gas, for 3 minutes at flow rates ranging from 10 slm to 100 slm.

The next steps involved the transfer of samples to a low-pressure CVD furnace for deposition of amorphous silicon at 580°C, followed by thermal oxidation at 750°C for 24 hours and a NO anneal at 1175°C for 2 hours.

To complete fabrication of their MOSFETs, Ramadoss and co-workers: added polysilicon gates, formed by deposition at 630°C, and doped by diffusion from a phosphorous spin-on dopant; and annealed nickel silicide ohmic contacts at 800°C for 120 s, with aluminium deposited as the top metal.

In addition to these devices, which have a gate oxide thickness of around 44 nm and a channel length and width of 140 μm and 110 μm, respectively, the team produced control devices, involving gate oxide growth by thermal oxidation of SiC and an industry standard NO anneal.

"The control devices are designed to replicate the performance obtained from a current industry standard process," explains Ramadoss.

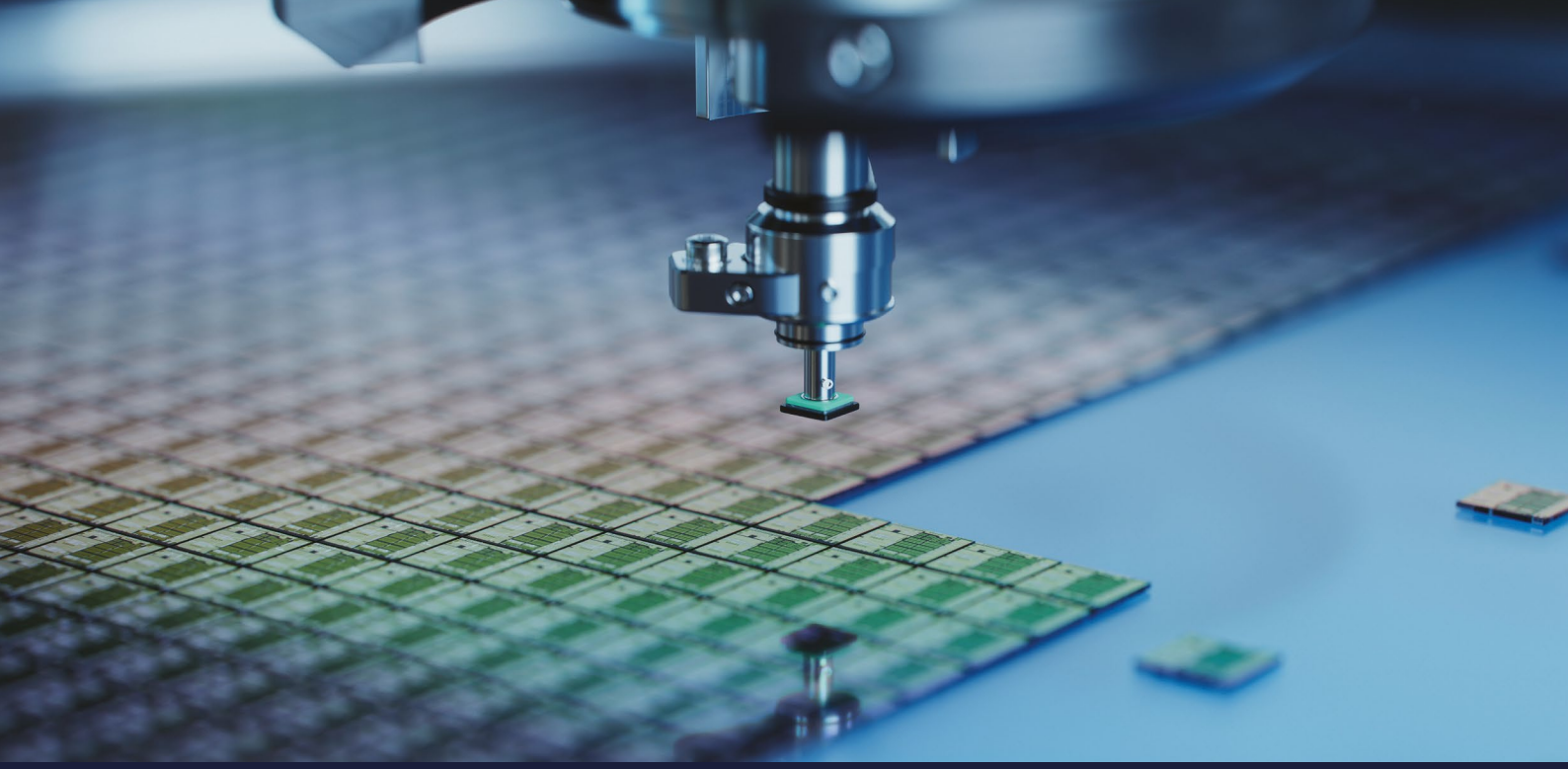
Transfer characteristics revealed that devices with a 100 scccm silane treatment exhibit a sharp increase in drain current and a negative threshold voltage. These MOSFETs deliver a dramatic improvement in peak field-effect mobility, which hits 80 cm^2 V^{-1} s^{-1}, more than three times that of the control device.

To understand the reason behind this hike in mobility, the team turned to capacitance-voltage characteristics. Measurements uncovered a reduction in total trap density by a factor of around 2.5, a condition that lowers the negative interface charge in inversion, reduces Coulomb scattering, and increases channel mobility at a lower threshold voltage. In addition, the reduced trap density could account for the low threshold voltage.

One downside of the device is a relatively high low-field leakage, possibly due to the higher density of bulk traps in the oxide or the lower ionisation energy of these traps. However, the main weakness of the team's high-mobility MOSFETs is their negative threshold voltage. This is not acceptable in a commercial devices.

"We are working on process changes that will produce a positive threshold voltage while retaining the mobility improvement," says Ramadoss. "Moreover, we are conducting experiments to better understand the role of silane in the SiC surface treatment process."

REFERENCE
K. Ramadoss *et al.* Appl. Phys. Express **19** 011001 (2026)



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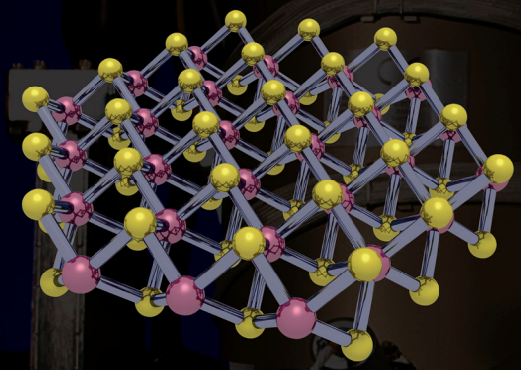

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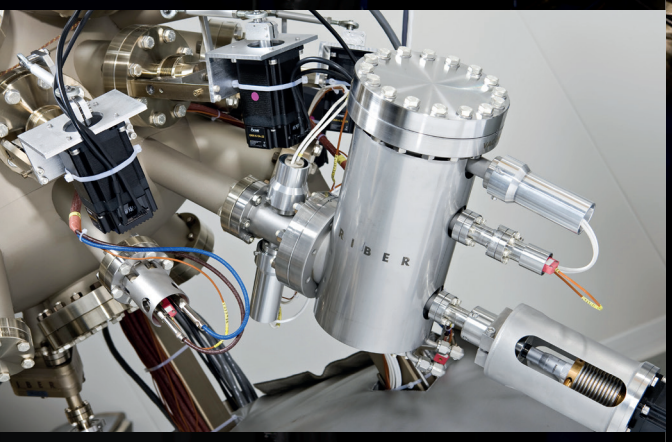

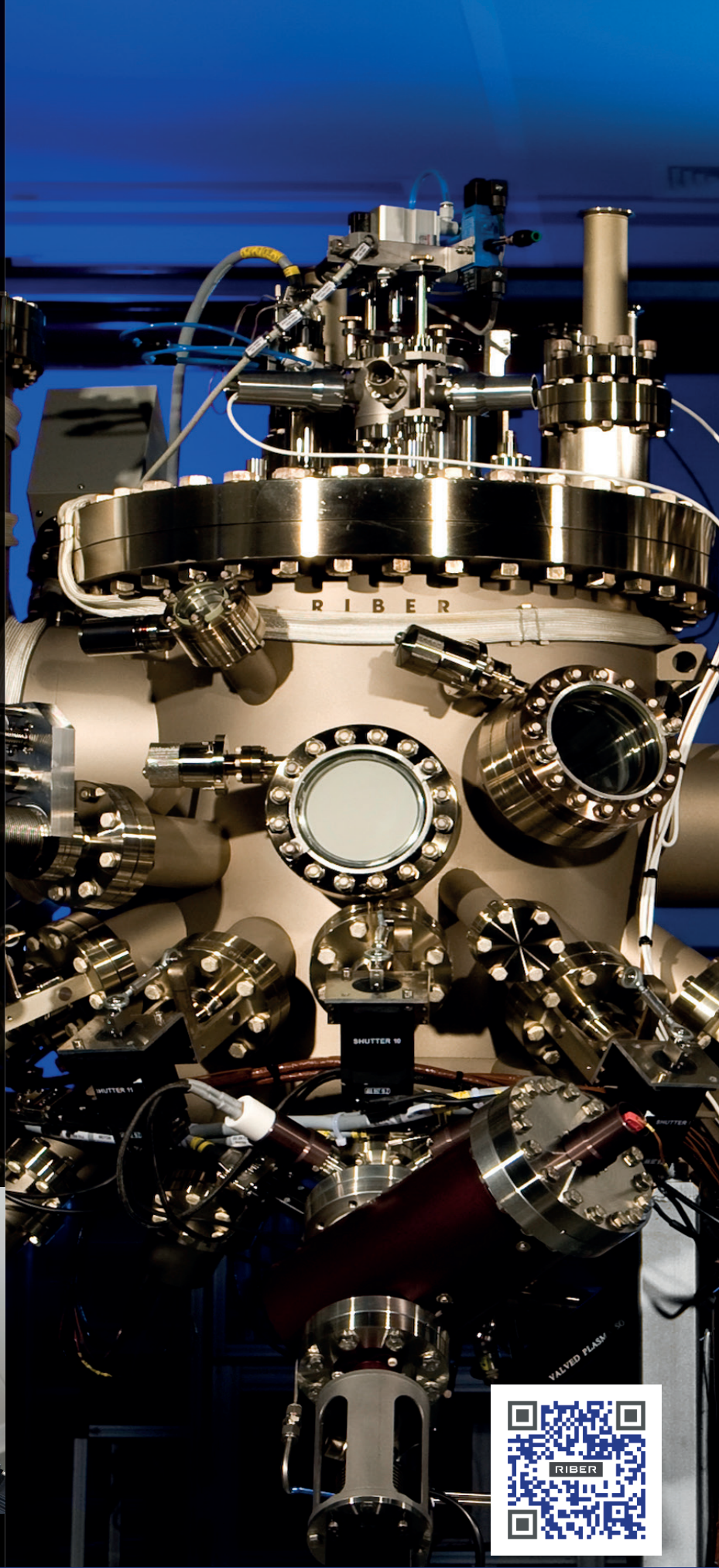

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