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VOLUME 28 ISSUE III 2022

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### INSIDE

News, Analysis, Features,  
Editorial View, Research  
Review and much more

### PERFECTING WITH POROSITY

Porosity enables red GaN-based microLEDs to deliver a performance that's comparable to their blue and green cousins

### EASING DATA CENTRE DEMANDS

Speedy, simple InP lasers offer a cost-effective solution to addressing the insatiable demand for more data

### ENHANCING GALLIUM OXIDE

Devices that pair nickel oxide with gallium oxide can handle the harsh transients found in power electronic systems



# Global mega trends require best performance III-V materials

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# VIEWPOINT

BY DR RICHARD STEVENSON, EDITOR

## PICs get off the ground

▶ WHEN I think of photonic integrated circuits (PICs), I'm drawn to the incredibly complex InP chips produced by Infinera. It is the introduction of these devices, incorporating lasers, detectors and many other elements, that has helped us all to enjoy far faster internet without having to pay much more for it.

But don't fall into the trap of thinking that optical communications is the only market for the PIC. There is also much interest in PICs for healthcare, neural networks, AR and VR, and quantum technologies – as well as opportunities that exist beyond terrestrial applications.

Developers of PICs that are directing their efforts in the latter direction include a team from the University of California, Santa Barbara (UCSB), led by Jonathan Klamkin. He and his co-workers are developing PICs based on GaAs and InP for the likes of free-space communication, remote lidar for gas sensing, and topographical lidar.

Writing for us in this issue (see p. 30), Klamkin and colleagues describe the development and testing of their PICs, along with details of the applications.

One opportunity for this team's InP PIC platform, which spans 1200 nm to 1600 nm and can produce an optical output power in excess of 250 mW, is detecting atmospheric CO<sub>2</sub> from a low earth orbit. The technology targeting this has been developed through a NASA-funded project entitled *Integrated Micro-Photonics for Remote Earth Sensing Lidar*. By fulfilling this task with a single InP chip, rather than a number of off-the-shelf



components, the UCSB team are offering savings in weight and size – these are very valuable gains when putting any technology into space.

It's a similar story with topographical lidar, used to study land, vegetation and ice. Today's systems, operating at around 1000 nm and constructed from bulk and discrete optics, are installed on aircraft, such as the twin-propeller Beechcraft B200 King Air. However, this could change, thanks to development by Klamkin and colleagues of GaAs PICs that combine a tuneable laser with a semiconductor optical amplifier to produce an output power of more than 75 mW, alongside diffractive optical elements for beam-steering. In this case, the weight and space savings could enable a switch from deployment on aircraft to mounting on cubesats, a step that would yield more of this valuable data.

I take my hat off to the UCSB team for expanding the possibilities of the PIC, and providing yet another example of how compound semiconductor devices can enrich humanity.



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GaN-based red microLEDs are now delivering a comparable performance to their blue and green cousins, thanks to the introduction of a simple step that produces porous material

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PICs based on InP and GaAs prepare to slash the size, weight and power of systems to be deployed in space and on-board aircraft for a variety of sensing applications

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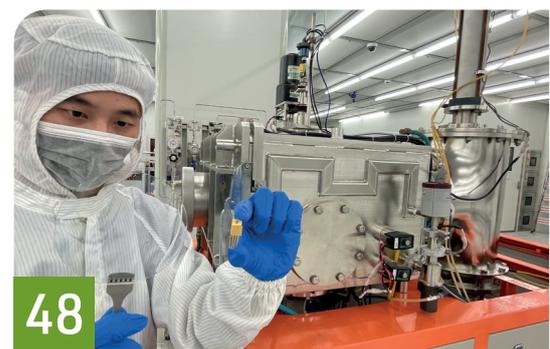
Simple InP lasers operating at 100 Gbit/s will provide a cost-effective solution to addressing the insatiable demand for more data

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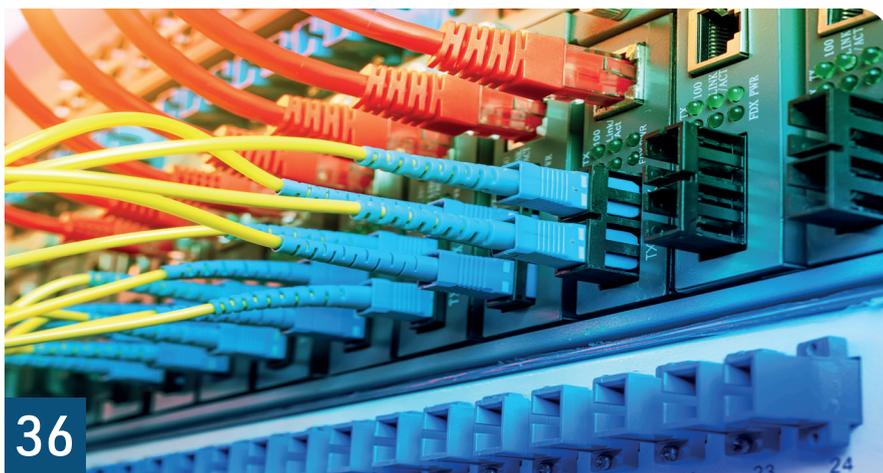
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# II-VI accelerates investment in SiC

II-VI, a maker of wide-bandgap semiconductors, is accelerating its investment in 150 mm and 200 mm SiC substrate and epitaxial wafer manufacturing with large-scale factory expansions in Easton, Pennsylvania, and Kista, Sweden. This is part of the company's previously announced \$1 billion investment in SiC over the next 10 years.

The global urgency to decarbonize energy consumption is accelerating the 'electrification of everything' and driving a sea change in power electronics technology with the adoption of SiC, a wide-bandgap material that enables more efficient and compact power electronics subsystems than those based on silicon. To meet the accelerating global demand for SiC power electronics, II-VI will significantly build out its nearly 300,000 square-foot factory in Easton, to scale up the production of its state-of-the-art 150 mm and 200 mm SiC substrates and epitaxial wafers.

Easton's 150 mm and 200 mm SiC substrate output is expected to reach the equivalent of 1 million 150 mm substrates annually by 2027, with the proportion of 200 mm substrates growing over time. The expansion of



the epitaxial wafer capacity in Kista is aimed at serving the European market.

"Our customers are accelerating their plans to intersect the anticipated tidal wave of demand for SiC power electronics in electric vehicles that we expect will come right behind the current adoption cycle in industrial, renewable energy, datacenters, and more," said Sohail Khan, executive VP, New Ventures and Wide-Bandgap Electronics Technologies. "The Easton factory will increase II-VI's production of SiC substrates by at least a factor of six over the next five years, and it will also

become II-VI's flagship manufacturing center for 200 millimetre SiC epitaxial wafers, one of the largest in the world."

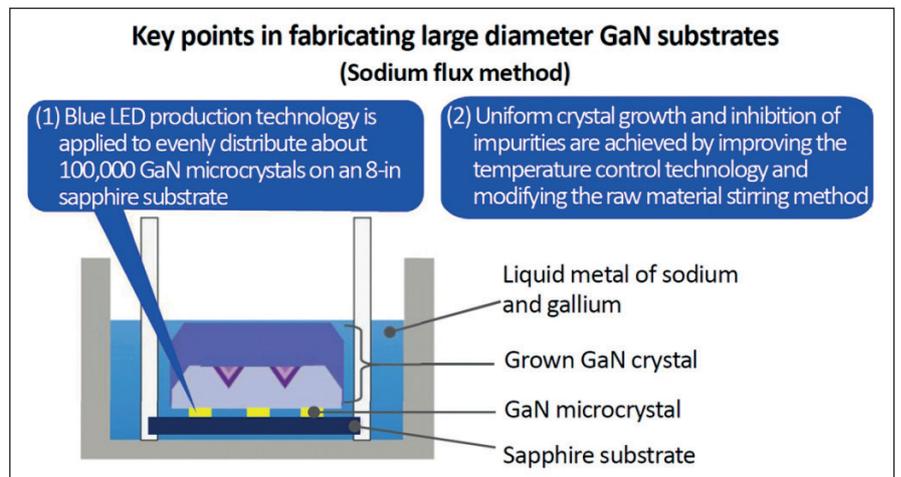
II-VI will use its industry-leading epitaxial wafer technology developed in Kista. This technology, differentiated by its ability to achieve thick layer structures in single or multiple regrowth steps, is ideally suited for power devices in applications above 1 kilovolt.

The Easton factory will be powered by an uninterruptible and scalable microgrid based on fuel-cell technology to provide high assurance of supply.

# Toyoda Gosei makes GaN substrates over 6 inches

IN A PROJECT headed by the Japanese Ministry of the Environment, Toyoda Gosei and Osaka University have fabricated a high quality GaN substrate (GaN seed crystal) of over 6 inches. With help from Toyoda Gosei's expertise in GaN semiconductors (blue LEDs and UVC LEDs), they used a method of growing GaN crystals in a liquid metal of sodium and gallium (sodium flux method).

They will next conduct quality assessments for mass production of 6-inch substrates, and continue improving quality and increasing diameter size (more than 6 inches). The technology innovation is part of a large project that includes verification



of CO<sub>2</sub> reductions from social implementation of applied products

based on the development of GaN substrates.

# Trumpf announces VCSELs for 3D sensing

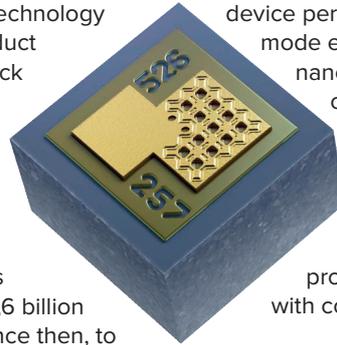
TRUMPF PHOTONIC COMPONENTS has announced new advanced VCSEL solutions to expand its portfolio for 3D sensing in consumer and industrial applications. The new generation 940 nm VCSEL arrays enable improvements in various functionalities combined with a high reliability performance such as long product lifetime at a broad temperature range.

The new VCSEL generation is said to provide better results in optical applications such as proximity sensing, laser auto focus applications or under OLED display sensing. Trumpf also addresses the trend of all-screen-display in high-end consumer electronics, and the challenge of system designers to place advanced optical sensing technologies underneath the displays.

Furthermore, the new generation is described as an 'ideal' light source for advanced industrial and automotive time-of-flight applications, referring to first customer feedback.

"We stand for highest technology standards and fast product development. It was back in 2015 when the first Trumpf VCSEL, and the first VCSEL at all, was put into a smartphone for proximity sensing. Our innovation leadership is substantiated by over 1,6 billion VCSELs shipped out since then, to enable 3D sensing and illumination in smartphones" says Ralph Gudde, VP marketing and sales at Trumpf Photonic Components.

To enhance the quality in proximity sensing and laser auto focus applications the new single-mode 940 nm VCSEL array (pictured above) consists of twelve quadratic emission zones to generate a high output power of 18 mW. Optical application design becomes significantly easier thanks to the absolutely symmetrical and Gaussian-shaped beam profile. The



device performance remains single-mode even when operated at nanosecond pulses and stable output power performance over lifetime is ensured by the robust design.

Trumpf is also planning to soon launch a second new product, a multimode VCSEL with controllable polarization.

The feature of stable and advanced linear polarisation improves the illumination quality and resolution in demanding 3D illumination applications such as optical sensing through OLED display. This new multimode 940 nm VCSEL comes with two emission zones, that generate an optical power of 8 mW. Polarization is locked by a surface grating etched directly into the GaAs.

Due to the optimized grating design the new polarized VCSELs achieve almost 100 percent of the efficiency compared to standard non-polarized VCSELs.



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# German AIscN project hopes to halve 5G energy losses

FRAUNHOFER INSTITUTES IAF and IIS along with the University of Freiburg and multiple industrial partners have begun a three-year project to develop and test an energy-efficient edge-cloud system by 2025, making use of AIscN-based components and demand-driven control. The German Federal Ministry of Education and Research (BMBF) is funding the project known as *EdgeLimit-Green ICT* as part of its wider Green ICT initiative.

*EdgeLimit-Green ICT* follows a successful preliminary project that evaluated innovative semiconductor technologies and application approaches. In the summer of 2021, the preliminary project succeeded in a BMBF innovation competition.

“Energy-efficient microelectronics, as we are developing in *EdgeLimit-Green ICT*, exemplifies how new technologies can become more powerful and at the same time conserve resources,” says Rüdiger Quay, project coordinator and executive director of the Fraunhofer Institute for Applied Solid State Physics IAF.

The project consortium, which in addition to Fraunhofer IAF includes the Fraunhofer Institute for Integrated Circuits IIS, The Institute for Sustainable Systems Engineering (INATECH) at the University of Freiburg, and partners from industry, now aims to realise

its solution for more energy-efficient mobile radio base stations by 2025.

Quay says: “The novel power semiconductor components being developed by Fraunhofer IAF, in combination with the intelligent, AI-assisted networking and control of the antenna system designed by Fraunhofer IIS, promise to halve energy losses during millimeter-wave 5G transmission.”

The industrial partners in the project network are supporting the project through collaborations in the development of novel high-frequency transistors (Nokia), circuit processing (United Monolithic Semiconductors), and the real-world evaluation and transfer of test results (Deutsche Telekom AG).

Savings due to energy-efficient AIscN components and intelligent cloud-edge implementation.

On the one hand, the high energy-saving potential of the antenna system that will be developed in *EdgeLimit-Green ICT* results from the superior material properties of the power semiconductor AIscN.

Researchers at Fraunhofer IAF produce AIscN by MOCVD and use this material in building HEMTs. Due to its high current-carrying capacity, AIscN



potentially allows significantly higher power density and gain compared to established semiconductors such as silicon, GaAs or GaN. On the other hand, the savings result from an efficient design of the electronics.

Thomas von der Grün, head of locating and communication systems department at Fraunhofer IIS, explains: “We are developing an innovative electronics architecture at Fraunhofer IIS to make possible intelligent networking and demand-driven control of the transmitter and receiver modules with the support of artificial intelligence. This provides for a partial shift of processing capacities from the central infrastructure (cloud) to the edge of the network and the implementation of data processing systems.”

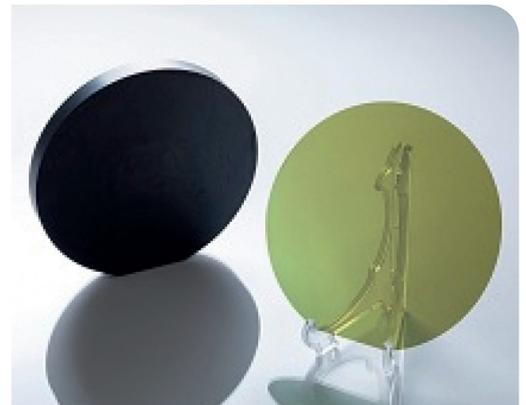
Overall, the combination of energy-efficient components and optimised organisation shall reduce the energy losses of the remote radio head implemented in *EdgeLimit-Green ICT* by at least 50 percent. For this purpose, researchers double the power efficiency at the amplifier level at new frequencies between 26 GHz and 34 GHz, halve the loss in power converters, and implement demand-driven system control.

## Showa Denko to mass produce 6-inch SiC wafers

SHOWA DENKO KK (SDK) has started mass production of SiC single-crystal wafers with a diameter of 6 inches (150 mm), which are used as materials for SiC epitaxial wafers for power semiconductors.

The demand for SiC power semiconductors is increasing rapidly in various fields, especially those for use in EVs, railcars, and industrial equipment. In addition, a number of SDK customers have adopted SDK's SiC epitaxial wafers made from the in-house produced 6-inch SiC wafers.

SDK says it will continue purchasing SiC wafers from its partners in order to respond to rapidly growing demand for SiC epitaxial wafers for power semiconductors. Thus, SDK will diversify sources of SiC wafers, thereby establishing a stable supply chain for SiC epitaxial wafers.





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# MICLEDI announces agreement with GlobalFoundries

IMEC microLED spin-off MICLEDI Microdisplays has announced a manufacturing collaboration with GlobalFoundries (GF) to enable AR glasses to achieve the brightness, resolution, power, size, and economies of scale needed to become affordable for consumers.

Under the agreement, MICLEDI's solution will be combined with GF's 22FDX platform that provides the low power and broad feature integration needed to build MICLEDI's microLED arrays in mass production. Such companion chips, which can be customised for different applications, will provide the image processing, driver and control functions needed to complete the display modules using wafer-to-wafer hybrid bonding.

The overall global AR market is estimated to reach \$88.4 billion by 2026 with a compounded annual growth rate of 31.5 percent from 2021 to 2026 as it becomes the next consumer platform.



“Demand for AR and VR products will soar as users experience more immersive augmented reality,” said Ed Kaste, vice president of Industrial and Multi-Market at GF.

“MICLEDI's microLED solution, combined with GF's 22FDX platform, addresses the demanding needs of future AR glasses by providing ultra-high resolution displays and advanced imaging technology that make stunning visual detail and colour possible.”

“We are pleased to collaborate

with GF as we move from pilot-line manufacturing to mass production in a world-class fab,” said Sean Lord, CEO at MICLEDI Microdisplays.

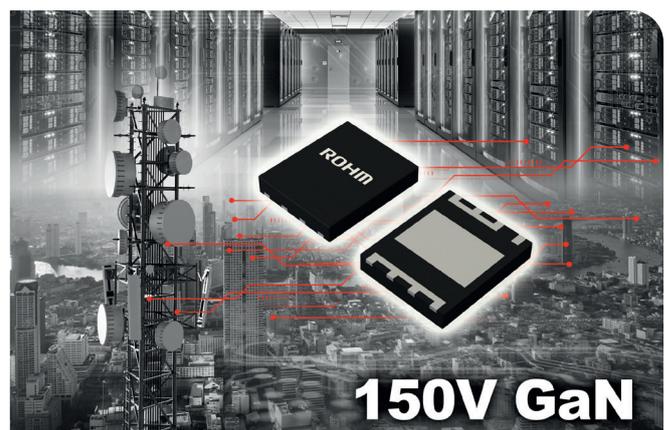
“To enable optimum microdisplays for AR, MICLEDI has developed a unique and innovative solution for microLED manufacturing, integrating both the controller IC and emitter module to leverage GFs' 300 millimetre semiconductor manufacturing technology, capitalizing on manufacturing precision for product performance, high volume and low-cost.”

## Rohm starts to produce 150 V GaN HEMTs

ROHM has announced 150 V GaN HEMTs that increase the gate withstand voltage (rated gate-source voltage) to 8 V – ideally to be applied in power supply circuits for industrial equipment, such as base stations and data centers, along with IoT communication devices. As well as mass-producing industry-leading SiC devices and feature-rich silicon devices, Rohm has developed GaN devices that achieve superior high-frequency operation in the medium-voltage range, allowing us to provide power solutions for a wider variety of applications.

These new products, from the GNE10xxTB series, use an original structure that raises the rated gate-source voltage from the conventional 6 V to 8 V. As a result, degradation is prevented, even if overshoot voltages exceeding 6 V occurs during switching – contributing to improved design margin and higher reliability in power supply circuits. According to Rohm, the GNE10xxTB series is offered in a versatile package featuring superior heat dissipation and large current capability, facilitating handling during the mounting process.

Rohm has trademarked GaN devices that contribute to greater energy conservation and miniaturization under the



name EcoGaN, and is working to expand the lineup with devices that improve performance. Going forward, Rohm will continue to develop control ICs that leverage analogue power supply technology, such as Nano Pulse Control, and modules that incorporate these ICs, along with power solutions that contribute to a sustainable society by maximizing the performance of GaN devices.

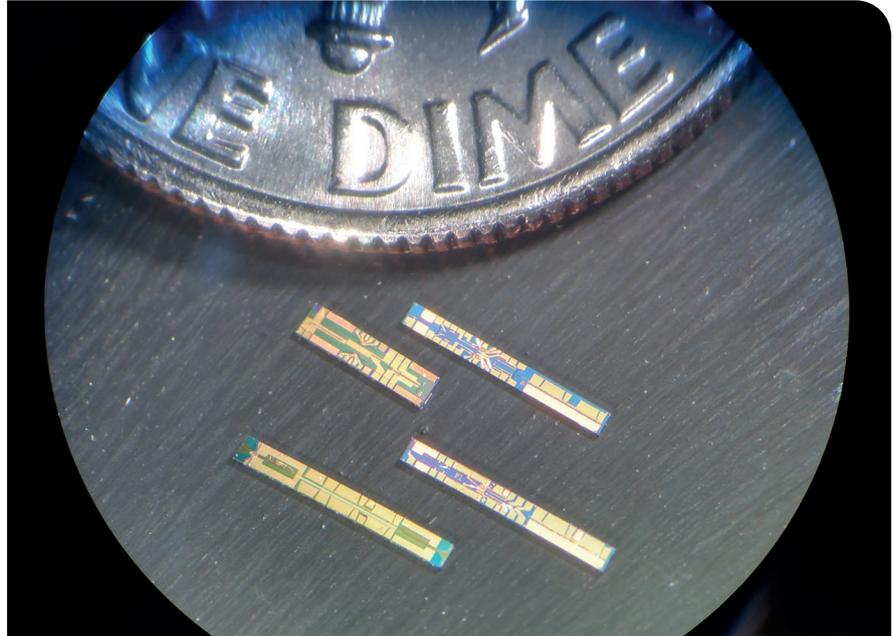
# Luminar to acquire laser chip firm Freedom Photonics

LUMINAR, a US-based automotive technology company, is acquiring laser manufacturer Freedom Photonics. This transaction follows a multi-year collaboration and brings fundamental next-generation chip-scale laser technology, IP, and production expertise in-house for Luminar lidar systems.

Luminar is vertically integrating across core lidar components that will enable low costs, supply chain security and improved performance. This transaction follows the acquisition of subsidiaries Black Forest Engineering for custom signal processing chips in 2017 and Optogration in 2021 for receiver chips.

“Component-level innovation and integration is critical to our performance, cost and continued automotive technology leadership. Bringing Freedom Photonics into Luminar enables a new level of economies of scale, deepens our competitive moat and strengthens our future technology roadmap,” said Jason Eichenholz, co-founder and CTO at Luminar.

“We’ve worked closely with the Freedom team for the past several years. They have proven to be the best in the world for breakthrough



semiconductor laser chip technology, where both power and beam quality are needed simultaneously for true high resolution at long range.”

The Freedom Photonics executive team will continue to lead and expand the business upon close of the transaction, which is expected in the second quarter. “Joining Luminar is the perfect opportunity for Freedom Photonics,

providing us an accelerated path to at-scale commercialisation of our world-class diode laser technologies,” said Milan Mashanovitch, co-founder and CEO at Freedom Photonics.

“In addition to helping extend Luminar’s automotive industry leadership, we will continue to serve and grow our broad customer base across other key markets.”

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# Semikron and Danfoss Silicon Power announce merger

SEMIKRON and Danfoss Silicon Power have announced a merger to create a joint business specialised in power electronics focusing on power semiconductor modules.

The companies will combine their existing workforce of more than 3,500 power electronic specialists and focus on future investments, paving the way for a more sustainable, energy efficient and decarbonised future. This will include driving the technology shift into SiC solutions in both industrial and automotive applications.

Danfoss President & CEO Kim Fausing, said: "The new Semikron-Danfoss builds on a strong long-term partnership and more than 90 years of combined technology leadership in

power module packaging, innovation, and customer application expertise. With electrification driving the green transition, Semikron-Danfoss aims to become the preferred decarbonising partner for customers. We have the passion, competences and technologies to more than double our business in five years."

Semikron CEO Karl-Heinz Gaubatz added: "This really is an exciting moment. Based on close, trusting conversations over the last months we have identified that Semikron and Danfoss are a unique fit with complementing assets, a strong team and shared values."

Gaubatz also remarked: "By combining Semikron's expertise as a pioneer

for semiconductor technology with more than 70 years of experience in the development of top-class power modules and systems and the strength, innovativeness and fast-paced operations of Danfoss Silicon Power and the Danfoss Group we are positioned ideally to become one of the strongest players in power electronics."

Semikron-Danfoss will retain the two main locations in Germany, Nuremberg and Flensburg. The current factories and sales offices of Semikron and Danfoss Silicon Power will continue operations as usual.

The newly formed joint business will be owned by the current owner-families of Semikron and the Danfoss Group, with Danfoss being the majority owner.



► Pictured above from left to right: Claus A. Petersen, general manager, Danfoss Silicon Power; Dominik Heilbronner, shareholder, Semikron International; Karl-Heinz Gaubatz, CEO/CTO, Semikron International; Jorgen Mads Clausen, Shareholder, former chairman of Danfoss A/S; Bettina Martin, shareholder, Semikron International; Felix Hechtel, head of supervisory board, Semikron International; and Kim Fausing, president and CEO, Danfoss A/S

# Microchip unveils 3.3 kV SiC power devices

MICROCHIP TECHNOLOGY has announced the expansion of its SiC portfolio with the release of very low on-resistance 3.3 kV SiC MOSFETs and high current-rated SiC Schottky barrier diodes (SBDs), enabling designers to take advantage of ruggedness, reliability and performance.

The devices are for electrified transportation, renewable energy, aerospace and industrial applications.

Until now, the availability of 3.3 kV SiC power devices has been limited. Microchip's 3.3 kV MOSFETs and SBDs join the company's portfolio of SiC solutions that include 700 V, 1200 V and 1700 V die, discretes, modules and digital gate drivers.

Microchip's 3.3 kV SiC power devices include MOSFETs with what is claimed to be the industry's lowest  $R_{DS(on)}$  of 25 m $\Omega$  and SBDs with the industry's highest current rating of 90 A. Both MOSFETs and SBDs are available in die or package form. These new levels of performance enable designers to simplify their design, create higher-power systems and use fewer paralleled components for smaller, lighter and more efficient power solutions.

"We focus on developments that provide our customers the ability to quickly innovate systems and move their end products into a competitive advantage position faster," said Leon Gross, vice president of Microchip's discrete product business unit.

"Our new family of 3.3 kV SiC power products allows customers to move to high-voltage SiC with ease, speed and confidence and benefit from the many advantages of this exciting technology over silicon-based designs."

Microchip says that it has released hundreds of SiC power devices and solutions to production over the last three years, ensuring designers can find the right voltage, current and package fit for their application requirements. The company's devices are backed by its customer-driven obsolescence

practice, which ensures devices will continue to be produced for as long as customers need them, and Microchip can produce them.

The expanded SiC portfolio is supported by a range of SiC SPICE models compatible with Microchip's MPLAB Mindi analogue simulator modules and driver board reference

designs. The Intelligent Configuration Tool (ICT) enables designers to model efficient SiC gate driver settings for Microchip's AgileSwitch family of configurable digital gate drivers.

These 3.3 kV SiC die and discrete devices in a variety of package options are available for order in production quantities.

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## SiC market: a multi-billion-dollar prospect

IN A NEW REPORT *Power SiC 2022*, Yole Développement forecasts that the SiC device market will grow beyond \$6 billion by 2027 from a \$1 billion business in 2021.

It's a market strongly driven by automotive applications, especially in the EV main inverter, according to Yole. There were multiple newly released EVs and announcements in 2020 and 2021, following Tesla's adoption of SiC.

"Moreover, Tesla's record shipments helped SiC devices to reach the order of \$1 billion in 2021. To fulfill the demand for a long driving range, an 800 volt EV is the solution to empower fast DC charging. This is where the 1200 volt SiC devices play crucial roles," says Poshun Chiu, technology and market analyst specialising in Compound Semiconductor & Emerging Substrates at Yole.

As of 2022, BYD's Han-EV and Hyundai's Ioniq-5 have enjoyed good sales by offering fast charging. More OEMs – such as Nio and XPeng – plan to bring SiC EVs to the market in 2022.

In addition to automotive applications, Yole says that industrial and energy applications have a higher than 20 percent growth rate in the forecast period. High-power charging infrastructure with SiC modules is one application, and the growing installation of photovoltaics.



Among the top SiC device players, STMicroelectronics and Wolfspeed grew their year-over-year SiC revenue by more than 50 percent in 2021, aligning with the 57 percent growth in the global SiC device market. Infineon Technologies delivered a 126 percent growth by entering the main inverter business. Onsemi also entered the game with strong growth in 2021.

As these companies grow SiC to billion-dollar businesses, competition in the coming years can also be identified in supply chain integration. Mergers, acquisitions and partnerships in SiC are reshaping the SiC ecosystem.

The SiC module is the next level for players to compete in, and Yole has identified new products being released for automotive, industrial, and energy applications.

On April 28, 2022, Peter Friedrich, VP SiC at Infineon Technologies, with Poshun Chiu, technology and market analyst specialising in Compound Semiconductor & Emerging Substrates at Yole, and Amine Allouche, technology and cost analyst at System Plus Consulting, will answer questions in a Yole webcast called *SiC evolution: Cars drive a multi-billion dollar business*.

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# BluGlass: High hopes for California dream facility

As laser diode developer BluGlass buys a purpose-built manufacturing facility in Silicon Valley, **REBECCA POOL** talks to President, Jim Haden, to find out his plans for future success

IN LATE MARCH, this year, Australia-based GaN laser diode developer BluGlass revealed bold plans to acquire a laser diode production facility in Silicon Valley, US. For Jim Haden, BluGlass chief executive, buying the fab makes a lot of sense right now.

While the company designs and performs epitaxial growth on its 2-inch GaN substrates at its Silverwater facility in Sydney, it has relied on contract manufacturing for the next steps from wafer fabrication to chip-on-sub-mount packaging, with performance and reliability testing taking place in-house. But not anymore.

Thanks to the Fremont-based laser diode production facility, which churned out InP-based devices in its previous guise, these core fabrication processes will all be brought in-house.



BluGlass  
President,  
Jim Haden

As Haden highlights, this move will eliminate supply chain variability, raise laser diode quality and also provide the company with more control over development, so it can launch more products, sooner.

“While we’ve been making it work, our supply chain has been rather complicated – we’ve been developing lasers and exciting the market, but we believe we will do much better with a captive fab,” Haden tells *Compound Semiconductor*.

“Soon, we’ll ship the epitaxial wafers we grow and characterize at Silver Water to Silicon Valley, where they will be converted to coated bars before being sent to our east-Coast facility in New Hampshire for testing and characterization,” he adds.

Haden is also certain the new set-up will help his company speed up so-called engineering turns. “We’ll be able to reduce the length of time it takes to turnaround and learn from our development runs – combining our learning experiences in this fab will facilitate delivery of a continuous supply of innovative products to the market in less time,” he says. “Contract manufacturers also often have limited engineering and production capacity – they have other customers – so ultimately the new fab will help us to raise our revenues.”

## Unexpected opportunity

Haden came across the 19,000 ft<sup>2</sup> Fremont fab via a friend, who as he says, ‘knew of this company that was shutting one of its fabs’. The chief executive won’t name that company, but following talks, agreed to buy the assets for \$2.5 million, a fraction of the estimated \$40 million it would have cost BluGlass to build the fab from scratch.

“The fab is in Silicon valley with all of its advantages and access to talent,” says Haden. “And it was also manufacturing on two- and three-inch wafers - we’re

on two-inch GaN wafers, so the equipment will be quick to get up and running.”

Equipment-wise, the move from churning out InP- to GaN-based devices should be straightforward. As Haden points out, lithography steps are similar, and the only sticking point may come from the fab’s vision systems being set up for InP wafers, although some plant personnel have experience with GaN power chips.

“This is an epi-ready fab and has everything we need to support epitaxy to wafer processing – initial packaging and testing were also taking place here,” he says. “Our modelling suggests this two-and-a-half-million-dollar investment will give us the capacity to address revenues of around \$170 million. We’ve called the fab a once-in-a-lifetime opportunity as it’s not very often that you come across something like this.”

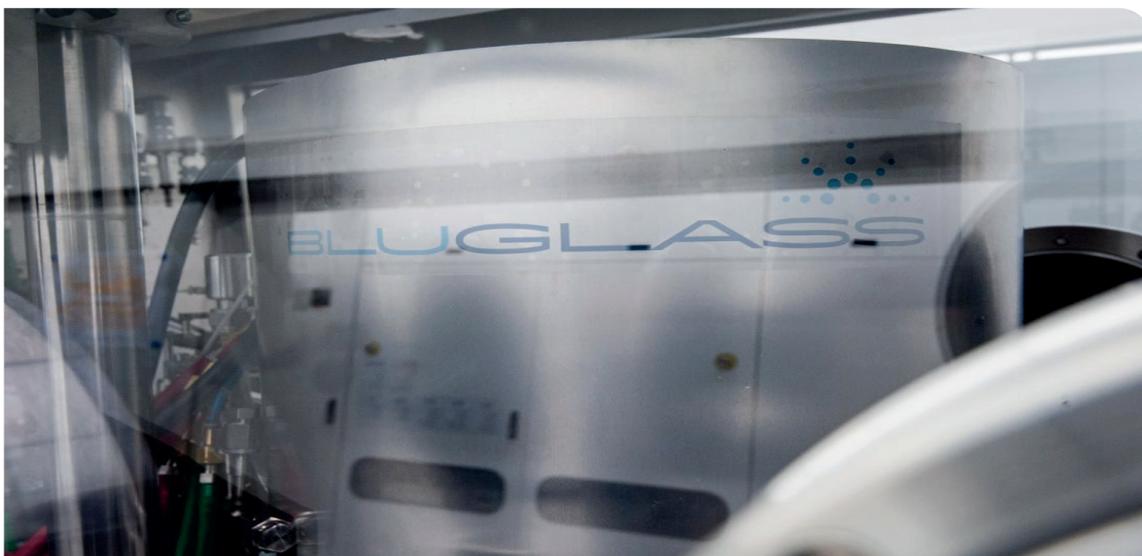
So what happens now? A one-month transition phase with the previous fab owners is currently underway, which includes removing InP materials and cleaning and preparing the equipment for future chip fabrication. After this, BluGlass will get the facility up and running, and Haden reckons process development will commence within a month or two of fab start-up.

Once operating 24/7, the fab will deliver around 10,000 wafers a year, which according to a BluGlass investor relations report is quadruple the annual wafer capacity that could have been reached by its contract manufacturers. The company also predicts wafer production costs to plummet by 50 percent. “We’ve been modelling how we work with contract manufacturers, and taking into account costs such as labour and rent, we think the per wafer cost with the new facility will be about half that of contract manufacturing,” says Haden. “So we have the cost advantage and the ability to learn faster, which becomes a performance advantage.”



BluGlass currently offers a range of single-mode and multi-mode, 405 nm to 450 nm, violet and blue laser diodes, but now intends to develop longer wavelength green, as well as ultraviolet laser diodes, sooner rather than later. “Getting this fab is key to giving us the capacity to accelerate the development of these new wavelength laser diodes,” explains Haden.

He also expects GaN photonics to transition to 4-inch in the not-too-distant future. “It’s difficult to predict exactly how long this transition will take – GaN LEDs that don’t require the same quality substrate required for laser chips will likely transition first,” he says. Still, as the BluGlass chief executive highlights, the Silicon Valley facility is more than pushing them in the right direction. “We’re now more on par with competitors,” he says. “We still have some more capital investments to make, but Fremont is a great step towards competing at this level.”



# Innoscience aims high at global GaN

With new operations in the US and Europe, China's Innoscience is increasing investment and ramping 8-inch GaN-on-silicon production for worldwide markets, reports **REBECCA POOL**

IF YOU WANTED yet more confirmation that GaN players anticipate significant market growth soon, China-based Innoscience recently launched design and sales operations in the US and Europe. Founded in December 2015 to develop high and low voltage HEMTs using its 8 inch GaN-on-silicon technology, the integrated device manufacturer has already shipped more than 30 million devices globally and is currently ramping production at its two China-based fabs.

On-board charging is a market that Innoscience is targeting.

As Denis Marcon, general manager of Innoscience Europe, tells *Compound Semiconductor*: “We have a very nice market share in China, which is getting bigger and bigger, so saw the opportunity to expand our market to Europe and the US.”

“We believe that today's customers are now ready to move full speed into GaN, which is different to how things were several years ago,” he adds.

While many GaN players are currently manufacturing GaN-on-silicon devices on 6-inch wafers, Innoscience has been focused on 8-inch production from day one. Marcon highlights how company founders always believed the market would ‘explode’, and wanted to make affordable chips within a large-scale manufacturing capacity and high-throughput silicon manufacturing processing that guaranteed security of supply.

With this in mind, Innoscience opened its first fab in Zhuhai in 2017 with its second, Suzhou fab, following



in 2020. Combined manufacturing capacity right now is some 10,000 8-inch wafers per month – with 4,000 wafers coming from Zhuhai and 6,000 from Suzhou – but this figure is expected to rise to around 70,000 come 2025, as expansion at Suzhou continues.

Critically, the fabs are kitted out with the latest 8-inch manufacturing tools, including Aixtron G5+C MOCVD reactors – Marcon reckons the company can produce nearly twice as many devices on an 8-inch wafer compared with a 6-inch wafer. And the already automotive-qualified Zhuhai fab is expected to churn out devices for automotive applications come 2024.

“We really invested in production and people used to ask are you going to need that much capacity?” he says. “But now we have a lot of capacity – and huge market requests.”

## Delivering HEMTs

Innoscence is currently manufacturing low-voltage, 30 to 150 V, and high-voltage, 650 V, enhanced-mode HEMTs. As Marcon points out, the company has worked hard to reduce specific on-resistance and shrink device size by depositing a stress-enhancement layer after gate formation, during epitaxy. He also claims both  $R_{DS(ON)}$  and off-state leakage show excellent wafer-to-wafer reproducibility, with both wafer and device yields being high.

“Many companies focus on either low or high voltage devices – as far as I know, we are the only one that competitively offers both in several applications,” says Marcon. “And as well as performance, we offer the largest volume capabilities with strong security of supply.”

So far, power delivery and fast charging has been a key market for Innoscience, with the company also making in-roads to DC-to-DC conversion in data centres and LED drivers. But, of course, electric vehicle markets are key, with Marcon describing lidar laser drivers and DC-to-DC conversion within electric vehicles markets as ‘low hanging fruit’. “I think we will also reach 650 volt on-board chargers

in the near future and then of course there is the main power inverter which is where we all want to go to,” he says.

Marcon isn’t overly fazed by market competition from technology-rival, SiC, here. “We already have a nice history and I think the main battle, especially at 400 and 800 volt, is going to be on price, and our intrinsic cost will be more competitive than silicon carbide,” he says. “But what is missing right now is 1200 V GaN - this is something that we are thinking alongside multi-level conversion as a possible alternative [solution].”

But what about GaN’s age-old reliability concerns? Like many in the industry, Macon believes these are no longer a real issue. As he puts it: “There is tonnes of reliability data and we’ve been carrying out a lot of advanced reliability tests.”

Marcon also points to Texas Instrument’s links to the JEDEC JC-70 Committee for Wide Bandgap Power Electronic Conversion Semiconductors, which recently devised test methods and circuits for continuous switching of GaN power transistors. “We really need to keep working with JEDEC on qualification, which will provide good consumer confidence,” he says. So what now for Innoscience? Besides new US and Europe operations, recent news reports from Asia indicate the company recently won nearly CN¥ 3 billion, some £360 million, in investment funds and now intends to get GaN into as many applications as possible.

For his part, Marcon reckons it will take years for industry players, currently working with 6-inch wafers, to make the transition to 8-inch substrates and deliver wafer capacities that match Innoscience’s present volumes. “We are not yet so well-known in the Western world but this is changing very quickly,” he says. “We are the largest IDM fully-focused on GaN technology, have more R&D engineers than many companies have employees, and want to see GaN in widespread use.”

“So we will now put ourselves in partnership mode and want to form collaborations to see how we can make this happen faster,” he adds.



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## Flexibility between lab and fab

As epitaxial structures become more complex, quality control adopts lab methods

BY TIM GORTER AND LARS GRIEGER, **MALVERN PANALYTICAL**

COMPOUND SEMICONDUCTOR functionality is all about the layer structure. But unlike a cake, it's rare that you wish to slice up your wafer to see what is going on inside.

Fortunately, though, in this instance you can turn to metrology technologies, such as X-ray diffractometry (XRD), to generate accurate and precise structural metrology in a non-destructive manner. Here, advanced capabilities beyond the rocking curves are becoming ever more important for the production of epitaxial wafers.

Production of compound semiconductor wafers continues to rise, as our society seeks to unlock the potential of these materials that offer significant sustainability benefits. If you are a regular reader of this magazine, you will know all too well about the energy savings that come from widespread deployment of compound semiconductors in LEDs or power converters. Increasing manufacturing excellence of

compound semiconductor lowers cost, so that these chips can feature in even more electronic products shipped and sold around the globe.

### Malvern Panalytical's XRD offering



- MRD XL can be upgraded from R&D to FAB configuration
- Clean room ISO 4 available
- SECS/GEM compliance
- Large application envelope with automation available
- World wide support with epi experience

The epitaxial growth these devices is monitored by XRD techniques – but what does the maturation of the compound semiconductor industry mean for analytical XRD instruments and those who use them?

### Method transfer from lab to fab

A significant difference between a typical fab and the majority of research labs is the performance criteria for the equipment. Often the difference comes from the jump in the accompanying quality benchmarks that must be met. Almost all CS fabs maintain a cleanroom environment in line with ISO and federal classifications for their epitaxial department. Consequently, fabs need to adopt the latest Semiconductor Equipment and Manufacturing International (SEMI) standards to ensure that production lines comply with ISO cleanroom practices and enable their yield targets.

In parallel, automation is increasingly widespread, justified by the grown volume in these markets. It is a valuable asset in semiconductor production, with automated solutions reducing the need for human involvement and cutting contamination.

Of course, a significant upfront investment may be needed to set up a fab with the appropriate instruments, technologies, and quality controls to ensure that it runs smoothly – and the financial outlay can cause headaches of its own.

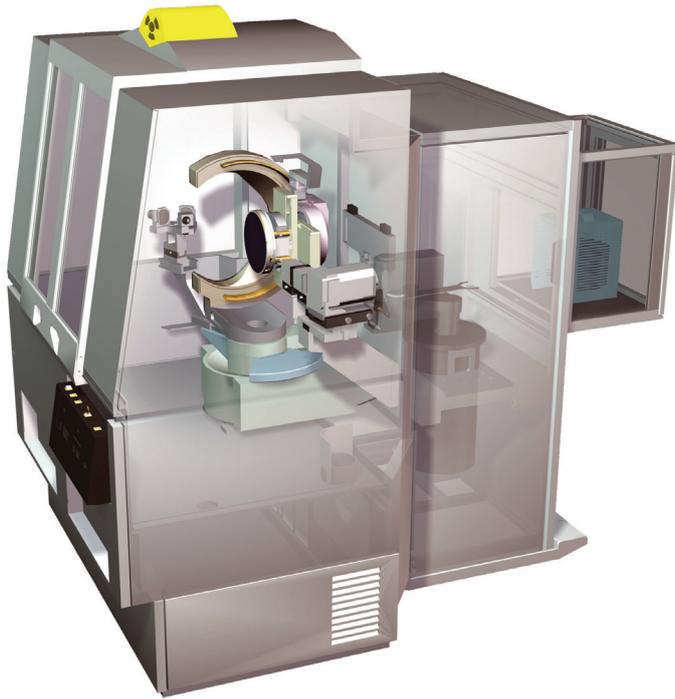


➤ The infrastructure for metrology tools located at R&D sites are different compared to fabrication sites.

The good news is that solutions exist to spread the CapEx. As a compound semiconductor company matures, its needs to undergo a development process, evolving from lab procedures to fab processes. But with multiple options available to those responsible for the tool portfolio employed for the chip production process, making the right choice would appear to be a critical, tough challenge. How does one decide which tool will provide the best functionality and support to ensure a smooth scale-up from research to production? And how can one make sure it is delivered in time?



➤ By making machines futureproof and flexible, Malvern Panalytical keeps working ahead of customer needs and developments within the market, building on years of experience.



► The MRD XL consists of a base module containing the measurement chamber and a frontend providing the automation capability. This makes lab functionality like in-plane measurements available on the fab floor, integrated into standard recipes.

► It is labour intensive to manually place wafers into metrology equipment and less reproducible than a robot with prealigner.

At Malvern Panalytical, we understand what makers of compound semiconductor epiwafers and devices are looking for in their XRD solutions. It all starts with advanced, accurate, precise characterisation of the structural composition of epitaxial wafers – in fact, it all starts with our X'Pert<sup>3</sup> MRD XL. Flexible and reliable, the MRD XL is a world leader in X-ray scattering applications for semiconductor industries. Drawing on four decades of experience in this arena, our technology remains at the cutting edge of what is possible – but wherever our customers

are in their own journey, from development to production, we pride ourselves on having the systems that will support them every step of the way.

Our goal is to ensure that our high-performance instruments and software programs are accessible to labs and fabs working at all stages of the process, from research to quality control. In line with this, our MRD XL is a fully modular design.

By adopting this approach, companies may begin by purchasing our core machine for R&D, before buying add-on fab components from us as and when their operations require them to. It's an approach that avoids a huge initial outlay for a 'fixed' solution that provides functionality beyond what is initially needed. When XRD techniques or production requirements change – by becoming more automated, for example – we recommend purchasing new hardware and software modules, which are easily integrated with the MRD XL.

Having a metrology tool with the flexibility to keep pace with the growth of a product and its manufacturer is a major asset. This is true for small and medium enterprises, for niche fabs producing several different product lines on a single machine and product lines in large fabs that require increasingly complex metrology.

When these firms invest in an MRD XL, it can flex between research to pilot-scale fabrication and finally to full-scale production and back. By growing the capability of the MRD XL piece by piece, fab managers have far more flexibility when considering



their CapEx budgets and timeframes.

Automation is obviously a significant factor in realising the desired cleanroom status. As robotic capabilities continue to advance – perhaps as far as ‘lights-out’ fabs with no hands-on human interference – the importance of relevant SEMI standards is sure to rise. There will be more requirements to adhere to, such as the SEMI E5 (SECS-II) and E30 (GEM) standards, a pair of key protocols governing communications between the equipment and the host or carrier. Enabling the transfer of bespoke measurement data, these interfaces are essential to the success of any semiconductor fab infrastructure.

Delivering superior semiconductor materials and devices clearly depends on much more than just having excellent XRD metrology for wafer analysis. SEMI-standard fabs have to have a consistent, high-quality, reliable process for chemical mechanical polishing (CMP), both for substrate polishing and during processing. Just as a layered cake may need its top trimmed and flattened before icing is applied, a wafer surface needs the right planarity to ensure that all the deposited layers sit on top of one another exactly as required. Here our particle sizing products Mastersizer and Zetasizer allow tight control of slurry specs with a push of a button.

In any fast-moving industry, decision makers must keep an eye on the future – or find a trusted partner with the capabilities to do that for them. For those chip makers and developers partnering with us, this is not a concern for them, because they never need to worry about investing in lab-to-fab equipment that will quickly be outstripped by newer models. Our solutions are informed by decades of experience, a wealth of expertise and run easily for more than a decade.

Some compound semiconductor developments are already coming into view on the horizon, such as lights-out fabs, the shift to larger wafer sizes, and the increasing complexity of superlattices in compound semiconductors. Other, more distant advances are harder to foresee. But we are dedicated to continuously improving and upgrading our hardware and software to ensure that these solutions – and our customers – are always ready to tackle and overcome the next challenge.

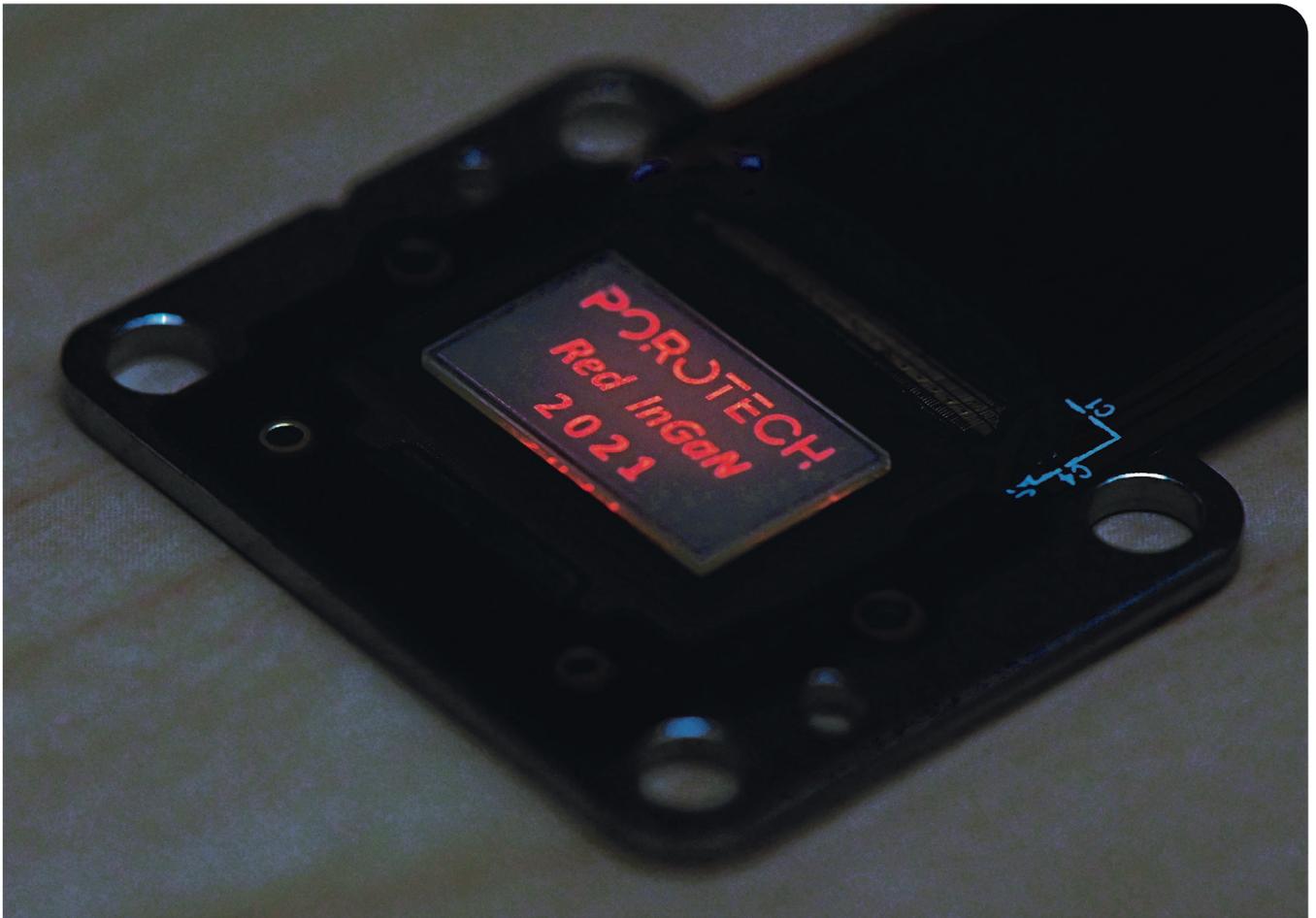


➤ Malvern Panalytical delivers a multitude of metrology tools for the semiconductor and electronics industry such as particle characterization equipment used for CMP slurries, like the Mastersizer.



➤ Malvern Panalytical understands the full process from front-end to electronics assembly and offers more solutions, not mentioned here.

Lab to fab investments come with CapEx. Malvern Panalytical offers flexible XRD solutions which can grow with your company's needs



## Simplifying displays with porous GaN microLEDs

GaN-based red microLEDs are now delivering a comparable performance to their blue and green cousins, thanks to the introduction of a simple step that produces porous material

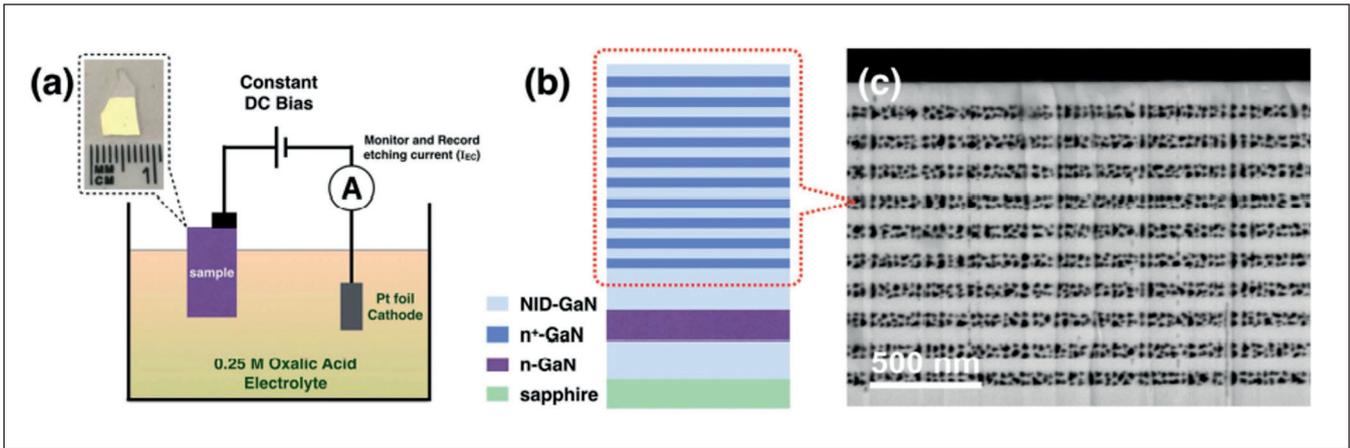
BY TONGTONG ZHU FROM **POROTECH**

OVER OUR LIFETIME displays are continuing to evolve. Many of us have already witnessed a shift from TVs based on cathode ray tubes to those featuring liquid crystals, initially backlit with cold cathode fluorescents and now LEDs. Over the coming years, we shall see a growth in sales of near-eye displays, supporting virtual reality, head-up displays and augmented/mixed reality applications.

These emerging forms of technology are placing tougher demands on display performance. Driven by this demand, new display technologies are undergoing rapid development, with microLEDs leading the way. These miniature marvels are the

front runner for next-generation displays, because compared with rival technologies based on LCDs, LEDs, miniLEDs and organic LEDs, they offer an outstanding set of attributes: superior brightness, high contrast, unparalleled efficiencies, a longer lifetime, and increased stability. What's more, thanks to the 'micron-scale' size of these microLEDs, they deliver a far higher image resolution.

To match human visual receptors and provide a really realistic image, full-colour displays need to combine sources with red, green and blue emission. This requirement has led designers to employ red, green and blue emitters that can be independently



► Figure 1. (a) Porotech employs a relatively straightforward set-up for electrochemical etching. The inset shows a photograph of a sample after etching under room-light illumination. (b) Schematic of the DBR structure. (c) Cross-sectional scanning electron microscopy image of the 10 pair GaN/mesoporous-GaN DBR structure.

modulated. Ideally, this is accomplished with a simple, lightweight display architecture that is capable of meeting all criteria for next-generation displays.

In such an architecture, it is the norm to employ InGaN-based microLEDs as the high-efficiency blue and green emitters. With conventional means, it is not possible to stretch the emission of these devices to the red while retaining efficiency, so the source that's used to cover that spectral domain is the red AlInGaP microLED. Combining this with InGaN devices emitting in the blue and green offers a way to make full-colour displays.

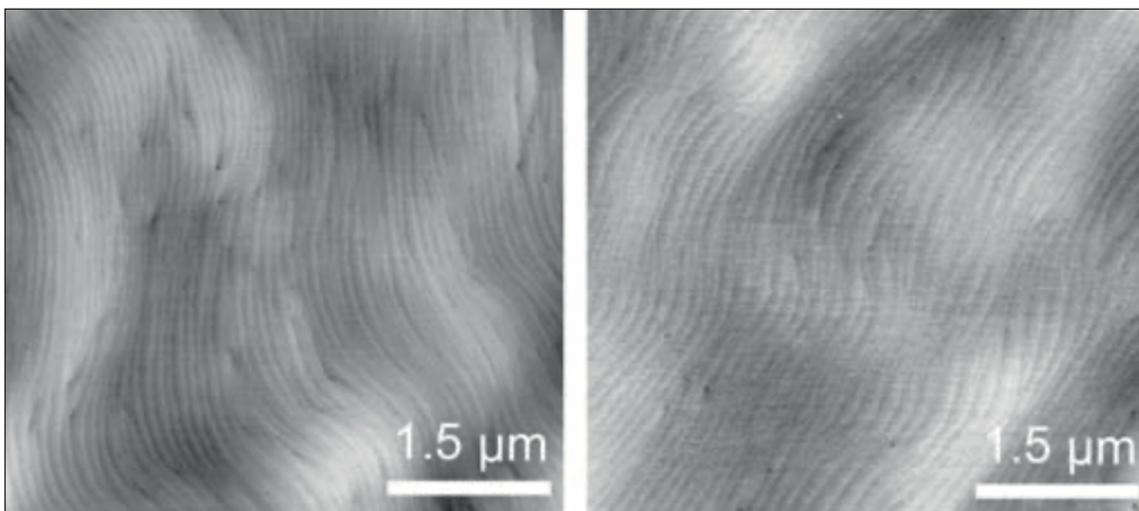
Unfortunately, this mixed-material approach is far from ideal, presenting several significant barriers to widespread adoption of microLED-based displays. One concern is that compared with InGaN-based devices, red AlInGaP LEDs suffer from a more severe drop in efficiency as device size diminishes. This makes it difficult to meet the performance and pixel sizes demanded by the likes of alternative-reality and mixed-reality applications. Another

concern that's also related to the performance of the AlInGaP LED is that its decline in efficiency with increasing temperature is far more pronounced than that for its GaN-based cousin, adding complication and expense to the final display design.

As well as those stumbling blocks associated with performance-related criteria, there are issues related to production costs. Mixing multiple material systems over micron-length scales necessitates the development of complex and expensive mass-transfer technologies for positioning individual red, green and blue chips into the desired pixel design. One consequence is a substantial addition to the final device cost, limiting applicability of this approach to the mass market.

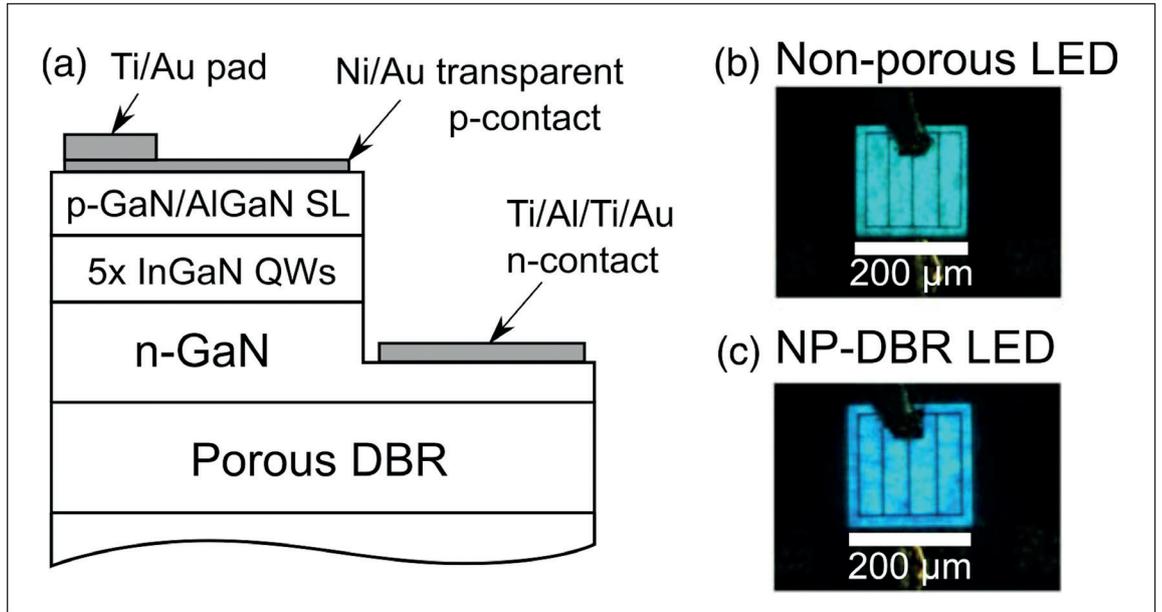
### Removing barriers

To address these issues, our team at Porotech, a spin out of the Cambridge Centre for Gallium Nitride, has developed a porous InGaN platform that delivers all three primary colours with a high efficiency.



► Figure 2. Atomic force microscopy images of a template surface (a) before and (b) after electrochemical porosification, showing that the smooth surface and the epi-ready terraces are maintained. Z-scale (black to white): 4 nm.

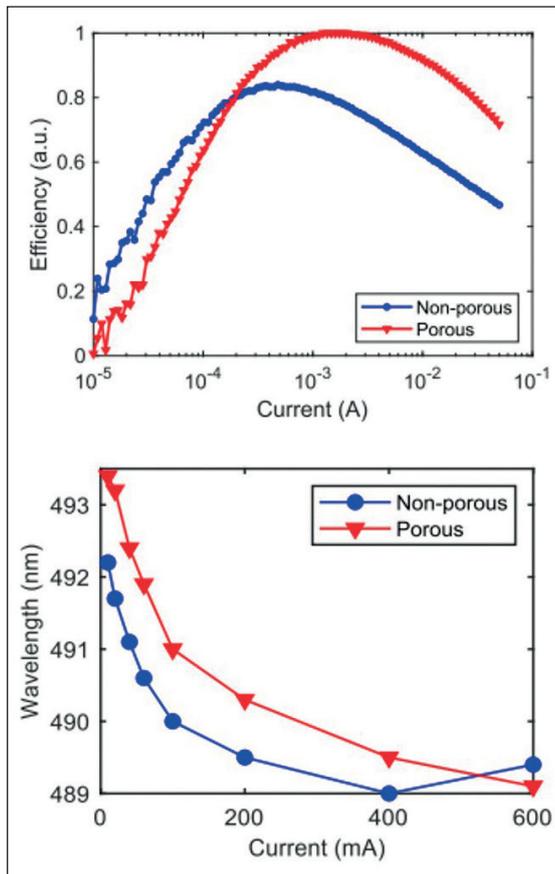
► Figure 3. Porotech has processed wafers (a) to produce (b) non-porous LEDs and (c) a mesoporous DBR LEDs.



Realising red emission with InGaIn has not been easy, due to strain that stems from the lattice mismatch between InGaIn and GaN. This condition limits the proportion of indium that can be incorporated within the InGaIn quantum well, and therefore restricts emission to shorter wavelengths. To relieve this strain, we introduce an engineered subsurface porosity. This allows more indium to be incorporated into the wells, and ultimately extends emission into the red.

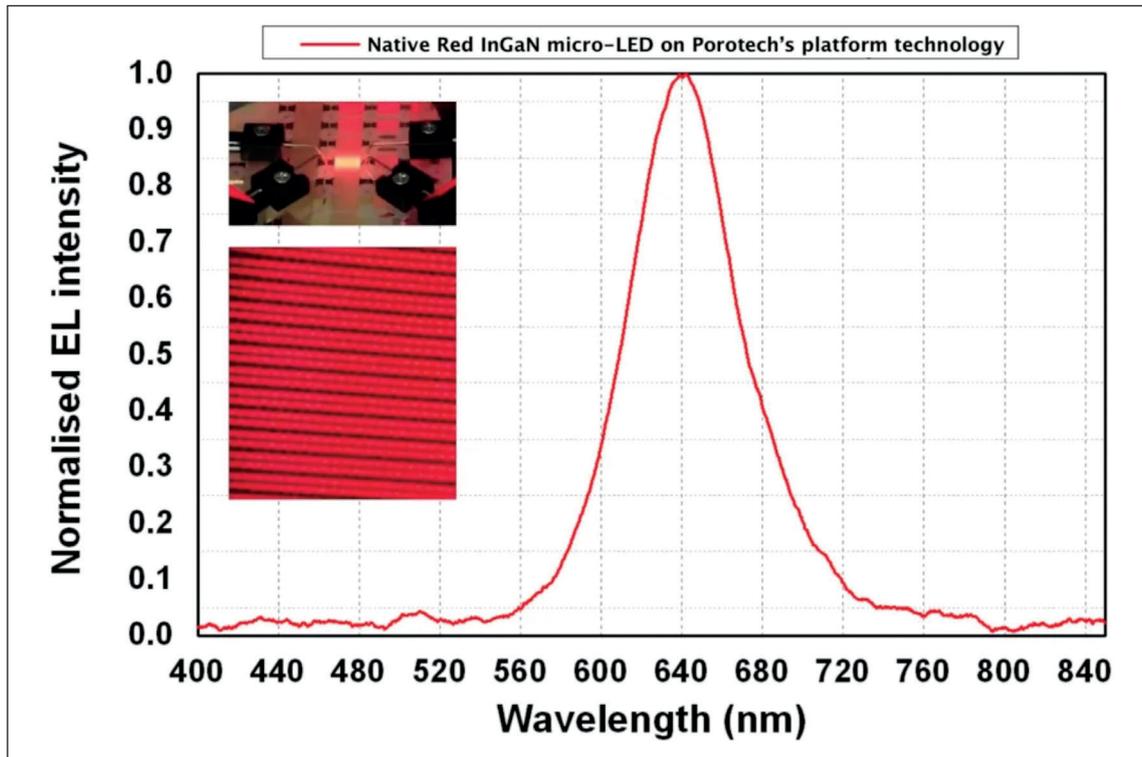
The benefits of our technology are not limited to the obvious, crucial breakthrough of realising all three colours on the same InGaIn platform. Additional strengths of our approach are that they tackle the efficiency-size problem for the red emitter, and they simplify the transfer technology for making full-colour displays. Furthermore, since the porosity we introduce is sub-surface, the surface is left intact – this means that the rest of the supply chain for LED device manufacturing does not require adaption in its processes or investment in new equipment. It is also worth noting that by introducing strain relief, we ensure an additional benefit of reduced wafer bow – this simplifies and increases the yield of monolithic displays produced by direct wafer-to-wafer bonding. And last but by no means least, our process is highly scalable and reproduceable, ensuring excellent uniformity across the wafer, from wafer-to-wafer, and from batch-to-batch.

► Figure 4. (top) Light-current (L-I) measurements for devices made by Porotech that are processed on porous and non-porous templates. (bottom) Plots of peak position showing similar blue-shifts with increasing injection current.



One of the essential building blocks for developing next-generation optoelectronic devices is the distributed Bragg reflector (DBR). Formed from alternating layers of high and low refractive index material, the DBR can be thought of as a one-dimensional photonic crystal. When incorporated within an LED, the DBR acts as an integrated mirror and/or filter, helping to direct and tune the emitted light. As well as providing high reflectivity and low absorption, the DBR ideally has good conductivity, allowing efficient electrical injection of charges into the device. An excellent candidate for the DBR is the non-polar III-nitrides, a family of materials that combine higher rates of radiative recombination for improved device efficiencies with unique, attractive properties, such as the emission of strongly linearly polarised light. Note that non-polar DBRs are used alongside conventional, polar LEDs, making this technology applicable to today's high-volume fabs.

It is very difficult to apply conventional epitaxy-based polar nitride DBR fabrication, involving the growth



► Figure 5. Porotech's demonstration of the world's first native red InGaN-based microLED using its platform technology.

of alternate layers of different nitride alloys with different refractive indexes, to non-polar orientations. The problem is that there are no available alloys that will lattice-match to non-polar GaN. Attempts to do so lead to cracking and low reflectance.

Overcoming this issue are a number of DBR fabrication strategies for non-polar GaN-based structures, including mesoporous DBRs. This form of DBR has much merit, offering a spectral response that can be tuned in three ways. As well as adjusting the layer thicknesses and the number of repeat periods – this pair of levers can be applied to all forms of DBR – porosity can be varied, leading to changes in refractive index contrast.

Our core technology is based on the mesoporous DBR, which we have collectively spent decades studying and developing.

We advocate a one-step, selective electrochemical process for porosification (see Figure 1 for an illustration of this process, as well as an image of the resulting DBR microstructures). This step can be carried out at room temperature in constant voltage mode using no UV illumination, with the removal of material monitored via the etching current signal. The electrochemical process begins with localised injection of holes, driven by applying a positive anodic bias. Alternating  $n^+$ -GaN layers are oxidised under this condition.

A cross-sectional scanning electron microscope image of the resulting nanoporous DBR structure confirms that it is just the  $n^+$ -GaN layers that are etched into the mesoporous structure (see Figure 1 (a)). Etching is uniformly achieved across the entire

sample that's submerged in the etching solution, demonstrating the high uniformity of the process. When processing batches of wafers in this way, a high level of uniformity is maintained wafer-to-wafer and batch-to-batch – this demonstrates the scalability of this approach and its applicability to mass-manufacture of optoelectronic devices.

One of the major advantages of the selective porosification process is that, by only etching the  $n^+$ -GaN layers, by design the surface of the template remains unchanged. Evidence of this is provided by atomic force microscopy images of a template before and after electrochemical porosification (see Figure 2). It is possible for etching to penetrate undoped GaN layers via nanoscale vertical pathways that exist in the as-grown material (no pre-patterning is necessary).

A practical implication of maintaining the same surface is that the porous wafers can be processed into LEDs without having to change any downstream processes. Or, to put it another way, chipmakers can exploit the benefits of the porous DBR structures without having to disrupt their device manufacturing supply chain.

## Device demonstrations

We have shown that porous GaN templates can be processed into LEDs using industry-standard recipes, and that the resulting devices deliver an improved efficiency, thanks to the mesoporous DBR structure.

Our initial demonstration involved the use of MOCVD for GaN template growth and LED regrowth. We grew a pair of templates with a dislocation density of around just  $3\text{-}6 \times 10^8 \text{ cm}^{-2}$  and a latent

mesoporous-DBR structure, formed from alternating layers of undoped and highly *n*-doped GaN. We applied an electrochemical porosification process to one of the wafers, before processing both into blue-emitting *p-i-n* LED structures (see Figure 3 (a) for an illustration of the device's design, and (b) and (c) for optical micrographs, demonstrating the relatively uniform electroluminescence emission from both non-porous and porous samples). As the uniformity of emission is similar in both structures, we can conclude that the growth of the LED layers is not significantly altered by the presence of the mesoporous-DBR in the regrowth template.

Electrical and optical measurements have been conducted on both types of LED. Plots of the light output at various drive currents show that the introduction of porosity to the DBR delivers an increase in the maximum efficiency, and shifts the onset of efficiency droop to a higher current density (see Figure 4). In both samples, the shift in peak wavelength with injection current is similar.

By demonstrating a similar performance with increased efficiency, we have equipped our team with the foundation for delivering InGaN-based blue, green and, critically, red microLED technology and products. Another benefit that comes from using the porous structure is a reduction in wafer bow – it is trimmed by more than 30 percent, due the strain relief that stems from the introduction of porosity. Reducing bow helps to ensure a high-yield LED for epiwafer production, chip processing and wafer-to-wafer bonding, especially for microLED displays, where it is crucial to have better than micron-scale precision.

### A red revolution

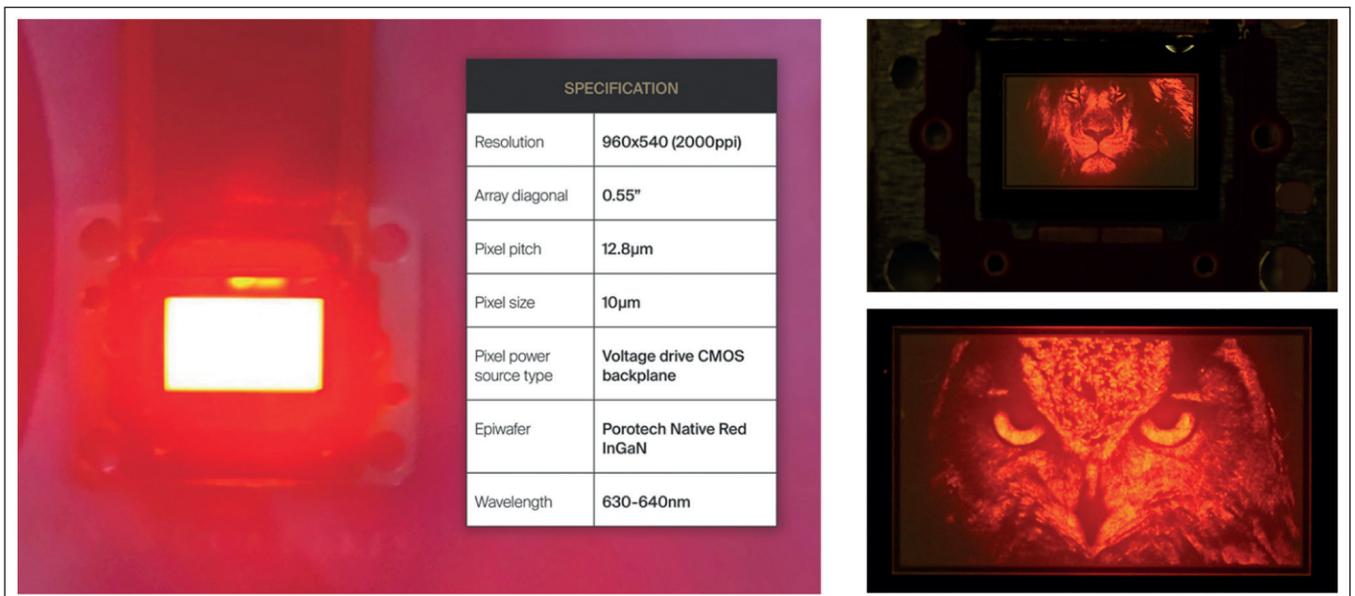
Following further development, we have used our porous platform to deliver the world's first native

InGaN-based red microLED. This milestone removed a key bottleneck for the whole industry. Our porous structure relieves strain that is introduced by the lattice mismatch between the InGaN and GaN, and allows greater concentrations of indium to be incorporated without degrading material quality. Emission is shifted to the red, with the peak wavelength occurring at 640 nm (see Figure 5).

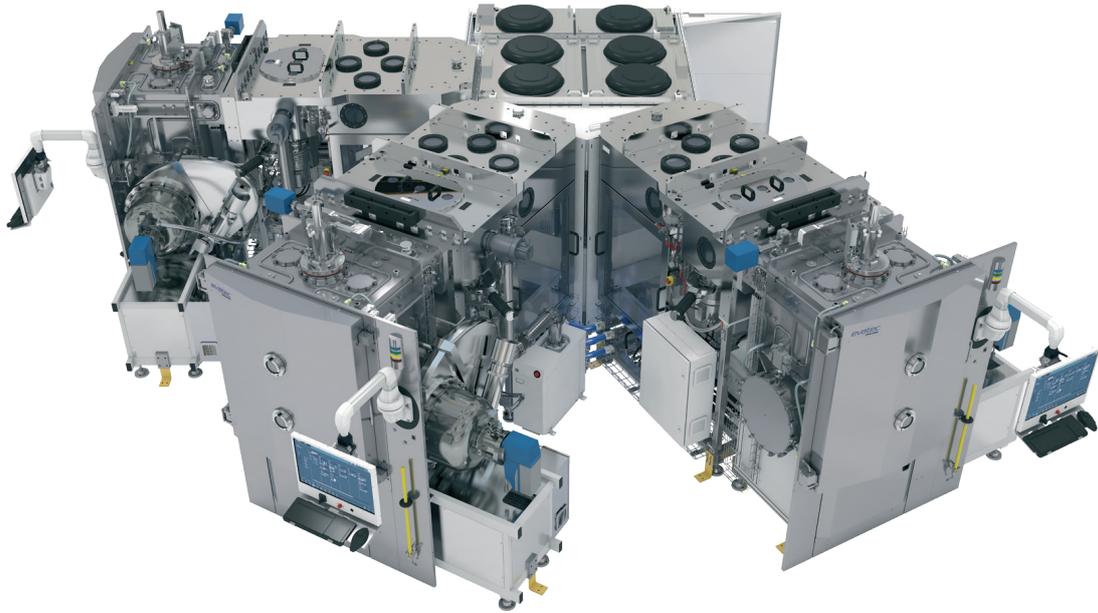
We have used our porous-enabled red microLED technology to produce the world's first native InGaN-based red microdisplay (see Figure 6), which has an active area of 0.55 inches diagonally and a resolution of 960 by 540, equating to 2000 ppi. This microdisplay provides an initial and quick demonstration that proves the capability of our technology. When we remove sapphire, we expect an increase of the brightness of this display and reduced backscattering.

With this demonstration we have shown, for the first time, that all three light-emitting elements can be produced with a single toolchain. This breakthrough highlights how to eliminate the complexity and expense associated with fabricating displays that mix devices from different material families.

Our successes have placed us in an enviable position where we can play a crucial role in the future of microLED displays. We are attracting much attention, thanks to our demonstration of the world's first native InGaN red microdisplay, and the breaking of a major barrier, by showing that a single material system can be used to make green, blue and red microLEDs. The scalability of our process, along with the lack of disruption to the rest of the supply chain, positions our technology as a critical enabler for the mass manufacture of next-generation display technologies.



➤ Figure 6. Porotech has demonstrated the world's first native InGaN red micro-LED display. Note that the sapphire has not been removed – hence further improvements in backscattering and brightness can be achieved with further optimisation.



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## Getting PICs off the ground

PICs based on InP and GaAs prepare to slash the size, weight and power of systems to be deployed in space and on-board aircraft for a variety of sensing applications

BY JONATHAN KLAMKIN, PAUL VERRINDER, VICTORIA ROSBOROUGH AND FENGQIAO SANG FROM THE [UNIVERSITY OF CALIFORNIA SANTA BARBARA](#)

ONE OF THE MOST powerful technologies of our time is the photonic integrated circuit (PIC). By integrating all the required functions on a single chip, the PIC significantly reduces the cost, size, and weight at the system level, while improving performance, stability, and reliability.

To produce this multi-faceted photonic device, wafers are processed in a manner that is similar to that employed for the electronic circuits that have revolutionised our society. However, the materials that are used can be somewhat different. While silicon is the semiconductor of choice for making electronic circuits, those employing photonics can also be formed from InP and GaAs. Both these III-Vs are attractive options, because they enable monolithic integration of gain material for light sources and their amplification.

Pioneers of the PIC developed this technology with telecommunications applications in mind. They focused on the centre-band, or C-band, which spans the spectral range from 1530 nm to 1565 nm, a domain associated with ultra-low-loss transmission of light through an optical fibre. Recently, though, PICs have gained traction in applications involving the O-band (1260 nm to 1360 nm), such as optical interconnects within and between data centres.

Note, though, that the potential for PICs is not limited to these wavelengths, nor to communications, or even to terrestrial applications. There are opportunities lying well beyond these boundaries, such as those we are exploring at the University of California, Santa Barbara (UCSB). We are targeting space and airborne applications of PICs, namely free-space communications, remote

lidar for gas sensing and topographical lidar. Our work on free-space communications has focused on extending the power-handling capabilities of InP PICs. Success on this front opens the door to higher data rates and/or longer link distances. Output powers with our InP PIC platform have exceeded 250 mW, a value far higher than any previous demonstration.

We have also broken new ground while participating in a NASA-funded project entitled IMPRESS Lidar – short for *Integrated Micro-Photonics for Remote Earth Science Sensing Lidar*. Through this project we have demonstrated the first ever fully functional PIC-based gas remote sensing lidar system that targets atmospheric CO<sub>2</sub>. This system operates near a relatively weak absorption line that is centred at 1572.335 nm, a wavelength falling within the communications L-band (1565-1625 nm) that allows us to leverage mature InP PIC technology. Through this project we have been able to demonstrate a shrinking of the system volume by a factor of more than one hundred, compared with a system built with discrete components by collaborators at NASA.

Another avenue explored by our team has been the development of a GaAs-based PIC, which extends operation to other spectral domains. This tuneable laser PIC, developed for 10XX nm wavelengths, features beam-steering capability when it is used in conjunction with diffractive optical elements.

### Sensing gases with InP PICs

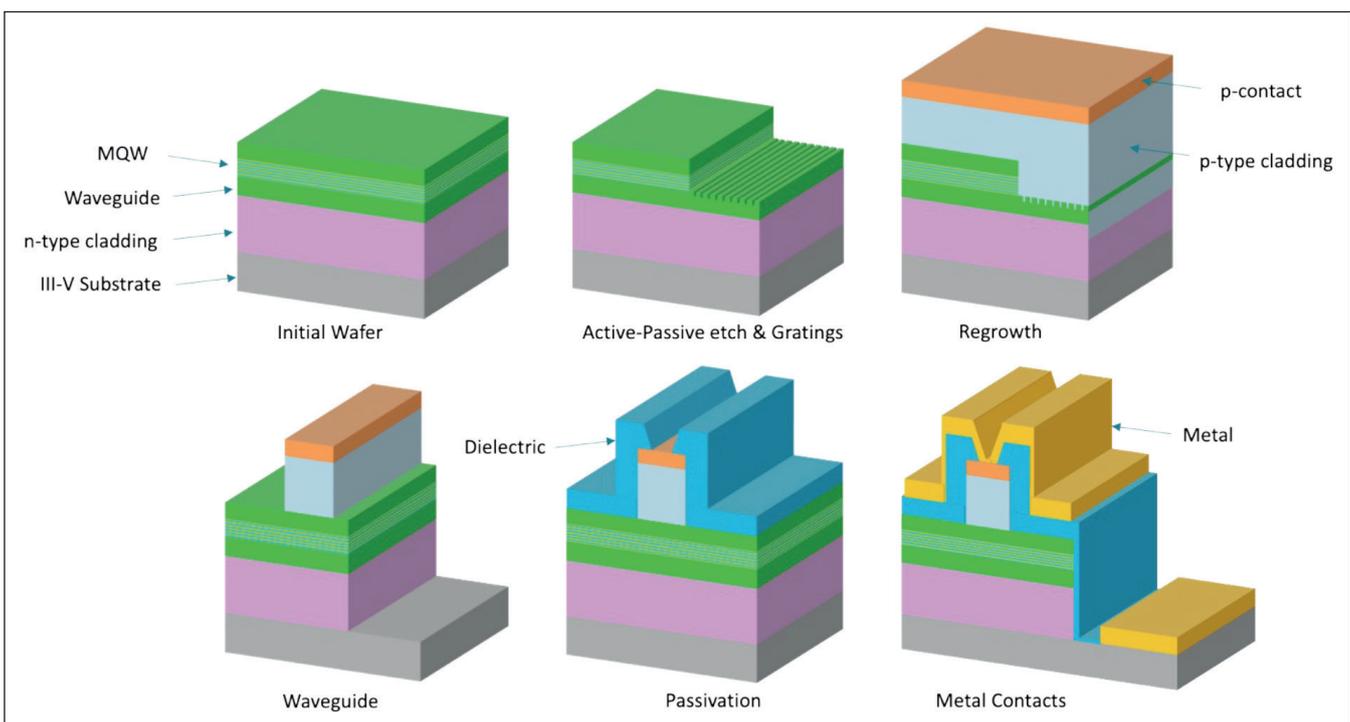
Our InP PIC platform, equipped with high-efficiency lasers, provides broad wavelength coverage across the 1.2 μm to 1.6 μm range. This platform is ideal for active remote sensing of CO<sub>2</sub>, which can be accomplished with a laser source at the sensing

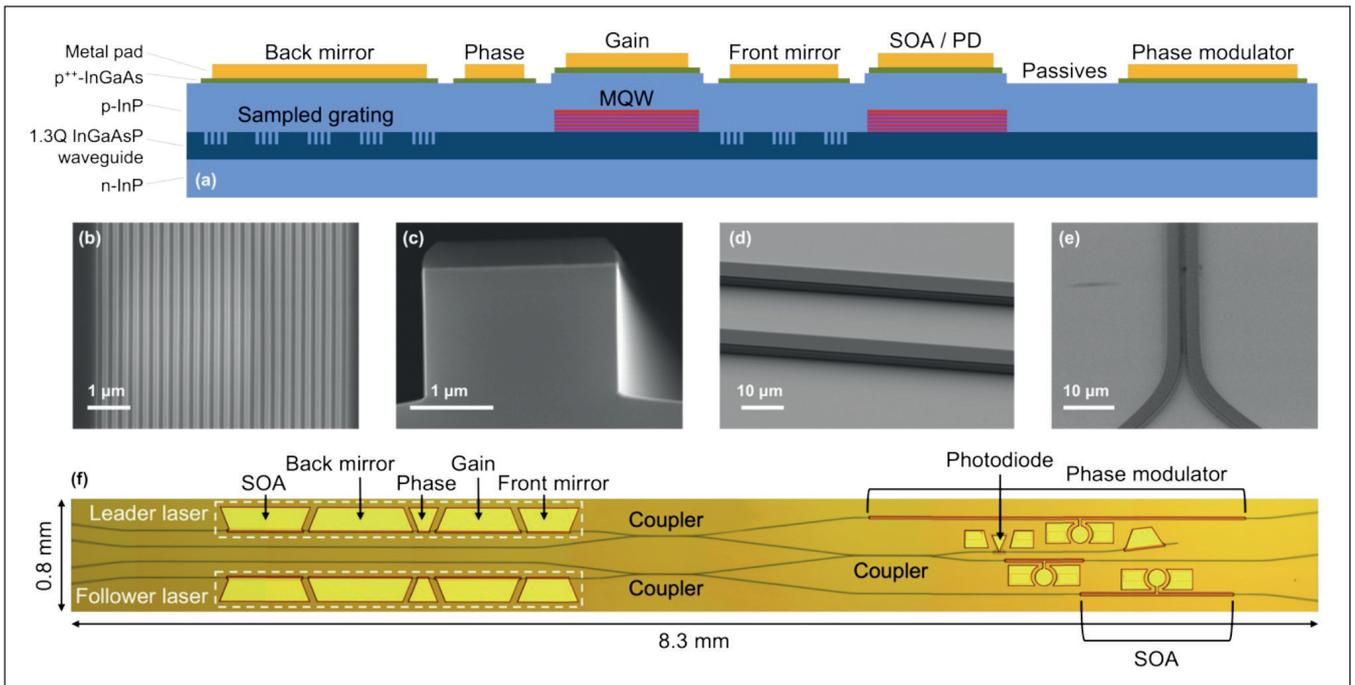
wavelength of 1572.335 nm, using a sensing window of 30 GHz. A PIC-based approach for CO<sub>2</sub> sensing has many merits over the active remote sensing systems formed from commercial off-the-shelf optical components, which are compromised by their size, weight, and high power consumption. Usually, sensing experiments are performed from a near earth orbit, to minimise the high cost associated with launching large spacecraft into orbit. One of the strengths of our PIC technology, which has the potential to enable systems that are far more compact and power efficient, is that it could lead to increased deployment of this form of sensor on small spacecraft that launch more often.

The PICs we produce are designed and fabricated with what we refer to as an offset quantum-well platform. We deposit multi-quantum wells on top of a low-loss waveguide core in such a way that the wells are slightly offset from the centre of the vertical optical mode. Taking this approach enables us to selectively remove the wells to form separate active and passive regions. Coupling between those regions is high, typically between 90 and 95 percent, with reflections managed by angled interfaces. The active regions, where wells remain, provide gain in laser cavities and optical amplifiers. Meanwhile, the passive regions, where wells are absent, contain mirrors, filters, phase-tuning elements and optical modulators, as well as interconnects between sections and components (see Figure 2(a) for a sideview of the offset quantum well PIC platform used for InP CO<sub>2</sub> active sensor development).

To form our gratings, we etch into the waveguide core layer after defining active and passive regions. Adopting this approach enables us to form sampled

► Figure 1. Overview of III-V PIC fabrication process.





► Figure 2. (a) Simplified side-view schematic of an offset quantum-well PIC platform. Scanning electron microscopy images of (b) the top-view of fabricated gratings for the sampled grating distributed Bragg reflector (SGDBR) lasers, (c) cross-section of a fabricated ridge waveguide, (d) plan-view of two parallel waveguides, and (e) plan-view of a directional coupler with a 1 μm gap between the waveguides. (f) Top-view optical microscope image of a fully fabricated CO<sub>2</sub> lidar PIC.

grating distributed-Bragg-reflector (SGDBR) lasers, which provide leader and follower lasers for the active sensor. These lasers combine a gain section for generating photons with a back SGDBR mirror, a front SGDBR mirror, and a phase tuning section. As the sections of the laser are electrically isolated, each can be addressed separately. In addition to providing gain for a laser, active sections may also be used to form: a photodiode, which operates under reverse bias; and a semiconductor optical amplifier, operating under current injection. The amplifier can compensate for passive waveguide losses and boost the PIC output power.

Images acquired with a scanning electron microscope reveal the various elements during the fabrication process (see Figure 2 (b) to (e)). Even with an optical microscope, it is possible to identify the various components of a PIC designed to sense CO<sub>2</sub> using lidar. This PIC, with a footprint of approximately 0.8 mm by 8.3 mm, employs passive waveguides and directional couplers to route optical signals and connect active and passive elements. After the leader laser is a directional coupler and a phase modulator, the latter of which stabilizes the laser. The follower laser is followed by a directional coupler and a semiconductor optical amplifier, incorporating a high-speed pad configuration that enables encoding of high extinction pulses. Directional couplers tap a fraction of the signals from the leader and follower lasers, routing the combination to a high-speed photodiode.

Our PIC-based CO<sub>2</sub> sensing architecture, illustrated in Figure 3, features a leader laser that is locked to the 1572.335 nm CO<sub>2</sub> absorption line by an absolute CO<sub>2</sub> reference cell. An integrated phase modulator, driven at 125 MHz, enables the use of a frequency modulation technique. Fed with an output signal, a mixer extracts an error signal, which is fed to a control servo for signal filtering and processing, and coupled to the phase section of the leader laser to realise locking. An optical phase-lock loop, leveraging the high-speed photodetector for beat-note detection, enables the follower laser to be offset-locked to the leader laser by +/- 15 GHz. The output of the follower laser is coupled to a semiconductor optical amplifier pulse carver, which aids generation of the desired frequency-stepped pulse train for gas sampling.

An illustration of the measured error signal and gas transmission for the absolute reference cell, measured using the leader laser, is shown in Figure 4 (a). We have measured stabilization over 30 minutes with a 1 second gate time, and compared performance with and without feedback to characterize the relative impact of the stabilization circuit (see Figure 4 (b)). Without feedback, the peak-to-peak frequency stability is typically 675 MHz and the frequency standard deviation 86 MHz. Introducing feedback delivers a tremendous impact, with measurements revealing a reduction in the peak-to-peak stability to 2.75 MHz and a fall in the standard deviation to 465 kHz.

Once the leader is stabilized, the follower laser can be offset-locked to it. Our measurements, considering laser stability over 30 minutes with a 1 second gate time, show that the introduction of an optical phase-lock loop cuts the peak-to-peak frequency stability down from 1.36 GHz to 29 kHz, and the standard deviation from 181 MHz to 3.61 kHz.

Additional measurements of this PIC by our team show: that the optical spectra for the stabilized leader laser and for the follower laser can be offset by between 1-15 GHz (see Figure 4(d)); and an exemplary pulse can be generated with the semiconductor optical amplifier that follows the leader laser, demonstrating an extinction of 40 dB when swinging the drive current from 0-100 mA (see Figure 4(e)). We have also generated a frequency-stepped pulse train, enabling measurements of a CO<sub>2</sub> sample in a separate pressurized tube cell (results are reported in Figure 4(f)). Taken together, our set of measurements confirm the full operation of our PIC CO<sub>2</sub> lidar system.

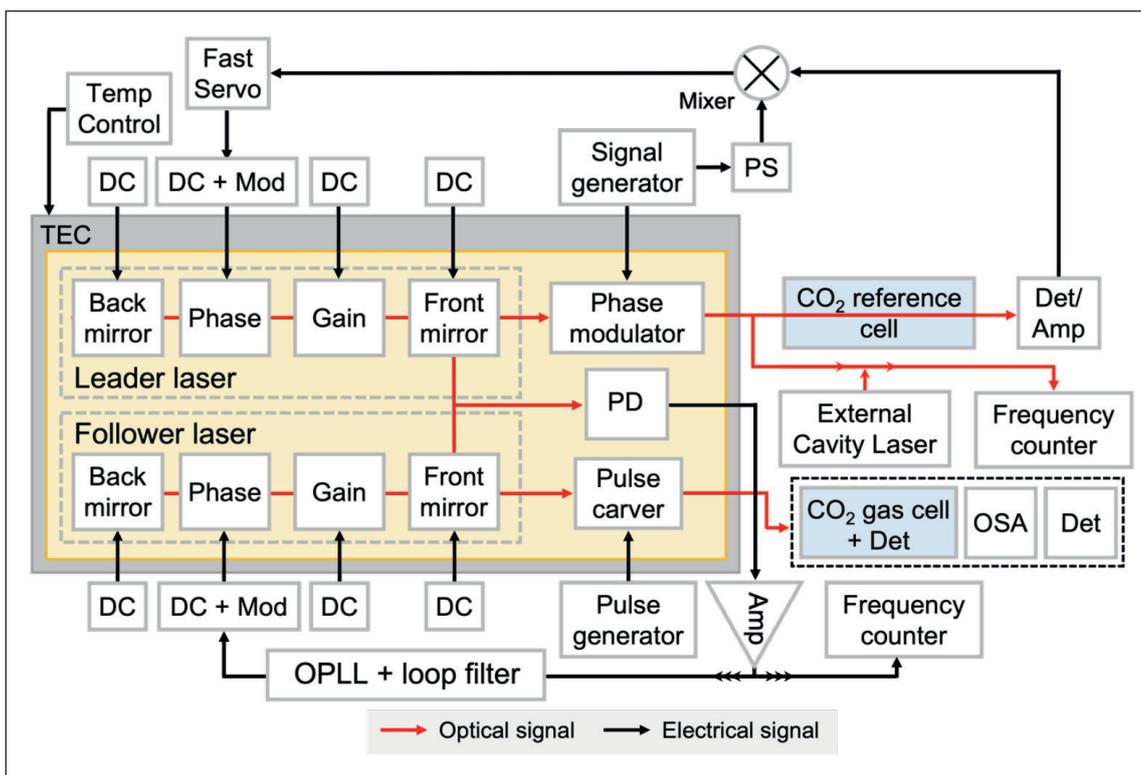
### Topographical lidar with GaAs PICs

As today's airborne topographical lidar systems tend to be built from commercial off-the-shelf components, such as bulk and discrete optics, this restricts their deployment to larger spacecraft or aircraft. One such example is NASA's Land, Vegetation and Ice Sensor, which is mounted on a Beechcraft B200 King Air. It will now come as no surprise that to enable deployment on small satellites, such as CubeSats, there needs to be a substantial reduction in size, weight and power – requirements that can be realised once again by turning to PIC technology.

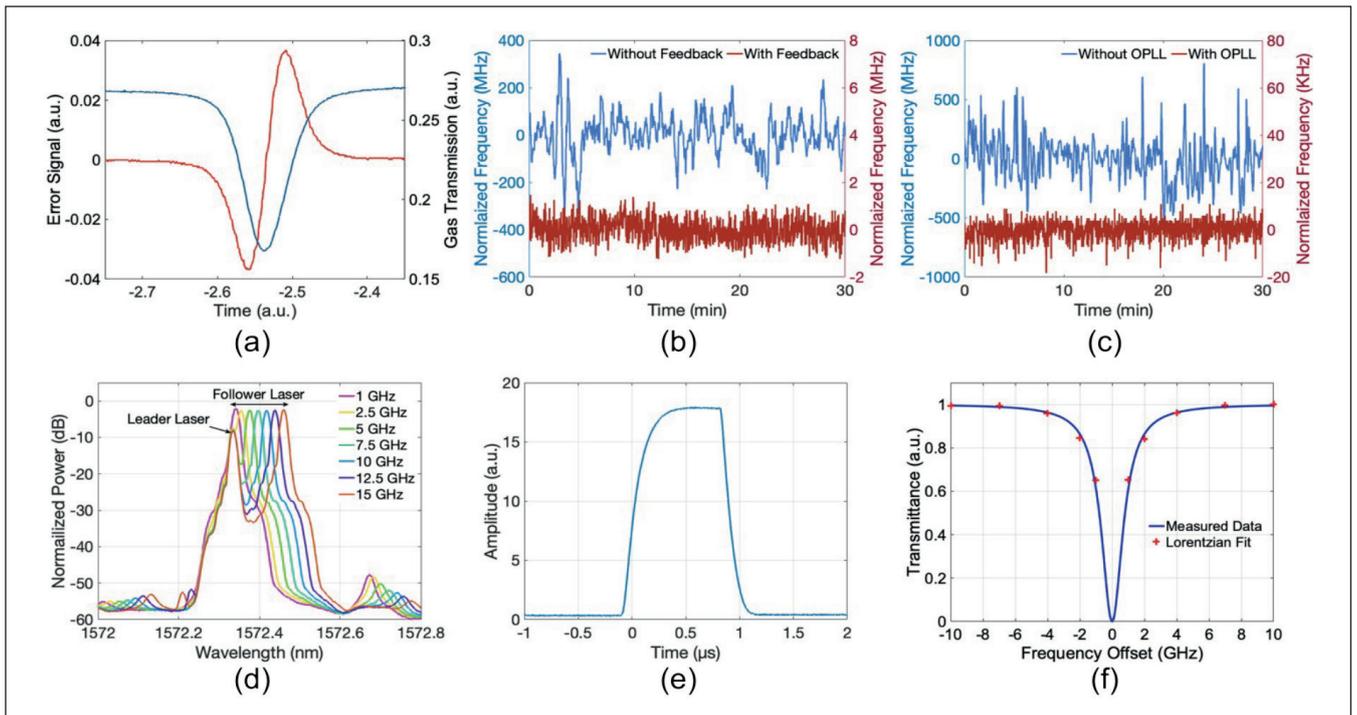
For topographical lidar, the laser typically has a wavelength near 1000 nm, which is within a spectral range that has a relatively low atmospheric absorption and benefits from the existence of highly sensitive detectors. As this wavelength region requires the GaAs material platform, we have adapted our PIC platform for this III-V. We have fabricated a widely tunable laser, producing a centre wavelength near 1030 nm, which can be combined with diffractive optical elements for beam steering. Tuning the wavelength of the laser alters the angle of reflection from the grating element and effectively steers the beam, enabling wider surface coverage.

Our laser consists of a gain section, front and back mirrors for coarse wavelength tuning, and a phase section for fine wavelength tuning (see Figure 5 (a) for a side-view schematic, Figure 5 (b) for a top-view microscope image of the fabricated chip, and Figure 5 (c) for scanning electron microscopy image of a laser chip mounted on a carrier, with the metal pads wire-bonded to the carrier traces).

To tune the laser's output wavelength, we apply a current to the mirror and the phase sections. Coarse wavelength tuning is accomplished by tuning front and back mirrors, while fine tuning is realised with adjustment to the phase section. Our measurements show eight different lasing output spectra overlaid, demonstrating approximately 22 nm of coarse wavelength tuning (see Figure 6 (a)), and the use of the phase section for finer wavelength tuning (see Figure 6 (b)). We have also produced contour plots, which show the laser wavelength as a function of front and back mirror tuning, and demonstrate the full tuning capability (see Figure 6 (c)).



► Figure 3. PIC remote lidar CO<sub>2</sub> sensing architecture and test schematic.

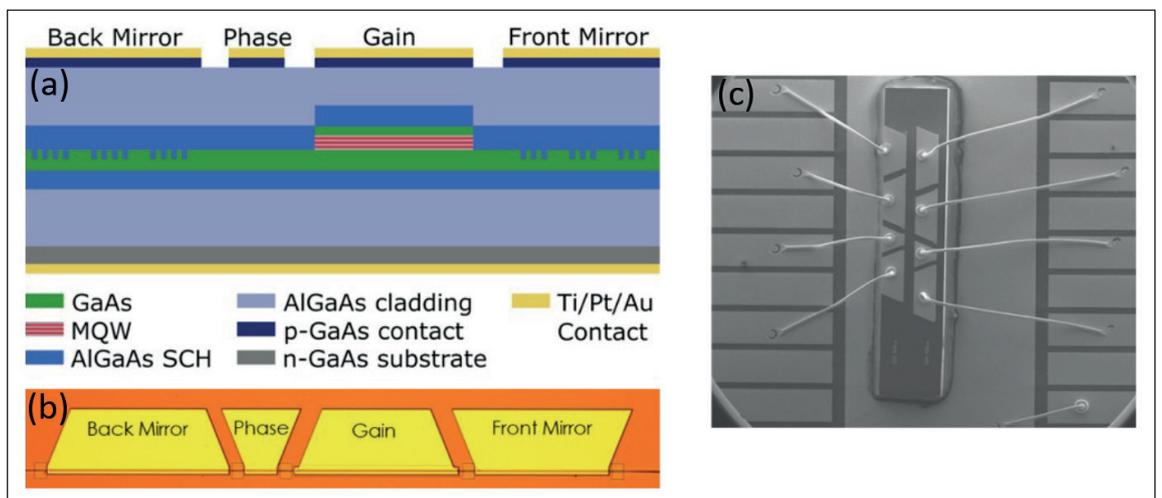


► Figure 4. (a) CO<sub>2</sub> reference cell absorption and the frequency-discriminating error signal used to stabilize the leader laser. The reference is a tube pressurized with CO<sub>2</sub>. (b) Beat-note between the leader laser and an external cavity laser with and without feedback to the leader laser phase section. (c) Beat-note between the leader and follower laser with and without an optical phase lock loop (OPLL) engaged. (d) Overlaid spectra measured from the leader and follower laser as the follower laser is tuned from 1-15 GHz offset. (e) Exemplary 1 μs pulse generated by sweeping the bias on the semiconductor optical amplifier from 0 mA to 100 mA. The pulse rise time is 262 ns and the fall time is 169 ns. (f) Measured absorption of a CO<sub>2</sub> test cell along with a Lorentzian fit. The full-width at half-maximum (FWHM) of the fit is 1.6 GHz.

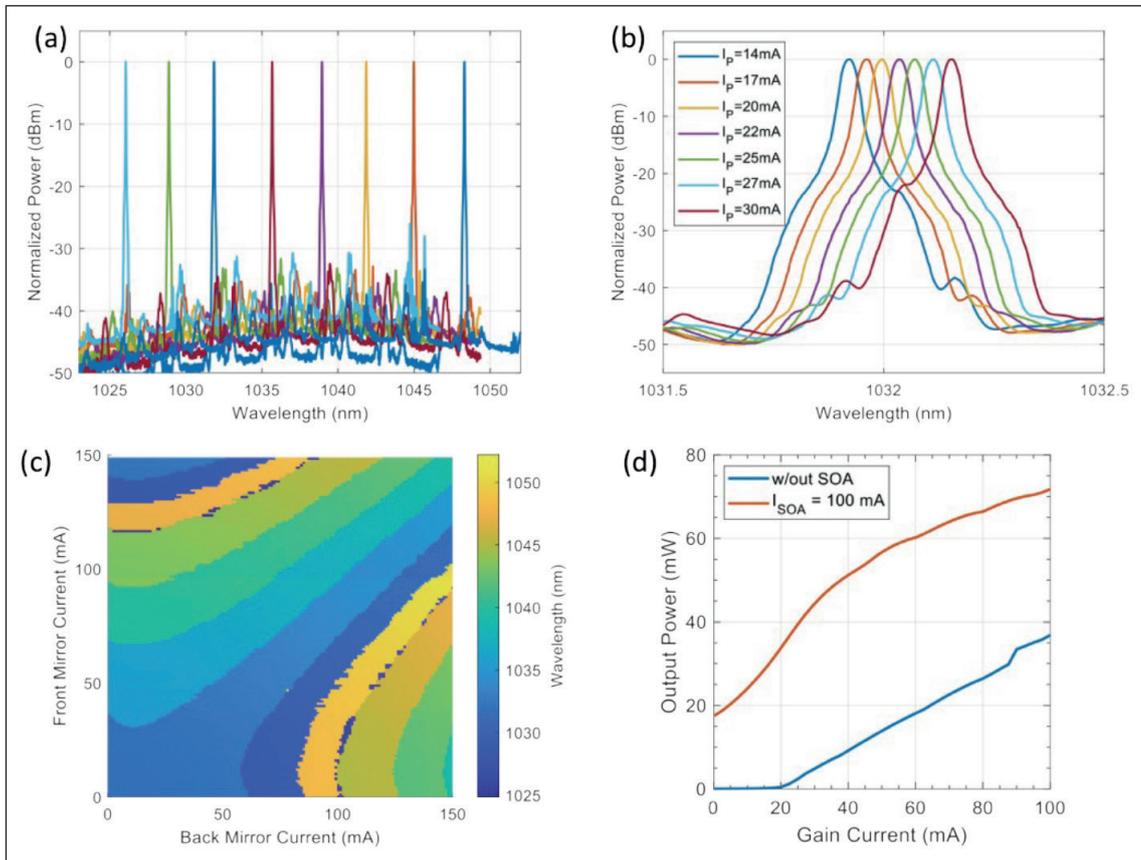
We have also investigated the capability of a semiconductor optical amplifier to increase the output power produced by the PIC (see Figure 6 (d)). For a conventional laser, without a semiconductor optical amplifier, output power is just above 35 mW at a drive current of 100 mA. For that drive current, when an equivalent laser is combined with a semiconductor optical amplifier biased at 100 mA,

total output power exceeds 75 mW (see the red curve in Figure 6 (d)).

Our two PIC platforms developed for space and airborne lidar – the InP PIC platform for active sensing of atmospheric CO<sub>2</sub> and the GaAs PIC platform for topographical lidar – highlight the promise of this technology for slashing the size,



► Figure 5. (a) Side-view schematic of GaAs-based widely tuneable laser, (b) top-view optical microscope image of a fabricated laser, and (c) top-view scanning electron microscopy image of mounted and wire-bonded laser chip.



► Figure 6. (a) Overlaid spectra illustrating a 22 nm tuning range, (b) fine wavelength tuning with phase section, (c) contour plot showing wavelength as a function of front and back mirror currents, and (d) power output as a function of current with and without amplification.

weight and power of systems serving these applications. Armed with these merits, these systems should see an increased frequency of deployment on small space platforms. To further this, in the near term we shall deliver hardware to our collaborators at NASA, so that they can perform their own sensing experiments in a laboratory setting. In conjunction, we will direct efforts at realising closer electronics integration, as this could lead to even lighter, smaller and more frugal systems. Beyond this, our plans include undertaking some space qualification, such as radiation testing, through

ongoing collaborations, and working with NASA to bring our technology to the next level of technology readiness – this is considered an ‘instrument programme’.

◉ The authors acknowledge funding support from NASA, technical contributions from Joseph Fridlander, Shannon Lee, Mark Stephen, Jeffrey Chen, Kenji Numata, Stephan Kawa, Fabrizio Gambini, Guangning Yang, Michael Krainak and Larry Coldren, and technical discussions with Parminder Ghuman and Amber Emory.

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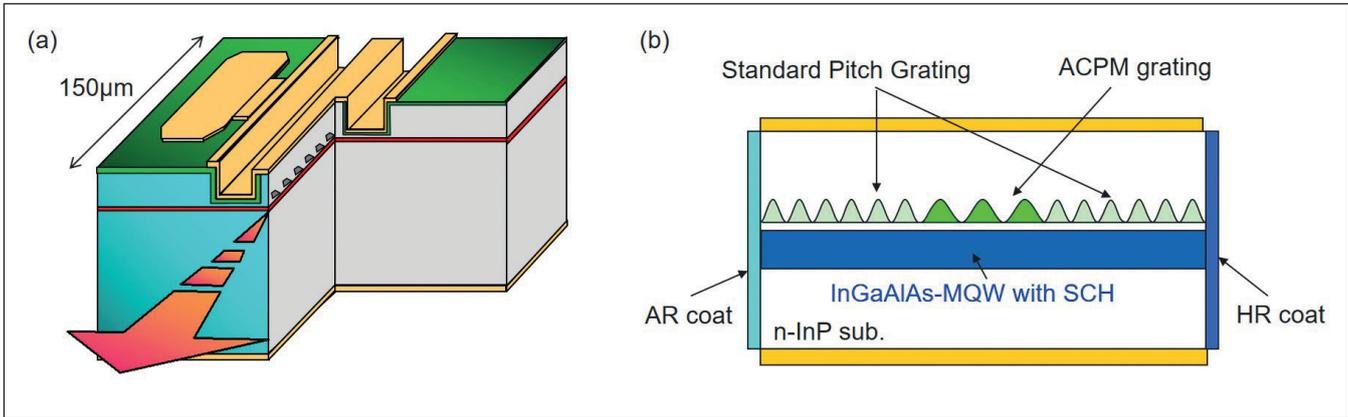
## Easing data-centre demands with directly modulated lasers

Simple InP lasers operating at 100 Gbit/s will provide a cost-effective solution to addressing the insatiable demand for more data

BY MASARU ONGA, TAKAYUKI NAKAJIMA, YUJI SEKINO, AKIRA NAKANISHI, NORIKO SASADA, RYOSUKE NAKAJIMA, HIRONORI SAKAMOTO AND KAZUHIKO NAOE FROM **LUMENTUM JAPAN**

To meet the continued explosion of network traffic there has to be an expansion in capacity. Part of the solution is to introduce new components. They must cost no more than their predecessors, to prevent the budget from spiralling out of control; and they must minimise power consumption to keep down running costs and restrict the carbon footprint of optical infrastructure.

A particularly significant proportion of global network capacity is associated with the data traffic in data centres and 5G wireless networks. In response to a recent increase in demand, over the last few years designers of data centres have moved on from deploying optical transceivers for 100GbE, which can for example be formed from four lasers running at 26 Gbit/s, to 400GbE, a data rate that may be realized with four 106 Gbit/s lasers. For these 106 Gbit/s sources, 53-GBaud four-level pulse amplitude modulation (PAM4) has been widely adopted, enabling a transmission speed of 106 Gbit/s. PAM4 is expected to be utilized in optical transceivers



➤ Figure 1. (a) The structure of a ridge-waveguide directly modulated laser. (b) Cross-sectional view.

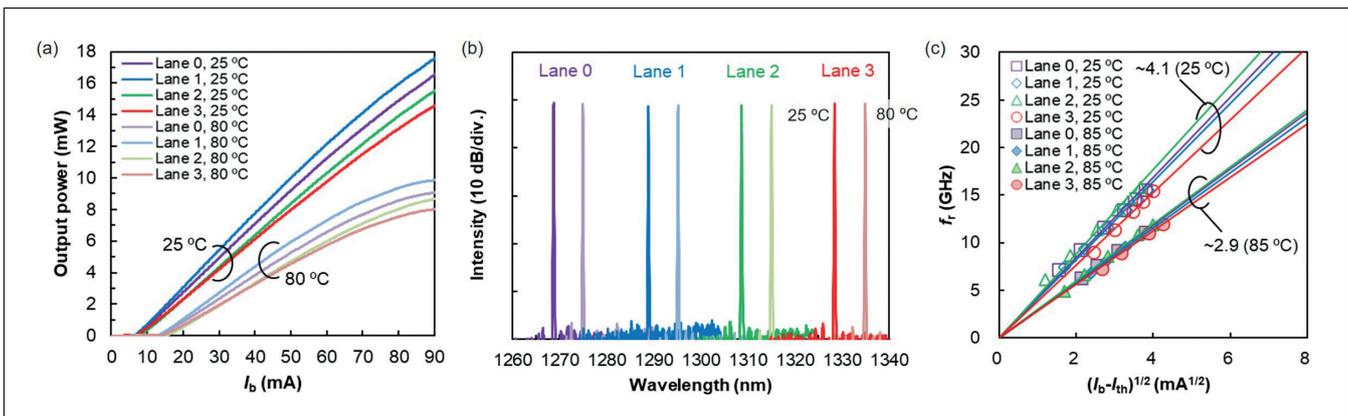
in data centres, for example, in 400GBASE-DR4 or 400GBASE-FR4 in 400GbE. In addition, 106 Gbit/s PAM4 technology is being considered for 800GbE short-reach applications, such as 800G-PSM8, formed from eight lasers operating at 106 Gbit/s.

One very promising candidate for providing 106 Gbit/s lasers in these multi-wavelength transceivers is the directly modulated distributed-feedback (DFB) laser. Compared with alternatives, such as the electro-absorption modulator integrated DFB laser, it has many advantages, including a simple structure, a low driving current, a small size and cost effectiveness. What's more, the directly modulated DFB laser is advantageous from a thermal management perspective. In the preceding 100GbE era, this class of laser operated without thermoelectric cooler control over a wide temperature range – and the anticipation is that at 400GbE and beyond, it will continue to operate in uncooled setups while drawing very little power. Also, developers of directly modulated lasers for this application must consider the lasing wavelengths that will be required. For example, for the coarse wavelength-division multiplexing (CWDM) range for 400 GbE, four sources must span 1271 nm to 1331 nm and each emit at wavelengths slightly offset from one another.

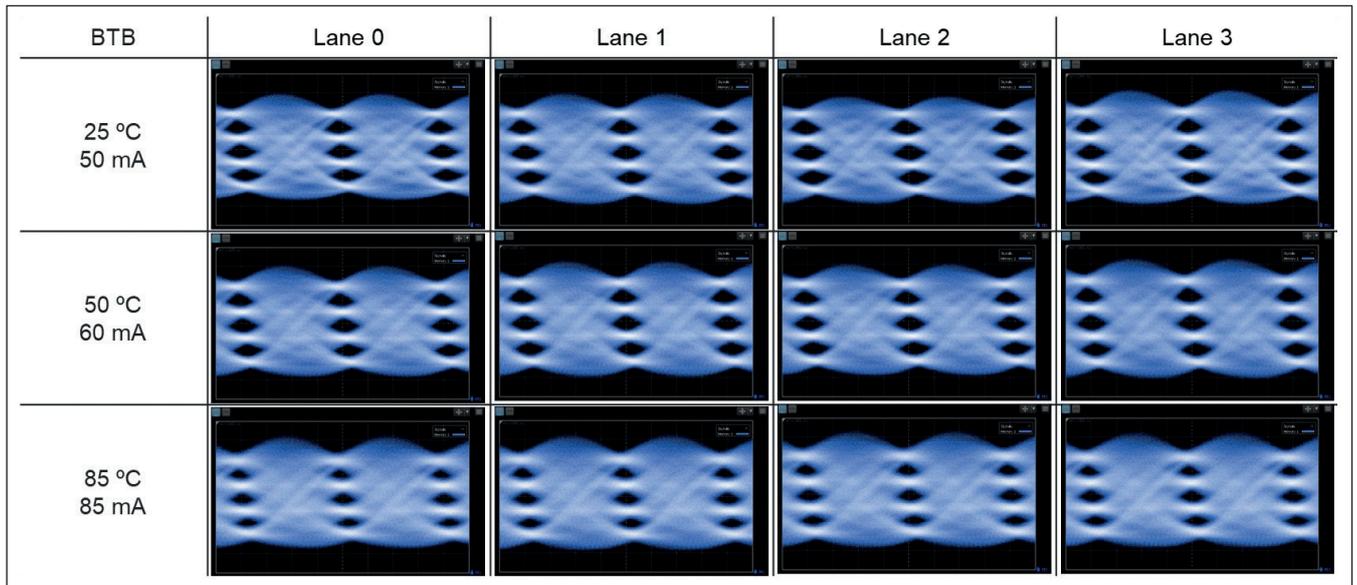
Options for these applications include a variety of directly modulated InP-based laser architectures. Candidates include the distributed-reflector laser with a buried heterostructure, and variants with a ridge-shaped buried heterostructure and a *p-n* blocking buried heterostructure. However, all these designs are held back by the use of some additional structures like a buried heterostructure – it requires additional epitaxial growth that adds complexity and cost.

Offering far more promise is the ridge-waveguide directly modulated laser. With the potential to provide a simple, easy-to-fabricate structures for uncooled 106 Gbit/s operation, it is an excellent candidate for ensuring high-volume production of cost-effective transceivers. However, success is not trivial, with innovation required to ensure an increase in bandwidth. Introducing external optical feedback can accomplish this, but it additionally requires external structures, so is not preferable.

Working with this restraint, our team from Lumentum, Japan, has developed ridge-waveguide directly modulated lasers operating at four different wavelengths within the CWDM range (see Figure 1(a)). To achieve a high bandwidth that



➤ Figure 2. (a) Light-current characteristics, (b) spectra and (c)  $f_r$  (relaxation oscillation frequency) -slope characteristics of four directly modulated lasers.



► Figure 3. 106 Gbit/s PAM4 optical eye-diagrams of the four directly modulated lasers at 25 °C, 50 °C and 85 °C with drive currents of 50 mA, 60 mA and 85 mA, respectively. 106 Gbit/s PAM4 eye diagrams were evaluated by using a Keysight M8045A pattern generator to produce an electrical signal with a short-stress pattern, random quaternary test pattern. The directly modulated lasers were modulated at up to 35 mA peak-to-peak with a single-ended signal inputted through an RF amplifier. DC bias ( $I_b$ ) was also applied via a bias tee just before an RF probe. Optical waveforms were detected by a Keysight N1092C sampling oscilloscope. The eye diagrams were measured with a 5-tap feed-forward equalizer in a back-to-back configuration. The outer extinction ratio, adjusted to 3.0 dB, was limited by a signal-voltage of the pattern generator output and the RF amplifier gain.

enables 106 Gbit/s operation, our lasers exhibit a high relaxation oscillation frequency, even at elevated temperatures, thanks to their high differential gain and high optical-confinement factor. Drawing on these strengths, our transmitters are capable of producing clear 106 Gbit/s PAM4 eye openings from 25 °C to 85 °C.

We have also evaluated the transmission capabilities and the bit-error rate characteristics of these sources, considering links of 500 m and 2 km. Strong results from these investigations showcase the great potential of our lasers for making cost-effective transceivers with low power consumption and high data-transmission rates.

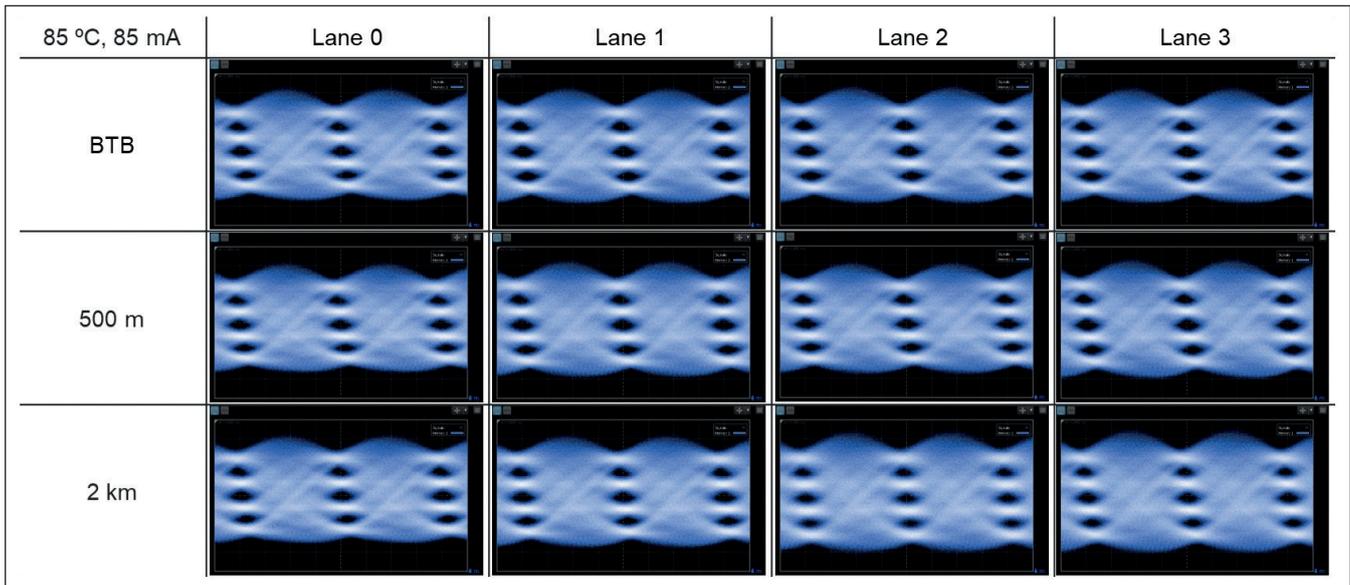
Our extensive measurements highlight the capability of our directly modulated lasers for serving in optical networks. These ridge-waveguide devices deliver 106 Gbit/s operation at up to 85 °C within the 1.3 μm CWDM range.

### Speedy designs

Our latest devices draw on our previous lasers, namely the development of ridge-waveguide directly modulated lasers operating at 25 Gbit/s and 50 Gbit/s. Using this foundation, we have developed lasers that: are capable of higher speeds; emit at four different wavelengths; and feature a high differential gain and a high optical confinement factor.

Semiconductor multilayers of our lasers were epitaxially grown on *n*-type InP substrates by MOCVD. To ensure high-temperature operation, the photoluminescence wavelength for each lane targeted optimal wavelength detuning. By optimising the band structure of the InGaAlAs multi-quantum-well layers and the zinc doping, we realised a high differential gain, even at high temperatures. Contributing to optical confinement were the multi-quantum-well layers and the separate-confinement heterostructure layers – working together, they increased interaction between the electron and photon systems.

We devoted much thought to the design of our ridge-waveguide lasers. For all four lanes we have employed a cavity length of 150 μm and normalized coupling coefficients of around 2.0. We suppressed longitudinal spatial hole-burning with an asymmetric corrugation-pitch modulated grating. The grating pitches for our four directly modulated lasers were set to 195 nm, 198 nm, 202 nm and 205 nm,



➤ Figure 4. 106 Gbit/s PAM4 eye-diagrams of the four directly modulated lasers in a back-to-back configuration and after 500 m and 2 km transmission at 85 °C and a drive current of 85 mA.

corresponding to the CWDM range, namely, 1271 nm (Lane 0), 1291 nm (Lane 1), 1311 nm (Lane 2) and 1331 nm (Lane 3). To complete device fabrication, we added a *p*-electrode pad on a buried organic insulator (this decreased parasitic capacitance and ultimately prevented high-frequency performance degradation); and we deposited anti-reflection and high-reflection coatings on the front and rear facets of our lasers.

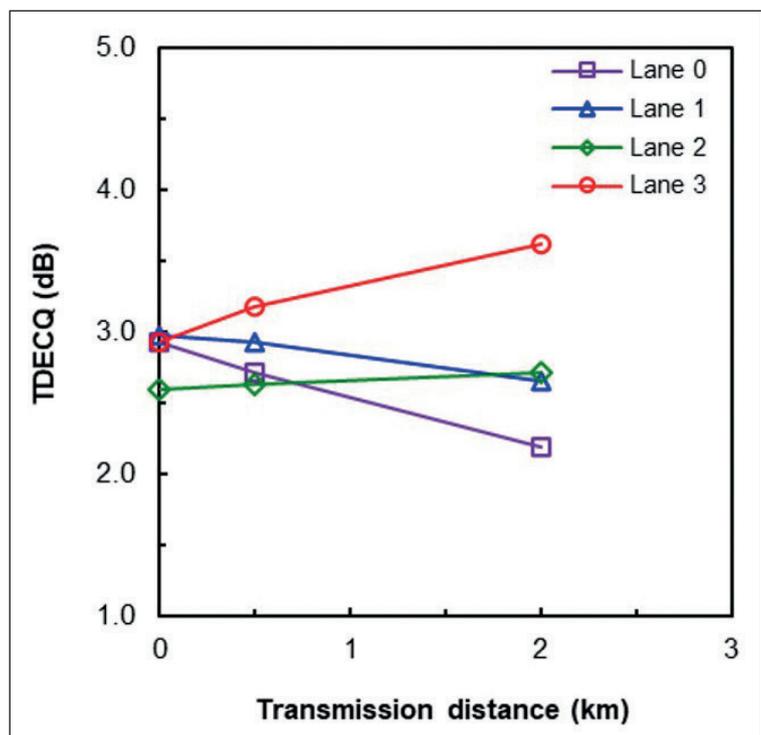
To evaluate our devices, we mounted four directly modulated laser chips on ceramic carriers with resistors that ensured 50 Ω impedance matching. We used this chip-on-carrier configuration, alongside a thermoelectric cooler that controlled the device temperature, to gain insights into all characteristics of our laser chips – including electro-optical responses, waveforms and bit-error rates.

Our plots of light output at a range of currents and temperatures (see Figure 2 (a)) showed that at 80 °C threshold currents range from 13.7 mA to 16.3 mA. When biased at 70 mA, our laser output exceeded 6.7 mW, a value sufficient for optical networks. Spectral measurements showed that all four lasing wavelengths were well separated into each lane. Driven at 50 mA at 25 °C, all four directly modulated lasers had a side-mode suppression ratio of over 45 dB, indicating stable single-mode lasing in spite of the high normalized coupling coefficients.

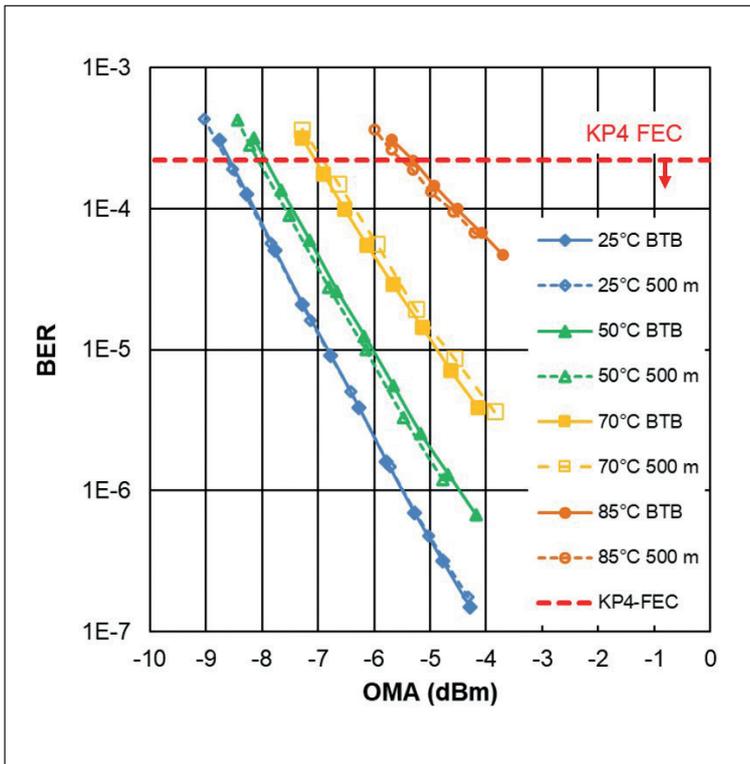
Measurements of the electro-optical response revealed values of the relaxation oscillation frequency between 3.8 and 4.4 at 25 °C, and 2.8 and 3.0 at 85 °C, indicating a high bandwidth for all four directly modulated lasers. Driven at 70 mA and operating at 85 °C, 3 dB bandwidths for all four lasers were 20.1 GHz.

### To 100 Gbit/s

Measurements on our lasers at device temperatures from 25 °C to 85 °C revealed eye openings over four levels using a back-to-back geometry (see Figure 3). In this configuration, measurements on the four directly modulated lasers produced values for a metric known as the Transmitter and Dispersion Eye Closure Quaternary (TDECQ) of 2.6 to 3.0 dB at



➤ Figure 5. Transmitter and Dispersion Eye Closure Quaternary versus transmission distance in four directly modulated lasers at 25 °C.



➤ Figure 6. Bit-error rate characteristics of Lane 2 in a back-to-back configuration and after 500 m of transmission at device temperatures of 25 °C, 50 °C, 70 °C and 85 °C. A gray-coded optical signal with a pseudo-random binary sequence (PRBS) 2<sup>31</sup>-1 pattern was received by a bit-error-rate tester consisting of a commercially available QSFP28 transceiver compatible with 100GBASE-FR1. An optical attenuator controlled optical power received at the transceiver.

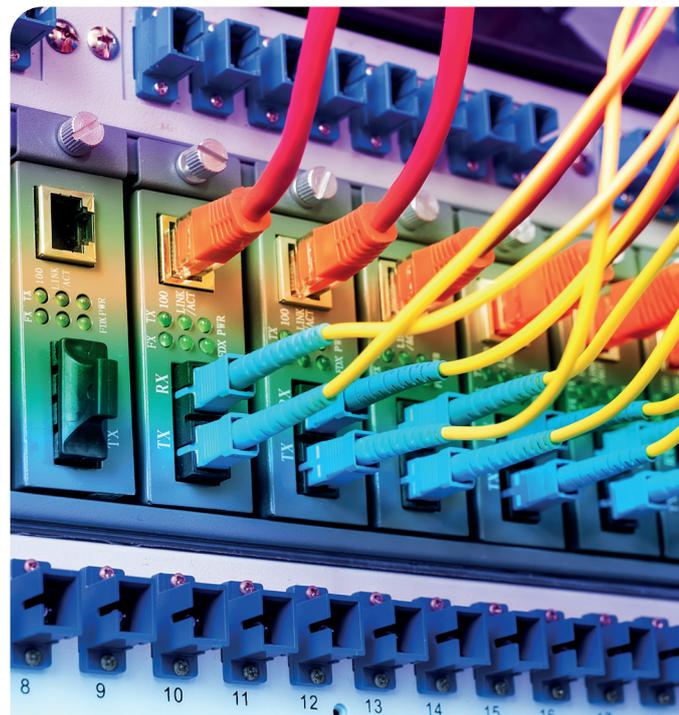
25°C, and 3.1 to 3.4 dB at 50 °C. These values satisfy the 400GBASE-FR4 specification of 3.4 dB.

Using single-mode fibre with zero dispersion wavelength at 1310 nm, we evaluated the transmission properties of our directly modulated lasers from 25 °C to 85 °C. We aimed to check the feasibility for the 400GBASE-DR4 specification for 500 m transmission, and 400GBASE-FR4 for 2 km transmission. Clear eye openings indicate successful transmission even at 85 °C (see Figure 4).

Note, though, that we found that chromatic dispersion can distort the eye diagram during transmission, especially in Lanes 0 and 3, which are far from the zero-dispersion wavelength of the single-mode fibre. So, to clarify the effect of chromatic dispersion, we plotted TDECQ values in a back-to-back configuration, and for transmission

over distances of both 500 m and 2 km at 25 °C. These measurements showed that TDECQ values for Lane 0 and 1 gradually decrease as waveforms are transmitted, due to negative dispersion; while those for Lane 2 and 3 slightly increased, owing to positive dispersion. These findings are consistent with the relationship between each lasing spectrum and the zero-dispersion wavelength of the single-mode fibres.

For both a back-to-back configuration and transmission through 500 m of fibre, we measured bit error rates at various values for the optical modulated amplitude for Lane 2, for laser temperatures of 25 °C, 50 °C, 70 °C and 85 °C (see Figure 6). Signals over optical modulation amplitudes of -3.5 dBm were not detected, due to losses related to fibre transmission and switching. While bit error rates increased with optical modulation amplitude as the temperature of the laser rose, it is still possible to realise excellent bit error rates that are below the threshold of KP4-FEC in 400GbE – that is, below  $2.2 \times 10^{-4}$  – at up to 85 °C. These characteristics for the bit error rate directly demonstrate the feasibility of our uncooled directly modulated lasers for 400GbE applications.



Our extensive measurements highlight the capability of our directly modulated lasers for serving in optical networks. These ridge-waveguide devices deliver 106 Gbit/s operation at up to 85 °C within the 1.3 μm CWDM range, with measurements of eye openings underscoring the capability for data delivery over several kilometres of fibre. Thanks to the simple design and fabrication process, allied to low power consumption and lack of need for cooling, our lasers are a very promising candidate for providing cost-effective transceivers for hyperscale data centres.

### FURTHER READING

- N. Sasada *et al.* *J. Lightwave Technol.* **37** 1686 (2019)
- T. Nakajima *et al.* *J. Lightwave Technol.* **40** 1815 (2022)

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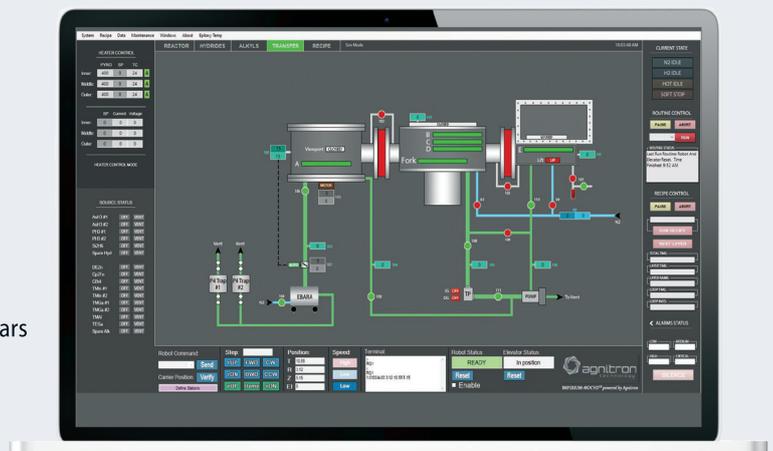


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# On the way to coherent VCSEL arrays

Replacing an oxide aperture with one based on the tunnel-junction allows a shift to a planar design that facilitates the fabrication of coherent arrays

BY ANTOINE PISSIS AND EVGENY ZIBIK FROM II-VI

DEPLOYED IN DATA CENTRES, computers, TVs and smartphones, the VCSEL is undoubtedly a great commercial success. Although it doesn't deliver the optical power and efficiency of its edge-emitting cousin, it has the upper hand in many other regards, combining lower fabrication costs with a far, far smaller footprint and surface emission, which simplifies testing and integration into more complex systems.

One of the key differences between the VCSEL and the edge-emitter is the approach that's taken to confine the light and ensure optical feedback, a prerequisite for stimulated emission. In a VCSEL, the mirrors above and below the cavity are formed from a stack of alternating layers of III-Vs that combine to create a distributed Bragg reflector (DBR). These mirrors have a very high reflectivity – it is typically around 99 percent – but they do not confine light in the lateral plane. So, to accomplish this feat in a GaAs-based VCSEL, which may emit at 850 nm

or 940 nm depending on whether it has GaAs or InGaAs quantum wells at its heart, an aluminium-rich layer is added and subsequently oxidised to form an electrically insulating layer. This oxidised layer, equipped with a lower refractive index, features a non-oxidised region in the middle that acts as an aperture, confining current and guiding light. With this architecture, VCSELs are able to combine efficiency with a low threshold current, attributes that ensure commercial success.

Despite all the engineering effort devoted to its development, the oxide aperture has its limitations. One of them arises from a variation in the oxidation depth across the wafer, which makes it challenging to guarantee good reproducibility of apertures when diameters are smaller than 4  $\mu\text{m}$ . A second limitation arises from having to oxidise a layer close to the active region. Due to this restriction, there is a need to etch the semiconductor through the top mirror and form a mesa around the aperture of the VCSEL, as this exposes the aluminium-rich layers to the oxidation process. A significant consequence of this pair of limitations is that it restricts the defining of an aperture of arbitrary shape, and in turn constrains the cavity geometry of the VCSEL.

Any loss of freedom when designing the cavity geometry is far from ideal. Why? Because the cavity geometry is the key design factor for selecting and promoting the resonating optical modes of the laser – and these modes govern its optical properties. Thus, if it were possible to find a way to control mode formation within the optical cavity of the VCSEL, this could extend the capabilities of this class of laser, and possibly enable it to serve new applications.

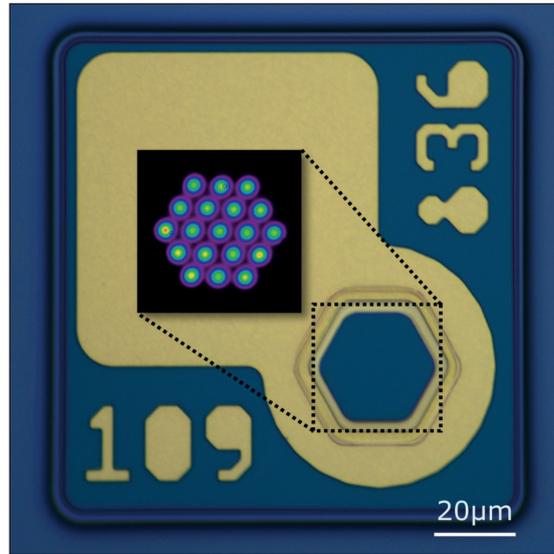
## Turning to tunnel junctions

At II-VI in Zurich we have tackled the issues associated with an oxide aperture by introducing a tunnel-junction lithographic aperture. This breakthrough allows us to switch to a planar design that avoids



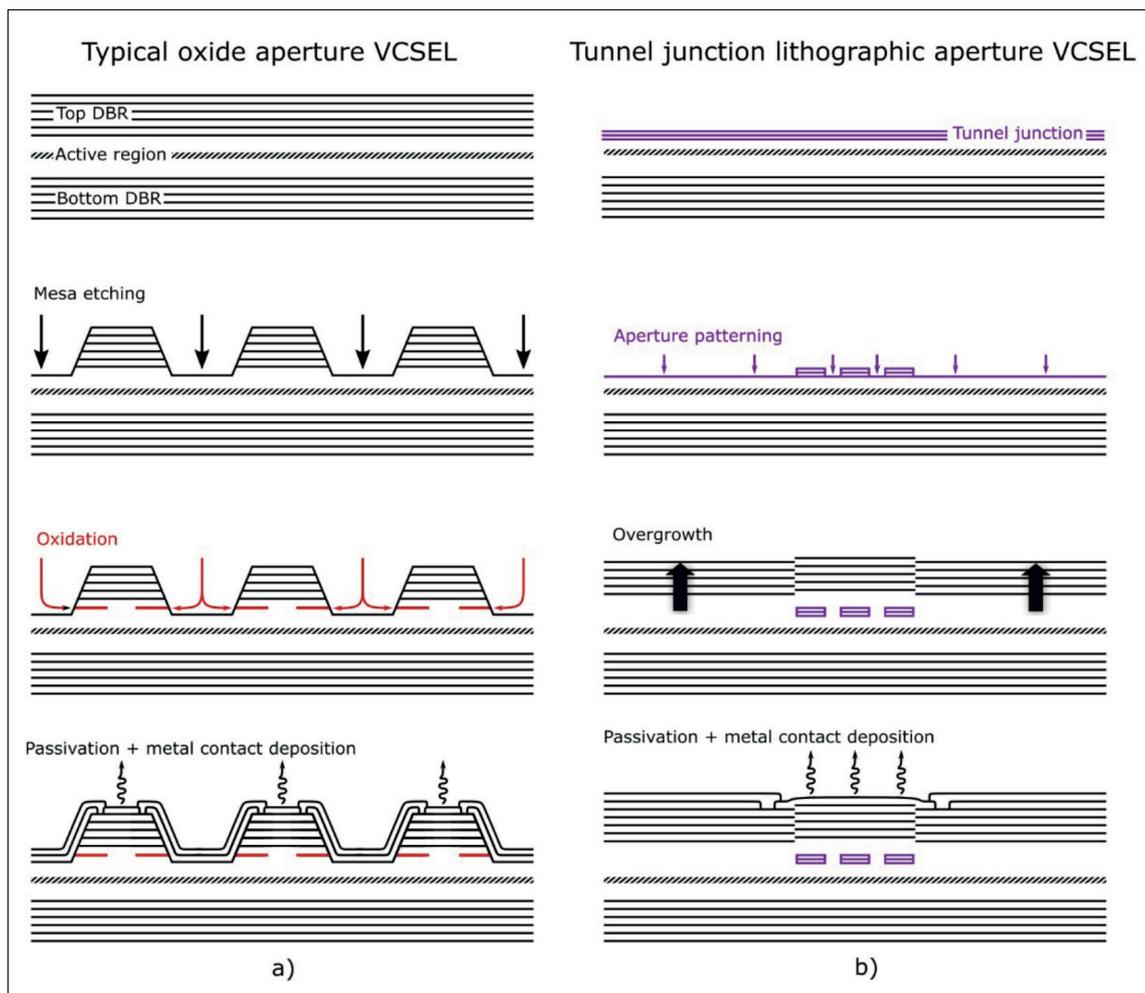
the limitations of a mesa-based geometry. Using this architecture, we can produce VCSEL arrays, such as that with 19 elements shown in Figure 1 (due to the planar design, the 19-element array structure is not visible). Thanks to this planar design we enjoy greater flexibility, resolution, and reproducibility of all VCSEL cavities, because they are defined by lithography rather than the standard oxidation process. What's more, our planar structure improves heat dissipation and guarantees excellent device reliability.

When manufacturers produce 940 nm VCSELs with an oxide aperture, fabrication tends to involve two steps (see Figure 2 (a)). The first is to take an *n*-doped GaAs substrate, load it into an MOCVD or MBE reactor, and deposit the VCSEL heterostructure that consists of an *n*-doped bottom DBR, a low-doped laser cavity that includes the active region, and a *p*-doped top DBR. After this step, the VCSEL emitter is still to be defined. To accomplish this – the second step in VCSEL fabrication – the epitaxial structure must be etched and oxidised to form the aperture of this emitter. Once this is done, the VCSEL emitter is passivated to protect it from further oxidation, and metal contacts are deposited.



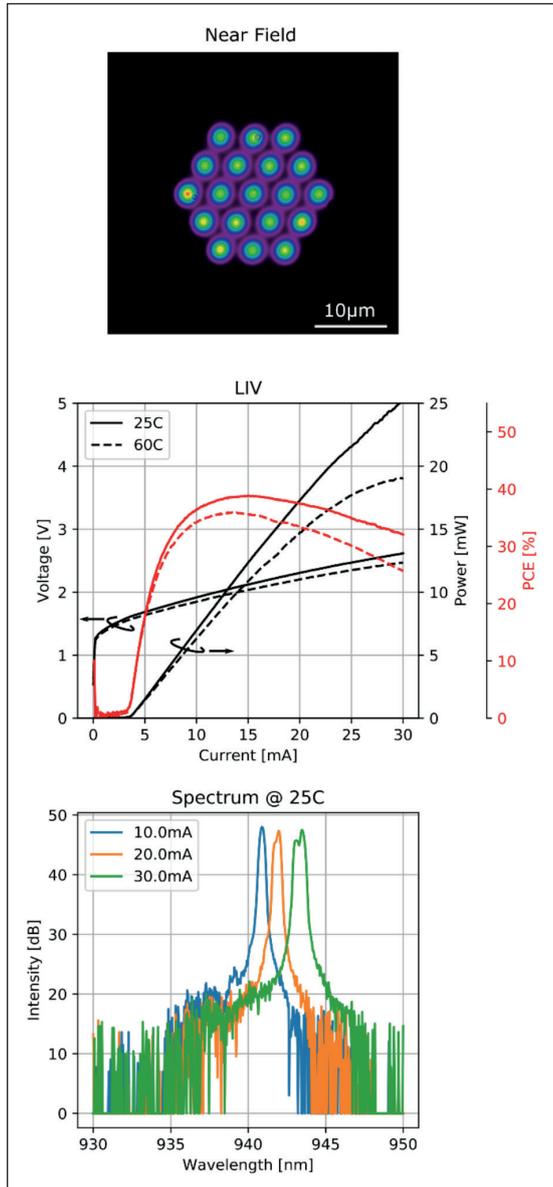
► Figure 1. Optical microscopy image of a 19-emitter VCSEL array defined by a tunnel-junction lithographic aperture. A near-field image is presented in the inset.

We adopt a markedly different process flow when forming our tunnel-junction lithographic aperture VCSELs (an overview of this approach is provided in Figure 2 (b)). Rather than using a single growth process, we form our epitaxial structure in two sub-



► Figure 2. A comparison of the fabrication process flow for a standard oxide aperture and a tunnel-junction lithographic aperture VCSEL array. For the same aperture size and number of emitters, the tunnel-junction lithographic aperture process allows an arrangement that is more compact.

► Figure 3. Electro-optical characteristics in CW operation, for a 19-emitter VCSEL array defined by a tunnel-junction lithographic aperture.



growth steps, separated by an aperture processing step. Fabrication begins by growing the bottom structure, consisting of an *n*-type bottom DBR and a partial laser cavity containing the active region. Terminating this bottom structure are highly doped *p*<sup>++</sup> and *n*<sup>++</sup> layers, which form a tunnel junction. Applying a direct bias to the laser leads to a reverse bias of the tunnel junction, allowing electrons and holes to tunnel through it.

With our VCSELS, optical lithography defines the area where current flows. Our etching step removes much of the tunnel-junction layers, leaving just the area that is to become the VCSEL aperture. The processed wafer that results from this localised etching is sent back to the growth reactor, where a top growth completes the epitaxial structure, adding an *n*-type DBR and an *n*-contact layer.

During the second growth, we fully define our VCSEL cavity in the vertical and lateral directions.

Two of the consequences of the shallow post, formed by etching that creates a tunnel junction that is only present in the aperture area, are a local increase in the cavity optical thickness and a cavity resonance shift. This shift, equivalent to an effective refractive step, confines light laterally and restricts the VCSEL cavity in the plane of the wafer.

Another merit of our design is that by growing an *n*-type region over a *p*-type region outside the aperture, where the tunnel junction is etched away, we create an interface that acts as a *p-n* diode biased in the reverse direction. This provides a local blocking of current flow, thereby ensuring that current can only flow through the area containing the tunnel junction. Thanks to this design, current is laterally confined by the lithographically-defined aperture.

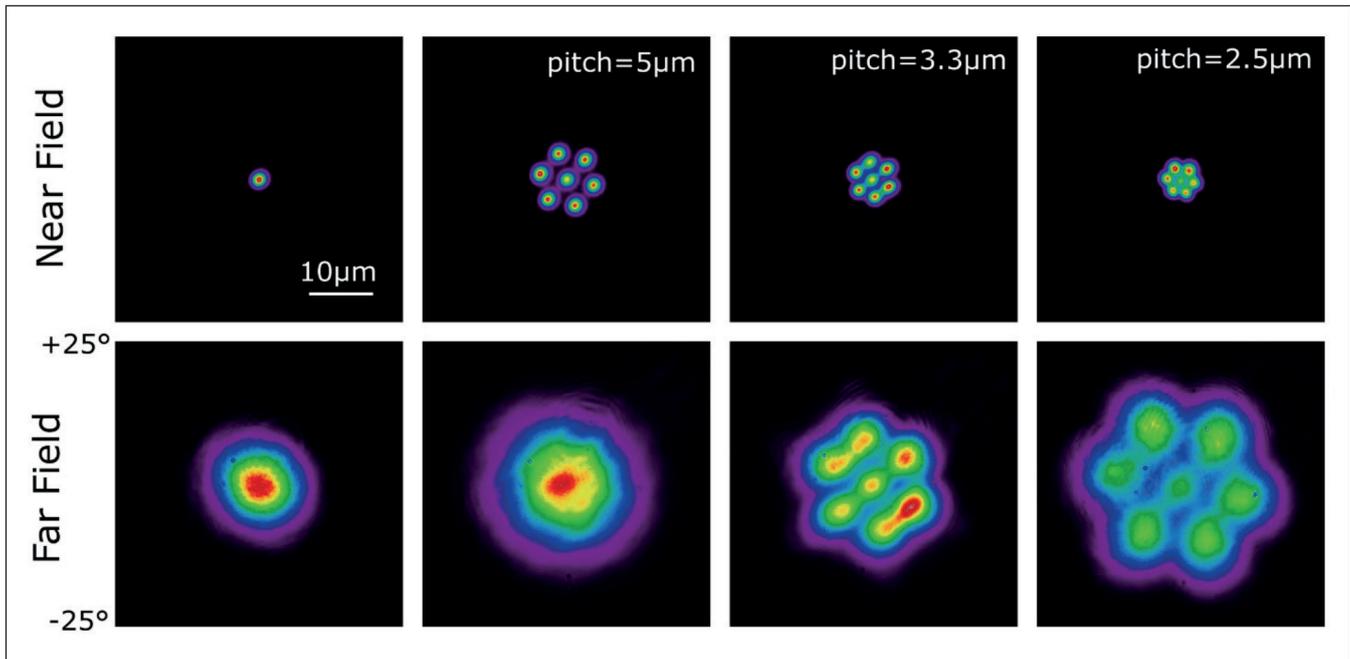
To complete our VCSEL fabrication process, we protect the surface with a passivation layer, prior to depositing ohmic metal contacts. Note that our process does not require any oxidation, unlike that for producing VCSELS with oxide apertures.

For VCSELS with an oxide aperture, it is the mesa lithography and the oxidation depth that define the aperture's shape and dimension. With this process, the aperture is defined by the mesa border shape that is transferred toward the mesa centre via oxidation. With our VCSELS it is a very different state of affairs: the dimensions of the aperture are determined by the tunnel-junction's area, which is defined by lithography. This enhances the control of the aperture shape.

We have used our approach to successfully fabricated VCSELS that have a 2 µm-diameter emitter. Our process provides good reproducibility over the entire wafer. In comparison, even with careful monitoring of the mesa oxidation depth, it is challenging to realise such reproducibility with an oxide aperture. Variations arise from local non-uniformity of the aluminium content in the oxidation layer – this influences the oxidation rate.

Our mesa-free, fully planar structure offers the possibility of fabricating dense arrays of VCSEL emitters, such as the array of 19 emitters shown in Figure 1 (in that array, VCSELS have 2 µm-diameter apertures and are arranged on a hexagonal lattice with a 5 µm pitch). One of the attributes of this array is that its footprint is smaller than that of the single mesa of an oxide aperture VCSEL emitter.

Measurements of this compact array reveal that it produces more than 25 mW of optical power at 25 °C, and has a power-conversion efficiency in excess of 30 percent at drive currents up to 30 mA. Near-field images show uniform current injection to all emitters within the array, thanks to the excellent conductivity of the *n*-doped top DBR and the tunnel junction. One consequence of such a small aperture size is that each emitter operates in single mode, resulting in a single spectral peak for the array.



► Figure 4. Near-field and far-field images of a single-emitter VCSEL and a 7-emitter VCSEL array defined by a tunnel junction lithographic aperture. The multi-lobe far-field pattern observed when decreasing the array pitch indicates that the array is coherent.

## Coherent control

An additional advantage of our mesa-free structure is that it opens up the possibility to exchange light between neighbouring emitters. For this to happen, the emitters need to be close enough to each other to enable evanescent coupling. When this occurs, the phase of light that's emitted is locked, creating a coherent array, with all emitters acting as a single laser.

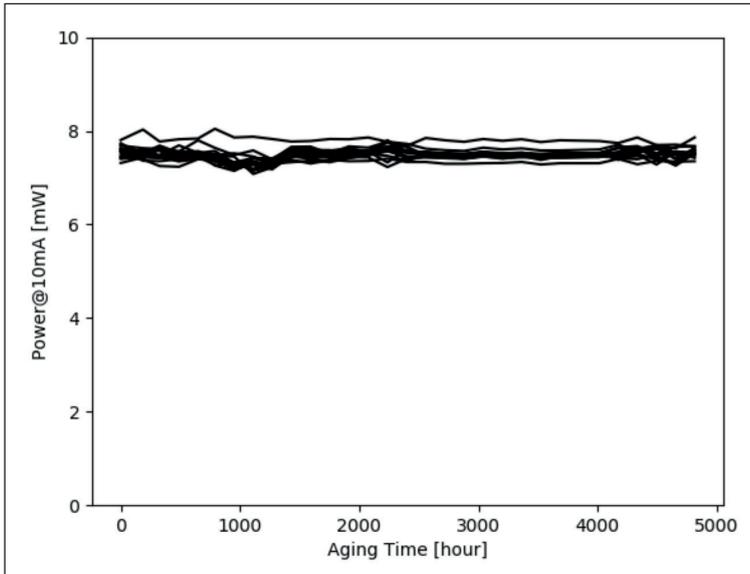
With our lithographic aperture technology, we can control both the emitter diameter and the spacing between emitters to an accuracy that is less than 100 nm, and is limited only by the lithography tool resolution. In comparison, in standard VCSEL arrays with oxide apertures, the presence of the mesa trenches prevents coherence, which holds the key to enhanced characteristics and high brightness.

One of the characteristics for coherent arrays is interference in the far field. We have observed this with our arrays formed from VCSELS with the tunnel-junction lithographic aperture (see Figure 4). By modifying the spacing between our emitters, we have adjusted their coupling strength. When we bring them closer together, this leads to more

pronounced interference patterns. Using a 5 µm pitch between the emitters, which are 2 µm in diameter, we obtain a far-field pattern that is similar to that from a single-emitter. When we reduce this pitch to 3.3 µm or 2.5 µm phase-locking results, with the source operating as a coherent emitter array with distinct narrow far-field lobes. By controlling the optical phase shift between emitters, we alter the far-field pattern on demand. As one would expect, increasing the number of emitters increases the output power: operating at room temperature, we have realised more than 10 mW of optical power from a coherent array of 7 emitters; and in excess of 17 mW from a coherent array with 19 emitters.

Our tunnel-junction lithographic aperture VCSELS have an electro-optical performance that is competitive to that of their oxide-aperture counterparts. Those with a tunnel junction have a threshold current density that's around just 2 kA cm<sup>-2</sup>; and with an optimal emitter diameter, power conversion efficiency can hit 45 percent. Such a high efficiency stems from a knee voltage of just 1.4 V, and a differential resistance of around just 100 Ω for the epitaxial structure and 8 µm emitter diameter. This strong performance in

By modifying the spacing between our emitters, we have adjusted their coupling strength. When we bring them closer together, this leads to more pronounced interference patterns



► Figure 5. Reliability performance of a 6 μm-diameter, single-emitter tunnel-junction lithographic VCSEL stressed under 25 kA cm<sup>-2</sup> at 125 °C. No output optical power degradation has been observed up to 5,000 hours of aging.

key VCSEL characteristics demonstrates that the introduction of the tunnel junction does not induce any penalty on the performance of this class of laser. Crucially, in addition to enhanced cavity geometry control and strong performance, the tunnel junction promises excellent reliability. Our tests conducted on a 6 μm-diameter single-emitter defined by a tunnel-junction lithographic aperture uncover no sign of degradation up to 5,000 hours of aging, using a current density of 25 kA cm<sup>-2</sup> and an operating temperature of 125 °C (see Figure 5).

We attribute this remarkable reliability to multiple factors. With our buried tunnel-junction VCSEL, the structure is stress free, thanks to the absence of lattice constant mismatch; that not the case for VCSELs with an oxide aperture, because this form of aperture introduces stress close to the active region, which can be responsible for degradation. Another advantage of our planar structure is that it improves heat removal. This reduces the thermal impedance of the device and limits its degradation, even in harsh operating conditions.

With the tunnel junction lithographic aperture, we propose an innovative technology platform, which could expand the functionality of VCSELs and open new markets and applications. Future development will continue to understand phase coupling between emitters within an array and may lead to a new class of product with beam properties that can be designed on demand.

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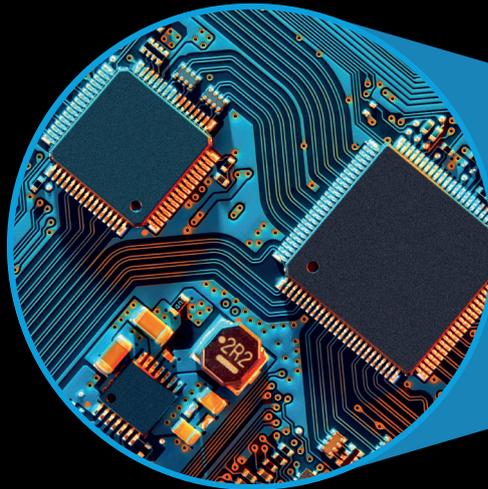


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## NiO equips $\text{Ga}_2\text{O}_3$ with bipolar conduction

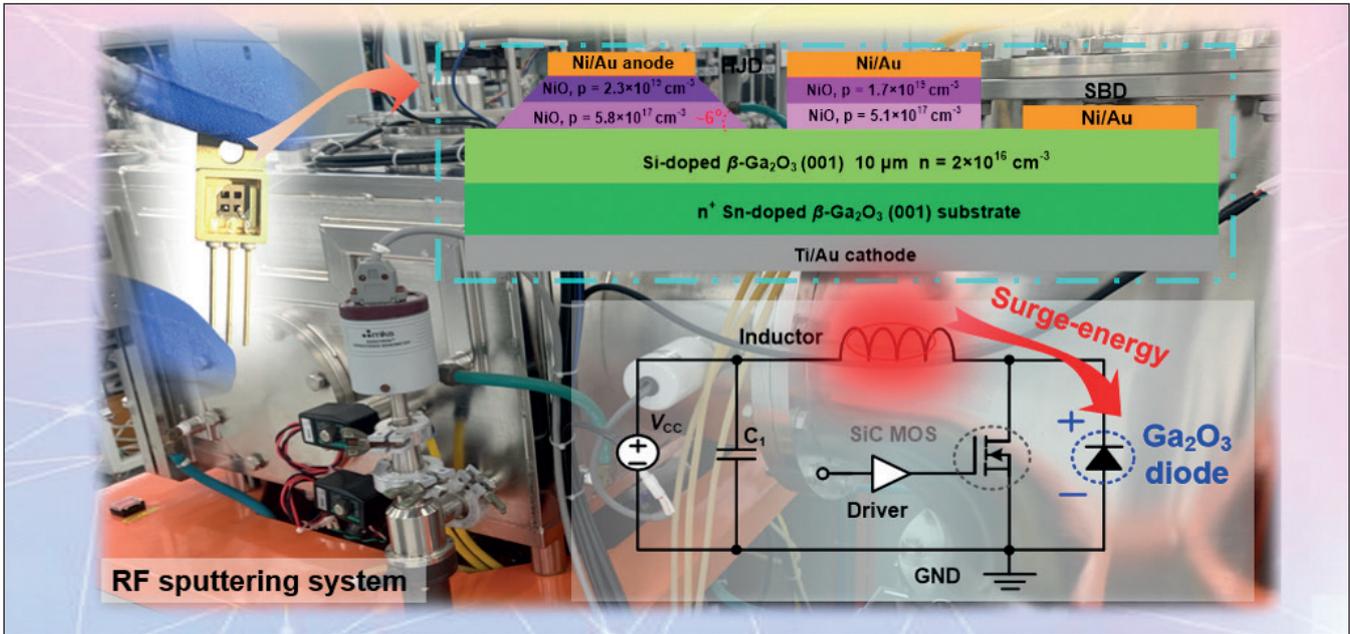
Diodes formed from *p*-type NiO and *n*-type  $\beta\text{-Ga}_2\text{O}_3$  embrace the harsh transients found in power electronic systems

BY JIANDONG YE, HAI LU AND RONG ZHANG FROM [NANJING UNIVERSITY](#)

THERE'S NO DOUBT that power electronic circuits are playing an ever-increasing role in our lives. They are key building blocks in big-data centres, electric vehicles, cloud computing and the internet of things. We have a diverse network of power electronic equipment to thank for keeping us immersed in the pleasure of technology at all times. To provide this level of service, circuits must operate for a long time without failure and handle unavoidable high-voltage/current transients.

These transients – momentary spikes in voltage or current – tend to be accompanied with lightning,

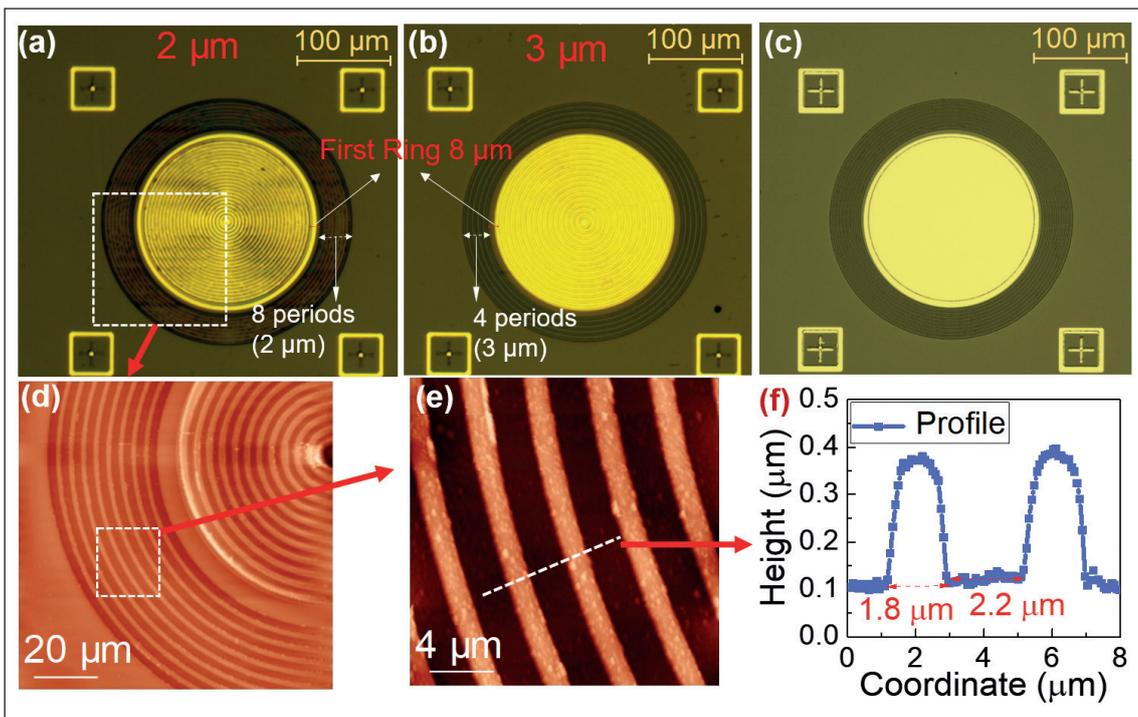
electrostatic discharge. When power circuits experience such a sudden change in the switching process caused by transients, this threatens to disrupt or damage power devices connected to signal or power lines (see Figure 1). Such transients can deteriorate power systems, because power electronic devices have to operate under critical conditions of high voltages and large currents. Consequently, there is tremendous desire to increase the robustness of power devices against transients, as this will ensure the availability of essential building blocks for power modules providing safe operation.



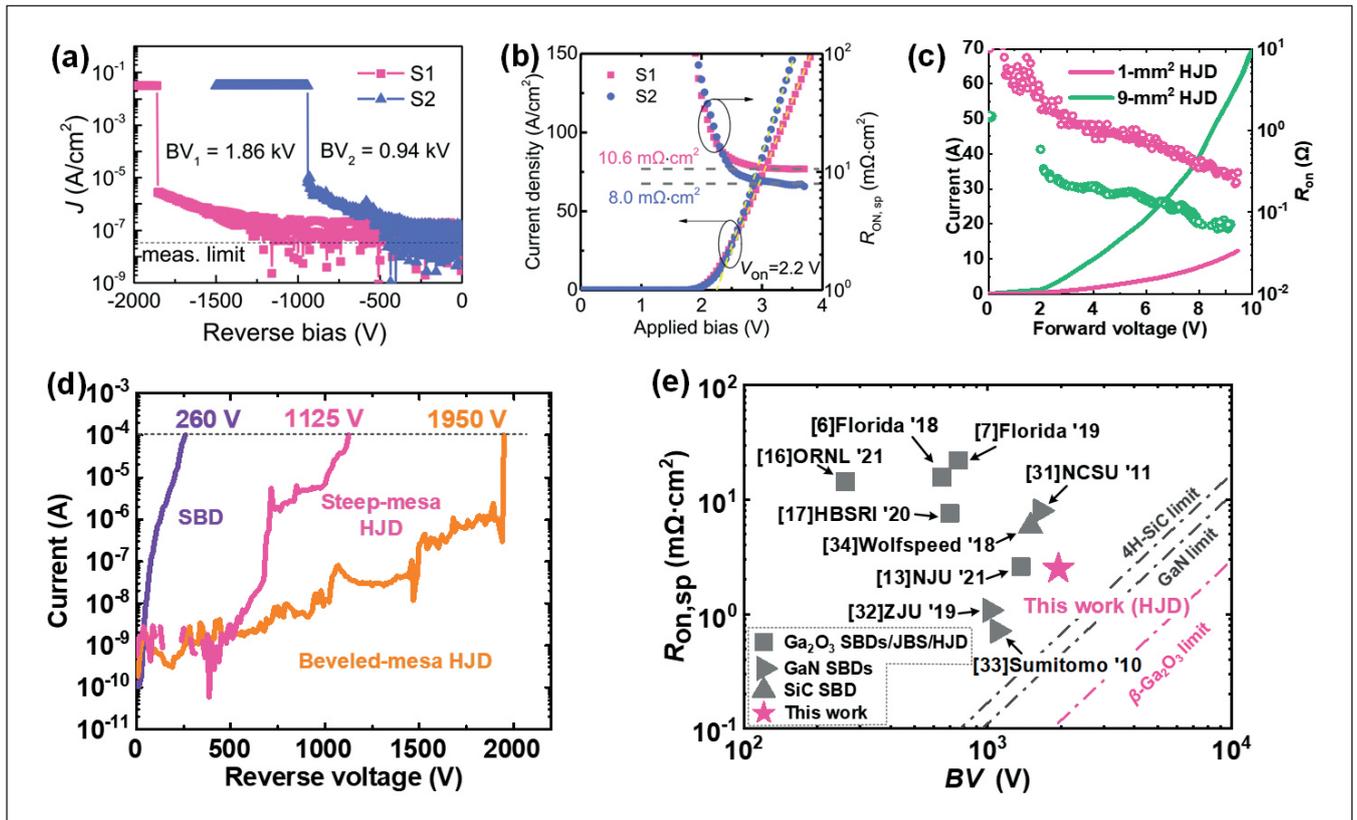
➤ Figure 1. The NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power rectifiers, with different bevel angles adjusted by a magnetron sputtering system. Inset: schematic cross-section of NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes and a Ni/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diode. The transient energy shocks that degrade device performance stem from the lumped or parasitic elements in the power circuit.

One option for ushering in an era of high-reliability power circuits is to replace silicon devices with those made from wide-bandgap semiconductors, which are well-suited to delivering high-temperature, high-power operation. Amongst these wide bandgap semiconductors,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has many

attributes: an ultra-wide bandgap, an ultra-high breakdown electric field, and a decent electron mobility. These virtues make this oxide a very competitive candidate for high-power applications. Furthermore,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is renowned for its high thermal stability, ensuring high-temperature



➤ Figure 2. Top-view microscopy image of the heterojunction barrier Schottky diodes with *p*-NiO ring width/spacing of (a) 2  $\mu$ m and (b) 3  $\mu$ m. (c) NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes with a uniform field limiting rings (FLRs) with a width/spacing of 2  $\mu$ m. (d) and (e) Atomic force microscopic images of (a). (f) Height profile of *p*-NiO rings extracted from (e).



► Figure 3. (a) Comparison of breakdown characteristics for double-layer NiO films (S1) and single-layer NiO films (S2). (b) Forward current-voltage characteristics of devices S1 and S2. (c) Pulsed current-voltage (*I*-*V*) characteristics and corresponding on-resistance ( $R_{on}$ ) of the 1 mm<sup>2</sup>/ 3 mm<sup>2</sup> heterojunction diodes (HJDs). (d) Reverse *I*-*V* characteristics. (e)  $R_{on}$  versus blocking voltage (*BV*) benchmarks of the bevelled-mesa HJDs against the 1 mm<sup>2</sup> Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes (SBDs)/junction barrier Schottky diodes (JBS)/ HJDs, GaN SBDs, and commercial SiC SBD.

operation; and for its short minority carrier lifetime, enabling fast switching with low power losses.

Unfortunately, the potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is yet to be unleashed. The biggest sticking point is the absence of *p*-type conduction, which obstructs the design of bipolar power devices. Due to this, the majority of reported  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power rectifiers detail the design and capability of regularly unipolar Schottky barrier diodes. With these devices, it is very hard to realise high-voltage ratings and high-power levels, due to the limited barrier height. What’s more, this form of diode is particularly susceptible to self-heating at high current levels. So today, despite much effort, unipolar Schottky barrier diodes are restricted to serving in the terminal designed domain, primarily because this accommodates premature breakdown and transient overvoltage instabilities.

A solution to breaking this deadlock is to introduce power rectifiers with bipolar conduction – this will banish the trade-off between the reverse blocking capability and the forward current output. Implementing *p*-*n* bipolar structures in power devices will open the door to simple device fabrication processes and enhanced reserve-blocking voltages, while delivering extremely high current densities with reduced on-state resistances.

Merits of such a strategy include a large safe-operation-area under both a forward surge-current and reverse transient-energy spikes, as well as the potential for fast switching.

Aiming to make this happen is our team led by Rong Zhang from Nanjing University. We kickstarted our efforts at constructing  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> *p*-*n* bipolar devices by carefully considering several foreign *p*-type semiconducting oxide materials that promised to overcome the technological bottleneck of *p*-type  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Piquing our interest during the search through the *p*-type transition metal oxide family came NiO. It is an attractive, well known transparent hole-transport layer in solar cells and photodetectors, thanks to its decent hole conductivity and its desirable transparency that stretches from the ultraviolet to the near infrared. It is believed that the origin of this oxide’s high hole concentration is the formation of Ni<sup>3+</sup> from Ni<sup>2+</sup> nearby nickel vacancies, coming from the reaction with excess oxygen atoms. This chain of events creates holes that are localized on the nickel sites and offer the acceptable mobility.

Thanks to this great set of attributes, NiO is our material-of-choice for constructing *p*-*n* heterojunctions with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Back in 2020, we

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► Figure 4. The team led by Hai Lu at Nanjing University has developed a high-speed, high-reliability dynamic test system to characterize the dynamic performance of power devices based on wide-bandgap semiconductors.

reported the first demonstration of a double-layered  $p$ -NiO/ $n$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction power rectifier, which had a breakdown voltage of up to 1.86 kV. Since then we have devoted much effort to building on this triumph, and advancing  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> based bipolar power devices. Recent successes include: an enhanced reverse blocking capability; high forward current outputs, together with nanosecond reverse recovery; a high power-conversion efficiency; and more than a million-time overvoltage surge-current ruggedness.

### Building heterojunctions

Using our in-house advanced material growth and microfabrication facilities, we have produced a portfolio of NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> vertical heterojunction diodes on the conductive, tin-doped (001)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate. To make these devices, we developed room-temperature, selective-area growth of

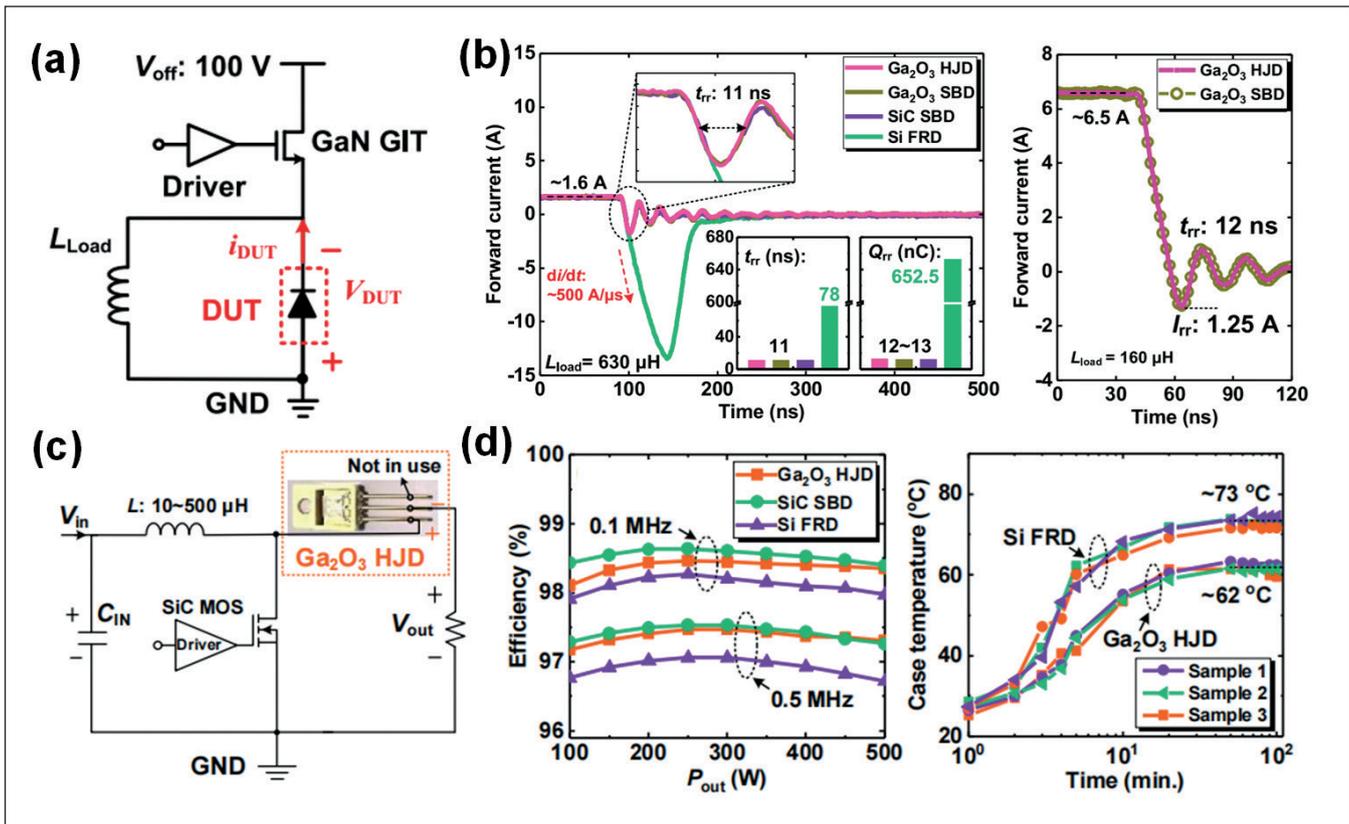
NiO. Using radio frequency (RF) magnetron sputtering, a technique used in industry, and have heteroepitaxially grown high-quality, single-crystalline NiO thin films on  $c$ -plane sapphire, ZnO and GaN substrates. We have found that the crystalline quality of NiO is sensitive to the exposed strain and to the in-plane crystallographic symmetry of the substrates. For instance, NiO epilayers have high-quality single crystallinity on (-201)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates, but exhibit polycrystalline features on the (001)-oriented  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. There is also a concern that the sputtering process could introduce plasma damage to the NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface.

To maximize the advantages of NiO technology in device fabrication, those within our team that are led by Jiandong Ye have developed relatively mild sputtering conditions for the growth of this oxide, and equipment that allows small adjustments to the deposition angle. Efforts have also been directed at developing optimized thermal treatment to improve the interface quality of NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterostructures. Introducing these well-developed processing recipes has enabled us to fabricate high-performance NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes with a low interfacial state density.

Another tremendous advantage of our sputtering technique, which stems from its adjustability and flexibility, is that it is possible to naturally form devices with a bevelled mesa termination structure – this avoids any dry etching damage, and results in an architecture that greatly suppresses the peak electric field. The use of this non-invasive formation of termination, rather than dry etching, has previously been employed to realize heterojunctions with other  $n$ -type wide bandgap semiconductors, such as those in the AlGaIn/GaN system, where much effort has focused on developing normally-off transistors. By turning to sputtering, we are using a film growth technique that offers compatibility between our Ga<sub>2</sub>O<sub>3</sub>-based power devices and the mature CMOS platforms.

Drawing on our readily available NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub>  $p$ - $n$  heterojunction, it has been relatively easy for us to pursue several strategies for electric field engineering. We have fabricated a series of high-performance power devices, including  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction barrier Schottky diodes,

To make these devices, we developed room-temperature, selective-area growth of NiO. Using radio frequency magnetron sputtering, a technique used in industry, we have heteroepitaxially grown high-quality, single-crystalline NiO thin films on  $c$ -plane sapphire, ZnO and GaN substrates



► Figure 5. (a) Schematic of the double-pulse test circuit. The fast-speed commercial GaN gate-injection transistor has been used as a control switch. (b) Reverse recovery characteristics of different diodes. (c) The power-factor-correction (PFC) circuit with the packaged Ga<sub>2</sub>O<sub>3</sub> heterojunction diode. (d) System efficiency versus output power ( $P_{out}$ ) of a 500-W PFC circuit at switching frequencies of 0.1 MHz and 0.5 MHz and the extracted case temperature of the three test samples at 0.3 MHz/500 W.

heterojunction FETs, reduced-surface-field MOSFETs and the first  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>-based lateral superjunction MOSFETs. With the heterojunction barrier Schottky diode, where the NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub>  $p$ - $n$  heterojunction serves as field plates and field limiting rings, we can freely modulate the electrical parameters of this power rectifier that combines a low on-state conduction loss with a superior reverse-blocking capability (see Figure 2).

### Intriguing electrostatic performances

Electrical measurements on a range of our power rectifiers reveal the impact of the hole concentration in  $p$ -NiO on the voltage blocking capability. When we reduced the hole concentration from  $3.6 \times 10^{19}$  cm<sup>-3</sup> to  $5.1 \times 10^{17}$  cm<sup>-3</sup>, this lifted the breakdown voltage from 0.94 kV to 1.86 kV (see Figure 3 (a)). Unfortunately, the far lighter doping had unwanted consequences, increasing the differential specific on-resistance of the NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction diode and exacerbating on-state power loss. Due to this, we have to limit the forward current output for this device to 150 A/cm<sup>2</sup> (see Figure 3 (b)).

By employing more elaborated techniques and expanding device dimensions, we have realised

high current outputs. To this end, we have fabricated large-scaled NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub>  $p$ - $n$  heterojunction diodes with sizes of 1 mm<sup>2</sup> and 9 mm<sup>2</sup>. These power rectifiers deliver forward currents of over 12 A and 70 A for the smaller and larger devices, while on-resistances are just 260 m $\Omega$  and 65 m $\Omega$ , respectively. The expansion of conduction area does introduce concerns, however, with blocking voltages unevenly distributed, due to severe electric-field crowding at the NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> mesa edge.

One way to address this challenging issue is to use a bevelled mesa design with different bevel angles. Recently, by implementing a bevel mesa design with a 6 $^{\circ}$  bevel angle, we have boosted the blocking voltage of our NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes from 1.1 kV to over 1.9 kV (see Figure 3 (d)) while maintaining their excellent forward conduction characteristics.

We can benchmark our NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes using Baliga's power figure-of-merit. For our large-scaled power rectifiers, this benchmark produces a value of over 1.8 GW/cm<sup>2</sup>. It is a value that approaches the limit of SiC unipolar devices, and is comparable to state-of-the-art large-sized Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes rectifiers, as well as

commercial Schottky barrier diodes based on GaN and SiC (see Figure 3 (e)).

### Dynamic switching characteristics

For emerging Ga<sub>2</sub>O<sub>3</sub> power devices, systematic investigations of dynamic characteristics are still lacking. This is a significant omission, because an insight into the dynamic characteristics of these devices is crucial for designers of power electronic circuits for practical applications. To evaluate the dynamic performance of power devices, those within our team that are led by Hai Lu have developed a high-speed, high-reliability dynamic testing system. This is capable of evaluating all switching parameters normally listed in device datasheets (see Figure 4). Measurements undertaken with this set-up include the double-pulse switching test, which features a fast-speed commercial GaN transistor, serving as an active switch that is capable of on/off switching within 50 ns (Figure 5 (a)).

Traces on one of our oscilloscopes show that during the switch-off process, the reverse recovery losses in our NiO/β-Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes are almost zero, while the switching time is around just 12 ns (see Figure 5 (b)). We attribute this fast-speed switching to a sub-nanosecond minority-carrier lifetime, and limited storage charges in the drift region that are easily extracted by the high reverse bias during the switching process.

A straightforward, valuable way to evaluate power devices is to assess their power-conversion capability. We have taken this approach, constructing a 500 W power-factor-correction circuit to exploit the power-conversion efficiency of our NiO/β-Ga<sub>2</sub>O<sub>3</sub> heterojunction diode (see Figure 5 (c)). In this circuit our device has a power conversion efficiency of 98.5 percent, and provides stable switching for the 100 minutes under test (see Figure 5 (d)). These figures underscore the promise of our

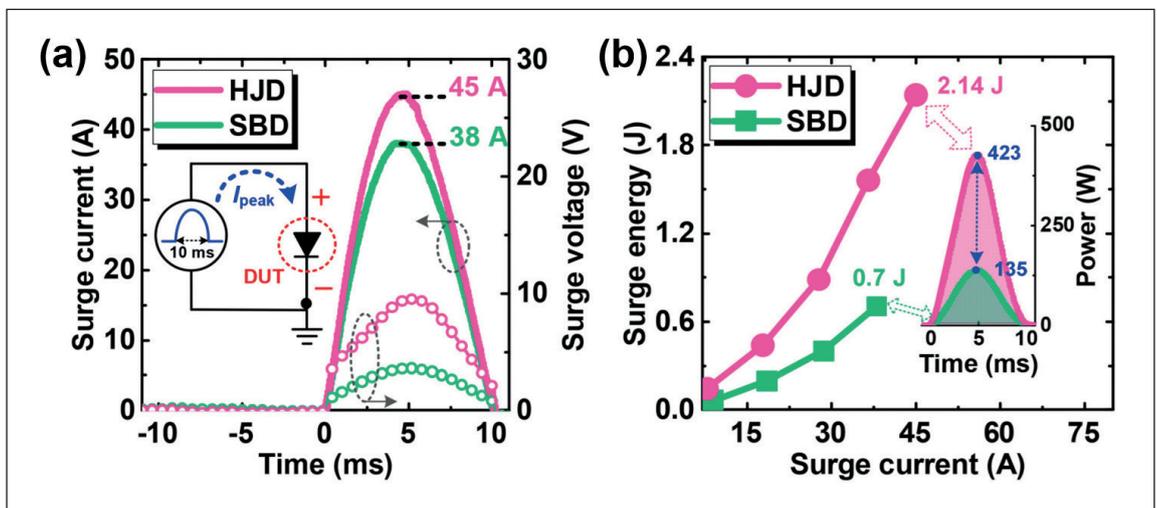
NiO/β-Ga<sub>2</sub>O<sub>3</sub> rectifiers for serving in high-power, high-efficiency power applications.

The Achilles' heel of β-Ga<sub>2</sub>O<sub>3</sub> is its rather low thermal conductivity. This well-known flaw is of such concern that it has led some to question whether Ga<sub>2</sub>O<sub>3</sub> is a viable material for making power devices. However – and this will come as a surprise – in our NiO/β-Ga<sub>2</sub>O<sub>3</sub> power rectifiers the self-heating effect caused by this weakness is not a major worry. When elevating the temperature of our rectifier from 25 °C to 200 °C, we found that our device exhibited an enhanced current capability, alongside a significant reduction in on-resistance. The case temperature for our device at a switching frequency of 0.3 MHz was only just over 60 °C, and more than 10 °C lower than that of the commercial silicon fast-recovery diode. Note that this is not the case for other forms of Ga<sub>2</sub>O<sub>3</sub> device – in those variants, there is significant self-heating that results in a high junction temperature and ultimately severe degradation of the forward-current output.

### Enhancing reliability

The rapid progress that has been realised with Ga<sub>2</sub>O<sub>3</sub> power devices has not been accompanied by a systematic characterization of device reliability. Particularly lacking are reports of device behaviour under large forward surge-currents and high reverse transient-energy spikes. When high currents run through the device for a long duration, or it experiences current overshoot/oscillation surging, this can generate a huge amount of Joule heat within the resistive diodes. Heat accumulating inside these diodes leads to an abrupt rise in junction temperature, and in turn a hike in on-resistance that deteriorates device performance.

Using a resonance circuit to generate a half-sinusoidal surge current, we have found that our Ga<sub>2</sub>O<sub>3</sub> heterojunction diode produces a peak surge of 45 A, with a high surge power of 423 W. These



➤ Figure 6. (a) Surge current-voltage (I-V) waveforms of the 9-mm<sup>2</sup> heterojunction diode (HJD) and Schottky barrier diode (SBD). Inset: The resonance circuit generates a 10 ms half-sine surge current pulse to go through the device under test. (b) The corresponding surge power and energy.



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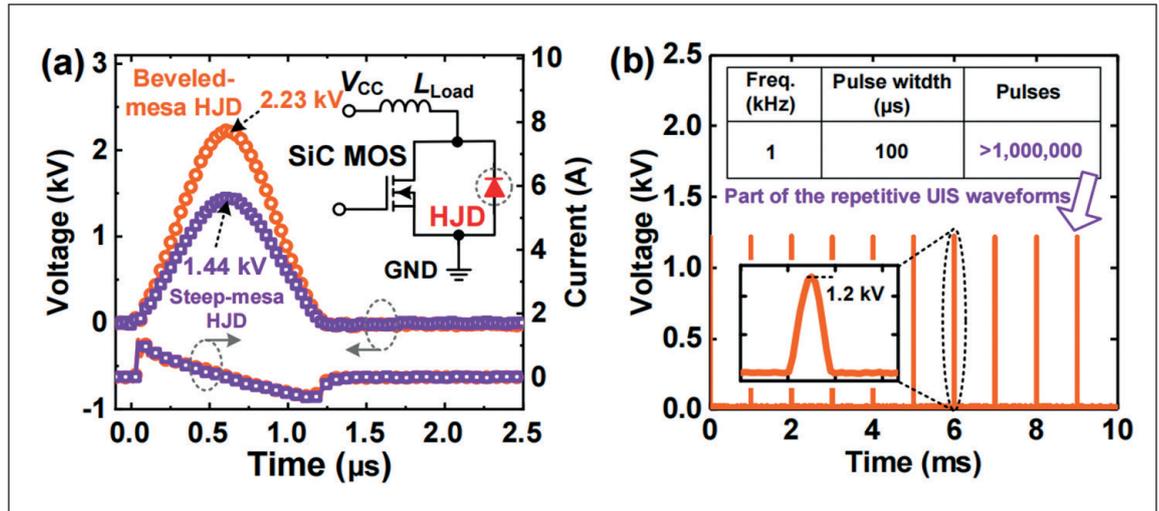


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➤ Figure 7. (a) The unclamped inductive switching (UIS) current and voltage waveforms of the bevelled-mesa Ga<sub>2</sub>O<sub>3</sub> heterojunction diode (HJD) and the step-mesa Ga<sub>2</sub>O<sub>3</sub> HJD, respectively. Inset: schematic of the test circuit. (b) Repetitive UIS waveforms and parameters.



values are far higher than those of the Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes counterpart (see Figure 6). The superior conduction capability of our devices comes primarily from the bipolar conductivity modulation effect in a dynamic/transient level, which is induced by minority carrier injection and diffusion.

In addition to withstanding the released energy stored in the inductors of inductive switching circuits, such as power-factor-correction circuits, in order for power devices to offer good levels of reliability, it is critical that they provide transient overvoltage ruggedness – that is a measure of the dynamic blocking voltage.

To see if this is the case, we have used an unclamped inductive switching test setup to determine the reverse overvoltage reliability of our Ga<sub>2</sub>O<sub>3</sub> rectifiers. We have found that our device with a 6° bevel angle exhibits an ultra-high dynamic blocking voltage of 2.23 kV and can handle a repetitive breakdown over 1 million times (see Figure 7). These results demonstrate that appropriate electric field management can ensure advantageous overvoltage ruggedness.

Several strengths of the device are behind its superior breakdown performance. Firstly, there is minimal electric-field-crowding at the small-angle mesa edge, in stark contrast to the large electric field found in the step-mesa heterojunction diode, containing sharp corners that are the cause of premature breakdown.

Furthermore, our latest devices benefit from: an extension of the off-state *p-n* depletion region that contributes to the suppressed leakage current; and our room-temperature sputtering process, which reduces interfacial traps and trims the leakage current. The benefits are significant – we are breaking new ground when experimentally verifying that NiO/β-Ga<sub>2</sub>O<sub>3</sub> heterojunction diodes are capable of delivering robust reliability, both in forward and reverse operation; and we have overcome the grand challenge of transient surge-current and breakdown in actual power circuits.

Our successes are important breakthroughs, taking this device one step further towards providing the key building block in a new generation of power electronics delivering unprecedented levels of power, efficiency and reliability.

### FURTHER READING

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# Improving GaN-on-silicon RF devices

Dialling back the trimethylaluminum flow prior to buffer growth yields high-quality GaN-on-silicon devices with a low RF loss

A TEAM FROM China and Japan is helping to close the gap in performance between GaN RF devices grown silicon and those formed on SiC, which are superior but more expensive.

Spokesman for the collaboration, Xuelin Yang from Peking University, says that the team's GaN-on-silicon growth process yields epiwafers that break new ground for dislocation density, while ensuring a low RF loss.

layer, substrate nitridation or the use of MBE. While these approaches have suppressed aluminium diffusion and consequently RF loss, this has come at the expense of degradation to crystal quality.

Avoiding this compromise, the team – from Peking University, China's CEC Compound Semiconductor, the Collaborative Innovation Centre of Quantum Matter in Beijing, and Japan's International Centre for Materials Nanoarchitectonics – has triumphed by investigating samples produced with a variety of growth and pre-growth conditions.

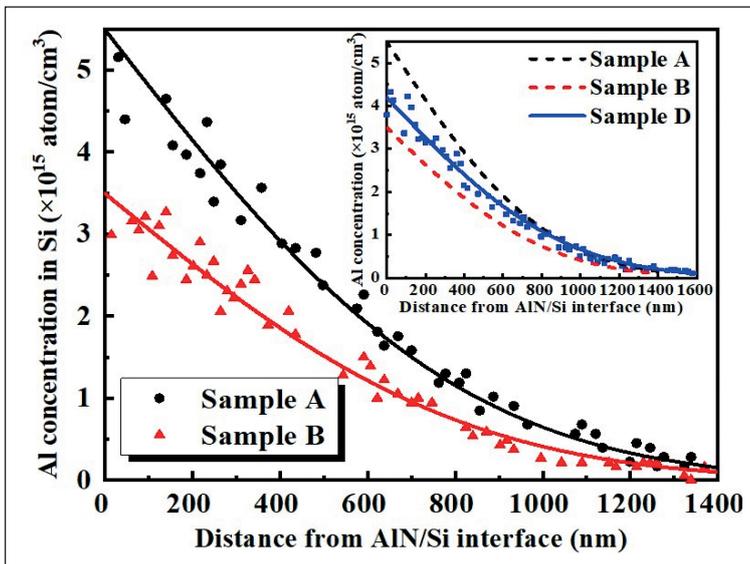
These trials began by loading 150 mm high-resistivity silicon substrates into a planetary MOCVD reactor and annealing them under hydrogen gas for 10 minutes. Samples were formed by flowing trimethylaluminum for 3 minutes at rates of either 15 sccm, 10 sccm or 5 sccm, prior to the growth of a 90 nm-thick AlN buffer. The team also produced a fourth sample using a pre-flow rate of 10 sccm for 3 minutes, followed by the growth of a 190 nm-thick buffer. For all four samples, the researchers added a 1.3  $\mu\text{m}$ -thick GaN layer, using a lattice-mismatch-induced stress-control technology.

Transmission electron microscopy revealed that the lowest trimethylaluminum flow rate of 5 sccm led to cracks in the epiwafer. With higher flow rates, cracks were absent. Investigating the crack-free samples with secondary ion mass spectrometry (SIMS) showed that dialling back the trimethylaluminium flow prior to AlN growth from 15 sccm to 10 sccm cut the concentration of aluminium at the AlN-silicon interface from  $5.5 \times 10^{15} \text{ cm}^{-3}$  to  $3.5 \times 10^{15} \text{ cm}^{-3}$ . The extent of this reduction followed the fall in trimethylaluminium flow. Measurements also revealed that increasing the AlN buffer thickness from 90 nm to 170 nm increased the aluminium impurity concentration at the substrate surface from  $1.8 \times 10^{11} \text{ cm}^{-2}$  to  $2.4 \times 10^{11} \text{ cm}^{-2}$ .

Based on the findings provided by SIMS, Yang and colleagues concluded that aluminium diffusion is more sensitive to trimethylaluminium flow prior to AlN growth than the thickness of AlN that is deposited.

To determine RF losses, the team added transmission lines in a coplanar waveguide configuration to their heterostructures. The sample with the lowest level of aluminium diffusion produced the lowest RF loss, of just 0.25 dB  $\text{mm}^{-1}$  at 10 GHz. For this sample, the dislocation density is  $2.9 \times 10^9 \text{ cm}^{-2}$ .

Yang believes that even better results may be possible by investigating a greater range of trimethylaluminium flows and AlN thicknesses.



► For the growth of high-quality GaN layers, the lowest level of aluminium in a silicon substrate comes from a pre-growth flow of 10 sccm, and an AlN thickness of 90 nm (sample B). Sample A had a higher flow of 15 sccm, and sample D had a 10 sccm flow rate and an AlN thickness of 190 nm (sample C, not shown and having a 90 nm-thick AlN layer produced with a 5 sccm flow, had cracks in the epilayers).

Success on both these fronts has come from tackling issues associated with the growth of the AlN buffer layer. Prior to and during its growth, aluminium diffuses into the silicon substrate, where it acts as a shallow acceptor impurity, forming a *p*-type parasitic layer that causes RF loss. Yang and co-workers have minimised this diffusion by optimising the trimethylaluminium flow rate.

Note that these researchers are by no means the first to try and improve the quality of GaN-on-silicon material for RF applications by suppressing the diffusion of aluminium. Others have turned to either a reduction in growth temperature, insertion of a 3C-SiC blocking

## REFERENCE

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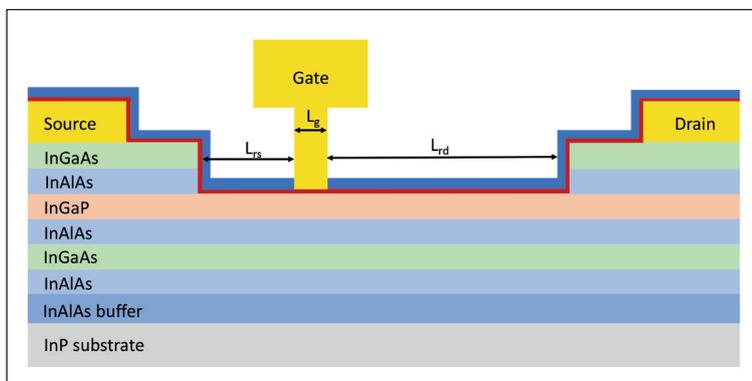
# Steam annealing enhances the InP HEMT

Fabricated with a steam annealing step, InP HEMTs with an ultra-thin  $\text{Al}_2\text{O}_3$  gate dielectric produce a high maximum-oscillation frequency over a wide bias range

ENGINEERS from Fujitsu have realised a high-frequency performance for an InP HEMT over a wide bias range with a fabrication process that involves steam-annealing an  $\text{Al}_2\text{O}_3$  gate dielectric.

This HEMT's combination of a reduced gate leakage current, an increased forward-breakdown voltage and a maximum oscillation frequency ( $f_{\text{MAX}}$ ) that's in excess of 700 GHz over a wide bias range, has much promise for the future of mobile communications.

When 6G is eventually rolled out, it may well use carrier frequencies in the 275 GHz to 320 GHz range to boost bandwidth compared with previous communication standards. Due to significant attenuation at these very high frequencies, amplifiers with a high output frequency will be needed, a requirement met by InP HEMTs.



► Fujitsu's insulated-gate HEMT has values for gate length ( $L_g$ ),  $L_{\text{RS}}$  and  $L_{\text{RD}}$  of 75 nm, 70 nm and 150 nm, respectively.

Historically, this class of HEMT has been held back by a large leakage current, a low breakdown voltage and a lack of high linearity. But that's not the case for Fujitsu's device, which overcomes all these weaknesses with an  $\text{Al}_2\text{O}_3$  gate dielectric – it is renowned for its wide bandgap, high dielectric constant and high breakdown voltage.

To produce this transistor, the team took an InP substrate and deposited an epitaxial stack that included a 9.5 nm-thick  $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$  channel and a carrier supply layer comprising a 3 nm-thick,

unintentionally doped  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  spacer and a 4 nm-thick, *n*-type  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  doping layer. Selective wet etching formed a gate recess area, on which the team added a 2 nm-thick  $\text{Al}_2\text{O}_3$  film, grown by atomic layer deposition. To minimise defects in this oxide, the engineers applied steam annealing for 1 hour at 300 °C.

According to work by other groups, annealing in an oxygen-containing environment enhances passivation of dangling bonds, including oxygen vacancies in oxide films. In particular, the use of steam is expected to accelerate hydrolysis of carbon impurities in  $\text{Al}_2\text{O}_3$  films caused by trimethylaluminium.

Following steam annealing, the researchers added a 10 nm-thick SiN passivation layer by plasma-enhanced CVD, before defining a gate region by etching with  $\text{SF}_6$ . Finally, they formed a Y-shaped Ti/Pt/Au contact (see figure for the completed structure). In addition, the team fabricated a control device, free from  $\text{Al}_2\text{O}_3$  and featuring a Schottky gate.

To examine chemical bonds in devices before and after annealing, the team turned to Fourier transform infrared spectroscopy. Peaks associated with C-C and C-O bonds were far weaker after steam annealing, while the signal associated with the Al-O bond increased in intensity. Based on these findings, the team suggested that steam annealing enhanced the hydrolysis of carbon impurities and the passivation of dangling bonds in the  $\text{Al}_2\text{O}_3$  film.

Another potential consequence of steam annealing is that it affects electron traps within the transistor. To determine whether this is the case, the team measured the sheet resistance of their HEMTs, using the transmission line method. This investigation showed that steam annealing reduced resistance in the insulated gate HEMT from 262  $\Omega/\text{sq.}$  to 211  $\Omega/\text{sq.}$ . The team attributed this fall to the hydrolysis of carbon impurities and the passivation of dangling bonds.

Electrical measurements on both types of device showed that the insulated-gate HEMT had a superior transconductance profile. Thanks to this, values for  $f_{\text{MAX}}$  and the cut-off frequency,  $f_{\text{T}}$ , undergo very little change with gate bias. The favourable flat profile for  $f_{\text{MAX}}$  peaks at 801 GHz, for a gate bias of 0.05 V, and is in excess of 700 GHz between -0.5 V and 0.25 V.

The team claims that its results show that its insulated-gate HEMT promises to improve the RF performance of InP HEMTs for very high frequency applications.

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# Optimising GaN crystal growth

Very high temperature oxygen vapour phase epitaxy looks to simplify bulk GaN crystal growth

ENGINEERS from Japan have improved the quality of GaN crystals produced with oxygen vapour phase epitaxy by shifting growth to very high temperatures.

Their success increases the promise of the oxygen vapour phase epitaxy technique (OVPE), which delivers several advantages over the incumbent, HVPE.

Benefits of OVPE over HVPE include the absence of solid by-products, such as  $\text{NH}_4\text{Cl}$ , and the production of material with a high carrier concentration and low resistivity, thanks to the incorporation of a high concentration of oxygen, which acts as a donor.

Spokesman for the Japanese team, Shigeyoshi Usami from Osaka University, told *Compound Semiconductor* that the key to the latest breakthrough has been the establishing of a pre-growth technology.

“Since GaN decomposes at 1300 degrees Celsius, it was very difficult to grow at such a high temperature,” explains Usami.

However, Usami says that by introducing a pre-growth process, he and his co-workers can now suppress the decomposition of the seed substrate and grow GaN at 1300 °C.

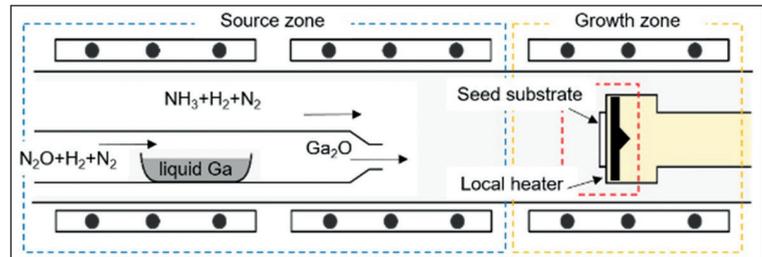
When these engineers were previously restricted to a growth temperature of 1250 °C, they produced polycrystalline GaN at a growth rate of around 100  $\mu\text{m/hr}$ . When cranking up the temperature to 1300 °C, they almost eliminated polycrystallinity, while doubling the growth rate.

With OVPE, GaN is produced by reacting gallium oxide and ammonia; water and hydrogen are the by-products. Gaseous gallium oxide is formed by oxidising gallium pellets.

To produce bulk GaN, the gallium oxide and ammonia are directed at a GaN seed that is placed in the growth zone and heated with a resistive heating system (see Figure).

Once the temperature of the seed exceeds 500 °C, ammonia is directed at its surface to prevent GaN decomposition. However, this is not sufficient when the temperature of the seed is as high as 1300 °C. At that temperature voids form at the interface between the seed and epi-layer.

In this latest work, Usami and colleagues show that introducing  $\text{Ga}_2\text{O}_3$  gas during the heating-up period



prevents decomposition of the seed at 1300 °C. Initial success came from using a  $\text{Ga}_2\text{O}_3$  flow rate of 2.1 sccm for heating between 1200 °C and 1250 °C, before increasing to 4.2 sccm over the 1250 °C to 1300 °C range.

Scanning electron microscopy images show that GaN grown with these conditions is free from large pits, polycrystallinity and voids at the interface between the seed crystal and the epilayer. These findings indicate that  $\text{Ga}_2\text{O}_3$  gas flow prevents decomposition of the seed prior to GaN epigrowth.

A second set of experiments considered the impact of temperature on the extent of polycrystallinity at high growth rates. The researchers compared growth at 1200 °C, without any pre-growth flow of  $\text{Ga}_2\text{O}_3$  gas; growth at 1250 °C, using a  $\text{Ga}_2\text{O}_3$  flow rate of 2.1 sccm when heating between 1200 °C and 1250 °C; and the conditions previously used for growth at 1300 °C.

Scanning electron microscopy images of a number of samples produced during this study showed that at 1200 °C and 1250 °C, the higher the  $\text{Ga}_2\text{O}_3$  gas flow during GaN growth, the greater the extent of polycrystallinity. However, at 1300 °C the polycrystalline density did not increase with  $\text{Ga}_2\text{O}_3$  gas flow, and GaN with almost no polycrystallinity could be produced at a growth rate of 195  $\mu\text{m/hr}$ .

Usami thinks that it will be possible to grow GaN at even higher temperatures, such as 1350 °C, which will help to accelerate growth.

“But, the higher the temperature, the more severe the decomposition, so it is necessary to precisely optimize the pre-growth conditions.”

The team is aiming to realise growth rates of over 1 mm/hr.

► With oxygen vapour phase epitaxy, GaN is produced by reacting gallium oxide and ammonia. Water and hydrogen are by-products.

## REFERENCE

► A. Shimiz *et al.* Appl. Phys. Express 15 035503

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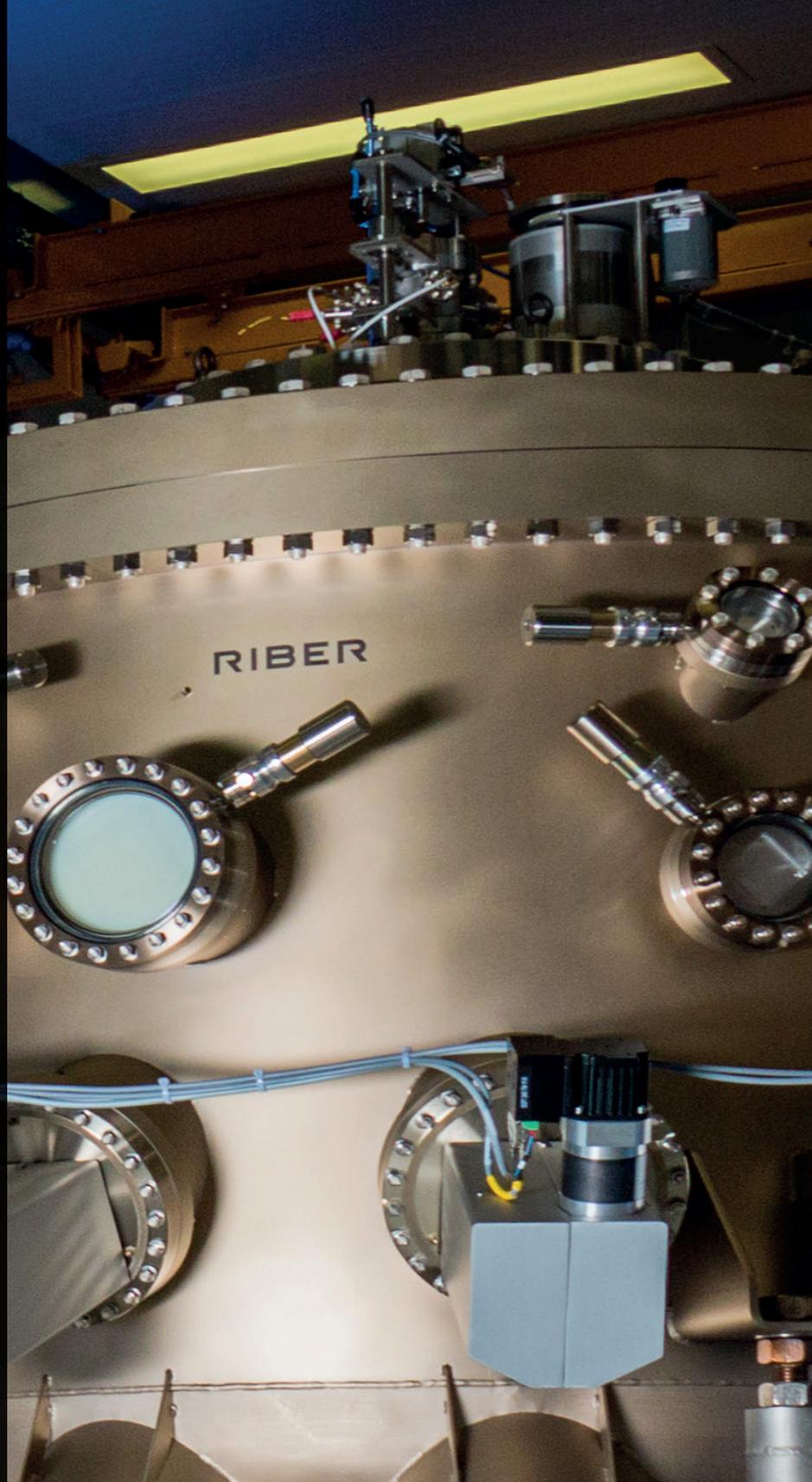
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