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Great electrical characteristics and intrinsic radiation hardness makes the GaN HEMT ideal for driving motors in space

Supporting a surge in UV performance

Defect control during the growth of AlGaN layers on AlN substrates enables record-breaking optoelectronic devices

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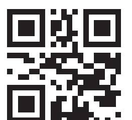

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VIEWPOINT

By Richard Stevenson, Editor

Quantum technologies

WHAT DO YOU THINK of when you hear the word 'quantum'? In my case, my mind harks back to my undergraduate days when I studied physics. In particular, I recollect the second-year quantum mechanics course, where we considered the solutions to the particle in a box – shrink its dimensions and the energy of the particle increases. But, fortunately for me, this fascinating piece of physics did not end there. In my third year, I investigated the photoconductivity of a heterostructure featuring a quantum well sample, getting to see for the first time that quantum wells were not restricted to text books and exam questions, but can be formed through the growth of epilayers.

Like many of you, when you I hear quantum I also think of the wells in the LEDs that illuminate our homes and offices, or those in laser diodes that are at the heart of the internet.

But this is not the quantum of quantum technologies. That term, which I really don't like but can offer no better alternative, is concerned with phenomena that Einstein's referred to as the spooky action at a distance. It is the technologies that are associated with entanglement, such as ultra-secure communications, enabled by quantum key distribution, and financial modelling that's underpinned by quantum computers.

The two forms of quantum that I've mentioned are actually entwinned, with compound semiconductor devices featuring quantum wells needed for the new quantum tech. For example, the VCSEL is the preferred source for the optical pumping of atomic transitions in a chip-scale atomic clock.

What this means is that the promise of growth of a quantum technologies industry is good news for our community. However, grabbing this opportunity will not be easy. The challenges, outlined in more detail in the

opinion piece *Component viability risks bursting the quantum bubble* (see p. 28), is that the specifications are very tight, causing yield to take a massive hit.

It really helps if the device that's needed for quantum tech has already been established for other applications. That's the case with the VCSEL, widely used in datacoms and facial recognition systems. With this starting point, it's possible to draw on all the accumulated knowledge to try and meet the very demanding specs, which can be particularly tough as narrowing in on one can be detrimental to another.

An established market also aids production, because it increases the total volume for a device. This puts VCSELs at advantage over the likes single-photon emitters and detectors. Getting them to market at an acceptable cost will not be easy, but if quantum tech is compelling enough, I expect this leap to be made.

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High voltage WBG power electronics come of age

800V EVs charge into the mainstream using SiC power electronics, says IDTechEx report

THE DEMAND for electric vehicle (EV) power electronics will increase dramatically in the next ten years, primarily driven by rapid growth in the BEV car market, where IDTechEx predicts a 15 percent CAGR globally over the next decade.

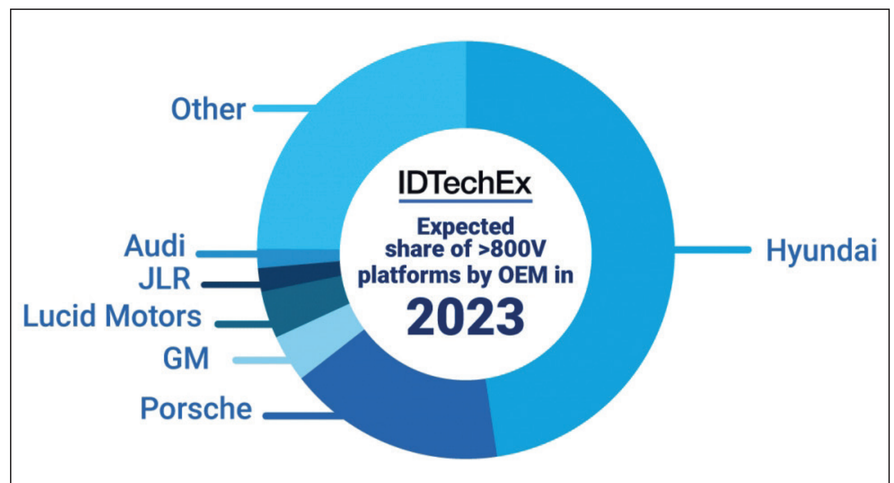
Currently, the weighted-average battery capacity of BEV cars is increasing in all regions, piling pressure on battery supply chains, and creating uncertainty. The result is that drive cycle efficiency must come to the forefront of powertrain design, meaning the time has come for high-voltage wide bandgap (WBG) power electronics.

The IDTechEx report *Power Electronics for Electric Vehicles 2023-2033* details the evolving semiconductor and package materials, die-attach materials, wire bonding, thermal management and more.

While silicon IGBTs have dominated the medium-to-high power device range for 20 years, including in EV power electronics, they are giving way to SiC and GaN. This will fundamentally impact the design of new power devices, including the package materials, as high-voltage and high-power-density modules operating at higher temperatures becomes the trend.

The two drivers often cited to move from 350-400 V to 800 V and beyond are higher power levels of DC fast charging (DCFC), for example, 350 kW, and drive cycle efficiency gains. DCFC compatibility today is a relatively weak driver due to low availability versus AC chargers and the high costs associated with 800 V infrastructure.

IDTechEx estimates around 3 million AC charging installations took place in 2022, compared with 50,000 DCFCs over 100 kW. In addition, higher levels of DCFC does not necessarily drive a transition to 800 V, although it is more optimal. Tesla is a good example, having deployed 250 kW superchargers without moving beyond its 350 V platform.



The efficiency argument for 800 V is stronger. This allows joule losses to be reduced and high-voltage cabling to be downsized. Combined with SiC MOSFETs, it typically leads to 5-10 percent efficiency gains, which can potentially downsize the expensive battery, save costs, or improve the vehicle's range, creating a competitive advantage.

Yet, it is a challenging time for the automotive industry and 800 V adoption experienced some pitfalls in 2022. The Lucid Air, the first 900 V production car, sold around 7,000 units in 2022 after an initial goal of 20,000. Porsche's Taycan was also one of the OEM's best-selling models in Europe between 2020 – 2021, but sales declined in 2022. Both are the results of continued parts shortages and supply chain challenges, for example, wire harness shortages with the Russia-Ukraine war.

On the other hand, Hyundai is demonstrating the success of 800 V platforms. Sales of the company's models using the 800 V E-GMP platform more than doubled in South Korea to around 70,000 units/year, driven by the popularity of the IONIQ 5 and Kia EV6. This takes the 800 V car market into the mainstream car segments for the first time. To support the rapid growth, Hyundai is diversifying its SiC supply partnerships, signing new deals with onsemi and STMicroelectronics in 2022 to add to existing relationships with Infineon and Vitesco.

China is also signaling a transition to 800 V vehicles, with development plans from major OEMs in 2022, including BYD, XPeng, Great Wall Motors, GAC, and others. These vehicles will most likely use SiC MOSFETs, allowing the SiC industry to tap into the world's largest EV market, as China sold over 6.5 million EVs in 2022.

While 1200 V SiC MOSFETs (adopted in 800 V vehicle platforms) will play a key role in optimising drive cycle efficiency, it is still only one piece of the puzzle. Drive cycle efficiency can be improved in many areas, from improved battery chemistry to solar bodywork, high-voltage cable reduction per vehicle, 600 V SiC, improved motor design, and so on. The task for automakers is to work towards constantly improving the overall drive cycle efficiency to ensure battery supply does not go wanting.

Wolfspeed host first stop on 'Invest in America' tour

President Biden delivered remarks about initiatives aimed to grow the American economy

AMERICAN SiC chip company Wolfspeed hosted the first stop of President Joe Biden's 'Invest in America' tour at the company's Durham, NC, headquarters.

The US President highlighted initiatives designed to boost American manufacturing, rebuild the nation's infrastructure and strengthen supply chains. US Secretary of Commerce Gina Raimondo and North Carolina Governor Roy Cooper were also in attendance at the event.

"We're honoured to have been the first stop on the President's 'Invest in America' tour and to be recognised for our commitment to growing US manufacturing and making a name for North Carolina in the tech space," said Wolfspeed President and CEO, Gregg Lowe.

"SiC is at the heart of what we do – it's essential to accelerating the adoption of EVs, delivering energy savings to consumers, and meeting global emission reduction targets. Wolfspeed is proud to play a critical role in fulfilling the objectives of the CHIPS & Science Act and the Inflation Reduction Act, and to reinforce US leadership in the energy transition and the semiconductor industry."

Wolfspeed currently produces more than 60 percent of the world's SiC materials at its Durham, NC, headquarters, but is engaged in a $6.5 billion capacity expansion effort to increase production.

This includes the opening of the company's 200 mm Mohawk Valley device fab in April 2022, and the construction of The John Palmour Manufacturing Center for SiC, a 445-acre SiC materials facility in North Carolina, which will expand the company's existing materials capacity by more than 10 times. Phase one construction for the materials facility is anticipated to be completed in 2024. This year, Wolfspeed also announced plans to build a 200 mm wafer fabrication facility in Saarland, Germany.

➤ left to right: Wolfspeed CTO, Elif Balkas; President Joe Biden; Wolfspeed CEO, Gregg Lowe.

Cree LED delivers breakthrough light output

CREE LED has released a new range of high power LEDs which offer 228 lumens-per-watt (LPW) typical at 4000K, 70 CRI and 1 W.

The J Series LEDs are said to deliver up to three times the light output of competing 5050 LEDs at the same efficacy level. These advanced LEDs are also designed with superior corrosion resistance for the most challenging environments.

With the addition of the new E Class LEDs, Cree LED now offers four performance levels in the J Series 5050 LED portfolio to address most directional general lighting applications.

Unlike other 5050s with asymmetric die layouts that reduce intensity through secondary optics, J Series 5050 LEDs feature optimised layouts that deliver peak intensities up to 12.5 percent higher than the competition as well as improved colour-over-angle.

"The breakthrough performance of 5050C E Class LEDs enables substantial system cost savings through the reduction in optics, PCBs, and chassis material. Up to 40 percent system cost savings and 57 percent reduction in size are possible when redesigning from a lower performance 5050 LED to the 5050C E Class LED," said David Peoples, vice president of marketing at Cree LED. "To speed up the design-in process, 5050C E Class LEDs are compatible with optics designed for existing square LES 5050 LEDs."

Suitable for outdoor area, high/low bay, roadway, and indoor professional applications, the new 5050C E Class LEDs are available in 2200K-6500K correlated colour temperatures (CCTs) as well as 70, 80 and 90 CRI options for all CCTs.

Product samples are available now and production quantities are available with standard lead times.

Avicena and Ams Osram partner on chip-to-chip interconnects

SUNNYVALE-BASED AvicenaTech has partnered with Ams Osram to develop high-volume manufacturing of GaN microLED arrays for its LightBundle communication architecture.

Avicena's LightBundle links use densely packed arrays of GaN microLEDs to create highly parallel optical interconnects with typical throughputs of more than 1 Tb/s at less than 1 pJ/bit. A LightBundle cable uses a highly multicore multimode fibre to connect a GaN microLED transmitter array to a matching array of silicon photodetectors (PDs).

Arrays of hundreds or thousands of LightBundle's microLEDs and PDs are said to be easily integrated with standard CMOS ICs, enabling the closest integration of optical interconnects with electrical circuits.

In addition to high energy efficiency and high bandwidth density, these LightBundle links also exhibit low latency since the modulation format of the individual links is simple NRZ, instead of PAM4, which is common in many modern optical links but has the disadvantage of higher power consumption and additional latency.

The need for next generation computing power is here, driven by strong AI/ML and HPC application demand – for products like ChatGPT, DALL-E and autonomous vehicle training. Attempts to scale current architectures are running headlong into physical limits leading to slower throughput growth, power-hungry and hard to cool systems.

The LightBundle architecture breaks new ground by unlocking the performance of xPUs, memory and sensors – removing key constraints of bandwidth and proximity while simultaneously offering an order-of-magnitude reduction in power consumption.

"We acquired our fab from Nanosys in October to accelerate our development efforts and support low-volume prototype manufacturing," says Bardia Pezeshki, founder and CEO of Avicena. "However, we are addressing very sizeable markets requiring high-volume manufacturing. We are very pleased to partner with one of world's top GaN LED companies to provide a path to satisfy the expected high volumes required by our customers."

Robert Feurle, executive VP and managing director, OS Business Unit at Ams Osram, added: "Avicena's LightBundle technology provides an opportunity for GaN microLEDs to impact numerous key applications including HPC, AI/ML, sensors, automotive and aerospace. We are excited to partner with Avicena to transform these very large and important markets."

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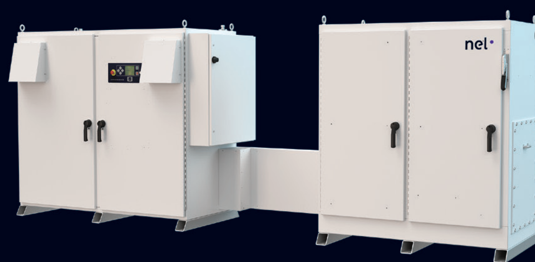

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Mitsubishi to build SiC fab

Company to respond to rapidly increasing demand for SiC power semiconductors for EVs and other low energy loss applications

MITSUBISHI ELECTRIC has announced plans to build a new wafer plant to increase production of SiC power semiconductors.

The company is responding to increasing demand for SiC chips for EVs as well as expanding markets for applications that require low energy loss, high temperature operation or high-speed switching.

Mitsubishi's announcement means that the company will now invest around $2 billion in the five-year period to March 2026, which is double its previously announced investment plan. $756 million will be used to construct a new 8-inch SiC wafer plant and enhance related production facilities.

The new factory, which will incorporate a facility in the Shisui area of Kumamoto Prefecture, will produce large-diameter 8-inch SiC wafers, introduce a clean room featuring state-of-the-art energy efficiency and high-level automated production efficiency.

In addition, the company will enhance its production facilities for 6-inch SiC wafers to meet growing demand in this sector as well.

Mitsubishi will also invest approximately $75 million in a new factory that will consolidate existing operations, currently dispersed throughout the Fukuoka area, for the assembly and inspection of power semiconductors. The company says the integration of design, development and production technology verification will greatly enhance the company's development capabilities and facilitate timely mass production in response to market demand.

The remaining $150 million, all new investment, will be targeted at equipment enhancements, environmental arrangements and related operations.

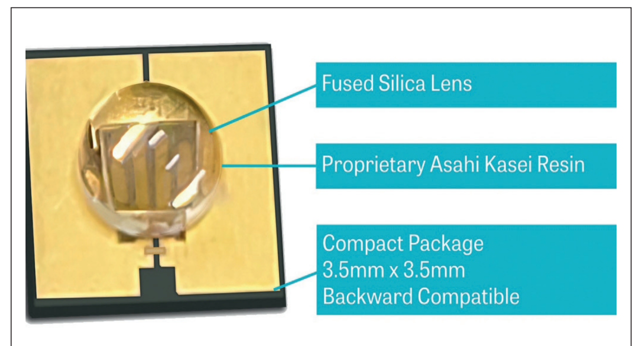
Crystal IS demos 160 mW UVC LED

CRYSTAL IS, a subsidiary of Asahi Kasei, has demonstrated a next-generation Klaran single-chip UVC LED that emits at 160 mW in the germicidal range of 260-270 nm. Claimed to set a new record for single-chip device output in a commercial device, this marks a 60 percent increase over prior Crystal IS devices.

Crystal IS says this higher-output device will be used to accelerate the adoption of UVC LEDs and hasten the widespread replacement of low-pressure mercury lamps.

While the new device will retain the Klaran 3.5 mm x 3.5 mm package and solder pad design to allow backward compatibility with existing customer designs, the higher output will allow UVC LEDs to meet the performance and cost targets needed to expand into new applications in high-flow water and air treatment.

The new UVC LED design, built on Crystal IS' AlN substrate, uses a rigid fused silica lens and a thin layer of proprietary UVC transparent resin developed by Asahi Kasei to withstand the intense UVC output.



In contrast to soft moulded lens, the rigid fused silica lens allows higher transmission of the UVC light, ensuring stable long-life performance and high-temperature stability.

"This new high-output and long-life Klaran device is made possible by the strong cooperation between Crystal IS and Asahi Kasei innovation teams," said Eoin Connolly, president and CEO. "With this new device in our portfolio, Klaran UVC LED devices make another significant step forward in replacing low-pressure mercury lamp technology and promoting the transition to non-mercury/non-ozone generating devices."

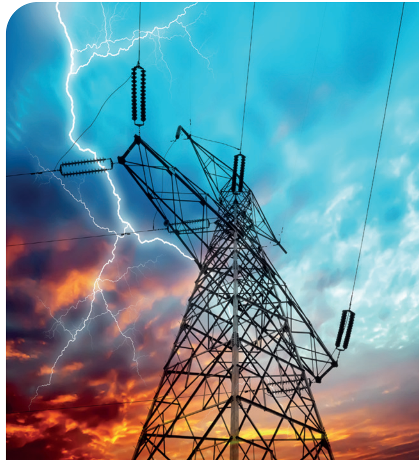
US DOE announces $48 million grid project

ULTRAFAST project will advance performance limits of silicon, wide bandgap, and ultra-wide bandgap semiconductors to improve their actuation methods

THE US Department of Energy (DoE) has announced $48 million in funding to support a new programme focused on developing power grid technologies that improve control and protection of the US domestic power grid.

The goal of ULTRAFAST (Unlocking Lasting Transformative Resiliency Advances by Faster Actuation of Power Semiconductor technologies) is to advance the performance limits of silicon, wide bandgap (WBG), and ultra-wide bandgap (UWBG) semiconductor devices that will enable faster switching and/or triggering at higher current and voltage levels for improved control and protection of the grid.

Unforeseen power grid outages are estimated to cost the US economy $150 billion annually. The DoE says that modernising the US grid infrastructure with improved efficiency and resilience against extreme weather events is critical to ensuring that clean energy and transportation options can reach communities across the country. Grid modernisation will also support



President Biden's goals to accelerate the deployment of renewables, boost the nation's energy independence, and achieve 100 percent clean electricity by 2035.

ULTRAFAST will fund projects that aim to enable utilities to more effectively control grid power flow to avoid disturbances, and quickly isolate and route around disruptions.

Managed by DoE's Advanced Research Projects Agency-Energy (ARPA-E), the ULTRAFAST's categories include:

- Device and/or module technologies targeting protection functions at high current and voltage levels by achieving very fast by-pass, shunt, or interrupt capability at as low level of integration as possible with nanosecond-level reaction time (and corresponding slew rates)
- High switching frequency devices and/or modules which enable efficient, high-power, high-speed power electronics converters
- Complementary technologies such as wireless sensing of voltage and current, high-density packaging with the integrated wireless actuators and device/module-level protection, power cell-level capacitors and inductors, and thermal management

ARPA-E first held a workshop on this topic last year. Workshop participants provided expert inputs on the technical aspects of ultra-fast-triggered semiconductors, and how such devices can aid US national goals to develop future high-performance resilient power systems.

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Wise-integration and Powernet team up on GaN PSUs

Combined technology is industry's first solution designed to replace analogue controls

WISE-INTEGRATION, a French pioneer in digital control of GaN power supplies and GaN ICs, and Powernet, a Korean power supply manufacturer, have announced an agreement to build compact and energy-efficient technology for power-supply applications that are currently limited to analogue control.

The memorandum of understanding addresses the needs of OEMs that require compact, digitally controlled power-supply systems for faster, smaller and more energy-efficient electronic equipment in products ranging from USB PD fast chargers to monitors, TV sets and electric vehicles.

The breakthrough system will combine Wise-integration's WiseWare digital controller and Wisegan, a 650 V enhancement-mode GaN-on-silicon IC for power applications from 30 W to 3 kW, with Powernet's switched mode power supply (SMPS) technology that efficiently converts electrical power. "We expect our collaboration to be the start of a new era in the power-supply industry by combining Powernet's well-established experience in productising power supplies and Wise-integration's GaN IC and digital-control technologies," said Lee Don Ju, CEO of Powernet, which is a supplier to Korea's semiconductor industry.

"This partnership, guided by our long-term business and development roadmap, will bring Wise-integration's unique GaN IC and digital-control technologies to global markets and enable Powernet to increase the power density and reduce the size of its SMPS products," said Thierry Bouchet, CEO of Wise-integration. "We will jointly deliver the high-level of compactness and superior performance required for the mass-market applications."

Wise-integration is believed to be the first company to bring digital control to the power-supply market, where previously only analogue controls were available. Original design manufacturers (ODM) such as Powernet are trying to meet growing demands from OEMs, which require increasingly small and ultra-efficient power supplies for their

future product lines. GaN is seen as a key material to delivering these features, but it is very difficult for power-suppy manufacturers to go above switching frequencies of 300 kHz with analog devices. Composed of a standard MCU 32-bit-based controller and running the company's proprietary firmware, WiseWare manages the WiseGan devices and controls the power supply. Because fewer components are required than in analog controllers and thanks to high running frequency, the new power-electronic architecture reduces weight and volume of standard solutions by 30 percent and significantly reduces production costs.

Transphorm and Weltrend partner on GaN SIP

GaN COMPANY Transphorm and Taiwanese fabless chip firm Weltrend Semiconductor have released their first GaN System-in-Package (SiP).

The WT7162RHUG24A SIP integrates Weltrend's WT7162RHSG08 multi-mode flyback PWM controller with Transphorm's 240 mΩ, 650 V SuperGaN FET.

The SIP is designed for use in 45 W to 100 W USB-C PD power adapters charging smartphones, tablets, laptops, and other smart devices. It offers peak power efficiency of greater than 93 percent. Device samples will be available in the second quarter of 2023.

Transphorm will show the Weltrend SiP

for the first time at the 2023 Applied Power Electronics Conference (APEC). The companies will also release details on the related WTDB_008 65W USB PD Power Adapter Evaluation Board during the event.

"The WT7162RHUG24A is the industry's first publicly announced SiP using Transphorm GaN. It enables manufacturers to develop a less expensive system solution given fewer components are required and a smaller PCB can be used among other advantages," said Tony Lin, president, Weltrend. "It also reduces system development time. Effectively, we're removing design barriers for adapter manufacturers,

Lin added: "Notably, this product also allows Weltrend to move into a new market. It is the first-ever SiP for our PWM controllers, validating our commitment to supporting high-volume growth sectors. And, with the integration of the GaN FET, we've raised the level of performance output."

Infineon to acquire GaN Systems

$830 million acquisition will strengthen GaN portfolio and power system expertise

INFINEON TECHNOLOGIES intends to acquire Ottawa-based GaN Systems for $830 million. The planned acquisition is an all-cash transaction and will be subject to customary closing conditions, including regulatory approvals.

"GaN technology is paving the way for more energy-efficient and CO_2-saving solutions that support decarbonization. Adoption in applications like mobile charging, data centre power supplies, residential solar inverters, and onboard chargers for electric vehicles is at the tipping point, leading to a dynamic market growth," said Jochen Hanebeck, CEO of Infineon.

"The planned acquisition of GaN Systems will significantly accelerate our GaN roadmap, based on unmatched R&D resources, application understanding and customer project pipeline. Following our strategy, the combination will further strengthen Infineon's leadership in Power Systems through mastery of all relevant power technologies, be it on silicon, SiC or GaN."

Jim Witham, CEO of GaN Systems, said: "The GaN Systems team is excited about teaming up with Infineon to create highly differentiating customer offerings, based on bringing together complementary strengths. With our joint expertise in providing superior solutions, we will optimally leverage the potential of GaN. Combining GaN Systems' foundry corridors with Infineon's in-house manufacturing capacity enables maximum growth capability to serve the accelerating adoption of GaN in a wide range of our target markets."

Wittham added: "I am very proud of what GaN Systems has accomplished so far and cannot wait to help write the next chapter together with Infineon. As an integrated device manufacturer with a broad technology capability, Infineon enables us to unleash our full potential."

In February 2022, Infineon announced doubling down on wide bandgap market by investing more than €2 billion in a new frontend fab in Kulim, Malaysia, strengthening its market position. The first wafers will leave the fab in the second half of 2024, adding to Infineon's existing wide bandgap manufacturing capacities in Villach, Austria.

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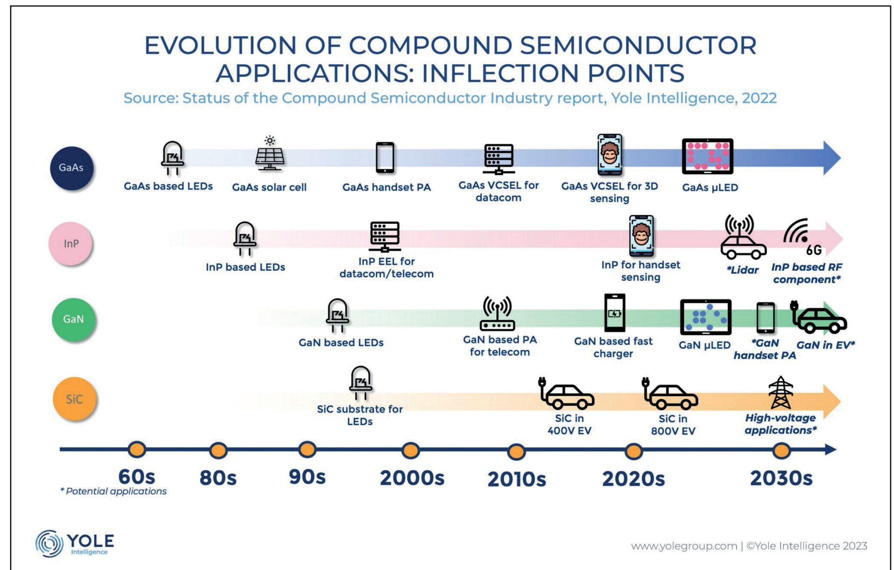
CS substrate market to double by 2027

SiC for power applications will represent the largest sector, growing at CAGR of 25 percent, say Yole

AS THE WORLD demands ever greater power and efficiency, the market for compound semiconductor substrate materials is set to more than double by 2027 – with SiC for power applications expected to significantly increase its market share compared to silicon. All mega trends have an increase use of compound semiconductor devices in their roadmap.

In its new *Status of Compound Semiconductors 2022* report, Yole Intelligence predicts the CS substrate material market will grow from $945 million in 2021 to $2.3 billion in 2027, at a 17 percent CAGR. By 2027, SiC for power applications will represent the largest sector, growing at a CAGR 2021-2027 of 25 percent and increasing market share among compound semiconductor substrates by around 50 percent. The photonics InP market will also increase its share and grow at a 20 percent CAGR. The third major market, RF GaN, which encompasses the substrates silicon and S.I. SiC, will maintain its market share but continue to grow with other applications at a 11 percent CAGR 2021-2027.

In 2021, ON Semiconductor (today onsemi) acquired SiC manufacturer GT Advanced Technologies. The same year, Hunan Sanan Semiconductor opened a $2.5 billion Chinese SiC production line that covers the entire supply chain – from crystal growth to power devices, packaging and testing – in a bid to increase its market share in power electronics. Wolfspeed, an existing leader in SiC substrates, epiwafers and processes, recently announced a new 8 inch SiC facility in Germany to cement its leading position and expand into the SiC device market. And, semiconductor giant Infineon partnered with automaker Stellantis in 2022. The deal, worth more than €1 billion, will see Infineon reserve manufacturing capacity and supply SiC chips in the second half of the decade to Stellantis' Tier 1 suppliers.



The RF GaN market is expected to grow in terms of size but not market share, partly as a result of the impact of the US sanctions on Huawei in 2019, which impacted the GaN-on-SiC supply chain. In 2023, the market is expected to gain momentum to grow again, thanks to the 5G base station market in various countries, such as India.

Navitas, which employs a GaN-on-silicon platform, is making moves within SiC with its recent acquisition of GeneSiC, which is expected to see it launch new GaN and SiC technologies in power electronics. Most recently, Infineon Technologies signed a deal to acquire GaN Systems for $830 million, which is by far the largest sale to date within the power GaN sector, representing around 18 percent of Infineon Technologies' power electronics' revenue and 4 times higher than the value of the entire power GaN market as of 2022.

In the photonics sector, mergers and acquisitions are helping companies competing in the sensing and telecom/ datacom sectors gain more market share and join-up competencies in InP and GaAs. For example, Coherent's acquisition by II-VI saw its competencies in InP and GaAs become more distributed across materials, components, and systems.

MicroLEDs is a serious growth vector for the GaAs photonics market. Ams Osram announced the construction of a €800 million microLED fab in Malaysia, which will be ready for mass production in 2024, to supply Apple with microLED displays for smartwatches.

As well as its photonics activities, Coherent is also a major supplier of SiC substrates for power and RF applications. Here, the company is attempting to move from the substrate to device level through its partnership with GE, which it recently expanded for three years. Coherent is also working to enter the RF GaN device market following on from its lead in RF GaN substrates through II-VI's competencies – it is partnering with Sumitomo Electric Device Innovations (SEDI) to do so.

Lumentum, on the other hand, has a contrasting business model. While its R&D is in house, it uses foundries such as IQE and WIN Semiconductors for manufacturing before supplying devices to Apple.

CrayoNano UVC LEDs reach 100 mW and 5 percent efficiency

UVC LED is a “game changer in the disinfection market”

NORWEGIAN START-UP CrayoNano has announced a performance improvement of its CrayoLED H-series UVC LED. Entering the class of 100 mW, 5 percent wall-plug efficiency at a standard operating current of 350 mA, this LED is said by the company to be a game changer in the disinfection market.

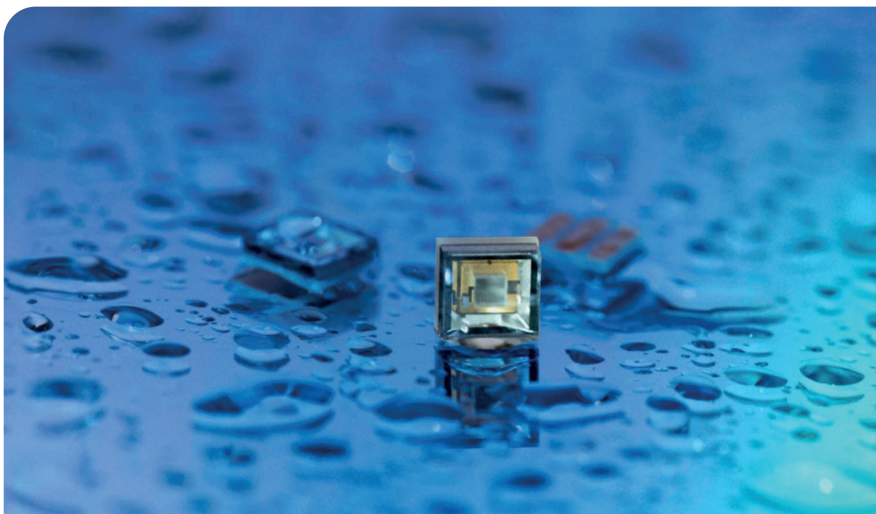
“Our dedication to continuous development and commitment to quality and performance has culminated in more than 30 percent improvement since the product’s launch. Entering the performance class of 100 mW, 5 percent wall plug efficiency, high drive current capacity without compromising our values of quality first – make the CrayoLED a reliable, efficient, and robust solution, ideal to enable mass UVC LED adoption into disinfection applications,” says Michael Peil, CRO. “With these results, we look forward to further characterisation of our LEDs at a higher drive current capacity.”

The improved wall plug efficiency of 5 percent means that the LED is not only more energy-efficient and generates less heat, but has a longer lifetime. The CrayoLED has a L70, TM-21 extrapolated lifetime of more than 10,000 hours at 350 mA, a defining industry required standard.

The CrayoLED would have an effective lifespan of up to 5-10 years in commercial and residential point-of-use and point-of-entry water disinfection systems. These systems typically use UV-C LEDs for several minutes per operation cycle, for a total annual usage of approximately 1,000-2,000 hours. The CrayoLED provides a reliable and long-lasting solution for water disinfection.

The long lifetime and high-power output of 100 mW reduce the need for frequent replacement, facilitating the adoption of UVC LED disinfection in municipal water treatment facilities. These facilities require reliable and powerful solutions to handle higher water flows and reduce maintenance needs. The combination of the CrayoLED’s UVC LED longevity and performance makes it an efficient and effective solution for water treatment applications.

CrayoLED H-series (CLH-N3S) is available in both sample quantities and in stock for volume production.



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5G: Good for GaAs

Following a flatlining of revenue for RF front-ends, sales are tipped to climb over the next five years, a trend that will support the growth of the GaAs industry

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

RIGHT NOW, the titans of the GaAs microelectronic industry are going through a tricky time. Take US industry stalwart Qorvo: its latest quarterly sales are just $743 million, down from $1.1 billion for the equivalent quarter of the previous financial year. It's a similar story for Skyworks – its latest quarterly sales came in at $1.3 billion, down almost $200 million year-over-year.

However, while the sales of these makers of GaAs power amplifiers are struggling in the short term, due to a combination of rampant inflation, geo-political tensions and inventory corrections – all are having an impact on the sales and supply chain for smartphones – the longer term prospects are actually very good, according to Yole Intelligence. The French analyst is forecasting that sales for the RF front-end – the unit in the handset that combines GaAs power amplifiers with RF filters, switches and low-noise amplifiers made from other technologies – will climb to $26.9 billion in 2028. That's a compound annual growth rate of 5.8 percent over the 2022 to 2028 timeframe.

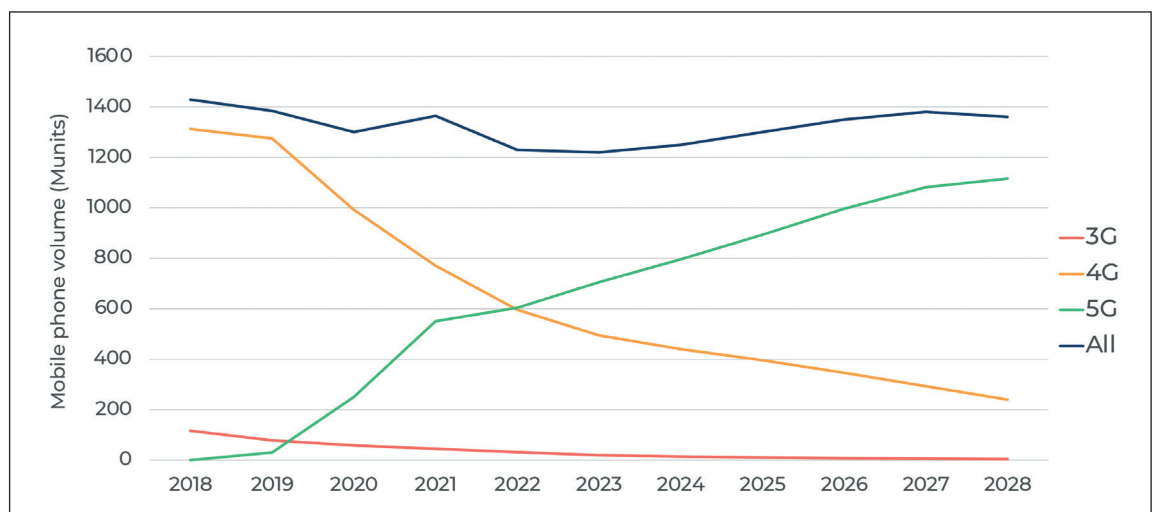
While the proportion of this total annual revenue that can be attributed to GaAs is not given – in recent times it has little meaning, given that the makers of handsets buy front-end modules rather than power amplifiers – there's no doubt that rising sales of the RF front-end will ensure an increase in activity for all those involved with the GaAs RF sector.

In the RF front-end market five big players account for around 80 percent of total revenue: Qorvo, Skyworks, Murata, Qualcomm and Broadcom. These firms employ a range of approaches for production, with Qorvo and Skyworks making GaAs power amplifiers internally for their own RF front-ends, while Qualcomm and Broadcom adopt fabless models.

Of the five, Broadcom is currently enjoying the most success, with its market share rising from 18 percent to 20 percent from 2021 to 2022. With this progress, it has leapfrogged Qualcomm to take pole position.

Cédric Malaquin, Team Lead Analyst of RF activity with the Power & Wireless Division at Yole Intelligence, part of Yole Group, attributes Broadcom's recent success to its strength in producing mid-band power amplifier modules. The company has taken complexity to a new high, with modules incorporating 30 or so die.

"Broadcom is scaling up the complexity while shrinking the overall package footprint. This is what really matters to the end customer, and this is how they maintain their leadership position."



➤ According to Yole, revenues associated with the RF front-end will climb throughout this decade, driven by sub-7 GHz 5G technology.

The big five have been fighting it out in a market that continues to ebb and flow. The pandemic pushed down the number of handset sales, which recovered in 2021, before dropping more recently, due to a number of factors that include chip shortages, inflation, the war in Ukraine and tension between China and Taiwan.

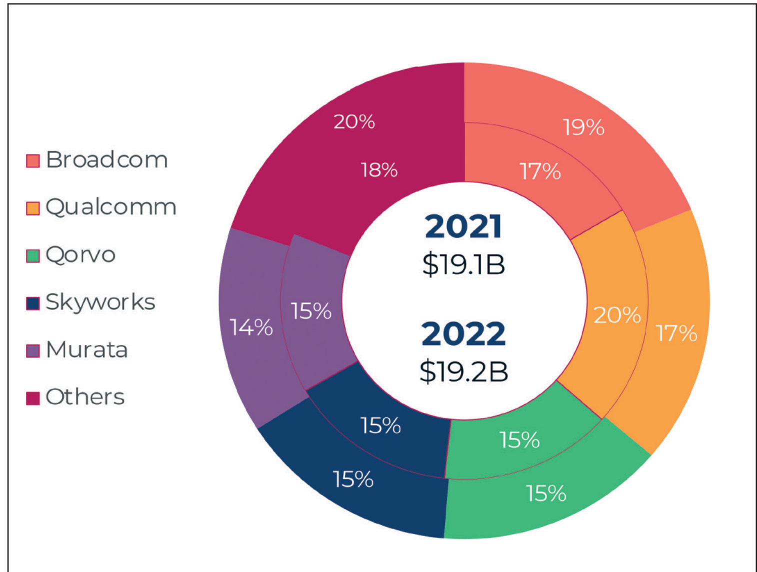
Despite the recent downturn in handset sales, Yole doesn't think there has been a fall in revenue in the RF front-end market. "It has increased, with 5G being scaled up," argues Malaquin.

During recent turbulence in this sector, makers of RF front-ends have adjusted their production plans and worked through their inventory. "We believe there are maybe two more quarters of adjustment moving forward, and then the situation will get back to normal."

Many owners of smartphones do not have a compelling reason to upgrade to a model that offers 5G connectivity. "It's not like you have twice the speed of 4G," points out Malaquin. However, the latest versions from the leading brands are equipped with this feature; and that, in itself, is good news for the GaAs microelectronics industry.

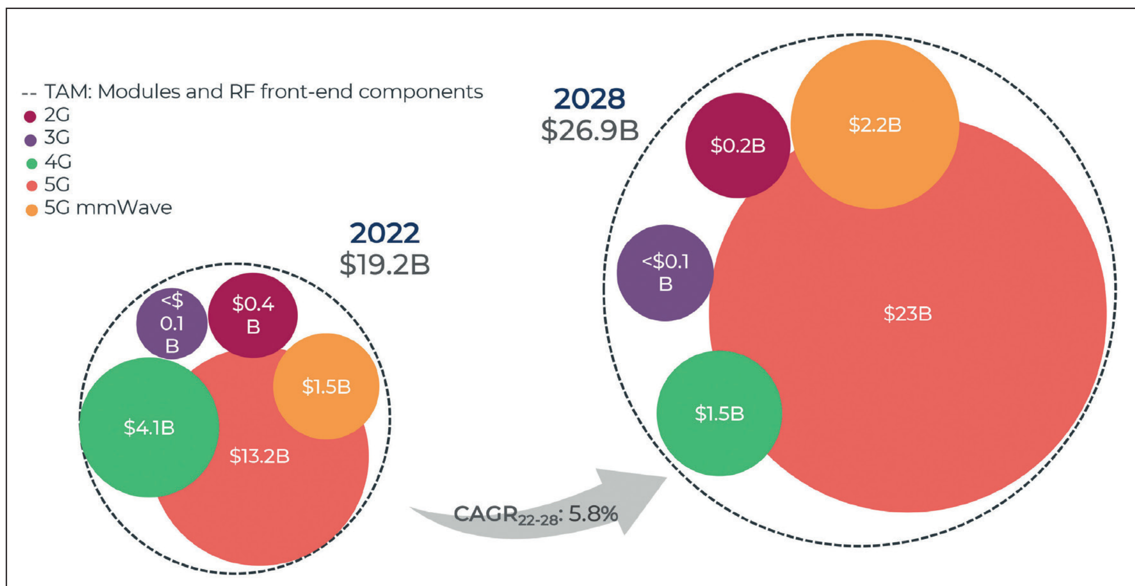
For power amplification below 7 GHz, known as the sub-millimetre form of 5G, GaAs offers the best trade-off between performance, cost and form factor, according to Malaquin. "It's also a very mature technology. We don't see it moving away from the smartphone."

However, Malaquin is not tipping GaAs to play a role in amplifying 5G signals at millimetre-wave frequencies. He says that at the moment, when designers consider the requirement for amplification in this higher-frequency domain, efficiency is not their primary concern. Instead, their focus is on integration and a small form factor, because this amplifier is not turned on all the time. "It's just turning on when it needs to communicate with the base station," explains Malaquin. Note that in many countries, the 5G roll-out does not include mm-wave coverage. It is present in the likes of the US and Japan, but even there it is only available in some dense urban areas.

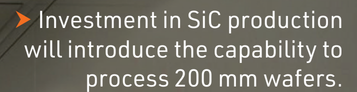


➤ Yole has determined that of the big-five suppliers of RF front-end modules, Broadcom is currently enjoying the greatest success.

Due to the limited access to millimetre-wave 5G, throughout this decade the growth in sales of RF front-ends will be driven by a ramp in the variant of 5G that does not feature this capability. Between 2022 and 2028 Yole is forecasting that sales of RF front-end components and modules associated with 5G millimetre-wave will grow from $1.5 billion to $2.2 billion, while the other form of 5G will increase from $13.2 billion to $23 billion. Given these figures, it seems that throughout this decade and beyond, GaAs is sure to retain its position as the key technology for power amplifiers in smartphones.



➤ Yole is forecasting substantial growth in the sales of smartphones with 5G technology throughout this decade.



Investment in SiC production will introduce the capability to process 200 mm wafers.

SiC production to soar at Microchip

An $880 million investment at Microchip's Colorado Springs campus will create a 200 mm line for producing SiC diodes, MOSFETs and modules

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

RIGHT NOW, barely a month or so goes by without another major maker of power electronics unveiling plans to ramp SiC capacity. Arguably the chipmaker that's been attracting the most attention in this regard is Wolfspeed, which is devoting $6.5 billion to expand production, with efforts including the construction of new fabs in the US and Switzerland and a massive expansion of its crystal growth facility in North Carolina. Others moving in a similar direction include: onsemi, which is investing $300 million to expanding capacity at its fab in Roznov, Czech Republic; and Microchip, which this February revealed that it would be spending $880 million on its Colorado Springs facility, to increase SiC and silicon capacity.

Offering an incredibly diverse product portfolio that includes SiC diodes, MOSFETs and modules, Microchip has a pedigree in SiC that dates back 20 years. Its technology comes via an acquisition of Microsemi, which got its hands on this class wide bandgap power electronics when it bought Advanced Power Technology, a company that launched SiC products in 2003.

Microchip combines internal and external capacity to ensure supply chain redundancy. In the US, Microchip's dual-fab strategy uses an internal and external fab for SiC production, with SiC epiwafers processed into a variety of devices.

At Microchip's Colorado Springs campus, scaling of production and efficiency is continuous, according to Clayton Pillion, Vice President of the company's SiC Business Unit. When asked whether SiC production is at full capacity, Pillion responded by saying that this is a moving target. "It's a hard concept for people to believe, because it's either full or it's not in most people's minds. From our perspective, we continue to scale."

Helping to increase this capability is an increase in external capacity, which, despite market constraints, is delivering small expansions. Microchip is not disclosing its split between SiC and silicon in its $880 million investment that will be spent on facility, equipment and hiring. However, even if this chipmaker were more forthcoming, it would still be unable to provide a definitive figure. "Some of the equipment and some of the labour that goes with that is fungible between the two technologies," says Pillion.

Expansion of the Colorado Springs facility is supported by state and local incentives, totalling around $47 million, as well as the CHIPS and Science Act. Microchip is a valuable asset to national security – although it's not the only maker of SiC chips in US, it has a strong track record in supplying to this country's aerospace and defence markets. Investment at Colorado Springs will create a 200 mm line for SiC. However, Pillion says that the company will only move to this larger format when it's prudent to do so, making manufacture with 150 mm wafers likely for foreseeable future.

To aid expansion of the facility, Microchip is planning to add 400 staff to the 850 currently employed at the Colorado Springs campus. While expertise in SiC is ideal for new hires, it's not going to be a pre-requisite, according to Pillion. "That skill pool [for silicon carbide] is limited in size. You're always working to balance silicon carbide experience with those that have very good engineering basics, who can grow to learn silicon carbide."

With so many chipmakers competing for sales of SiC products, those that are to thrive need to stands out from their peers. Helping Microchip to have an edge over its rivals is the level of robustness of its products, underscored by compelling reliability data. This allows designers to reduce the level of chip redundancy, and ultimately trim costs.

➤ The Colorado Springs facility has existed for many years. In 1989 Honeywell sold this to Atmel, which was acquired by today's owners, Microchip, in 2016.

Another asset of Microchip is the level of support it offers its customers. "We never say 'Here's your product. Go away'. That's not in our DNA," says Pillion. Instead, Microchip supports its customers, drawing on its expertise to help develop designs at the system level. To illustrate this point, Pillion remarked: "We had a visitor to our corporate headquarters two days ago. They were asking us to sit there and work with them, to help them optimise the performance and the balance of the design – total system cost versus performance – and work through some experiments."

One of Microchip's goals is to expand its sales beyond the aerospace and defence markets, where it has enjoyed success for many years.

"In January I took over the group, and we are now focused on driving into a broader industrial and commercial space," reveals Pillion, who says that the company is starting to target some automotive applications. "We prefer a more diversified market, much like we do with our core business at Microchip. Our embedded business is highly, highly diversified, and that's the approach we're taking for silicon carbide."

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Taking Ga_2O_3 to the next level

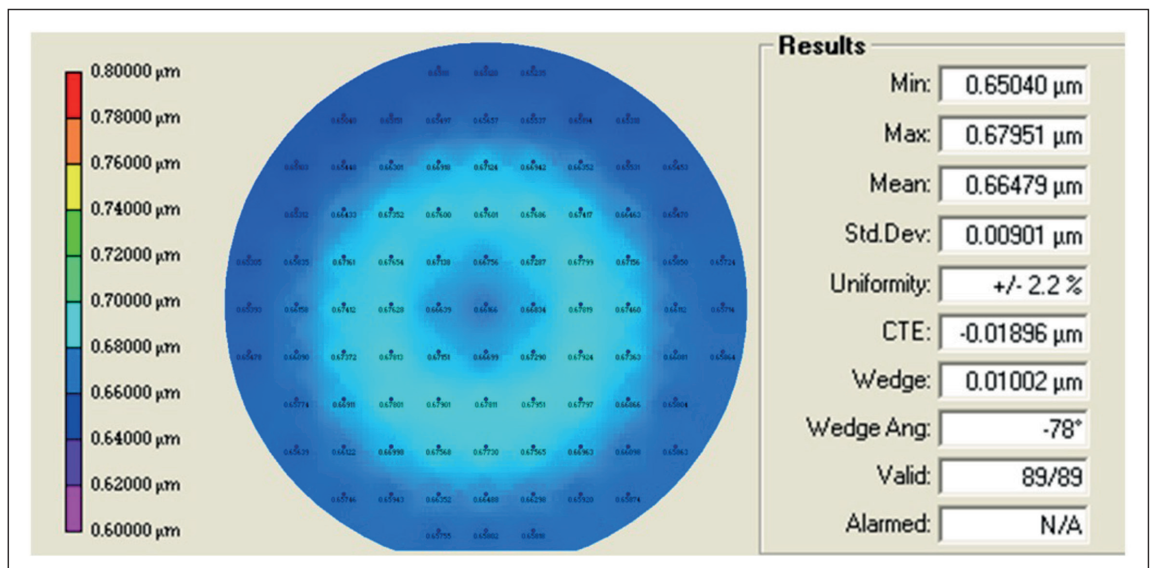
Agnitron's MOCVD reactors are underpinning tremendous advances in the material quality of Ga_2O_3, as well as leaps in the performance of various power devices made from this ultra-wide bandgap semiconductor

BY FIKADU ALEMA, AARON FINE AND ANDREI OSINSKY FROM AGNITRON, ARKKA BHATTACHARYYA AND SRIRAM KRISHNAMOORTHY FROM UCSB, AND CAMERON GORSAK AND HARI P. NAIR FROM CORNELL UNIVERSITY

ON THE BACK OF continuous rapid strides, Ga_2O_3 devices are poised to shape the future of the power semiconductor market. This ultra-wide bandgap material has all the key characteristics necessary to produce better devices and, at the same time, the potential for cost-competitiveness, thanks to the capability to make high-quality melt-grown bulk substrates.

It is now a decade since device and materials research into Ga_2O_3 began in earnest. Over that time tremendous progress has been made, in terms of both the quality of the epitaxial material and the performance of Ga_2O_3 diodes and transistors. Recent reports include β-Ga_2O_3-based devices with a breakdown voltage over 8 kV and critical breakdown fields beyond 5 MV/cm, a regime that exceeds the theoretical limits of SiC and GaN. Such success establishes β-Ga_2O_3 as the most promising candidate for next-generation solid-state power-switching applications.

Now is the time to build on all this progress and deliver further improvement to the quality of β-Ga_2O_3 epitaxial films, as progress on this front will open the door to practical power electronic devices that fully exploit the potential of this oxide. That's the key message at the heart of this feature, which summarises the latest MOCVD process optimisation that has ensured high-quality materials and ultimately high-performance devices. It is clear that when β-Ga_2O_3 is grown by MOCVD using optimal process conditions, the resulting material is of unrivalled quality.



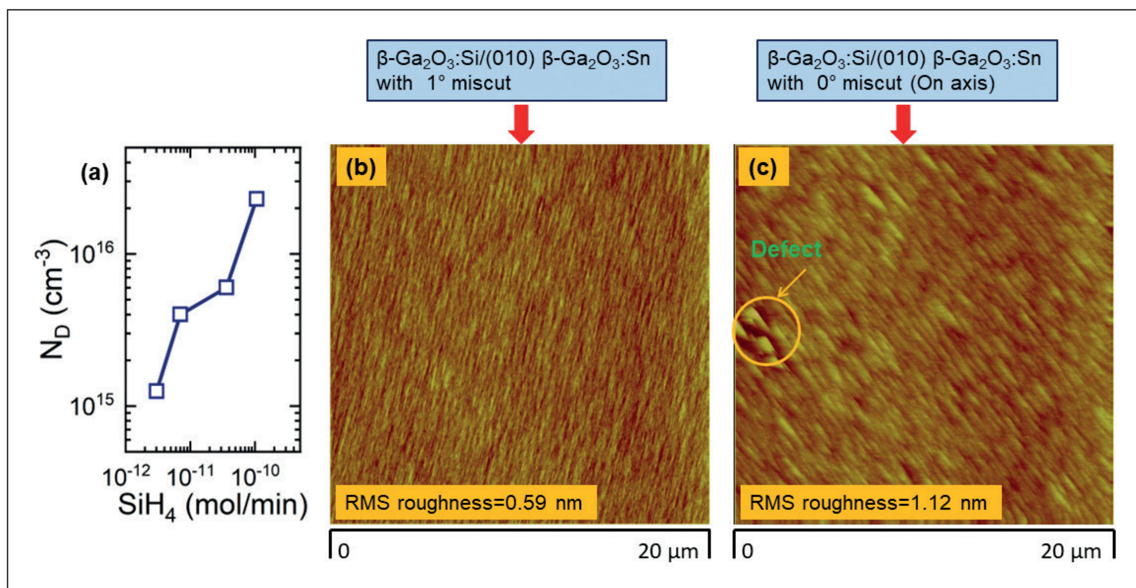
➤ Figure 1. 2D thickness map of a Ga_2O_3 thin film grown on a 50 mm sapphire substrate using the Agnitron Agilis 100 MOCVD reactor. A 2 mm edge exclusion is applied to the map. Film thickness is very uniform, with a non-uniformity of only about 2 percent.

At Agnitron Technology of Chanhassen, MN, we have a well-deserved reputation for being the world's leading provider of MOCVD reactors for the growth of β-Ga_2O_3. One of our most well-known tools, the Agilis, is being used in both our laboratory and in various world-class institutions, including: the University of California, Santa Barbara (UCSB); Cornell University; the US Naval Research laboratory (NRL); Iowa State University, the University of Utah, the Ohio State University (OSU), and Bristol University, UK. Researchers from these institutions are greatly satisfied with the top performances of our reactors and continue to produce ground-breaking material and devices results. Here we highlight the results of Ga_2O_3 grown on our reactors in our laboratory and in the labs of our co-authors at UCSB and Cornell University.

Growing highly uniform films

Thanks to continuous improvements in the supply of large-area Ga_2O_3 substrates, now available in diameters of up to 100 mm, there's a compelling need to be able to grow highly uniform thin films, in terms of both thickness and doping uniformity. While our Agilis 100 MOCVD is primarily intended for R&D, using far smaller substrates, it is capable of accommodating wafers up to 50 mm in diameter. Due to this, it is crucial that this reactor can realise uniform films on wafers of such sizes.

Our Agilis 100 employs a unique remote-injection showerhead design. Oxygen enters the reactor from a single central injector with an inert gas push flow, while the gallium metalorganic source, typically tri-ethyl-gallium, is introduced from the showerhead area that surrounds the central oxygen injector, again with an associated push flow. Merits of this design include laminar flow conditions, and prevention of mixing of the oxygen and metalorganic sources until they reach the substrate, thereby mitigating gas phase reactions and an associated reduction in growth rate. Another advantage of separate



➤ Figure 2. Capacitance-voltage measurements determine the doping concentration dependence of the silane molar flow rate, for the growth of β-Ga_2O_3 films at Agnitron Technology using optimal process conditions (a). 2D atomic force microscopy (AFM) images of 5.1 µm thick layers grown on (010) β-Ga_2O_3 substrates with miscut angles of 1° (b) and 0°, also known as on-axis (c). The features on the film grown on the on-axis substrate are bigger than those for the film on the substrate with miscut angle of 1°.

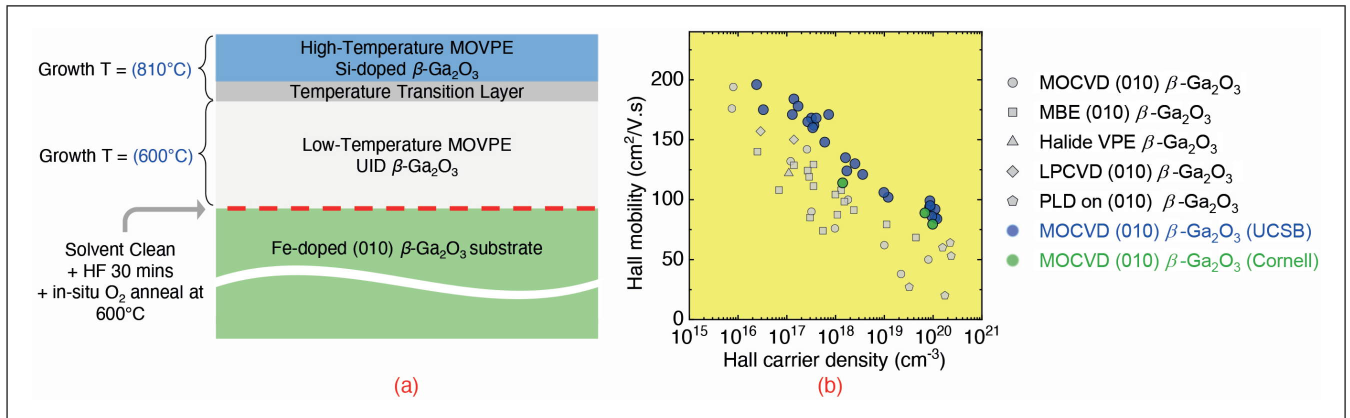


Figure 3. The channel structure used for uniformly and intentionally silicon-doped films for the doping range of 10^{17}–10^{20} cm^{-3}, grown using Agnitron's Agilis 100 (a). Room-temperature Hall mobility of the channel stacks as a function of Hall carrier density, benchmarked with various state-of-the-art reports (b). Effectiveness of the growth steps is confirmed by Cornell University, using the same Agilis 100 reactor. Details of the data in (b) can be found in reference [5].

injection is that it provides an additional knob for fine-tuning the reactor's gas flow profile.

Following installation of our Agilis 100 MOCVD reactor at Cornell University, we worked together to identify process conditions for increasing the uniformity of Ga_2O_3 films on 50 mm substrates. We found that through careful tuning of the flows and the reactor pressure, we could produce Ga_2O_3 films with a thickness non-uniformity of around 2 percent (see Figure 1). To realise the highest uniformity, we combined high total gas flows with low reactor pressures, conditions that are known to mitigate buoyancy associated with flow instabilities [1]. These conditions are conducive to the growth of films with high mobilities and smooth surfaces – measurements have revealed a root-mean-square roughness below 1 nm. The combination of a high carrier mobility and a low surface roughness is essential for the fabrication of high-performance devices over the entire 50 mm substrate.

Another strength of our design of reactor is that thanks to its unique injection system, it is amenable to further modifications. For example, adding a nozzle with a reduced diameter to the central injector increases the velocity of gas flow, and thus ensures a higher growth rate.

Realising low doping

Due to an absence of *p*-type doping, most Ga_2O_3 device architectures are unipolar. This limitation means that there is a need to grow thick epitaxial films with a low doping concentration to realise efficient voltage-blocking power devices. If there is a high doping concentration in the Ga_2O_3 epitaxial layer, which is also known as the drift layer, the depletion region narrows, resulting in a strong electric field at the junction between the metal and Ga_2O_3. This high electric field exerts a substantial force on electrons, propelling them across the junction. In turn, the electrical current through the device increases, leading to a threat of electrical breakdown. Due to these concerns, it is far better to have a low doping concentration in the drift layer. When that's in place, the depletion width increases, reducing the electric field at the junction and thus increasing the breakdown voltage. Note that it's important that the drift layer is thick enough to either match or exceed the depletion width.

We recommend MOCVD for the growth of devices with a thick drift layer, because this technique offers high-speed growth – a rate of around 10 μm/hr is possible – alongside nanometre surface roughness and uniform doping [2]. Last year, in the pages of this publication, we reported that with this growth technology we had demonstrated free-carrier concentrations that range from around 7×10^{15} cm^{-3} and around 2.5×10^{16} cm^{-3}, for unintentionally doped and lightly silicon-doped β-Ga_2O_3 films, respectively. Recent process optimisation has improved these figures, with the realisation of even lower doping concentrations that have a tremendous advantage for vertical power devices. Our latest breakthrough came from film growth at a reduced growth pressure of less than 20 Torr, which drives down gas phase reactions and lowers defects and inclusions in the film.

Capacitance-voltage measurements (see Figure 2 (a)) on our epitaxial films unveiled the relationship between their doping concentration and the molar flow rate for silane (SiH_4/N_2). This study showed that the doping concentration varied linearly with silane molar flow rate, as expected. However, the key breakthrough is that when we dialed the silane molar flow rate down to around 3×10^{-12} mol/min, the doping concentration in the film fell to around 1.5×10^{15} cm^{-3}.

Miscut merits

One of the big challenges with vertical power devices grown using MOCVD is that the growth of the thick, low-doped drift layer can lead to the formation of macro defects, with hillocks, particles,

and pits forming on the film's surface. The drift layer may need to have a thickness of tens of microns, but after around 3 μm of growth its surface is hampered by the defects just described, leading to a high surface roughness of more than 5 nm. Compounding matters, as film thickness increases, the defects get larger and more abundant.

Multiple origins are to blame for the surface defects in these epilayers. They can be traced back to the substrate, the growth process conditions and the substrate preparation methods. For example, researchers from the University of Utah that are using our Agnitron reactor recently observed the propagation of line defects, such as nanopipes, into the epitaxial layers out of the substrates [4]. Left unmanaged, these defects will degrade film quality and account for the premature breakdown of devices.

The issues seen in MOCVD growth are also present in films formed by halide vapor phase epitaxy (HVPE), an alternative approach for growing thick layers of β-Ga_2O_3. When growing Ga_2O_3 by HVPE, there's a need to smooth the extremely rough epitaxial layers with chemical-mechanical polishing. However, this post-growth polishing hampers efforts to realise sharp doping profiles and abrupt heterointerfaces, not to mention the challenge with the lateral doping inhomogeneity to begin with. With MOCVD, it's possible to minimise surface defects by optimising the growth process and using a suitable substrate with a few degrees miscut.

We have investigated the influence of low-pressure optimal process conditions on the surface quality of thick β-Ga_2O_3 films. Using the process conditions for a doping concentration of low 10^{15} cm^{-3}, we grew a 5.1 μm-thick lightly doped β-Ga_2O_3 epitaxial layers on two (010)-oriented tin-doped substrates. Co-loaded into the reactor, this pair of substrates had different orientations: one was a regular on-axis substrate, and the other had a 1° miscut.

Inspecting these films revealed that the surface quality improved with optimal process conditions (see Figures 2 (b) and 2 (c), showing atomic force microcopy images of 20 μm by 20 μm scan areas). The epilayers on both substrates have a smooth surface, but the value for the root-mean-square roughness is lower for that with a miscut foundation, at just 0.59 nm.

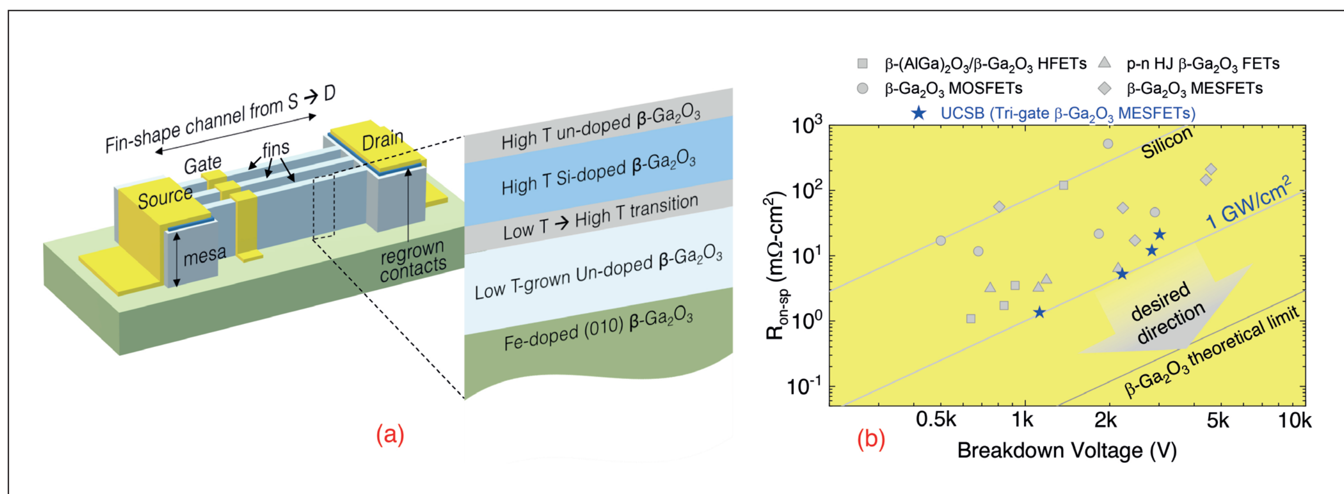
One of the key benefits of a low growth pressure is that it minimises the gas phase reaction in the chamber, thereby reducing the formation of particles that can land on the substrate and act as a seed for the nucleation of defects. The upshot is a trimming of the defect density in the epilayers.

Combining this low growth pressure with a substrate with a few degrees of miscut leads to further gains, in terms of the surface quality of the films. Thanks to the introduction of terraced surfaces, in the miscut wafers, there is the potential to enhance diffusion of gallium adatoms on the substrate's surface during the growth process.

Our initial studies have identified the importance of investigating whether β-Ga_2O_3 substrates with higher miscut angles can lead to a further reduction in surface defects on thick films. Our plan is to study (010) β-Ga_2O_3 substrates with miscut angles between 2° and 4°.

Enhancing channel mobility

A very active area of β-Ga_2O_3 material research is associated with attempts to increase the channel mobility in β-Ga_2O_3 epitaxial films. A higher channel mobility is a prized asset, essential to realising a low on-resistance that leads to low conduction and switching losses in devices, and ultimately to ensuring minimal energy waste in power circuits. Working at UCSB, Sriram Krishnamoorthy's team have been using an Agilis 100 reactor to carefully tune MOCVD processes and enhance the electron



➤ Figure 4. The tri-gate β-Ga_2O_3 MESFETs (with a SiN_x wrap-around passivation not shown) feature a high-mobility channel stack with low-temperature buffer layers (a). (b) Benchmark plot of the differential specific on-resistance as a function of blocking voltage for tri-gate β-Ga_2O_3 MESFETs, with literature reports showing record transistor performance [6].

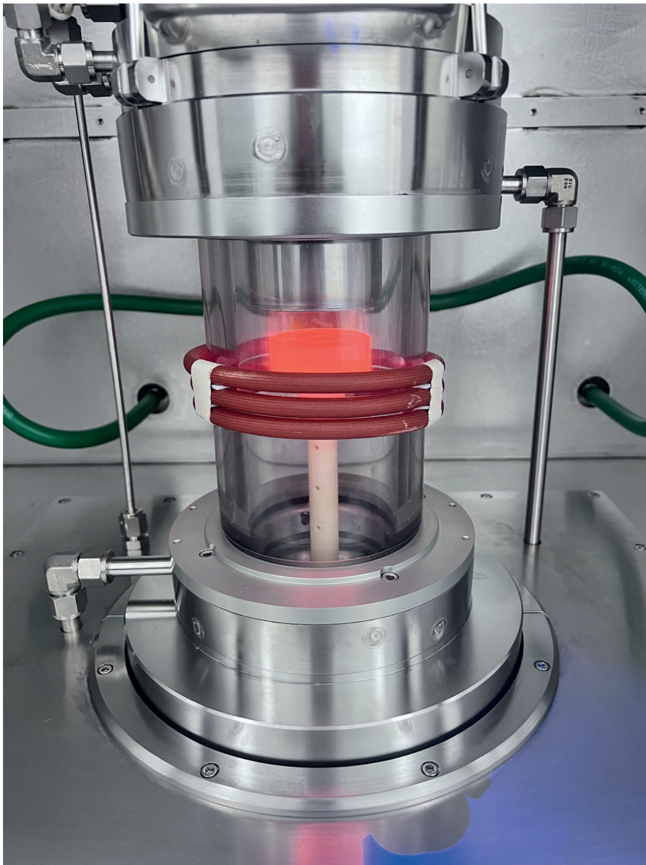


Figure 5. The Agnitron Agilis 100 and Mini MOCVD systems offer maximum flexibility with their ability to feature both remote injection and close injection showerhead flanges, enabling users to quickly and easily switch between the two options to optimise their processes. Furthermore, the close injection showerhead flanges are designed with multiple preset distances from the wafer to increase experiment flexibility. The blue light is for optical reflectometer for *in-situ* monitoring of the films growth rate.

Agilis 100 reactor with UV light source exposure

mobility of films with a wide range of doping concentrations [5]. These efforts have included the development of a substrate cleaning process involving hydrofluoric acid, and the introduction of a hybrid channel structure with low-temperature buffer layers. The latter led to record-breaking electron mobility for both uniformly silicon-doped (3D doped) and δ-doped (2D doped) Ga_2O_3 epitaxial films grown on (010) iron-doped bulk substrates. For substrate cleaning, the team started with solvent cleaning, followed by treatment for 30 minutes in HF (49 percent in water) and then *in-situ* oxygen annealing in the MOCVD reactor prior to epilayer growth. This procedure produced an atomically smooth surface and compensated for any undesired low-mobility electron channel at the interface between the epitaxial layer and the substrate.

To produce the channel structure, those at UCSB modulated the epitaxy growth temperature from 600 °C, used for growth of the un-doped Ga_2O_3 buffer layer and then the transition layers, to 810 °C for the silicon-doped Ga_2O_3 channel layers (see Figure 3 (a)). Note there was no growth interruption. For doping ranging from 2×10^{16} to 1×10^{20} cm^{-3}, this structure provided room-temperature Hall mobilities of 196 - 85 $cm^2 V^{-1} s^{-1}$ – that's an enhancement in electron mobility of around 30-50 percent over this

doping range (see Figure 3 (b)). At Cornell University comparable results for mobility have been reported using similar process conditions, again using the Agilis 100 system (see Figure 3 (b)). Taken together, these very promising results from two world-class universities champion the versatility of our reactor, and highlight its capability to break new ground, in terms of both epitaxy and device development. The team at UCSB have also produced δ-doped channels with sheet charge of 9.1×10^{12} cm^{-2} that provided a mobility of 110 cm^{2} V^{-1}s^{-1}.

Lateral devices

Lateral transistors that utilise these uniformly silicon-doped channels with low-temperature buffers exhibit state-of-the-art performance (see Figure 4(a)). These devices produce a very low reverse leakage for breakdown voltages up to 3 kV. What's more, thanks to enhanced electron mobility, they exhibit low on-state resistances. Combining these virtues with effective electric-field management leads to a figure of merit for power as high as around 1 GW cm^{-2}, a new record for Ga_2O_3 transistor device technology (see Figure 4 (b)) [6].

In addition to this progress in lateral transistors, there have been significant, recent advances in lateral diodes based on materials grown using the Agilis 100 reactor. Those at UCSB have fabricated a novel lateral β-Ga_2O_3 Schottky barrier diode featuring a high permittivity dielectric superjunction structure, leading to a breakdown voltage of −1487 V. The performance of this diode makes it an attractive candidate for low-to-medium voltage applications that require lower conduction losses. Normalizing to the active current-conducting area yielded a power figure-of-merit of 2.7 GW cm^{-2} – that's higher than the SiC's unipolar power figure of merit [7]. While this high value comes from the superjunction effect, with the strength of the electric field inside the lateral drift region reduced through the distribution of the depletion region over the entire length of the diode, it is the MOCVD grown material that makes this possible.

15 Years of MOCVD

The common thread that links all the great results just discussed is that they have been obtained using Agnitron's MOCVD tools. Agnitron this year will be celebrating 15 years of innovation and cutting-edge technology.

By continuing to develop Agnitron's systems for MOCVD of β-Ga_2O_3, Agnitron has enabled them to become more efficient and cost-effective while still providing reliable results. The great versatility of the Agilis 100 explains why it is the most featured and referenced growth tool in this article. Note that its versatility actually makes it a compelling candidate for a wide range of experiments beyond β-Ga_2O_3.

At the heart of all of Agnitron's tools is a proprietary vertical growth chamber that features a high-speed rotating disc reactor (RDR), capable of operating at over 1300 revolutions per minute. Agnitron

Testimonials for Agnitron Technology

Hari P. Nair, Cornell University

"Agnitron's Agilis 100 MOCVD system was installed in my lab in the summer of 2022. Within a span of two days, we were able to demonstrate all the material's quality specs needed for the acceptance of the system and achieve high-quality gallium oxide epitaxial films on par with other leading gallium oxide research groups around the country, which by the way, were also grown using Agilis 100 MOCVD systems. This is a testament of the consistent high performance of the Agilis platform. The Agnitron team provides excellent support to their customers. They are very committed to ensuring that their customers get the best out of their systems. They promptly respond to questions that arise, be it related to growth parameters or general troubleshooting."

Sriram Krishnamoorthy, Materials Department, UCSB

"I started out my research group at The University of Utah and ordered one of the first Agnitron Agilis 100 MOCVD systems, after taking notice of the early research breakthroughs from the in-house gallium oxide epitaxy research at Agnitron. This platform enabled us to make rapid strides in demonstration of impressive material quality and the associated device performance, within such a short time frame. When my research group moved to UCSB, it became an obvious choice to double down on the Agilis 100 system and we are currently installing it. I'm beyond excited to see where this takes us. I have ordered a brand new MOCVD system from Agnitron with two different showerhead geometries to capitalise on the enormous possibilities enabled by the Agnitron MOCVD platform and the system will be installed soon in UCSB's Institute of Energy Efficiency (IEE) building, Henley Hall."

Michael A Scarpulla, University of Utah

"Agnitron has been a remarkable equipment supplier and material and process development partner for the University of Utah. From the planning phase for acquiring our Agilis reactor to more recent collaboration on growing layers designed for specific studies of point defects, Agnitron's staff have always been in open communication and working together to get the best performance. I'm impressed that they not only supply good machines, but have also been setting records in terms of material quality too. They have also worked through equipment challenges and collaborated with us on developing the procedures for optimal epitaxial growth. Agnitron is a superb equipment supplier but also R&D partner – this is a rarity in my more than 20 year research career."

Houqiang Fu, Arizona State University

"Agnitron is a top supplier of MOCVD reactors for various materials systems. They capitalise on their R&D laboratory to demonstrate record-performance materials on similar tools that they sell. While at Iowa State University, I bought an Agnitron Agilis 100 oxide reactor; I've now moved to ASU, and it was an easy decision to utilize Agnitron again. In fact, my ASU colleague (Dr. Nidhin Kurian Kalarickal) and I have purchased two Agnitron Agilis tools. An Agilis-100 for oxides and an Agilis-mini for high-temperature nitrides. Agnitron has been great to work with from start to finish. They support everything from pre-delivery facility preparation to troubleshooting issues after delivery. Their staff are patient and responsive, always helping us solve problems and optimise growth recipes. One of their strengths is the willingness to customise reactors for unique research needs."

Agnitron has developed a patent-pending technology that upgrades the close-injection gas distribution system, ensuring oxygen injection across the entire wafer carrier, rather than just centrally. This system, in combination with Agnitron's RDR fast rotation, leads to superior thickness and doping uniformity of epitaxial layers.

minimises the chances that any deposition within the chamber reaches the wafer surface through material science and design engineering. The high-speed RDR's unique flow dynamics repress particle recirculation, leaving areas above the wafer clean and free of deposition. Another virtue of the high-speed rotation of Agnitron's RDR is that it allows a higher degree of control, ensuring superior thickness distribution uniformity.

The Agilis 100 reactor, developed by Agnitron, is equipped with optical reflectometry in the UV and blue range, enabling users to determine film growth rate and thickness in real-time. This hardware is fully integrated into the Imperium analytical control software. To control the purity of Ga_2O_3 epitaxial films, Agnitron added the capability to expose a UV light directly on the wafer during the growth process. This method enables management of point defects and further reduces any residual carbon that can incorporate into Ga_2O_3 films during the MOCVD process. The method is proven effective in MOCVD of GaN, as has been extensively explored by researchers at North Carolina State University [8].

Agnitron had previously demonstrated high purity β-Ga_2O_3 films with a record low-temperature electron mobility of more than 23,000 $cm^2\ V^{-1}\ s^{-1}$ and acceptor concentration of 2×10^{13} cm^{-3} using one of its Agilis reactors [9]. This was achieved by mitigating the carbon incorporation into the films through process conditions. But, with the current UV exposure capability, we believe that a far purer material with robust process reproducibility can be achieved.

Agnitron's MOCVD systems, especially the Agilis 100, are highly flexible, allowing operators to switch between various sources by adding a few hardware components. Moreover, within two hours of maintenance, regardless of the source selected, users can change the gas distribution configuration between remote and close-injection delivery. This option provides researchers with the convenience to experiment and enhance their processes effortlessly. Additionally, extra nozzles can be attached to the gas distribution flanges, which can be used to refine the process or clean the wafer carrier. This range of desirable features makes Agnitron's reactors an attractive alternative for various applications.

To address the high cost of wafers and gas consumption in R&D, there is a need to grow on a single large-area wafer. Agnitron's β-Ga_2O_3 MOCVD reactors, specifically the Agilis 500/700, can now accommodate wafers up to 100 mm and 160 mm in diameter, respectively. These larger multi-wafer reactors maintain the same footprint as the Agilis 100 and were responsible for some of the results in this article. This expansion provides excellent capability for scientists interested in growing larger diameter wafers for a matching fab line.

Agnitron will soon expand its oxide portfolio with the GOX 300, a fully automated production Ga_2O_3 MOCVD system offering further capabilities for larger wafers. Additionally, the company added the Agilis Mini to its range. This reactor is equipped with the same capabilities as the Agilis 100, but with a smaller footprint and a more cost-effective price.

Agnitron has developed a patent-pending technology that upgrades the close-injection gas distribution system, ensuring oxygen injection across the entire wafer carrier, rather than just centrally. This system, in combination with Agnitron's RDR fast rotation, leads to superior thickness and doping uniformity of epitaxial layers.

Agnitron's hardware engineering department continues to make improvements and advancements to its MOCVD tools, ensuring that each new generation of reactor provides greater reliability and versatility for process engineers. These breakthroughs pave the way for future advancements in high-voltage power devices.

Equipment and process development results discussed in this article were partly funded by the Office of Naval Research (ONR) through the STTR Phase II program, contract number N6833518C0192, under the direction of Mr. Lynn Peterson, and Air Force's AFWERX SBIR Phase I program, Contract Number: FA8649-21-P-0304.

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Component viability risks bursting the quantum bubble

To speed the arrival of quantum technologies, the incredibly demanding compound semiconductor devices that lie at the heart of them need to be produced on high-volume platforms

BY DENISE POWELL AND WYN MEREDITH FROM THE COMPOUND SEMICONDUCTOR CENTRE, SAMUEL SHUTTS FROM CARDIFF UNIVERSITY, MOHAMED MISSOUS FROM THE INTEGRATED COMPOUND SEMICONDUCTORS, MOHSIN HAJI FROM THE NATIONAL PHYSICAL LABORATORY AND CHRIS MEADOWS FROM CSCONNECTED

THERE IS no doubt that quantum technologies have the potential to revolutionise every sector we can think of. Their impact will include: highly accurate navigation, enabled by quantum gyroscopes; GNSS-free communications, underpinned by atomic clocks; ultra-secure communications, via quantum key distribution; improved manufacturing control and timely maintenance on infrastructure; the detection of anomalies in organs such as the brain and heart, through quantum magnetometers, alongside rapid drug and materials discovery; and financial modelling, enabled by quantum computers.

The possibilities for quantum technologies are so vast that this revolution is anticipated to be on a par with that of AI, in terms of scale. In fact, these two headline-grabbing technologies are complementary, with the true magic underway when quantum systems are enabled by AI. This is not just fantasy:

AI is already applied to data from quantum systems at the UK's National Physical Laboratory to ensure rapid analysis.

Unfortunately, for any nascent technology, promise is no guarantee of success. History attests that when a technology with great potential delivers encouraging results, substantial investment follows – but this optimism may well be short lived, with the bubbles breaking to induce a widespread cull that leaves those hanging under the spotlight having trying to salvage a future for their revolutionary technology. Today some firms are still recovering from the lidar aftermath, and reports suggest AI is next for re-evaluation.

And what of quantum? Why aren't we seeing widespread deployment of this technology, on the back of investment totalling hundreds of millions of dollars? You might be thinking that the humble laser draws on quantum effects, so quantum is already well-embedded in our lives. That's somewhat true, but misses the point that here we are considering what most refer to as 'Quantum 2.0' – that is, technologies that utilise superposition or entanglement, or as Einstein famously said, "spooky action at a distance".

To delve deeper into the future of quantum, it's helpful to consider an example. One highly successful Quantum 2.0 product is the world's first commercially available chip-scale atomic clock, Microchip's Microsemi SA.45s CSAC. According to the National Institute of Standards (NIST), this triumph is the culmination of more than 10 years of extensive R&D, costing several tens of millions of dollars, with support from both the Defence Advanced Research Project Agency (DARPA) and NIST. John Kitching, a key researcher at NIST involved in this development, rightly suggests that given that the market for chip-scale atomic clocks is worth around $200 million per annum, it's difficult for industry to invest the amount needed for fundamental R&D in this area.

VCSELs: a hero in the making

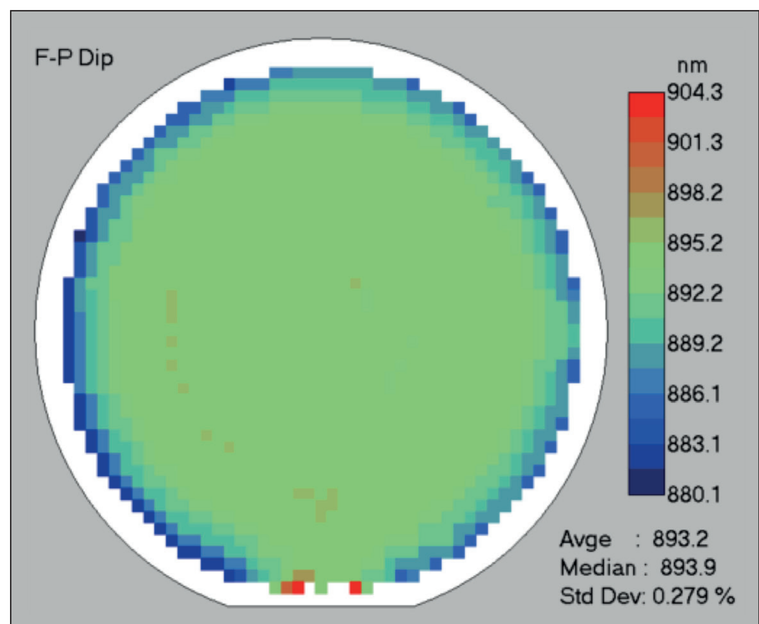
A key component in miniature atomic clocks, as well as other quantum systems based on alkali metal vapour, is the VCSEL. Renowned for its low power operation, circular beam profile and intrinsic reliability characteristics, this class of laser is ideal for interrogating the alkali metal atomic species, typically rubidium or caesium, that are contained in a small cell within the atomic clock. As the clock's principle of operation is coherent population trapping, the VCSEL must emit at highly precise wavelengths corresponding to atomic energy transitions. For example, the emission must coincide with D1 transitions at elevated temperatures, which occur at 795 nm and 894.6 nm for rubidium and caesium, respectively.

In addition to these highly stringent wavelength requirements, there are many other specifications that must be met, including single-mode operation with a narrow linewidth and high mode stability. Fulfilling them all is not easy, as in some cases adhering to one narrow tolerance makes it harder to meet the demands of another. Given this state of affairs, it's no surprise that it's not a stroll in the park to realise the high levels of epitaxial material design, growth and fabrication demanded for VCSELs deployed in quantum technologies.

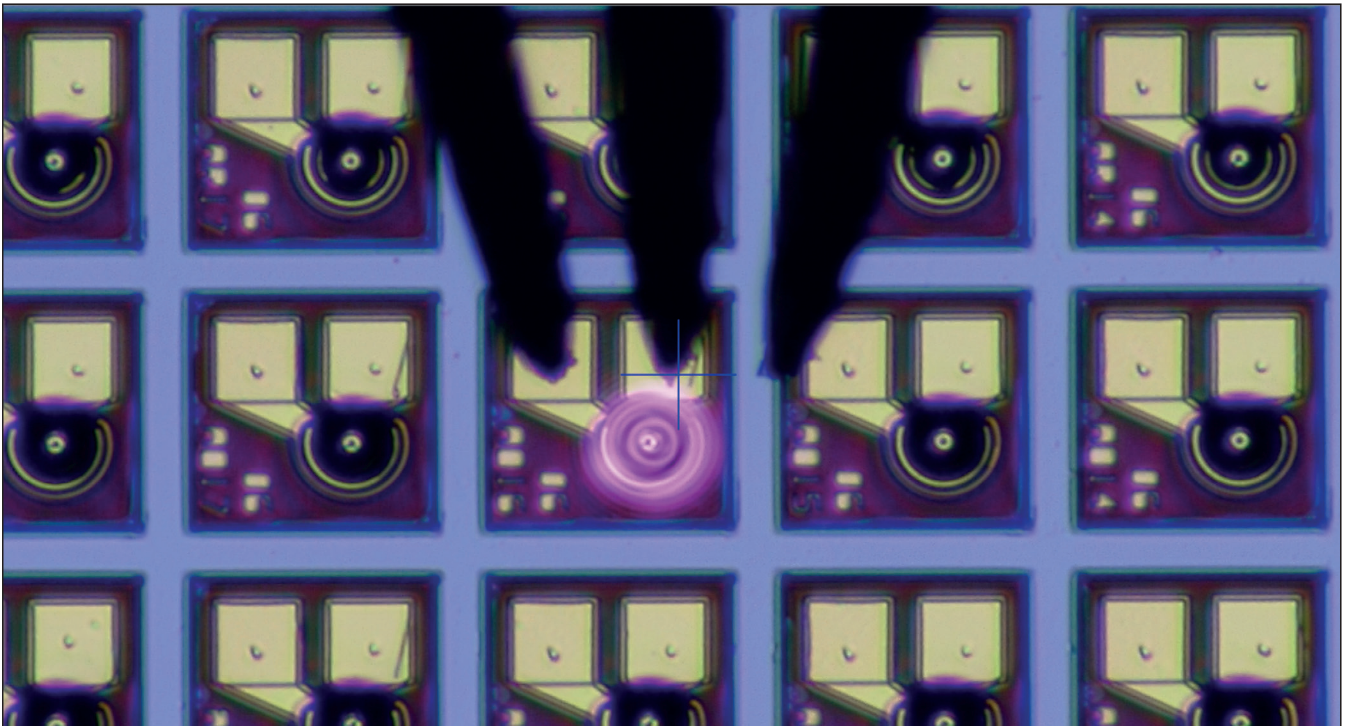
To illustrate this point, when VCSELs serve in quantum technologies, the ideal uniformity for the Fabry-Pérot dip across a wafer is below 1 nm, with the precise figure depending on the current tuning capability. In stark contrast, telecommunications applications can tolerate a non-uniformity of this parameter of several nanometres across a wafer.

There is significant effort in the UK to develop VCSEL technology that is customised to the stringent needs of quantum applications. The Compound Semiconductor Centre (CSC), a joint venture between IQE Plc and Cardiff University, has worked extensively on improving the centre-uniformity profile for 100 mm epiwafers produced with Aixtron series G3/4 MOCVD tools. This is the preferred substrate size for the VCSEL design, fabrication and test partner Integrated Compound Semiconductors, of Manchester, UK.

Fabrication is equally challenging, demanding tight control of the oxidation processes to ensure single-mode operation at the required optical output power. Naturally, these process challenges impact yield. Whilst standard VCSEL platforms boast yields typically in excess of 90 percent, those developed specifically for quantum applications are far lower, due to the cumulative effects of stringent specifications.



➤ The Fabry-Pérot profile across a 894.6 nm VCSEL structure grown on a 100 mm GaAs substrate using Aixtron G3 series MOCVD system.

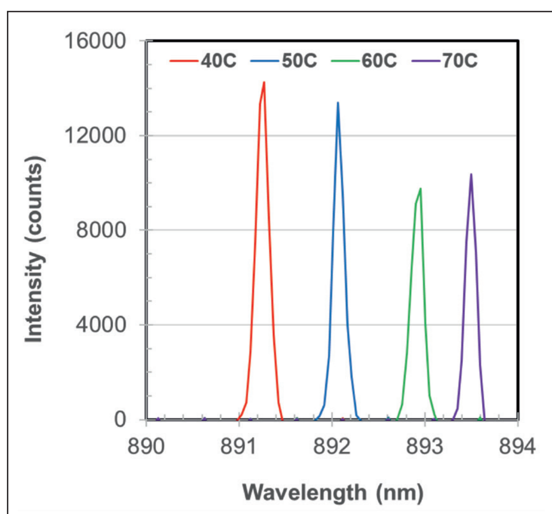


➤ Fabricated VCSEL devices at ICS, Manchester

The hefty price tag on Quantum 2.0

Product pricing depends heavily on manufacturing yields. For VCSELs for consumer applications, many thousands of lasers can come from a 150 mm wafer, with yields typically allowing for a fully processed device to cost up to $5. That's not a feasible price-point for highly customised VCSELs for quantum applications.

VCSELs can also serve in other alkali metal vapour-based quantum systems, such as quantum magnetometers and gyroscopes, where they are again used for coherent population trapping. In all these products, other custom components are also required, such as: wafer cells to contain the alkali metal species; niche optics; crystal oscillators, in the case of atomic clocks; and shielding and/or coils, when fabricating gyroscopes and magnetometers.



➤ Optical spectra of a single mode VCSEL fabricated at ICS, Manchester

Progress is being made on all these fronts. For example, MEMS wafer cell technologies are emerging. However, in addition to efforts at improving yield, a lot of fundamental research and development still needs to be undertaken to understand the effect of process and cell parameters on application performance.

One crucial question plaguing the quantum sector is this: What level of product mark-up is tolerable for end-users, so they don't stick to other, perhaps more proven technologies? And related to this is the question of what is the price-point at which the advantage of Quantum 2.0 is too expensive to justify? It's an unspoken reality that quantum systems will not be widely deployed until critical components are manufactured at accessible costs, unless value at the system level far outweighs the cost. You'll not be surprised to hear that defence and security are often the early adopters for emerging technologies, enabling low-volume production that provides a pipe cleaner step for a subsequent volume ramp.

Upscaling an existing asset base

The issue of manufacturability for quantum is not limited to VCSELs. There are applications requiring single-photon light sources or detectors. Producing these devices is even more challenging than VCSELs, because they are at a lower technology readiness level, having not benefited from years of volume production for non-quantum applications. Viewed in that light, it's not that surprising that miniaturised atomic clocks are one of the first quantum systems to be commercialised. The lack of maturity in the production of some types of devices, along with their high

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Reliability Of Compound Semiconductors Workshop taking place on Monday 15 May 2023 of the CS MANTECH week (15-18 May 2023), in Orlando, FL, will be fully part of the offerings of CS MANTECH (previously ROCS was part of JEDEC). It will run in parallel to the CSMANTECH workshop which in 2023 will focus on "Art of CS Manufacturing: Foundational & Advanced Fabrication Techniques.

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Exhibits

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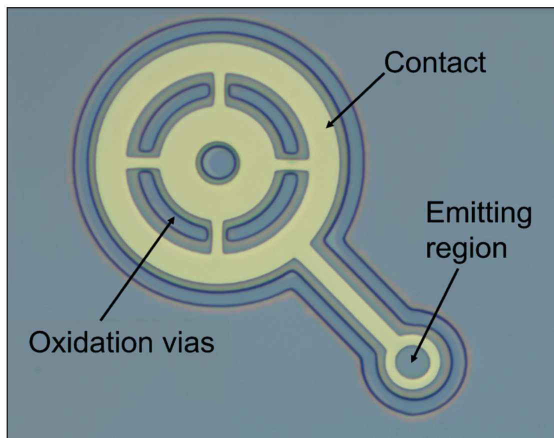
The CS MANTECH exhibits are an excellent opportunity to visit suppliers of materials, services, and equipment from around the world.

Check out the Exhibit Hall to see who will be exhibiting



A Quick Fabrication VCSEL structure produced at Cardiff University.

manufacturing costs, creates a substantial barrier for many quantum industries, including quantum key distribution, quantum sensing and quantum computing. The solution is to manufacture quantum devices alongside other semiconductor processes, and leverage existing assets and infrastructure.

Helping to bridge that gap is a three year, £5.8 million project, part-funded by the UK Quantum Technologies Challenge under UK Research & Innovation (UKRI), that draws on existing assets and infrastructure across 12 partners in the UK.

This venture, the QFoundry project, is establishing a foundry for quantum photonic components and is focused on upscaling manufacturability of these devices and understanding drivers of yield, reproducibility and reliability.

Another contributor to the progress made by CSC is through the CSconnected compound semiconductor cluster in South Wales, that is supported under UKRI Strength in Places programme and is actively involved in establishing UK supply chains for a range of quantum technologies. CSC, which has access to volume MOCVD reactors through IQE, works closely with Cardiff University who have developed a novel Quick Fabrication (QF) VCSEL process to determine the impact of material design changes or growth parameters in less than half the time it would normally take to fabricate full devices.

Those that have read *Move Over MOCVD* (issue V, p. 20, 2022) may wonder why MBE is not the growth method of choice, given its capability to deliver superior uniformity. However, the reason is simple: MBE would cast an additional financial burden on the already high cost for custom design and fabrication of VCSELs for quantum technologies. To ensure the success of quantum, its devices must be made alongside volume platforms and create additional market opportunities for the same wafer platform.

Underscoring the importance of running quantum fabrication alongside standard volume semiconductor processes is the approach taken by the leading developer of quantum computers, PsiQuantum, which has partnered with Global Foundries. According to PsiQuantum, the only path to creating a commercially viable quantum computer is the one that leverages the trillions of dollars invested in the semiconductor industry, which now dates back more than half a century. Through collaboration with Global Foundries, PsiQuantum gains access to high-precision lithography and other high-end toolsets, as well as running design-of-experiments at volume to accelerate development.

It's a sure bet that one day quantum will be a natural part of everyday life. However, getting there involves tackling fabrication challenges, and taking sensible pathways to commercialisation and eventual volume deployment.

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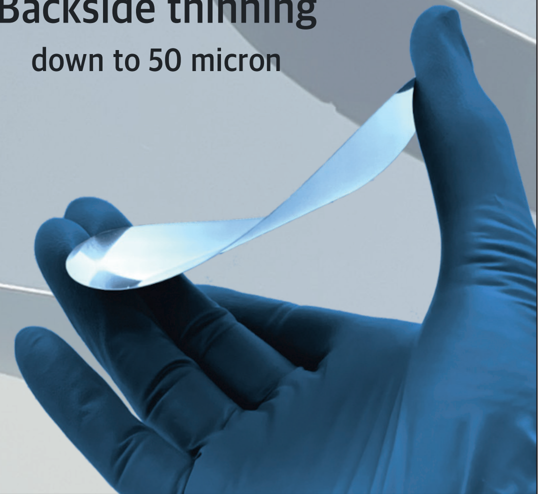

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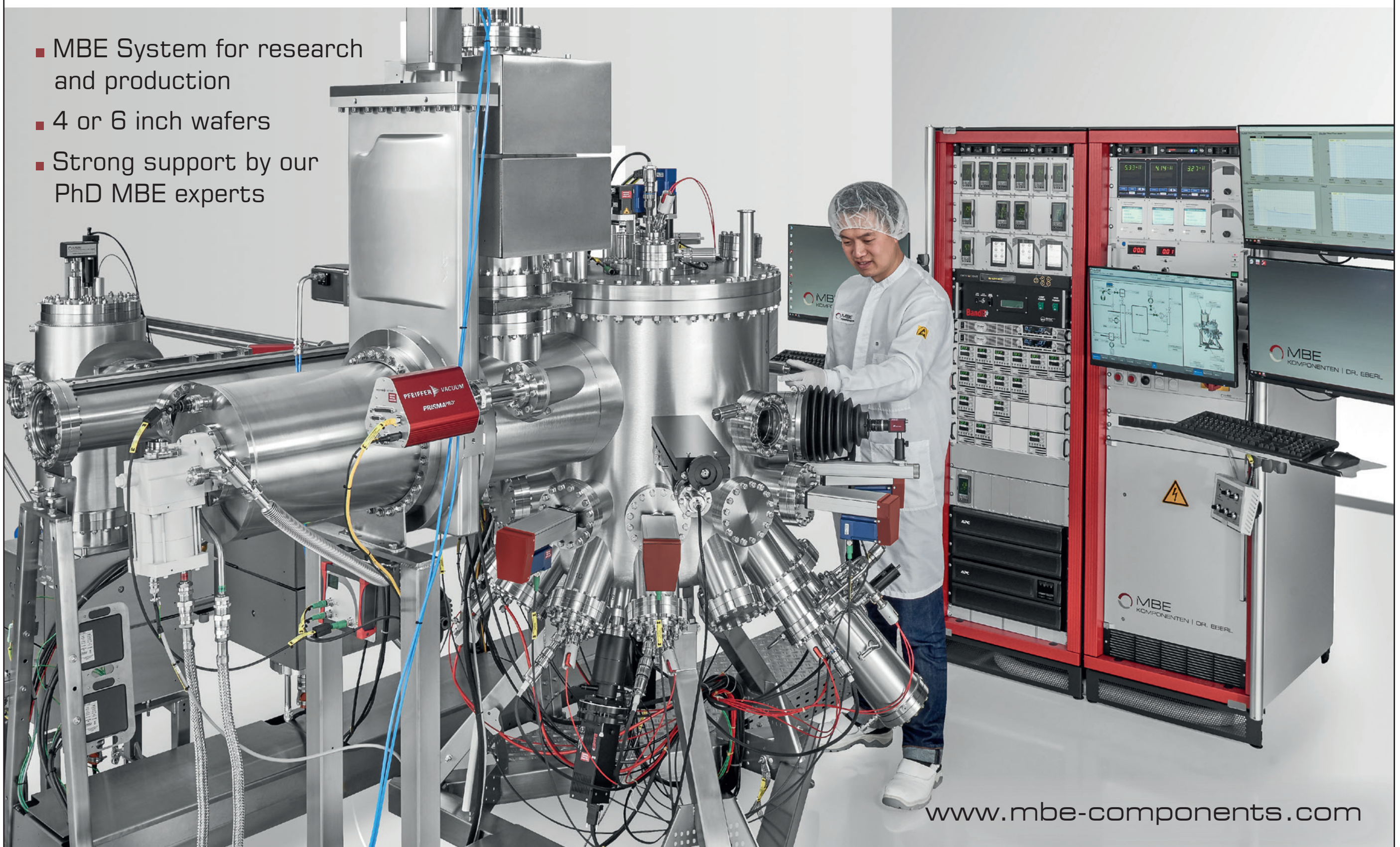

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This year's IRPS was held in Monterey, CA, bot far from the famous Bixby Bridge.

Superior testing of SiC

Speakers at the International Reliability Physics Symposium detail the most insightful approaches for evaluating the long-term capability of SiC power devices

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AT THE VERY EARLIEST STAGES of development of any power device, the focus is always on instantaneous performance characteristics, such as on-resistance, blocking voltage and peak current delivery. But it's not that long until evaluation expands to include insights into reliability. After all, if the device doesn't last long enough to serve in any practical application, it will never be commercially viable.

As the device matures and volume production begins, new questions need answering when assessing reliability. For example, there is a need to know what fraction of devices will fail at any point in time. It's also beneficial, from the perspective of the customer base, to vary the conditions of assessment to reflect different applications; and it may be crucial to pinpoint any drifts in key characteristics, even if this doesn't lead to device failure, as it could still be a compromise too far.

All these sorts of questions are now being asked of SiC transistors and diodes, power devices that are well beyond the stage of simply being promising – they are netting billions of dollars per year, with sales ramping fast.

Insights into better approaches for assessing the reliability of SiC power devices, alongside commentary considering what traditional methods may overlook, formed the heart of several presentations at the recent *International Physics Reliability Symposium*.

At this meeting on 28 to 30 March, held on-line and also in person in Monterey, CA, illuminating talks on SiC included those from: ABB's Elena Mengotti, who revealed the various tests that this company is using to assess the reliability of SiC MOSFETs from different suppliers; Kin Cheung from NIST, who explained why exceptional wafer cleaning fails to guarantee a great gate oxide; and Peter Moens from onsemi, who made a strong case for distinguishing between the lifetime of the SiC MOSFET and its useful time.

Seeking standardisation

Mengotti, a Principal Scientist at ABB's Corporate Research Centre in Switzerland, claimed that one of the issues surrounding SiC power devices is the variation in testing.

"The standardisation of silicon carbide diodes and MOSFETs has not yet converged to a set of stable

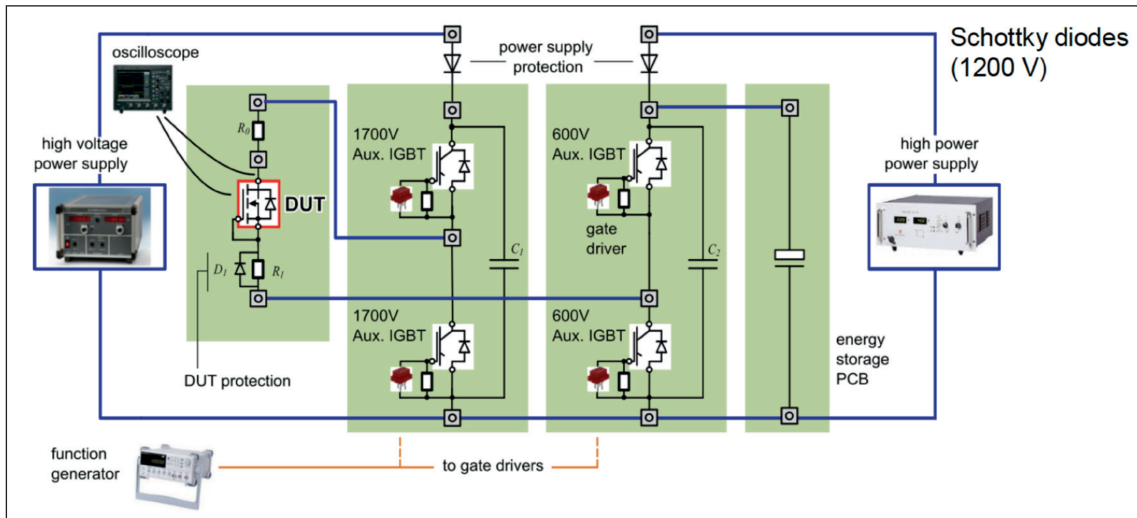


Figure 1. ABB evaluates SiC power devices with a variety of tests. Two half-bridge legs subject devices to stress, with characterisation following this procedure.

and specific tests to pass that the industry can simply request from the supplier," argued Mengotti.

While she is in no doubt that SiC outperforms silicon, she points out that any new technology introduces new failure mechanisms. Consequently, new qualification methodologies are needed to minimise the risk during initial device deployment.

Taking action on this front, ABB has developed a number of in-house tests, covering both the chip and the package.

One such test is that of avalanche ruggedness, an assessment that's suitable for applications where there is a switching of the inductive load. At ABB this test, conducted on chips in a TO-247 package, begins by charging the load inductor with a current that's low enough to avoid device self-heating.

The device is then turned off, with avalanche energy dissipated in the MOSFET. Those carrying out this test determine the destruction energy limit for five samples, before conducting further tests on eight MOSFETs, using 100 pulses with an energy that's 95 percent of that of the destruction limit.

ABB uses its avalanche ruggedness test to assess SiC MOSFETs from six different suppliers. "Pre- and post-stress curves did not show sign of ageing electrically," remarked Mengotti. "The avalanche ruggedness of state-of-the-art silicon carbide MOSFETs is sufficient to allow unclamped switching of inductive loads."

Another test at ABB, helpful for determining how SiC power devices behave during start-up and shut-down procedures in grid-connected solar and wind farms, is a study of the repetitive surge current.

"During the test we stress the silicon carbide diode or the body diode of the MOSFET, which is supposed to be a weak part of the device," said Mengotti.

The set-up involves two half-bridge 'legs' (see Figure 1). One generates rectangular high-current pulses with a 10 μs width at a frequency of 10 Hz. The other leg delivers a blocking voltage that's 80 percent of the nominal value between the surge pulses.

Using this approach, engineers at ABB evaluate devices by first increasing the surge current pulses, an approach that tests five samples to destruction. Then ten samples are aged with 1,000 pulses, using a current that's 90 percent of the value that led to device destruction. After that characterisation of the devices is undertaken. "No electrical aging sign has been observed," revealed Mengotti, who added that all of the SiC devices that have been tested show a very good level of reliability, in terms of repetitive surge current operation.

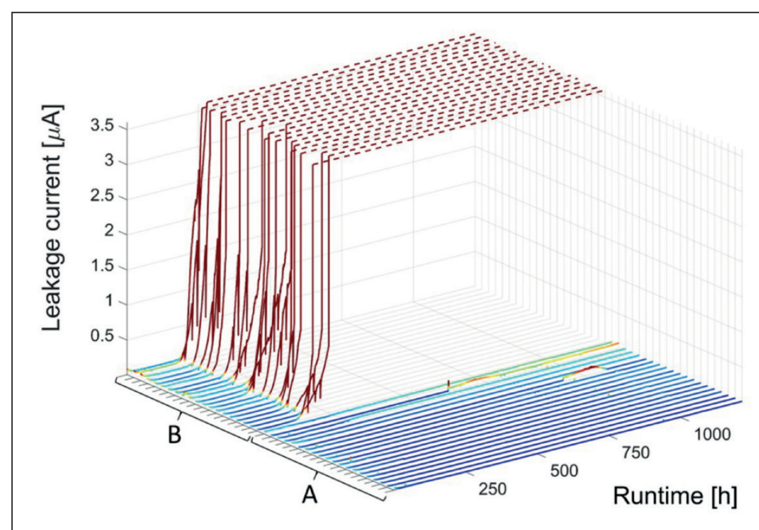
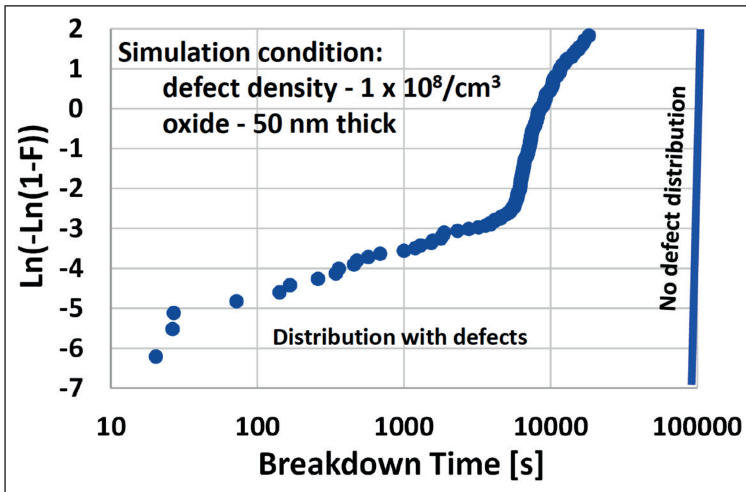


Figure 2. The H3TRB-HVDC test carried out at ABB runs for 1200 hours and involves a temperature of 85 °C, a relative humidity of 85 percent, and a drain-source voltage of 80 percent of the maximum value. The leakage current recorded throughout this test reveals substantial differences between suppliers.



➤ Figure 3. Simulations by NIST catering for variations to the energy of the defect, the width of the energy distribution, and the density of the defect, can model the extrinsic tail of failures associated with the lucky defect.

Also included in the testing suite at ABB is passive 'dV/dt' switching – this is also known as the dynamic reverse-bias test. For this evaluation, 20 devices are tested in parallel for 1000 hours, using a frequency of 60 kHz, and a dV/dt of 100 V/ns.

Using this test to monitor the drain source leakage indicated no sign of device aging. Only the very first generations of diodes showed an abrupt failure, due to an issue associated with edge termination.

"Since no failures were observed in devices from generation two onwards, and no ageing signs were seen, we currently regard this test as unnecessary," remarked Mengotti.

There have always been concerns associated with the quality of the gate oxide in SiC MOSFETs. There are imperfections at the interface of SiO_2 and SiC, and the dielectric oxide is relatively thin. To evaluate the quality of this oxide, the team at ABB elevates the temperature of the SiC MOSFETs to 175 °C, steps up the voltage every 24 hours and monitors the threshold voltage and the gate leakage current.

Using this approach, Mengotti and co-workers have aged 30 planar and 30 trench MOSFETs simultaneously. "The trench [devices] failed at a latter voltage value, indicating higher robustness than the planar. But the planar presented a lower standard deviation, indicating a more mature technology," revealed Mengotti. Another plus for the planar device over its trench cousin is a lower failure rate at the use condition, in terms of gate voltage.

The representative from ABB also discussed a number of other reliability tests for chips. They involved subjecting them to: a high reverse bias, which indicated that reliability is beyond expectation; transfer curves, to study threshold voltage hysteresis; transient measurements of drain current, which revealed that SiC MOSFETs behave differently to their silicon counterparts, but there is no cause for concern; and a test combining voltage and humidity, known as H3TRB-HVDC (see Figure 2 for details).

As well as all these chip-level tests, ABB carries out others at the package level, including power cycling, a test widely used for silicon MOSFETs. This examination involves looking at temperature differences after devices had undergone current cycling that increased their temperature to 80 °C. This test uncovered a difference between packaged devices that had wires soldered and sintered to the baseplate of a SiC MOSFET. "The failure for the solder is reached at around 50,000 cycles, with a smooth increase in the 'delta-T' junction that is proven to be a solder die attach failure mechanism, while for the same temperature condition, the number of cycles has improved to around 90,000 for the sintered junction," remarked Mengotti. In the latter case, failure is due to a wire bond lift-off.

The lucky defect model

A presentation by Kin Cheung, a Project Leader at NIST, provided a more detailed discussion relating to concerns associated with the gate oxide of SiC MOSFETs.

"A few years ago, I heard from a number of silicon carbide companies that there is a persistent, extrinsic tail in the breakdown distribution," remarked Cheung, who explained that this small proportion of problematic devices remained after exhaustive efforts to clean the wafer.

He said that at this time, this was considered a specific SiC problem, because a thermal oxide grown on SiC has more defects than a thermal oxide grown on silicon. When SiC is oxidised, as well as the addition of SiO_2, CO_2 is also added – it cannot easily escape the oxide layer, and may lead to trapped carbon.

One may expect that this extrinsic breakdown problem is unique to SiC. But that's not the case. Cheung pointed out that it has also been reported in silicon, back in 2007, for an oxide thickness of 55 nm.

Historically, there has been just one model for extrinsic failure, based on local thinning. It's been argued that local thinning, caused by particulates and contamination, leads to a lower growth rate that is to blame for a higher electric field in that region and ultimately an earlier device breakdown. But if that were the cause, there's no explanation for extrinsic failure in cleaned wafers.

A model that can do just this is the 'lucky' defect model, which Cheung championed. He argued that while debate continues over the cause of breakdown in the oxide of SiC devices, there is consensus that this failure mechanism is related to current flow across the dielectric, with higher currents leading to a shorter lifetime.

As well as local thinning, trap-assisted tunnelling can increase the current, remarked Cheung: "If you have defects at the right energy and the right spatial

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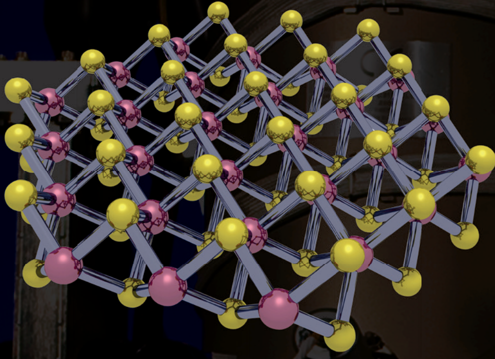

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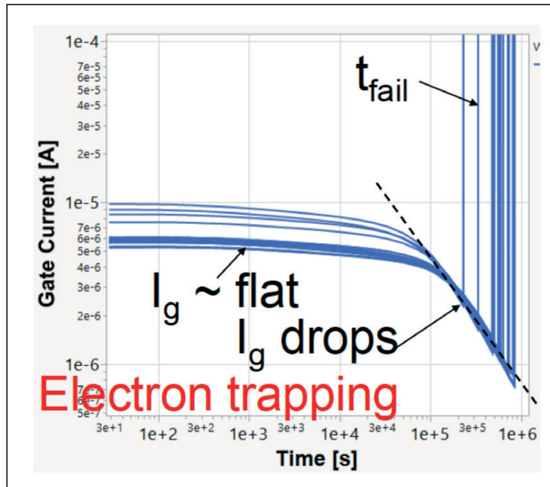

Figure 4. Investigations by onsemi reveal that gate currents of a SiC MOSFET show a similar trend, for a range of voltages and stress times. The gate current is initially flat, before it drops and then rapidly climbs, due to failure. A 'use' time, referred to as t_0, can be defined from the intercept of two lines: one for the gradient of the flat part of the curve, and a second from when it is dropping.

location, this can greatly enhance the tunnelling probability through the trap-assisted tunnelling mechanism." When this happens, there's an increase in the local current, leading to a shortening of device lifetime.

Cheung said that there is a sweet spot at which the effect is strongest. "The effect decays away rapidly as you move away from the sweet spot. That is the reason why it's called a lucky defect model."

It's important to note that with the lucky defect model, even if the oxide is grown on a perfectly clean wafer, defects will still be present. Simulations confirmed this, modelling a 50 nm-thick oxide with a defect density of 1×10^8 cm^{-3} (see Figure 3). To produce this plot, Cheung and co-workers considered variations to the defect's energy, its density, and the width of its energy distribution.

"The good news is that the lucky defect model gives you another way to further improve the extrinsic failure distribution, which is to improve the growth process," remarked Cheung. "Some companies have reported that improving the growth process did help to reduce the extrinsic failure, although exactly what they've done is proprietary information."

The lucky defects have implications for common tests that are applied to SiC MOSFETs, such as those involving the ramping of voltage (V-ramp) and high-field screening.

Cheung explained that producing SiC MOSFETs that are completely free of extrinsic failures is both hard to realise and difficult to prove. When efforts are directed at improving the growth process, a technique is needed to determine whether changes are beneficial. The standard method for assessing the gate oxide – the time-dependent dielectric breakdown method – is far from ideal for this particular task. One major drawback is that this technique requires the measurements of many thousands of devices, because only a small proportion exhibit concerning characteristics.

"Some vendors prefer a much faster alternative, which is the V-ramp test. With that you improve your growth process," explained Cheung. However, he added that to ensure product reliability in the field, it is very common for chipmakers to also use high-field screening before they ship their products.

But do these strategies actually work? "If extrinsic breakdown is due to local thinning, it likely does – at least, there is no strong evidence to say it wouldn't work," said Cheung. However, if extrinsic breakdown is due to lucky defects, it doesn't."

Determining the safe operating area

Peter Moens from onsemi also discussed concerns related to the gate dielectric in SiC MOSFETs. He pointed out that during gate stress, substantial charge trapping occurs in the dielectric. "This results in parametric shifts, limiting the use time of the device." These shifts could cause device characteristics to stray outside the values given in the accompanying data sheets. To avoid that from happening, Moens championed the introduction of a 'use time', which he agued is preferential to a 'lifetime'.

To promote this concept, Moens presented an internal study, considering 1.2 kV *n*-type SiC MOSFETs with a 30 A on current, an on-resistance of 20 mΩ and an oxide thickness of around 40 nm. Measurements were made at both the wafer level, and on chips housed in a TO-247 package. "Typically, when people look at lifetime, they look

The good news is that the lucky defect model gives you another way to further improve the extrinsic failure distribution, which is to improve the growth process," remarked Kin Cheung from NIST. "Some companies have reported that improving the growth process did help to reduce the extrinsic failure, although exactly what they've done is proprietary information

at time to fail," remarked Moens. "But it's more instructive to look at the complete gate current versus time characteristics."

Plots of this for a device temperature of 175 °C show that initially the gate current is almost flat, before it drops significantly due to electron trapping, and then hikes when the device fails (see Figure 4). This trend is seen for different gate voltages and for stress times of up to 7 months, with plots revealing what Moens refers to as an "envelope curve" that is independent of both gate voltage and temperature. "And strangely enough, this same envelope curve is also observed on silicon technologies," added Moens, who said that this finding shows that device behaviour must be related to the characteristics of SiO_2.

Based on the plots, Meons suggested that rather than giving a lifetime for SiC MOSFETs, it is more insightful to give a use time, defining this as the intercept of the flat gate-current curve with that of the envelope curve. The use lifetime, given the moniker t_0, can also define the safe operating area – this corresponds to a timeframe when the on-resistance shifts by only around 10 percent and the shift in threshold voltage is below 1.2 V. In comparison, between t_0 and device failure, the on-resistance can change by more than 100 percent. Meons and co-workers have also considered SiC MOSFET behaviour at 0 °C, a temperature where hole trapping occurs. Due to this, during gate stress an there's initial increase in the gate current due to hole trapping, followed by a fall due to electron trapping; and over that timeframe there is also a decrease and a subsequent recovery in the threshold voltage, driven by these changes.

Further investigations, considering different stress voltages, revealed that hole trapping only takes place at gate fields in excess of 8 MV cm^{-1}. The team from onsemi also determined that there is no hole de-trapping at 0 °C, and there is some electron de-trapping at 175 °C.

Drawing these findings together, Moens concluded that for high gate voltages, corresponding to a gate field of more than 8 MV cm^{-1}, changes in threshold voltage determine the safe-operating area. But at the 'use' gate voltage, which is set by electron trapping, the change in threshold voltage is less than 1.2 V over 20 years, and t_0 should be used to define the safe operating area.

This insight into how to best to describe the working life of the SiC MOSFET, along with the findings provided by NIST and ABB, show that there's still a long way to go to refine the way we characterise and assess SiC devices. Progress is highly valued, as it will help to accelerate the shift from SiC to silicon power devices, by equipping engineers with the confidence that they understand the superior alternative, and know what to expect from it for many years.

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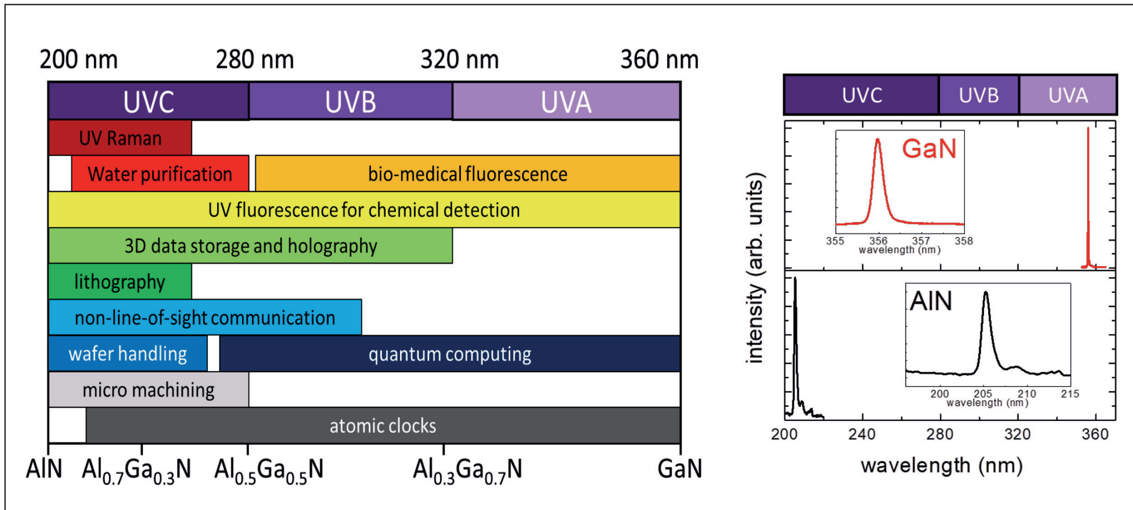
Supporting a surge in UVC optoelectronics

Defect control during the growth of AlGaN layers on AlN substrates ensures record-breaking performances for UVC LEDs, lasers and avalanche photodiodes

BY PRAMOD REDDY, RONNY KIRSTE, RAMON COLLAZO AND ZLATKO SITAR FROM ADROIT MATERIALS

OUR VIEWS on what is a basic human right will differ from person to person. But the vast majority of us will agree that all of humanity should have access to clean drinking water. This view is supported by the United Nations General Assembly, which has explicitly recognised the right to water and sanitation, acknowledging that both are essential for realising all human rights. Helping to ensure that this will happen is a resolution from 2010: it calls upon countries and international organisations to support efforts to provide safe, clean, accessible and affordable drinking water for all, by providing financial resources, helping with capacity-building and aiding the development of relevant technology.

One leading option for ensuring that water is safe to drink is to treat it with UV light, as this destroys the DNA of microorganisms. While this is also possible with chemical treatments, UV light offers the safest, most reliable and sustainable way to free water from microbial contamination.



➤ Figure 1. (left) Potential applications for UVA (360–320 nm), UVB (315–280 nm), and UVC (280–200 nm) laser diodes. (right) Bandgap emission of GaN and AlN, illustrating that the ternary semiconductor AlGaN can cover the UVA, UVB and UVC wavelength range.

Additional applications involving of the use of UV light for the benefit of mankind include the sterilisation of air and surfaces. The pandemic has piqued interest in this, with sales of UV light sources increasing to combat the virus.

The incumbent technology for providing UV light is the mercury-based lamp. However, it's far from ideal, as it is bulky, fragile, and employs toxic material. Offering far more promise is a chip-based technology, the LED, which can operate in the UVC.

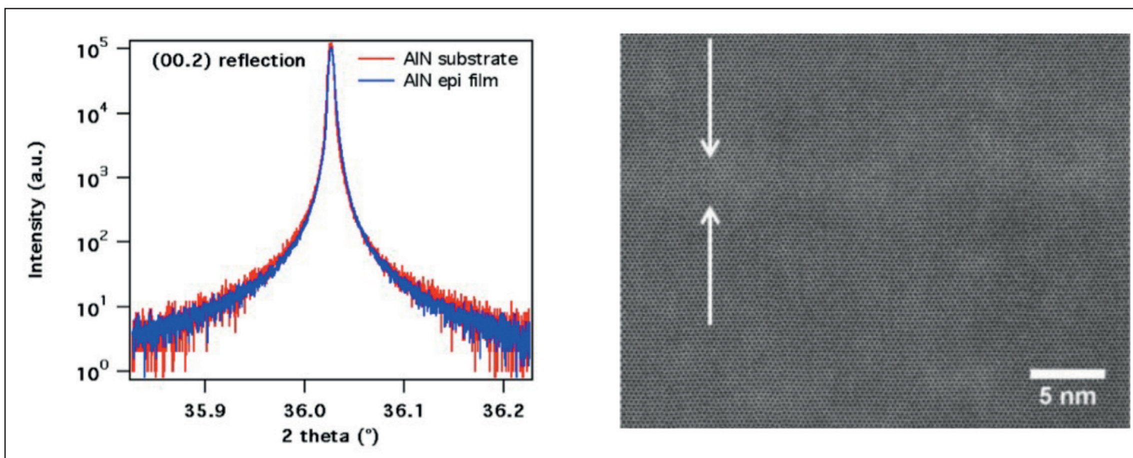
Semiconductor-based devices that operate in the UVC are also promising candidates for the detection of light. Again, it's the story of replacing an incumbent technology shrouded in glass – in this instance a photomultiplier tube – with a chip-based alternative, this time the avalanche photodiode (APD). The latter is compact, lightweight, runs off a low voltage, ensures long-term operation with highest reliability, and has excellent detection characteristics: high sensitivity; substantial gain; and excellent solar spectrum rejection, implying that it is hardly affected by stray light.

Thanks to all these attributes, avalanche photodiodes operating in the UVC have the potential to be deployed in many applications. As well as being used in atomic clocks for autonomous and deep-space operation, due to the development of mid- and far-UV detector arrays, these devices could serve in astronomy, space observation, quantum sensing, and other fields with UV photography.

LEDs and photodetectors operating in the UVC, as well as lasers that emit in this spectral range, share the same material system. All these devices are made from the ternary alloy AlGaN, which has a bandgap that varies from 3.4 eV to 6.03 eV – equating to 365 nm to 205 nm (see Figure 1, which details the wide variety of applications where this alloy, which has immense potential, could find deployment).

The challenges …

Various factors within the device layers are impeding the realisation of AlGaN-based optoelectronics. Developers of these devices are having to contend with challenges within the layers, related to doping and non-radiative recombination,



➤ Figure 2. X-ray diffraction 2θ-ω scan of an AlN homoepitaxial layer in comparison with the substrate (left) and high-resolution transmission electron microscopy of an homoepitaxial AlN film showing perfect lattice continuation across the interface (marked with arrows) (right).

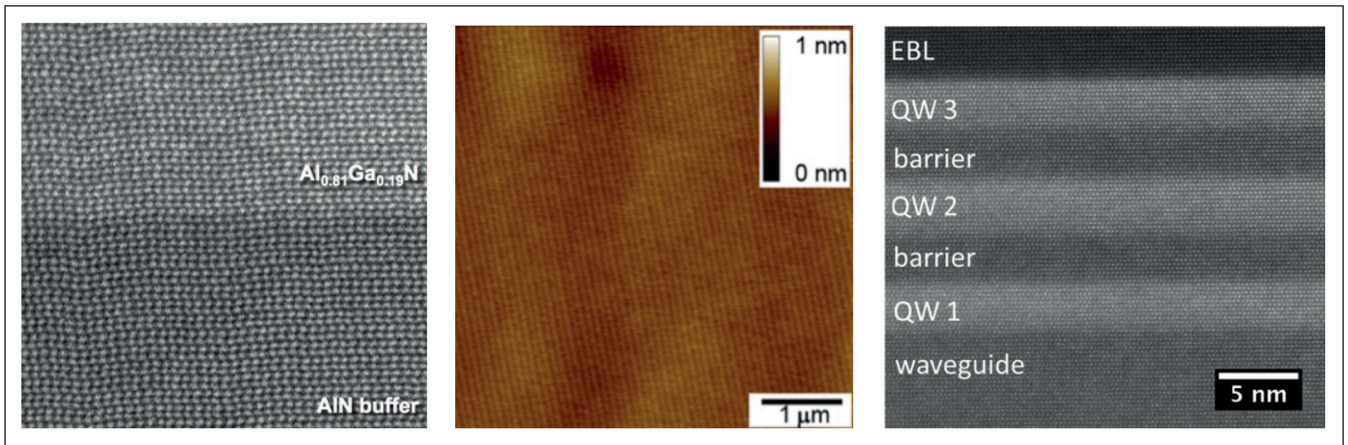


Figure 3. (left) High-resolution transmission electron microscopy micrograph for AlGaN on AlN for a nominal 80 percent aluminium content; no dislocations were observed at the heteroepitaxial interface or in the AlGaN. (middle) Atomic force microscopy image of $Al_{0.7}Ga_{0.3}N$ grown on vicinal (0001)-oriented AlN. The surface consists of desired bilayer steps with a root-mean-square roughness of less than 50 pm. (right) Scanning tunnelling electron microscopy image of an $Al_{0.55}Ga_{0.45}N$/ $Al_{0.65}Ga_{0.35}N$ multi-quantum well structure with an electron-blocking layer. All wells and barriers are well defined and of homogenous composition.

and difficulties at the material surface that lead to the likes of poor ohmic contacts and ineffective passivation.

The primary source of all these impediments arises from crystal defects. They include: extended defects, such as dislocations; and point defects, including impurities, vacancies, and their complexes. When AlGaN-based heterostructures are grown on substrates such as sapphire and SiC, the large degree of lattice mismatch with the epilayers results in high threading dislocation densities.

The imperfections in the material of these UVC LEDs leads to low efficiencies and a compromised output power, preventing them from being suitable for sterilisation. These deficiencies also account for the lack of demonstration of a laser with AlGaN-based quantum wells that emits at wavelengths below 300 nm, and the absence of commercial APDs and other detectors based on AlGaN. While several groups have reported APDs with $Al_xGa_{1-x}N$ layers with a high aluminium content ($x > 0.4$), grown on sapphire substrates, these detectors are impaired by a trade-off between device area and signal gain. Primarily, performance is limited by high screw dislocation densities, linked to both the premature breakdown of the diodes under reverse bias and the high noise levels associated with leakage currents. Note that there is yet to be a demonstration of Geiger-mode operation with AlGaN-based photodiodes.

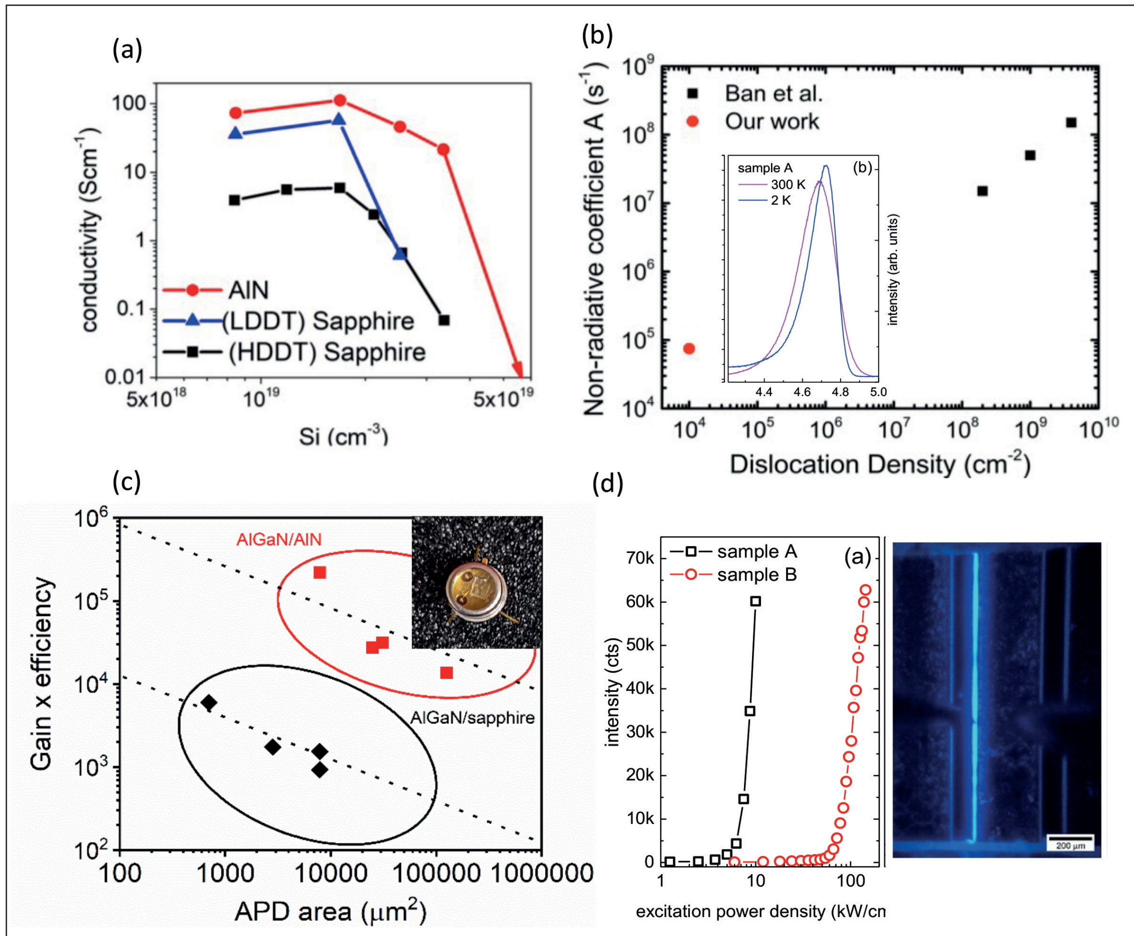
Another major challenge facing those that are keen to develop UVC optoelectronics with AlGaN is that at higher aluminium contents the activation energy of the magnesium-acceptor increases. An unwanted consequence is the promotion of compensating point defects, such as nitrogen vacancies. The upshot of these trends is that it's challenging to realise *p*-type doping with aluminium-rich AlGaN and produce an associated *p*-type conductivity. Resistivities are typically more than 50 Ω cm, hindering carrier injection and introducing a significant power loss that's a drag on efficiency. As well as these electrical challenges, adding magnesium induces absorption losses in the waveguide, preventing laser operation.

To address poor ohmic contacts associated with aluminium-rich AlGaN, many device designers employ a magnesium-doped GaN hole-injection layer. Keeping this layer thin enables ohmic contacts and efficient carrier injection, but at the expense of absorption in the desired UV spectrum. The resulting heavy absorption losses impact emitters and detectors.

Fortunately, these issues don't plague *n*-type doping of AlGaN, which has been established for aluminium-contents of up to 80 percent. However, device developers still face a point-defect problem in AlGaN. Quashing peak conductivity is a high doping limit that results in self-compensation through vacancies and complexes; and there's also a low doping limit, due to impurities such as carbon, that introduces recombination centres in quantum wells and leakage in multiplication regions. Due to these issues, point defect control is a pre-requisite for high-performance UVC optoelectronics.

...and the solution

At Adroit Materials of Cary, NC, we are working with partners to support the production of electronic and optoelectronic devices offering expertise in the growth, characterisation and delivery of state-of-the-art epitaxial AlGaN-based structures and templates. Key to the growth of high-quality material is our defect-control technology, which includes extended defect control via homoepitaxy on AlN and GaN single-crystal substrates.



➤ Figure 4. (a) Conductivity of silicon-doped $Al_{0.7}Ga_{0.3}N$ on sapphire and AlN. (b) The non-radiative coefficient (A) is reduced by several orders of magnitude in samples grown on AlN due to a low dislocation density, along with point defect control, resulting in (inset) photoluminescence with an internal quantum efficiency of more than 90 percent. (c) A comparison of APD performance with AlGaN on AlN substrates with those obtained on AlGaN grown on sapphire and (inset) a packaged APD on AlN. (d) Record low UVC laser threshold of optically pumped lasers achieved on AlN substrates and a micrograph of a fabricated laser structure.

The foundation for our work is the high-quality AlN boule, grown by physical vapor transport and licensed and commercialised by several companies. Substrates cut from these boules have an average threading dislocation density below 10^3 cm^{-2} – that's a million-fold improvement on threading dislocation densities of more than 10^9 cm^{-2}, seen in AlN/GaN grown on sapphire.

According to X-ray diffraction studies and high-resolution transmission electron microscopy, when we grow thin films of AlN on AlN single-crystal substrates no new defects form at the interface and there is perfect lattice continuity (see Figure 2). Thanks to this foundation, when we undertake heteroepitaxy of AlGaN on AlN substrates with pseudomorphic growth, our epistructures are free from threading dislocations and have atomically smooth surfaces. These merits enable near ideal interfaces and multi-quantum well structures with exceptional quality (see Figure 3). Drawing on this growth technology, we can use single-crystal substrates as the foundation for nearly extended defect-free AlGaN films constituting the various active layers of lasers, LEDs and APDs.

It's important to note that the growth of AlGaN on substrates made from GaN results in tensile strain and cracking. So, to realise high-quality thin films on that alternative foundation, there's a need for facet-controlled epitaxial layer overgrowth, a more complex technique. We have developed point defect control frameworks, such as chemical potential control and defect quasi Fermi level control. These technologies enable us to pursue a targeted reduction of impurities in AlGaN layers of devices. In turn, we have been able to push the doping limits for AlGaN and enable improved electrical conductivities and carrier transport, alongside reductions to thermal and non-radiative recombination losses.

Every aspect of device performance benefits from our extended and point defect control. By mitigating

self-compensation in silicon doped *n*-AlGaN, these layers can realise conductivities as high as more than 150 S cm^{-1}. Non-radiative recombination rates are exceptional, with a three-orders of magnitude improvement ensuring a record-breaking internal quantum efficiency of more than 90 percent, thanks to the use of our defect control frameworks. Drawing on these virtues, we have demonstrated AlGaN multi-quantum well laser structures with record low lasing thresholds of less than 10 kW cm^{-2} (note that the first electrically injected UVC laser diode and the best optically pumped laser diodes had single crystalline substrates for their foundation). Finally, we have demonstrated a nearly two orders of magnitude improvement in APD performance, in terms of the product of gain and efficiency, over a wide range of detection areas. This triumph has resulted in technological viability of solar-blind AlGaN APDs.

It is only in the last ten years that major progress has been made in the field of AlGaN UVC optoelectronics. Compared with other optoelectronic devices, that's not that long. Consider, for example, the GaAs laser diode, which took decades to mature before widespread commercialisation. While recent progress may not be obvious, tremendous advances have been made in this field, creating a very positive outlook.

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Driving motors in space

Its intrinsic radiation hardness and excellent electrical characteristics position the GaN HEMT as the ideal device for making circuits that drive motors in space

BY ANTHONY MARINI AND MAX ZAFRANI FROM EPC SPACE

THE NUMBER of satellites circling the globe in a low-Earth orbit is increasing at an astonishing rate. Back in 2019, active and defunct satellites totalled just over 3,000; today it's around 10,000; and by the end of this decade this figure will have rocketed to several hundred thousand.

This breath-taking growth in the level of activity in the outer reaches of the Earth's atmosphere has ensured that ventures and activities that at one time appeared far-fetched are now a certainty. That includes the commercial development of this sector, which is well underway, as well as manufacturing in space.

The latter, an activity that offers intriguing possibilities, will involve the use of all types of motors to perform every mundane and precision task associated with manufacturing. For those designing manufacturing systems for space, as well as having to source the most appropriate motor, efforts will need to be directed at carefully selecting the most appropriate driver, to ensure that the motor runs efficiently and reliably. Making such decisions are not easy, because the motor and its driver behave as a tandem entity, with their interplay

determining the system's mechanical and electrical attributes – both criteria are of critical importance for overall system performance. Partner a motor with an inferior driver and it will be incapable of operating efficiently and delivering its peak performance. Note that up in space efficiency really matters, alongside radiation hardness – excellence on both these fronts is needed without compromising the mechanical attributes of the motor, such as its speed and positional accuracy.

Varying requirements

When using a motor in space, there are specific challenges that depend on the physical location of the system, particularly with regards to radiation. Satellites orbiting the Earth have to handle radiation fields that are not found in stationary locations, such as the surface of the Moon or Mars.

Two classes of radiation are found in space: cosmic radiation, coming from high-energy particles that are moving at relativistic speeds; and lower energy protons and electrons from the solar wind, trapped in Van Allen radiation belts, due to the Earth's magnetic field.

When sensitive electronics is deployed in space, it is surrounded by shielding. However, there is a limit on how much shielding can be applied. Shielding adds mass to the launch – this incurs substantial costs, due to the energy required to either place objects in orbit or to escape the Earth's gravity. This cost-related limitation is particularly pressing in commercial space ventures, where financial margins really matter, and where constellations of low-cost satellites are stationed in primarily low-Earth orbits.

Due to this state-of-affairs, there's a need for electronics that has an inherent radiation 'hardness' or tolerance, and can survive high-energy insults and longer-term, lower-dose radiation exposure over the duration of the planned mission.

Another factor influencing the type of radiation, and its magnitude, that electronics will encounter in Earth's orbit is the altitude of the satellite. The radiation hardness requirement for a satellite in a low-Earth-orbit differs from that in a geosynchronous Earth orbit – and both these sets of requirements differ from those for landers and missions to the Moon and other planets, and for deep space probes. In all cases, those working on their particular ventures must consider the radiation profile over the life of the satellite or spacecraft, and carefully select every component within the motion control system to prevent its premature failure.

For motion control systems under bombardment by radiation, their weakest link is the electronics associated with their motor drives. The motors themselves are not a concern, as they provide a very robust component of the system – they are constructed from wire, and thus present an inherent radiation hardness during operation. That's not the case for the electronics that comprise the motor driver. This driver contains numerous interconnected semiconductor components, including: power switches for motor windings; associated catch diodes; and electronics that interfaces between circuitry. All circuits and constituent components have to have an assured/tested level of radiation hardness to ensure that the mission will succeed long-term.

There are operational implications from a radiation-induced event, ranging from erratic operation to outright system failure. Consider the case where a motor phase is being driven in an H-bridge configuration, as shown in Figure 1. In this circuit, the switches S1 through S4 represent the power switch transistors driven by the gate drivers. As depicted in Figure 1 (a), for the forward motor direction switches

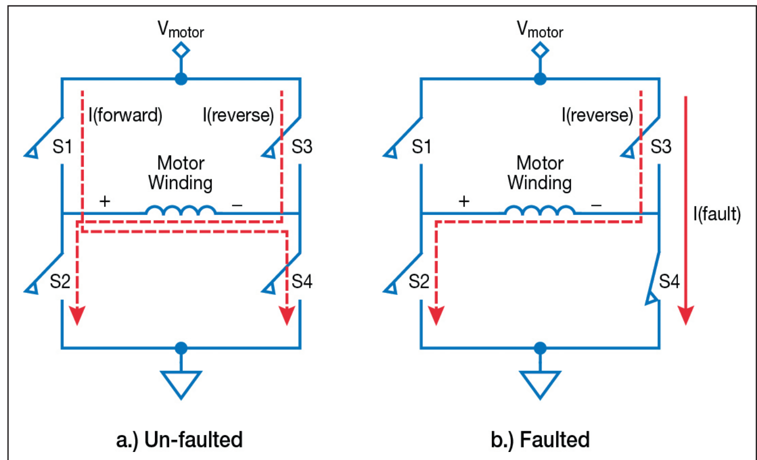


Figure 1. A single-phase motor driver with speed and direction control.

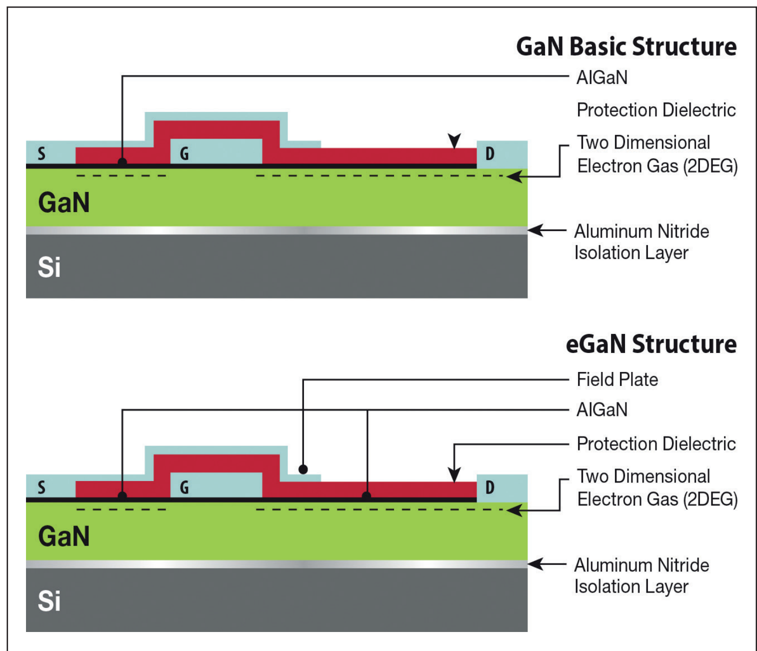
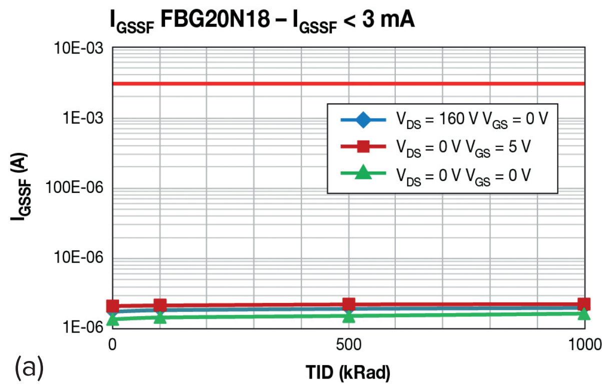
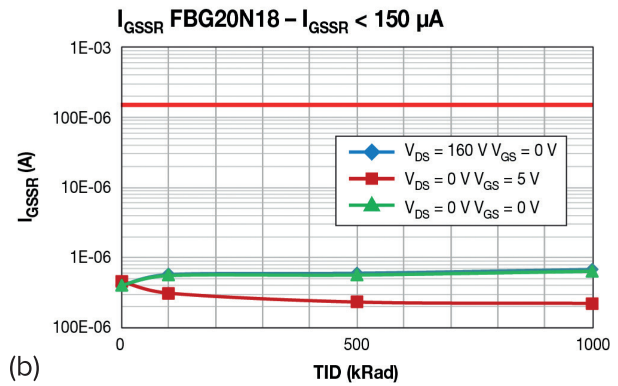
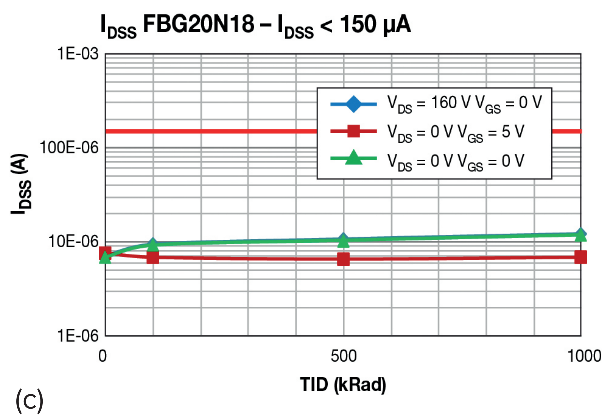
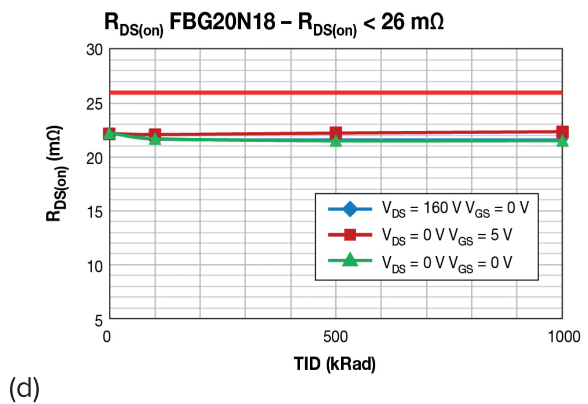


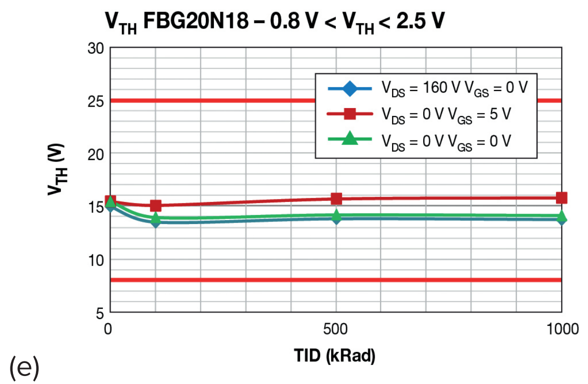
Figure 2. Depletion-mode (top) and enhancement-mode (bottom) GaN transistor structures.











➤ Figure 3. (a) Gate-to-source forward leakage, I_{GSSF} vs. total dose. (b) Gate-to-source reverse leakage ,I_{GSSR} vs. total dose. (c) Drain-to-source leakage I_{DSS} vs. total dose. (d) On-resistance, $R_{DS(ON)}$ vs. total dose. (e) Gate-source threshold voltage, $V_{GS(th)}$ vs. total dose.

S1 and S4 are closed/switched; and for the reverse direction, switches S2 and S3 are closed/switched. In both cases, it is the pulse-width modulation control of the switches that determines the speed of the motor.

If high-energy radiation disrupts the gate driver circuit or the output power switch, represented by S1-S4, this can cause S1 to S4 to either open or close momentarily. In the open switch case no damage occurs, and the only downside is a missed switching opportunity. But in the closed case, the damage can be catastrophic. For example, consider what could happen when S4 is induced closed by radiation when it isn't supposed to be, and S3 is simultaneously closed in normal reverse-direction operation. In that scenario, shown in Figure 1 (b), a cross-conduction event will occur from V_{DD}-to-ground through S3 and S4, destroying one or both switches. Clearly, this event, arising from uncontrolled current flow, must be avoided at all costs.

In the space environment, GaN transistors are ideal candidates for rad-hard transistor switches. These devices are blessed with an inherent tolerance to total ionizing dose radiation. They can be exposed to megarads of radiation without serious consequence; the only noteworthy changes are a slight rise in the gate and drain leakage currents. Thanks to their lateral structure and the absence of gate oxides and substrate-related junctions, these devices are immune to damage from interaction with single, energetic particles, so long as the transistor is well designed (see Figure 2). The robustness

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info@pe-international.net

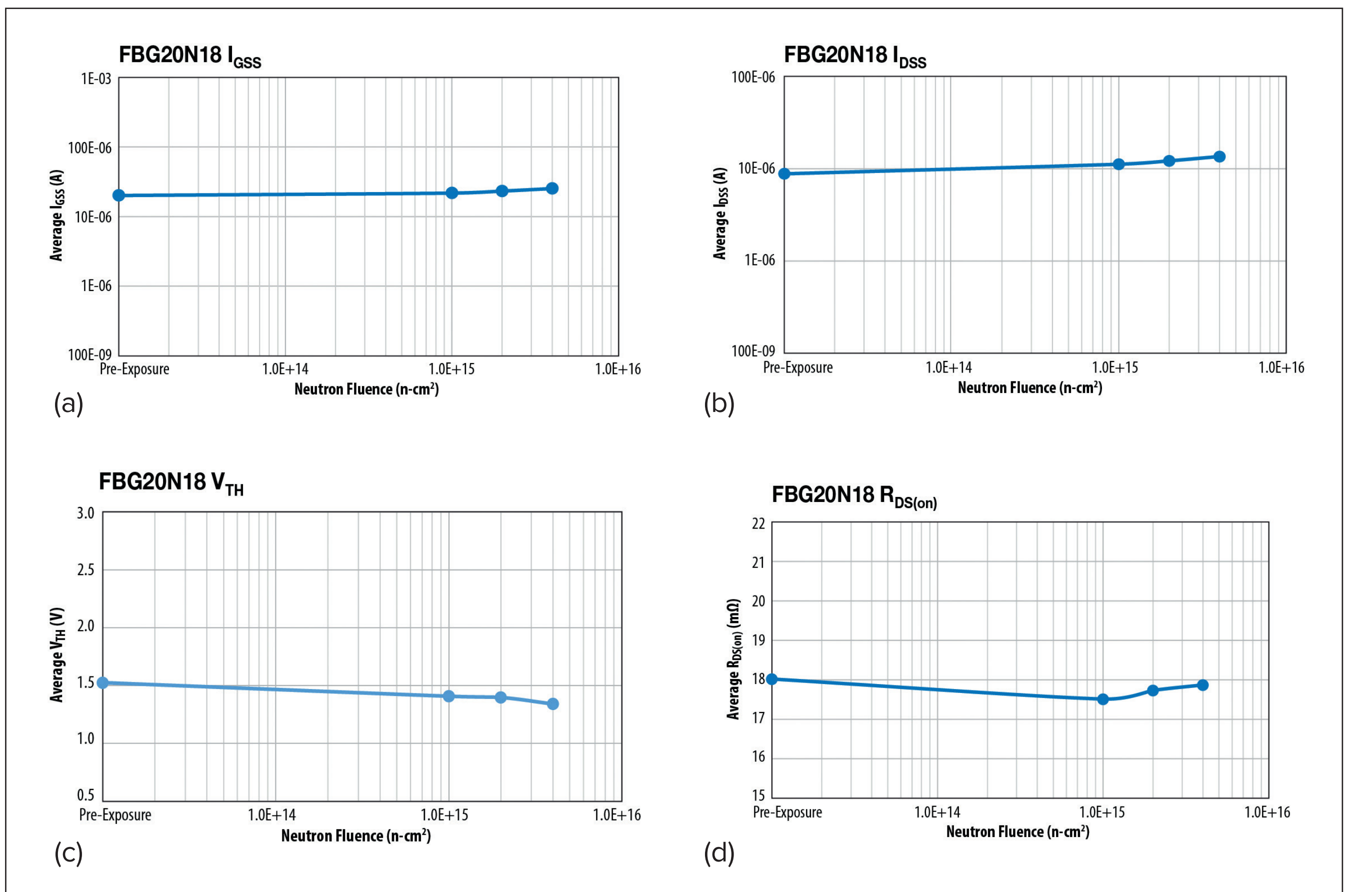
Our products offer inherent radiation hardness, a trimming of size and weight, and a reduction in losses from heat generation, allowing designers to focus on optimising the electro-mechanical performance of the motor system

that a 200 V, 18 A discrete GaN HEMT provides is illustrated by typical radiation performance data. This device is adept at handling ionising doses (see Figure 3), neutron radiation (see Figure 4) and heavy ion bombardment (see Figure 5). These results underscore the robust immunity GaN transistors provide to various forms of radiation found in space.

As well as great robustness to radiation, GaN HEMTs excel in electrical performance, due to their high electron mobility and wide bandgap. The transistors also exhibit a low on-resistance and low input capacitance, ensuring that the figure-of-merit that comes from the product of these two characteristics tends to be more than ten times lower than that of similarly rated silicon MOSFETs.

At EPC Space, a joint venture between EPC Corporation and VPT Corporation, we have been developing a product line of rad-hard discrete and modular components for space motion control, as well as other power-related applications. Drawing on EPC's proprietary Rad Hard eGaN HEMTs, our portfolio of discrete devices provides two packaging configurations: hermetically-sealed devices in thermally-efficient AlN ceramic packages; and discrete devices mounted to AlN ceramic die adapters/'inteposers', designed for hybrid applications. Modular devices in our family include single and dual low-side gate drivers; single and dual low-side power drivers, incorporating proprietary GaN-driving-GaN gate drivers, along with power HEMT switching elements and Schottky catch rectifiers; and a half-bridge driver comprised on independent low- and high-side power drivers. All devices have demonstrated radiation performance.

One of the products within this portfolio, the FBS-GAM02-P-R50 module, can be readily configured in a half-bridge configuration (see Figure 6). This module, housed in an 18 pin non-hermetic plastic



➤ Figure 4. (a) Gate-to-source leakage, I_{GSS} vs. neutron fluence. (b) Drain-to-source leakage, I_{DSS} vs. neutron fluence. (c) Gate-source threshold voltage, $V_{GS(th)}$ vs. neutron fluence. (d) (d) On resistance, $R_{DS(ON)}$ vs. neutron fluence.

over-molded package, features low- and high-side power switches, gate drivers and Schottky catch rectifiers, a high-side bootstrap capacitor and diode, an under-voltage 'power good' function, and input shoot-through protection.

Many of the motors that are used in space drive reaction wheel assemblies. This includes the use of three-phase motors to drive spinning masses in the *x*, *y* and *z* axes, to create inertia in one or more of these axes and ultimately control the altitude and position of a spacecraft in orbit. By selectively changing the speed of rotation, and thus the inertia of the spinning mass, it is possible to control the pitch, yaw and orbital position of the spacecraft. To control the three-phase motor, three half-bridge drivers are required per motor. And as three axes require control, nine half-bridge drivers are needed for each reaction wheel assembly system.

To address this motor drive requirement, we have developed the EPC7C006, a three-phase motor demonstration board that utilises the GAM02 as the three-phase control switches (see Figure 7). This board is designed to be either stand-alone, with phases driven by external three-phase digital pulse-width modulation signals, or to interface with the EPC9147A microcontroller interface board – it features a Microchip DSP to provide a pulse-width modulation signal for each phase, based on voltage, current and optional positional feedback. This control board utilises the Microchip motorBench Development Suite, under license to EPC. Thanks to this, designers either control the motor to be driven in the end-application with an existing control system developed in-house, or with a purpose-built control system that interfaces to a computer via a USB connection and GUI interface provided by us or EPC.

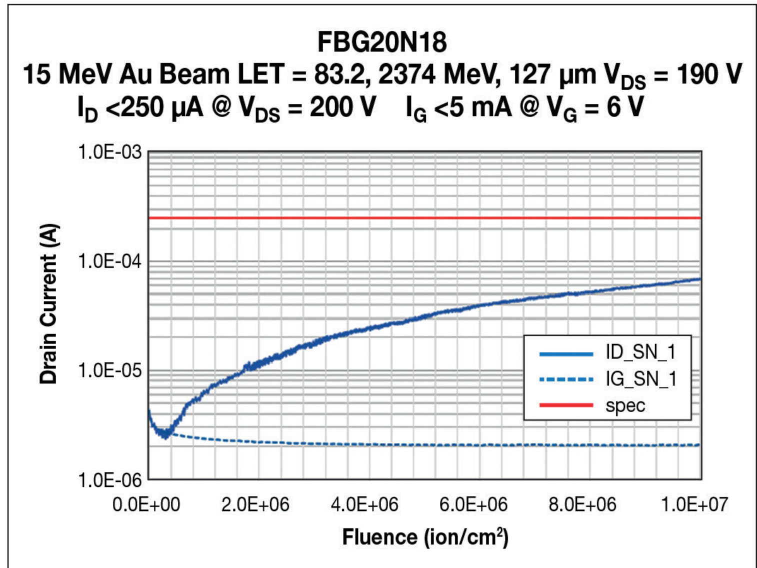


Figure 5. Gate to Source leakage and Drain to Source Leakage, I_{GSS}, I_{DSS} vs. Fluence at LET =83.

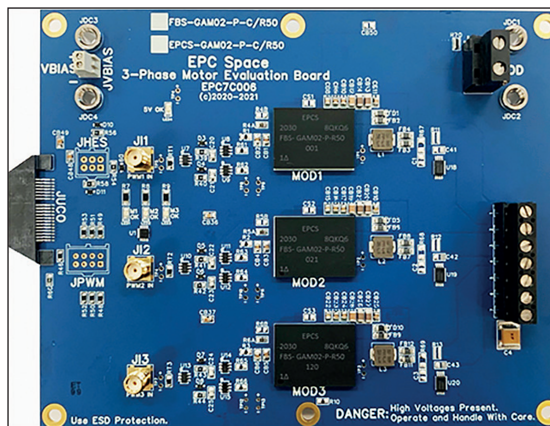


Figure 7. EPC Space EPC7C006 three-phase motor driver demo board, which measures 6.50 inch by 5.22 inch.

There's no doubt that the commercial and industrial activities planned for space, both in orbit and extra-terrestrially, are demanding and exciting. Many motors are already spinning away in space, and it is a sure bet that far, far more will follow. Thanks to our efforts, circuit designers no long need to feel daunted by the task of implementing high-reliability motor control circuits, due to the availability of robust, rad-hard, high-performance discrete devices and modular components for motor drive/control. Our products offer inherent radiation hardness, a trimming of size and weight, and a reduction in losses from heat generation, allowing designers to focus on optimising the electro-mechanical performance of the motor system. Do this, and the biggest benefit of all is keeping the motor system in question on-orbit, or fulfilling its mission elsewhere.

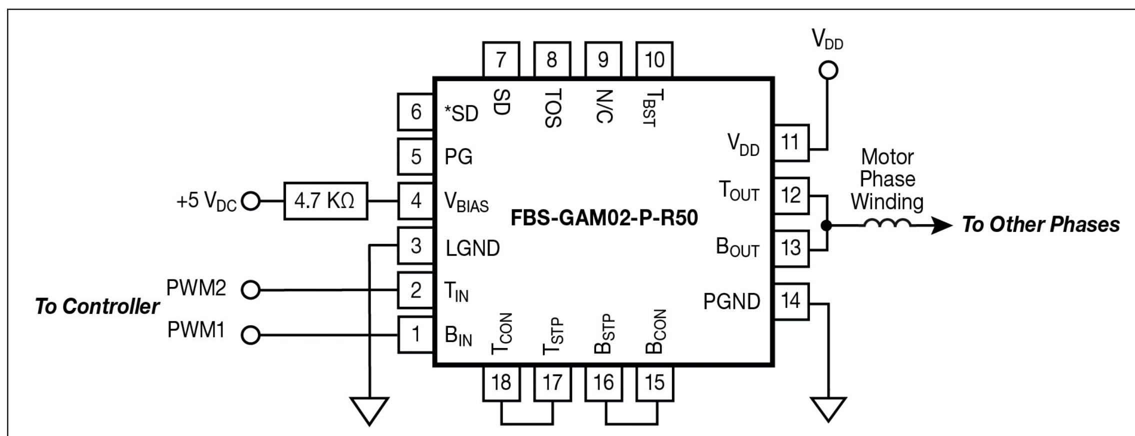
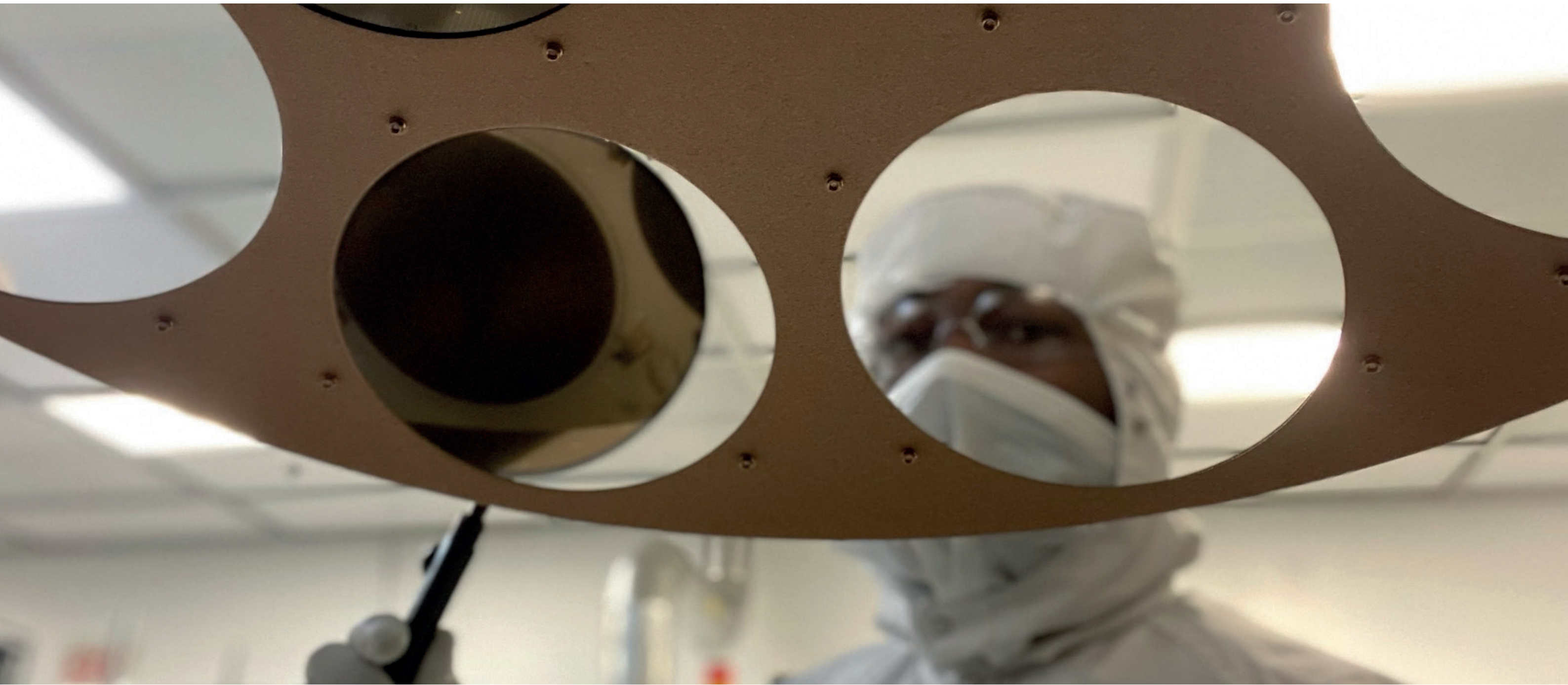


Figure 6. EPC Space FBS-GAM02-P-R50 in a half-bridge configuration.



Tackling the foot

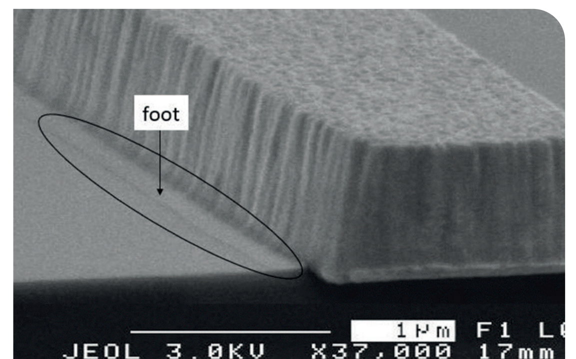
A two-paced deposition process offers the best compromise for forming a metal gate in a high-throughput GaAs fab

BY KEZIA CHENG AND GUOLIANG ZHOU FROM SKYWORKS SOLUTIONS

THE RECENT chip shortage has piled immense pressure on foundries looking to increase their production via a boost in throughput and a trimming of cycle time. For those that work there, ramping production is certainly not unchartered territory. However, that does not imply that succeeding is trivial. For example, in GaAs fabs that produce a key component for mobile phones, metallization is often a bottleneck, with wafer yield impacted by a very common yet seldom discussed defect: gold foot diffusion. This issue is so widespread that it can account for up to 40 percent of yield loss.

In these GaAs fabs, a common approach to increasing the deposition rate for metallisation – and ultimately realising a higher wafer throughput – is to add a crucible liner to the evaporation tool. The logic behind this fix is straightforward: Doubling the deposition rate halves the process time and hikes the number of wafers produced per shift. However, cranking up the rate that gold is deposited has its downsides, such as an increase in the likelihood of gold spitting and premature gun failure. To address these concerns, some fabs add tantalum pellets to the crucible liner during gold evaporation. The tantalum 'getters' the carbon in the molten gold, thereby tackling the primary reason for metal spitting. A benefit of the crucible liner is that it thermally isolates the gold from the hearth cooling water, ensuring a high deposition rate at a fraction of the normal power.

The combination of the crucible liner and tantalum 'getters' looks like a win-win: the deposition rate increases while reducing gold spitting. But under the eagle eye of a scanning electron microscope



➤ Figure 1. Scanning electron microscopy of a metal line shows the typical columnar growth and a metal foot, which is a characteristic feature of lift-off evaporation. If the gold overlaps titanium, it will be a reliability concern.

a concern arises, as a foot may be seen on the edge of the metal lines after lift-off. While it may be tempting to dismiss this issue, arguing that this little foot looks like nothing, the reality is that this feature can severely impact yields. Up until now, there hasn't been much exploration into this issue – but before every GaAs microelectronic fab starts to add crucible liners to its evaporators, there's a need to look closely at the effects on device performance.

Picking up where we left off

Our team at Skyworks has been pondering these issues for many years. Back in 2007 we published an article in this magazine entitled *Palladium barrier cuts materials bill* (September 2007, p. 19), describing a study of GaAs pHEMT fabrication that identified that the combination of high deposition rates and a beam sweep produced a pronounced foot at the base of the gate electrodes. We were concerned by this, because our process allowed palladium and gold to contact the semiconductor – and threaten, when sufficient activation available, the diffusion of these elements into the epilayer to create current leakage paths.

To avoid this detrimental occurrence, we reduced our deposition rates for gold and palladium, and applied a beam sweep and a high deposition rate for only the titanium layer. With these modifications, we minimised the gold and palladium overlap with titanium at the base of the gate metal.

One of the key conclusions from that study was that if we could learn how to reduce this foot, we could benefit from higher yields and make an even stronger case for a palladium-based barrier. At that time, we were also exploring how the sticking coefficients of the metals play a role in foot formation – this effect can also have a negative impact on wafer yield.

Fifteen years on, we have conducted experiments that build on our previous study and help us to improve wafer yield further, by also looking at the use of crucible liners for gold evaporation. These recent investigations reveal that a high gold deposition rate, a crucible liner, and a beam sweep all contribute to an exaggerated foot and gate leakage in a pHEMT – and ultimately contribute to device failure. Here, we'll discuss the results of our experiments to study the gate foot, and our findings on how the size of the foot corresponds to the deposition condition. In addition, we'll detail our proposed solution.

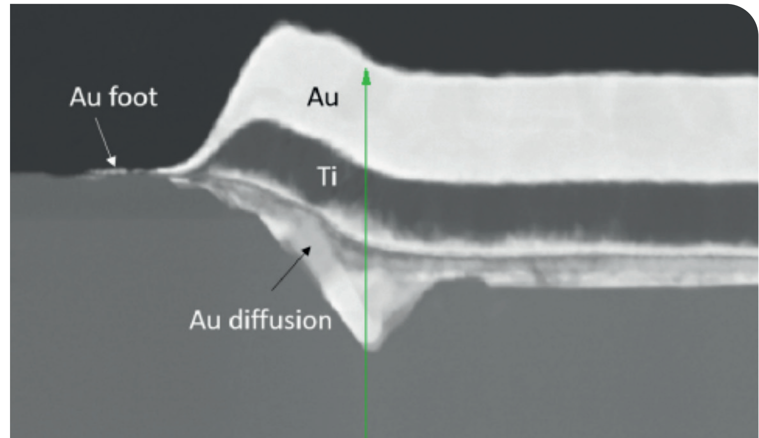


Figure 2. Gold diffusion at the edge of base metal contact.

Gate foot formation: the thorn in our side

The primary metallisation process for fabricating compound semiconductor devices is electron-beam evaporation and lift-off. This begins by placing wafers in high vacuum, prior to deposition with line-of-sight characteristics, thanks to a long mean-free-path and minimal scattering. As previously mentioned, the scrutiny of an electron microscope reveals that this process is imperfect, as a foot may be seen on the edges of metal lines, where a very thin layer of metal extends from the main body beyond the photoresist-defined critical dimension. Note that the physics of foot formation is closely related to metal fencing formation.

There are several stumbling blocks to minimising or eliminating the metal foot. For example, if gold overlaps the underlying titanium, it might diffuse into

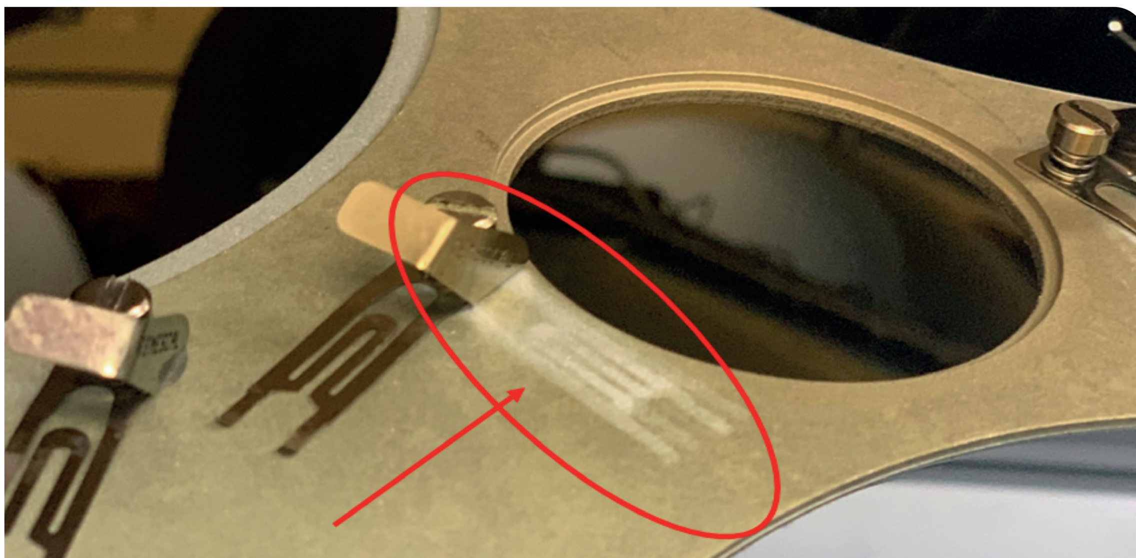


Figure 3. The wafer clip leaves a shadow on the back of the wafer dome, providing clear evidence of gold re-evaporation due to a low sticking coefficient.

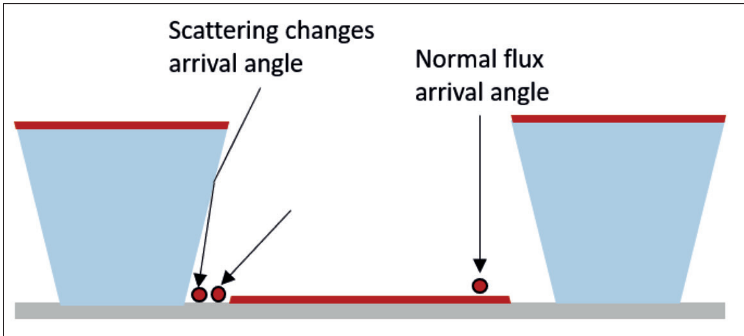


Figure 4. High evaporation rates cause collision between atoms. Scattering changes the arrival angle that contributes to metal foot formation early in the deposition process.

the channel during downstream processing, causing a high leakage pHEMT. This issue is not limited to the pHEMT, with the presence of a foot in a metal contact causing a similar leakage problem in HBTs.

Several approaches have been tried to reduce the size of the gold foot, including doubling the thickness of titanium and reducing the thickness of gold. However, none have succeeded in trimming either the gold foot or the leakage current.

The role of deposition

High deposition rates are attractive in fabs, as they can unlock an increase in throughput. For evaporators to provide a high deposition rate, they must be driven at high powers. In this regime there's an increase in the molten area, with gold atoms sent into a flurry, causing them to collide more frequently. Due to this greater scattering, the spread of the flux-arrival-angle increases, amplifying the presence of the metal foot –which, as we've said before, is the bane of our existence.

Another consequence of turning to high deposition rates and elevated evaporation temperatures is that it leads to higher thermal radiation, with heat transferred from the gold source to the shields inside the chamber. Due to this, areas with a lower sticking coefficient are more likely to experience gold re-evaporation. We have observed this, with gold deposition clearly visible on the back of the wafer dome, attributed to gold re-evaporation from surfaces with a low gold sticking coefficient (see Figure 3, which shows a wafer clip masking the reflected gold atoms and leaving its outline on the dome surface).

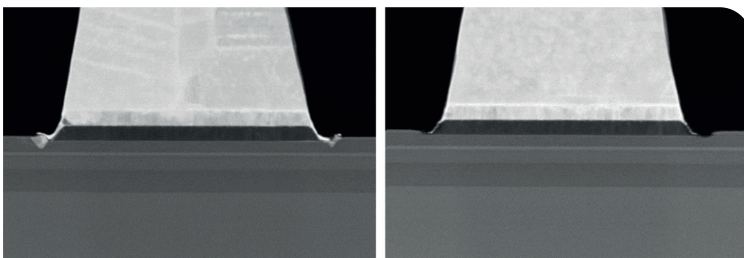


Figure 5. A gate electrode produced with a high deposition rate for gold has pronounced foot and gold diffusion (left). Meanwhile, a gate electrode formed with low deposition rate and no beam sweep has a minimal gate foot and no diffusion (right).

The re-deposition of gold from nearby structures is more likely when there's a poor sticking coefficient. This has to be considered when forming gate electrodes, because re-deposition is a factor early in the process of deposition, and can determine the appearance and the size of the metal foot.

As well as considering this, it's also important to account for: the reflection of gold atoms off chamber walls and shields, and even the gate photoresist (see Figure 4); and increases in scattering and flux angle variation, associated with a crucible liner.

We have carried out a number of experiments to determine the influence of the crucible liner. Our key findings are that:

- pHEMTs with the lowest leakage come from wafers produced with a low gold deposition rate, in evaporators without a crucible liner
- using a high deposition rate, but no crucible liner, leads to a more-than-doubling of the pHEMT leakage current
- introducing a crucible liner increases leakage current more than twice. The high leakage accounts for a yield loss of 40 percent
- the combined effects of a beam sweep and a high deposition rate double the circuit leakage
- compared with pHEMTs produced using no crucible liner and a low deposition rate, those fabricated with a high deposition rate in an evaporator with a crucible liner have five times the leakage current

These conclusions may lead you to wonder why the addition of a crucible liner is so deleterious to pHEMT performance. Part of the reason is that in its absence, the gold source in a copper hearth can be completely transformed from solid to liquid, so long as this source is clean and the beam properly adjusted. Due to the contact between the molten gold and copper hearth, there is a steep temperature gradient from the centre of this metallic source to its edge. The gold that's in contact with the copper hearth maintains a lower temperature, causing evaporation to primarily take place in the centre of this source, where the beam strikes. Thanks to this state of affairs, gold deposition from evaporators without a crucible liner resembles that of a virtual point source.

That's not the case when a crucible liner is included. Its addition leads to thermal isolation of the source from the water-cooled hearth, and completely molten gold, even at low power. As gold is a good thermal conductor, the temperature of the molten source tends to stay uniform across the entire surface. Adding to concerns, the beam sweep keeps the source molten where the beam passes. Due to this situation, when a beam sweep is applied during deposition, its impact is similar to a source-to-substrate misalignment.

The takeaway from our cumulative experimentation is that contrary to popular practice, a high deposition rate and the use of a crucible liner are detrimental to overall wafer yield. Cranking up the deposition rate and adding a liner leads to an increase in the highly undesirable gate foot, and a higher proportion of unacceptable devices.

Our solution: ramping up

Increases in the area for source evaporation and a hike in gold re-deposition accentuate the source-to-substrate misalignment, a factor behind gate foot formation. The situation is not permanent, however, as during evaporation the metal that's deposited on the photoresist reduces the opening and the collimating the path for the gold atoms to reach the foot. This means that as evaporation continues, the angle at which gold atoms reach the base and thus form the foot diminishes – and at a certain point, the metal thickness is tall enough to prevent the gold atoms from reaching the base directly. However, even then, some atoms can still reach the foot via re-deposition (see Figure 7).

Based on this observation, it is worth investigating whether an acceptable compromise can be reached by starting the deposition at a lower rate, before ramping up to a higher one, once a certain thickness has been deposited.

To see if that approach is worthwhile, we launched a new experiment to see whether the gate leakage can be minimised without a penalty to throughput by turning to a two-step deposition process. We began with a low deposition rate, as this should ensure a small gate foot. Then, once the gold thickness reached a point that prevents scattered gold atoms from reaching the base directly, we increased the deposition rate to shorten the process time.

We have compared the leakage of devices produced using the nominal rate of 0.5 Å/s with those that use this rate initially, before increasing to 1.0 Å/s for half the total gate metal thickness. The leakage for the control is -0.218 μA, a value that falls in the historic baseline of this pHEMT mask (see Table 1). In comparison, devices produced with the two-paced deposition exhibited an increase in gate leakage by around 60 percent, to an average of -0.349 μA. The two-paced growth also led to a doubling of off-current leakage. However, there is no difference in other critical FET parameters.

Although starting the deposition at a low rate before ramping this up led to a higher leakage, the leakage is still much smaller than that when producing the entire gate thickness at a high rate. It's also quite possible that we can improve the trade-off between leakage and throughput by adjusting the ratio between the low and high deposition rates of our two-step process.

Our results are consistent with the theory that gate foot formation mostly develops early in the deposition process. It's intuitive to reason that once the metal in the resist opening has built up to certain level, gold atoms will have a limited path for reaching the bottom of the opening. Based on this view, it follows that the impact of a high deposition rate will diminish after reaching a certain thickness in the resist opening.

In a nutshell, we can say that while the ramped rate leads to a high leakage, the value is still acceptable, and it comes with the crucial benefit of a higher throughput.

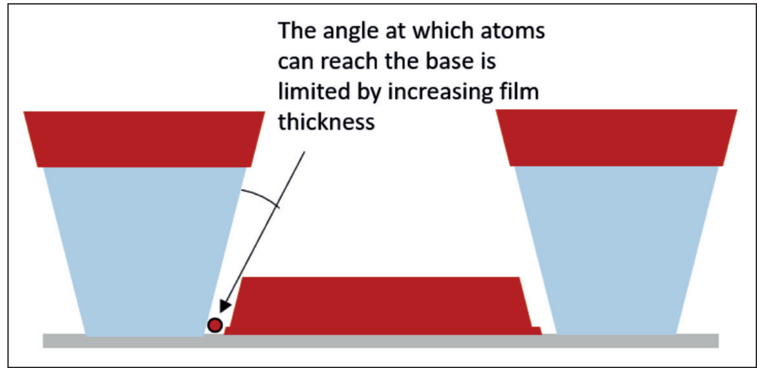


Figure 6. A film deposited on the photoresist closes the opening. Increasing film thickness inside the photoresist opening limits the number of atoms that can reach the foot to a narrow angle.

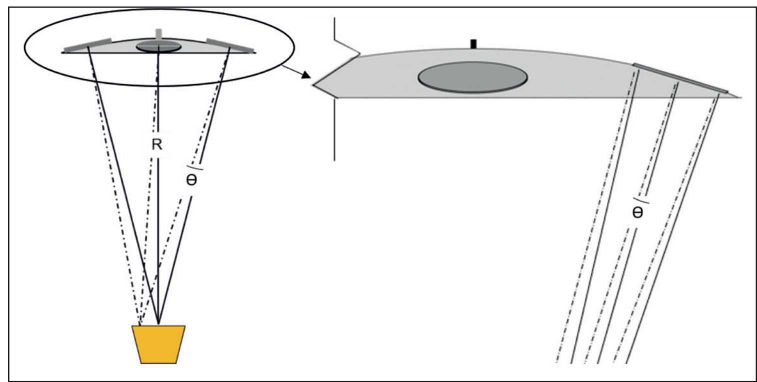


Figure 7.A crucible liner has effects similar to source-to-substrate misalignment.

PCM	Low Rate	Ramped rate
I_{off}	0.106 μA	0.192 μA
I_g	-0.218 μA	-0.349 μA

Table 1. Leakage comparison between POR and the ramp-rate group.

FURTHER READING

K. Cheng, "Elimination of Metal Fencing by Optimizing Evaporator Dome Alignment", IEEE Transactions on Semiconductor Manufacturing. 33 November 2020.

Pioneering N-polar HEMTs

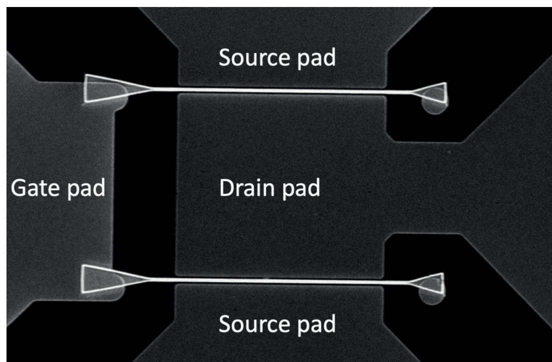
N-polar AlGaN-based HEMTs on AlN substrates offer great promise for excelling in RF performance and thermal management

A US COLLABORATION is claiming to have fabricated the first N-polar GaN/AlGaN/AlN HEMT on a single-crystal AlN substrate.

The team, a partnership between Cornell University, the University of Notre Dame and Asahi Kasei Corporation, says that these transistors have the potential to exploit the thermal and power-handling capabilities of AlN, as well as the merits of N-polar structures, such as a strong back barrier.

Another strength of these HEMTs, which feature AlN buffer layers, is that they don't require deep-level dopants. In comparison, conventional GaN-based HEMTs need deep-level dopants to compensate for the high unintentional doping concentration in the thick epitaxial GaN buffer layers, which are required to suppress the buffer leakage current and RF loss.

The team's latest breakthrough, which promises to utilise AlN for high-power, high-frequency and extreme environment applications, builds on its recent success in developing an *in-situ* cleaning technology for N-polar substrates, which led to the discovery of a two-dimensional electron gas in GaN/Al(Ga)N heterostructure on AlN substrates.



➤ A scanning electron microscopy image of a fully processed N-polar HEMT.

One of the virtues of growth on an AlN substrate is that it ensures a lower dislocation density in the epilayers, typically 10^4 - 10^5 cm^{-2}, compared with 10^9 - 10^{10} cm^{-2} for growth on foreign substrates, such as SiC, silicon and sapphire. What's more, the native substrate removes a high thermal boundary, which has been shown theoretically to overshadow the benefits of a higher thermal conductivity, such as that found in SiC. Commenting on the suitability of their choice of substrate for volume production, spokesman Eungkyun Kim remarks: "Bulk AlN substrates have already demonstrated their high potential as a promising platform for optoelectronics and power/RF devices, and we believe the cost and the availability of AlN substrates will improve as the growth technology becomes more mature."

Fabrication of the team's novel HEMTs began by loading 100 μm-thick Asahi-Kasei N-polar AlN substrates into a plasma-assisted MBE reactor and depositing a 1 μm-thick AlN buffer layer, followed by a 20 nm-thick $Al_{0.91}Ga_{0.09}N$ impurity blocking layer, a 8 nm-thick channel and a heavily-doped 6.4 nm-thick GaN capping layer, employed to enabled easy formation of non-alloyed ohmic contacts. After protecting the N-polar layer by blanket deposition of a 10 nm-thick Al_2O_3 layer via thermal atomic layer deposition, the team defined source and drain contacts by photolithography, and added a T-shaped gate by electron-beam lithography.

Electrical measurements revealed a contact resistance for the HEMT of 0.66 Ω mm. As there are reports in the literature of a contact resistance of just 0.14 Ω mm for other N-polar HEMTs, the team should be able to trim the contact resistance of its devices.

When moving from a long-channel HEMT to one with a T-gate, on-resistance fell from 4.12 Ω mm to 1.56 Ω mm and maximum drain current increased from 1.2 A/mm to 2.6 A/mm, traits indicative of good scaling behaviour.

Compared with a device with a 500 nm Al-polar AlN layer grown on SiC, the variant on the native substrate had a leakage current through the buffer that's lower by two orders of magnitude. The team attributes this superiority to the lower dislocation density in the epilayers.

RF measurements revealed a maximum oscillation frequency of 100 GHz and a cut-off frequency of 68 GHz, held back by a high parasitic source resistance and a low transconductance.

Kim admits that many electrical issues need to be addressed with these first-generation devices. "The most important areas to address right now are to achieve a higher transconductance, a lower gate leakage, and a larger breakdown voltage. Once we optimise the electrical properties of our HEMTs, we plan to take a deep dive into thermal properties and show that the heating problem can be solved at a device level by eliminating the thermal boundary resistance at the growth interface."

REFERENCE

➤ E. Kim *et al*. Appl. Phys. Lett. **122** 092104 (2023)

Refining the tunnel-junction in UV LEDs

Tunnel junctions with compositional grading and a high level of doping reduce the voltage drop in UV LEDs

ONE OF THE CHALLENGES with the UV LED is to develop a design that allows the injection of carriers into the device while avoiding optical absorption and a hike in the operating voltage.

Offering a breakthrough in this regard is a team from The Ohio State University and Sandia National Labs. They meet all these objectives with a AlGaN tunnel junction with compositional grading and a high level of silicon doping.

The external quantum efficiency for these devices is only just over 1 percent, but optimisation of the growth conditions for the active region and the introduction of extraction techniques could lead to higher values, according to team spokesman Agnes Maneesha Dominic Merwin Xavier from The Ohio State University.

The difficulties of carrier injection into UV LEDs are well known. It is challenging to make an ohmic contact to *p*-AlGaN, and replacing this with *p*-GaN or an AlGaN-based superlattice leads to absorption and electrical losses, respectively. Adding to the challenge, the acceptor activation energy in AlGaN is high, causing a low hole concentration in the *p*-type layers.

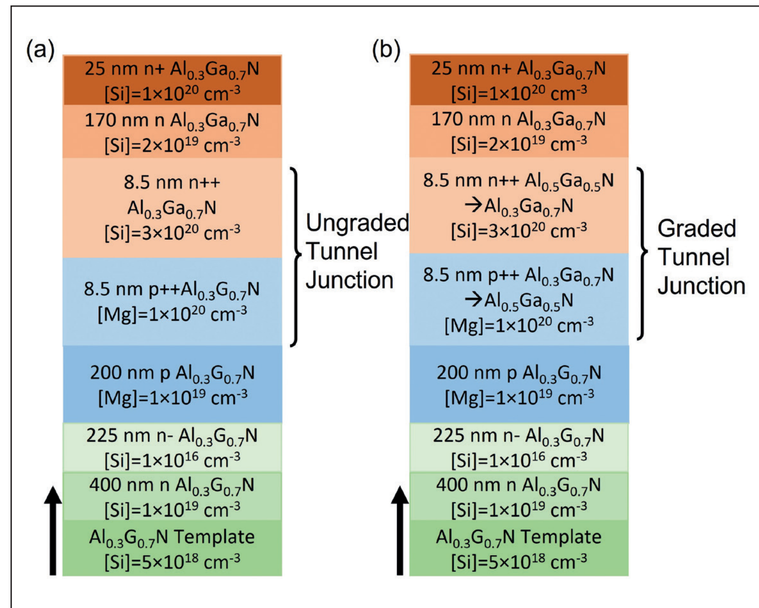
One way to address these issues is to introduce a tunnel junction. Other teams produce such structures by combining AlGaN with InGaN and GaN interlayers, but this leads to light absorption. Transparent homojunctions can combat this, but have higher voltage losses, compromising efficiency.

Dominic Merwin Xavier and co-workers avoid all these pitfalls with graded tunnel junctions that have an aluminium content of at least $Al_{0.3}Ga_{0.7}N$. This type of UV LED exhibits a voltage drop of just 1.86 eV across the tunnel junction at a drive current of 20 A cm^{-2}.

The development of these devices began with a study of the effects of grading in heterostructures featuring a *p*-*n* junction and a tunnel junction (see Figure for details of these structures, grown by MBE on MOCVD-grown *n*-type $Al_{0.3}Ga_{0.7}N$ templates). After etching to define square mesas, the team fabricated devices featuring top and bottom contacts.

Electrical measurements on these structures revealed that grading reduced the total voltage drop across the device at 20 mA cm^{-2} from 5.26 eV to 5.77 eV.

Modelling with Silvaco Atlas TCD offers some insight into the benefits of grading, including a large concentration of free carriers in the tunnel-junction region, induced by polarisation charges. Compared to a non-graded junction, that of AlGaN with aluminium graded from 30 percent to 50 percent delivered an eight-fold hike in hole concentration and a four-fold increase in the tunnelling rate.



➤ Comparing electrical characteristics of diodes revealed the benefits of a graded tunnel junction.

On-wafer measurements of 100 μm by 100 μm LEDs with the graded tunnel junction revealed a voltage drop of 5.55 V. The external quantum efficiency peaked at 1.02 percent for a drive current of 80 A cm^{-2}, and an increase in drive current from 100 A cm^{-2} to 350 A cm^{-2} produced a shift in the emission peak from 339 nm to 343 nm.

While MBE has been used to produce these devices, they could also be grown by MOCVD, a technology better suited to mass production.

Dominic Merwin Xavier says that by optimising the doping and grading of the tunnel junction layers, the approach the team has used to make devices emitting above 300 nm could be extended to UVC LEDs, which emit below 280 nm. "However, there may be a higher voltage penalty as the composition of the AlGaN layers increase."

She says that the next goal for the team is to extend their design and optimise the tunnel junction for low voltage UVC tunnel-junction LEDs.

REFERENCE

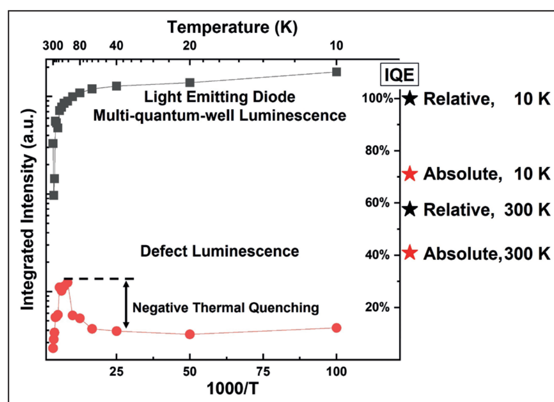
➤ A. M. Dominic Merwin Xavier *et al.* Appl. Phys. Lett. **122** 081108 (2023)

Debunking a dubious assumption

Assuming a perfect internal quantum efficiency at temperatures approaching absolute zero is not justified, according to modelling of photoluminescence data

ONE OF THE widely held assumptions with our community is that the internal quantum efficiency (IQE) of light-emitting structures reaches 100 percent at very low temperatures. But this view is incorrect – and it can even be very wide of the mark – according to Can Bayram and co-workers from the University of Illinois at Urbana-Champaign (UIUC).

The team's finding has tremendous implications for IQE measurements of LEDs and lasers. IQE is a crucial metric for evaluating these light emitters, which have roadmaps for increases in efficiency that will ensure a trimming of CO_2 emissions. For example, the US Department of Energy is pushing for an increase in blue LED efficiency from 70 percent to 90 percent by 2035, an improvement that could deliver annual energy savings of 450 TWh.



➤ UIUC reports the absolute internal quantum efficiency of a generic blue LED on silicon (111) to be as low as 71.1 percent at 10 K – far from the assumed 100 percent.

Bayram told *Compound Semiconductor* that for many years, he has harboured concerns relating to the measurement of IQE: "The community does not have an 'absolute' basis for assessing LEDs or photonic structures, and has no consensus means of comparing IQE values from the large variety of structures across research/publishing groups." Bayram wants to see the community establish an "absolute" IQE measurement that would ensure robust comparisons of: devices by different vendors, designs by different research groups, and materials from different growth chambers.

Another problem that comes from assuming a perfect IQE at low temperatures – this might be 4K, 10 K or even 77 K – is that it leads to a misrepresentation of the origins of losses, along with misappropriation of losses to other effects.

The approach UIUC takes shares some similarities with the standard approach for measuring IQE, which involves measurements of photoluminescence at different temperatures. However, Bayram and colleagues don't simply compare the total intensity of the main multi-quantum-well luminescence at different temperatures. Defect luminescence behaviour is included, alongside its negative thermal quenching action that impacts the primary luminescence peak.

Bayram and co-workers have investigated an GaN-based LED on sapphire, grown by Chinese vendor Xiamen, as well as an LED grown on silicon by Veeco.

Atomic force microscopy uncovered V-shaped defects and spiral hillock-like steps on the surfaces of the LEDs with a sapphire and a silicon foundation, respectively. This form of microscopy also determined values for the defect density: 6×10^9 cm^{-2} for the LED on sapphire, and 5×10^8 cm^{-2} for that on silicon. X-ray reciprocal space mapping and Raman spectroscopy revealed that the degree of compressive strain is higher in the LED on sapphire.

Photoluminescence spectra from the two types of LED at a range of temperatures revealed blue emission from the active region, along with: a broad yellow luminescence; UV emission; near band-edge emission; and a broad red luminescence, restricted to just the LED on silicon. Plotting integrated intensities for each of these peaks as function of temperature revealed a quenching of the highly luminescent multi-quantum-well emission, coinciding with a rise in defect luminescence, due to a redistribution of carriers.

From the increase in this intensity and subsequent modelling drawing on data such as device strain, the team determined values for IQE for the LEDs grown on silicon and sapphire of 71 percent and 28 percent, respectively. The latter is "very low compared to what can be achieved today," says Bayram.

He and his co-workers will now study LEDs from various vendors, comparing values for IQE from optical and electrical measurements.

"We believe the path to the world's most efficient, next-generation LEDs will require new assessment techniques," adds Bayram. These will be employed to compare conventional and novel LEDs, such as those with a cubic geometry.

REFERENCE

➤ Y. Chiu *et al.* Appl. Phys. Lett **122** 091101 (2023)

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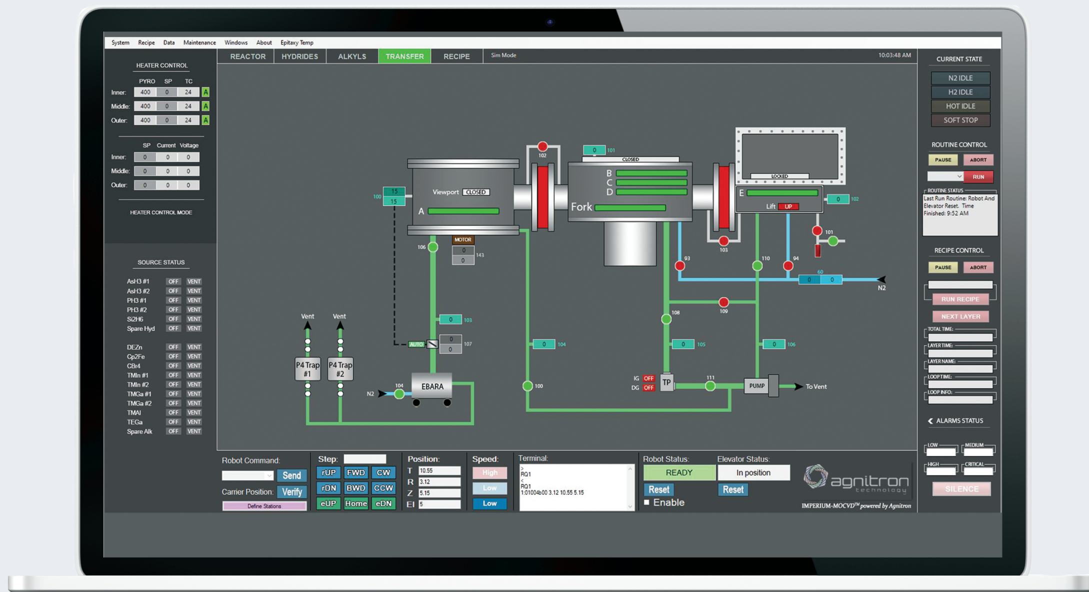

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