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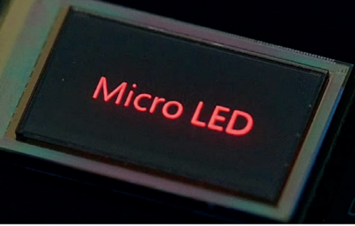

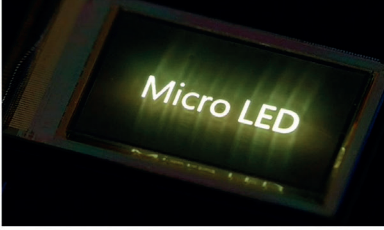

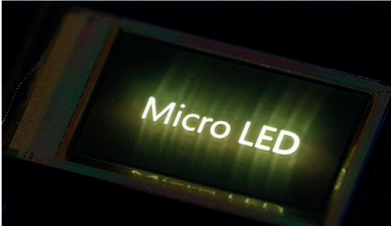

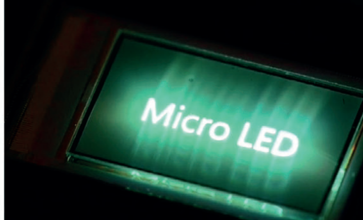

POLYCHROMATIC PIXELS

VOLUME 30 ISSUE III 2024

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

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INSIDE

News, Analysis, Features, Editorial View, Research Review and much more

Ultraviolet LEDs go micro

Shrinking UV LEDs to a micron or so delivers multiple benefits, including higher efficiencies and new opportunities

Scrutinising the gate atom by atom

Atom probe tomography unveils the distribution of elements at the key interface of the SiC MOSFET

Opportunities for InAlN-based HEMTs

Pairing InAlN/GaN HEMTs and GaN-on-insulator technology ensures monolithic integration of high-frequency GaN and CMOS

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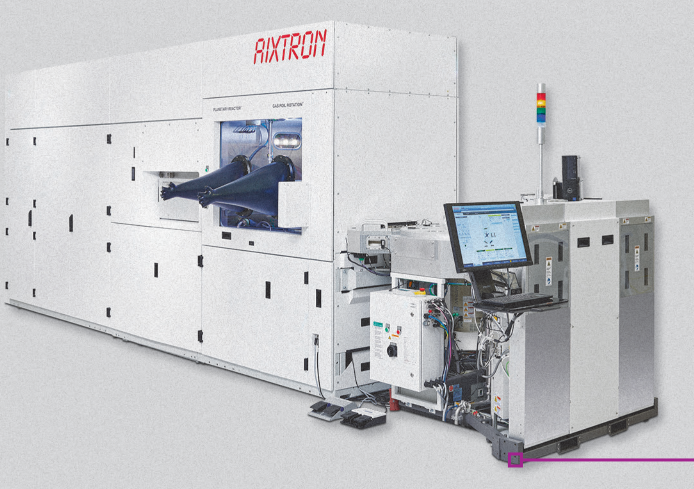

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VIEWPOINT

By Richard Stevenson, Editor

Mulling over the future of the microLED

It's rare that news within our industry truly shocks me. But this happened recently, when Apple decided to abandon its plans to manufacture a new generation of Smartwatches with microLEDs made by ams Osram.

I have much sympathy for Osram. Listening to its hastily arranged conference call left me in no doubt whatsoever that this chipmaker failed to see the coming of this crushing announcement. You have to feel for the company, given that it seems to have kept its side of the bargain, making timely progress with its technology, as well as building a new fab in Malaysia dedicated to high-volume production of microLEDs.

While it's never easy to know exactly where the fault lies, it would appear that Apple's concerns were not with the microLEDs themselves, but the methods used to pick them up and make displays. That's not surprising, given that many have raised the alarm over the difficulties in picking and placing individual emitters, and what's needed to make this process commercially viable.

Apple's about turn has to be a major concern for all those with an interest in microLEDs. While these miniature marvels outperform OLEDs, which are the incumbent technology for Smartwatch displays, the performance gap is shrinking all the time.

One after-shock from Apple's action is going to be a reluctance from investors to put their cash behind microLED start-ups. So, if the microLED industry is to blossom, progress is probably going to have to come from those already refining their technology.

Against this backdrop, one potential game changer is the polychromatic pixel, an emitter that eradicates the need to produce and manoeuvre millions of individual red, green and blue chips. Detailing the merits of this approach in the pages of this edition is a pioneer of this approach, Q-Pixel (see p. 18). This start-up argues that compared to its rivals that are also developing this novel form of emitter, its microLEDs require a smaller voltage range to realise colour tuning, simplifying the drive electronics. Q-Pixel also boasts a number of world records: the smallest ever full-colour pixel, having an emitter diameter of just 1 μm; the highest pixel density for a display, of 10,000 pixels per inch; and the highest resolution for an active matrix colour display – it's 6,800 pixels per inch.

I wish Q-pixel well, along with its rivals. After all, it would be great for all the efforts at developing the microLED to lead to commercial products. But as well as that, I hope that there is a new future for Kulim 2, Osram's new fab. This building of the world's first high-volume 200 mm LED fab is a milestone for our industry, and it would be a great shame if all the expenditure, in both time and money, failed to bare any fruit.

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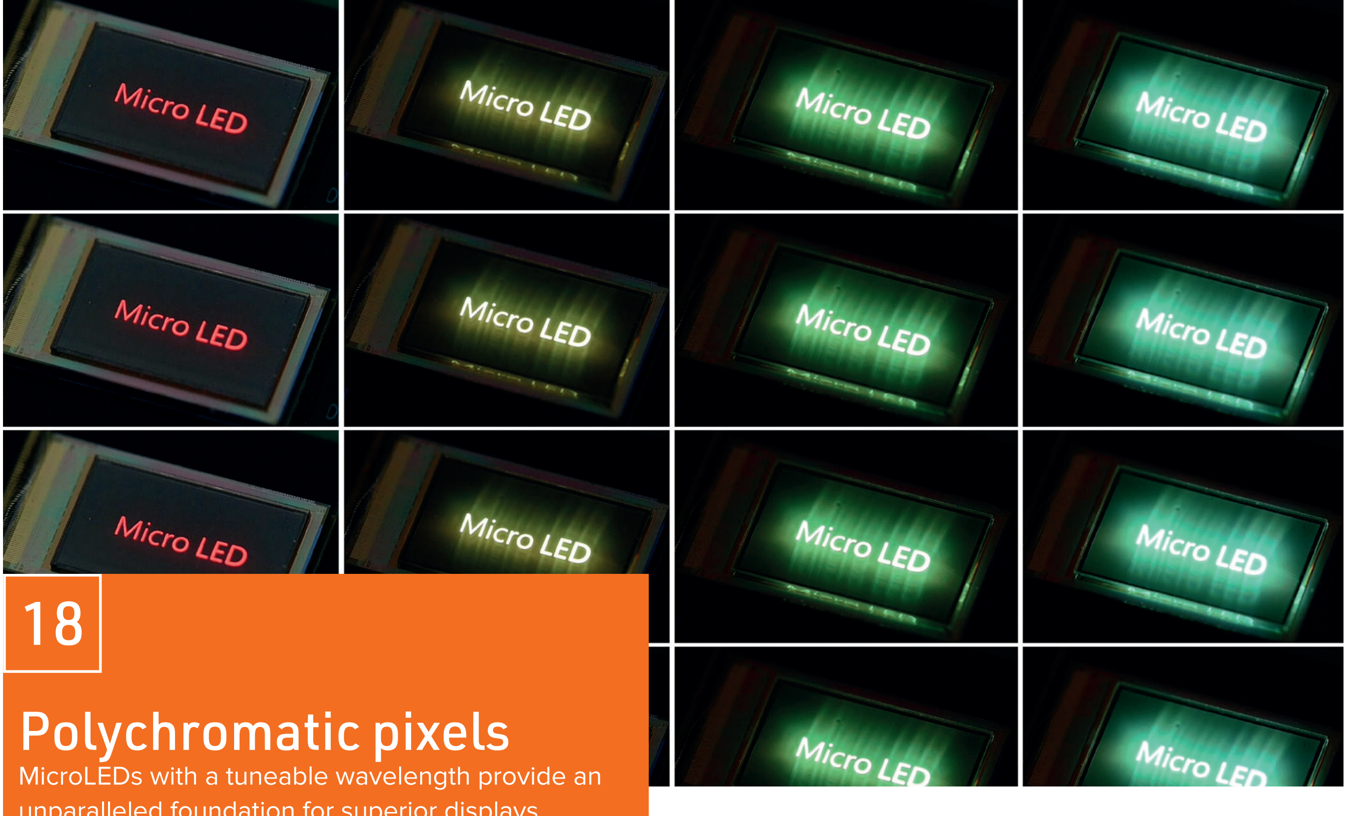

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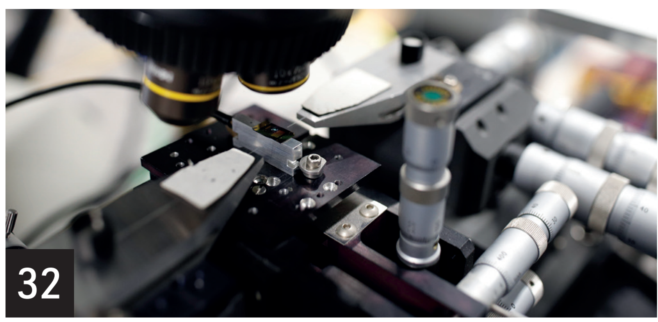

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SiC fabs continue to ramp

SiC power device to reach $5.33 billion by 2026, according to TrendForce

ACCORDING TO TrendForce, the SiC power device market is expected to reach $5.33 billion by 2026, with mainstream applications highly reliant on electric vehicles and renewable energy sources.

Recently, the widely-publicised SiC market has seen new developments involving companies such as Mitsubishi Electric, Mersen, and Ascen Power.

According to recent reports from Nikkei, Mitsubishi Electric plans to commence construction of a new 8-inch SiC fab in Kumamoto Prefecture, Japan, in April 2024, with operations scheduled to start in April 2026.

The new fab, spanning six floors with a total floor area of around 42,000 m^2, will primarily handle front-end processes for 8-inch SiC wafers. Mitsubishi plans to gradually increase capacity, aiming to increase SiC production capacity by five times by the fiscal year 2026 (compared to fiscal year 2022).

Recently, Shao Yonghua, the plant manager of Ascen Power's fab, announced that the company plans to produce 240,000 pieces of 6-inch automotive-grade SiC chips annually by the end of this year. The reserved 8-inch production line is next to the 6-inch line and will have the capability to produce 240,000 pieces of 8-inch automotive-grade SiC chips annually once completed.

Ascent Power's SiC chip manufacturing project is a major project under Guangdong's *Strengthening Chip Technology Project* with a total investment of around $1 billion, covering an area of 150 acres.

In November 2022, the project's clean room was officially put into use, achieving a monthly production capacity of 10,000 pieces. Its automotive-grade and industrial-grade chips have been successfully mass-produced and sampled, and these chips are about to complete the automotive verification.

On March 12, European graphite materials and SiC wafer supplier Mersen announced that it has received investment from the French government for capacity expansion of its SiC wafer project. The subsidy amount may exceed €12 million, .

Mersen intends to advance the research and industrial production of *p*-SiC wafers with this investment. *p*-SiC is a low-resistivity polycrystalline SiC wafer that can be combined with single-crystal SiC active layers, enabling SiC device manufacturers to improve production yield and transistor performance.

Infineon introduces next-gen CoolSiC MOSFETs

INFINEON has introduced the next generation of SiC MOSFET trench technology. The company says that its CoolSiC MOSFET 650 V and 1200 V Generation 2 improve MOSFET performance figures, such as stored energies and charges, by up to 20 percent compared to the previous generation.

A DC fast-charging station for electric vehicles, which is equipped with CoolSiC G2, allows for up to 10 percent less power loss compared with previous generations, while enabling higher charging capacity without compromising form factors. Traction inverters based on CoolSiC G2 devices can further increase electric vehicle ranges. In the area of renewable energies, solar inverters designed with CoolSiC G2 make smaller sizes possible while maintaining a high power output, resulting in a lower cost-per-Watt.

"Megatrends call for new and efficient ways to generate, transmit and consume energy. With the CoolSiC MOSFET G2, Infineon brings SiC performance to a new level," said Peter Wawer, division president Green Industrial Power at Infineon. "This new generation of SiC technology enables the accelerated design of more cost-optimised, compact, reliable, and highly efficient systems harvesting energy-savings and reducing CO_2 for every watt installed in the field. It's a great example of Infineon's relentless spirit, constantly pushing for innovation to drive decarbonisation and digitalisation in the industrial, consumer and automotive sectors."

Infineon says its pioneer CoolSiC MOSFET trench technology provides an optimised design trade-off, allowing higher efficiency and reliability compared to SiC MOSFET technology available so far. Combined with the award-winning .XT packaging technology, Infineon is further increasing the potential of designs based on CoolSiC G2 with higher thermal conductivity, better assembly control and improved performance.

NCT grows 6-inch gallium oxide crystal

Vertical Bridgman technique paves way for larger high-quality wafers

NOVEL CRYSTAL TECHNOLOGY (NCT), a specialist in Ga_2O_3 technology, has successfully grown the first 6-inch Ga_2O_3 single crystal using the Vertical Bridgman (VB) technique.

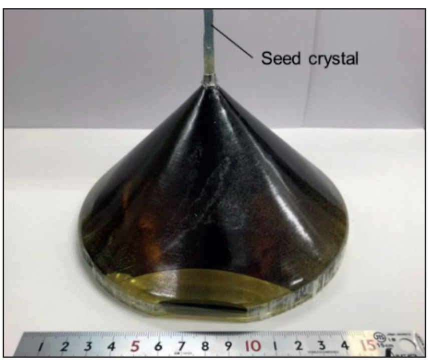
This achievement marks a significant step forward in NCT's efforts to deliver larger, high-quality semiconductor wafers for Ga_2O_3-based power devices.

The development of the VB growth technique for Ga_2O_3 single crystals (pictured below) was initiated by Shinshu University, successfully achieving growth of 2-inch and 4-inch crystals. NCT acquired and extended their techniques to enable larger-diameter crystal development.

The VB technique offers several advantages over NCT's existing Edge-defined Film-fed Growth (EFG) method. By growing the crystal in a cylindrical shape, VB significantly reduces costs associated with substrate cutting.

Additionally, it allows for production of substrates in various crystalline orientations, unrestricted by limitations imposed by crystal anisotropy.

Furthermore, the controlled thermal environment of VB growth leads to superior crystal quality with minimal defects, compared with EFG. Finally,



dopant uniformity within the substrate is expected to improve, aligning with industry standards for other semiconductors like silicon.

NCT carried out a comparative evaluation between VB and EFG crystals with National Institute of Advanced Industrial Science and Technology (AIST). This revealed a dramatic improvement in crystal quality.

Synchrotron radiation X-ray topography analysis confirmed minimal defects in the VB-grown crystal, compared with the high density of defects observed in the EFG-grown crystal. This clearly demonstrates the superiority of the VB technique for producing high-quality Ga_2O_3 substrates.

Established in 2015, NCT manufactures 2-inch and 100 mm Ga_2O_3 substrates and epi-wafers for power devices. These are commercially available and used by universities, institutes, and power-device companies worldwide.

NCT is actively developing larger substrates such as 6-inch. Beyond substrates, NCT has a vision for broader Ga_2O_3 device production. It is already offering samples of their first Ga_2O_3 Schottky barrier diode, with qualification tests expected to be completed in September 2024.

This research and development program was partially funded by the Adaptable and Seamless Technology Transfer Program through Target Driven R&D (A-STEP) of the Japan Science and Technology Agency (JST).

We cordially invite you to join the Institute of Novel Semiconductors at Shandong University

1. About Us

The Institute of Novel Semiconductors is a key academic special zone supported by Shandong University. Leveraging the solid foundation of Shandong University in the field of semiconductor material research, the institute aims at the future development direction of semiconductor material technology. It focuses on the major demands in energy, information, rail transit, and other fields, cultivating the development of new generation wide bandgap and ultra-wide bandgap semiconductor single crystal materials, enhancing breakthroughs in key technologies of semiconductor devices, and promoting application demonstrations in typical application fields.

2. Application Conditions

(A) Basic Conditions

1. Born after January 1, 1969 (inclusive);
2. In principle, should have a Ph.D. degree;
3. Have obtained a formal teaching or research position at overseas universities, research institutions, or corporate R&D institutions;
4. Have-obtained researchor technical-achievements recognized-by peers in the field,and havethepotential-to-becomea leading-academic-or-outstanding-talent-inthefield.

(B) Research Directions and Professional Fields

Growth of new generation semiconductor single crystal materials such as silicon carbide, gallium nitride, gallium oxide, diamond, aluminum nitride, boron arsenide, thin film growth, substrate processing, advanced laser technology; fabrication of power devices, optoelectronic functional devices, acoustic devices, microwave devices; and the related technology fields of packaging testing, modules, etc.

3. Compensation and Benefits

(A) **High Starting Point for Career Development:** Eligible for appointment as a professor and doctoral supervisor;
(B) **Competitive Salary:** Comprehensive annual salary not less than 600,000 RMB, with no cap on total income;
(C) **Sufficient Research Funding:** Research funding ranging from 3 to 10 million RMB during the employment period;
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(E) **High-Quality Team Resources:** Provides full quotas for recruiting PhD students and postdoctoral researchers during the employment period;
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Wolfspeed tops out world's largest SiC fab

$5 billion investment aims to help accelerate transition from silicon to SiC

WOLFSPEED has celebrated the topping out of construction at the $5 billion John Palmour Manufacturing Center for SiC, hosted by Senator Thom Tillis and other local officials. Located in Chatham County, North Carolina, the JP will produce 200 mm SiC wafers, significantly expanding Wolfspeed's materials capacity, and meet the demand for next-generation semiconductors critical to the energy transition and AI.

"We are excited to mark this critical milestone alongside our hard-working team, loyal customers, community partners, and ardent supporters like Senator Thom Tillis," said Wolfspeed president and CEO, Gregg Lowe (pictured above right, with Tillis). "This facility is a testament to Wolfspeed's commitment to our local community and domestic workforce, furthering our position as the global leader in SiC production. The JP will help maintain America's lead in energy innovation, and unlock significant benefits for our local community by growing the state's economy by more than $17.5 billion over the next two decades and creating 1,800 good-paying jobs by 2030."

"Wolfspeed's $5 billion investment in Chatham County is another example of why North Carolina is the best state in the country to do business," said Senator Tillis. "I was proud to vote in favour of the CHIPS and Science Act, which provides critical support for domestic semiconductor manufacturing, and I applaud Wolfspeed's commitment to developing technology here in North Carolina that supports our national security and economic interests."

The JP represents a total investment of $5 billion, complemented by public and private support, to help accelerate the transition from silicon to SiC and

ramp up supply of this material recently deemed as critical to the energy transition by the US Department of Energy. By the end of 2024, phase one of construction is expected to be completed on the 445-acre site.
The ramp of the JP will support recently signed customer agreements with Renesas, Infineon, and additional companies, while driving meaningful progress towards Wolfspeed's long-term growth strategy.

Vishay acquires Newport Wafer Fab for $177 million

Acquisition accelerates Vishay's SiC production plans

US-BASED Vishay Intertechnology has completed the acquisition of Nexperia's wafer fabrication facility and operations located in Newport, South Wales, UK, for approximately $177 million.

The Newport wafer fab, located on 28 acres, is an automotive-certified, 200 mm semiconductor wafer fab with capacity to produce more than 30,000 wafers per month. The fab is the UK's largest semiconductor fab with a long history in supplying components to the automotive and industrial markets.

Vishay plans to position the facility as a manufacturing excellence centre focusing on net zero transformation of decarbonisation and electrification.

As a new member of the Compound Semiconductor Cluster in South Wales, Vishay plans to collaborate with local universities and others in the UK to enhance its research and development efforts on power compound semiconductors.

"The acquisition of Newport aligns with the strategic shift the Board envisioned with its decision to appoint new leadership. Under Joel's leadership, Vishay is making this shift, investing in technologies and incremental capacity to drive faster growth and enhance returns to stockholders. The goal is to prepare Vishay to capitalise on the megatrends of e-mobility, sustainability, and connectivity," said Marc Zandman, executive chairman of the board.

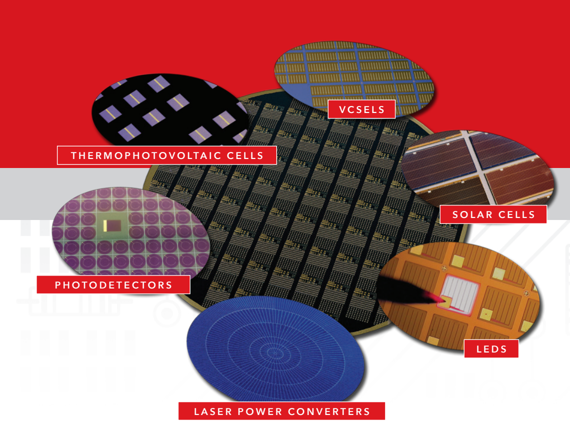
"With a Vishay-owned fab to qualify and scale our SiC portfolio, we are accelerating our participation in the SiC MOSFETs and diodes marketplace, as desired by our customers," said Joel Smejkal, president and CEO of Vishay.

He remarked: "In late 2022, the MaxPower acquisition advanced our SiC intellectual property and MOSFETs product technology. We are excited to further develop our SiC and GaN technology as a new member of the Compound Semiconductor Cluster in South Wales."

"We welcome the highly skilled and dedicated employees at the Newport wafer fab into the Vishay family. Vishay is committed to investing in Newport to grow capacity, and to accelerate our SiC and GaN production and technology development. We look forward to the contributions of Newport's employees to our shared success," added Smejkal.

The transaction was funded by Vishay with cash on-hand. To affect the transaction, Vishay acquired a 100 percent interest in the legal entity Neptune 6 Limited, and its wholly-owned operating subsidiary, Nexperia Newport Limited, which owns and operates the Newport facility.

Neptune 6 Limited is expected to be renamed 'Vishay UK Holdings Limited' and Nexperia Newport Limited is expected to be renamed 'Vishay Newport Limited'.



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Global LED demand rebounds

Revenue expected to grow 3 percent in 2024 with market focus on automotive displays, says TrendForce

TRENDFORCE'S latest LED industry report indicates that the global market is set to recover in 2024, with estimated revenues reaching $13 billion – marking a year-over-year growth of 3 percent.

This resurgence is primarily driven by demand across various sectors, including automotive lighting and displays, general/architectural/agricultural lighting, LED video walls, and UV/IR LEDs. Additionally, the successful deployment of microLEDs in large displays by Samsung and luxury watches by Tag Heuer has played a significant role in this growth.

TrendForce points out that automotive displays present significant growth potential this year. Thanks to momentum from the NEV market, advanced technologies like ADB headlights, miniLED taillights, full-width taillights, smart ambient lighting, and miniLED backlit displays are set to propel the automotive LED market value to $3.4 billion. Furthermore, the microLED is making inroads into reading lights and control knobs in European OEMs.

Meanwhile, European, US, and Japanese automakers plan to introduce microLED transparent displays. With automakers requiring microLED HUDs to achieve a transparency rate exceeding 70 percent and accommodate curved designs, the automotive market is set to embrace transparent microLED displays for AR-HUD or window displays by 2026–2027 as the technology matures and becomes more cost-effective. The miniLED video wall market is witnessing rapid growth, propelled by leading manufacturers like Samsung, LG Electronics, Leyard, Unilumin, and Absen.

In the UV LED segment, manufacturers continue to roll out high-power sterilization and purification products to meet market demands. The application of UV-C LED in air sterilization by Huawei AITO – with orders spanning 2023 to 2025 – is poised to hasten the adoption of automotive air sterilisation applications. Compared to traditional UV lamps, UV LEDs offer a longer lifespan and simpler optical design. Companies such as Nichia, Seoul Viosys, and Violumas have launched comprehensive UV-A/B/C LED product lines to satisfy the demand for UV lamp alternatives.

Agricultural lighting is gaining momentum in Central and Eastern Europe, particularly in Czechia and Poland, where the cost reduction of horticultural lighting end products has improved the ROI of plant factory solutions. Furthermore, investments in horticultural lighting for cultivating vegetables and fodder in high-latitude Asian and Nordic regions aim to mitigate the adverse effects of prolonged winters on food suppliers, promising to uplift the horticultural lighting LED market in 2024.

World's first 6-inch InP scalable wafer fabs

COHERENT has established the world's first capability for 6-inch InP wafer fabrication, in the company's Sherman, Texas, and Järfälla, Sweden, wafer fabs.

This milestone enables Coherent to increase production capacity and lower die costs for InP optoelectronic devices, widely used in applications such as coherent optical communications, datacom transceivers, AI interconnects, advanced sensing for consumer electronics and wearables, medical and automotive applications, and, in the future, in 6G wireless and satellite communications networks.

"We are very excited to announce our 6-inch InP wafer fabrication capability in both our Sherman and Järfälla fabs, which is a result of our continuous investment in innovation and technology development, and our years of investment and operating experience in high-volume VCSEL array manufacturing for mobile handsets," said Giovanni Barbarossa, chief strategy officer and president, Materials Segment.

"Vertical integration at scale is a core strategy that we have been relying upon in several of our markets, and it has enabled our optoelectronics products to win in the marketplace by delivering world-class quality, performance, time-to-market, and cost advantage."

"Moving to 6-inch wafers will enable us to continue to deliver massive productivity improvements, including manufacturing 4 times the number of devices per wafer, achieve a greater than 60 percent reduction in die cost, and allow us to transition our fabs to higher-capacity, more-efficient automated process tools," said Beck Mason, executive VP, Telecommunications.

Innoscience denounces Infineon accusations

Innoscience claims that Infineon's lawsuit, filed in the US, will have little to no effect on its capability to import products to that country

INNOSCIENCE TECHNOLOGY has countered the accusations made by Infineon in a recent patent infringement lawsuit.

The lawsuit, filed in the district court of the Northern District of California, concerns a US Infineon patent covering core aspects of the company's GaN power semiconductors around reliability and performance. Infineon is seeking a permanent injunction against Innoscience.

Infineon alleges that Innoscience infringes the Infineon patent by making, using, selling, offering to sell and/or importing into the United States various products, including GaN transistors for numerous applications, within automotive, data centres, solar, motor drives, consumer electronics, and related products used in automotive, industrial, and commercial applications.

Innoscience says it denies Infineon's allegations of patent infringement as well as the validity of the Infineon patent. It also questions Infineon's intention with this litigation.

"Even a cursory review of Infineon's patent portfolio reveals that the alleged 'invention' of the asserted patent was already disclosed in Infineon's own earlier prior art patents, raising concerns that it may have committed fraud on the United States Patent and Trademark Office, for not making proper disclosures during the prosecution of the asserted defective patent," states Infineon in a press statement.

In addition, Innoscience says that contrary to Infineon's wrong characterisation that the claims of the asserted defective patent 'cover core aspects of GaN power semiconductors,' the lawsuit only concerns a small fraction of Innoscience's packaged high-voltage (650 V - 700 V) GaN transistors. It does not affect the vast majority of its other products (including unpackaged transistors and wafers, low-voltage transistors, and certain packaged transistors).

Therefore, the lawsuit should have little to no effect on Innoscience's current ability to make, use, sell, offer to sell, or import into the United States its products for customers.

Germanium's great versatility

As well as providing a great foundation for multi-junction solar cells and VCSELs, germanium substrates can provide a unifying force between the compounds and the silicon industry

BY BENDIX DE MEULEMEESTER FROM UMICORE

WHAT IS the germanium substrate used for? If you are a veteran of this industry, you'll surely have an answer to this, as you'll know that it is widely used as the bedrock for producing multi-junction solar cells, which now power numerous satellites orbiting our planet. That's the market that sparked the launch of the commercial germanium substrate in the 1990s, and accounted for all of its use for the first 20 years or so. But during the last decade, this platform has started serving other applications, a direction of travel that is sure to continue. You might be aware of some of these new uses – but there's a good chance that others will come as a surprise.

On the back of the success of highly efficient multi-junction cells in space, many companies tried to diversify this technology to the terrestrial solar market. Interest in this rocketed during the beginning of this century, before pioneers were forced to abandon their plans, thwarted by plummeting prices for silicon panels and a global credit crunch that chocked investment.

Now, though, there is hope of a rival, with a modified form of concentrated photovoltaics, which combine the generation of electricity from the sun's rays with the storage of thermal energy. The latter allows the opportunity to power the grid precisely when it is needed. For this new form of green-energy generation, solar cells must be as thin as possible to ensure efficient cooling and recovery of heat. Addressing this requirement is a cost-effective germanium wafer re-use technology, currently under development and testing, that could provide a compelling alternative to the substrate thinning approach performed by a grinding process.

Optoelectronic opportunities

Over the last few years, the usage of germanium substrates has started to branch out into other optoelectronic applications. You may have come across the development of GaAs-based VCSELs on this foundation. Interest in this particular substrate stems from its superior material properties, compared with GaAs, for epitaxial growth of compound semiconductors. Key merits of germanium are a lattice constant between that of GaAs and AlAs, and a matching thermal expansion coefficient. These attributes make germanium an ideal substrate for the epi-growth of photonic devices incorporating distributed Bragg reflectors based on the pairing of GaAs and AlAs.

The VCSEL is by no means the only optoelectronic device that can benefit from germanium. This substrate could offer great value in next-generation, high-volume photonic applications, such as microLEDs, still a promising source for displays, despite Apple's headline-grabbing decision to move away from working with ams Osram. High volumes will be aided by the size of this foundation, available in the form of dislocation-free wafers with diameters of 200 mm and even 300 mm. As well allowing for more devices to be fabricated per wafer, significantly improving throughput and reducing cost per device, these large wafers have the advantage of enabling processing in state-of-the-art silicon foundries. Utilising existing silicon manufacturing infrastructure is a big win, slashing costs and streamlining production processes.

Note that after the growth of microLEDs on germanium, substrate removal is required to enable integration with the backplane. The good news is that substrate removal technology is advancing, due to efforts in concentrated photovoltaics.

It is also possible to integrate III-V photonics on germanium substrates, opening new avenues for device architecture and functionality. These new directions can involve the monolithic integration of photonic and electronic components, essential for developing more compact and efficient high-performance optoelectronic systems. Integration is particularly beneficial in space-limited high-volume consumer applications, such as time-of-flight-based depth sensors.

What's more, engineers can draw on the low-bandgap of germanium to support their development of advanced photonic devices for data communication in the short-wave infrared. And there are opportunities to exploit next-generation complementary FETs, with improved performance characteristics.

A logical extension

Even more exciting is the radical move of integrating compound semiconductors with existing silicon logic platforms. This holds profound implications for the advancement of photonics and electronics, promising enhancements in performance, efficiency, and scalability that were previously challenging to achieve.

With so many opportunities for the germanium substrate, are there concerns over material supply? No – and that will remain, given that germanium recycling is easy. The substrate can be removed by grinding or selective etching, and germanium can be 100 percent recycled for re-use, limiting reliance on primary raw materials.

Thanks to such a promising future, which is not held back by supply issues, there's a very bright future ahead for germanium.

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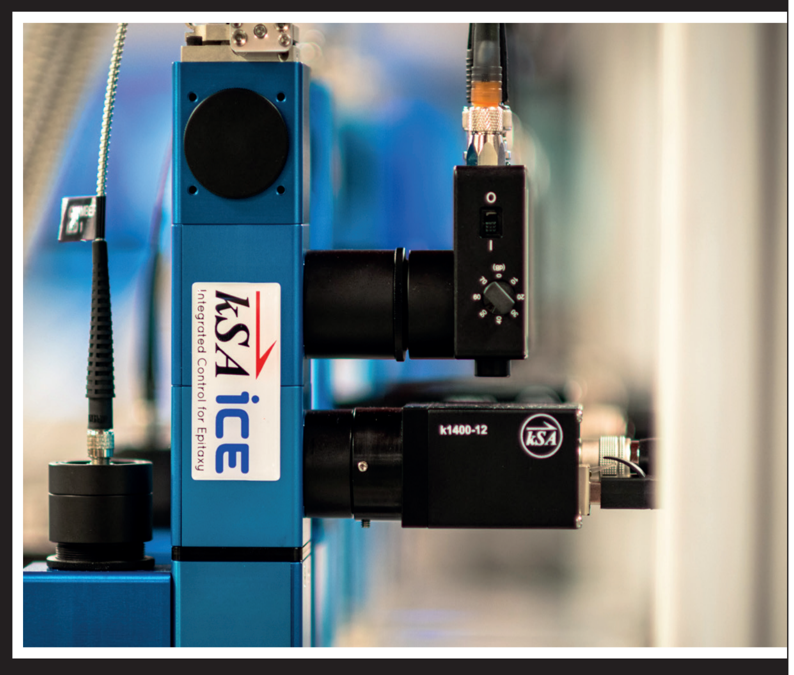

A fatal blow for the microLED?

By pulling the plug on its supply agreement with Osram, Apple's actions have sent shock waves through the fledgling microLED industry

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE NASCENT microLED industry has been plunged into jeopardy, following Apple's decision to terminate its supply deal with ams Osram. Apple's action, which caused Osram share price to plummet by 40 percent, has led this chipmaker to consider selling its second fab in Malaysia, built solely for the production of microLEDs for Apple Smartwatches.

According to Eric Virey, a Principal Analyst from Yole Group, Apple's move has widespread implications, including delivering a massive and devastating blow to the microLED industry.

Virey points out that Apple has played a major role within this space for many years, having created the microLED industry through the acquisition of start-up Luxvue in 2014. "From that moment, dozens of startups and most OEM and display makers started investing in the technology."

However, Virey believes that there is still a possibility that Apple has not inflicted a fatal blow to the microLED industry.

"If Apple had pulled the plug two or three years ago, we are confident this would have been a death sentence for the industry. However, the situation is different now: we consider that with sizable investments across all players and continents, the microLED industry has now gained enough momentum to continue on its own, although on a different path, with an immediate focus on applications where microLEDs can offer highly differentiating performance and functionalities."

Promising opportunities for the microLED exist in the automotive industry, in augmented reality, and a variety of display technologies, according to Virey.

Despite ditching its partnership with Osram, Virey does not expect Apple to turn its back on the microLED: "We believe the company is still very interested in the technology, but will no longer try to develop its own technology and supply chain."

Instead, Virey expects Apple to continue evaluating technologies and products developed externally, and to potentially adopt microLED displays developed by suppliers in some of its products, if and when it makes sense for them.

For Virey, Apple's recent decision did not come as a great shock, as he viewed the project as challenging and risky.

"The multiple slips in Osram's microLED fab ramp-up timeline indicated that Apple and its other partners were encountering problems and delays downstream, especially with the mass transfer and assembly of the microLED on the backplane and overall process integration," remarks Virey, adding: "Yields remained low, which was a major challenge in meeting cost targets."

Over the last two years, Virey and his colleagues have been arguing that the microLED Smartwatch project at Apple has been an incubator, not only

for the company and its partners, but for the whole microLED industry.

"We continually warned the industry that the failure of this project remained a possibility despite the strong commitment and sizable investments made by Apple and its partners."

The levels of investment are certainly eye-wateringly. Apple spent more than $2.6 billion to develop microLED displays, plus $420 million acquisition of Luxvue, and Osram invested $1 billion on its Kulim 2 fab. In addition, Apple's partners, such as LG and Kullicke & Soffa spent considerable sums to prepare to ramp manufacturing for the first microLED Apple watch, which had been scheduled to hit the market in 2026.

A state of shock

Responding to Apple's decision, Osram's leaders held a conference call to discuss the implications on 29 February.

Osram's CTO, Rainer Irle, highlighted the company's progress, saying that it had built Kulim 2, the world's first high-volume 200 mm LED fab, in record time, and had made a huge commitment to deliver microLEDs to its former partner.

"We thought everything is on track, and then came that sudden change in the strategy of our customer. We don't understand where that suddenly came from, so we're very disappointed."

Echoing this view, company CEO Aldo Camper added that while there was still some work to do, he had confidence that all the remaining 'riddles' could be solved.

Osram has calculated that the impairment cost associated with the Kulim 2 fab, its equipment, and the R&D expenditure associated with developing the microLED technology totals €1.3 billion.

"Out of the 1.3 billion, we have to write off 600 to 900 million. That includes the equipment that is still on order," said Irle. As Osram will no longer produce any samples in its Kulim 2 fab, the operating costs of running this facility will fall. However, the company will have to keep running the heating, ventilation and air-conditioning system to maintain the value of the cleanroom.

Despite the axing of future business from Apple, Osram's future is not in jeopardy, due to its strong position in other markets that use LEDs. According to Kamper, Osram is the well-established leader in the production of LEDs for the automotive market, and enjoys healthy sales in medical, industrial and consumer sectors.

Sales of microLED to Apple would only have started to make a small impact to revenue in 2026 – and for that year the revised revenue growth is 6-8 percent, down from 6-10 percent.

With available capacity at Kulim 1 and Osram's fab in Regensburg, Germany, the company has no plans to use Kulim 2 to produce its existing LED portfolio. Selling Kulim 2 is an option, but negotiations are complicated by a sale-and-leaseback arrangement for the facility, initiated in October 2023 to release proceeds of around €400 million.

As well as having to consider the future of that fab, Osram's management will need to consider what lies ahead for the 200 or so staff that have been working on the microLED development programme. Kamper is keen to retain these "bright minds". They may well shift to projects involving the development of new headlamps or sensors.

Future prospects

For many, the big question now is who might take over leading the commercialisation of the microLED. Virey and his colleagues say that the epicentre of the microLED industry has now shifted to Taiwan, which has a strong domestic ecosystem, thanks to AUO, PlayNitride and Ennostar.

However, for these and other players, there is a limited window for success. Displays based on OLEDs are improving on many fronts, including cost, efficiency, brightness and lifetime, and as this rival becomes increasingly entrenched, this reduce the chances of success for the microLED.

Targeting regional expertise with a Catapult

By opening offices within the heart of existing regional clusters, the UK Compound Semiconductor Applications Catapult is providing catalysts that enhance local expertise

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WHILE IT'S EASY to judge a company by looking at its balance sheet, that's not an option for not-for-profits. For such entities, success has to be assessed by other means, such as its impact and the benefits it delivers on those its works with.

Judged against these metrics, the UK's Compound Semiconductor Applications (CSA) Catapult is thriving. Founded in 2018 within the compound semiconductor cluster in South Wales, over the last year this not-for-profit has started to strengthen its support of activities in other parts of the UK by adding local offices.

As part of this effort, last year this Catapult opened a Future Telecoms Hub in Bristol and CSA Scotland, and started work on establishing an office in North-East England to support companies in that region operating in telecoms, satellites communications and defence sectors.

Emphasizing the rational for the expansion of the Catapult, its CEO Martin McHugh remarks: "Whilst we're located in Wales – that's because there was an early stage cluster there – our remit is still the UK. We need to be seen to be a UK player. What the Catapult is trying to achieve is allowing regional clusters to have their own identity."

Even those that support this view may have raised an eyebrow at the setting up of the Future Telecoms Hub, given it's just a 20 minute drive from the South Wales office. But McHugh rebuffs this: "It's important that we're in the region, amongst the cluster, and they're feeling the beat of it and the mood of it."

Bristol is home to a number of household names within the telecom industry. This city, the biggest in the south-west, has offices for Qualcomm, Broadcomm, Nokia and Toshiba, and will soon accommodate a British Telecom research centre. Diversifying this mix are a handful of start-ups in related fields, including Zero Point Motion, a developer of chip-scale optical inertial sensors, and Axelera AI, an artificial intelligence chip manufacturer that creates AI hardware and software platforms for edge computing. Both are supported by Bristol University's Quantum Technology Information Centre.

➤ As well as spaces for assessing hardware that features compound semiconductor devices, The Future Telecoms Hub is equipped with a large meeting room.

The university also has strong academic programmes in the telecoms sector. Dimitra Simeonidou leads the Bristol Digital Futures Institute, as well as the Smart Internet Lab.

"You also have the semiconductor side," adds Nick Singh, CTO of the CSA Catapult. "Gallium nitride is one of the potential workhorses for next-generation telecoms, and that is reflected by some of the work that Professor Martin Kuball has been doing."

The Future Telecoms Hub is backed by £6.5 million from Innovate UK. The UK's innovation agency provided £2.5 million in March 2023 and a further £4 million in November.

Much of this funding will be used to improve the UK's capability in wireless infrastructure, including WiFi, 5G and 6G. Projects will involve the development of capabilities associated with data transmission, using frequencies approaching the terahertz domain, as well as AI and small cells.

Singh says that within such efforts, the Future Telecoms Hub will help to drive the development of advanced telecom hardware.

"It's also a unique space to address what we call CMICS," adds Singh, explaining that this acronym is short for convergence, miniaturisation, intelligence, connectivity and sustainability. Offering some detail on each of these five focus areas in turn, Singh argues that while convergence is key to making practical breakthroughs, progress can be held back by companies failing to share their progress and their plans. The Telecom Hub can address this obstacle to success by providing a space for co-creation, co-design, co-simulation and co-development.

Singh says that miniaturisation hinges on integration, which is supported by advanced packaging, an area of expertise for CSA. When it comes to intelligence, Singh claims: “Everything is getting clever and smarter. There will be programmable photonics.”

There is ever greater connectivity within society, which has increasing concerns regarding climate change, according to Singh: “Data doesn’t come cheap, and data is hungry for energy.”

For the last couple of years, the CSA has been involved in a project called ORanGaN, focused on establishing the capability to fully develop and manufacture commercial RF GaN devices within the UK.

Within this effort, IQE has provided 150 mm GaN-on-SiC epiwafers from its St Mellon’s facility that are processed at Inex Microtechnology, which has developed a 0.15 µm technology during the project. Contributions from the Catapult have included modelling, characterisation and benchmarking.

While a successful project such as this is important and valuable, one should not over-state its impact, argues McHugh. In his view, establishing supply chains requires multiple programmes, each of which need to connect SMEs, OEMs and universities.

McHugh sees one of the legacies of ORanGaN as providing a platform for another phase of supply chain development, pointing out that the progress-to-date cannot be described in terms of wafer-starts-per-month.

Due to such a wide variety of opportunities within the field of telecoms, McHugh warns against the Hub from spreading its efforts too thinly. Instead, the Bristol office must focus on just a few areas, where it will strive to make a big impact. As well as GaN-on-SiC technology for wireless, the Hub will help to pioneer efforts associated with integrated quantum photonics.

It is possible that the Hub will also support the cluster of companies within the region developing technologies related to space.

While the work of the Bristol office of the CSA Catapult has much promise, it would be folly to expect too much too soon. Both McHugh and Singh stress that it takes time to build up regional clusters and get the many players that are there to work together, before it is possible to finally enjoy the fruits of their labour. But by setting up offices within the heart of these regions, there’s every chance that progress will be made in a manner that is efficient and beneficial to the UK.

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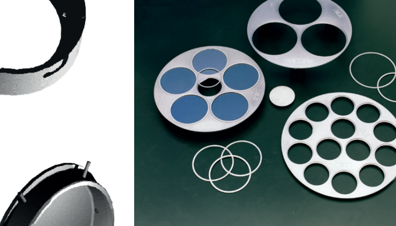

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Polychromatic pixels

MicroLEDs with a tuneable wavelength provide an unparalleled foundation for superior displays

BY MICHELLE CHEN FROM Q-PIXEL INC.

FROM COMMUNICATIONS to entertainment, displays play a critical role in the human-computer interface, dominating the way we interact with data and information. Accordingly, it is important to optimise the design and engineering of all forms of display. The best technology allows outstanding displays to be a major plus point for the marketing of new generations of computers, phones, tablets, TVs, and smart wearables. While consumers have different tastes, they are all united in a desire for brighter, longer lasting, more energy-efficient, higher resolution displays – delivered at a lower cost. But what exactly makes the ideal display? And what technologies will get us there?

The ideal display

Displays that draw the eye and engage the user are bright, colourful, and crisp. However, when engineering and implementing a display, there's a need to think beyond just these metrics. As well as the aesthetic appeal, good displays have a number of consumer-centric features, including a long lifetime, great energy efficiency and a low cost. It is the combination of all these factors that determines the overall performance and value proposition of the device or appliance that houses the given display.

While the criteria for an excellent display appear to be straightforward, no single display technology is commercially available today that encompasses all the desired characteristics. The mainstays of current display technology, liquid crystals and organic LEDs, dominate market share due to their low cost. However, both are held back by fundamental physics constraints, which are reflected in their disadvantages: short device lifetimes, issues with image burn-in, limited display resolution, and high power consumption. The latter is a major weakness, given that typically more than half a smartphone's power consumption comes from just its screen. In a wireless world, where battery life is paramount, is there an optimal technology for a bright yet energy-efficient screen?

From a physics perspective, microLEDs based on compound semiconductor materials have long been considered the holy grail of the display industry. They are highly sought after for display technology due to a combination of attributes: self-emissivity, high energy efficiency, durability, extensive lifetime, fast response time, and the potential to provide a high pixel density and a superior display resolution. However, today's microLED technology faces labour-intensive, cost-prohibitive manufacturing challenges that impede widespread commercialisation.

One notable bottleneck to realising microLED displays is the complex assembly methods required

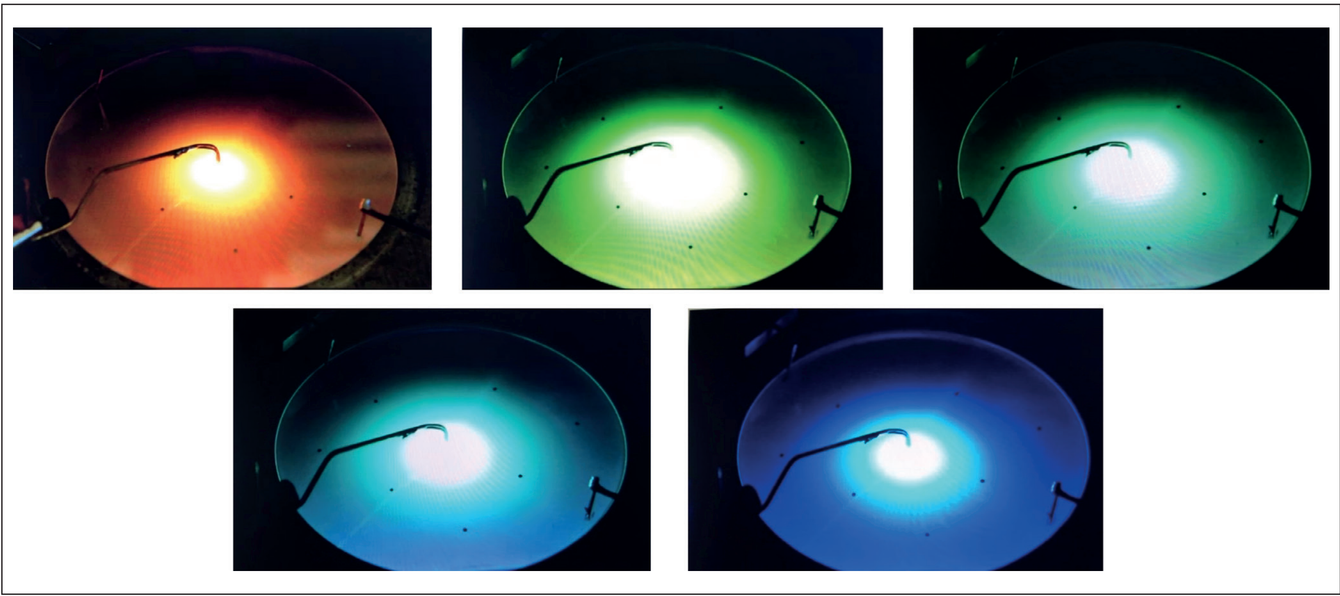


Figure 1. Wafer level demonstration of a polychromatic LED epi-wafer tuned across the entire visible spectrum.

to make pixels capable of covering the entire visible light range. The traditional approach for accomplishing this task is to consolidate individually grown red, green, and blue (RGB) sub-pixels into one pixel. As industry moves to smaller pixel sizes to produce higher-resolution displays, RGB sub-pixel assembly is increasingly difficult and expensive. Another challenge is that the circuits that access the three individual RGB sub-pixels occupy finite space, further constraining pixel density and display resolution.

Beyond century-old technology

The assembly of red, green, and blue sub-pixels for full-colour displays is deeply rooted in an obsolete aspect of LED technology: the monochromatic light approach. The first LED was fabricated almost a century ago. Since then, research in visible-light LEDs has emphasised materials capable of producing single-colour light of the highest quality and efficiency. While this has been indispensable for some applications, such as illumination lighting, the focus on monochromatic LEDs has inadvertently hindered the path to widespread adoption of microLED display manufacturing.

Due to the LED industry's fixation on producing wafers that yield monochromatic light, there is a barrier towards full-colour displays that begins at the material level. Typically, efforts at manufacturing mini-and microLED displays begin with the production of separate epiwafers for the emitters of red, green, and blue wavelengths. To produce full-colour pixels, all three types of epiwafer are diced into chips, before miniature red, blue, and green emitters, or sub-pixels, are grouped to form one pixel on a driving backplane.

The positioning of the red, green and blue chips to form a full-colour pixel – a process known as mass transfer – demands precision accuracy and high yield. Unfortunately, current mass transfer technology is by far the most expensive and least reliable step of microLED display assembly, due to its low throughput, and the need for extensive testing and repair, especially as pixels become smaller. The result is that mass transfer of individual red, green, and blue sub-pixels is a major showstopper to the commercial viability of microLED displays. With 4K televisions having over 8 million pixels (or 24 million RGB sub-pixels), it is easy to see why microLED display products are yet to be an affordable or widespread offering within the mainstream consumer market.

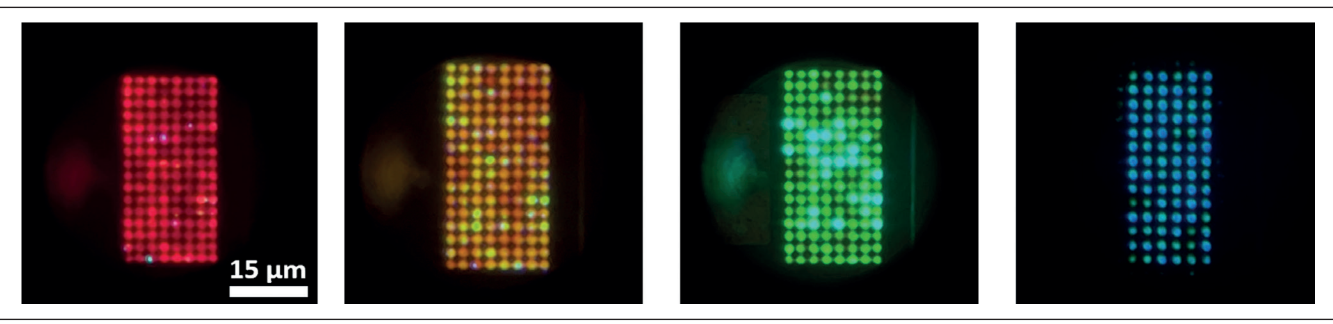
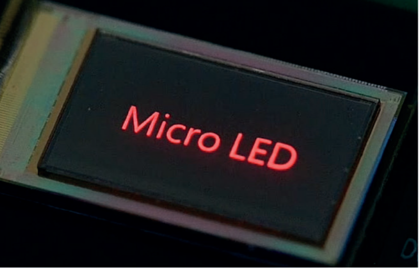
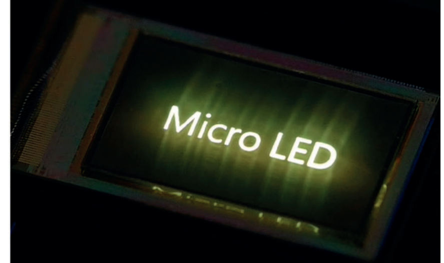
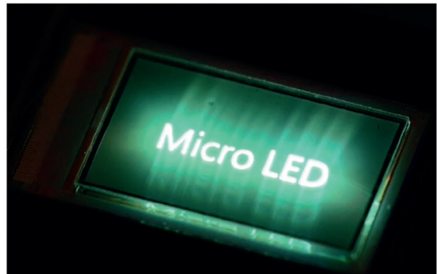


Figure 2. 10,000 pixels-per-inch passive microLED display with world's smallest (1 μm diameter) full-colour pixels.







➤ Figure 3. World's highest resolution (6,800 pixels-per-inch) active-matrix microLED display.

A polychromatic paradigm shift

At Q-Pixel, a Los Angeles based start-up focusing on LED innovations, we are side stepping the monochromatic barrier while rapidly advancing microLED technology towards commercialisation. The secret to our success lies in an entirely different approach to both LED design and the traditional methods of microLED pixel assembly. Rather than relying on monochromatic red, green, and blue LEDs grown on separate wafers, we pursue the monolithic growth of tuneable-wavelength LEDs to realise the full visible spectrum.

Lying at the very core of our tuneable polychromatic microLEDs is the material: uniform, full-colour tunability LEDs, grown across a single compound semiconductor wafer and tuned using one current driving channel, without any use of sub-pixels, quantum dots, colour filters, polarisers, or mechanical stacking. When combined with innovative fabrication processes, our wafers yield single pixels capable of emitting light across the full spectrum of visible colour.

The approach that we take to realising full-colour tunability is one that has been explored using different techniques over the years. Our method involves producing a GaN-based active region designed for red, green, and blue emission, where colour is tuned through different applied voltages. Compared to different groups' approaches, our main advantage lies in the production of monolithic LEDs using fully industry-compatible processes, which deliver full colour tunability using a single current driving channel, over a small voltage range compatible with conventional display drivers.

> Lying at the very core of our tuneable polychromatic microLEDs is the material: uniform, full-colour tunability LEDs, grown across a single compound semiconductor wafer, without any use of sub-pixels, quantum dots, colour filters, polarisers, or mechanical stacking

Our game-changing technologies, involving proprietary growth, process, and assembly methods, promises to overcome the major manufacturing obstacles currently faced by the entire display industry in implementing microLED-based displays. By replacing red, green and blue sub-pixels with a single colour-tuneable LED, we eliminate the bottleneck of sorting, binning, and picking-and-placing separate LED sub-pixels, and we replace mass transfer with simplified assembly processes. Reducing these costly, time-consuming steps significantly streamlines full-colour display assembly and lowers manufacturing overhead. In addition, the use of a single polychromatic LED in a pixel – rather than three sub-pixels, plus their corresponding circuitry – promises new opportunities for realising the ultra-high pixel densities needed for superior-resolution displays.

Revolutionising resolution

Ultra-high resolution is an urgent requirement for near-eye display applications, such as those used in virtual reality and augmented reality devices, as well as other head-mounted displays. The higher the display resolution, the less pronounced the undesirable 'screen door effect', a visual artefact that arises from visible gaps between large pixels or sub-pixels. Until recently, ultra-high resolution microLED displays, equating to more than 2,000 pixels per inch, had only been demonstrated in single colours, due to the constraints of assembling small red, green, and blue sub-pixels at ever increasing densities. Our tunable polychromatic LED technology has successfully surpassed this plateau, realising previously unattainable pixel densities in full-colour displays.

Last May we unveiled our full-colour microLED display with a record-breaking pixel density of 5,000 pixels per inch, far surpassing the previous world record of 2,000 pixels per inch. Six months later, we reported further progress, raising the bar to 10,000 pixels per inch for a full-colour microLED display. This more recent breakthrough broke two world records simultaneously: the highest resolution for a full-colour display; and the world's smallest full-colour pixel to date, realised with an emitter with a 1 μm diameter.

At the beginning of this year we hit another important milestone, producing the world's highest-resolution active-matrix colour display with our tuneable polychromatic technology. This astounding 6,800 pixel-per-inch display (around 1.1 cm by 0.55 cm, and around 3K by 1.5K pixels) is a landmark achievement, representing a first step towards widespread adoption of microLEDs by the display industry.

Bringing microLED displays to market ultimately comes down to a question of cost – in order to make microLEDs truly competitive in the display market, the cost of manufacturing needs to fall by over ten-fold from present rates – a target that can only be accomplished with a multi-faceted approach.

We have addressed this by developing scalable, cost-effective manufacturing technologies for microLED displays. Our emphasis is on assembly processes that minimise the number of defective pixels and maximise assembly speed for high-yield, high-throughput, large-area microLED displays. To remain competitive in a diverse market, we have devised assembly methods that are applicable to a wide range of display sizes and their respective applications, such as: televisions, tablets, personal computers, smartphones, automobiles, and wearable devices.

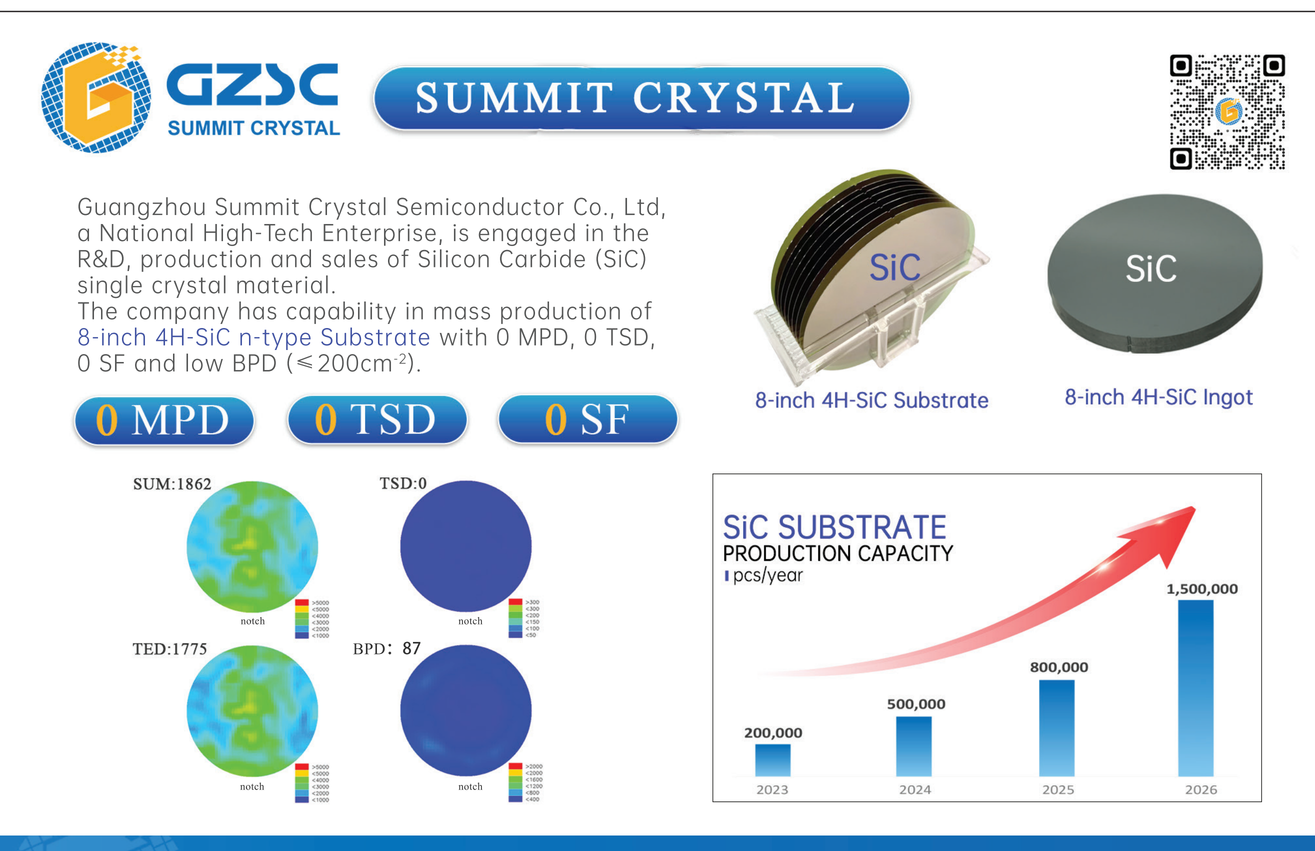
MicroLED moment

Up until now, microLED technology has struggled to find a footing in the display and consumer electronics market. It has been impeded by the cost and inefficiency of the manufacturing process, a limitation so severe that it has made microLED technology impractical to compete with existing display technologies.

Meanwhile, existing display technology has stagnated, despite being a multi-billion-dollar market. Lack of new progress in displays is evidenced by major industry players and start-ups scrambling towards new technological solutions. The entire display industry is now on the cusp of a major paradigm shift, with microLED displays tipped to play a major role in eventually succeeding technologies based on organic LEDs and LCDs. It is not so much a question of if, but when the industry will adopt microLED technology. However, while the direction of travel is certain, there is still the ever-present question of which technological approach will be adopted in the process.

Our technological achievements provide early evidence that it is possible to produce cost-competitive, colourful, ultra-high resolution microLED displays. By moving beyond the traditional red, green, blue sub-pixel assembly and into the realm of the polychromatic pixel, we have effectively eliminated the most expensive step of microLED display manufacturing, without compromising quality. By delivering the world's highest-resolution active display in colour, as well as demonstrating commercially viable microLED displays, we have proven that tuneable polychromatic LED pixel technology surpasses all current display technologies – even highly mature OLED technology – in making ultra-high-resolution displays.

Now the moment for microLED displays has arrived, and its future looks bright.



UV LEDs go micro

Shrinking UV LEDs to a micron or so delivers multiple benefits, including higher efficiencies and opportunities in new applications

BY JENS RASS FROM FERDINAND-BRAUN-INSTITUT FBH, BERLIN

MANY APPLICATIONS can be served by the UV LED, including disinfection, sensing, and material processing. For this class of device, sources emitting within the far-UVC at wavelengths below 240 nm are attracting considerable attention, as they have the potential to deactivate pathogens without damaging human skin. However, the uptake of the UV LED is being held back by its efficiency – it is far lower than its siblings that emit visible light.

For those visible emitters, over the last few years much effort has been directed at scaling dimensions, with the diameter of the LED reduced to below 100 μm, and sometimes shrunk to less than 10 μm. Motivating this miniaturisation is the creation of light-emitting pixels for display technologies, such as augmented- and virtual-reality headsets.

Our research team at the Ferdinand-Braun-Institut FBH, Berlin, has brought these two worlds together by developing UV microLED arrays. This format offers two substantial advantages over conventional UV LEDs with large emitter areas: a higher efficiency, thanks to enhanced light extraction; and the opportunity to create individually addressable emitter arrays, which can generate temporarily and spatially modulated UV radiation patterns. A number of applications could benefit from these arrays, including material processing, mask-free photolithography, sensing, non-line-of-sight communication, and UV-fluorescence microscopy.

One issue that plagues LEDs emitting in the far-UVC is a fairly low emission efficiency. Typical values for external quantum efficiency (EQE) and wall-plug-efficiency are below 1 percent, due to a number of factors that include strong non-radiative recombination of charge carriers, a low injection efficiency, and a low light-extraction efficiency. For the latter metric, values are 10-20 percent for LEDs emitting in the UVB and UVC, and fall to about 5 percent for those that emit in the far-UVC.

The main reason for the poor light extraction efficiency is the high degree of total internal reflection at interfaces. The trapped light is subsequently absorbed in various layers of the LED chip (see Figure 1).

For UVB and UVC LEDs, the light that's generated in the AlGaN-based layer structure is emitted through the transparent substrate. In most cases this is sapphire, which has a refractive index in the UVC of 1.8 - 1.9. As the AlGaN stack has a refractive index of approximately 2.7 and the surrounding air a value of 1, only radiation within a small angular range can leave the chip. Consequently, most of the photons that hit the AlGaN-sapphire and sapphire-air interfaces do so at angles beyond the critical angle for total internal reflection, causing them to be trapped inside the chip. Since many of the materials typically used to make the LED are inevitably absorbing – light can be absorbed at the metal contacts, the GaN *p*-side contact layer, and sometimes the insulators – there is a low probability for photon emission after several reflections.

Unfortunately, the likelihood that light is trapped within an LED increases at very short UV wavelengths. Reaching this spectral domain requires an increase in the aluminium mole fraction in the active region of the AlGaN quantum wells. This leads to a re-ordering of the valence subbands, resulting in a switching of the optical polarisation of the generated photons from dominantly transverse-electric, with the electric field vector lying in the chip surface and the photon emission perpendicular to it, to transverse magnetic. Since light polarised in the transverse magnetic direction is emitted parallel to the chip surface, the majority of photons traverse

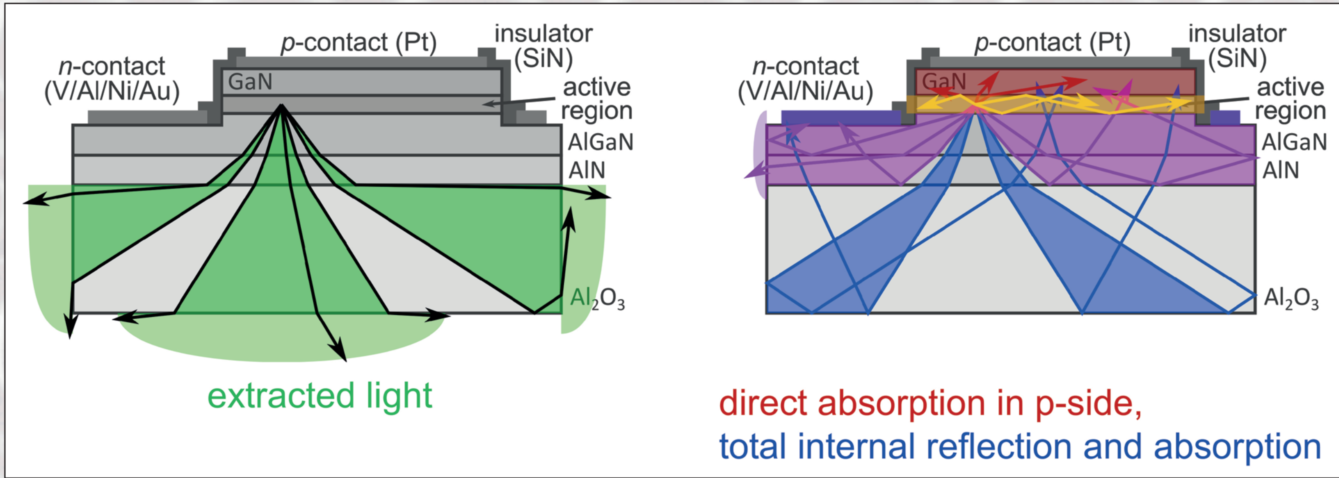


Figure 1. UV LEDs have a low light extraction efficiency (LEE), due to the trapping of photons in the chip and subsequent absorption within the device structure, including layers of GaN, metals, and insulators. Light trapping is more severe in far-UVC LEDs, since more transverse-magnetic polarised light is travelling in the quantum well plane.

with a direction outside the light escape cone, and thus have a very high probability of undergoing total internal reflection and subsequent absorption.

Increasing the light-extraction efficiency is a common goal for all developers of LEDs. For devices emitting in the visible and UV, improvements come from introducing surface patterning, reflective contacts, and encapsulation techniques. However, it's far from easy to enjoy success with these approaches with the UVC LED. Progress is held back by strong absorption and instability of materials under irradiation with high photon energies.

Getting the right angle

Our approach is to pattern the surface of the AlGaN-based LEDs into arrays of individual micro pixels with a slanted mesa side wall. With this architecture, photons emitted parallel to the chip surface are redirected towards the chip backside where they can be extracted (see Figure 2). To optimise performance, the micro pixels need to have a small diameter and smooth, reflective sidewalls with an angle near 45 °.

To fabricate these emitters, we began by growing LED layer structures made of AlGaN on 2-inch sapphire substrates by MOCVD. The active region in these epiwafers is designed to deliver single peak emission at 233 nm.

We patterned the wafer surface by photolithography and employed chlorine-based plasma etching to create circular mesas with diameters between 1.5 μm and 100 μm and a sidewall angle of 45 ° to 50 ° (see Figure 3). While this step proved to be very challenging, it is crucial for guaranteeing a high efficiency through the re-direction of transverse-magnetic polarised photons. Our work involved having to fine-tune the parameters for the photolithography process on the transparent and heavily bowed wafers, and developing suitable plasma etch conditions, including the gas mixture, plasma power, and pressure.

Following etching, we deposited and annealed *p*- and *n*-metal contacts. In order to realise a high reflectivity at the tilted mesa surface, we then deposited a SiO_2 layer. This electrically insulating

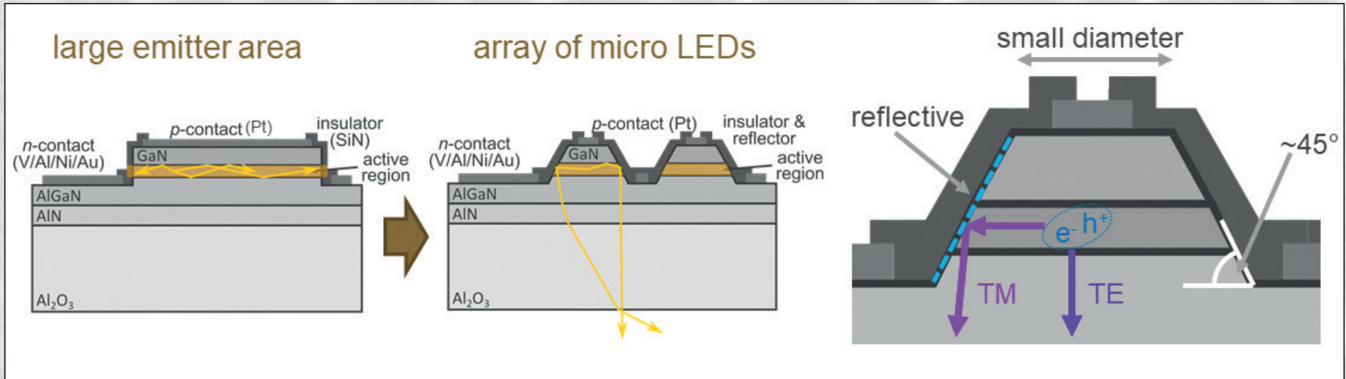
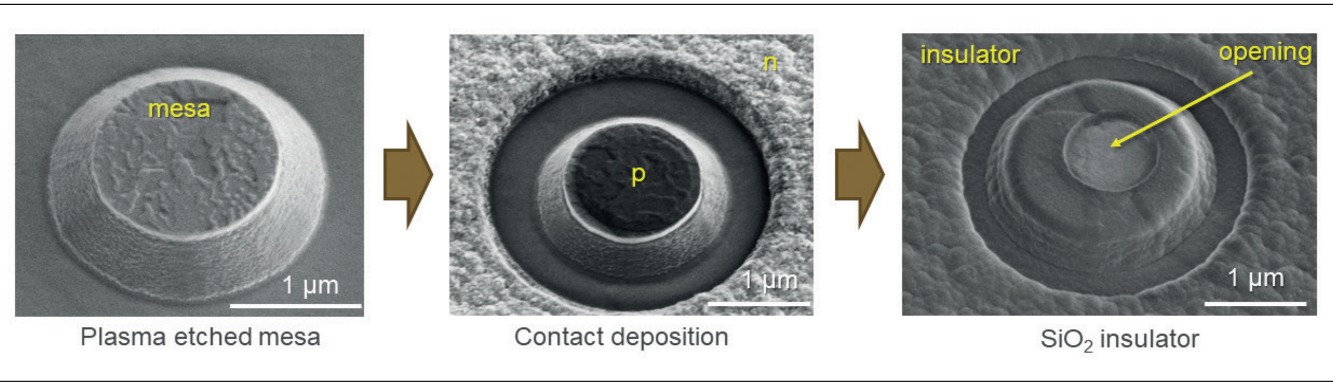


Figure 2. Light extraction from the UV microLED is enhanced by internal reflection at the mesa side wall and redirection towards the chip back surface. This requires small mesas with slanted and highly reflective side walls and small diameters.



➤ Figure 3. The mesa definition is a crucial step in the production process, in particular the adjustment of the sidewall angle, as well as the alignment of the following layers.

oxide is fully transparent in the entire UV range, and offers a high refractive index contrast to AlGaN, enabling it to act as a reflector. We capped the SiO_2 with aluminium, also acting as a reflector, before adding thick metal pads for an electrical contact.

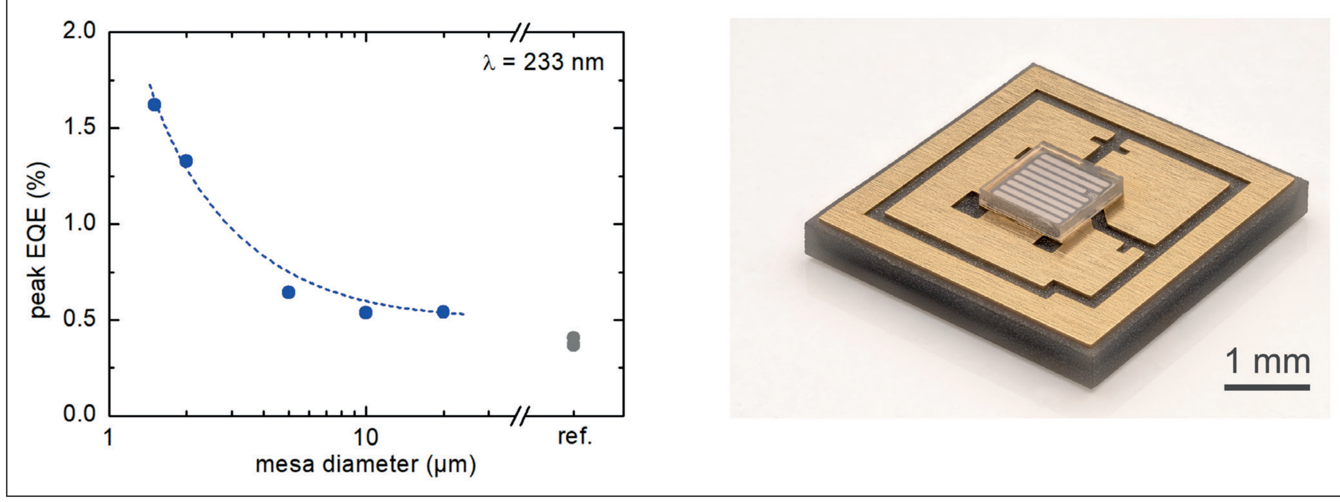
The final processing steps involved dicing LED chips from the processed wafer and mounting them on ceramic submounts in a flip-chip geometry. For comparison, we also produced LEDs that incorporate a different insulator, by replacing SiO_2 with SiN_x. Since SiN_x has a smaller refractive index contrast to AlGaN and absorbs in the UVC range, LEDs with this insulator should not provide a significant enhancement in light extraction.

Miniature marvels

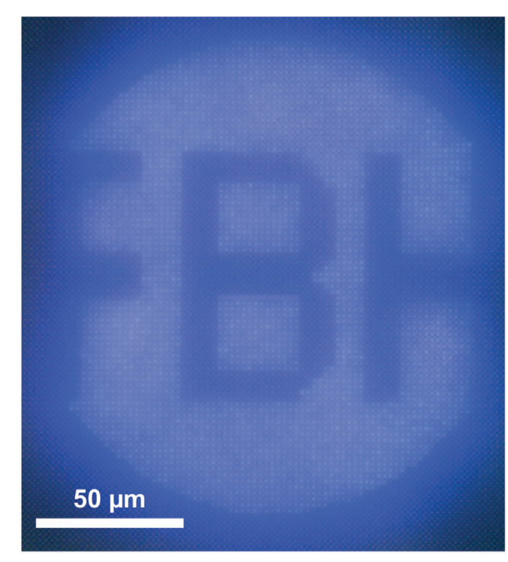
Measurements of the electroluminescence characteristics of our devices, using an integrating sphere, reveal that the micro pixel architecture produces a very strong increase in output power, and therefore efficiency. Moving from a conventional design to a pixel diameter of just 1.5 µm produces a fourfold hike in peak EQE (see Figure 4). Scaling to such small dimensions is needed to benefit from miniaturisation – there is no benefit for only reducing the LED diameter to 5 µm. Note that this is not the case with visible microLEDs, where benefits are already realised for devices with diameters of 10 µm or even more. What's more, for our devices the peak EQE occurs at current densities between 70 A cm^{-2} and 200 A cm^{-2}, while for LEDs in the literature, the record peak EQE tends to occur at very low current densities that are unsuitable for applications.

Another noteworthy attribute of our UVC emitters is that their improvement in light extraction efficiency does not saturate at small mesa diameters. In sharp contrast, for microLEDs in the visible range – and especially those emitting in the green and red – there is a strong reduction in the EQE at small diameters. This fall in efficiency is attributed to non-radiative recombination of charge carriers at defects at the plasma-etched mesa side wall. As we do not see such an effect, we can conclude that any possible increase in losses must have been more than compensated for by the improvement in the light extraction efficiency.

This is further confirmed by the LEDs that employed the SiN_x insulator: The emission power was not significantly enhanced for small diameter structures since the refractive index contrast to AlGaN was too low to achieve total reflection, but neither did the efficiency drop for the small diameters, as would be seen if nonradiative carrier recombination at the mesa sidewall was an issue.



➤ Figure 4. Left: The peak EQE is drastically increased by reducing the diameter of the micro pixels due to increased light extraction. Right: UVC LED chip with standard large area chip layout mounted in flip-chip geometry on a ceramic submount.



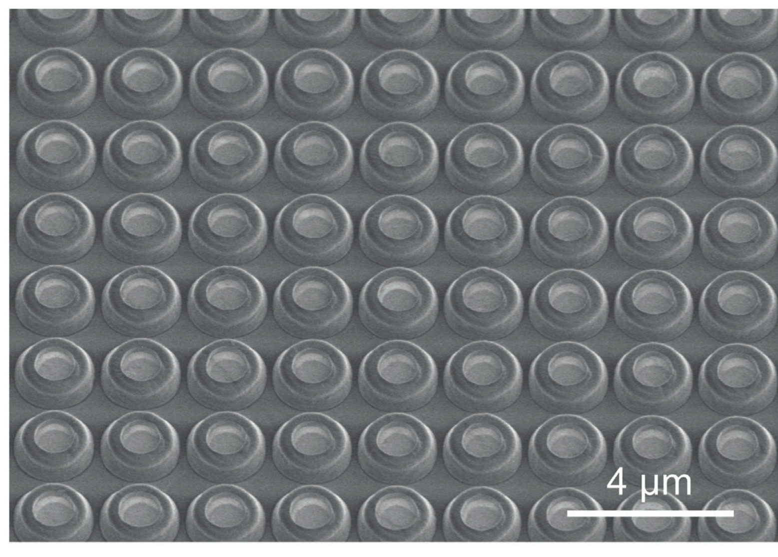


Figure 5. A UV micro-LED array with pitch of 2 µm and a pixel diameter of 1.5 µm emitting at a wavelength of 300 nm. Light microscopy image (left) and scanning electron microscope image during the production process (right).

Our 233 nm microLEDs produce a record peak EQE of 1.6 percent and a wall-plug efficiency of 0.88 percent. Output powers are 1.7 mW and 3.5 mW at 20 mA and 50 mA, respectively. While these values are lower than those for LEDs emitting in the visible, UVB and near-UVC, they are the highest numbers currently reported. That makes our progress a significant step towards bringing far-UVC LEDs closer to deployment in practical applications, such as nitrogen oxide gas sensing and skin-safe eradication of pathogens.

We are now working on further improvement to the efficiency and output power of our far-UVC LEDs. Our investigations include improving the AlN-sapphire templates, the AlGaN-LED heterostructure, and the microLED chip process. By packing pixels more densely, adding additional layers for efficient current spreading, and using strain engineered templates to enhance transverse-electric polarised optical emission, we have already realised our first promising results, with EQE increasing to peak values of up to 2.9 percent.

These improvements in the efficiency of far-UVC LEDs, resulting from an increased light extraction efficiency, are important for the realisation of high-power emitters. However, it's important to not overlook a number of other interesting opportunities connected to this technology.

One of these is to combine our UV LED, patterned into electrically separated pixels, with a matrix- or CMOS driver chip. It's a marriage that creates UV light engines and UV micro displays that can serve in many new applications. For example, the spatially and temporarily modulated light pattern generated by such a device could illuminate the photoresist on wafers, thereby creating a mask-free lithography system. Such a source of UV emission could also be deployed for rapid prototyping and 3D printing/patterning. Opportunities also exist in the life sciences, with arrays of UV microLED pixels providing the light source for DNA fluorescence spectroscopy and other sensing applications.

It's also worth noting that our technology is not restricted to the far-UVC. It can also be applied to nitride-based LEDs emitting in the UVC, UVB, and all the way to UVA, opening up a large number of applications.

In order to demonstrate the feasibility of such an approach, we have developed a chip emitting at 300 nm that emits our FBH-logo (see Figure 5). While the device cannot yet change its pattern, it illustrates the potential of UV microLED technology.

FURTHER READING / REFERENCE

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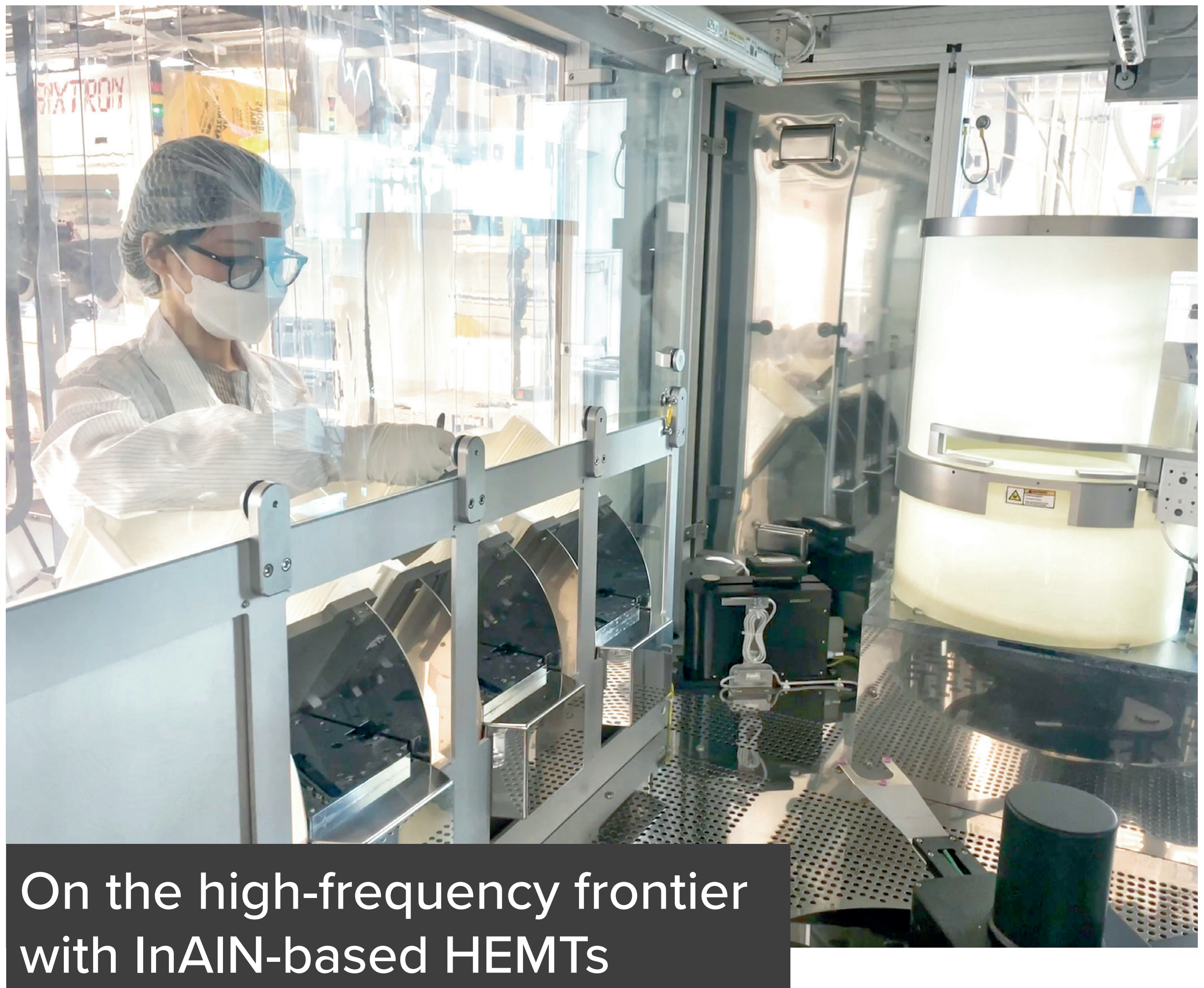
- M. Kneissl and J. Rass, *III-Nitride Ultraviolet Emitters - Technology and Applications* (Springer, 2015)



On the high-frequency frontier with InAlN-based HEMTs

Combining InAlN/GaN HEMTs with GaNOI technology ensures the monolithic integration of high-frequency GaN devices with CMOS technology

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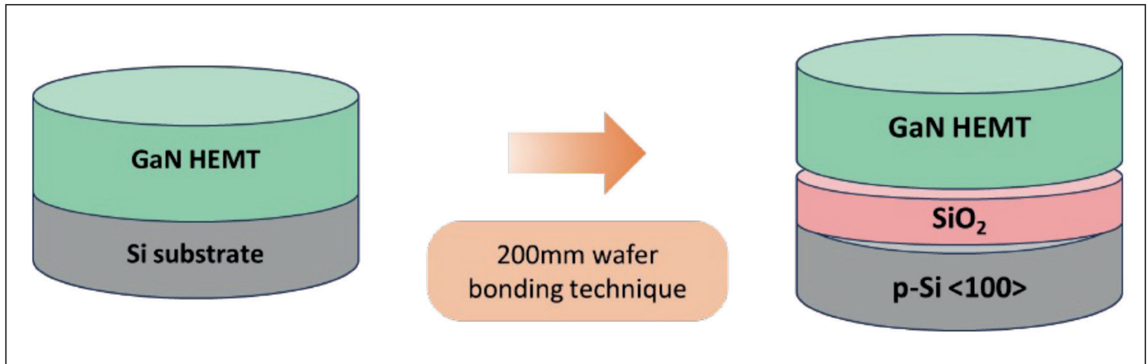
WITHIN THE FAMILY of compound semiconductors, GaN is held in particularly high regard. This material is renowned for its many strengths, including its wide bandgap, its high critical electric field, and the high density present in its polarisation-induced two-dimensional electron gas (2DEG).

One device that draws on these merits is the GaN-based HEMT, which outperforms its silicon-based counterpart. Thanks to the robust power-handling ability of GaN, this class of HEMT is well suited to serving in millimetre-wave applications in wireless communication technologies.

While GaN outperforms silicon, it cannot match its maturity. This makes the integration of GaN and silicon CMOS technology attractive, creating a marriage that offers a cost-effective scalable solution by leveraging existing silicon infrastructure while capitalising on GaN's superior efficiency and thermal stability. However, it is easier said than done. Integration poses notable challenges, particularly in preserving the breakdown voltage and ensuring optimal RF performance.



➤ Figure 1. GaN-on-insulator (GaNOI)-on-silicon wafers are produced by adding an insulating layer between the GaN epilayers and the silicon substrate.

Taking on these challenges, our collaborative team from the Singapore-MIT Alliance for Research and Technology, Nanyang Technological University, and Massachusetts Institute of Technology, is pioneering the use of wafer-bonding technology to enable a GaN-on-insulator (GaNOI) architecture on a silicon substrate.

It's an effort that's been underway for several years, with our initial success presented at the VLSI Symposium 2019. At that meeting we reported validation of the enhanced breakdown voltage of the GaNOI structure and its compatibility with silicon CMOS technology.

Our innovative method, described in prior reports, enables the processing of large silicon wafers in standard silicon foundries. Using this approach, we have enhanced device reliability by eliminating the initial transition layer, characterised by a multitude of dislocations and subpar thermal conductivity.

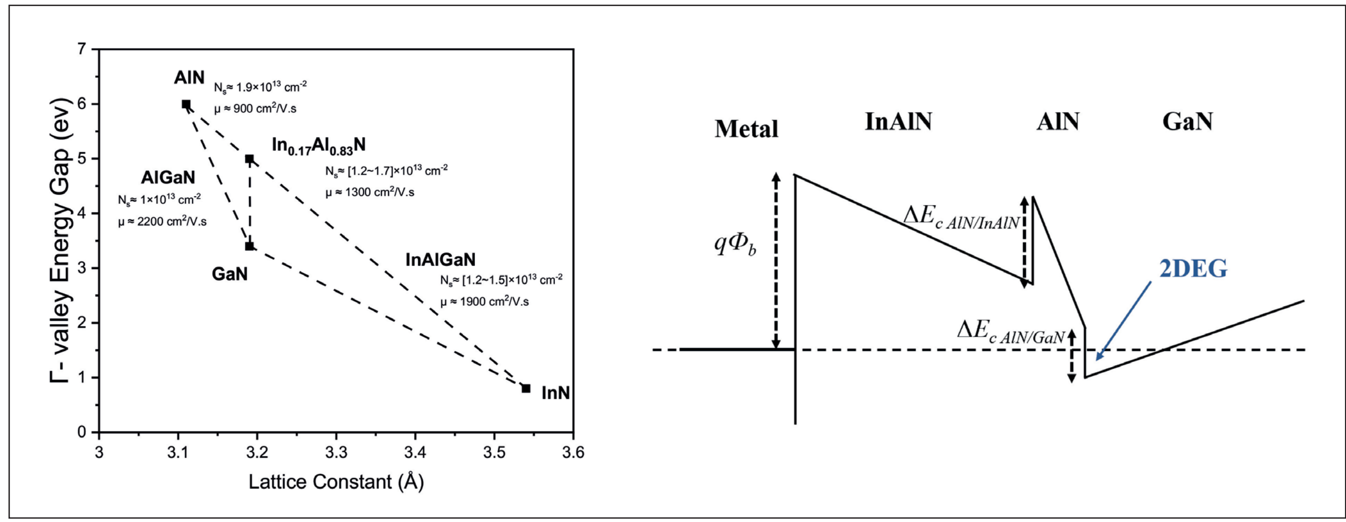
Another refinement has been substituting the original silicon (111) substrate, which is prone to fragility after high-temperature GaN growth, with a more robust silicon (100) substrate. This switch significantly diminishes the likelihood of wafer breakage during production, leading to increased yield.

More recently, we have started to explore the potential of GaNOI technology in high-frequency applications. By constructing GaN HEMTs on an insulating substrate, GaNOI technology is expected to trim parasitic capacitance and ultimately improve frequency performance.

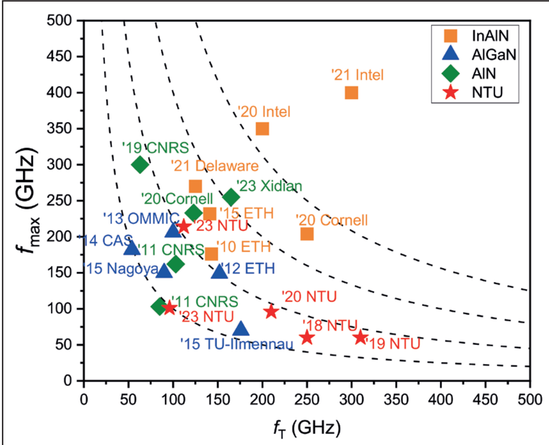
Typically, GaN-based HEMTs employ either AlGaN, InAlN or AlN as the barrier material. The selection from these three has a great influence on overall device performance and reliability, especially under harsh conditions, such as high temperatures. The 2DEG that forms at the interface between the barrier layer and GaN lies at the heart of the HEMT, acting as a quantum well filled with high-mobility electrons. Levers for optimising the properties of the 2DEG, such as its density and mobility, include varying the thickness and the material composition of the barrier layer.

Traditionally, AlGaN has been the go-to material for the barrier layer. However, it is not without weakness. A significant downside is the stress induced by the piezoelectric effect, leading to possible lattice defects.

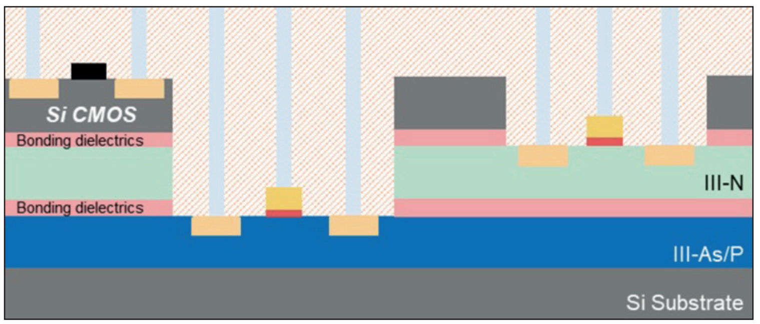
This is where InAlN comes in to play, offering a compelling alternative that's lattice-matched to GaN, thus minimising strain effects (see Figure 2).



➤ Figure 2. Cross-sectional InAlN/GaN heterostructure schematic showing the location of the 2DEG and energy band diagram of a GaN heterostructure.



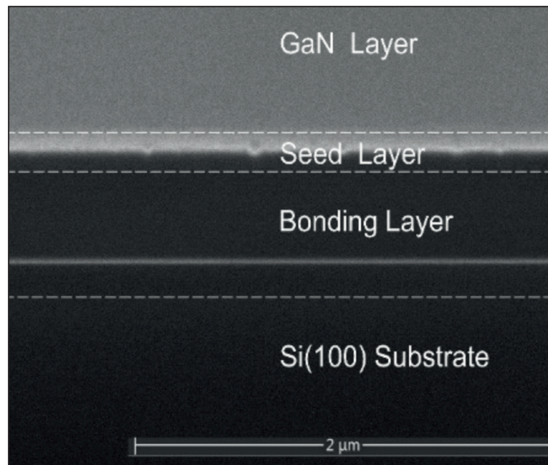
➤ Figure 3. Reported f_T/f_{max} values for various GaN-on-silicon HEMT technologies.



➤ Figure 4. There is much promise associated with the integration of silicon-CMOS, RF devices and high-power devices, comprising HEMTs on both III-N and III-As/P layers, on a single wafer forming a hybrid substrate.

Switching to InAlN is the move behind record current-gain cut-off frequencies, which indicate the potential of InAlN/GaN HEMTs in high-frequency applications.

To date, the highest cut-off frequency for AlGaN/GaN HEMTs on silicon substrates is 152 GHz, realised with devices with a recessed gate that have a 75 nm gate length. With this particular device, an AlGaN barrier layer thickness of 25 nm results in 2DEG density of 1×10^{13} cm^{-2}. By replacing this with an InAlN barrier, the thickness of this layer can be trimmed to around 8 nm, while realising an even higher 2DEG density, in the range 1.2 - 1.7×10^{13} cm^{-2}. This improvement is due to



➤ Figure 5. Cross-sectional transmission electron microscopy image of a GaNOI wafer.

a higher spontaneous polarisation for InAlN/GaN, compared with AlGaN/GaN. The thinning of the barrier layer while maintaining a high sheet carrier density is desirable, enabling increased gate modulation control by reducing the gate-to-channel distance, and ensuring an increase in transconductance. With an InAlN/GaN HEMT on silicon, we have recorded values for the cut-off (f_T) and maximum oscillation (f_{max}) frequency of 300 GHz and 400 GHz, for a 30 nm gate length (see Figure 3).

Moreover, in high-temperature applications, InAlN/GaN heterostructures offer unparalleled robustness. At high temperatures, strain effects in the system can become more prevalent, threatening reliability. InAlN is lattice-matched, and thought to provide higher reliability in ultra-high temperature environments, due to the absence of piezoelectric strain.

The improved performance makes it even more attractive to integrate silicon CMOS with high-frequency devices such as GaN HEMTs, and high-power components like power amplifiers (PAs) on GaN layers. Wafer-level integration is a key enabler for developing compact, versatile, and efficient integrated circuits for serving in a wide array of applications, from consumer electronics to advanced communication systems.

Wafer bonding and layer transfer

Wafer bonding has emerged as a promising method for integrating III-Vs onto silicon substrates, a key process for the development of advanced semiconductor devices. Among the various techniques for taking on this task, we prefer fusion bonding, particularly plasma-activated bonding. Its merits include its compatibility with low-temperature processing and the opportunity to use atmospheric pressure conditions. In addition, plasma-activated bonding is able to accommodate materials with mismatches in coefficients of thermal expansion, and is seamlessly compatible with CMOS process technology, making it a versatile choice for diverse semiconductor applications.

The fabrication of our devices began by preparing several sets of wafers, each including: a silicon handle wafer, a 200 mm InAlN/GaN-on-silicon (111) wafer, and a new silicon (100) wafer substrate. A critical initial step was the plasma-enhanced chemical vapour deposition (PECVD) of SiO_2 on the front sides of both the silicon handle wafer and the InAlN/GaN HEMT wafer, followed by densification of this oxide. After this, we thoroughly cleaned the surfaces and treated them with plasma activation to promote adhesion, prior to bonding.

Following the first wafer bonding, we turned to grinding and wet etching in an HF/nitric acid/acetic acid solution to completely remove the original silicon substrate. Deposition of 200 nm oxide layers by PECVD on both the GaN HEMT wafer and the

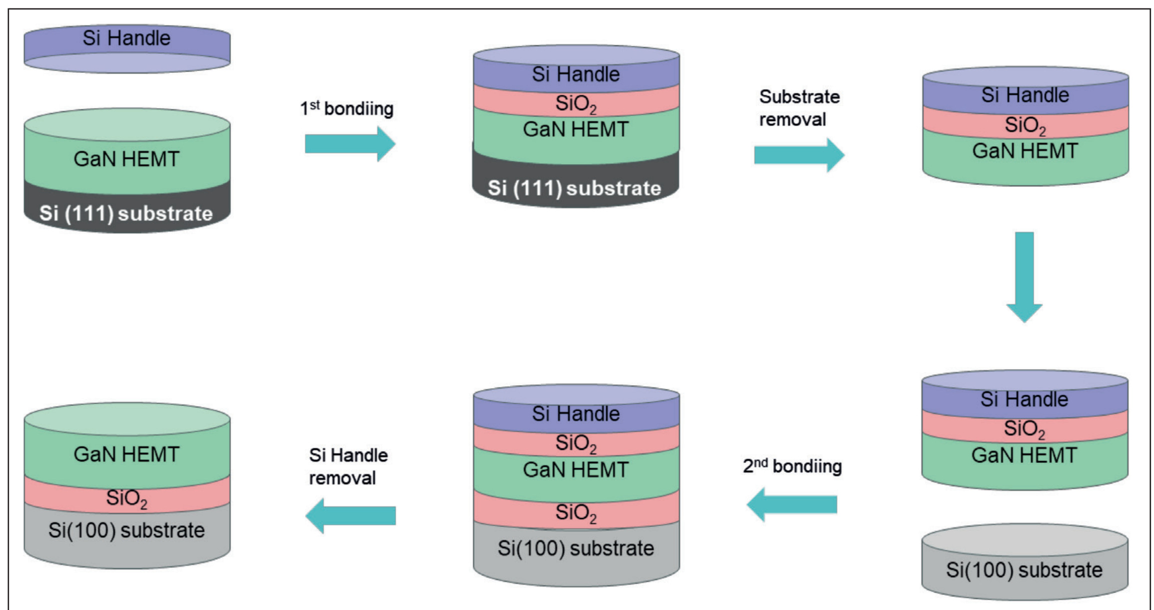


Figure 6. GaNOI-on-silicon wafer fabrication flow.

silicon (100) substrate followed, prior to densification at 600 °C for several hours in nitrogen gas. The latter step eliminated residual gas molecules and any by-products incorporated into the layer during the oxide deposition. After this densification, we applied chemical mechanical polishing to smooth the PECVD oxide for the second bonding process. The bond strength increased by annealing the bonded wafer pair for 3 hours at 300 °C in an atmospheric N_2 ambient (see Figure 5).

Scrutinising material quality

We have rigorously evaluated the material quality of our heterogeneous structure with a variety of techniques. According to transmission electron microscopy, our 200 mm GaNOI-on-silicon wafer shows no visible bubbles at the bonding interface, an indication of the high quality of the bonding process (see Figure 6).

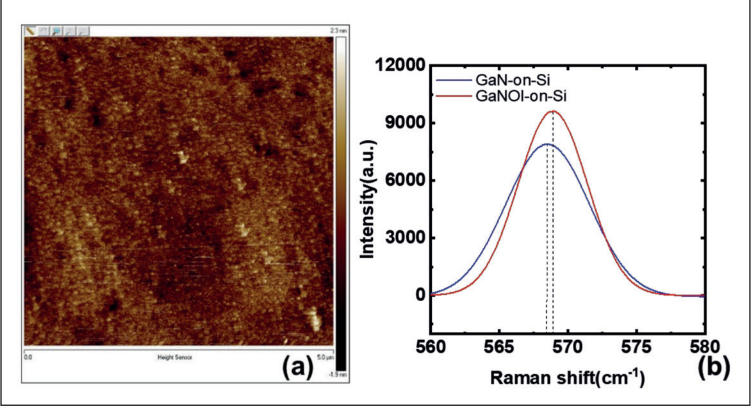


Figure 7. (a) Atomic force microscopy of InAlN/GaN on a GaNOI-on-silicon substrate and (b) Raman spectra of both GaN-on-silicon and GaNOI-on-silicon samples, high resolution E2 modes.

Prior to device fabrication, we undertook a comprehensive characterization of our epitaxial wafer, using techniques that included atomic force microscopy, X-ray diffraction, micro-Raman spectroscopy and Hall measurements. Atomic force microscopy provided values for the root-mean-square (RMS) roughness of the wafer surface, while X-ray diffraction and Raman measurements were pivotal in determining the crystallographic structure and quality, providing insights into the strain, defects, and layer compositions of the GaN epitaxial layers. This pair of non-destructive techniques allowed us to evaluate crystalline quality, revealing information about dislocation densities and lattice mismatches, potential obstacles to realising an impressive device performance.

According to atomic force microscopy of a 5 μm by 5 μm area, the RMS roughness of our InAlN/GaN HEMT epilayer on a GaNOI substrate is just 0.7 nm. Such a low value indicates that no significant misfit dislocations are exposed on the top surface.

Sample	Lattice parameter a_0=b0 (Å)	a Spread (Å)	Lattice parameter c_0 (Å)	c Spread (Å)	a Strain (%)
Before bonding	3.19099	4.25×10^{-4}	5.18402	4.81×10^{-5}	5.60×10^{-2}
After bonding	3.191079	1.29×10^{-4}	5.18399	3.17×10^{-5}	5.30×10^{-2}

Table 1. Comparison of key X-ray diffraction parameters.

Sample	Sheet Carrier Conc. [$\times 10^{13}$ cm^{-2}]	Mobility [cm^2 V^{-1} s^{-1}]	Sheet Resistance [Ω □$^{-1}$]
Before bonding	1.97	930	301
After bonding	1.89	1380	284

Table 2. Hall parameters for wafers pre- and post- bonding.

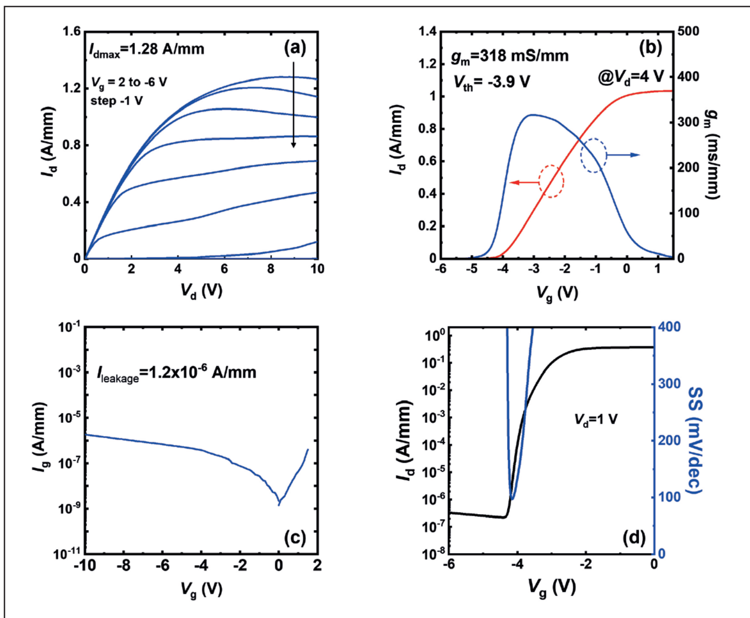


Figure 8. (a) Output and (b) transfer characteristics of a 120-nm gate GaNOI device. (c) Gate leakage characteristics and (d) semi-log-scale transfer curves at V_{ds} = 1 V.

During the layer transfer processes, the in-plane lattice strain reduced by 5 percent (see Table 1). This could be attributed to the release of stress. Our view is that strain relaxation probably results from diminished elastic strain/deformation, due to the removal of a highly-mismatched silicon (111) substrate.

Micro-Raman spectroscopy supports this hypothesis, unveiling a significant reduction in compressive stress in the material system, highlighted by a shift in the GaN peak (see Figure 7(b)). Additional evidence for the decline in compressive stress comes from X-ray diffraction measurements. Another insight provided by Raman spectroscopy is the extent of stress within the GaN channel. According to simple calculations based on the shift in the Raman wavenumber, there is a reduction in stress of 0.1 GPa after layer transfer, associated with a reduction in strain in the GaN epilayer.

The reduction in stress resulted in increases in the 2DEG mobility and the concentration of carriers within the InAlN/GaN heterostructure. Note that similar observations have been reported by Cosmin Romanitan and colleagues at the National Institute for Research and Development in Microtechnologies, IMT Bucharest.

We have also undertaken room-temperature Hall measurements to determine the carrier concentration, mobility, and sheet resistance for both our GaN-on-silicon and GaNOI-on-silicon wafers. These results, presented in Table 2, reveal that after substrate replacement, the mobility of the $In_{0.17}Al_{0.83}N$/GaN heterostructure increases from 930 cm^2 V^{-1} s^{-1} to 1380 cm^2 V^{-1} s^{-1} and the 2DEG density slightly decreases from 1.97 × 10^{13} cm^{-2} to 1.89 × 10^{13} cm^{-2}, leading to an improvement in sheet resistance from 301 to 284 Ω/square. These gains translate into an enhanced performance for our GaNOI-on-silicon devices.

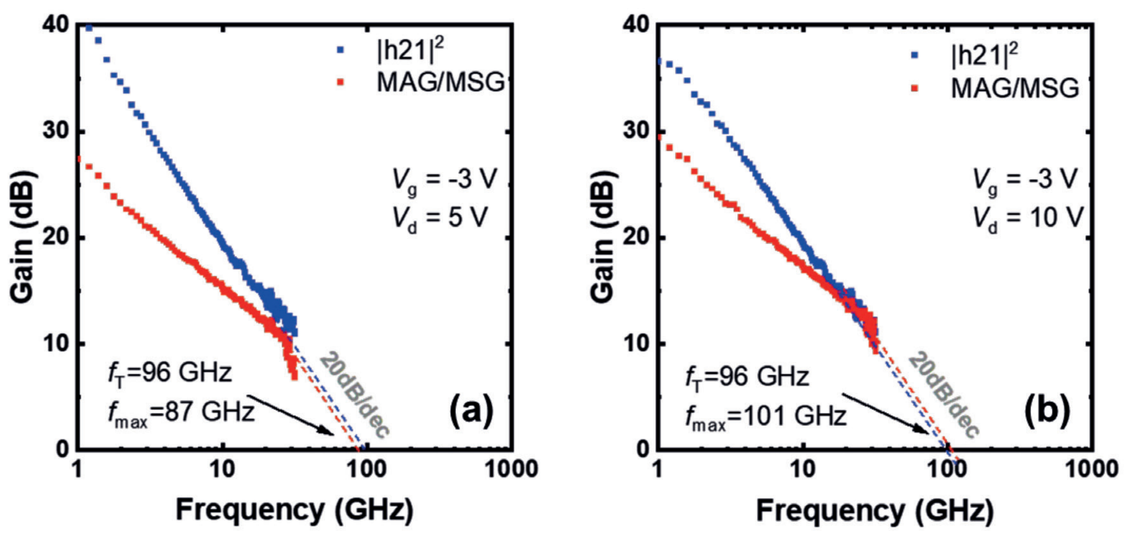


Figure 9. RF small-signal characteristics of a GaNOI device at (a) V_{ds} = 5 V and V_{gs} = -3 V and (b) V_{ds} = 10 V and V_{gs} = -3 V, with the pad parasitics de-embedded.

Device evaluation

Using a standard fabrication process flow, we have fabricated GaN HEMTs from a small piece of a 200 mm InAlN/GaNOI-on-silicon wafer, using inductively coupled plasma-reactive ion etching with a Cl_2-based plasma to realise device mesa isolation. We formed ohmic contacts using a Ti/Al/Ni/Au metal stack annealed for 30 s at 775 °C. According to linear transmission line model analysis, ohmic contact resistance is 0.21 Ω-mm. To complete transistor fabrication, we formed Ni/Au T-shape Schottky gates, with a gate foot length of 120 nm, a head length of 500 nm and a stem height of 170 nm.

Here we report current-voltage (I-V) and RF measurements of devices with a 2 × 20 μm gate width, and gate-source and gate-drain distances of 1.5 μm. Saturation current density peaks at 1.28 A mm^{-1}, for a gate-source voltage of 2 V, and on-resistance is 2.3 Ω·mm (see Figure 8(a)). Transfer characteristics included a peak transconductance of 320 mS/mm and a threshold voltage of - 3.9 V (see Figure 8(b)).

Additional measurements reveal a Schottky gate barrier of 0.81 eV, and an off-state gate leakage current of about 117 μA mm^{-1} at -10 V (see Figure 8(c)). This indicates no apparent electron tunnelling through the barrier layer, despite the highly localised electron density near the gate.

We also plotted semi-log-scale transfer curves for a drain-source voltage of 1 V (see Figure 8(d)). Under reverse bias, we determined an on-off ratio for the current of the GaNOI device of 2.6 x 10^6 and a subthreshold slope of 89 mV dec^{-1}. These values confirmed that our devices offer good gate control.

To evaluate the high-speed capability of our HEMTs, we measured their current gain ($|h21|^2$) and maximum available gain/maximum stable gain, using measurements up to 40 GHz (see Figure 9 for details). We obtained peak values for f_T and f_{max} of 96/87 GHz and 96/101 GHz by extrapolating from the current gain ($|h21|^2$) and the maximum available gain/maximum stable gain with a -20 dB/dec slope.

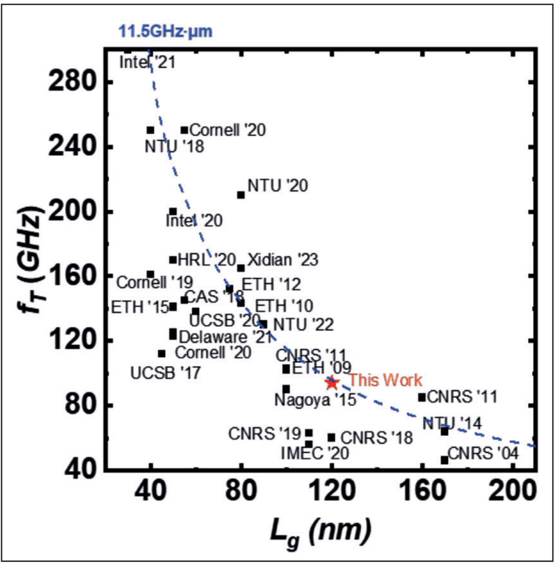


Figure 10. Comparison of the f_T of GaNOI and GaN HEMTs, both produced on silicon substrates.

Benchmarking our devices with GaN-on-silicon HEMTs using a figure of merit that's the product of f_T and the gate length determined that our device is comparable to the state-of-the-art. This underscores the great potential for improving high-frequency performance with GaNOI technology, with GaNOI-on-silicon offering much promise for future millimetre-wave applications. We have no doubt that this technology will be able to meet the demands of future advanced wireless communication systems, and open up new possibilities in high-frequency electronics.

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A SiCOI chip under test

Integrated photonic platforms:
The case for SiC

The potential of SiC integrated photonics is starting to be unleashed, thanks to the unique photonic properties of this material and the development of high-quality epitaxial growth

BY HAIYAN OU FROM THE TECHNICAL UNIVERSITY OF DENMARK

THE MOST mature and applied semiconductor ever, silicon, is the pillar for modern microelectronics. For the last 50 years or more it has been revolutionising human life, with progress in computation prowess spurred on by adherence to Moore Law, leveraging planar processing.

However, the shrinking of device dimensions cannot continue forever. Line widths are now approaching their physical limit, leading those at the forefront of this technology to search for a way forward to address the looming bottleneck. One promising option involves turning to integrated photonics.

Electrons versus photons

A crucial difference between integrated electronics and integrated photonics is the carrier. Evaluated in this regard, the latter has much appeal. The merits of the photon include: an absence of charge, preventing interference from electromagnetic fields; and an absence of mass, enabling devices to operate at far faster speeds than their electronic counterparts (see Table 1). However, there are challenges in the photonic domain, including the manipulation of this carrier.

In integrated electronics, silicon dominates. Meanwhile, in integrated photonics multiple material platforms co-exist, including silicon, Si_3N_4, GaAs, InP, GaP, AlN, $LiNbO_3$ and SiC. This high level of diversity reflects the fact that no single material provides the six basic building blocks for an integrated photonic chip: a light source, a waveguide, a modulator, detection, low-cost assembly and intelligence.

Silicon is playing a very active role in photonics, thanks to a well-developed material and its mature processing, refined over many decades of manufacture of integrated electronics. However, silicon has two significant drawbacks. The first is that it

	Photons	Electrons
Mass	0	9×10^{-31} kg
Charge	0	-1.6×10^{-19} Coulombs
Speed	3.0×10^8 m/s	0, or less than 3.0×10^8 m/s
Spin	1	Half
Antiparticle	None	positrons

Table 1. Comparison of photons and electrons

is an indirect bandgap semiconductor, so is inherently inefficient for light emission; and the second is that due to a bandgap of 1.12 eV, strong two-photon absorption occurs at telecommunication wavelengths, screening other nonlinearities, such as four-wave mixing, which provides wavelength conversion.

These two restraints create opportunities for other materials, such as III-Vs and wide bandgap semiconductors. For example, direct bandgap III-V semiconductors are ideal for integrated lasers solutions, while wide bandgap semiconductors have negligible two-photon-absorption within the telecommunication wavelength range.

SiC: Pros and cons

Within this family of compound semiconductors, SiC is emerging as a very promising candidate for integrated photonics. This wide bandgap material has many strengths, including being CMOS compatible, bio-compatible, abundant, non-toxic and thus sustainable; and it has unique photonic properties, such as both high second-order and third-order nonlinearities, a high refractive index, a wide bandgap, and a low intrinsic material loss. Additional strengths include having more than 250 polytypes with variable properties, a thermal conductivity that's more than three times that of silicon, and stable mechanical, physical and chemical characteristics. Furthermore, the processing of SiC is advanced – there is a mature growth technology for producing high crystal-quality SiC, engineers know how to dope this material, and mature material growth and device fabrication has already been established for SiC power electronics, laying the foundation for efforts to scale SiC in integrated photonics.

The wide adoption of SiC power devices, particular in electric vehicles, has laid a solid foundation for the deployment of this material system in SiC photonics. However, despite these advances in materials and fabrication, three substantial challenges have to be addressed: the formation of SiC-on-insulator (SiCOI) stacks, in order to confine

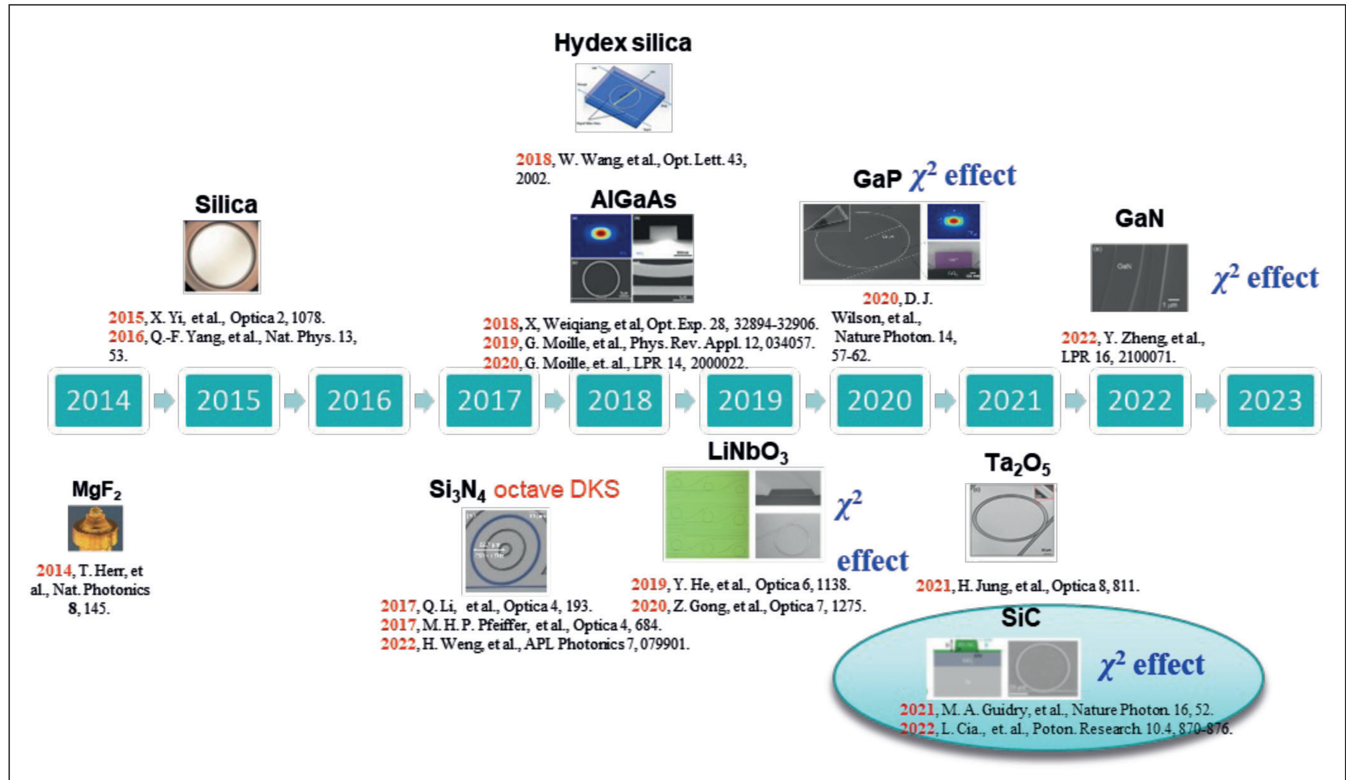

Figure 1. The microcomb development roadmap.

Table 2: Comparison of SiC with other material platforms in integrated photonics.

Material	n	2nd NL (pm/V)	3rd NL (m^2/W)	Bandgap (eV)	Loss (dB/cm)
Si	3.5	0.6	6.7×10^{-18}	1.12	0.3
SiO_2	1.4	0	3×10^{-20}	9	0.06
MgF_2	1.38	0	9×10^{-21}	10	
Si_3N_4	2	0.3	2.4×10^{-19}	5	0.07
SiON	1.8	0	7×10^{-20}		0.06
AlN	2.1	1	2.3×10^{-19}	6	0.6
Ta_2O_5	2.1	0.34	7.23×10^{-19}	3.8	0.3
$LiNbO_3$	2.2	27		4	0.027
AlGaAs	3.3	0	2.6×10^{-17}	1.4-2	1.4
GaP	3.1	82	1.2×10^{-17}	2.26	1.2
SiC	2.6	50	8.6×10^{-19}	2.4-3.3	0.08

the light in SiC; the development of nanofabrication technology, for low loss and dispersion control; and the introduction of an efficient coupling scheme for the coupling of light in and out of a chip.

In photonic circuits, the path of the photon is controlled by the waveguide, using total internal reflection to steer light through the structure. To ensure that photons are confined within a SiC layer, this material is embedded in low refractive index material, such as SiO_2. Commercially available SiC tends to be in the form of wafers, typically 500 μm-thick, while the SiC layer in a SiCOI stack is normally less than 1 μm.

The first big challenge to address is to transfer SiC from a wafer to a thin layer. Our team at the Technical University of Denmark initially took on this challenge with an ion-cut method, also known as smart cut, well established for the production of SOI wafers. Unfortunately, this approach led to a high optical loss of around 6 dB/cm, resulting from ion implantation.

This loss could not be reduced dramatically by thermal annealing, due to limitations associated with the lower melting temperature of the silicon substrate. One possible solution might be to turn to laser annealing, rather than furnace annealing, as this source can be focused to a small spot, allowing just the SiC layer to experience a high temperature for defect recovery, while maintaining the silicon substrate below its melting point.
Our current approach differs from this. We avoid ion implantation altogether, using a bonding and grinding method to form our SiCOI structures. However, the yield is still very low.

Another concern is waveguide loss, resulting from imperfections in fabrication. If there is any roughness at the surface of the SiC waveguide, this increases its loss. To minimise this we have optimised our SiC waveguide fabrication process, which consists of electron-beam lithography, dry etching and top-cladding SiO_2 deposition. This approach enables us to form SiC waveguides with a well-defined geometry and a smooth surface.

A typical cross-sectional geometry of our SiC waveguides is around 500 nm by 500 nm. While this is much bigger than the feature size of a FET, the transistor used to control electron transport in ICs, it is still much smaller than a spot size from a standard single mode fibre – that's around 10 μm. Due to this significant difference in size, we have devoted much effort to ensuring efficient light coupling between a standard single-mode fibre and a SiC waveguide, using mode conversion on the chip. We also aim to achieve extremely low loss within the waveguide, so that we don't need an on-chip amplifier, a device that doesn't exist yet.

To test our SiC optical chips, we use a high magnification microscope to aid the alignment of SiC waveguides and optical fibres (see opening image). This task is supported by mounting the optical chip and the fibre ends on three-dimensional adjustable stages.

Optical frequency combs

Back in 2005, the Nobel Prize in physics went to pioneers in the field of optics. Roy Glauber won half the award for his contribution to the quantum theory of optical coherence, and the other half was shared by John Hall and Theodor Hänsch, for their contribution to the development of laser-based precision spectroscopy, including the optical frequency comb (OFC) technique. An OFC produces a spectrum with discrete, distinct, and equally spaced frequency lines – it is like a ruler for measuring light frequencies.

The chip-scale frequency comb, also called a microcomb, represents the third generation of OFC. It follows the mode-locked laser OFC, the first generation of this technology, and the more recent fibre laser OFC, the second generation of this technology. Combining the advances of nanofabrication and nonlinear optics, the microcomb is attracting much interest. It's now a very hot research topic, due to strengths that include the compactness of the OFC, its efficiency, its ultra-wide band output, and its potential to serve in a wide range of applications. Microcombs could be used for spectroscopy, optical communication, metrology, optical atomic clocks, bio/chemical sensing, distance ranging and searching for exoplanets.

Progress with microcombs has propelled them to an advanced state called the octave and dissipative Kerr soliton, which realises self-reference and coherence. Thanks to the highly compact geometry, comb tooth spacings can now be in the range of tens of gigahertz to terahertz, further expanding the application range of traditional mode-locked laser combs.

Among the different material platforms that can be considered for photonic integration (see Table 2), SiC is one that is going to open a door to new optical devices, including microcombs, thanks to its unique optical properties. Its strengths include a wide bandgap, and high second-order and third order optical nonlinearity.

Due to its wide bandgap, frequency comb light sources based on SiC can cover an ultra-wide band from near ultraviolet to mid-infrared. Within this wide spectral domain disinfection, lighting, communication, biosensing and gas sensing all

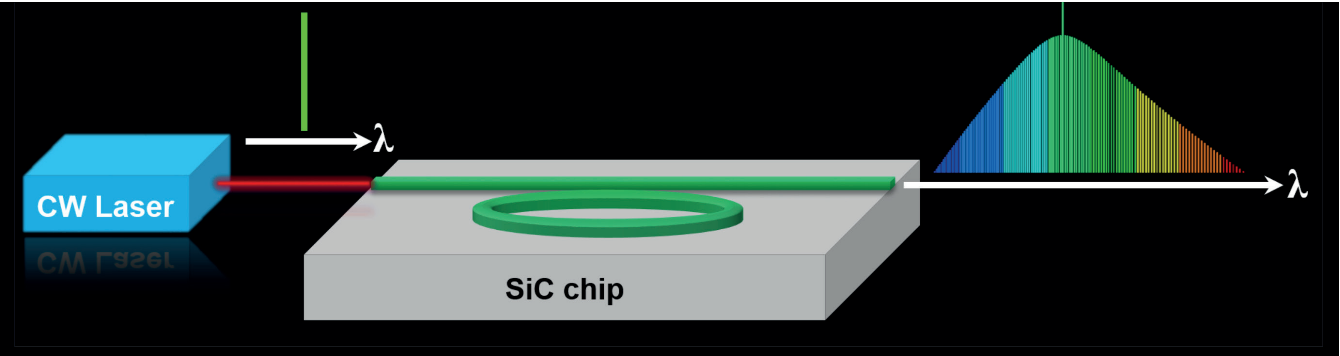

Figure 2. SiCOI OFC generated from a microring resonator.

have individual footprints, some of which are yet to be covered by standard lasers. The high second-order and third-order non-linearity of SiC are advantageous, because they make the SiC frequency comb energy efficient and broad.

There are also significant opportunities for the SiC OFC in the likes of quantum optics and quantum networks, quantum computing, sensing, and imaging. This technology is sure to make an impact, enabling more secure and scalable integrated quantum networks, and possibly new embedded biosensors that revolutionise medical diagnosis, thanks to the biocompatibility of SiC material.

Over the last 10 years much progress has been made in chip-scale OFCs, also known as microcombs (see Figure 1 for a brief development roadmap since 2014). Key breakthroughs include the demonstration of chip-scale OFCs using MgF_2 in 2014, SiO_2 in 2015, Si_3N_4 in 2017, both AlGaAs and Hydex silica in 2018, $LiNbO_3$ in 2019, GaP in 2020, both Ta_2O_5 and SiC in 2021, and GaN in 2022.

Aside from $LiNbO_3$, which generates an OFC through second-order nonlinearity (an electro-optic comb), the rest of the OFCs are realised through a third-order nonlinearity, and are known as a Kerr comb. Of these, Si_3N_4 is marked with an octave dissipative Kerr soliton, and provides a fully stable OFC. $LiNbO_3$, SiC, GaN and AlN are marked to have second-order nonlinearity. Unlike materials without second-order nonlinearity, these four have the capability to realise an octave bandwidth through wavelength conversion via frequency doubling. Despite the late arrival of SiC to OFCs, this material has caught up, demonstrating its capability and showcasing its tremendous potential in photonics, due to a nanofabrication-friendly nature and unique optical properties. Illustrating this point is a Kerr comb generated from a SiCOI microring resonator, shown in Figure 2.

Pioneering SiC OFCs

Our team is a trailblazer of SiC OFC technology, realising a number of important milestones over the last few years. In 2019 we reported the first integrated SiC microring resonator from 4H SiCOI made by the ion-cut method, as well as demonstrating four-wave mixing and deriving a non-linear refractive index for 4H SiCOI. A year later we demonstrated supercontinuum generation from 4H SiCOI waveguides made by the ion-cut method, and in 2021 we announced optical

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parametric oscillation from 4H SiCOI made by the ion-cut method. Further breakthroughs have followed in the last few years. In 2022 we demonstrated a 4H SiCOI beam splitter, polarisation beam splitter and Mach-Zehnder interferometer, and filed a patent for fabricating 4H SiCOI material stacks. And in 2023 we demonstrated: a 4H SiCOI polarisation and mode multiplexer; OFC from 4H SiCOI; and four-wave mixing from amorphous SiCOI, as well as deriving the non-linear refractive index for this particular material.

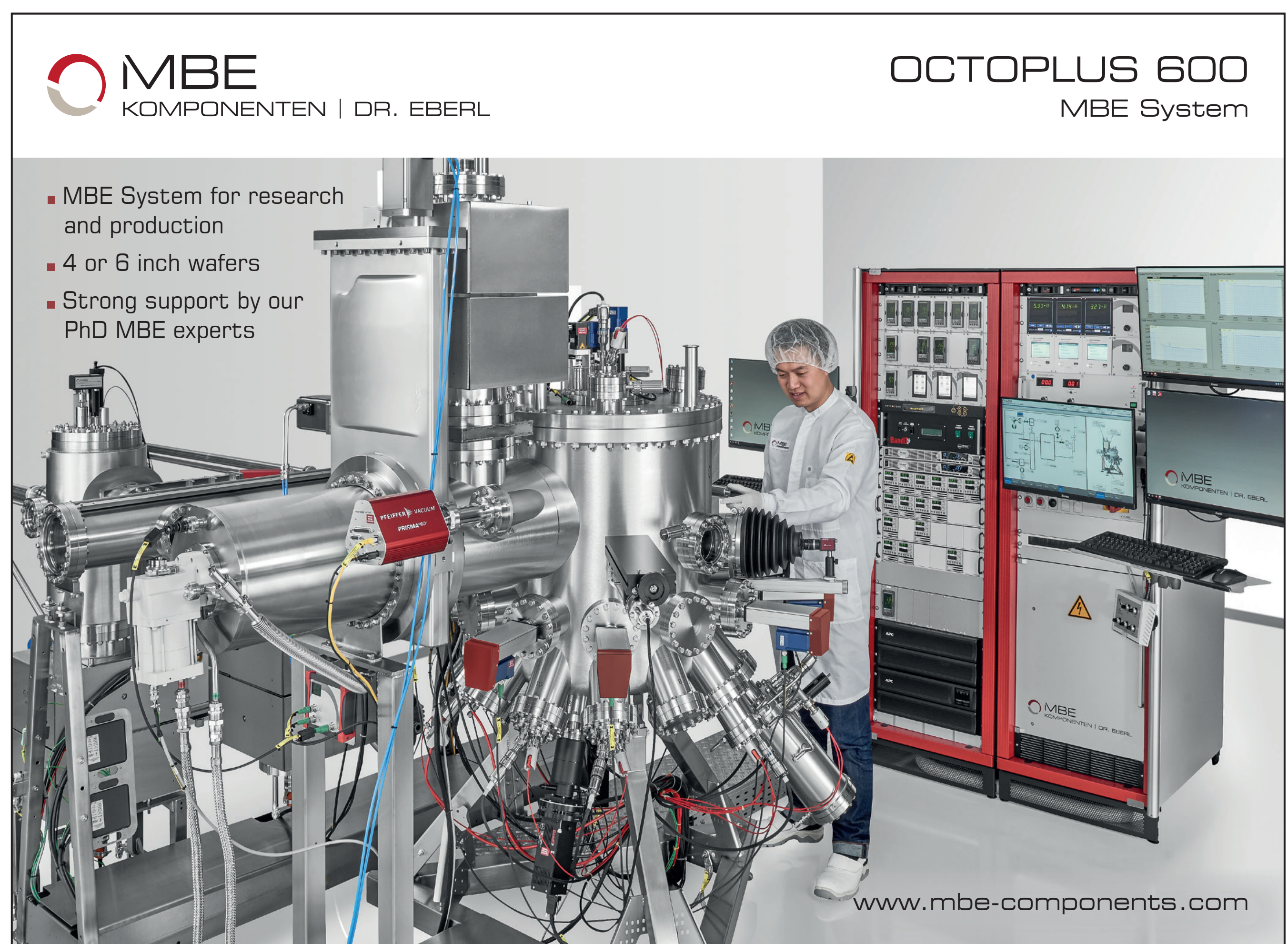
SiC is now attracting intensive interest for integrated photonics, spurred on by advances in crystal growth, thin-film transfer and nanofabrication. Key breakthroughs to date include the demonstration of second-order and third-order non-linearities in SiCOI. These non-linearities enable wavelength conversion, optical modulation/switching, optical frequency comb generation, and so on. Another important advance is the realisation of a family of high-performance passive components. Testing reveals that some of these components work in both the classic and quantum regime.

Leveraging the triumphs of SiC in integrated photonics, this material is making a promising entry into integrated quantum photonics. Here one of its attributes is the multi-species of colour centres, which could offer a solution in the quest for single-photon sources operating at room temperature.

Looking ahead, in the short term our plans include developing and optimising the six building blocks for integrated photonics with SiCOI. In a long term, SiC will be an active player as a material platform for quantum photonic integrated circuits, with the monolithic integration of single-photon sources in SiCOI with other building blocks. SiCOI has the potential to outperform diamond, in terms of both scalability and its wide selection of colour centres, with emission wavelengths spanning the visible to infrared. This material also appears to have the upper hand over III-V quantum dots, because SiCOI promises to produce single-photon sources working at room temperature, key to transferring quantum technology from the lab to practical applications.

We have the fortune to pioneer the SiC photonics field. We look forward to embracing upcoming opportunities and challenges, to driving further development of this technology, and to providing novel solutions for a more sustainable future.

Acknowledgement: EU H2020 FET Open project 'CMOS compatible and ultra-broadband on-chip SiC frequency comb' (SiComb, project No. 899679).



SiC MOSFETs

Scrutinising the gate atom by atom

Atom probe tomography unveils the composition and the distribution of key elements in the vicinity of the interface SiO_2 and SiC

BY LAKSHMI KANTA BERA, SHIV. KUMAR, NAVAB SINGH, UMESH CHAND, ABDUL HANNAN BIN IBRAHIM ABDULLAH YEO, VOO QIN GUI ROTH AND SURASIT. CHUNG FROM A*STAR AND PIERRE-YVES CORRE FROM CAMECA INSTRUMENTS

OVER THE LAST DECADE, much effort has been devoted to the development of the SiC MOSFET. This is paying off, with sales soaring, driven by the uptake of this device in electric vehicles.

The success of the SiC MOSFET comes from its key attributes. One great strength is its wide bandgap, enabling high-temperature operation and a trimming of energy loss during device operation. Additional assets include its high thermal conductivity, aiding efficient heat dissipation and helping maintain device performance and longevity; and a simple integration flow, following in the footsteps of silicon technology, that involves the growth of SiO_2, using thermal oxidation.

However, the SiC MOSFET has an Achilles heel. In stark contrast to the interface of silicon and its native oxide, SiO_2, that grown on SiC is riddled with a high interface-state density. The numerous imperfections significantly reduce carrier mobility in the MOS channel and threaten device reliability.

Due to these significant concerns, much effort has been devoted to understanding the origins of the high density of interface states. This has been attributed to carbon-related defects, including C-clustered, C-interstitial, and C-vacancies. Within the scientific community, it is widely agreed that these defects play a significant role in influencing the density of interface states at the SiC/SiO_2 interface.

Many studies, such as those investigating native point defects and carbon clusters in 4H-SiC, as well as the structure and energetics of carbon-related defects in SiC, have provided much insight into the impact of these carbon-related defects on material properties. However, despite many years of investigation by several research groups, the distribution of different elements and compounds in bulk SiO_2 and at the SiO_2/SiC interface is yet to be completely understood. To a large extent, this comes down to a lack of information at the atomic scale. There is a need to know the identity and the precise location of different species.

Two common techniques for materials characterisation that fall short in this regard are X-ray photoelectron spectroscopy and Auger electron spectroscopy. Both these forms of spectroscopy are hampered by a poor lateral resolution in the micrometre-range, as well as a relatively poor detection limit – it is around

0.1 atomic percent – that leads to a low detection sensitivity, and hampers complex quantification of chemical analysis.

Another widely used technique within the compound semiconductor community, secondary ion mass spectrometry, excels in detecting trace elements down to parts-per-billion levels. However, its sub-micrometre lateral resolution limits atomic-scale analysis. In addition, quantification of results is challenging, due to the dependency on ionization energy for secondary ion yield.

A versatile tool that provides detailed investigations at the sub-nanometre level is high-resolution transmission electron microscopy. Advances in one form of this, high-angle annular dark-field scanning transmission electron microscopy, have enabled, in special cases, three-dimensional characterisation at the atomic scale.

However, the ultimate characterisation technique for studying materials at the atomic level is atom probe tomography. This incredibly powerful technique, which our team from the Agency for Science, Technology and Research, Singapore, is using to scrutinise the interfaces of SiO_2 and SiC, can't be beaten when it comes to discovering the position of individual atoms in materials with nearly atomic resolution. One of its key merits is equal sensitivity for all elements.

Basic principles

Atom probe tomography operates on the principle of field evaporation, with surface atoms extracted from specimens with an electric field. This process involves directing a laser at the sample, alongside simultaneous high-voltage pulsing, conditions that cause surface atoms to evaporate with near 100 percent ionisation. The evaporated atoms are projected onto a position-sensitive detector for analysis.

To maximise the effectiveness of this technique, there is a need to prepare sharp needle-shaped specimens with a radius of 50-100 nm. Such samples ensure precise analysis through field evaporation of surface atoms. The chemical nature of the atoms is identified with time-of-flight mass spectrometry (see Figure 1 for an overview of this experimental setup).

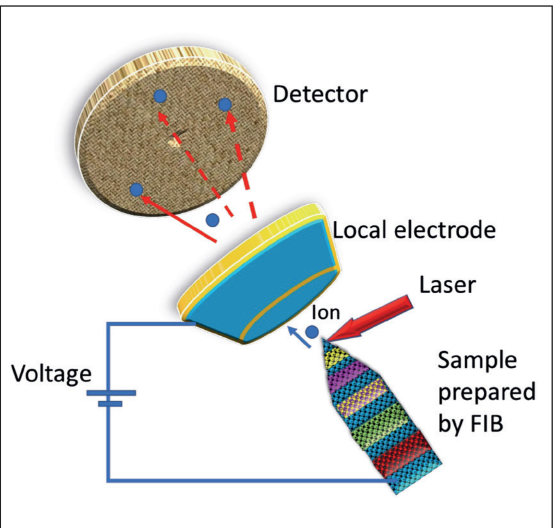


Figure 1. The experimental setup for atom probe tomography.

After loading samples into an atom probe tomography analysis chamber, specimens are cooled to around 50 K and maintained in an ultra-high vacuum, typically 10^{-11} Torr. Applying a DC voltage of typically between 2 kV and 10 kV results in a high electric field at the surface of the tip. The field at the tip's apex is proportional to the applied voltage, and inversely proportional to its radius of curvature.

For electrically conductive materials, atom probe tomography involves the application of voltage pulses to the tip to generate an electrical field that induces field ionization. For less conductive samples a different approach is needed, with laser pulses ensuring the thermal evaporation of ions. The application of laser pulsing is especially advantageous in higher resistivity materials, such as semiconductors, where high-voltage pulses alone may be insufficient for promoting field ionisation.

The detection of ions that are liberated from the sample is correlated to the high-voltage and laser pulses. Ions are converted into a mass-to-charge-state ratio, measured in a unit known as the Dalton. This conversion is crucial for chemical identification of each ion, which is identified by the relationship between its time-of-flight and its mass-to-charge-state ratio.

A mass spectrum is produced during atom probe tomography – this is a histogram of the resulting

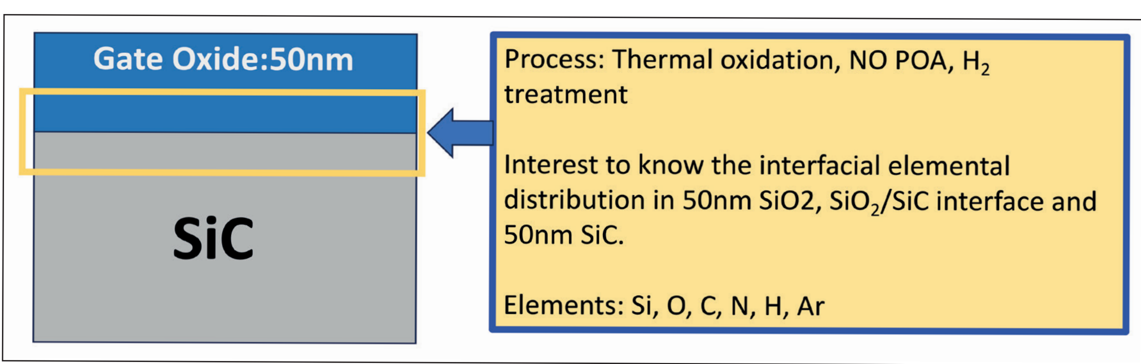


Figure 2. Schematic cross section of sample for interest of investigation of several elements and their distributions.

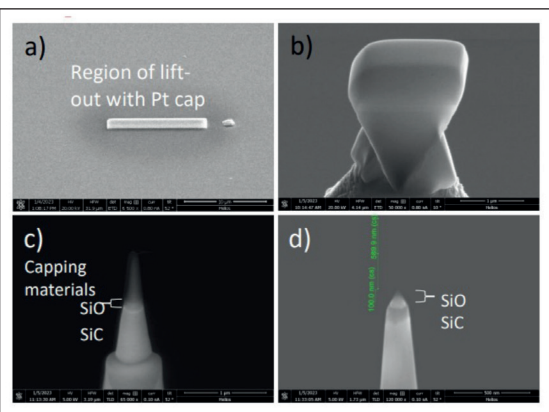


Figure 3. Typical scanning tunnelling electron micrscopy images of a sample ready for atom probe tomography measurements.

mass-to-charge ratio of the detected ions. The correlation of the chemical and physical properties of a specimen's surface aids characterisation of the mass spectra, as well as improving the precise accuracy of compositional material analysis and initial position at the specimen surface.

To determine the spatial distribution of atoms at the atomic scale, there is a need to generate a three-dimensional reconstruction of the analysed volume. This enables the determination of the local chemical composition of any arbitrary sub-volumes with a sub-nanometric resolution. Note that metals can provide concentration profiles with a depth resolution better than half an atomic plane.

Studying SiC MOSFETs

Within the SiC community, a two-step oxide-formation process has been widely adopted for making power MOSFETs. This involves either the thermal oxidation of SiC; or deposition of SiO_2, followed by interface nitridation with a nitric oxide gas. Neither process is ideal, leading to a high density of interface states. This issue continues to motivate effort to consider other processes for forming the gate oxide.

We have used atom probe tomography to study SiC MOSFETs produced with alternative processes that have much promise. Our study has considered both pre- and post-oxidation treatment with and without hydrogen gas, and the impact of a post-oxidation anneal using nitric oxide.
Our interest lies in understanding the elemental distribution of silicon, oxygen, carbon, nitrogen, hydrogen and argon in SiO_2, the SiO_2/SiC interface, and SiC beneath the SiO_2 layer (see Figure 2 for an illustration of the cross section of different zones of the sample). Through the use of atom probe tomography, we are able to gain insight into the composition and structure of these materials, and ultimately enhance our understanding of device characteristics, including interfacial properties, reliability of the gate oxide and MOSFETs channel mobility. In turn, these findings can enhance the development of new technologies and materials with improved performance and functionality.

The preparation of our sample began by sputtering 100 nm of nickel, followed by 300 nm of platinum, on the oxide surface to prevent subsequent damage. We then used annular ion beam milling at 30 kV to produce a needle geometry with a tip diameter of no more than 100 nm (see Figures 3(a-d) for typical images of the prepared sample).

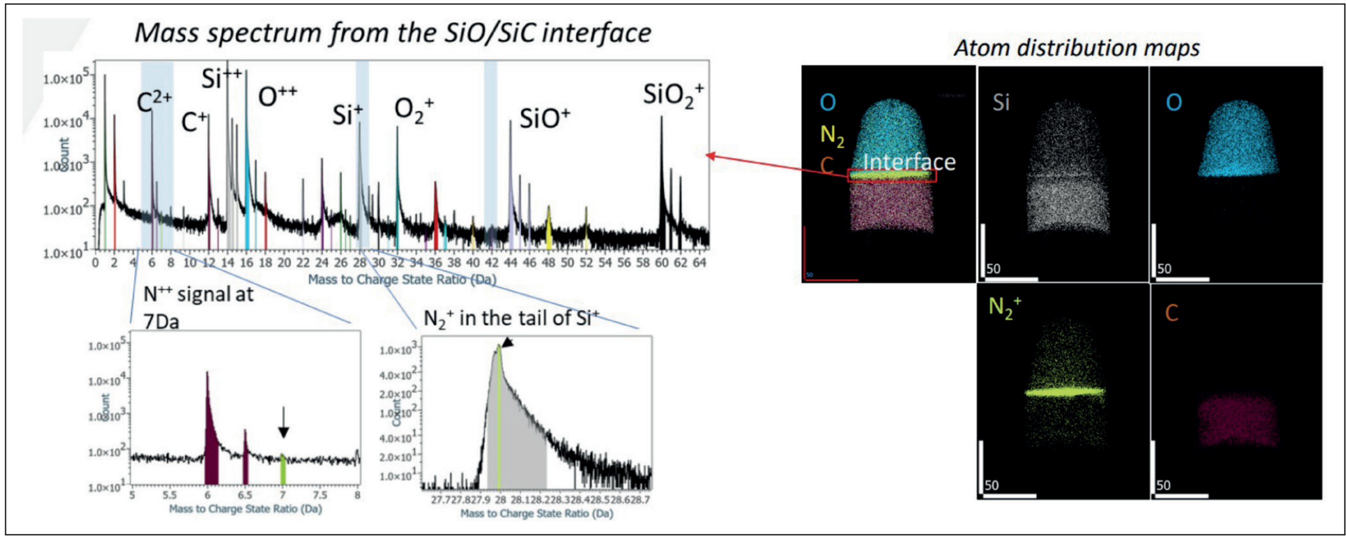
To mitigate damage from gallium implantation during the focused-ion beam process used for milling, all our specimens underwent low-energy cleaning with a 1 kV ion beam. This step is crucial for maintaining sample integrity and ensuring accurate results.

Our atom probe tomography measurements were undertaken with a laser power of 0.10 nJ/pulse to elucidate the influence of hydrogen gas treatment on the SiO_2/SiC interface. To ensure data reliability, we repeated experiments three times, for each type of sample. This ensured a rigorous approach, which gathered consistent, replicable results (see Table 1 for experimental details).

Atom probe tomography has enabled us to investigate the impact of hydrogen gas treatment before oxidation and after oxidation on the atomic distribution of different species in SiO_2 and at the SiO_2/SiC interface. Those species include carbon, nitrogen, oxygen, silicon and hydrogen (see Figure 4 for the line scan mass spectrum of different species and the three-dimensional elemental distributions for our sample that involved pre-oxidation hydrogen gas treatment, oxygen gas oxidation, and nitric oxide post-oxidation annealing).

Wafer	Experiments	Total Ions	Laser Power (nJ)	Pulse Frequency (Hz)	Temperature (K)
W4 (H_2 Anneal. +Oxi.+N_2 POA)	S1	13,952,096	0.10	367000	50
	S2	18,000,406	0.10	440000	50
	S3	30,000,210	0.10	200000	50
W6 (Oxi.+H_2 POA+ NO POA)	S1	13,952,096	0.10	367000	50
	S2	18,000,406	0.10	440000	50
	S3	30,000,210	0.10	200000	50

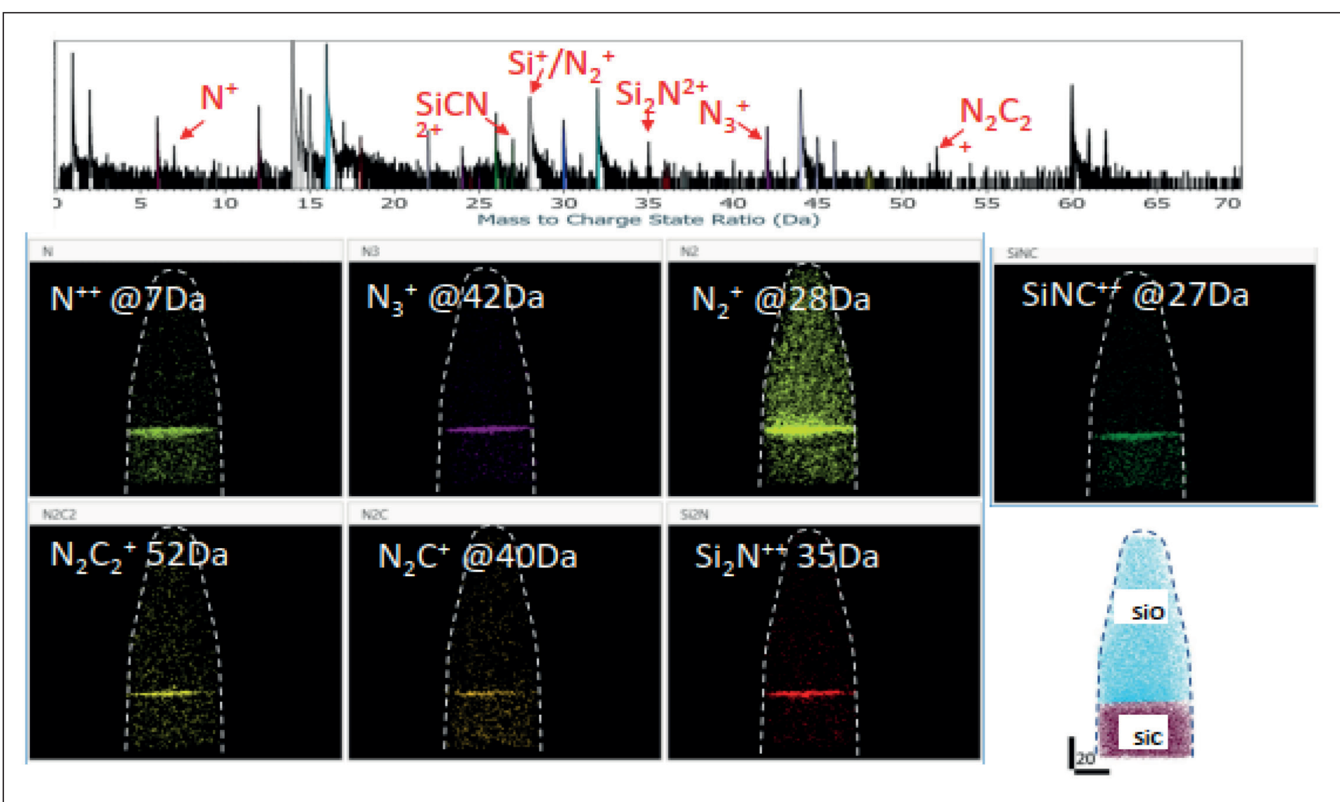
Table 1. Experimental parameters used for atom probe tomography analyses.



➤ Figure 4. The mass spectrum containing the interfacial region between SiO_2 and SiC from W4 obtained using atom probe tomography. Enrichment of nitrogen at the SiO_2/SiC interface is clearly observed in three-dimensional distribution maps.

The primary providers of the nitrogen signal are normally 7 Da (N^{++}), 14 Da (N^+), and 28 Da (N_2^+). Of these three, the detection of a possible N^+ signal at 14 Da is obstructed by the large Si^{++} signal.

For naturally abundant silicon, the ratio between Si-28/29 is 19.7. That's not the case for our sample with pre-oxidation hydrogen gas treatment, oxygen gas oxidation, and nitric oxide post-oxidation annealing. The presence of nitrogen at the interface changes this ratio, which is higher than that expected by a factor of 2.4. Using this piece of information, we applied a correction to deconvolute the nitrogen signal at the interface, obtaining an accurate concentration for this element of 4.0 percent. The three-dimensional atomic distribution clearly shows significant nitrogen



➤ Figure 5. Distribution of nitrogen-related signals in the analysed volumes obtained by atom probe tomography for the SiO_2/SiC interface subjected to oxidation with oxygen gas, and post oxidation annealing under hydrogen gas and then nitric oxide. Peak assignment has been undertaken based on the m/Z values: 7Da for N^{++}, 27Da for $SiCN^{2+}$, 28Da for Si^+ and $N_2^{\pm}$, 35Da for Si_2N^{2+}, 42Da for N^{3+}, and 52Da for $N_2C_2^{\ +}$, respectively.

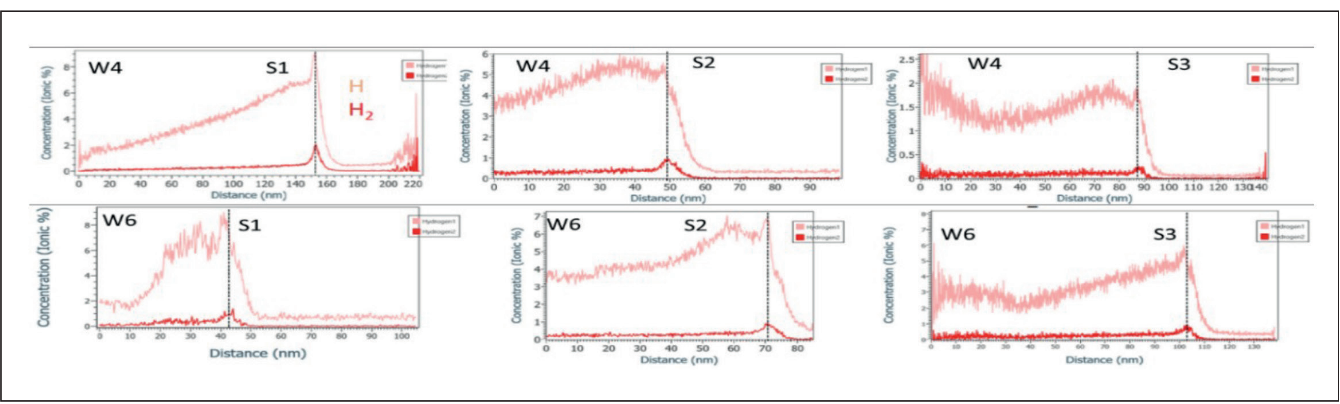


Figure 6. The plots show a reference for the observed trend of H and H_2 signals in the depth direction for the S1, S2 and S3 samples.

incorporation, predominantly at the SiO_2/SiC interface, with some traces in bulk SiO_2 as observed from the N^{2+} distribution map. Carbon is absent in both the SiO_2 and SiO_2/SiC interface.

We have also investigated the region-specific mass spectra of the SiO_2/SiC interface of the MOSFETs that undergo oxidation with oxygen gas, and post oxidation annealing under hydrogen gas and then nitric oxide. Region-specific mass spectra of the SiO_2/SiC interface are shown in Figure 5. There are a large number of nitrogen-containing peaks in this data, with red arrows used to indicate nitrogen-containing signals at the interface region.

The ejection of complex ions from this sample, a situation not observed in the other sample, suggests that the combination of post-oxidation annealing under hydrogen gas and then nitric oxide treatment at high temperatures may lead to the production of many compounds through a complex process. This process involves diffusion of hydrogen gas and nitric oxide, as well as a chemical reaction involving various atoms, including silicon, carbon, nitrogen, oxygen, and hydrogen.

On the other hand, the sample that has undergone hydrogen gas treatment before oxidation may have potentially taken part in hydrogen-termination, diffusion into interstitial spaces, and the creation of carbon-hydrogen bonds. Subsequent oxidation of the SiC surface layer may have decreased the possibility of a chemical reaction that forms many complicated compounds during post-oxidation annealing by nitric oxide.

We are surprised to note that our atomic concentration profiles show that there is nitrogen enrichment, confined at the interface to a depth of around 2.8 nm. We also note that we find no evidence for excess carbon or clustering in the bulk oxide, at the interface, or in SiC beneath the interface. Examining the hydrogen gas species, we observe an increase in the hydrogen signal in SiO_2 with depth, spikes at the SiO_2/SiC interface, and then a sharp decrease after crossing the interface.

The 2.8 nm-thick interfacial layer, rich in nitrogen and hydrogen, acts as a transition layer between materials. The presence of nitrogen and hydrogen plays a crucial role in reducing carbon cluster formation and passivating carbon or silicon-related defects at the interface. This passivation process helps to trim the interface state density and thus enhance the performance of the MOSFET, including its reliability. Further investigation is essential to verify both channel mobility enhancement and reliability properties of SiC power MOSFETs.

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Enhancing β-Ga_2O_3 diodes with oxygen annealing

Oxygen annealing and self-aligned mesa-termination takes β-Ga_2O_3 diodes further down the pathway to commercialisation

WHILE β-Ga_2O_3 power electronics has come a long way, challenges remain, including establishing high-yield processes for producing large-area devices with adequate breakdown voltages.

Making recent substantial progress on that particular front is a partnership between researchers at the University of Science and Technology of China and Hebei Semiconductor Research Institute. This team has shown that oxygen annealing of samples produced by HVPE of β-Ga_2O_3 reduces the surface roughness and the dislocation density of these films, leading to an increase in the breakdown voltage of Schottky barrier diodes.

According to team spokesman Feihong Wu, another of this team's breakthroughs is the use of mesa termination, which alongside the oxygen annealing has been used in the fabrication of devices as large as 3 mm by 3 mm. These Schottky barrier diodes, capable of blocking more than 700 V, deliver 8.7 A under a forward bias of 2 V.

Many techniques are available for the epitaxial growth of β-Ga_2O_3, including HVPE, MOCVD and MBE. Of these, MOCVD produces superior mobilities, while HVPE is renowned for the rapid growth of thick films and relatively low equipment costs.

Wu points out that the commercially available β-Ga_2O_3 samples sold by Novel Crystal Technology, Japan, are produced by HVPE.

"Therefore, it can be acknowledged that HVPE currently holds certain advantages," says Wu. "However, since commercially viable β-Ga_2O_3 samples are still under development, it is premature to determine which method is superior."

To investigate the influence of oxygen annealing, Wu and co-workers produced a portfolio of devices with undisclosed dimensions – but significantly smaller than 3 mm by 3 mm – using epiwafers from Novel Crystal Technology that feature a 10 μm-thick lightly silicon-doped drift layer, deposited by HVPE on a tin-doped β-Ga_2O_3 substrate with a carrier concentration of 5×10^{18} cm^{-3}.

Fabrication of the Schottky barrier diodes began by chemical cleaning, followed by thermal annealing for 30 minutes at either 200 °C, 400 °C, 600 °C or 800 °C. To eliminate the increase in ohmic contact resistance that results from annealing, the team turned to inductively coupled plasma etching, before adding contacts and then defining mesas with inductively coupled plasma etching (see Figure).

According to atomic force microscopy, annealing reduces the root-mean-square roughness, falling from 0.435 nm to 0.245 nm for a 2 μm by 2 μm scan area.

The current density of the team's diodes under a forward bias of 2 V falls with higher annealing temperatures, due to decreases in carrier concentration. The Schottky barrier height peaks at 1.16 eV, for annealing at 600 °C, and the breakdown voltage peaks at 400 °C. Wu and colleagues have also considered the power figure-of-merit, which peaks at 173 MW cm^{-2} at 400 °C, declared to be the optimum annealing temperature.

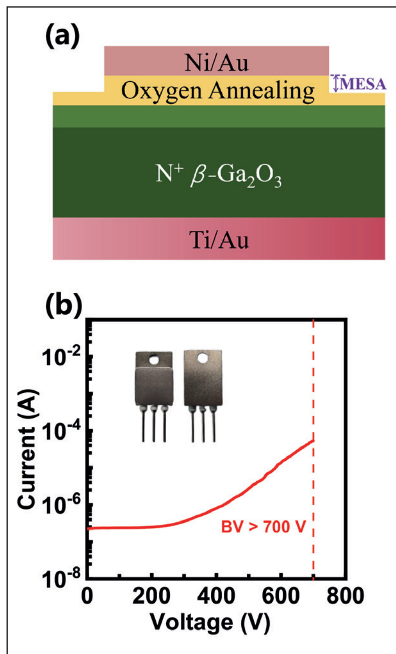
Etching, employed to produce the mesa structures, leads to increases in blocking voltage for all annealing temperatures, and is attributed to more extensive repairing of surface defects.

The team packaged its 3 mm by 3 mm diode in a TO-254 shell, using a parallel sealing and welding process to protect the device in a nitrogen environment. Benchmarking this device revealed that its power-figure-of-merit of 45 MW cm^{-2} is at the forefront of reported work.

Wu says that many of the devices used for benchmarking differ from their diode by employing complex terminal structures. "While there are some devices of similar area with simple structures, their performance does not match that of our device."

One of the team's plans is to develop a deeper understanding of the repair mechanism provided by oxidation annealing.

"Additionally, we aim to investigate the effects of oxygen annealing on mesa termination," says Wu. "For instance, we seek to understand why the device breakdown voltage experiences a significant increase when thermal oxidation is combined with mesa termination."



➤ (a) The addition of a mesa helps increase the blocking voltage (b) of β-Ga_2O_3 Schottky barrier diodes.

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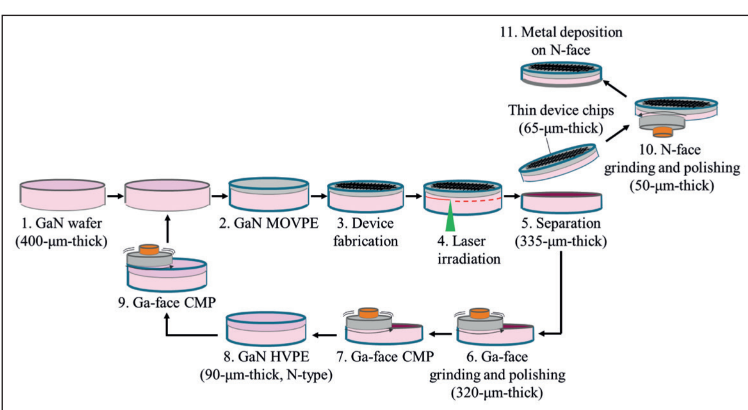
Cutting the cost of vertical MOSFETs with laser slicing

Slicing substrates with a 532 nm laser promises to trim the cost of producing GaN power MOSFETs without compromising performance

GaN VERTICAL MOSFETs are very promising power devices for electric vehicles, having the upper hand over SiC equivalents in channel mobility, a key metric. However, commercial success is held back by the high cost of the native substrate.

To address this concern, a number of teams have been investigating technologies for recycling GaN substrates. They include a collaboration between researchers at Mirise Technologies, Nagoya University and Hamatsu, that is claiming to have produced the most comprehensive demonstration of success with this approach.



➤ The GaN recycling process involves laser slicing and HVPE growth of GaN to maintain the thickness of the substrate.

According to team spokesman Takashi Ishida from Mirise, previous reports of recycling GaN substrates have been limited to evaluating just part of the process. “It is indispensable to evaluate the device characteristics fabricated on a recycled wafer,” argues Ishida, “and our paper reported this result for the first time.”

Ishida adds that while their result is encouraging, there’s more work to do before their process can be applied on an industrial scale. As GaN substrates need to be recycled multiple times to drive down manufacturing costs, there is a need to prove that devices are not compromised when grown on substrates produced from several rounds of recycling.

The Japanese partnership’s recycling process, outlined in the figure, involves separating the device and substrate with a 532 nm laser. This source, irradiated onto the substrate from the N-face, drives decomposition into metallic gallium and nitrogen via two-photon absorption at the focal plane.

Following separation, the N-face of the chips are ground and polished to obtain smooth surfaces, prior to metal deposition and mounting into packages.

Grounding and polishing is also applied to the Ga-face of the released substrate, prior to chemical mechanical polishing to realise flatness at the atomic level, followed by HVPE, used to deposit a layer of GaN with a thickness of around 90 μm. According to the team, after an additional chemical mechanical polishing step, the GaN substrate is as good as new.

To assess their process, the team have measured lateral MOSFETs and vertical *p-n* diodes fabricated from the same wafer. Both classes of device have been formed from epiwafers produced during the MOCVD of: a 4 μm-thick *n*-type GaN layer, doped to 1 x 10^{17} cm^{-3}; followed by a 2 μm-thick *p*-type GaN layer, doped to 5 x 10^{17} cm^{-3}.

This study began by evaluating the performance of both classes of device before and after slicing from a GaN substrate. Plots of the MOSFET drain and gate current at various gate voltages, and diode reverse currents under different values of reverse bias, showed no apparent changes due to laser slicing. This led the team to conclude that the devices are ‘virtually unaffected’ by the slicing process, which can lead to heating from the laser source and stress associated with the separation step.

Ishida and co-workers have compared these measurements with those for lateral MOSFETs and vertical *p-n* diodes produced using a recycled substrate. Results are very similar, with the difference in gate leakage of the lateral MOSFET attributed to a variation in the quality of the gate insulator.

According to the team, their results show that there is no critical degradation in device performance after the GaN recycling process.

Ishida says that in addition to recycling the GaN substrate, there needs to be an increase in its size to make the cost of device production more competitive. The team are interested in demonstrating their re-cycling process with larger GaN substrates.

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Deepening the understanding of post-trench restoration

A detailed investigation offers new insights into the impact of wet etching during the fabrication of trench-based GaN-on-GaN power devices

GaN-on-GaN POWER DEVICES, renowned for their high breakdown voltage, high current capability and excellent dynamic performance, often feature a trench architecture to improve performance. Typically defined by inductively couple plasma etching, this trench also increases leakage current while degrading channel and blocking characteristics, so wet etching with tetramethylammonium hydroxide (TMAH) is often employed to restore device performance. But what exactly happens during this anisotropic etching step?

Claiming to offer the most detailed answer yet to this crucial question is a team from Zhejiang University, China.

"Building on previous results, our work not only explores the relationship between corner morphology and electric field distribution, but delves deeper into the anisotropy of TMAH treatment, including differences in trench structure and surface morphology on *a*/*m*-plane sidewalls," says team spokesperson Yanjun Li. She points out that previous studies have only focused on how TMAH treatment yields smoother trench bottom corners, thereby enhancing the device's breakdown voltage.

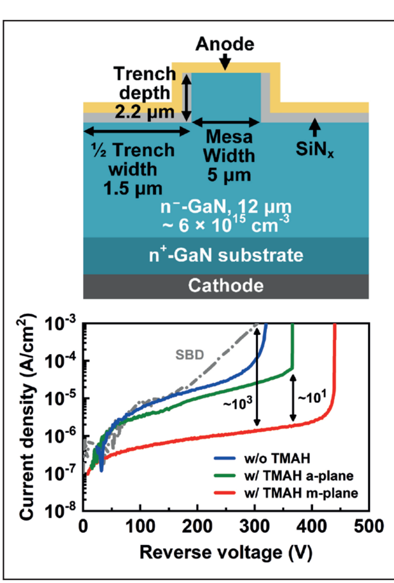
The team produced trench structures through inductively couple plasma etching, using a mixture of chlorine gas and BCl_3, and a SiO_2 hard mask. Employing a chamber pressure of 10 mTorr, the team assessed the impact of etching at RF powers of 100 W and 20 W, inductively couple plasma powers of 150 W and 250 W, DC bias conditions of 300 V, 200 V and 95 V, and the use and absence of TMAH treatment.

A scanning electron microscope revealed the presence of micro-trenches in some samples, caused by deflected ions that bombard the bottom of the sidewall. These micro-trenches, which could lead to significant electric-field crowding in vertical GaN power devices, can be avoided with a low DC bias, realised by increasing the inductively coupled plasma power and decreasing the RF power.

Li and co-workers refined the profile of the trenches by wet-etching in a 25 percent concentration of TMAH at 85 °C for 1 hour. Inspecting these trenches with a scanning electron microscope showed that all sidewalls become more vertical after etching. However, the *a*-plane has sharp bottom corner, while the *m*-plane sidewall has a rounded bottom corner. According to Li, simulations and experimental results demonstrate that this anisotropy suppresses electric-field crowding along the *m*-plane sidewall, in contrast to the *a*-plane sidewall. "This highlights the need for paying attention to crystal orientation during the design and fabrication of vertical GaN power devices."

The anisotropy introduced by TMAH treatment extends to sidewall surface morphology. This wet-retching step does not improve the striped, rough surface produced on the *a*-plane sidewall by the inductively coupled plasma, but TMAH treatment leads to a noticeably smoother *m*-plane sidewall.

"Typically, a smoother surface is beneficial for reducing scattering of carriers in the channel, thereby enhancing device conduction characteristics," points out Li.



➤ Wet etching quashes the reverse-bias leakage current in trench MOS barrier Schottky rectifiers.

To assess the impact of post-trench treatment on reverse-blocking characteristics, Li and her co-workers produced trench MOS barrier Schottky rectifiers featuring a 12 µm-thick *n*-type GaN drift layer. For these devices, featuring a 2.2 µm-deep trench with a mesa width of 5 µm and a trench width of 3 µm, electrical measurements highlight the benefit of TMAH treatment. This wet etching reduces leakage current, particularly along the *m*-plane (see Figure).

Additional work by the team involved the fabrication of metal-oxide semiconductor capacitors, used to determine the capacitance and the density of interface states of the mesa, trench bottom and sidewalls.

"The density of interface states for the etched sidewall is critical for vertical GaN power transistors, as the sidewall is typically utilized as the channel region," says Li.

The team is now planning to employ its post-trench restoration process to the vertical GaN trench MOSFET, where the trench sidewall surface serves as the gate channel.

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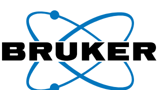

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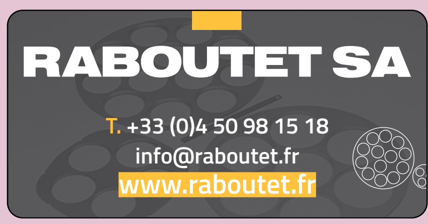

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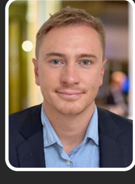

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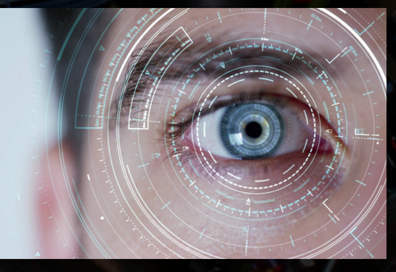

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