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VOLUME 31 ISSUE III 2025

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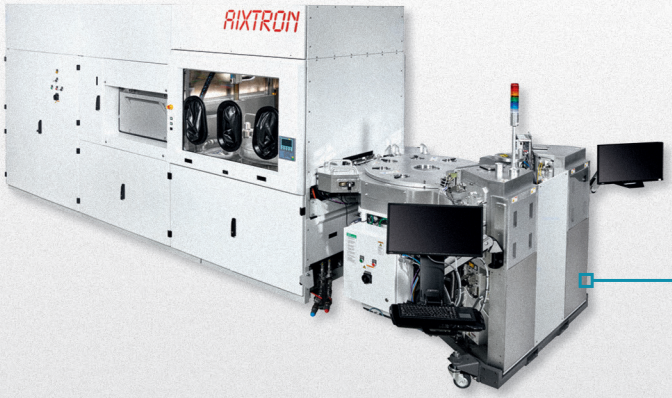


G10-SiC

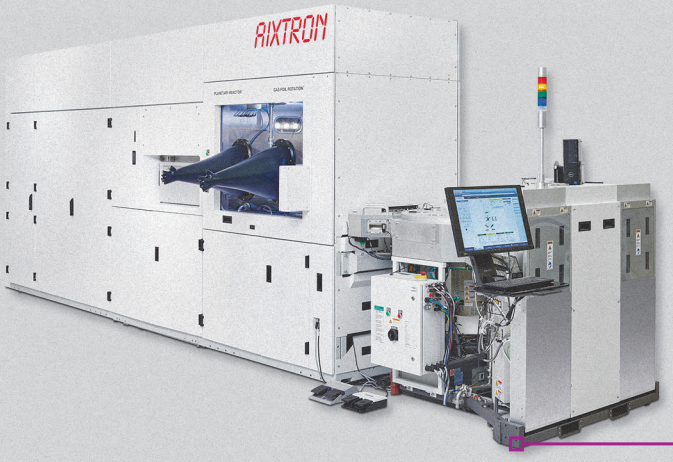
- 9x150 mm (6") or 6x200 mm (8")
- New hardware & process surpassing Single Wafer Reactor uniformities
- +50 % productivity per fab area with large batch technology & small footprint

End Markets/Products:
EV inverters & charging infrastructure

G10-GaN

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated compact GaN MOCVD cluster designed 100 % for Si Power fabs
- Novel hardware solution for unmatched barrier uniformities and device yields

End Markets/Products:
Power Electronics & Wireless communication



G10-AsP

- 8x150 mm (6") or 5x200 mm (8")
- 1st fully automated AsP MOCVD system enabling 10x lower defect density
- Unmatched wavelength uniformity on all wafer sizes

End Markets/Products:
Micro LED, Optical Data communication, 3D-sensing & LiDAR

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

Tumultuous tariffs

This April, CS International celebrated its 15th anniversary. You'll not be surprised that I have been to them all, and I still really look forward to attending. As well as hearing plenty of talks, providing an excellent overview of how our industry is progressing on all key fronts, I enjoy the numerous networking opportunities.

Often my conversations with delegates from all around the world focus on matters related to the commercialisation of new technologies, such as microLEDs and ultra-wide bandgap devices. But this year, global events dominated our conversation, as the Trump administration had just announced details of its tariffs, which sent stock markets into a tailspin.

I failed to find anyone who is supportive of these measures. That's hardly surprising, as working with other countries is the norm for our industry. Raw materials are mined in one location and shipped elsewhere to produce boules, which are sliced and polished into substrates, possibly using equipment made in other countries. And then there's the growth of epiwafers, chip production, and packaging, activities that may involve goods transported over borders. The thought of high tariffs at every stage threatens a snowballing of prices for compound semiconductor devices, which will be used in products subjected to additional tariffs.

However, while widespread tariffs are not popular, and are viewed as a blunt instrument that will harm our industry – and the world at large – they are being introduced against the backdrop of an unlevel playing field. Understandably, governments all around the world have always taken steps to support their own industries. But there's no agreement on what's fair and what oversteps the mark.

I'm aware that Washington has a strong desire to bring manufacturing back to the US, to generate wealth for the nation. It's a laudable aim, involving replacing global

supply chains with sovereign capability. However, it's hard to imagine the introduction of packaging houses in the US, a move that would struggle to generate good wages for workers or competitive products for the domestic market.

Since my return from CS International, the US has started to tinker with its tariffs. Initially, Washington watered them down to many countries, a move that's helped turbulent stock markets recover some of their losses. And more recently, there has been a slashing of the whopping 125 percent tariff imposed on China for a range of products, including smartphones, electronic devices and components, such as semiconductors, solar cells and memory cards.

I'm almost certain that by the time you read this there will have been more adjustments to Trump's tariffs. These changes might be good or bad, but what's sure is that we are living in an era of uncertainty – and that's a headwind to both the compound semiconductor community and the global economy.

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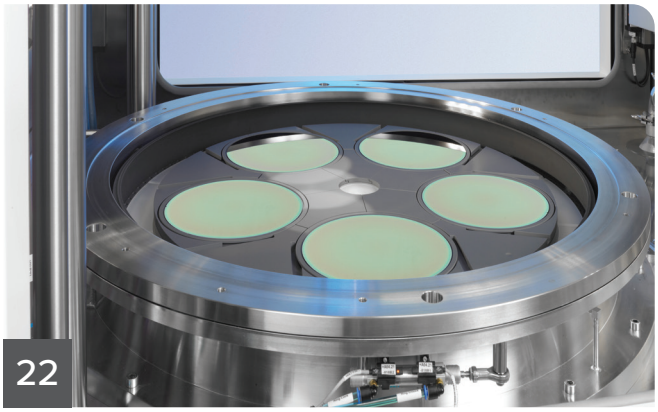

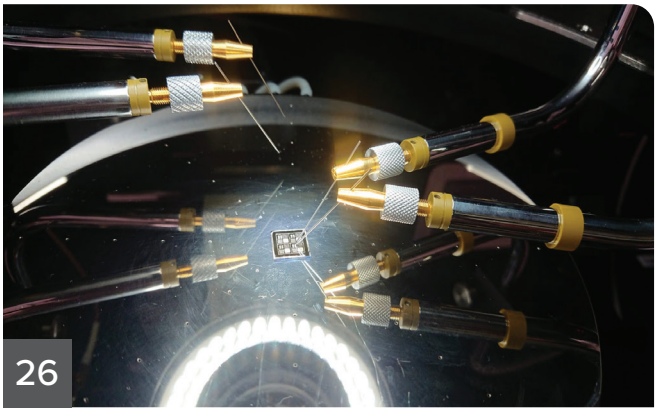

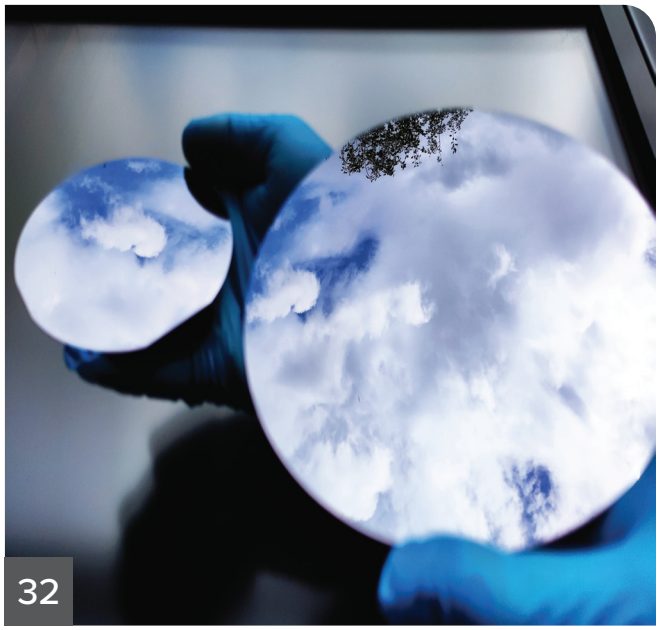

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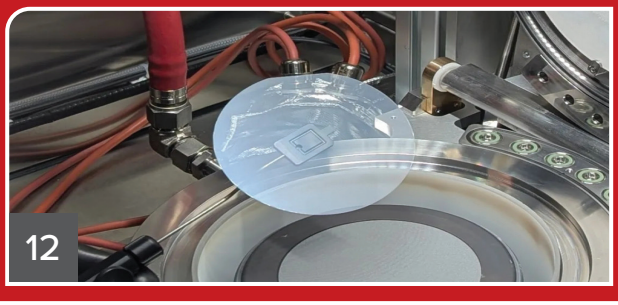

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T: +44 (0)2476 718970 **E:** info@angelbc.com
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Angel BUSINESS COMMUNICATIONS

Compound Semiconductor is published nine times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £115.00 per annum (UK), €165 per annum (Europe), $198 per annum (air mail) (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2025. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing. US mailing information: Compound Semiconductor, ISSN 1096-598X, USPS Permit Number 25366, is published 9 times a year, Combined Jan/Feb, March, Combined April/May, June, July, Combined August/September, October, November, December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP, UK. Airfreight and mailing in the USA by agent named World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA. Periodicals Postage Paid at Brooklyn, NY 11256. POSTMASTER: Send address changes to Compound Semiconductor, Air Business Ltd, c/o World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA. We strive for accuracy in all we publish; readers and contributors are encouraged to contact us if they recognise an error or omission. Once a magazine edition is published [online, in print or both], we do not update previously published articles to align old company names, branding, marketing efforts, taglines, mission statements or other promotional verbiage, images, or logos to newly created or updated names, images, typographic renderings, logos (or similar) when such references/images were accurately stated, rendered or displayed at the time of the original publication. When companies change their names or the images/text used to represent the company, we invite organizations to provide Angel Business Communications with a news release detailing their new business objectives and/or other changes that could impact how customers/prospects might recognise the company, contact the organisation, or engage with them for future commercial enterprise.
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SiC slowdown is only short term, says Yole

BEV slowdown is delaying short-term expansion, but the $10 billion future remains on track

DESPITE a temporary slowdown in BEV shipments, the SiC market remains on a long-term growth trajectory, according to the Yole Group.

Its analysts forecast the power SiC market will exceed $10 billion by 2029, driven by a strong rebound in 2026 with CAGR between 2024 and 2029 close to 20 percent.

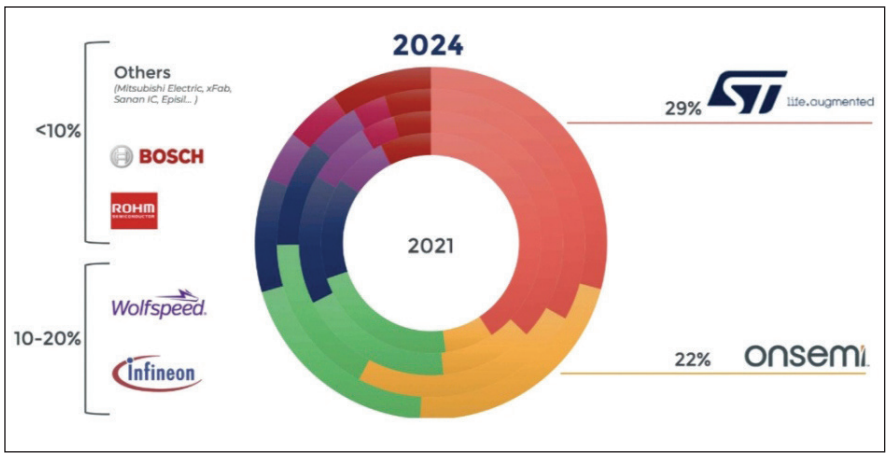
“SiC adoption has accelerated since 2018-2019, primarily led by Tesla, the early disruptor in automotive electrification. In 2024, Tesla continued to dominate the SiC-based BEV segment with nearly two million units shipped, although that figure is down 5 percent from 2023,” said Poshun Chiu, senior technology and market analyst at Yole Group.

Meanwhile, other OEMs, especially from China, are gaining ground. BYD, Nio, Geely, and Xiaomi are expanding their SiC-based BEV portfolios.

Despite these positive trends, the overall market deceleration has impacted the revenue growth of key SiC suppliers such as STMicroelectronics and onsemi, though Infineon Technologies continues to grow, supported by its diversified applications across both automotive and industrial sectors.

While many players are expanding capacity, especially in transitioning from 6-inch to 8-inch wafers, current end-system demand may not yet justify this scale.

Ezgi Dogmus, activity manager, Compound Semiconductors at Yole Group says: “Industry feedback suggests that total announced capacity could outpace short-term SiC device consumption. Suppliers are now adjusting production volumes on a per-order basis and slowing down some expansion plans to match market realities for 2024 and 2025.”



Key factors to monitor include wafer quality, yield, and supply chain efficiency. As competition intensifies, vertical integration becomes more critical. Leading companies, including STMicroelectronics, onsemi, Wolfspeed, and Infineon Technologies, are doubling down on internal wafer manufacturing and module production to meet their billion-dollar revenue targets.

Yole identifies STMicroelectronics’ approach as one of the most ambitious moves among non-Chinese semiconductor players. Faced with rising competition and China’s push for local sourcing, the leading semiconductor company has adopted a unique ‘become Chinese in China’ strategy.

Yole Group’s analysts spotlight three key partnerships underpinning this approach: a $3.2 billion joint venture with Sanan Optoelectronics for SiC devices, a manufacturing collaboration with Hua Hong Semiconductor for 40 nm automotive MCUs, and a strategic investment in GaN leader Innoscience. These moves are designed to localise production, support Chinese OEMs, and secure long-term market share in China’s EV and industrial sectors.

This detailed analysis, based on the *Power SiC/GaN Compound Semiconductor Market Monitor, Q1 2025*, suggests that these bold moves could significantly boost STMicroelectronics’ growth from 2026 while also shaping the competitive landscape in SiC markets.

Yole says although the short-term outlook has cooled, analysts remain confident in SiC’s long-term momentum, especially as BEV demand recovers and industrial applications continue to expand.

Despite these positive trends, the overall market deceleration has impacted the revenue growth of key SiC suppliers such as STMicroelectronics and onsemi, though Infineon Technologies continues to grow, supported by its diversified applications across both automotive and industrial sectors

£250 million to turbocharge Welsh cluster

Vishay's investment in UK's largest semiconductor fab will be vital to EV production and support hundreds of highly-skilled jobs

WALES is set to benefit from a £250 million investment from the semiconductor company Vishay Intertechnology, that will be vital to the production of electric vehicles, supporting the UK government's Plan for Change in delivering more skilled jobs, and turbocharging the economy.

The Chancellor Rachel Reeves is welcoming Vishay Intertechnology's intention to invest in the Newport plant – the UK's largest semiconductor facility – as part of plans to develop large-scale compound semiconductor manufacturing in the country.

The investment will boost production at the factory where it will make advanced SiC semiconductors. Vishay's investment is expected to directly support over 500 high value, high skilled jobs in the region and indirectly support hundreds more in the wider supply chain.

It comes after the Chancellor Rachel Reeves' Spring Statement where she vowed to bring about "new era of security and national renewal" to kickstart economic growth, protect working people and keep Britain safe.

Supported by the government's Automotive Transformation Fund (ATF), the investment will help secure domestic supplies of semiconductors critical to the UK automotive industry, and other key industries including renewable energy and defence.

This funding also strengthens the UK's position in a competitive, global semiconductor landscape, supporting long-term growth for the UK economy.

Through the ATF, delivered in partnership with the Advanced Propulsion Centre (APC), the UK government continues to unlock private investment in UK automotive design,

development, and manufacturing as the sector transitions to zero emission technology. To date, the ATF and APC funding programmes have leveraged over £6 billion of investment from the private sector.

The UK's Autumn Budget confirmed over £2 billion for capital and R&D funding over five years for zero emission vehicle manufacturing and their supply chains. Mike Hawes, SMMT (Society of Motor Manufacturers and Traders) CEO, said: "This significant investment in compound semiconductors is a huge contribution to the innovation and advanced technology necessary to drive the future of UK Automotive. British-made next-generation semiconductors will create jobs, support supply chains and enhance the UK's strategic capabilities."

Secretary of State for Wales, Jo Stevens, said: "This massive investment by Vishay and the UK Government is a huge boost for Wales's world-leading semiconductor industry. Earlier this month I was at Vishay to see the work they do on advanced manufacturing, renewable energy and defence industries – all key sectors in the Welsh economy."

Wyn Meredith, chair of CSconnected, the Welsh Semiconductor Cluster, said: "Since the launching the Welsh Semiconductor Cluster in 2015, our partners have invested heavily in creating a world-leading research and innovation ecosystem, with a highly skilled talent pipeline to address a semiconductor market opportunity which is set to surpass $1 trillion per annum by 2030. Global semiconductor players like KLA, Microchip, IQE, Vishay, and recently announced Cadence, have recognised the value of our proposition and have committed in excess of £600 million investment to fuel the continued growth of semiconductor manufacturing in South Wales."

Roy Shoshani, COO Semiconductors and CTO for Vishay, said: "This is an exciting moment, and the start of our plans for growth in the UK. We can see through the development of the Industrial Strategy and the skilled workforce in Newport that there is a real opportunity to play to the UK's strength in advanced semiconductors, delivering greater economic security and supporting Net Zero."

Aixtron delivers InP tool to Nokia

G10-AsP system will allow company to produce 6-inch InP wafers for next gen photonics

AIXTRON SE will supply Nokia with its G10-AsP system to enable the company to produce 6-inch InP wafers, marking the next step in the evolution of photonic integrated circuits (PICs).

This follows Nokia's completion of its $2.3 billion acquisition of InP specialist Infinera, in late February 2025.

The G10-AsP system is designed to provide precise and uniform processes that PICs require in contrast to traditional transceivers, as demonstrated in particular on 6-inch InP wafers.

For example, thanks to an innovative injector and advanced temperature control the platform offers up to 4 times superior on-wafer-uniformity for critical layers compared with the previous generation, according to Aixtron.

Combined with *in-situ* cleaning, the company says these new levels of uniformities can be consistently reproduced without the need for hardware exchange or calibration between the different growth steps of the complex circuits. The automated cassette-to-cassette wafer loading ensures highest operator efficacy for the MOCVD tool.

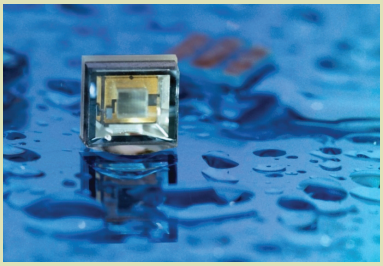
"We are thrilled to support Nokia's innovation in photonic integrated circuits with our G10-AsP system. The ability to produce 6-inch InP wafers will significantly enhance their manufacturing and technology capabilities and drive the adoption of next-generation optical technologies," said Felix Grawert, CEO and president of Aixtron SE.

Steve Stockman, who leads Nokia's InP-based PIC manufacturing added: "The acquisition of Aixtron's state-of-the-art G10-AsP platform is a strategic investment in our production capabilities. This advanced technology will enable us to meet the growing demand for high-performance photonic integrated circuits and expand our leadership in the industry."

CrayoNano puts assets up for auction

IN A SAD STORY of an innovative firm running into funding problems, CrayoNano, the Norwegian UVC LED company, has filed for bankruptcy and recently auctioned its assets.

Back in August 2024, the company announced record shipments to the drinking water disinfection market in North America, and around the same time raised $1.5 milion (16.2 million NOK) capital in a private placement.



But there continued to be liquidity problems, despite the company's management and board working hard to raise capital to sustain operations and facilitate the long-term business plan.

Early December 2024, despite interest from several investors in a subscription for a Convertible Loan to raise a minimum of around $1.4 milion (15 million NOK), CrayoNano did not receive enough subscriptions to cover it.

The company continued discussions with potential industrial partners but eventually exhausted all options to secure short-term financing. In January this year, it came to the end of the line and filed for bankruptcy.

The auction to acquire CrayoNano's complete technological assets took place on March 17. It included patents, research materials, hard disks and servers.

Wolfspeed appoints new CEO amidst funding crisis

Chip veteran Robert Feurle takes the helm of SiC specialist at time of great uncertainty over $750 million expected CHIPS Act Funding

US SiC specialist Wolfspeed has appointed Robert Feurle as CEO, effective May 1, 2025. Feurle succeeds Thomas Werner, who is serving as interim executive chairman and will return as chairman of the board following the transition.

Feurle brings more than 20 years of leading organisations that develop advanced power semiconductor solutions in automotive and other high-voltage applications, including both silicon and SiC. However, he arrives at a difficult time for Wolfspeed, whose shares on the 28th March 2025 lost half their value (hitting their lowest level since 1998), as funding through a Joe Biden-era legislation that promised subsidies for chip making in the United States remains uncertain.

Wolfspeed is waiting on about $750 million in federal funding under the US CHIPS Act, the 2022 bipartisan law which promised $52.7 billion in subsidies for domestic semiconductor chips manufacturing and production. But earlier this month, President Donald Trump said US lawmakers should get rid of the law and use the proceeds to pay debt.

“Wolfspeed’s CHIPS Act grant ended up being the highest-dollar CHIPS grant

to not be officially awarded before Biden’s exit, leaving it particularly vulnerable to being pulled under the new administration,” Brooks Idlet, senior analyst at CFRA Research told the news agency Reuters.

Without the grant, Wolfspeed would face devastating consequences requiring major restructuring to preserve cash, Idlet added. The chipmaker has revealed that it accrued $865 million in tax credits, using which it intends to strengthen its capital structure.

Feurle previously served as executive VP and general manager of the Opto Semiconductors Business Unit at Ams Osram AG, where he was responsible for managing more than 10,000 employees in sites and factories around the world. There, he expanded market share and accelerated the introduction of cutting-edge LED and laser products into automotive and new advanced LED applications.

During his tenure at Infineon, Feurle became familiar with the SiC industry. He said: “I believe we have just begun to scratch the surface of the vast potential of SiC. Wolfspeed’s world-class facilities, exceptional talent, and robust intellectual property, position us to maintain and expand our market leadership”.

At Infineon, he spearheaded new product introductions in the field of IGBT and SiC technologies and increased focus on competitive differentiation and profitable growth.

He was also part of the team at Infineon supporting the proposed acquisition of the Wolfspeed operations in 2016.

A citizen of both the United States and Germany, Feurle will be returning to the United States where he previously spent a decade in executive roles at Micron Technology and will be relocating to the company’s headquarters in Durham, North Carolina, where he will work closely with Werner to ensure a smooth transition.

Lumentum shows InP advances at OFC

Company demonstrates readiness for 400G-per-lane AI data centres

AT THE RECENT OFC 2025 exhibition in San Francisco, Lumentum announced a number of advances in its InP photonic chip technologies for delivering higher bandwidth and more power efficiency in next-generation AI data centres.

The InP innovations enable future 400 Gbps-per-lane optical links, more efficient 200 Gbps-per-lane optical links, and co-packaged optics.

"Building on decades of InP expertise, Lumentum is driving industry technology leadership and volume production readiness for the future 400G per lane generation of optical interconnects, along with more efficient 200G per lane optical interconnects, to enable data centre compute capacity scaling," said Matt Sysak, Lumentum CTO of Cloud and Networking.

"Lumentum InP technology is also enabling new co-packaged optics solutions to significantly reduce power consumption in AI data centre networks, supporting larger AI installations and accelerating the

transition from copper to photonic interconnects." For example, Lumentum demonstrated two key 400 Gbps-per-lane photonic technologies which will enable the 3.2T generation of optical transceivers at OFC 2025.

These included a 448 Gbps data transmission using a 224 GBaud PAM4 externally modulated laser technology in collaboration with Keysight Technologies and NTT Innovative Devices. And a 450 Gbps PAM4 distributed feedback (DFB) laser with an integrated Mach-Zehnder modulator for 400 Gbps-per-lane technologies.

To address power challenges in bandwidth scaling, Lumentum engineers presented a technical paper at OFC 2025 detailing results from Lumentum's new 200 Gbps-per-lane differential drive electro-absorption modulated laser. These lasers operate at a lower drive voltage, reducing power dissipation while offering excellent signal integrity and cross-talk immunity.

Lumentum also highlighted its ultra-high power (UHP) 1310 nm DFB lasers designed for co-packaged optics to support higher-density optical interconnects.

The UHP platform is based on InP pump lasers for Raman amplification applications.

5N Plus gives GaN IP back to Allos

5N Plus Inc, a Canada-based producer of specialty semiconductors and materials, has entered into an agreement, through its subsidiary, Azur Space Solar Power GmbH, with Dresden-based microLED and GaN-on-silicon expert Allos Semiconductors.

The aim is to complete the development and commercialisation of a GaN IP portfolio that 5N Plus has provided to Allos Semiconductors for a nominal value in exchange for future royalties.

Prior to becoming part of 5N Plus in 2021, Azur had acquired a package of technology and patents for High Power Electronics (HPE) and RF applications from Allos Semiconductors in 2020. This package will now be transferred back to Allos, along with additional GaN IP.

"This transaction allows 5N Plus to focus on its core business while benefiting from the growth of the HPE market through royalties. With Allos, we have found the strongest possible partner to commercialise the technology over time," said Gervais Jacques, president and CEO, 5N Plus.

"With this acquisition we are further strengthening our IP position," said Burkhard Slischka, co-founder and CEO of Allos Semiconductors.

The company specialises in 200 mm and 300 mm epiwafers for microLED applications that can be processed in standard silicon fabs. Allos' customers are microLED and display companies, working with silicon foundries to achieve the yield and unit cost breakthroughs that are critical to turning microLED display prototypes into mass consumer products.

Slischka added: "We remain focused on our successful microLED technology while exploring synergies with the rapidly growing HPE market. We are open to new partnerships in GaN HPE and our now expanded IP portfolio remains available for licensing."

Navitas Partners with Great Wall for 400 V-DC power

GaNSense technology boosts 8-times power in ultra-high power density DC-DC converters

GaN and SiC specialist Navitas Semiconductor has announced that its GaNSense power ICs will power GreatWall's latest 2.5 kW ultra-high power density DC-DC converter for AI data centres.

Great Wall has developed a 2.5 kW DC-DC converter in 1/4 brick outline with what it claims is the world's highest power density of 92.36W/cm^3, up to 8 times higher than the output power of traditional silicon designs.

With a high half-load efficiency of 97.9 percent and a wide input range of 320-420 V_{DC}, this solution achieves the increasingly stringent efficiency guidelines and regulations from Open Compute Project and can be widely used in applications from AI data centres, telecommunications, and industrial equipment.

The DC-DC converter is powered by Navitas' GaNSense NV6169. The 650 V, 45 mΩ device is claimed to deliver 50 percent more power than prior designs, in an industry-standard, low-profile, low-inductance, 8 x 8 mm PQFN package for high-efficiency, high-density power systems.

GaNFast power ICs with GaNSense technology have features such as loss-less current sensing and fast short-circuit protection, with a 'detect-to-protect' speed of only 30 ns, six times faster than discrete solutions.

NV6169 is rated at 650 V for nominal operation plus an 800 V peak-rating for robust operation during transient events. The GaN gate is fully-protected and the whole device rated at 2 kV.

"With its faster switching frequency and higher efficiency, GaN has become a key factor in unlocking the next generation of power supplies," said Michael Zhang, head of DC Product Line at Greatwall Power. He added: "We are very pleased to collaborate with Navitas, an industry leader in GaN technology, and successfully enable this industry-leading ultra-high-power density and ultra-high efficiency DC-DC converter."

MoD to put £200 million into UK compound semi fab

THE UK's MoD will put a further £200 million into Octric Semiconductors, the re-named GaAs fab in Newton Aycliffe, County Durham which the Ministry of Defence (MoD) bought in September 2024 for £27 million.

According to a report in *Electronics Weekly*, the investment will be used to produce GaAs and GaN chips for military systems, radars and power electronics. Octric aims to expand with further processes: it is looking for engineers with experience in a range of compound semiconductors, including InP.

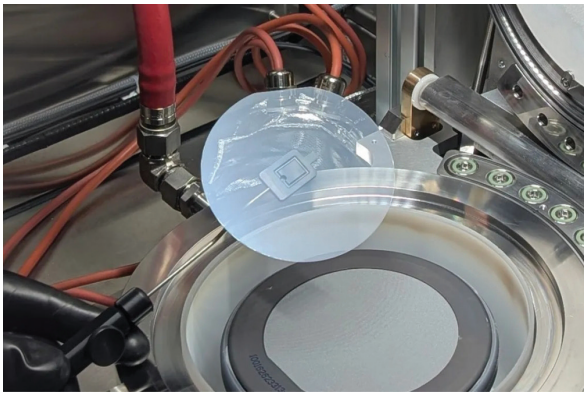
Most recently owned by US company Coherent, the UK fab was bought by the MoD as a crucial supply chain to UK defence.

The site is said to be the only secure facility in the UK with the skills and capability to manufacture GaAs semiconductors, vital for a number of military platforms, including to boost fighter jet capabilities.

4-inch gallium oxide facility established in Swansea

University centre to become national hub for thin film gallium oxide R&D

RESEARCHERS at the Centre for Integrated Semiconductor Materials (CISM) at Swansea University have established the first 4-inch thin film gallium oxide (Ga_2O_3) capability in the UK.



This advance was achieved using a newly commissioned Aixtron close-coupled showerhead deposition system that can precisely grow high-quality crystalline thin-film gallium oxide on 4-inch substrates. These have been tested and shown to be uniform and of high quality.

This capability is housed in the new Oxide and Chalcogenide MOCVD Laboratory at CISM, which is now set to become a national hub for thin-film gallium oxide research and development in areas such as power electronics, deep-UV photodetectors and transparent conductive oxide applications.

Dan Lamb, research lead at the Oxide and Chalcogenide MOCVD Centre said: “This new facility represents a major step forward for our research, and I’m incredibly excited about the possibilities it unlocks for novel materials and device development. With this advanced equipment, we can push the boundaries of our existing work while also creating new opportunities for collaboration with research groups across the UK and beyond.”

John Heffernan of the National Epitaxy Facility, which supports semiconductor research in UK universities, said: “Swansea University’s MOCVD capability is now accessible to researchers through direct collaboration. Researchers can also gain access to feasibility studies through Swansea partnering with the UK National Epitaxy Facility’s Pump Priming scheme. This initiative ensures that academic and industrial partners can leverage Swansea’s expertise in epitaxial thin-film growth to accelerate their research and technology development.’

The achievement follows the recent announcement of a £250 milion investment by Vishay supported by the UK Government’s Automotive Transformation Fund in it’s Newport plant to dramatically expand advanced wide band gap power semiconductor component manufacturing.

Sam Evans, director of quality assurance and external affairs, Vishay Newport, said: “This is a major step forward for wide band gap materials innovation in our South Wales Semiconductor Cluster, underpinning efforts to grow regional manufacturing in advanced power electronics such as Vishay’s recently announced £250 million investment in SiC component expansion.”

The deposition system was funded by a £2.7 million grant from the Engineering and Physical Sciences Research Council (EPSRC – Strategic Equipment Programme), reinforcing the UK’s commitment to advancing semiconductor innovation.

Polar signs GaN-on-silicon agreement with Renesas

Partnership to make 650 V GaN-on-silicon devices in Minnesota aims to strengthen the US supply chain

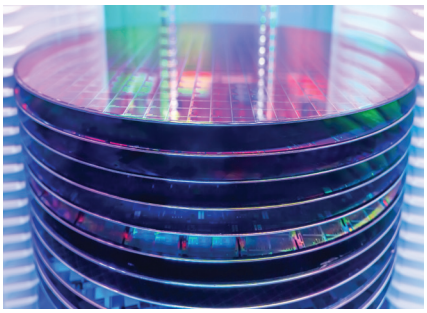
POLAR SEMICONDUCTOR, a US-owned merchant foundry, has sighed a deal with Renesas Electronics to license the Japanese firm's GaN-on-silicon D-Mode GaN-on-silicon technology.

As part of this agreement, which is to ensures the US has a reliable, domestic source for this semiconductor technology, Polar will fabricate high-voltage 650 V class GaN-on-silicon devices for Renesas and other customers in its 200 mm automotive quality high-volume manufacturing facility in Minnesota.

Polar and Renesas will work together to scale commercial production of GaN devices, expanding its use across automotive, data centre, consumer, industrial, and aerospace and defence markets. The agreement ensures the US has a reliable, domestic source for this cutting-edge semiconductor technology.

Surya Iyer, president and COO of Polar Semiconductor said: "This licensing and commercial production agreement underscores our commitment to strengthening the domestic semiconductor ecosystem. GaN is a game-changing technology for power and RF, and with Renesas as our partner, we are well-positioned to ramp commercial production, secure key defence programs, and drive the next wave of semiconductor innovation."

"We are excited to partner with Polar to scale our proven GaN technology to 200 mm wafers and leverage our know-how across broad power conversion



markets ranging from infrastructure and AI to energy and industrial to e-Mobility and xEVs to high-value IoT," said Chris Allexandre, SVP nd GM, power products group, at Renesas. "This collaboration ensures a strong, US-based manufacturing capability for GaN products, provides multi-sourcing to our customers, and meets the growing demand for high-performance power solutions."

Navitas and GigaDevice announce partnership

NAVITAS SEMICONDUCTOR has announced a partnership with GigaDevice, a Chinese maker of microcontrollers and flash memory, to create a joint-lab for integrating and tailoring Navitas' GaNFast ICs and GigaDevice's microcontrollers for AI data centres, EVs, solar, and energy saving systems.

As GaN and SiC power technologies transition power conversion to faster, lighter, and more compact solutions, such as single-stage BDS converters, MCUs need to be optimised to maximise fast switching characteristics, such as high processing speeds and fast I/O capabilities.

A co-developed solution of Navitas' power and GigaDevice's control will further accelerate the adoption of GaN and SiC into higher-power markets, according to the companies.

The joint R&D laboratory will integrate both company's technical product and system-level application expertise to develop power management solutions. Integrating Navitas' GaNFast technology with GigaDevice's advanced MCU products will enable a new level of integration, performance, and high-power-density digital-power solutions. GigaDevice has been widely adopted across diverse sectors including power systems, industrial automation, automotive electronics, and motion control, with cumulative shipments exceeding 2 billion units.

GigaDevice's GD32 MCU series has been designed for applications including industrial automation, photovoltaic energy storage, graphic displays, digital power supplies, and motor control.

"Digital power stands as one of GigaDevice's core strategic markets. MCUs play a pivotal role in advancing the intelligence of digital power systems, enhancing energy efficiency, and ensuring operational security," said Vincent Li, GigaDevice SVP, CTO, and general manager of MCU business unit. "By working with Navitas, we will deeply integrate GigaDevice's advanced MCU with Navitas' leading GaNFast technology to develop competitive solutions for industrial automation and new energy vehicles. This collaboration is not only technological synergy but also a critical step toward greener, more efficient industry development."

"Navitas continues to innovate our GaNFast power IC technology to achieve our mission to 'Electrify Our World'", said Charles Zha, SVP and GM of Navitas Asia-Pacific. "The joint lab with GigaDevice will amplify our complementary strengths in IC design, manufacturing, and ecosystem development and accelerate R&D for next-gen, high-efficiency power solutions, reinforcing our 'Smart + Green' strategic vision. We look forward to delivering faster, energy-saving innovations to global customers and pioneering a new era of collaboration in power electronics."

The tantalising promise of wider bandgaps

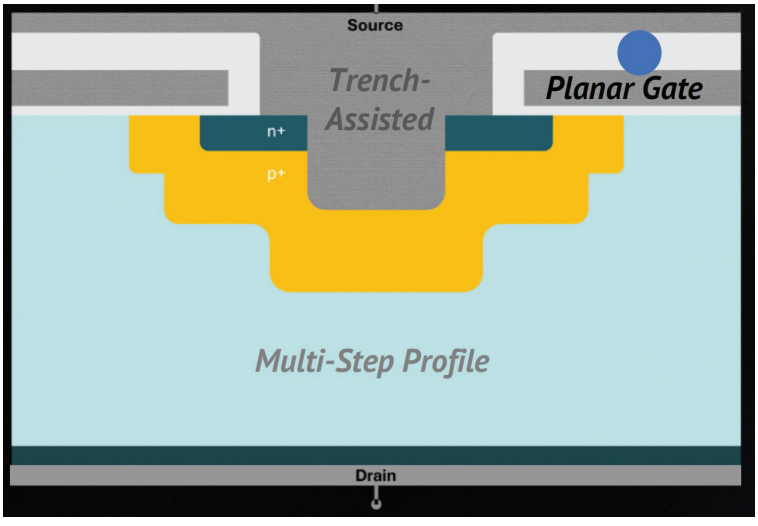
Producing power devices with ever wider bandgaps is far from easy, but realising success slashes on-resistance while boosting blocking capability

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

ONE OF THE primary purposes of CS International is to provide a detailed overview of the latest trends with our industry. To fulfil this goal, the key themes of this conference have evolved over the last 15 years. While progress in GaAs RF electronics played an important role in the first few meetings, this has subsequently taken a back seat, with CS International now focusing on optoelectronics and power electronics, with the latter accounting for the lion's share of the 40 or so presentations.

Today, SiC accounts for the majority of the revenue generated by compound semiconductor power electronics, and sales are forecast to continue to climb, as many of the leading suppliers expand their production capacities, enhance their portfolios, and ship more products for deployment in electric vehicles.

At this year's CS International – held at the Sheraton Hotel, Brussels, from 8-9 April – two leading chipmakers, Navitas and Infineon, detailed the strengths of their approaches in a session entitled *Optimising opportunities for SiC success*.



The Navitas trench-assisted planar MOSFETs

Speaking on behalf of Navitas, Senior Director for Product Management and Marketing for SiC and GaN, Llewellyn Vaughan-Edmunds, discussed the company's novel trench-assisted planar technology for SiC MOSFETs.

Vaughan-Edmunds argued that while the traditional planar architecture offers repeatable high-yield, low-cost manufacture, and has a high level of reliability that benefits from a rugged gate oxide, which ensures a stable threshold voltage, these strengths come at the expense of slow switching and high values for the drain-source on-resistance, both as a function of area and as a change in temperature.

According to Vaughan-Edmunds, the SiC trench MOSFET also has some significant weaknesses. While this design addresses the shortcomings of the traditional SiC MOSFET, this class of transistor suffers from an inconsistent trench etch that hampers yield and leads to higher production costs. What's more, reliability is impaired by failures from the non-uniform gate oxide, and the device is held back by a lower short-circuit capability.

Offering the best of both worlds, says Vaughan-Edmunds, is the trench-assisted planar SiC MOSFET. It is claimed to combine the manufacturing merits of the planar MOSFET with the performance of its trench-based cousin, while excelling in reliability – this design has excellent avalanche capability, a long short-circuit withstand time, and features a rugged gate oxide that ensures a stable threshold voltage.

To benchmark the performance of Navitas' trench-assisted planar MOSFETs, Vaughan-Edmunds presented a plot of the key figure-of-merit – the product of the drain-source on-resistance and area – for currents up to 100 A. The Navitas device delivers the most impressive performance, with the next-best values coming from the planar devices produced by Toshiba and General Electric.

Vaughan-Edmunds also discussed the pros and cons of various architectures from a production perspective. Standard trench MOSFETs have a complex structure, with their production requiring 40 percent more process steps than planar architectures. For planar designs, the trench-assisted architecture that features a novel source contact on the side wall enables a smaller cell pitch and an increased power density.

Some of the advantages of the trench-assisted planar SiC MOSFET over both the traditional planar and standard trench designs are attributed to a multi-step profile that: smooths the electric-field distribution, leading to an increase in long-term reliability; and improves currents spreading, leading to a lower drain-source on-resistance. The latter can be up to 20 percent lower at elevated temperatures, leading to lower conduction losses and a cooler performance.

Another strength of Navitas' trench-assisted planar technology is its reduction in switching losses by up to 15 percent. Thanks to this, the trench-assisted planar SiC MOSFET ensures faster, efficient high-frequency switching, enabling a higher power density, according to Vaughan-Edmunds.

Expanding SiC capacity

Among the chipmakers increasing production capacity, Infineon is attracting much attention for its construction of a colossal facility in Kulim, Malaysia.

Offering an update on this project, the company's Vice President of SiC, Peter Friedrichs, explained to delegates at CS International that Infineon has had a presence in Malaysia since 1974, initially with backend manufacturing, and in 2006 it added 200 mm silicon front-end processing in Kulim. The Kulim facility has undergone several expansions, including in 2022 the addition of Kulim 3.1, supported by more than €2 billion, that's enabled the introduction of SiC and GaN production. Now capacity is now being increased with Kulim 3.2, via a second phase of investment that totals up to €5 billion. Helping to support this venture are design wins worth around € 5 billion, and customer pre-payments of around € 1 billion.

Friedrichs explained that Infineon has designated its Villach facility as its competence centre for wide bandgap materials, with its GaN and SiC power

➤ Alan Dolittle from Georgia Tech gave a presentation entitled *A solution to doping AlN enabling a new era of nitride semiconductors* in the session *Ultra-wide bandgap materials: The ultimate devices*.

electronics technologies developed at this Austrian site. When these technologies enter large-scale production, they are introduced at the Kulm site, a move that is said to enable high-volume production, alongside supply chain stability, quality and efficiency.

According to Friedrichs, the opening of Kulim 3 is ensuring that Infineon is on track to become the industry's most cost-competitive provider of SiC technology. Supporting this endeavour is: the qualification of more than six SiC wafer and boule suppliers; what's claimed to be a superior trench technology that yields 30 percent more chips per wafer than its planar counterpart, along with unmatched reliability and zero field returns; in-house packaging technologies that are said to be best-in-class; and a deep system understanding, drawing on decades of experience.

The allure of Ga_2O_3...

One of the materials for the future that has a significantly wider bandgap than SiC is Ga_2O_3. At this year's CS International, Xiaohang Li from

Ga_2O_3 ICs and devices are promising candidates for operation in a range of extreme environments, such as space, quantum applications and the petrochemical and geothermal industries. By 2035, the number of transistors/diodes in space might exceed 10^{20}, according to a report produced by McKinsey and company and General Electric.

Another recent advance by Doolittle and his team has been the first ever AlN *p-i-n* diodes, which produced a nearly ideal turn-on of around 6 V. This diode is held back by a high series resistance associated with the n-contacts.

KAUST discussed the prospects for this oxide in ICs, after outlining the strengths and weaknesses of this material – its downsides include a low thermal conductivity and poor *p*-type doping, but it has strengths that include a high value for the tunnelling effective mass, excellent radiation hardness, the capability to operate at high temperatures, and the potential to produce low-cost substrates in high volume.

Li argued that Ga_2O_3 ICs and devices are promising candidates for operation in a range of extreme environments, such as space, quantum applications and the petrochemical and geothermal industries. By 2035, the number of transistors/diodes in space might exceed 10^{20}, according to a report cited by Li and produced by McKinsey and company.

The common approach to producing ICs is to use two building blocks – nMOS and pMOS – but forming highly dense, stacked circuits is costly and complex. Ambipolar transistors can overcome this difficulty by trimming costs, reducing the number of logic gates and delay, and decreasing energy consumption by between 30 percent and 70 percent.

Until recently, ambipolar transistors have been limited to narrow bandgap material, but Li has broken down this barrier by pairing Ga_2O_3 with NiO. To ensure good gate control, the team from KAUST employs a gate-all-around architecture. According to benchmarking against state-of-the-art ambipolar transistors, those made by Li and his team have the highest on-off ratio, and a sub-threshold swing that's competitive.

... and AlN

Offering an even higher bandgap than Ga_2O_3 is AlN. Thanks to a bandgap of 6.1 eV, this nitride has a critical electric field five times higher than SiC, and when judged against major performance predictors, it's the best or a close second. However, its major weakness has been its lack of doping.

To overcome this issue, Alan Doolittle and his co-workers from Georgia Tech have recently shown that it's possible to produce *n*-type and *p*-type AlN by metal-modulated epitaxy.

Speaking at this year's CS International, Doolittle revealed that additional motivation for his development of AlN materials and devices has come from theoretical work by Emmanouil Kioupakis' group at the University of Michigan, with calculations revising the peak mobility for this material from around 400 $cm^2\ V^{-1}\ s^{-1}$ to more than double this value. According to Doolittle, if this holds up, AlN will surpass c-BN and diamond as the transistor material with the highest potential. Note that those at Georgia Tech have already measured mobilities of more than 500 $cm^2\ V^{-1}\ s^{-1}$ in AlN.

Another recent advance by Doolittle and his team has been the first ever AlN *p-i-n* diodes, which produced a nearly ideal turn-on of around 6 V. This diode is held back by a high series resistance associated with the *n*-contacts.

While this effort is in its infancy, progress on materials with very wide bandgaps is gathering pace, and will feature at the next CS International, to be held on 21-22 April, 2026.

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Innocent Innoscience?

The latest ruling from the US Patent Office draws jubilation from Innoscience, while EPC claims to have strengthened its key patent. But aside from the lawyers, will there ever be a winner in this long-running dispute?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE GaN IP war raging between EPC and Innoscience is now entering a new phase, following rulings from the US Patent and Trademark Office (USPTO) this past month.

As is often the case in complex matters that involve IP, both sides are talking up the positives, while glossing over the negatives.

Innoscience, on its back foot since the imposition of a ban on importation into the US, is now incredibly upbeat. It is claiming it achieved an 'ultimate victory' in what it describes as EPC's meritless two-year-long patent war, and says that the USPTO ruling shows that EPC's allegations relating to enhancement-mode GaN transistors are 'completely unfounded'.

Unsurprisingly, US firm EPC has a different take on these matters. As well as emphasising a strengthening of its key patent, it is planning to appeal the USPTO's cancellation of its claims.

From four patents to only one

When EPC initiated its legal action against Innoscience back in May 2023, it claimed infringement of four patents, all associated with enhancement-mode GaN HEMT technology. The fabless chipmaker subsequently decided to drop two patents in the case directed to HEMTs with a self-aligned gate having 'ledges'. This left two patents being asserted against Innoscience: US Patent No. 8,350,294 (directed to a FET made with a 'compensated' GaN layer); and US Patent No. 8,404,508 (directed to a multi-step process for fabricating a self-aligned gate E-mode HEMT).

Relating to the '508 patent: EPC went to trial at the International Trade Commission (ITC) in July 2024, with the Administrative Law Judge (ALJ) deciding that the '508 patent was not infringed by Innoscience.

While Innoscience did not enjoy a full victory, having failed to convince the ALJ that the '508 patent was invalid, there is no doubt that it was pleased with the result, according to patent attorney David Radulescu, who is an expert in GaN IP. Radulescu, who is the head of the patent litigation boutique firm Radulescu LLP and has been litigating semiconductor patents in courts throughout the US for three decades, points out that EPC is now suffering from an undeniable loss on the '508 patent: "EPC has no right to an injunction (or any compensation) with its lawyers being unsuccessful in establishing use of its patented fabrication process."

However, EPC may draw some comfort from Innoscience's unsuccessful invalidity challenge before the patent office, where a final determination recently went in its favour. "For Innoscience, it was a complete loss at the USPTO, because all five claims were found to not be invalid," remarks Radulescu.

Relating to the '294 patent: In contrast to the ITC finding of no infringement on the '508 patent, EPC was successful in obtaining an infringement ruling on the '294 patent, which resulted in the ITC issuing an importation ban. The impact of the adverse ruling, however, was blunted when Innoscience claimed to have changed the design of its products to sidestep the ban. "Even so, the redesign had to be painful, particularly when lawyers are involved in device design decisions based on a patent landscape that is so fraught with traps," says Radulescu.

The 'compensation' conundrum

The on-going dispute is now focused on the '294 patent, related to the use of a 'compensated' GaN layer in a FET. Innoscience has widely reported that its devices use *p*-type GaN, but it is not disclosing whether transistor production includes an extra step to expel hydrogen, an approach widely used in the manufacture of GaN LEDs.

During the intentional doping of any semiconductor material with impurities, there will always be some degree of compensation, because no semiconductor is 'perfectly' doped with one type of impurity without other defects/impurities in the crystal lattice. With GaN grown by MOCVD, a number of factors are at play following the addition of magnesium, the common *p*-type dopant. One is that magnesium may be complexed with hydrogen, leading to compensation, because this impurity fails to create a hole. A second factor is that lattice defects and vacancies, of which there are many in GaN grown by MOCVD on lattice-mismatched substrates, could lead to compensation. Lastly, unintentional impurities, such as carbon and oxygen,

could also lead to compensation. Due to all these possibilities, characterising magenesium-doped GaN as 'compensated' or 'not compensated' is complicated to apply when that concept is written into a patent claim, says Radulescu. "It's not so simple as focusing on if hydrogen is present while ignoring other impurities or defects."

This complication hampered the efforts of EPC's lawyers, who needed to demonstrate that the patent is both infringed and not invalid.

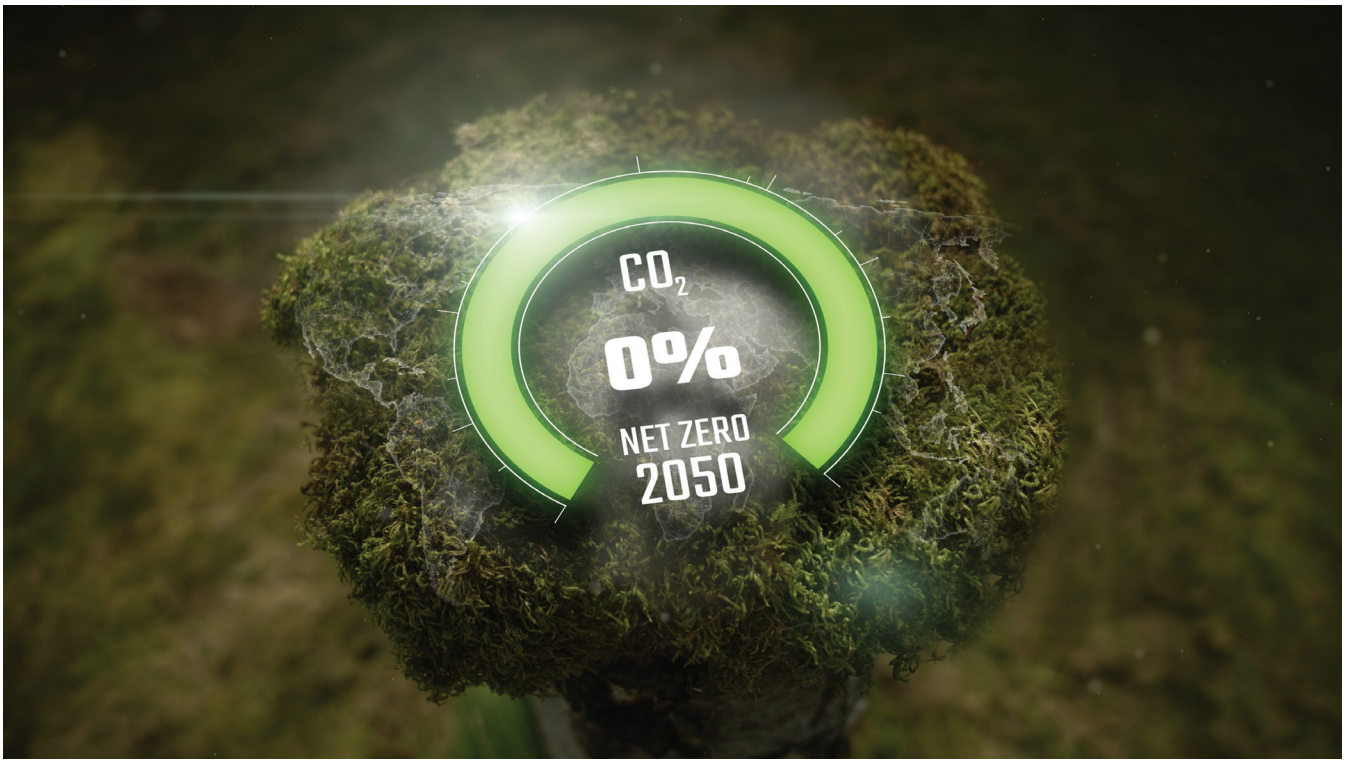
"If you represent the patentee, the job of the lawyers is to walk the line between infringement and invalidity," explains Radulescu. "If you want to argue your claims are broad to show infringement, then you could be stepping over into invalidity territory and you could have the patent invalidated."

Although Innoscience was successful in having the all asserted claims of the '294 patent recently invalidated, EPC was successful in having two new 'substitute' claims added to its patent that escaped Innoscience's invalidity challenge. Both claims are directed to GaN-based enhancement-mode transistors with more specificity to distinguish from the prior art. In particular, these new claims require that 'no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate voltage' and refer to a 'semi-insulating III-N layer', which includes a 'compensated GaN layer containing acceptor-type dopant atoms passivated with hydrogen'. These claims continue to not only refer to the hotly contested phrase 'compensated', but add a further complication by referring to a 'semi-insulating' layer (without any quantification of how insulating/conducting). "With all this added language, the claim scope is rich with opportunity to allow a lawyer with GaN experience to argue on either side of the dispute," Radulescu believes.

What happens next?

How both parties proceed from here will depend on a number of factors, some unknown. For EPC, if it wants to continue its battle with Innoscience, it will have to focus on appeals, attempting to overturn unfavourable decisions – which is always an uphill battle. In addition, it could file a new infringement action using other patents or the '294 patent with the new claims that have been litigation-hardened. Meanwhile, Innoscience may decide to direct its efforts at removing the import ban, given that the infringed '294 patent claims were recently ruled as invalid. So far, there has been silence on this matter, but it's possible private negotiations are underway.

What the future holds is anyone's guess. Even those with tremendous expertise in these matters, such as Radulescu, can only speculate – and they will only do so after reeling off a string of caveats. Radulescu surmises that among a number of possible scenarios, one that would not surprise him is a sudden truce in this battle between EPC and Innoscience, with cross-licencing following. And if that were to happen, he would expect all the details to be confidential, with both companies just issuing a press release stating that they have cross-licensed their technology. Motivation for such a move would include avoiding paying more in legal fees, which may already total $15-20 million for each side.



Power semiconductors for carbon neutrality

Advances in semiconductor and power electronics technologies, led by increasing deployment of wide-bandgap power devices, are essential for reducing greenhouse gas emissions and developing a carbon-neutral energy system by 2050

BY YUHAO ZHANG FROM THE UNIVERSITY OF HONG KONG

THE LAST decade has witnessed an increase in the adoption of wide-bandgap power devices, led by those based on GaN and SiC. Both these materials have enabled improvements to the performance of power electronics systems in numerous applications. But beyond performance, what impacts are these advanced semiconductors having? Are they set to play a major role in driving down greenhouse gas emissions? And are they critical to reaching carbon neutrality?

Recently, I have been digging into these important questions, working with departmental colleagues at the University of Hong Kong, and collaborators from Virginia Tech and the University of Cambridge. Together, we published our findings earlier this year in *Nature Reviews Electrical Engineering*. Our paper traverses the full material-device-circuit-application spectrum, to scrutinise the combined impacts of wide-bandgap semiconductors and power electronics on greenhouse gas emissions. This thorough investigation has led us to conclude that wide-bandgap power semiconductors are critical enablers to carbon neutrality.

Since 2015, 195 countries have joined the Paris Agreement, signing up to mitigate their greenhouse gas emissions and strive towards the goal of carbon neutrality by 2050. Currently, energy generation and energy use accounts for around three-quarters of greenhouse gas emissions, mainly associated with four sectors: electricity generation, transportation, industrial processes, and the cooling and heating of buildings. Power electronics are utilised ubiquitously in all these sectors for electrical energy conversion, such as stepping up and down the current and voltage, as well as converting between AC and DC forms.

Crucial to determining the efficiency, power density and form factor of power electronics systems are the power semiconductors, in conjunction with the circuit topology and control. While it is well known that the adoption of GaN and SiC devices can bring significant performance advances, their environmental impact on carbon emissions is less researched. Filling the gap between semiconductor technology and carbon footprint demands a multi-disciplinary approach, covering the full spectrum of material, device, circuit and application.

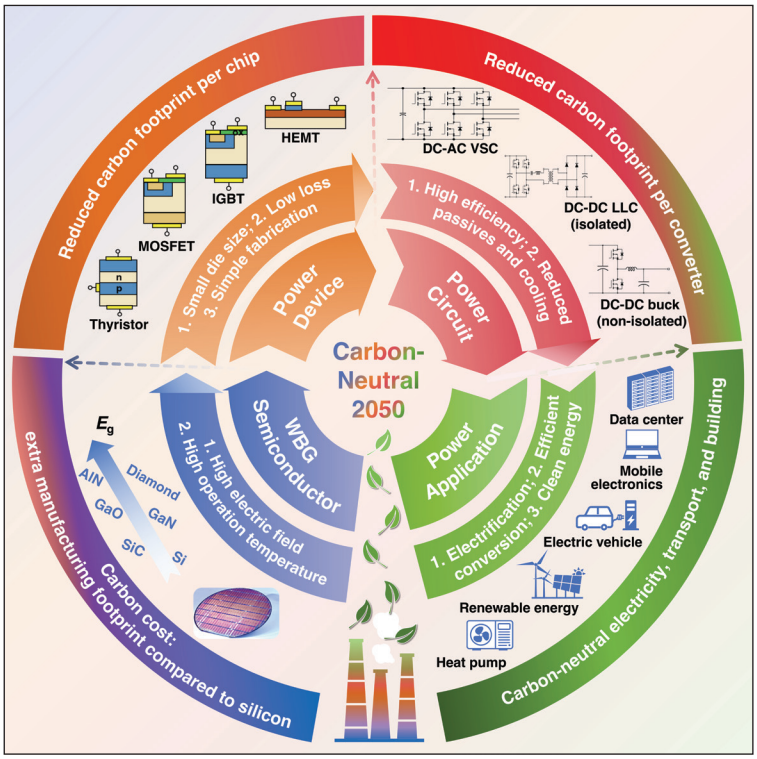
The uptake of GaN and SiC power devices cuts carbon footprints on many fronts. At the device and circuit level, these wide bandgap diodes and transistors can potentially have smaller carbon footprints than their silicon cousins, due to their smaller die size and superior performance. These strengths enable: a lower per-chip carbon footprint for the same energy and chemicals used in manufacturing a wafer; reduced energy loss, associated with an increased converter efficiency; and dematerialisation, that is, a reduction in the volume of materials used for passive and cooling components.

At the application level, wide bandgap semiconductors cut carbon emissions on three key fronts. First, they reduce energy loss in power conversion and trim the energy consumed by cooling systems; for example, these devices and co-optimised circuits increase the efficiency of electrical conversion from grid edge to the processors in data centres from below 80 percent to over 90 percent. Second, power devices and circuits aid the use of renewable energy in electricity generation, for example, through the use of solar photovoltaics, wind power generation, electric vehicles and heat pumps. Third, power electronics with a fast dynamic response, high switching frequencies and a high-power density promotes the electrification of transportation and buildings, for example, by boosting an electric vehicle's driving range, its charging time and its energy efficiency.

We have analysed and quantified the potential reduction of carbon emission across four pivotal sectors – renewable energy systems, electric vehicles, data centres, and heat pumps – from the perspectives of electrification and energy conversion efficiency. This led to a number of interesting findings, such as the replacing of 80 percent of fossil-fuel electricity generation with GaN/SiC-based photovoltaic systems could lead to an annual reduction in US greenhouse gas emissions of at least 1,236 million tonnes – that's equivalent to the annual emissions of 245 million gasoline passenger vehicles.

According to our study, substantial savings in US greenhouse gas emissions can also be realised with other significant initiatives, such as a reduction by 390 million tonnes by replacing 80 percent of gasoline cars with GaN/SiC-based electric vehicles. Meanwhile, in data centres, if silicon devices were replaced with those made from GaN and SiC, this could reduce US greenhouse gas emissions by at least 1.7 million tonnes per year; and if US homes currently heated by natural gas switched to heat pumps powered by photovoltaic systems, this could slash greenhouse gas emissions by around 260 million tonnes per year.

To ensure rigour in our findings, we considered the extra carbon emissions associated with GaN and SiC production, compared with those for legacy silicon manufacturing. Despite the smaller size of wide bandgap devices, the raw materials, chemicals and energy used in their production could be very different from those for silicon.



➤ Figure 1. The role of wide-bandgap power semiconductors in achieving carbon neutrality.

For this part of our analysis, we surveyed the normalised carbon emission by corporate revenue for GaN, SiC and silicon manufacturing, based on data disclosed from third-party-verified sustainability reports from major power semiconductor companies. From the survey, we estimated the extra carbon footprint for GaN/SiC manufacturing. We found this to be marginally small compared with the system-level carbon saving.

We hope that our recent paper, offering the first quantitatively analysis of the impact that wide-bandgap power semiconductors could have in realising carbon neutrality, will become a useful reference for researchers, engineers, and policymakers. Despite their potential to deliver significant change, the consequences of increasing the deployment of SiC and GaN devices have not been considered in detail, such as their impact on sustainability. But what we do know is that further innovation across materials, devices, circuits and systems, as well as a shift to designing power electronics based on the principles of reuse, remanufacturing and recycling, is essential to fulfil the potential of wide-bandgap power electronics for carbon neutrality.

FURTHER READING / REFERENCE

➤ Y. Zhang *et al*. "Wide-bandgap semiconductors and power electronics as pathways to carbon neutrality" nature reviews electrical engineering **2** 155 (2025)

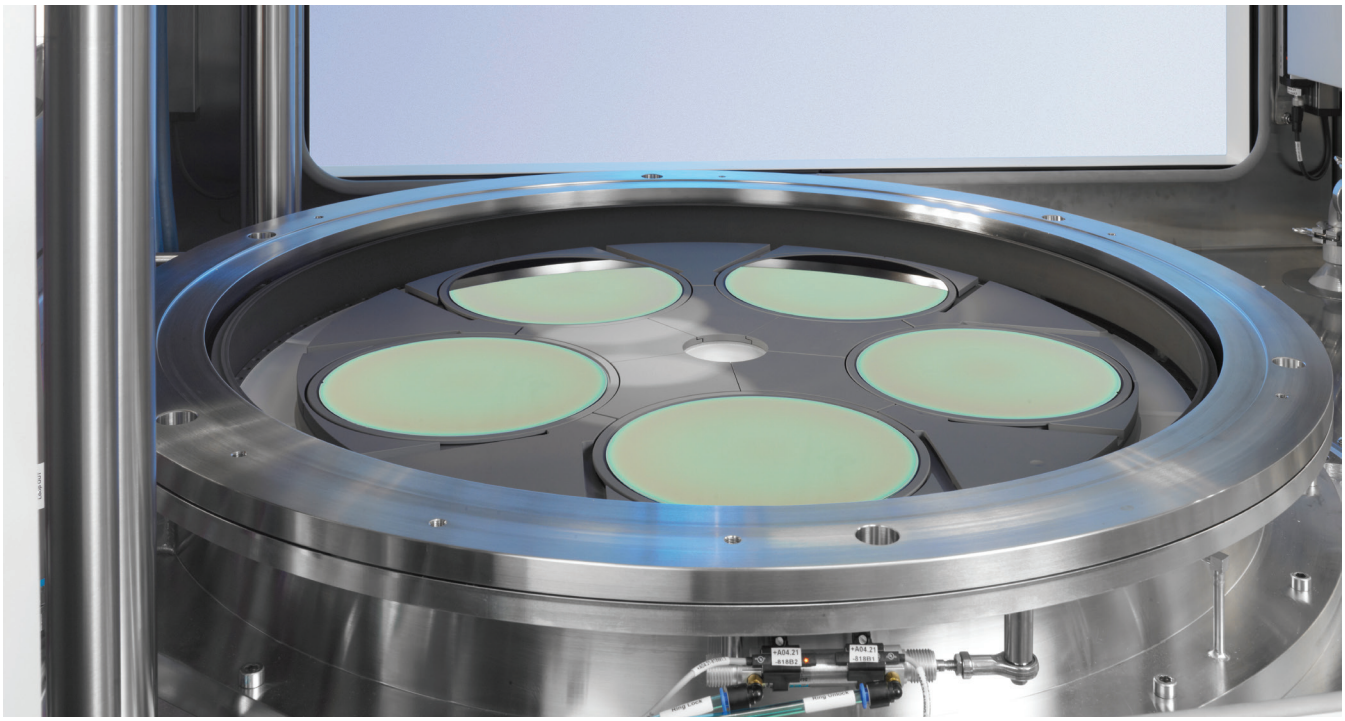


Photo: Aixtron

Improving GaN with a dash of oxygen

Depositing a partial monolayer of oxygen between a silicon substrate and GaN device layers trims defect density and improves material quality

BY ROBERT MEARS FROM ATOMERA

THROUGHOUT the semiconductor industry, those working in R&D look to new materials to push the boundaries of technology, with a focus on enhancing performance and reducing power consumption. Progress on these fronts is imperative for developing the next generation of mobile devices, consumer electronics and data centres – all require devices that draw less power without compromising performance. These objectives may be meet by advancing devices made from silicon, but compound semiconductors such as GaN are beginning to play a role, particularly in enabling more-efficient power delivery.

At Atomera, a semiconductor materials and technology licensing company based in California, we are supporting efforts to develop efficient, high-performance devices produced with a number of different materials with our novel epitaxial technology.

Initially, we developed a unique epitaxially grown silicon material technology, which we refer to as Mears Silicon Technology, or simply MST. We describe this epitaxial technology as 'silicon with a twist.' It's variant on conventional silicon epitaxy, with the novelty being the interruption of growth at intervals, during which time there is the deposition of a partial monolayer of oxygen, or sometimes other elements. Crucially, the conditions for this deposition ensure that there are sufficient silicon atoms available on the surface to allow high-quality silicon epitaxy to continue.

Over the years, we have discovered that MST can be used to define a diffusion-blocking layer, enabling abrupt junctions and the shielding implants from point defects, which are the main source of dopant diffusion. By creating a thin undoped region that is maintained throughout the silicon manufacturing process, our growth technology enables the engineering of a variety of desirable transistor characteristics, including enhanced carrier mobility, reduced threshold voltage mismatch, and improved short-channel effects. It's also possible to improve junctions and contacts with MST. What's more, further benefits may be realised in some forms of scaled silicon devices, including reduced surface roughness scattering and improved wafer-level reliability metrics, such as bias temperature instability and time-dependent dielectric breakdown.

Recently, we have expanded the application of MST to a wider range of devices. It's now applied to a variety of silicon technologies, from CMOS and

DRAM to power and RF devices, and it's also being used to improve the process for growing GaN on silicon.

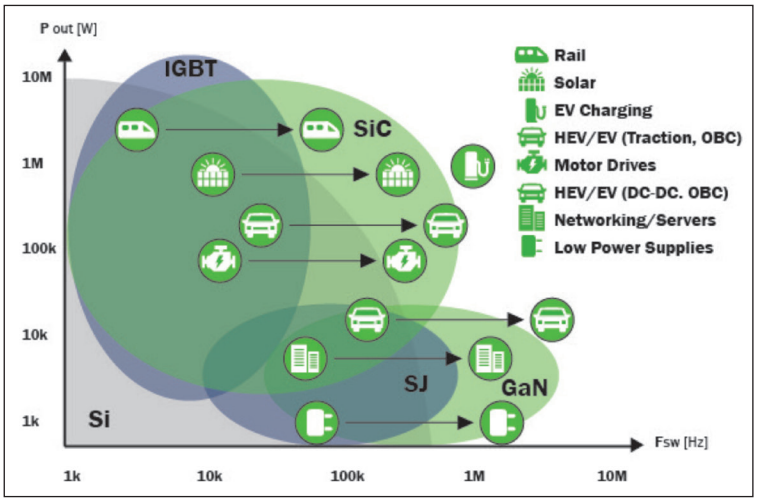
We have been working on silicon power devices since 2016. Over that timeframe we have proven that our technology enables unique device-doping profiles. Key merits of the MST layer are the suppression of diffusion below the film, as well as localising doping in the vicinity of the film to enhance conduction.

Initially, we applied our MST technology to 5 V power devices, with our novel MST Smart Profile design used to produce an asymmetric device with higher localised shallow *p*-body doping. Thanks to this doping profile, these power devices combine an expanded safe-operating area with industry-leading values for the specific on-resistance as a function of breakdown voltage for a given silicon process node.

Over time we have extended the reach of our technology to designs covering the 7-48 V range. This work has involved additional doping profile engineering of the drift region. Such success has helped us to showcase the capability of our MST technology, which we licensed to STMicroelectronics in 2024 for its Smart Power products.

From silicon to GaN

GaN technology, a newcomer compared with silicon, has matured considerably since its introduction into power devices. While yet to receive as much attention as SiC for high-voltage, high-power applications in the automotive and industrial sectors, GaN has inherent advantages over both silicon and SiC in terms of its high mobility – and hence its higher frequency. In addition, compared with silicon, it offers a markedly better on-resistance as a function of blocking voltage. Due to its superior efficiency at high frequencies, GaN is well-suited to deployment in DC-DC converters and various lower-power converters.

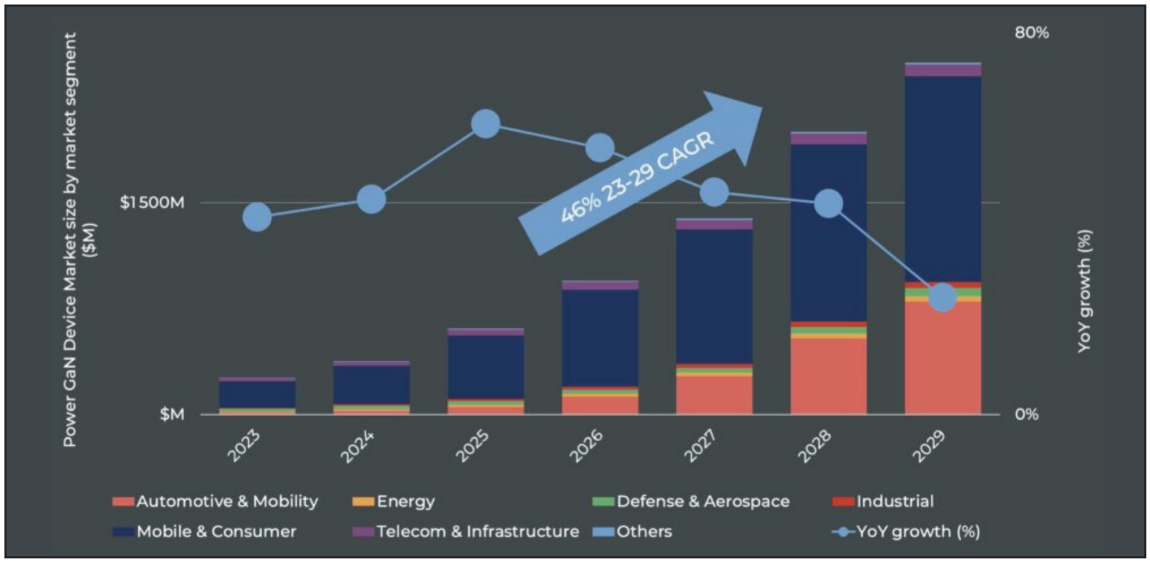


➤ Figure 1. Power versus switching frequency by device technology option and market segment.

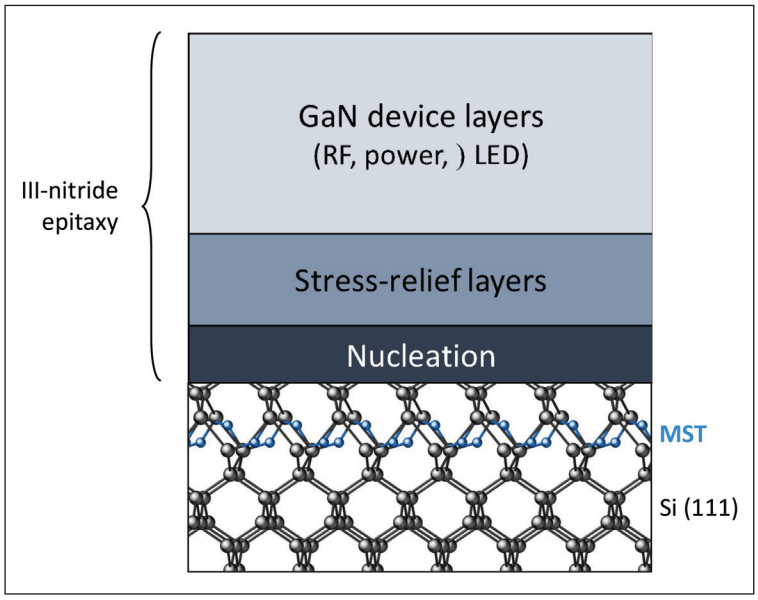
Today, the majority of sales of GaN devices are associated with fast-charging for consumer electronics. However, GaN could serve in many more applications, as these devices are capable of operating in units with power capabilities of up to tens of kilowatts, and frequencies from tens of kilohertz to tens of megahertz.

Helping to expand the opportunities for this wide bandgap semiconductor will be advances in GaN material growth quality, alongside a reduction in cost that could come from the introduction of 300 mm wafers. It's anticipated that consumer electronics products, such as laptop chargers and mobile phone fast chargers, will continue to drive the majority of the demand for GaN, while increases in revenue will be driven by the automotive segment, with GaN a strong candidate for onboard chargers and ADAS systems.

Note, though, that the automotive market is not the only one that promises growth for GaN. Artificial intelligence and machine learning will benefit from GaN, as the GPU and memory processors in this high-performance compute application require high power.



➤ Figure 2. Growth of GaN power device market by market segment. Source: *Power SiC & GaN Compound Semiconductor Market Monitor, Q1, 2024*, Yole Intelligence.



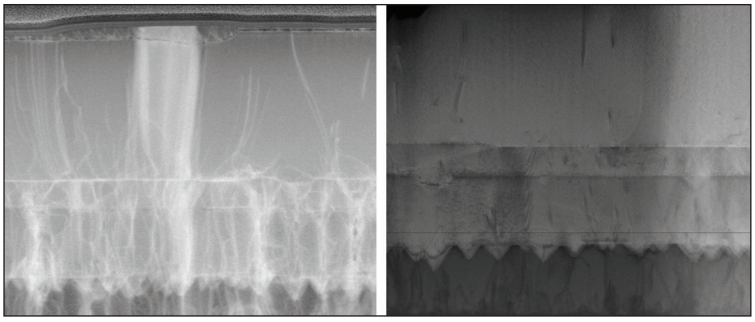
➤ Figure 3. GaN on MST on silicon (111).

When market analyst Yole Group considered all the opportunities for GaN, they forecast that annual revenue will total more than $2 billion by the end of this decade (see Figure 2).

Unlocking the potential of GaN

Our current licensing of MST is directed towards improving the electrical characteristics of a wide application space of silicon products, from power and RF through memory to the most-advanced logic nanosheet applications. So, what can MST offer GaN? In short, a more compliant lattice for the growth of lower-defectivity GaN-on-silicon (see Figure 3). In this sense, MST offers chemical and mechanical advantages, as opposed to the previously characterised electrical benefits.

In our early days, we devoted much effort to the fundamental *ab initio* modelling of the inserted partial monolayers of oxygen in the silicon lattice, as well as detailed experimental characterisation. Back then we often considered a ball-and-stick model, with a silicon-silicon bond bending to enable a stable Si-O-Si bond that retained the silicon lattice. As oxygen is introduced, the stability of the overall structure increases via the proximity of adjacent oxygen. We discovered that over a characterised temperature range, stability improves with oxygen density, according to a power law with a factor of roughly 2.5.



➤ Figure 4. Defect reduction using MST. Same epi recipe and cross-sectional transmission electron microscopy imaging conditions for both samples.

Another insight from this work is that due to the electronegativity of oxygen, charge transfer occurs from adjacent silicon atoms. Due to this, next-nearest silicon neighbours have a smaller opposite charge, and the charge spatial 'wave' dissipates over about four atomic spacings. Related to this is a local distortion of the lattice to accommodate oxygen, again with dissipation over about four atomic spacings.

According to our theoretical simulations, this modified silicon lattice is better at accommodating lattice mismatch. This observation provided our starting point for virtual substrate work and, in particular, our development of GaN-on-silicon technology.

Growth on silicon

The conventional growth of GaN-on-silicon begins by taking (111) orientated silicon wafers with nominally zero-degree off-cut and loading them into a reactor for epitaxial growth. In contrast, silicon epitaxy for electronic applications typically involves (100) orientated wafers with a 4° offcut.

Removing the off-cut presented us with a challenge. Based on conventional epi wisdom, zero-degree growth is too slow and can be defective. Addressing these issues has taken some time, but we have been able to overcome these challenges and apply our MST technology to silicon (111) substrates.

Assisting us in this endeavour, in late 2023 we started to engage with Wayne Johnson, a veteran in GaN technology. Johnson had previously worked at Nitronix, a pioneer in the GaN space, before working for Kopin and then IQE. Through Johnson, we were introduced to another GaN pioneer, the academic Edwin Piner of Texas State University. These introductions led us to sponsor a programme at Texas State University to grow baseline GaN HEMT material.

The first phase of this project focused on the physical characterisation of GaN grown on MST substrates. For this investigation, Piner's team compared results with their stable process-of-record GaN baseline stack, consisting of AlN buffer layers followed by GaN of around 2 μm thickness, a heterostructure suitable for RF applications. For the first phase dataset, the process-of-record recipe was kept constant, and various MST structures were grown to start to explore how our technology interacts with the baseline. To everyone's delight, the first set of wafers showed very promising results.

This promise is clear in side-by-side transmission electron microscopy images, comparing the process-of-record GaN-on-silicon stack with the same stack on the MST (111) wafers. Images at the microscopic level reveal that the MST wafers have fewer defects, both in the AlN buffer and in the top GaN layer.

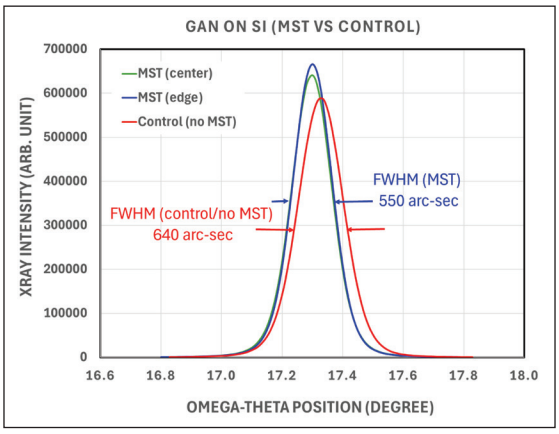
While the transmission electron microscopy images are encouraging, they have the potential to mislead, because they only consider a very small region. To cater for this concern, we turned to X-ray diffraction to examine crystal quality, considering the width of the diffracted beam.

The benchmark for this is the X-ray diffraction spectra from the process-of-record GaN-on-silicon stack produced by Piner and his co-workers that's been characterised over a number of years. Diffraction peaks from this material, considering the (002) and (114) diffraction directions, have typical values for the full-width at half-maximum of 650 +/-30 arcsec. Such values are considered to be good for industry-grade 2 μm GaN.

X-ray diffraction spectra for the MST design has confirmed the promise provided by transmission electron microscopy. X-ray diffraction peaks for the (002) and (114) directions are narrower (see Figure 5), with different trends observed in the composition and spacing of the MST layers.

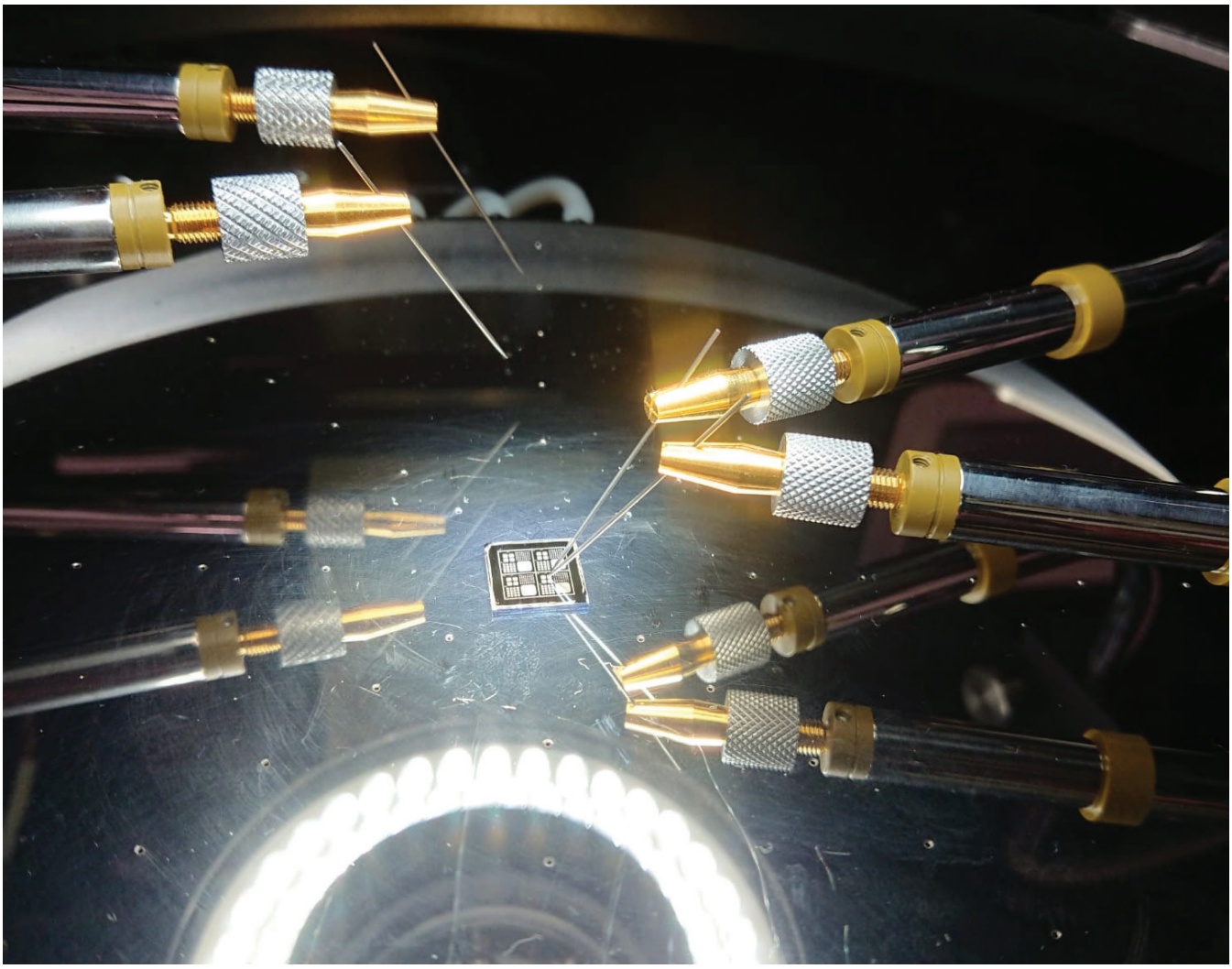
Collaborating with Sandia Labs

Recently, we announced a collaboration with Sandia National Labs – a Department of Energy, Office of Science, Nanoscale Science Research Center – with this partner performing electrical tests on our MST-supplied silicon (111) substrates, with GaN epilayers grown at Texas State University. The purpose of this project is to validate MST's mechanical and electrical benefits for GaN-on-silicon epiwafers. This effort will build upon improvements already observed at the materials level in GaN/MST-on-silicon wafers.



➤ Figure 5. Example of X-ray diffraction (XRD) full-width at half-maximum (FWHM) improvement with MST.

While GaN is helping to usher in a new era of electronics, challenges persist. However, many of them can be addressed by leveraging our innovations in material science, which open the door to even higher efficiencies, greater power handling, and enhanced stability. Such gains will help to enable electrification in many fields. By providing a cost-effective alternative to SiC, our MST technology is expanding the limits of GaN chip performance.



Exposing SiC defects

Conductance and optical excitation measurements offer unique insights into interfacial defects in SiC devices

BY PIYUSH KUMAR, MANUEL BELANCHE AND ULRIKE GROSSNER FROM ETH ZURICH

SILICON CARBIDE is transforming the future of semiconductor devices. Strengths of this wide bandgap matertial include low conduction and switching losses, a high blocking-voltage capability, fast switching, and high operating temperatures. It's a set of attractive properties that make SiC a compelling candidate for high-power, high-temperature electronics, and radiation-hard applications.

One crucial driver behind the development of SiC power electronics is its similarity to mature silicon transistors, in terms of the manufacturing processes and the device structure – both technologies employ the native oxide SiO_2. Thanks to extensive understanding of this dielectric, SiC enjoys a significant advantage over other wide bandgap semiconductors, with its development drawing on existing fabrication processes established for producing silicon devices.

The devil in the defects

Unfortunately, unlocking the promise of SiC demands addressing a number of key challenges. A major one is an imperfect interface between SiC and SiO_2 that prevents SiC technology from reaching its full potential. Growth of this dielectric, a thin layer of SiO_2, involves thermal oxidation of SiC at high temperatures. During this step many unwanted electrically active defects, commonly referred to as traps, form at the SiO_2-SiC interface. These defects drag down channel mobility and capture charges, which cause threshold voltage instabilities, a major concern in the development of SiC MOSFETs.

To address these issues, it is essential to understand the nature of these electrically active defects. Knowing them is the first step to avoiding them.

At the Advanced Power Semiconductor Laboratory, located at ETH Zurich, we are making many important contributions to this objective with conductance and optical excitation measurement techniques. These novel approaches offer new insight into the electrically active defects at the SiO_2–SiC interface. Our internally developed optical excitation method uncovers hidden defects near the valence-band edge that tend to be invisible to conventional methods; and our conductance measurements, an improved version of traditional CV and conductance techniques, allow us to study capture dynamics of slow and fast traps in SiC.

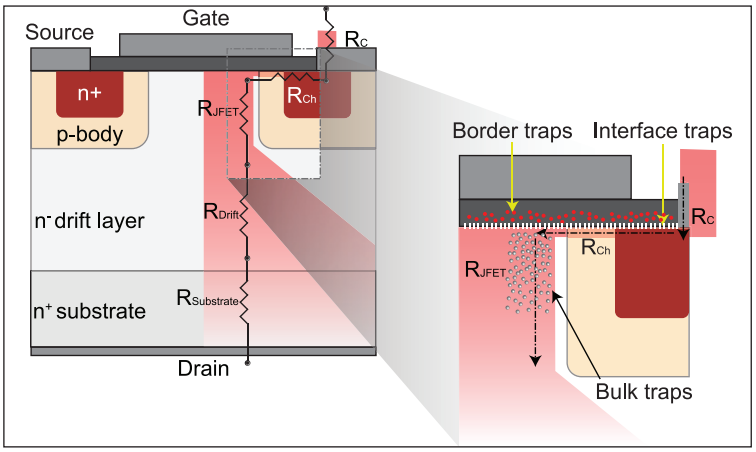
This pair of innovative methods is crucial for improving the performance and reliability of SiC devices. By probing SiO_2–SiC electrically active defects in a manner that's not possible with conventional methods, as well as revealing the concentration of these defects, we are able to uncover their energetic and spatial positions and their capture cross sections. These have the potential to improve SiC's low channel mobility and threshold-voltage instabilities, because these findings expose the source, a key first step to device improvement.

Conventional methods are not enough

Capacitance-voltage (CV) measurements are an established methodology for investigating the interface between the gate oxide and the underlying semiconductor. One of the merits of this approach is its apparent simplicity, in both execution and interpretation. By comparing a low-frequency or quasi-static capacitance curve with a theoretical or high-frequency CV curve, one can extract the density of interface traps. This methodology is known as the C-ψ method.

Although widely used, low capacitance measurements are prone to inaccuracies. They are quite sensitive to systematic errors, coming not only from the influence of the set-up parameters, but also from the evaluation of the density of interface traps. These inaccuracies, which are difficult to detect, have a strong influence on the final results of the density of traps.

A number of investigations involving extracting the density of interface traps from CV measurements have identified a critical source of errors: the relation between the applied DC bias and the surface potential on the semiconductor. The latter is calculated as a function of the quasi-static capacitance, the oxide capacitance and an integration constant. It is a constant determined from the extrapolation of a linear fit of the surface potential, as a function of the reciprocal of the square of the depletion capacitance (C_{dep}), which is obtained from the high-frequency CV measurement.



➤ Figure 1. An illustration of a vertical power MOSFET. The inset shows the region where the current transport occurs from the source to the drain. Also shown is the location of the border, the interface, and the bulk traps generated as a consequence of thermal oxidation.

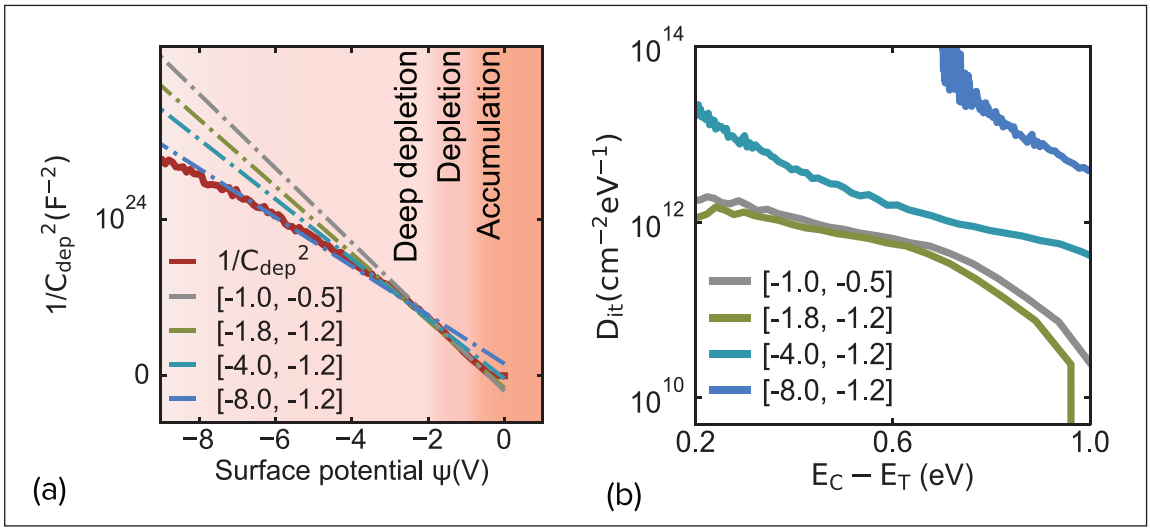
As there are small variations in the integration constant for different fitting ranges, it is tempting to overlook this matter. However, to do so would be a significant oversight, as these small variations in the integration constant compute into a non-negligible shift in the profile of the density of interface traps within the bandgap.

Illustrating this issue is an example of our high-frequency CV measurement, shown in Figure 2 (a). Here, measured values are shown by the red solid curve, and dashed lines correspond to different fitting curves, each using a slightly different range of surface potential. Note that the integration constant, obtained at the intersection of the fitting curve with the *x*-axis, ranges from 0.1 V to 0.9 V. Variations in the integration constant lead to a significant shift in the curve for the density of interface traps, and could potentially result in a wrong estimation by several orders of magnitude (see Figure 2 (b)). The root cause of this uncertainty is the non-linear behaviour of C_{dep}^{-2}, observed in the SiC metal-oxide-semiconductor capacitor measurements that differs across samples. We tentatively relate the small curvature to inhomogeneity of the dopant depth profile, but this hypothesis requires further investigation.

The numerous sources of uncertainty inherent in this methodology, and how to avoid them, is a long-winded discussion that highlights the necessity for exploring alternative techniques. This has driven us to develop and implement more robust methods, such as conductance measurements and above-bandgap optical excitation. Read on to discover how these advanced techniques promise to provide a clearer, more accurate understanding of interface and border traps.

Conductance measurements

To account for inaccuracies associated with extracting defect-related information from conventional CV measurements, we have



➤ Figure 2. Impact of the linear fitting range on the D_{it} analysis of the SiC/SiO_2 interface. (a) Linear fitting of $1/C_{dep}^2$ (red) for four different voltage ranges and their extrapolation to obtain the integration constant K. (b) Impact of the small variations in K on the D_{it} extraction.

started to investigate interface and border traps with conductance measurements, using a wide frequency range that spans 1 Hz to 10 MHz.

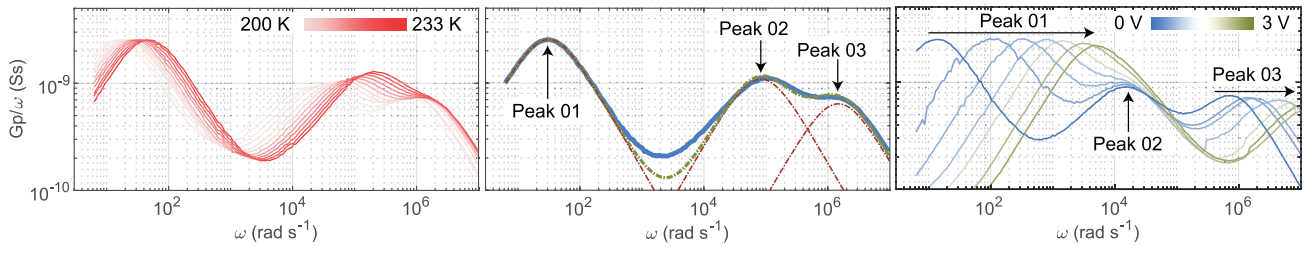
During these measurements, we vary the frequency of the AC signal, the sample's temperature and the applied DC bias. By tuning these three parameters, we can study the capture dynamics of slow and fast traps in just one measurement. Reducing the minimum measurement frequency to 1 Hz – that's far, far lower than 1 kHz, often quoted in the academic literature – ensures that we capture very slow traps, which have a capture/emission process that is dominated by tunnelling from the border trap to the conduction band edge of SiC.

Usually, this study is not possible with the conventional high-low CV measurement. There is a price to pay, however, with our novel approach: the extra information extracted from the conductance measurements tends to require longer measurement times.

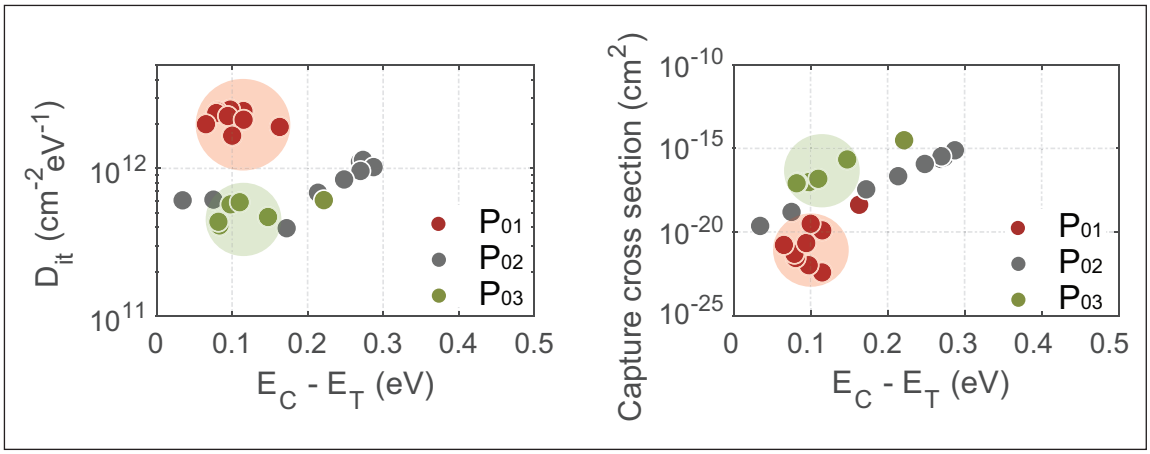
The samples used for the measurements shown in Figure 3 were produced using thermal oxidation and post-oxidation annealing in a NO environment. This investigation involved recording the conductance as a function of angular frequency for a sample under a fixed DC bias of 0 V at temperatures ranging from 200 K to 233 K (see Figure 3 (a)). The plots uncover three temperature-dependent peaks (see Figure 3 (b)): one at a low frequency, in the range of a few hertz (Peak 01); another at a relatively high frequency, on the order of 10 kHz (Peak 02): and the third at high frequency of around 100 kHz (Peak 03). It worth noting that Peak 01 and Peak 03 show a bias dependence, while the Peak 02 remains almost fixed in frequency for changing DC bias (see Figure 3 (c)).

By varying the temperature during the measurements, we are able to evaluate the parameters associated with these defects. This has enabled us to determine the density of interface traps, the activation energy, and the capture cross-section (see Figure 4). Peaks 01 and 03 result in two clusters with a very small spread in activation energy and capture cross-section, whereas the P02 defects have a spread in both parameters. The first cluster results in defect levels with an activation energy of no more than 0.1 eV with respect to the conduction band edge, and a concentration in the range of 1×10^{12} cm^{-2} eV^{-1}.

We have determined that this cluster of defects, associated with Peak 01, have a capture cross-section no more than 1×10^{-20} cm^2 – that's several orders of magnitude smaller than that typically expected for bulk defects in SiC. Also featuring in the plots is a second cluster of peak P03, with a very similar activation energy to P01, but a much larger capture cross-section.



➤ Figure 3. The conductance spectrum of the thermally oxidised and NO annealed sample is shown. The spectrum comprises of three peaks and show a temperature as well as a bias dependence.



➤ Figure 4. The concentration of the three defect groups extracted from the conductance measurements and their capture cross section as a function of energy.

According to reports in scientific literature, some defects observed in the conductance measurements would require electrons to tunnel from the conduction band into the oxide, resulting in a reduced effective capture cross-section – it is reduced by a tunnelling probability. This probability ranges from 1 x 10^{-3} to 1 x 10^{-6}, assuming a potential barrier of 2.7 eV, a tunnelling effective mass that is 0.42 times the mass of the electron, and border traps located between 1 nm and 2.5 nm from the interface. As shown in Figure 4, the P01 and P03 defects have similar values for the activation energy, but the carrier cross-section for P01 is 10^{-3} to 10^{-5} times smaller than that for the P03 defect. Assuming that the defects associated with P01 are located around 2.0 nm away from the interface, the resulting carrier cross-section for P01 would be on the same order of magnitude as for the P03 defects.

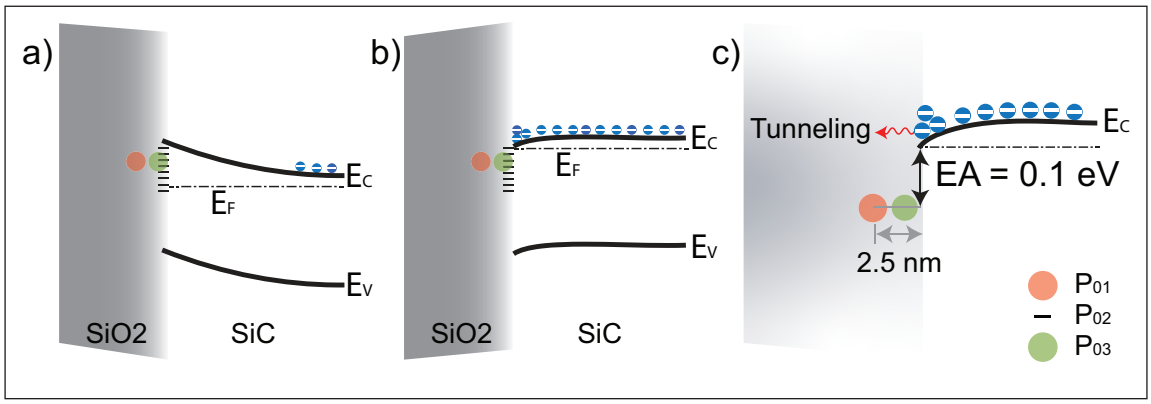
In short, the P01 and P03 defects exhibit similar intrinsic properties, but due to a spatial separation of around 2.0 nm in the oxide, P01 behaves like a slow trap, while P03 has a relatively fast response, in the range of a few microseconds. The defects associated with P02 show a spread in both the activation energy and the carrier cross-section, attributed to interface defects. We summarise the position of the three defect species in Figure 5.

One of the strengths of conductance measurements is that they provide a deeper understanding of electrically active defects near the conduction band edge. However, in order to obtain a picture that is both more detailed and complete, there's also a need to closely examine the valence band edge. That's where above bandgap optical excitation comes into play.

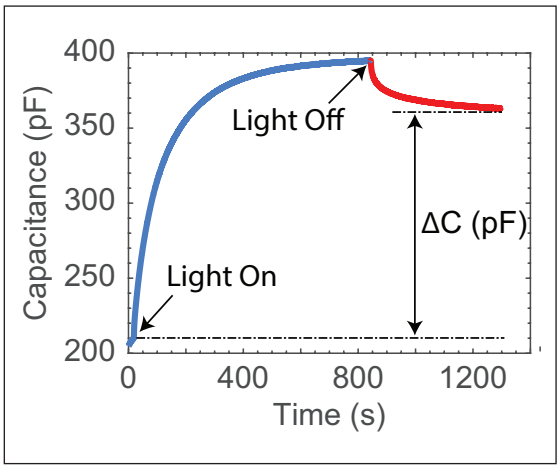
Above bandgap optical excitation

By turning to optical excitation with energy higher than the bandgap, our newly developed technique probes charge capture and emission from the border trap near the valence band edge. While the defects close to the conduction band edge in an *n*-type sample can be studied with conductance measurements, those close to the valence band edge remain hidden, due to the absence of minority carriers (holes) in SiC metal-oxide-semiconductor capacitors. But we can lift this veil with above-bandgap optical excitation, a technique that generates electron-hole pairs and allows us to study defects close to the valence band edge.

Under optical illumination, using a 365 nm ultraviolet LED that's emitting above the bandgap of 4H SiC, we observe a rise in the small-signal capacitance of the metal-oxide-semiconductor capacitors. Depending on the sample, the DC bias conditions, and the optical power, rise time ranges from a few seconds to a few hundred seconds. At the start of this experiment, we observe a fast rise in capacitance. But as time progresses, the process slows down – and eventually almost no rise is seen, occurring at a time when effective saturation begins.



➤ Figure 5. The evaluated location of the three defect species extracted using conductance measurements.



➤ Figure 6. Change in capacitance of a MOS-cap under optical excitation with above bandgap light.

At this point, we turn off the UV LED. This leads to a sudden drop in capacitance, followed by a slow decay. We view this measurement as complete when the capacitance stops changing for at least 1 minute (see Figure 6).

We attribute the persistent increase in capacitance at the end of optical excitation to the capture of holes at border traps near the valence-band edge. The increase in capacitance is directly proportional to the concentration of captured charges. Due to this phenomena, optical excitation on *n*-type metal-oxide-semiconductor capacitors allows us to study the concentration of border traps located near the valence-band edge, and ultimately enables us to obtain a more comprehensive understanding of charge capture and emission processes, as well as the intricate dynamics at play within these semiconductor devices.

Our insights must be viewed against a backdrop of advances in SiC device technology, particularly for high-power and high-temperature applications. While there are challenges with electrically active defects at the SiO_2–SiC interface, much insight into their nature can be uncovered with our innovative techniques, such as conductance measurements and above bandgap optical excitation.

By understanding the capture dynamics of slow and fast traps near the conduction-band edge and exploring defects near the valence-band edge, we are helping to build a foundation for improving the performance and reliability of SiC devices. Our insights, enhancing our understanding of SiC, will lead to the introduction of more efficient and robust semiconductor technologies.

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As-grown 4-inch and 6-inch InP-on-GaAs engineered substrates produced at the Fraunhofer ISE institute.

Cutting the cost of InP-based devices

Engineered InP-on-GaAs substrates with diameters up to 200 mm provide a rigid, low-cost platform that can be rapidly ramped to production volumes

BY FRANK DIMROTH, CARMINE PELLEGRINO, JENS OHLMANN AND DAVID LACKNER FROM FRAUNHOFER ISE AND JÖRG SCHWAR FROM III/V-RECLAIM

OUR INDUSTRY is driven by constant demand for materials offering superior performance, scalability, and cost-effectiveness. Devices utilising III-V compounds on InP boast unique properties, such as the exceptionally high electron mobility of InGaAs and the ability to absorb and emit infrared light up to 1500 nm and beyond. Thanks to these features, devices based on InP and its related alloys are ideal for a number of high-end applications, including infrared cameras, photodetectors, and high-speed transistors. However, although InP substrates have been the gold standard for such applications, their high cost and limited availability pose significant challenges for large-scale production.

To address these concerns, our collaboration between Fraunhofer ISE and III/V Reclaim has been developing an innovative technology that leverages our expertise in growing metamorphic materials as well as polishing them to create high-quality InP layers on GaAs substrates. Our progress has led us to release a new product, the InP-on-GaAs engineered substrate, that can effectively replace a standard InP wafer in a wide variety of applications. This novel substrate, now available in 4-inch and 6-inch diameters, with the opportunity to scale to 8-inch on the horizon, delivers comparable performance to pure InP while significantly reducing costs and enabling higher production volumes. Due to these strengths, our new substrates are the ideal choice for manufacturers looking for competitiveness in a rapidly evolving market.

InP bulk substrates present significant challenges for large-scale production of optoelectronic devices. Among a number of concerns, the most significant

are probably a high cost, brittleness, and limited availability. These weaknesses can be attributed to the process used for manufacturing high-quality InP ingots for wafer fabrication – compared to that employed for producing GaAs, it is more complex and necessitates more costly equipment. The complexity arises from the intrinsic properties of InP, such as its high decomposition pressure at its melting temperature and its greater tendency to twin. Due to these factors, stricter quality assurance standards are essential for managing defects and ensuring wafer quality.

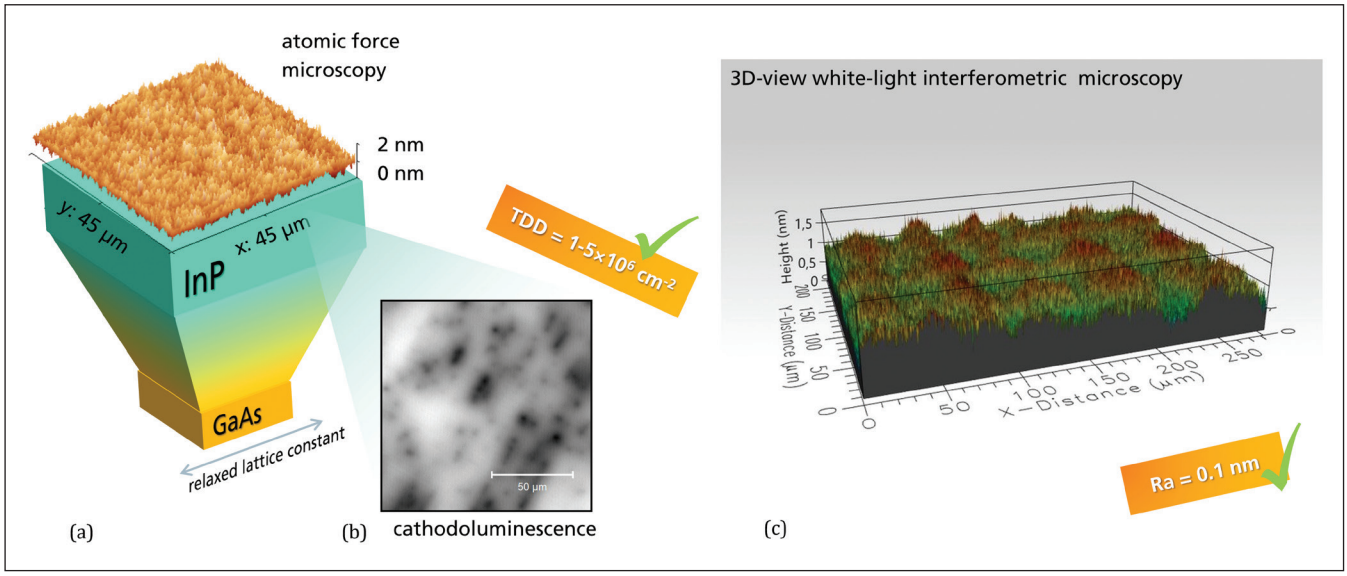
Another downside of the high complexity of the InP production process is that it hampers scalability, limiting availability of larger substrate sizes. Currently, InP substrates are predominantly available in sizes ranging from 2-inch to 4-inch, with the 6-inch variant only recently entering production. This limited range of diameters is a key obstacle to upscaling. Efforts on magnifying dimensions are also impaired by the brittleness of InP that increases the risk of breakage during device fabrication, and leads to a lowering of production yield that escalates costs.

On top of that, InP technologies rely on indium, a relatively rare and expensive element. Market prices for this metal can be volatile, due to a limited supply, as well as high demand in various industries. For instance, last year indium prices shot up by 50 percent. This factor, alongside others just outlined, collectively hinder the widespread adoption and economical mass production of InP-based optoelectronic devices.

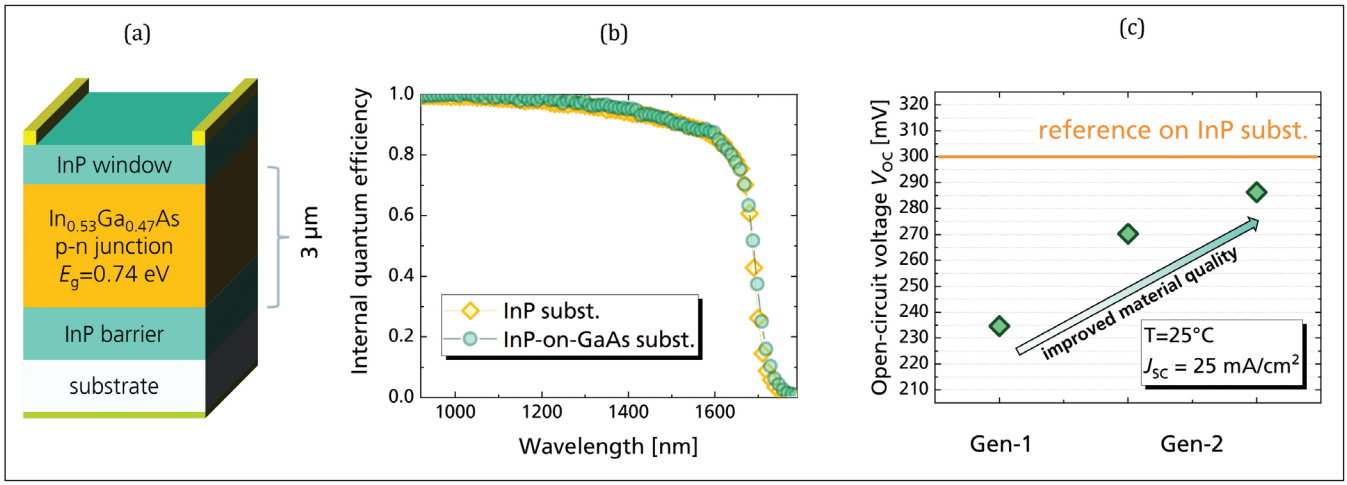
In comparison, the GaAs industry holds significant advantages in terms of large-scale production, since GaAs substrates are generally less expensive to produce, thanks to more mature manufacturing processes refined over many decades. Unlike InP, GaAs substrates are more robust and available in formats up to 8-inch diameter, making them better suited to high-volume manufacturing. The higher stability of GaAs also allows for thinner wafers, consuming fewer of the precious metals. These factors make GaAs a more cost-effective and practical choice for large-scale production of optoelectronic devices.

Integrating InP-based technologies onto GaAs substrates is far from easy, due to one of the most critical challenges in semiconductor manufacturing: the lattice mismatch. There is a difference in atomic spacing of almost 4 percent between InP and GaAs, hindering high-quality epitaxial growth of InP directly on GaAs due to defects forming uncontrolled throughout the layer structure. Harmful defects, also known as threading dislocations, act as recombination centres that slash carrier lifetimes, leading to severe degradation in device performance and efficiency.

By capitalising on our long-standing expertise in developing metamorphic materials, we have developed a robust manufacturing process that ensures that our InP-on-GaAs substrates are of the highest quality. Our final InP-on-GaAs wafer (see Figure 1(a)) features a GaAs substrate, topped with a series of epitaxial buffer layers, culminating in an almost fully relaxed InP surface. This surface, with a threading dislocation density in the range of just 1-5 x 10^6 cm^{-2} "(see Figure 1 (b)), serves as a virtual substrate for subsequent epitaxial growth of InP-based devices. Thanks to this excellent material quality, our engineered wafers ensure reliable performance, even for devices sensitive to degradation in carrier lifetime.



➤ Figure 1. (a) An illustration of the InP-on-GaAs engineered substrate, including a GaAs substrate, an engineered stack of epitaxial buffer layers and the final relaxed InP surface layer. An atomic force microscope image shows the surface morphology and (b) a cathodoluminescence image reveals the low threading dislocation density (TDD) of 1-5 x 10^6 cm^{-2}. (c) A white-light interferometric microscopy image reveals a surface roughness, R_a, of 0.1 nm, comparable to prime InP wafers.

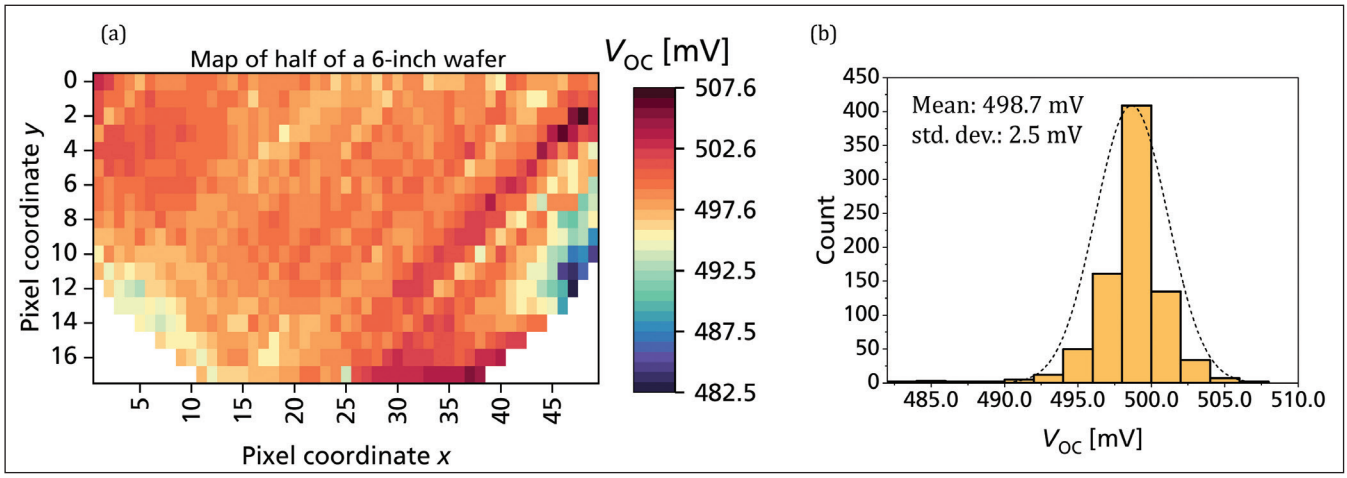


➤ Figure 2. (a) Sketch of the laser power converter grown on InP and InP-on-GaAs substrates. (b) Calibrated internal quantum efficiency (IQE) of laser power converters grown on a reference InP substrate (orange diamonds) and on an InP-on-GaAs engineered substrate (green circles). (c) Open circuit voltage (V_{OC}) measured at a photocurrent density (J_{SC}) of 25 mA cm^{-2} for the laser power converter grown on InP (orange line) and for different generations of InP-on-GaAs substrates (green symbols). Our latest generation of InP-on-GaAs substrates (Gen-2) feature V_{OC} values only 15 mV below the reference device on a InP bulk substrate.

To ensure an epi-ready surface, our as-grown wafers undergo a specialised chemical mechanical polishing process. According to white-light interferometric microscopy, these engineered substrates have exceptional surface morphology, with an arithmetic mean roughness (R_a) of just 0.1 nm, a figure that's comparable to prime InP wafers.

One of our latest experiments provides a representative example of what can be expected with our novel wafers. To provide a fair comparison of the performance of devices made on InP and on InP-on-GaAs, we have fabricated an $In_{0.53}Ga_{0.47}As$ laser power converter (band gap of 0.74 eV) on both a 4-inch pure InP wafer and a 6-inch InP-on-GaAs engineered substrate (the device structure is outlined in Figure 2 (a)). By employing identical epitaxial growth and processing steps, we effectively produced the same device on both substrates.

We have compared the performance of these devices using electro-optical characterisation. Calibrated internal quantum efficiency measurements produce very similar values for photocurrent generation efficiency for devices on InP-on-GaAs and reference InP substrates (see Figure 2 (b)). For the performance metric of the *p-n* junction, we considered the open-circuit voltage of our power converters, measured at a photocurrent density of 25 mA cm^{-2}. The two types of device produced similar values for this metric, with that



➤ Figure 4. (a) Open-circuit voltage (V_{OC}) map of a 6-inch InP-on-GaAs substrate populated with InGaAs laser power converters. Each pixel with coordinate (x,y) corresponds to an individual device with a nominal area of 5.4 mm^2. A total of 826 cells were processed and measured. The photocurrent density was on average 7.98 A cm^{-2} with a standard deviation of 0.11 A cm^{-2}. The V_{OC} performances are reported in histograms in (b).

grown on InP delivering an open-circuit voltage that's higher by 15 meV. Our view is that there is the potential to close even this small gap by fine-tuning the growth conditions, a step that we did not take in this investigation.

While a high-performance is encouraging, manufacturers need good results for all devices across a wafer. The good news is that our engineered substrates fulfil this crucial citeria, with exceptional performance consistency realised across the entire 6-inch substrate area. This strength ensures high productivity by maximising the usable wafer area.

To highlight the great degree of uniformity of devices produced with our technology, we have produced a dense matrix of pixel cells, each with a nominal active areas of 5.4 mm^2. Fabrication involved mesa-etching of every pixel to ensure electrical isolation from adjacent cells. This step has enabled accurate on-wafer characterisation.

In total, we have processed 826 devices on one half of a 6-inch wafer, using a pixel pitch of 2.46 mm by 3.60 mm. We then mapped the performance of the laser power converter across this half wafer using an automated current-voltage characterisation setup featuring a pulsed Xenon lamp, which provided a broadband illumination source. The resulting map of the open-circuit voltage has confirmed the exceptional consistency of performance across the substrate (see Figure 3 (a)), underscoring our wafer's capability to maintain high standards of productivity by fully utilising its area.

Our efforts demonstrate that InP-on-GaAs engineered substrates offer a cost-effective alternative to InP bulk wafers, by leveraging lower material costs and an established supply chain for GaAs wafers. This platform produces a similar performance at the device level, realised at a fraction of the cost, making it feasible for manufacturers to trim production expenses without significantly compromising quality. Even chipmakers producing small volumes will benefit from the very competitive cost of our engineered substrates – they are significantly below that of InP, and there is the promise of a price that's below 20 percent of today's InP price, for large volumes.

Another attribute of our technology is that thanks to the use of GaAs as the starting material, it is possible to quickly ramp manufacturing volumes, as our approach avoids limitations in InP supply. This merit is highly valued by manufacturers in search of shorter lead times, and keen to target the growing demand for high-performance semiconductors in markets such as 5G and upcoming 6G telecommunication, data centres, and advanced photonics.

We are excited to bring this technology to market. It offers manufacturers a new way to fulfil their performance goals while reducing costs and increasing production capacity, benefits that boost a device's bang-per-buck and open new market opportunities. For chipmakers looking for a cost-effective, scalable, high-performance foundation for the growth of epiwafers, our InP-on-GaAs engineered substrates can be the answer, opening the door to the next generation of semiconductor technology.

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➤ The European Large Logistic Lander enables a series of ESA missions, such as the delivery of supplies, rovers, and the return of sample packages from the Moon to Gateway.

Picture Credit: ESA Gallery.

Launching SiC into space

For future space missions, makers of electrical systems need better power devices, a requirement that's met by SiC

BY ANTXON ARRIZABALAGA FROM THE EUROPEAN SPACE AGENCY (ESA)

WE ARE GOING back to the moon, and this time we are going to stay there. Ensuring success is the Artemis programme, a collaboration between the European Space Agency (ESA), NASA, and other international and commercial partners. Together we will establish the first long-term human presence on this celestial body.

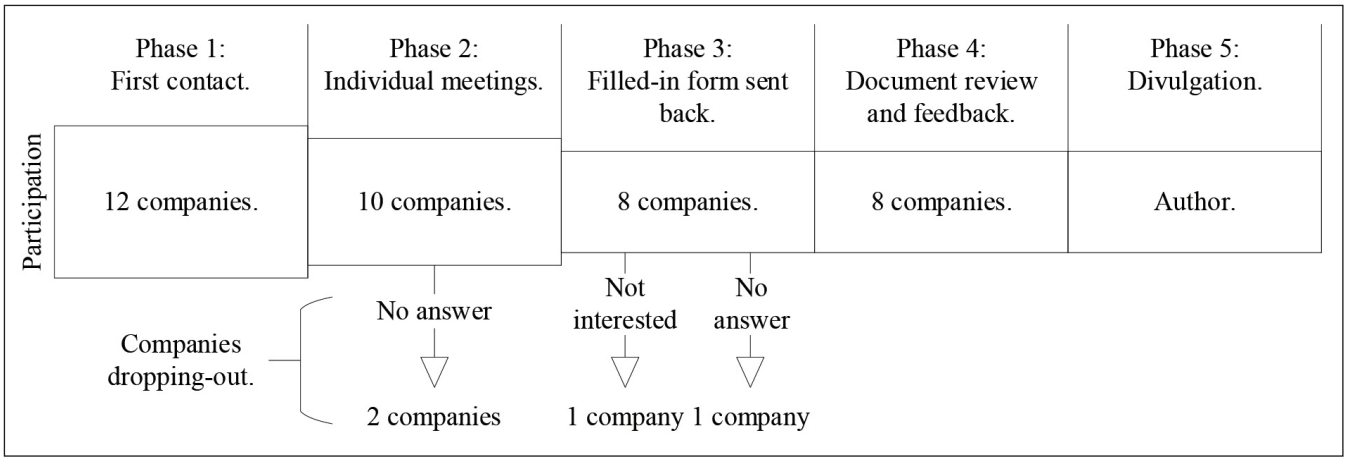
Critical to this success is a number of breathtaking technologies. They include: Gateway, the first space station orbiting the moon; lunar landers, such as Argonaut, able to ship cargo, infrastructure, heavy machinery, rovers, and power stations; and lunar habitable modules, already under development. While all these missions have differing objectives, they share a significant strand: the need for high-power.

Detailing the problem

Needing high power is a major issue, because space-qualified silicon power devices are unable to provide the technical requirements demanded by these high-power missions. Due to this inadequacy, the space power industry is searching for superior alternatives to replace them.

At the ESA, like many other organisations in the space power industry, we have noted an exceptional rise in interest and deployment of SiC power devices, and we have been investigating whether this could meet our needs. Unfortunately, there are no space-qualified SiC power devices on the market today, because producers of wide bandgap transistors and diodes are directing nearly all their attention at the huge automotive industry. Up until now, the general feeling has been that the space market for SiC is too small to generate a business case. But with the recent demand for high power, this is about to change.

To simplify the job of the SiC manufacturers and ensure fast adoption of these devices by the space power industry, we have been talking to the leading space power companies in Europe. During these discussions, we have focused on establishing



➤ Figure 1. The organised phases of the project, together with the number of companies participating in each one. Two companies did not answer the first contact email, while two other companies dropped out after the first meeting with them. One of the companies told us they mainly focus on low-power applications, and they are satisfied with the current available power device technology. The other company participated actively in the meeting, giving positive feedback, proposing ideas and even providing further information in the following months after the meeting. However, they failed to send back the filled-in form with the requested specific information. We sent a reminder, but they still did not send the form, so even if we included their feedback in the documentation, we considered them as dropping out. We were contacted by this company again after the technical talk in ICSCRM 2024, asking for follow-up information, which we gladly provided.

a clear idea of their needs, identifying potential applications, classifying the main technical drivers, and opening a new market for SiC manufacturers. Drawing on all that we have learned will enable the design of optimised devices for specific applications, making the technological transition seamless for the space industry and their adoption of these devices faster. In addition, this chain of events will create a clear business case for SiC manufacturers.

We organised our project in five phases. Efforts began by making an initial contact with the most important European companies. We then continued with individual meetings, the filling-in of specially designed forms, and gathering, classifying and documenting all the information. The final phase, divulgation, has involved reporting our findings to the SiC community using various platforms, including this publication. As part of this effort, we delivered an extended talk in a technical session at the most recent International Conference on Silicon Carbide and Related Materials, held in Raleigh, North Carolina, last autumn.

What does industry need?

After gathering and collating information from various companies, we had to classify it to ensure public access to this huge resource. We based our first classification according to industry needs.

One of our key findings is that the space industry needs to increase the power level of its systems, without losing performance. This can only be accomplished by increasing either the voltage of the system, its current, or both. Mainly due to limitations in the blocking-voltage capability of space-qualified devices, together with other technologies, increasing the current is the most common approach. Unfortunately, it's not possible to succeed on this front with state-of-the-art space power device technology without impacting performance.

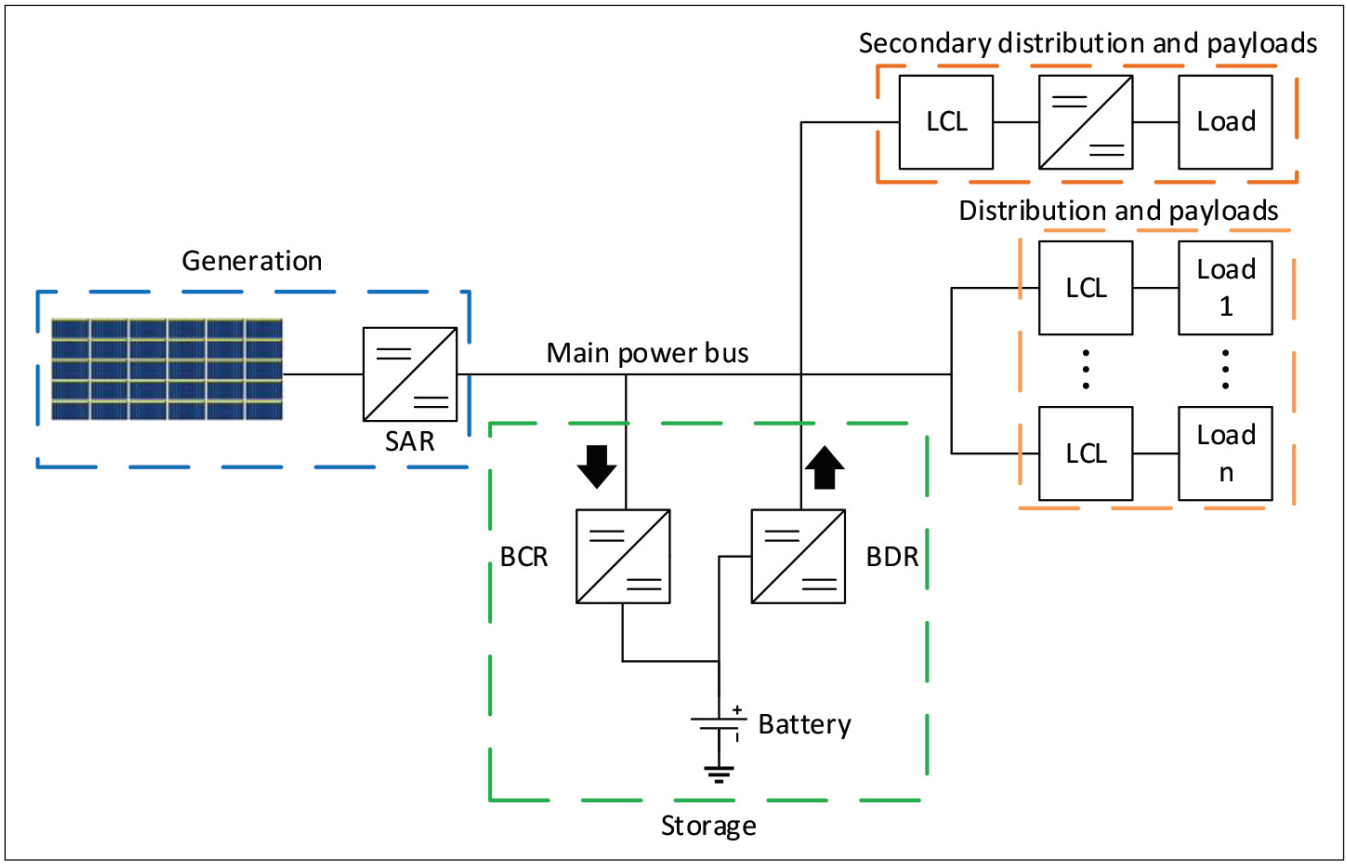
What the space industry needs is 'bigger' devices, with a higher blocking-voltage capability and a higher rated current, strengths that will allow the handling of more power in a single device while maintaining the performance figures provided by low-power systems.

Note that the space industry already has high-power solutions. How do they do it? It's through unwanted compromises, such as slow high-current devices or paralleling several lower-current ones. These approaches lead to complex layouts, high volume and lossy systems. Due to these weaknesses, the space industry is keen to improve the performance of already existing high-power systems. What this means is 'better' devices, operating at a high voltage with a lower conduction resistance, and at high current with improved switching characteristics.

Which applications?

Space systems are nothing more and nothing less than systems that provide autonomous energy generation, storage, distribution and consumption. They can be thought of as a microgrid, working in island mode, in either orbit or in space.

As is the case with any autonomous energetic system, the generated electrical power must be transformed, distributed, and transformed again, before it is either stored or consumed by the payloads – those are the end users of the satellites or space systems. DC is used for power generation from solar arrays, storage with batteries, and consumption by most payloads.



➤ Figure 2. The power architectures of satellites include several power conversion and distribution stages. Each regulator is a converter, usually based on several devices. Specific loads might require secondary distribution lines, with their own DC-DC converter to regulate the voltage to the required level by the payload. Each one of these electronic systems requires an increase in power for the future missions, providing the space industry with the opportunity to introduce SiC devices in their designs.

Generation with solar arrays, storage with batteries and consumption by most of the payloads is done in DC. To carry out the various tasks required in space, there is the need for power conversion, predominantly involving DC-DC converters based on the power devices we study. If the power of the payload increases, so does power generation, and in turn the power of the converters providing power conversion and distribution.

The space industry is considering SiC for the main DC-DC converters in satellites, the solar array regulator, the battery charge and discharge regulators, and the converters supplying the payloads. All of these DC-DC converters will have to be high-power and high-voltage. In addition, these DC-DC topologies will tend to need to include a rectifying stage. Regardless of whether this rectification is realised by diodes or synchronous active switches, these devices will need to match the high-voltage and high-power levels of the application. SiC will also play a vital part in the rectification.

Latching current limiters, traditionally based on silicon *p*-type MOSFETs for control simplicity, are used to manage the distribution and payload current limitation. However, the performance of these devices degrades drastically under high voltages, and they are very limited in current, so high voltages and high powers are not feasible with this technology. Alternatives that have warranted attention include *n*-type MOSFETs, even involving switched configurations based on GaN devices. However, as voltage and power requirements in the distribution increase, the appeal of SiC enhances. The space industry is interested in using SiC for high-voltage and high-power latching current limiters in the near future, to enable high-power distribution.

There is also a growing demand for high-power electric motor drives, mostly related to lunar landers and heavy machinery. These specific converters are not common in satellites, but they operate with similar concepts, having a dedicated battery. Due to voltage limits, these motor drives have to be very high-current systems. Even if they only operate for short periods of time, they have performance requirements that are very hard to meet with today's silicon devices.

It would be remiss of us to not mention very high-voltage applications. These are rare, involving the use of several hundred volts to supply power to scientific equipment or propulsion units. If very high-voltage distribution is needed, this requires

specific very high-voltage systems, such as current breakers. For all of these applications, specific main drivers should be optimised, improving determined technical requirements.

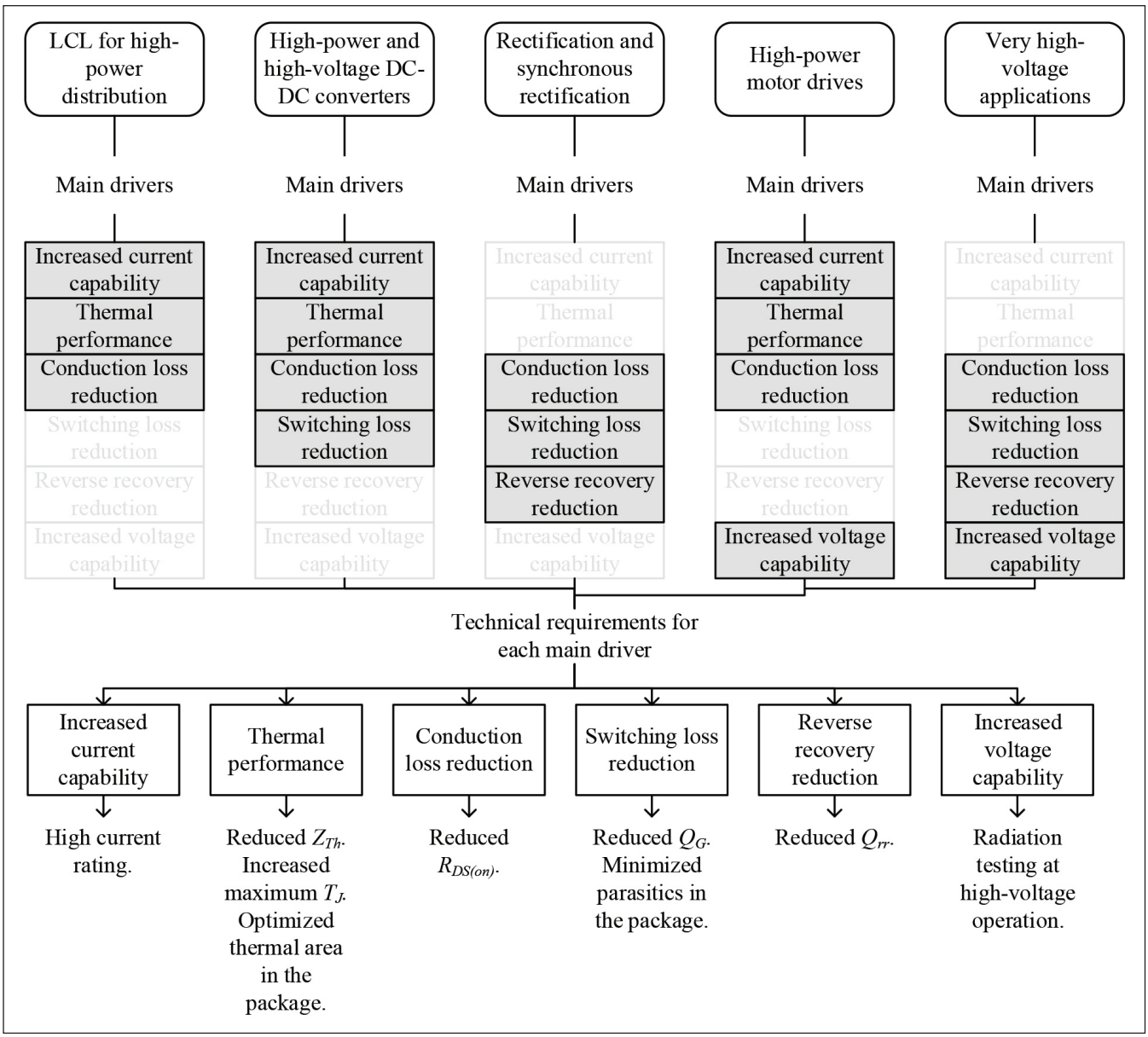
What about packaging?

Every package should be an enabler, and never a limiting factor on the operation of power devices. To ensure that this is the case, the package must be considered from the very beginning of the design process, to ensure that it provides all the functions required in a particular application.

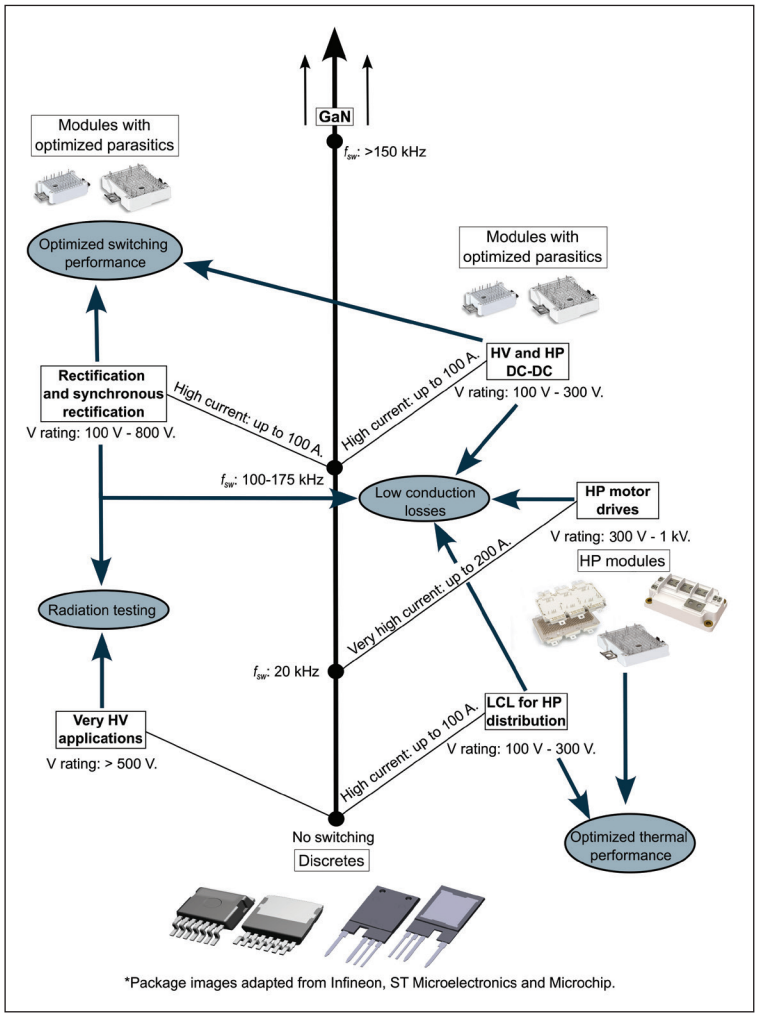
Once the target application of a new product is defined, its manufacturer must identify the main drivers and start working on the package, to ensure it is designed accordingly. This approach can be a game-changer for the adoption of a new product by industry.

It is in the low switching frequencies where we tend to find the highest power applications, such as high-power motor drives. Here, several tens of watts may be generated in the form of heat – and this needs to be removed from the die. The space industry is looking for a specific high-power package with an optimised thermal plate, directly connected to a cooling system, to ensure a low thermal impedance path.

Meanwhile, in applications requiring a high switching frequency, the devices that are deployed have the lowest gate charge and thus the fastest switching dynamics. As this leads to rapid changes in current and voltage in the converter, the package cannot



➤ Figure 3. The most mentioned applications among all the responses and feedback to the ESA from industry. During this information-gathering exercise the ESA ensured that industry made it clear what were the main drivers they wanted to be optimised in each application. The ESA has also detailed the technical requirements that the new devices need to fulfil to make a positive impact in each main driver.



➤ Figure 4. Packaging should be an enabler in a power device. As each application has its own main drivers, the devices used in them should also adapt to provide the required performance figures, together with the packaging. Moving from discrete components, where the cooling of die is done individually, industry sees the opportunity to introduce popular power modules, integrating more than one device. For very high-power applications, cooling of the die is optimised through a thermal plate, which conducts heat directly to the cooling system. For high-frequency applications, where parasitic components gain importance, the burden of creating good layouts is taken off the power engineers if the power modules already optimise the connections between the switches.

have long bonding wires and connections, because that would create current loops that insert several nano-Henries into the switching loops. In this case the package must be designed to ensure the best layout and trim inductance in the switching loop, as this will prevent undesired ringing and overshoots during fast switching.

Will industry adopt SiC?

The key to answering the question of whether the space industry will adopt SiC is to first understand how it operates. Understandably, this industry is heavily reliability driven. Due to this, there is openness to applying minor changes, if they offer demonstratable performance gains; but there is great reluctance to applying big changes to systems. The space industry loves to keep using its well-tested, reliable systems with a wide flight heritage.

Knowing this, it is clear that a new device has a much better chance of early adoption if it can be deployed in a conventional system. In the case of our power devices, this means operating SiC devices with space-qualified, well-known drivers and peripheral technology, such as the PCB, capacitors and connectors. Taking this approach reduces the development effort, time and cost for the space power electronics makers, while increasing the confidence level in their new product.

The approach to introducing SiC should be based on offering performance-enhancing innovations, as this addresses the two primary needs of the industry, which we have already discussed (to recap, they are increasing the power level of the system without diminishing its performance, and improving the performance of already existing high-power systems). It is critical that these performance enhancements impact the main drivers of the target application, without changing any peripheral technology.

However, while this approach is the best way to ensure a fast and seamless adoption of SiC technology by the space industry, it is detrimental

Radiation requirements

WHEN SiC power devices are flying in space, they will be exposed to hard radiation environments. This could lead to single-event (SE) effects that degrade the voltage-blocking capability of SiC devices in space. These effects are related to the impact of an energetic particle, leading the device to suffer from SE leakage (degradation), SE burnout (complete destruction), or SE gate rupture (if hit in the gate region). For now, the consensus among radiation experts is that the best way to prevent any SE-related issue is to derate the blocking voltage of the SiC devices. By using 1.2 kV SiC power devices, designers can derate SiC considerably while still being able to operate at over 100 V in space. However, performance comparisons need to use the operating voltage, rather than the terrestrial rating. This is the approach taken by the ESA, when using its testing platforms to compare the performance of space-qualified silicon and industrial SiC, even though it demands a case-by-case radiation analysis for every design. This need for thoroughness highlights why qualifying new SiC devices is a must for the space industry. Having qualified parts will allow aeronautical engineers to create designs without having to analyse the radiation performance case to case, ensuring repetitive behaviour and safe operation under defined radiation limits.

Failure modes

SPACE is a reliability driven industry. Every electronic design and unit accepted by ESA should be free from single-point failure. Hot and cold redundancies are common techniques to avoid single-failure modes in electronics designs, both at the component and the unit level. Every company is obliged to perform failure modes, effects, and criticality analysis before a unit is approved to fly.

This analysis is tiring and extremely time consuming. Extended knowledge on failure modes of SiC, its propagation principles and statistical data will provide invaluable information to the space power industry. In fact, this data is so important that it is hard to imagine any space power company adopting a new device for its major products without detailed communication and collaboration from the device manufacturer. This is a clear message from the space industry to SiC manufacturers: data and knowledge on failure modes and device degradation is as valuable as nominal operation data. Having a good understanding of these phenomenon, alongside maintaining a transparent and collaborative approach with the space industry, will massively help to increase the acceptance of the technology and ease its adoption.

to the performance of these wide bandgap power devices. That's because using space-qualified drivers for SiC, rather than those that are specially optimised, impacts the performance of the power device, limiting the benefits that can be enjoyed. It is crucial to test the performance of this setup that's not been optimised for SiC, and compare it to the state-of-the-art system. The degree of success in these tests will define the adoption of SiC by the space industry.

What is ESA doing?

At the ESA, we are advancing the technology readiness level of SiC devices in space applications, and testing their performance in space operation conditions. We have developed two testing platforms for these tasks: one is designed for discrete components, and the other is intended to test high-power half-bridge SiC modules.

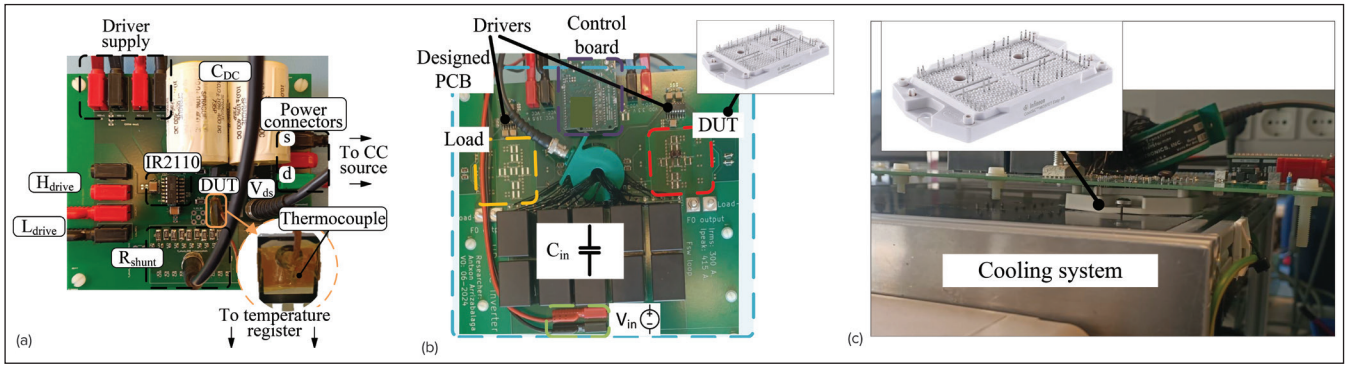
Both these platforms have the same objective, which is to show the space industry that it is possible to obtain performance gains with SiC without having to make major changes to the system. By only using space-qualified, well-known drivers and peripheral technology in our two platforms, we are following the approach that the space industry wants for early technology adoption.

In the discrete component platform, the power device is replaceable. It is possible to solder both space-qualified silicon and industrial SiC in the same system. With this platform, engineers can compare conduction and switching performance under the same operating conditions for both technologies. With the high-power platform, we are able to replicate the high current operation condition of the high-power motor drives. Successful testing could lead to one high-power half-bridge SiC module replacing up to eight space-qualified silicon MOSFETs, a move that can introduce substantial gains in the system. Again, all the peripheral technology is space-qualified for a fair comparison, and to ensure a seamless adoption by industry.

As mentioned before, our activities extend to actively presenting our results, and sharing them in written and spoken forms. We are also offering assistance to interested companies, as well as guidance to the SiC manufacturers.

In addition, the ESA is funding space-qualified SiC development projects. They include EPOSiC, which is targeting the development, manufacture and full space qualification of a 300 V 50 A half-bridge SiC module that's manufactured completely in Europe. This ambitious project shows our agency's commitment to developing technology that will take us back to the moon and allow us to stay there.

In the meantime, we will focus on launching SiC into space. As W. Clement Stone said: "Aim for the moon. If you miss, you might hit a star."



➤ Figure 5. The ESA has developed two testing platforms. One is for discrete components and the other is for high-power modules. In both platforms, all peripheral technology is space-qualified, including the drivers. Proving performance gains with SiC power devices, while still using well known space-qualified peripheral technology, will increase the acceptance of the new technology, accelerating its adoption. This is being tested in space operation conditions in ESA labs, with satisfactory results, increasing knowledge and the device's technology readiness level.

Transferrable vertical microLEDs arrays

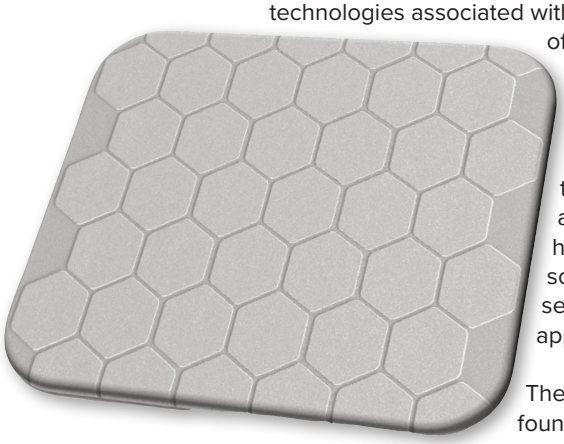
It's not easy to transfer arrays of incredibly small, vertical GaN-based microLEDs to another platform. But there is a promising solution: selective-area growth of these emitters on hexagonal boron nitride

BY SURESH SUNDARAM AND ABDALLAH OUGAZZADEN FROM GEORGIA TECH EUROPE

MANY are viewing microLEDs as the future of displays. Compared with their organic counterparts, these miniature marvels offer superior efficiencies, higher brightness levels, exceptional contrast, a wide colour gamut, and ease of manufacturability.

Unfortunately, it's not easy to leverage the standard GaN-based LED growth process and apply it to microLEDs with a top-down fabrication process. That's because succeeding on this front, which would unlock the door to mass manufacturing, requires addressing a number of key challenges. For example, when etching is employed to define the dimensions of the microLED, this process induces side-wall damage that causes efficiency to plummet with increasing miniaturisation.

Compounding this concern, reliable mass transfer technologies associated with the manufacture of microLED displays are seen as complex and costly. There is a need for devices to be more flexible and offer better heat dissipation, so that they can serve in niche applications.



The most common foundation for LED production is the sapphire substrate. However, due to its poor thermal and electrical conductivities, as well as its lack of flexibility, there's a compelling case for trying to remove this particular substrate from the active device package.

Offering an approach doing just this is our team from the Georgia Tech-CNRS Lab at Georgia Tech Europe in Metz, France. We have overcome all the issues just described with a novel growth technology that employs two-dimensional materials and the selective-area growth of GaN. Taking this approach eliminates the need for device isolation and dicing microLED arrays, and thus eliminates the threat of side-wall damage. What's more, there's the opportunity for colour tuneability via the size of the microLED, a feature that promises to lead to simple monolithic integration of full-colour displays while avoiding complex issues.

2D materials

Compelling candidates for providing ease of transfer and flexibility for microLED-based displays are those that involve the heterointegration of III-nitrides with two-dimensional (2D) material platforms, such as graphene and hexagonal boron nitride (h-BN). They may be produced by advanced growth methods, such as van der Waals epitaxy and remote epitaxy. While there are many ways to separate sapphire substrates from active devices, standing out for its simplicity is mechanical exfoliation using sacrificial 2D material.

We are making much progress on this front, having demonstrated the growth of a number of important optoelectronic devices on the h-BN platform – such as LEDs, HEMTs and solar cells – and their transfer to flexible and rigid substrates, foundations that ensure improved optical and electrical performance.

This approach offers several other major advantages, including scalability, with wafer sizes up to 6-inch demonstrated, and the use of thin buffers that trim the thickness of overall device structures to less than 1 μm, cutting the time and energy associated with the

growth process. What's more, our easy transfer to a desired platform ensures a vertical LED architecture that eliminates many front-end processing steps, including mesa-etching. Working with Jeehwan Kim's group at Massachusetts Institute of Technology, and Young Joon Hong's team, formerly of Sejong University, we have gone on to demonstrate a vertically stacked microLED display, produced using van der Waals epitaxy. This ground-breaking vertical stack architecture for a full-colour display is incredibly thin – it's less than 10 μm-thick – and it has a density of 5,500 pixels per inch, sufficient for augmented-reality and virtual-reality headset displays.

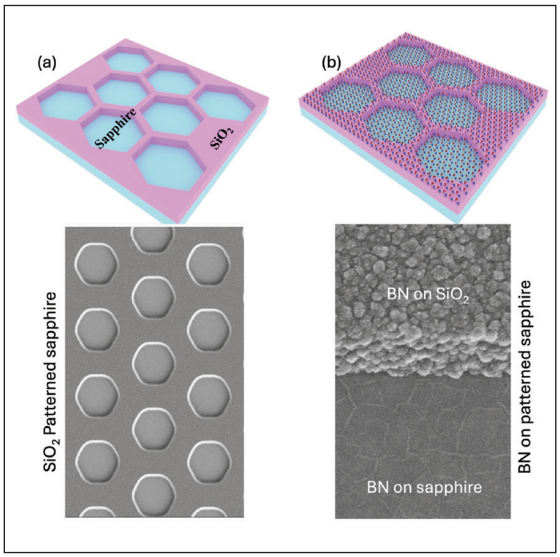
Another key breakthrough by our team is the development of a unique bottom-up approach that allows the fabrication of a matrix of transferrable microLEDs, with sizes down to around just 1 μm^2. This involves selective-area van der Waals epitaxy, which may solve an inherent issue with the van der Waals epitaxially grown structures: self-delamination during growth/post-growth processing. This concern is addressed while simultaneously providing solutions to the above-mentioned issues associated with microLEDs.

The fabrication of our devices starts with patterning sapphire substrates with dielectric layers to the required geometry, in terms of size and shape, before growing GaN-based LEDs on h-BN. We use a standard photolithography process to produce square, hexagonal, and triangular openings in a dielectric, such as SiO_2 or SiN_x, that's deposited on a sapphire substrate (an example, hexagonal patterns, is shown in Figure 1(a)). These openings range from around just 1 μm^2 to several hundred times this size, and employ dielectric mask widths ranging from 2 μm to 5 μm.

Selective growth?

The use of layered materials, such as h-BN in selective-area growth, is new and unexplored. To us, the big questions have been whether BN can be grown selectively, and whether the BN platform can be used for GaN selective-area growth. It's expected that when BN is grown on different substrates, this yields layers of a similar quality, due to the weak van der Waals forces and the absence of polar bonding between the layers and substrates. However, the orientation of the nucleus and the grain sizes of layered material are governed by substrate orientation and crystalline quality.

Our investigations began by growing a thin covering of BN on a sapphire substrate patterned with dielectric materials, such as SiO_2 and SiN_x. We found that the BN film inside the opening in the patterned area matches the quality of standard h-BN on the sapphire surface, forming semi-hexagonal wrinkles (see Figure 1 (b)). According to localised scanning electron microscopy and transmission electron microscopy images, the BN on the dielectrics has a comparable thickness to that on the patterned area, but has drastically different morphology and crystallinity.



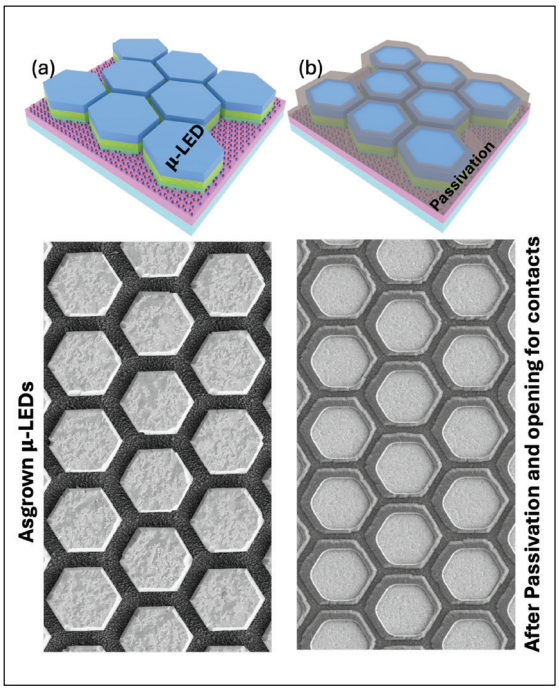
➤ Figure 1. (a) Structure and scanning electron microscopy (SEM) images of SiO_2 mask deposition by PECVD and hexagonal patterning on epi-ready sapphire substrates for growth. (b) Structure and SEM image of h-BN grown by MOCVD on patterned sapphire substrates, showing high-quality BN with wrinkles on sapphire and granular BN deposits on mask patterns.

These forms of microscopy reveal that the BN on the dielectric is completely non-crystalline, with a granular morphology (see Figure 1 (b)), while that on sapphire has long-range order. Even though BN grows and conforms over the dielectric pattern, there is an unprecedented difference in lateral quality that exists between the BN that's grown on sapphire and the BN on the dielectric patterns, and this may lead to the selectivity of the GaN-based device structures.

As previously discussed, the selectivity of GaN that's grown on h-BN-on-patterned-sapphire substrates is an important and highly attractive feature for designing innovative high-quality microLED device architectures. Merits include the opportunity to avoid Kerf losses, and the elimination of several front-end processing steps, such as mesa etchings to isolate/contact devices.

The growth of GaN

Pursuing this attractive approach with vigour, we have produced isolated GaN-based microLED structures with sizes down to around just 1 μm^2 on h-BN on patterned sapphire substrates. There is complete selectivity, with the growth of GaN only occurring on h-BN on *c*-sapphire (see Figure 2 (a)). Although we detected deposits of non-crystalline AlGaN on the BN-on-dielectrics, this ternary does not interfere with the selective-area growth of GaN. Our view is that selective-area van der Waals epitaxy probably promotes the growth of large h-BN

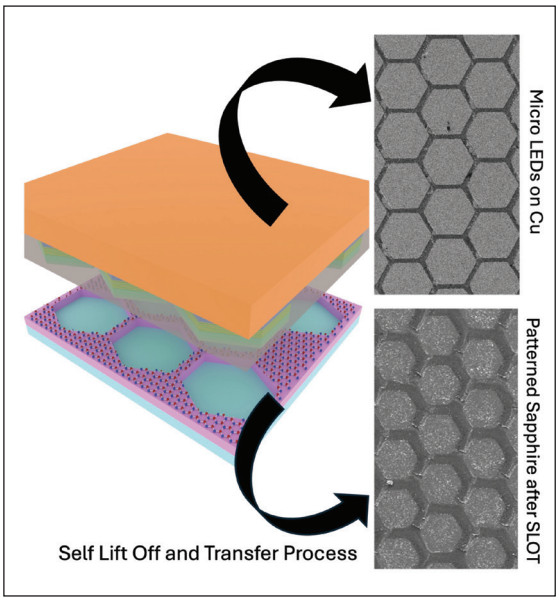


➤ Figure 2. (a) Selective-area growth of a GaN-based LED heterostructure by MOCVD. Structure and scanning electron microscopy (SEM) image of microLEDs grown on hexagonal openings. (b) An SEM image after LED's sidewall insulation by SiO_2 deposition and opening the top surface for a *p*-type contact.

and AlGaN grains, leading to more homogeneous lateral coalescence. The upshot is a reduction in the generation of stacking faults in h-BN and dislocations in subsequent GaN/AlGaN layers, compared with growth on a pristine substrate. Thanks to this, there are considerable improvements in electrical and optical performance.

As expected, our approach mitigates the random self-delamination of layers from the substrate during growth or post-growth processing, due to effective strain relaxation within available free lateral surfaces. This lack of self-delamination is promising for realising thick device buffer layers and high-power devices, along with improvement in yield and reproducibility.

We have recorded a noticeable, continuous shift in the emission colour with the size of the microLED. Shrinking dimensions from 32 μm^2 to around just 1 μm^2 shifts emission from 474 nm to 520 nm. Driving this red-shift is an increase in indium incorporation, as well as a thickness augmentation in quantum wells, associated with changes in surface dynamics that result from selective-area growth. It is possible that by adjusting the geometry of the patterns – that is, the size of the mask and the openings – or by increasing indium content in the quantum well, it may be possible to propel the emission of GaN-based microLEDs to the red. Success on this front could lead to the monolithic integration of red-blue-green vertically stacked active matrix microLED displays.



➤ Figure 3. (a) Deposition of a *p*-type contact, seed layer and copper electroplating for self-lift-off process and transfer to copper substrate, and a scanning electron microscopy image of lifted-off arrays of hexagonal microLEDs on copper and remaining sapphire substrates with just emptied patterns on it.

With our approach, prior to the transfer process, we deposit SiO_2 to insulate the sidewalls and define an opening in the top surface, to allow for the addition of a *p*-type contact (see Figure 2(b)).

Our next step is to transfer our arrays of LEDs to thick copper templates with a self-lift-off and transfer process. This involves the deposition of a titanium (10 nm) and gold (15 nm) seed layer, followed by electroplating a 30 μm-thick layer of copper.

Subsequent heating of this hetero-layer creates thermal stress that induces self-lift-off of the GaN microLED arrays to copper (see Figure 3).

As expected, our approach mitigates the random self-delamination of layers from the substrate during growth or post-growth processing, due to effective strain relaxation within available free lateral surfaces. This lack of self-delamination is promising for realising thick device buffer layers and high-power devices, along with improvement in yield and reproducibility

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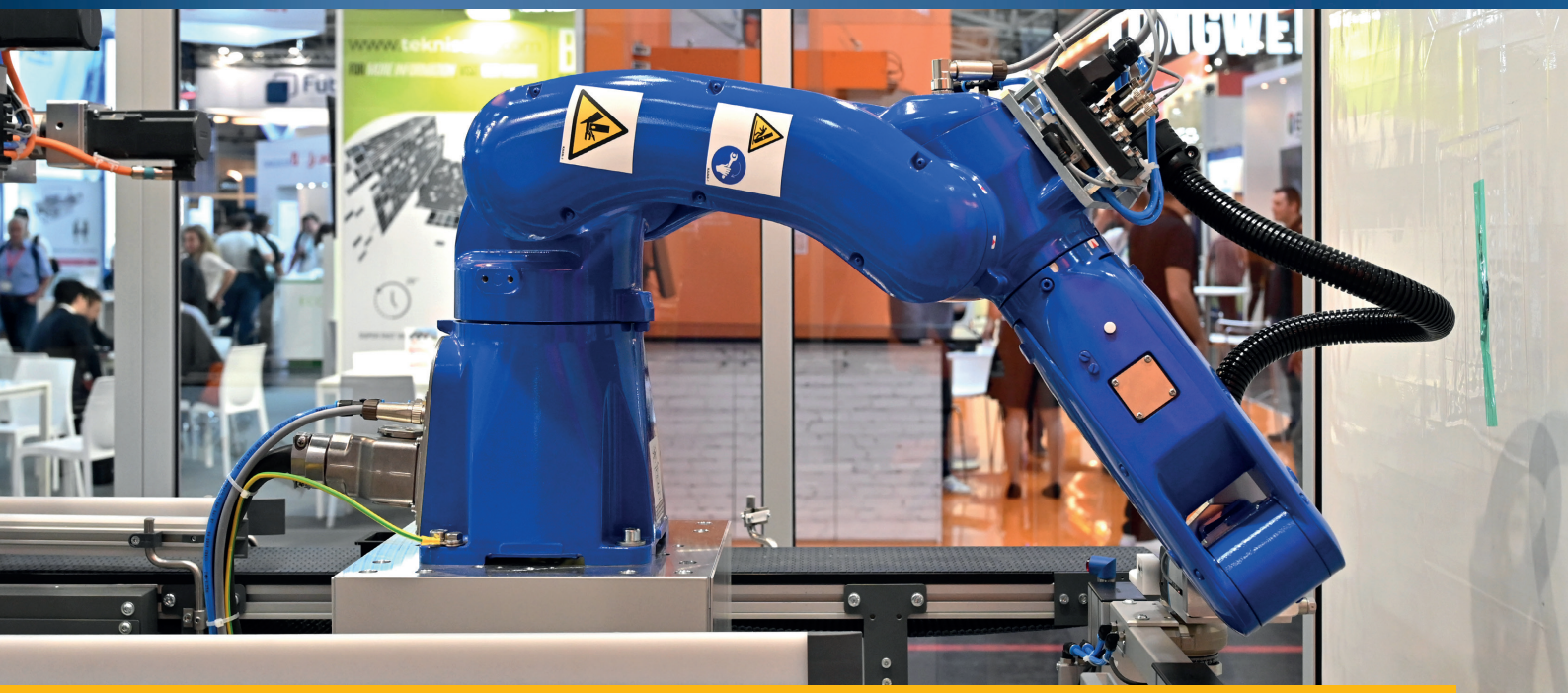

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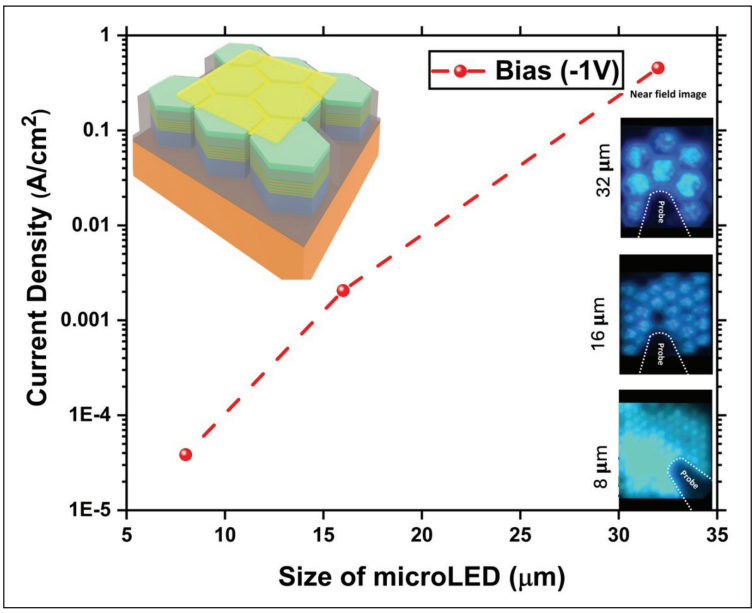
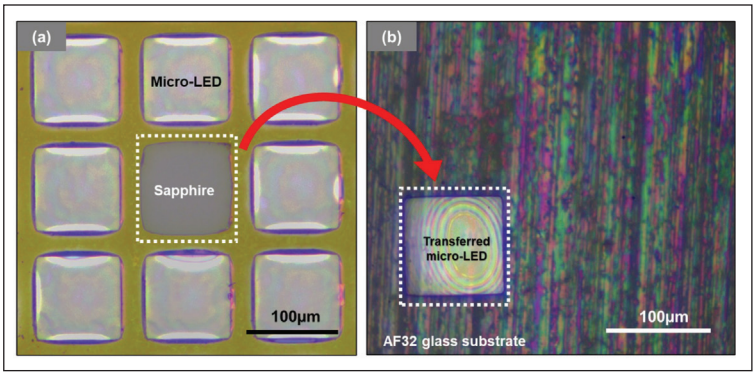


➤ Figure 4. Variation of current density (at –1 V bias) with the size of the microLED shows a four-orders-of-magnitude lower current density for an 8 μm² size LED. Left inset shows the complete structure of microLED arrays with an ITO top contact on a copper carrier and right inset shows the near-field images of the emission from the microLED arrays of different sizes, with changes from blue to cyan with the size of the microLED.



➤ Figure 5. (a) Optical microscope image of (a) the as-grown sample after an individual microLED lifted off using a transfer printing machine, and (b) the microLED transferred onto a flexible substrate.

FURTHER READING / REFERENCE

- Ayari *et al.* "Method for large scale growth and fabrication of III-nitride devices on 2D-layered h-BN without spontaneous delamination" US 12,155,005 B2 dated Nov. 26, 2024.
- R. Gujrati *et al.* "Multiple Shapes Micro-LEDs with Defect Free Sidewalls and Simple Liftoff and Transfer Using Selective Area Growth on Hexagonal Boron Nitride Template". Adv. Mater. Technol. **8** 2300147 (2023)
- T. M. Tran *et al.* "Transferrable GaN-based Micro-LED heterostructures grown on h-BN for optogenetic applications". J. Cryst. Growth **650** 127979 (2025).

Note that when we transfer microLEDs, with sizes of up to 8 μm², their structure completely lifts off from the sapphire substrate. Following the transfer, there is no trace of the microLED in patterned sapphire – providing evidence of 100 percent yield – and there are no induced defects or cracks, according to scanning electron microscopy images (see Figure 3). Our microLEDs maintain well defined crystallographic facets and a smooth surface all around, irrespective of the mask width, providing proof of high-quality selective-area growth and effective transfer.

A great strength of smooth side walls, alongside simplistic passivation, is that it solves side wall leakage, one of the major problems with microLEDs. As they get smaller, the maximum external quantum efficiency, which peaks at a higher current density, falls. Such behaviour is common, and has been ascribed to an increase in leakage current and/or Shockley-Read-Hall non-radiative recombination, caused by sidewall defects in smaller chip geometries that are associated with etching damage.

Interestingly, we find that as the size of our microLEDs decreases from 32 μm² to 8 μm², the reverse current density under a reverse bias of 1 V continuously falls by around four orders of magnitude (see Figure 4). We attribute this behaviour, which is in stark contrast to that reported for microLEDs fabricated with mesa etching, to the superior crystalline quality of the smooth side walls that comes from selective-area van der Waals epitaxy.

Another attribute of our approach is that it enables the transfer of individual pixels to arbitrary flexible templates using a transfer printing machine (see Figure 5). These transferred microLED arrays or pixels can be addressed by a full front-end process, simplifying the manufacture and integration of microLEDs with any platform, including CMOS and TFT.

Our efforts have created a significant, novel microLED growth technology that mitigates several complex performance and manufacturing issues. The progress that we have made provides a foundation for driving the broader adoption of microLEDs, and bringing down the cost of microLED displays from the premium category.

Our next steps are to make this material structure even better, and to monolithically integrate red, blue and green microLEDs. Offering a reduction in cost at industrial scale, we are hopeful that the 2D materials in microLED manufacturing will reach commercial maturity.

The authors thank Jean Paul Salvestrini, Paul L Voss, Phuong Vuong, Rajat Gujrati, and Ashuthosh Srivastava for their contributions to this work.

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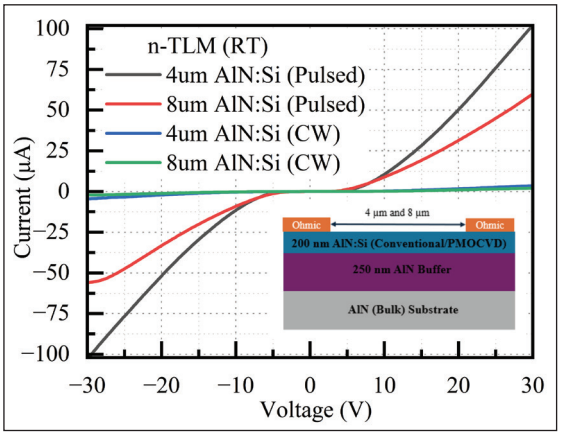
Pulsed MOCVD improves *n*-type AlN

Switching from conventional MOCVD to a pulsed variant enables a hike in the conductivity of *n*-type AlN

ONE OF THE weaknesses of AlN, which hampers its deployment in high-power and high-temperature electronics, is its limited *n*-type conductivity when grown by MOCVD. But this drawback can be overcome by moving to migration-enhanced pulsed MOCVD, according to engineers from the University of South Carolina and Texas Tech University.

Tariq Jamil from University of South Carolina told *Compound Semiconductor* that as well as the introduction of pulsed MOCVD, a well-established technique, *n*-type conductivity benefits from the use of low defect-density substrates and pseudomorphic growth. "This removes any complications in doping measurements from the extended defects that are common in hetero-epitaxial growth," argues Jamil, who adds it is also important to carefully optimise the growth temperature and the dopant concentration for each pulse to avoid over-doping, which can lead to compensation.

Jamil and co-workers have demonstrated the merits of pulsed-MOCVD by comparing silicon-doped AlN layers produced by this technique with those grown by its conventional counterpart.



➤ Pulsed-mode MOCVD is far better at producing silicon-doped AlN layers than conventional MOCVD, according to current-voltage transmission line measurements using electrodes with 4 μm and 8 μm spacings.

For this investigation, the researchers cleaned *c*-orientated AlN substrates with organic solvents, before loading them into an MOCVD chamber and annealing them under ammonia at 1150°C. After growth of a 200 nm-thick undoped AlN layer at 1150°C using conventional MOCVD, the team added a 200 nm-thick *n*-type AlN layer at the same growth temperature, producing samples by both conventional MOCVD and pulsed MOCVD. For the latter process, the introduction of the silicon-dopant coincided with a pulse of the aluminium-based precursor.

Characterisation revealed high material quality. Atomic force microscopy determined very smooth surfaces, with root-mean-square values for surface roughness of 0.92 nm and 0.42 nm for *n*-type epilayers grown by conventional and pulsed MOCVD, respectively. High-resolution X-ray diffraction produced linewidths for the off-axis (1012) and on-axis (0002) of below 40 arcsec for *n*-type AlN produced by both forms of MOCVD, enabling estimates for dislocation densities in this layer of around 10^3 cm^{-2}.

Pumping samples with a 193 nm laser provided photoluminescence spectra, featuring a peak at 5.93 eV, due to emission from the AlN band edge. The sample produced by pulsed MOCVD has a more intense peak, attributed to higher-quality material.

Another feature in the photoluminescence spectra is a peak at 3.2 eV, associated with aluminium-vacancy formation that results from silicon doping. According to the team, the significant difference in conductivity between the two samples cannot be explained by the aluminium-vacancy/silicon complexes, and might result from a reduction in point defects. To look into this, the team is now undertaking low-temperature photoluminescence measurements.

Jamil and co-workers have already investigated the conductivity of their samples with the transmission-line method, adding ohmic contact metals spaced 4 μm and 8 μm apart and annealed at 950°C for 30 s. Current-voltage plots are non-linear at low currents (see figure), hampering estimates of contact resistance. What is clear, though, is the superior conductivity of the sample grown by pulsed MOCVD, which produces a current at a 25-volt bias exceeding that of its conventional counterpart by more than an order of magnitude.

Undertaking current-voltage plots at a range of temperatures has enabled the team to estimate the donor ionisation energy for silicon in AlN. The value obtained is around half that reported by other groups, suggesting pulsed MOCVD leads to a different mechanism for silicon incorporation.

Optimising the growth process is still a work in progress, according to Jamil: "Pulse growth mode has a lot more knobs one can turn. They include aluminium and ammonia pulse widths, metal-organic/dopant concentration in the pulse, temperature, and pressure."

Over the coming months, the team expects to report additional progress in its pulsed-mode growth technology, and to start investigating new dopants, such as germanium for *n*-type doping.

REFERENCE

➤ T. Jamil *et al.* Appl. Phys. Express **18** 025501 (2025)

InGaN full-colour monolithic microLED displays

A full-colour passive matrix display with almost 1,000 pixels is formed from a single wafer

TOYODA GOSEI has unveiled a full-colour InGaN monolithic microLED display produced by stacking and selective removal of light-emitting layers.

This breakthrough builds on this company's development of a monolithic InGaN LED structure, detailed in a previous paper in *Applied Physics Express*, published in autumn 2023.

According to the Japanese chipmaker, while displays can be made by combining single-colour monolithic microLEDs emitting in the green, red and blue with a prism – this is a technology that has been commercialised – from cost-reduction and miniaturisation perspectives, a better option is to realise full-colour emission from a single monolithic microLED chip.

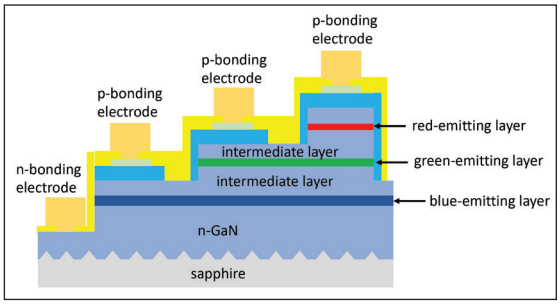
Toyoda Gosei's previously announced approach to realising this involves stacking layers that emit in the red, green and blue on top of *n*-type GaN, prior to selective removal of specific portions of these layers, followed by re-growth of a *p*-type layer (see figure). In the red-emitting region, silicon-doped intermediate layers prevent any electroluminescence from blue-emitting and green-emitting layers that are present. Similarly, in the green-emission region, where red-emitting layers are removed, silicon-doped intermediate layers prevent any electroluminescence from underlying blue-emitting layers.

Building on this full-colour monolithic InGaN technology, engineers at Toyoda Gosei have recently focused on demonstrating displays driven with a passive matrix.

The fabrication of these displays begins depositing an epitaxial structure featuring layers emitting in the blue, red and green. Following selective removal of the light-emitting layers, a *p*-type layer is regrown to form a multi-colour structure, and devices are then created by forming mesas, adding a *p*-contact electrode, isolating sub-pixels between rows, and forming a SiO_2 passivation layer and *n*- and *p*-type bonding layers.

Two additional dry-etching steps ensure that this structure is suitable for a passive matrix display. These two steps involve: removing *n*-type GaN between the rows (there's no need to remove *n*-type GaN between adjacent pixel sub-pixels, due to a passive matrix circuit connecting to a common cathode); and removing the *p*-type layer between adjacent sub-pixels.

Optical measurements highlight the benefits of partial removal of these layers. When probing a green subpixel, in structures that have not undergone *p*-type layer removal, holes that are leaking into adjacent subpixels lead to unintended light emission from these regions, resulting in multi-colour emission. Once the *p*-type layer is removed, leaking is eradicated, and probing the sub-pixel produces emission of only the intended colour.



➤ Toyoda Gosei's full-colour monolithic microLED.

The team have produced a 3 mm by 3 mm display of 96 by 96 pixels, with pitch of 30 μm by 30 μm. Probing the sub-pixels, which have a light-emitting area of 6 μm by 17 μm, with currents from 10 μA to 200 μA, has verified single-peak emission. External quantum efficiencies for red, green and blue sub-pixels are estimated to be about 0.2 percent, 2 percent and 3 percent, respectively.

The drive voltage for the blue microLED is 0.7 eV higher than that for its red-emitting sibling, due to the difference in bandgap. The green LED has the same drive voltage as the blue variant, a concerning matter thought to be due to processing. Toyoda Gosei's engineers are investigating this issue.

To operate the chip as a display, the engineers from Toyoda Gosei added two wiring layers by evaporation. These V/Al/Ti layers are separated by a sputtered 400 nm-thick insulating film of SiO_2.

Using a microcontroller and drive currents of approximately 200 μA, 100 μA and 100 μA for the red, green and blue subpixels, has enabled the demonstration of a display with a colour gamut of 58 percent of the ITU-R Recommendation BT.2020 and 70 percent of the National Television System Committee standard.

One of the next goals for Toyoda Gosei is to demonstrate displays with sub-pixel sizes smaller than 30 μm. Another aim is to improve the efficiency of red InGaN. Results related to this are due to appear in subsequent publications.

REFERENCE

➤ K. Goshonoo *et al*. Appl. Phys. Express **18** 022003 (2025)

Turbocharging AlN/GaN HEMTs

A selective etching process for heavily doped *n*-type contacts enables the scaling of AlN/GaN HEMTs

ENGINEERS from The Ohio State University are claiming to have opened the door to the fabrication of far smaller AlN/GaN HEMTs operating at much higher frequencies.

The team's breakthrough involves the combination of *in-situ* passivation and the addition of re-grown heavily doped *n*-type contacts using a selective etching process.

AlN/GaN HEMTs are a very promising class of transistor for RF and power devices. Compared with the more conventional AlGaN/GaN form of the III-N HEMT, they are free from alloy scattering and have far higher values for electron mobility and the density of the two-dimensional electron gas – up to 4 x 10^{13} cm^{-2}, and between 1000 cm^2 V^{-1} s^{-1} and 1800 cm^2 V^{-1} s^{-1}, respectively.

Back in 2010, Keisuke Shinohara and co-workers from HRL Laboratories reported values for the cut-off frequency and maximum oscillation frequency of AlN/GaN HEMTs of 220 GHz and 400 GHz, respectively. According to the engineers from Ohio, an even better performance could come from scaling the source-drain spacing. However, this is not easy with the conventional process, involving re-growth and a lift-off step using SiO_2.

The Ohio approach is claimed to offer an alternative that facilitates the production of aggressively scaled HEMTs with a very low contact resistance.

To demonstrate the potential of their novel process, the engineers from Ohio have produced AlN/GaN HEMTs from epiwafers featuring an AlN nucleation layer, a 1.5 μm-thick semi-insulating buffer, a 100 nm-thick unintentionally doped GaN channel, a 5.8 nm-thick barrier and a 4.3 nm-thick *in-situ* SiN layer. According to Hall effect measurements, the two-dimensional electron gas in this epistructure has a carrier density of 2.2 x 10^{13} cm^{-2} and an electron mobility of 1060 cm^2 V^{-1} s^{-1}.

Device fabrication began with selective etching to expose the sidewalls of the two-dimensional electron gas and enable a source-to-drain spacing of 3 μm. After applying gallium polishing to desorb sub-oxides from the surface and the sidewalls of the two-dimensional electron gas, the team loaded the processed epiwafer into an MBE chamber and deposited a layer of heavily doped *n*-type GaN, grown to a height that leads to an extension above the SiN surface of 20 nm. This approach is designed to ensure sidewall contact with the two-dimensional electron gas. Chemical etching selectively removed the polycrystalline GaN formed on the unetched *in-situ* SiN layer to expose the active region for the gates.

The team has analysed the quality of its processed wafers by various forms of electron microscopy, and found no obvious dislocations or boundaries at the etched edge and regrowth interface, suggesting high-quality lattice-matched *n*-type GaN re-growth.

To complete the fabrication of the AlN/GaN HEMTs, the team used plasma-etching to form a mesa, employed electron-beam evaporation to add non-alloyed metal stacks on the regrown GaN regions, and formed 0.7 μm Ni/Au gates by optical lithography and electron-beam evaporation.

Scrutinising these transistors with a focused ion-beam scanning tunnelling electron microscope revealed a straight and clear interface between titanium and SiN. This suggests that processing did not cause any breaking or damage to the thin SiN layer, so it can fulfil its role of preventing the AlN surface from being exposed.

Scanning electron microscopy images reveal that the edge definition for the regrown *n*-type GaN is straight and clear with sharp acuity. In contrast, images for a control device produced with a conventional lift-off process uncover irregular and rough edges, a weakness that hampers aggressive device scaling.

Hall effect measurements on the HEMTs produce similar values to those on the epiwafers, indicating that processing did not induce surface damage.

The engineers measured an interface resistance of 0.058 Ω mm, which is close to the theoretical value. Based on this finding, the team suggests that their etching process does not degrade the interface between the regrown *n*-type GaN and the etched two-dimensional electron gas sidewall.

Electrical measurements on HEMTs with a gate length of 0.7 μm determined a maximum transconductance of 0.25 S mm^{-1}, and a linear fit and extrapolation suggest a threshold voltage of -4.9 V. The maximum drain current is 1.57 mA mm^{-1}, and there's an on-resistance of 1.85 Ω mm at a gate voltage of 1 V. Breakdown voltage is 23.3 V, similar to that for control devices produced with conventional process, suggesting that the engineer's selective etching process does not degrade breakdown performance.

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➤ C. Cao *et al*. Appl. Phys. Express **18** 036501 (2025)

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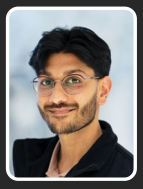

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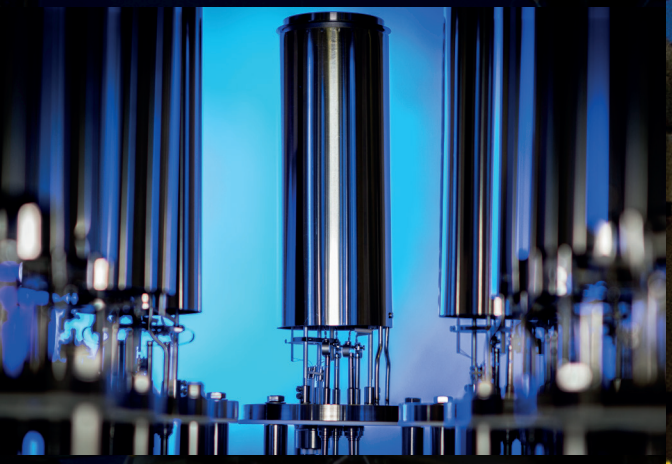

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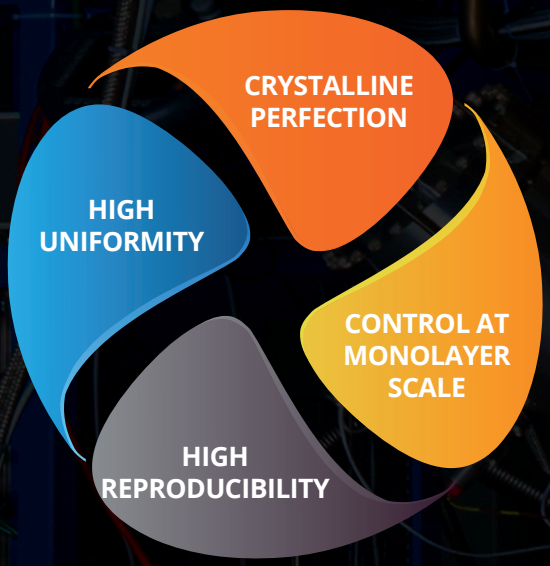

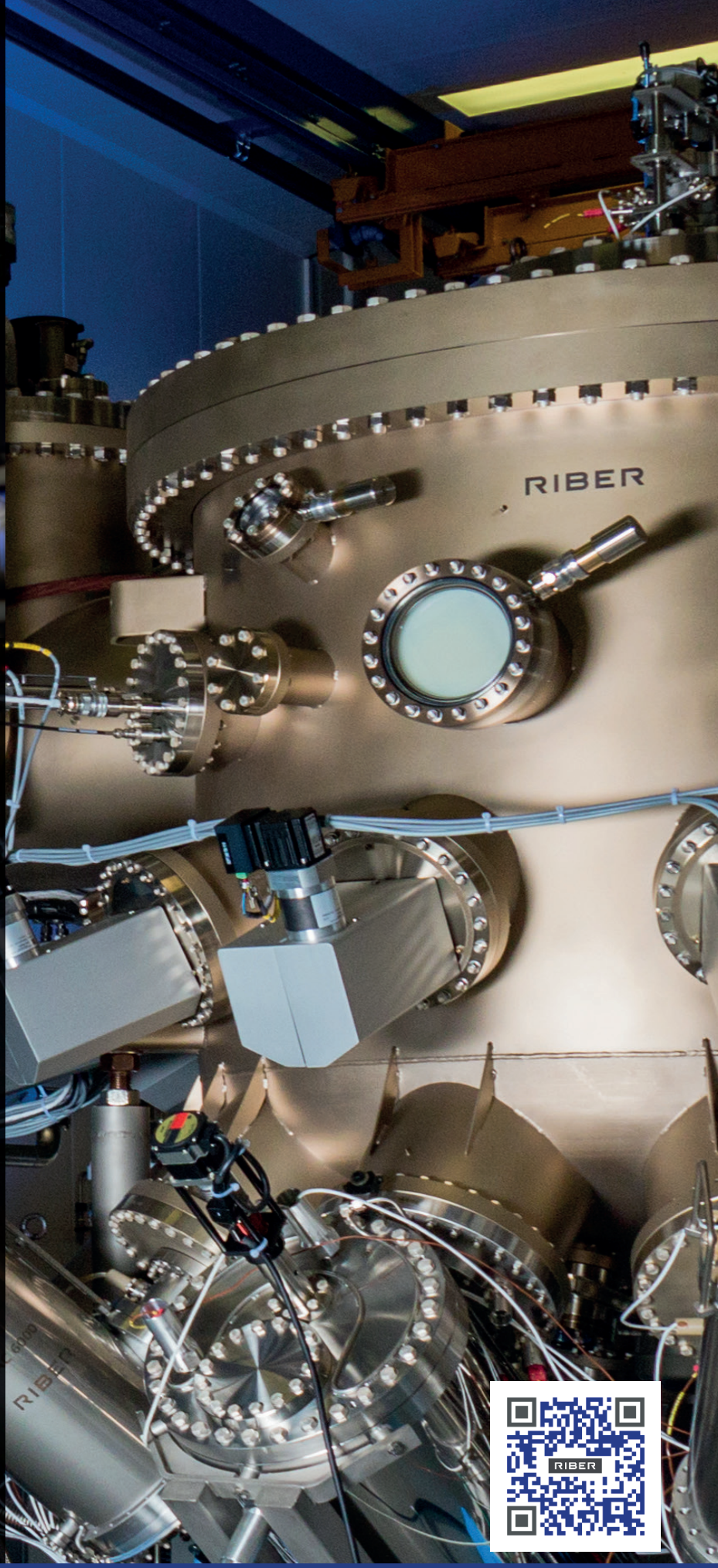

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