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VOLUME 32 ISSUE III 2026

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

GaAs PAs: Could the reign end soon?

IT'S EASY to assume that entrenched technologies will dominate forever. Surely telecom lasers will always be made from InP, light bulbs will always be powered by GaN LEDs, and the power amplifier for the smartphone will be made from GaAs.

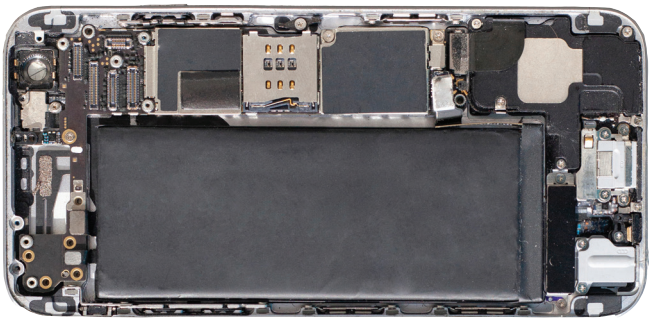
But for the latter, change may be on its way. Last year, in an exclusive interview with Pierre-Yves Lesaicherre, CEO of MIT spin-out Finwave, we reported claims that GaN could displace GaAs in the handset by 2030. And in the Research Review section of this edition, we detail efforts on that front by a collaboration between engineers at A*STAR, Nanyang Technological University and Soitec. This team has been developing a GaN-on-silicon HEMT that's a promising contender for serving in tomorrow's smartphones operating at millimetre-wave frequencies.

The GaN-on-silicon HEMT produced by this partnership combines an impressive performance with manufacturing advantages. While GaAs HBTs are made on native 150 mm substrates, GaN HEMTs could be manufactured in 300 mm silicon lines, using CMOS-compatible processes. This promises to deliver superior economies of scales, enabling a trimming of production costs.

Another advantage of the GaN HEMT over the GaAs HBT is its higher breakdown voltage. As well as aiding robustness, this could lead to a simplification of protection circuits.

The team's GaN-on-silicon HEMTs are produced using standard processes, and have the advantage of avoiding aggressive scaling – the gate length is 100 nm.

Measurements on these transistors have generated many impressive results, including a power-added efficiency of just over 62 percent, a linear gain of more than 11 dB, and



a minimum noise figure that's below 1.4 dB right across a frequency range spanning 10 GHz to 40 GHz.

Based on the latter result, GaN HEMTs could be deployed for low-noise amplification as well as power amplification. And if further work suggests that the GaN HEMT can also offer high-quality switching, there's the tantalising prospect of a monolithic transmit/receive module that will trim parasitics.

According to Qingyn Xie from A*STAR's National Semiconductor Translation and Innovation Centre for Gallium Nitride, efforts by the team with now be directed in three directions. One goal is to optimise the HEMTs for high performance at low voltage – and the other aims are to explore E-mode transistors, and to characterise the linearities of these devices.

With much still to do, it feels that GaAs HBTs could be the incumbent power amplifier technology in handsets at the start of the next decade. But will GaN HEMTs have taken over by the end of the 2030s? That one to keep a track on through the pages of this publication.

Stay tuned.

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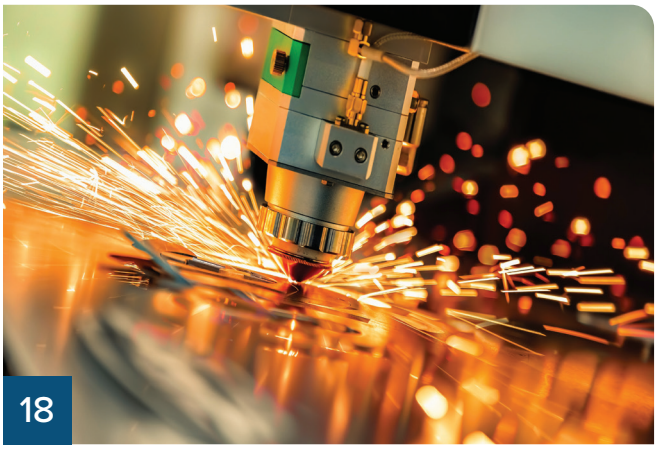

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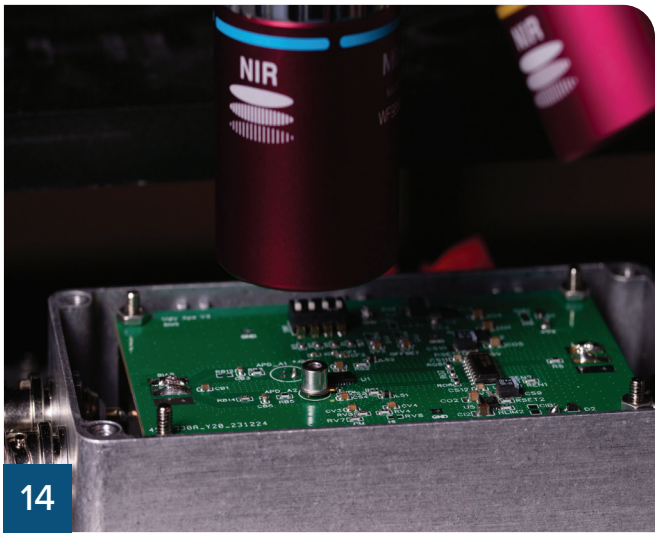

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6-inch InP fab begins construction in Eindhoven

€150 million European Chips Act investment is a “launchpad for Europe’s future digital economy”

THE NETHERLANDS ORGANISATION for Applied Scientific Research (TNO) and High Tech Campus Eindhoven are starting construction of foundry for producing InP photonic chips on a 6-inch wafer scale.

By connecting R&D with scalable production, the aim of this facility is to accelerate the path from concept to market-ready solutions for a new generation of energy-efficient AI data centres, 6G networks, medical innovations and supercomputers.

Tjark Tjin-A-Tsoi, CEO of TNO, said: “With this factory, TNO is taking a unique step: for the first time, we are building an industrial pilot line. By bringing research and manufacturing closer together, we strengthen the Netherlands’ position within the European semiconductor landscape and help companies scale-up high-quality photonic technology more quickly and efficiently. This is an investment in our technological strength and in future economic growth.”

The €150 million investment stems from the ambition of the European Chips Act. As part of the pan-European

consortium PIXEurope, the factory aims to ensure that the ‘brains’ of the future digital economy are developed and produced on European soil.

The project is a public-private partnership between TNO, TU/e, PhotonDelta, Smart Photonics, and High Tech Campus Eindhoven. In addition to technological progress, the factory will create high-quality jobs. After the initial ramp-up phase, around 40 specialists will be employed at the factory, a number expected to grow further.

According to Netherlands government adviser Peter Wennink, the impact of integrated photonics is comparable to the rise of integrated electronics decades ago: “By investing now in scalable production capacity, we are creating an ecosystem that can help shape the global technological direction. This is a launchpad for Europe’s future digital economy.”

Rohm to licence TSMC GaN technology

ROHM will integrate its own development and manufacturing technologies for GaN power devices with the process technology of TSMC.

By licensing TSMC GaN technology, Rohm says it will strengthen its supply capability to meet growing demand for GaN in applications such as AI servers and electric vehicles.

Rohm began developing GaN power devices at an early stage and established a mass-production system for 150 V GaN at Rohm Hamamatsu in March 2022. In the mid-power range, Rohm has built its supply structure while advancing external collaborations. One of the key partners in this effort has been TSMC: Rohm has adopted a 650 V GaN process since 2023, and in December 2024, the two companies entered into a partnership related to automotive GaN, further deepening their collaboration.

This latest integration represents an evolution of that partnership. Under a newly concluded license agreement, TSMC’s process technology will be transferred to Rohm Hamamatsu. Rohm aims to establish the production system in 2027 to meet expanding demand in applications such as AI servers.

Upon completion of the technology transfer, Rohm and TSMC will amicably conclude their automotive GaN partnership. At the same time, the two companies will continue to strengthen collaboration for higher efficiency and more compact power supply systems.

Nvidia to invest $4 billion in Lumentum and Coherent

Partnerships aim to grow capacity, advance US-based manufacturing and deepen R&D collaboration

NVIDIA has announced multi-year strategic agreements with two US photonics companies; Lumentum and Coherent. It will invest $2 billion in each company.

The aim is to accelerate innovation in advanced optics technologies, including research and development, to enable next-generation AI infrastructure and systems designs.

The non-exclusive agreement wth Lumentum includes an Nvidia multi-billion purchase commitment and future capacity access rights for advanced laser components. In addition, Nvidia is investing $2 billion in Lumentum to support R&D, future capacity and operations as the company builds out its US-based manufacturing capabilities in a new fab.

The non-exclusive agreement with Coherent includes an Nvidia multibillion-dollar purchase commitment and future access and capacity rights for advanced laser and optical networking products.

Nvidia is investing $2 billion in Coherent to support research and development, future capacity and operations as Coherent builds out its US-based manufacturing capabilities.

Optical interconnect technology and package integration are critical for the continued scaling of AI factories, improving the energy efficiency and resiliency of large-scale AI networks.

These expanded collaborationa will draw on the strengths of Nvidia's expertise in AI, accelerated computing and networking, with Lumentum's and Coherent's expertise in optics and manufacturing.

"AI has reinvented computing and is driving the largest computing infrastructure buildout in history," said Jensen Huang, founder and CEO of Nvidia.

"Together with Lumentum, Nvidia is advancing the world's most sophisticated silicon photonics to build the next generation of gigawatt-scale AI factories."

He added: "With Coherent, Nvidia is pioneering next-generation silicon photonics to enable AI infrastructure at unprecedented scale, speed and energy efficiency."

"This multiyear strategic agreement reflects our shared commitment to advancing the optics technologies that will power the next generation of AI infrastructure," said Michael Hurlston, CEO of Lumentum. "In support of this collaboration, we are also investing in a new fabrication facility to increase capacity and accelerate innovation. We're excited to work together to expand what's possible for the AI optical architectures of tomorrow."

"This strategic relationship underscores Coherent's role as a key enabler of next-generation AI data center infrastructure," said Jim Anderson, CEO of Coherent. "We are proud to expand our 20-year relationship with Nvidia by increasing their access to include multiple product families to help them build the AI data centers of the future."

> "This multi-year strategic agreement reflects our shared commitment to advancing the optics technologies that will power the next generation of AI infrastructure"

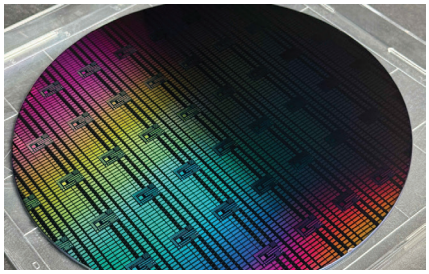
IVWorks nets $4.5 million to expand ‘reGaN’ market

Korean company targeting E-band/W-band RF applications in satcoms and wireless backhaul

IVWORKS, a Korean specialist in GaN epitaxial wafer technology, is accelerating its expansion into the GaN semiconductor market through its proprietary ‘reGaN’ technology while continuing to expand its core epitaxial wafer business across multiple advanced device platforms.

Using its epitaxy expertise, the company is positioning itself as a key provider for next-generation RF and power semiconductor applications, including AlN HEMT on SiC, GaN HEMT on silicon, and vertical GaN epiwafers.

To support this growth, IVWorks recently closed a funding round of approximately $4.5 million, bringing its cumulative investment to $33 million. The newly secured capital will be deployed to strengthen mass production infrastructure and stabilise the global supply chain, enabling a rapid response to growing



global demand for GaN materials and advanced epitaxial solutions.

The company’s ‘reGaN’ technology is built on its core selective-area regrowth capability for advanced GaN device integration. Recently, reGaN demonstrated commercial readiness and technical reliability by completing major foundry qualification and supplying qualified products to leading global semiconductor foundries. This solution directly addresses key industry challenges, particularly contact resistance reduction in GaN devices, significantly improving device performance and efficiency.

The technology is currently expanding into E-band and W-band RF applications for satellite communications and wireless backhaul, while also entering AI power delivery markets through PoL converters for advanced computing platforms, including high-bandwidth memory and GPU systems.

In parallel with this investment, IVWorks has initiated preparations for a KOSDAQ listing, with Korea Investment & Securities CO., LTD. serving as the lead underwriter. Young-Kyun Noh, CEO of IVWorks, stated, “This investment reflects our shareholders’ confidence in IVWorks’ technical roadmap. We remain committed to solving critical technical challenges for our global partners through reGaN while building a sustainable growth foundation through our planned IPO.”

Nuburu enters the counter-drone market

US semiconductor laser company Nuburu’s Italian subsidiary Lyocon has completed the proof-of-concept of a portable directed-energy laser dazzler platform designed for counter-drone (C-UAV) defence applications.

Counter-drone technologies have become a critical priority for defence agencies worldwide as the proliferation of low-cost ummanned aircraft systems (UAS) reshapes modern battlefield and security environments.

The Lyocon counter-drone system, built using Nuburu’s laser technology, is designed to generate optical interference capable of disrupting UAV sensors and visual systems.

Key technical capabilities include multi-wavelength directed-energy configuration with green, blue and

infrared laser bands. Scalable optical power output ranges from 1 W to 10 W, and advanced beam control includes adjustable beam divergence: 2.5 mrad to 30 mrad.

Lyocon has been technically validating the prototype with a large government-owned defence electronics company in its domestic market. Prototype trials have been completed and production-prototype trials have been successfully finalised. Paola Zanzola, executive director of Lyocon, commented: “The successful completion of the proof-of-concept confirms the robustness of the architecture we have engineered and the scalability of Lyocon’s directed-energy platform. Our objective has been to design a compact, modular system capable of delivering effective optical countermeasures against drone threats while maintaining portability and operational flexibility.”

Dario Barisoni, Co-CEO of Nuburu Inc. and CEO of Nuburu Defence LLC, added: “Counter-drone protection has become one of the most urgent priorities for defence forces and critical infrastructure operators worldwide. Lyocon’s portable directed-energy platform represents a highly adaptable non-kinetic C-UAV solution capable of protecting personnel, vehicles, and sensitive infrastructure from evolving UAV threats.”

Aixtron to build new plant in Malaysia

New location will include assembly & test, engineering support and local purchasing for South East Asian customers

AIXTRON, a supplier of deposition equipment for compound semiconductors, has decided to build a new manufacturing facility in Malaysia in order to tap into the fast-growing semiconductor equipment ecosystem in South East Asia.

The company aims to manufacture some of its 100/150/200 mm products in the new plant in the Penang region, mostly to address customers in Asia.

The new location will include assembly & test, engineering support and local purchasing capabilities. This will allow local assembly of some of Aixtron's products, and sourcing of many parts from the local supply chain of module and component makers.

Aixtron says the modular factory design allows for future expansion with little additional investment.

Dato' Loo Lee Lian, CEO of InvestPenang, said: "Aixtron's decision to build a new facility in Penang underscores our region's growing reputation as a premier destination for advanced technology investments.

> "Overall, this represents a clear growth step for us, strengthens our position in the Asian market. We remain dedicated to our European locations in Herzogenrath, Germany, and Cambridge, UK"

This new facility highlights Penang's attractiveness as a strategic hub for innovation and manufacturing, reflecting the company's confidence in our highly skilled workforce and favourable business environment."

Felix Grawert (pictured above), CEO of Aixtron said: "Overall, this represents a clear growth step for us, strengthens our position in the Asian market. We remain dedicated to our European locations in Herzogenrath, Germany, and Cambridge, UK. Both locations are central pillars for research, development, and also production, especially due to many strong and specialised suppliers. The plant in Malaysia complements the strengths of the existing locations and allows to leverage 'the best of both worlds' by adding access to the South East Asia supply chain. No personnel reduction is planned in Europe as a result of this".

The capex for the new site is estimated at around €40 million, to be spent in H2/2026 and H1/2027. The plant is expected to start operation in the spring of 2027, with first shipments expected in the second half of 2027. The start-up costs expected in 2026 in connection with preparing for production will not affect the forecast for fiscal year 2026.

QuinAs links memory device physics to AI performance

New research highlights UltraRAM's potential as a compact, energy-efficient platform for future AI hardware.

QuInAs Technology, the UK developer of the compound-semiconductor memory technology UltraRAM, has published new research in the *Journal of Applied Physics* that links device-level physics directly to AI system performance.

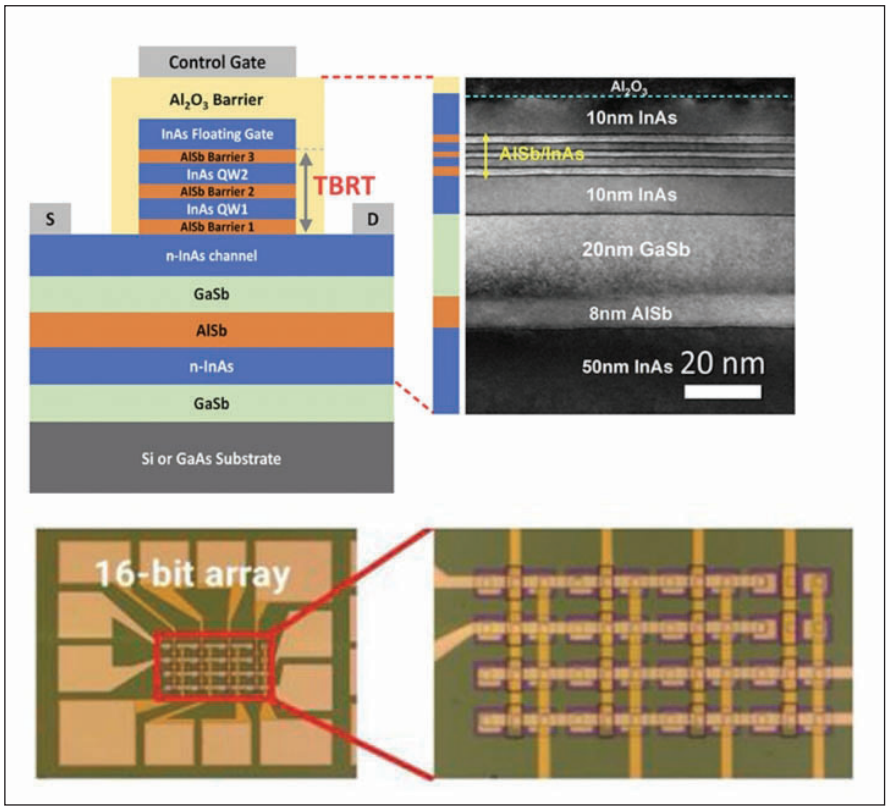
The paper *Artificial synapse based on UltraRAM memory device for neuromorphic applications* uses compact modelling and hardware-aware benchmarking to address a key limitation in how emerging memory technologies are typically evaluated. It demonstrates how UltraRAM can be modelled and evaluated as a synaptic memory element for next-generation AI hardware.

The company presented this work at the International Symposium on Quality Electronic Design (ISQED) 2026, in San Francisco from 8-10 April, focussing on system integration and design considerations, bringing ULTRARAM into the electronic design automation and system design community.

Developed in collaboration with IIT Roorkee and Lancaster University, this new research introduces a physics-based compact modelling framework that links device-level behaviour – including resonant tunnelling and floating-gate charge dynamics – to circuit- and system-level performance.

This enables, for the first time, hardware-aware evaluation of UltraRAM in neuromorphic and in-memory computing architectures, using crossbar array simulations and DNN+NeuroSim benchmarking on tasks such as CIFAR-10 classification.

"Much of today's AI hardware research evaluates memory technologies under idealised assumptions," said James Ashforth-Pook, CEO of QuInAs Technology. "This work takes a different approach – connecting real device physics directly to system-level performance. That's essential if we are to build practical, energy-efficient AI systems."



The research shows that UltraRAM can achieve competitive accuracy while offering advantages in energy efficiency and area compared to conventional SRAM-based approaches, highlighting its potential as a platform for future AI hardware.

> QuInAs Technology, the UK developer of the compound-semiconductor memory technology ULTRARAM

Lead author Abhishek Kumar added: "By integrating physics-based modelling with system-level benchmarking, we can better understand how emerging memory technologies behave in real AI workloads, rather than relying on idealised models."

UltraRAM is based on III-V compound semiconductor heterostructures and leverages resonant tunnelling to enable ultra-low energy switching and long data retention, positioning it as a candidate for neuromorphic and in-memory computing applications.

Audi Q3 now comes with adaptive projection lighting

Ams Osram EVIYOS HD25 lighting delivers adaptive illumination and driver feedback while enhancing road safety

THE NEW Audi Q3 is equipped with Ams Osram's EVIYOS HD25 pixel-based microLED lighting solution, delivering a higher level of adaptive illumination and driver feedback while enhancing road safety.

"EVIYOS represents a paradigm shift in automotive lighting, from passive illumination to active, data-driven light communication," says Sylvia Weise, senior product manager at Ams Osram: "By integrating this technology into the Audi Q3, we are enabling a new class of compact vehicles to deliver premium-level safety and user interaction through light."

EVIYOS HD25 is a fully digital, high-resolution lighting solution comprising a matrix of over 25,000 individually addressable pixels. This architecture is designed to enable the precise, real-time modulation of the light distribution pattern based on sensor input, vehicle dynamics, and environmental conditions. The system supports both static and dynamic projections, allowing for context-aware visual communication between the vehicle and its surroundings.

Light-guiding functions like lane and orientation lights are now more closely linked to driver assistance systems, projecting key information directly onto the road to enhance safety. New features include visual warnings from the lane change assistant in the lane light when a vehicle is in the blind spot, lane departure indications, and an ice warning symbol projected at speeds above 70 km h^{-1} (43.5 mph).

In construction zones, the digital matrix LED headlights automatically switch from lane light to orientation light to simplify staying in one lane in narrow areas. Drivers can deactivate functions like lane lights individually via the Audi MMI, and choose between three extended coming-home or leaving-home light designs. Combined with the microLED light source, the digital Matrix LED headlights offer highly precise high-beam distribution and improved glare control, enhancing overall road safety.

First real-world demo of PCSEL-based free space optical comms

Vector Photonics and Fraunhofer UK prove the practicality of PCSEL technology for secure, long distance, fast communications

VECTOR PHOTONICS, a Scottish start-up pioneering the use of photonic-crystal surface-emitting lasers (PCSEL) in secure communications, has announced the first successful public demonstration of PCSEL technology for optical communication outside of a lab.

On 31st March 2026, Vector Photonics' PCSELs were used to transmit data across the river Clyde from the Glasgow Science Centre to the Clydeside Distillery, using a system designed and built by Fraunhofer UK.

Richard Taylor, CEO and Founder of Vector Photonics said: "This is a major step forward for Vector Photonics, proving that our technology is a commercial reality in real-world applications. We believe that the demo is the most advanced application of a PCSEL to date, advancing it from a Technology Readiness level (TRL) of 4/5 to 6/7."

Employing the technology in open space means that it can perform successfully under different environmental conditions – temperature, humidity, precipitation, wind turbulence – and over a considerable distance. Previously, only lab experiments using ideal conditions and simulations, have been attempted.

PCSELs are a new type of laser, combining the high power of edge-emitting lasers with the speed and surface emission of VCSEL. They are highly advantageous for secure, free-space optical communication systems due to their ability to emit narrow, high-brightness beams with excellent beam quality and low divergence, which is critical for minimising signal loss over long distances.

Unlike conventional laser sources, PCSELs combine the benefits of surface emission with coherent, single-mode output, enabling efficient coupling into free-space optics without the need for complex beam-shaping elements.

These properties position PCSELs as a next-generation laser source for compact free-space optical communication systems and the Vector Photonics' breakthrough will enable faster, secure internet connections between buildings, campuses, and even satellites, without relying on cables or radio signals.

With its wide wavelength flexibility spanning ultra-violet to far infra-red, PCSEL technology can also be applied to AI data centres, lidar systems and additive manufacturing (3D printing).

The free-space optical communication system was designed and constructed using Vector Photonics' PCSELs by Fraunhofer Centre for Applied Photonics, part of Fraunhofer UK.

Data transfer at 50 Mb s^{-1} was demonstrated over 500 m, with error rates below standard forward error correction thresholds. This was twice the system spec required for the experiment, but well below the figure achievable by PCSELs, which have a naturally high data rate.

Gerald Bonner, principal Researcher at Fraunhofer CAP, said: "This project has been a great opportunity to deploy Fraunhofer CAP's capabilities in the development of optical systems to assist Vector Photonics in demonstrating the growing maturity of PCSELs and the potential of this important new diode laser technology in optical communications."

Pictured above: Richard Taylor, CEO and founder of Vector Photonics, with the PCSEL and optical communications system at the successful demo across the River Clyde.

Rio Tinto invests in Supra for gallium and scandium recovery

Investment will enable Supra to commercialise its modular critical mineral recovery technology

US START-UP Supra Elemental Recovery has announced an investment from Rio Tinto and Founders Factory through their mining technology accelerator.

The investment, structured as a combination of cash and in-kind services, will enable Supra to build and commercialise its modular critical mineral recovery technology with support from Rio Tinto. Supra is initially focused on gallium and scandium, two elements vital to the semiconductor industry that the US is currently 100 percent import-dependent on, with China dominating the critical minerals market.

Supra pumps waste through proprietary, reusable, sponge-like cartridges that selectively capture and release the minerals in sequence, with the potential to recover billions of dollars worth of critical minerals that are trapped in domestic waste streams. Compared to incumbent refining methods, Supra's approach is said to enable 100 times greater selectivity and speed, enabling higher purity and lower costs, according to early test results. The technology is also said to be non-toxic.

Supra was selected as one of six start-ups globally from more than 500 applicants. The cohort is focused on advancing exploration and processing technologies to meet growing demand for materials such as copper, lithium, and critical minerals.

Supra joins Foresight Spatial Labs (Ottawa, Canada), Chemshift (Calgary, Canada), Material Difference (Cambridge, UK), Voluna (Boston, US), and Watergenics (Berlin, Germany).

Jordan Sessler, co-founder and COO of Supra, said: "We look forward to working closely with Rio Tinto and leveraging the firm's global expertise to accelerate our path to commercial deployment. We look forward to recovering high-purity elements from complex streams, including ore, tailings, and byproducts."

Rio Tinto and Founders Factory join Supra's existing pre-seed investors, including Crucible Capital, Climate Capital, Portmanteau Ventures, and UT Seed Fund. The funding will support continued technology development and preparation for commercial pilots.

Polar Light Technologies wins €1.1million EU grant

POLAR LIGHT TECHNOLOGIES, a Swedish maker of microLED and nanoLED technology, has been awarded an EU Eurostars grant.

The 18-month project, named 2ndGenmicroLED, aims to deliver the world's first dual-colour microLED microdisplay prototype built on a bottom-up pyramidal LED architecture and has a total budget of €1,100,000.

German die bonding leader Finetech GmbH & Co. KG joins the consortium, contributing its expertise in high-accuracy die attach and advanced packaging.

The project responds to a rapidly growing need for smaller, brighter, and more energy-efficient microdisplays for next-generation Head-Up Displays (HUD) and spatial computing platforms.

"Securing this EU grant is a strong endorsement of Polar Light Technologies and our next-generation microLED platform," said Oskar Fajerson, CEO of Polar Light Technologies. "The Eurostars funding validates both the scientific excellence of our bottom-up pyramidal technology and its commercial potential. With this support, we will accelerate development toward a dual-colour demonstrator – a critical milestone on our path to monolithic RGB microdisplay."

"Next-generation microdisplays demand extreme bonding accuracy," said Carlotta Baumann, CEO of Finetech. "Finetech brings its ultra-precise bonding expertise to integrate dual-colour microLEDs and ensure a seamless transition from prototype development to scalable production."

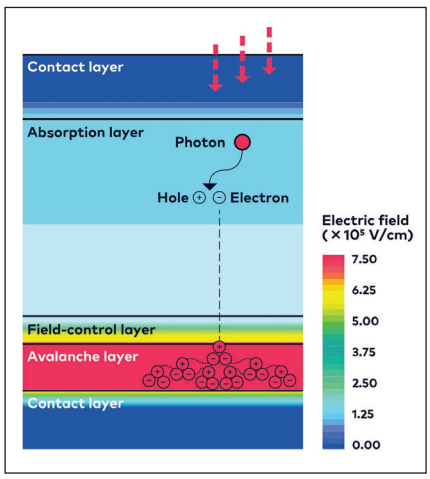
Antimony addition advances the APD

Phlux's award-winning APDs feature an AlGaAsSb multiplication layer that delivers a step-change in sensitivity

With compound semiconductor devices, there's no doubt that the devil is in the detail. Incremental changes to just one layer can be a game-changer – shifting emission to hit the target wavelength, boosting mobility to record levels, or enabling countless electrons to leak away, or the dislocation density rise to damaging levels.

When it comes to the avalanche photodiode (APDs), a device that dates back to the 1970s and has undergone minimal revision over most of that time, a hike in performance is now being realised by one start-up, UK-based Phlux, through a modification to the crucial multiplication layer. Out goes InP, and in its place a quaternary containing antimony.

That's the only significant change to the APD, a class of detector deployed in optical communication networks, lidar systems, and optical test equipment. This device absorbs incoming photons in an InGaAs layer, with the resulting electron-holes pairs swept into a multiplication region, traditionally made from InP, where the electrical signal is amplified through a process known as impact ionisation.



➤ The structure that produces an internal gain mechanism in an avalanche photodiode.

As APDs are deployed in low-light applications, the signal must be amplified – but this comes at a price, as noise increases more than the signal in traditional devices.

To address this issue, much effort has been devoted to developing a superior methodology for amplifying these very weak signals. Alternative approaches include the introduction of complex 'staircase structures' that manipulate the journey electrons take through the device. But this has delivered limited success.

That's not the case for Phlux's ground-breaking technology. This spin-out of the University of Sheffield, founded in 2020, is now grabbing headlines for impressive product specifications and a coveted industry award.

According to company CEO and co-founder, Ben White, critical to success has been the search for new materials with properties ideal for multiplication.

He is a humble man, freely admitting that they stumbled on using antimony-based materials, specifically AlGaAsSb, a quaternary he describes as having really weird properties.

"The electrons within the conduction band can multiply quite readily, whereas the holes within the valence band are really heavy and very, very sluggish," says White. What's more, the holes struggle to get enough energy to reach the split-off band, where they would multiply.

Thanks to the introduction of AlGaAsSb in the multiplication region, Phlux's APDs provide a sensitivity that's an order-of-magnitude higher than the incumbent. This level of superiority ensures a higher signal-to-noise ratio and ultimately allows adopters of this device to produce products with better specifications, such as lidar with an increase range and test equipment with a lower noise floor.

A second chance

White has spent many years developing Phlux's technology, initially investigating AlGaAsSb technology with the company's other co-founders – the University of Sheffield academics Jo Shien Ng and Chee Hing Tan – when a PhD student between 2012 and 2016, and then following 18 months of travelling, working as a research associate.

Soon after his return to the lab, the team published a high-impact paper on the use of AlGaAsSb in APDs.

Previously, when Tan and co-workers realised similar academic success with a different material system, they patented their work and waited for a company to license and commercialise their exciting technology. But that never happened. It is this a painful experience that the team learnt from, vowing to not to let another opportunity slip through their fingers.

This time the team would take control of its destiny. To White, this makes a lot of sense: "We know more about this technology than anybody, and we're

really excited about it for what it can do for the world. We should be the ones that do this."

At that pivotal time, White could afford to take the personal risk of pursuing this dream, and with the support of his two co-founders, convinced Sheffield University to back them with a small investment.

The Royal Academy of Engineering also played its part, helping to assist the first steps to commercialisation by providing White with an Enterprise Fellowship.

For the first two years, Phlux focused on technical milestones. Could they build a working device? How would the dark current change with the introduction of antimony? What about reliability?

After tackling all these challenges, Phlux produced a product, netted its first sale, and then secured a number of commercial design wins.

Underpinning all this progress was the securing of substantial funding, a task that's not been easy for III-V chipmakers, according to White.

In his experience, investors can be put off by deep-tech, and semiconductors in particular, due to lengthy design cycles. He says that a few years' ago, start-ups focusing on software-as-a-service had far more appeal, although now there are concerns that the plans of these companies can be disrupted, unless they scale to a substantial level.

Very recently, interest in photonics has risen, due to the rise of AI and increased demand on data centres, which are switching from electrical to optical signals. "I think the awareness of photonics, and potential impact of it, is now much bigger than it's ever been before," enthuses White.

It's a state-of-affairs that did not exist in 2022, and White is grateful for the investors that understand the optoelectronics space, and provided £4 million that year to fund the development of the first product. This time last year Phlux raised another £9 million to scale the technology, and penetrate new markets.

➤ Laser rangefinders provided early demand for Phlux's high sensitivity avalanche photodiodes. The components deliver much-improved performance, including an extended range.

As well as commercialising its technology, funding has enabled the expansion of the team, which has evolved from just those with technical expertise to those that offer other skills, such as operational experience, marketing and finance. Headcount is forecast to grow by another five or six this year, taking the team to around 30 staff.

Initially, Phlux drew on the expertise of the UK III-V National Facility, located within the heart of Sheffield, for the fabrication of its APD epiwafers. Today this supports R&D, but production is outsourced, with Phlux a fabless entity that has partners providing growth, processing and packaging.

However, at the start-up's headquarters, which occupies around 3,500 ft^2, there's more than desks and computers. There's also a cleanroom and an engineering lab, used for what's described as 'look-ahead testing.'

"When you do the full range of reliability testing, you need some very specialised equipment," explains White. While Phlux does not have that capability, it is able to gauge how a batch of devices is performing, as well as investigating variations in characteristics and undertaking quality assurance.

The facility is also used to produce products that combine an APD with a low-noise amplifier, which is critical to getting the best performance from this detector.

As it's a challenge to grow epitaxial structures with quaternary layers, this is a key element of Phlux's IP. "But just as much IP is now in the fabrication as in the growth," says White, who points out that it's far from easy to progress from making one working APD to millions of them.

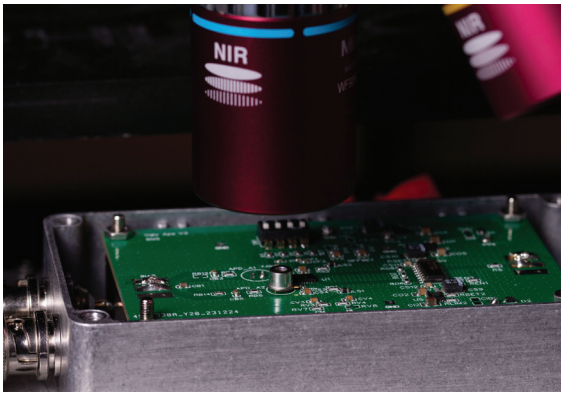
Multiple markets

As Phlux' founding coincided with what White describes as a peak-hype cycle for autonomous vehicles, the company initially pursued the lidar market. But when that promise failed to fully materialise, and competition for short-range applications intensified, they adopted the traditional approach for a start-up, focusing on high-value, lower-volume applications. They are related to defence, sensing, test equipment, and next-generation lidar.

Today, White views the communication industry as the biggest potential market, but also sees a great, longer-term opportunity in robotics, due to the high level of integration required to build products.

Crucial to success is raising the profile of the company, an objective that will be helped by the winning of a Prism Award, which White refers to as the Grammys for the photonics industry.

"We genuinely did not expect to win up against companies like ams Osram. But it was an amazing reflection on the success of the team over the last few years, and the great opportunity that we have for us at Phlux."



➤ Phlux Technology has invested in in-house facilities for APD performance testing and quality assurance.

Vexlum: Expanding VECSEL production capacity

To ramp production of its VECSELs for the quantum tech industry, Finish start-up Vexlum is investing in its cleanroom, including the addition of an MBE tool

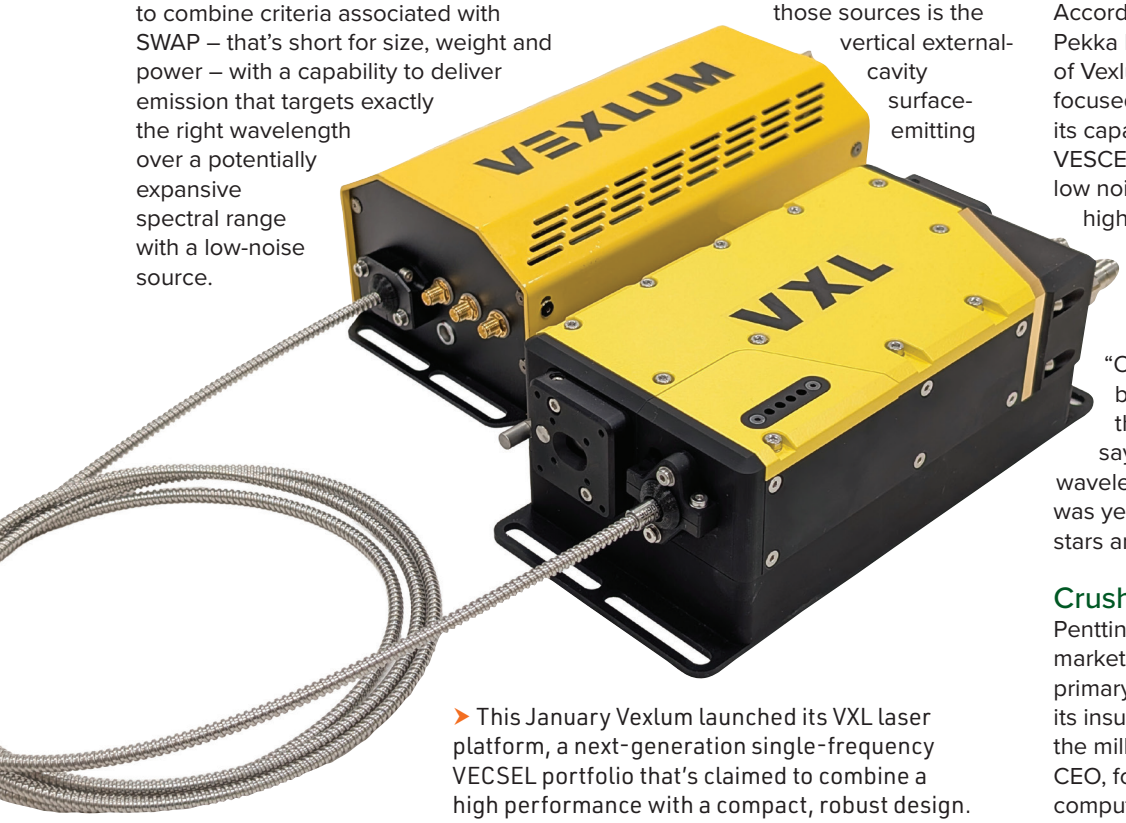
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

When designing any product, there's a lengthy wish list one needs to try and address. Often versatility and accuracy of its output will be favoured, along with robustness, compactness and competitive pricing. But it's impossible to excel on all these fronts, so compromise is inevitable. This poses the crucial question: What factors really matter?

It's a dilemma at play for those that are looking to serve the quantum tech industry with lasers for pumping atomic transitions. They will want to combine criteria associated with SWAP – that's short for size, weight and power – with a capability to deliver emission that targets exactly the right wavelength over a potentially expansive spectral range with a low-noise source.

That's a tough set of criteria to fulfil. So, in situations where size and weight are not a deal breaker, one can consider cumbersome, complex contraptions, involving multiple boxes that may house a combination of seed sources, amplifiers, frequency-doubling cavities and locking electronics. But if a compact source tops the agenda, makers of VCSEL will sense an opportunity – although it's not easy to produce this laser with an emission that matches a particular atomic transition.

Offering an attractive alternative to both those sources is the vertical external-cavity surface-emitting laser (VECSEL). It's a source that employs a laser diode, used to pump a semiconductor gain chip that's positioned in a cavity formed by two mirrors, made from stacks of alternating III-Vs with different refractive indices.



➤ This January Vexlum launched its VXL laser platform, a next-generation single-frequency VECSEL portfolio that's claimed to combine a high performance with a compact, robust design.

One of the pioneers of the VECSEL is Vexlum. Founded in 2017, this spin out of the University of Tampere has just raised €10 million to increase VECSEL production, in response to increasing global demand for optical sources for atomic clocks and quantum computing.

According to company CEO Jussi-Pekka Penttinen, the unique strength of Vexlum, which is the only company focused on just producing VESCELs, is its capability to make single-frequency VESCELs with a narrow line width, very low noise, excellent beam quality, and high power across the visible range. That includes wavelengths that are difficult to access with other classes of laser.

"Our company colour is yellow, because I'm sure you know there's this famous yellow gap," says Penttinen. "One of the first wavelengths we made at the university was yellow – lasers for sodium guide stars and then dermatology."

Crushing the competition

Penttinen says that for the quantum markets Vexlum is now targeting, the primary rival is not the VCSEL, due to its insufficient power that's is limited to the milliwatt range. According to the CEO, for applications such as quantum computing, output powers of several

watts are needed, with more power enabling the pumping of more atoms. Due to this, competition comes from large, complex laser systems, such as amplified diode lasers, frequency-doubled diode lasers, and frequency-doubled fibre lasers.

"Seeing the roadmaps of these quantum companies, it's no longer viable to make very large laser systems, because you would start to fill factories with just lasers," says Penttinen.

There are also concerns regarding the energy consumption of these large laser systems. Due to this, Vexlum's watt-level lasers are "very tempting", says Penttinen, as they are just a few litres in size, so roughly one-tenth that of the competition.

With the VESCEL, dimensions are determined by cavity length and mode size. Consequently, advances in engineering and electronics can drive reductions in volume – a trajectory Vexlum is pursuing.

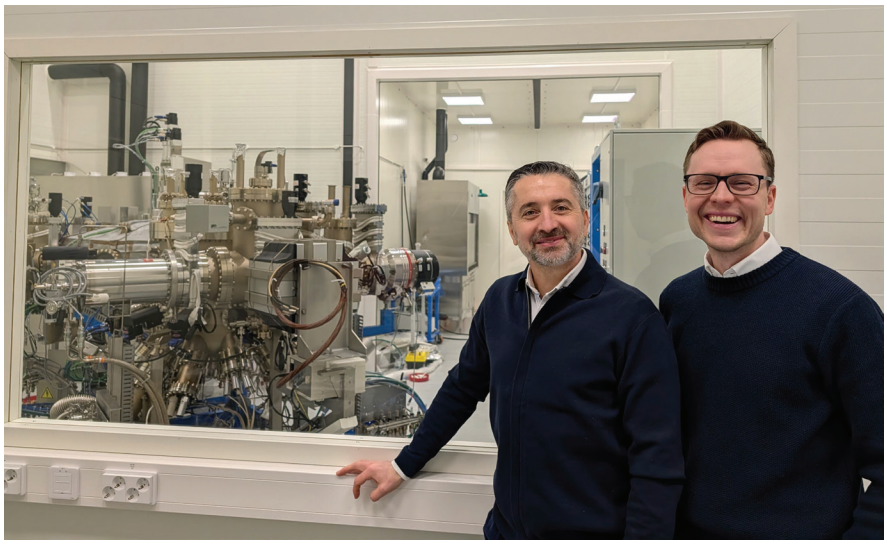
Another attribute of Vexlum's VECSELs is the quality of their emission. Thanks to the combination of surface-emitting gain and an external cavity, optical output has a very low linewidth and minimal noise. And wavelength tuning is available: "Our lasers can be frequency locked to the target using the cavity piezo, with an inter-cavity electro-optical modulator."

From the deep UV to the IR

A key competency of the Finnish start-up is its capability to span a vast spectral range, by drawing on a variety of semiconductor gain chips based on quantum-well emission. Using the GaAs material system, Vexlum covers 700 nm to 1.3 μm; and switching to InP and GaSb increases the upper end to 1.7 μm and 2.2 μm, respectively. Meanwhile, frequency doubling extends the emission down to 350 nm.

On the one hand, gain chips are difficult to grow, as they contain many tens of epilayers; but they are free from doping.

"I often joke that if you can grow a quantum well, you can always make a VECSEL, but you cannot always make a diode laser, because doping is often more complicated," remarks Penttinen.



Vexlum's CEO, Jussi-Pekka Penttinen (right) with Executive Chairman, Chief Scientific Officer and academic at the University of Tampere, Mircea Guina (left).

When considering this remark, it's important to be aware that Vexlum is drawing on two decades of experience in developing gain material. "We can make new wavelengths within weeks that could take someone else twenty years," says the company CEO.

Penttinen has been involved in the development of Vexlum's technology for many years. Initially inspired by a news article detailing efforts at the Optoelectronic Research Centre at the University of Tampere, he took a summer internship in 2010, before switching to a full-time role. During his initial interview, he remarked that he would like to play a role in a start-up emerging from the Optoelectronic Research Centre, a dream now fulfilled as co-founder and CEO of Vexlum, where he leads a team of around 40.

The first whiff of commercial potential came in 2012, when quantum researchers at NIST in Boulder got in touch, explaining that they needed a laser emitting at around 1.1 μm for magnesium-ion trapping.

"We found out, together with the quantum researchers at NIST, that VECSEL technology is very good match, because of the wavelength versatility, noise, power and beam properties, and also the intra-cavity doubling."

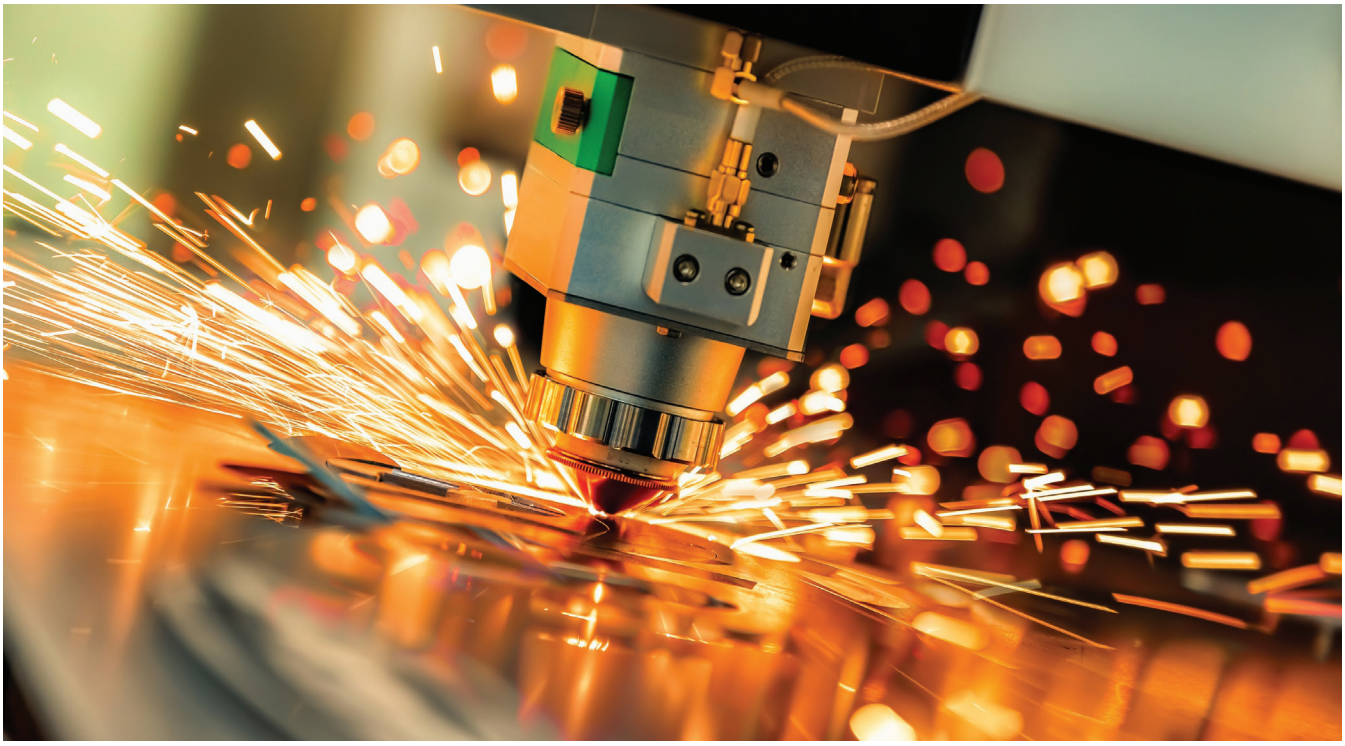
This helped spur the founding of Vexlum in 2017, when interest in quantum was far less than it is today – so much so that the university's innovation service warned Penttinen that the target markets were 'too niche'. Fortunately, he did not heed this advice. Vexlum sold its first laser in 2019, and hundreds more since then. Sales will continue to climb, and the aim is to double production capacity every year.

Today Vexlum rents space from Tampere University, which has five MBE tools and an extensive cleanroom. The €10 million of seed funding, coming primarily from Nordic investors, will be used to complete Vexlum's own cleanroom, with equipment that includes an MBE tool.

Part of the reason for using this epitaxial technique is that it reflects the company's expertise. However, Penttinen argues that MBE is also more versatile than alternative forms of epitaxy for producing gain chips spanning a very wide spectral range.

With its own MBE tool, Vexlum will benefit from increased capacity, allowing the company to expand on many fronts.

"Quantum is certainly our starting market," says Penttinen, but there are also opportunities in markets using older laser technologies, such as gas lasers. "We are already providing prototypes [there]," adds Penttinen, who is sure to play a key role in expanding the deployment of the VECSEL in many applications.



Diode improvements drive fibre laser growth

Thanks to a Moore's law rate of improvement in the bang-per-buck of GaAs diode lasers, cleaning and heating join a growing list of fibre laser applications

BY TOBY STRITE FROM IPG PHOTONICS

A PRIMARY USE of high-power GaAs lasers is the processing of material. Sales of material processing systems based on lasers now net more than $23 billion per year, with more than half that revenue inextricably linked to GaAs and silica fibre through the industrial fibre laser. Thanks to fibre lasers, the laser marking, cutting and welding of metals has entered the mainstream. This has spawned billion-dollar markets, with fibre lasers providing a cost-effective, reliable platform around which automation and metrology will increasingly simplify the displacement of legacy solutions.

Underpinning the success of the industrial fibre laser is the substantial investment in this technology by the telecom industry during the 1990s. Progress provided a foundation for the first high-power industrial fibre lasers in the early 2000s – and from there, in just ten years, and propelled by advances in GaAs diode performance, fibre became the dominant industrial laser, supplanting CO_2 and Nd:YAG lasers as the platform of choice for marking, cutting and welding.

To understand this transformation, it's helpful to consider a metric that captures industrial laser productivity: the $/Watt at acceptable reliability. It's a yardstick that places a premium on laser power, which is commonly synonymous with the process speed when thermally treating metals. A 2 kW laser can generally mark, cut or weld in half the time of a 1 kW laser, and increased power often holds the key to deployment in new applications, such as the ability to cut or weld thicker or shiny metals.

When explaining the expanding success fibre lasers, one should note that they are composed almost entirely of passive optical components, so performance and cost are largely dictated by GaAs-based pump laser components. As GaAs diodes are manufactured in capital-intensive fabs, their performance, economics and quality are subject to the same virtuous cycle as silicon integrated circuits. So, it's not surprising that over the last 40 years diode laser advancements have kept pace with Moore's Law (see Figure 1), enabling their value proposition to improve by a factor of 100 every 15 years. GaAs diode practitioners have every hope and intention this trend will continue into the future.

Prior to the uptake of fibre lasers for material processing, early adopters employed gas or solid-state lasers for high-value applications inadequately addressed by legacy processes (see Figure 2, which qualitatively depicts legacy and fibre laser introduction into metal material processing). Regardless of the specific application – either laser marking/serialisation, flat sheet cutting, welding or cleaning – introducing fibre lasers caused a market inflection, spurring hypergrowth that led to the emergence of billion dollar markets for marking, cutting and welding.

Examples of this migration include the introduction of pulsed nanosecond fibre lasers with output powers of around 10 W, which began a long cycle of Nd:YAG laser displacement for metals marking, beginning in the mid 1990s. There's also the rise of kilowatt fibre lasers, initiating the displacement of CO_2 gas lasers and other incumbent techniques for sheet-metal cutting in the mid-2000s; and the introduction of quasi-CW fibre lasers in the early 2010s, providing a superior alternative to flashlamp-pumped Nd:YAG lasers for welding. More recently, in the mid-2010s, hundred watt-class nanosecond pulsed fibre lasers started to displace Nd:YAG lasers for cleaning.

In all cases, the availability of the fibre-laser platform, which delivers performance and economic benefits, has created an inflection point. That's provided a starting point for continuous improvement in fibre laser capability, which propels hypergrowth and mass adoption.

While the laser now dominates metals marking and cutting, today laser welding comprises just 20-25 percent of the welding systems spend. This provides an opportunity for growth in laser welding that outstrips GDP, while mature marking and cutting applications are expected to grow at a rate closer to GDP.

As well as these revenue streams, on the horizon is the exciting potential of fibre lasers to impact global markets for cleaning and heating solutions, worth more than $100 billion per annum.

There are many opportunities for fibre lasers that are related to cleaning. Through multiple mechanisms (see Figure 3), fibre lasers can remove foreign materials, such as oils, lubricants or light oxidation from a metal surface, while utilising less time, energy and consumables compared with traditional abrasive and chemical processes.

One clear advantage laser cleaning has over rival approaches is that by selective heating at the metal surface, there's no need to treat the entire part. And another benefit comes from adjusting the laser power: at high doses, the laser energises a thermal phase transition, vaporising foreign materials; and more elegantly, at lower doses, contaminants that are weakly

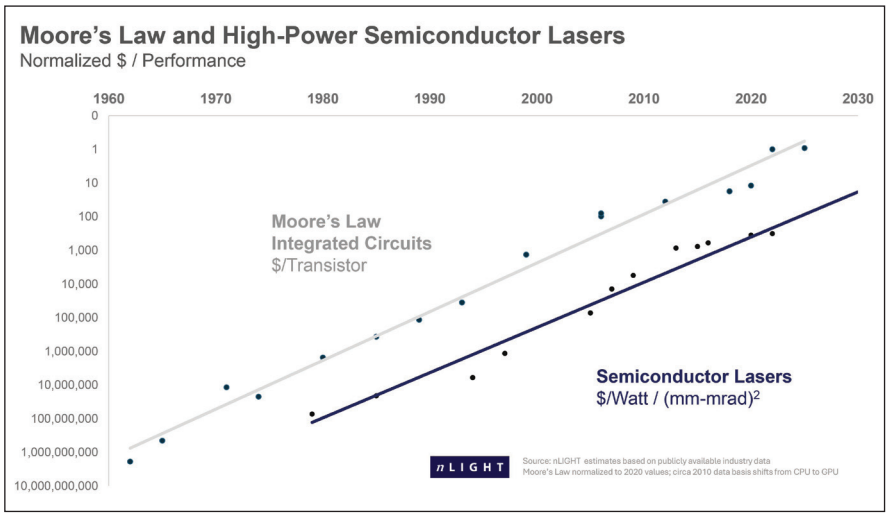


Figure 1. GaAs diode performance improvement over more than 40 years of mirrors Moore's law. Reproduced with permission from Scott Keeney, nLIGHT, Inc.

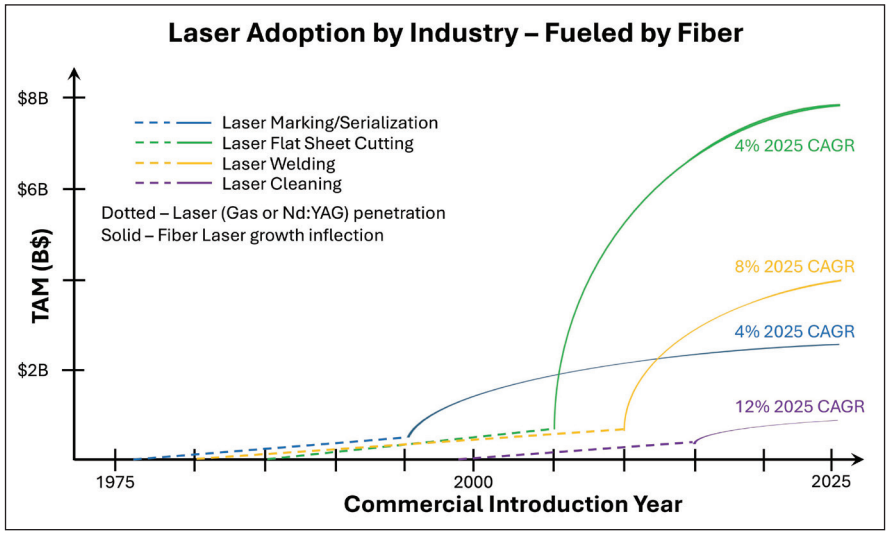


Figure 2. Laser adoption trajectories in major metal processing applications.

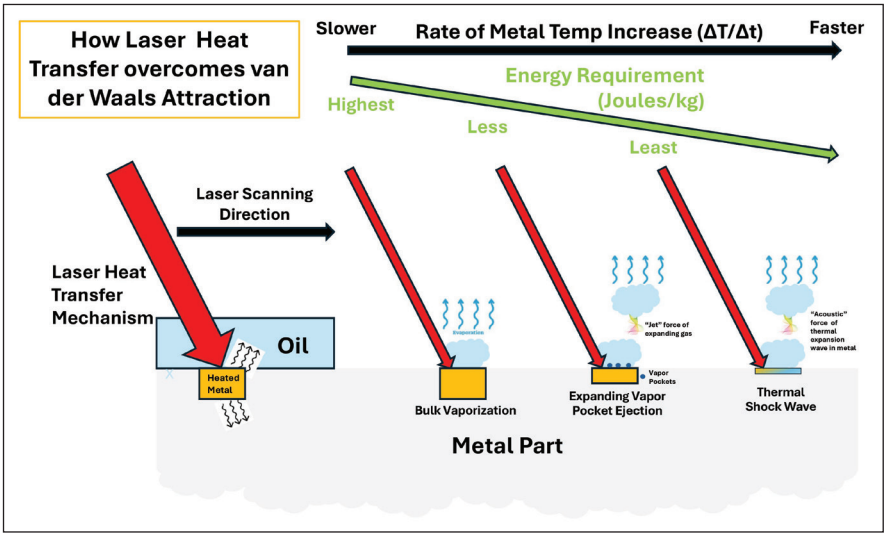


Figure 3. Dose dependent degreasing recipes range from bulk vaporisation (brute force) to elegant, more energy efficient cleaning utilizing high rates of localised heating.

bonded via van der Waals forces can be separated from the substrate through energy-efficient ejection mechanisms, driven by high rates of localised heating. Currently, laser cleaning amounts to much less than 1 percent of the available cleaning market, but it's growing at a double-digit rate, indicating that the fibre laser inflection has already occurred.

Recently, projecting kilowatt lasers over large surfaces, such as several square metres, has demonstrated their utility for curing/drying industrial coatings and for heating silicon wafers. For these tasks, lasers rely on leverage gained by selective heating. For example, heating a layer of paint, but not the part beneath it in a 'cold oven' configuration (see Figure 4), saves cost by slashing process time and energy consumption.

An intuitive way to appreciate the game-changing potential of laser heating is an analogy to American Thanksgiving. For those of us that mark this occasion, turkeys will sit in a convection oven for hours, to no good effect, until the final hour or so when the bird reaches temperature, and cooking finally commences. The superior alternative – rapid, surface-selective heating provided by lasers – allows an industrial coating, curing or drying process to commence almost instantaneously. For throughput-obsessed industries, such as chip making, the ability to slash unproductive process time by rapidly heating a silicon wafer to temperature is invaluable.

At just a few million dollars in annual sales, large-area laser heating is in its infancy. But, applying the lessons of history, if we turn the clock forward by 15 years and anticipate ongoing improvement in GaAs diode laser performance, we can rightly expect laser cleaning and heating to be mainstream applications in the 2040s, commanding substantial portions of the laser material processing marketplace.

In a follow-up article, published in the next edition of CS magazine, Toby Strite will describe the opportunities for laser-based heating in more detail.

Figure 4. Rendering of a 'cold' laser oven. Engineers at IPG prepared beautifully baked cookies from supermarket dough in just 90 seconds, and fed the results to their Board of Directors.

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Advancing AlN and aluminium-rich AlGaN

High-quality epilayers with exceptional electrical quality are realised in Agnitron's systems, including its new horizontal MOCVD reactor, the AgniGaN 400

BY FIKADU ALEMA, WILLIAM BRAND, AARON FINE, VITALI SOUKHOVEEV AND ANDREI OSINSKY FROM AGNITRON

WITH a bandgap of just over 6 eV, AlN promises to provide ground-breaking power-electronic devices. But its success is stymied by difficulties in realising sufficiently high and stable free-carrier concentrations and mobilities in the device layers of diodes and transistors.

The most common dopant for realising *n*-type doping in AlN is silicon. Incorporating this element into AlN is relatively straightforward, but it does not behave as it does in GaN, where it forms a shallow donor. Instead, adding silicon to AlN creates deep defects, called DX centres. These defects are a menace, trapping electrons near the conduction-band edge, with activation energies ranging from 78 meV to 345 meV [1]. Due to this issue, only a small fraction of silicon dopants release free electrons at room temperature, hampering efforts to realise the carrier concentrations required for device operation.

To increase the *n*-type carrier concentration, engineers add more silicon to the AlN crystal. Initially this pays dividends, boosting the number of free electrons. However, there's a limit to what's possible, and beyond a certain level the free-carrier concentration falls. This occurs because higher doping levels introduce additional defects – such as vacancies and defect complexes – that trap or compensate for free electrons. Due to these deleterious effects, there's a limit to how effectively AlN can be doped. That's a major obstacle to realising the high *n*-type conductivity required for practical devices.

Critical to improving the electrical properties of AlN, and particularly for realising stable and efficient *n*-type doping, is the control of point defects. Two factors govern their concentration: the chemical potential of the crystal, and the position of the Fermi level. Through careful control of both parameters, engineers can reduce the formation of defects that trap or compensate carriers, and ultimately increase the activation efficiency of intentional dopants.

Our team at Agnitron, a US producer of OEM MOCVD hardware for wide and ultra-wide bandgap semiconductors, has grown AlN epilayers with our epitaxial systems to demonstrate their capability. With our reactors, defect density is controlled by adjusting the chemical potential through changes to growth conditions and modulation of the Fermi level via UV-assisted growth. These approaches were discussed in the pages of this magazine last year (see issue VII), for results obtained using our Agilis 100 remote-injection showerhead (RIS) and close-injection showerhead (CIS) reactors. Now we are providing an update on improving the quality of AlN films grown with these reactors, and our newly introduced horizontal MOCVD reactor, the AgniGaN 400.

Agilis 100: Electrical results

As part of a DARPA-funded programme, we have developed an MOCVD process for growing high-quality films of AlN. This effort has focused on our Agilis 100 MOCVD platforms, equipped with RIS and CIS configurations, and employing *c*-plane AlN substrates from Hexatech and Crystal IS as the foundations for epi-growth.

Based on this work, it is clear that reactor design and injection geometry govern film quality – particularly surface morphology, background carbon and oxygen incorporation – as well as the structural and electrical properties of AlN layers. Initial findings were discussed in last year's issue VII of *Compound Semiconductor* magazine [2]. More recently, we have built on that success, optimising key growth parameters – including pressure, substrate temperature, silane flow rate, and V/III ratio – to improve the electrical quality of these films.

Characterisation shows that these AlN films exhibit excellent structural and surface properties (see Figure 1). For epilayers around 12 μm-thick, the X-ray diffraction (XRD) rocking curve has a full-width at half-maximum (FWHM) of about 21 arcsec, and a surface roughness, in terms of root-mean-square roughness, of about 0.26 nm [3].

We have also obtained electrical data for AlN films, with measurements from over 150 AlN samples, grown on native AlN substrates using RIS and CIS Agilis 100 reactors at Agnitron Technology and Arizona State University (ASU) (see Figure 2 (a) for a summary of the results). Included in these measurements is electrical data from samples produced on the recently commissioned Agilis 100 reactor installed at ASU, which is equipped with the RIS showerhead geometry. To ensure Hall measurements are reliable, a 70-80 nm highly conductive AlGaN contact layer (carrier concentration of more than 10^{19} cm^{-3}, and a resistivity of 15 mΩ cm) is deposited on the AlN surface using the Agilis reactors. After depositing metal contacts at the four corners of the samples, etching AlGaN exposes the AlN surface, enabling stable Hall measurements with both DC and AC Hall systems.

Measurements reveal free-carrier concentrations in the AlN layers ranging from around 3 x 10^{14} cm^{-3} to 4 x 10^{16} cm^{-3} and electron mobilities between about 6 cm^2 V^{-1} s^{-1} and 221 cm^2 V^{-1} s^{-1}. A clear trend is observed, with a high mobility occurring at a

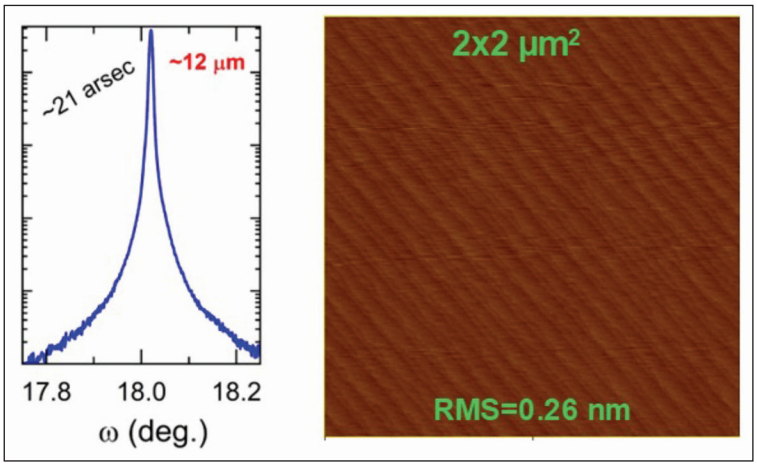


Figure 1. X-ray diffraction rocking curve (left) and a 2 μm × 2 μm atomic force microscopy image (right) of a 12 μm thick AlN film grown on a Crystal IS substrate using the RIS Agilis 100 reactor at Agnitron Technology.

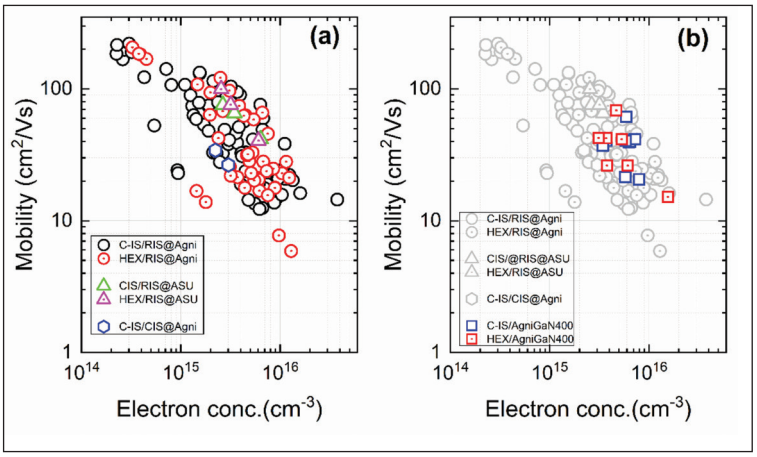
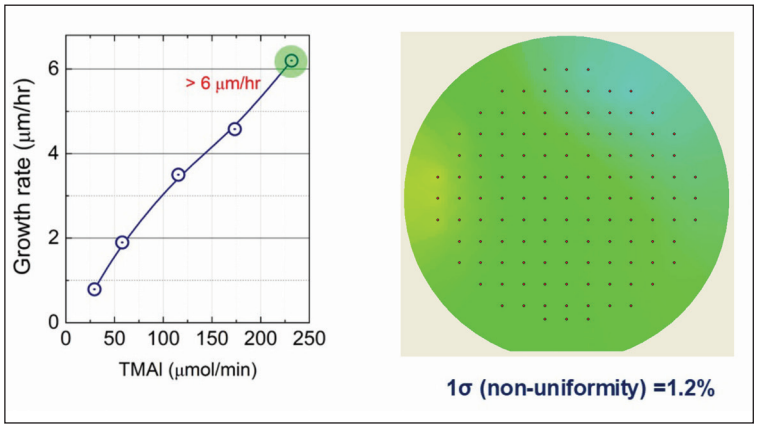


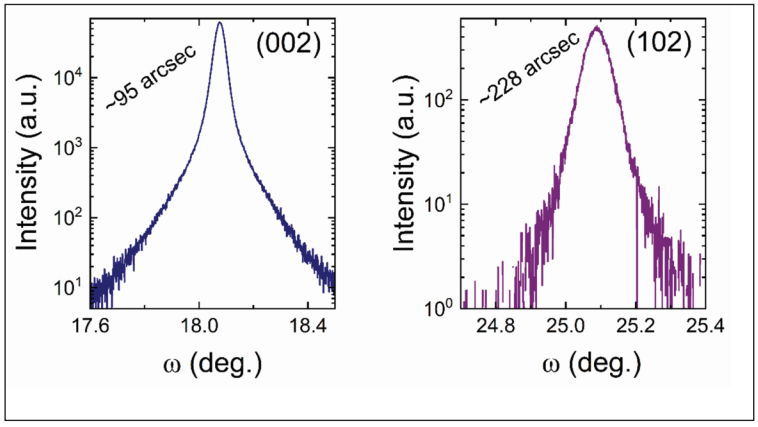
Figure 2. Electron mobility as a function of free-electron concentration in intentionally silicon-doped AlN layers grown by MOCVD under varying growth conditions. (a) Results from Agilis 100 reactors: remote-injection showerhead (RIS) at Agnitron (circles), close-injection showerhead (CIS) at Agnitron (hexagons), and RIS at Arizona State University (triangles). (b) Results from AlN layers grown using the AgniGaN 400 horizontal reactor (squares), compared with data from the Agilis reactors. Different colours indicate the substrate used for growth.



➤ Figure 3. AlN growth rate as a function of trimethylaluminium (TMAl) molar flow rate (left) and a two-dimensional thickness map of an AlN film grown on a 50 mm sapphire substrate (right) using the AgniGaN 400 reactor. A 2 mm edge exclusion was applied in the thickness uniformity analysis.

low carrier concentration (μ_e around 221 $cm^2 V^{-1} s^{-1}$, for *n* around 3 x 10^{14} cm^{-3}), and higher carrier concentrations leading to lower mobilities (for example, μ_e around 15 $cm^2 V^{-1} s^{-1}$, for *n* around 4×10^{16} cm^{-3}). These electrical properties are realised through systematic variation of various growth parameters, including pressure, substrate temperature, silane flow rate, and V/III ratio. After process optimisation, comparable electrical results are obtained from growth on Crystal IS and Hexatech substrates, although somewhat different growth temperatures are required.

One important finding is the similarity in results across different platforms and users. For this study, most samples were grown by us in our RIS Agilis 100 reactor – but we also produced some using the CIS configuration, and they show similar performance. Data from the RIS Agilis 100 reactor installed at ASU closely matches our own results, highlighting the reproducibility of our Agilis platform across different installations. Nearly all samples grown in the Agilis reactors are conductive, with most exhibiting a bulk resistivity below 30 Ω cm. The lowest resistivity is around just 11 Ω cm (μ_e around 15 $cm^2 V^{-1} s^{-1}$, and *n* around 4 x 10^{16} cm^{-3}), a substantial improvement over the best previously reported value of around 28 Ω cm [4].



➤ Figure 4. X-ray rocking curves of a 6 μm-thick AlN film grown on a sapphire substrate using the AgniGaN 400 reactor: (002) reflection (left) with a FWHM of about 95 arcsec and (102) reflection (right) with a FWHM of about 228 arcsec, indicating low screw and edge dislocation densities in the film.

Recently, we integrated a high-power deuterium vacuum ultraviolet (D_2-VUV) source directly into the showerhead gas distribution flange of our RIS Agilis 100 reactor. The benefits of introducing a source of UV are a suppression of compensating defects and enhanced silicon dopant activation in AlN. Compared with previously employed mercury-xenon lamps, the deuterium source delivers a much stronger photon energy, above the AlN bandgap, making this form of illumination especially effective and efficient when supporting the growth of ultrawide-bandgap semiconductors.

According to secondary ions mass spectrometry, D_2-VUV exposure has a negligible impact on impurity levels, with oxygen background concentrations around 4 × 10^{16} cm^{-3} and carbon concentrations at the detection limit. Based on these findings, improved electrical performance is not associated with a reduction in impurity incorporation, and should be attributed to improved dopant activation and/or suppression of compensating defects.

We have also conducted Hall measurements on our AlN films grown under D_2-VUV exposure. These measurements determined a free-electron concentration of about 2.9 × 10^{16} cm^{-3} and electron mobility of about 80 $cm^2 V^{-1} s^{-1}$, corresponding to a resistivity of around 2.74 Ω cm. This value, amongst the lowest ever reported for silicon-doped AlN by MOCVD, highlights the important role D_2-VUV plays in improving the electrical performance of AlN.

AgniGaN 400 horizontal reactor

We have recently expanded our portfolio of MOCVD reactors with the AgniGaN 400, a system designed for the growth of GaN, AlN, and AlGaN thin-films at high growth rates. We developed this horizontal-flow reactor for the Naval Research Laboratory (NRL) under an SBIR Phase II programme funded by the Office of Naval Research (ONR). The AgniGaN 400 operates over a wide pressure range, from low pressures up to above atmospheric pressure growth. The system can accommodate three 2-inch wafers, or one 4-inch wafer, and reach substrate temperatures up to 1350°C.

To evaluate the performance of this reactor, we have grown AlN and AlGaN layers on sapphire and native substrates. Trials have focused on key metrics, such as growth rate, thickness uniformity, crystal quality, and electrical properties.

Our AgniGaN 400 is a multizone gas flow design, facilitating separate delivery of metalorganic

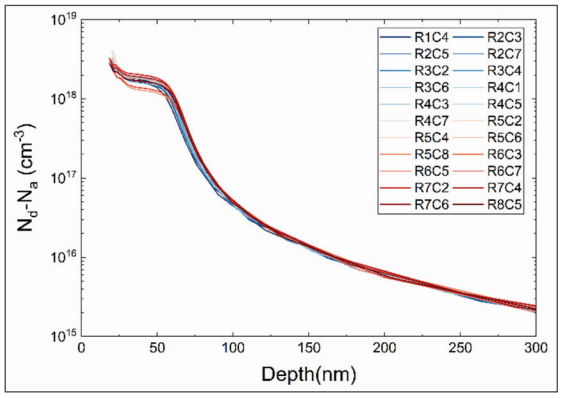
precursors (alkyls), hydrides, and pushing gases into the reaction zone. By optimising the total gas flow rate through the injection system, one can control premature gas-phase reactions, growth rate, and thickness uniformity. One feature of the AgniGaN 400 is a heated gas injection port, capable of reaching +150°C – this enables the use of low-vapour-pressure precursors, such as those required for materials like AlScN.

Users of the AgniGaN 400 can produce high-quality AlN and AlGaN films at high growth rates. Under optimised growth conditions, we realise AlN growth rates exceeding 6 μm/hr (see Figure 3, left), limited only by the maximum aluminium precursor flow. Thickness uniformity measurements of AlN films grown on sapphire show a 1σ non-uniformity of around 1.2 percent across a 50 mm wafer (see Figure 3, right).

Another strength of these AlN films is their low dislocation densities. Engineers at NRL have characterised the AlN layers we grew on sapphire with thicknesses ranging from around 2.6 μm to 6.0 μm. XRD rocking curves for an AlN film around 6 μm-thick have FWHM values of 95 arcsec for the (002) reflection and 228 arcsec for the (102) reflection. For thinner films, FWHM values are slightly higher, ranging from 107 arcsec to 95 arcsec for the (002) plane and 258 arcsec to 228 arcsec for the (102) plane, due to a reduction in screw and edge dislocation densities with increasing film thickness. These results reveal that the structural quality of AlN films grown using the AgniGaN 400 reactor is comparable to the best results reported in the literature.

We have also evaluated our AgniGaN 400 for conductive AlGaN growth, for aluminium compositions from 65 percent to 90 percent. For aluminium contents below 80 percent, we have produced conductive AlGaN layers with carrier concentrations up to 1 x 10^{19} cm^{-3} and electron mobilities exceeding 50 cm^2 V^{-1} s^{-1}, asserting our system's capability to produce high-quality AlGaN. We have also produced an $Al_{0.83}Ga_{0.17}N/Al_{0.66}Ga_{0.34}N$ HEMT structure featuring a two-dimensional electron gas mobility around 150 cm^2 V^{-1} s^{-1} and a sheet charge density of about 5 x 10^{12} cm^{-2}. These values validate our reactor's suitability for growing device-quality AlGaN heterostructures.

Further evaluation of the electrical quality of AlN films produced with the AgniGaN 400 reactor has come from the characterisation of intentionally silicon-doped AlN layers, grown on native AlN substrates. Using the Hall method, we determined the electron mobility of these films, with thicknesses ranging from around 1.3 μm to 4.0 μm, and benchmarked the results against those obtained from AlN films grown with our Agilis 100 reactors (see Figure 2 (b)). Our measurements reveal that AlN layers grown in the AgniGaN 400 reactor exhibit free-carrier concentrations of around 3.1 x 10^{15} cm^{-3}



➤ Figure 5. N_d-N_a profiles of MOSFETs measured from 22 spots on a 1-inch iron-doped (010) Ga_2O_3 wafer.

to 1.6×10^{16} cm^{-3} and electron mobilities ranging from about 15 cm^2 V^{-1} s^{-1} to 70 cm^2 V^{-1} s^{-1}, corresponding to bulk resistivities of around 17-50 Ω cm.

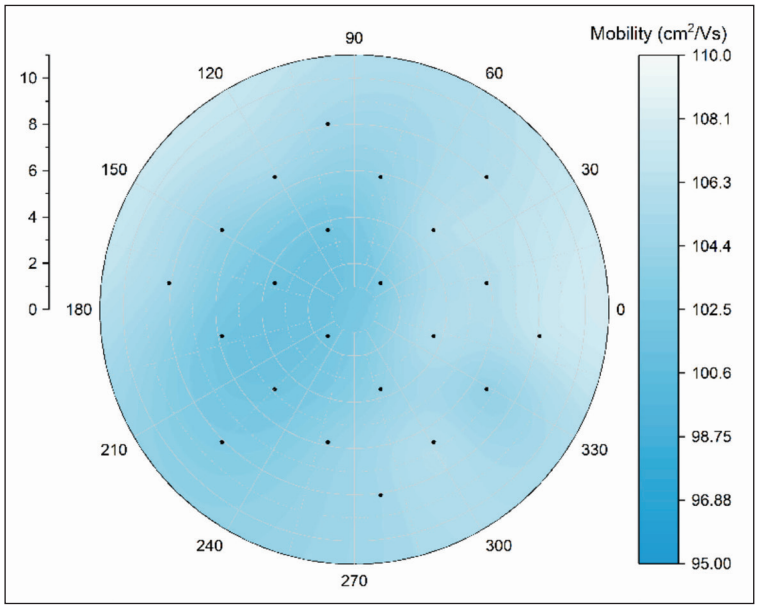
Based on these results, we conclude that the electrical performance of AlN films grown with the AgniGaN 400 is comparable to those obtained using our Agilis 100 platforms. This is very encouraging, given the limited experiments performed, and a growth process that's still to be fully optimised. Even now this reactor is delivering high-quality AlN films with bulk resistivity as low as around 17 Ω cm – that's a value comparable to results realised with our Agilis reactors, and significantly better than many values reported in the literature [4].

Nitrogen doping of Ga_2O_3

As well as advancing the growth of Al(Ga)N, we remain at the forefront of MOCVD reactor and process development of Ga_2O_3. Since 2018, we have introduced two Ga_2O_3 multi-wafer platforms; the Agilis 500, which supports up to one 4-inch wafer; and the Agilis 700, which accommodates up to one 6-inch wafer. Both these systems employ susceptor rotation speeds up to 2000 rpm, key to enabling excellent film uniformity and crystal quality. Using these platforms, we have demonstrated record Ga_2O_3 performance, including exceptional purity, record low-temperature electron mobility above 23,000 cm^2 V^{-1} s^{-1} [5], and controllable doping from the low 10^{15} cm^{-3} to above 3 x 10^{20} cm^{-3}.

One problem plaguing Ga_2O_3 lateral devices since the explosion of Ga_2O_3 research in the 2010s is the accumulation of silicon at the interface between the native substrate and the epitaxial layers. This accumulation creates a secondary conduction channel that increases reverse-bias leakage currents and introduces inconsistencies to MOSFET threshold voltages. Traditionally, HF etching prior to epitaxial growth suppresses the silicon peak, but this adds extra steps to pre-growth cleaning [6].

Recently, a number of research groups have investigated the use of nitrogen as a compensative dopant in gallium oxide, spurring interest in its use in lateral FETs. Over many years, we have carried out a comprehensive evaluation of nitrogen as a potential Ga_2O_3 dopant, using dilute ammonia,



➤ Figure 6. Hall mobility map of MOSFETs measured from 22 spots on a 1-inch iron-doped (010) Ga_2O_3 wafer.

nitric oxide and nitrogen dioxide. All these nitrogen-incorporating sources have pros and cons. When nitrogen dioxide is employed as the main oxidizer, a high chamber pressure is needed to efficiently decompose this oxide into nitrogen and oxygen, leading to high particle concentration that degrades epitaxial quality. Switching to nitric oxide works well for incorporation to the mid-10^{18} cm^{-3}, which may be sufficient for certain applications, but the silicon spike at the surface of the Ga_2O_3 substrate often rises to the low-10^{19} cm^{-3}, and nitric oxide fails to fully compensate for this charge. The third candidate, ammonia, has a very linear incorporation rate from low 10^{16} cm^{-3} to high 10^{19} cm^{-3}, giving it great flexibility in structure growth [7]. However, as ammonia incorporates hydrogen along with nitrogen, this threatens to counter the desired resistive effects. Note, though, that this has not been observed in any electrical results to date.

As part of our SBIR programme on large-area Ga_2O_3 FET development, we have used ammonia when producing a nitrogen-doped buffer layer, to separate the FET channel from the substrate interface. According to capacitance-voltage profiling, the nominal nitrogen concentration, 6 x 10^{18} cm^{-3}, completely removed any observable interfacial charge (see Figure 5).

Our FET structure, grown on a 1-inch (010) iron-doped Ga_2O_3 substrate, consists of a low-temperature nucleation layer, a 100 nm-thick nitrogen-doped buffer, a 120 nm-thick unintentionally doped layer, and a 65 nm-thick silicon-doped channel. Capacitance-voltage measurements at 22 locations across the wafer have determined a uniform difference between the density of donors and acceptors of 1.6 x 10^{18} cm^{-3}, and no detectable interface conductivity, indicating that nitrogen compensation effectively suppresses the interfacial silicon contribution. Mobility mapping (see Figure 6) has offered additional evidence of excellent uniformity, with an average mobility around 10^4 cm^2 V^{-1} s^{-1} at *n* of about 8 x 10^{17} cm^{-3} and a 1σ non-uniformity of around 1.5 percent.

These advances in Ga_2O_3, as well as those on AlN and aluminium-rich AlGaN, highlight the critical role that we are playing in advancing the epitaxy of ultra-wide bandgap semiconductors.

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Asymmetry spawns superior SiC superjunctions

By breaking conventional performance limits, asymmetric SiC superjunctions boost power-conversion efficiency

BY DAISUKE IIZASA, HIROAKI SHIRAGA, SUGURU OKUYAMA, SEIGO MORI AND YUKI NAKANO FROM ROHM

GLOBAL ELECTRICITY consumption is rocketing, driven by the growing adoption of electric vehicles and increasing demands on data centres. To increase supply, while addressing concerns related to carbon footprints, many nations are boosting their renewable energy systems. However, efforts in this direction should go hand-in-hand with increases in power-conversion efficiency, as every fraction of a percentage point ensures that the electrical energy that's generated is used as wisely as possible.

Helping to succeed on this front is an uptake of SiC devices, now sitting at the heart of modernised electrical energy infrastructure. Thanks to their intrinsic material advantages, including a wide bandgap, a high critical electric field and excellent thermal conductivity, SiC devices operate efficiently, even when having to handle high voltages at high temperatures.

Within the diverse family of SiC device architectures, the superjunction structure attracts a great deal of attention. It is a promising approach to breaking the long-standing trade-off between specific on-resistance and breakdown voltage, a bottleneck that has traditionally constrained performance.

In the medium-voltage systems used in renewable-energy converters and electric-vehicle inverters, even modest reductions in specific on-resistance deliver meaningful gains in efficiency at the system level. But succeeding in this endeavour is not easy, as it is costly and slow to optimise SiC superjunction structures through experimental trial and error. The processing steps involved – such as trench-refill epitaxy, implantation into trench sidewalls, and repeated cycles of epitaxial growth and ion implantation – are demanding and highly sensitive to fabrication variability. Due to these challenges, theoretical evaluation is indispensable. When one works with a reliable computational model, this accelerates design cycles and clarifies the underlying physical limits, thereby providing a strong foundation for more-efficient, cost-effective manufacturing.

Initially, the superjunction concept took the form of a full-superjunction, with *n*-type and *p*-type pillars extending through the entire drift layer (see Figure 1(a), (b)). Modifications have followed, such as semi-superjunctions that feature an additional drift region beneath the pillars (see Figure 1(c)).

The design space of full-superjunctions has been thoroughly explored, with investigations considering pillar doping, pillar width, and the depth of the superjunction region. Their fabrication is challenging, involving extremely intricate processes that include multiple high-energy implantation steps, combined with epitaxial growth or the use of trench-refill epitaxy.

In comparison, semi-superjunctions are more practical for real devices. However, despite this, there are relatively few theoretical studies of these structures, an omission that we are addressing at Rohm. Our investigation led to the design of asymmetric SiC superjunctions that can overcome conventional performance limits.

A particularly important, but often overlooked factor in the study of SiC superjunctions is impact

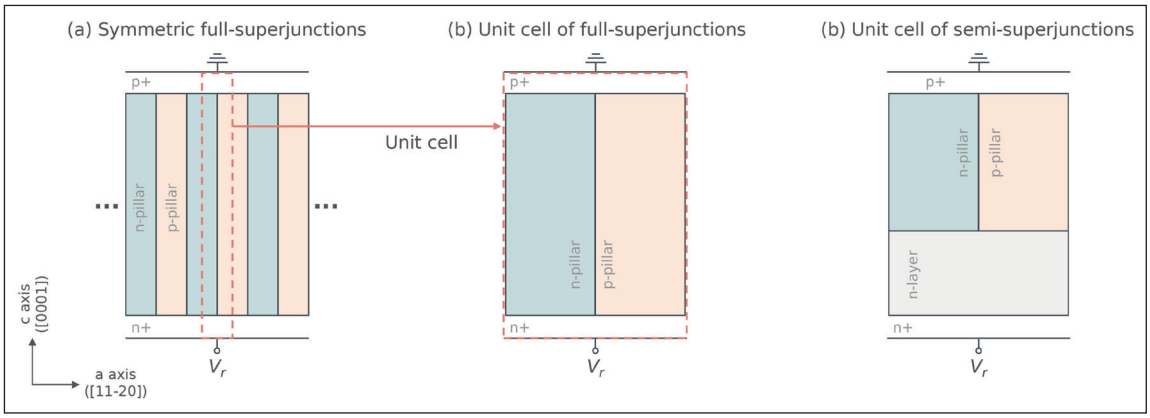


Figure 1. Cross-sections of SiC superjunction devices under reverse bias. Panels (a) and (b) show full-superjunction structures with pillars extending through the entire drift layer, while (c) illustrates a semi-superjunction structure in which the pillars partially extend into the drift layer above an additional drift region.

ionisation anisotropy. Despite its strong influence on the breakdown behaviour of the SiC superjunction, optimisation studies tend to treat impact ionisation as isotropic – that's a troublesome oversight that leaves a significant gap between theory and the real physics governing device performance. It is critical to capture anisotropy accurately, and this is needed to ensure a realistic prediction of blocking voltages and identification of the true performance limits of superjunction devices, especially when efforts are directed at balancing the specific on-resistance and blocking voltage.

Impact ionisation anisotropy

In stark contrast to silicon, SiC exhibits pronounced crystal anisotropy in impact ionisation coefficients. This variation originates from its crystal structure, with the excitation energy required to generate additional conduction carriers varying markedly with crystallographic direction. As a result, electrons and holes experience different avalanche generation rates, depending on the axis of travel, for example between the [0001] and [11$\bar{2}$0] directions. In fact, the electron impact ionisation coefficient along the *a*-axis is significantly larger than that along the *c*-axis (see Figure 2(a)). Due to this anisotropy, SiC devices enter avalanche breakdown earlier than predicted by conventional isotropic models. Therefore, the anisotropy associated with impact ionisation must be carefully considered when evaluating device behaviour near the critical electric field.

With superjunctions, it is particularly important to account for anisotropy associated with impact ionisation. In these devices, alternating *n*- and *p*-type pillars form a distinct two-dimensional electric-field landscape. There is charge compensation between the pillars, resulting in lateral depletion, which produces large electric-field peaks at pillar interfaces. These peaks strongly interact with the anisotropic impact ionisation process, as shown in Figure 2 (b).

Under these conditions, there are a number of electrical breakdown trajectories. Paths may run through the centres of the *n*- or *p*-pillars, or follow a winding route along the pillar interface, where there is a highly concentrated local electric field. Among these variations, the winding path tends to trigger the earliest breakdown. This is driven by strong coupling between the intense electric field that's oriented along the *a*-axis in SiC superjunctions, and the pronounced anisotropy of the impact ionisation coefficients.

When simulations or theoretical models neglect anisotropy, the price that's often paid is an

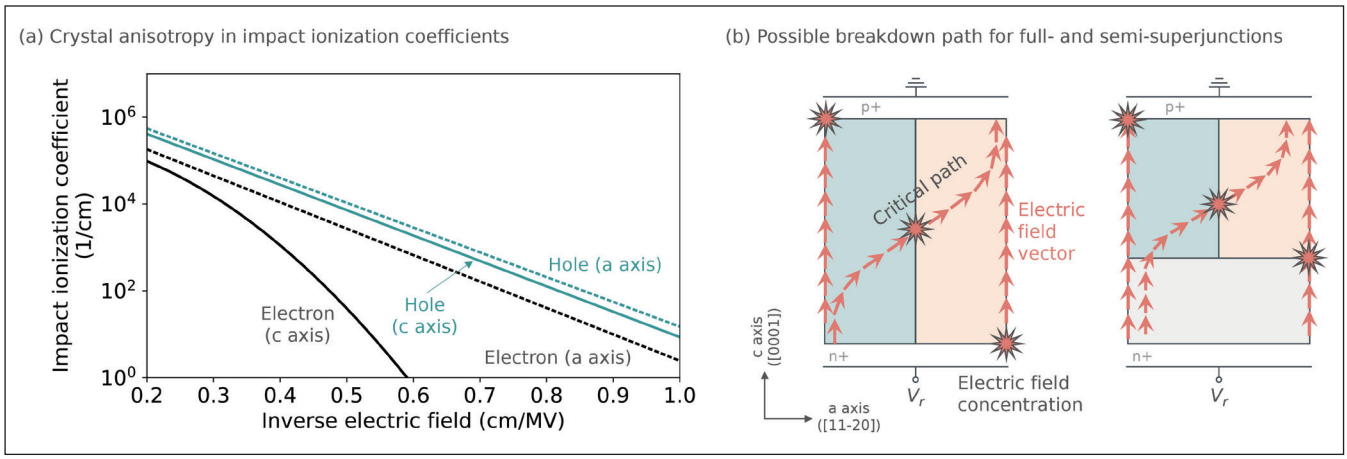
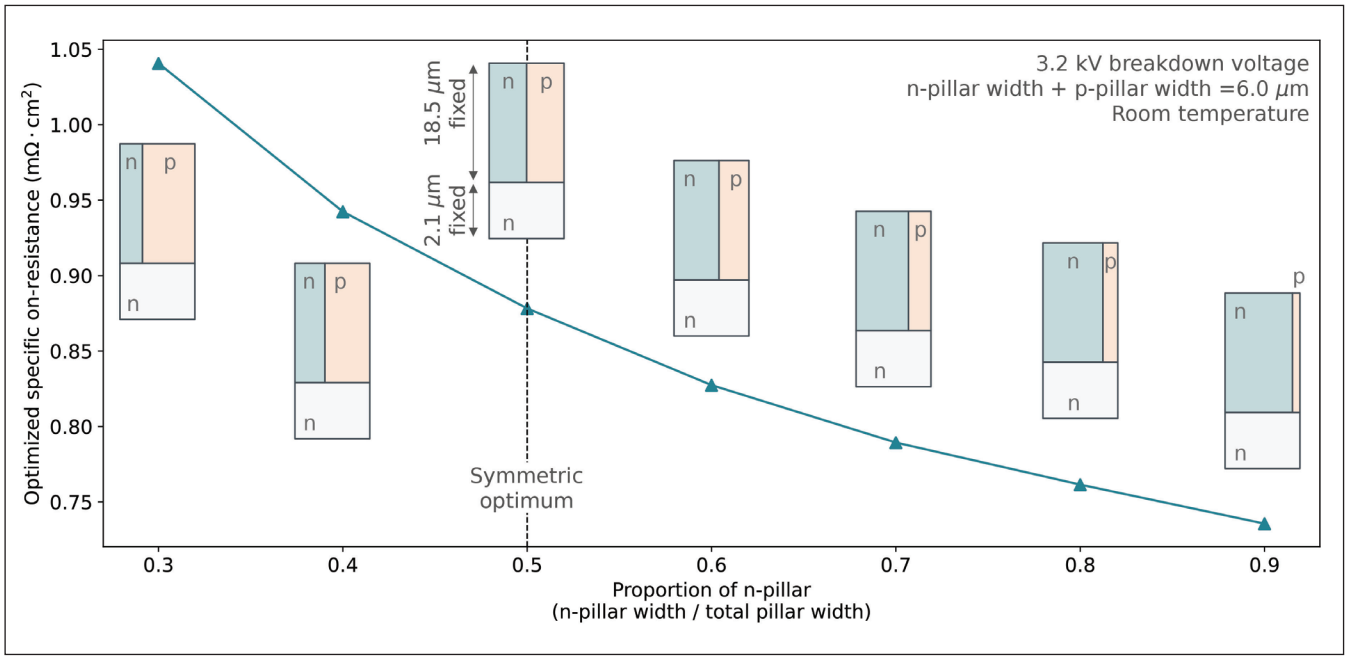


Figure 2. Impact ionisation anisotropy and breakdown paths in SiC superjunctions. (a) Electron impact ionisation is much stronger along the *a*-axis than the *c*-axis, highlighting the importance of crystal anisotropy. (b) Strong electric-field concentrations appear near pillar centres and interfaces, and the breakdown path typically follows these high-field regions.



➤ Figure 3. Enhanced performance of semi-superjunctions achieved through asymmetrically tuned geometry. A proportion of 0.5 for the *n*-pillar corresponds to the perfectly symmetric case, which defines the conventional performance optimum. Asymmetric geometries with wider *n*-pillars and narrower *p*-pillars provide further reductions in specific on-resistance beyond this symmetric limit.

overestimate of the blocking voltage. This oversight arises because the actual ionisation rate along the interface path is notably higher than that assumed in isotropic models. One unwanted, dire consequence of optimisation studies that ignore anisotropy is that they draw misleading conclusions concerning the performance ceiling of SiC superjunction devices. To ensure meaningful design and optimisation, prior to fabrication, it is essential to accurately capture the interplay between anisotropic impact ionisation and the superjunction field structure.

Beyond symmetry

Traditionally, theoretical and TCAD-based analyses of SiC superjunctions tend to assume symmetric geometries, namely equal pillar widths and matched doping concentrations. This approach offers mathematical simplicity, as with symmetry geometries, charge balance is straightforward to satisfy and analytical treatment is far more manageable. However, there is a disconnect between these simulations and real devices – the latter rarely maintain ideal symmetry, as fabrication processes introduce unavoidable variations in geometry and doping.

In practice, asymmetries influence both specific on-resistance and blocking voltage. For example, widening the *n*-type pillar may lower the resistance by enhancing conductance, but this can be accompanied by a disturbing of charge balance and a strengthening of the electric-field concentration near the top of the *n*-pillar centre. Unfortunately, this electric-field localisation may be amplified by differences in doping concentration between *n*- and *p*-type pillars.

Collectively, these effects determine actual device performance, so it's essential for predictive models to incorporate them in a physically consistent manner. Although prior studies have investigated asymmetric semi-superjunction geometries in terms of the trade-off between specific on-resistance and blocking voltage, they have failed to offer systematic insight, including the role that's played by impact ionisation anisotropy.

Previous work by our team took an initial step in closing this gap, by developing a theoretical model for symmetric semi-superjunctions. That particular approach, which explicitly considered impact ionisation anisotropy, provided clear insight into the performance limit of symmetric structures when accounting for impact ionisation anisotropy.

The weakness of our initial model is that symmetry represents just one special case. To accurately reflect real devices, it is indispensable to use a more general framework that's capable of handling arbitrary asymmetry. By developing such a model, we reveal how deviations from perfect symmetry influence static performance characteristics, and we define the attainable trade-off between the specific on-resistance and the blocking voltage beyond the symmetric regime.

A unified framework

Key to our progress is the development of a unified computation framework that provides performance evaluation of SiC superjunctions with arbitrary geometric asymmetries. The cornerstone of this framework is the derivation of an exact solution to

Poisson's equation. This solution provides closed-form expressions for the electric-field distribution as a function of position, doping concentration, and pillar width. With this approach the electric field can subsequently be referenced, allowing us to quantify the blocking voltage without having to rely on CPU-intensive discretised numerical computation.

In parallel, we have constructed an analytical formula for specific on-resistance. This model takes into account incomplete ionisation of dopants, as well as a mobility degradation that depends on doping levels.

By combining these expressions, we are able to analyse the trade-off between specific on-resistance and blocking voltage across a broad design space in a matter of seconds, using just a standard CPU. In sharp contrast, TCAD simulations typically take hours.

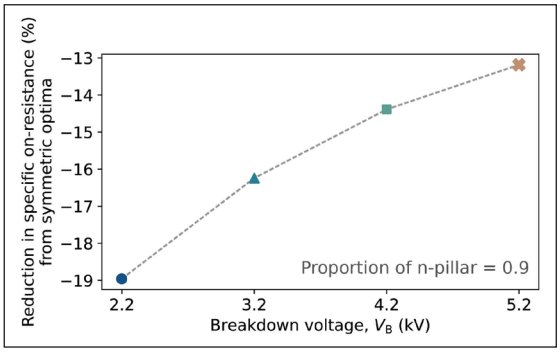
Our unified model combines computational efficiency with clear physical insight. It reveals how geometric parameters and doping concentrations jointly shape the electric-field landscape, and it clarifies which factors govern breakdown and conduction. Thanks to these valuable attributes, our framework functions as a powerful tool for pre-fabrication design optimisation, allowing rapid exploration of potential device structures and providing meaningful theoretical guidance for process engineers.

The asymmetric advantage

Using our unified computation model, we have systematically investigated how geometric asymmetry influences the relationship between specific on-resistance and blocking voltage. Our results reveal that well-designed asymmetric semi-superjunctions exceed the performance of symmetric ones, and effectively surpass the conventional design limit.

Highlighting this trend is a comparison of symmetric and asymmetric geometries that sustain a breakdown voltage of 3.2 kV, and have a 6 μm pillar pitch (see Figure 3). In this case, we have plotted the optimised specific on-resistance as a function of *n*-pillar proportion, which we define as the *n*-pillar width divided by the total pillar width. We keep the overall device pitch unchanged. The plot for 0.5 considers the perfectly symmetric case, which represents the theoretical optimum for symmetric semi-superjunctions. This graph also shows that widening the *n*-pillar while narrowing the *p*-pillar leads to a reduction in specific on-resistance, realised without compromising blocking voltage. The benefit is not trivial – it's up to 16 percent lower than the symmetric optimum. The greatest gains are realised when the *p*-pillar is extremely narrow, corresponding to an *n*-pillar proportion of 0.9.

We have extended this analysis to several voltage classes (see Figure 4 for a summary of the results). For every voltage class, we have plotted the maximum reduction in specific on-resistance under an asymmetric geometry. The optimum gain always occurs at an *n*-pillar proportion of 0.9. We have found meaningful improvements in specific on-resistance for a wide range of voltage classes when adopting finely tuned asymmetric geometries. Enhancement is highest for 2.2 kV devices, which benefit from a 19 percent reduction in specific on-resistance.

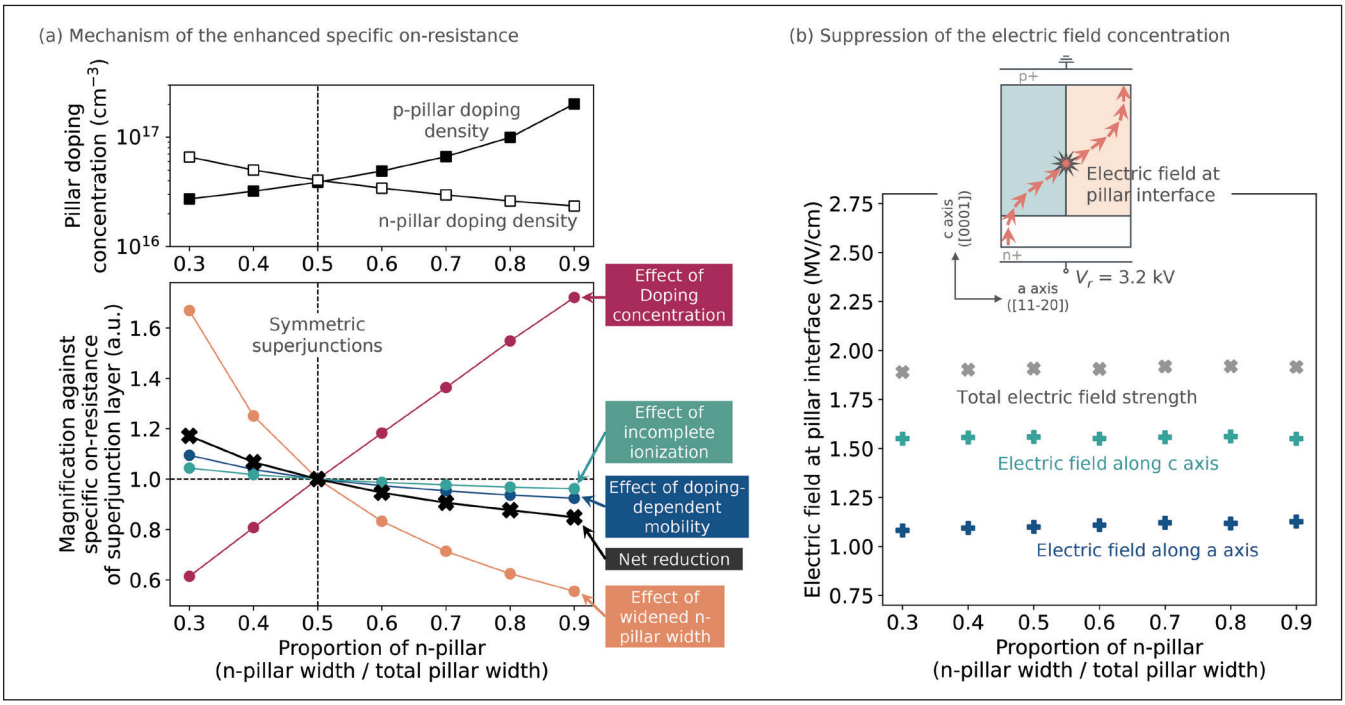


➤ Figure 4. Maximum specific on-resistance enhancement obtained with asymmetric geometry across different voltage classes. All voltage classes show a substantial improvement compared with conventionally optimised symmetric semi-superjunctions, with the best case appearing at an *n*-pillar proportion of 0.9.

To understand the origin of these improvements, we began by examining the design parameters that led to them. This included an investigation of how device performance evolves when geometry deviates from symmetry. Considering a 3.2 kV case, and the *n*-pillar proportion becoming larger, we have found that performance improves when the *p*-pillar doping density increases and the *n*-pillar doping density decreases. This shift in doping is needed to maintain charge balance under the wider *n*-pillar and narrower *p*-pillar configuration.

We are able to interpret the underlying physics of this state of affairs. When the *n*-pillar is wider, this boosts conductance by increasing the cross-sectional area for carriers, which reduces the specific on-resistance (see the lower panel of Figure 5 (a)). Meanwhile, when there's a lowering of *n*-pillar doping, while raising the *p*-pillar doping to preserve charge balance, this suppresses incomplete ionisation and increases the carrier density at room temperature. Note that this adjustment also enhances electron mobility, further contributing to the reduction in specific on-resistance. These positive effects are considerable – they collectively outweighing the resistance increase normally associated with reducing

Another benefit of the optimised design is that it stabilises the electric-field profile in the superjunction region. Our work shows that the dominant contributor to electrical breakdown in optimised semi-superjunctions is the electric-field concentration at the *p-n* pillar interface



➤ Figure 5. Mechanism behind the reduced specific on-resistance in asymmetric semi-superjunctions and its impact on breakdown. (a) Specific on-resistance improves when the *p*-pillar doping density is increased and the *n*-pillar doping density is decreased, with key contributing factors such as doping, incomplete ionisation, mobility and pillar width plotted relative to the symmetric case. (b) Despite these changes, the electric-field concentration at the pillar interface remains essentially unchanged over the *n*-pillar proportion, allowing the device to sustain its breakdown voltage while benefiting from lower specific on-resistance.

the *n*-pillar doping density, and they enable an overall improvement in specific on-resistance for asymmetric geometries.

Another benefit of the optimised design is that it stabilises the electric-field profile in the superjunction region. Our work shows that the dominant contributor to electrical breakdown in optimised semi-superjunctions is the electric-field concentration at the *p*-*n* pillar interface (see Figure 5 (b)). According to our calculations, the electric-field components along the *a*-axis and *c*-axis of SiC, as well as the total field magnitude, remain essentially unchanged over the range of *n*-pillar proportions. This is a welcome finding, indicating that the blocking voltage remains stable, even in highly asymmetric geometries.

We can conclude that the resulting device configuration maintains a high breakdown voltage that's comparable to symmetric designs while offering a significantly lower specific on-resistance. This finding highlights that geometry is a powerful design variable, which can be employed to enhance the performance of SiC superjunctions under impact ionisation anisotropy, supported by an efficient computation framework.

Looking ahead, we are expecting this combination of anisotropy-aware modelling and asymmetric design to have a significant impact on the future of SiC superjunctions, informing both discrete device roadmaps and volume-production design rules. When manufacturers embed this framework early in the development flow, they will shorten iteration cycles, reduce process risk, and have the opportunity to explore higher-voltage operating regimes that would be prohibitively expensive to probe by just trial and error.

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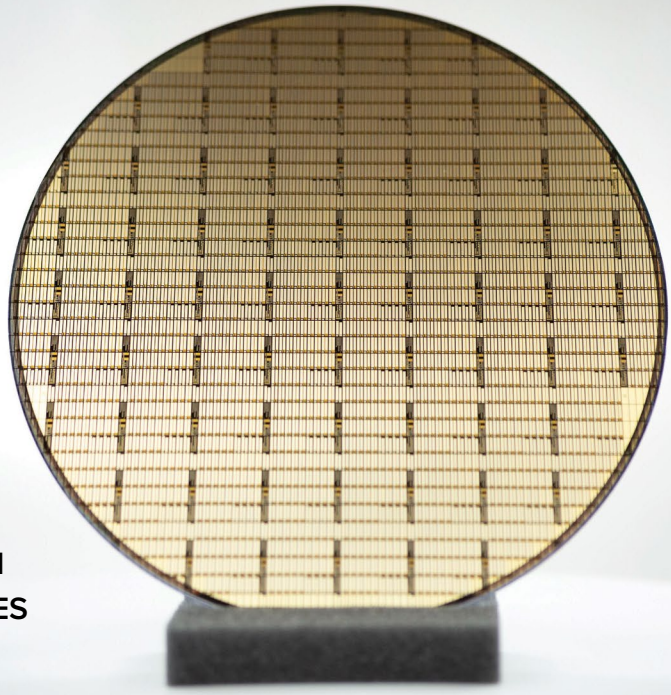
Stress-tested, future-ready GaN

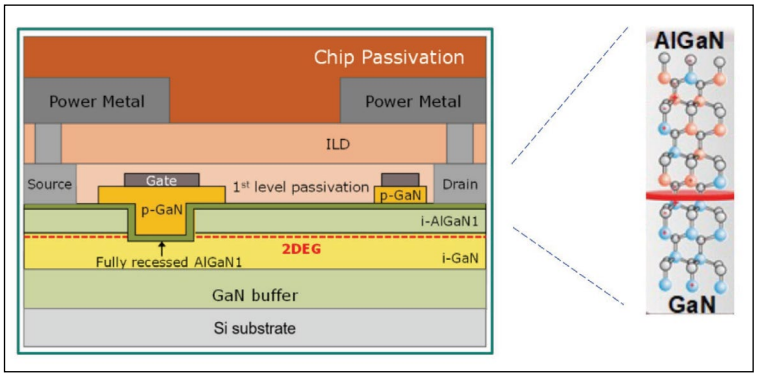
Reliable GaN unlocks the door to a hyper-efficient future where AI thrives, humanoids awaken, and data centres pulse cooler, faster, and smarter

BY GABRIEL LANSBERGEN AND SAMEH KHALIL FROM INFINEON TECHNOLOGIES



FOR DECADES, silicon-based semiconductors have been the bedrock of power electronics. Their deployment has spanned consumer devices, industrial automation and automotives, with devices delivering remarkable scalability and cost efficiency.

But evolution is underway. As global energy demands surge and applications grow more electrified, driven by desire for 'digitalisation' and 'decarbonisation', wide bandgap devices are making an impression in the power landscape. The era of co-existence is underway, with these three material systems are forming a complementary toolkit: silicon is retaining its dominance in low-to-mid-voltage applications; SiC is now excelling in high-voltage environments, such as grid infrastructure, automotive and industrial applications; and GaN is rapidly gaining ground in high-frequency, high-efficiency domains, such as fast chargers, solar microinverters, radar systems and AI-centric data centres.



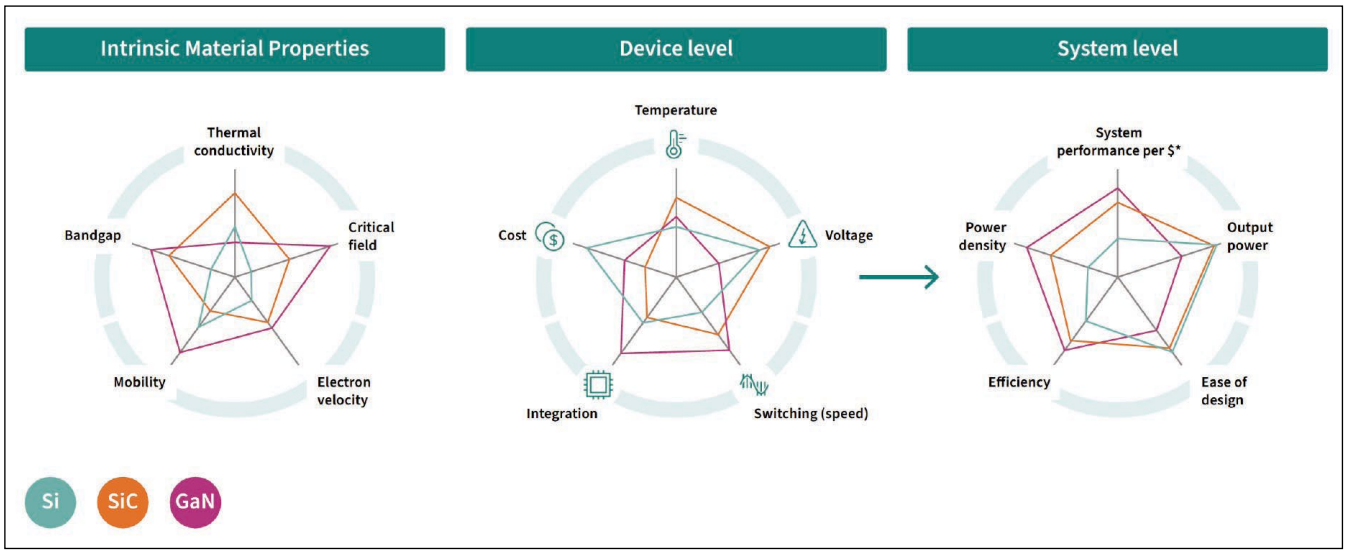
➤ Figure 1. Cross-section of the unit cell of Infineon's high-voltage lateral GaN HEMT, depicting the 2DEG sheet of electron charges and the absence of a *p-n* junction in the drift region. The higher the off-state breakdown requirements, the longer the gate-to-drain spacing. The high critical-electrical-field makes this distance much shorter than that of silicon counterparts while the high mobility and the high density 2DEG sheet of electron charges provides the low ohmic resistivity.

In the future, megatrends like e-mobility, AI-driven data factories and humanoid robotics will rely on advanced power electronics to deliver reliable, compact and thermally resilient energy. By 2030, it's possible that electrified transport and data centres alone will be trimming their energy consumption from what it could have been by over 150 million tons of CO_2 every year, thanks to wide bandgap adoption. At the same time, this trend will unlock billions in economic activity across automation, cloud infrastructure and intelligent machines.

The attraction of lateral GaN HEMTs

Advantages of GaN-based power devices can be broadly grouped into two categories. First, there's their intrinsic material properties, including a wide bandgap of 3.44 eV at 300K, and a high saturation electron drift velocity of 2.5 x 10^7 cm s^{-1}. And the second strength is their distinct device design, particularly when implemented in a lateral HEMT (see Figure 1) – this architecture allows for an exceptionally low on-state resistance for a given breakdown voltage, enabling enhanced efficiency and a higher power density.

There are also merits that arise from a wider bandgap (see Figure 2). Compared with that for silicon, just 1.12 eV, that for GaN is almost three times higher, ensuring a higher critical electric field that allows device designers to implement more compact



➤ Figure 2. Comparison between silicon, SiC and GaN at a material level, a device level and a system level, highlighting their unique advantages and complimentary nature.

unit cells for the same breakdown requirements. A smaller chip area is a major offsetting factor in what otherwise could lead to uncompetitive chip costs. What's more, the wider bandgap of GaN allows devices made from this material to operate at much higher temperatures, due to a lower intrinsic concentration of the thermally-generated electron-holes pairs, which are a potential source of noise that could hamper optimal device operation, especially under stringent applications conditions.

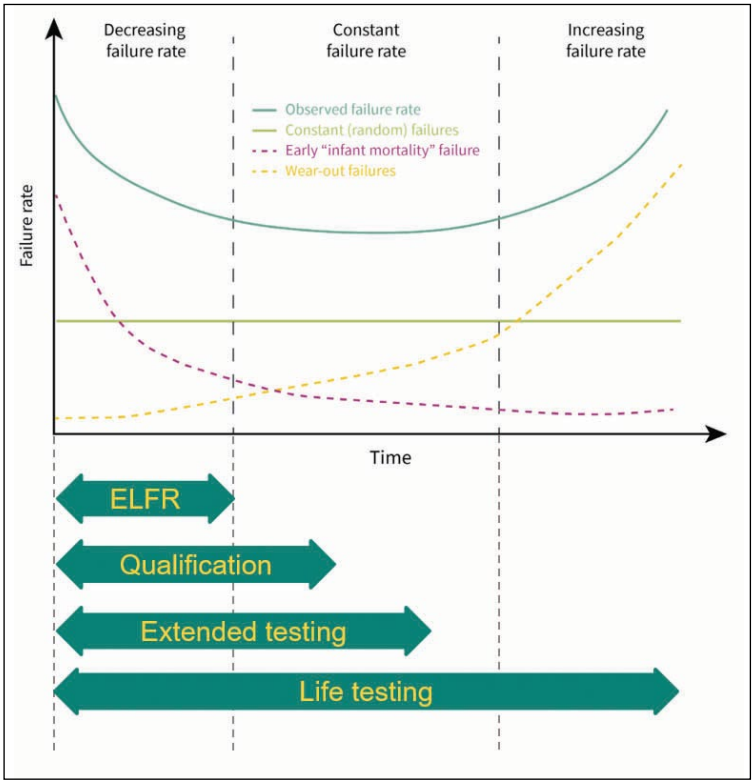
GaN HEMTs are renowned for their very low specific on-state resistance, a characteristic defined as the product of the on-state resistance and the device area. Contributing to this is a two-dimensional electron charge density reaching up to 1-2 x 10^{13} cm^{-2}, and an electron mobility as high as 2,000 cm^2 V^{-1} s^{-1}, resulting from GaN's high saturation electron drift velocity and its ability to form a two-dimensional electron gas layer.

Yet another advantage of the GaN HEMT is its capability to operate at high frequencies, thanks to a lack of minority carriers and a high saturation velocity. Behind this is an absence of a *p-n* junction diode to hold off an applied voltage in the off-state. The upshot is that circuit designers and system architects can produce smaller, lighter products that handle higher powers using higher frequencies.

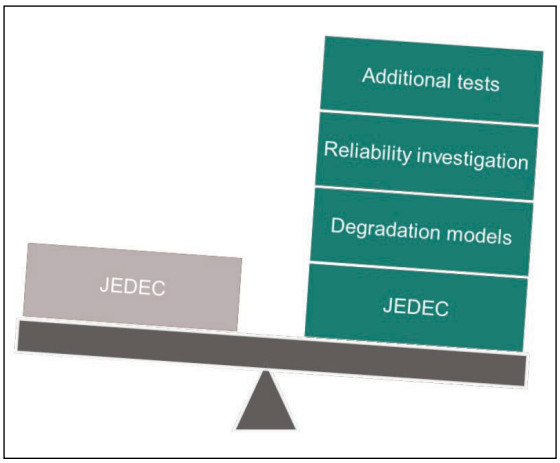
Reliability: a mission-critical enabler

As our society accelerates into a future that's powered by intelligent machines, data factories, electrified mobility and resilient infrastructure, GaN reliability is no longer a checkbox – instead it's the anchor point of progress, the silent guarantor of robust, high-efficiency power electronics that will shape a world worth living in.

Over the past two decades, engineers, physicists and reliability specialists studying GaN HEMTs have amassed a substantial body of data, driving significant advances in device reliability. These investigations have provided the foundation for product qualifications that meet the stringent demands of consumer, industrial and automotive-grade applications.



➤ Figure 3. Bathtub Curve. Device failures falls under three regimes, long conceptualised by insurance companies in the late 19th and early 20th centuries to describe mortality rates: a diminishing Early Life Failure Rates (ELFR), random (constant) failure rate and an increasing 'wear-out' failure rates, corresponding to infant mortality, stable middle years and increased risk of mortality with aging mortality in humans, respectively.



➤ Figure 4. The comprehensive reliability of GaN-based devices go far beyond baseline JEDEC standards.

At Infineon, we have been playing our part in these efforts, with several key challenges shaping the focus of our work. First, while the critical electric field of GaN – approximately ten times higher than that of silicon – provides the advantage of compact device geometries, as well as the means to operate under much stronger electric fields, particularly at or near the surface, we know that this comes at a price. It places significant stress on passivation and interfacial layers.

Our other area of concern relates to heteroepitaxial growth. Most GaN technologies rely on GaN layers, or related III-nitride stacks, that are grown on non-native substrates, predominantly silicon or sapphire. This approach tends to introduce defects and mechanical stress, originating from lattice and thermal mismatches between epitaxial layers and the underlying substrates.

To address these challenges, there needs to be sustained progress in defect reduction, alongside failure root-cause identification, advanced screening methodologies and the gaining of a deeper understanding in the underlying physics driving device degradation mechanisms – all have been central priorities throughout the development phase of our GaN technology.

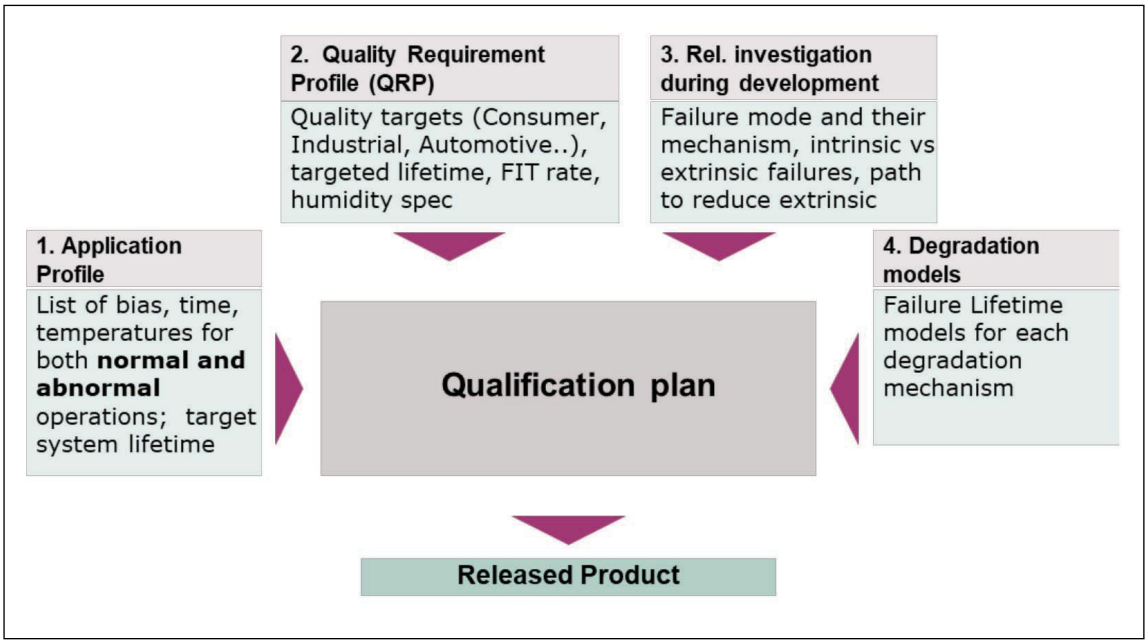
Device failures fall under three categories, analogous to and originally conceptualised by insurance companies in the late 19th and early 20th centuries, to describe mortality rates (see Figure 4). These categories, which correspond to humanity's infant mortality, stable middle years and increased risk of mortality with aging, are: a diminishing early life failure rate; a random (constant) failure rate, and an increasing wear-out failure rate. When considered together, they produce what's commonly described as a 'bathtub' curve, a term coined in the 1950s by aerospace and electronics engineers.

Rigorous methodology

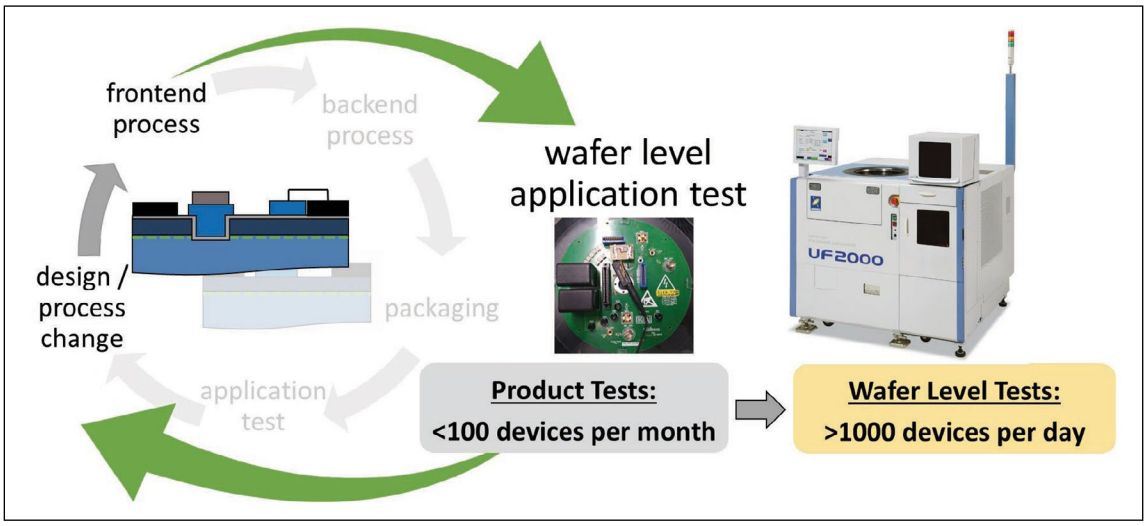
We employ a comprehensive approach to reliability, ensuring that our GaN products meet both the intrinsic (wear out) and the extrinsic (ELFR) failure rates in the field. We use standard JEDEC (Joint Electron Device Engineering Council) tests as a baseline, and turn to rigorous technology and product-accelerated lifetime tests to assess the ELFR and wear-out mechanisms, to estimate failure rates that are tailored to customer-use conditions (see Figure 5).

To make sure that we meet reliability and quality criteria, we apply four inputs to the qualification plan. This approach includes the development of statistically viable failure models, which support our efforts to ensure that we meet the system target operating lifetime.

The qualification of our products begins with capturing the Application Profile, which quantitatively describes the stress conditions faced by the device through its lifetime in



➤ Figure 5. Qualification methodology depicting the main four inputs that drive product release at Infineon Technologies.



➤ Figure 6. Application specific reliability testing (switching DHTOL) at the wafer-level speeds up reliability investigation during development and generates predictive models for lifetime.

the application. We also specify the Quality Requirements Profile (QRP), which states quality targets, such as lifetime and Failure-in-Time (FIT) rates targets. During the technology development phase, we uncover device failure modes and mechanisms for both intrinsic and extrinsic failures, and we identify and pursue a path for extrinsic failures reduction. Efforts also include accelerated reliability testing, undertaken to generate degradation models and estimate lifetime and failure rates at use conditions.

Based on these four pillars, we determine a qualification plan that exceeds the standard JEDEC baseline.

To bring the reliability of GaN electronics to new levels, it's not possible to simply draw on standard techniques established in older material systems. Instead, to break new ground we investigate the reliability of our devices using advanced methodologies that are specifically tailored to the peculiarities of GaN.

One characteristic that's specific to GaN is its propensity for charge trapping in the buffer layers and the first layer of the passivation, as per Figure 1. Another trait is that due to its polar nature, GaN material suffers from mechanical stress. Due to these factors at play, GaN 'breaks down' by failure modes that differ to those of the older material systems of silicon and SiC.

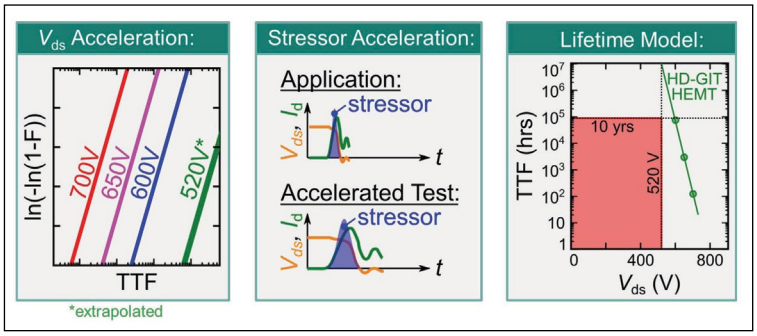
We have developed test systems and methodologies to address just these effects. To consider the dynamic nature of charging, we look closely at Dynamic High-Temperature Operating Life (DHTOL) tests. For this work, we consider the likes of a switching stress to the device under accelerated conditions, mapping all effects of the charge re-distributions specific to GaN.

To speed up our reliability learning, we apply wafer-level test set-ups, with switching electronics fully integrated on the probe card. If we were to test in the classical way, using packaged parts, this would be slower and more cumbersome – before testing could commence, we would need to undertake a full back-end process and packaging. With our wafer-level approach, depending on the test, we can measure several thousand devices per day, rather than as few as possibly tens of devices per month (see Figure 6).

Another strength of our wafer-level DHTOL set-ups is that, thanks to their flexibility, they are well-suited to degradation model learning (see Figure 7). In the simplest way, we measure time-to-failure at 700 V, 650 V, and 600 V, and use the results to extrapolate the failure time for an application bias of 520 V.

We also employ a more advanced approach, tuning switching characteristics. They range from no overlap between the high voltage and the load current (so-called 'soft switching') to a large overlap between the two ('hard switching'), and cover everything in between. This overlap, generating a high energy-loss in the device, acts as a key factor limiting end-of-life reliability. By drawing on this switching locus variation, and employing a new sophisticated stressor model, we are able to model the DHTOL lifetime of processes and technologies during development in GaN application-like conditions.

One of the most challenging tasks we face is generating the extrinsic model that's used to estimate the infant mortality failure rate. In one case,



➤ Figure 7. Wafer-level switching DHTOL uses a sophisticated stressor model based on a switching locus variation to extract the DHTOL lifetime of processes and technologies.

we tested more than 100,000 parts in burn-in ovens at three different accelerated conditions to extract the voltage and temperature acceleration factors (see Figure 6).

These figures are then applied to the application profile, to estimate the extrinsic branch and failure rates through the lifetime of the device (in the example shown (see Figure 8), 15 years lifetime is assured). Note that we have to use such a large statistical sample size, due to the extremely low extrinsic failure rates.

While such efforts are far from trivial, it's crucial to understand the reliability of GaN. Without this, it's not possible to unleash its full, tremendous potential.

FURTHER READING

- C. Ostermaier, "The Role of Defects in the Dynamic Lifetime of GaN Power Devices" IRPS Tutorial 2023
- C. Koller, "Catalyzing Innovation: Bridging System Efficiency to Fundamental Device Physics" IEDM 2024

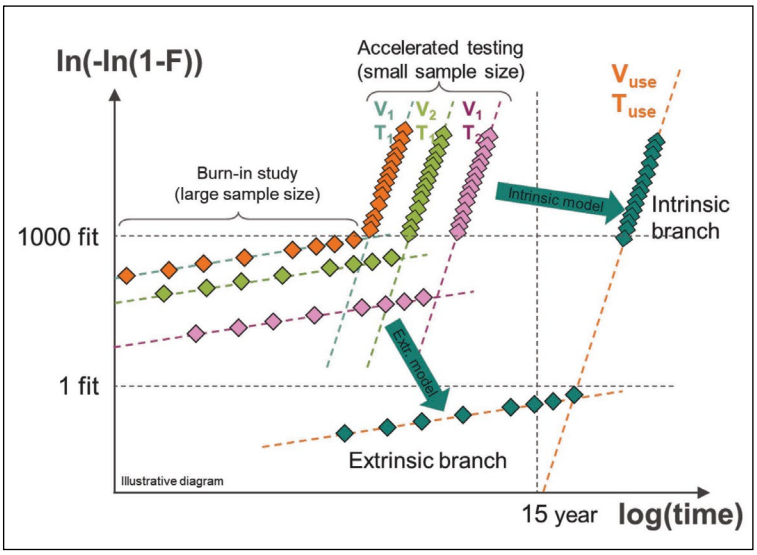
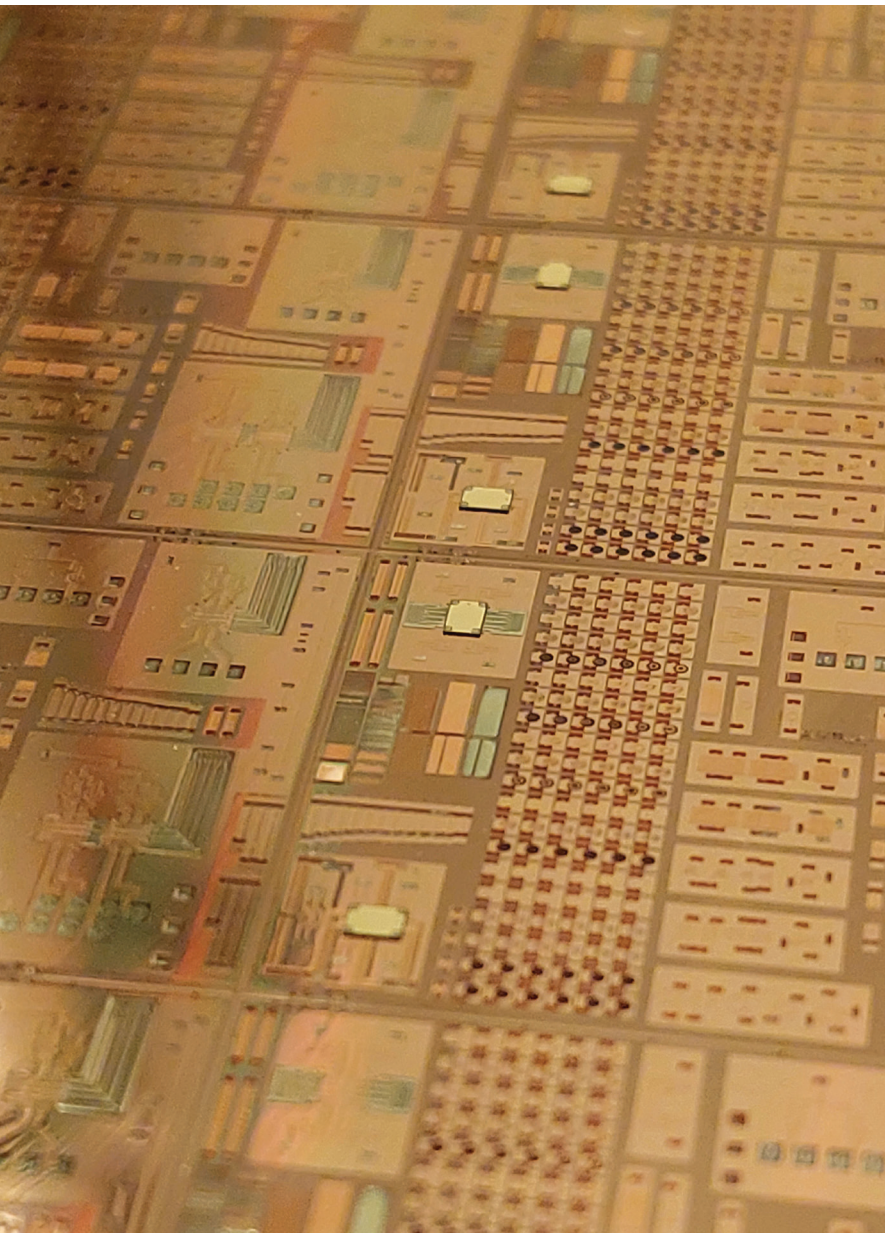


Figure 8. Accelerated life stress testing is undertaken with an extensive sample size, exceeding 100,000 devices, to identify both intrinsic and extrinsic branches. The evaluation applies well-established mathematical models that incorporate the mission profile of the target application.

Unifying III-Vs and silicon with an RF interposer

Compact heterogeneous systems are set to benefit from a RF silicon interposer platform that delivers low-loss, high-density interconnects up to 325 GHz

BY XIAO SUN FROM IMEC



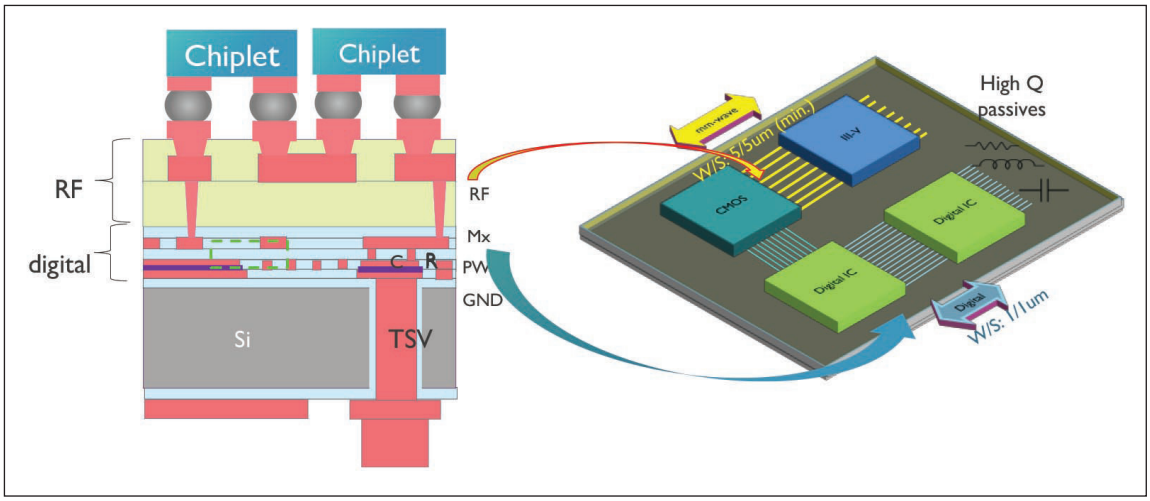
EXTRAORDINARY THINGS happen when you bring together the worlds of silicon and compound semiconductors. It's a marriage that benefits from the scale, manufacturability and integration density of silicon, traits demanded by modern digital systems. And it's a pairing that draws on the strengths of III-Vs, such as InP and GaN, that provide high power, gain, and speed that's essential for millimetre-wave and sub-terahertz front-ends. For decades, these two domains have evolved in parallel, separated by fundamental differences in materials, processing, and cost. But the times, they are a changing.

Helping to bridge the gap is a new RF silicon interposer platform developed by our team at imec. This purpose-built technology is capable of uniting these two disparate worlds, by providing a common substrate that allows InP power amplifiers, SiGe LNAs, and CMOS control logic to coexist, interact, and thrive.

Designed for chiplet-based heterogeneous systems, our platform provides a record-low loss and an exceptionally broadband performance from 20 GHz to beyond 300 GHz. This breakthrough opens the door to next-generation extreme data-rate short-range radio, high-resolution radar, terahertz imaging, and high-speed wireline systems.

Why heterogeneous integration matters

As communication systems move up in frequency to the D-, G-, and J-bands – that's 110 GHz to 170 GHz, 140 GHz to 220 GHz, and 220 GHz to 325 GHz – there are increasingly pronounced trade-offs between speed, power, and integration. There is much to like concerning compound semiconductors, such as InP and GaN, as they continue to deliver superior performance for high-power, high-frequency applications – but they remain expensive, are difficult to scale, and they lack the mature backend infrastructure silicon provides. Due to this



➤ Figure 1. An RF silicon interposer for next-generation high-performance RF and mixed-signal applications.

state-of-affairs, the future of millimetre-wave and sub-terahertz electronics is not about selecting silicon or III-V technologies – it's about integrating them intelligently.

Guided by this philosophy, we have developed a 300 mm RF silicon interposer (see Figure 1) that brings together low-loss, polymer-based RF routing and fine-pitch digital interconnects. With our interposer, one can bridge analogue and digital domains within a single, scalable platform. Our technology features a new portfolio of compact, low-loss, high-Q passive components, alongside thermally managed chiplet assemblies that fully leverage the strengths of each semiconductor technology.

Our journey toward heterogeneous RF integration began with our first-generation silicon interposer, introduced in 2022 and characterised up to 110 GHz. That platform used a moderately resistive silicon substrate (15-25 Ω cm), shielded by a 1 μm copper ground plane, to reduce substrate losses.

This first-generation interposer featured a pair of stacked BCB dielectric layers, implemented to minimise parasitic capacitance and conductor losses. By leveraging BCB's low dielectric loss and stable permittivity, we realised a high-fidelity millimetre-wave interconnect. However, as applications pushed beyond 140 GHz and required additional routing layers, we hit a wall, impaired by the processing limitations of BCB.

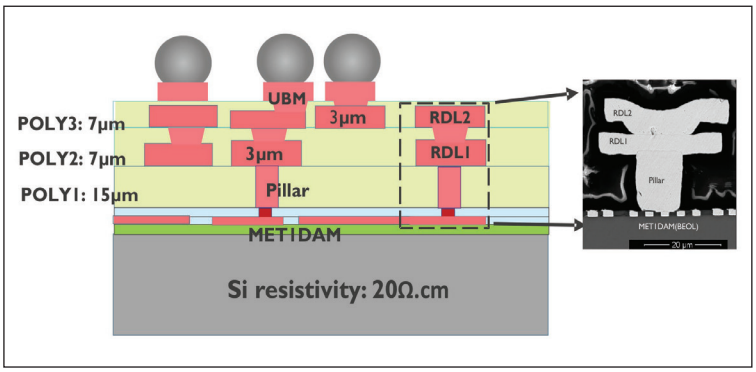
To address this issue, we have developed a second-generation platform, replacing BCB with CYCLOTEN XP80 – it's a photo-imageable, low-loss RF polymer, produced by DuPont and now sold through its spin-off, Qnity Electronics. XP80 is a great polymer, retaining the excellent dielectric properties of BCB while offering better mechanical stability, reduced internal stress and improved processability – qualities that enable the stacking of multiple redistribution layers (RDLs) for higher-density routing. Note that this material is not a 'forever chemical', aligning with the industry's shift toward environmentally safer materials.

Inside the RF Interposer

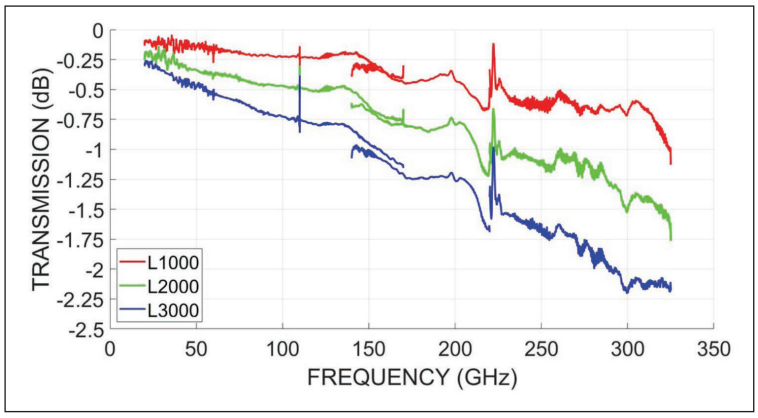
Our latest 300 mm silicon-based RF interposer integrates three thick copper RDLs with three polymer layers to form a multilayer stack capable of routing both RF and digital signals with minimal loss. The layer composition, illustrated in Figure 2, has: a MET1DAM ground plane, which serves as an RF shield, minimising substrate-induced losses in silicon; 15 μm-high copper pillars, which provide vertical connections between the BEOL ground plane and the upper interconnect layers; three XP80 polymer layers (thicknesses 15 μm, 7 μm, and 7 μm), which offer electrical isolation and act as low-loss RF waveguides; copper RDL1 and RDL2 (3 μm-thick each), dedicated to low-loss RF signal routing; a 5 μm-thick 'under-bump utilisation' layer, which supports bump interconnects for die-to-interposer connections; and CuNiSn micro-bumps, enabling thermocompression bonding of InP, GaN, or CMOS dies.

By supporting routing pitches of 5/5 μm for RF lines, and 1/1 μm for digital interconnects, this advanced stack delivers the integration density and performance required for next-generation mixed-signal and heterogeneous systems.

The greatest triumph of our interposer is its ultra-low transmission loss, a critical metric for millimetre-



➤ Figure 2. An RF silicon interposer demonstrator consists of a standard, low-resistivity silicon substrate, a full ground shield, three spin-coated low RF loss polymer layers (POLY1, POLY2, POLY3), three thick metal layers (RDL1, RDL2, UBM) and micro-bumps.

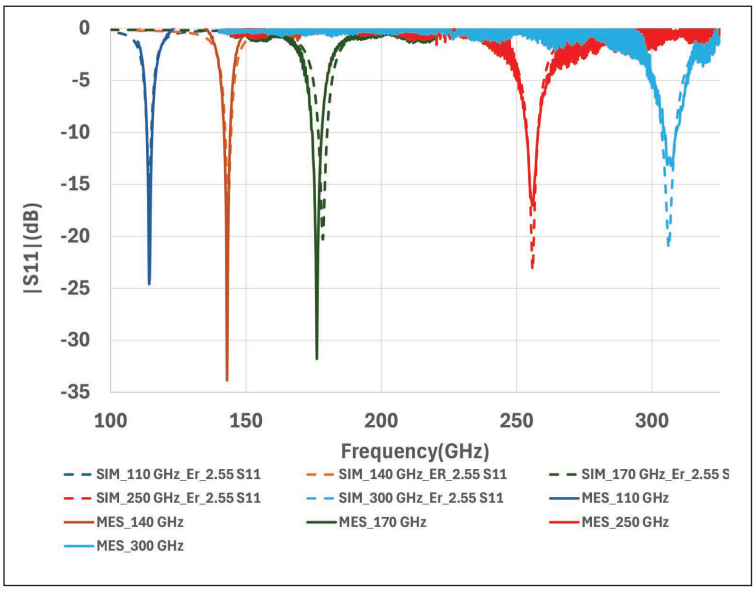


➤ Figure 3. Insertion loss for 1 mm, 2 mm, and 3 mm long microstrip lines on RDL2.

wave packaging. According to our characterisation of microstrip lines of 1-3 mm, based on frequencies from 20 GHz to 325 GHz and using thru-reflect-line calibration, at 140 GHz insertion losses are 0.30 dB mm^{-1} and 0.23 dB mm^{-1} for RDL1 and RDL2, respectively, and the corresponding reflections are below -19 dB and -22 dB. At the higher frequencies of 220 GHz and 325 GHz, losses remain below 0.6 dB mm^{-1} and 0.9 dB mm^{-1}, respectively.

To put these figures in perspective, note that they are comparable to or better than those for advanced glass interposers and PCBs (see Figure 3). The lower losses are much valued, as they translate directly into a higher amplifier efficiency and better signal integrity, essential for compound semiconductor modules. By combining smooth copper surfaces with the XP80's low loss tangent, stable performance is possible, even up to the J-band, a milestone for sub-terahertz packaging.

It is essential to have precise knowledge of XP80's dielectric properties when co-designing interconnects, antennas, and high-Q passives. We have equipped ourselves with this information by using patch-antenna and resonator-based methods to extract the dielectric constant and loss tangent up to 325 GHz (see Figure 4).



➤ Figure 4. Comparison between measured and simulated reflection coefficients using an adjusted substrate permittivity of 2.55.

For this work we used microstrip patch antennas, designed for 110 GHz, 140 GHz, 170 GHz, 250 GHz, and 300 GHz. The measured results, closely matching simulations, provide values of 2.6 for the relative permittivity and 0.009 for the dielectric loss tangent. After tuning simulations to match our measurements, we derived an average relative permittivity of 2.55, with a variation across the full frequency range of just ±1.5 percent. After confirming these values with resonator structures, including ring and gap-coupled types, we concluded that we had produced broadband impedance-controlled interconnects.

Thermal management

Outstanding electrical performance counts for little, unless it's accompanied by effective thermal control. In high-power modules, InP and GaN amplifiers may generate intense heat – as high as several watts per millimetre of gate width – making thermal management a defining factor for reliability and lifetime.

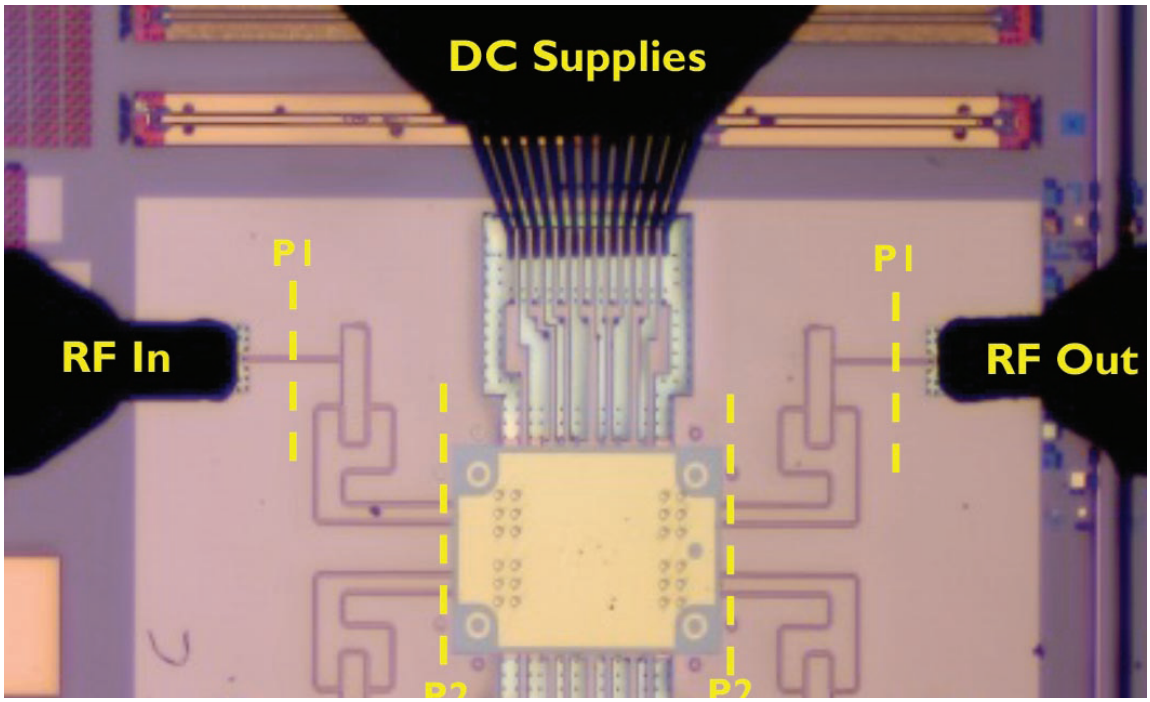
To tackle this challenge, we have built thermal intelligence directly into our RF silicon interposer. This is realised through seamlessly embedding microscale heaters and sensors within the RDL and back-end-of-line layers, where copper meanders – just 200 μm by 200 μm in RDL1 and 100 μm by 100 μm in MET1 – act as both heat sources and precise temperature monitors.

By combining on-chip measurements with advanced finite-element modelling, we have determined a thermal conductivity for the XP80 polymer of around 0.15 W m^{-1} K^{-1}. This insight, key to accurate thermal prediction and co-design, ensures that even high-power III-V die operate safely and efficiently, thanks to effective thermal-mitigation strategies.

In short, we have a proven platform that ensures RF performance and thermal reliability go hand-in-hand – supporting the next-generation of compact, high-power, and thermally balanced millimetre-wave and sub-terahertz systems.

As the ultimate proof of this concept, we have co-packaged a two-stage differential InP power amplifier – designed using Teledyne's 250 nm InP HBT process – directly onto our RF silicon interposer (see Figure 5). Fabrication involved flip-chip bonding of the die via CuNiSn micro-bumps, with the entire assembly process kept below 250°C to protect delicate InP back-end metallisation.

Measurements of post-assembly performance confirm that our interposer introduces no measurable degradation (see Figure 6). This effort



➤ Figure 5. Top view of an InP chiplet mounted on the RF silicon interposer showing RF input/output and DC probes.

has determined a small-signal gain of 16.3 dB, a 3 dB bandwidth that spans 116 GHz to 148 GHz, an input/output match that's better than -10 dB, and a reverse isolation of -40 dB.

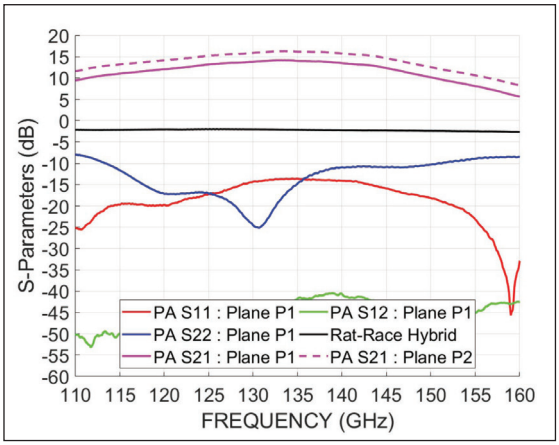
When driving this co-packaged system under large-signal operation at 130 GHz, we recorded a value for P1dB – that's the input or output power level where the device's gain drops by 1 dB from its ideal linear gain – of 13-15 dBm. Power-added efficiency (PAE) is between 15 percent and 28 percent (see Figure 7), closely matching the performance of standalone InP power amplifiers.

The key point to be taken from these results is that our silicon interposer technology introduces virtually no parasitic penalty, validating the precision of our design and fabrication processes. Our success is a major step towards fully co-packaged III-V and silicon systems, where high power meets high integration on a single scalable platform.

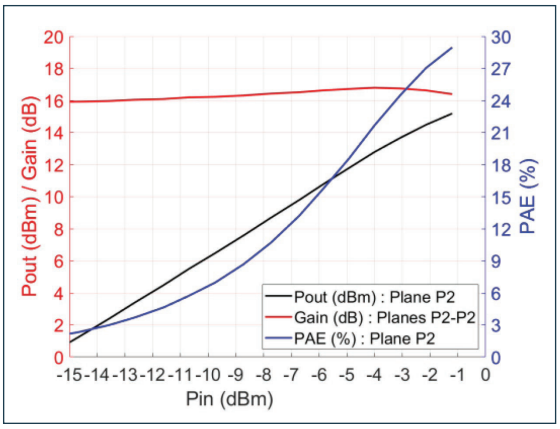
Serving compound semiconductor systems

There has been little change in the semiconductor status quo over the last few years. Silicon continues to dominate logic and memory, while compound semiconductors, such as InP and GaN, excel in RF and photonic performance.

Our RF silicon interposer brings these strengths together, providing a CMOS-compatible, 300 mm manufacturable substrate for scalable integration of compound chiplets. With this approach, as well as enabling high-density routing, our platform offers a thermal advantage, with silicon providing a superior thermal conductivity to glass and PCB, enabling better heat dissipation. Another merit of our technology is that it's fully compatible with 300 mm



➤ Figure 6. Solid lines represent the small signal S-parameters of the PA at reference plane P1. By subtracting the loss of the rat-race hybrid (black line) from the S21 of the PA between P1-P1 (solid magenta), the reference plane can be shifted to the S21 of the PA between P2-P2 (dashed magenta).



➤ Figure 7. Large signal parameters of the PA at 130 GHz between reference planes P2-P2.

wafer processing in standard CMOS fabs, ensuring manufacturability at scale.

With our architecture, InP and GaN chiplets may be minimised to their active PA cores, while biasing, filtering, and impedance matching are migrated to the interposer. The upshot is a truly heterogeneous system with smaller footprints, lower cost, and higher yield, combining the high performance of III-V devices with the scalability and integration density of silicon.

As our interposer supports multi-band modules, operating from 20 GHz to 325 GHz and thus covering the D-, G-, and J-bands, it is ideal for future high-capacity wireless links, radar, and sensing systems. Its combination of sub-terahertz signal integrity, low-loss routing, thermal co-design, and dense chiplet integration sets a blueprint for next-generation heterogeneous architectures.

In short, our second-generation RF silicon interposer bridges the divide between silicon and compound semiconductors. Particularly noteworthy is XP80 polymer-based RF routing, a low-loss performance up to 325 GHz, and a built-in thermal co-design for reliable high-power operation. These assets have helped us to successfully co-package a fully functional InP D-band amplifier without performance degradation, and to ultimately demonstrates the feasibility of heterogeneous systems, where InP, GaN, SiGe, and CMOS operate side by side.

As the world advances toward next-generation wireless and wireline communications, sub-terahertz sensing, and ultra-fast radar, our interposer stands as more than a packaging solution – it's the bridge between the precision of silicon and the power of III-Vs.

This work was carried out by the imec teams, with support from Qnity Electronics for the XP80 polymer materials. The author thanks imec colleagues involved in RF interposer design, fabrication, assembly, dielectric characterisation, and thermal modelling for their valuable contributions – Siddhartha Sinha, Martijn Huynen, Reinier Broucke, Melina Lofrano, Vladimir Cherman, Angel Uruena, Ehsan Shafahian, Damien Leech, Nazia Fathima, Andy Miller and Eric Beyne – as well as Nadine Collaert and Joris Van Driessche for their support through the ARF programme.

FURTHER READING

- X. Sun *et al*., "Cost-effective RF interposer platform on low-resistivity Si enabling heterogeneous integration opportunities for beyond 5G," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 7-11.
- S. Sinha *et al*., "Hetero-Integration of InP Chiplets on a 300 mm RF Silicon Interposer for mm-wave Applications", 2024 IDEM, San Francisco, 7-11 December 2024
- X. Sun *et al*. "RF Si interposer platform for chiplets based heterogenous systems", 2025 IEEE 75th Electronic Components and Technology Conference (ECTC), Dallas, USA, 2025

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In the 40 years since its inception, CS MANTECH has broadened its scope beyond GaAs technologies, growing to become internationally recognized as the premier technical conference for compound semiconductor manufacturing. We have been steadfast in maintaining the core objective set forth from the 1st conference by He Bong Kim and Jim DiLorenzo (1st Technical Program Chair) in our mission to 1. Bring together professionals from industry, academia, and government organizations, and 2. Provide a forum to exchange and discuss new ideas that propel our industry forward.

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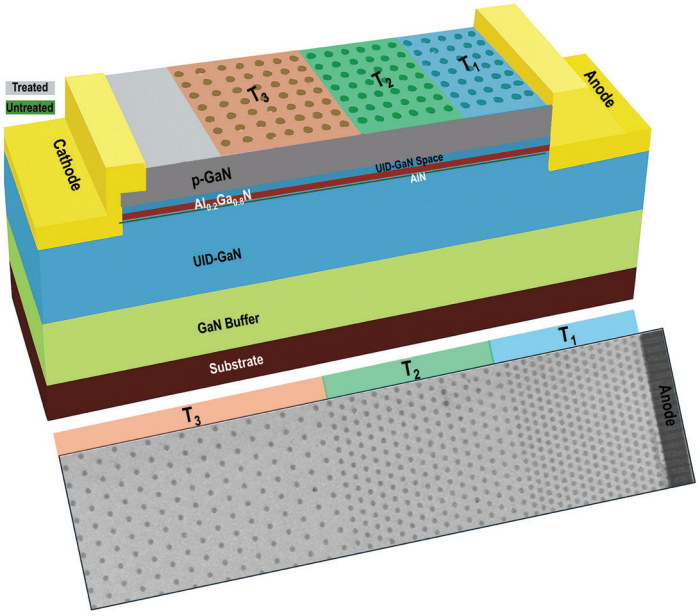
A new approach for 10 kV GaN

A simple plasma-based edge termination approach yields 10 kV-class GaN diodes with a lateral geometry

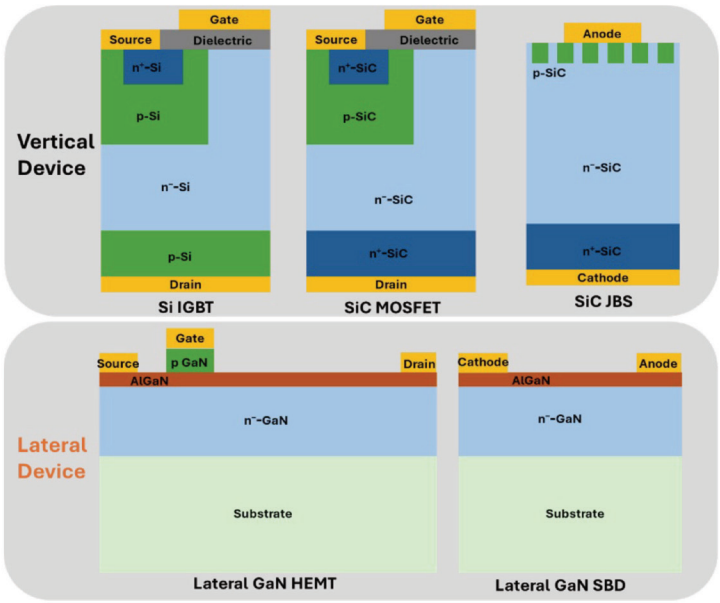
BY DAWEI WANG AND HOUQIANG FU
FROM ARIZONA STATE UNIVERSITY



➤ Figure 1. Commercial high-voltage vertical silicon and SiC power devices (top) and lateral GaN power devices (bottom).

AMONG the competing semiconductor technologies for power electronics, GaN already enjoys significant success. This material delivers an unrivalled performance when there's a need to block several hundred volts and provide very low power losses. Thanks to these attributes, GaN power devices have established a 'killer' application in fast chargers for a range of mobile devices.

Where GaN is yet to make a commercial impact is at voltage ratings of 1.7 kV and more, which are critical for applications like the electric grid, wind turbines, electric drives, and high-voltage power supplies. At these high blocking voltages, the commercial products that are available include silicon insulated-gate bipolar transistors (IGBTs) and thyristors (up to 6.5 kV), and SiC MOSFETs and junction barrier Schottky (JBS) diodes (up to 10 kV). In the labs, researchers have even demonstrated SiC transistors and diodes withstanding up to 30 kV.



However, silicon and SiC devices have significant drawbacks. Due to a bipolar nature, with both majority and minority carriers, high-voltage silicon IGBTs and thyristors are only capable of low switching frequencies and suffer from high switching loss. That's not an issue for unipolar SiC MOSFETs and JBS diodes, which offer similar high-voltage ratings, and can operate at much higher switching frequencies, thanks to majority-carrier operation. However, commercial SiC high-voltage devices are produced on expensive SiC substrates and need thick epitaxial layers, requirements that lead to an elevated cost per die, due to increased chip size and low yield at high voltages.

A potential solution is to increase the operating voltage of GaN power devices, as they have many strengths, including the capability to combine higher efficiencies and temperatures with a reduced footprint, minimal cooling requirements and robust operation. When compared with silicon devices, their far wider bandgap enables either higher voltage ratings with the same thickness, or a similar voltage rating with far less material. Another

attribute is the creation of a two-dimensional electron gas with a high mobility, key to allowing GaN power devices to switch far faster than those based on both silicon and SiC. What's more, GaN power devices can leverage the existing fabrication infrastructure from the mature GaN LED industry for performance improvement, cost reduction, and manufacturability.

At Ariona State University we are working to unleash the capabilities of GaN at high blocking voltages with a simple, damage-free process for producing devices with a lateral geometry.

High-voltage GaN

Uniting commercial high-voltage silicon and SiC power devices is their vertical device geometry. Benefits of this architecture include a high current and a high-voltage capability, a small chip size, immunity to surface issues and good thermal performance.

In contrast, commercial GaN power devices are predominantly lateral high-electron-mobility transistors (HEMTs). This design, used for voltages up to 900 V, offers a low junction capacitance, a high switching frequency, and a low switching loss. What's more, the lateral GaN HEMT platform facilitates the monolithic integration of power transistors, drivers, and auxiliary circuits, dramatically reducing the footprint of power electronics and quashing parasitic effects, such as gate ringing and false turn-on.

Within the GaN research community, some effort has been directed at vertical power devices. This has led to demonstrations of transistors and *p-i-n* diodes with blocking voltages up to 2-5 kV.

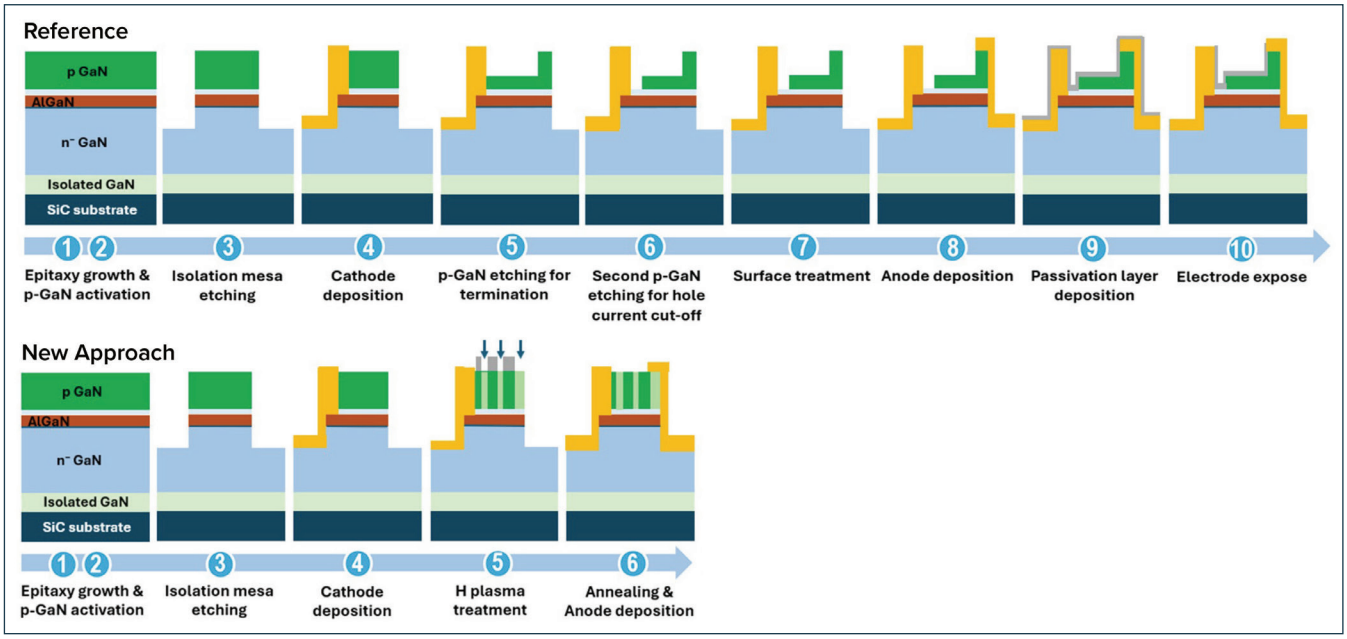
However, for high-voltage applications, lateral GaN power devices based on the HEMT platform are very attractive alternatives to GaN and SiC vertical devices. Key merits include growth on cost-effective substrates, such as sapphire and silicon, and the need for just a fraction of the epitaxial layer thickness required for 10 kV vertical power devices. Due to these advantages, there have already been demonstrations of prototype 10 kV-class diodes and transistors on the GaN HEMT platform – they feature superjunctions, multiple channels, and reduced-surface-field (RESURF) structures.

When designing and fabricating 10 kV-class devices, a non-uniform electric field distribution is a major challenge – and unfortunately, this is exacerbated in lateral devices. The electric field tends to concentrate at device edges, causing premature device breakdown at these locations. To address this shortcoming, engineers employ edge termination, an indispensable addition for 10 kV-class power devices that smoothens the electric field distribution.

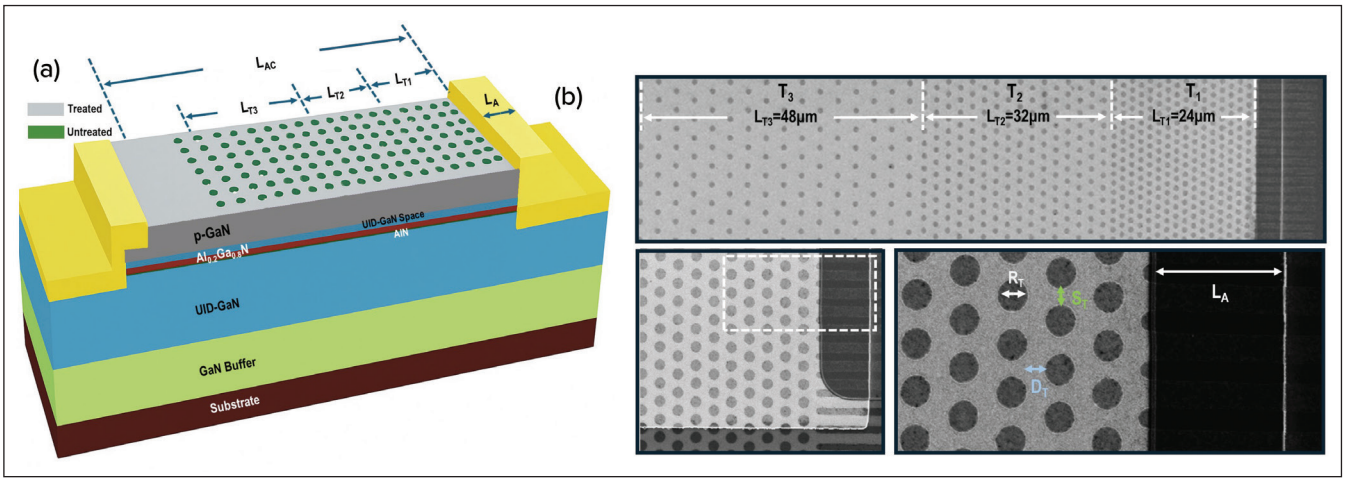
Unfortunately, that's not the only modification – 10 kV-class GaN devices that have been reported usually require complicated designs, in terms of device epitaxial structure, edge termination and passivation, as well as the need for extra fabrication steps in etching, dielectric deposition, and surface treatment. That's far from ideal, because complicated fabrication processes threaten to impair device yield and reliability, and often lead to a hike in fabrication costs.

Simplifying edge termination

Against this backdrop we are proposing a simple edge termination approach for fabricating 10 kV-class GaN power devices. What makes it simple? Well, it avoids etching and passivation processes (for an illustration of our proposed plasma-based edge termination for lateral GaN power devices on the commercial GaN HEMT platform, see Figure 2).



➤ Figure 2. Representative fabrication processes for high-voltage lateral GaN power devices using a reference approach (top) and our new approach (bottom).



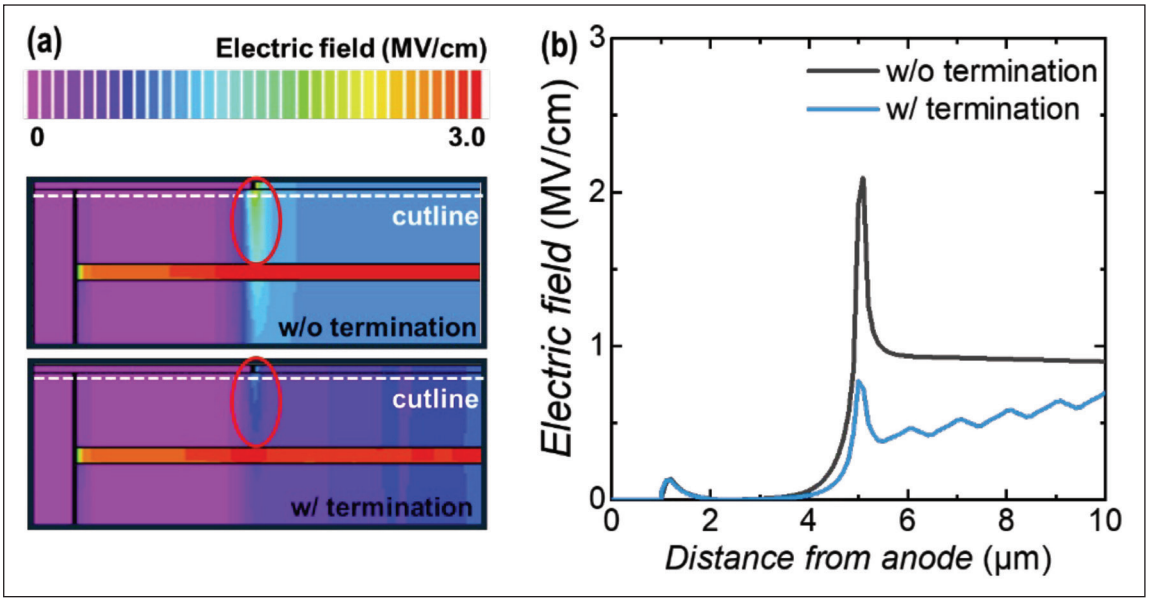
➤ Figure 3. (a) Schematic of high-voltage lateral GaN diodes with the plasma-based edge termination. (b) Top-view scanning electron microscopy images of the device at different magnifications.

Eliminating etching is a significant step forward, because this process can cause surface damage, and post-treatment and passivation is often needed to alleviate detrimental device effects. Another benefit is that there's no longer the need for precise etching, required for some of the reported 10 kV GaN devices. Precise etching is not easy, as one has to consider the thin-film thickness, film uniformity, and etching rate fluctuation. But with our approach, as well as low surface damage that comes from the absence of etching, there's inherent passivation – so no additional passivation is needed.

Our device structure consists of a thick GaN buffer layer, an unintentionally doped layer of GaN, an AlN space layer, an AlGaN layer, another unintentionally doped layer of GaN that acts as a space layer, and *p*-type GaN layers. Our plasma-based edge termination is realised through conductivity tuning of the top *p*-GaN layer, and formation of arrays of treated and untreated *p*-GaN regions by a hydrogen plasma process (see Figure 3 (a)). We use a hydrogen plasma, created in a traditional inductively coupled plasma etching tool, to selectively inject hydrogen atoms into the *p*-type GaN layer. Once the hydrogen atom is bound to the magnesium acceptors in the *p*-type GaN, charge-neutral magnesium-hydrogen complexes are formed, rendering the hydrogen-plasma-treated *p*-type GaN highly resistive.

To assess the feasibility of our proposed plasma-based edge termination approach, we have turned to TCAD simulations. This allowed us to evaluate the impact of edge termination, employed to reduce peak electric fields and realise a more uniform electric field distribution (see Figure 4 for the simulated electric-field distributions in devices with and without our proposed edge termination).

What's clear from our simulations is that there's one single, large electric-field peak at the edge of the



➤ Figure 4. (a) Simulated electric field mapping for the lateral GaN diodes with and without the plasma-based edge termination. The circled regions indicate high-electric-field locations. (b) The extracted electric field distribution along the cutlines in (a).

anode in the device without the edge termination. Once edge termination is introduced, so long as the conductive *p*-GaN layer near the anode is partially retained, there is a dramatic suppression in the peak electric field in this vicinity, leading to a more uniform electric field distribution. We have found that crucial to realising a very high breakdown voltage is optimisation of the geometry of edge termination.

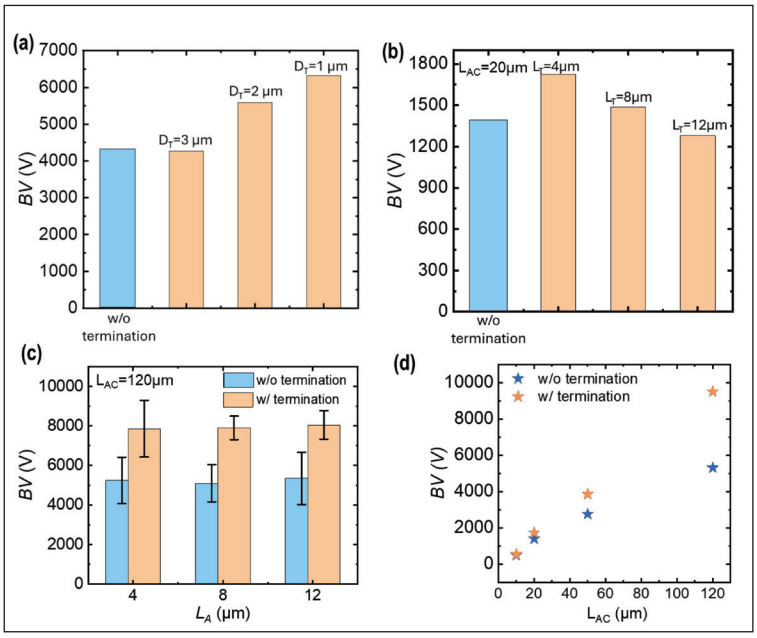
In addition to our simulations, we have fabricated and characterised devices, forming an array of circular structures, with hydrogen plasma treatment providing the edge termination of the top *p*-GaN layer. This involves treating the outside of the circular areas of *p*-GaN with a hydrogen plasma, to ensure they are resistive; and not treating the inside of the circular areas, so they retain their conductivity. Note that this difference in conductivity is visible in scanning electron microscope (SEM) images (see Figure 3 (b)).

We have investigated the performance of our diodes by adjusting various design parameters. All our devices have three array regions, designed and denoted as regions T_1, T_2, and T_3, with increasing length L_T from the anode to the cathode (see Figure 3 (b)). In each array, there are three important design parameters: the vertical spacing between each circle (S_T), the lateral spacing between each circle D_T, and the diameter of the circle R_T. In our design, we increase S_T and D_T from 0.5 μm to 2 μm from region T_1 to T_3, while maintaining R_T at 0.75 μm. These dimensions are selected to promote the distribution of the electric field – rather than crowding at the edge of the anode, the electric field is spread over the whole surface between the anode and the cathode at reverse bias. To provide a benchmark, we also fabricated a reference device, free from edge termination.

Operating under forward bias, our devices show excellent rectifying behaviour. The turn-on voltage is 1.1 V, the ideality factor is around 1.5, the on/off ratio is 10^{10}, and the on-resistance 97 Ω mm. However, the device with the plasma-based edge termination has a current degradation of around 15 percent, due to the partially depleted 2DEG channel from the untreated *p*-GaN. Encouragingly, device on-resistance scales linearly with anode-to-cathode length (L_{AC}), indicating dominant channel resistance and negligible contact resistance; and repetitive forward and backward current-voltage scans show good stability under forward bias.

Device capacitance at 0 V is 4.2 pF mm^{-1}, and is mostly independent of L_{AC}; and cut-off frequency is inversely proportional to capacitance and on-resistance, and increases from 0.8 GHz to 8.4 GHz as L_{AC} decreases from 120 μm to 10 μm. We also find that as anode length (L_A) increases, so does device capacitance, driving a decrease in device frequency.

When we run our device under reverse bias, we are able to investigate the effects of plasma-based edge termination on device breakdown. This study has involved a simplified edge termination structure that only has region T_1, and considered the relationship between the lateral spacing between circles, D_T – that's the density of the plasma treated area – and the length of region (L_T).



➤ Figure 5. (a) The impact of different D_T on device breakdown voltages. (b) The impact of different L_T on device breakdown voltages. (c) Comparison of high-voltage lateral GaN diodes with and without the plasma-based edge termination. (d) Device breakdown voltage as a function of L_{AC} with or without the plasma-based edge termination.

We have determined that reducing D_T – so moving to a larger circle density – helps to increase device breakdown. However, when D_T is too large, there is only a minimal gain in the device's breakdown voltage, with values comparable to those of devices without edge termination (see Figure 5 (a)). This result indicates that to ensure better electric-field management, the D_T of hydrogen plasma treated regions must be small.

As part of this investigation of device characteristics under reverse bias, we have investigated the influence played by the length of region L_T, considered at an L_{AC} of 20 μm. We have found that a larger L_T leads to lower device breakdown voltage, due to stronger electric field crowding at the edge of the termination structure (see Figure 5 (b)).

Finally, we fabricated 10 kV-class GaN diodes with L_{AC} of 120 μm. Generally speaking, plasma-based edge termination increases the device average breakdown voltage by about 3 kV. We obtained a maximum breakdown voltage for a device with the plasma-based edge termination of 9.5 kV, compared with just 5.3 kV for the device without edge termination (see Figure 5 (c)). Variations in L_A show minimal impact on device breakdown voltages. The

relationship between the maximum breakdown voltage and L_{AC} indicates that plasma-based edge termination provides a stronger boost for breakdown voltages at larger L_{AC} (see Figure 5 (d)).

Benchmarking

We have benchmarked the performance of our device against state-of-the-art lateral and vertical GaN and Ga_2O_3 Schottky diodes (see Figure 6). Our diode has a Baliga's figure of merit of 0.79 GW cm^{-2}, comparable to that of 10 kV-class GaN and ultrawide bandgap Ga_2O_3 Schottky diodes.

It's worth remembering that we have realised state-of-the-art performance with a very simple device structure, produced using simple, low-cost fabrication processes. And one should note that our edge termination technology can be transferred to other plasma-based or implantation-based fabrication processes.

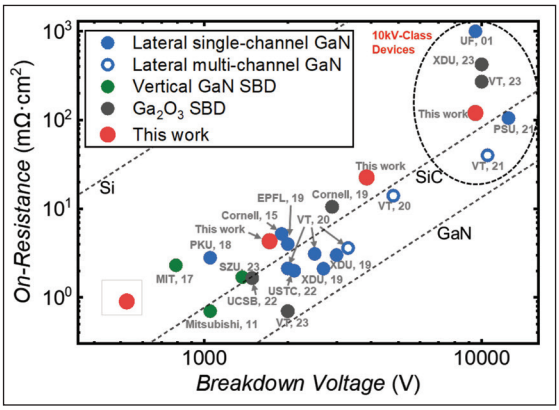


Figure 6. Comparison of on-resistance and breakdown voltage for state-of-the-art high-voltage GaN and Ga_2O_3 power Schottky diodes.

In short, our work provides an alternative avenue for realising cost-effective 10 kV-class GaN power devices. To further assess the potential of our approach, we will evaluate dynamic switching performance, long-term high-voltage stability, avalanche capability, and device packaging. These investigations will increase the maturity of our technology.

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- D. Wang *et al*. "Multi-kV AlGaN/GaN Heterojunction Schottky Barrier Diodes with Hydrogen Plasma Guard Array Termination", IEEE Electron Dev. Lett. **46** 960 (2025)

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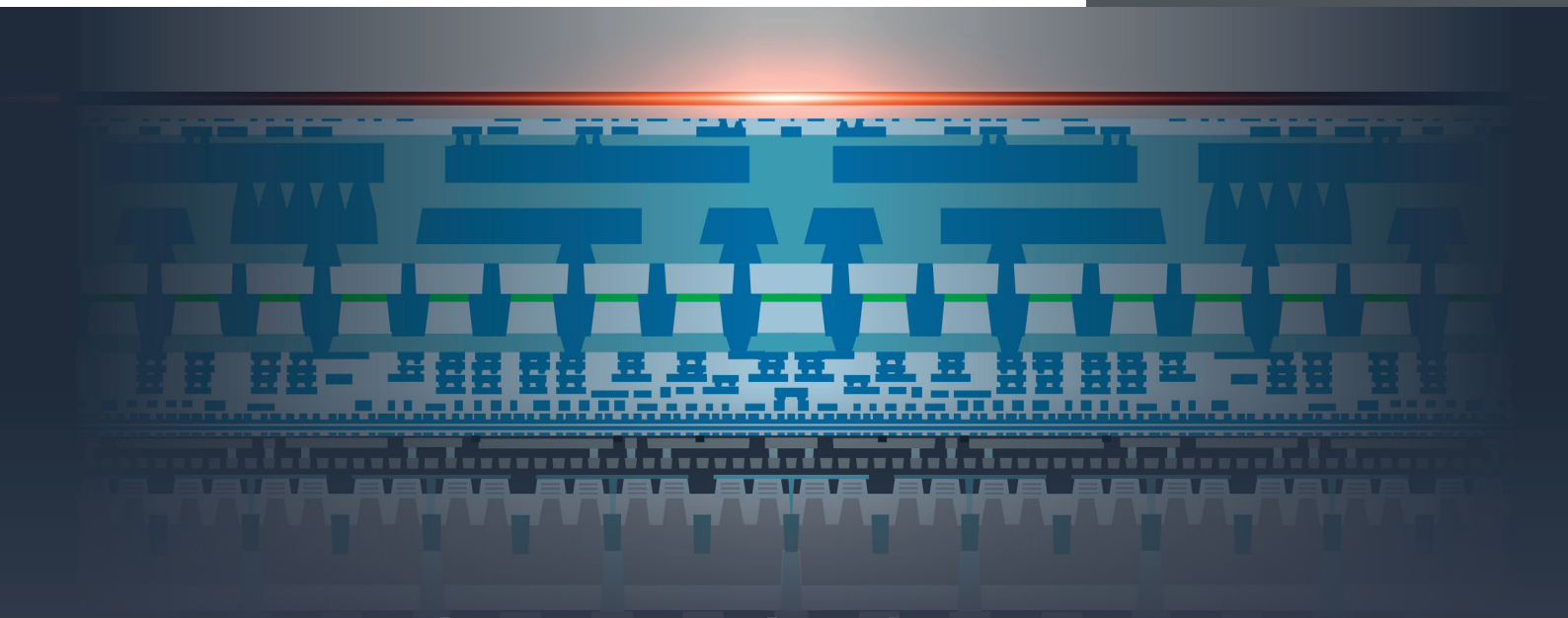

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Accelerating GaN-on-silicon RF power amplification

Driving power amplification beyond 100 GHz positions the GaN-on-silicon HEMT as a strong candidate for sub-terahertz 6G communication

BY GEOK ING NG FROM NANYANG TECHNOLOGICAL UNIVERSITY AND AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH, SINGAPORE

AS HUMANITY enters a hyperconnected era that's driven by phenomenal leaps in AI, it is critical to roll-out a robust infrastructure that supports this revolution. This means upgrading the capabilities of data centres and telecommunication networks, with the latter needing to accommodate extremely high 6G data rates of around 1 Tbit s^{-1}. It's a requirement that will be fulfilled with massive arrays of compact cells operating in the sub-terahertz range – a domain that must be employed, because channels with bandwidths as wide as tens of gigahertz are only possible in relatively unexplored sub-terahertz frequencies.

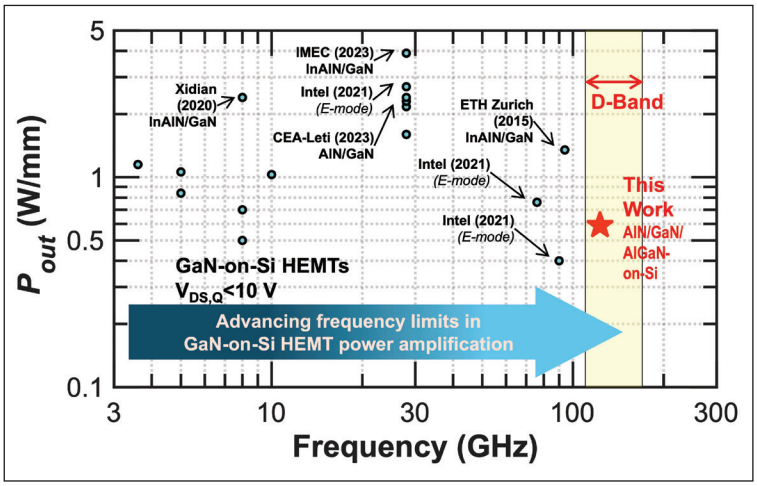
The development of technologies for producing and amplifying these frequencies will provide benefits extending beyond telecommunication networks. Progress will also aid: highly automated smart factories, by helping radar sensors to offer millimetre-level precision detection; and support the development and production of test instruments operating up to the D-band (110 GHz to 170 GHz) and beyond.

With all these factors at play, it's not surprising that there's tremendous interest in low-cost, high-performance semiconductors operating in the D-band.

It's a frequency range that's within reach for a number of established compound semiconductor technologies, notably InP HBTs, and GaN-on-SiC HEMTs.

Another candidate is the GaN-on-silicon HEMT, a relatively new contender that is yet to receive much attention. What it offers over its rivals is the compelling combination of superior material properties associated with III-N heterostructures and the widespread availability of large-diameter (up to 300 mm) silicon substrates, which enable a sizeable cost reduction that can spur the broad adoption of these ultra-high frequency systems.

Over the years, rapid progress in GaN-on-silicon HEMT technology has failed to go hand-in-hand with an expansion in the frequency range for power amplification. This is still confined to the Ka band (26.5 GHz - 40 GHz) and W band (75 GHz - 100 GHz) – a limitation that reveals that there's a great opportunity to advance the GaN-on-silicon HEMT for D-band power amplification (see Figure 1).



➤ Figure 1. Benchmarking the output power (P_{out}) as a function of frequency for GaN-on-silicon. To the best of the authors' knowledge, this work advances the frequency limits of GaN-on-silicon HEMT power amplification into D-band for the first time.

Critical to the fabrication of every high-performance GaN transistor is the epitaxial structure and device design. The D-band GaN-on-silicon HEMT is no exception.

Answering the challenge is our team, led by researchers at Nanyang Technological University and involving contributions from various institutions in Singapore, including the National Semiconductor Translation and Innovation Centre for Gallium Nitride, Agency for Science, Technology and Research (A*STAR); Institute of Microelectronics, A*STAR; Singapore-MIT Alliance for Research and Technology; and National University of Singapore.

Our latest progress with RF GaN-on-silicon HEMTs, involving amplification at unprecedented frequencies, draws on our previous expertise with these devices.

We have considerable experience employing *in-situ* SiN/AlN/GaN/AlGaN heterostructures by MOCVD. These epi-stacks feature an AlN barrier just 5 nm-thick – it provides strong polarisation that results in a high charge density of 1.7 x 10^{13} cm^{-2}. Our design also incorporates an AlGaN back barrier that provides good 'vertical scaling', by ensuring excellent carrier confinement.

A feature of our HEMTs is their *in-situ* SiN layer, designed to serve two purposes: passivation and a gate dielectric. By applying a thin passivation layer, we hope to strike a balance between surface passivation and parasitic capacitance. We view our design as an 'educated guess' for an optimal D-band GaN-on-silicon HEMT.

Fabrication of our transistors began with the use of chlorine-based inductively coupled plasma reactive ion etching to provide mesa isolation. We then formed alloyed Ti/Al/Ni/Au ohmic contacts, which provide a contact resistance of 0.3 Ω mm. Note, though, that it's possible to realise an even lower resistance with re-grown contacts formed by either MBE or MOCVD. We employed the Ni/Au stack for T-shaped gates, defined prior to atomic layer deposition of 10 nm-thick Al_2O_3 at 300°C.

Thanks to the thin passivation structure, consisting of 5 nm-thick SiN grown *in situ* with the AlN/GaN stack, plus 10 nm-thick Al_2O_3, our HEMTs have decent current collapse characteristics. This is accomplished while ensuring that parasitic capacitance, which may limit high-frequency performance, remains as low as possible.

Dimensions for our device are a gate length of 140 nm and a source-to-drain distance of 1.3 μm. We use a small gate finger width – it is 2 x 16 μm – to reduce signal propagation delay along the width direction, enabling an increase in gain.

Our devices deliver excellent DC characteristics, including a maximum drain current of 2.0 A mm^{-1}, an on-resistance of 1.1 Ω mm, and a maximum transconductance of 0.65 S mm^{-1}. Breakdown voltage is 35 V, limited by breakdown at the drain edge of the gate. According to RF small-signal measurements at a drain voltage of 10 V, and modelling with a small-signal model, values for

Our next step is to boost the performance of our GaN-on-silicon HEMTs for high-frequency power amplification. These efforts, including refinements to epitaxy, will focus on reducing the RF loss of the GaN-on-silicon substrate and increasing mobility through a reduction in intermixing in the AlN/GaN heterostructure

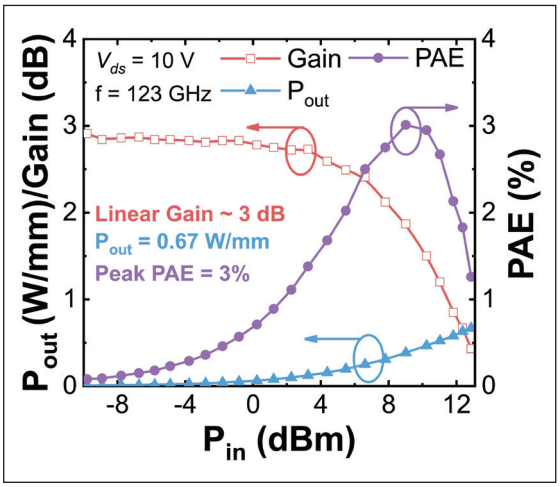


Figure 2. RF large-signal performance at 123 GHz in continuous wave (CW) mode, and V_{ds}=10 V. A maximum P_{out} of 0.67 W mm^{-1} is achieved.

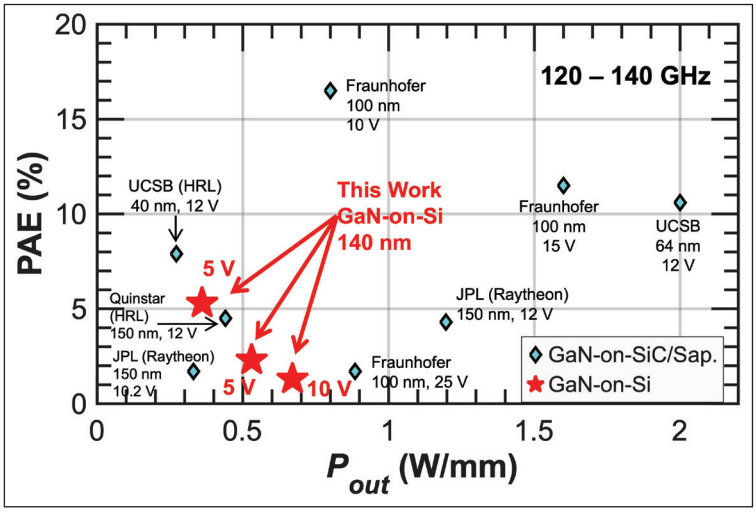


Figure 3. Benchmarking RF large-signal performance of GaN HEMTs and MMICs at 120 GHz – 140 GHz, in terms of PAE and P_{out}. The gate length and V_{ds} are specified. The name of the foundry, if different from the publishing affiliation, is written in parentheses. All epitaxial structures are metal-polar, unless otherwise specified. All reports are pre-matched GaN MMICs, except this work, which is a GaN HEMT with external load/source impedance tuning. In the case of MMICs, P_{out} is normalised by the gate periphery of the final stage transistor.

the cut-off frequency and the maximum oscillation frequency are 112 GHz and 205 GHz, respectively.

The highlight of this work is the RF large-signal performance at D-band, determined with an on-wafer D-band passive load-pull system. These measurements were obtained with a vector network analyser (VNA, Agilent N5247B) with VNA extenders (VDI WR6.5) as the signal source.

We employed passive tuners (Focus W1701100BV) at the fundamental frequency of 123 GHz for source and load tuning. Calibration was conducted for the VNA extender, input coupler, tuners, probes, power source, and power receiver, in that sequence. After performing power calibration, the signal source provided power ranging from -10 to 10 dBm.

Measurements on our HEMTs involved a drain-source voltage of 5 V, which is a supply voltage that's favourable for mobile user equipment. Using continuous wave (CW) Class AB operation, and tuning for optimal power-added efficiency (PAE), we recorded a maximum output power of 0.53 W mm^{-1}, and an associated PAE of 2.3 percent. Increasing the drain-source voltage to 10 V boosted the maximum output power to 0.67 W mm^{-1}, realised with an associated PAE of 1.3 percent (see Figure 2). The peak drain efficiency is 27.5 percent.

Benchmarking RF large-signal performance reveals that our GaN-on-silicon HEMTs produce a promising performance when compared with GaN-on-SiC HEMTs operating at a similar drain-source voltage (see Figure 3). What's more, we have extended the frequency limits of GaN-on-silicon HEMT power amplification into the D-band. Thanks to these encouraging results, GaN-on-silicon HEMT technology is a worthy contender for sub-terahertz power amplification. We attribute the results to the combination of an epitaxial structure that's suitable for high-frequency HEMTs, and an *in-situ* SiN layer that serves as thin passivation and a gate dielectric.

Our next step is to boost the performance of our GaN-on-silicon HEMTs for high frequency power amplification. These efforts, including refinements to epitaxy, will focus on reducing the RF loss of the GaN-on-silicon substrate and increasing mobility through a reduction in intermixing in the AlN/GaN heterostructure. We also plan to explore common features in high-frequency HEMTs, such as regrown contacts and deep transistor scaling (gate length and source-to-drain spacing). In addition, we shall optimise the device layout.

To the best of our knowledge, we have provided the first demonstration of the feasibility of GaN-on-silicon HEMT power amplification at frequencies beyond 100 GHz. This work establishes GaN-on-silicon HEMTs as strong candidates for low-cost sub-terahertz 6G cellular infrastructure, test instruments in data centres, and more. We hope this work could make a modest contribution to bringing 6G connectivity to reality.

*This work was supported in part by the Agency for Science, Technology and Research (A*STAR) under Research, Innovation and Enterprise 2025 (RIE2025) Manufacturing, Trade and Connectivity (MTC) under Award M21K6b0134 and in part by the National Research Foundation (NRF)/A*STAR under RIE2025 MTC under Grant M23WSNG001.*

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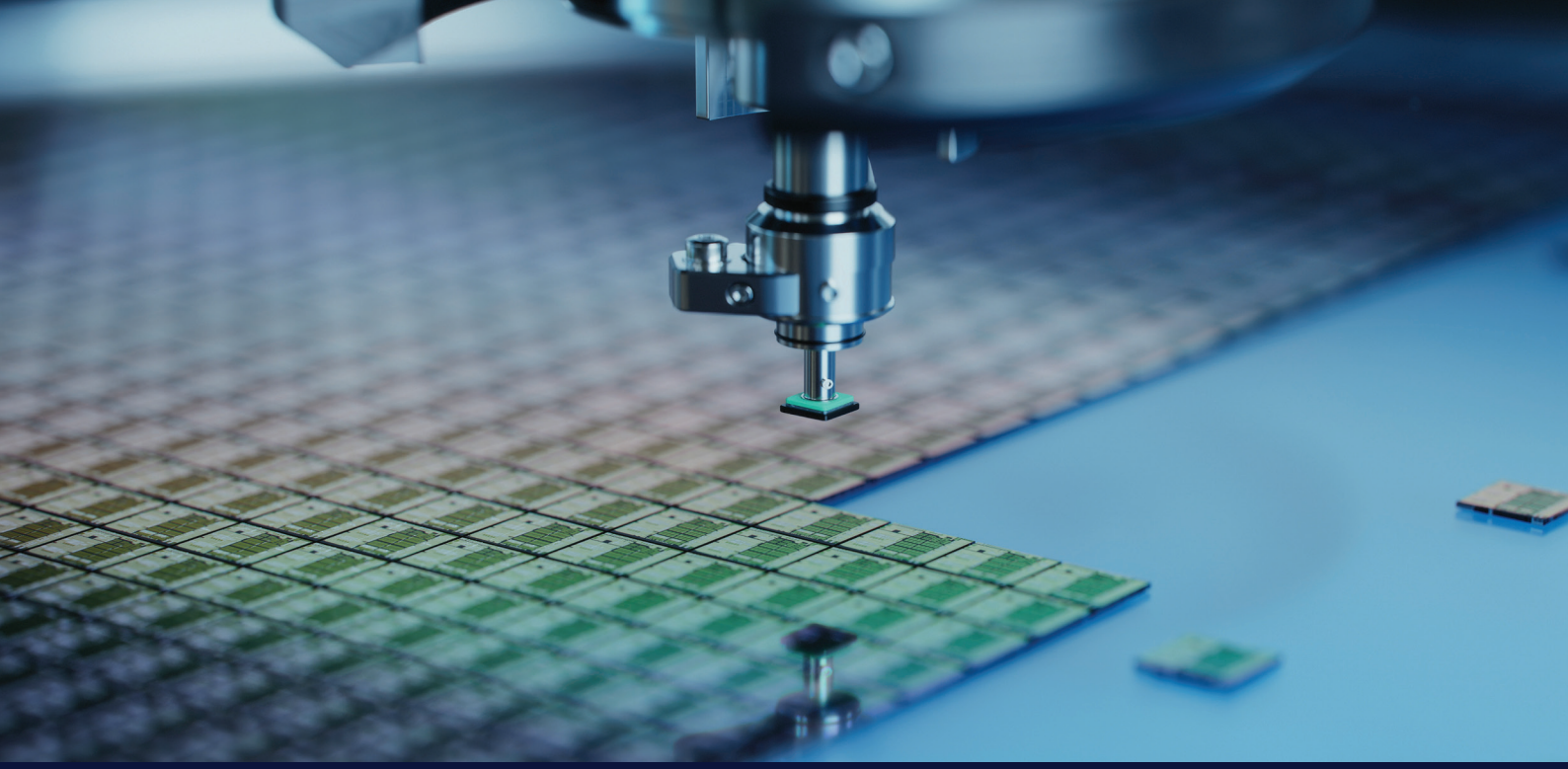

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Unlocking the potential of AlN-buffer HEMTs

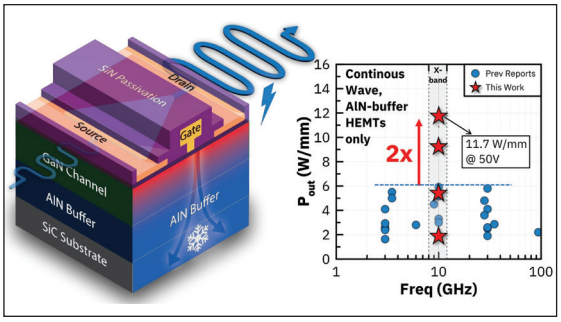
Reducing current collapse and boosting blocking voltage enables a doubling of the continuous-wave output power of AlN-buffer HEMTs

ENGINEERS from Soctera and Trinix Technology are claiming to have delivered a substantial increase in the continuous-wave (CW) output power of AlN-buffer HEMTs.

According to team spokesman, Soctera CTO Reet Chaudhuri, prior to this success, CW output powers of AlN-buffer HEMTs have been below 6 W mm^{-1}, leading to scepticism surrounding this promising technology. While there is much reason for optimism, due to the excellent thermal conductivity of AlN, underwhelming output powers have led to concerns surrounding the two-dimensional hole gas and traps at the interface between GaN and AlN.

"We show that 6 W mm^{-1} is not an intrinsic limit, demonstrating record high output powers of more than 11 W mm^{-1} for AlN-buffer HEMTs across the frequency spectrum," says Chaudhuri.

Previous generations of AlN-buffer HEMTs have been held back by current collapse and/or breakdown. Amongst efforts to improve performance, work has been directed at reducing dispersion, with approaches including the introduction of a δ-doped back barrier. However, successes have tended to come with a trade-off in breakdown voltage.



➤ Soctera's AlN-buffer HEMTs deliver a ground-breaking CS output power density, attributed to an advanced fabrication flow.

Chaudhuri and co-workers argue that they are breaking new ground by reducing current collapse while simultaneously increasing breakdown voltage, likely through a reduction in surface traps. "These combined factors enable us to access CW output powers higher than previously reported in AlN-buffer HEMTs."

Fabrication of this class of transistor began by loading 100 mm semi-insulating SiC substrates into an MOCVD chamber and depositing metal-polar heterostructures. The epi-stack consists of an AlN buffer layer, and undoped GaN channel, and an AlGaN barrier.

To determine the thermal resistance from the two-dimensional electron gas (2DEG) channel to the SiC substrate, the team turned to frequency-domain and steady-state transient reflectometry. This revealed a thermal resistance of 5.5 m^2 K GW^{-1}, around one third of that for a standard HEMT featuring a 1.5 μm-thick GaN buffer on a SiC substrate.

According to room-temperature Hall effect measurements on the AlN-buffer heterostructure, the 2DEG has a density of around 1 x 10^{13} cm^{-2} and a mobility of around 1700 cm^2 V^{-1} s^{-1}.

Using these epiwafers, Chaudhuri and co-workers formed two-fingered HEMTs featuring SiN passivation, a source-to-drain distance of 2 μm, and a gate width of 2 x 100 μm.

Measurements on these devices determined a breakdown voltage of 98 V, and a peak CW output power of 11.7 W mm^{-1} at a drain-source voltage of 50 V. Maximum output power exhibits an almost linear increase with operating bias.

Benchmarking the maximum CW output power against other AlN-buffer HEMTs has shown that the team's transistors produce the highest output power across the entire frequency spectrum, and deliver a power almost double that of the previous record.

Chaudhuri says that Soctera is actively commercialising its technology, which will bring electrically and thermally co-optimised GaN power amplifiers (PAs) to market. "These PAs are specifically designed for next-generation communication networks, offering significant size, weight, power, and cost benefits, and reduced reliance on foreign supply."

Developed in partnership with a US-based supply chain, Soctera's initial 'samplable' PAs are scheduled for launch by the end of this year.

The company will continue to develop its device technology. Efforts will now be directed at utilising source-connected field plates to enhance breakdown voltage and power handling capabilities, while simultaneously optimising device design for maximum thermal performance.

"On the manufacturing side, we are concentrating on scaling-up production, maximising yield, and ensuring high uniformity across the wafer, as we move closer to high-volume production," reveals Chaudhuri.

REFERENCE
➤ R. Chaudhuri *et al*. IEEE Electron. Dev. Lett. **47** 680 (2026)

GaN-on-silicon HEMTs for tomorrow's handsets?

GaN HEMTs with high power-added efficiencies, high power densities and low-noise amplification could serve in next-generation smartphones

A COLLABORATION between A*STAR, Nanyang Technological University and Soitec is claiming to have broken new ground in the development of GaN-on-silicon HEMTs for wireless communication. The team's transistors combine two critical attributes for transmit/receive modules, namely high efficiency and low noise, despite a level of scaling that's described as moderate (the gate length is 100 nm).

Due to these strengths, the GaN HEMT is a compelling candidate for replacing the GaAs HBT, the dominant semiconductor technology in RF front-end modules in cell phones for more than a decade. It is forecast that wireless communication will move to higher date rates, which require higher bandwidths at higher frequency ranges, a non-negiotiable that plays into the hands of the wider bandgap transistor technology.

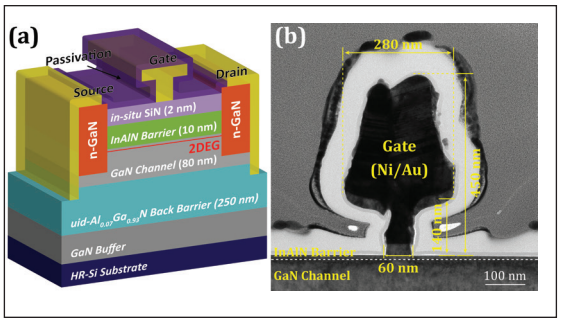
According to team spokesman Qingyn Xie from A*STAR's National Semiconductor Translation and Innovation Centre for Gallium Nitride, another asset of the GaN-on-silicon HEMT over the HBT is its higher power density, a valued characteristic in the power amplifier (PA). "With backward compatibility concerns, the same chip area must support a wide range of bands, therefore power density becomes a critical parameter," argues Xie.

According to the A*STAR researcher, another advantage of the GaN-on-silicon HEMT is its higher breakdown voltage, which promises to enable a more robust technology that could simplify on-chip protection circuits. And as GaN-on-silicon HEMTs could be manufactured using 300 mm CMOS-compatible GaN-on-silicon processes, these transistors could fulfil demand for mass-market, low-cost components.

Production of the transistors involved processing MOCVD-grown 150 mm epiwafers featuring high-resistivity silicon substrates. The heterostructure has a carbon-doped GaN buffer optimised for RF performance, a 250 nm-thick unintentionally-doped $Al_{0.05}Ga_{0.95}N$ back barrier, an 80 nm-thick channel, a 10 nm-thick InAlN barrier and a 2 nm-thick SiN cap.

The InAlN barrier provides strong polarisation and a low gate-to-channel distance, enabling improved two-dimensional electron gas control; and the ultra-thin GaN channel and AlGaN back-barrier enhance electron confinement, effectively supressing short-channel effects and lowering channel noise.

Fabrication of the HEMTs involved etching, lithography, MBE re-growth of *n*-type GaN, the formation of T-shaped gates, atomic layer deposition of Al_2O_3, and plasma-enhanced CVD of SiN. Using these steps, the team produced HEMTs with a source-to-drain spacing of 2 μm, a gate width of 2 x 25 μm, and gate lengths of 60 nm, 100 nm and 150 nm.



➤ The GaN-on-silicon HEMT technology targeting millimetre-wave applications features a T-shaped gate and bilayer passivation.

Characterisation of these devices determined a maximum drain current of 1.58 A mm^{-1}, an on-resistance of 1.48 Ω mm, and a threshold voltage of -2.9 V. Operating under a drain-source voltage of 10 V, the cut-off frequency and maximum oscillation frequency are 100 GHz and 254 GHz, respectively, for the HEMT with a 100 nm gate length. Under continuous-wave operation at a gate-source bias of -2.8 V, the HEMT with a 100 nm gate length produces a saturated output power density of 1.19 W mm^{-1}, a power-added efficiency of 62.3 percent, and a linear gain of 11.1 dB.

The team have also evaluated low-noise performance, described as 'outstanding'. Across 10 GHz to 40 GHz, the minimum noise figure is less than 1.4 dB, suggesting that this HEMT could be deployed as a low-noise amplifier (LNA) in next-generation smartphones.

"In the future, if the RF switch performance using this GaN-on-silicon process would be promising, this GaN-on-silicon process could theoretically be used for the LNA, PA, and switch, therefore forming a monolithically integrated transmit/receive module," says Xie. "Such on-chip solutions are desired for millimetre-wave communication, due to the lower parasitics."

One of the plans for the team is to optimise these devices for higher performance at low voltage, which may be accomplished by trimming the on-resistance, via shrinking the source-drain distance while maintaining the gate length and other process features. "Secondly, we will explore E-mode transistors; and thirdly, we hope to characterise the linearity of these transistors," added Xie.

REFERENCE
➤ Y. Zhuang *et al*. IEEE Electron. Dev. Lett. **47** 482 (2026)

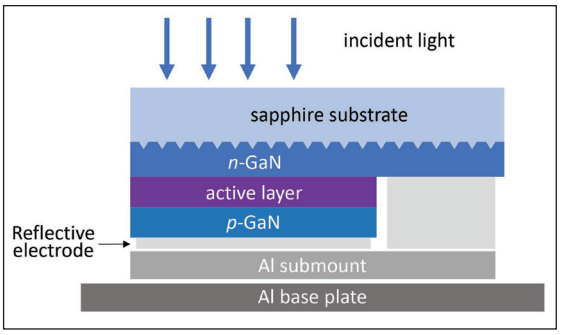
GaN: Boosting optical power converter efficiency

Optical power converters based on GaN are robust, capable of operation at high-temperatures, and now have efficiencies over 60 percent

WHEN electrical power is required, but it's impractical to supply this via the mains or batteries, optical power converters provide an attractive alternative. It's a technology that's focused on GaAs and InGaP, but GaN has the upper hand on a number of fronts – and now boasts a power conversion efficiency of more than 60 percent, thanks to efforts at the Japanese optoelectronics trailblazer Nichia.

According to this team, one significant advantage of switching from traditional III-Vs to GaN and its related alloys is a superior temperature stability, both for the optical power-convertor and the source, which could be a GaN-based LED or laser diode. What's more, GaN is well-suited to operation in harsh environments, such as aerospace, due to its high thermal conductivity and high radiation resistance.

Efforts to develop optical power converters can draw on the development of solar cells fabricated with the same material system. For GaN-based solar cells, InGaN/GaN multi-quantum wells are often used as the absorber, which must harvest a broad emission spectrum. With optical power converters, a key difference is the need to optimise absorption for a single wavelength.



➤ The design of Nichia's optical power converter is similar to that of a high-power LED.

For both optical power converters and solar cells, high light absorption must go hand-in-hand with a high fill factor – and for GaN-based devices, that's challenging, because thick multi-quantum wells tend to degrade material quality and carrier transport. Another potential limitation is a contact resistance that is not low enough to maintain performance under high-intensity illumination. Due to these issues, prior to Nichia's breakthrough, the highest reported power conversion efficiency for GaN optical power converters was about 43 percent, realised under a power intensity of just 5 mW cm^{-2}.

To deliver a significant improvement in both these figures – and those for the fill factor and absorption efficiency – Nichia's engineers have leveraged technology developed for high-power LED products. This included drawing on the company's high-quality GaN epitaxial growth on sapphire substrates.

The optical power converter produced by Nichia is said to have a device structure similar to that of a high-power LED. At the heart of this converter, formed using MOCVD, is an active layer consisting of 60 pairs of 2 nm-thick $In_{0.12}Ga_{0.88}N$ and 2.3 nm-thick GaN. This design, with an absorption edge around 420 nm, is chosen to balance absorption efficiency with high-quality epitaxial growth.

The optical power-converter chip, 1.4 mm by 1.4 mm in size, is flip-chip bonded to an AlN sub-mount with the reflective electrode on the rear facet, so that light is incident from the sapphire substrate side. No coating is applied to the light-incident facet. With this design, incident light may be internally reflected several times, aiding overall absorption.

Under a -2 V bias, the reverse-leakage current is as low as 20 nA cm^{-2}, indicating good crystal quality. Based on the temperature dependence of the reverse-leakage current, Nichia's engineers have concluded that trap-assisted, thermally activated carrier transmission is dominant.

Electro-optical measurements have determined that the external quantum efficiency peaks at around 80 percent at 400 nm. At shorter wavelengths, efficiency falls, due to increased absorption loss in *n*-type GaN; and at longer wavelengths reduced absorption in the active layer drags down efficiency.

Using an in-house 401 nm laser and an illumination intensity of 96 W cm^{-2}, the fill factor is 86.2 percent and the power conversion efficiency 60.1 percent. Over the range of illumination intensity from 20 W cm^{-2} to 96 W cm^{-2}, power conversion efficiency remains above 60 percent, peaking at 60.2 percent at 45 W cm^{-2}.

Nichia's engineers have also evaluated the temperature dependence of the power-conversion efficiency at an illumination intensity of 96 W cm^{-2}. While this efficiency declines with temperature, it's as high as 55.6 percent at 125°C.

Based on reports of violet laser diode efficiencies of more than 45 percent, researchers claim that end-to-end transmission efficiencies of nearly 30 percent are feasible, using technologies well-suited to high-volume production.

REFERENCE

➤ H. Ogawa *et al.* Appl. Phys. Express **19** 021009 (2026)

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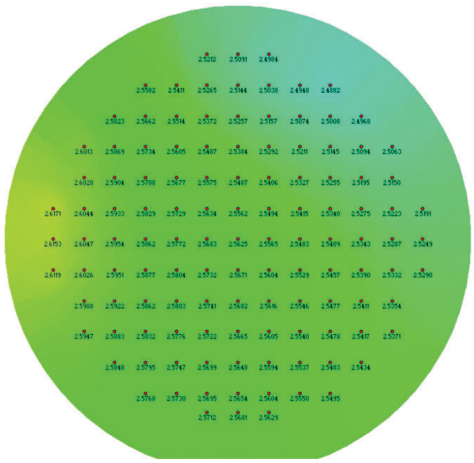

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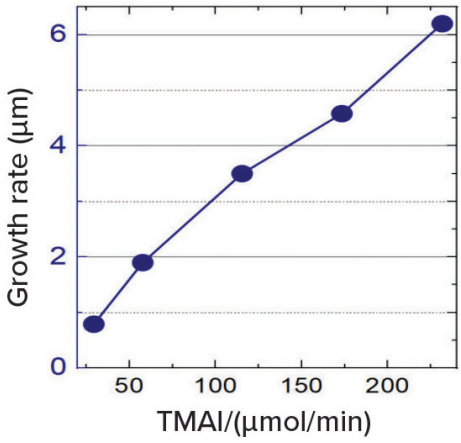

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