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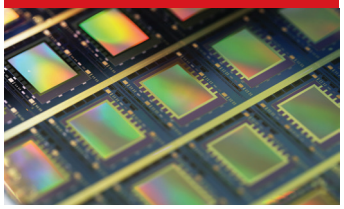
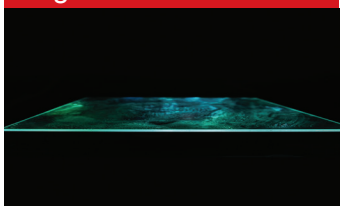
Miniaturising displays with microLEDs



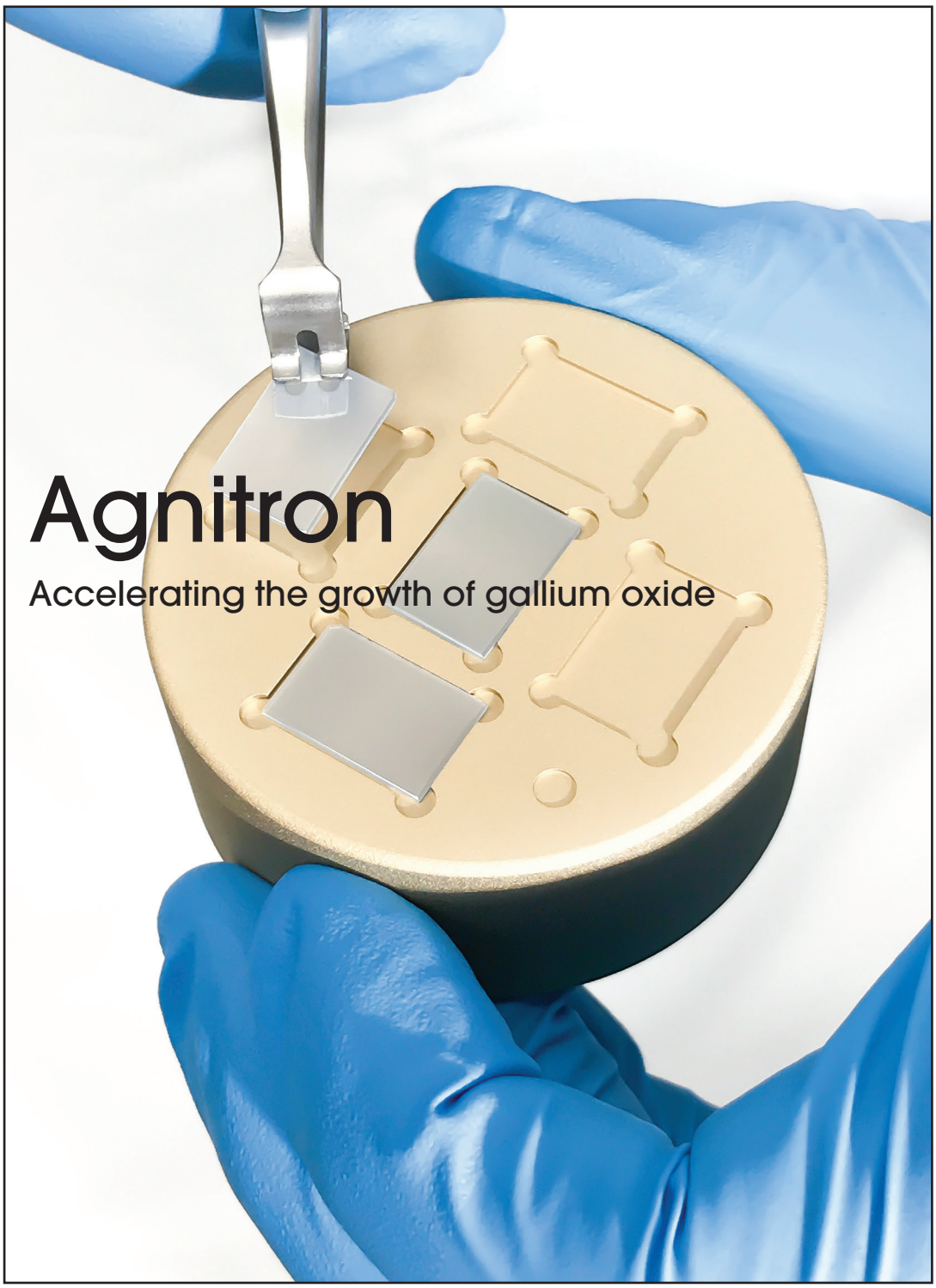
Growing various III-Vs on glass substrates



Nitride nanowires start lighting up silicon chips

Maintaining Moore's law with nanowire MOSFETs

European equipment makers see shares soar



Agnitron

Accelerating the growth of gallium oxide

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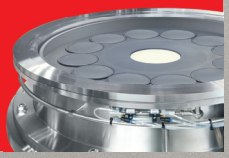

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Viewpoint

By Dr Richard Stevenson, Editor

Lighting up silicon chips with the nitrides?

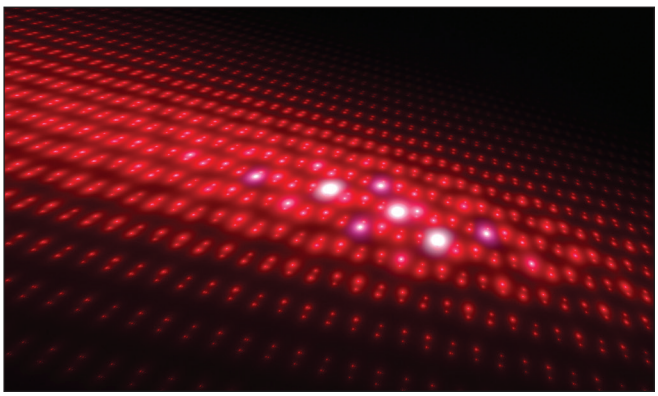
I'VE SAT THROUGH enough talks on the use of nitrides in optoelectronics to know that this class of material has the potential to yield emitters spanning the UV right through to the infrared.

But that's not the way I tend to think of this material system. I see it as one that can be used to make promising emitters in the UV, great cousins in the blue, and variants that produce an ever-declining efficiency as emission is pushed on to the green, yellow and then the red.

Now, though, my view is changing, thanks to the work of Pallab Bhattacharya and his co-workers at the University of Michigan. They have devoted a great deal of time to developing a light source that can be added heterogenously to a silicon chip, and after struggling with the drawbacks of GaAs-based and InP-based materials – lattice mismatch, anti-phase domains and differences in thermal expansion coefficients – they are now enjoying success with the nitrides.

Reaching the infrared with planar nitride devices would be nigh-on impossible, so Bhattacharya and his colleagues are adopting an entirely different approach: nitride nanowires. And they have their own way of going about this, inserting InN disks into GaN nanowires to produce lasers that emit at 1.3 μm, the sweet spot for silicon photonics (see p.46 for details). Encouragingly, these devices can be modulated at up to 3 GHz.

The team has also produced photodiodes, another key building block for optical links. These structures, typically 1 mm in



length and 50 μm wide, can produce a healthy current when illuminated by infrared light.

So far, the highlight of the work at Michigan is the creation of a photonic integrated circuit, comprising laser, photodiode and detector. Efforts are in their infancy, but the photodiode is picking up the light from the laser.

Can this technology kick on and address the looming bottleneck for silicon ICs? After all, there is a need for light-based communication to increase the rate of information transfer between and within CMOS chips.

Only time will tell if nitride nanowires will serve silicon ICs. But whatever the solution is, it is sure to come from our community, which without a doubt continues to excel in innovation.

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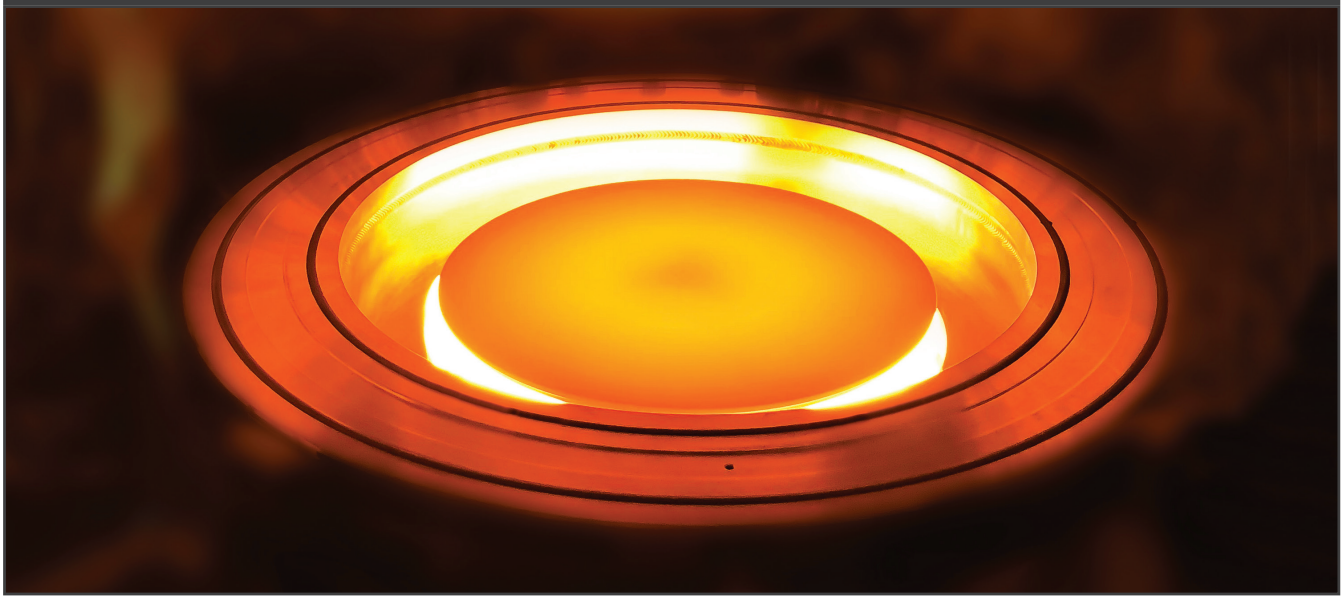

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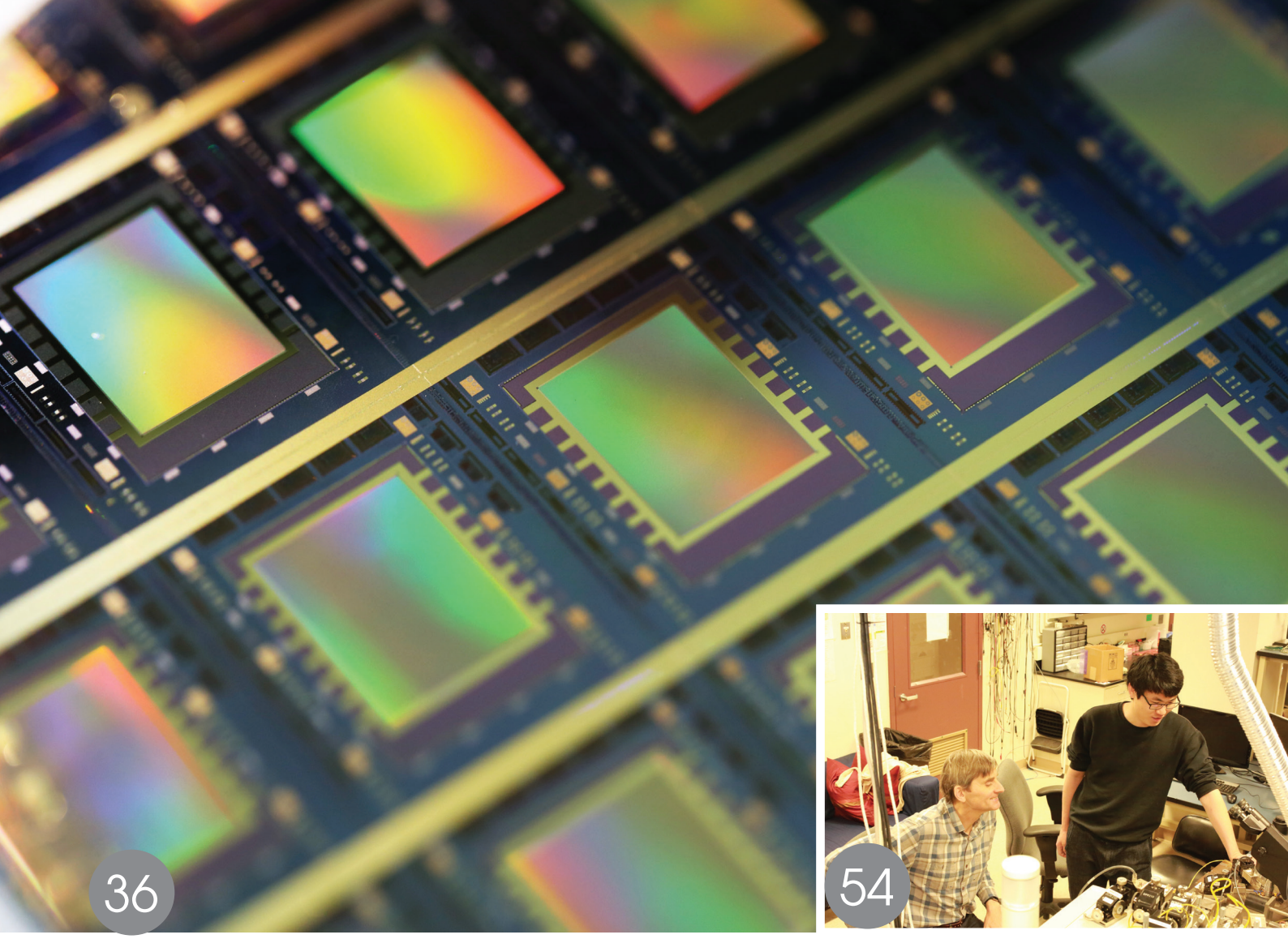

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UV LED market share trebles

YOLE DÉVELOPPEMENT'S latest report on UV LED technology forecasts that UV LEDs will reach 25 percent of market share from other UV illumination technology in 2018, rising from 8 percent of the market in 2008.

In 2008, UV LED was still considered an emerging technology and industry, trying to make its way into promising applications such as UV curing and counterfeit detection. Then, the LED industry only had eyes for the booming display applications, and was preparing for the rise of general lighting, considered to be the killer application for visible LED. Much has changed since then.

"From around ten players in 2008, there are now over 65 players in 2018", asserts Pierrick Boulay, technology and market analyst at Yole. "Since 2010, several visible LED players have turned to UV LEDs, seeking new growth drivers and higher profit margins."

The UVA LED market segment was the first to witness this industrial evolution, experiencing strong price reductions that have further accelerated the technology's penetration. But after several years of double-digit growth, UV curing application revenues, which represent more than 80 percent of the UV LED market, have started to decline due to commoditisation and a highly competitive environment. In the short-to-mid term, only players that can innovate will be able to maintain a profitable business in this area, according to Yole.

In parallel, UVB/UVC LED market has been less negatively impacted by the flood of new entrants, because the barriers to entry are much higher. Additionally, UVB/UVC LEDs still suffer from low performance, so entry of new players has helped boost device development. But despite devices being good enough today at a performance and cost level, the UVB/UVC market is slow moving. UV LED systems require extended development to fully benefit from the technology, which is taking more time than expected.

In the short term, the UV LED industry will experience a slow-down phase as the UV curing market starts to plateau and the UV disinfection market's boom will be delayed, says Yole. "In this context, we expect the UV LED market to reach $320 million in 2020, from $160 million in 2017", confirms Pars Mukish, business unit manager at Yole. "Then, the market will be driven by UVC applications, showing a strong increase to $1 billion in 2023."

This period is also showing a strong evolution in term of business model and strategy and these trends have been analysed by Yole's solid-state lighting team. A large part of the visible LED industry has turned to UV LEDs. However, strategies put in place differ between players, depending on wavelengths

targeted. Several players still focus on device manufacturing, whereas others are vertically integrating towards modules and systems. For example, in UVA LEDs, Ushio produces UVA LED chips, packages and also now curing modules, which are supplied to printer manufacturers or end-users. In UVC, Nikkiso was initially a UVC LED manufacturer, but has moved to module and system level by acquiring AquiSense Technologies in 2016.

In addition to UV LED players, some new entrants are trying to make their way into the industry, mostly at the module or system level, which represents the sweet spot in terms of business opportunities. The only missing companies are the UVC system suppliers, which seem still to be in "wait and see" mode.

Osram acquires VCSEL firm Vixar

Osram has acquired US-based fabless VCSEL firm Vixar to widen its portfolio of security products. Vixar was founded by pioneers in the VCSEL industry, having first brought VCSEL to the data communication market in the late 1990s, and more recently by founding Vixar in 2005 to pursue sensing applications. Approximately 20 employees of the company, which is based in Plymouth, Minnesota, will transfer to Osram as a result of the acquisition.

Vixar is profitable both on an operational and net results level. The parties to the deal have agreed not to disclose financial details. Closing of the transaction is expected in summer. "The acquisition of Vixar is adding to our expertise, particularly in the fast-growing market for security technologies," said Olaf Berlien, CEO of Osram Licht AG.

While currently known primarily for identification applications in mobile devices, VCSEL also can be used to recognise gestures and measure distances in medical, industrial, and automotive applications. Osram has already succeeded in bringing to market infrared light sources for fingerprint sensors, iris scanners, and 2D facial recognition. The acquired capabilities from Vixar will pave the way for further security technologies, including ultra-compact 3D facial recognition. In addition to unlocking smartphones and other consumer electronics devices, such technologies also can be used for high-security access controls in industry. The way in which VCSEL technology captures 3D environmental data has applications in everything from gesture recognition, augmented reality, robotics, and proximity sensors to autonomous driving.

Seoul AC LED modules pass 4 kV surge testing

LED firm Seoul Semiconductor has demonstrated a 277 V AC lighting module using its NanoDriver Series LED driver that complies with the industry standard 4 kV surge testing.

Prior to this, AC LED modules have been mainly used in residential lighting applications due to the technology's limited capability to meet the surge requirements for industrial and commercial applications. This demonstration module proves that it is possible to achieve a 277 V AC module with high surge capability using Seoul Semiconductor's NanoDriver Series LED driver.

Prior to Seoul Semiconductor's recent product introduction, many LED fixture designers perceived AC LED technology as a low-performance, low-cost solution, assuming that AC LED technology had compromised performance,restricting its applicability. This demonstration module proves that it is possible to get a high efficacy, low flicker solution using AC LED technology, according to the company.

"This demonstration module proves that AC LED and driver technology can be successfully integrated for industrial and commercial lighting, expanding the market for these smaller, simpler, lower cost fixture designs," explained Keith Hopwood, executive vice president at Seoul Semiconductor.

"The NanoDriver Series devices are the industry's smallest 24 W LED drivers available, enabling lighting engineers to develop luminaire designs with dramatically reduced size, weight and volume," explained Hopwood.

"Expanding the NanoDriver's applications to include commercial and residential lighting brings to customers in those markets the benefits of Seoul Semiconductor's AC LED technology – efficacy, low flicker, simpler topologies, and reduced size."

The NanoDriver Series LED drivers are ideal for a variety of commercial and industrial applications such as bollards, wall sconces, downlights, and flush-mount fixtures. Their small size enables ultra-thin and novel fixture designs, making conventional lamp replacement possible without the need for a large volume recess for the driver, or a reduction in the light output. The NanoDriver Series LED drivers make it possible to convert many conventional fixture designs to LEDs because the driver's small size makes it possible to integrate it into the fixture housing.

The NanoDriver Series devices are suitable for luminaire designs up to 3,000 lumens, making possible the integration of the control circuitry with the external converter. This facilitates the capability to add commercial lighting 0-10 V controls, motion and daylight sensors, as well as integrating wireless control. The NanoDriver Series devices are small and lightweight enough to make airfreight economical, which reduces lead time and streamlines the supply chain.

II-VI opens new epitaxial wafer facility

II-VI, a provider of compound semiconductor epitaxial wafers, has opened its new high tech compound semiconductor material centre of excellence in Champaign, Illinois.This represents a significant milestone in II-VI's ongoing investment in its manufacturing footprint to ramp up production capacity of high performance compound semiconductor epitaxial wafers.

These products serve growing markets and are at the core of 3D sensing, optical networking, wireless communications and power electronics. Since the ground-breaking for this expansion, in November 2016, II-VI continues to actively recruit managers, engineers and technicians to join its experienced team.

Illinois Governor Bruce Rauner was present at the inauguration's ribbon cutting ceremony.

"On behalf of II-VI, I would like to express my thanks to the Illinois Department of Commerce & Economic Opportunity for its ongoing support and unwavering commitment to our success," said Quesnell Hartmann, general manager and co-founder of II-VI EpiWorks. "The completion of this phase in our expansion provides us with the critical infrastructure to scale our production, advance our technology, and enable us to serve the rapidly growing demand from our global customer base."

"II-VI and the State of Illinois have formed a strong partnership, sharing a vision that businesses with leading edge technology and advanced manufacturing capabilities are the most competitive over the long-term," said Chuck Mattera, president and CEO, II-VI Incorporated. "With support from Illinois, we expect to continue to invest in this Champaign facility, by adding state-of-the-art manufacturing capacity, improving process capabilities, broadening the product portfolio and recruiting and developing a lot of talent to fill the anticipated growth in jobs and opportunities for career growth."

"It's a thrill to participate in the opening of a manufacturing facility that will develop key technology enabling some of the most exciting new consumer electronics in the world," Illinois Governor Bruce Rauner said. "It showcases how local industry, strong university systems and state government can partner to realize a bold vision for a globally competitive semiconductor manufacturing center of excellence that's built right here, in the heart of our wonderful state of Illinois."

GaN driving RF power semiconductor growth

SPENDING on RF power semiconductors with frequencies below 4 GHz and powers of more than 3 W was nearly $1.5 billion in 2017. The wireless infrastructure segment was flat but other markets – notably military/defence – are moving forward, according to ABI Research, a US market-foresight advisory firm.

Additionally, GaN – long seen as the likely promising new 'material of choice' for RF power semiconductors – is continuing its march to capture share.

"GaN has the promise of gaining market share in 2018 and is forecast to be a significant force over the next few years, It bridges the gap between two older technologies, exhibiting the high-frequency performance of GaAs combined with the power handling capabilities of Silicon LDMOS. It is now a mainstream technology which has now achieved measurable market share and in future will capture a significant part of the market."noted ABI Research director Lance Wilson. Wireless infrastructure, while representing about two-thirds of total sales, has been lacklustre recently, says ABI. Growth for other segments outside of wireless infrastructure is showing mid-single digit CAGR over the forecast period of 2018 to 2023.

The vertical market showing the strongest improvement in the RF power semiconductor adoption business, outside of defence, is commercial avionics and air traffic control, which Wilson describes as being now 'a significant market'.

While the producers of these devices are in the major industrialised countries, this sub-segment market is now so global that end equipment buyers can be from anywhere. These findings are from ABI Research's *RF Power Semiconductors Market Data* report and a companion narrative and discussion *RF Power Semiconductors: Silicon, Gallium Nitride, and Gallium Arsenide High-Power RF Devices* report.

Soraa expands white light LED disinfection programme

SORAA, the US maker of violet-LED based full spectrum lighting, has announced the availability of an expanded collaboration programme for its patented white light disinfection technology. This disinfection technology is based on Soraa's violet LEDs, which can be used to provide a disinfecting action while also delivering natural white light.

In announcing the collaboration programme, Jeff Parker, CEO of Soraa, referenced Soraa's extensive portfolio of patents in the field of bactericidal LEDs used for white light generation and disinfection, a portfolio that includes patents dating back to at least 2009. This programme is further buttressed by Soraa's recent acquisition of certain

foundational GE patents on GaN LEDs, dating back to 2001.

"We are extremely proud of our early inventions in this space, and are actively engaged in partnerships with key players in the field that will leverage our expertise with violet LEDs," says Parker. "These unique lighting solutions give us the ability to help usher in a new era of 'white light' disinfection to create healthier environments."

Luminus expands high-power LED horticulture range

LUMINUS DEVICES, a manufacturer of high-performance LEDs and solid-state light sources, has expanded its horticulture LED portfolio with new SST-20 series white LEDs to complement the company's broad range of horticultural LEDs with discrete wavelengths from UVA (365 nm) to far red (730 nm).

Incorporating white light in horticulture fixtures provide illumination in the greenhouse and make it easier to observe crops for signs of disease and, in many cases, white LEDs can replace blue LEDs as they provide similar PPF, and thereby potentially reduce production costs.

With a flexible offering spanning 2700K to 7000K, customers can now select the light most appropriate to their needs.

"The need for improved crop yields and more sustainable food supplies is more important than ever and our horticulture LED advances enable innovative luminaires that directly address the market's needs," said Yves Bertic, Luminus' senior director of global product marketing.

As the horticulture and farming research community discover productivity and crop quality gains through wavelength and spectrum engineering, Luminus continues to expand its offering by adding new wavelengths to its current portfolio so that growers and farmers can maximise production yields, become more sustainable and reduce costs.

"With this addition to our SST series, we now offer a comprehensive horticulture product portfolio that delivers the highest performance and efficacy with competitive lead times of 12 weeks or less," said Bertic.

Cree extends metal chip-on-board LED range

CREE has expanded its XLamp High Current LED Array family with new CMT LEDs that extend Cree's latest metal-based chip-on-board (COB) LED technology to the most prevalent COB form factors.

Cree XLamp High Current LED Arrays offer 45 percent more lumen density and up to 17 percent higher efficacy, according to the company, and feature an innovative metal substrate technology that delivers higher reliability than competing metal COBs.

With more than 6,000 hours of LM-80 data available, Cree says that the expanded family of LEDs enables lighting manufacturers to upgrade their designs for DesignLights Consortium and ENERGY STAR eligible applications, such as track, downlight and outdoor lighting.

"With the new High Current CMT LEDs, Cree has given us a full portfolio of solutions for our upcoming luminaire designs, in terms of both performance and ease of integration," said Shawn Keeney, technology manager, Ledra Brands, a manufacturer of innovative, specification grade LED lighting fixtures and systems.

"By choosing Cree, we know that we are leveraging the highest performance and best long-term reliability for COB LEDs to continue our leadership in solid state lighting design."

The CMT LEDs and the recently announced High Current CMA LEDs make Cree's new metal-based COB technology available in form factors that are compatible with most commercially available holders and optics in the market.

The newly expanded High Current LED Array family (CMA and CMT) join Cree's Standard Density and High-Density families (CXA and CXA2), which creates a broad portfolio of COB LEDs. COB LEDs mount directly to a heat sink without a separate circuit board, simplifying the luminaire manufacturing process and reducing system cost.

Dave Emerson, executive vice president and general manager, Cree LEDs said: "In light of recent reports of some companies falsifying lifetime data, our customers can remain confident that Cree LEDs, including our latest High-Current COB family, undergo rigorous testing to allow them to consistently deliver reliable long-term performance."

The CMT LED family includes 10 LEDs across three (9.8 mm, 14.5 mm and 22 mm) light emitting surface sizes to address a wide variety of applications.

Featuring Cree's EasyWhite bins, the XLamp CMT LED arrays are available in 2700K-6500K CCTs with standard colour options of 70, 80 and 90 CRI and premium colour options that include high fidelity (98 CRI) and specialty colour points.

Fraunhofer 'LED backhaul' launched In Japan

FRAUNHOFER HHI has leveraged its ongoing development of optical wireless communication (OWC) technologies, also called Li-Fi, in an initial test deployment by industry partner Sangikyo Corporation. The Japan-based telecommunications system company has launched its first Li-Fi product called LED Backhaul.

Core technology was initially introduced as a 4K/8K video relay; it can now achieve data rates between 100 and 750 Mbit/s.

Fraunhofer HHI believes this development could play an important part in future 5G systems, arguing that 5G network deployments will require flexible frequency spectrum solutions, and that there are considerations about implementing optical links for data backhauling. Further, that systems such as LED Backhaul may offer significant contributions in areas where RF signals cannot typically penetrate or where wireline links are not practical.

Since 2014, HHI has pioneered short-range optical wireless backhaul links through two European research projects (SODALES and 5G Crosshaul).

Apart from backhauling, the newly-developed system can be used as a flexible network, or as a form of LAN extension if no cable is available. The companies said they believe LED Backhaul may offer solutions for factories or subways or any area this is not easily penetrated by radio waves.

Yasukazu Sengoku, COO of Sangikyo, commented, "We have worked with HHI to advance the joint development of high-speed wireless communication with LED light and have attained a realistic application. In future, LED backhaul will be standardized by IEEE 802.15.13 and by international standardization activities of HHI."

Ronald Freund, Head of Photonic Networks & Systems at HHI, said, "We are developing the communication technologies of the future and are pleased that the new wireless system with LED light, which was brought to the market in cooperation with Sangikyo, will be used on the Japanese market. We will continue to work with Sangikyo and develop a wide range of high-speed wireless systems with LED light."

Optical wireless transmission is a future-oriented technology for fixed and mobile wireless optical communication over comparatively short distances.

Possible applications are wireless backhaul and fronthaul for 5G, wireless communication for industry 4.0 as well as in indoor areas alongside WiFi and LTE.

Osram increases LED efficiency by 40 percent

THE SIGNIFICANT drop in light output (green gap phenomenon) exhibited by green LEDs has often been the cause of efficiency problems and high costs in customer applications. For its InGaN-based green LEDs, Osram Opto Semiconductors has now succeeded in reducing the typical forward voltages by around 600 mV. With a simultaneous increase in optical output power, customers benefit from improvements in efficiency of up to 40 percent compared to predecessor products across the entire UX:3 portfolio, says Osram.

Developers at Osram have managed to reduce the typical forward voltages of green direct emitting InGaN LEDs by 600 mV to 2.6 V at power densities of 45 A cm^{-2}. The benefits are considerable, particularly for applications in which red, blue and green LEDs are used in combination. Because all three colours now have a voltage of less than 3 V the drivers, which were previously designed for higher maximum voltages, can now be dimensioned smaller. This in turn reduces both dissipative power loss and costs. The crucial factors in increasing efficiency were improved charge carrier transport and optimised material quality in the epitaxial layers. At 350 mA, 1 mm^2 UX:3 chips achieve efficiencies of 175 lm/W and higher at wavelengths around 530 nm with the new technology. Light output in excess of 300 lm at a pumping current of 1 A opens up new applications.

"Until recently, these efficiency values seemed unattainable for green direct emitting InGaN LEDs. We are now moving into areas that up to now have been achievable only with phosphor conversion emitters but with significantly reduced spectral quality. Thanks to the success of our development team we have been able to drastically reduce the green gap phenomenon for our customers," said project manager Adam Bauer from Osram Opto Semiconductors.

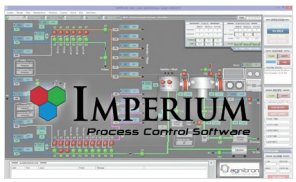
10 Years of MOCVD Solutions and Services

2018 marks the 10th anniversary of Agnitron Technology serving the MOCVD community. Our team is celebrating a number of notable achievements made possible by decades of collective experience in the industry.

- Expansion of Agilis MOCVD Series to include configurations for ß-Ga_2O_3, III-V and TMD materials
- Expanding Laser Diode Production MOCVD Equipment Offering
- More than 50 MOCVD Systems Operating with Imperium-MOCVD Control Software

OEM MOCVD Systems

Refurbished and Upgraded MOCVD



PLC and Control Software Upgrades

MOCVD Support & Maintenance Services, Facility Planning

Agnitron is a supplier of Original and Certified Refurbished/Upgraded MOCVD Equipment for R&D and production applications. Over the course of 10 years a comprehensive line of products has been developed and we've established a strong record supplying high-performance MOCVD equipment. Our advanced Imperium Control Software and matched PLC package solutions offer sophisticated and reliable capabilities for production users as well as flexibility for users requiring upgrades for unsupported, modified or custom equipment. Various configurations within the Agnitron Agilis MOCVD Equipment Series support growth work for standard and highly specialized III-V, oxide, TMD and many other related applications.

agnitron technology

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Gas Sensing Solutions expands team

THE SCOTTISH technology company, Gas Sensing Solutions (GSS), has hired Bill Proudfoot to be its second business development manager. He is the latest addition to the company's team that is growing to meet increased demand for its award-winning products. This growth is so great that the company is in the process of doubling the size of its premises to accommodate the additional staff and more than doubling its production capability.

The company has revolutionised the design of carbon dioxide (CO_2) sensors by using proprietary LED technology that dramatically cuts power consumption and speed of response. This enables CO_2 monitors to be designed that, for the first time, can be battery powered with long operational lives.

This opens up whole new application areas such as battery-powered CO_2 monitors for offices and factories that cuts out the costs of mains cabling. Additional areas include CO_2 level monitors for diving, wearable alarms for people who might enter high CO_2 concentration areas in factories, and monitoring of CO_2 levels in exhaled breath as an indicator of ill health.

"Over the years, we have developed excellent relationships with customers around the world with a global network of distributors providing local support," explained Calum MacGregor, CEO at GSS. "At the end of last year, we added two more prestigious awards to our collection, i.e. the 2017 Elektra Awards for Design Team of the Year and for Excellence in Product Design – Medical. These have raised our global profile even further as the organisers, Electronics Weekly, have a world-wide audience. We have also invested heavily in trade shows around the world and our website to further raise our global presence and so we have hired Bill Proudfoot to respond to the resulting enquiries and further develop our export market."

Bill Proudfoot added, "I have been working in the electronics industry for many years and I think that GSS technology is a real game changer. It enables small, battery powered CO_2 monitors to created that were previously impossible as rival CO_2 sensors are so power hungry that they need a mains supply. It's perfect timing with the growing realisation of the effects of even slightly elevated levels of CO_2 on health. Yawning in a stuffy room is not lack of oxygen but a level of CO_2 high enough to start affecting your ability to think clearly.

Higher levels have even worse effects on health. Authorities around the world are starting to become aware of this and legislate for maximum CO_2 levels, and this in turn is driving the demand for CO_2 sensors. I am pleased to say that Scotland has pioneered this with the requirement that all new houses must have a CO_2 level alarm. The importance of CO_2 monitoring has recently been highlighted by NASA using GSS sensors at the heart of personal CO_2 monitors worn by the crew of the International Space Station where high levels of CO_2 could really compromise health."

Siltectra announces three new patents

SILTECTRA, a wafer company, has added three new patents to its IP portfolio. The first patent relates to the company's Cold Split laser process and extends the approach to non-polymer applications. The second patent secures Cold Split for all substrate materials.

The third patent covers an extension of the company's SiC process capability to split materials with sub-100-µm material loss, regardless of vendor-specific SiC crystal-growing processes.

Siltectra says that cost reductions enabled by its technology could speed deployment of SiC for a broader range of applications, such as electric vehicles and 5G technology.

The company's IP portfolio now consists of 70 patent families with 200 patents. Collectively, the patents cover every innovation associated with the company's laser-based Cold Split wafer-thinning process.

Cold Split demonstrated early differentiation by thinning wafers to 100 µm and below in minutes with extreme precision and virtually no material loss.

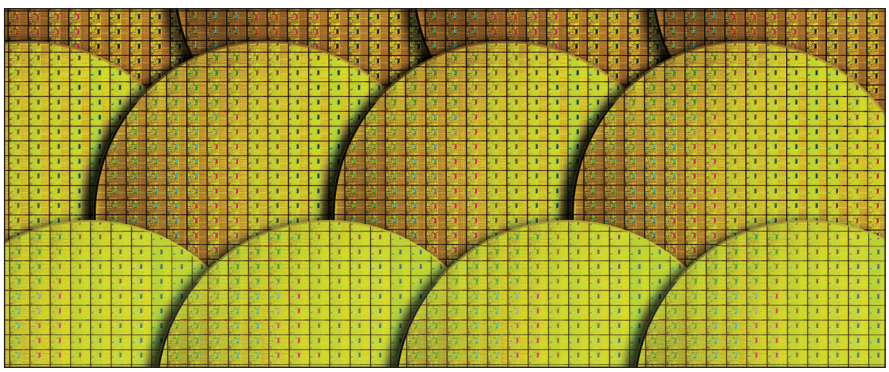
These enabling advantages drew high interest from integrated device manufacturers (IDMs) who had previously relied on grinding to thin their wafers. Grinding is a slower, less precise process that generates material loss and reduces overall yield. In contrast, Cold Split is a much faster laser-based thinning approach with higher yield and strong cost-of-ownership benefits.

In a development announced earlier this year, Siltectra reported a breakthrough new capability for Cold Split that increased the value of the technology for cost-sensitive IDMs. Thanks to a novel adaptation known as 'twinning' the company demonstrated that Cold Split can reclaim substrate material generated (and previously wasted) during backside grinding and create a second fully optimisable bonus wafer in the process.

Siltectra validated the breakthrough by producing a GaN-on SiC-HEMT on a split-off (or 'twinned') wafer at its new state-of-the-art facility in Dresden. The HEMT showed results that were superior to a non-COLD-SPLIT-enabled HEMT when measured for CMP characterization, as well as GaN epi, metal layer and gate layer outcomes.

Siltectra's CEO, Harald Binder, noted: "Like all technology companies, Siltectra's leadership and future growth depend on continually innovating to extend our capabilities and further enrich the value of our solution. Naturally, therefore, it's a strategic priority to protect the innovations along the way so that our competitive differentiation and enabling advantages to remain strong in all regions where customers are located. Our robust IP portfolio reflects this priority."

Jan Richter, Siltectra's CTO, stated: "Our R&D team is relentlessly pushing the limits of our Cold Split technology to fulfil its enormous potential. The additional patents further strengthen our market position, while enabling us to drive Cold Split's material loss far below 50 microns."



BluGlass appoints industry expert Mike Krames

BluGlass, the Australian developer of Remote Plasma Chemical Vapour Deposition (RPCVD) for making LEDs and other devices, has appointed Mike Krames as an advisor to the company. Krames will provide expert guidance on the technical development and commercialisation plans of RPCVD.

Krames has more than 20 years' leadership experience in the compound semiconductor industry and is a recognised world authority on LEDs and their applications for lighting and displays. In 2015, Krames established Arkess LLC, an independent advisory and technology development consultancy based in the US.

Prior to this he was CTO at Soraa, an LED company founded by Nobel Prize winner Shuji Nakamura, and, executive VP at Philips Lumileds. There, he ran the Advanced Laboratories and pioneered programmes in LEDs and related materials, including leading the development of the technology necessary to enable LEDs to serve as automotive headlights for the first time.

Krames will advise the company in a strategic and technical capacity to assist in the commercialisation of BluGlass' low temperature RPCVD technology.

Managing director Giles Bourne said: "The appointment of Mike to advise BluGlass at this pivotal stage of our development represents a fantastic opportunity for the company to gain expert technical and commercial guidance from one of the recognised nitride industry leaders."

Krames has served on numerous roundtables and panels for the US Department of Energy. He is Chair of the SPIE Photonics West Conference on LEDs. He has more than 80 peer-reviewed publications and 100 granted US patents and has served on several boards of directors/advisors.

A golden future for CST Global

CST Global anticipates that 2019 will herald a photonics gold rush

TREMENDOUS OPTIMISM is permeating through the corridors of Compound Semiconductor Technologies (CST) Global, the optoelectronics foundry on the outskirts of Glasgow. Shipments are up, head count is rising fast, and right now the order book is incredibly healthy.

To raise the profile of company's success even higher, showcase its investment in its facilities, and offer details of its plans for the future, the company held an open day on 10 May.

Speaking to those in attendance – a mix of leading engineers in industry and academia, investors, Members of Parliament and the technical press – company co-founder and CEO Neil Martin explained that feelings of anticipation and urgency were running high in today's photonics industry.

A dedicated tool for bar stacking is helping to increase the throughput at CST Global.

"Before us is a vast gold rush opportunity in photonics technology," said Martin, who argued that it is crucial to prove the feasibility of the technology first, because the company that has done that will capture the market.

"Just like back in 1849 with land, some technology will deliver an obvious, quick return: the gold," claimed Martin. But that will not be the case with all technology, as some developments may never produce a commercial return, while others "may produce oil in years to come."

So there is a need to pursue a diversified technology portfolio, which is the approach adopted by CST Global. At this site, epiwafers are processed into a range of optoelectronic products. Shipments are dominated by lasers that are used in the products of companies operating in the telecom, cloud computing, transport, storage and phone industries.

Martin believes that the photonics gold rush will be driven by opportunities in long-distance optical telecoms, cloud computing, touch screens, facial recognition and mobile communications.

To be in a position to exploit these opportunities, CST Global has been investing in its facility, and it has increased its manufacturing floor space by 30 percent over the last year. It has also spent £1.5 million on tools, increasing automation and throughput by removing the need for both the visual inspection of material and the manual stacking of laser bars. These refinements have helped to propel production to 2 million InP lasers per month.

To maintain its technology at the cutting-edge, CST Global is playing its part in many collaborative research programmes.

"We currently operate fourteen research projects, co-funded by the government and worth over one million pounds to CST Global," said Martin.

He believes that government funding is a major asset, accelerating development and ultimately speeding entry into new technology sectors and markets where there is a race to get their first. In addition, government funding can lead to substantial private investment. "More funding means more feasibility and a bigger stake in the future of photonics."

During the last year, CST Global has doubled its workforce to almost 70, to cope with the growing workload. Recruiting high-quality staff with the skills that enable them to make a contribution from day one is not easy, but the company appears to have the upper hand over many of its rivals.

"Our most common recruitment path is via our university links and the PhD projects that we are involved in," explained Martin.

These links are particularly strong for students at Glasgow University. The MOCVD tool owned by the university is sited and managed at CST Global, and after the students have produced their epiwafers, they can process them in the foundry.

Adopting this approach allows PhD students to gain commercial experience, by developing their technology in an industrial environment. "[The students] rub shoulders with top engineers and produce work of commercial value," explained Martin.

Photonics in parliament

The keynote address at the open day came from Carol Monaghan, MP for Glasgow North West. Monaghan, a physics and optoelectronics graduate from the University of Strathclyde, is active in the sector where CST Global operates, having set up the All Party Parliamentary Group on Photonics in October 2016.

Monaghan is championing a "golden strip" of excellence in photonics. "The central belt of Scotland is a hotbed for photonics research, from Glasgow and Strathclyde in the west to Herriot-Watt, Edinburgh and St Andrews in the east."

Despite this strength, Monaghan accepts that there is a skills shortage in the technologies relevant to the photonics industry, and she is concerned that the exit of the UK from the EU could compound this issue.

"Access to the single market and to skilled and experienced staff is vital to our photonics companies," argued Monaghan, who is campaigning for the UK to continue to collaborate with all its European research partners, and draw on the best talent within the industry.

High profile attendees at the CST Global open day included (left to right) Carol Monaghan MP, Sharon Doonin PA to CEO, Monica Lennon MSP, Ged Killen MP, CEO Neil Martin, and Cylina Porch PA to Carol Monaghan.

"Our EU national colleagues and partners still need certainty over their current and future status, and it is an utter disgrace that nearly two years after the vote to leave the European Union, we still do not have clarity on this."

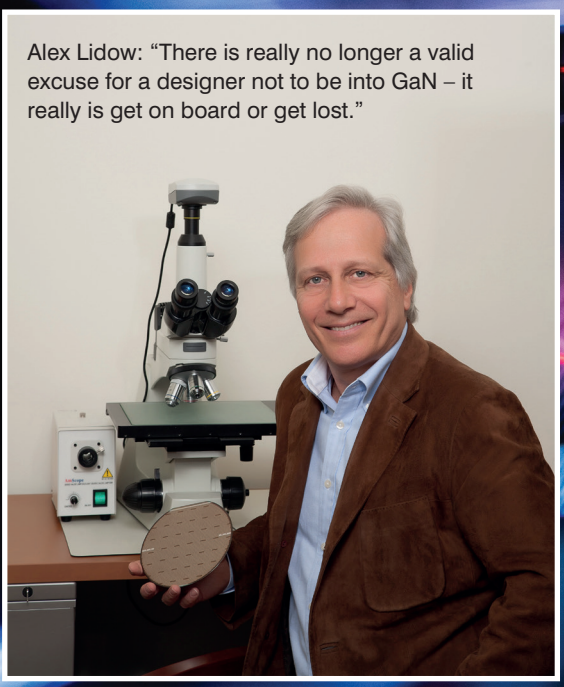
Martin and his colleagues may well agree with these sentiments, but they will have little influence over the Brexit debate. What they do know is that the best way forward to securing their future is to continue to innovate with III-V technologies.

To that end, they are drawing together leading companies and academics in this sector, and trying to create roadmaps for commercialising promising technologies. The first of these gathering will take place this November, where discussions will identify what is needed to take quantum optics out of the lab and into the marketplace.

Success on this front will come too late for the golden year of photonics in 2019 – but it could help to spur a golden decade for CST Global.

Driving GaN into the fast lane

With automotive qualification in tow, EPC's GaN FETs are hitting the highways, reports Rebecca Pool.



Alex Lidow: "There is really no longer a valid excuse for a designer not to be into GaN – it really is get on board or get lost."

ASK EPC's chief executive, Alex Lidow, what the future holds for his GaN power device business, and automotive certification features prominently.

Recently delivering AEC Q101-qualified 80 V discrete transistors for LiDAR, 48 V power distribution systems and other applications, the company's latest enhancement-mode FETs deliver higher switching frequencies and efficiencies than silicon MOSFETs, in a smaller footprint. And this is just the beginning.

"We have more transistors as well as integrated circuits designed for LiDAR [sensors] and are proceeding with automotive certification here," highlights Lidow. "LiDAR is under intense cost and performance pressure so integrating components and improving performance while lowering the cost is a big deal."

According to the GaN pioneer, the industry is under a lot of pressure right now to get many GaN components AEC qualified. LiDAR sensor makers such as Veladyne and Quanergy have been supplying devices to the likes of Caterpillar and Ford for several years, for use in autonomous vehicles as well as safety systems and mapping applications. Here GaN FETs can be used to create the high-current, short-width pulses that LiDAR needs for high-resolution, long-distance measurements.

Meanwhile industries from cars to computing are shifting from 12 V to 48 V electrical distribution buses as demand for high intensity headlamps and in-car high fidelity-infotainment swells. Each application benefits from small, fast and efficient GaN transistors.

"I see a dozen businesses putting GaN into production and whether it's Chrysler or General Motors, the car companies are very serious and want everything to have automotive qualification," says Lidow. "So we're seeing a pull for automotive certification on these products, and importantly, qualification also says to the entire world that we are ready – the bar was set and GaN jumped right over it."

Indeed, Lidow is certain that industry concerns have dissipated. Reticence and reliability concerns from design engineers already working with silicon power MOSFETs have gone, the supply chain is more than in place and, importantly, prices are competitive.

"In volume pricing, some of parts are in the US 20 cents range which is where silicon MOSFETs tend to floor out as well," he says. "I do think some people have a misimpression on the price of GaN, based on the fact that low-volume pricing is all you see if you go to a distributors website. Until you really find out the high-volume price, you don't get that nice surprise."

"So GaN does have this reputation, but we are eating away at it one volume order at a time," he adds.

All onboard

From word go, EPC has focused on low-voltage devices, leaving higher-voltage applications to the likes of Transphorm and MACOM. Indeed, last year, Transphorm delivered the world's first AEC-Q101 qualified GaN transistor, which at 650 V, targeted AC-DC conversion for electric vehicle on-board chargers and auxiliary high-voltage DC-DC conversion in air conditioning, heating, power steering and oil pumps.

While many manufacturers continue to push higher-voltage GaN-on-silicon devices through qualification, Lidow still reckons the real action lies with lower-voltage devices, and as such, his company has a two-pronged strategy.

First, the company will continue to deliver smaller, cheaper and higher-performing chips. "We're at 'Generation 5' today but if we assume we can reach theoretical performance, then we have the opportunity to shrink these devices by 300 times," says Lidow. "That would take us to 'Generation 8' over a period of sixteen years, and that's very much like the trajectory of the power MOSFET in the 80s and 90s."

At the same time, Lidow and colleagues will deliver more and more sophisticated GaN integrated circuit systems. While the company has been working with Texas Instruments and other companies on co-packaged silicon driver ICs and GaN device systems, monolithic GaN ICs are coming.

"Unless you have a very small GaN device that you can drive off a logic gate, then you need a driver IC, and Texas Instruments, uPI, Murata, Maxim and Intersil have all been making ICs to work with our GaN," points out Lidow. "However, the silicon driver really limits the speed of the GaN device... but integrating the driver electronics onto the GaN transistor chip eliminates this."

Indeed, EPC launched its first driver plus FET ICs in March this year. These 200 V integrated gate driver ICs are free of the parasitic inductances that reduce transistor speeds, and have been designed to target wireless power and high-frequency DC-to-DC conversion applications.

Come 2019, Lidow reckons the half-bridge circuits, level shifters and drivers will all be monolithically integrated onto his eGaN FETs. "Right now we are at the beginning of a general trend of adding more functionality to the GaN discrete device to save money, design time, performance, everything," he says.

Without a doubt, GaN has been moving forward rapidly, broadening the performance gap with silicon with each passing year. Today, more and more players, including China-based companies, are joining the market and as Lidow puts it: "there is really no longer a valid excuse for a designer not to be into GaN – it really is get on board or get lost".

But as more companies join the industry, isn't EPC concerned about increasing competition? In short, no.

"More companies in the supply chain make customers more inclined to use the product, nobody likes sole sources," points out Lidow. "So, as I have said to others in this GaN world; for the next five years you are my friend and I will promote your products like I promote my own, but after that the gloves come off."

β-Ga_2O_3 The next chapter

Speeding MOCVD growth sets the stage for device development

BY ROSS MILLER, FIKADU ALEMA AND ANDREI OSINSKY FROM AGNITRON TECHNOLOGY

GALLIUM OXIDE is a very promising material for making power and optoelectronic devices. It has a great set of intrinsic properties, and preliminary device testing indicates that it could have the upperhand over SiC and GaN power devices in high-voltage switching. What's more, it has the potential to produce high-performance solar-blind UV photodetectors.

This ultra-wide band gap material comes in five different flavours. The most promising is the monoclinic polymorph β-Ga_2O_3. It has the unique combination of a very large bandgap energy – it is 4.9 eV – and a conductivity that can be varied over a vast range, due to doping control that extends from 1 x 10^{15} cm^{-3} to 1 x 10^{20} cm^{-3}. Armed with these attributes, β-Ga_2O_3 can withstand electric fields that could cause failure in SiC and GaN.

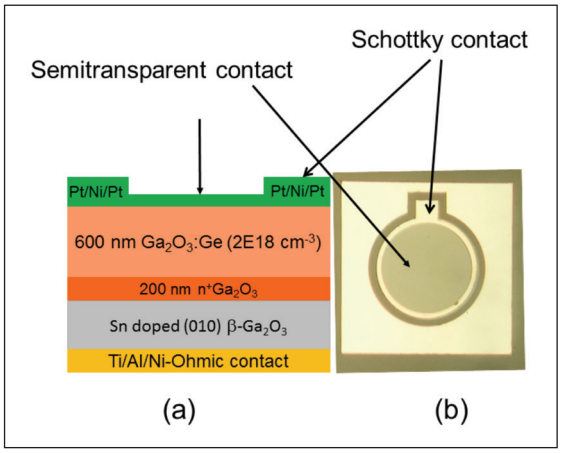


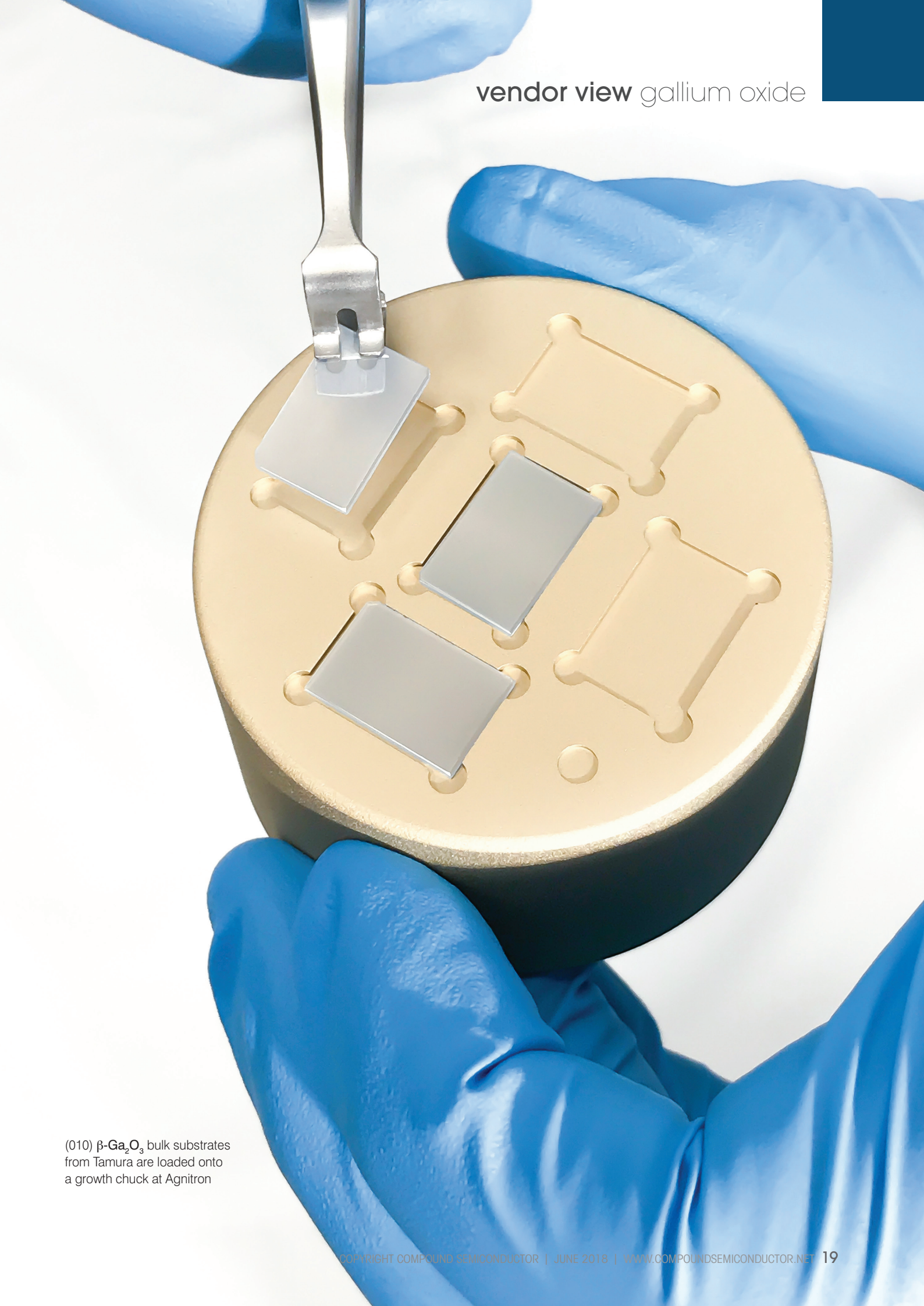
Figure 1. (a) Cross-sectional view of the photodiodes based on a β-Ga_2O_3:Ge homoepitaxial film grown by MBE on the bulk n^+ β-Ga_2O_3 substrate. (b) Optical image showing the top view of the vertical Schottky photodiode.

Holding back progress with β-Ga_2O_3-based devices are weaknesses associated with the growth of its epilayers. Drawbacks with MOCVD, MBE and HVPE are preventing the rapid deposition of thick films of β-Ga_2O_3 and its related alloys with properties needed to underpin the commercialisation of power devices and photodetectors.

But these issues are not insurmountable, according to our work at Agnitron Technology of Eden Prairie, MN. Our efforts have shown that with the right approach, MOCVD has been demonstrated to support growth rates up to 10 μm/hr, which is more than an order of magnitude higher than previously; far higher electron mobilities than before; and complementary AlGaO alloys with an aluminium content of more than 40 percent.

Native substrates

Another appeal of β-Ga_2O_3-based technology is that native substrates are available and can enable growth of high-quality epilayers without special techniques required when epilayers and substrates are crystal lattice mismatched. This foundation can be produced by several techniques, including edge-defined film-fed growth and the Czochralski technique.



(010) β-Ga_2O_3 bulk substrates from Tamura are loaded onto a growth chuck at Agnitron

	Si	GaAs	4H-SiC	GaN	β-Ga_2O_3	Diamond	AlN
Bandgap E_g (eV)	1.1	1.4	3.3	3.4	4.9	5.5	6.2
Electron mobility μ ($cm^2 V^{-1}s^{-1}$)	1400	8000	1000	1200	250	2000	850
Breakdown field E_{br} (MV cm^{-1})	0.3	0.4	2.5	3.3	8.0	10.0	15.4
Relative dielectric constant ϵ	11.8	12.9	9.7	9.0	10.0	5.5	8.5
Saturation velocity V_{SAT} (10^7 cm s^{-1})	1.0	1.2	2.0	2.5	1.1	1.0	2.0
Thermal conductivity λ (W m^{-1} K^{-1})	150	50	370	130	10 [100] 30 [010]	2000	340
Baliga's FOM $(\mu\epsilon E_{br}^3)$	1	15	340	870	3444	24661	59160
JFOM $(V_{SAT}E_{br})$	1	2	17	28	29	33	103
HMFOM$(E_{br}\mu^{0.5})$	1	3	7	10	11	40	40
HCAFOM $(\epsilon\mu^{0.5}E_{br}^2)$	1	5	48	85	225	619	1479
HTFOM $(\lambda\epsilon^{-1}E_{br}^{-1})$	1	0.23	0.36	0.1	0.01	.86	0.06

Table 1. Comparison of various semiconductor material properties as well as several key figures of merit (taken from the last two papers listed in *Further reading*). Commercial development of β-Ga_2O_3 devices will have to consider thermal management and packaging R&D, due to the relatively low thermal conductivity of this oxide.

One tremendous advantage of being able to produce native substrates is that it enables the growth of low-defect-density epitaxial films. These are a prerequisite for producing power electronics devices with a high critical electric field strength as defects are a primary cause for device breakdown at lower than expected fields.

In addition, melt techniques – and specifically the Czochralski technique that is used to make countless silicon substrates – have already realised low material costs by scaling up production. Assuming sufficient demand, one should expect that costs for β-Ga_2O_3 substrates can asymptotically approach cost parity with those for silicon and sapphire.

Note that the road to commercialisation for β-Ga_2O_3 is markedly different to that for SiC and GaN. Both those materials have far better material properties for high-voltage operation than those of silicon, but have faced manufacturing challenges, due to various issues related to substrates and processes. This leaves the door ajar for alternative material systems, including Ga_2O_3, which is not hampered by those weaknesses and may offer differentiated performance for some applications.

Our initial involvement with β-Ga_2O_3 was not associated with power devices, but with UVC photodetectors. Working in partnership with researchers at the University of California, Santa Barbara (UCSB), and the University of Central Florida (UCF), we fabricated Schottky photodiodes with this material system.

Despite a lack of optimisation, these detectors exhibited a high photoresponsivity and a high rejection ratio (see Figures 1 and 2). We believe that further effort, enabling a tuning of the energy gap and cut-off wavelength by bandgap engineering via compositional tuning of β-$(AlGaIn)_2O_3$ alloys, could lead to the commercialisation of true solar-blind, full UV spectrum detectors.

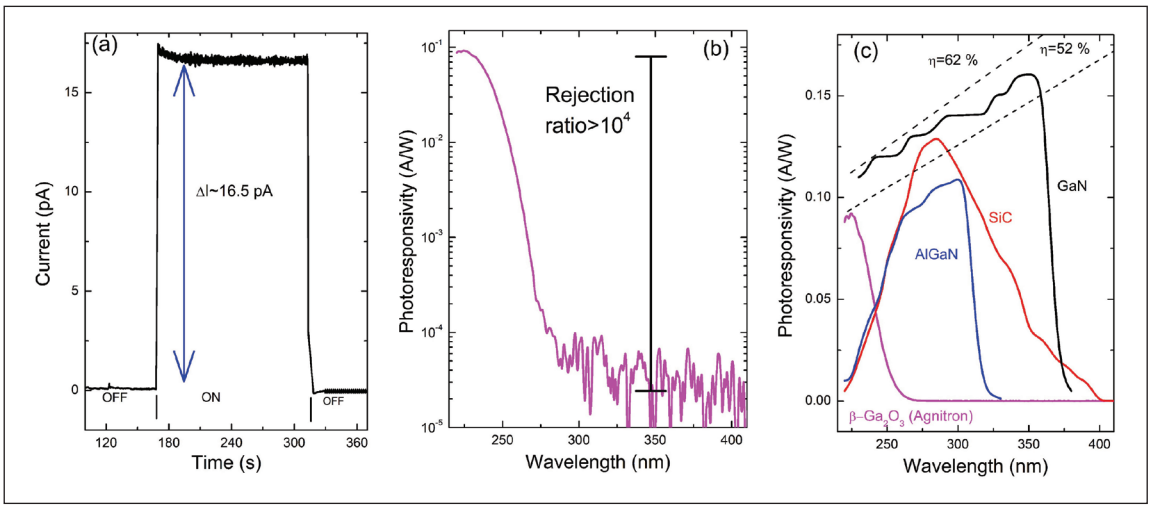
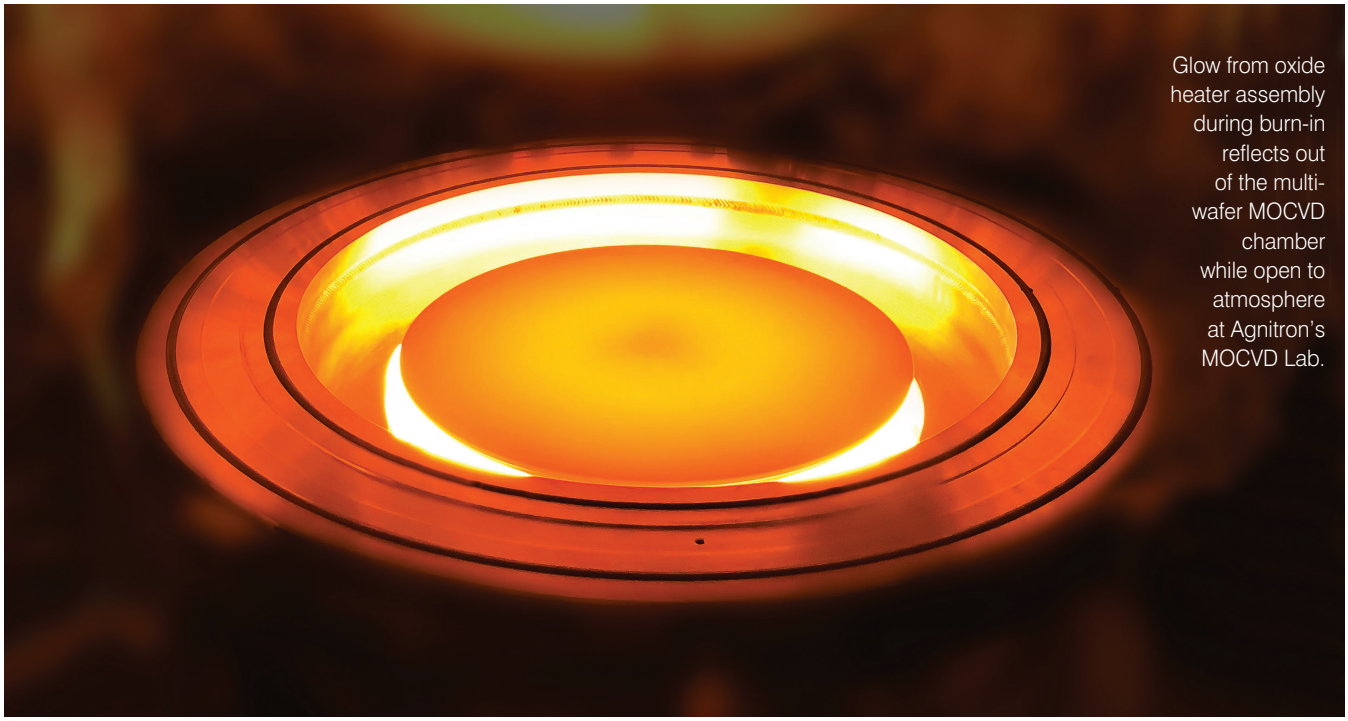


Figure 2. (a) Current-time characteristics of the vertical Schottky device based on β-Ga_2O_3: Ge epitaxial film from Figure 1 under dark and illuminated conditions. (b) Spectral response of the Pt-β-Ga_2O_3:Ge vertical Schottky photodiode. (c) Comparison of the photoresponsivity of the non-optimized β-Ga_2O_3: Ge photodiode (magenta) with commercial devices based on GaN (black), SiC (red) and AlGaN (blue) wide bandgap semiconductors. Estimated quantum efficiency is represented by the dashed lines.



Glow from oxide heater assembly during burn-in reflects out of the multi-wafer MOCVD chamber while open to atmosphere at Agnitron's MOCVD Lab.

There is no doubt, however, that β-Ga_2O_3 is attracting the greatest interest as a material for making power electronics. Offsetting its many strengths is that, like other oxide semiconductors, realising a usable *p*-type doping in this material is elusive – and this might always be so.

However, due to its ultra-wide bandgap and controllable *n*-type doping over a vast range, there is much interest in developing unipolar devices with vertical and lateral conducting topologies for switching and RF device applications. Progress to date for demonstration of over 1 kV vertical devices includes Schottky diodes, reported in 2017 by a team from NICT in Japan as well as FETs recently by Cornell University – and far greater success could follow, as the great intrinsic properties of β-Ga_2O_3 put realisation of vertical geometry devices with switching voltages exceeding 10 kV on the horizon. Recent demonstration of high mobility two-dimensional electron gas (2DEG) in β-Ga_2O_3 based heterostructures by Ohio State University and Air Force Research Laboratory also indicates a path to devices which may exceed the voltage performance of GaN HEMTs.

Epitaxial growth challenges…

For high-power β-Ga_2O_3-based diodes and transistors operating in the kilovolt range, epilayers with a thickness of typically 10 μm or more are needed. Growth rates for MBE are only hundreds of nanometres per hour, ruling out this approach.

The low growth rate is not the only issue, however. Power devices also require layers of the alloy $(Al_xGa_{1-x})_2O_3$, in order to form a two-dimensional electron gas. Studying the phase diagrams for Al_2O_3-Ga_2O_3 reveals that it is challenging to achieve

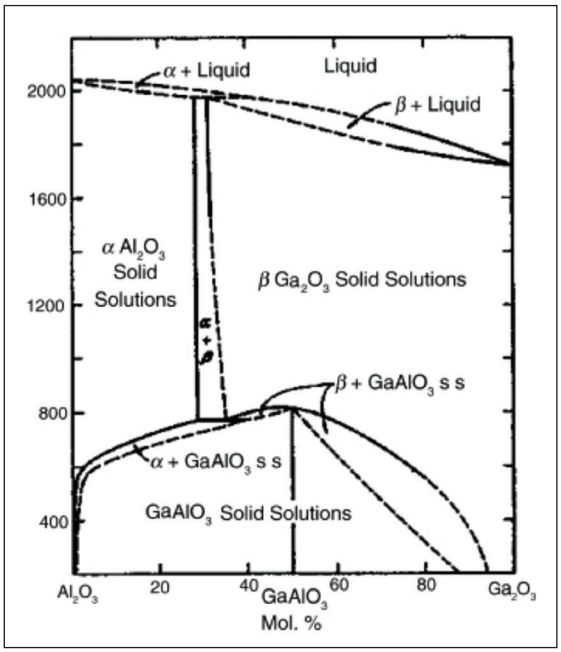


Figure 3. The phase diagram of Ga_2O_3 and Al_2O_3. [Hill *et al.* J. Am. Cer. Soc. **35** 135 (1952)]. Solubility of Al_2O_3 in β-Ga_2O_3 is drastically reduced below 800°C by formation of the $GaAlO_3$ intermediate compound. MBE growth temperatures are limited to around 600-700 °C due to decomposition of Ga_2O_3 to volatile sub-oxides. Thus, in MBE growth, the maximum Al_2O_3 content in β-Ga_2O_3 is around 20 percent. In contrast, MOCVD growth over 800 °C would facilitate growth above the solid phase congruent point and would allow up to about 60 percent Al_2O_3 content in the β-Ga_2O_3 phase.

Table 2. Summary of various β-Ga_2O_3 material parameters illustrating recent advances for β-Ga_2O_3 MOCVD growth processes. *The result indicates incorporation of an aluminium mole fraction of 0.43 can be achieved in an β-$(Al_xGa_{1-x})O_3$ alloy grown by MOCVD.

Properties of β-Ga_2O_3 MOCVD Epitaxial Films	Agnitron Results
UID β-Ga_2O_3 electron mobility ($cm^2 V^{-1}s^{-1}$), RT	120-150
UID β-Ga_2O_3 carrier concentration, cm^{-3}	$<3x10^{16}$
SI β-Ga_2O_3 sheet resistance, MΩ/square	>1
Controlled doping concentration range, cm^{-3}	$3x10^{16}$-$1x10^{20}$
XRD FWHM (arcsec)	<40
Growth rate (μm hr^{-1})	Up to 10
RMS roughness (nm)	< 0.3
Al in β-$(Al_x, Ga_{1-x})_2O_3$	0.43*

the temperatures and pressures required for growth of aluminium-rich $(Al_xGa_{1-x})_2O_3$ alloys (see Figure 3).

Prior to our work, many limitations also plagued MOCVD. Its growth rate for β-Ga_2O_3 could not exceed 500 nm/hr; doping concentration was limited, and could not drop below 1 x 10^{17} cm^{-3}; electron mobilities lagged behind theoretical levels, and those demonstrated by MBE; and the composition of $(Al_xGa_{1-x})_2O_3$ was limited, and its doping challenging.

… and breakthroughs

Our overcoming of all these limitations can be traced back to our involvement in a two-year STTR programme sponsored by the Army Research Office. In the latter part of this effort, we were tasked with finding a suitable buffer layer for enhancing the performance of solar-blind, MgZnO-based photodetectors. Up until that point, ZnO had been used as a buffer on sapphire – but this limited device performance, by tending to absorb incident radiation at longer wavelengths than that of the MgZnO films.

The remedy, recommended by acting ARO programme monitor Michael Gerhold, involved a switch to β-Ga_2O_3, in the form of either a substrate or buffer material. Through the course of investigating this material, we became acutely aware of MOCVD growth limitations.

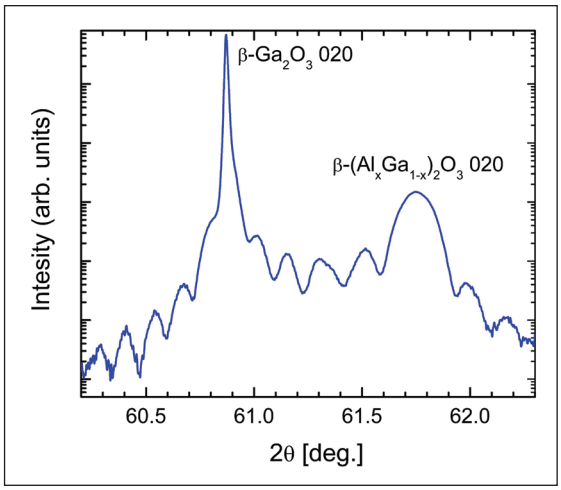


Figure 4. XRD ω-2θ scan profile of a strained β-$(Al_{0.21}Ga_{0.79})_2O_3$/$Ga_2O_3$ heterostructure grown on a (010) β-Ga_2O_3 substrate by MOCVD. The β-$(Al_{0.21}Ga_{0.79})_2O_3$ layer is 70 nm thick.

Following the completion of this project, we embarked on a programme sponsored by the Office of Naval Research (ONR) that focused on increasing the growth rate of MOCVD-grown β-Ga_2O_3. Success would aid the development of high-voltage power electronic devices, which could be used on military vessels for weapon and transportation systems, such as rail guns, as also for air and missile defence radar and propulsion.

We have made major strides in this latest STTR programme, involving UCSB, and through this effort we have been able to increase the growth rate to 10 μm/hr. Success is not realised by simply increasing the flow of precursors. Although this helps a little, it doesn't address the limiting factor. The difficulty with the growth of Ga_2O_3 is that when metal organic precursors are injected into the oxygen-rich environment of the growth chamber, they react rapidly in the gas phase, impairing precursor efficiency and ultimately applying the brakes to the growth rate. Our solution is to optimize the pressure and growth temperature, and combine this with a close injection showerhead design that reduces the time that the process gases are mixed, prior to reaching the growth surface. Thanks to this, there is an increase in the number of active precursor species reaching the growth surface, leading to a hike in both the precursor efficiency and the growth rate.

An increase in the growth rate of β-Ga_2O_3 must go hand-in-hand with other improvements in MOCVD growth technology for this ultra-wide bandgap oxide. Advances must also be made in the range of dopant concentrations, and in realising low background concentrations, a high carrier mobility, a smooth surface morphology and high aluminium content β-$(Al_xGa_{1-x})_2O_3$ alloys. We have succeeded on all these fronts (see Table 2 for details).

Our breakthroughs in the doping of β-Ga_2O_3 include the use of a new approach. Previous efforts involved either tetraethyl orthosilicate (TEOS) or tri-ethyl tin (TESn), while we have used silane as a source of Silicon. Merits of the latter include its common use in MOCVD production processes, allowing delivery in high and low concentrations that support high and low doping levels – the doping range exceeds previous reports by roughly an order of magnitude in both directions.

We have also realised a substantial increase in the electron mobility of epitaxial, undoped bulk films achieving comparable mobility as is observed in the high-quality undoped native substrates – about 150 $cm^2 V^{-1} s^{-1}$. In addition, we have set a benchmark for electron concentrations in MOCVD-grown films – our material can have electron concentrations that are more than three times lower than those in any other reports. Yet another encouraging result is that, according to X-ray diffraction scans, our epitaxial film crystal quality is so high that it is limited by the starting native substrate. Taken together, all these experimental results indicate a reduction in carrier compensation and scattering in our material, due to reductions in gallium vacancies, dislocations and point defects.

Another breakthrough is the development of a novel, proprietary process for the growth of highly resistive semi-insulating β-Ga_2O_3 epitaxial films. Layers of highly resistive semi-insulating β-Ga_2O_3, which are essential for the fabrication of lateral and vertical conducting power devices, are usually formed by adding deep impurities, such as iron or magnesium. But these additions are far from ideal: as they are highly mobile, they can diffuse to adjacent layers, where they are so detrimental that they hamper device performance.

What's more, when iron and magnesium impurities are introduced into an MOCVD growth chamber they have a 'memory effect', and special treatment is needed to prevent them from having an unwanted impact on subsequent growths. Our proprietary processes avoids these pitfalls for semi-insulating films, while expanding the range of controllability for *n*-type doped β-Ga_2O_3 using a range of precursors, which improves process flexibility.

We have also championed the MOCVD growth of aluminium-rich $(AlGa)_2O_3$ alloys, breaking new ground with a ternary with an aluminium content of 43 percent. Note that even higher values should be possible. We have also formed: a high-quality, strained $(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ heterostructure, which is a critical building block for various device structures (see Figure 4 for an X-ray diffraction spectra); and a strained β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ superlattice with abrupt interfaces (see Figure 5). The latter promises to provide defect/dislocation management during the growth of heterostructures, and could be used to form an active region for multi-channel, laterally conducting devices. The next steps will include further optimisation of controllable, *n*-type doping in AlGaO alloys, a key ingredient for making devices.

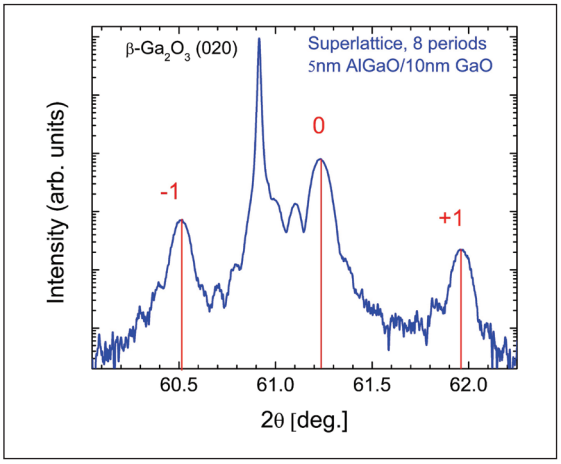


Figure 5. (020) XRD ω-2θ scan for the first β-$(Al_{0.21}Ga_{0.79})_2O_3$/β-$Ga_2O_3$ superlattice structure grown by MOCVD at Agnitron Technology. The superlattice structure has 8 periods of β-$(Al_{0.21}Ga_{0.79})_2O_3$/β-$Ga_2O_3$, and the thickness of the β-$(Al_{0.21}Ga_{0.79})_2O_3$ barrier and β-Ga_2O_3 well are 5 nm and 10 nm, respectively. Although this structure is not optimized, observation of Pendellösung fringes in the XRD scan are an indication of surface and crystal qualities. This result represents an important demonstration of MOCVD capabilities.

The successes we have had will enhance the foundation for upcoming device development. We believe that by optimising the MOCVD process, β-Ga_2O_3 and its related alloys can be achieved with properties to enable fabrication of devices which encroach theoretically predicted performance. Growth rates are now high enough for commercial device production, but they need to be realised in far larger multi-wafer platforms delivering sufficient throughput of high-quality epitaxial material.

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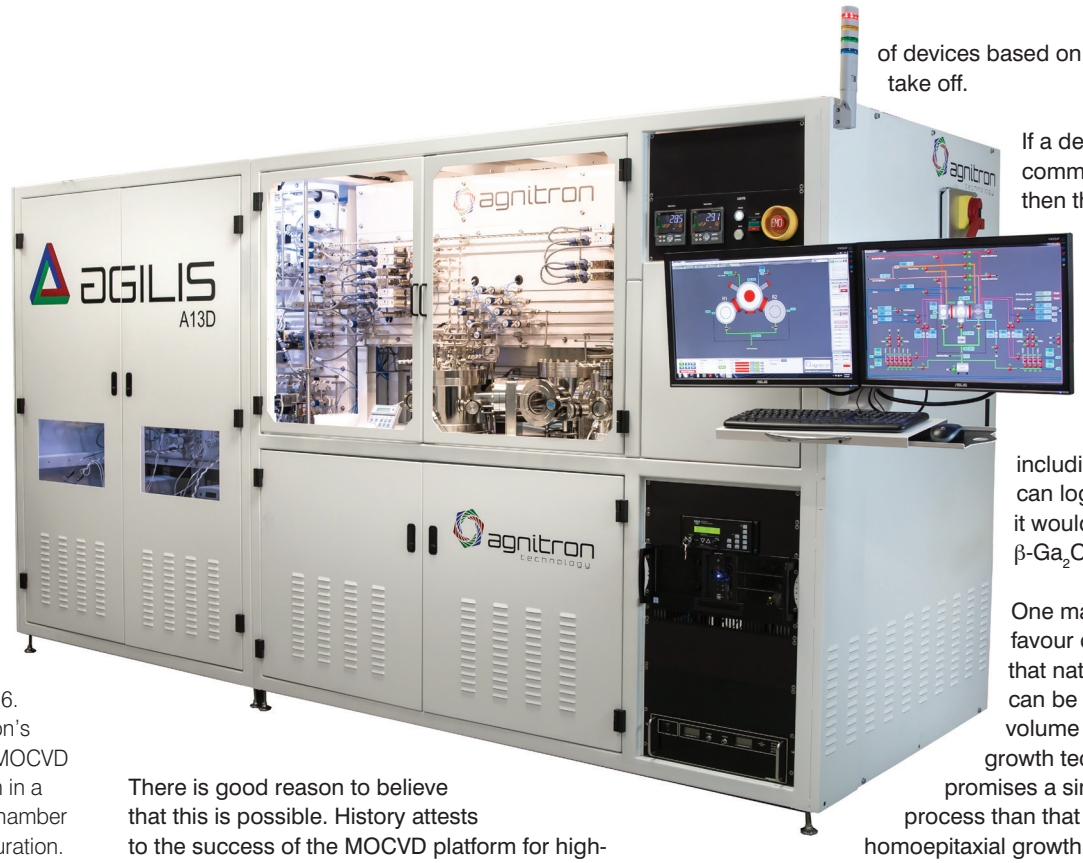

Figure 6. Agnitron's Agilis MOCVD system in a dual-chamber configuration. The β-Ga_2O_3 configuration is currently available with single chamber designs and specifications noted in Table 3.

There is good reason to believe that this is possible. History attests to the success of the MOCVD platform for high-volume manufacture of LEDs, laser diodes, and power devices. This growth technique also offers wide process windows and an expansive set of precursors, equipping engineers with the levers they need to optimise selective regrowth, alloying, doping, compensation control, growth rates and gas phase reactions. However, even though MOCVD is a proven success for high-volume manufacturing of nitrides, phosphides and arsenides, it doesn't follow that it's a sure bet for β-Ga_2O_3. Oxide MOCVD growth has its own unique set of process-related challenges, and they must be addressed if the commercial production of devices based on β-Ga_2O_3 is to take off.

If a device is to be a commercial success, then the costs associated with epitaxial growth must be modest. After all, that's been the case for other compound semiconductor device types, including LEDs, so one can logically assume that it would be the same for β-Ga_2O_3 based devices.

One major factor in favour of β-Ga_2O_3 is that native substrates can be produced by volume scalable bulk growth techniques. This promises a simpler growth process than that for GaN. With SiC, homoepitaxial growth is used, but the substrates are pricey, so it is feasible that the production costs for β-Ga_2O_3-based devices could even undercut those for SiC and GaN, if volumes were high enough.

To support the commercialisation of β-Ga_2O_3, we have been working with UCSB to improve MOCVD growth technology associated with this oxide. Efforts began with extensive flow and chemical modelling to identify ideal precursor candidates and establish growth condition windows. This work also helped with the reactor design.

MOCVD System Parameter	Single Wafer	Multi-Wafer
Wafer loading capacity	1x2"	5x2"
Heating method	Induction, 1-zone	Resistive, 2-zone
Max process temperature	1050°C+	950°C
Max rotation speed (RPM)	300	1500
Alkyl source channels	5	5
Oxygen precursors	O_2, H_2O, tert-Butanol	O_2, H_2O, tert-Butanol
Carrier gasses	N_2, Ar	N_2, Ar
Number of dopant source channels	2	2
Control system package	Imperium-MOCVD	Imperium-MOCVD

Table 3. System specification for the new Agilis β-Ga_2O_3 Configuration MOCVD system from Agnitron. Specifications refer to the standard system configuration; some parameters are customizable or expandable.

We are now on our fourth and fifth generations of reactor configurations for the growth of β-Ga_2O_3. These latest configurations, featuring improved gas injection, are capable of providing process conditions required to achieve world-class β-Ga_2O_3 material growth.

Using this configuration, we have recently added a tool to our portfolio of Agilis Series R&D MOCVD Systems (see Figure 6). This system is available with single and multi-wafer reactor geometries, and initial customer orders are scheduled for Q3 delivery.

The release of this tool will help to spur the development of β-Ga_2O_3 optoelectronic and power applications. But there is much work still to do. The multi-wafer configurations are small, and must be scaled while maintaining material quality, in order to trim epitaxial costs. In addition, while it is clear that wide bandgap devices are destined to improve the energy efficiency in electric vehicles, data centres and distributed energy resources, there is still uncertainty over the role that will be played by the various wide bandgap devices. What are the best opportunities for β-Ga_2O_3, and where can GaN and SiC shine?

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HIGHLIGHTING HETEROGENEOUS INTEGRATION

Rising sales of GaN-on-silicon power and RF transistors, alongside the emergence of photonic and logic devices on silicon, is underscoring the bright future for heterogeneous integration

BY RICHARD STEVENSON

GaN is a revolutionary material. It is behind the development of the solid-state lighting industry, it has provided the key ingredient in the Blu-ray player, and it is now starting to improve the efficiencies associated with wireless infrastructure.

In addition, there is also another legacy that GaN is leaving – but in this case, one that is easy to overlook. Due to the lack of affordable, widely available native substrates, GaN has shown that heterogeneous integration can yield high-quality commercial devices. Pairing GaN epilayers with either sapphire, silicon or SiC substrates has enabled the manufacture countless, reliable devices that crop up everywhere.

Where GaN has led, can GaAs and InP follow? Well, the motivation of slashing chip costs by switching to a cheaper substrate, such as silicon, still stands, but it's not so easy with those III-Vs. While GaN devices can be riddled with defects and still deliver a strong performance, that's not the case for variants based on GaAs and InP. Progress is being made, but it is lagging behind that of GaN.

An opportunity to judge how far GaAs and InP devices are off the pace set by GaN – and an insight as to how far the latter has come – was given to delegates at this year's CS International Conference, held on 10 and 11 April at the Sheraton Airport Hotel in Brussels. At that gathering, co-located with the third Photonic Integrated Circuits International and the inaugural High End Sensors International, attendees had the chance to hear: Yole Développement's Technology and Market Analyst, Hong Lin, discuss the status and outlook of the GaN-on-silicon market; Jean-Pierre Locquet from KU Leuven detail developments

CTO of NaAsP$_{III-V}$, Wolfgang Stolz, explained that the company's defect-free GaP-on-silicon templates have been used to produce lasers using pseudomorphic growth.

in a European project aiming to deliver the dense integration of GaN power switches and CMOS drivers; Wolfgang Stolz, CTO of NAsP$_{III-V}$, outline the construction of III-V devices on CMOS-compatible silicon; and Lars-Erik Wernersson from Lund University talk about the development of III-V nanowire MOSFETs for RF and digital applications.

GaN-on-silicon success

Lin began her talk by saying that GaN, which has a 17 percent lattice mismatch with silicon and a thermal coefficient mismatch of over 50 percent, is now a mainstream technology in the power sector, a challenger in RF, and a candidate for making microLEDs.

The Yole analyst pointed out that GaN-on-silicon is no longer a new technology in the power industry. "The first devices were in 2010, by International Rectifier. Since then, other companies have come to the playground." These firms include EPC and Transphorm, which released their first GaN devices within a year or so of IR, and more recently Fujitsu, Panasonic, GaN Systems, Texas Instruments and Visic. The majority have produced devices with blocking voltages of around 600 V, while EPC has launched a portfolio of products operating at 200 V and below.

One trend that Lin noted is a shift from discrete GaN-on-silicon power devices to power ICs. This can take the form of power devices integrated with drivers and possibly other analogue IC functions, an approach adopted by Navitas and Dialog; or a system-in-a-package, an approach taken by Texas Instruments.

Lin expects the GaN-on-silicon power market to mushroom over the next few years, with total sales climbing from $23 million in 2017 to almost $462 million in 2022. By then, sales to power supply manufacturers will be the largest sector, worth $242 million, while the electric and hybrid electric vehicle market will generate $58.9 million, and the server and data centre market $54.5 million.

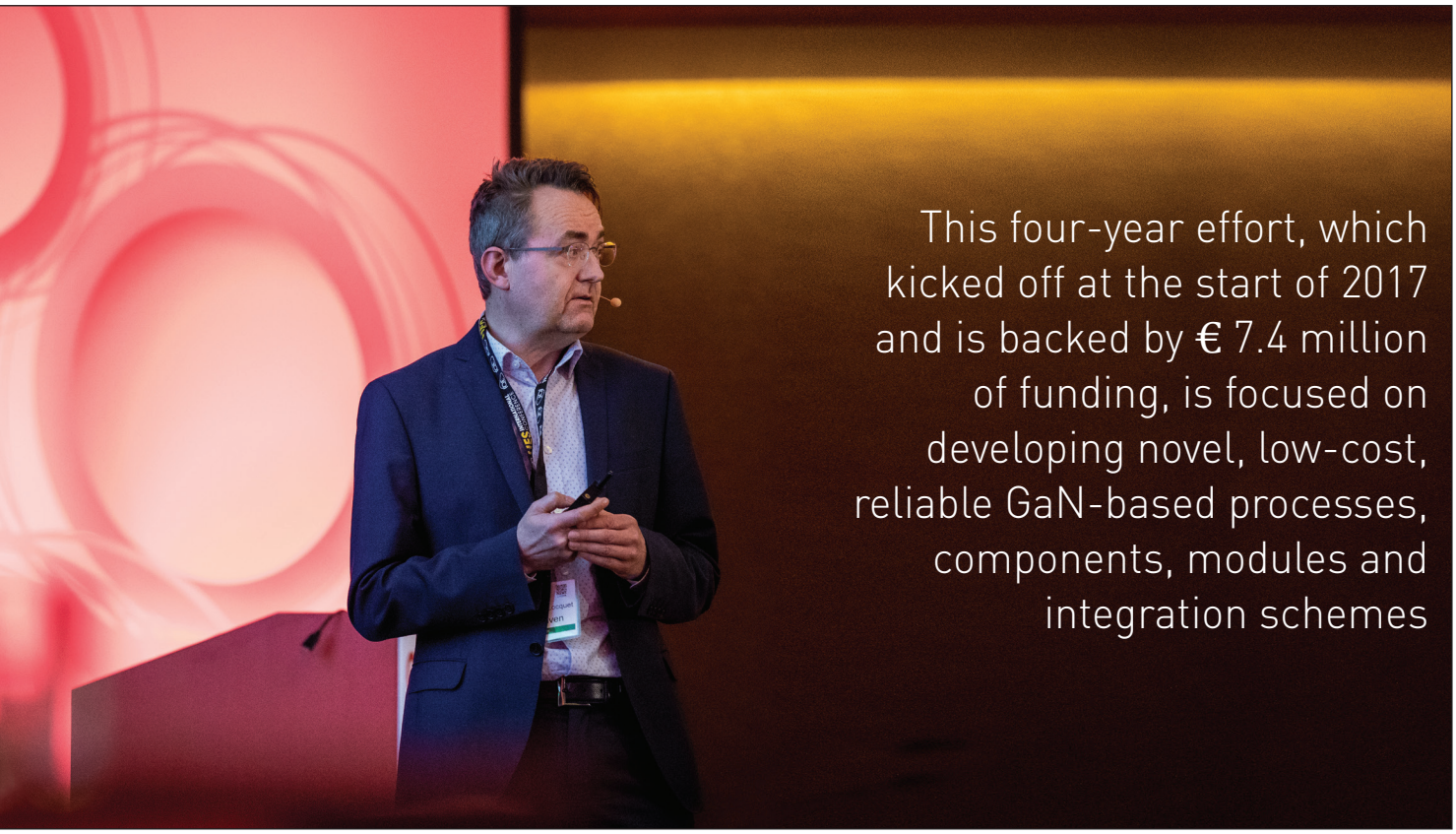
Despite this rapid ramp in sales, the power market for GaN-on-silicon will still be far smaller than that for GaN RF. According to Lin, global sales for GaN-on-silicon and GaN-on SiC products for RF applications will net $457 million in 2018, climbing to $1.14 billion by 2022, with revenue dominated by the military and base station markets.

Both of these markets are performance driven, so Lin expects them to be dominated by GaN-on-SiC (see Figure 1). She argues that the best opportunities for GaN-on-silicon are in the RF energy, cable TV, and satellite markets, where this material combination can serve high-volume, cost-sensitive applications. This could help to swell sales for GaN-on-silicon RF towards $100 million by 2023.

GaN on CMOS

The keynote presentation in the heterogeneous integration session came from Jean-Pierre Locquet from the Functional Nanosystems Group at KU Leuven, who detailed the on-going GaN on CMOS project.

This four-year effort, which kicked off at the start of 2017 and is backed by €7.4 million of funding, is focused on developing novel, low-cost, reliable GaN-based processes, components, modules and



Jean-Pierre Locquet from the Functional Nanosystems Group at KU Leuven gave a keynote presentation detailing the on-going GaN-on-CMOS project.

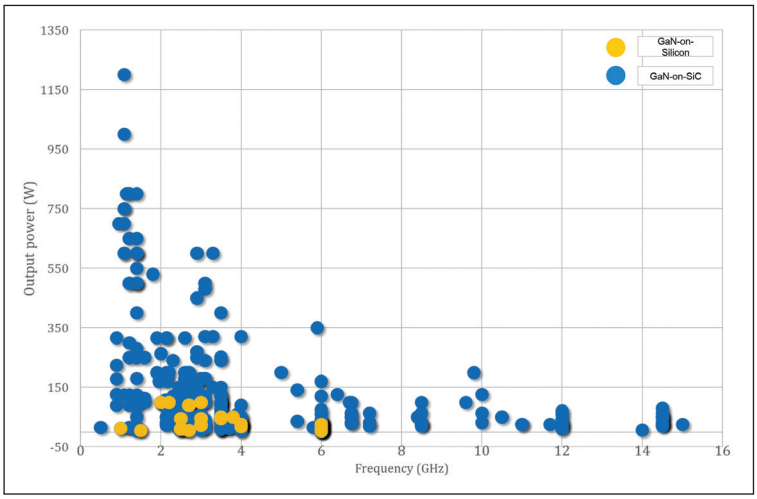


Figure 1. GaN-on-SiC devices operating in the RF are more plentiful, and can operate over a wider range of frequencies, compared with those based on GaN-on-silicon. Data is taken from the 2018 Yole Développement report *RF GaN Market: Applications, Players, Technology and Substrates*.

integration schemes. Success on all fronts will allow the team to demonstrate the performance and economic potential of their technology at the system level, and showcase its capability to slash the energy consumed by a wide range of products, including those that require voltages of 100 V or less.

Eleven partners are involved in the project. They are the academic institutions KU Leuven, IHP, Fraunhofer IAF, Tyndall, and several companies operating at different positions within the supply chain: EpiGaN, XFab, AT&S, NXP, Recom, PNO Innovations and IBM.

Many of the delegates may not have heard of AT&S, but it is, according to Locquet, the biggest PCB board manufacturer in Europe. Meanwhile, the most well-known partner is the project, IBM, is hoping to benefit from its results. “They have a power issue with their servers,” explained Locquet.

During the project, the team will develop ever more sophisticated techniques for unifying GaN and silicon CMOS technologies. The starting point is at the package level, with a GaN switch on top, bonded to a laminate that has inductors, capacitors and CMOS chips embedded within it. Following on from this, the team will integrate at the stack level, sandwiching the GaN switch between a laminate containing capacitors on one side, and on the other side a CMOS chip with

embedded inductors. The final solution is described as a fully integrated device – the GaN chip is unified with the CMOS chip using a back-end-of-line process.

Locquet believes that the project will be highly innovative. Developments will include: dense integration of GaN power switches and CMOS drivers via direct wafer bonding; improvements to epiwafers, to enable a trimming of loss in switches operating below 100 V; the fabrication of normally off devices using a low temperature process; and the introduction of new soft magnetic core materials and packaging techniques that boost inductor efficiencies. In addition, Locquet provided details of how this may be accomplished, and the level of improvement wrought. He claimed that today's typical 650 V devices, which are E-mode designs that sport a cascade configuration, have figures of merit at 600 V of 5 mΩ cm^2 for the product of on-resistance and current, and 0.5 nΩC for the product of on-resistance and charge. The plan is to develop 100 V devices that save energy, thanks to values of 0.1 mΩ cm^2 and 0.05 nΩC.

Further gains will come from improving the process for making the GaN contact, by replacing an 800 °C step involving 30 s of annealing with one between 400 °C and 450 °C, using laser annealing. There will also be the introduction of a laminate nanocrstalline core material, rather than the standard single-plated nickel; and the replacement of a 32 nm silicon CMOS technology for making the buck convertor with a GaN-on-silicon device. These changes will enable a hike in the frequency for the voltage regulator module to more than 10 MHz, and an increase in the system power density from typically 0.09 Wmm^{-3} for today's GaN-based systems to more than 0.3 Wmm^{-3}.

Locquet and co-workers are planning to produce a portfolio of demonstrators. There will be a 200 W demonstrator at the package level, a 20 W prototype at the stack level, and a 5 W device at the chip level. These devices are targeting the manufacturers of cars, airplanes, electric bikes and boats, and the builders of datacentres.

The partners are working on the development of their new technologies and processes. The project still has more than two years to run, and during that time results of working devices will start to appear.

Growing III-Vs on silicon

High-efficiency solar cells, III-V FETs, lasers and other photonic devices are all potential applications for III-Vs on silicon, according to CTO of $NAsP_{III-V}$, Wolfgang Stolz. At this year's CS International, he highlighted the capability of his company's growth technology, now pursued with an Aixtron tool that accommodates 300 mm diameter silicon wafers.

Results that showcase the company's defect-free, GaP-template technology include X-ray diffraction scans that highlight the uniformity of the material across the 300 mm-wide surface, and dark-field transmission electron microscopy images that reveal the high quality of the III-V layer. Stolz also showed atomic force microscopy scans, indicating a root-mean-square surface roughness of just 0.23 nm over a 15 μm by 15 μm area.

These defect-free, GaP-on-silicon templates have been used to produce lasers, using pseudomorphic growth. "There is no lattice mismatch, and no misfit dislocations," said Stolz, who argued that his company's technology offers the potential for producing devices with long lifetimes.

Lasers have been formed with the GaP-on-silicon templates that feature BGaAsP wafeguides and claddings, and GaNAsP quantum wells. By varying the composition and thickness of these wells, the electroluminescence peak can span the spectral domain from 850 nm to 1.2 μm.

Stolz and his co-workers have verified electrical injection with their devices, and are now working on optimising the electrical efficiency of their lasers and developing ridge waveguide structures. This could lead to the introduction of completely embedded lasers, formed by depositing the devices in recessed stripes (see Figure 2). Using this geometry could retain the planarity of the silicon wafer, and prevent cross-contamination, if silicon overgrowth and SiO_2 side-wall passivation are used to hide the devices.

Nanowire MOSFETs on silicon

Within the silicon IC industry, two of the key changes since the turn of the millennium have been the introduction of new materials with a higher dielectric constant, and architectures that increase the control that the gate has over the carriers in the channel. The next step could be the use nanowires. According to Lars Wernersson from Lund University pointed out that new architectures and materials are needed to maintain the march of Moore's Law – and that III-V nanowires could have a big part of play in this evolution.

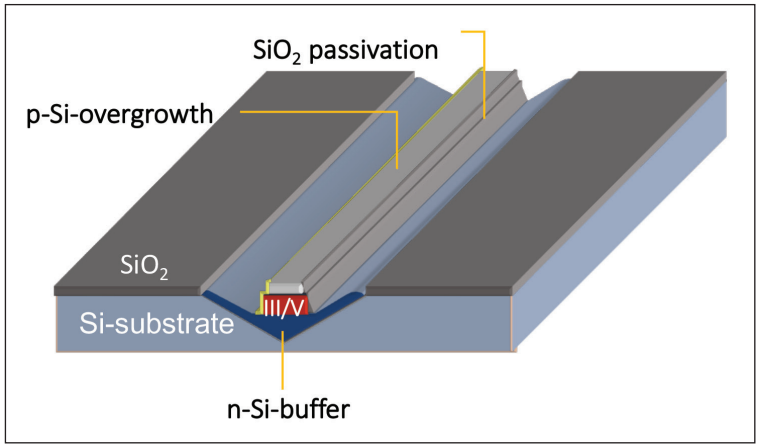


Figure 2. Work at $NAsP_{III-V}$ could lead to the introduction of completely embedded lasers, formed by depositing devices in recessed stripes. Merits of this approach include retaining the planarity of the silicon wafer and preventing cross-contamination.

Lars Wernersson from Lund University, who spoke at CS International, silicon nanowire FETs are moving towards production, while variants based on III-Vs are promising to enhance CMOS logic and RF performance.

To make the case that III-Vs are no longer seen as a highly esoteric material within the silicon industry, Wernersson cited the work of TSMC, which has developed a III-V buffer on 300 mm silicon wafers and produced fin-based devices with a sub-threshold swing of around 80 mV/decade; and he recounted the efforts of a collaboration between IBM and Samsung that had produced devices with an on-current of 250 μA/μm, using a technique known as aspect ratio trapping.

Continuing in this vein, Wernersson and his co-workers are developing III-V FETs that feature a nanowire. Merits of this one-dimensional structure include advantageous transport and a wrap gate geometry – enabling a high transconsductance, high drive current, and a low output conductance. What's more, nanowires have a small footprint. "This avoids defect propagation from the surface," argued Wernersson.

Vertical nanowires are used by the team from Lund, because they increase the available space for the ohmic contacts, relax the requirements for shrinking dimensions, and, according to some results, they deliver a superior performance – for nanowire ring oscillators, power is 35 percent higher at the 5 nm node with a vertical geometry.

Back in 2017 Wernersson's team reported the results of III-V vertical MOSFETs formed with nanowires with a 28 nm diameter. These transistors, which had a 75 nm gate length, combined a transconductance of 2.4 mS/μm with an on-current of 410 μA/μm and operation at 85 mV/decade.

Wernersson and his co-workers have also produced lateral InGaAs nanowires on InP. These devices, which are claimed to be "state of the art", sport a transconductance of 3.3 mS/μm, an on-current of 650 μA/μm at 0.5A, and a maximum oscillation frequency in excess of 400 GHz.

To evaluate the capability of these devices as ICs, the researchers have teamed up with IBM and Leti. This effort has shown that III-Vs can be processed at low temperatures, using an approach the has no impact on circuits formed with a fully depleted, silicon-on-insulator technology.

The team from Lund has also partnered with Fraunhofer IAF. On 4-inch GaAs wafers, engineers produced 80 nm lateral MOSFETs without a spacer layer between the oxide and the channel, before using these building blocks to construct amplifiers that delivered 20 dB of gain from 75 GHz to 100 GHz.

Wernersson and co-workers have also explored tunnel FETs. Vertical InAs-based devices with nanowire widths of 88 nm and 63 nm have produced sub 60 mV/decade operation at drive currents ranging from 1 nA/μm to 300 nA/μm, along with good electrostatic control.

The efforts of the team from Lund, and other developers of compound semiconductor devices on silicon, show that the benefits of this form of heterogeneous integration can be exploited. Sales of these devices are sure to rise over the coming years.

Yole Développement's Technology and Market Analyst, Hong Lin, told delegates at CS International that she expects the GaN-on-silicon power market to grow very fast over the next few years, with total sales climbing from $23 million in 2017 to almost $462 million in 2022.

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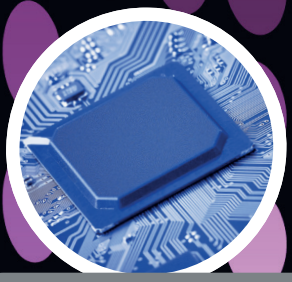

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Power

Varying fortunes for CS shares

European makers of growth tools are topping this year's share price leaderboard

IT'S NOT BEEN a great 12 months for investors in the compound semiconductor industry. Within this sector, it is slightly more likely for share prices to have fallen than gained. However, a canny investor – or indeed a lucky one – could still have enjoyed great returns with shares within this industry. The key is not just to identify which type of company is going to see the greatest increase in share price, but pick the winners.

The best companies to have invested in for the last 12 months have been a pair of equipment manufacturers: Aixtron and Riber. Share price gains for these two firms have been just over 150 percent and 100 percent, respectively. However, their rival across the pond, Veeco, has not enjoyed anything like the same success. Although, over the last few years, it has overtaken Aixtron as the leading supplier of MOCVD tools, an indifferent last 12 months has seen its share price tumble by more than 50 percent. That drop has led Veeco to foot this year's share *Compound Semiconductor Share Price Leaderboard* (see p.34).

A turnaround at Aixtron

The tremendous hike in Aixtron's share price over the last 12 months is a reflection of the transformation of the company. Back in early 2017, the German toolmaker ran at a loss, but now it's profitable, orders are up, and the future is far, far brighter.

Speaking to investors on 26 April to discuss the results for the first fiscal quarter 2018, ending on 31 March this year, company president, Bernard Schulte remarked that Aixtron was having the strongest start to the year since 2011.

"Our business enjoys a positive momentum with strong interest for our full range of products, but

in particular for all manufacturing solutions for the production of lasers, such as vertical-cavity surface-emitting lasers for 3D sensing and optical datacom applications," added Schulte.

Aixtron's business is continuing to outperform its own expectations. Orders for the first quarter stood at €79 million, 27 percent higher than the same quarter last year, and 20 percent ahead of the previous quarter.

Encouragingly, the growth in the size of the order book has gone hand-in-hand with an increase in gross margin. This hit 43 percent in the most recent quarter, up 4 percent sequentially, and an increase of 18 percent year-on-year.

The high gross margin is helping the company to turn a profit. Judged in terms of earnings before interest and tax, the last quarter netted close to €8 million, while net profit came in slightly above €12 million. Schulte attributes the success to several factors, including a robust line of products, and a resilient, cost-effective, flexible business model that has enabled the tool maker to benefit from today's strong market conditions.

"We have gone through a successful reorientation of our technology portfolio, and now have a durable and focused product portfolio in growth areas such as specialty LEDs, lasers and power electronics."

When the order book for any company grows, some will question whether the firm can handle the additional work. This should not be an issue for Aixtron.

"Our manufacturing model is very well capable of digesting this uptick," argued company president Felix Grawert during the latest earnings call. According to him, tool manufacture is aided by preassembly from Aixtron's suppliers. This allows engineers at Aixtron to focus on production planning, orchestration of the assembly on the shop floor, and testing assembled tools.

Growing orders will place strain on the service team. To address this, the aim is to not recruit staff, but improve efficiency, via a reduction in the installation time per tool.

The outlook for Aixtron is very positive. In February the company revealed that sales for the year should be in the range €230 million to €260 million, and the figure for earnings-before-interest-and tax should be between 5 percent and 10 percent of sales. With recent business going better than anticipated, the company now expects the 2018 figures to be towards the top of its earlier guidance.

Riber's rebound

At Riber, the French manufacturer of MBE tools and evaporation sources, the company's finances have followed a very similar path to those at Aixtron. Helping to almost double Riber's share price has been a return to profitability, a considerable increase in gross margin, and a buoyant order book.

For the French firm, dramatic growth in evaporators to the photovoltaic and screen industries has driven the increase in sales. Despite a fall from €8.8 million to €7.2 million for MBE system revenue between fiscal 2016 and 2017, sales have shot up from €16.5 million to €30.6 million over that timeframe, primarily due to a hike in evaporator revenues from €3 million to €16.2 million.

On 26 April, Riber released its results for the first fiscal quarter of 2018, which ended on 31 March. Sales were down €2 million compared with the previous quarter in 2017, but this should not be a concern, according to the company, because it reflects a staggering of deliveries for the photovoltaic and screen industries over the first two quarters of this year.

Compound Semiconductor share price leaderboard						
Rank	Company	Ticker	Share value, April 28, 2017 ($)	Share value, April 27, 2018 ($)	% appreciation	Change in Rank
1	Aixtron (Frankfurt)	AIX	6.13*	15.59*	154.5	+12
2	Riber (Paris)	RIB	2.106*	4.39*	108.5	+2
3	Cree	CREE	21.99	37.33	69.8	+12
4	IPG Photonics	IPGP	126.32	213.21	68.8	+6
5	IQE (London)	IQE	86.10*	142.7*	65.8	-4
6	Lumentum	LITE	42.75	50.95	19.2	-1
7	NASDAQ composite	IXIC	6047.61	7136.88	18.0	+5
8	Infinera	INFN	9.92	11.70	17.9	+8
9	Qorvo	QRVO	68.03	67.32	-1.0	-1
10	Oclaro	OCLR	8.01	7.79	-2.7	-4
11	Rubicon	RBCN	7.50	6.87	-8.4	+3
12	AXT	AXTI	6.75	5.98	-11.5	-10
13	Skyworks	SWKS	99.74	87.32	-12.5	-4
14	Finisar	FNSR	22.84	15.50	-32.1	-3
15	Emcore	EMKR	9.00	4.60	-48.9	-8
16	Veeco	VECO	33.00	15.80	-52.1	-13
	* Converted to dollars using the exchange rates on 28 April of 1 EURO = 1.2131 USD and 1 GBP = 1.3776 USD					

What is encouraging is Riber's order book. On 31 March this stood at €36.1 million, 112 percent higher than it was a year ago. Included are orders for 13 MBE systems, nine of which are production machines.

Cree's beneficial U-turn

In third place on the *Compound Semiconductor Share Price Leaderboard* is Cree. Its shares have risen steadily over the last 12 months, to increase in value by nearly 70 percent.

Cree is now heading in a very different direction to the one it planned just over a year ago. Back then it came close to selling Wolfspeed, its SiC electronics business, to Infineon. That deal was blocked, and Cree has subsequently bought Infineon's RF business, a move that will help the company to position itself as one that is not just interested in lighting.

"Wolfspeed, our smallest and most profitable business today, will become our largest and most profitable business over the timeframe of the long-range plan, roughly quadrupling in revenue by 2022," said CEO Greg Lowe during a conference call held on 24 April, to discuss earnings for the third fiscal quarter 2017.

Of late, performance of the Lighting Products segment has been so poor that it has been considered to be overvalued. This has led to a $247.5 million goodwill impairment charge, taken in the most recent quarter. For those three months, sales dropped by 10 percent to $131 million, while gross margin was just 19 percent.

For lighting products, which netted $43 million, gross margin is a little higher – it's just over 26 percent. But that's still far less than that for Wolfspeed. Gross margin of products in this division is 48 percent, while revenue is $83 million, an increase of 46 percent year-over-year.

To maintain this spectacular rate of growth in sales, efforts are underway to double power device capacity compared with where it stood at the end of fiscal 2017.

"As we ramp this new capacity, we anticipate we could have some variability in our initial production yields and factory utilization," explained company CFO Mike McDevitt during the recent earnings call.

So the road to higher margins and greater profitability will be bumpy, but Cree is heading in the right direction.

Aixtron's share price has climbed steadily over the last 12 months.

Veeco's woes

The recent history at Veeco is not dissimilar to that at Aixtron. Revenues are rising and gross margins are getting better, but with Veeco profitability is still around the corner.

Those leading the company are certainly upbeat about its future. "2017 was a truly transformational year for Veeco, remarked John Peeler in the most recent earnings call, held on 12 February to discuss results for the fourth fiscal quarter 2017.

"We completed the acquisition of Ultratech, which is providing us with a more diversified revenue stream, and the integration is proceeding well with greater synergies than we originally expected."

Another major change has been the consolidation of the New Jersey manufacturing facility, a move that is said to generate good annual savings.

"Lastly, we delivered nearly 41 percent non-GAAP gross margins, and our healthy bookings demonstrate our leading position in the markets we serve, and give us confidence in our ability to accelerate profitable growth."

Veeco dominates the MOCVD market, with a 55 percent share of tools for making GaN LEDs, according to IHS. Sales dipped several years ago, due to overcapacity, but the outlook is good.

During the February earnings call, Peeler said that in China, utilization rates in the leading GaN LED chipmaking fabs are in upper 80s, while the figure for the "tier two" fabs is in the upper 70s. "Taiwan's in the 80s. Korea might be low 80s or a little lower."

These rates are high, indicating chipmakers are running close to full capacity, and are buying MOCVD tools.

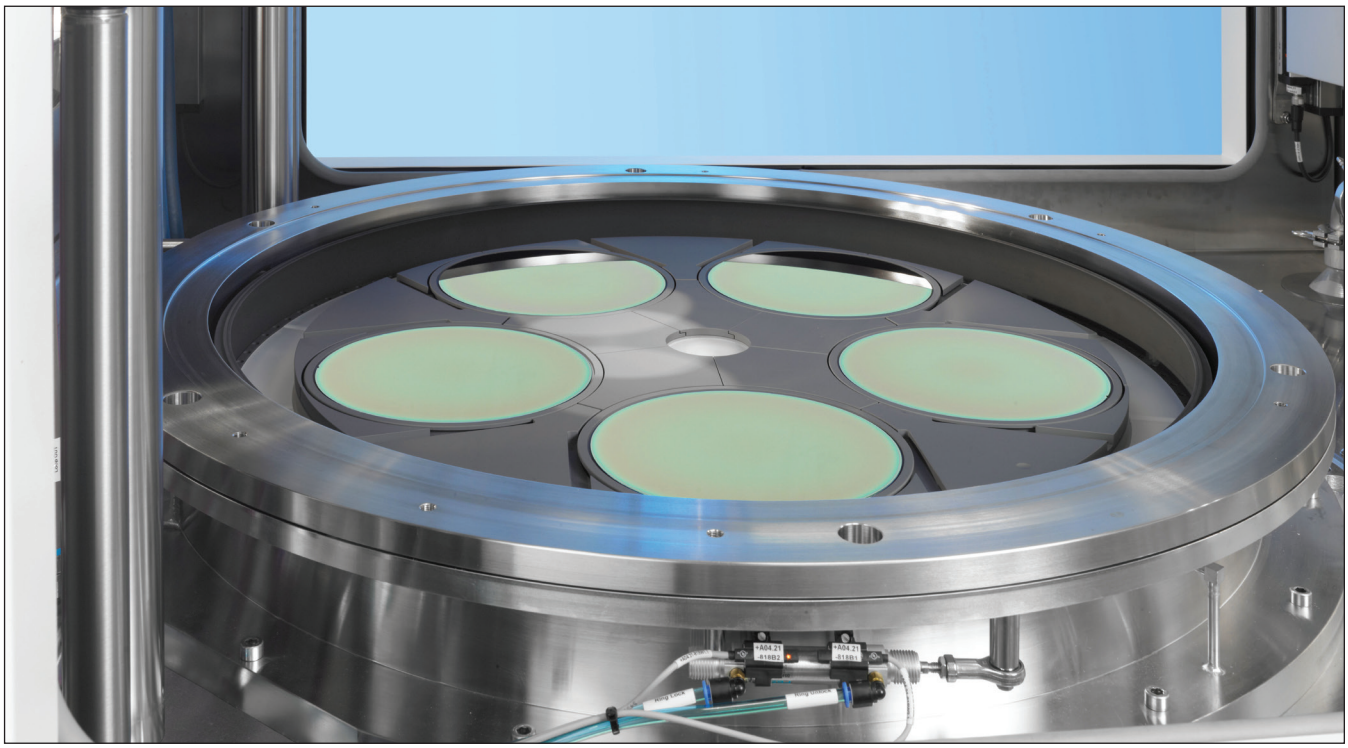
"We expect a solid year in the marketplace," said Peeler. "I think we had some 400 plus reactors in 2017. We think the market will grow over that number, maybe even significantly over that number in 2018."

Targeting this market is the EPIK 868, released last September. "We've shipped several large orders [for this tool] to Chinese customers, as our platform enables greater productivity and lower cost of ownership," said Peeler. "Feedback from customers has been excellent."

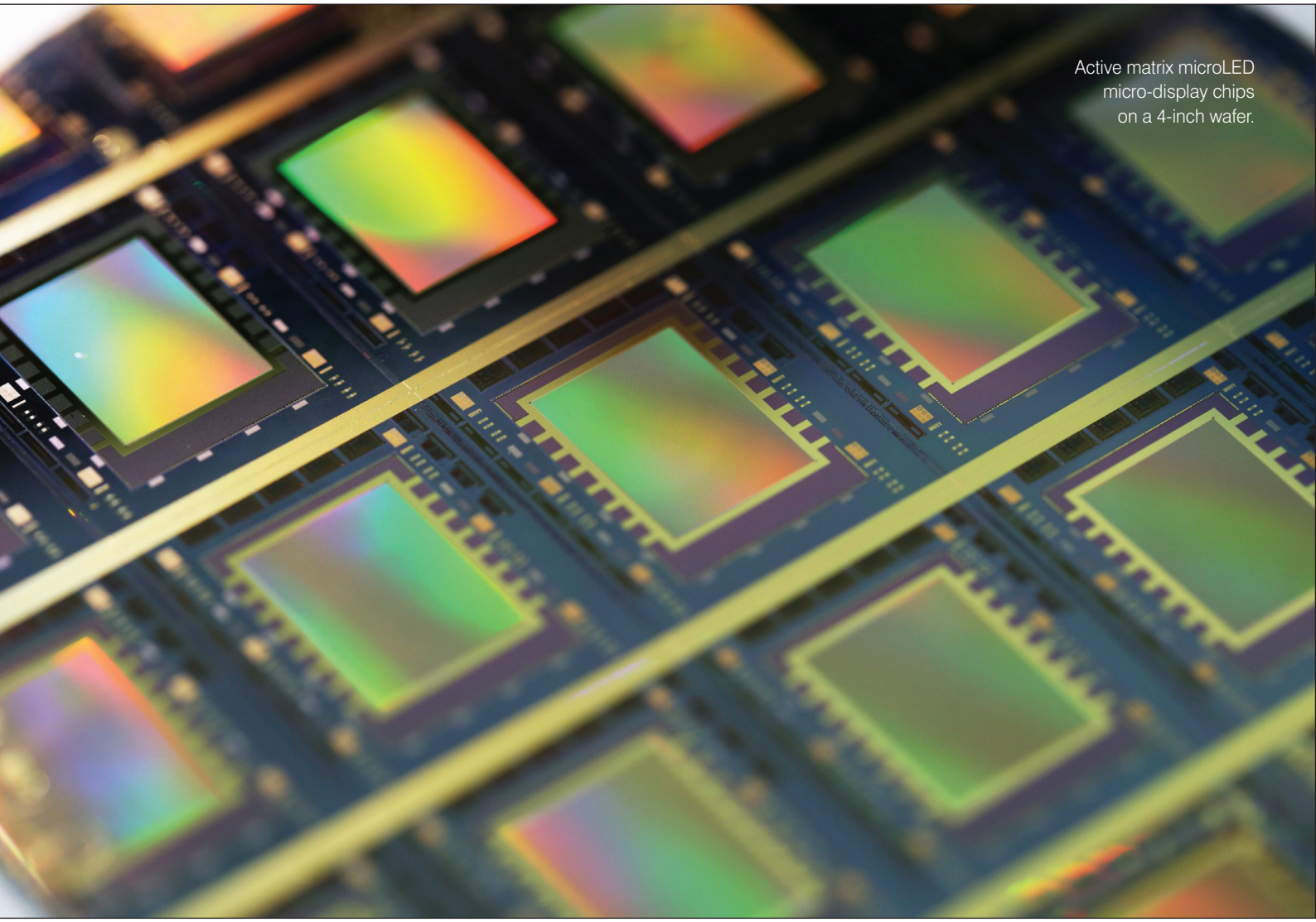
Veeco is also seeing increasing interest in MOCVD tools for the growth of other photonic devices, and also RF devices. This January Osram Opto Semiconductors placed orders for the Veeco K475i and Propel systems, which are designed for the production of power electronics, RF semiconductor devices, LEDs and laser diodes – including VCSELs. Peeler said volumes of the latter device will grow, as it is deployed in smartphones, where it is used for 3D sensing; in LiDAR sensors, used in autonomous vehicles; and in data centres, where it delivers high-speed data transmission.

Further signs of a rise in sales of MOCVD tools for power electronics came in April, when Veeco reported that On-Semiconductor had ordered a Propel High Volume Manufacturing MOCVD tool for the growth of GaN-on-silicon epiwafers.

With bookings growing – they increased for the third consecutive quarter to hit $179 million – and end markets having a positive outlook, Veeco should return to profitability, so long as it can operate with a healthy gross margin. If it succeeds on that front, it is unlikely to be footing the share price leaderboard in 2019.



Aixtron is seeing a growth in sales of MOCVD tools for making power electronic devices. To target this market, it offers the Aixtron G5+, which can accommodate five 200 mm wafers.



Active matrix microLED micro-display chips on a 4-inch wafer.

Mastering the manufacture of **microLED micro-displays**

Wafer-level integration holds the key to high-volume manufacture of ultra-high resolution microLED micro-displays

BY FANG OU AND LEI ZHANG FROM JBD

A REVOLUTION is now underway in micro-displays. Demand for this technology is rising fast, due to a range of emerging applications that include wearable electronics, head-up displays and augmented reality. However, to succeed in the marketplace, these miniaturized displays, which typically have a diagonal screen size of no more than an inch, will have to meet stringent technical requirements that are not fully satisfied by current technologies.

One of the most promising technologies for forming these micro-displays is based around the microLED. This tiny device – the LEDs have dimensions on the order of microns – are directly integrated as pixel elements onto the silicon driver IC backplane.

Taking this approach allows the excellent light emission capabilities of compound semiconductor devices to be paired with the unsurpassed functionalities of the ICs. The displays that result outperform those based on liquid crystal and organic LED technologies, by having the upper hand in terms of brightness/contrast, power efficiency, response time and device reliability. However, their manufacture is far from easy, due to the tremendous challenges associated with the integration of compound semiconductor microLEDs and silicon-based ICs – devices with vastly different material properties and fabrication processes.

Overcoming these obstacles has been the goal of many researchers in academia and industry, who have been spurred on by the alluring market potential of microLED micro-displays. And many have turned their attention to flip-chip technology, which is the most common method for integrating compound semiconductor functional device arrays with silicon-based ICs.

Flipping the chip

The starting point for the flip-chip approach is the design and fabrication of microLED arrays on one substrate, and the design and production of silicon-based pixel driver ICs on another. Crucially, the geometric layouts on both these entities must be identical.

Chip-level fabrication follows, with the individual chips that contain microLED arrays diced and separated from the original wafer. Using a high-precision alignment bonder, microLED arrays are then flip-bonded to silicon ICs using an array of solder bumps. This provides an electrical connection to the pixel driver circuit array.

Aided by good progress in flip-chip technology, some groups have recently reported demonstrations of GaN-based active-matrix microLED micro displays. However, one should note that there are inherent drawbacks associated with flip-chip technology – and they limit the performance and cost of microLED micro-displays.

One significant drawback is that as the fabrication process is at the chip level, it requires precise alignment, which hampers throughput and increases cost. In addition, often transparent substrates are essential, because the microLED growth substrate tends to remain after hybrid integration. And yet another issue is that there is a significant thermal mismatch between the compound semiconductor device substrate and the silicon substrate. This difference introduces built-in stress in the micro-display chips, compromising manufacturing yield and long-term reliability.

What's more, there is limit to how small the pixel size of the microLED can be. It is determined by the capability of the manufacturing equipment and the flip-chip process. Today, there are efforts in industry to realise a pixel size as small as 20 μm, but there is not a foreseeable, clear path with the flip-chip process to shrink this to less than 10 μm while maintaining a reasonable yield and cost. That's a big issue, because microLEDs with a pixel size of less than 10 μm are needed to make displays for augmented reality.

At Jade Bird Display (JBD), a start-up founded in 2015 and headquartered in Hong Kong, we are addressing all the drawbacks of conventional flip-chip technology for the microLED micro-display with a novel, wafer-scale technology. At its heart is the transfer of entire compound semiconductor epitaxial layers onto a silicon IC wafer. This is accomplished by wafer bonding and substrate removal. By adopting a wafer-level epi-transfer process, we eliminate the need for precise alignment, a pre-requisite for flip-chip technology, and we are ultimately able to turn to a high-throughput, wafer-scale fabrication process.

Once we have formed our epi-on-IC templates, we use standard semiconductor device fabrication processes to produce our hybrid chips with different functionalities. With high precision photolithography equipment and processes well established in the semiconductor industry, we can fabricate our compound semiconductor functional device arrays on top of pixel driver circuit arrays with sub-micron alignment accuracy. This holds the key to hybrid

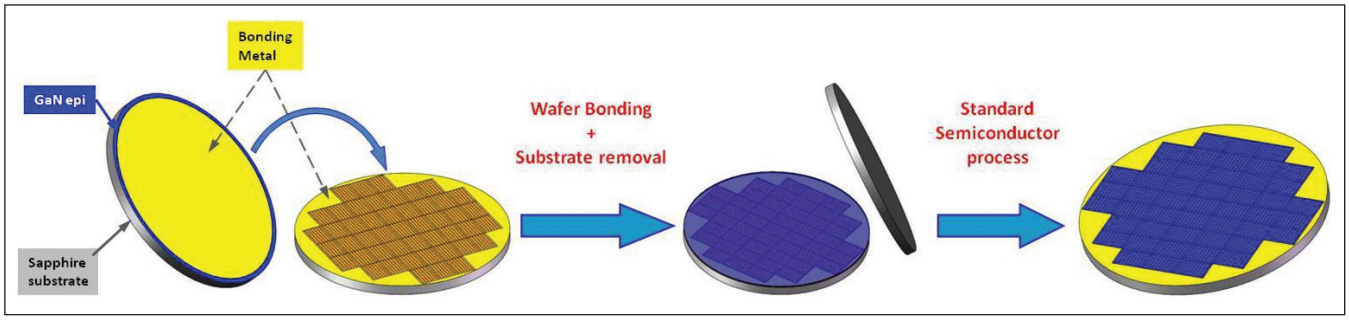


Figure 1. JBD's wafer-scale monolithic hybrid integration technology.

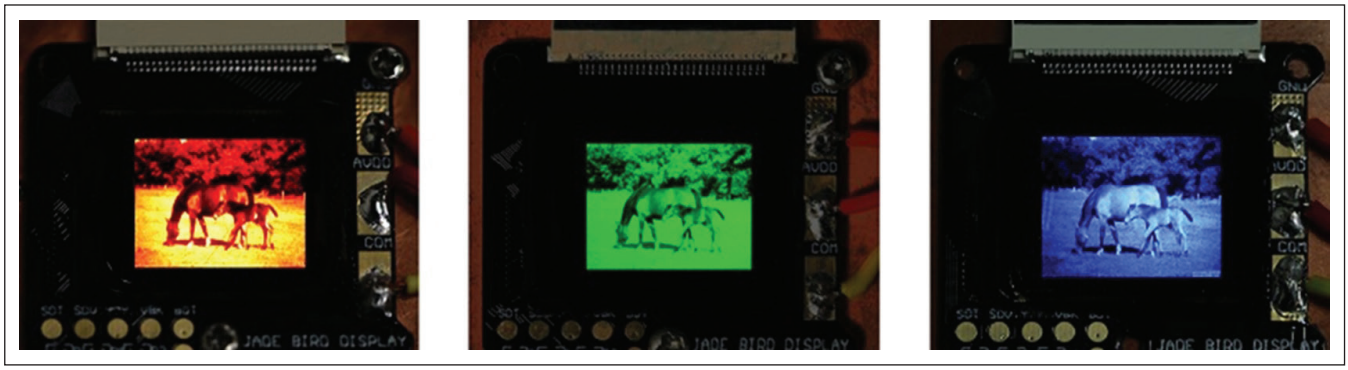


Figure 2. Packaged red, green, and blue active matrix microLED micro-displays.

integration of fine pitch device arrays on silicon ICs with pixel sizes that can be as small as a few microns (see Figure 1).

Another considerable advantage of our technology is that it can utilize well-established infrastructure. Working with equipment sets and semiconductor processes developed by the silicon-based IC industry, we can draw on low-cost mass-production techniques to produce integrated functional hybrid chips, including our high-performance microLED micro-displays.

Promising prototypes

Armed with our technology, we have already made significant strides in the development of microLED micro-displays. Effort began in early 2016, and we realised our first milestone later that year: our first micro-displays. They exhibited exceptional device performances, combining excellent brightness/contrast with power efficiency and a small device footprint. Even with our first attempt, our prototype outperformed existing micro-display technologies by a substantial margin (see Figure 2).

These first monochromatic red, green and blue micro-displays were made in a VGA format and had a standard definition display resolution of 640 pixels by 480 pixels. The green and blue microLEDs were made from InGaN/GaN-based materials, while AlInGaP/GaAs-based materials were used for the red. All these LEDs had a circular geometry, with a diameter of just 6 μm, and they formed a micro-display with a pixel pitch of 20 μm, which corresponds to a resolution of 1,270 pixels per inch. Driven at a peak current per pixel of 20 μA, the brightness of the green LEDs in this display can exceed $5x10^5$ nits – that's over 500 times that of existing, OLED-based self-emissive micro-displays.

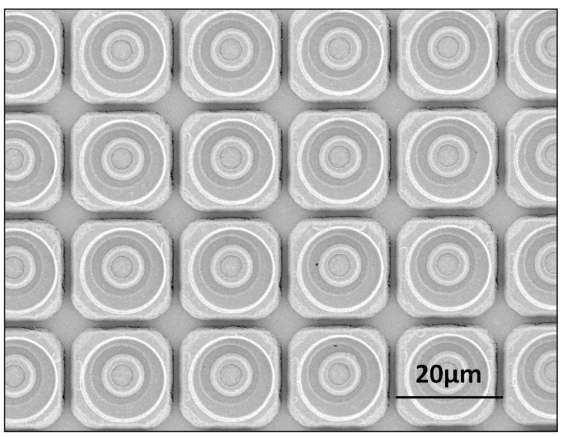


Figure 3. A pixel array with a 20 μm pitch on an active matrix microLED micro-display.

To construct a full-colour micro-display, we could combine three monochromatic microLED micro-displays with external optics, such as a cross dichroic (X-cube) prism. Although this option will appear to lead to increases in the size and volume of the overall display, that's not necessarily the case, because our technology is capable of producing very small microLED micro-displays.

In addition to this approach, which is our current front-runner, we are considering the use of multiple epi transfer processes, which could produce different colour microLED arrays in different layers on the same driver IC substrate. If we were to pursue this, we would expect to use a pixel pitch that is larger than that for our monochromatic displays, as pixels of microLED arrays with different colours will have to be arranged next to each other. Another potential drawback is a reduction in brightness, because light may be blocked by this structure.

To commercialise our core technology, the monochromatic micro-display, we are pursuing a distributed manufacturing strategy. We buy our LED epiwafers, from which microLEDs are made, from conventional LED chip manufacturers. Epiwafers with different substrates can be used to make our displays, so long as the substrate can be successfully removed after the epi-wafer is bonded to the backplane wafer. In most cases, this can be accomplished by making a minor alternation to the fabrication process.

For the backplanes, we outsource the design of the driver IC to firms with extensive expertise in this area, while the tape-out of driver IC backplane wafers is undertaken on a standard 8-inch CMOS line through a foundry service. We use 4-inch LED epiwafers for

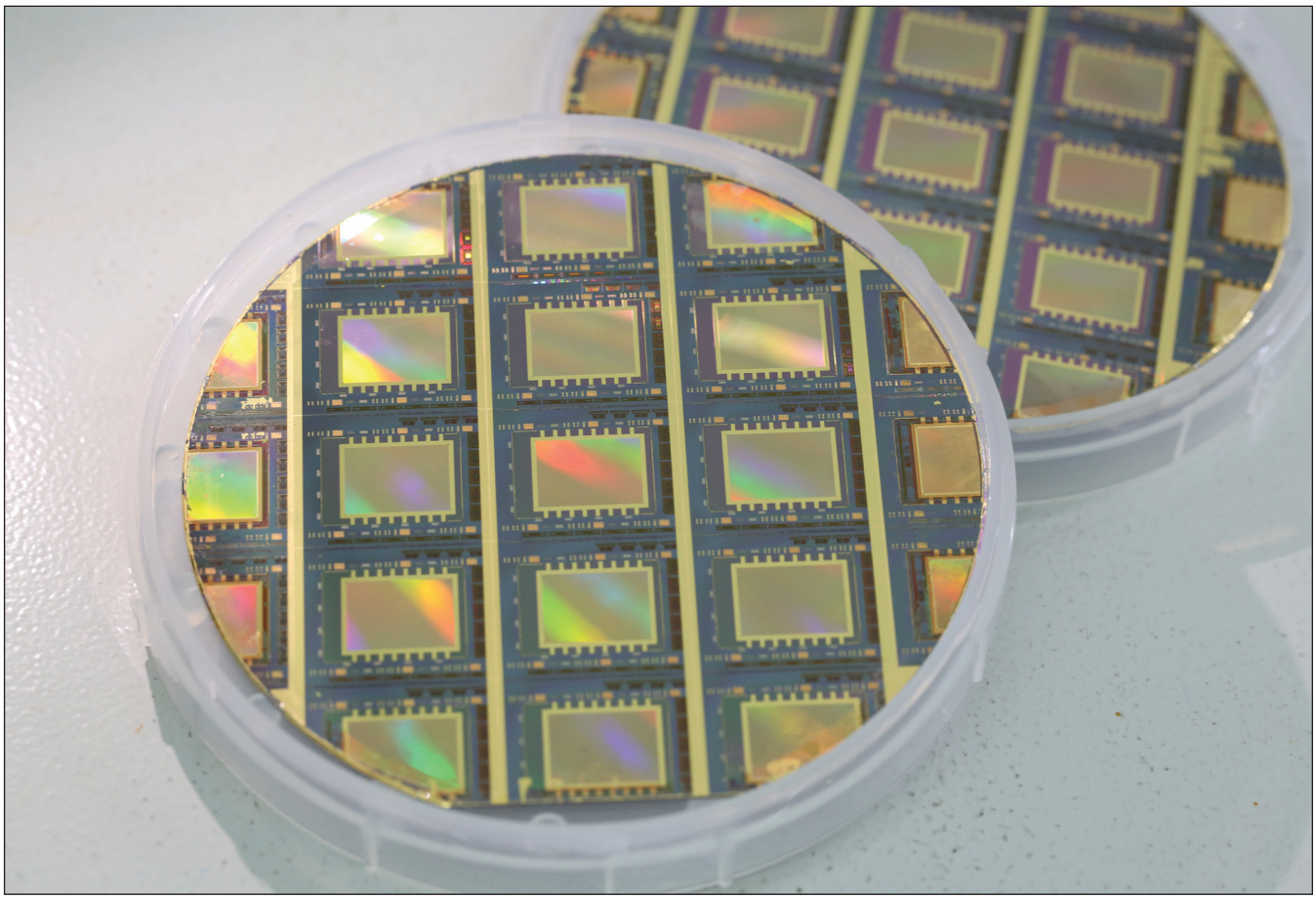


Figure 4. 4-inch wafers of active matrix microLED micro-display chips fabricated using JBD's monolithic hybrid integration technology.

our demonstrations. To accommodate their size, we tailor 8-inch CMOS IC wafers to 4-inch for subsequent device processing. This part of the production process has been performed at a pilot plant operated by one of our strategic partners (see Figure 4). Note that it is easy to scale production to larger diameters than 4-inch, by switching to larger LED epiwafers.

A major benefit of our manufacturing process is its high degree of flexibility. We can make choices that are influenced by epiwafer availability, IC design capability, and the services provided by a CMOS foundry. Ultimately, by outsourcing, we reduce costs associated with capital investment.

Following on from our initial success with microLEDs in late 2016, we have made further progress in two key areas: brightness and resolution. Success on both fronts increases the competitiveness of our technology for projectors and augmented reality, respectively.

Ultrahigh brightness

One of the significant market opportunities for the microLED micro-display is in various forms of projectors, including portable projectors and rear-projection televisions. For these applications, a high luminance of the micro-display panel is essential. Fulfilling this requirement with microLED micro-displays is challenging, with success hinging on various factors, including LED epi-quality, the particular device structure of microLED pixels, and the fabrication process.

Drawing on our extensive R&D experience in the semiconductor industry, we have undertaken a wide-ranging effort, considering modifications to the device structure, optimisation of the fabrication process and the selection of high-luminance LED epiwafers. The fruits of this labour include a reduction in the carrier leakage and the optical loss of microLEDs, and an optimisation of their light extraction efficiency. The devices that result are brighter and more efficient, and have enabled an increase in the brightness of green LEDs on our micro-displays – fabricated on the same driver backplane as those in the initial demonstration – to more than 10^6 nits. For the red, green and blue microLED arrays, external quantum efficiencies are 9 percent, 12 percent and 18 percent, respectively.

In parallel, we have scrutinized the spatial emission properties of our microLEDs, to see whether it is possible to improve brightness in projection applications. Many forms of LED have an inherently large divergent angle that pegs back the optical efficiency for projection systems.With many microLEDs, the root cause of this inefficiency is that a large proportion of light that's emitted from the device is outside the acceptance angle of the

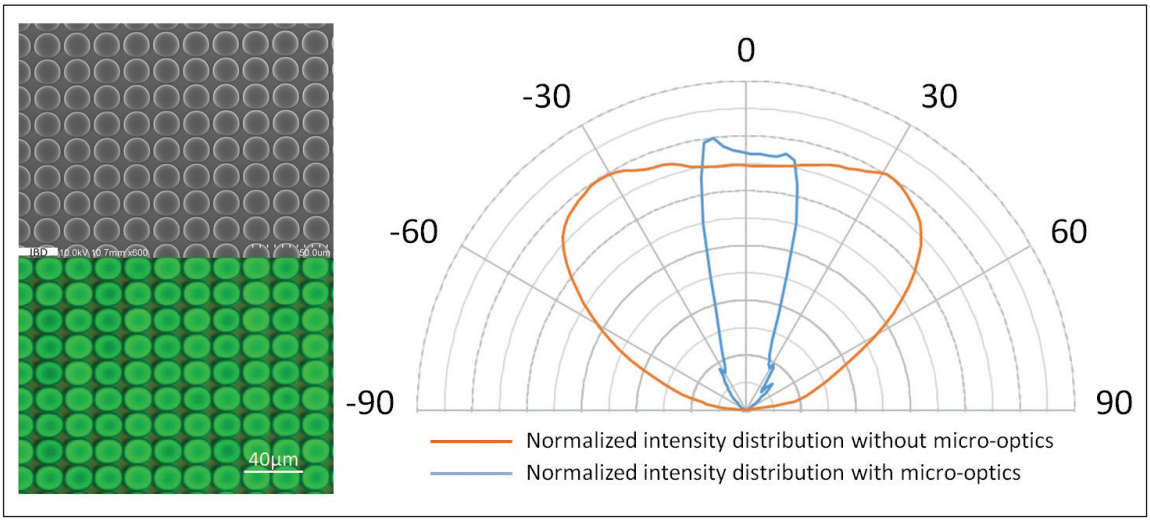


Figure 5. Micro-optics integrated on an active matrix microLED micro-display panel and the measured angular distribution of emission with/without micro-optics.

projection system, so it is wasted. However, with our novel technology, we overcome these issues. That's because our technology does not have a growth substrate covering the microLED arrays. Instead, micro-optic arrays are added on top of the microLED arrays, to reduce the divergence of the emitted light and enhance light projection efficiency.

Using this approach, we have fabricated micro-displays that feature both micro-reflector and micro-lens arrays. These modifications deliver a six-fold increase in brightness in the normal direction, propelling brightness in the green to in excess of 3×10^6 nits (see Figure 5).

… and resolutions

An even larger market for micro-displays – and possibly the biggest of all for this technology – is that of augmented reality. For this application, the requirements for high levels of brightness and contrast, which are needed for outdoor operation under a strong ambient light background, are joined by the need for high resolution. The latter is crucial, because it allows a micro-display panel to achieve a large field of view without compromising the image quality and system compactness.

Our technology is well-suited to meeting these requirements. To showcase its potential for augmented reality, we have produced micro-displays with more than 5,000 pixels per inch (see Figure 6).

We believe that this feat – employing microLEDs with a diameter of just 2 μm, separated by a pixel pitch of 5 μm – sets a new benchmark for high-resolution active matrix microLED micro-displays.

Even higher resolutions should be possible. We believe that the pixel density can exceed 10,000 per inch, through refinements in device design and the fabrication process. When combined with luminance level well above 10^5 nits, this could result in ultra-high resolution active matrix microLED micro-displays that are the most desirable, promising solution for augmented reality.

To make this happen, we will now focus on converting our micro-display prototypes into products, and bringing them to market. While we work on this, we will respond to market demand by continuously pushing the limits of micro-display technology, and dedicating ourselves to the perfection of high-performance microLED micro-displays.

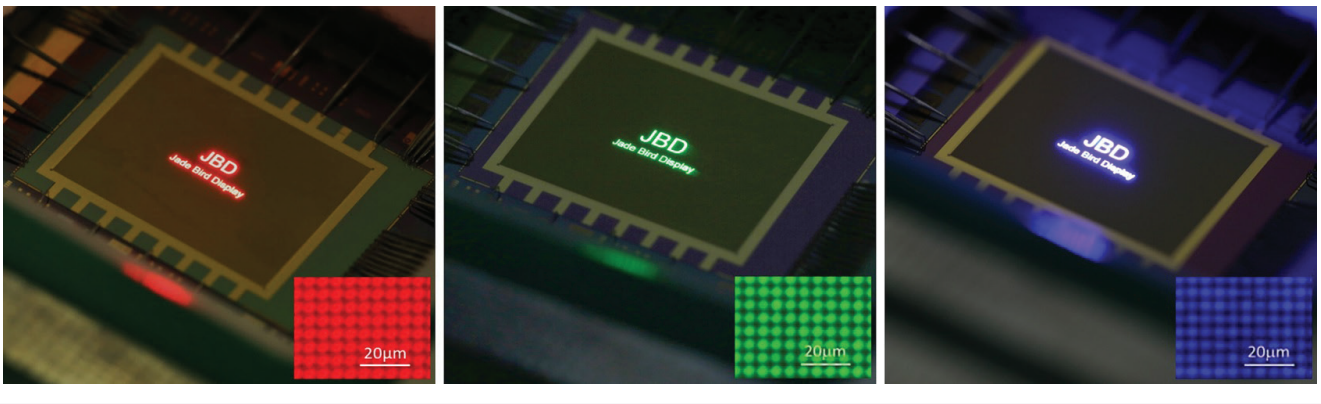


Figure 6. Wafer-level test of active matrix microLED micro-displays with a resolution that is higher than 5,000 pixels per inch.

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CSindustry awards WINNER

CS High-Volume Manufacturing Award

This award recognises success in high-volume manufacture, including the tools delivering high throughput with high yields and milestones in product manufacture

Winner: Beneq Oy

Beneq C2: ALD solution for automated batch wafer equipment for high volume manufacturing

BENEQ C2 is a brand-new Atomic Layer Deposition (ALD) solution for automated batch wafer equipment for high volume manufacturing. It offers a combination of high capacity batch ALD processing and standard cassette-to-cassette automation.

Beneq C2 provides a solution for high performance ALD on wafers in industrial applications, such as optical coatings, insulators and barriers, and high-volume manufacturing of wafer coatings in the semiconductor and MEMS industry. The new product has been designed with special focus on power and RF devices, RF and Piezoelectric MEMS, MEMS sensors and actuators, image sensors, LED and OLED. The thermal batch ALD process of Beneq C2 is ideal for oxide and nitride processes used for dielectric, conductor, barrier and passivation purposes.

The new automated cluster solutions have been designed for industrial ALD applications where high capacity is needed. The number of wafers that can be processes with the new tool is massive compared to traditional ALD equipment. It brings both the speed and operation costs of ALD to a completely new level that makes full-blown wafer ALD production possible. Beneq's high-capacity ALD solutions have enabled completely new innovative products and coatings that have not been possible in industrial scale before. The Beneq C2 ALD equipment has taken deposition speed, capacity and throughput of ALD equipment to a completely new level.

When we talk about ALD throughput in industrial wafer manufacturing, we must consider many different factors of the production setup. There is of course the deposition rate of the actual ALD process in the chamber (in nm/min), but you should also consider the capacity of the chamber (the batch size) and the automation solutions around the ALD equipment. Things like heating the wafers to the process temperature and the cooling time after the processing matter a lot when we count the total throughput. When the target is a thin (for example 10-nanometres) ALD film on a large number of wafers, the wafer handling, heating, cooling, etc. takes much more time than the actual ALD deposition. To increase throughput, one then must optimize all the auxiliary equipment around the ALD tool.

Let's compare for example the effect of pre-heating wafers in a traditional ALD tool that uses batch heating in the reaction chamber to the advanced pre-heating system that we use on the Beneq C2 ALD equipment: A typical case of a temperature sensitive ALD process, such as TiO_2, in batch heating in the ALD tool itself: 25 wafers, loading at room temperature, heated in the ALD reaction chamber – pre-heating time 120 min to reach uniform temperature.

Single wafer heating of Beneq C2: same 25 wafers, pre-heated wafer-by-wafer, 10 s/wafer, total pre-heating time 25 times 10 s = 250 s = 4 minutes and 10 seconds. This combined with the speed of the actual ALD process results in a unique combination of high capacity batch processing and standard cassette-to-cassette automation. Beneq C2 can process up to 20 000 semiconductor wafers per month (10 nm of Al_2O_3 ALD coating on 200 mm wafers).

Editors comment

"With ALD becoming an increasingly common process in the manufacture of compound semiconductor devices, it is reassuring to know that a high-performance, multi-wafer tool from Beneq is meeting chipmaker's needs."

CSindustry awards

WINNER

CS Innovation Award

It is the great ideas of today that can shape the technology of tomorrow. This award celebrates the success of companies that are inventing new types of device, or taking existing devices to breath-taking performance levels

Winner: Veeco

GENxcel R&D MBE System

VEECO has a strong track record of developing award-winning products rooted in pioneering technology. Veeco's GENxcel™ R&D molecular beam epitaxy (MBE) deposition system is the latest demonstration of the company's deep understanding of industry challenges and how to address them through innovative engineering. The GENxcel is designed specifically for compound semiconductor R&D and pilot production markets and produces high quality epitaxial layers on substrates up to 100 mm in diameter for a wide variety of applications and materials including GaAs, InP, nitrides and oxides.

With its inventive architectural concept, the GENxcel system achieves a number of industry firsts. As the first MBE system designed specifically for integrating multiple epitaxial techniques, it has the ability to transfer wafers in-situ from the MBE system to other processes such as Veeco-CNT atomic layer deposition (ALD), providing the opportunity for novel compound semiconductor research. Additionally, it is the first MBE system designed with EtherCAT protocol—improving ease-of-use and reliability while also allowing easier serviceability. All of these features have been incorporated in the system's efficient single frame design that combines all vacuum hardware and on-board electronics to make it up to 40 percent smaller than other 100mm wafer MBE systems, saving valuable laboratory space.

The GENxcel exemplifies Veeco's expertise of designing high performance MBE systems through a system capable of high-quality epitaxial growth on single 100mm substrates. The GENxcel features 12 symmetrical, large capacity effusion cell ports for unmatched process flexibility.

The innovative architectural concept of combining the MBE hardware with the electronics and controls in order to reduce footprint while improving accessibility and serviceability is unique within the MBE industry, making Veeco the only company to develop a 100mm MBE system that is fully integrated into a single platform. Similar MBE systems have the MBE hardware, electronics cabinet and software control computer as three separate components. This design element saves users tens of thousands of dollars in cleanroom laboratory expenses.

First introduced in August 2017, the GENxcel system is invaluable to customers as the compact design saves precious laboratory real estate and saves room for multiple systems. GENxcel's lower upfront capital cost, coupled with reduced ongoing operational costs through reduced liquid nitrogen consumption, improved material utilization and improved overall system reliability sets an entirely new benchmark for industry standards and expectations.

Editors comment

"Researchers need versatile MBE tools that don't take up much room, and are easy to access and service. Veeco is meeting their needs with the GENxcel."

CSindustry awards

WINNER

CS Metrology Award

Measurements of substrates, epi-wafers and devices are essential to manufacturing; needed to unveil problems with processes, ensure high yields and enable the delivery of products complying with specifications. This award recognises specialist measurement services, manufacturers of metrology equipment that either offer a new insight into materials, or set a new benchmark for the time taken for material characterisation

Winner: KLA-Tencor Corporation

Zeta Optical Profiler for Patterned Sapphire Substrate Metrology

WITH rising demand for LED chips for a wide range of applications, including general lighting, backlighting and displays, the use of patterned sapphire substrates (PSS) has climbed in recent years due to the significant increase in light extraction efficiency these wafers afford. Process control challenges for LED manufacturers using PSS wafers such as diffuse surface reflectivity and cone shapes with high slopes require optically efficient metrology with high light throughput.

The Zeta Optical Profiler was designed to solve these challenges. The Zeta Optical Profiler is a fully automated optical profiler for bump height, roughness, etch depth, film thickness and wafer bow applications. Proprietary ZDot™ technology is used for automated macro defect inspection of patterned sapphire substrate (PSS) wafers to find missing PSS structures, bridging, tear out and contamination. Process-critical metrology measurements of the cones, domes and pillars as well as the height, pitch and the diameter of PSS bumps can also be made.

Once defects are detected, the system automatically scans the defects of interest and provides high-resolution images. Multiple broadband white light high-brightness LED light sources enable simultaneous acquisition of surface metrology data and substrate color information. ZDot optical profiling technology overcomes the disadvantages of white light interferometry with a high light throughput optical design that is impervious to vibration and sample tilt – key benefits in working with PSS wafers.

Before the introduction of the Zeta Optical Profiler, PSS size and height measurements were performed using either scanning electron microscope (SEM) or atomic force microscope (AFM) metrology—both slow, inefficient and costly approaches. The Zeta Optical Profiler offers a unique, non-contact, non-destructive, high throughput and low-cost approach. The ZDot optics and unique algorithms provide a complete set of inspection and metrology solutions for both dry-etch and wet-etch PSS. The 100μm^2 inspection area is much larger than the 10μm^2 or smaller area that an AFM or SEM can inspect, allowing users to collect statistical information from hundreds of bumps in one quick scan – typically in less than 30 seconds. By comparison, AFM or SEM can take several minutes to scan one site.

Additionally, the Zeta Optical Profiler can identify process variations down to 20 nm changes in height, a critical parameter for PSS wafer quality.
Since its introduction, the Zeta Optical Profiler has become the tool of record for PSS manufacturers around the world. The low-cost of ownership—due to the absence of consumables such as AFM probe tips—greatly reduces long-term costs for customers, and its speed and non-contact features enable PSS manufacturers to monitor their processes with many more data points and real-time feedback, significantly improving quality control.

Editors comment
"Patterned sapphire is now a key ingredient in the majority of LEDs. It is important to have a tool that can quickly measure all the key properties of these wafers."

Constructing interconnects with **nitride nanowire arrays**

Silicon photonics is held back by the lack of a suitable monolithic light source. The solution: introduce lasers, waveguides and photodetectors that are formed from arrays of nitride nanowires with InGaN disks

BY PALLAB BHATTACHARYA AND ARNAB HAZARI FROM THE UNIVERSITY OF MICHIGAN

THROUGHOUT the twentieth century, engineers improved the performance of the silicon IC by simply reducing the size of the transistors. But in recent times, progress has been far harder to come by. It has hinged on the introduction of exotic materials and architectures to ensure that the miniaturisation of the transistor does not produce dire consequences – and it will not be long before there is a need to add light-based communication, to enable faster transfer of information within and between CMOS chips.

The latter technology, often referred to as silicon photonics, has much promise, because light travels far faster than electrons (see Figure 1 for an example of a simple photonic circuit). Due to this hike in speed, circuits that incorporate photonics can operate at far higher communication rates than their electronic cousins, shortening on-chip and off-chip delays.

Fulfilling the promise of the optically equipped IC is not easy, however. Silicon will undoubtedly remain the material for the electronics, but its indirect bandgap hampers its use in the components needed for optical communication. While impressive progress has been made in research and commercial development of silicon-based detectors, modulators and passive waveguides, III-Vs are the essential ingredient for making a light source.

The current solution is to bond either GaAs-based or InP-based lasers to the silicon wafer. That's not ideal, though, because it creates thermal issues: the silicon gets hot, pegging back laser output and efficiency. A far better approach is the epitaxial growth and fabrication of a diode laser on silicon. Ideally, this source must emit at around 1.3 μm, the zero-dispersion wavelength for the SiO_2 waveguide. Note that another advantage of this spectral range is that it is in the regime of eye-safe operation.

Unfortunately, success with this approach is hampered on three fronts: there is a large lattice mismatch, giving rise to a high density of dislocations; there is a thermal expansion coefficient mismatch that can cause strain in the device; and there is the potential for unwanted antiphase domains, which can be created during the growth due to the polar/non-polar nature of the epitaxial layers and the substrate.

Despite all these drawbacks, encouraging progress has been made by using devices that sport suitable buffer layers. At the University of Michigan, we have led the way, demonstrating the first InAs/GaAs quantum dot laser that is grown directly on silicon. And other groups are now following in our footsteps, improving the performance of this device on (001) silicon substrates.

However, progress is slow, and problems remain. The silicon that's used as a foundation for the lasers is offcut at 4° towards the (011) direction in order to avoid anti-phase domains and resulting defects. Meanwhile, CMOS circuits are formed on (001), a situation that's not going to change. In addition, fabrication of the lasers involves the growth of complicated buffers and intermediate layers, making the whole process cumbersome.

Switching to nitrides

Our view is that instead of trying to address all of these problems, it is far better to switch to another material system. We chose the nitrides, because they combine tremendous tunability of the bandgap with growth on a variety of substrates, such as sapphire, SiC and silicon – including the form that's used for CMOS circuits.

One distinguishing feature of GaN and its related alloys is its large, intrinsic polarisation. The fields that result aid the design of HEMTs, but are a drawback to LEDs, hampering radiative recombination efficiency and limiting the thickness of the quantum well. A further complication is that increasing the indium content of an InGaN well to propel its emission from the blue to the green creates compositional inhomogeneities. This makes it very challenging to produce light sources with acceptable efficiency beyond the blue. And magnifying this issue is the high density of defects, arising from the substantial lattice mismatch with the substrate.

To sidestep these issues, we are avoiding planar III-nitride semiconductors, and instead working with nanowires. Arrays of these nanowires can be grown directly, without masks or catalysts, on various substrates including CMOS-compatible (001) silicon. The density of the nanowires in these self-organized random arrays may range from 10^8 cm^{-2} to 10^{11} cm^{-2}, and their diameter can be between 20 nm and 80 nm (see Figure 2).

Issues related to high polarisation fields are greatly diminished in these wires, thanks to radial relaxation

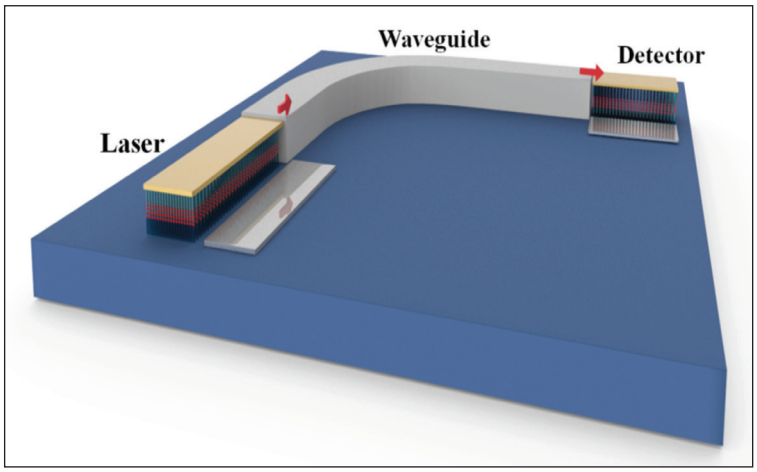

Figure 1. The simplest example of a photonic integrated circuit on a silicon platform. At the University of Michigan, diode lasers and photodiodes are fabricated with III-nitride heterostructure disk-in-nanowire arrays grown directly on silicon by MBE. The waveguide is formed by dielectric deposition.

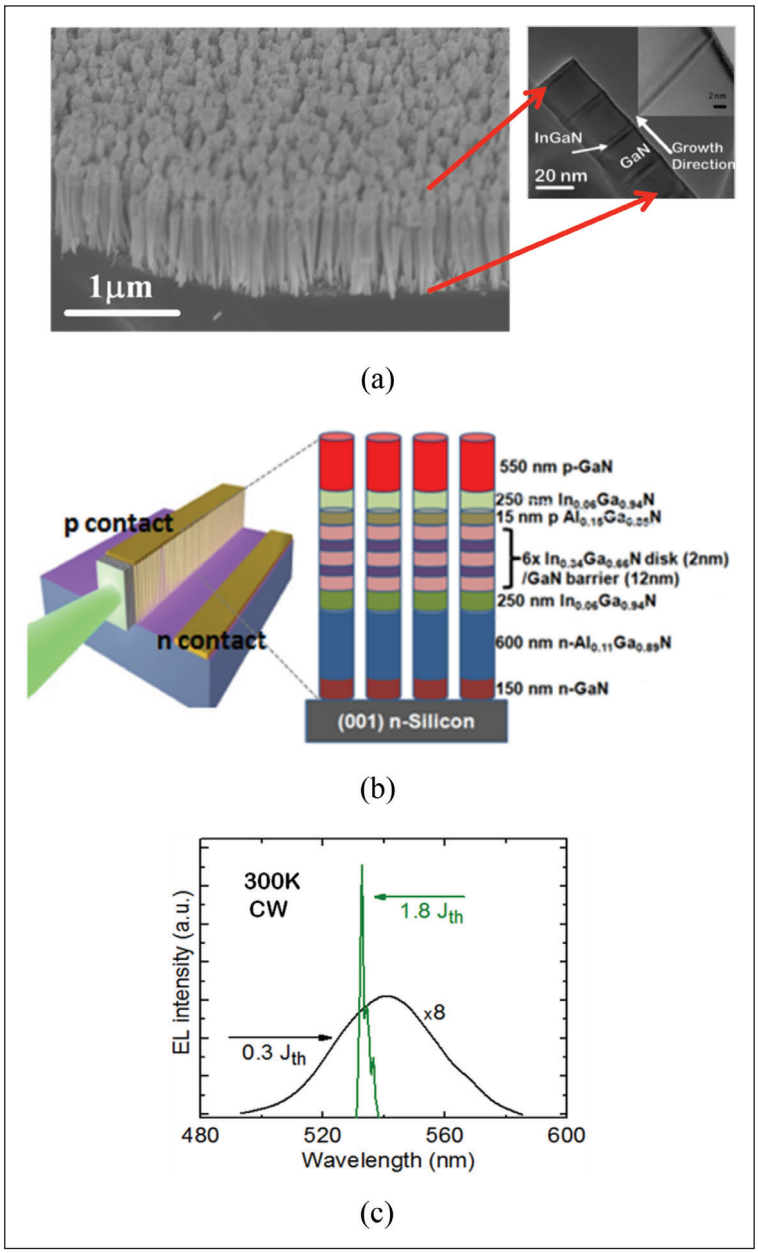

Figure 2. (a) Scanning electron microscopy and high-resolution transmission electron microscopy images of a disk-in-nanowire array on silicon; (b) an illustration of a disk-in-nanowire edge-emitting diode laser; (c) output emission characteristics of a green-emitting laser below and above threshold injection.

of strain during epitaxial growth. The nanowires also suppress extended defects, thanks to the larger surface-to-volume ratio; and emission can span a far wider spectral range through the insertion of lower bandgap disks, such as those made from InGaN, into larger bandgap GaN or AlGaN nanowires. Note that emission from the structure may be tuned by tweaking the composition of single or multiple disks.

Another benefit of the nanowires, which we realised soon after embarking on this effort, is that the indium incorporation in the InGaN disks can be far higher than it is in planar quantum wells, without any adverse effects. And we can realise quantum efficiencies of more than 50 percent.

We have used these disk-in-nanowire arrays to produce green- and red-emitting LEDs – and more importantly, diode lasers for the first time. Note that our edge-emitting nanowire array lasers (see Figure 2) appear exactly like planar devices after fabrication on the (001) silicon substrate. To realise emission in the green and red, the InGaN disks that form the active (gain) media within the GaN waveguide and AlGaN cladding have an indium content of 34 percent for 534 nm emission, and 51 percent for 630 nm emission.

Hallmarks of these emitters include the absence of reflections, scattering and distributed feedback, due to the wavelength associated with the emission being far larger than the diameter of the nanowire (the polymer parylene surrounds the wires, creating a structure that behaves as a composite medium with a refractive index of 2.1). Characteristics associated with photonic crystals are also avoided, due to the randomness of the array.

Typical output powers for these lasers are 10 - 15 mW. The threshold current densities are fairly insensitive to temperature variations (T_o >200K), and have a typical value of about 1 kA cm^{-2}. Electrical modulation indicates that the modulation bandwidths reach 3 GHz without implementing any special designs to the nanowire heterostructures.

Realising the near-infrared

To propel the emission of our lasers from the visible to the near-infrared we have had to crank up the indium content in the InGaN disks. Following careful optimization of the MBE parameters, metal fluxes and growth temperature, we have incorporated multiple $In_{0.85}Ga_{0.15}N$ disks in our GaN nanowires. Encouragingly, these structures produced strong, room-temperature photoluminescence at the desired wavelengths. We are thankful for the assistance of Millunchick's research group at the University of Michigan – they offered an insight into the quality of our nanowires, by undertaking detailed imaging with a transmission electron microscope.

We have fabricated lasers from these heterostructure nanowire wafers at our university's Lurie Nanofabrication Facility. Production of the devices involved a series of steps that included photolithography, etching, metal deposition, planarization and the addition of the polymer parylene. Fabrication is not easy, because rough laser facets that result from dicing the nanowire array/parylene composite reduce reflectivity to such an extent that it prevents the necessary cavity feedback. To overcome this, we smooth the facets with focused ion beam etching. A further enhancement to facet reflectivity comes from the addition of multiple periods of ZnSe and MgF_2, which together form a distributed Bragg reflector. This enables a hike in reflectivity to around

90 percent, and ultimately the fabrication of lasers with an emission peak of 1.2 μm and a room-temperature output of around 7 mW. These first-of-a-kind, near-infrared, III-nitride-based diode lasers are transparent to silicon, thereby making it possible to realize low loss photonic circuits monolithically on silicon.

In these devices, there is a large polarisation field, revealed by the blueshift between the electroluminescence peak below threshold and the coherent lasing peak above threshold. Nonetheless, these fields are far smaller than those in planar quantum wells.

Other encouraging attributes of these lasers are: the absence of any significant material segregation in the active disks; a low threshold current; a high degree of temperature stability of the threshold current (T_0 >200K); a high differential gain; and good modal characteristics.

In our quest to realise a laser emitting at 1.3 μm – the sweet spot for silicon photonics – our only remaining option to red-shift the emission was to attempt to incorporate binary InN disks in the GaN nanowires. This is a far better approach than forming thicker InN regions along wires, because the disks provide quantum confinement, and tend to have a lower dislocation density.

Epitaxial growth of InN disks is far from easy. It is critical to determine the optimum growth temperature, which was an unknown parameter. We were also hampered by the low sticking coefficient of indium. If we selected too high a substrate temperature, this would enhance indium desorption; and if we chose too low a value, the heterostructure would be plagued by poor crystalline quality and defects. Following some optimisation, we selected a substrate temperature of 489°C.

We were delighted to discover that our InN/GaN disk-in-nanowire arrays could produce strong photoluminescence and a high radiative efficiency. The latter is 67 percent, a value exceeding that for ternary InGaN disks of all alloy compositions, before or after passivation with parylene. Photoluminescence intensity peaks at 1.6 μm, an extremely encouraging result.

To improve the performance of our edge-emitters, we adjusted the design, introducing a waveguide

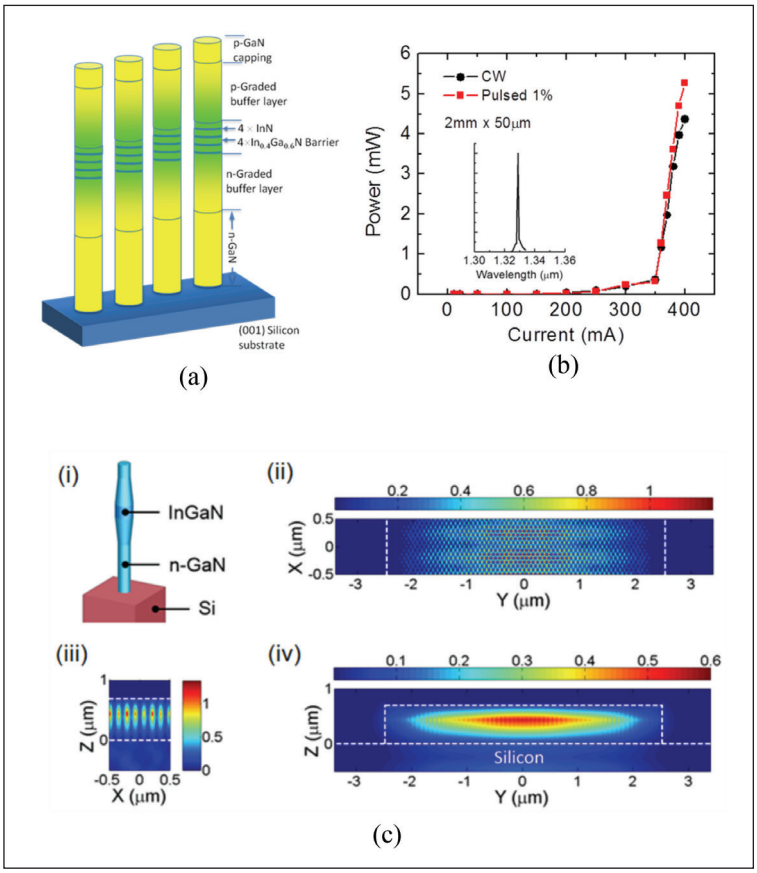

Figure 3. A 1.3 μm disk-in-nanowire array diode laser on (001) silicon. (a) a nanowire heterostructure with InN disks; (b) output light-current characteristics; (c) mode propagation and confinement calculated by the finite-difference time-domain technique.

with a graded refractive index that has various compositions of InGaN. The device that resulted, which has multiple 6 nm-thick InN disks incorporated in the middle of the waveguide region, produces very promising output powers, good modal characteristics, extreme temperature stability (T_0 ~220K) and a large differential gain, all at room temperature (see Figure 3 for details of the output light-current characteristics). With the emission peak at about 1.3 μm, our device is a promising candidate for silicon photonics.

Collaborators have simulated the performance of our lasers. Using the finite-difference time-domain method, Junseok Heo at Ajou University, South Korea, has studied the characteristics of the propagating

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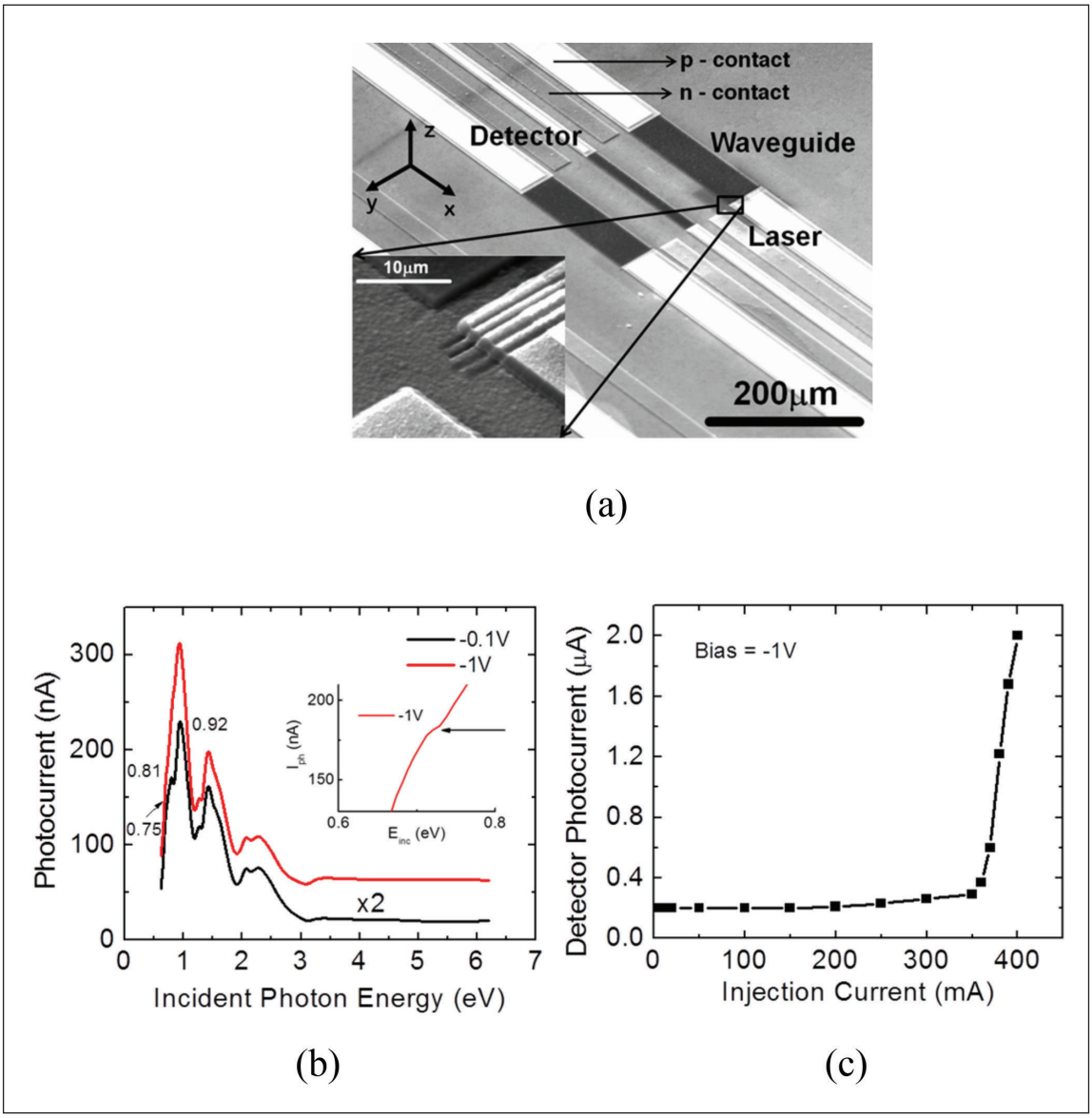


Figure 4. (a) Scanning electron microscopy image of a fabricated nanowire photonic integrated circuit on (001) silicon; (b) photocurrent response of integrated photodiode; response of photodiode to increasing injection current applied to the laser. The peaks and shoulders in the responsivity spectra result from interband transitions in the InN disks and other regions of the nanowire heterostructure.

mode (see Figure 3). Meanwhile, John Dallesasse and his group at the University of Illinois, Urbana-Champaign have calculated the strain distribution and bandstructure in the disks. Both studies have helped us to increase our understanding of the electronic and structural properties of the InN disks and the characteristics of the lasers made with them.

To determine the usefulness of our lasers in communication-based applications, we have undertaken high-speed measurements on these devices. Using small-signal modulation measurements, we have found that our lasers can be modulated at frequencies of up to 3 GHz. This is by no means the limit of their capability: refinements to the design will increase this bandwidth.

Producing photodiodes

Another key component in even the simplest conceivable communication link is the photodetector. Success with our lasers has motivated us to investigate near-infrared guided wave photodiodes fabricated with the same nanowire array. This effort draws heavily on our previous work, because the only difference between the fabrication of our lasers and our photodiodes is that the reflective mirrors on the laser facets are replaced by anti-reflective dielectric coatings, made from SiO_2.

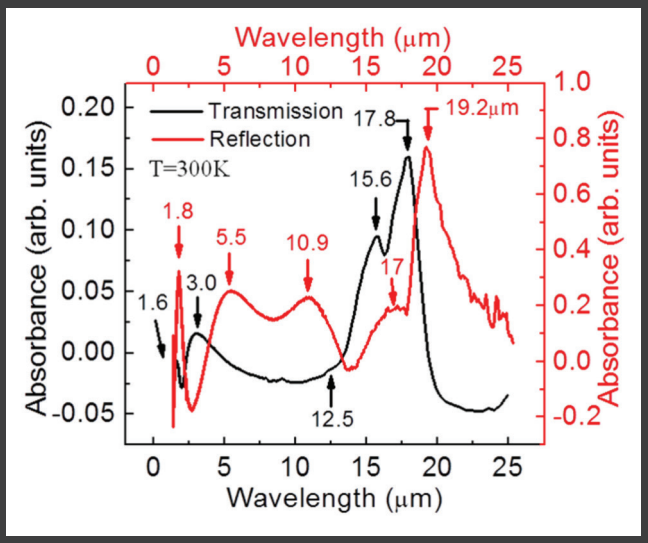
Our photodiodes, which are typically 50 μm-wide and 1 mm-long, have been characterized under reverse bias. Dark currents are a few tens of nanoamperes. Meanwhile, responsivity is 0.1 A/W at 1.3 μm, according to measurements that use spectrally filtered light from a broadband source, directed through a monochromator and collected by a fibre that is focused on a facet of a photodiode (see Figure 4).

Following the fabrication of these devices, we have realized and tested an entire photonic integrated circuit consisting of a laser, photodiode and a waveguide. For the latter component, we have turned

III-Nitrides beyond the near-infrared

Significant research is being undertaken to explore applications of III-nitride materials beyond the near-infrared. The detection of light beyond 1.6 μm is possible by utilizing intersubband electronic transitions, rather than interband transitions. Intersubband transitions have been observed in $In_{0.34}Ga_{0.66}N$/GaN heterostructure nanowire arrays grown epitaxially on (001) silicon.

The polarization field in the InGaN disks is weaker than that in GaN equivalent quantum wells, due to strain relaxation in the nanowires during epitaxy. Consequently, the band bending in the active region is weaker, leading to a larger number of electron and hole bound states. Electronic intersubband transitions take place between these bound electron and hole states during absorption of infrared light in the 3-20 μm spectral range. Measurements of absorption peaks in an array of $In_{0.34}Ga_{0.66}N$/GaN disks-in-nanowires have been made by Alexander Soibel and Sarath Gunapala from the NASA-Jet Propulsion Laboratory (see Figure).



Infra-red absorption has applications in a wide range of fields, including chemical spectroscopy, and terrestrial and extra-terrestrial communication. These applications could be targeted by detectors based on nanowire-based technology that offer significant advantages over the traditional infrared detectors, which unite compound semiconductor based detector arrays and silicon readout integrated circuits with indium-bump bonding. This expensive technology is avoided, as nanowire array infrared detectors are epitaxially grown on silicon. And there is also the promise of room-temperature operation!

to an InN/InGaN/GaN heterostructure disk-in-nanowire arrays, identical to the one used for the fabrication of the 1.3 μm laser and photodiode (see Figure 3). Again, growth was by MBE, on a (001) silicon substrate.

To fabricate the photonic integrated circuit, we used process steps that are identical to those employed for the two active devices. However, we used an extra dielectric deposition step to form a multi-layer Si_3N_4/SiO_2 waveguide between the laser and the detector. Waveguide deposition parameters were optimized to minimize waveguide loss, measured in identical control waveguides. To improve the quality of the communication link, we deposited a ZnSe/MgF_2 multi-layer distributed Bragg reflector (DBR) on the laser facet that is away from the waveguide, and added a SiO_2 anti-reflective coating on the detector facet away from the waveguide.

Further improvements resulted from the introduction of a reflective coupling facet of the laser to the waveguide. To accomplish this, air/semiconductor (nanowire-parylene) DBR mirrors were defined by focused ion-beam etching. Just four periods of this DBR can provide sufficient reflectivity for successful laser operation and waveguide coupling.

To test the complete optical link (see scanning electron micrograph image in Figure 4), we gradually increased the bias to the laser and measured the photocurrent of the detector. As we had hoped, the photocurrent behaviour is identical to that of the light-current characteristics of the laser, confirming that light from the laser couples to the detector via the waveguide. The input power to the photodiode, for the maximum measured photocurrent of about 2 μA, is estimated to be 20 μW.

Our results demonstrate that an optical communication link can be formed on a (001) silicon substrate, the platform for all CMOS circuitry, from monolithic integration of an epitaxially grown 1.3 μm laser, photodetector and waveguide. The next steps in the development of this technology may include the introduction of a light modulator, as well as laser and detector biasing circuits based on silicon transistors. While the primary application for our technology is optical communication on silicon chips, it could also serve in future optoelectronic and biomedical applications.

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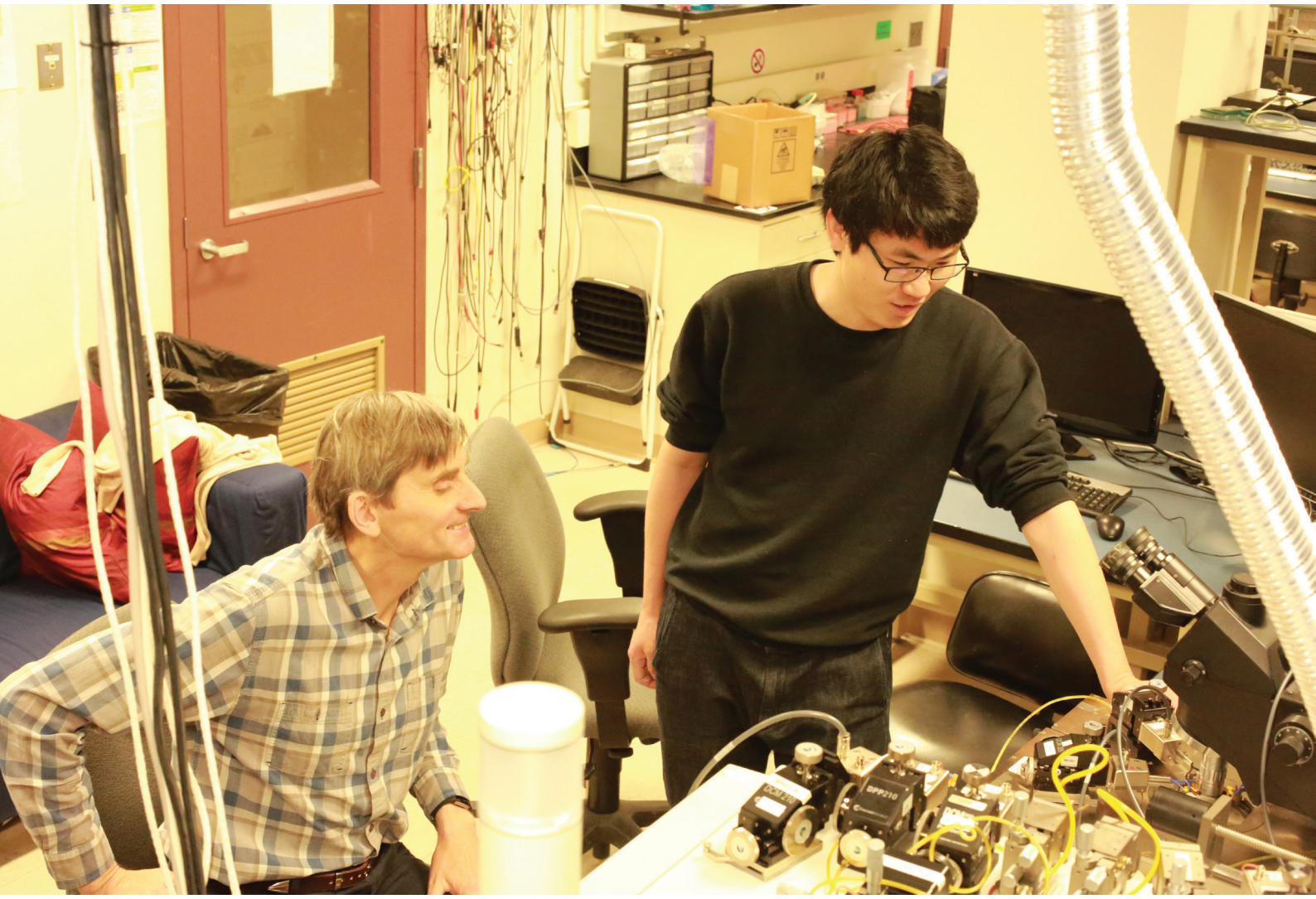

Shrinking the vertical **nanowire MOSFET**

Silicon transistors are tipped to offer diminishing returns at the 7 nm CMOS node and beyond. Can InGaAs vertical nanowire MOSFETs step in and maintain the march of Moore's Law?

BY XIN ZHAO, WENJIE LU, ALON VARDI AND JESÚS A. DEL ALAMO FROM MASSACHUSETTS INSTITUTE OF TECHNOLOGY

THE SILICON MOSFET is fulfilling the moto 'smaller is better'. Continuous reductions to its size for five decades have enabled it to keep pace with Moore's Law, while underpinning a microelectronics revolution that has transformed virtually every aspect of human life.

But scaling can't go on forever. As the transistor shrinks into the nanometre regime, smaller is not always better. Simply reducing dimensions even further will cause severe short-channel effects to will escalate, impairing device performance. To overcome this issue, the silicon IC industry has switched from planar device geometry to a FinFET structure (see Figure 1). The new architecture, introduced at the 22 nm mode, has a conducting channel residing in a thin fin of semiconductor, which sticks out of the wafer surface. This design provides a high degree of electrostatic control, enabling the scaling of the gate length to very small dimensions. Today, the width of this fin in state-of-the-art FinFETs can be as narrow as 7 nm – and from here on, it will be a grand challenge to keep shrinking lateral dimensions, so more devices can be packed in a given footprint.

A characteristic shared by planar MOSFETs and FinFETs is that current flows parallel to the wafer surface. In contrast, in the power electronics industry, engineers manufacture vertical structures, with current flow perpendicular to the wafer.

One key advantage of the vertical geometry is that it decouples aggressive footprint scaling from gate length and contact length scaling. Thanks to this, the footprint can be trimmed again and again without giving rise to short channel effects.

Immunity to short channel effects is particularly prevalent in nanowire transistors, a class of device that sports a unique gate-all-around geometry.

The vertical nanowire transistor has the potential to propel Moore's law further into the future than any other device structure.

Impeccable InGaAs

Many groups have already made vertical nanowire MOSFETs that are based on silicon. But unlike their planar counterparts, the performance is rather unimpressive. Carrier mobility in silicon is not that high, so it is common practice to increase this by introducing strain into the device. But for the vertical nanowire MOSFET, no efficient methods exist for strain engineering the channel.

Far more promising is the family of III-V compound semiconductors, which has attracted considerable interest to advance logic CMOS. The jewel in the crown is InGaAs, which has an outstanding electron velocity. This ternary has held the key to fabricating record-breaking HEMTs and HBTs. In addition, InGaAs is a perfect candidate for the channel material in vertical transistors. At MIT we are using it in that manner, and breaking new ground by scaling the vertical nanowire MOSFET to far smaller dimensions than our peers.

By adjusting its composition, InGaAs can cover a wide range of lattice constants, effective masses and bandgaps, allowing its electrical properties to be fine-tuned. What's more, when InGaAs is paired with other III-Vs, such as InAlAs and InP, this enables flexible, powerful bandgap and strain engineering.

Note that the vertical channel configuration is a perfect fit for III-Vs, because carrier flow takes place in the direction of epitaxial growth. This opens up, for the first time, the possibility of band structure engineering along the carrier transport direction, expanding device design opportunities – they can include leakage current reduction, through bandgap engineering of the drain and source; and strain engineering, to boost both the carrier density and the velocity.

Interest in III-Vs goes beyond its high speed advantage. When III-Vs are integrated with silicon, systems can be produced that combine logic, terahertz sensing, imaging and communication,

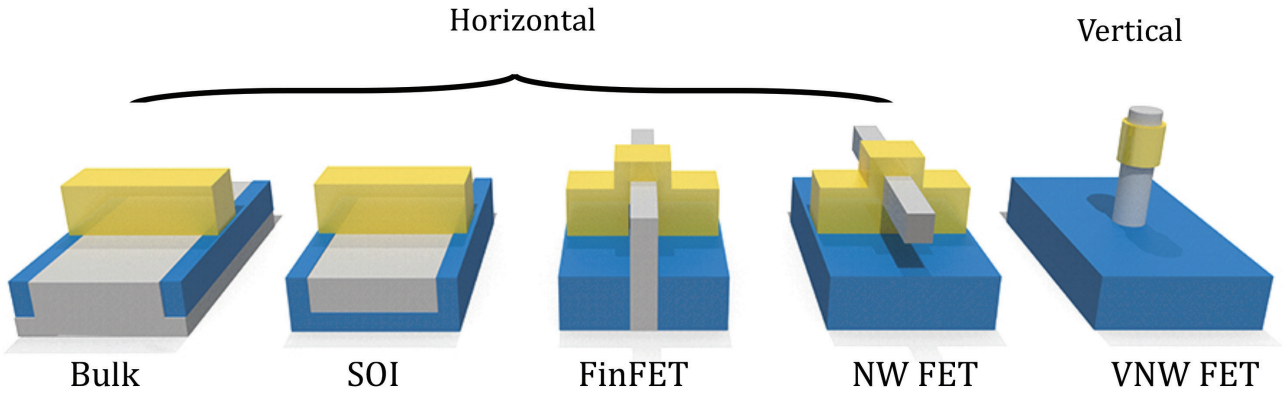

Figure 1. The evolution of logic transistor architecture, from a planar device to a vertical nanowire MOSFET (note that SOI is short for silicon on insulator).

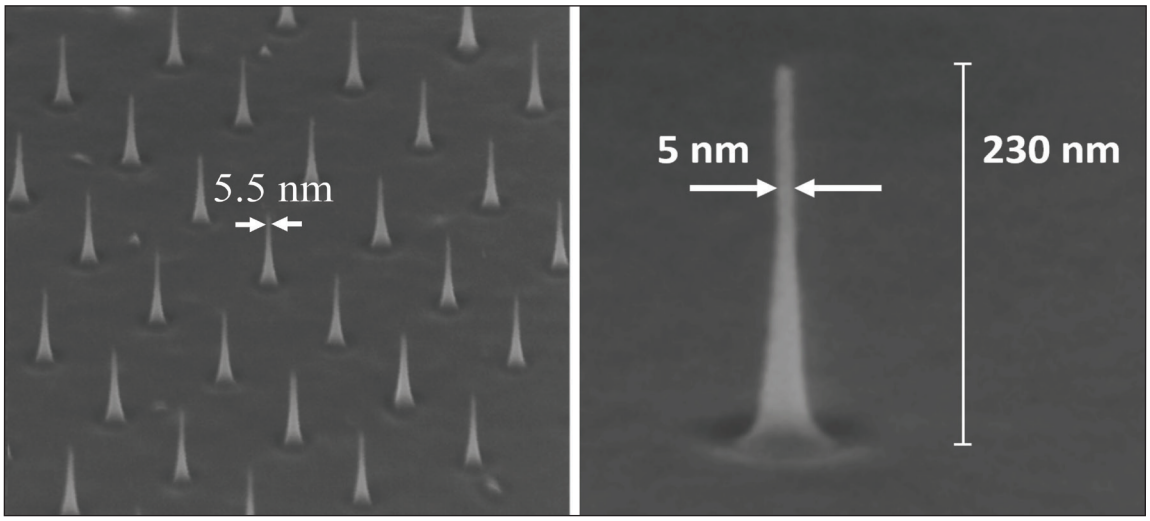

Figure 2. Scanning electron microscopy images of an InGaAs vertical nanowire array (left) after seven digital etch cycles in 10 percent H_2SO_4 in methanol. The 5.5 nm diameter nanowire yield is 90 percent. On the right is an exemplary single InGaAs vertical nanowire with a diameter of 5 nm and aspect ratio of over 20.

as well as optical functions, opening the door to numerous novel applications.

Armed with its excellent set of attributes, InGaAs has recently been used to demonstrate planar MOSFETs and FinFETs with impressive characteristics. Fabrication has drawn on: the development of highly scaled metal-oxide-semiconductor gate stacks, which have excellent interfacial characteristics; ohmic contacts with a low contact resistance; and very tight, self-aligned designs. One of the upshots of these efforts is that they have laid a solid foundation for advancing InGaAs vertical nanowire MOSFETs.

Shrinking InGaAs nanowires

The performance of the vertical nanowire MOSFET is governed by the quality of the nanowire. At the point of insertion into the CMOS roadmap, vertical nanowire transistors must have a vertical nanowire with a diameter of less than 10 nm, as well as vertical, smooth sidewalls.

Given these requirements, it is of no surprise that the formation of the nanowires is a critical issue. One option is the bottom-up approach, which involves the growth of compound semiconductor heterostructures, using either catalyst nanoparticles or patterned oxide masks as a template. This approach, which minimizes threading dislocations via two-dimensional confinement, is attractive because it enables the relatively straightforward integration of III-Vs on a silicon wafer. Note that engineers adopting the bottom-up approach have several options, including the vapour-liquid-solid method, selective-area epitaxy and template-assisted growth.

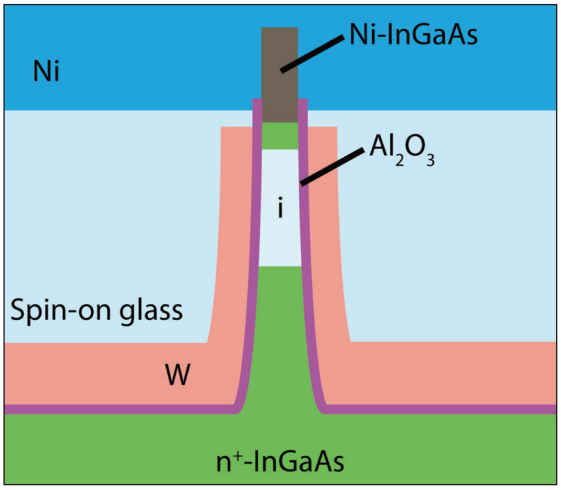

Figure 3. MIT's InGaAs vertical nanowire MOSFETs features an Al_2O_3 dielectric and a nickel-InGaAs top contact.

Approaching the challenge from the opposite direction is the family of top-down techniques. Here, the key technology is reactive ion etching, an industry-standard process that creates high-aspect ratio structures, thanks to its high degree of directionality.

Prior to our work, top-down techniques could only define micrometre-scale structures in InGaAs.We have smashed through this barrier, using a combination BCl_3, $SiCl_4$ and argon to etch nanowires with diameters as thin as 15 nm and aspect ratios in excess of 15.

A key breakthrough associated with our work is the use of a 'digital etch', which provides precise trimming of the nanowire diameter and smoothing of the sidewalls through a highly controlled, self-limiting chemical process. Additional merits of this process are the preservation of nanowire shape and an improvement to the electrical quality of the sidewalls.

We have discovered that it is of paramount importance to select an appropriate solvent for the acid that is used in the digital etch process during the oxide removal step. Using water allows precision dimension engineering, as well as successful mitigation of surface damage that is introduced during a dry etch. However, a water-based approach also leads to the destruction of vertical nanowires when their diameter is 10 nm or less. This is caused by the high surface tension of the water-based acid.

For our work, alcohol is a better option. Making the

switch greatly improves the mechanical yield for nanowires with diameters below 10 nm. By turning to 10 percent H_2SO_4:methanol, we can use digital etching to produce a yield of 90 percent for nanowires with 5.5 nm diameter (see Figure 2). Close inspection of nanowires within this array reveals that we have produced structures with a 5 nm diameter and aspect ratio over 20. To our knowledge, this sets a new benchmark for miniaturization of the InGaAs vertical nanowire. Note that there is a vertical sidewall towards the top of the nanowire, where active device layers are present.

One of the big challenges with vertical nanowire transistors with diameters below 10 nm is the addition of electrical contacts. For non-alloyed contact metals, such as molybdenum and tungsten, full depletion under the contact can only be avoided by using a mushroom-shaped top contact region – and this creates a wider nanowire tip. A top-heavy structure results, which is mechanically fragile, adding considerably to process complexity. To address this, we use nickel-alloyed contacts. Nickle reacts with InGaAs to form a highly conducting NiInGaAs metallic phase.

Record performance

Our vertical nanowire MOSFETs are made out of InGaAs, and consist of an intrinsic channel region sandwiched between two n^+ contacts (see Figure 3). The gate stack includes high-κ dielectric Al_2O_3, deposited via atomic-layer-deposition, onto which tungsten is sputtered. To provide isolation between drain, gate and source electrodes, two steps of planarization and etch back are undertaken using spin-on glass, before nickel is sputtered as the top contact metal. Fabrication is completed with a forming gas anneal at 200 °C, to drive a reaction between nickel and InGaAs that forms a top contact. In addition, this final step improves the interface between the oxide and the semiconductor.

Electrical measurements on a typical vertical nanowire MOSFET, which has a diameter of 7 nm, reveal an on-off ratio close to 10^5 at a drain-source voltage of 0.5 V. A record peak transconductance of 1.7 mS/μm at an on-resistance of 1100 Ω μm is obtained, highlighting the strength of this device to achieve high-performance computing. The minimum linear sub-threshold swing, measured at 0.05 V, is 85 mV/decade, while the saturated sub-threshold swing, measured at 0.5 V, is 90 mV/decade. These values indicate reasonable sidewall and interface quality. A drain-induced barrier lowering of 222 mV/V is observed.

The output characteristics for this 7 nm-diameter device do not show current saturation. This indicates that the top contact is still slightly Schottky in nature, and that it absorbs a significant fraction of the drain-source voltage. In contrast, when the dimeter is 15 nm, there is good current saturation in the output characteristics (see the bottom row of Figure 4). Note

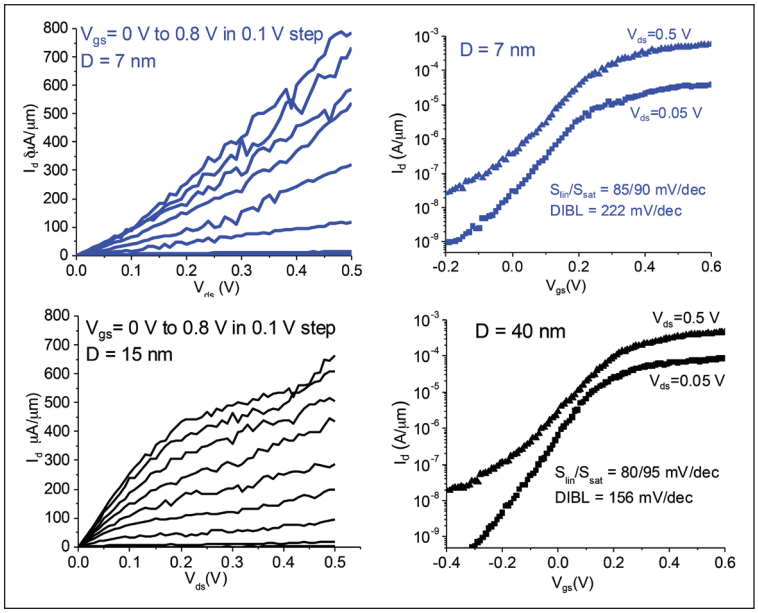

Figure 4. Subthreshold and output characteristics of InGaAs vertical nanowire MOSFETs with nickel contacts and diameters of 7 nm (upper row) and 15 nm (bottom row). All figures of merit are normalized by the nanowire periphery.

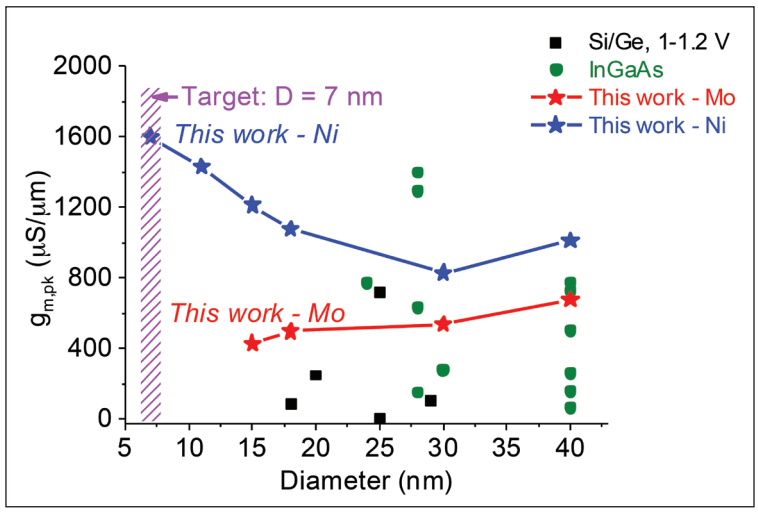

Figure 5. Judged in terms of a peak transconductance at a drain-source voltage of 0.5 V, MIT's vertical nanowire MOSFET compares well to silicon and germanium variants. The work at MIT is ground-breaking on two fronts: it demonstrates the first sub-10 nm diameter vertical nanowire transistors, and the devices deliver record performance. Note that the labels 'Ni' and 'Mo' refer to nickel and molybdenum, the metals used in the top contacts of MIT's vertical nanowire MOSFETs.

that we obtain a lower transconductance of 1.1 mS/μm in this wider device.

We have found that the final annealing step has a profound effect on the electrical characteristics of our devices – especially when they have small diameters. For nanowire MOSFETs with a 7 nm diameter, the absence of annealing leads to a reduction in the on-current by five orders of magnitude, as well as an absence of gate control.

An important figure of merit for benchmarking our transistors against the state-of-the-art is the transconductance. We have undertaken this exercise, considering the peak transconductance of vertical nanowire MOSFETs made from silicon, germanium and III-V materials, and found that our devices produce a very competitive performance, judged against that of silicon and germanium cousins. All devices are rather immature, underlying the potential of the III-V vertical nanowire MOSFET.

It is worth noting that until we announced our recent results, the narrowest silicon vertical nanowire MOSFETs presented in the literature had a diameter of 18 nm, while this figure for InGaAs devices stood at 23 nm. Both these devices are far larger than the target dimension of 7 nm, while our transistors, made with an alcohol-based digital etch, have entered the territory that is relevant for future ultra-scale logic applications.

What is particularly encouraging is that the performance of our nickel-contacted devices continues to improve as their diameter shrinks, with a record transconductance realised for a 7 nm diameter. We attribute this improvement with scaling to a combination of factors, which include volume inversion and a shorter effective channel length, due to enhanced nickel diffusion in narrow devices.

In sharp contrast, devices that are identical, apart from the contact being made of molybdenum rather than nickel, have a performance that degrades as the diameter shrinks (see Figure 5). This stems from increases in the top contact resistance as the contact area is reduced. So great is this problem that if the diameter of the nanowire is reduced to below 15 nm, the device ceases to exhibit transistor characteristics.

We will now build on our success, having demonstrated the smallest vertical nanowire transistor ever made on any kind of material system. Our goals for the future include even higher performance, improved current saturation, reduction of leakage and better reliability. Success in these areas could allow the introduction of III-Vs into logic, and ultimately enable a continuation of the march of Moore's Law.

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Growing III-V on glass

A textured film of MgO promises to enable the growth of III-V devices on large glass sheets

By ASHOK CHAUDHARI FROM SOLAR-TECTIC

IS SILICON a superior substrate to sapphire for making GaN-based LEDs? Well, some companies certainly think so. Take Plessey Semiconductors of the UK: it has argued that silicon has the upper hand not only in cost, but also in thermal attributes. Meanwhile, Samsung of South Korea claims that cost savings could be as high as 60 percent, by combining 200 mm GaN-on-silicon epiwafers with wafer-level, chip-scale packaging. That's a view shared by Allos of Germany, which thinks that these cost savings could eventually be even more substantial, as the process matures.

At Solar-Tectic LCC of Briarcliff Manor, NY, we applaud the move away from costly sapphire wafers. But we think it's possible to go even further, and make even greater savings. Our idea is that instead of using a silicon wafer, GaN can be grown on a thin film of silicon or germanium. So production then involves taking a cheap substrate, such as soda-lime glass, and depositing on this a thin film of silicon (or germanium), and following it up with the growth of a GaN LED heterostructure. As well as slashing substrate costs, this approach could deliver another key advantage for the manufacture of microLEDs: the devices could be made monolithically, without the transfer of pixels, since GaN can be grown directly on the silicon film.

We expect that our approach will arouse some skepticism within the compound semiconductor community, which sees high-quality heterostructures as the bedrock for successful devices. It is clear that with our approach, a polycrystalline film of silicon is not acceptable. But how much better does it need to be? If it is not exactly single crystal, but close, is that good enough?

There are those in the materials community that have been wrangling with these questions for decades. Through their efforts, they have realised that the silicon film must have a 'preferential orientation' or a 'texture'. One way to accomplish this is to produce a thin buffer layer on a highly textured surface

of glass. By adopting this approach, texture or orientation can be introduced in the silicon film. This holds the key to creating a textured silicon film that would be close enough to a single crystal silicon wafer in quality that device performance would be equal. On this film, oriented III-V materials for LEDs could then be grown heteroepitaxially.

We accept that there is a compromise with this approach: the removal of the thermal advantage associated with silicon, which has a much higher conductivity than soda-lime glass. However, that's not a big issue for the display industry, because the manufacture of displays often involves a processing step that deposits crystalline silicon thin-film on buffered glass, known as low temperature polysilicon (LTPS). Alternatively, an amorphous (a-Si:H) silicon thin-film is deposited by plasma-assisted CVD. The latter is the most common method used today.

Outweighing this minor drawback, the inferior thermal conductivity, there is virtually no limit to substrate size with our crystalline silicon thin-film approach. It is only the reactor that limits the dimensions of the substrate. What's more, the process for depositing the thin-film of silicon is much cheaper than MOCVD; and as the approach is monolithic, all the supply chain elements can be brought together: LEDs, thin-film transistor backplanes, and chip transfer (pick and place is not used).

Growth issues

It is well known that it is not easy to grow high-quality GaN epilayers on a silicon substrate. This pair of materials has a significant lattice mismatch, and thermal expansion coefficients differ by nearly 50 percent. These differences give rise to crystalline defects, such as dislocations and cracks, that impair efficiency and reliability – and ultimately lead to low yield and increased cost.

When GaN is grown on a thin film of silicon, these problems are less of an issue, because there is less strain. This reduces the dislocation density, minimises wafer cracking, and alleviates or eliminates the need for AlN or AlGaN buffer layers.

A thin film also introduces more freedom into the design. For example, there is the possibility to switch from silicon to germanium, which has a lattice parameter that is almost a perfect match for GaAs. Note that with either thin-film, it is possible that the density of defects in the GaN is less than it would be for materials grown on a silicon substrate. And with our approach, it is possible to control the smoothness of the film, by selecting its thickness with nanometre precision.

Our efforts at developing thin films on glass began several years ago when we were developing a process to cut the cost of photovoltaics. At the time, we were working with textured buffer layers of Al_2O_3 (sapphire) and MgO, and our efforts led to the first ever (111) *c*-axis oriented thin-film insulator on soda-lime glass. This was a key milestone, as this orientation can greatly improve the electronic performance of a material.

Other groups have also produced textured films. However, they used ion-beam-assisted deposition, which is much more expensive than our patented approach: electron beam evaporation.

The initial films of MgO were far better than we had hoped for. We expected to see a single peak in the X-ray diffraction scan, to indicate high texture. But we also found a second peak. This parallel peak of (111), namely (222), revealed growth of MgO (111) with almost perfect crystalline (111) alignment along the *c*-axis.

Since then, we have scrutinised our films with the likes of transmission electron microscopy (see Figures 1 and 2), electron backscattered diffraction (see Figure 3), optical transparency (see Figure 4), and adhesion tests. Together, these techniques revealed that the MgO has high texture, complete transparency and good adhesion to the soda-lime glass. Its only inferiority to MgO formed by ion-beam-assisted deposition is that the more expensive process produces films with a bi-axial orientation. This gives the subsequent layers a biaxial texture, and an even better crystalline quality than the ones that we grow

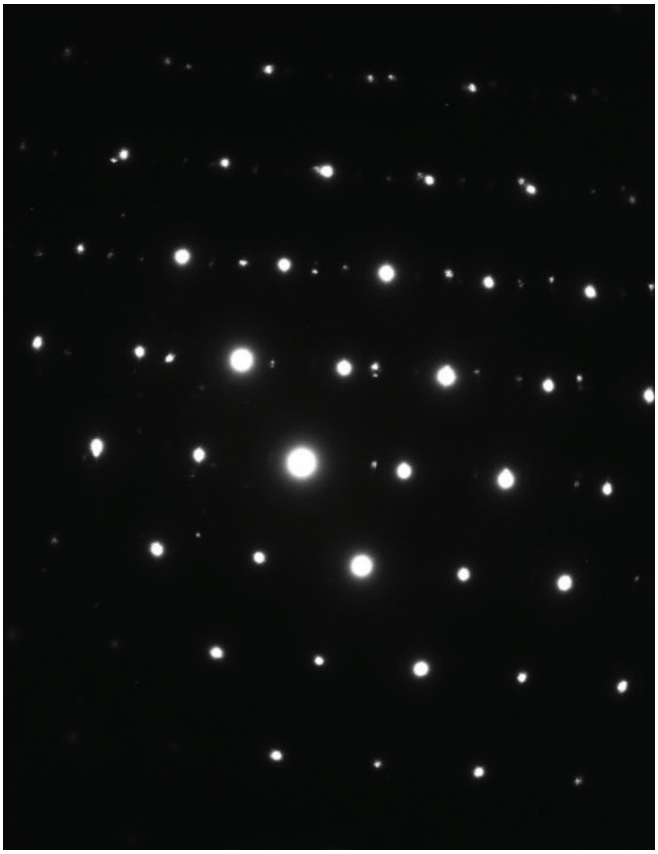

Figure 1. Transmission electron microscopy of 7 μm MgO film on soda-lime glass grown at 450°C showing aligned atoms which are indicative of texture.

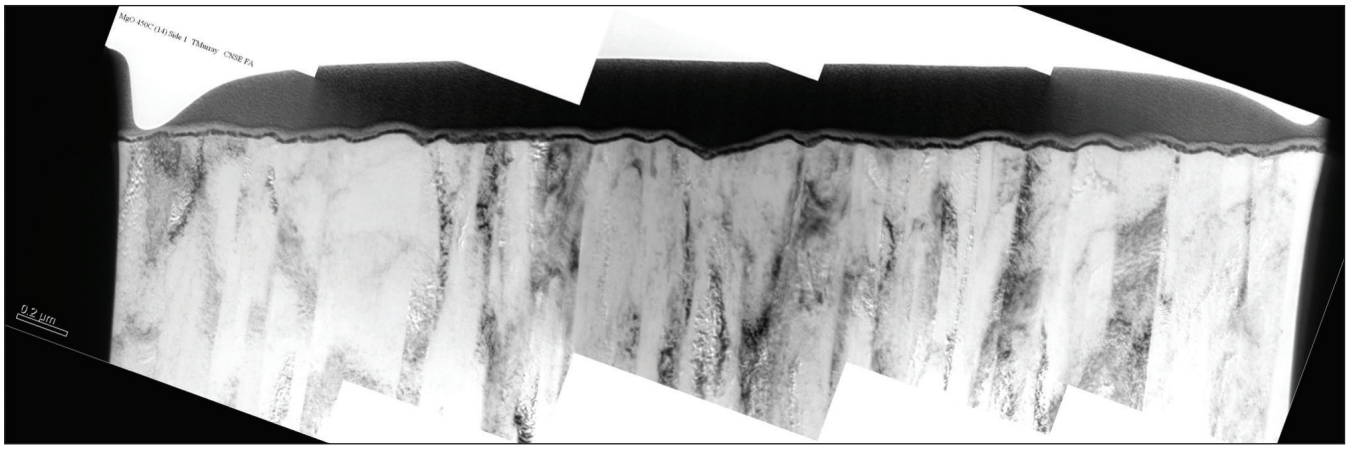

Figure 2. Transmission electron microscopy cross-section of the MgO (111) film on soda-lime glass at 450 °C.

by electron-beam evaporation.

When developing photovoltaics, we have found that electron-beam evaporation can form a buffer layer with texture that is preferably (111) oriented. This is highly desirable, because it could lead to the growth of textured silicon or germanium films that boost efficiency. We have also observed that if aluminium is added during the low-temperature crystalline growth, the film that's formed is *p*-type, and can serve as the bottom conducting layer in a *p-n* junction.

Within such a structure, an insulating MgO layer can act as a diffusion layer and texture promoter for the aluminium-silicon thin-film. It is also possible to grow silicon single crystal nanowires on the MgO. Note that aligning these nanowires perpendicular to the substrate is aided by the (111) orientation of the film since nanowires are grown in the (111) direction.

The MgO that we grow has parallels with c-axis aligned, crystalline indium gallium zinc oxide, the growth of which has been pioneered by Shunpei Yamazaki's group at the Semiconductor Energy Laboratory, Japan. Like our MgO, indium gallium zinc oxide is textured out-of-plane, but not in-plane – that is, the crystals are aligned along the *c*-axis but not the *a-b* axis. However, indium gallium zinc oxide differs from our MgO, because it is not polycrystalline along the *a-b* axis. There is also another crucial difference: indium gallium zinc oxide is a semiconductor, while MgO is an insulator. So, in the display industry, MgO could serve as an insulating layer in the thin-film transistors used in displays, while indium gallium zinc oxide can form the channel of this device.

We are very excited by this opportunity. The display industry currently uses two kinds of insulator materials: SiO_2 and SiN_x. Neither are crystalline, let alone textured. Switching to our material would be revolutionary. It would open the door to textured silicon films that promise far higher electron mobilities, thanks to the lower angles of the grain boundaries.

Note that this is the first ever report of an insulating film grown with a (111) orientation. Back in 2005, a team at the National Renewable Energy Laboratory adopted a similar approach, but produced CeO_2 (100), textured bi-axially.

Another breakthrough of ours is the annealing of the silicon film by an excimer laser. This is not trivial – it creates the possibility of being able to grow a highly oriented silicon thin-film channel by excimer laser annealing in a new, modified, low-temperature polysilicon process.

In the scheme, the layer of MgO (111) not only induces (111) ordered grains in the silicon film, but also protects the glass substrate from the heat generated by the annealing process. The upshot is that it allows the use of cheap soda-lime glass.

When gallium forms on the silicon layer, after diffusing to the surface of the gallium-silicon eutectic alloy, nitrogen can be introduced to the gallium to form GaN by carefully selecting the precursors. GaN forms on the highly crystalline film (or if indium and a phosphor precursor are chosen, then it is InP).

This promise has caught the eye of a major display company. They are testing our technology, and are highly encouraged by preliminary results of laser annealing of a 50 nm-thick film of a-Si:H on textured MgO (111)/soda-lime glass.

Growing III-Vs

Earlier this year, we received a patent for the growth of III-Vs on thin films of silicon on textured MgO. This process exploits the formation of a eutectic alloy consisting of III-Vs, such as gallium, combined with either silicon or germanium, deposited by either electron-beam evaporation or sputtering.

When gallium forms on the silicon layer, after diffusing to the surface of the gallium-silicon eutectic alloy, nitrogen can be introduced to the gallium to form GaN by carefully selecting the precursors. GaN forms on the highly crystalline film (or if indium and a phosphor precursor are chosen, then it is InP). It is probably not possible to form GaN at a low temperature. However, thanks to the very high melting point of MgO – it is over 2800 °C – the deposition temperature can be increased significantly when a suitable glass substrate is chosen (perhaps Lotus NXT).

This approach does not lend itself to subsequent laser lift off. However, that's not necessarily an impediment, because the very thin layers of both silicon and GaN could have advantages, depending on the device needed.

If our technology is used to make LEDs, this would allow these devices to be fully integrated – there is no need to transfer them elsewhere. All the materials would be grown directly on the glass substrate. As the underlying silicon thin-film is textured, the silicon channel mobility could potentially approach that of a single-crystal CMOS thin-film transistor, and the final screen

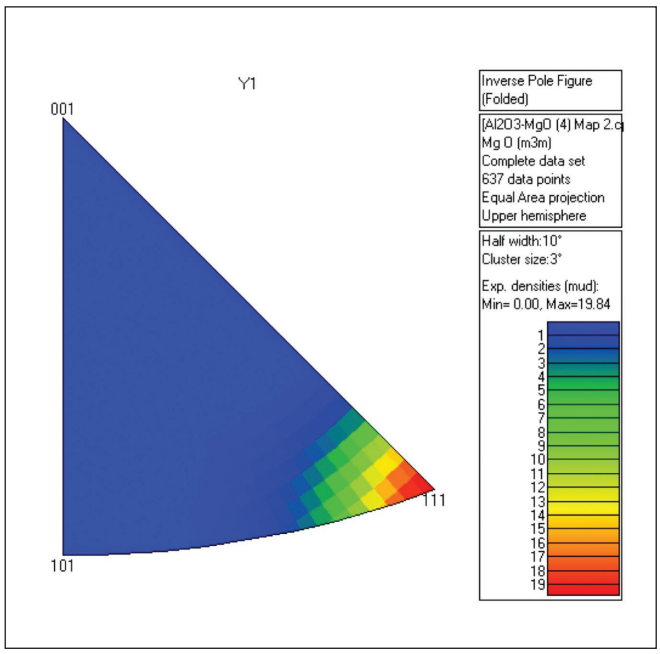

Figure 3: Electron Backscatter Diffraction (EBSD) of 7 μm MgO film on soda-lime glass at 450°C. The image clearly shows that the grains (crystals) of the film are highly oriented along the (111) plane.

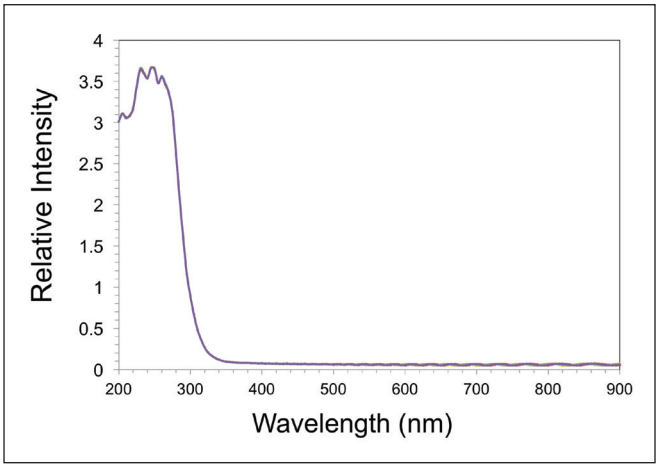

Figure 4: MgO has high transparency across a wide spectral range. Transmission measurements were also taken and are estimated to be 89 percent.

size could be less than 1 inch (due to the tighter integration). This approach could potentially also be applied to 5G wireless technology where GaN-on-silicon is already being explored with great interest.

Encouraging, we have just reported a mobility of 188 $cm^2 V^{-1} s^{-1}$ in silicon films made from a eutectic alloy. This result is with a polycrystalline MgO film, and we are convinced that an even higher value is possible with a textured buffer layer.

Another encouraging result is the growth of Al_2O_3 (111) on MgO (111)/glass, using a temperature above 600 °C. In principle, GaN could be grown on the Al_2O_3 (111), thereby providing another alternative to the sapphire wafer.

There is no doubt that there is much to like about replacing wafers of silicon and sapphire with crystalline thin-films made from silicon or germanium. This could trim the costs associated with the production of LEDs, and in particular, microLEDs. However, while much progress has been made, there is still more work to do.

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Improving ultraviolet LEDs with ITO

Purging with a tin-based metal organic increases the transmittance of ITO, and lowers the operating voltage of the LEDs that employ this oxide

THE COST of ultraviolet LED is compromised by complex device processing, such as flip-chip packaging or substrate lift-off, that is needed to address the low hole density of *p*-type AlGaN. But the problems with *p*-type GaN can be overcome by introducing an MOCVD-grown, transparent electrode of ITO, according to a team from Sun Yat-Sen University, China.

"We believe that our MOCVD-ITO technology can achieve high transmittance in the UVA and UVB range and make the fabrication of UV optoelectronic devices cheap and easy," remarks team spokesperson Gang Wang.

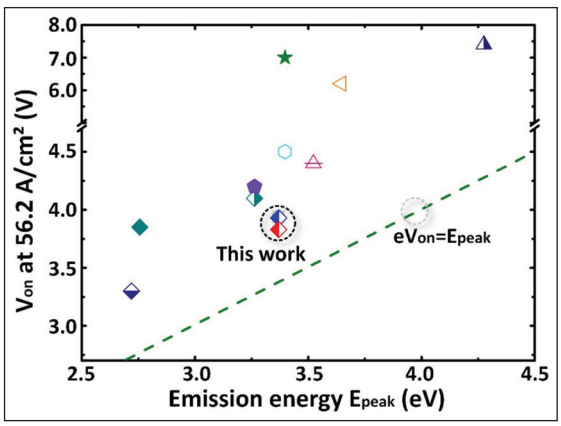
Another strength of the team's technology is that it has enabled UVA LEDs to operate at a lower voltage for a given current density (see Figure).

ITO is often used as a transparent conductive oxide in blue LEDs, but transferring it to UV variants is not easy, because the high work function of *p*-type nitrides hampers the formation of an ohmic contact between the ITO electrode and the *p*-type upper layer of the LED.

"Using interface treatment, we modify the interface property, so that the Schottky barrier at the ITO/LED interface is lowered," explains Wang.

The team has tried a variety of treatments, purging the interface with oxygen, trimethylindium (TMI) and tetrakis(dimethylamino)tin. Using the later, known as TDMASn, turned out to be the most effective treatment for improving the performance of the UVA LED.

"We want to emphasise that *in-situ* treatment may only be realised with MOCVD," argues Wang. "If ITO is grown by other methods, such as magnetron sputtering or thermal evaporation, *in-situ* treatment seems impossible."



Purging with tetrakis (dimethylamino) tin improvers the interface between ITO and GaN, leading to UV LEDs with lower forward voltages.

The ITO films were added in a home-built MOCVD tool.

"We built our lab-made MOCVD system because we believe that an MOCVD system for oxides could be cheaper," explains Wang, who points out that similar tools for growing nitrides are more complicated. "The designer has to isolate the growth chamber from atmosphere in order to suppress oxygen contaminants."

For oxygen, there are obviously no issues associated with oxygen contamination. Thus, the design of the MOCVD tool is much easier, and its cost far lower.

The researchers uncovered the benefits of purging with TDMASn by taking AlGaN-based LED structures and depositing 85 nm-thick layers of ITO by MOCVD. For the control, they deposited ITO directly on the device; they also produced two alternatives, involving intermediary 6s purges with either TMI or TDMASn.

As well as making 250 μm by 760 μm LEDs from these epiwafers, the engineers produced isolated ITO films with the three different treatments, to determine the impact of these processes on transmission through the oxide. All three samples had a transmission in excess of 90 percent at 368 nm, with the variant formed with TDMASn producing the highest value, 95.9 percent.

Additional benefits of the TDMASn purge included a reduction in surface roughness, a lower sheet resistance, and a lower forward voltage. At a 100 mA drive current, this LED operated at 3.83 V, more than 0.1 V lower than the cousins formed by the other processes.

"We are now using our MOCVD-ITO as electrodes in flip-chip UVA LEDs," explains Wang. In a conventional flip-chip LED, a metal mirror has a dual role, acting as a reflector and an electrode. However, the refectance of the mirror is inferior to that of a distributed Bragg reflector, so Wang and his co-workers are trying to increase light extraction efficiency by combining the distributed Bragg reflector with ITO.

"We are also focusing on large-size, one watt, high-power UVA-LEDs and their application in UV curing."

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Scrutinising thick films of AlInN

A range of characterisation techniques reveal that while AlInN films have some great attributes, they can be let down by surface pits

TO PRODUCE GaN-based lasers that are lattice-matched, there needs to be a switch from the conventional choice of cladding material, AlGaN, to the alloy AlInN.

Unfortunately, very little is known about the characteristics of AlInN layers with a thickness comparable to that of the cladding – but researchers from Japan are addressing this omission by produced these structures on sapphire, before scrutinising them with a range of techniques, including X-ray diffraction, cross-sectional transmission electron microscopy and spectroscopic ellipsometry.

Prior to this recent work by a collaboration between Nagoya Institute of Technology and Meijo University, there have been very few reports of AlInN films greater than 100 nm thick – and for those thicker films, no details have been provided.

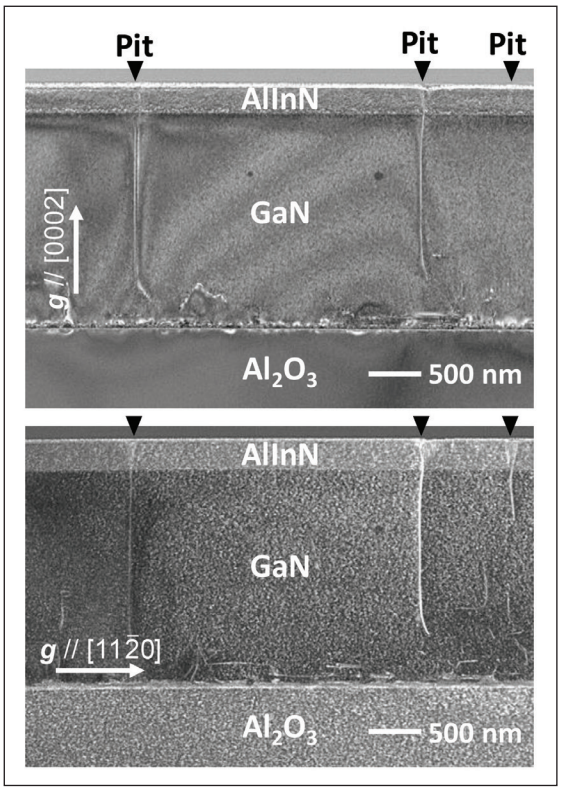
To study thick AlInN films, the team from Japan took a 2-inch GaN-on-sapphire template, loaded it into an MOCVD chamber, and deposited $Al_{0.17}In_{0.83}N$ layers with thicknesses of 40 nm, 90 nm and 300 nm, using conventional precursors, a susceptor temperature of 830 ˚C, and a pressure of 13.3 kPa.

Films of AlInN were deposited at 0.6 μm/hr, a growth rate that is markedly lower than that used for GaN. "However, this is not necessarily slow, considering conventional AlInN growth," explains corresponding author Makoto Miyoshi.

X-ray diffraction scans produced a strong peak for AlInN and periodical fringe peaks. Taken together, this indicates that AlN is a single-phase crystal, probably forming an abrupt interface with GaN. The X-ray spectra had a high degree of correlation with a corresponding simulation, which confirmed the thickness and the composition of the AlInN alloys.

To determine crystal quality, the researchers turned to X-ray rocking curves, atomic force microscopy and cross-sectional, dark-field transmission electron microscopy along two different crystal directions. These techniques revealed that the AlInN films have: a mosaicity that is strongly dependent on the underlying GaN; surfaces that feature flat areas and pits, which increase in size with the thickness of the film; and that these pits, originating from threading dislocations in the underlying GaN, are pure-edge and edge/screw-mixed dislocations.

The root-means-square roughness of the surface of the 300 nm-thick AlInN film is 1.82 nm. According to Miyoshi and co-workers, this value is not as small as it is for atomically flat surfaces, but it is still "rather good", considering the influence of the pits.



Cross-sectional, dark-field transmission electron microscopy images, acquired along two different crystal directions, reveal that the pits seen on the surface originate from threading dislocations in the underlying GaN.

However, the team believes that these AlInN films are not good enough for making lasers. "We need to decrease the surface pits," says Moiyoshi, who adds that the thickness of the film will have to be increased to around 500 nm.

Miyoshi and co-workers have turned to spectroscopic ellipsometry to determine the thickness of the film, and also its optical constants and bandgap. This technique revealed a value of 4.02 eV for the bandgap of the AlInN film.

The team plans to carry out more experiments with AlInN films. Their work will include understanding the mechanism of AlInN growth, growing free-standing GaN substrates with fewer threading dislocations, growing 500 nm-thick AlInN films, and controlling the impurity doping and conductivity of AlInN films.

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Better buffers boost laser lifetimes

High-quality buffer layers increase the lifetime of quantum dot lasers to millions of hours

RESEARCHERS in California claim to have set a new lifetime record for III-V-on-silicon, 1.3 μm lasers by slashing the threading dislocation density in the GaAs buffer layer.

The quantum dot lasers that they form, which can operate for millions of hours, could aid efforts directed at the monolithic integration of large-scale silicon electronics and III-V photonic devices.

"The breakthrough of our work is that we have reduced the threading dislocation density in the GaAs-on-silicon template from $3x10^8$ cm^{-2} to $7x10^6$ cm^{-2}," explains Daewhan Jung, spokesman for the partnership between researchers at the University of California, Santa Barbara, and Intel.

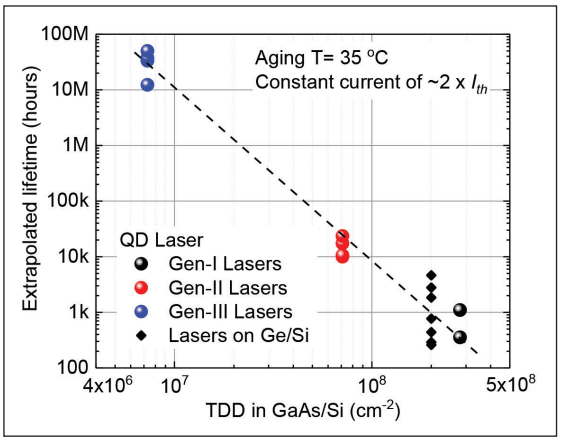
This lower threading dislocation density increased the lifetime of the laser by five orders of magnitude to more than ten million hours. In comparison, the incumbent III-V-on-silicon technology that has been developed over the last decade – GaAs-based quantum-well lasers – tends to lead to device failure within just hundreds of hours, due to dark-line defects.

The West-coast team underlined the importance of a high-quality buffer layer by evaluating the lifetime of quantum dot lasers formed on GaAs-on-silicon structures of varying quality.

For all the lasers, the underlying structure included an MOCVD-grown, 45 nm-thick psuedomorphic layer of GaP that is free from strain relaxation and anti-phase domains. "Through a special heat treatment and surface preparation before film growth, high-quality GaP can be grown on on-axis (001) silicon without an intentional miscut," adds Jung.

First-generation lasers were produced on a GaAs buffer layer that was formed by MOCVD growth at two different temperatures, while fabrication of second-generation devices involved an additional four cycles of thermal annealing. The team also produced third-generation lasers by starting with the second-generation approach and adding strained superlattices, formed from the pairing of InGaAs and GaAs. These superlattices are designed to act as dislocation filters.

Scrutinising all three forms of buffer layer with electron channel contrast imaging revealed that the threading dislocation density could be cut from 2.8 x 10^8 cm^{-2} to 7.1 x 10^7 cm^{-2} and then to 7.3 x 10^6 cm^{-2} by progressing from the process used for generation one lasers to that used for generations two and three.



Reducing the threading dislocation density enables a tremendous improvement in the lifetime of the quantum dot laser.

After conducting these measurements, the engineers loaded all three forms of template into an MBE chamber and grew GaAs/AlGaAs graded-index separate confinement heterostructures. Seven modulation-doped quantum dots layers were used in the first and second generation lasers. Meanwhile, third-generation devices contained five unintentionally doped quantum dot layers – this active region promises to lead to lower threshold currents at room-temperature.

Engineers processed the epiwafers into lasers with ridge waveguide widths between 3 μm and 5 μm, and cavity lengths varying from 1 μm to 1.64 μm. To improve performance, one of the laser facets was coated with a film that has a reflectivity of 99 percent.

Reliability testing at Intel revealed that the first generation lasers had a lifetime, defined as the time taken to double the threshold current, of just 355 hours at 35 °C. In comparison, second and third generation devices had lifetimes of tens of thousands of hours and tens of millions of hours, respectively. When the temperature of the third-generation devices reached 60 °C, lifetime fell to around 65,000 hours.

Jung says that in data centres, lasers may have to operate at temperatures of between 60 °C and 80 °C. "We chose 60 °C as a first step to test our laser's viability at increased temperatures. We plan to increase the testing temperature to 80 °C."

Reference

D. Jung *et al.* Appl. Phys. Lett. **112** 153507 (2018)

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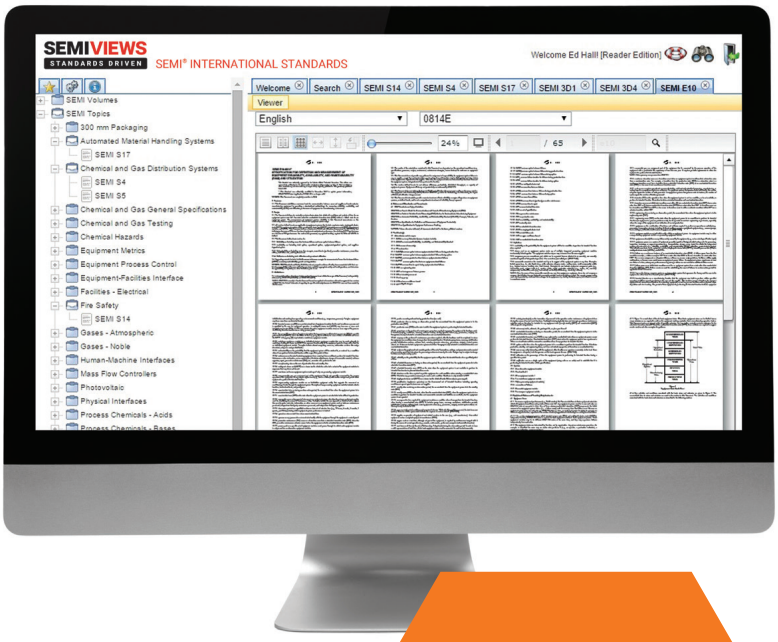

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