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VOLUME 31 ISSUE IV 2025

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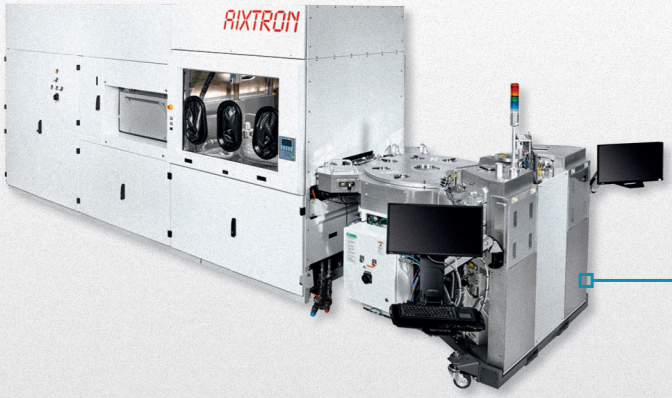


### G10-SiC

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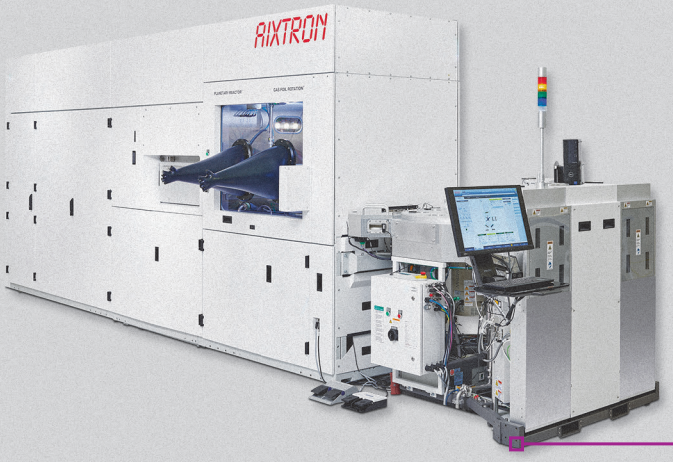


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# VIEWPOINT

BY RICHARD STEVENSON
EDITOR

# Imperfect perspectives

It's very easy to get caught up in the mood of the moment, allowing this to exert too much influence on your thinking.

I found myself guilty of exactly this when preparing this issue. Let me explain...

For more than a decade, we've been using issue IV to look at how the valuation of many companies within our industry has changed over the last 12 months – and when I took on this task this year I feared the worst, fuelled by thoughts dominated by escalating tariffs, a tumbling stock market, and concerns over falls in GDP that threaten to lead to a global recession.

But when I compiled the data, it's not as bad as I feared (and although it's not pretty, it's worth noting that there has been a rally in stocks in the last few days). While it's true that for many companies, their share price has fallen over the last year, that's not the case for all. Bucking this trend and soaring high are Lumentum and Coherent, recording gains of around 20 percent and 40 percent, respectively, on our *Compound Semiconductor Share Price Leaderboard*.

What's behind this success? Primarily, it's the incredibly strong demand for InP lasers that are supporting data centres, particular those providing AI.

With this demand showing no sign of abating, and the sector suffering from an industry-wide shortage of InP capacity for optical components, Lumentum and Coherent are taking steps to boost production. As part of these efforts, Lumentum is constructing a large three-story facility and cleanroom in Thailand, and Coherent is planning to expand its 150 mm InP line in Sherman, Texas, supported by the US CHIPS Act.

Aside from Lumentum and Coherent, those on this year's Leaderboard have seen their share price head south. Some of these falls are modest, others are more significant, and Wolfspeed's is an alarming 87 percent, highlighting some significant concerns for the company. It's faced a perfect storm of a global decline in SiC substrate demand, high costs of capacity expansion, and doubts that it will actually get to receive $750 million of funding under the US CHIPS Act.

Trying to navigate these incredibly choppy waters is the new CEO Robert Feurle, who will benefit from two recently appointed external advisers to the Board, Paul Walsh and Mark Jensen, who have both held CFO roles elsewhere.

Turning Wolfspeed into a profitable entity will not be easy, but there is still much promise, given that the long-term outlook for SiC is so strong. While it's easy to focus on the here and now – and clearly there are some severe problems to solve for Wolfspeed – outsiders should be wary off getting too caught up in this particular moment.

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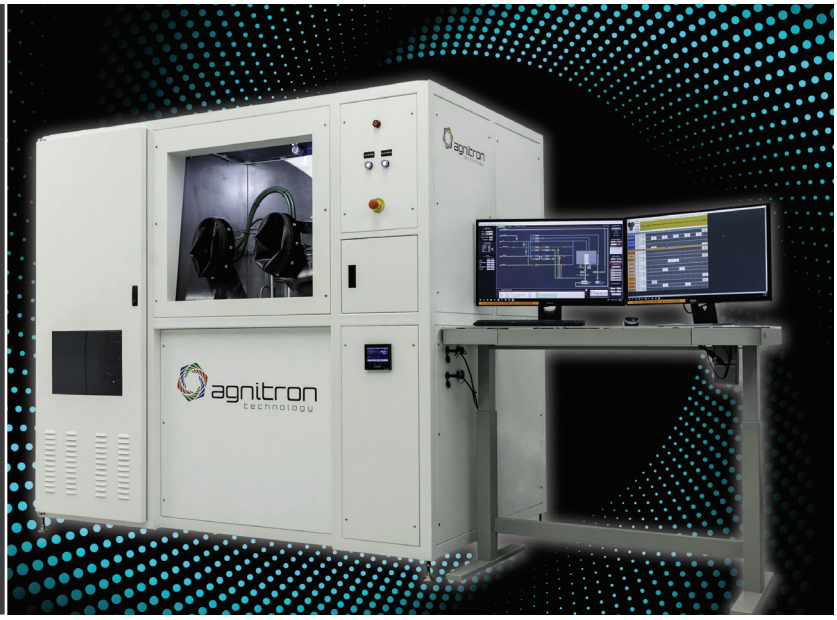




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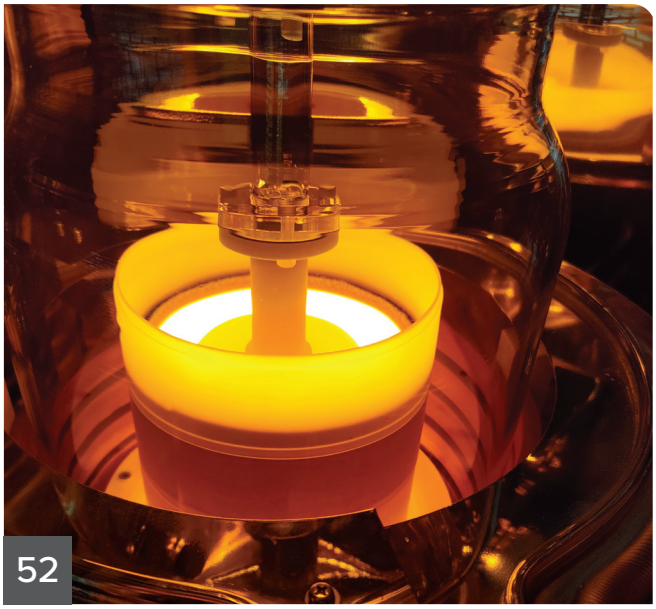
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## NEWS




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Printed by: The Manson Group. ISSN 1096-598X (Print) ISSN 2042-7328 (Online) © Copyright 2025

# Worries about Wolfspeed as a 'going-concern'

Company takes on external advisors to assist with strategic alternatives and capital restructuring

US SiC giant Wolfspeed has announced results for Q3 2025, with shares tumbling nearly 25 percent due to concerns for the company's long-term survival.

Q3 2025 revenue was $185 million, compared with $201 million for Q3 2024. The Mohawk Valley Fab contributed $78 million in revenue compared with $28 million in Q3 24. Gross margin was -12 percent.

While the top-line figures don't seem too bad, the company is struggling with $6.5 billion of debt obligations. And – as it said in the regulatory filing – "there is substantial doubt about the company's ability to continue as a going concern as of the issuance date, in accordance with the requirements of ASC 205-40."

Wolfspeed is waiting on $750 million in federal funding under the US CHIPS Act. In March 2025, President Donald Trump said US lawmakers should get rid of the law and use the proceeds to pay debt.

Meanwhile, Wolfspeed's customers are dealing with tariff-induced uncertainty, with General Motors trimming its 2025 profit forecast, while Mercedes-Benz had pulled its earnings outlook for 2025, according to Reuters.

TrendForce's latest research shows that weakening demand in the automotive and industrial sectors slowed shipment growth for SiC substrates in 2024, with global revenue for *n*-type SiC substrates down 9 percent year-over-year. Despite the decline, TrendForce says long-term SiC demand remains strong as the 8-inch roadmap gains momentum. Wolfspeed leads the SiC substrate market with 33.7 percent market share in 2024 and is leading the transition to 8-inch wafers. Chinese vendors TanKeBlue and SICC have 17.3 percent and 17.1 percent market shares respectively, placing them in second and third place. Coherent, by contrast, dropped to fourth place with a share of 13.9 percent.

Wolfspeed says its current operating forecast over the next 12 months will allow it to maintain operations and meet its obligations to customers, vendors and employees in the ordinary course of business. It has engaged external advisors Paul Walsh and Mark Jensen to the board to assist with strategic alternatives, including capital restructuring.

Walsh most recently served as CFO and SVP, Finance and Administration, at Allegro Microsystems. He previously served as CFO of Rocket Software and held multiple finance roles at Silicon Laboratories, ultimately serving as SVP and CFO. He currently serves on the boards of Kopin Corporation and Semtech Corporation.

Jensen brings an extensive background in finance and accounting, having most recently served as US managing partner, Technology Industry, at Deloitte from 2001 to 2012. Before joining Deloitte, he held senior roles as CFO of Redleaf Group and managing partner at Arthur Andersen. Jensen currently serves on the boards of 23andMe and Lattice Semiconductor.

Tom Werner, chairman of the board of Wolfspeed, said: "At the beginning of the year, the company outlined a plan focused on strengthening our capital structure, improving our path to profitability, and raising cost-effective." capital to support our growth plan. I'm pleased to report that the board and management have made significant progress against all of the priorities we outlined – completing our $200 million ATM offering, receiving $192 million of our Section 48D cash tax refunds, simplifying the business to focus on our pure-play 200 mm capabilities and accelerating our path to cash flow breakeven, and hiring Robert Feurle (pictured left) as Wolfspeed's new CEO."

"Most importantly, we continue to work closely with our lenders on ways to address our capital structure, so that Wolfspeed has a strong financial foundation to support its continued success."

Feurle, added, "One of the key drivers in my decision to join the company was Wolfspeed's enormous potential, underpinned by strong foundational elements. The company's SiC technology is second-to-none and the company has already established a greenfield, best-in-class, fully automated 200 mm manufacturing footprint to provide next-gen solutions to our customers. I am aligning the organisation to drive innovation across the business and in key strategic verticals that demand quality, reliability, and efficiency – precisely where our purpose-built 200 mm platform sets us apart."

Wolfspeed says its current operating forecast over the next 12 months will allow it to maintain operations and meet its obligations to customers, vendors and employees in the ordinary course of business.

# Introducing trench-based superjunction SiC

Infineon to use new SiC technology to expand the efficiency and compactness of its CoolSiC range

INFINEON is introducing trench-based SiC superjunction (TSJ) technology, adding to its existing CoolSiC product offering spanning 400 V to 3.3 kV.

"With the introduction of the TSJ concept, we are significantly expanding the technological capabilities of SiC," said Peter Wawer, president of Infineon's green industrial power division. "The combination of trench and superjunction technology enables higher efficiency and more compact designs – an important step for applications requiring the highest levels of performance and reliability."

Infineon says it intends to gradually expanding its CoolSiC product portfolio with SiC TSJ technology. This expansion will encompass a diverse range of package types, including discretes, molded and frame-based modules, as well as bare dies. The extended portfolio will cater to a broad spectrum of applications, targeting both the automotive and industrial sectors.

The first products based on the new technology will be 1200 V in Infineon ID-PAK for automotive traction inverters, and combine the advantages of trench technology and superjunction design, capitalising on Infineon's more than 25 years of experience in SiC and silicon-based superjunction technology (CoolMOS).

This scalable package platform supports power levels of up to 800 kW, enabling a high degree of system flexibility.

Key benefits of the technology include increased power density, achieved through an up to 40 percent improvement in $R_{DS(on)}$*A, allowing for more compact designs within a given power class.


Additionally, the 1200 V SiC trench-superjunction concept in ID-PAK enables up to 25 percent higher current capability in main inverters without compromising short-circuit capability.

This advancement also results in enhanced overall system performance, according to the company, delivering improved energy efficiency, reduced cooling requirements, and higher reliability for demanding automotive and industrial applications.

Moreover, the system benefits from reduced parallelisation requirements, which simplify the design process and lower overall system costs.

With these innovations, the Infineon ID-PAK package equipped with SiC TSJ technology contributes to the development of more efficient and cost-effective traction inverter designs for automotive applications.

As an early customer, Hyundai Motor Company development teams will engage with Infineon's trench-superjunction technology, using its benefits to enhance their EV offerings. This partnership is expected to drive the development of more efficient and compact EV drivetrains.

Initial ID-PAK 1200 V samples are available for selected automotive drivetrain customers. The SiC TSJ-based ID-PAK 1200 V package is expected to be ready for volume production in 2027.

# IQE announces 2025 results and new CEO

Company announces ‘solid’ financials and appoints Jutta Meier as CEO

COMPOUND semiconductor wafer firm IQE plc has announces its results for the full year ended 31 December 2024.

Jutta Meier, CEO and CFO of IQE, commented: “IQE delivered a solid set of financials in line with our January 2025 trading update. Our focus has been on reducing costs and optimising our footprint, and I am pleased to see this has resulted in an improved adjusted EBITDA position year-on-year.”

She added: “The strategic review remains ongoing and we have been encouraged by progress so far despite a challenging macro environment. IQE has a strong foundation from which to unlock value for all of our stakeholders and with a diverse customer pipeline, the continued end-market demand for our technology gives us confidence for the future. I am also delighted to be appointed as CEO as we continue to deliver on the positive progress we have made.”

## Financial highlights

Revenue for FY 2024 was £118.0 million, up £2.7 million sequentially.

Wireless revenue of £67.3 million increased 25 percent year-on-year, reflecting an increase in wireless GaAs sales linked to a higher penetration of Asian markets and an increase in GaN sales for 5G infrastructure.

Photonics revenue of £49.9 million decreased 16 percent year-on-year primarily because of softness in 3D Sensing and telecoms infrastructure markets, partially offset by a strong performance in Aerospace and Security markets for infrared-related products

CMOS++ revenue of £0.8 million was down 62 percent on a reported basis, reflecting a strategic rebalancing of the business’ product portfolio and a shift in focus towards diversification into GaN Power and MicroLED sectors. In FY 2025 IQE will no longer reporting CMOS++ revenue as a standalone segment.

Cash and cash equivalents were £20.6 million as at 31 March 2025.

## Business update

The company has been developing in various areas, including launching a Quantum Dot Laser foundry service for high-efficiency optical communications in data centres, with opportunity to take significant market share from incumbent laser technologies.

It has expanded the GaN RF Aerospace and Security business serving fast-growing end-market, including satellite internet constellation platforms (Low Earth Orbit Satellites – LEOS).

On the power front, IQE has a joint development agreement with X-FAB to create a Europe-based GaN Power device platform solution for automotive, data centres and consumer applications.

In other areas, it has developed InP and GaSb laser and detector technologies with a leading consumer OEM for healthcare sensing applications, and launched an 8-inch GaN-on-silicon microLED foundry service with in-house wafer cleaning, compatible with advanced Silicon CMOS manufacturing.

## Board update

Jutta Meier has been appointed IQE’s CEO following her successful period as Interim CEO. Jutta will continue in her dual role as CEO and CFO. Female representation on IQE’s board now stands at an above average 57 percent.

Mark Cubitt will continue to act as executive chair, providing support to Jutta and the executive leadership team through the ongoing strategic review. The composition of the Board will be re-evaluated following the conclusion of the Strategic Review.

Cubitt said: “I would like to recognise Jutta’s success as CEO of IQE since she took on the interim role over six months ago. The Board felt she was an excellent candidate and in that time she has stabilised and refocused the business and rebuilt confidence with both customers and employees.”

## Current trading and outlook

Global markets are being impacted by macroeconomic uncertainty and as a result, some end customer demand is being fulfilled with existing inventory. This was visible in Q1 trading but is expected to correct in H2 2025. Costs and capacity continue to be optimised to improve margins and cashflow.

IQE says its customer pipeline remains strong and is predicted to grow in H2 2025, driven by new product and customer engagements. Additionally, existing segments, including Aerospace and Security and optical communications are also expected to deliver growth, offsetting anticipated softness in wireless segments resulting from challenged consumer markets, particularly in Asia.

There is currently no direct impact to IQE from the implementation of US tariffs, however developments are being closely monitored and options are being explored with both suppliers and customers to mitigate any potential risk.

Revenue and adjusted EBITDA for the full year are expected to be within the range of analyst forecasts for FY 2025, with weighting towards H2 consistent with the destocking seen in Q1 and typical industry seasonality. These forecasts assume the inclusion of IQE Taiwan revenues pending the outcome of the strategic review.

# Uviquity emerges from stealth with $6.6m funding

US start up to develop PIC-based far-UVC technology for disinfection

UVIQUITY, a far-UVC start-up has emerged from stealth mode with $6.6 million in seed funding. The round was led by Emerald Development Managers, an early-stage venture capital firm specialising in deep tech, with participation from AgFunder and Mann+Hummel, companies involves in food and agriculture venture capital and filtration solutions.

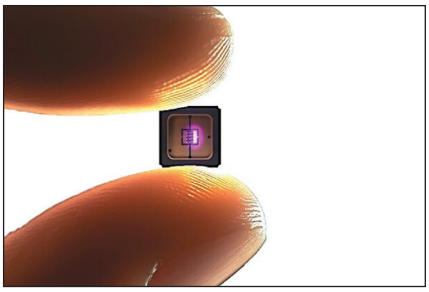
Uviquity is developing solid-state far-UVC (200 nm to 230 nm) semiconductor light sources designed to deliver safe, continuous, and chemical-free disinfection for air, food, and water applications.

The funding will support Uviquity's R&D efforts, accelerating the commercialisation of its proprietary PIC that couples blue laser light into frequency-doubling waveguides, enabling a scalable, single-chip far-UVC solution that can integrate into a wide variety of applications using standard photonic packages.

"We believe far-UVC light is the future of pathogen control – and Uviquity's wide-bandgap semiconductor platform is the key to making it practical, scalable, and safe," said Scott Burroughs, CEO and co-founder of Uviquity. "This funding allows us to bring our vision to life and unlock a new standard for clean air, safe food, and pure water – at scale and without chemicals."

Far-UVC light has been proven safe for continuous exposure to human skin and eyes while rapidly inactivating all known pathogens, including viruses, bacteria, fungi, and mold spores.

Uviquity says its chip-based semiconductor approach offers a



compact, energy-efficient, and durable solution that can be integrated into light fixtures, air handling systems, food packaging and processing equipment, agricultural crop protection systems, water purification systems, and consumer appliances.

"With its proven team and novel technology, Uviquity fits perfectly with our goal to invest in exceptional companies that are solving real problems," said Cy Schroeder of Emerald Development Managers.

# Riber secures major order from Australia

MBE 412 cluster system to be used to advance research in IR technologies

FRENCH MBE firm Riber has announced the sale of a research MBE 412 cluster platform with an automatic wafer transfer system to a leading Australian research laboratory.

The Western Australia Node of the Australian National Fabrication Facility (ANFF WA Node), based at the University of Western Australia, is the only research center in the country with expertise and device fabrication capabilities for infrared (IR) sensors, including high density imaging focal plane arrays.

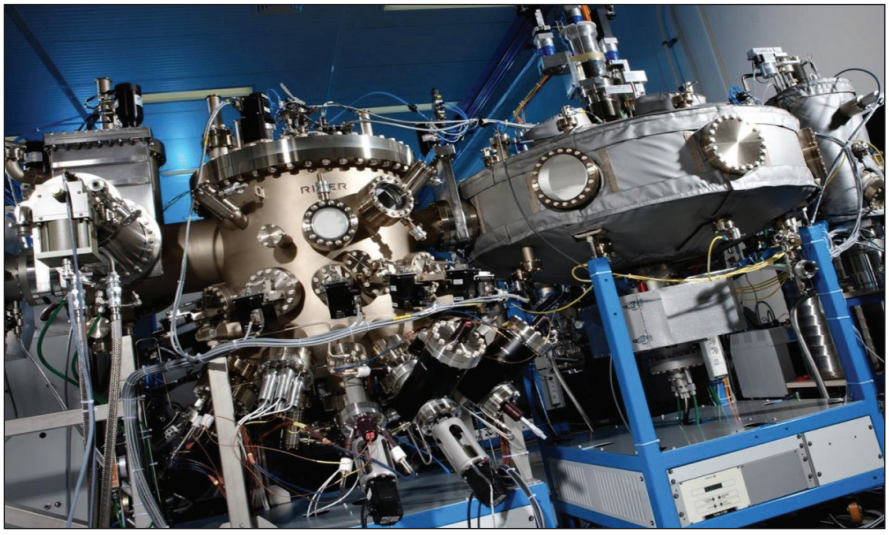
To advance its research in IR technologies and to support the development of sovereign IR sensor capabilities in Australia, the ANFF WA Node has placed an order for a new Riber MBE 412 system. This dual chamber cluster platform will play a key role in long-term R&D efforts and is expected to significantly enhance the laboratory's capabilities.

Specially designed for research on next-generation infrared imaging devices, the MBE 412 system is fully automated, supports wafers up to 7 x 7 cm, and is equipped with Riber's Crystal XE software for state-of-the-art uniformity performance.

To meet customer needs, the system is mecury-compatible, enabling the growth of HgCdTe structures. All components – including equipment, pumps, and effusion cells – have been customised to comply with the lab's specific requirements, with comprehensive technical and process support provided.

The system will be installed in 2026 in a new laboratory at the University of Western Australia, adjacent to an existing MBE system.

Annie Geoffroy, chair and CEO of Riber commented: "We are proud to continue supporting our long-standing partners. This order placed 36 years after the acquisition of a first Riber 32P system – still in operation today – illustrates the enduring trust in our technology. The MBE 412 platform, equipped with the latest innovations, reaffirms our commitment to delivering high-performance, reliable, and safe MBE solutions tailored to the evolving needs of research institutions."



## Finwave nets $8.2 million

GaN INNOVATOR Finwave Semiconductor has announced a new $8.2 milion bridge investment round, led by Fine Structure Ventures, Engine Ventures, and Safar Partners – with strategic participation from technology partner GlobalFoundries.

Finwave will use this investment to accelerate revenue generation, expand its product portfolio and continue developing GaN-on-silicon technology for high-power RF switches, power amplifiers for communications infrastructure, and power amplifiers for mobile devices.

"We are emboldened by the support of our investors, who share our belief in the commercial potential of our technology," said Pierre-Yves Lesaicherre, CEO of Finwave. "This funding round validates the years of engineering and innovation behind our proprietary GaN-on-silicon technology and provides resources we need to move from the development phase to delivering differentiated, high-performance products. More than just funding, this is a clear endorsement of our direction – and a strong signal that the industry believes in the path we're on."

"Since our initial investment, Finwave has made remarkable progress towards becoming a leader in GaN-on-silicon high-performance RF components," said Jennifer Uhrig, senior managing director, Fine Structure Ventures.

"Their strategic foundry partnership with GlobalFoundries and distribution partnership with RFMW have been particularly notable, legitimising their design capabilities and giving customers confidence in Finwave's ability to bring high-performance, reliable products to market."

# Singapore-MIT group to make machines 'see' like humans

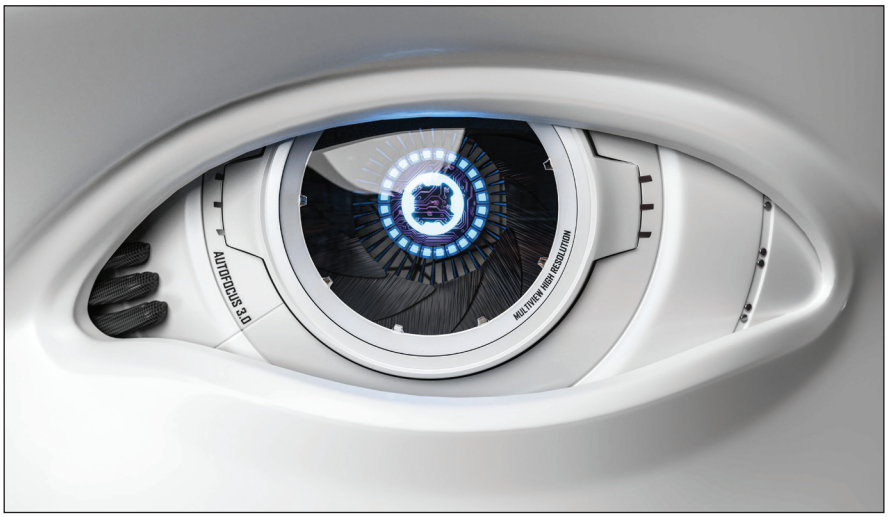
WISDOM programme to use wafer-scale integration to combine LEDs and VCSELs, metasurfaces, and CMOS electronics

THE Singapore-MIT Alliance for Research and Technology (SMART) has launched a new interdisciplinary research group focused on developing next-generation 3D-sensing technologies for practical use across industries such as automotive, consumer electronics, aerospace and healthcare.

The multi-million-dollar WISDOM (Wafer-scale Integrated Sensing Devices based on Optoelectronic Metasurfaces) research group will use wafer-scale integration to combine three separate elements: optical metasurfaces; optoelectronic devices, with a focus on LEDs and VCSELs; and silicon CMOS electronics.

Jointly led by faculty from MIT and Nanyang Technological University, Singapore (NTU Singapore), the group will focus on developing ultra-thin, scalable sensing devices to allow machines such as autonomous vehicles and robots to perceive depth, shape and spatial detail safely and with more versatility, much like human vision.

Using this approach, the team aims to redefine the capabilities of lidar systems to enhance detection accuracy, extend range and field-of-view, and




reduce motion artifacts. The group thinks the technology also opens the door to new applications like glasses-free 3D displays and high-speed optical communication.

SMART WISDOM will be led by co-lead principal investigators Juejun Hu, professor of materials science and engineering at MIT, and Tan Chuan-Seng, professor of electronic engineering at the school of electrical and electronic engineering at NTU Singapore.

"What makes me really excited about WISDOM is that we're putting together pieces that haven't been combined before – to benefit a ton of industries and use cases. For example, think how a super light and powerful lidar system could make trips to planets beyond Mars a reality. It's like having a whole new set of eyes for exploration, and about making the seemingly impossible, possible," said Juejun Hu.

The project is supported by the National Research Foundation Singapore under its Campus for Research Excellence and Technological Enterprise programme.

# Indium Corp and Rio Tinto's gallium sourcing project

Companies successfully extract gallium from feed sourced at Rio Tinto alumina refinery in Quebec

INDIUM CORPORATION and Rio Tinto have announced the successful extraction of gallium from feed sourced at Rio Tinto's Vaudreuil alumina refinery in Saguenay, Quebec, Canada.

They say that this achievement highlights the power of collaboration in building a more robust global supply chain for gallium.

Gallium is currently produced in limited quantities worldwide. This partnership is working to create a reliable and sustainable supply of this essential material to meet growing global demand for advanced technologies. Indium Corporation designed and developed this gallium extraction process in the United States at its Rome, NY, research and development facility.

"This milestone is a major step forward in our joint efforts to create a new and robust supply of gallium," said Ross Berntson, president and CEO of Indium Corporation. "Through this collaboration, we have demonstrated the viability of gallium extraction and laid the groundwork for commercial production to benefit industries worldwide."

Jérôme Pécresse, CEO, Rio Tinto Aluminium, added, "We are very proud to announce this significant milestone in our important research and development project to extract and valorise gallium from our aluminum operations in Quebec. Together, through this innovative partnership, Rio Tinto and Indium Corporation strive to strengthen the North American supply chain for gallium, a critical and strategic mineral."

Indium Corporation will continue to develop the extraction process at its research and development facility to meet the planned commercial scalability needs for a 3.5-tonne demonstration plant that would be located in Saguenay, Quebec, and then eventually commercial-scale capacity of 40 tonnes annually, addressing an estimated five to 10 percent of global gallium supply.

**SENSING**
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**InP**
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# RIBER's **MBE production systems**

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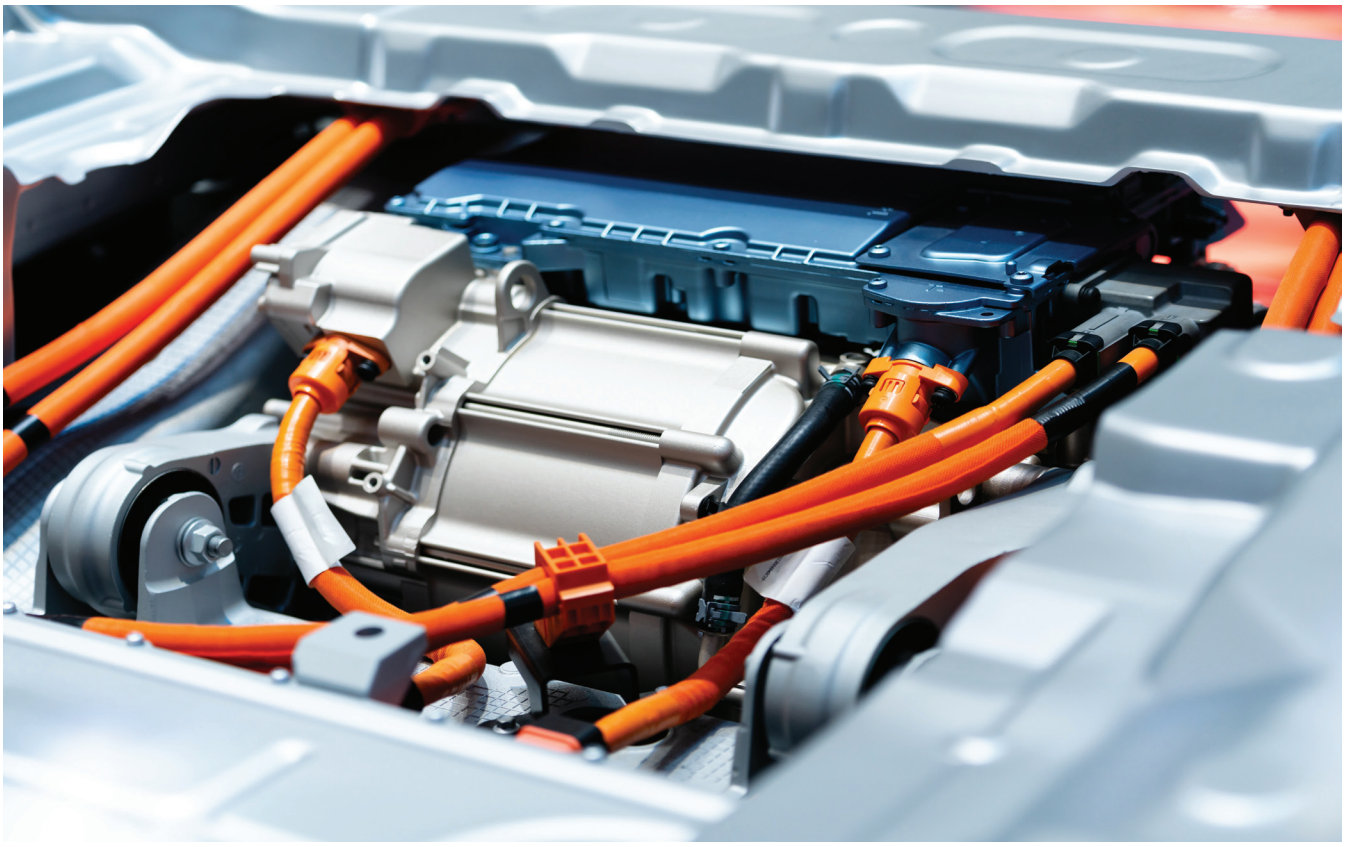


# Smart GaN HEMT + IGBT = EV success?

Cambridge GaN Devices is targeting the powertrain of electric vehicles with the combination of IGBTs and its proprietary integrated circuit enhancement GaN technology.

**BT RICHARD STEVENSON, EDITOR, CS MAGAZINE**

TODAY'S DESIGNERS of power trains for electric vehicles face a difficult choice. Should they view cost as paramount and select silicon IGBTs; or should efficiency be the priority, and they deploy SiC MOSFETs? Whichever they choose, a significant compromise will be made.

But now there's the promise of a third way, pioneered by a handful of producers of GaN – they are claiming that they could offer products with a price close to that of silicon solutions, while delivering an efficiency similar to that of SiC, by pairing a GaN HEMT with a silicon transistor.

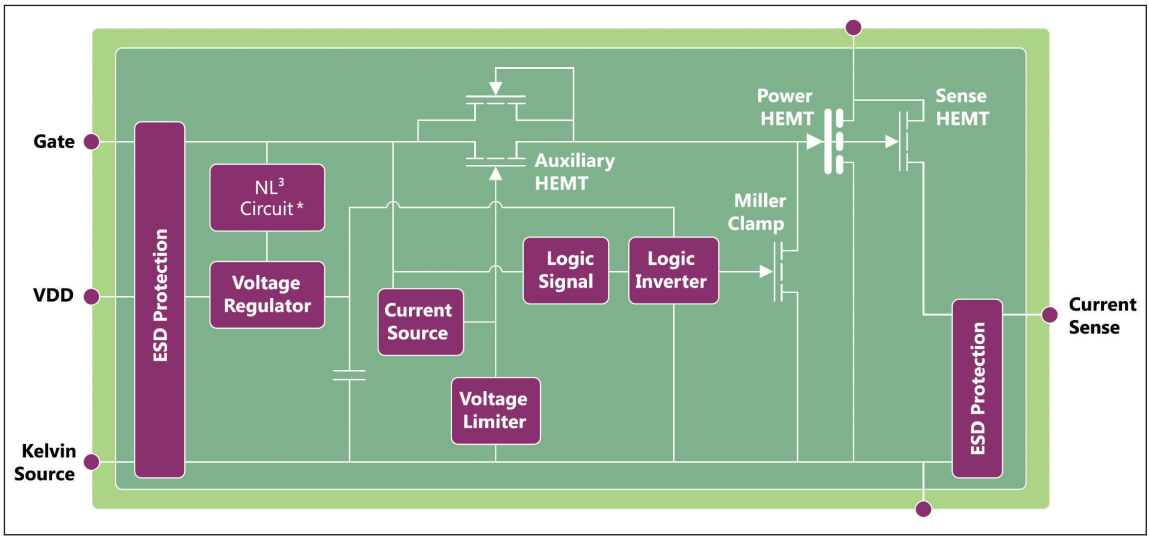
Amongst these trailblazers, Cambridge GaN Devices (CGD) claims that it is standing out from the crowd with its proprietary integrated circuit enhancement GaN technology, which it refers to as ICeGaN. The company is championing the combination of its 'intelligent' GaN HEMTs, which feature an enhancement-mode *p*-GaN HEMT rated at 650 V, and an IGBT. It's a patent-pending pairing with the moniker Combo ICeGaN.

According to Daniel Murphy, Director of Technical Marketing at CGD, the company's ICeGaN is its core technology, as well as its unique selling point. "This is what we're building the company around. The DNA of CGD, if you like."

One of the primary strengths of ICeGaN is that it provides ease of use. "You can essentially treat a GaN transistor like a MOSFET," says Murphy. Due to this, it's possible to use a very simple, low-cost driver to accompany the GaN HEMT.

Another great attribute of ICeGaN is that it facilitates zero-voltage switching, thanks to the inclusion of a Miller clamp. "There's no need for a negative voltage to be applied to switch the device," says Murphy, explaining that this refinement allows the driver to be simpler and cheaper. What's more, the Miller clamp ensures a very efficient turn-off of the GaN HEMT.

In addition to these valuable assets, absent in conventional GaN HEMTs, CGD's ICeGaN




➤ IceGaN is a form of smart power HEMT that features advanced sensing and protection capabilities.

technology has a slightly higher threshold voltage for the transistor.

"We've shifted it up to about three volts," says Murphy, explaining that this adjustment brings ICeGaN technology in line with standard silicon devices. "Hence, you can use standard silicon drivers."

The slight increase in threshold voltage also eliminates the danger of spurious turn-on.

With Combo IceGaN, higher efficiencies are realised by drawing on the complementary benefits of both classes of transistor.

"GaN comes into play at light loads, where you have very low switching losses. It brings increased efficiency," enthuses Murphy, who adds: "At high loads, and in some fault conditions, the robustness of the IGBT comes into play."

While the levels of efficiency provided by Combo IceGaN are not quite as high as they are with a full SiC solution, it provides a cost saving of around 40 percent to 50 percent, according to Murphy. And compared with only IGBTs, efficiency is 3 percent higher, based on measurements that consider the Worldwide Harmonised Light Vehicles Test Procedure cycle. "That obviously translates into either a less expensive battery or extended range," remarks Murphy.

As well as targeting the power train, CGD is pursuing opportunities in on-board chargers and DC-to-DC converters in electric vehicles, as well as industrial data centres, through the development of more innovative approaches. In this sector, power densities and power levels tend to increase year-on-year. "So, we're needing to improve the form factor all the time, and investigate different ways to address the packaging to meet the thermal requirements," says Murphy.

As all these applications involve very high power levels, the increase in chip area associated with additional features of ICeGaN, such as advanced sensing and the protection function, is relatively modest. Thanks to this, CGD is able to produce highly functional, competitively priced products.

Like many players in GaN power electronics, CGD is fabless, with chips produced at TSMC. This world-renowned Taiwanese foundry is responsible for the growth of epiwafers and their processing into devices. Packaging is undertaken at another partner, ASE.

As the Combo GaN technology can incorporate a range of IGBTs, CGD is planning to operate at the chip level within the supply chain. "We're looking for module partners, we're looking for car makers, tier ones that are interested to adopt this approach, and then we would support them with the sale of bare die," says Murphy.

One of the reasons why CGD is focusing on the traction inverter within the electric vehicle market is the volume of GaN that's required. "It is so much higher, because the power level is so much higher," claims Muphy, who adds that the other big draw is the substantial technical challenge. "We're a company with lots of smart people, and we're very ambitious. So that's why we're targeting traction."

Given the conservative nature of the automotive industry, it will take time for CGD to penetrate this market. The plan is to begin by launching discrete products for on-board chargers and DC-to-DC converters in 2026.

"The idea is for traction to try and enter a carmaker platform around 2028 timescale, and sooner than that with on-board chargers and DC-to-DCs," says Murphy.

So, while the makers of SiC MOSFETs are going to face stiff challenge from other wide bandgap devices, the competition is not going to begin immediately.

# Infineon's expanding 2 kV portfolio

Joining Infineon's 2kV MOSFETs are Schottky barrier diodes with identical voltage ratings

**BY RICHARD STEVENSON, EDITOR, CS MAGAZINE**

HIGH ON THE AGENDA of many design engineers in increasing the electrical efficiency of their systems. Gains on this front trim carbon dioxide emissions and utility bills, while reducing heating, which simplifies thermal management and enhances reliability.

Today, two well-trodden routes may be taken to increase the efficiency of electrical systems. One of these proven pathways is to replace silicon power electronics with those that have a wider bandgap, as this reduces resistance. And the other common approach is to increase the voltage of the electrical system, and this enables a reduction in current and ohmic heating.

While both approaches pay dividends, rather than picking one over the other, it's better to adopt both practices. And helping to do just that is the trailblazer of the SiC Schottky barrier diode (SBD), Infineon Technologies: it added a 2kV SiC SBD last October, and has just introduced a sibling, rated at the same voltage and housed in a different package. This pair of diodes complement Infineon's 2 kV MOSFET, launched in March 2024.


➤ Infineon's 2kV SiC Schottky barrier diode in a TO-247-2 package majors on clearnace.

Infineon has been refining the SiC SBD for decades, having brought the first commercial device to market back in 2001. Major revisions to this diode since its debut include a new backside die metallisation and die attach technology, and more recently, the introduction of thin wafer technology, making an appearance in the fifth-generation portfolio. With these SBDs, the thickness of the die is slashed from 350 μm to just 110 μm.

In 2018, the European powerhouse introduced a sixth-generation of SiC SBDs, featuring an electrochemical barrier between the metal and semiconductor that reduces the knee voltage by around 0.1 volts.

"For 650 volts, this is a big advantage, but not so much for other blocking voltages," remarks Peter Friedrichs, Infineon's Vice President of SiC. "For that reason, Gen 6 remained at 650."

By offering fifth-generation 2 kV SiC SBDs in two different packages – initially TO-247PLUS-4-HCC, and now the TO-247-2 package – Infineon is giving design engineers the opportunity to select between a diode that majors on clearance and on creepage. The former metric is related to the physical distance between the pins, with a higher value reducing the chances of arcing, while creepage considers the conductance pathway along the package surface.

"[With the TO-247PLUS-4-HCC] there's an extra gap in the plastics that forms a longer creepage," says Friedrichs.

It's not clear which of the two variants will prove more popular. "We can scale both of them according to customer needs," says Friedrichs.

Infineon is mainly targeting two markets with its expanding portfolio of 2 kV power devices: the solar sector and the charging of electric vehicles.

To provide high-power, fast charging of electric vehicles, bus voltages as high as 1,500 V are employed. So, to ensure reliability in this application, power devices are ideally rated at 2 kV.

Within the solar market, one of the trends has been an increase in the output voltage of the panels. "Today, 1,500-volt panels are state-of-the-art, but there are already first solutions with 2 kV and even higher," says Friedrichs.

While it is theoretically possible to serve both these applications with silicon devices related at 2 kV, the electrical losses are unacceptable. So wide bandgap

By offering fifth-generation 2 kV SiC SBDs in two different packages – initially TO-247PLUS-4-HCC, and now the TO-247-2 package – Infineon is giving design engineers the opportunity to select between a diode that majors on clearance and on creepage

devices with a low voltage rating have been adopted, using what is referred to as a multi-level topology.

"You stack components with a lower blocking voltage in series to manage the higher voltage," explains Friedrichs, illustrating this point by suggesting that rather than using a 2 kV device, two 1.2 kV devices may be used in series. However, as well as doubling the number of devices, multi-level topology designs increase the complexity for controlling the circuit and magnify cost at the system level.

As one would expect, Infineon's 2 kV devices are more expensive than their 1.2 kV siblings.

"2 kV comes at a higher price, since we need a thicker epitaxial layer, a thick drift zone and a larger area. This, of course, contributes to cost, but it's still more affordable than putting two 1.2 kV in series," explains Friedrichs.

For SiC devices, the substrate accounts for a significant proportion of device cost, especially for SBDs, even though they are smaller than MOSFETs. However, substrates costs are falling, with a significant reduction in the last 12 to 15 months, according to Friedrichs.

For both of the applications that Infineon is targeting humidity is an issue, as electric vehicles and solar panels operate outdoors.

Friedrichs says that humidity is a particularly significant concern for solar applications, due to the low night-time temperatures that leads to condensation in the system. It's not possible to address these concerns with a perfect hermetic seal, and if moisture enters the power devices, this can impact long-term reliability.

Infineon has been aware of this issue for many years, having been supplying devices to makers of solar systems since 2010. "From that point onwards, we have integrated special measures to protect the silicon carbide chips against any moisture-related degradation," says Friedrichs.

Two sites for production of its SiC portfolio have been established by Infineon: Villach, Austria; and Kulim, Malaysia.

"In Kulim, we are just starting to ramp silicon carbide front-end production," says Friedrichs. "We start with the MOSFET. So, at the moment, all the diodes are produced in Villach."

But with demand for SiC power devices set to rise, it will potentially not be long before the Kulim fab is serving customers all around the world with a broad and expanding portfolio that includes high-voltage SBDs.


➤ Thanks to an extra gap in the plastics, the TO-247PLUS-4-HCC suits engineers requiring a high degree of creepage

# The tipping point for AlN

Advances in AlN substates are positioning this nitride as a transformational material in next-generation electronic and optoelectronic applications

**BY KASEY HOGAN FROM CRYSTAL IS**

DEPLOYMENT of devices in space is increasing at a phenomenal rate, creating a lucrative opportunity for our industry. However, winning sales in such a harsh environment is not easy, as it involves extreme temperatures and persistent bombardment by radiation, conditions that make it very challenging for RF and power devices to deliver high levels of performance throughout the lifetime of the mission. In addition, reducing the payload mass is critical to easing launch costs and meeting the strict size, weight, and power constraints of aerospace systems.

But that's what's required – in fact there's demand for robust devices that combine a high-power density with a high-voltage capability and a high-frequency capability in many extreme environments; spanning both spaceborne and ground-based systems where reliability, efficiency, and compactness are critical.

The challenge of meeting these exacting requirements is driving interest in new semiconductor materials. Over the last decade, devices made from silicon have been displaced by those made from two wide bandgap materials, SiC and GaN, that are enabling a higher power density, improved thermal management, and broadband operation. But the defence and aerospace industries are not satisfied. Instead, it craves even higher levels of performance – and promising to fulfil them are ultrawide bandgap semiconductor materials, such as AlN, diamond, and $Ga_2O_3$.

Within that family of ultrawide bandgap devices, AlN has generated significant attention for many years. Judged by various figures-of-merit, there's no doubt that this nitride has tremendous potential. However, it has a reputation as a difficult material to dope, and it's been challenging to produce substrates with a significant size at volume. Due to these issues, some may have dismissed AlN as a material that's never going to make an impact.

But recent developments suggest otherwise, and there's good reason to believe that after showing its promise for several decades, AlN is now on the cusp of becoming a mainstream material for chip production.

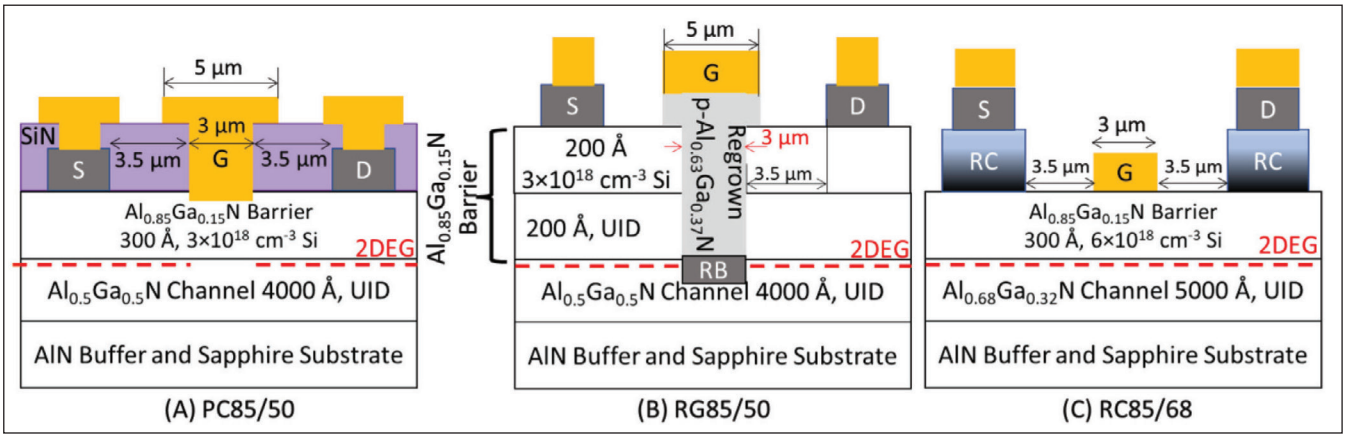
For many years, significant technical challenges in the doping, contacting and the fabrication of devices, along with the availability and cost of native substrates, has hindered progress and the adoption of native AlN devices. Due to bandgap of 6.2 eV, AlN is challenging to dope, due to deeper dopant levels. In addition, it's far from easy to form an ohmic contact with standard metallisation. However, recent work shows that these challenges are not insurmountable.

Another attraction of AlN, which marks it out from the other members of the ultrawide bandgap community, is that it's part of the III-Nitride material system, which includes GaN and AlGaN. Thanks to this, it's possible to produce devices that leverage a very wide compositional range. Such devices could be produced on bulk single-crystal AlN substrates that provide a close lattice-matched foundation that minimises dislocation density and enhances thermal management, and ultimately unlocks the full potential of III-Nitride-based architectures. With recent advancements in AlN substrate technology, this is now a reality.

## Commercially viable substrates

As well as its potential for serving in space, AlN has been viewed for many years as an enabling technology for optoelectronic devices, thanks to its high thermal conductivity, ultrawide bandgap, low dislocation density and its close lattice matching with other III-Nitrides.

Due to these strengths, AlN substrates are used to produce commercial UVC LEDs, with a manufacturing ecosystem producing thousands of 2-inch diameter substrates per year. Now that the




➤ Transistor epitaxial architectures and layout indicating locations of the source (S), gate (G), drain (D), regrown barrier (RB), regrown contact (RC), and 2D electron gas (2DEG).

viability of commercial optical-grade substrates is beyond doubt, this material is being considered for electronic device development.

To succeed in this new domain, it is critical that large-diameter, high-quality, native substrates are widely available – they are a crucial component in the semiconductor supply chain. Recently, much progress has been made on this front. Last year, my company, Crystal IS, reported the availability of 100 mm bulk AlN substrates for research purposes – along with announcements on consistent progress in quality and manufacturability. These milestones in the development of AlN substrates have spurred the development of AlN-based devices in areas ranging from academia to government programmes. There have been significant investments all over the world to develop an industrial supply chain. While technological barriers still exist to realising the full promise of AlN, it's important to note that there have been two recent works related to novel transistor structures on AlN that show progress. Read on to learn more about them.

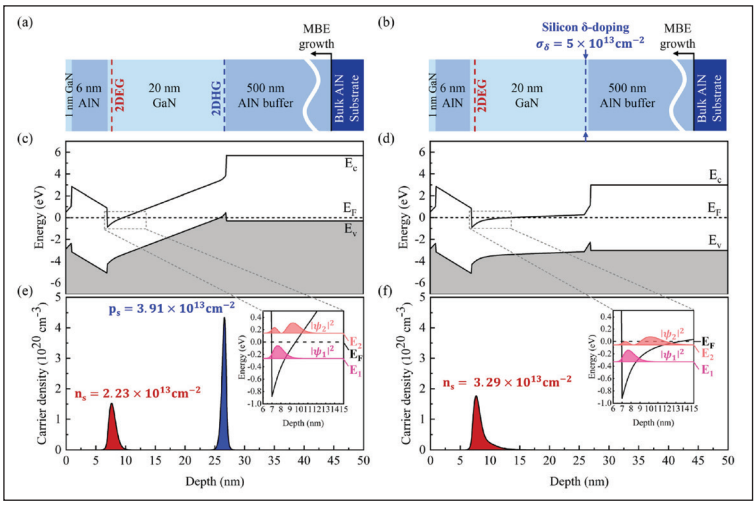
## Overcoming barriers for AlN-based devices

One of the strengths of the AlN substrate is that it provides a foundation for utilising aluminium-rich AlGaN layers or thick AlN layers – which may offer a transformational performance compared with what is possible with wide bandgap materials. Ultra-wide bandgap materials, such as AlN, have a high bond strength and a high thermal conductivity that allows for high breakdown fields and operation in extreme environments. Devices made from them are capable of reliable performance and longevity in space, sea, and desert.

Traditionally, research into AlN-based materials has been undertaken on thin AlN templates, grown on sapphire substrates. However, with the availability and cost-reduction of bulk AlN substrates with diameters of 2-inch, 3-inch and 100 mm, this research can now be conducted on material with far superior quality and thermal conductivity.

Having widespread availability of native substrates is helping to address the challenges associated with doping and contacting native AlN material, as well as aluminium-rich AlGaN, which has a high bandgap. A team at Sandia National Laboratory has recently reported a low ohmic contact resistivity in aluminium-rich layers, realised by utilising a re-grown reverse compositionally graded contact. They also describe a re-grown *p*-type AlGaN gate structure, which leads to a large positive threshold voltage and negligible gate leakage. Together, these developments provide a promising route towards high-current aluminium-rich AlGaN transistors that will enable a new operating regime for discrete high-power devices, by setting a new bar for breakdown voltage and on-resistance.

Another key breakthrough, coming from a team at Cornell University, is an AlN/GaN/AlN quantum-well HEMT on the bulk AlN substrate platform. This device offers substantial performance benefits for next-generation RF and power electronics.




➤ (a) Schematic of the epitaxial undoped AlN/GaN/AlN QW HEMT heterostructure. (b) δ-doped AlN/GaN/AlN XHEMT heterostructure includes a sheet of *n*-type donors.

According to recent published work, this group has developed a so-called delta-doping method to enhance the electron mobility in the thin GaN well. Other efforts have focused on making the GaN layer thicker, to distribute the high electric field caused by the GaN/AlN polarisation discontinuity across a larger distance. However, this approach may induce significant defects into the material, limiting thermal performance.

Cornell's approach allows the channel to remain thin and strained, while enjoying the extremely high crystalline quality afforded by the AlN substrate. The delta-doping method offsets the high electric field and the presence of an undesired polarisation-induced positive charge, without sacrificing crystalline quality or creating an unwanted second channel. This team's HEMT combines a high electron density and a high mobility with a low sheet resistivity. Controlling and enhancing the doping in this material through polarisation charge, rather than the traditional method of implantation or incorporation of dopant atoms, is a promising development.

Drawing on the recent increases in native AlN substrate availability by the main global players, now is time for RF and power device manufacturers to ramp up their development efforts on this material. While historical concerns around the technical challenges of doping and forming ohmic contacts remain, they can be overcome with significant effort and investment.

The key point is that the bulk AlN substrate diameter has reached the electronic-industry relevant diameter of 100 mm, and there's a proven route for this material to achieve commercially relevant volumes. Due to this triumph, AlN is now well positioned to lead the ultra-wide bandgap materials into the future, but to do so requires continued innovation within our community.

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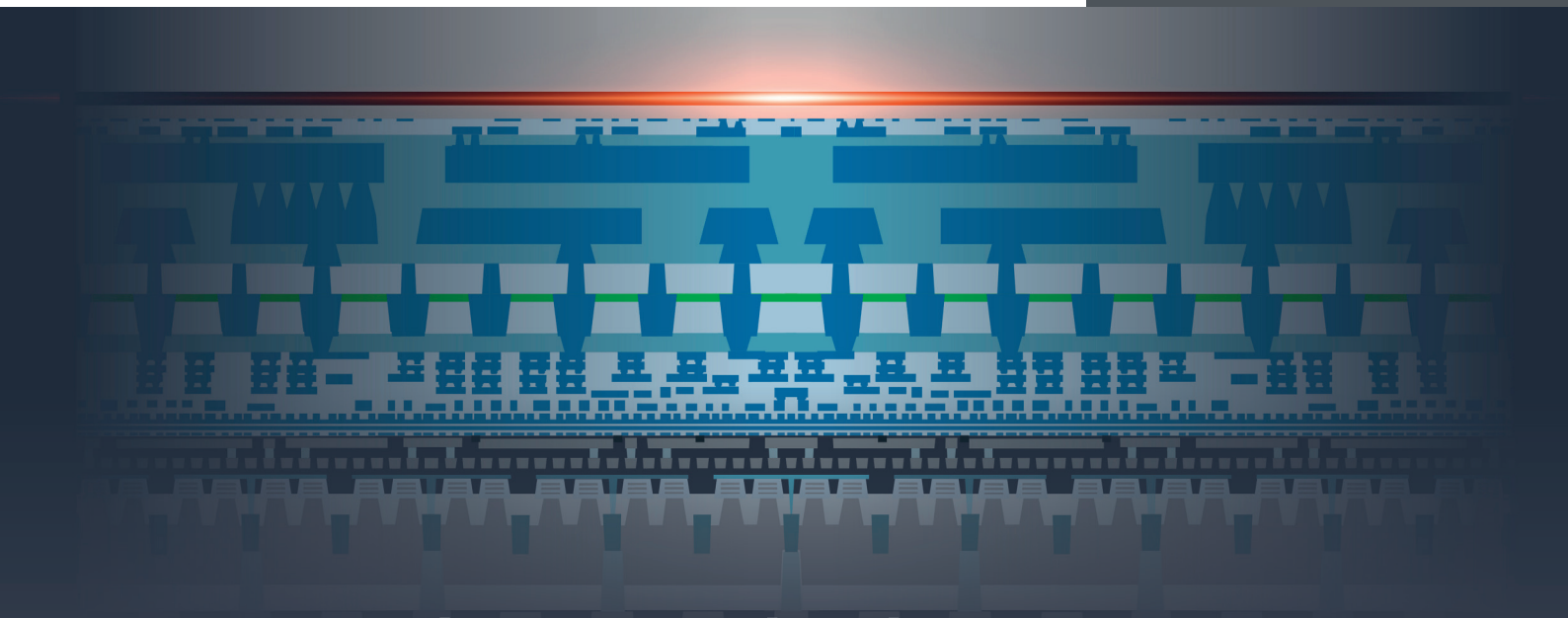

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# Scaling the growth of novel materials

From 4-inch gallium oxide films to next-generation transition metal dichalcogenides, Agnitron's US-driven breakthroughs on large-area wafers are ushering in a new era of semiconductor devices

**BY WILLIAM BRAND, AARON FINE, FIKADU ALEMA, PAUL FABIANO AND ANDREI OSINSKY FROM AGNITRON**

IN THE fledgling days of our industry, production of compound semiconductor devices just involved those based on GaAs and InP. But over a number of decades, our palate has expanded to include a number of new materials with more impressive characteristics. Devices made from GaN are now serving in the optoelectronic, RF and power domains, where they are generating substantial revenues, and SiC is supporting a revolution in mobility. But that's by no means the end of our journey. Now piquing much interest is gallium oxide ($Ga_2O_3$), an ultra-wide bandgap material that promises to deliver unprecedented efficiencies in electrical systems, and transition metal dichalcogenides (TMDs), which could spur advances in electronics, energy storage and sensors.

Helping to usher in a new era for compound semiconductor devices that is driven by the introduction and uptake of $Ga_2O_3$ and TMDs is our company, Agnitron Technology. For nearly a decade, we have been leading the development of advanced MOCVD reactors and processes for high-quality $Ga_2O_3$ and its alloys, and more recently we have been expanding our reach into TMDs. Due to this, our MOCVD systems are now deployed at leading universities and research institutions worldwide, supporting cutting-edge $Ga_2O_3$ and TMD research.

More recently, we focused on scaling our MOCVD technology to support multi-wafer and large-area $Ga_2O_3$ growth. In 2018, we introduced

two new multi-wafer MOCVD platforms, both designed explicitly for $Ga_2O_3$. These reactors feature susceptor rotation speeds up of to 2000 revolutions-per minute (RPM), key to enabling excellent film uniformity and crystal quality. Our Agilis 700 supports wafer loading of up to one 6-inch wafer.

Working with our partners, we have used these platforms to demonstrate record-breaking material performance. Highlights with the Agilis 500 include the growth of $Ga_2O_3$ thin films with exceptional purity and a record low-temperature electron mobility, exceeding 23,000 $cm^2/ V^{-1} s^{-1}$ [1]. Additional triumphs with our Agilis platform are: controllable doping down to low $10^{15}$ $cm^{-3}$, a pre-requisite for drift layers in vertical power devices; and through the optimisation of silicon doping, conductivity values surpassing 2500 S $cm^{-1}$, corresponding to free-carrier concentrations of $3.4 \times 10^{20}$ $cm^{-3}$ [2]. Similar high-doping results have been independently reported by researchers from the Naval Research Laboratory (NRL) on an Agilis 500 tool operating at high rotation speeds [3].

## Innovation in Gas injection: The Agilis 700 platform

We are continuing to pioneer advancements in semiconductor manufacturing equipment, exemplified by our newly redesigned Agilis 700 MOCVD platform. Central to this innovation is a novel gas injection methodology, replacing traditional central-injection and checkerboard patterns with an all new advanced Close-Injection Showerhead approach. By ensuring precisely controlled precursor flows in separated zones directly above the substrate surface, this refinement minimises gas-phase reactions and precursor depletion. The improved control delivers significant gains in uniformity and material quality – critical for large-area wafer deposition, and evidenced by recent preliminary electrical results from pioneering 4-inch $Ga_2O_3$ devices.

The Agilis 700 underscores our commitment to scalability and flexibility, providing a robust platform for both research and production. It supports various substrate configurations, and can accommodate seven 2-inch wafers, a single 4-inch wafer or even a 6-inch wafer, all without compromising growth uniformity or material quality. Sharing core design features with its predecessors – the Agilis 100 (up to 3-inch wafers) and Agilis 500 (up to five 2-inch wafers) – the Agilis 700 bridges the gap between R&D and production, enabling seamless process translation across scales.

As well as providing a range of tools for research, we serve the needs of high-volume manufacturers through our GOX300 platform, an automated, production-focused MOCVD system. This mass-production tool builds on the reactor technology and scalability principles of our Agilis line while incorporating automation and advanced process control that's tailored to industrial semiconductor production. The GOX300 allows manufacturers to access high-throughput, high-uniformity processing, which is essential for commercialising next-generation electronic and optoelectronic devices. We are very active in equipment innovation, with efforts extending further into reactor design, the optimisation of deposition efficiency, and supporting high-performance materials growth across a wide range of semiconductor applications.

## Revolutionising deposition: The RDR reactor

Our proprietary Rotating Disc Reactor (RDR) is the core of our oxide MOCVD systems, including the Agilis 700. With over 16 years of innovation, our engineering legacy can be traced back to early RDR simulations at Sandia and MIT Lincoln Lab. While others with an interest in epitaxy focused on theory, we grasped the RDR's commercial potential – especially for wide and ultra-wide bandgap semiconductors.

This led to a dedicated effort to optimise our RDR for materials like $Ga_2O_3$ and AlN. Significant successes have followed, including the deposition of the highest-purity $Ga_2O_3$ film reported to date, solidifying our leadership in oxide MOCVD. Since 2018, our team and equipment users have contributed to over 250 peer-reviewed publications and conference papers focused on the epitaxial growth and device applications of $Ga_2O_3$.

Key to our success is our patented showerhead design that enables precise flow and thermal stability while preventing unwanted wall deposition – a common shortcoming in traditional systems.

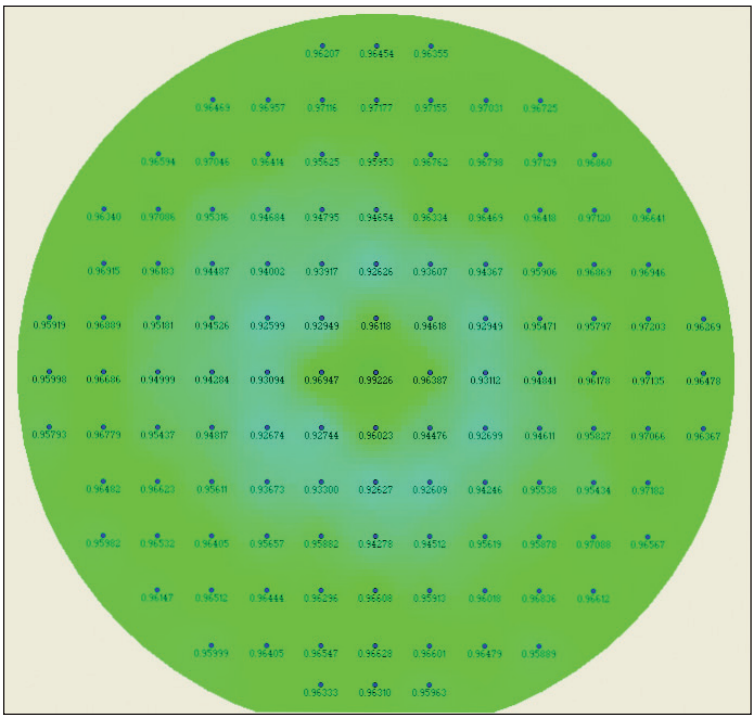
The RDR's dimensionless process equations also allow it to scale easily, from a single 2-inch wafer to 21 x 2-inch configurations and even 12-inch substrates.

As we continue to advance our platform, our domestic innovation and our collaborative partnerships remain central to our mission.

## Scaling $Ga_2O_3$ to 4-inch wafers

Equipping our Agilis 700 reactor with an all-new gas-distribution flange that's optimised for growth of β-$Ga_2O_3$ on large-area substrates ensures the growth of highly uniform epitaxial films. Vital to this optimisation is the support that's come from the Air Force Research Laboratory (AFRL) through the SBIR direct to Phase II program.

For this work, we selected trimethylgallium (TMGa) as the gallium precursor, due to its ability to facilitate faster deposition rates than the more conventional triethylgallium (TEGa), commonly used for $Ga_2O_3$ growth. Our films were grown under the following conditions: 800 °C growth temperature, 25 Torr



➤ Figure 1. Two-dimensional thickness map of $Ga_2O_3$ film grown on a 4-inch sapphire substrate using the Bowtie showerhead. The growth rate was 2 μm/hr, and a 2 mm edge exclusion has been applied during thickness mapping.

chamber pressure, 800 RPM susceptor rotation, and a molar flow for TMGa of approximately 240 μmol $min^{-1}$.

A key concern when using TMGa is the potential for carbon incorporation, introduced during decomposition of the methyl groups. Note that with TEGa, the threat of carbon contamination is avoided, due to different breakdown mechanisms. When we use TMGa, we mitigate the risk of carbon incorporation by maintaining a VI/III ratio above 500 – this condition has been previously identified as the threshold for avoiding carbon incorporation and ensuring film purity. Under these optimised conditions, we reached growth rates of around 2 μm $hr^{-1}$, resulting in films with a thickness of around 1 μm. According to 121-point reflectivity mapping on a 4 inch substrate, thickness non-uniformity is just 1.39 percent. Realising this level of uniformity is essential for the scalability and reliability of $Ga_2O_3$-based devices.

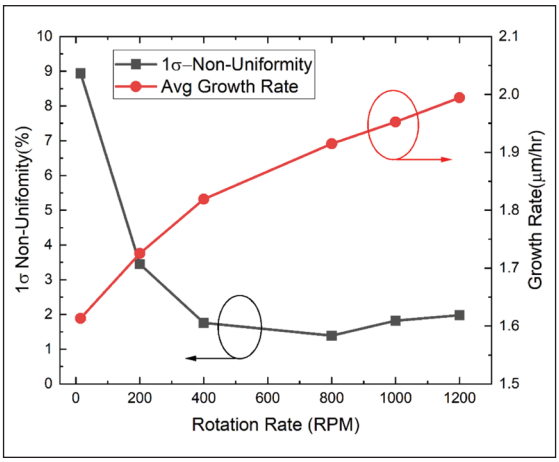
As part of our study into $Ga_2O_3$ thin-film growth on 4-inch substrates, we examined the effect of susceptor rotation speed on growth rate, varying RPMs up to 1200. We identified a clear linear trend between 400 RPM and 1200 RPM, where the growth rate increased from 1.8 μm $hr^{-1}$ to 2.0 μm $hr^{-1}$. This increase is accompanied by little change in thickness non-uniformity, which remained stable across the RPM range. All our samples within this range exhibited a 1σ value of less than 2 percent (the best value, just mentioned, is 1.39 percent, at 800 RPM). However, we found that reducing the RPM below 400 led to a more rapid decrease in growth rate, and a significant increase in non-uniformity. For instance, at 200 RPM, non-uniformity jumps to approximately 3.5 percent, and at 0 RPM, it increases to 9 percent.

These results highlight that with our new gas-injection scheme, it is critical to maintain a high-speed rotation to ensure optimal growth rates and uniformity. The increased non-uniformity at lower RPMs also suggests that slower rotation speeds hinder diffusion of precursors, hampering controlled growth.

Due to the limited availability of native 4-inch $Ga_2O_3$ substrates, we have also investigated the surface morphology and the electrical properties of $Ga_2O_3$ films grown on native 2-inch (010) substrates. For this study, we formed an epitaxial structure consisting of a low-temperature nucleation layer, followed by 200 nm of unintentionally doped material, and a 65 nm silicon-doped layer. This stack is designed for the fabrication of a lateral FET, a common $Ga_2O_3$ device.

Through optimisation of parameters – 800 °C growth temperature, 25 Torr chamber pressure, and 48 μmol $min^{-1}$ TEGa molar flow – we achieved a film thickness non-uniformity of just 0.83 percent. According to Atomic Force Microscopy (AFM), there is a uniformly smooth surface across the 2-inch wafer. Across five mapped locations, 5 μm x 5 μm AFM images show an average root-mean-square roughness of 1.02 nm. We attribute this high level of uniformity to the enhanced gas-injection system, which uses separate injection zones for metalorganic precursors and oxygen. This configuration improves adatom diffusion prior to oxidation, reducing surface roughness and improving film quality.

To assess the electrical properties of our films, one of our partners, Soctera Inc, fabricated Hall-effect pads and capacitors across the wafer. Measuring a



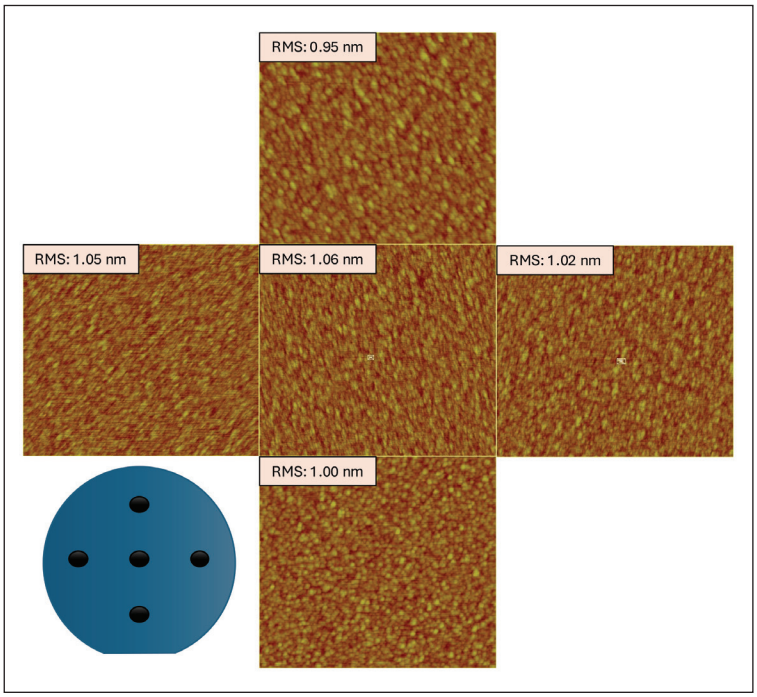

➤ Figure 2. Effect of susceptor rotation speed on film uniformity and growth rate.

total of 22 devices on our 2-inch sample determined an average electron mobility of 138.4 $cm^2 V^{-1} s^{-1}$ and a mobility non-uniformity of 3.8 percent. The highest value recorded for electron mobility was 147 $cm^2 V^{-1} s^{-1}$. Average bulk electron concentration for the devices was 4 x $10^{17}$ $cm^{-3}$. Capacitance-voltage measurements of the channel region indicate a higher electron concentration of 7.3 x $10^{17}$ $cm^{-3}$, with an electron concentration non-uniformity of 8 percent. Using this reactor, a roughly 2 μm-thick unintentionally doped (UID) $Ga_2O_3$ film exhibited high electron mobility (around 179 $cm^2 V^{-1} s^{-1}$ and low carrier concentration ($9.9\times10^{15}$$cm^{-3}$). Further reduction of residual carrier concentration is possible through adjusting the oxygen-to-gallium ratio in the gas phase. These results demonstrate the reactor's capability to grow device-quality epitaxial films with excellent thickness and doping uniformity across a 2-inch wafer.

Through recent experiments, we have developed a process achieving 2.5 x $10^{20}$ $cm^{-3}$ electron concentration and 42 $cm^2 V^{-1} s^{-1}$ electron mobility with RMS roughness values of less than 0.5 nm. In the future, we plan to use this process as an ohmic regrowth for the source and drain terminals in the FETs to greatly improve our contact resistance.

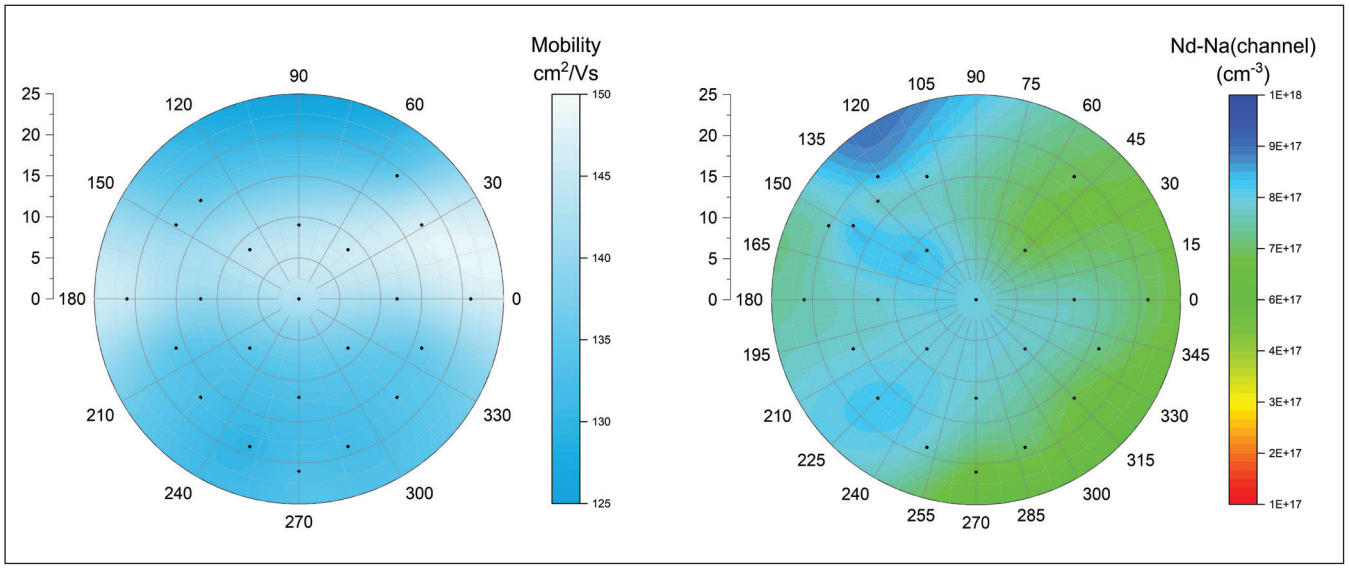
Based on all these measurements of electrical characteristics, we conclude that our films are of excellent quality, with mobility values and electron concentrations that are promising for the future scalability of this growth technology. When larger native substrates become more readily available, this will unleash the promise of this growth method for large-scale device fabrication.

As highlighted in the preceding sections, the Agilis 700 equipped with the new gas-distribution flange has shown outstanding results in film material quality and uniformity. To access another aspect of film growth, we began experimenting with the growth of gallium oxide alloys, specifically aluminum gallium oxide.

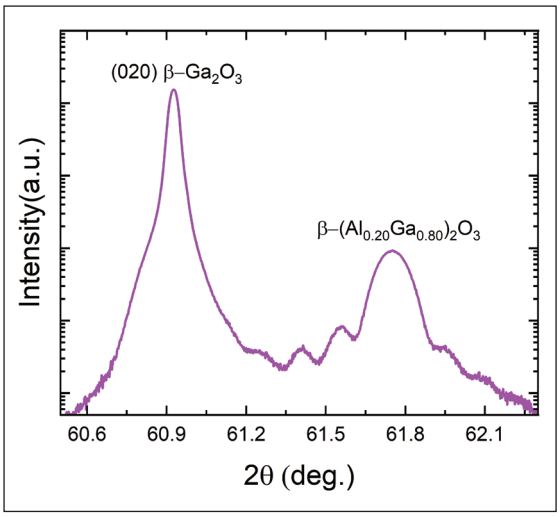



➤ Figure 3. Two-dimensional atomic force microscopy (AFM) images taken from five locations on a roughly 300 nm-thick $Ga_2O_3$ film grown on 2-inch Synoptic substrates using Bowtie Showerhead on the Agilis 700 reactor. The scan area is 5 × 5 $μm^2$.

Using our standard growth conditions, as preciously described, we grew around 70-80 nm of $(Al_xGa_{1-x})_2O_3$ with 100 nm of UID $Ga_2O_3$ on 2-inch *c*-plane Sapphire and (010) β-$Ga_2O_3$ substrate from Synoptics. For our metal-organic aluminum source, triethylaluminum (TEAl) was utilised for these experiments.




➤ Figure 4. Hall mobility (left) and free electron concentration (right) maps for a 65 nm-thick FET channel grown on a roughly 200 nm-thick unintentionally doped $Ga_2O_3$ layer on 2-inch Synoptic (010) β-$Ga_2O_3$ substrates.




➤ Figure 5. X-ray diffraction ω-2θ scan profile for β-$(Al_{0.20}Ga_{0.80})_2O_3/Ga_2O_3$ grown on (010) β-$Ga_2O_3$ Synoptics substrate using Agilis 700 with the improved gas-distribution flange. The thickness of the β-$Al_{0.20}Ga_{0.80}$ layer is 70-80 nm.

The films exhibited an excellent thickness non-uniformity of 1.2 percent over a 2-inch wafer. Surface roughness remained low with an RMS roughness value of 0.8 nm over a 5 μmx 5 μm scan area assessed by AFM. The composition of the $(Al_xGa_{1-x})_2O_3$ was determined to be around 20 percent aluminium using X-ray diffraction and can be seen in Figure 5. The observation of Pendellösung fringes indicate a highly abrupt transition from β-$Ga_2O_3$ to β-$(Al_xGa_{1-x})_2O_3$ and low surface roughness of both β-$Ga_2O_3$ and β-$(Al_xGa_{1-x})_2O_3$ layers. The success of uniform $(Al_xGa_{1-x})_2O_3$ growth expands the capabilities of $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures, enabling the development of epitaxial gate dielectrics and device structures such as HEMTs and MODFETs.

## Advances in TMD growth

Building on our success in scaling ultra-wide bandgap materials, we have made significant progress in expanding scalable growth of two-dimensional (2D) materials, specifically TMDs, through MOCVD. These 2D materials, and particularly TMDs, are poised to revolutionise the electronics, optoelectronics, and quantum technologies.

The general formula for TMDs is $MX_2$: M is a transition metal, such as molybdenum or tungsten; and X is a chalcogen, like sulfur, selenium, or tellurium. Unlike graphene, which lacks a bandgap, many TMDs possess sizeable and tuneable bandgaps, often transitioning from an indirect bandgap in the bulk to a direct one in monolayer form, making them ideal for semiconductor applications. Another strength of these materials is their layered structure, which enables mechanical exfoliation or chemical synthesis into monolayers, characteristics well-suited to nanoscale devices and heterostructures.

Thanks to advances in large-area synthesis techniques for MOCVD, it's now possible to deposit wafer-scale TMD films with sizes of 4 inches and beyond, while ensuring precise control over composition and thickness – this is critical for scalable electronic and optoelectronic device integration. However, there's still work to do with MOCVD. Here, the key challenge is the temperature-dependent interplay between transition metal adatoms' low surface mobility and the chalcogen species' high desorption rate during film growth.

While high growth temperatures are needed to enhance the surface mobility of the metal and improve crystallinity over large areas, they also promote chalcogen desorption (loss), leading to vacancies and defects that compromise material quality.

Chalcogen vacancies also play a key role in determining the phase stability of TMD polymorphs. For instance, in $MoTe_2$, the concentration of tellurium vacancies dictates whether the semiconducting 2H phase forms, or the metallic 1T′ phase. These two phases are markedly different. The 2H phase features a hexagonal structure and exhibits a bandgap transition from indirect (around 0.8 eV in bulk) to direct (around 1.1 eV at the monolayer level), making it suitable for optoelectronic applications. Meanwhile, the 1T′ phase has an orthorhombic structure and metallic conductivity, offering potential for quantum and topological devices. Due to these substantial differences, precise process control during MOCVD is essential for tailoring $MoTe_2$ and other TMD materials to specific applications.

Investing in the growth of TMDs by MOCVD makes much sense, because this technology is well suited to the growth of uniform films on large-area wafers. MOCVD offers tight control over critical parameters such as growth temperature and the chalcogen-to-transition metal flux ratio, which directly affect chalcogen vacancy concentrations and phase formation.

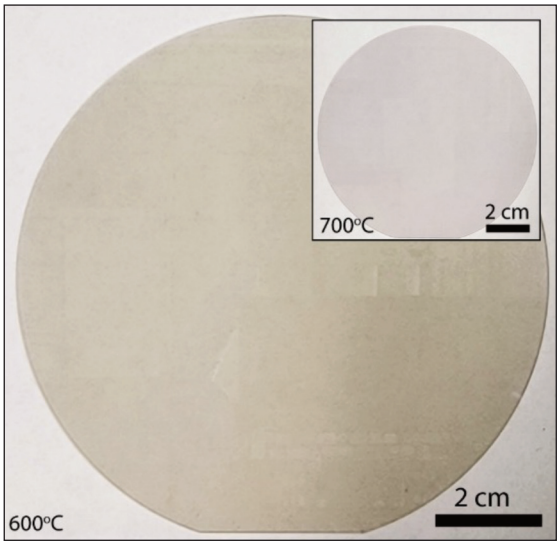
Over the past few years, we have been collaborating closely with Zakaria Y. Al Balushi's team at the University of California, Berkeley, to advance MOCVD growth of TMDs. As part of this effort, we have refurbished and upgraded a high-speed rotating disc MOCVD reactor and supported process development to enable wafer-scale growth.

This partnership has provided new insight into how MOCVD growth conditions influence the uniformity and polymorph phase control of $MoTe_2$ on large-area wafers [4]. $MoTe_2$ films have been deposited using di-isopropyl telluride and molybdenum hexacarbonyl precursors, with hydrogen as the carrier gas. Growth has been conducted on 4-inch *c*-plane sapphire substrates, both bare and coated with ultra-flat hexagonal boron nitride (h-BN) layers, which were developed under the support of the AFRL through the SBIR direct to Phase II program. Nucleation

on bare sapphire has proved challenging, while h-BN/sapphire templates – grown by our team and provided to our partners at Berkeley – have enabled more uniform growth.

Note that we have extensive expertise in MOCVD growth of high-quality 2D h-BN on substrates up to 6 inches in diameter. These h-BN layers have a number of applications, which include serving as ideal templates for GaN or AlGaN/GaN HEMTs, and acting as sacrificial layers for transferring devices onto high-thermal-conductivity substrates, such as diamond [5].

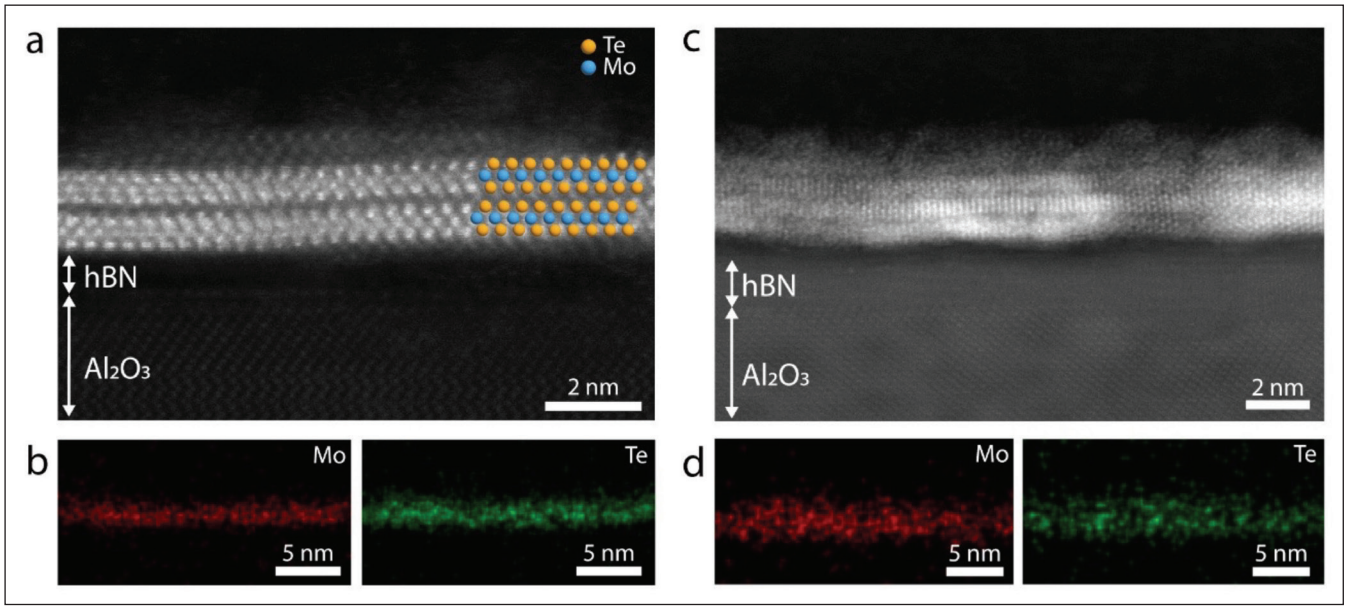
Our collaboration with the team at Berkeley has systematically investigated the effect of growth temperature on the optical properties of $MoTe_2$ thin films, using controlled MOCVD experiments that involve the growth of $MoTe_2$ on 4-inch h-BN/sapphire templates for 30 minutes. We have observed a distinct colour change with growth temperature, shifting from a darker brown at 600 °C (see Figure 6) to a pink hue at 700 °C (see Figure 6, inset), indicating changes in optical properties.




➤ Figure 6. Images of the MOCVD-grown $MoTe_2$ on 4-inch h-BN/sapphire wafers at 600 °C and at 700 °C (inset).

Greater insight into these films has been provided by cross-sectional scanning tunnelling electron microscopy. This technique reveals that $MoTe_2$ films grown at 600 °C exhibit well-crystallised bi- to tri-layers with a uniform molybdenum and tellurium distribution (see Figure 7 (a) and (b)). In contrast, growth at 700 °C produces non-uniform 1T′-phase layers with poor contrast in transmission electron microscopy images and signs of oxidation (see Figure 7 (c) and 7 (d)), despite consistent elemental distribution. The most probable cause of this degradation is the greater chemical reactivity and instability of the 1T′ phase.

These findings emphasise the critical role of temperature-induced tellurium vacancies in determining phase stability. In addition, they underscore the need for precise thermal control during MOCVD to tailor $MoTe_2$ for specific device applications. (For a more detailed analysis of these results, see the paper by B. J. Kim *et al*. ACS Nanoscience Au **5** 1 (2025)).




➤ Figure 7. (a) Cross-sectional transmission electron microscopy image of 2H-phase $MoTe_2$ grown at 600 °C, showing a well-defined layered structure, and (b) the corresponding energy-dispersive X-ray spectroscopy maps confirming uniform elemental distribution of molybdenum and tellurium. (c) Cross-sectional transmission electron microscopy image of 1T′-phase $MoTe_2$ grown at 700 °C, revealing nonuniform layer formation and (d) energy-dispersive X-ray spectroscopy maps for the 1T′-phase sample, showing consistent distribution of molybdenum and tellurium despite structural irregularities.

Building upon these foundational research achievements, we have invested in significant equipment innovations to enable large-area wafer processing.

## Driving innovation through collaboration

Unlike our European counterparts, our growth is rooted in US-based partnerships and funding – particularly through the Air Force Research Laboratory (AFRL) and the Office of Naval Research (ONR) through the SBIR programs. These collaborations strengthen America's domestic semiconductor infrastructure, and position Agnitron as a key contributor to national R&D and manufacturing efforts.

Looking ahead, we will continue delivering advanced MOCVD systems like the Agilis 700 to leading semiconductor hubs across the US and worldwide.

Built on innovation and technical excellence, we offer flexible tools for processing ultra-wide-bandgap semiconductors, III-nitrides, SiC, 2D materials, and oxides. Our systems are trusted by research institutions, government labs, and industry leaders alike.

From pioneering gas injection methodologies and RDR design to enabling the first release of electrical results from a 2-inch $Ga_2O_3$ device growth using a large scale reactor, we remain committed to enabling next-generation semiconductor breakthroughs – through responsive engineering, specialty materials expertise, and US-based manufacturing.

**Acknowledgement:** *The work discussed here was primarily funded by the Air Force Research Laboratory (AFRL) through the Direct to Phase II SBIR program (Contract No. FA239423CB010), under the direction of Dr. Adam T. Neal.*

*Agnitron also acknowledges support from the Office of Naval Research (ONR) through the STTR Phase II program (Contract No. N6833518C0192), under the direction of Mr. LJ Petersen. Agnitron would also like to acknowledge Prof. Travis Anderson of the University of Florida for conducting Hall measurements on our samples*

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## Testimonial from Silanna Semiconductor

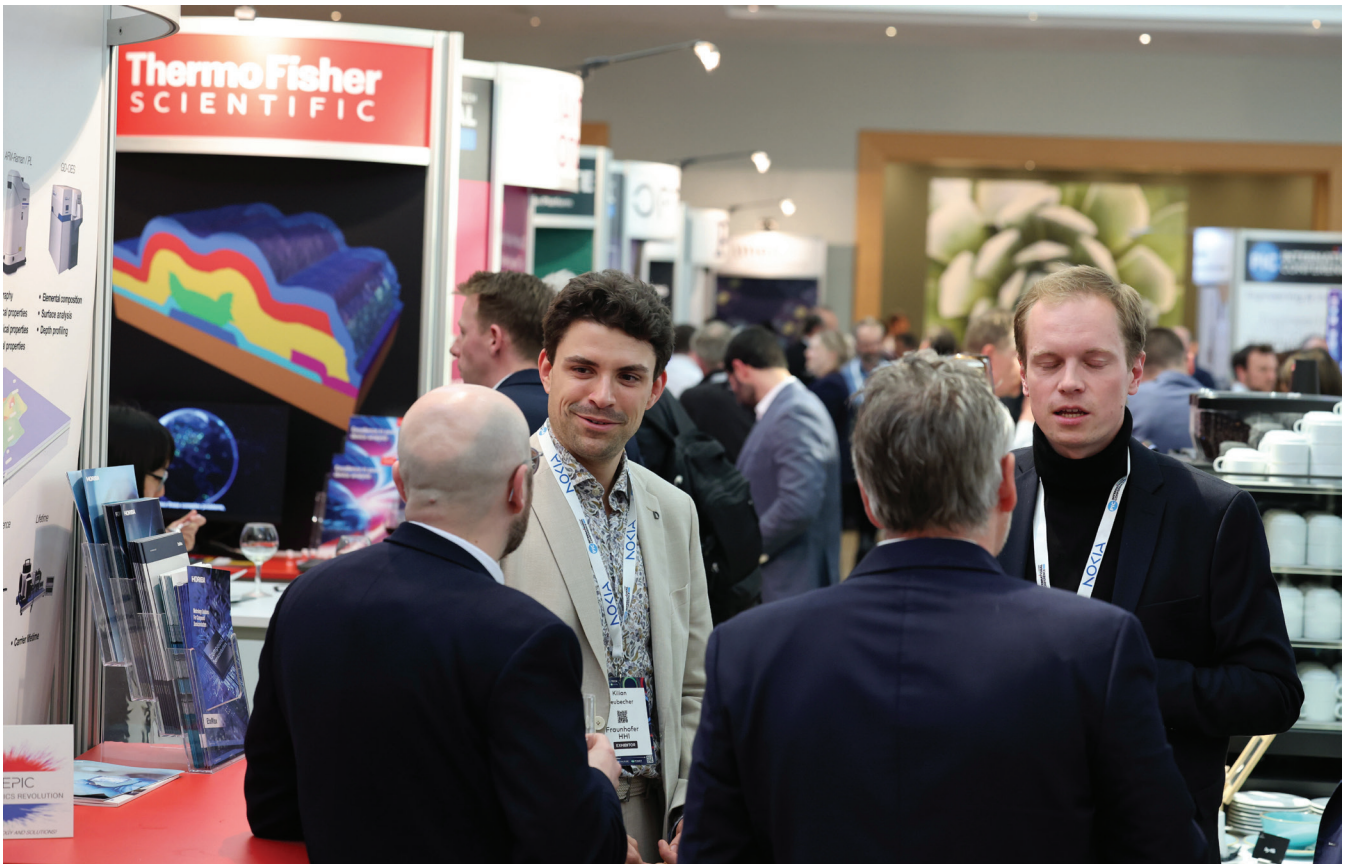
Silanna selected MOCVD and, specifically, the AGILIS MOCVD system for GOSiC development due to its unmatched precision, scalability, and proven industry acceptance for high-volume epitaxy. MOCVD enables the growth of high-quality $Ga_2O_3$ films with excellent crystal integrity and precise doping control – both critical for the vertical conduction architecture at the heart of GOSiC power devices.

The AGILIS platform's design supports scalability to 6-inch and 8-inch substrates, providing a seamless pathway from R&D to high-volume manufacturing of GOSiC wafers for automotive, industrial, and energy markets.

## Testimonial from Professor Zakaria Y. Al Balushi, University of California, Berkeley

Agnitron has played a pivotal role in enabling our lab's efforts to scale MOCVD growth of $MoTe_2$ and other TMDs to large-area wafers.

Their engineering support and customized reactor platforms have been key to our success in controlling phase formation and improving film uniformity. I view TMDs as a cornerstone for the future of 2D optoelectronics and quantum devices, and Agnitron continues to be a valuable partner in advancing this frontier.




# CS International champions the versatility of the nitrides

The portfolio of devices based on GaN continues to strengthen and expand, with recent key additions including polychromatic and nanowire microLEDs, VCSELs with improved efficiency, and GaN HEMTs for power electronics that are targeting new markets

**BY RICHARD STREVENSON, EDITOR, CS MAGAZINE**

THROUGHOUT the life of this publication, we have been covering major developments in GaN devices. In our very first issue, out 30 years ago, the cover story had the tagline *Blue and Green: Commercial applications of short-wavelength light-emitting diodes*. Within a few months, these fledgling GaN LEDs had been joined by laser diodes, thanks to another triumph of Shuji Nakamura. And over the last three decades the GaN device portfolio has mushroomed, with the introduction of microLEDs, VCSELs, and power and RF devices.

This year's CS International, held in Brussels on the 8th and 9th of April, captured the breadth and progress of GaN, with presentations detailing advances on a number of fronts. Amongst these many talks, speakers from Q-Pixel, Porotech and Aledia described progress in microLED technology, which is promising to revolutionise displays; while advances in GaN-based VCSEL production were outlined by Tetsuya Takeuchi from Meijo University; and Roberto Crisafell from STMicroelectronics spoke about his company's progress in GaN power devices.

## Maintaining microLED momentum

It's probably fair to say that the microLED is no longer a new kid on the block. For a number of years there has been much interest in commercialising this device for a wide variety of displays, from smartwatches and VR/AR headsets to smartphones, automotive head-up displays and TVs. In many of these applications, holding back commercialisation are challenges associated with forming closely packed red, green and blue pixels with a sufficient yield, precision and throughout to ensure acceptable production costs.

One promising solution to these challenges is the polychromatic pixel, a technology that's been developed by both Q-Pixel and Porotech.

Speaking on behalf of Q-Pixel at CS International, company CTO Michelle Chen remarked on the great opportunity provided by the display industry, as well as the lack of progress in microLED technology. She put the latter issue into perspective by pointing out that while the display industry is worth around $168 billion, revenue for today's microLED industry is less than 0.5 percent of that figure.

It should be noted that the lack of success is not due to a lack of interest. "Major consumer electronics, including Apple, Meta, Samsung, LG, Sony and more, are all working on microLED technology," explained Chen, who added that so far there's little to show for this. Samsung has a microLED TV on the market, but it retails for $150,000, and despite much investment, Apple has not introduced a microLED smartwatch.

Money is going to keep flowing into microLED technology, says Chen, who reported that over $12 billion has already been invested in research and development, a figure forecast to climb to $35 billion by 2030. "The reason that industry keeps throwing money at this problem is that they see that the customer market is huge."

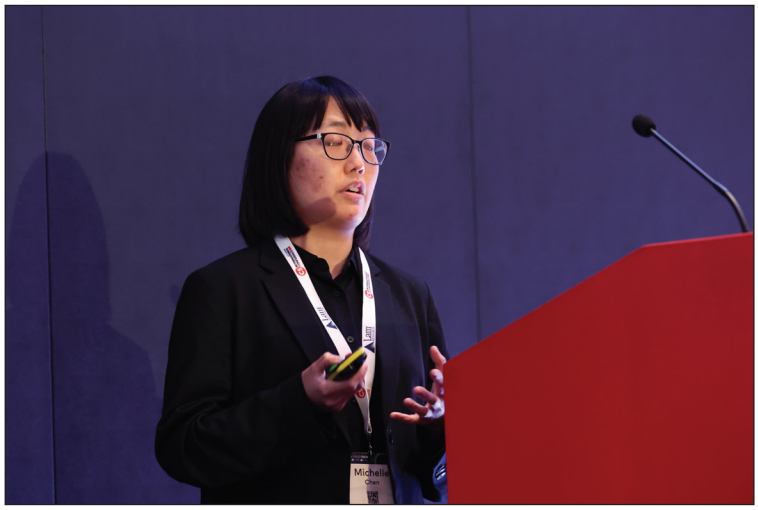
Helping to drive all this investment is that, from a physics perspective, the microLED is an ideal source for displays. "As far as the physical advantages [of the microLED], there's the brightness, lifetime, energy efficiency, and general robustness against ambient air," championed Chen, who explained that the biggest challenge is the high-cost, due to complex assembly.

"This is really deeply rooted in the way full-colour displays have been made for a full colour range," remarked Chen, who explained that this often involves red, green and blue subpixels from more than one material system, and the use of separate wafers for different colours prior to packaging.

Many developers of microLED technology are targeting the AR/VR market. According to Chen, success in this sector demands a very-high-resolution, needed to avoid what's known as the 'screen-door' effect – it's the occurrence of thin, dark lines or a mesh, caused by gaps between the pixels on a screen.

Having some success in this market is the Apple Vision Pro, which is based on microOLEDs. The resolution is high, reaching 3,400 pixels per inch, but the retail price is a concern – it's over $3,000 – and power consumption is around 30 watts, met with a cumbersome battery pack that adds weight.

Chen argued that Q-Pixel's technology is an attractive alternative to microOLEDs in this application. She explained that the company's colour-tuneable polychromatic pixels can replace red, green and blue sub-pixels, leading to substantial cost savings.



➤ Q-Pixel's CTO Michelle Chen described the company's polychromatic microLEDs that could simplify the production of AR displays.

"What we have is a single monolithic growth that is fully colour tuneable. It simplifies assembly a lot and it allows us to make very high-resolution displays," explained Chen, who added: "The colour is tuned from red to blue by applying different electrical currents or voltages. This is a very industry compatible process. We don't use any subpixels, there's no regrowth, quantum dots, colour filters or polarisers."

By adopting this approach, Q-Pixel is able to use standard material, substrates and structures, as well as industry-standard tools that are said to enable ease of integration and rapid, large-scale deployment.

Another strength of the company's technology, according to Chen, is the small difference in voltage required to adjust the colour from red to blue. "This is very good from a systems perspective, because it's more suitable for use with display drivers that are already on the market."

Q-Pixel has already enjoyed notable success. "We have state-of-the-art red GaN brightness, and very low power consumption, less than 0.5 nanowatts per pixel when we're operating in the green regime," claimed Chen, who added that the company has produced prototype passive displays with up to 10,000 pixels-per-inch, and has the world-record for active displays, 6,800 pixels per inch.

Opportunities are also being explored for the company's tuneable pixels in wearables in the health market, and also in automotive displays, where Chen claims microLEDs are a big contender. "Right now, current technologies simply don't have the lifetime or robustness to last the lifetime of a car – but microLEDs can do that."

With a brightness that's orders of magnitude higher than what's possible with OLEDs, Chen believes that microLEDs are also 'perfect' for transparent displays that could be used outdoors.

"Again, the big bottleneck so far has not been the physics, it has been the cost," says Chen. "How do

we make these large-area displays at a reasonable price that people would want to spend money on?"

Q-Pixel has a solution, called Q-transfer, that is said to overcome the mass-transfer bottleneck. "This is our patented technology, enabled by the fact that we're able to use this fully tuneable pixel. Not only is our resolution going to be higher, by virtue of the fact that we're not dealing with sub-pixels, but because we're only dealing with one kind of pixel, we can up the transfer speed and have higher throughput."

One issue with all forms of display is that they require an incredibly high degree of perfection, because the human eye is so critical of dud pixels. While with some approaches, repair and replace is needed, that's not the case with colour tuneable pixels. "If we have to adjust the wavelength, we can actually tune that electrically because we have this tuning capability."

This feature may allow the microLED TV to become a reality for many. "Right now, you can buy a microLED TV, if you have $150,000 to spare, but we want to reduce that cost down by two orders of magnitude. And with our technology, we think it can be done," argued Chen.

## Porous polychromatic technology

Offering technologies that include one that's a similar approach to that of Q-Pixel, as well as the use of porous GaN material and monochrome microLEDs, is the University of Cambridge spin-off Porotech. Speaking on its behalf at CS International, VP Display & Head of Taiwan, Kunal Kashyap, discussed the strengths of the company's technology, and its roadmap.

Established in 2020, Porotech has raised over $33 million, with Foxconn and GIS major shareholders. The company now has over 150 patents, spanning materials to optical modules; and employs more than 50 staff, located at either the UK headquarters and material lab, or at the R&D centre and production line in Taiwan.

Porotech has three core technologies. There's porous GaN, allowing a tailoring of some critical properties of GaN; native monochrome single colours that span the entire visible range with the InGaN material system; and what's referred to as Dynamic Pixel Tuning, which allows a microLED to emit any colour from the blue to the infrared.

Commenting on the latter, Kashyap remarked: "There are some trade-offs, which we are working on. But this is the holy grail technology."

Initially, Porotech employed sapphire for the production of its microLEDs, but it has now switched to 8-inch silicon, as this is compatible with CMOS technology.

The company is working with a number of partners in Taiwan. Together they have created the world's first hybrid bonding microLED ecosystem. EpiLEDs produces epitaxial wafers, pixelation is provided by PSMC, and Foxconn undertakes the hybrid bonding step. From here, Porotech's product is sent on to Rayprus, to carry out back-end and flip-chip processes and produce a light engine. Completing the supply chain is GiS, offering waveguide and lamination services, and Foxconn subsidiary Jorjin Technologies, which is able to produce AR glass.

Working with these partners, Porotech is able to mass produce displays with pixels sizes of just 1.5 μm and 1.25 μm. These emitters are united with drive electronics using hybrid bonding, which is said to combine a high accuracy and a high yield with low die loss and high reliability. While pick-and-place and mass transfer has an accuracy of up to around 0.5 μm, according to Kashyap, with hybrid bonding an accuracy of 0.2 μm is the starting point.

The company's first product, a microdisplay panel with a VGA platform and a pixel pitch of 3.75 μm, will enter high-volume production at the start of 2026. During summer 2026, this will be joined by Porotech's second-generation technology, an SVGA format with a 2.5 μm pitch. And before the year is out, Gen 2+ will be in high-volume production, featuring resonant-cavity microLEDs. Providing


➤ Porotech is working with many partners in Taiwan. Together, they have created a supply chain for AR displays based on the microLED.

collimated emission, this class of microLED improves coupling into the light engine, and enables a four-fold gain in efficiency at the system level.

Looking further ahead, Porotech plans to introduce its dynamic pixel tuning technology in 2027. This is already capable of spanning the visible spectrum, but prior to commercialisation, there needs to be an increase in brightness in the deep red.

## An edge from nanowires?

Also competing for success in the microLED sector is French chipmaker Aledia, which spun-out from CEA-Leti in 2012, and has spent the last two years building a manufacturing line in Grenoble that houses €200 million of production equipment. Today this pioneer of nanowire microLEDs employs 200 staff, with the majority in Grenoble and a handful in Shenzhen. Aledia has over 1,000 patents and more than 300 patent families, and it has raised more than €500 million.

Speaking on behalf of the company at this year's CS International, Head of Technology and Device Engineering Pierre Tchoulfian explained that Aledia is currently using 200 mm silicon as the foundation for its technology, with nanowires grown by MOCVD. However, scaling to 300 mm wafers is planned, with the company having demonstrated the capability to do so five years ago.

Throughout the remainder of this decade Aledia will be ramping its production capacity. In its 3,000 $m^2$ cleanroom, it will be capable of running 100 wafers per week through its lines in 2027, increasing to 500 in 2030, with CMOS-like yields, says Tchoulfian. "But we have the room and the space to go to 3,000, if the market needs that."

Tchoulfian touched on a number of issues that the emerging microLED industry is grappling with. They include: the reduction in the efficiency of this emitter with shrinking a microLED to a few microns in size; the lack of stability of red emission with current and temperature; mass transfer with a high yield and throughput; and the use of a flip-chip geometry that has two contacts on the same side of the device, when it's preferable to have a top and a bottom contact.


➤ Pierre Tchoulfian, Head of Technology and Device Engineering at the Aledia, explained how the company's nanowire technology addresses many of the issues of conventional microLEDs.

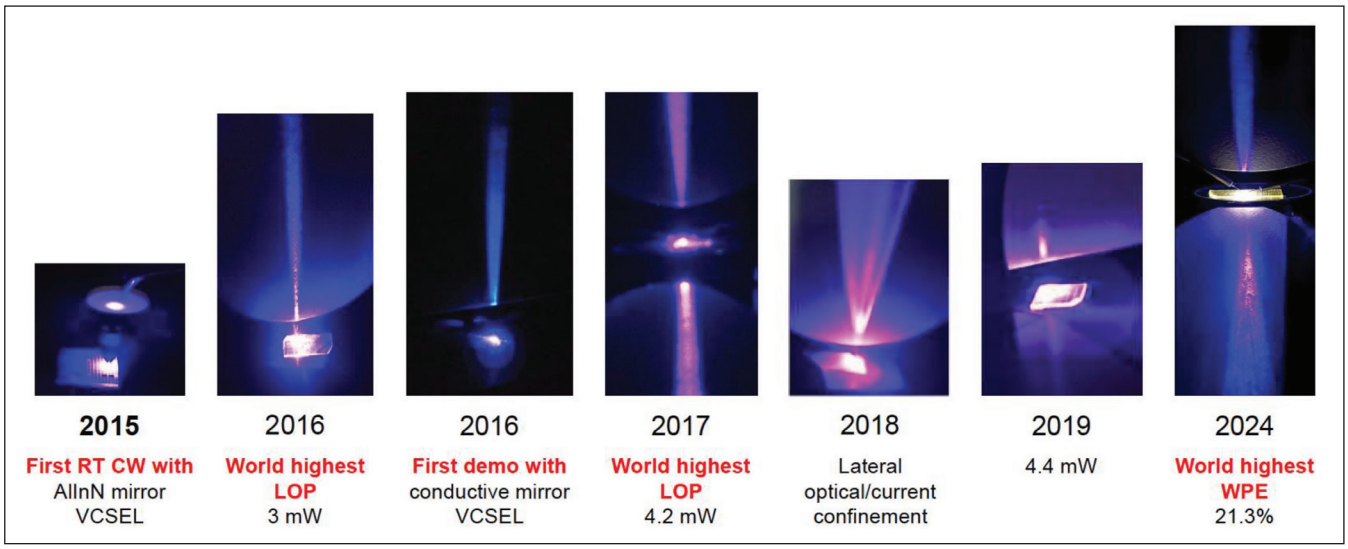
Addressing many of these concerns is Aledia's nanowire approach that produces blue microLEDs with an external quantum efficiency of 40 percent, for device sizes below 5 µm. Thanks to a favourable contact architecture, two microLEDs can be arranged in series and driven at 6 V or 9 V, enabling a 30 percent power saving at the panel level.

Drawing on a report from market analyst Yole, Tchoulfian claimed that by 2030 sales of AR headsets will total 25-30 million, with microLEDs accounting for around a 50 percent share. However, to enjoy that success, he argued that there's a need to succeed on three fronts, related to power consumption, cost and brightness.

These requirements are inter-related. "You want the glasses to be 30 to 50 grams, and the display to be efficient," said Tchoulfian, who pointed out that nanowires are a solution, benefitting from a photonic effect that enhances light extraction.

When it comes to cost, Tchoulfian believes that the full-colour displays for the glasses must be no more than $100. He sees epitaxy on 8-inch wafers and ultimately 12-inch wafers as the solution, with Aledia

Aledia's nanowire approach produces blue microLEDs with an external quantum efficiency of 40 percent, for device sizes below 5 µm. Thanks to a favourable contact architecture, two microLEDs can be arranged in series and driven at 6 V or 9 V, enabling a 30 percent power saving at the panel level




➤ Setting many milestone over many years, Tetsuya Takeuchi's group from Meijo University are pioneers of the GaN-based VCSEL.

providing 'mono-colour' panels of red, green and blue, with the wavelength controlled by the degree of indium incorporation.

## Improving the GaN VCSEL

Of all the mainstream light-emitting GaN-based devices, the VCSEL is the least mature by a considerable margin. Its Achilles' heel is its mirrors. Unlike the GaAs VCSEL, where it's relatively easy to produce a distributed Bragg reflector from the pairing of GaAs and AlGaAs, a combination with very similar lattice constants, there is no obvious nitride-based combination for making the mirrors. Due to this, developers of this device often turn to one or even two dielectric mirrors, and various approaches to fine-tune the thickness of the cavity.

One promising option in the latter regard, detailed by Tetsuya Takeuchi from Meijo University, involves the introduction of *in-situ* cavity control.

Describing this refinement to delegates at CS International, Takeuchi claimed that *in-situ* cavity control is the third key advance in the GaN VCSEL fabrication process that has delivered a substantial increase in wall-plug efficiency, following in the footsteps of the development of a high-quality AlInN/GaN mirror and lateral confinement of the current and the optical modes.

Takeuchi explained that day-to-day variations in growth rate can be ± 2 percent, leading to unacceptable mirror losses. What's needed is to ensure that this deviation is no more than 0.3 percent. "That's why we installed the in-situ reflectivity spectrum measurement system from Laytec," remarked Takeuchi.

With this tool, Takeuchi and co-workers collect wavelength spectral data, and a reflectivity intensity profile as a function of thickness. Drawing on all this information, the team has produced GaN VCSELs that benefit from very small deviations between the lasing wavelength and the centre wavelength for the distributed Bragg reflector. Lasers emitting at 420 nm produced 15 mW, and had a wall-plug efficiency of 21 percent. "I think this is still in the world's highest number," remarked Takeuchi.

## The rise of GaN power electronics

While GaN optoelectronics and RF electronics are well-established markets that have existed for decades, significant sales of GaN power electronics are relatively new. Power supplies for mobile devices provided the first killer application, and now companies are looking to find new markets that will benefit from the introduction of this wide bandgap semiconductor – it enables higher efficiencies, far higher power densities, speedy switching, smaller units and the absence of reverse losses.

At CS International, Roberto Crisafulli, Director of the GaN and RF Business Unit at STMicroelectronics, spoke about two of the biggest opportunities for GaN that will help to increase annual revenue to around $2 billion by 2030: data centres and electric vehicles.

Crisafulli highlighted the importance of increasing energy efficiency in data centres, pointing out that this year their energy consumption is expected to total 250 TW-hours, and is tipped to double in the next few years.

"A key performance indicator is the so-called power-usage effectiveness, which is a metric to measure how much of the power fed to a data centre is really consumed by the IT infrastructure," remarked Crisafulli. "Here we are still far from parity. The estimated average in 2025 is 1.3. It means that for every watt consumed to generate a digital response, there are still 300 milliwatts lost because of maintenance, because of cooling, because of

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- Agnitron provides high-quality material growth demonstration with system installation
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- System easily switches between remote (RIS) and close injection showerheads (CIS), both featuring a patented gas distribution flange for unmatched reactor design flexibility
- Ultra-compact and field-upgradable, one system can be reconfigured for dual use of both oxides and nitrides
- High-temperature delivery (+150°C) for low vapor
- In-situ UV exposure direct on wafer during growth
- Dual-wavelength pyrometer for accurate measurement and closed loop temperature control
- Ideal for advanced device growth, including UV LEDs, HEMTs, LDs, MQWs, SLs, power electronic devices, and 2-D materials
- Integrated UV/Blue reflectometry measuring in-situ growth rate and thickness. Analysis by AgniTemp software

Details on our website: **www.agnitron.com**

The Agilis mini is best suited to grow high quality β-$Ga_2O_3$, AlN, AlGaN, GaN, InGaN, NbN, III-V As/P alloys, MgZnO, ZnO, II-IV compounds; transition metal dichalcogenides (TMD), such as $MoS_2$, $MoSe_2$, $WS_2$, $WSe_2$; $Bi_2O_2Se$, Phosphorene, two-dimensional hexagonal BN, SiC, ScAlN, and YAlN.

agnitron technology

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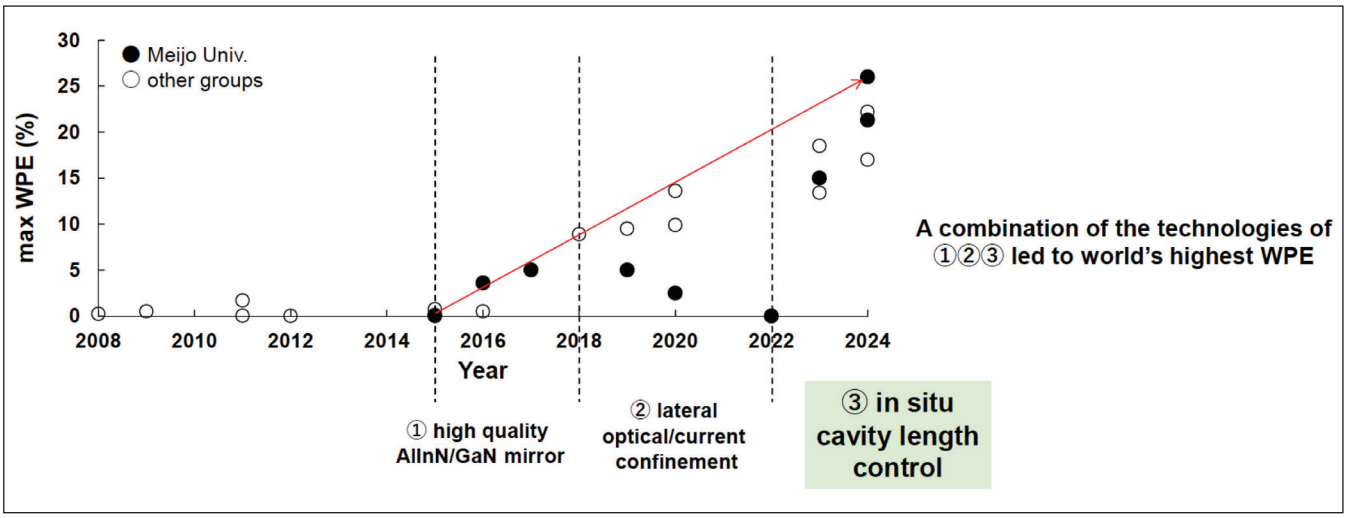



➤ At Meijo University, the most recent key breakthrough to improving the performance of the GaN-based VCSEL has been the introduction of in-situ cavity length control.

auxiliary functions." According to Crisafulli, these losses provide wideband materials in general, and GaN in particular, a great opportunity to help to achieve a target of parity.

He explained that data centres are undergoing tremendous change. The growth of AI is driving the replacement of uninterruptable power supplies with battery back-up units that will enable the integration of renewable energies into data centre power infrastructure. In addition, air-based cooling is being replaced with liquid-based variants.

Amongst these changes, power supply units are having to deliver far more power, due to the emergence of AI data and AI servers. Supplies of 1.2 kW and 1.5 kW are being replaced with more powerful variants, capable of delivering up to 12 kW.


➤ Roberto Crisafulli, Director of the GaN and RF Business Unit at STMicroelectronics, sees opportunities for this material in data centres, motor drives and electric vehicles.

"The total energy in the rack, which used to be in the range of 15 kilowatts, is now in reality already approaching 50 kilowatts, and this will rise and continue to rise up to 300 kilowatts until the end of the decade," explained Crisafulli, who added that these higher powers are accompanied by a change in circuit topologies, and the way power is distributed in the system.

Crisafulli predicts that GaN will have a role to play here, enabling efficiencies to exceed 97 percent. Advances will also come from new circuit designs that incorporate this wide bandgap technology.

Within the electric vehicle market, Crisafulli sees an opportunity in the on-board charger, with GaN enabling the introduction of single-stage AC-to-DC converters that simplify the structure and trim costs. GaN may also win deployment in the traction inverter, and in local DC conversion.

GaN could also help to curb the global carbon dioxide footprint by improving the energy of motor drives. These drives, ignoring those associated with electric vehicles, account for about 30 percent of the world's electrical energy consumption, and efficiencies are far from what's possible.

There's no doubt that the ST spokesman has an optimistic view for GaN, which he argues is on the verge of reaching more and more critical milestones in its adoption across various markets. "Partnerships to ramp-up production, to establish a resilient supply chain, is really key," said Crisafulli, adding: "The achievement of cost and quality parity with silicon is really within reach."

Thanks to progress of GaN on so many fronts, this material will surely be at the forefront of the CS industry for many years to come. And it will certainly take centre stage at the next CS International, to be held on 21-22 April, 2026.


# A tough 12 months for CS shares

Aside from a couple of makers of optical components, shares of companies in the CS industry have headed south over the last year

**BY RICHARD STEVENSON, EDITOR, CS MAGAZINE**

WITHIN OUR INDUSTRY, we know a great deal about the impact of our actions on the tasks in hand. We understand how molecular flow rates, pressure and temperature influence the growth of epilayers, and how changes to the architecture of LEDs, lasers and power devices alter their performance.

What's far harder to fathom – and impossible to know for sure – is the degree of influence of various forces on the share price of compound semiconductor companies, which have tended to suffer from a fall in valuation over the last 12 months. While the tariffs introduced by the White House have dragged down valuations, they are by no means the only headwind to share prices within our industry, with a softening of the growth in the electric vehicle market also having a significant impact.

Note, though, that not every company on this year's *Compound Semiconductor Shareprice Leaderboard* has seen its share price fall in the 12 months running up to the end of April 2025. Bucking that trend are a couple of companies that produce optical components: in pole position is Lumentum, which has enjoyed an increase in share price over the last year of almost 40 percent; while second-placed Coherent has a valuation that has climbed by nearly 20 percent.

Lumentum's share price has soared from around $40 throughout autumn 2024, and by late January it had hit just over $100, before falling back to around $60.

In an upbeat call on 7 November 2024 to discuss the first fiscal quarter 2025 results that went down well with investors and appeared to spur a climb in share price, the company CEO at that time, Alan Lowe, delighted in a revenue exceeding guidance. Sales for that fiscal quarter came in at $336.9 million.

During that call Lowe remarked: "We set a new record for datacom laser chip orders, including 200-gig EML (electro-modulated) laser chips, reflecting strong demand from multiple customers, including an AI infrastructure customer. Based on expanding cloud demand and improving trends in the broader networking market, we expect double-digit sequential revenue growth in the second quarter."

According to Lowe, another highlight from that fiscal quarter was the expansion and diversification of the company's cloud and AI business.

During those three months Lumentum secured a new hyperscale transceiver customer, which will provide volume shipments this year.

Lowe and his team are implementing a three-pronged strategy to grow Lumentum's cloud data centre business. Efforts are focused on: expanding cloud and AI customer opportunities at the component and transceiver levels, as customers migrate to higher speeds; scaling significant production capacity for components and transceivers outside China; and advancing differentiated technology roadmaps, to ensure that customers can scale future generations of cloud and AI data centre architectures to higher compute capacities in a more cost-effective, power-efficient manner.

Discussing each of these in turn, Lowe began by arguing that during a transition to higher speeds, Lumentum's technology becomes increasingly valuable.

"In the coming year, the transition to 200G lane speeds will drive growth and increase the importance of single-mode optics and indium phosphide laser transmitters," remarked Lowe, adding: "Our indium phosphide EML transmitters have established a strong reputation for high performance, high quality, and reliability. Underscoring this, our 100G EMLs are currently shipping in high volumes to a wide range of optical transceiver suppliers for use in leading-edge, single-mode 400G, and more importantly, 800G, optical transceivers."

Progress on the second prong – expanding manufacturing capacity at established Lumentum facilities outside China – is viewed as essential to ensuring a secure, reliable supply chain for cloud and AI customers.

Commenting on this goal, Lowe said: "We are on track to increase EML production capacity by 40 percent in Q4 of fiscal 2025, compared to our capacity in Q4 of fiscal 2024. This expansion will help alleviate the industry-wide shortage of indium phosphide capacity."

Lumentum's third prong of its cloud and AI strategy is to deliver innovative technologies to address the escalating challenges of scaling data centre compute capacity.

"We are collaborating with leading-edge customers to develop breakthrough solutions to enable higher data link capacities with enhanced energy efficiency that will support their multi-year cloud and AI infrastructure roadmaps," said Lowe.

He added that Lumentum had started to ramp 200G laser chips, and was working closely with its customer on future generations of higher speed optical links, as well as new architectures, including co-packaged optics, that will require unique ultra-high-power lasers.

"Our advanced indium phosphide and photonic integrated circuit capabilities are essential for meeting these upcoming demands. While we don't expect the deployment of these technologies to start until our fiscal 2026, we are actively collaborating with customers to shape the future of optical technology."

Lowe updated investors in a call discussing second fiscal quarter 2025 earnings on 6 February, the day before he handed over the reins to Michael Hurlston.

For that quarter Lumentum exceeded its guidance, with sales netting $402.2 million. The company would also have been encouraged by its improving operating margin, up 490 basis points sequentially and 600 basis points year-on-year.

"This level of performance was driven by robust demand from cloud customers, both inside the data centres as well as interconnecting data centres, along with an overall improving networking market," remarked Lowe.

Around the time of the call, the AI technology from China, DeepSeek, had been grabbing headlines in mainstream media. Commenting on this, Lowe argued: "Discussions with cloud customers reinforce that advancements in software efficiency are key to the long-term viability of the AI business model, just as efficiency gains in optical data transmission are essential for enabling AI in data centres. These reports on improved efficiencies highlight a positive trend that strengthens the AI market for both our customers and our business."

Offering an update on its transceiver capacity expansion, Lowe said progress is on-track. "Complementing our existing production lines in Thailand, construction of our large new three-story facility and clean room on the same campus is well underway, with the first floor completed and ready for tool installation."

During the second fiscal quarter, 2025, Lumentum broke its record for EML

*Compound Semiconductor* Shareprice Leaderboard

| Rank | Company | Ticker | Share value, April 26, 2024 ($) | Share value, April 25, 2025 ($)2 | % appreciation | Change in Rank |
|---|---|---|---|---|---|---|
| 1 | Lumentum | LITE | 42.16 | 58.82 | 39.5 | +8 |
| 2 | Coherent | COHR | 53.13 | 63.02 | 18.6 | +1 |
| 3 | NASDAQ composite | IXIC | 15821.34 | 17182.11 | 8.6 | +1 |
| 4 | Riber (Paris) | RIB | 3.15* | 2.91* | -7.9 | +1 |
| 5 | ams OSRAM | AMS.SW | 1.12* | 8.16*† | -27.1 | +10 |
| 6 | IPG Photonics | IPGP | 88.24 | 57.05 | -35.3 | +6 |
| 7 | WIN Semiconductor (Taipei) | 3015.TWO | 4.43* | 2.68* | -39.5 | +6 |
| 8 | Skyworks | SWKS | 102.70 | 61.02 | -40.6 | -1 |
| 9 | Veeco | VECO | 34.28 | 19.00 | -44.6 | -8 |
| 10 | Qorvo | QRVO | 114.70 | 62.54 | -45.5 | -5 |
| 11 | Aixtron (Frankfurt) | AIX | 25.21* | 12.58* | -50.1 | -1 |
| 12 | AXT | AXTI | 2.90 | 1.38 | -52.4 | -4 |
| 13 | IQE (London) | IQE | 0.360* | 0.120* | -66.7 | -7 |
| 14 | Wolfspeed | WOLF | 24.85 | 3.20 | -87.1 | 0 |

* Converted to dollars using the exchange rates on 25 April of 1 EURO = 1.13488 USD, 1 GBP = 1.33064 USD. 1 CHF = 1.20465 and 1 TWD = 0.0307331

† On 30 September, 20204, ams Osram introduced a 10:1 reverse share split

shipments, and started to deliver 200G lane-speed EMLs to multiple customers.

"Based on the breadth of our 200G EML design wins, we expect to gain additional laser transmitter market share in the upcoming wave of 800G and 1.6T transceivers utilising the more efficient 200G EMLs for AI applications," said Lowe. So strong is demand for Lumentum's EML chips that the company expects demand to exceed supply until at least the beginning of next year.

Lumentum is also selling into the industrial technology sector, where it claims to be developing new products that meet a growing demand for high precision and speed. Recently, it introduced a 26 kW fibre-laser, delivering cutting speeds up to three times faster than its predecessor. "We have shipped sample units to a key customer and are receiving very positive feedback," remarked Lowe.

Lumentum is anticipating a significant increase in sales over the coming quarters. Revenue for the third fiscal quarter is expected to range between $410 million and $425 million. Looking further ahead, the goal is a quarterly revenue of $500 million by the end of this calendar year.

## Coherent: Expanding InP capacity

Coherent, a colossus in our industry with a wide portfolio of lasers and SiC activity, has seen its share price on a similar trajectory to that of Lumentum, climbing strongly through the latter half of 2024 to eclipse $100, before falling to around two-thirds of that value.

➤ This February Michael Hurlston took over as CEO of Lumentum. He has previously held the roles of: CEO of Synaptics, the Nasdaq-listed provider of wireless connectivity and GPS technologies; and CEO of Finisar, shortly before it was acquired by II-VI, now Coherent.

For the most recently reported fiscal quarter – the second fiscal quarter, 2025, which ended on 31 December, 2024 – Coherent recorded revenue of $1.43 billion, up 6 percent sequentially and a 27 percent increase year-over-year.

In a call with investors to discuss these results, CEO Jim Anderson remarked: "During our fiscal second quarter, we made solid progress toward our goal of achieving durable companywide gross margin of over 40 percent."

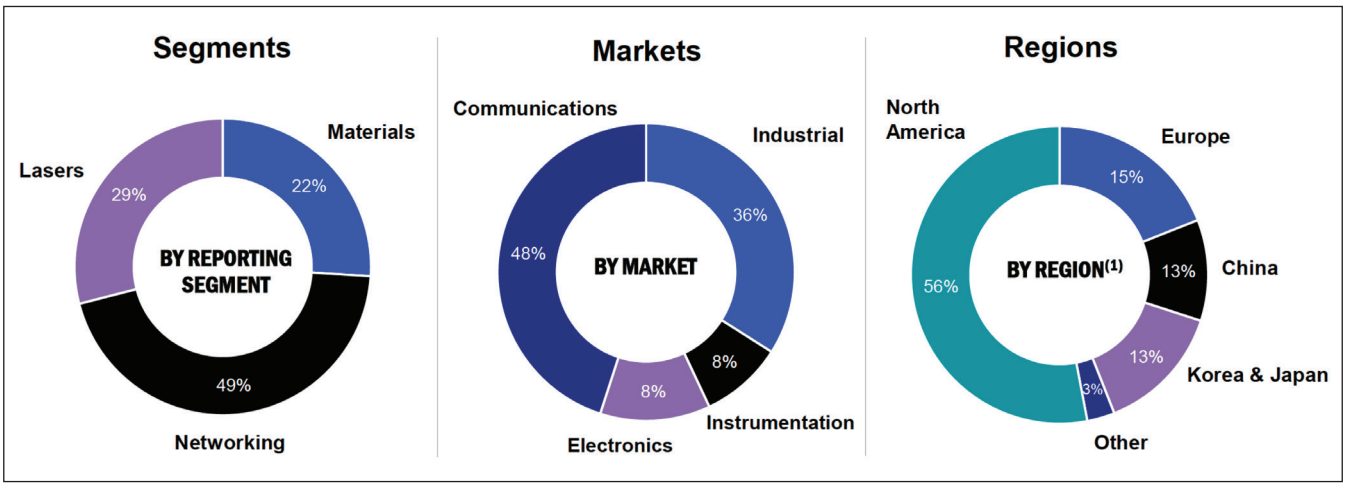
The company claims that it's gross margin, when measured with the most meaningful metric, is 38.2 percent – it is said to mark strong improvement on both a sequential and year-over-year basis, although Anderson believes the company still has a lot more work to do on this front.

Helping to drive up Coherent's revenue are sales to the data centre and communications markets.

"We achieved record Q2 datacom revenue, which grew 4 percent sequentially and by 79 percent year-over-year, due to ongoing strong AI data centre demand," remarked Anderson, who said that the number of customers adopting and ramping Coherent 800G transceivers is increasing, and revenue for variants at 400G and below remains strong.

"We also continue to make solid progress on our 1.6T transceiver products as we move through key engineering milestones with our customers. After delivering initial samples of our 1.6T datacom transceivers to customers last year, we remain on track to begin ramping sales in calendar 2025." Looking further ahead, Coherent is now developing 3.2T transceivers.

In early December, 2024, Coherent signed a non-binding preliminary memorandum of terms with the US Department of Commerce, for CHIPS Act funding for up to $33 million to support the modernisation and expansion of its cleanroom in Sherman, Texas. The funding would enable an expansion of the world's first 150 mm InP manufacturing line, adding advanced wafer fabrication equipment to support the production of InP devices at scale.




➤ Coherent operates in many sectors, with sales all over the world. Note that: revenue is by region, based on the customer headquarters address; and amounts may not recalculate, due to rounding. Credit: Coherent

Anderson mentioned this when remarking that InP production output has tripled on a year-over-year basis, when comparing the second fiscal quarters for 2025 and 2024.

"This enabled rapid year-over-year growth in our 800 gig transceiver products, some of which are EML-based and some of which are based on CW lasers combined with our silicon photonics solution."

According to the Coherent CEO, the expansion of InP capacity over the next few quarters will increase production capacity for EML and CW lasers.

"We also continue to execute on a road map of important ingredient laser technologies, such as our 200G differential EMLs; 200G VCSELs; and high-power CW lasers for our silicon photonic solutions."

Sales for the third fiscal quarter are expected to be similar to those for its predecessor, with revenue between $1.39 billion and $1.48 billion.

## Riber's rising revenue

Third on this year's leaderboard is the MBE equipment maker Riber – gaining that distinction, despite a fall in share price of almost 8 percent over 12 months.

Riber does not broadcast quarterly earnings calls with investors, so there's less detail disclosed behind its financial performance.

On 9 April, 2025, the company reported its financial results for 2024. Annual revenue had increased year-over-year by 5 percent to €41.2 million, and Riber recorded a net income for that period of €4.1 million.

Riber claims that it is strengthening its position in the MBE market, for both research and industrial production. During that year the company received orders for 13 new MBE systems.

One of Riber's new initiatives is the development of ROSIE (RIBER Oxide on SIlicon Epitaxy), a new system dedicated to the silicon photonics sector. The commercial launch of this tool is slated for 2026.

As of 31 December, 2024, Riber had an order book of €21.7 million, down 17 percent year-on-year. Orders included seven MBE systems (€16.7 million), of which five were for production. Orders for services and accessories totalled €5.0 million.

Riber has declined to provide guidance for this year. It has taken this stance due to uncertainties linked to the application of US customs duties and the economic environment.

## Woeful Wolfspeed

Investors in wide bandgap specialist Wolfspeed have had a few tough years. In November 2021 the company's share price peaked at almost $140, and since then it's plummeted, crashing from just over $70 at the start of 2023 to below $5 today. In the time period used for the leaderboard, the price plunged by 87 percent, enough for Wolfspeed to claim the bottom spot this year.

This substantial fall in share price reflects the company's financial position. It is running at a considerable loss, and there are concerns related to the strength of its diminishing reserves. Restructuring has been introduced to trim the wage bill, and it is hoped that the appointment of a new CEO, Robert Feurle, this March, will help to turn around the company's fortunes.

Not helping matters is uncertainty surrounding a $750 million grant under the US CHIPS Act.

For the most recently reported fiscal quarter, quarter two 2025, Wolfspeed recorded revenue of $181 million, slightly above the midpoint of guidance and down 7 percent sequentially. Sales of power devices contributed $91 millions, and materials added $90 million. Contribution from the recently constructed Mohawk Valley facility is rising, accounting for $52 million in Q2 2025, and is forecast to climb to between $55 million and $75 million in Q3 2025.

On the plus side, Wolfspeed has just introduced its Gen 4 MOSFET. Commenting on this product in a call on 29 January 2025 to discuss second fiscal quarter earnings, Chairman of the Board Thomas Werner described this device as a highly flexible platform that supports long-term road maps for high-performance applications and optimised products.

Werner added: "This new platform allows design engineers to create more-efficient, longer-lasting systems that perform well in tough operating environments at a better overall system cost."

Production of the Gen 4 MOSFET will involve the use of 200 mm wafers. "This will enable us to deliver products on the scale not seen in this industry before."

A headwind to Wolfspeed has been a slower than expected ramp in electric vehicles. Due to this, the company is exploring opportunities in other markets, including renewables and AI data centres.

"Demand in industrial and energy applications is showing some green shoots, but visibility remains limited," remarked Werner.

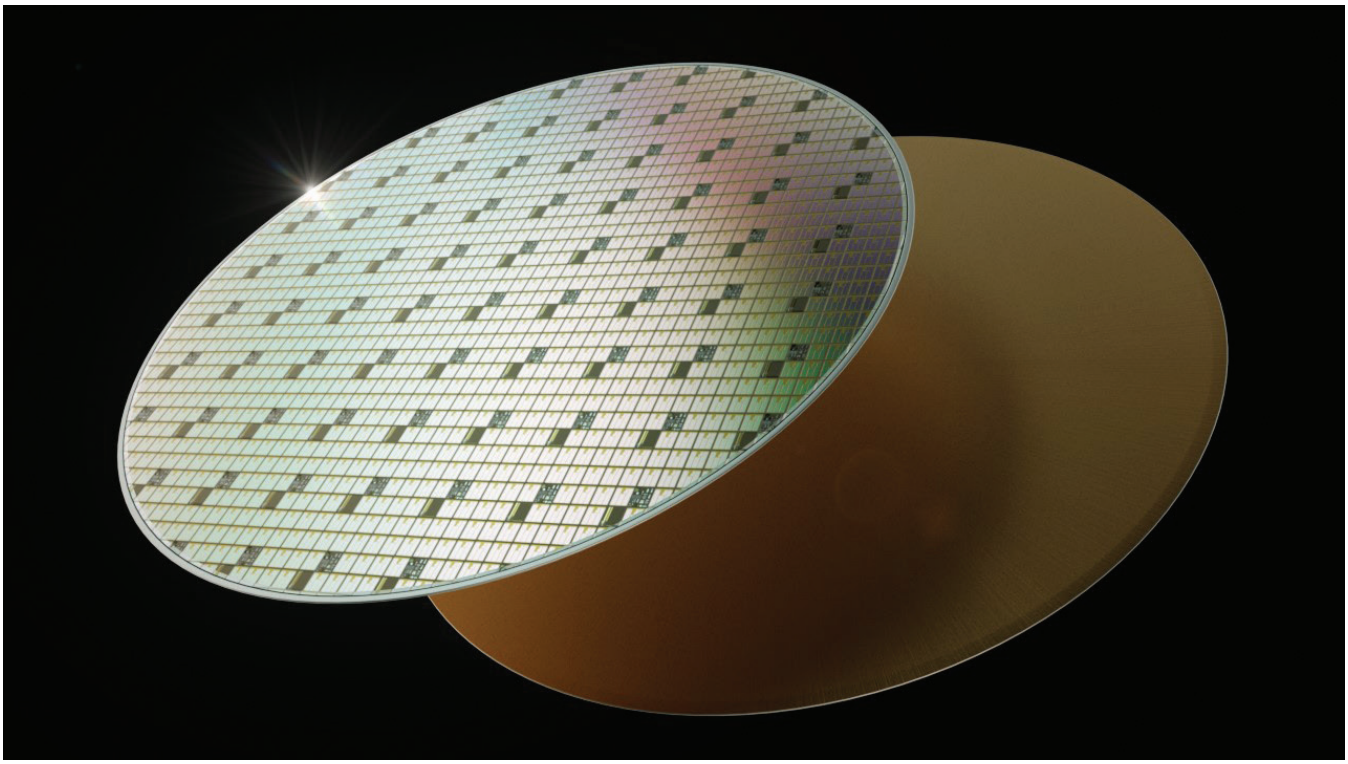
To try and improve Wolfspeed's financial position, as well as transitioning production from 150 mm to 200 mm wafers, the company is reducing its capital expenditure for fiscal 2025 to $1.2 billion.

"This level of CapEx allows us to continue to grow the top line while maintaining the capability to ramp supply rapidly, should a sharp turn in demand materialise," said Werner, who remarked that the company has also started to work on additional cost reductions, with a focus on operational efficiencies, lower manufacturing costs, and stricter cash management.

A more recent change, announced on 30 April, is the appointment of a new CFO. Outgoing CFO, Neill Reynolds, will be remaining with Wolfspeed to ensure an orderly transition.

The new CFO, and the recently appointed CEO, Feurle, face significant challenges in turning Wolfspeed around. It will not be easy, and they would welcome support and stability from the US government.

Right now, tariffs and uncertainties stemming from the White House are headwinds to the valuation of many companies, including those in the compound semiconductor sector. Quite what the future holds is anyone's guess, and it will be interesting to look at both the trends and the details in next year's *Compound Semiconductor Share Price Leaderboard*.



# Thick homoepitaxy on 200 mm SiC

The cost of SiC substrates needs to come down. But are we going to hamper these efforts by imposing limits on the thickness of this foundation?

**BY THOMAS KUHR FROM WOLFSPEED**

SiC is benefitting from the electric vehicle boon, with uptake of power devices based on this wide bandgap semiconductor enabling higher-efficiency electronics that reduce system losses by 80 percent or more. However, while this is impressive, it is only the tip of the iceberg. As well as its wide band gap, SiC has a high thermal conductivity and an excellent saturation drift velocity, allowing devices made from this material to operate at high electric field densities and serve in many technologies, including high-voltage DC, pulsed power, and solid-state transformers. Using single SiC MOSFET chips that can handle up to 10 kV, or even-higher-voltage bipolar devices, equips designers with the opportunity to simplify systems and reduce resistive-heating losses across many applications.

As SiC continues to demonstrate an improved performance over incumbent technologies, it is facing heavy scrutiny for its higher cost. Within the semiconductor industry, the common solution to this challenge is to move to larger wafers, which divide fixed processing costs over many more devices. This is underway, with SiC substrates currently undergoing a transition from 150 mm to 200 mm diameters. However, in contrast to the silicon industry, which increased wafer thickness with diameter, the SiC industry is considering retaining the 350 μm thickness used for today's 150 mm-diameter wafers for the 200 mm format.

At Wolfspeed, a world leader in SiC substrates and devices, we have been investigating how epitaxial layers of different thicknesses vary in quality, when using wafers with thicknesses of 350 μm and 500 μm. The growth of 'thin' SiC layers, used for production of 650 V and 1200 V devices does not tend to result in significant stresses from temperatures profiles, or from differences in doping between the substrate and the epitaxial film. However, when epitaxial layers are thicker and lower doped – they are the two key requirements for higher-breakdown-voltage devices – stresses are magnified, generating new defects and wafer shape concerns.

Additionally, epitaxial defects increase in size and area, because they are often generated at or near the substrate interface and grow commensurately with the film. The compounding effect of greater stress and larger defects, coupled with higher-voltage devices often being larger in size, results in much lower usable area of the wafer, leading to lower die yields and a higher cost per device.

## What could go wrong?

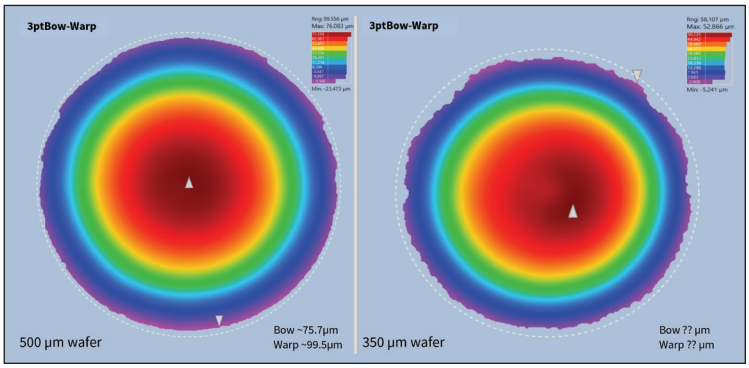
To deepen our understanding of the interaction of thinner substrates and thicker epitaxy, we have investigated the performance of homoepitaxial layers with three different thicknesses, grown on 200 mm SiC substrates that are 350 μm-thick and 500 μm-thick, using two commercially available reactor platforms. Admittedly, the best way to approach this evaluation would be to cut a single boule into multiple substrates with different thicknesses, as this would normalise the starting point for substrate defects – but for this work we used internal production wafers as they became available. We selected doping and thickness targets based on specific device requirements, chosen to hit the lowest resistance at the required breakdown voltage, and we have been able to identify if there are any potential manufacturing limits by utilising a suite of measurements that are part of our standard production fab flow.

One concern during epitaxy is the stability of wafer shape at high growth temperatures. The wafer shape may differ at room temperature and at more than 1600°C, and thinner wafers may change shape unpredictably. Any variations will adversely affect growth through thickness or doping non-uniformity, and in the worst-case scenario the wafer may break or be ejected from the carrier during processing.

Our results have dispelled this concern when reducing wafer thickness from 500 μm to 350 μm. If anything, the thinner wafers lead to improvements in film thickness and doping uniformity, although this is likely to depend on the reactor furniture design. Note that we need many more growth runs to establish statistically significant conclusions. However, our initial investigations indicate that there are no concerns associated with using thinner 200 mm wafers for the epitaxial growth process.

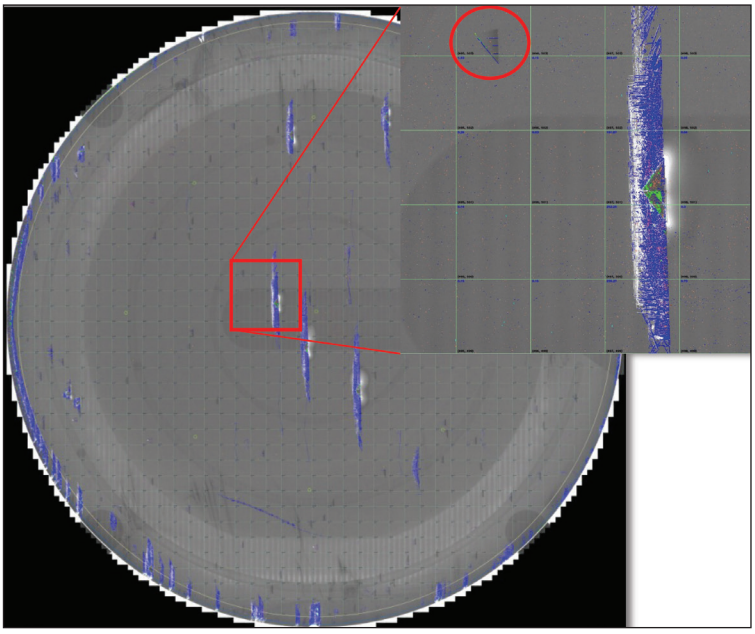
Due to similarities in the processing chemistry and device design for thin and thick SiC devices, our device fabrication team prefers a similar state for the surface of all epiwafers. To see if this is the case, we scrutinised our material with atomic force microscopy (AFM) and confocal imaging. AFM, useful for gauging short-range roughness, shows a matched performance in roughness, with the average roughness (Ra) less than 0.2 nm for thin and thick films. According to confocal imaging, long-range roughness for thicker films is greater than it is for thin films, with an average roughness (Ra) of around 0.6 nm.

These finding are independent of substrate thickness, though a bit more roughness is slightly more spatial on the confocal imaging scale. This suggests that like doping and thickness uniformity, surface roughness may be treated as a non-issue with respect to wafer thickness. However, there's a need to reduce surface roughness in thicker films, and to further refine spatial dependencies.

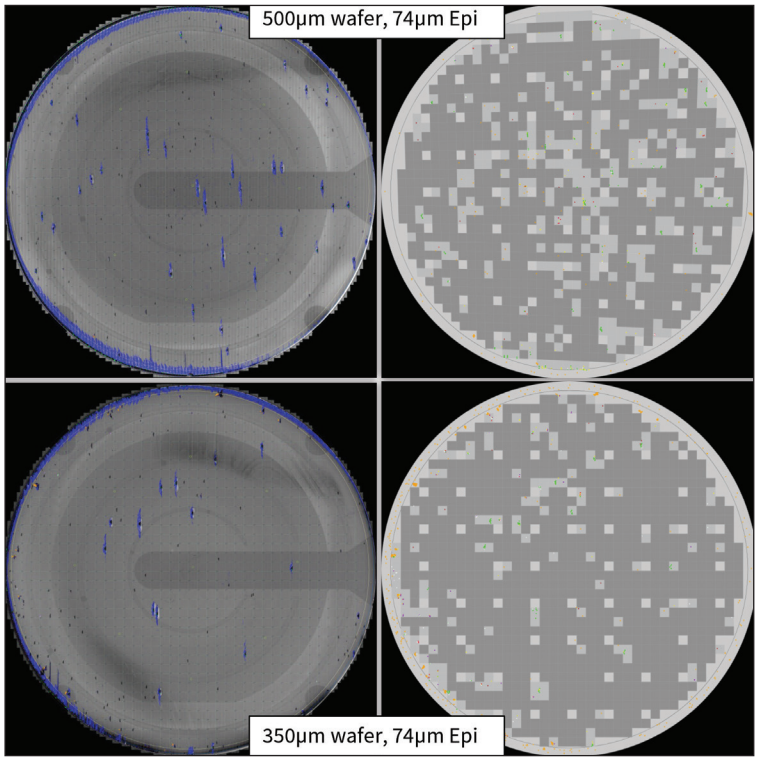



➤ Figure 1. Comparison of wafer shape maps for 500 μm (left) and 350 μm (right). Notice that in both cases the full map has not been generated, though the left scan is more complete. The bow and warp of the 350 μm wafer is clearly higher and outside the measurement range of the current tool configuration.

With thicker epitaxial layers resulting in larger defects and higher film stress, selecting thinner substrates exacerbates the stress problem. Due to this, we were not surprised to find a shape issue when growing thicker epilayers on thinner substrates. Using 200 mm-diameter SiC, growing a 13 μm-thick epilayer on a 500 μm-thick substrate leads to a bow of 20-40 μm; and increasing the thickness to 115 μm, and dropping the doping to the mid-$10^{15}$ $cm^{-3}$, increases the bow to around 80 μm. If the substrate is then thinned to 350 μm, bow increases to more than 100 μm, leading to threats of handling errors and wafer breakage during device fabrication processes. While 100 μm of wafer bow may seem miniscule compared with the hundreds



➤ Figure 2. Stitched image map with preliminary inking to estimate usable area for devices for 115 μm epitaxy on 500 μm-thick 200 mm substrates. An arbitrary 5 mm x 5mm grid was used for visualisation. Note that not all defects are correctly identified, but that area effect of gross defects like triangles can be seen, as shown in the insert.




➤ Figure 3. Stitched image maps with preliminary inking to estimate usable area for devices for 74 µm epitaxy on 500 µm and 350 µm thick 200 mm substrates. 5x5 usable areas of 75-85 percent shown.

of microns of bow that may occur during ion implantation, not all fabrication tools are capable at that starting point. Our view is that more work may be needed to compensate for wafer shape concerns, if substrates that are just 350 µm-thick are going to be used for growing thicker epitaxial layers.

The biggest disadvantages of SiC are its defectivity that's inherent in its crystal growth process, and the relative ease of defect formation. The defects that are generated during boule growth and reside in the substrate will propagate into the epilayer by either continuation of the growth, or by conversion to other types of defects. The sources of defects could be micropipes, threading dislocations, stacking faults, subsurface damage from surface preparation, or simply a dirty surface from inadequate cleaning; more generally speaking, anything that disrupts the natural stacking of the crystal lattice. For example, a common defect called a 'triangle' – it's a crystal stacking disruption that manifests as a triangular shape visible on the growth surface – increases in size with epitaxial growth, from 0.4 mm-long for 13 µm of epitaxial growth to 3.2 mm for a 115 µm-thick film. You might think what's the big deal, given that devices are typically 25 $mm^2$ or more in size, so a triangle defect should only affect one or two die.

Well... As we have already mentioned, film stress increases with thickness, and the doping offset between the film and the substrate. Due to this, and the very low formation energy for basal plan dislocations in SiC, it's possible for defects, such as triangles, to generate basal plane dislocations that glide vertically along the wafer, emanating from the source defect. Consequently, a defect that originally affected just one or two devices may now impact five-to-ten times as many die, slashing yield.

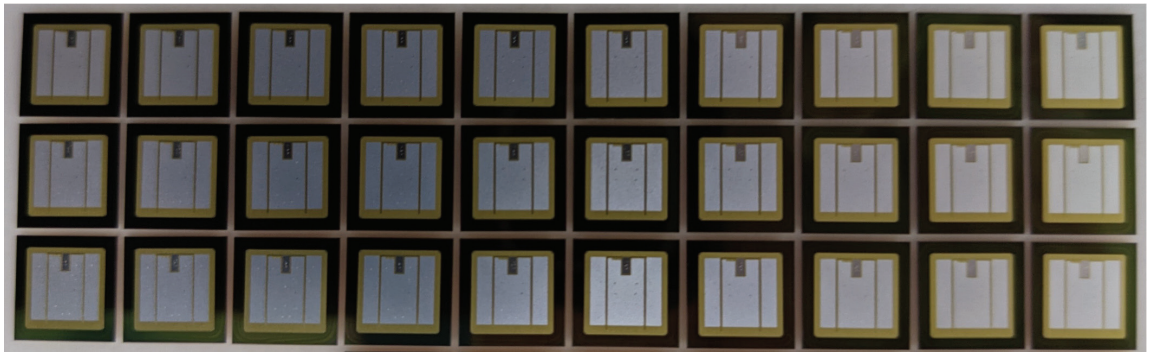
The good news is that by careful management of the temperature distribution on the wafer during epitaxial growth, it's possible to reduce excessive film stress. Even if this gain comes at the expense of an increase in wafer bow, this enables the processing of thinner wafers without increasing film defectivity.

Unfortunately, not all our measurements went particularly smoothly. Due to incomplete scans, our values for maximum bow on our thin wafers with thick epitaxial layers were initially incorrect. Correcting this error, a simple tooling limitation that can be overcome with minor adjustments, took time and effort.

We also encountered problems associated with automated inspection of defects, due to inspection algorithms that are trained for a different size defect or a smoother surface. This meant that applying our accurate defect classification and data acquisition to thinner epitaxial layers was initially troublesome for thicker epitaxial films.

Our issues related to wafer bow scans and defect inspection are far from insurmountable, and in the case of defects, they are not even substrate-thickness dependent. However, intervention and development are needed before these techniques can serve in a high-volume manufacturing process.

To summarise, thinner wafers will result in shape concerns that must be addressed, either before or during epitaxial growth. But if the temperature distribution and stresses are effectively managed,



➤ Figure 4. 10kV die ready for packaging.

additional stress-induced defects should not be problematic. This doesn't sound too bad... except the predicted yields don't look great, and the costs are still high.

Illustrating this point, let's consider 5 mm by 5 mm devices for a 1200 V MOSFET wafer. In this case, the useable area is more than 90 percent. But if thicker epitaxy is needed, the useable area falls to around 70 percent, due to the increased area effect – and if the device size increases, there's an additional fall in usable area, determined by simple Poisson statistics. Now that SiC wafer with a usable area of more than 90 percent for a 1200 V MOSFETs is potentially below 40 percent for 10 kV MOSFETs – and that's before the epiwafer has even ever entered a device fab.

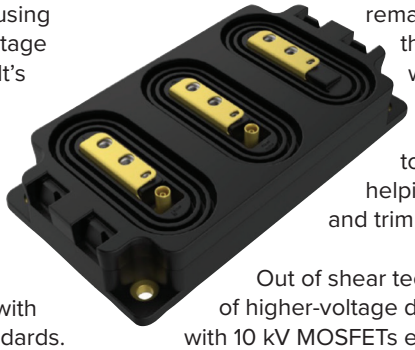
## A feasible thickness?

Let's return to the original question: does thinning the SiC substrate limit the capability of using thicker epitaxial layers to make high-voltage devices? Well maybe... and maybe not. It's clear that it's critical to get the wafer shape under control and manage the epitaxial growth stresses, in order to prevent complications during device fabrication and thus keep cost low. To support such efforts, adjustments are needed to ensure continuity of measurement and metrology methods with current best practices and industry standards. But what's also really importantly is for SiC substrate manufacturers to continue to focus on defect reduction. Without lower defect concentrations, device size and capability or device yield will continue to be trade-offs, and costs will remain high regardless of the optimisation of the epitaxial growth process.

> Thinner wafers will result in shape concerns that must be addressed, either before or during epitaxial growth. But if the temperature distribution and stresses are effectively managed, additional stress-induced defects should not be problematic

In closing, the drive for thinner SiC substrates will continue, because reducing their cost remains a huge motivator. Against this backdrop, innovators will find ways to deal with wafer shape, and substrate manufacturers will continue to decrease defect density, helping to improve device yields and trim costs.

Out of shear technological need, adoption of higher-voltage devices will continue to rise, with 10 kV MOSFETs eventually paving the way for even higher voltage IGBTs. The SiC revolution will continue!



➤ Left. High-performance half-bridge 10 kV, 50 mΩ all-SiC power module.


# Towards defect-free SiC epiwafers

Helping to drive improvements in SiC power devices, advances in epitaxy are producing nearly defect-free layers of SiC on the carbon face, and those that that are free from basal plane dislocations on the silicon face.

**BY NGUYEN XUAN SANG AND SHIV KUMAR FROM THE INSTITUTE OF MICROELECTRONICS, A-STAR, SINGAPORE, AND MARCIN ZIELINSKI OF SOITEC, FRANCE**

BY SURPASSING the performance limits of silicon devices, those made from SiC are capturing an increasing share of the power electronics market. However, the high cost of this wide bandgap semiconductor is still a headwind to success, with the price of devices exacerbated by yield losses that can be traced back to defects in the substrate and the epitaxial layers.

There are various types of defects that arise in SiC, due to the material's intrinsic physical properties. Defects include micropipes, triangles, carrots, stacking faults, and dislocations. For the latter class of imperfection, the main forms are basal plane dislocations, threading screw dislocations, and threading edge dislocations. Among them, basal plane dislocations are considered critical 'killer defects', because they induce bipolar degradation in SiC power devices.

Over the years, there has been significant progress in SiC bulk growth and substrate production, in terms of both wafer size and defect reduction. Regarding the former, manufacturers of SiC wafers are rapidly transitioning to 200 mm production.

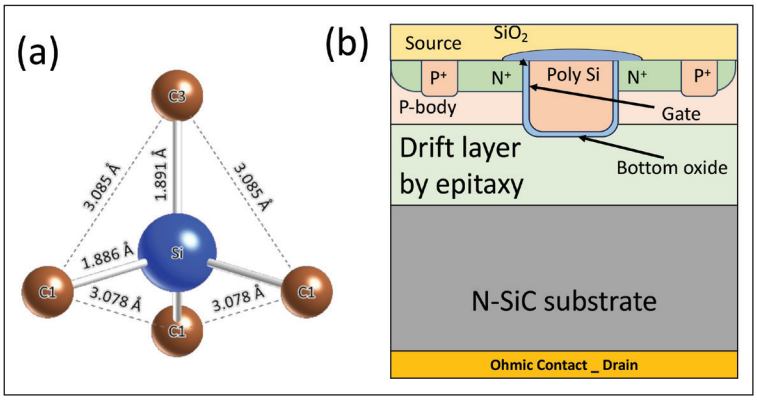
A key milestone in the sublimation process used to produce bulk SiC came in 2004, when Daisuke Nakamura and colleagues from Toyota Central R&D Laboratories, Japan, reported in a *Nature* paper the creation of seed that is free from micropipes and has very few dislocations. This advance opened the door to stable, optimised sublimation growth on high-quality seed layers. Thanks to this breakthrough, today's commercially available 150 mm and 200 mm SiC substrates are micropipe-free, and exhibit low dislocation densities: basal plane dislocations are less than 500 $cm^{-2}$, and threading edge and screw dislocations are both below 5,000 $cm^{-2}$.

Due to the polarisation of the Si-C bond, the top surface of SiC can exhibit either silicon-face or carbon-face polarity. These two polarities result in distinct surface characteristics and different properties. In terms of oxidation, the carbon-face has a higher oxidation rate than the silicon-face. This difference, attributed to the higher concentration of dangling bonds on the carbon-face, complicates passivation during the oxidation process. Another noteworthy difference is that carbon-face samples often exhibit 4H-SiC polytype inclusions that extend through the entire wafer, whereas silicon-face samples are typically free from such inclusions. Surface roughness also differs, with the silicon-face tending to have a rougher surface, with a higher density of cracks, particularly near the edges.

## Benefits of the carbon-face

Today's SiC high-power device technology primarily utilises silicon-face SiC substrates. This face ensures a high-quality interface and a large band-offset with the gate oxide. However, in SiC trench MOSFETs, the gate stack is formed on the SiC (113) plane for both silicon-face and carbon-face substrates (see Figure 1).

For trench MOSFETs, the carbon-face presents advantages, due to its faster oxidation rate. This characteristic enables the formation of an oxide layer at the trench bottom that is up to three times thicker than that on the sidewalls, simplifying fabrication and improving the gate breakdown voltage. These strengths are realised despite the lower band-offset between $SiO_2$ and carbon-face SiC.

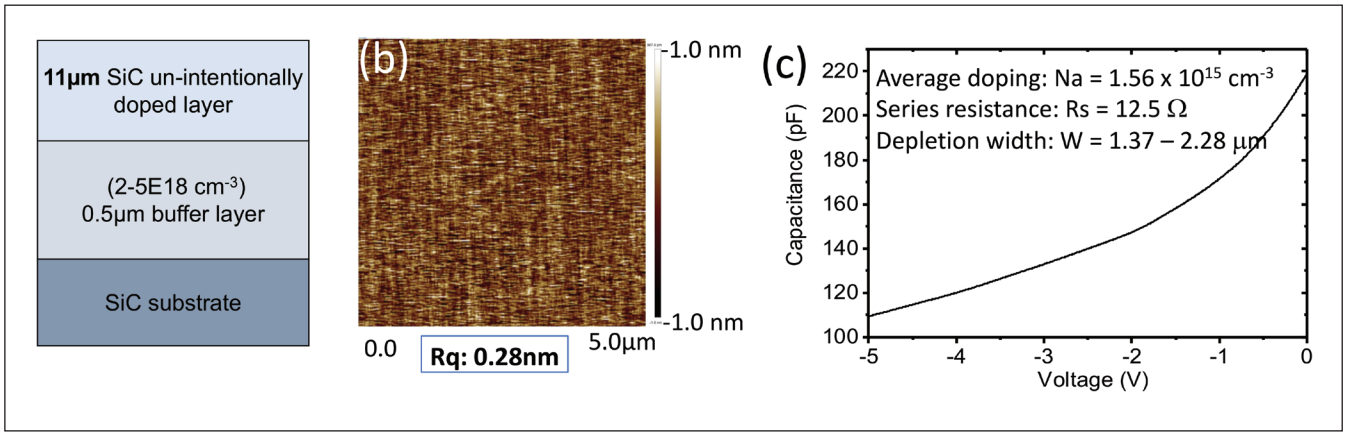



➤ Figure 1. (a) The basic structural unit of a SiC crystal and (b) typical design of SiC trench MOSFET.

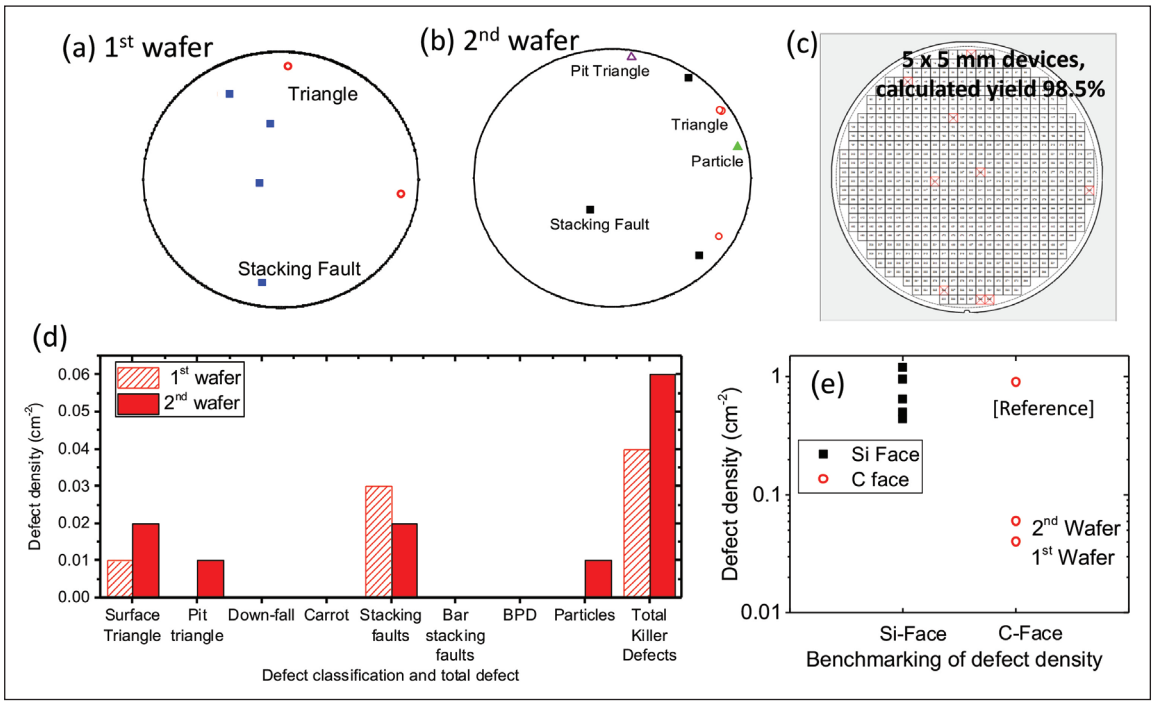
Helping to maximise the performance of devices using the carbon-face is our partnership between A-STAR, the National University of Singapore, and Soitec. Working together, we have demonstrated a nearly defect-free carbon-face SiC epitaxy growth process with an incredibly high growth rate – it's around 50 µm $hr^{-1}$ on 150 mm carbon-face SiC substrates.

For this work, we loaded an epi-ready, *n*-type carbon-face SiC 150 mm substrate with a 4° off-cut towards (11$\bar{2}$0) in a commercial hot-wall CVD system. After growing a buffer layer approximately 0.5 µm-thick, we added an 11 µm-thick SiC drift layer at a growth rate of 50 µm $hr^{-1}$.

Using Fourier transform infrared spectroscopy, we confirmed the thicknesses of the buffer and drift layers, and determined that the thickness uniformity is less than 3 percent (see Figure 2 (a)). According to atomic force microscopy, our epiwafers have a




➤ Figure 2. (a) Structure of SiC epitaxy growth on a 150 mm carbon-face SiC substrate. (b) Typical surface morphology scan by atomic force microscopy, determining a root-mean-square roughness, $R_q$, of around 0.28 nm. (c) Capacitance-voltage characteristics and calculated doping of SiC epilayer measured by a mercury probe.




➤ Figure 3. (a-c) Defect distribution and calculated yield in two carbon-face SiC wafers, obtained with a Candela 8520 scan. (d) Total killer defect density of the wafers, nearly defect-free obtained in carbon-face SiC epitaxy. (e) Benchmarking the killer defect density of carbon-face epitaxy with silicon-face epitaxy.

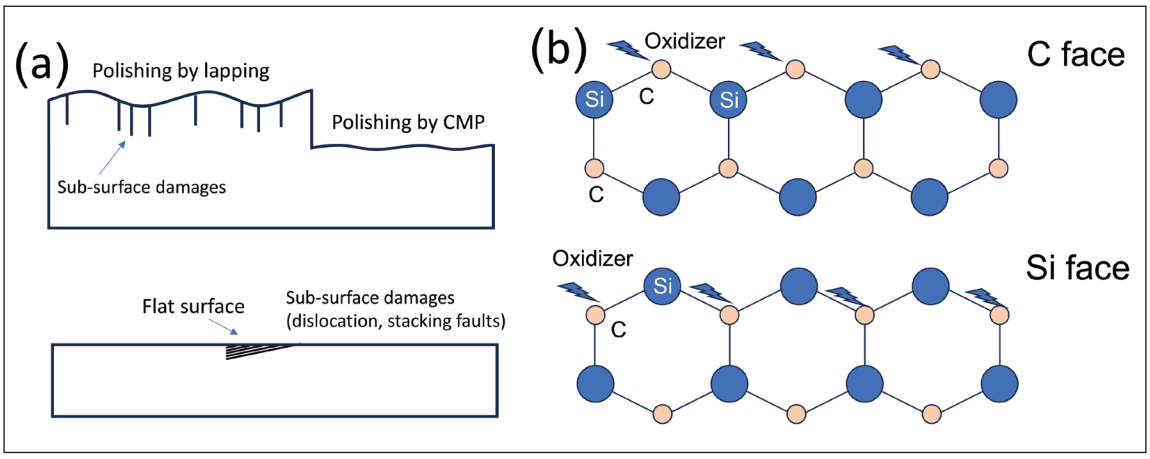
smooth surface, with a root-mean-square roughness just below 0.3 nm.

We have also investigated the electrical properties of our epiwafers. This has involved acquiring capacitance-voltage plots with a mercury-probe, and calculating doping profiles, derived from capacitance-voltage data (see Figure 2 (c)). Our results reveal that unintentional (or background) doping in the carbon-face SiC epilayer is around $1.5 \times 10^{15}$ cm$^{-3}$, a value low enough to enable precise control of doping in the drift layer within the range of $1\text{-}2 \times 10^{16}$ cm$^{-3}$ for MOSFET devices.

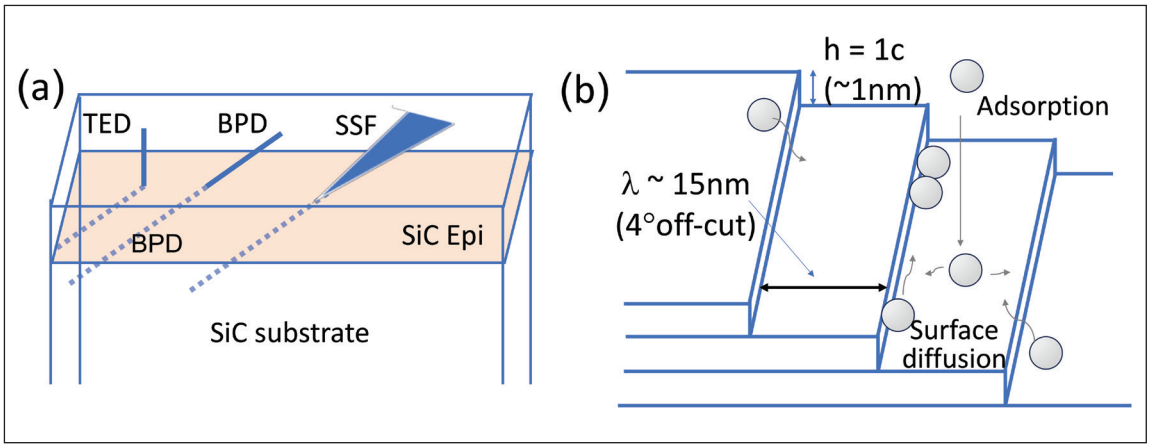
Using the KLA Candela 8520 system, we have measured the defect density in our carbon-face SiC epiwafers. This tool, which combines surface and photoluminescence defect analysis, has determined that there a very few defects in our material – the defect density of less than 0.1 cm$^{-2}$ (see Figures 3 (a-d)).

To benchmark our carbon-face SiC epiwafers, we have compared them with a silicon-face SiC epilayer and a reference carbon-face SiC epi layer (see Figure 3 (e)). Compared with these two, the defect density in our carbon-face SiC epiwafers is nearly an order of magnitude lower, illustrating that our growth process produces material nearly free from defects. This low defect density provides significant advantages for carbon-face SiC devices, particularly in large-scale device architectures, such as bipolar devices.

A key contributor to our nearly defect-free epitaxy is our dramatic reduction in pre-existing surface




➤ Figure 4. (a) The chemical mechanical polishing (CMP) process on a SiC wafer and the sub-surface damages observed on the wafer's flat surface. (b) Illustration of the oxidation process in carbon-face and silicon-face SiC, highlighting how the faster oxidation rate of the carbon-face SiC contributes to a higher material removal rate during the CMP process of SiC wafers.




➤ Figure 5. (a) Conversion of basal plane dislocations (BPDs) in SiC epitaxy and (b) step-controlled epitaxy process.

and sub-surface crystal defects in the SiC substrate. We have realised this by optimising our chemical mechanical polishing process, which involves oxidation and oxide removal (see Figure 4 (a) and (b) for an illustration of this process). Our approach is customised for carbon-face SiC, which has a far higher oxidation rate than that on the silicon face. By tailoring the chemical mechanical polishing process, we produce smooth surfaces with minimal sub-surface damage.

The most prominent defects occurring during the epitaxial process are basal plane dislocations and stacking faults. To minimise these imperfections, most basal plane dislocations, which have a defect density of around 500 $cm^{-2}$, are converted to threading edge dislocations. Employing an optimised hydrogen gas etching process prevents conversion of the basal plane dislocations into more troublesome Shockley stacking faults (see Figure 5 (a)). Conversion of basal plane dislocations into threading edge dislocations is also promoted by the high growth rate of 50 μm $hr^{-1}$, ensuring further minimisation of basal plane dislocations in the SiC epilayer.

Another asset of carbon-face epitaxy is favourable step-flow growth, thanks to the long diffusion length – it is greater than 1 μm (see Figure 5 (b)). Due to this, along with the high degree of conversion of basal plane dislocations into threading edge dislocations, we are able to enjoy nearly defect-free carbon-face SiC epitaxy.

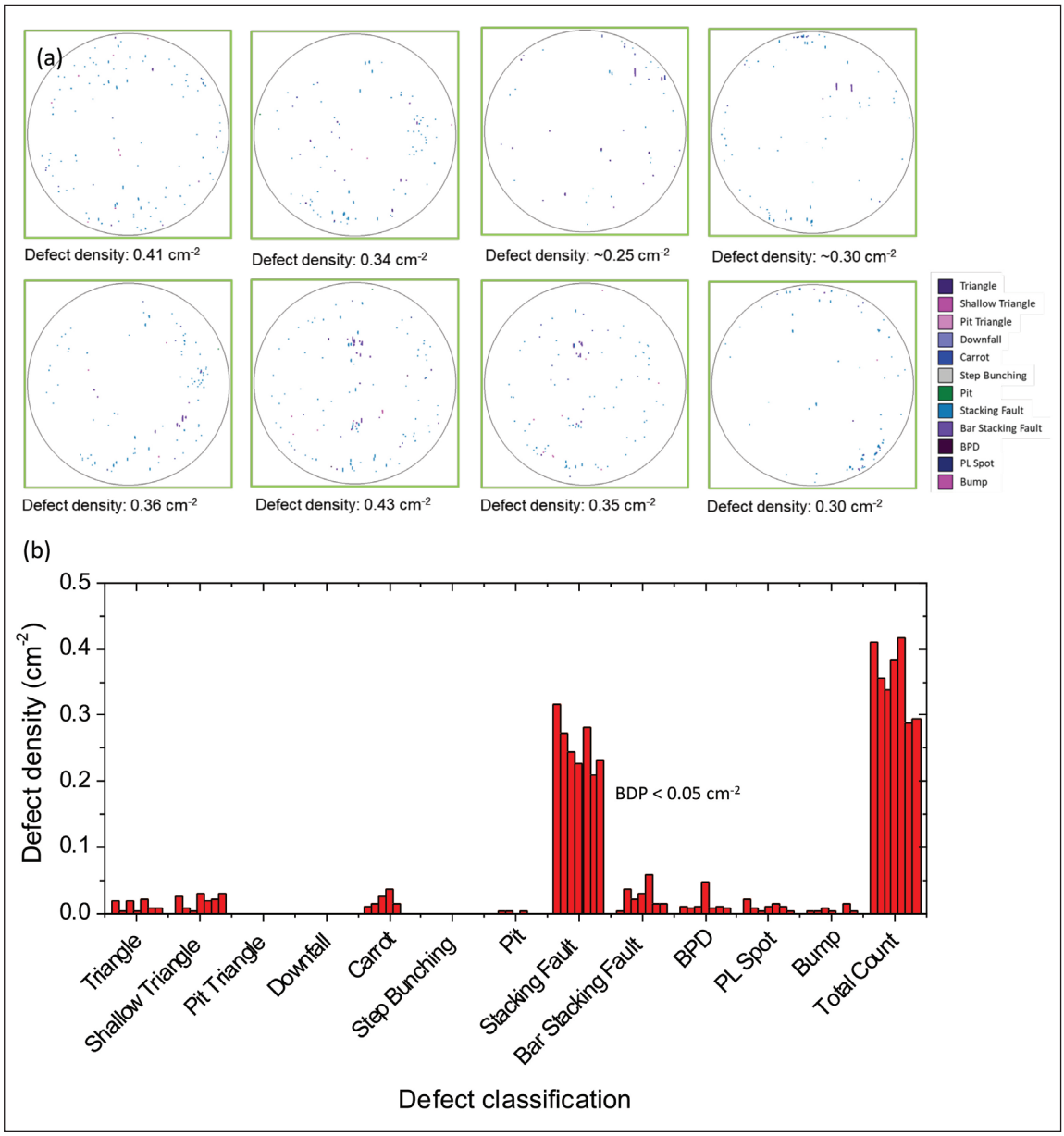
## Strengthening silicon-face epitaxy

In addition to our development of the epitaxy process on carbon-face SiC wafers, which has demonstrated the significant potential for defect reduction in SiC epitaxial growth, we have introduced innovations to the traditional epitaxy process on silicon-face SiC wafers. We have developed these breakthroughs on 200 mm SiC wafers. Key to our success is the conversion of basal plane dislocations in the substrate to threading edge dislocations in the buffer layer, prior to the growth of the device drift layer.

Our success builds on the work of Tangali Sudarshan's group from the University of South Carolina. Back in 2005, in *Applied Physics Letters* (**87** 151913), they reported that epitaxy can be free from basal plane dislocations by etching the substrate surface with potassium hydroxide prior to loading the wafer into the processing chamber. The disadvantage of that particular process is that it's impractical for large-scale production of SiC epiwafers. But there is much merit in the principle of preparing the surface by etching around the regions with basal plane dislocations, to promote their conversion to threading edge dislocations during epitaxial growth.

Drawing on this approach, we have developed an *in-situ* etching technique for SiC wafers that involves the introduction of two etching steps: one during baking, and another between the buffer layer growth steps. The combination of *in-situ* hydrogen etching at processing temperatures and surface recovery through etch-back and material recovery via low-temperature baking is effective at filtering out basal plane dislocations in the drift layer. Material produced by this process, which is practical and scalable for SiC epitaxy manufacturing, is almost 100 percent free of basal plane dislocations

In addition to our development of the epitaxy process on carbon-face SiC wafers, which has demonstrated the significant potential for defect reduction in SiC epitaxial growth, we have introduced innovations to the traditional epitaxy process on silicon-face SiC wafers. We have developed these breakthroughs on 200 mm SiC wafers. Key to our success is the conversion of basal plane dislocations in the substrate to threading edge dislocations in the buffer layer




➤ Figure 6. (a) Defect distribution and classification for 200 mm SiC epitaxy, captured by the KLA Candela 8520 measurement for a batch of eight wafers. (b) Defect density plot for these wafers, showing extremely low defect density and a nearly basal-plane-dislocation-free silicon-face SiC epitaxy layer.

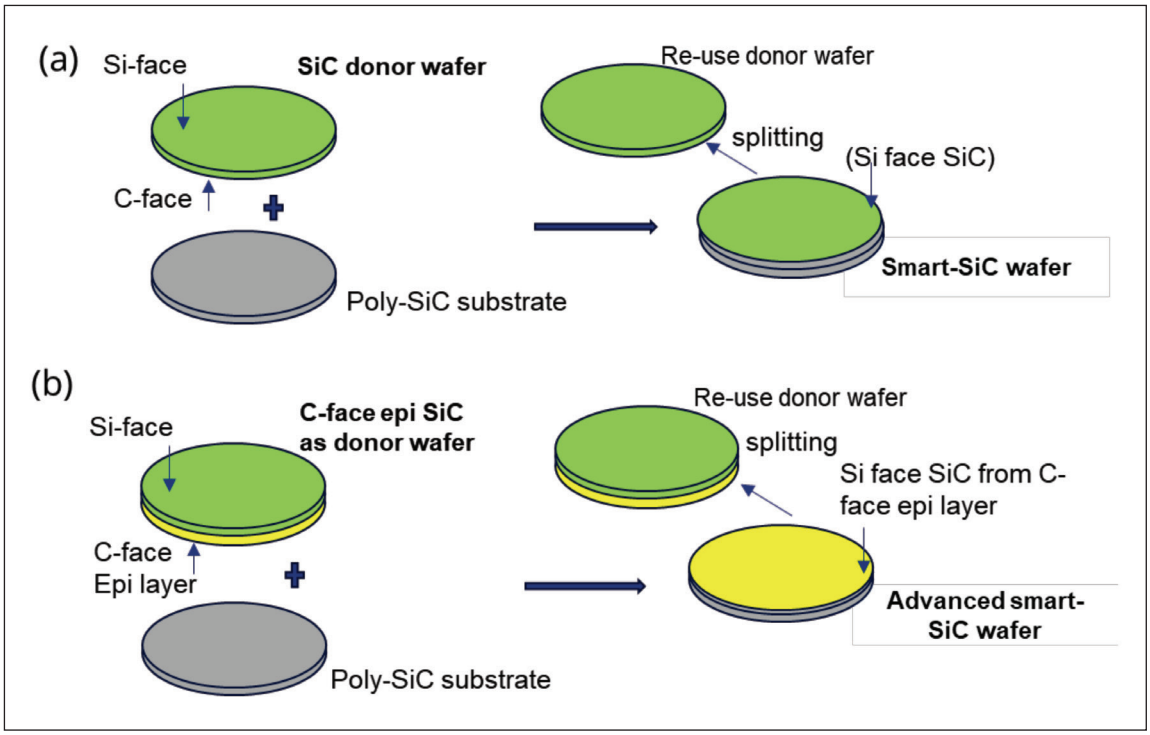
The effectiveness of our approach is highlighted by defect scans that capture the surface and total defect distribution of a batch of eight SiC wafers. These scans, acquired with a KLA Candela 8520 tool, reveal that the basal plane dislocations in the wafers are nearly eliminated, with a density less than 0.05 $cm^{-2}$ (see Figure 6). Another benefit of the process is a significant reduction in defect density, which falls from a typical value of 1.0 $cm^{-2}$ to just 0.3 - 0.4 $cm^{-2}$.

## Smart SiC substrates

Another approach to realising SiC epitaxial wafers that are free from basal plane dislocations is to start with substrates that do not have this imperfection. In this case, one potential candidate is SmartSiC, a material technology developed by Soitec.

This company's engineered substrates have a foundation for epi-growth that's formed through wafer bonding and layer transfer (see Figure 7 (a)). These substrates are produced by bonding carbon-face donor SiC wafers onto heavily doped poly-SiC substrates. After splitting a mono-crystalline SiC wafer, a layer of approximately 1 μm of SiC single crystal remains on the poly-crystalline SiC, forming a new type of SiC wafer known as Smart SiC.

One of the biggest benefits of Smart SiC is the higher substrate doping of the poly-crystalline SiC – this simplifies the SiC MOSFET fabrication process, by enabling a straightforward backside ohmic contact and reducing the on-resistance in SiC MOSFETs. However, there are additional merits of SmartSiC, relating to switching donor wafers from mono-SiC to a carbon-face epitaxial layer that's bonded to a poly-SiC substrate (see Figure 7 (b)). With this modification, the transfer layer in the SmartSiC wafers originates from the carbon-face SiC epitaxial layer, and retains its associated advantages.




➤ Figure 7. (a) Process flow of typical SmartSiC wafer fabrication from Soitec. (b) Advanced process for Smart SiC wafers using carbon-face SiC epitaxial layers.

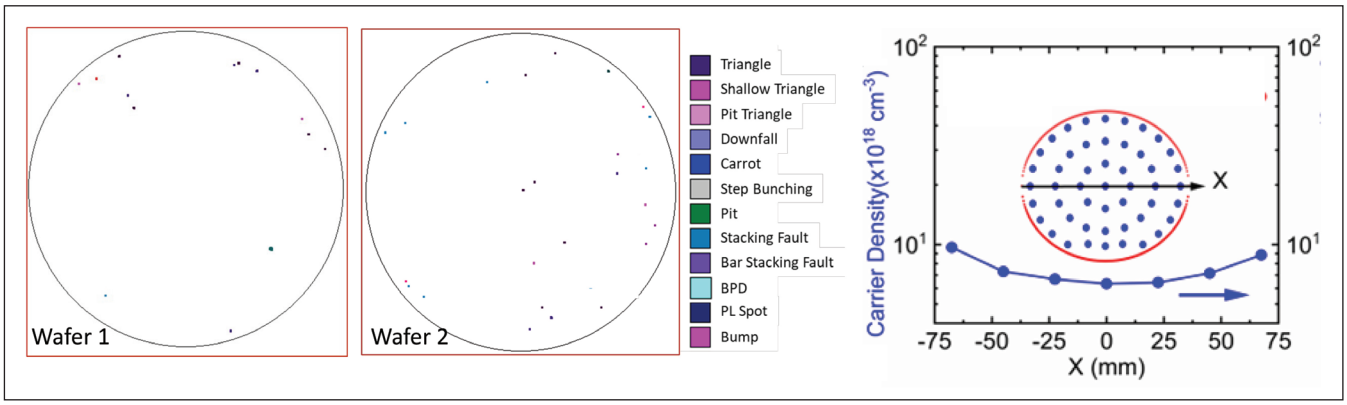
To be used as a donor wafer for Smart SiC, the carbon-face SiC epitaxial layer must exhibit a low defect density and high doping levels.

According to characterisation provided by the KLA Candela 8520 tool, the wafers we have developed in this work meet these criteria, exhibiting an extremely low defect density that's free from basal plane dislocations.

Doping measurements for these wafers indicate values exceeding 6 x $10^{18}$ $cm^{-3}$, showing that SmartSiC technology is a promising new approach for producing SiC MOSFETs.

While SiC wafers still have some way to go to become 'defect-free', as is the case for silicon epiwafers, much progress is being made in this direction – and our work provides another significant step along this path.

*The authors wish to thank Lakshmi Kanta Bera, Chand Umesh, Surasit Chung, Navab Singh, Gong Xiao and Yeo Yee-Chia from the Institute of Microelectronics, A-Star, Tok Eng Soon from the National University of Singapore, and Shian Yeu Kam, Loic Kabelaan, Walter Schwarzenbach, Ionut Radu and Loann Boudin of Soitec, France*




➤ Figure 8. (a) Defect density of a heavily doped carbon-face SiC epitaxial layer scanned using the KLA Candela 8520 system. The two wafers are free from basal plane dislocations. (b) Doping distribution along the X-direction of the carbon-face SiC epitaxial layer, showing a doping level exceeding 6 x $10^{18}$ $cm^{-3}$.

# The promise of halogen-free vapour phase epitaxy

Simple reactions based on metal sources can improve substrate production and the growth of a thick drift layer for vertical power devices

**BY TAISHI KIMURA AND DAISUKE NAKAMURA FROM TOYOTA CENTRAL R&D LABORATORY**

WHAT ARE the biggest technologies of today? While it's not easy to offer a definitive answer, a very strong case can be made for AI, and for automobiles powered by a battery.

These rise of these two technologies has widespread consequences, including devouring huge amounts of electricity. Consumption is so high that many AI tech companies, such as Google, Amazon, Microsoft and Meta, are interested in nuclear power plants; and those producing EVs have already played a major role in driving up the proportion of global energy consumption associated with transportation to 30 percent, a figure only expected to increase.

To control the distribution of electricity, designers of AI infrastructure, EVs, and the likes of chargers and power supplies, have tended to draw on well-established silicon technology, which includes silicon IGBTs and MOSFETs. However, the performance of these incumbents is held back by the small bandgap of silicon. Due to this limitation, there is now a growth in sales of power devices with a wider bandgap, including those made from SiC and GaN.

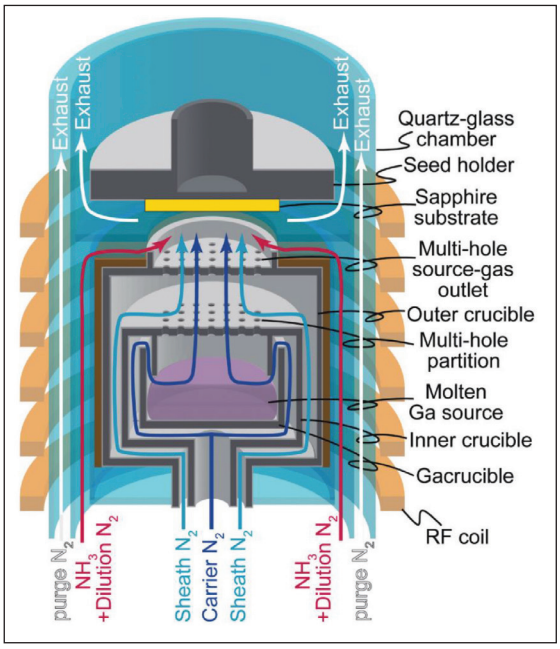
The strengths of GaN are not just a high breakdown voltage that results from the wide bandgap. In addition, GaN devices benefit from a high mobility. Thanks to these attributes, figures-of-merit for GaN are approximately 1,000 times higher than those for silicon, and exceed those for SiC by a factor of two to four.

A number of architectures are used to produce GaN devices. The lateral forms have enjoyed the greatest commercial success so far, but vertical power devices offer much promise – they are compelling candidates for serving in EVs/HEVs/HVs, where they combine a breakdown voltage of 1200 V with a current density of hundreds of amps-per-square-centimetre. If vertical GaN power devices were deployed in an electric vehicle's power control unit, this would: drastically reduce its size, due to smaller inductive parts; and increase efficiency – and driving range – thanks to GaN's excellent intrinsic material properties.

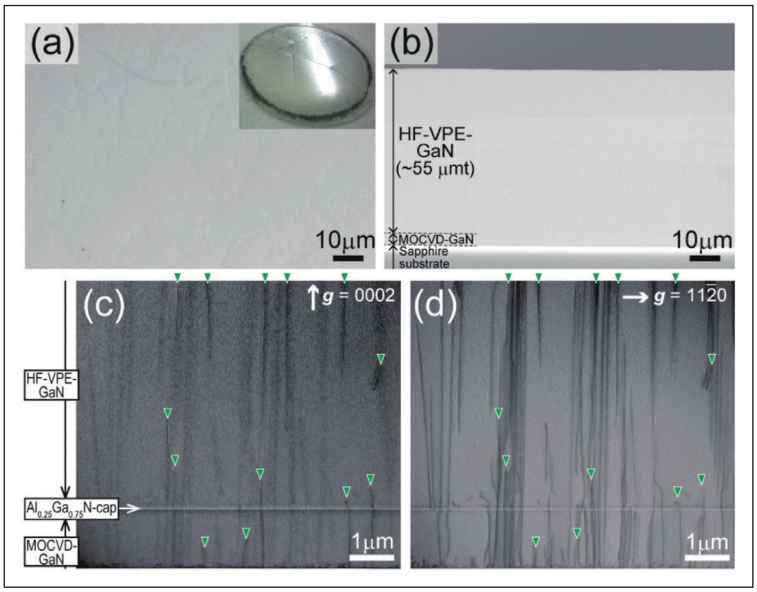
## Barriers to GaN power devices

There are two big issues relating to material preparation – that is, growth – that must be overcome to realise feasible low-cost GaN power devices. One is the development of a cost-effective GaN bulk growth method. To ensure the manufacture of high-performance highly reliable GaN-based power devices there is a need to produce large, high-quality native GaN single-crystal wafers at low cost; therefore, it is essential to develop crystal growth techniques for obtaining bulk GaN crystals.

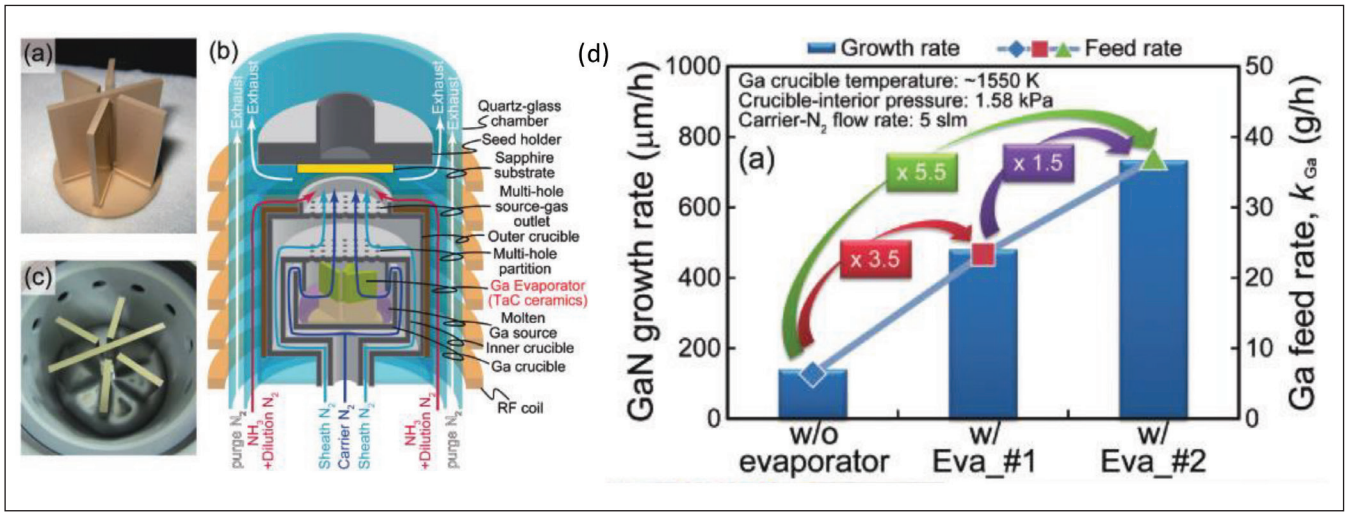
The other major issue relating to material preparation is to find a way to ensure high-purity and precise control of the dopant concentration in thick drift layers. In vertical power devices, unlike their RF counterparts, energy loss is governed by the resistive component of the *n*-type drift layer, employed to ensures a high blocking voltage. Due to this, there's a need to explore a cost-effective, highly precise GaN epitaxial growth method for drift layers.




➤ Figure 1. An illustration of the growth setup and gas-flow channels for HF-VPE. For more details see D. Nakamura *et al.* "Halogen-free vapor phase epitaxy for high-rate growth of GaN bulk crystals" Appl. Phys. Express. **10** 045504 (2017).



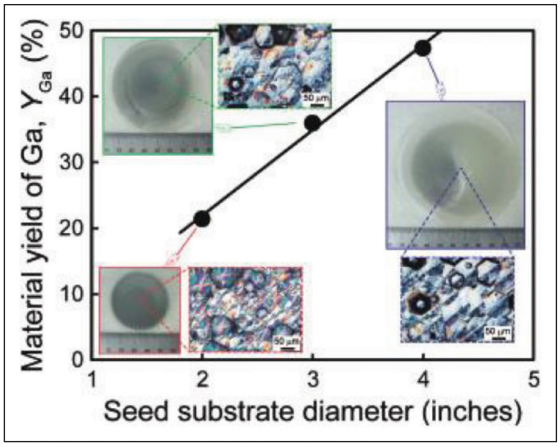

➤ Figure 2. (a) Plan-view and (b) cross-sectional scanning electron microscopy images of a thick HF-VPE-GaN layer (about 55 μm). The inset photograph shows the visual appearance of the as-grown halogen-free (HF)-VPE-GaN growth front (cracks originating from thermal stress due to the thermal expansion difference between GaN and underlying sapphire layers during after-growth cooling). Bright-field cross-sectional scanning tunnelling electron microscopy images taken from a thin HF-VPE-GaN layer (about 5 μm-thick) including the interface between MOCVD-GaN and HF-VPE-GaN layers at g vectors of (a) 0002 and (b) 11$\bar{2}$0, where mixed/edge dislocations are marked with/without green triangles. For more details see D. Nakamura *et al.* "Halogen-free vapor phase epitaxy for high-rate growth of GaN bulk crystals" Appl. Phys. Express. **10** 045504 (2017).




➤ Figure 3. (a) Photograph of as-manufactured evaporator (Eva_#2) made of TaC ceramic. (b) Schematic drawing of HF-VPE setup with an evaporator. (c) Photograph of postgrowth evaporator completely wetted with molten gallium. (d) Comparison of GaN growth rate and gallium feed rate with and without gallium evaporators. For more details see D. Nakamura et al. "Significant increase in GaN growth rate by halogen-free vapor phase epitaxy with porosity-controlled evaporator" Appl. Phys. Express. **10** 095503 (2017).

One of the difficulties associated with GaN is that it's not possible to produce crystals with the established Czochralski growth method. This approach, employed to pull a silicon crystal from molten silicon, is unavailable, because the equilibrium $N_2$ pressure of GaN is expected to exceed 6 GPa.

Due to this limitation, much effort has been devoted to developing alternative methods for producing GaN crystals, such as high-pressure nitrogen source growth, ammonothermal growth, acid ammonothermal growth, sodium-flux growth, and hydride vapor phase epitaxy (HVPE). Of these five, the first three are only appropriate for preparing the GaN seed crystals. Their low growth rates – less than 10 μm $hr^{-1}$ – are insufficient for producing boules. For the production of commercially available freestanding GaN substrates, material is grown by HVPE, which can employ growth rates of more than 100 μm $hr^{-1}$, and is capable of depositing GaN layers as thick a 1 mm on seed GaN substrates. Thanks to these strengths, freestanding wafers are produced by growing thick layers, prior to substrate removal. However, during the growth of GaN by HVPE, the reaction of gaseous GaCl with ammonia produces an unwanted by-product, $NH_4Cl$. This by-product, in the form of ash, increases maintenance costs and hampers the length of growth campaigns.




➤ Figure 4. Dependence of material yield of gallium during HF-VPE GaN growth on seed substrate diameter. Insets show images of respective as-grown samples and their surface morphologies. Hexagonal hillock structures on the surface are due to direct growth on sapphire without a buffer layer, and the blackish appearance of grown layers is due to the optical confinement effect caused by hexagonal hillock structures. For more details see D. Nakamura *et al*. "Ultrahigh-yield growth of GaN via halogen-free vapor-phase epitaxy" Appl. Phys. Express. **11** 065502 (2018).

## Eradicating halogen

To avoid this unwanted ash, our team from Toyota Central R&D Laboratory is pioneering the development of halogen-free (HF) VPE. This involves a switching of the source material from ammonia and gaseous GaCl to gallium and ammonia. Thanks to this move to halogen-free sources, our reaction produces GaN and hydrogen (see Figure 1). Our new process uses gallium vapour as the gallium source, with low pressures of around just 2 kPa enhancing gallium vapour supply.

Using this novel approach, we have demonstrated high-quality growth of GaN (see Figure 2). In addition, we have found that a porosity-controlled evaporator can enhance the molten gallium surface area, resulting in substantial increases in the gallium vapor supply and the growth rate, which can be as high as 700 μm $hr^{-1}$ (see Figure 3).

Another benefit of HF-VPE is that it leads to a higher yield. With conventional HVPE, gallium material yield is around just 10 percent. In comparison, with our growth technology, yield approaches 50 percent, thanks to a simple reaction that's free from any back reactions. This hike in yield, alongside the fast growth rate and the absence of unwanted by-products, underscores the capability of HF-VPE to deliver cost-effective growth of GaN bulk boules.

Our critical next step in the development of HF-VPE is the demonstration of thick GaN growth – that is, layers more than 5 mm-thick. To succeed, we need to address the parasitic growth of polycrystalline GaN around the seed crystal. This issue prevents lengthy growth, a pre-requisite for the production of high-quality bulk HF-VPE GaN.

We are investigating potential solutions to this issue. One is to introduce anti-parasitic reaction coatings, made from tungsten carbide, for our reactor components. Initial results are promising, with modified susceptors and crucibles ensuring a decrease in polycrystalline GaN formation around the crucibles (see Figures 5 and 6). Another idea we are pursuing, involving the use of crystal growth computer simulations, is to design a more appropriate ammonia nozzle that decreases formation of polycrystalline GaN around the GaN growth area.

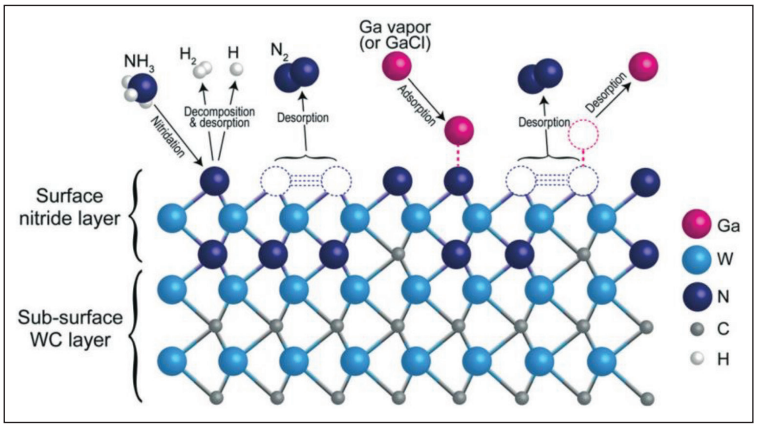
## Improving the drift layer

By far the most common method employed for the growth of GaN epiwafers is MOCVD. This epitaxial technology, offering excellent controllability in terms of thickness and impurity doping concentrations, is used for commercial production of GaN HEMTs, as well as lasers and LEDs.

As previously mentioned, the resistive component of the *n*-type drift layer in vertical GaN power devices has a large impact on energy loss. This key layer is typically around 10 μm-thick, and requires a precise control of the net carrier concentration, in the range $10^{15}$ - $10^{16}$ $cm^{-3}$.

According to the work of several researchers, carbon impurities that act as deep acceptor dopants can wreak havoc on vertical GaN power devices. The primary downside is a slashing of electron mobility that leads to mobility collapse, and in turn an extreme increase in on-resistance. Due to this, the drift layer must be grown with an impurity-free growth method. And while MOCVD is an option for this task, it suffers from several weaknesses.

The biggest drawbacks of using MOCVD for the growth of drift layers for power devices are a slow growth rate – it's typically just a few microns per hour – and high levels of carbon impurities. Addressing the latter is far from trivial, as the source of gallium is a metal-organic. Due to these issues, it is impractical to grow the drift layer of a GaN vertical power device by MOCVD.

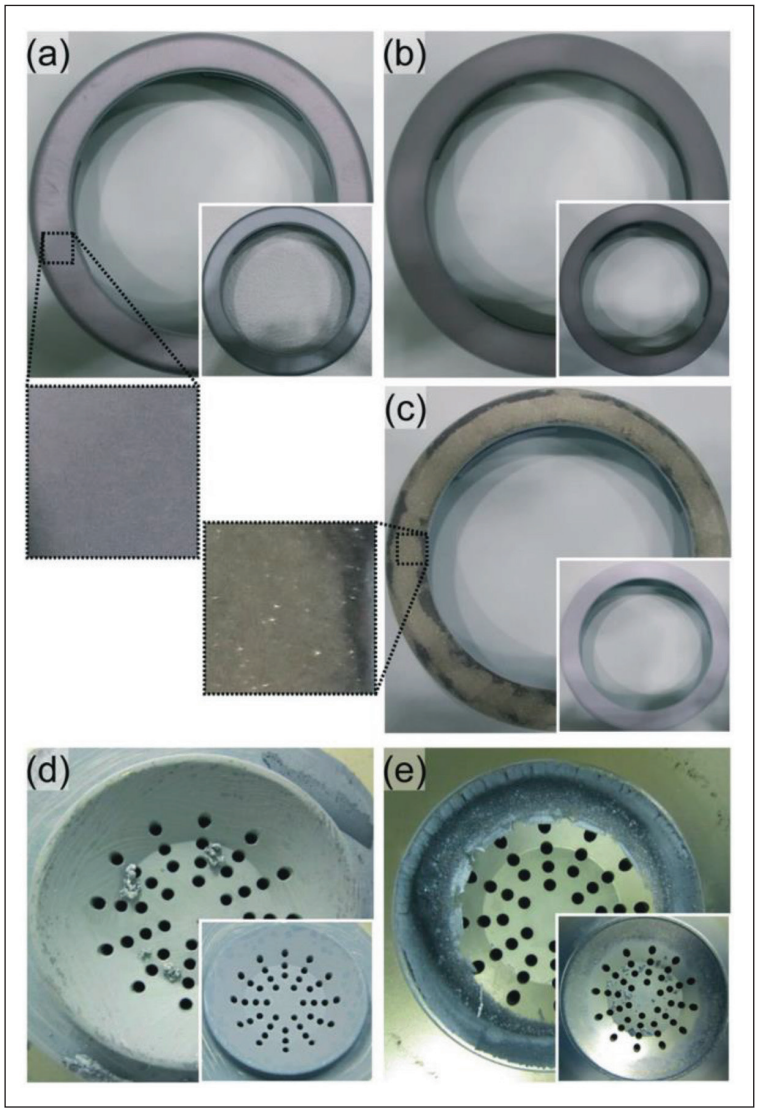



➤ Figure 5. Plausible mechanism of the anti-parasitic reaction effect of the WC catalytic layer based on surface nitride formation (accompanied by $H_2$, atomic H desorption, or both), which results in the absence of active nitrogen adsorbates (such as –NH, $-NH_2$, and $-NH_3$) for GaN formation. Surface nitrogen atoms desorb via $N_2$ formation, which can cause desorption of gallium adsorbates. For more details see D. Nakamura *et al*. "Tungsten carbide layers deposited on graphite substrates via a wet powder process as antiparasitic-reaction coatings for reactor components in GaN growth" Cryst. Eng. Comm. **22** 2632 (2020).

One alternative for the growth of a thick GaN drift layer, proposed by the Sumitomo chemical group, is to use high-purity HVPE. This approach, also known as quartz-free HVPE GaN, involves a reduction in the source zone temperature. To realise this, opaque quartz is introduced into the reactor. The refinement reduces radiative heat transmission and prevents heating of stainless steel used in the growth apparatus.

Sumitomo's approach has delivered some success, with researchers from the company demonstrating GaN with a high-purity – levels of carbon are below $1 \times 10^{14}$ $cm^{-3}$. However, the halogen gas utilised for HVPE can increase maintenance costs, due to by-products. There's the threat of a shortening of the growth apparatus lifetime, due to corrosiveness of the gas. What's more, it can be challenging to precisely control the doping level in thick layers. This issue arises because the HVPE growth condition is generally close to atmospheric pressure, making it difficult to form the sharp turn-on/off of the silicon dopant along the depth profile, due to the dopant gas's low flow speed. Furthermore, according to a team at the Institute of High Pressure Physics Polish Academy of Sciences, there are other difficulties in controlling the doping level with HVPE, due to unintentional silicon deposition inside the reactor or/and in the dichlorosilane line, used for silicon doping.

A better option for the growth of the drift layer is HF-VPE. This epitaxial technology offers high purity, thanks to the absence of carbon, and growth rates can be as high as a few tens of microns per hour. Another advantage of HF-VPE is that it's easy to use any solid source material for the dopant source.




➤ Figure 6. Photographs of 4-inch seed substrate holders made of (a) single-layer anti-parasitic-reaction-coated, (b) double-layer anti-parasitic-reaction-coated, and (c) conventional pBN-coated (for reference) graphite taken after HVPE GaN growth under identical growth conditions (seed temperature around 1080 °C; V/III ratio around 20). Gallium crucible outlets made of (d) double-layer anti-parasitic-reaction-coated and (e) TaC-coated (for reference) graphite after HF-VPE GaN growth under identical growth conditions (seed temperature around 1250 °C; partial $NH_3$ pressure 0.53 kPa; growth time of around 0.5 h). Inset photographs were taken before growth experiments. For more details see D. Nakamura *et al*. "Tungsten carbide layers deposited on graphite substrates via a wet powder process as antiparasitic-reaction coatings for reactor components in GaN growth" Cryst. Eng. Comm. **22** 2632 (2020).

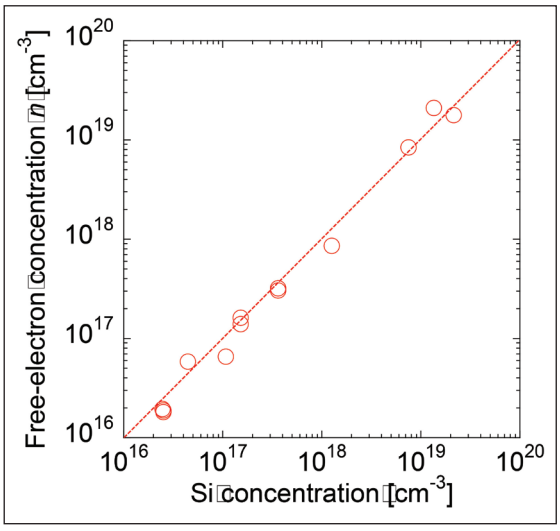
Our efforts on this front have involved silicon doping of GaN with a solid silicon source (see Figure 7). However, our initial results for electron mobility were lower than those for samples grown by HVPE, implying the possibility of large concentrations of other impurities. This finding questioned the promise of using HF-VPE for the growth of the drift layer in vertical-type power devices.

We did not give up, with further efforts identifying the source of contamination in our GaN layers grown by HF-VPE: nitrile gloves used for growth preparation. These gloves are made from nitrile rubbers that contain silicates (for example, $Mg_3Si_4O_{10}$ and calcite ($CaCO_3$)), used as fillers. During furnace maintenance, eluted contamination from nitrile gloves attaches to growth furnace parts, before entering epilayers during growth.

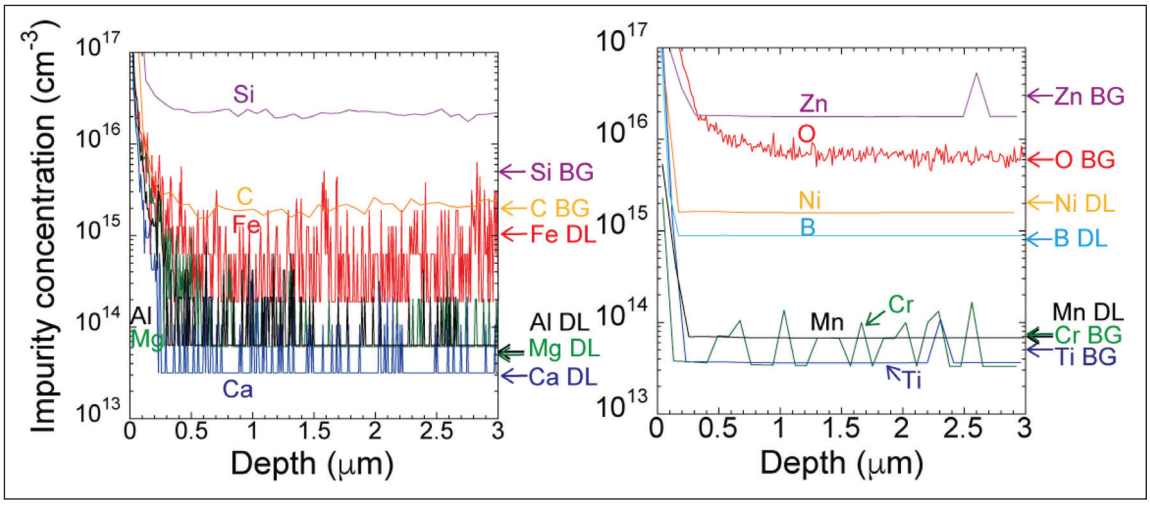
After identifying the source of contamination and eradicating it, we have demonstrated that HF-VPE can produce GaN layers similar to those produced by our revolutionary 'quartz-free' HVPE technology, in terms of growth quality and dislocation density. According to secondary ion mass spectrometry, our HF-VPE grown GaN layer has carbon and oxygen concentrations no more than $5 \times 10^{13}$ $cm^{-3}$ and $1 \times 10^{14}$ $cm^{-3}$, respectively. This form of spectrometry could not detect any boron, iron, magnesium, aluminium, calcium, chromium, zinc, nickel, manganese, or manganese in our GaN epilayer (see Figure 8).

We have also investigated carrier transport characteristics. Following the elimination of unintentional impurities, our HF-VPE grown GaN exhibits a high electron mobility (see Figure 9).

Based on characterisation of our material, we can conclude that our HF-VPE growth method is capable




➤ Figure 7. Relationship between the silicon concentration and net donor (Nd-Na) concentrations of silicon-doped-GaN grown by HF-VPE. For more details see T. Kimura et al. "Growth of high-quality GaN by halogen-free vapor phase epitaxy" Appl. Phys. Express. 13 085509 (2020).

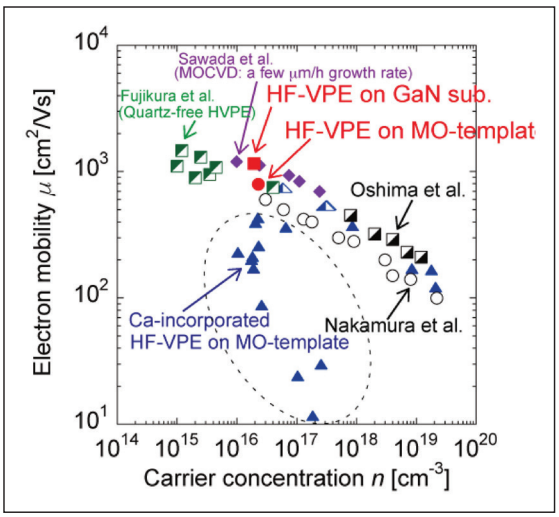



➤ Figure 8. Depth profiles of impurity concentrations in the HF-VPE GaN layer after upgrading the process. For more details see T. Kimura *et al*. "Impurity reduction in lightly doped *n*-type gallium nitride layer grown via halogen-free vapor-phase epitaxy" Appl. Phys. Lett. **124** 052104 (2024).

of growing high-purity GaN layers with a low dislocation density. Thess layers can be thick, thanks to a prolonged growth time, and are produced with a high material yield. In addition, our study provides the first experimental evidence of calcium impurities, in addition to carbon and iron, functioning as deep acceptors. We verified that it is critical to avoid these calcium impurities, as they lead to mobility collapse in lightly doped *n*-type layers.

Our plans for the future include investigating whether HF-VPE with a magnesium vapour supply is able to produce *p*-type GaN layers with enhanced control and simplicity. Success on this front would give this approach the edge over the existing HVPE method, which uses a solid MgO source. Another promise of HF-VPE is better control over doped epilayers, due to the very-low-pressure growth environment of just 1- 10 kPa.

There's no doubt that HF-VPE has great potential to provide epitaxial growth for tomorrow's GaN power device applications. A key stepping stone towards this goal is our demonstration of GaN layers that are devoid of carbon, iron and calcium impurities. Consequently, we believe that the HF-VPE growth method is a promising, cost-effective one for both bulk GaN and epitaxial GaN layers.




➤ Figure 9. Dependence of Hall mobility (mH) on carrier concentration for GaN layers at 300 K. For more details see [1] Fujikura *et al*. Appl. Phys. Lett. **117** 012103 (2020). [2] S. Kaneki *et al*. Appl. Phys. Lett. **124** 012105 (2024). [3] N. Sawada *et al*. Appl. Phys. Express. **11** 041001 (2008). [4] Y. Ohshima *et al*. Jpn. J. Appl. Phys. **45** 7685 (2006). [5] S. Nakamura *et al*. Jpn. J. Appl. Phys. **30** L1705 (1991). [6] S. Nakamura *et al* Jpn. J. Appl. Phys. **31** 2883 (1992).

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# Increasing the power-added efficiency of GaN-based HEMTs

## Better GaN channels and reduced residual silicon enable an increase in the power-added efficiency of GaN HEMTs operating at 2.45 GHz

ENGINEERS from Fujitsu are claiming to have broken the record for the power-added efficiency of transistors operating in the industrial, scientific and medical band.

The team's AlGaN/GaN HEMTs produce a power-added efficiency of just over 85 percent at 2.45 GHz, beating the previous record, also held by Fujitsu, of 82.8 percent.

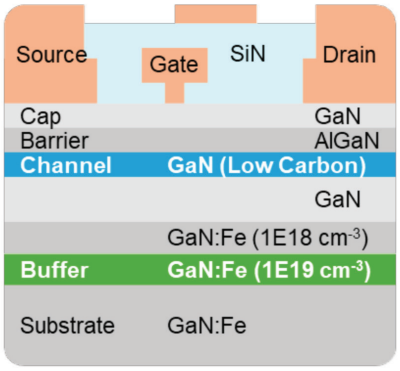
According to the team, the increase in efficiency results from improved crystal quality of the GaN channel and mitigation of effects of residual silicon at the interface between the substrate and the epitaxial layers.

For both generations of record-breaking HEMTs, Fujitsu's engineers have grown epilayers on native substrates – and for the latest devices, this has involved a 4-inch foundation.

Spokesmen for the team, Toshihiro Ohki, told *Compound Semiconductor* that while one of the benefits of using 4-inch GaN substrates is the demonstration of mass-production capability, the primary reason is that it allows the fabrication of higher-quality devices.

Fabrication of Fujitsu's latest generation of GaN HEMTs began by repeating the first step of the process used for making their forefathers, which involved chemical pre-treatment with HF acid to remove residual silicon from the surface of the GaN substrate.

This treatment, now applied to a semi-insulating 4-inch substrate with a dislocation density of less than $5 \times 10^6$ cm$^{-2}$, slashed the residual silicon concentration by two orders of magnitude, as well as the leakage current flowing laterally along the substrate surface.




➤ Increasing the concentration of iron in the buffer layer helped to increase the power-added efficiency of Fujitsu's HEMTs.

After chemical treatment, the team loaded their substate into an MOCVD chamber and deposited an iron-doped GaN buffer layer with a dopant concentration of $1 \times 10^{19}$ cm$^{-3}$.

"The iron-doped buffer itself is not new," remarked Ohki, who added: "This time, we added iron at a concentration exceeding the residual silicon in GaN-on-GaN to suppress leakage current."

To understand the effectiveness of the new buffer, Ohki and co-workers compared two samples through the use of an isolation evaluation pattern, produced by inactivating a two-dimensional electron gas (2DEG) with argon-ion implantation.

Compared with the buffer-free sample, that with the iron-doped buffer provided notably superior suppression of the leakage current.

During the growth of the epistructure, the engineers increased the III-V ratio in the GaN channel from 1600 to 8200 to reduce residual carbon and improve crystal quality.

Photoluminescence spectra, featuring a peak at around 560 nm associated with carbon-related defects, confirmed the reduction in residual carbon concentration.

To reduce the contact resistance of the ohmic electrode, Ohki and co-workers applied stripe-shaped periodic recess etching. According to the engineers, this structure ensures a more stable, lower contact resistance than a planar-type recessed structure, due to direct contact between the 2DEG and the electrodes, and the absence of a thin barrier layer. What's more, the stripe-shaped recess structure reduces the thermal budget, which can be an origin of electron traps.

Featuring a stripe-shaped recess that reduces contact resistance from 0.38 Ω mm to 0.25 Ω mm, the team's HEMTs, with a 0.5 μm gate length, produce a maximum drain current of 853 mA mm$^{-1}$ and have an on-resistance of 4.74 Ω mm.

Operating at a drain voltage of 10 V, these devices produce a maximum transconductance of 288 mS mm$^{-1}$ and have a threshold voltage of -1.77 V.

After setting fundamental and harmonic impedance to power-added-efficiency matching conditions, Ohki and co-workers determined that their HEMTs simultaneously exhibit a power-added-efficiency of 85.2 percent, a drain efficiency of 89.0 percent, and an output power of 44.04 dBm, which corresponds to a power density of 7.9 W mm$^{-1}$.

With a drain efficiency approaching 90 percent, Ohki and co-workers believe they are nearing the limit for this frequency.

Ohki added: "We intend to expand this technology to higher frequencies, such as millimeter waves."

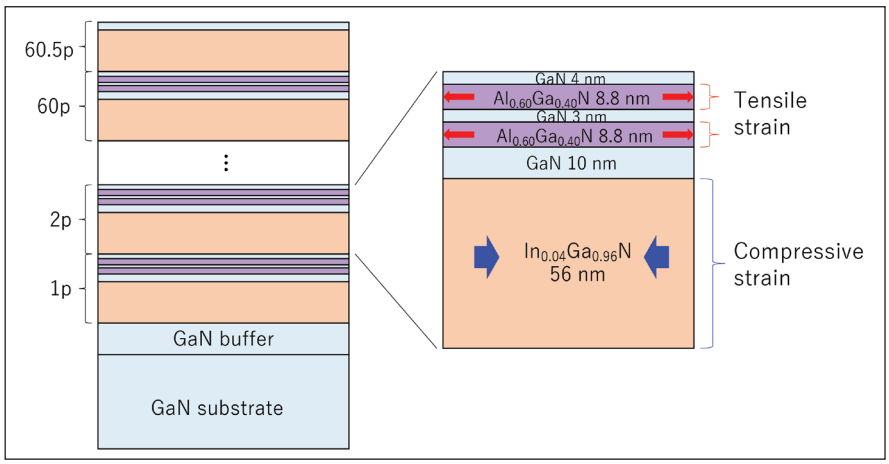
## REFERENCE

➤ T. Ohki *et al*. Appl. Phys. Express **18** 034004 (2025)

# Improving GaN-based mirrors

## A strain-balanced mirror with revolutionary dimensions improves the prospects for VCSELs made from GaN and its alloys

THE BIGGEST weakness of the GaN-based VCSEL is its mirrors – they can suffer from strain that degrades material quality, and growing these distributed Bragg reflectors (DBRs) takes many hours, making device production impractical. But there's hope that both these obstacles could be overcome, thanks to the work of engineers from Ricoh, Japan. In just 5 hours, these researchers can grow a novel, high-quality, strain compensated distributed Bragg reflector with 60.5 periods that provides a peak reflectivity of almost 100 percent.




➤ The novel DBRs from Ricoh improve the prospects for the GaN VCSEL, a promising source for retinal scanning displays and adaptive headlights.

The team's DBR, grown on a native substrate, employs an $Al_{0.60}Ga_{0.40}N$/GaN multi-layer for the low refractive-index component, and an $In_{0.04}Ga_{0.96}N$ layer as the high refractive-index component. Strain compensation results from balancing tensile strain that stems from $Al_{0.60}Ga_{0.40}N$ with compressive strain associated with $In_{0.04}Ga_{0.96}N$.

With conventional DBRs, two layers, each with a thickness equal to a quarter of the lasing wavelength (λ/4), are alternately stacked on one another. Departing from the norm, those from Ricoh have developed an asymmetric structure, pairing an $In_{0.04}Ga_{0.96}N$ layer that is thicker than λ/4 with the low-refractive-index multi-layer that's thinner than λ/4.

When designing this structure, the team decided to employ an InN mole fraction of 0.04 to prevent relaxation of the InGaN layer, which would have a thickness of several tens of nanometres. For the other mirror, the engineers initially tried AlN, but this layer suffered from pit formation, caused by island growth. To suppress this, they turned to a thin layer of GaN on top of $Al_{0.60}Ga_{0.40}N$.

Simulations show that in a conventional DBR with layers with a thickness of λ/4, deviations from this induce a phase shift that reduces reflectivity. But with the team's strain-compensated design, increasing the proportion of strained AlGaN and InGaN in the DBR and reducing the proportion of GaN produces an increase in reflectivity – that's because the increase in reflectivity, due to a higher refractive index contrast, outweighs the decrease due to phase difference.

To produce their mirrors by MOCVD, the team employed a temperature difference of just 150°C between InGaN and the AlGaN/GaN multi-layer, due to the low InGaN mole fraction. This relatively small temperature difference trimmed growth interruptions to less than 4 minutes.

Using light from a collimated halogen lamp, the team determined a centre wavelength of 440 nm for the DBR, and a centre reflectivity of more than 99.9 percent.

The team also produced a VCSEL structure featuring one novel DBR, an active region with three quantum wells, and a dielectric DBR made from 11 pairs of $Ta_2O_5$ and $SiO_2$. Optical pumping produced clear threshold characteristics.

Team spokesman Takeshi Kawashima says that with further development, it may be possible to grow a full GaN-based VCSEL that incorporates two semiconducting DBRs.

"The challenges lie in the control of electrical conductivity and growth temperature," remarks Kawashima, who explains that the use of AlGaN with an AlN mole fraction of 0.60 is expected to lead to a high electrical resistance.

"There is a possibility of achieving low-resistance *n*-type DBRs through composition grading or high-concentration doping of the AlGaN layers," explains Kawashima, but warns: "On the other hand, *p*-type GaN has very high resistance, making the realisation of practical *p*-type DBRs extremely difficult. One potential solution is tunnel junctions, but the reported tunnel junctions still have high resistance."

Kawashima reveals that the next two goals are to realise current-injection lasing and cut the growth time for the DBR. Commenting on the latter, he remarks: "We aim to minimise the temperature difference during the growth of the DBRs, ideally achieving the same growth temperature. This would allow us to grow the DBRs within 2-3 hours."

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# A debut for the vertical rutile $GeO_2$ Schottky barrier diode

## Schottky barrier diodes made with the very promising ultra-wide bandgap material rutile $GeO_2$ exhibit rectification

RESEARCHERS from Kyoto Institute of Technology are claiming to have broken new ground by demonstrating the first vertical rutile $GeO_2$ Schottky barrier diode (rutile $GeO_2$ is a tetragonal crystal structure, where $Ge^{4+}$ is bonded to six equivalent $O^{2-}$ atoms to form a mixture of corner and edge-sharing $GeO_6$ octahedra).

Putting this success in context, team spokesman Hiroyuki Nishinaka remarked: "While a Japanese venture company has shown a pseudo-vertical Schottky barrier diode on their website, it has not been published in a peer-reviewed journal with detailed information."

Nishinaka added: "While other groups have reported $GeO_2$ photodetectors, our work represents the first vertical power device demonstration."

Like its cousin, $Ga_2O_3$, rutile $GeO_2$ has an ultra-wide bandgap that ensures a high critical electric field, and makes this oxide a promising material for producing power devices.

But in addition to this similarity, rutile $GeO_2$ has several advantages over $Ga_2O_3$. Most notably, theoretical work suggests that rutile $GeO_2$ can doped both *n*-type and *p*-type.

According to these calculations, despite relatively high acceptor ionisation energies, co-doping strategies have the potential to increase acceptor solubility to enable hole conduction through an impurity band. "In contrast, β-$Ga_2O_3$ faces significant challenges with *p*-type doping due to its intrinsic material properties, and has not been successfully *p*-type doped to date," argued Nishinaka

He and his co-workers have produced vertical rutile $GeO_2$ Schottky barrier diodes on niobium-doped $TiO_2$ substrates, as native substrates are not commercially available.

"However, researchers at IKZ in Germany have reported highly conductive antimony-doped bulk rutile germanium oxide, suggesting that native substrates suitable for power device applications may become available in future."

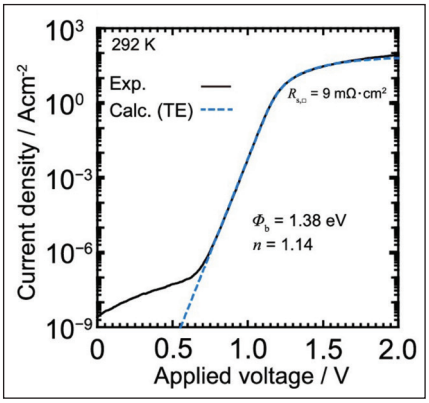
The team used mist-epitaxy to deposit their epistructure at 850°C. This consisted of an antimony-doped, graded $Ge_ySn_{1-y}O_2$ buffer layer and an unintentionally doped rutile $GeO_2$ layer.

"We use mist CVD for growth because I am one of the researchers who developed mist CVD at Kyoto University, so we have extensive expertise with this technique," explained Nishinaka. "Mist CVD has particular advantages in early-stage materials research because it can utilise any material that can be dissolved in solution. While MOCVD is also suitable – and has been used to grow rutile germanium oxide – mist CVD offers advantages in materials exploration."

Secondary ion mass spectrometry has revealed that the buffer is 149 nm-thick and the $GeO_2$ layer has a thickness of 198 nm. This technique also determined that antimony diffuses from the buffer into the $GeO_2$ layer, possibly due to defect-assisted diffusion mechanisms, such as dislocations or point defects.

After cleaning the samples, the team turned to evaporation to add nickel Schottky contacts with a diameter of 320 nm.

Electrical measurements determined:




➤ Forward current-voltage characteristics of the vertical rutile $GeO_2$ Schottky barrier diode, showing clear rectification behaviour.

clear rectifying behaviour, with a rectification ratio of 6 x $10^5$ at ± 2 V; an on-resistance of 9 mΩ cm², a value that is consistent with the resistance of the substrate; an ideality factor of 1.14; and a Schottky barrier height of 1.38 eV.

One of the weaknesses of the Schottky barrier diode is its relatively high reverse-leakage current, possibly due to a leakage path.

According to the team, improvements in epitaxial growth are needed to determine whether the reverse leakage current mechanism in ideal rutile $GeO_2$ can be accurately described by the thermionic emission model, which has already been successfully applied to 4H-SiC, GaN and β-$Ga_2O_3$.

Progress with rutile $GeO_2$ also hinges on reducing dislocations and/or point defects and realising uniform doping control in thick epilayers.

"Our next goals focus on achieving reliable *p*-type doping to realise *p-n* junction devices, ultimately leading toward MOSFET development for rutile germanium oxide," remarked Nishinaka.

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## Up to 40% Deposition Efficiency

With gold at an all-time high, optimizing the collection of gold during thin film deposition is more crucial than ever for cost-effectiveness and operational efficiency in semiconductor manufacturing.

Ferrotec's Coating Platform with patented HULA system provides an alternative lift-off compliant wafer motion to traditional box coaters. By providing planetary motion to the wafers during deposition, HULA eliminates the need for masks and enhances the collection efficiency and uniformity of the deposited material.

Visit: www.temescal.net/auratus-gold
Contact: thinfilmsolutions@ferrotec.com


## DIG UP THE SAVINGS!

| | Conventional Box Coater | Ferrotec UEFC-5700 |
|---|---|---|
| **Performance** | | |
| Wafers Per Batch | 20 | 42 |
| Batches Per Day | 15 | 20 |
| Wafers Per Day | 300 | 840 |
| **Operational Cost of Unreclaimed Gold*** | | |
| Cost of gold perf wafer | $19.28 | $9.60 |
| Cost of 100,000 wafers | 1,928,000 | $960,000 |

**Assuming $110/gram and reclaim cost of 80%*



FerroTec