COMPOUND SEMICONDUCTOR

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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

Aided by AI

THERE are some abbreviations that I assume you all know. In this publication I don't spell out LED, MOCVD or MBE – and more recently I have added AI to what is a relatively short list.

AI featured in talks given by many of the presenters at this year's CS International, as it's widely viewed as a driver of future sales. As this technology evolves, more powerful data centres will appear, running as efficiently as possible, thanks to wide bandgap power electronics and numerous optical links. Due to this, tomorrow's data centres promise to provide a ramp in sales for GaN and SiC power devices, and lasers and microLEDs.

Thanks to these lucrative opportunities, there has been a phenomenal increases in the valuation of companies at the top of this year's *Compound Semiconductor Share Price Leaderboard* (see p. 34).

After several years of footing this table, AXT is now in top spot, thanks to a rise in its share price of more than 5000 percent over the last 12 months. Eye-watering gains have also been made by Lumentum and IQE, two other players heavily involved in the supply chain for the manufacture of InP lasers, a workhorse for optical links.

For those of you with long memories, are there similarities to the expansion of the dot.com bubble? Remember JDSU, the optical components maker that had a peak valuation of just over $56 billion. Its share price plummeted by over 99 percent, from a peak of more than $1200, when the dot.com bubble burst at the beginning of this century.

During the inaugural rump session at AngelTech, attendees discussed the possibility of a bursting AI bubble. However, given that the leaders of various AI platforms are driving data-centre buildout, and will be fighting tooth and nail to dominate this sector, it's hard to see a fall in demand for

infrastructure components. What's encouraging is that a number of multi-year supply agreements are already in place to support long-term growth for all involved in these supply chains.

So maybe we should see today's AI in a similar vein to the early years of mobile communication, when many bought their first handset. Back then, business and consumer demand funded advances in technology, with next generations of mobile infrastructure, operating at ever faster data rates, providing long-term markets for a variety of compound semiconductor devices.

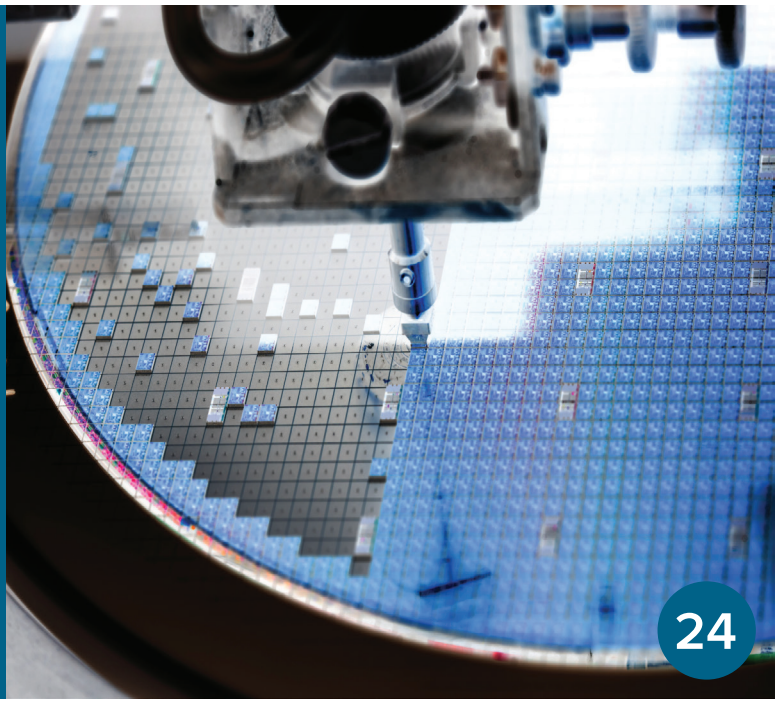
There's no question that AI will continue to advance, underpinned by higher-performing data centres, deploying superior devices. That's good news for our industry – and while it's unlikely to fuel phenomenal increases in share price seen in the last year or so, it should provide substantial sales for power and optoelectronic manufacturers for many years to come.

CS COMPOUND SEMICONDUCTOR

COVER STORY

Strengthening the world's first CS cluster

Underpinning recent success in the South Wales cluster is a five-year programme backed by £43 million. It's supported the scaling of epitaxy to 200 mm, a new power electronics capability, and the construction of a robust talent pipeline



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AI optical transceivers to net $26 billion in 2026

Component shortages are primary capacity bottleneck, says TrendForce

TRENDFORCE'S latest research indicates that the global market for AI-focused optical transceivers has entered a phase of rapid growth, with market size projected to expand from $16.5 billion in 2025 to $26 billion in 2026, representing over 57 percent YoY growth.

This surge is driven not only by specification upgrades but also reflects a broader structural reshaping of the optical communications supply chain amid accelerating AI data center deployment.

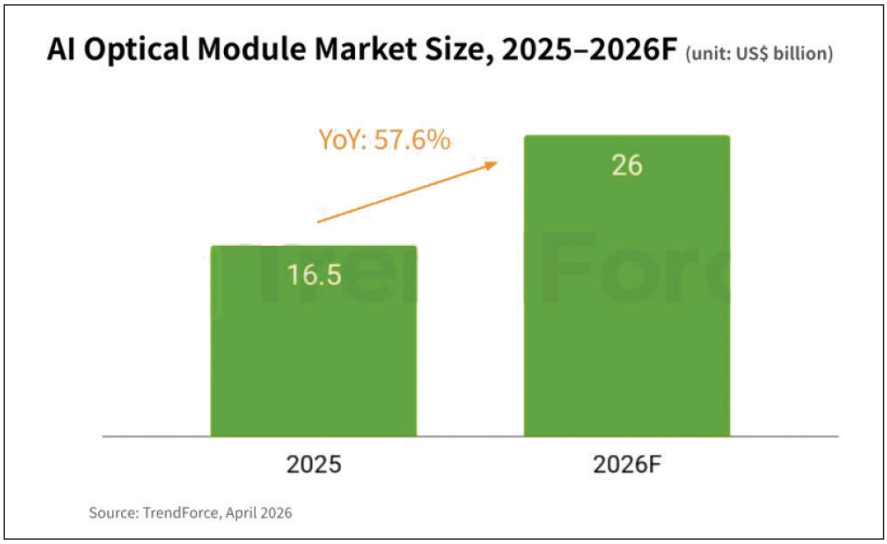
Demand is rising sharply for 800G and above optical transceivers used in AI server cluster interconnects as AI data centers continue to scale.

Traffic at hyperscale data centers in North America has sustained over 30 percent annual growth, prompting cloud giants such as Google, Microsoft, and Meta to expand GPU and AI server deployments. This has further boosted procurement of high-speed optical interconnects. Meanwhile, supply-side pressures are becoming increasingly evident.

TrendForce notes several key bottlenecks constraining capacity expansion. First, the supply of critical optoelectronic chips, such as electro-absorption modulated lasers (EMLs) and continuous-wave lasers, remains tight due to capacity allocation constraints.

Additionally, high-precision manufacturing processes, including optical alignment, limit scalable production. Power consumption and thermal management challenges also continue to affect system design and deployment timelines.

Upstream suppliers, led by Nvidia and major system vendors, are mitigating supply risks by shifting procurement strategies and adopting strategic



long-term agreements to secure key components and reduce reliance on spot-market purchasing. Meanwhile, technology roadmaps are accelerating toward low-power linear pluggable optics (LPO) and silicon photonics integration, aiming to replace traditional high-power DSP-based architectures and alleviate power and thermal constraints.

TrendForce further observes that growth in the AI optical transceiver market is shifting from single-product upgrades to three parallel drivers: market expansion, generational technology transitions, and application diversification. As the 1.6T generation gradually enters mass production, demand for edge computing and data center interconnect will also drive expansion of the 800G and 1.6T ZR/ZR+ coherent optical module markets.

Traffic at hyperscale data centers in North America has sustained over 30 percent annual growth, prompting cloud giants such as Google, Microsoft, and Meta to expand GPU and AI server deployments

In response to tightening component supply, leading international players such as Coherent, Lumentum, and Applied Optoelectronics, along with Taiwanese firms such as Elite Advanced Laser Corporation and LuxNet Corporation, have initiated capacity expansions and technology deployments.

The upgrade cycle offers significant structural growth opportunities for Taiwan's optical communications supply chain. Taiwanese firms have established solid capabilities in foundry services, EML laser chips, passive optical components, and module packaging and testing, with ongoing advancements in silicon photonics and LPO technologies. The years 2026 to 2027 are crucial for establishing a foothold in the 1.6T supply chain, where success in design-in at tier-one customers will likely be a key factor in determining future market share.

IQE secures £81 million investment led by Macom

Strategic review is over and IQE is no longer considered to be 'on offer'

UK COMPOUND SEMICONDUCTOR wafer firm IQE plc has announced a strategic investment from semiconductor maker and existing customer Macom Technology, along with other existing shareholders, raising gross cash proceeds of around £81 million.

Jutta Meier, CEO of IQE, commented: "This proposed transaction is transformational for IQE. The investment from Macom and other existing shareholders will provide the balance sheet strength to allow us to capitalise on the opportunities in front of us, while maintaining our unique global footprint."

Meier added: "We are now better positioned than ever to execute on our growth strategy, including in key technologies, such as indium phosphide and gallium nitride. We look forward to delivering value for shareholders with continued fiscal rigour and by serving our global customer base through operational excellence."

The proceeds of the fundraising will be used to repay existing bank debt, redeem existing loan notes and strengthen the balance sheet, ensuring the group has a strong capital position from which to fund operations and investments in its core technology.

As a result, the company's board is ceasing its Strategic Review and following this announcement, IQE is no longer considered to be in an 'offer period'.

Alongside the investment, IQE and the Macon will enter into long-term strategic supply agreements on completion enabling scalable, high-volume manufacturing across key growth segments.

Mark Cubitt, chair of IQE, commented: "This is an incredibly exciting time for IQE. I am pleased we have concluded the Strategic Review after a thorough process, achieving a fantastic outcome for all stakeholders. Today's announcement is a recognition of the intrinsic value of the company and its importance in key growth segments. This fundraise removes debt presures and leaves the group with a capital structure to enable future growth."

Stephen Daly, CEO of Macom, commented: "As a longstanding customer, Macom believes this transaction will allow IQE to realise its full potential in technology, operational execution and financial performance."

US ITC rules on Infineon and Innoscience patent case

Orders import and sales bans for GaN products against Innoscience in the US. Innoscience defends its position

THE Full Commission of the US International Trade Commission (ITC) has affirmed the ITC's ruling from December 2025 that Innoscience infringed an Infineon patent (US Patent No. 9,899,481) covering a lateral GaN transistor device featuring a package with source-sensing functionality.

The ITC has confirmed the patent's validity and ruled that Innoscience infringed it, leading to import and sales bans on the infringing, concerning GaN technology and ordered import and sales bans against Innoscience. The decision and the bans are subject to a 60-day review period of the US President.

"This decision once again highlights the robustness of Infineon's intellectual property. It reinforces our commitment to actively protect Infineon's patent portfolio and uphold fair competition in the industry," said Johannes Schoiswohl, SVP and head of GaN Systems business line at Infineon.

"With our industry-leading 300-mm GaN manufacturing, we are uniquely positioned to scale innovation and deliver the performance, quality, and cost advantages that our customers need to accelerate decarbonisation and digitalisation," he continued.

In a parallel dispute in Germany, Infineon is asserting infringement of three patents and one utility model in the Munich District Court.

In August 2025, the Munich court found infringement of the first Infineon patent by Innoscience. Trials for another patent and a utility model are scheduled in June 2026.

Meanwhile, Innoscience has pointed out that this latest ruling also affirmed the Judge's finding of no violation of US Patent No. 9,070,755 and confirmed that Innoscience's redesigned products – now embodied in its current commercial offerings – fall outside the scope of US Patent No. 9,899,481.

The Commission also invalidated four additional claims of the '481 patent. Innocience adds that only two claims of the '481 patent were found valid and infringed, and only with respect to legacy products that are no longer manufactured or sold.

As a result, the associated import ban has no practical impact on Innoscience's US business. Innoscience will continue supplying its existing GaN power products to US and worldwide customers uninterrupted.

Innoscience has asked the US Patent and Trademark Office to initiate review of the remaining two claims and is confident they will likewise be invalidated.

The disputes look likely to continue.

Canada to spin-off compound semi fab

THE Canadian government has decided to spin-off the only end-to-end pure play compound semiconductor wafer manufacturing facility in Canada, with the aim of creating a commercial entity with Canadian foundations and Canadian industrial development at its core.

Located at the National Research Council of Canada in Ottawa, the Canadian Photonics Fabrication Centre (CPFC) is a 40,000 square foot facility including 11,000 square feet of class 100/1000 clean room space.

It works with clients from start to finish on design refinement, fabrication and testing of compound semiconductor wafers using materials such as InP, GaAs and GaN for photonics applications in networks, defence and aerospace, medical imaging, data centres and advanced AI computational infrastructure.

Since 2021, Canada has invested over $115 million to expand and modernise the CPFC. In 2023, construction started on a new 8,000 square-foot building with state-of-the-art facilities, set to enhance competitiveness and support AI infrastructure, tele/data communications and defence supply chains.

Veeco wins InP tool orders worth over $250 million

AI scaling is driving demand for Spector, Lumina and WaferEtch wet processing systems

VEECO INSTRUMENTS has announced that it has received orders totalling more than $250 million from multiple customers for its Spector Ion Beam Deposition (IBD), Lumina MOCVD and WaferEtch wet processing systems. These orders, driven by momentum in silicon photonics, support the manufacturing of InP lasers, with deliveries beginning in 2026 and significantly accelerating in 2027.

According to Veeco, a substantial portion of the orders are for Spector IBD from manufacturers of 800G and 1.6T optical transceivers for hyperscale data centres. Spector IBD is used to deposit high-performance, low-absorption laser facet coatings that are required for high-power laser operation.

Recent industry commentary has highlighted InP laser manufacturing as a key bottleneck for AI infrastructure scaling, driven by limited qualified capacity and complex process integration.

"Veeco's differentiated portfolio of ion beam, MOCVD and wet processing technologies enables our customers to scale up advanced InP laser production with high performance, yield, and reliability," said Adrian Devasahayam, SVP of Veeco Instruments. "These orders reflect the strength of our long-standing customer partnerships, many spanning more than two decades, and our ability to support the evolving requirements of silicon photonics and the optical interconnect market."

Cyient launches India's first GaN power IC family

650 V DPAK GaN devices for edge AI computing and e-mobility are based on Navitas GaN technology

INDIAN COMPANY Cyient Semiconductors has announced the launch of seven new GaN power devices for the Indian market, developed using Navitas Semiconductor's GaN technology.

The DPAK devices combine drive, control, and protection functions, with integrated EMI management and current sensing.

This is Cyient's first commercial GaN product family and hailed as a major milestone in advancing India's domestic power semiconductor ecosystem. The new portfolio is designed to address the rapidly growing demand for high-efficiency, high-power-density solutions across AI data centres, telecommunications, consumer fast charging, industrial power systems, and e-mobility platforms.

Building on the collaboration with Navitas, announced in December 2025, the partnership enables customers in India to access commercially available GaN power solutions with enhanced local support, supply assurance, and alignment with emerging domestic sourcing initiatives.

Under the agreement, Cyient Semiconductors will license Navitas's GaN technology for use in India, accelerating the adoption of high-performance GaN solutions across a broad range of markets. In addition, Cyient Semiconductors will serve as a second source for select Navitas GaN devices already in mass production and strengthen supply chain resilience.

Over time, the licensing agreement with Navitas Semiconductor is expected to enable the domestic manufacturing of GaN power devices in India.

Suman Narayan, CEO, Cyient Semiconductors, said: "With this launch, Cyient Semiconductors is introducing its first family of GaN power ICs, marking our entry into high-performance power semiconductors with a strong roadmap for expansion."

"Built on Navitas' proven GaN platform, these highly integrated devices are designed to accelerate adoption and support next- generation power applications. This represents the foundation of a broader GaN portfolio that will address the growing power and efficiency demands of AI infrastructure, industrial systems, consumer power, and e-mobility applications."

Chris Allexandre, president and CEO of Navitas Semiconductor, said: "India is a key market in Navitas's high growth, high power strategy with Navitas 2.0. This launch furthers our vision of a robust local supply chain and manufacturing in India for the governments 'Make in India' initiatives. The partnership with Cyient delivers a strong local support infrastructure for our customers as we pivot our India strategy to focus on GaN-based product enablement and customer success."

Cyient Semiconductors expect to begin sampling the first set of GaN power products by June 2026.

InPhred closes $4 million seed round

US-based InPhred has completed a $4 million seed funding round to accelerate commercialisation of its patented nanoporous InP DBR technology.

The company say this will enable SWIR (short wave infrared) VCSELs for the first time at commercial scale. Funds are being deployed toward SWIR VCSEL product development, digital health prototype validation, and expansion of the company's foundry and ODM partner network across the US and Taiwan.

The company says it is is also actively developing custom solutions for Tier 1 OEM partners in AR/VR and digital health, and is seeking $20 million or more in Series B follow-on capital to pursue three market segments in parallel.

The company's DBR devices are engineered with alternating dense and nanoporous layers to create refractive-index steps of up to about 40 percent (exceeding AlGaAs/GaAs contrast) on standard foundry-grown InP or GaN epi. No exotic materials or wafer fusion are required.

The technology is said to be drop-in compatible with volume manufacturing, with the porosification step a single post-epi electrochemical process added to a conventional wafer-level flow.

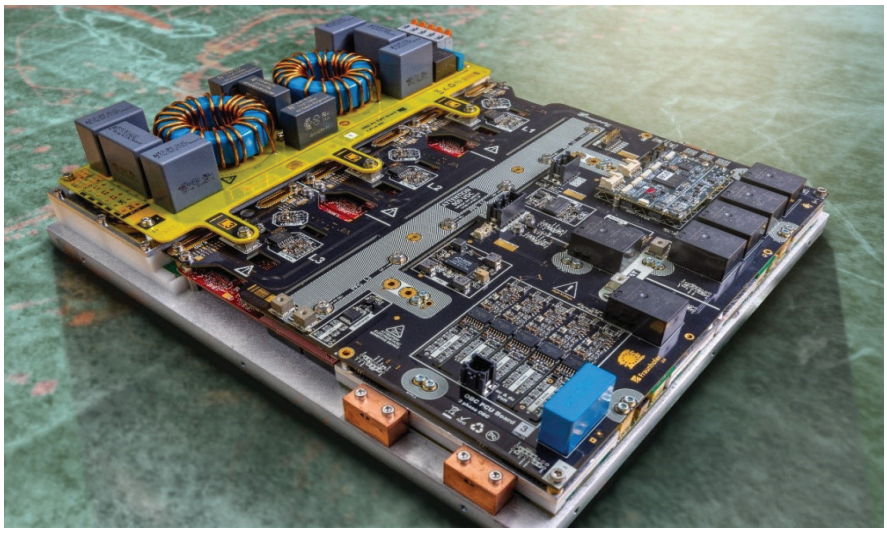
EU project develops next-gen on-board chargers

Bidirectional GaN helps shrink 22 kW OBC volume by two thirds

EVs should be powerful, better for the environment, and affordable. However, the chargers built into them are hindering progress, as current models are reaching their limits in terms of efficiency, size, and reliability.

The EU-funded HiPower 5.0 project aims to revolutionise this technology by harnessing the advantages of GaN and wide-bandgap semiconductors in market-ready products within a fully European value chain.

Most recently the Fraunhofer Institute for Reliability and Microintegration IZM (which is overseeing the HiPower 5.0 consortium) has produced a powerful 22 kW on-board charger (OBC) with a total size of only 4 litres – far smaller than the current market average of 12 litres.



The innovation revolves around bidirectional GaN chips provided by Infineon. These monolithically integrated switches enable more efficient conversion in a smaller package, since a single component does the work two. In addition, using Fraunhofer IZM's experience in packaging and system development, several electronic components have been embedded directly into the OBC's circuit boards, which shortens critical paths, reduces potential losses, and saves space overall. Fraunhofer IZM first exhibited an early version of the charger, without bidirectional GaN components, two years ago at the 2024 PCIM Europe.

Since August 2025 (finishing in June 2028), the consortium has been working on six use cases, including applications in the marine shipping industry, supported by €33.7 million in funding from the EU and its member states. The German Federal Ministry of Research, Technology, and Space is contributing €5.74 million and the Free State of Saxony is contributing €0.12 million. The HiPower 5.0 project brings together partners from ten European nations, including two OEMs, 21 tier-1 and tier-2 suppliers, six specialists for power electronics, ten universities, and seven research institutions.

Bosch launches 3rd generation SiC MOSFETs

Bidirectional GaN helps shrink 22 kW OBC volume by two thirds

BOSCH has announced its third generation SiC MOSFETs, based on the company's dual-channel trench SiC architecture with lower on-resistance, better ruggedness, and smaller chip sizes for broader EV adoption.

A 20 percent reduction in specific on-resistance, around 10 percent higher short-circuit withstand capability, and a 40 percent thinner die enable clear efficiency gains and more cost-effective power module designs, according to the company.

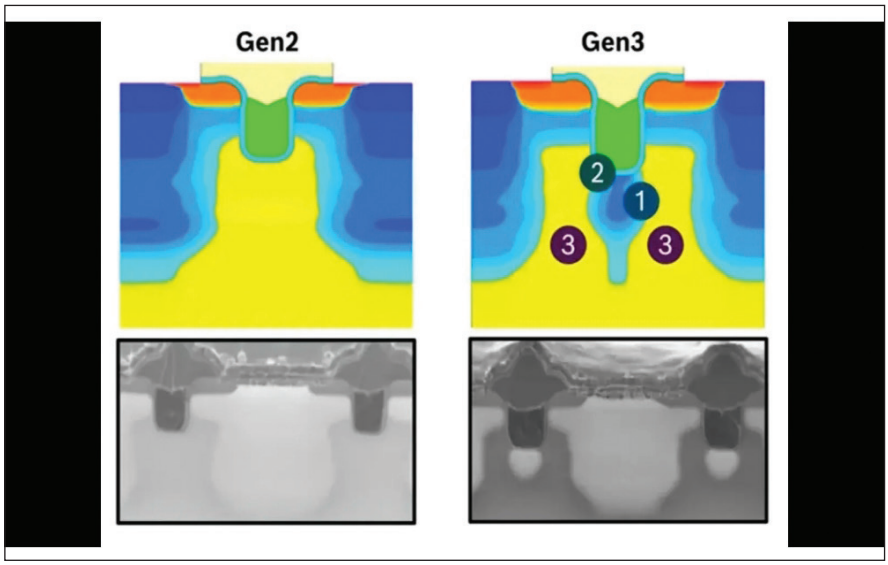
At the same time, the reduced die size has a direct impact on production efficiency and system-level costs, further supported by the transition to 200 mm wafer manufacturing, which increases chip output per wafer.

While Bosch's SiC chips are well-established in the demanding environment of high-performance electric vehicles, the company says these new features change the economic equation around SiC chip uses, enabling compact, efficient inverter and power module designs across a wider range of EVs from premium sports cars to mass-market models.

Gen 3 SiC MOSFETs offer measurable improvements in three key areas for automotive applications: electrical performance, thermal performance, and ruggedness.

In terms of thermal performance, reducing die thickness by 40 percent directly enhances heat dissipation and thermal conductivity. This supports higher power density and more efficient thermal management in high-performance semiconductor systems.

For ruggedness, the short-circuit withstand capability increases by about 10 percent, supported by the optimised two-zone JFET region and enhanced



gate oxide design. The design also improves robustness against parasitic turn-on at high switching speeds.

Additionally, the intrinsic body diode is optimised for soft recovery behaviour across the full automotive temperature range of -40°C to 200°C, reducing electrical stress during switching events and supporting stable operation under demanding conditions.

Three specific advancements in Gen 3 SiC-MOSFET architecture are shown in the diagram above including the trench (green), the new shield implant below the trench (blue), and the two-zone JFET region (yellow).

First, additional *p*-type shielding region introduced directly below the trench, provides full protection against off-state electric fields. This contributes to improved long-term gate oxide reliability under typical operating conditions. The existing hard mask of the trench etching process was reused for the new trench shield implant, eliminating the need for an additional lithographic process step.

Second, two-zone structure in the JFET region beneath the trench is such that each channel now corresponds to its own JFET region, providing significantly finer control over electric field distribution during both normal operation and fault events.

This improves the critical trade-off between on-resistance (R_{onA}) and short-circuit withstand time, expanding the available design space for robust, high-performance SiC power semiconductors.

Third, the die thickness in Gen 3 is reduced by 40 percent to only 100 µm. This reduces material usage and places the active semiconductor layer closer to the heat sink, accelerating heat dissipation.

Anne Bedacht, head of product management for power semiconductors at Bosch commented: "The Gen 3 upgrades are noteworthy for two reasons: their combined effect and how our engineers integrated them into well-established production processes."

Bedacht added: "Our design-for-manufacturability approach ensures that Gen 3 is production-ready and cost-effective from the outset."

MicroLED transceiver supply chain alliances take shape

MicroLED co-packaged optics market to reach $848 million by 2030, scaling fast in the second half of 2028, says TrendForce

TRENDFORCE'S latest research into the microLED industry highlights how generative AI is driving rapid growth in demand for high-speed optical communications, with the microLED emerging as one of the three major short-distance, high-speed intra-rack transmission solutions.

MicroLED technology offers power consumption as low as 1-2 pJ bit^{-1} and ultra-low bit error rates (BER) of no more than 10^{-10}. It's also emerging as one of the three major short-distance, high-speed intra-rack transmission solutions for scale-up data centre networks, alongside active electrical cables (AEC) and VCSEL-based near-packaged optics (VCSEL NPO).

As a result, TrendForce projects that the microLED CPO optical transceiver market will reach $848 million by 2030. Global supply chain players are expanding into optical communications and optical interconnects. Microsoft has introduced the Mosiac microLED co-packed optics (CPO) architecture, while MediaTek provides integrated active optical cable solutions. AEC leader Credo Technology Group acquired Hyperlume in 3Q25 to broaden its optical interconnect portfolio.

Global Micro LED CPO Alliance Overview

Leading Player	Microsoft	Avicena	Credo	AUO	Innolux	GIS	PlayNitride Brillink	HC SemiTek	Marvell
Partners	MediaTek Porotech InnoLight	ams OSRAM TSMC	Hyperlume (acquired by Credo in 3Q25)	Ennostar Tyntek	bEMC Brillink Artilux	Porotech Foxconn	Artilux	Shanghai New Vision Microelectronics	Mojo Vision

Startup Avicena has developed its ultra-low-power LightBundle technology and is preparing to launch a 512 Gbit s^{-1} microLED optical interconnect solution, with an 896 Gbit s^{-1} version scheduled for advancement in 2Q26 to further improve data-transmission efficiency and power consumption.

Meanwhile, Ams Osram has signed a development agreement with a leading global AI data centre infrastructure partner to accelerate the commercialisation of microLED optical interconnects.

Its in-house solution – targeted for launch in 2027 – is expected to integrate microLED chips, optical components, and dedicated ASICs.

In Taiwan, AUO is combining technologies from Ennostar and Tyntek to launch microLED CPO on glass redistribution layer interposers. Innolux is also expected to use resources from bEMC to gradually enhance its vertical integration and competitive edge. PlayNitride has already partnered with Brillink to expand into this sector. In China, HC Semitek has collaborated with Shanghai New Vision Microelectronics to develop microLED optical interconnect technologies.

Shipments of microLED CPO optical transceivers are expected to begin scaling significantly in the second half of 2028, eventually contributing approximately $848 million in market value by 2030.

Seoul Viosys eyes the AI data centre market

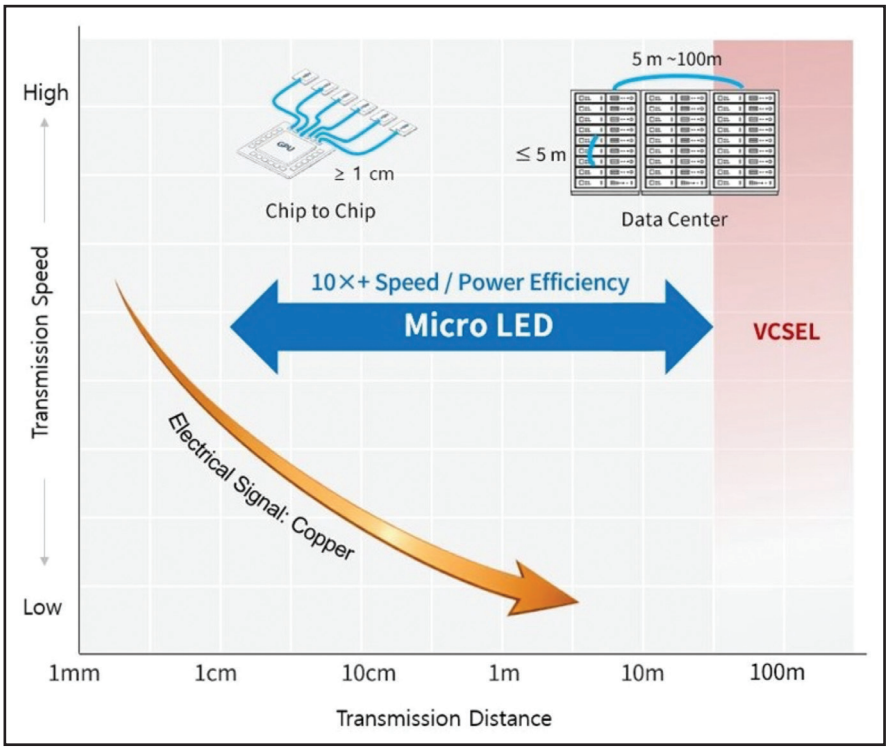
Company is expanding partnerships to provide a total transceiver solution

AS AI drives the shift in data centres from copper-based to optical-based architectures, opto-semiconductor specialist Seoul Viosys has announced that it is accelerating its entry into the next-generation photonics market supported by its 'No-wire' and 'No-package' patents and its competitiveness in VCSEL technology. The company is also expanding its business model beyond component supply into a total transceiver solution provider for data interconnects.

Seoul Viosys is currently in discussions with two global leaders in data interconnects on joint technology development, as well as potential joint ventures or OEM manufacturing. The company is also exploring expanded collaboration with additional partners in the US and Japan. Rather than simply supplying individual components, Seoul Viosys says it is securing a network of strategic partners to establish its position as a total-solution provider in the data interconnect transceiver market, spanning design, devices, drivers, and modules.

Seoul Viosys believes it's in a strong position, underpinned by its patented opto-semiconductor device technologies. In particular microLED-based photonic technology enables efficient, high-speed transmission of large volumes of data, making it well-suited for high-density infrastructure, such as AI data centres. This low-power, ultra-high-speed communication technology is expected to become essential across future applications, including autonomous vehicle communications and physical AI robotics.

Second, the company has WICOP, a proprietary technology that eliminates the need for both wires and packaging. This robust structure maximises light extraction efficiency while enhancing thermal management, enabling high efficiency, even at ultra-small scales down to the 1 μm level.



Third, the company says its strong patent barrier is a key competitive advantage. Seoul Viosys, including its subsidiaries, holds approximately 1,800 micro opto-semiconductor patents related to optical communications.

Built around these patents, the company has established a broad and defensible scope of rights, making it extremely difficult for competitors to develop products without infringement. For example, in February, its US subsidiary SETi secured a permanent injunction from a US court against a photonics company with a 40-year history in optoelectronics. Beyond patent volume, the portfolio comprehensively covers core processes, structures, and implementation methods, providing a solid foundation for technological leadership.

The parent company, Seoul Semiconductor, also holds a portfolio of approximately 15,000 patents in opto-semiconductor packaging and solutions.

Despite years of operating losses, Seoul Viosys has invested tens of millions of dollars annually in microLEDs under its vision of 'writing a new history of light', steadily strengthening its technological competitiveness. The company has also collaborated for more than 20 years with a research team at the University of California, Santa Barbara, led by Nobel Prize in Physics laureate Shuji Nakamura and Steven DenBaars, and completed development of an ultra-small 1-μm-class device in 2021.

Dae-Woong Suh, president and head of R&D at Seoul Viosys, said, "We have built production infrastructure in the United States, Vietnam, and Korea, and are also seeking new partners in India, while strengthening our capabilities in technology collaboration and supply chain response. We are open to working with companies that need our technology, and under strict confidentiality, we will introduce breakthrough products together with our partners."

MBE IS OUR DNA

Global market leader for research and production

MBE not only changes how we do it, it also changes what we can do.

Riber is the world leading supplier of MBE processing equipments and related services.

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CS INTERNATIONAL CONFERENCE

Another surge for SiC

Very fast charges for EVs, alongside power infrastructure for data centres, will provide the next big opportunities for SiC

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AT THIS YEAR'S CS International, onsemi's Senior Director of Technical Marketing, Mrinal Das, gave a wonderfully succinct synopsis of the next big opportunities for SiC. He described the next frontier as sustainably scaling the megawatt mountain.

"Driving a lot of this change is improving our quality of life through being more productive," argued Das, who expanded on this point by saying that SiC power electronics has a crucial role to play in trimming the time it takes to charge an EV, and helping to advance AI data-centres through better power supply.

According to Das, the EV industry is transitioning to very high-power charging. "1-megawatt charging is here today. The goal is to make the experience very similar to fuelling up at the gas tank or the petrol station."

Also evolving is AI, which is no longer a tool for just carrying out relatively simple tasks. "At the other end of the spectrum you have agentic AI, which is AI that has become so advanced that you can give it a goal-oriented task."

➤ Manuel Gärtner, Director Wide Band Gap & Electrification at STMicrolectronics, championed the benefits of extensive vertical integration, from powders to packaged devices.

These jobs for AI, undertaken with some level of reasoning and inference, require sophisticated, highly capable processor units with megawatt levels of power.

For applications with these power requirements, even incremental increases in efficiency are highly valued. Das said that switching from silicon to SiC easily delivers a 1 percent gain in efficiency, an energy saving that could be big enough in 2030 to power 40 million homes in the US. Note that in the EV industry, SiC has enabled efficiency increases of around 3 percent – that's a game-changing improvement.

Another trend that Das is seeing is a move to higher voltages within the data centre. They have already increased from 400 V to 800V, and he is expecting a further rise to 1500 V by the end of this decade.

Much lower voltages are also used in the data centres, and Das expects SiC to only serve at the upper end. "The silicon MOSFET is still a very, very good technology on the GPU or consumption end."

Smart grids, operating more efficiently than today's infrastructure, are also expected to feature SiC.

In inverters in EVs, the application behind the recent hike in sales, SiC is still widely used. "The growth is still there," said Das, who added: "Expectations were previously very, very high."

Infineon's insights

Providing anther perspective on market dynamics, Peter Friedrichs, Fellow of SiC at Infineon Technologies, reminded delegates that there have already been three occasions when SiC has enjoyed growth resembling the shape of a hockey stick. He pointed out that sales took off in the early 2000s, thanks to deployment of SiC in power supplies; during the previous decade, a second rapidly growing market for these devices came from supporting renewable power generation; and more recently, the introduction of EVs has accounted for a third ramp in revenue.

"Right now, we see a new opportunity. It's all about power infrastructure," remarked Friedrichs, who explained that SiC could serve in circuit breakers and solid-state transformers.

He said that the EV revolution is not limited to cars. It extends to trucks, requiring charging powers of several megawatts. Due to this, charging stations must operate at up to 30 MW, a power that cannot be met with existing platforms involving classical substations. There must be a move to a high-voltage DC bus, alongside the replacement of traditional, copper-based transformers with solid-state variants. "Since this is all about fast switching at high voltages, it's a clear playground for silicon carbide semiconductors."

Friedrichs referred to AI power servers as the other "big fish" in the game. He claimed that this application has power needs similar to those for charging infrastructure – and here he expects line frequency transformers and AC power supplies will be replaced by a high-voltage DC bus, initially served with line frequency transformers, but in time, solid-state transformers.

These changes represent a shift towards a DC grid, where solid-state circuit breakers will have a role to play.

"The market outlook for the circuit breakers based on solid-state materials is really substantial," estimated Friedrichs. He explained that even a small share of the total market – estimated to be worth over $6 billion, and increasing at a compound annual growth rate of 3 percent through the remainder of this decade – will lead to significant revenue.

By 2023, sales of solid-state circuit breakers could net more than $800 million, according to Infineon's predictions.

One of the merits of the solid-state circuit breaker is its speed. "You can isolate a fault much faster than in a mechanical-driven system," said Friedrichs. What's more, there's far greater sophistication, with the opportunity for failure recovery and safe diagnostics, as well as the avoidance of wear-out mechanisms – mechanical circuit breakers suffer from arcing.

Friedrich championed the SiC JFET for circuit breakers, as this class of transistor can handle a higher power density than the SiC MOSFET. He pointed out that another asset of the JFET is its superior stability, especially at high voltages and currents, that ensures linear-mode operation.

Where high-voltage SiC MOSFETs have a big role to play, according to Friedrichs, is in transformers converting 10-35 kV, AC, into a DC supply of more than 800 V for the IT racks in data centres. Here, the high-voltage reduces system complexity. For a 34.5 kV AC supply from the grid, if 1.2 kV devices are used, there needs to be around 40 sub-systems per phase. This figure falls to about 20 and 15 sub-systems per phase when using 2.3 kV and 3.3 kV MOSFETs, respectively.

ST: Valuing vertical integration

Along with onsemi and Infineon, another big hitter in the SiC market that will target emerging megawatt applications is STMicroelectronics. To increase its competitiveness, it's expanding its capacity.

Details surrounding this growth in capacity were discussed by Manuel Gärtner, Director Wide Band Gap & Electrification.

To put this expansion in context, Gärtner outlined the company's key milestones, now dating back three decades, that began with a collaboration with Catania University in 1996. By 2004 and 2009 ST had demonstrated its first SiC Schottky diode and power MOSFET, respectively, with production following in 2007 and 2014, respectively. Also featuring in the company's history are Tesla's adoption of its products, its acquisition of the SiC substrate maker Nortsel in 2019, and the creation of the world's first fully integrated SiC facility in 2024.

➤ Networking plays an important role in CS International, which this year took place at the Sheraton Brussels Airport Hotel on 21-22 April.

Gärtner emphasised the increasing extent of vertical integration at ST. "We get the raw material. We get silicon powder, carbon powder, a lot of energy, and we produce ingots. We go on to do devices, and also packaging."

He argued that this approach has a number of benefits: it reduces reliance on suppliers, improves process control and efficiency, and lowers transport costs.

One issue facing many companies is trade restrictions. Helping to address this, ST has two big fabs – one in Europe, and another in China, in a joint venture with Sanan. "It's very important that we can serve the China market, which is booming for e-mobility, with the same technologies," remarked Gärtner.

The two facilities, in Chongqing and Catania, will start production this year, with full build-out slated for 2028 and 2033, respectively. "We need a little bit longer in Catania, because we add the packaging and modules," said Gärtner, who explained that these fabs will feature many robots.

This will help boost yield, streamline manufacture, and ultimately aid the deployment of SiC power electronics in EVs, as well as megawatt chargers and power infrastructure for tomorrow's datacentres.

Wolfspeed: The 10 kV SiC MOSFET

As well as serving in motor drives, electrical infrastructure and uninterruptable power supplies, the10 kV SiC MOSFET could win deployment in mining and fertilizer production

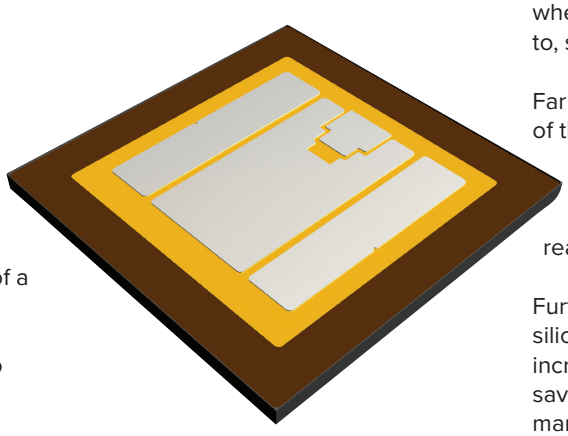
BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

Since mass-production of the SiC MOSFET commenced in 2010, portfolios have expanded, often through the introduction of products offering higher blocking voltages. This trend continues to this day, with Wolfspeed announcing yet another milestone this March: the world's first commercial 10 kV MOSFET, shipped in the form of a bare die.

This device, offering an alternative to the incumbent 6.5 kV silicon IGBT, is targeting a number of applications. Some are to be expected, such as electrical infrastructure and motor drives, while others could come as a surprise, such as opportunities in agriculture and the nuclear industry.

One of the primary applications for Wolfspeed's 10 kV MOSFET is in high-voltage motor drives, such as 4160 AC motor drives. In this particular case, the 10 kV MOSFET is an attractive alternative to SiC siblings operating at lower voltages, such as 3.3 kV; and to silicon IGBTs, which suffer from slower switching speeds, lower efficiencies and inferior thermal characteristics.

When engineers design motor drives with transistors operating at higher voltages, they can simplify circuits by turning to lower-level topologies that employ fewer devices, fewer gate drivers, and a simpler busbar. As well as potential to trim the total bill of materials, this elegant approach improves reliability.



➤ Wolspeed's 10 kV bare die MOSFET

The latter is a big deal, given that the motor drive could be deployed in an off-shore oil rig or up in a turbine.

"How expensive is it when something goes wrong in a place like that?" points out John Perry, VP & General Manager for Medium & High Voltage Products and Government Contracts at Wolfspeed. He argues that simply reducing the number of devices is a huge value proposition, thanks to increased reliability.

If silicon IGTs, widely available up to 6.5 kV, are replaced with 10 kV SiC MOSFETs, the benefits go beyond a lower-level topology. There's the opportunity for far faster switching speeds, which unleashes many merits.

"You can really radically shrink the magnetics, because your IGBT solution is limited to something like 600 Hz, whereas [10 kV SiC MOSFETs] could go to, say, 10 kHz," argues Perry.

Far faster switching enables a trimming of the size and weight of the drive, a much-valued gain on oil rig platforms, according to Perry: "That's some of the most expensive real estate in the world."

Further benefits coming from replacing silicon IGBTs with SiC MOSFETs include increased electrical efficiency, which saves energy and simplifies thermal management.

In some systems, Perry says that thermal management can account for half the volume of the motor drive unit, and switching to SiC MOSFETs promises to cut that in half. "That saves a lot of space and weight, really important to our customers."

Another advantage of the SiC MOSFET over the silicon IGBT is that it can tolerate more heat, enabling an additional trimming of the dimensions of the thermal management solution.

Wolfspeed also sees significant opportunities for its 10 kV MOSFETs in electrical infrastructure and uninterruptable power supplies.

Perry points out that transformers are bulky, heavy, lossy, and customers experience a really long lead time. "A solid-state version is going to be smaller, lighter, more efficient, and also enable a lot of system flexibility."

John Perry is the Vice President & General Manager for Medium & High Voltage Products and Government Contracts at Wolfspeed. He joined Wolfspeed (formerly Cree) in 2004, and has held several roles leading product management, marketing, and customer experience in LED, lighting and power devices.

There are also a number of applications that exploit the opportunity to deliver massive, incredibly short bursts of energy with 10 kV MOSFETs.

Interested parties are reaching out to Wolfspeed, looking to use these MOSFETs in mining, for blowing up rocks and drilling into the earth; and to generate plasmas, for nuclear fusion and for the production of fertiliser.

Device development

Aiding the development of Wolfspeed's 10 kV MOSFET are its variants operating at several kilovolts.

"We've been shipping high-voltage devices, so anything over 5,000 volts, for quite a while," says Perry, who reveals that this information has not been in the public domain.

Scaling up voltage demands thicker layers. For the 10 kV MOSFET, the drift layer is over 100 µm-thick, increasing the growth time for the epitaxial stack. "But in the grand scheme of things, it's not really a contributor to our overall cycle time," claims Perry.

Threatening to compromise the performance of every SiC MOSFET is bipolar degradation, an issue originating with electron-hole recombination at basal plane dislocations, and leading to a hike in leakage current. Helping to prevent this is the use of low-defectivity, uniform wafers.

In addition, at Wolfspeed there's targeted metrology in place. "We've established a closed-loop process that gives us full traceability, from the device all the way back to the materials," explains Perry.

To provide proven reliability, Wolfspeed's 10 kV MOSFETs have undergone much evaluation, including intrinsic time-dependent dielectric breakdown lifetime tests. This evaluation determined a lifetime of over 150,000 years, a substantial number that's not easy to comprehend.

"It just means our technology's reached the maturity where our gate oxide is as good as silicon. You don't need to worry about it," says Perry.

Another impressive figure is that for the cosmic-ray failure-in-time (FIT). Perry says that for the 6.5 kV IGBT, a typically quoted FIT rate is 100 failures per billion hours.

"Our fit rate per device is 0.57," says Perry. "You would multiply that by the number of die in a module – 24 is a reasonable number – but that still gets you to a fit rate of 14."

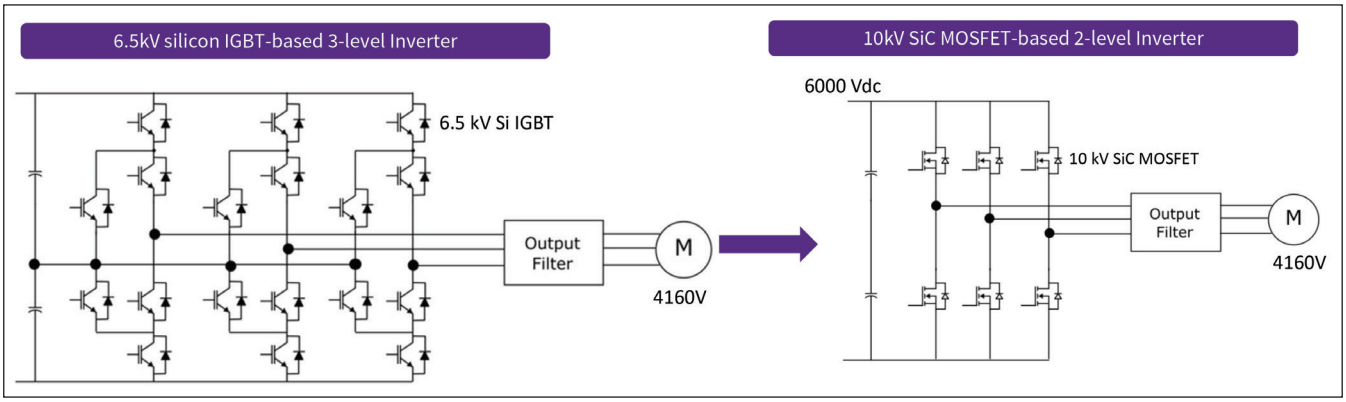
There are also a number of applications that exploit the opportunity to deliver massive, incredibly short bursts of energy with 10 kV MOSFETs. Interested parties are reaching out to Wolfspeed, looking to use these MOSFETs in mining, for blowing up rocks and drilling into the earth; and to generate plasmas, for nuclear fusion and for the production of fertiliser.

A welcome introduction

The strengths of Wolfspeed's 10 kV MOSFET have helped to spark a lot of interest in this device across different industries. "We're really excited about the response so far," says Perry.

He believes that even higher-voltage devices could be released further down the line, pointing to Wolfspeed's demonstration of a 27 kV SiC IGBT. The company has demonstrated a number of different devices, including thyristors and various diodes. This broad family includes bipolar devices, which are compelling candidates for operation at tens of kilovolts.

"We're just going to keep pushing the envelope there, to try to enable new applications," says Perry.



Moving from 6.5 kV silicon IGBTs to 10 kV MOSFETs allows designers to produce circuits with fewer devices.

Large-area laser heating

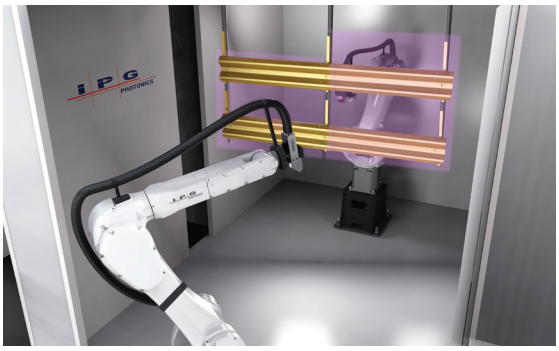
Laser heating is a sustainable, cost-effective solution that's impact will grow

BY TOBY STRITE FROM IPG PHOTONICS CORPORATION

DURING my career in high-power lasers diodes that spans nearly three decades, I have witnessed these sources progress from being a 'last resort' to 'solution of choice' for various thermal material processes, including marking, cutting, welding and cleaning. It's a revolution largely powered by leaps and bounds in GaAs-based diode laser performance (see Figure 1). Processes once infeasible became ordinary and then passé in just a few years. There are many examples of this, including laser marking and flat-sheet cutting of metals.

Over the last couple of years, it has become increasingly practical for diode lasers to heat large areas. This trend, supported by an urgency to switch from fossil fuels to sustainable alternatives, has established several industrial beachheads. It's now possible to deploy heaters based on multi-kilowatt lasers, which aggregate GaAs diodes and provide an electrical-to-optical conversion efficiency of up to 55 percent. This is an elegant solution, with fibre delivery allowing the laser cabinet to be remote – an architecture that enables convenient co-location of electrical and cooling facilities, often outside a cleanroom process environment.

With laser-based heating, advantages may be realised over traditional approaches, in terms of greater uniformity, directionality, and lower utility bills. Energy uniformity over areas of up to and above a square meter is in the few percent range, thanks to projection optics that image a homogenised diode laser output onto a target surface. Laser light is easy to direct, enabling most optical energy to impact the target; and lasers heat without raising the ambient temperature inside the enclosure. Thanks to the latter, 'cold' ovens save energy and infrastructure, by eliminating the heat spillage associated with conventional thermal ovens.

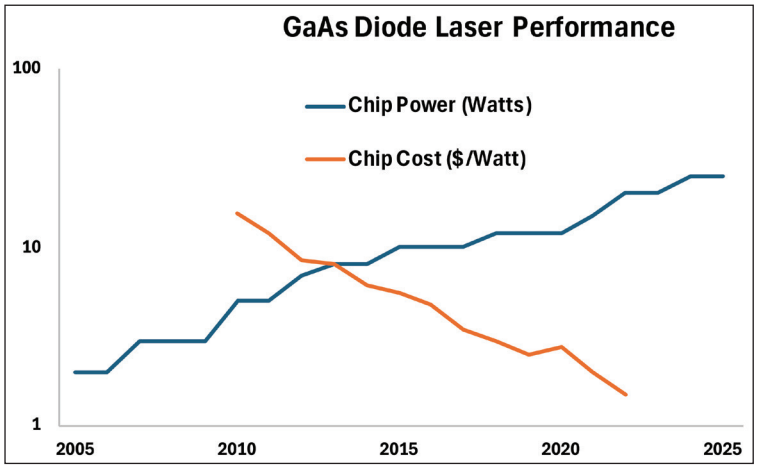


➤ Figure 2. Kilowatt lasers projected over meter-scale surfaces demonstrated their utility for curing/drying industrial coatings.

However, despite having outstanding characteristics, well-suited to certain applications, cost and efficiency limitations ensure that the laser will remain a niche heating technology.

For heating, the most attractive attribute of the laser is its speed, a strength that comes from its unmatched fluence (see Figure 3). Compared with convection ovens that deliver at most 1 W cm^{-2} to a surface, and broadband infrared sources that can be stretched to provide 2-3 W cm^{-2}, laser heaters fare far better, easily providing 10^{+} W cm^{-2}. This superior power density slashes the time taken to reach the process temperature from minutes to just a few seconds.

To ensure that the target process temperature isn't exceeded, fast heating must be combined with accurate, agile metrology. That's often realised by deploying lasers under closed-loop control, guided by an optical sensor. The low ambient temperature



➤ Figure 1. Exponential progress in GaAs diode laser performance at IPG Photonics.

in a 'cold' laser oven facilitates the installation of a pyrometer, providing direct surface-temperature measurements. This is a great improvement over inferred temperature measurements, common in thermal ovens. Merits of the optical control loop are speed and accuracy, and ultimately unprecedented agility to thermal processes. The upshot is a shorter total process time, through faster pre-heating that increases factory throughput while saving floor space.

Selectivity is another key attribute for laser-based heating. As lasers selectively heat at the surface, it is possible to cure or dry coatings without raising the temperature of the underlying material. For bulky metal parts, significant energy savings come from preferentially heating the coating, while additional time savings result from a shortened cool-down period. Another advantage comes from the shaping of a laser beam with projection optics to only cover the target area, an attribute that may not be replicated with less directable heat sources.

In the semiconductor industry, lasers are compelling candidates for heating silicon wafers. The speed, precision, reliability and efficiency offered by this source are highly valued in capital-intensive, throughput-focused wafer fabs. Laser heating can be deployed for a number of common semiconductor applications, including outgassing wafers, post-implant anneals, selective-area heating and full-wafer heating. If chipmakers heat chambers with IR bulbs, whose longer wavelengths couple weakly to the silicon, they use at least twice the optical power, while heating at slower rates, with much energy from the bulbs unproductively heating the ambient and chamber walls. These weaknesses are motivating chipmakers to eliminate IR bulbs, which degrade at variable rates and have challenging uniformity requirements, and a high service and consumables burden.

Note, though, that laser heating is not always a superior solution to traditional approaches. Attempts to fire porcelain-enamel coatings have revealed a limitation of the 'cold oven'. While porcelain-enamel powder is successfully fired by laser at 750°C in just two minutes, radiative losses – described by

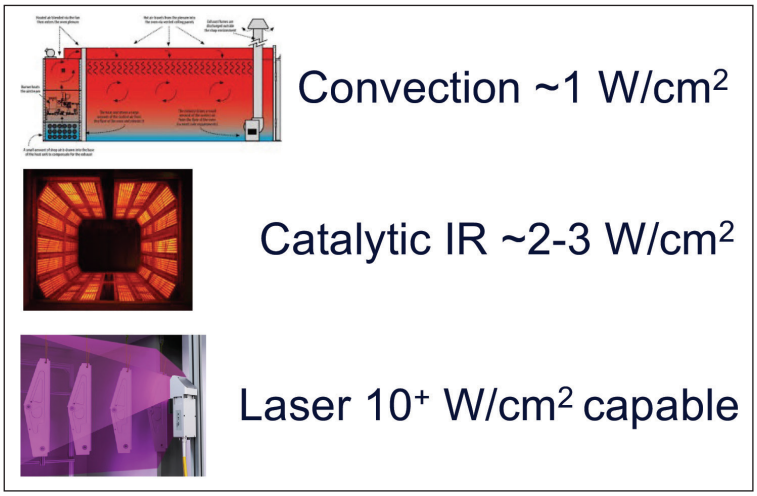


Figure 3. Lasers are capable of an order of magnitude higher heat flux than conventional alternatives, drastically shortening the time to reach process temperature.

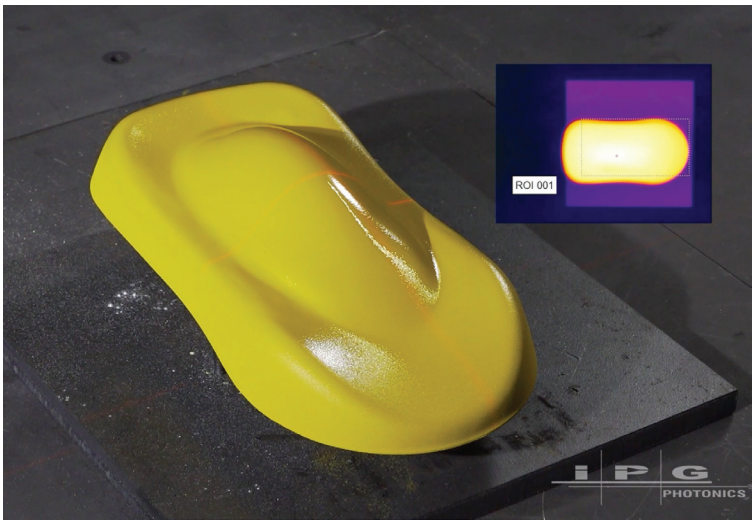
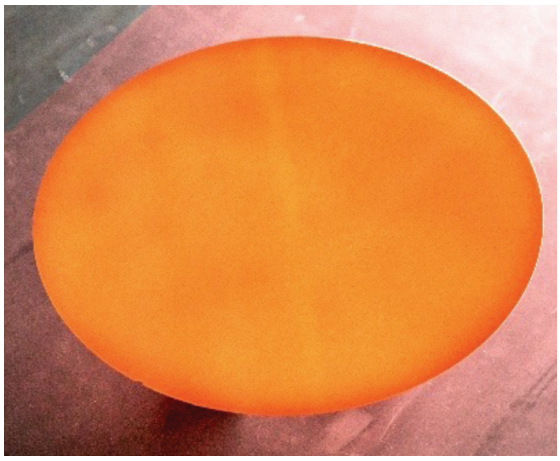


Figure 4. Lasers cure or dry paint ten times faster than conventional ovens because they selectively heat coatings with high energy fluence governed by agile closed-loop temperature control.



➤ Figure 5. 200 mm silicon wafer heated above 800 °C in less than 10 s using less than 20 kW.

Kirchoff's law and proportional to temperature-to-the-fourth-power – are so severe that cost and energy consumption is an order of magnitude higher than that associated with a conventional ten-minute 800°C convection furnace firing process. While a convection furnace entombs and recycles heat re-radiated by a target, a 'cold' laser oven cannot store photons for future use.

In terms of the key metric of $/Joule, there's no electric heating solution that competes with electric convection, which is governed by Ohm's Law. While GaAs diodes enjoy Moore's Law rates of improvement, one must keep in mind that 'trees do not grow to reach the sky'. For energy intensive thermal processes that are less cycle-time sensitive, such as the bulk drying of cement, it is hard to see lasers ever competing on purely $/Joule economics.

It's also worth noting that a laser can't heat a mirror, or a window. Instead, it works best heating surfaces where moderate (Beer-Lambertian) absorption prevails, allowing it to deposit energy uniformly throughout the heated material.

Estimates vary, but it is safe to say that drying and other thermal processes account for roughly 10 percent and 25 percent of total industrial energy consumption, respectively. In the US alone, drying processes were reported to consume over 1,178 TBtu of energy annually, representing roughly 10 percent of total manufacturing energy use. Back in 2015, the US Department of Energy estimated that next-generation drying technologies could reduce energy consumption in drying by up to 40 percent.

Since mankind lived in caves, our preferred heating solution has been to burn something. This behaviour must change, so design windows to replace legacy fossil fuels are open. The laser will be an important piece of the sustainable heating puzzle, alongside a bevy of other technologies.

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Strengthening the world's first CS cluster

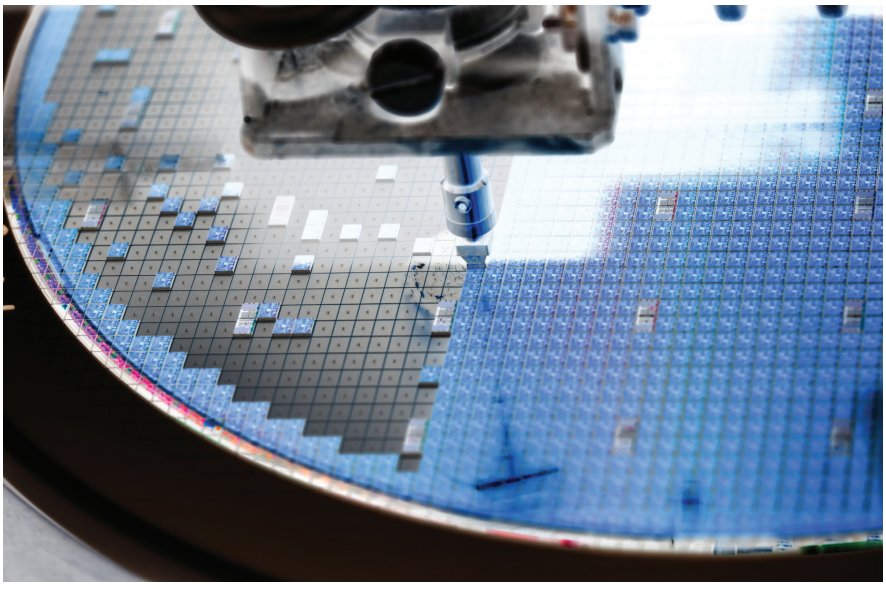
Underpinning recent success in the South Wales cluster is a five-year programme backed by £43 million. It's supported the scaling of epitaxy to 200 mm, a new power electronics capability, and the construction of a robust talent pipeline

BY WYN MEREDITH AND CAMILLE COLOMBIER FROM CSCONNECTED

CLUSTERS don't get built overnight. It has taken decades of devoted effort for the South Wales compound semiconductor ecosystem to reach a point where complementary companies, universities and government partners operate within a few miles of each other – IQE, KLA, Vishay Newport, Microchip, MicroLink Devices UK Ltd, and Cardiff and Swansea Universities. But proximity alone doesn't make a cluster. Also crucial is the connective tissue: shared infrastructure, coordinated R&D, and the depth of trust that only comes from working together over time.

These factors have been energised by the Strength in Places Fund (SIPF). Providing £43 million of investment over six years, it has produced results that are measurable at every level, from 200 mm GaAs VCSEL epitaxy to the inception and introduction of a SiC power module pilot line.

The South Wales cluster has a number of significant industrial players, all with a rich heritage. They include: IQE, the global leader in compound semiconductor epitaxial wafers; KLA, a world-leading manufacturer of metrology, inspection and wafer processing equipment that opened a purpose-built facility in Newport last year; Vishay Newport, the UK's largest semiconductor fab; and Microchip, which has a site in Caldicot that's operated in the semiconductor sector for decades. In addition, there's a strong research infrastructure, as the cluster is home to Cardiff University's Institute for Compound Semiconductors and Swansea University's Centre for Integrative Semiconductor Materials (CISM). The SIPF programme has strengthened the cluster by providing the framework to ensure that collaboration becomes a natural instinct across the ecosystem.



Compound semiconductor wafer during device fabrication.

Note that this programme, running from 2020 to 2026 and backed by UK Research and Innovation, has not been focused on creating a cluster. It was already there. The goal has been activation: taking the geographic concentration of compound semiconductor expertise in South Wales and turning it into a functioning, coordinated ecosystem with shared infrastructure, joint R&D programmes, and the trust and collaborative practice that's only realised with sustained co-investment.

The right foundation

If compound semiconductor manufacturing ecosystems are to excel, they must include physical infrastructure that individual companies are unable to justify building and maintaining alone. To bridge that critical gap, UKRI has invested directly in open-access capability across the region, specifically designed to service an extended supply chain from

materials development to module-scale manufacturing. At the heart of this strategy, Imperial Park in Newport now houses IQE, KLA and the Compound Semiconductor Applications Catapult in a purpose-developed advanced manufacturing environment. This co-location of epitaxial wafer production, process equipment development and applications prototyping fosters close interaction between equipment developers, material producers and device engineers – something that is harder to realise in more distributed industrial settings.

Less than 10 miles from Imperial Park is Cardiff University's Institute for Compound Semiconductors. Located within the university's Innovation Campus, it has cleanroom facilities and characterisation capability that supports academic research and industry-facing technology development. Complementary expertise comes from Swansea University's CISM, which focuses on wide-bandgap materials, including SiC and GaN, critical for power electronics applications.

Providing a translational bridge between the companies and the universities within the South Wales cluster is the Compound Semiconductor Applications Catapult. This entity ensures that research outputs become manufacturable processes and commercially viable technologies – this is often the most challenging transition in any advanced materials programme.

Complementing this infrastructure is Centre 7, a 51,000 ft^2 facility at Cardiff Gate, acquired by the Welsh Government as part of its international strategy to attract inward investment into the cluster. Designed as a flexible landing space for semiconductor companies, it provides a combination of lab-enabled environments, office space and collaboration facilities that lower the barrier to entry for organisations looking to establish a presence in South Wales. With early tenants including CSconnected and MicroLink Devices, and further companies expected to follow, Centre 7 plays a distinct role within the ecosystem: as a point of entry and expansion for SMEs and international partners, helping to translate the cluster's global reputation into tangible business activity on the ground.

➤ Semiconductor cleanroom with integrated process tools for wafer fabrication.

Four R&D programmes

At the technical heart of the SIPF initiative is four major collaborative R&D programmes, each targeting a distinct but interrelated challenge. These programmes focus on: next-generation optical communications and sensing; large-scale GaAs-based wafer manufacturing; the development of novel, more-efficient compound semiconductor wafer fabrication tools; and the introduction of advanced processes, for 5G and electric and autonomous vehicle systems. Together, these four workstreams are addressing the 'full vertical', from materials production through to process tooling and device-level applications – and are mapping directly onto the markets that will define compound semiconductor demand through the next decade.

Scaling epitaxy

Perhaps one of the most technically significant deliverables of the SIPF programme is IQE's successful scale-up of InP epitaxy from a starting point of 3-inch and 4-inch wafers to full 6-inch (150 mm) production. Success has required complete process redevelopment, equipment adaptation, and extensive qualification. IQE was the first in the industry to demonstrate this important capability that is now delivering material quality and uniformity equal to, or better than, established 100 mm lines, enabling IQE to supply the next generation of optical devices produced on large-diameter 6-inch wafers to meet future hyperscale datacentre demand.

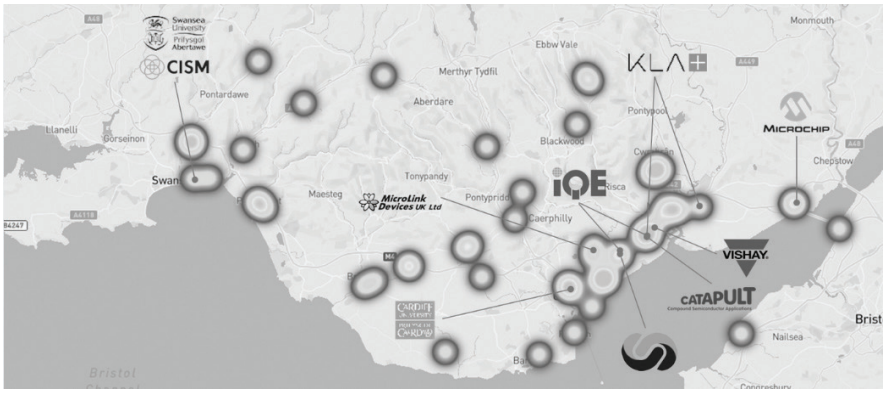
In addition, the programme enabled the demonstration of the world's first commercially available 8-inch (200 mm) VCSEL epiwafer, announced by IQE in 2022. The SIPF programme has enabled IQE to invest strategically in advancing its 8-inch platform, supporting the continued expansion of compound semiconductor applications.

Independent validation of device performance has come through collaboration with Cardiff University, with IQE retaining proprietary manufacturing know-how. When markets in AI/data centres, 3D sensing, lidar, and silicon photonics move to larger wafers – a migration that will certainly happen, with timing dictated by economics of scale – the South Wales cluster will be positioned to respond at commercial speed.

Tools and processes

KLA's participation in the SIPF programme highlights the cluster's strength and appeal across the semiconductor value chain. Supported by SIPF, KLA has made substantial advances in GaAs VCSEL etching, InP processing and, GaN etch solutions, including hardware improvements.

Critical to success has been access to large volumes of epitaxial material, beyond what customers typically supply for process development. Being part of the cluster has enabled access to more material, and engineers have gained deep insight into layer behaviour across a wide parameter space. Drawing on



➤ Heatmap showing the concentration of compound semiconductor activity across South Wales.

this, processes have been refined, and now provide improved uniformities, tighter profile control, and superior management of complex aluminium-containing layers that are notoriously difficult to etch predictably. During the programme, developments reached technology readiness levels appropriate for commercial deployment.

➤ Student engaging with virtual reality technology during a CSconnected outreach activity.

Building the pipeline

While physical infrastructure and R&D capability are necessary for a sustainable cluster, they alone do not guarantee success. That's because the compound semiconductor sector is skills-intensive, needing talent pipelines that take years to build. To strengthen these pipelines, CSconnected and SIPF have invested across every level, from primary school engagement to postgraduate research training that's directly connected to industry needs. In 2025 alone, SIPF-backed activity reached between 12,000 and 13,000 individuals across South Wales, predominantly through school-based programmes, with structured engagement running from primary school all the way through to college, university and adult professionals.

The SIPF, along with the Cardiff Capital Region, has jointly funded the flagship 'Sparking STEM Futures' initiative, managed by CSconnected. Starting in January 2024, this has reached more than 23,000 people across South and West Wales. Delivered through a coordinated network of regional education providers, this programme has introduced young people to compound semiconductors through hands-on, curriculum-linked activity at primary and secondary level. This April, a new interactive semiconductor exhibit opened at Techniquest, Cardiff's primary science engagement centre, providing a permanent public-facing asset that continues to deliver value beyond the programme's lifetime.

The CSconnected SIPF project has also supported the development of new semiconductor-specific qualifications at secondary school and technical college level, including teacher-training programmes to support delivery. The cluster's workforce data reflects this sustained investment: 19 percent of non-university cluster employees are engaged in R&D, average salaries sit at approximately £66,000 and the proportion of employees qualified to degree level ranges from 43 to 85 percent across private sector cluster firms.

What the data shows

Five years of support from SIPF has delivered measurable results. The total number of jobs across Wales supported by the activity of the cluster has climbed from 2,085 in 2020 to 3,140 in 2025, representing growth of just over 50 percent. That's an increase of more than 1,000 over a timeframe when Welsh manufacturing employment as a whole has fallen from 142,000 to 133,000.

The cluster has also made a substantial, growing contribution to the UK economy. Between 2020 and 2025, its direct contribution has grown from £172 million to £267 million, and reached £436 million when including supply chain and wage-spending effects. Last year exports totalled £480 million, accounting for more than 90 percent of industrial output.

Looking forward

While the CSconnected SIPF project ends this year, the cluster it has helped to build will continue to go from strength to strength. Ambitious targets have been set for the next phase: £1 billion in cluster revenue; and a community of 6,000 people within five years, with a continued focus on developing local talent. Technically, the priorities are already clear. The markets compound semiconductors will serve over the next decade – 6G infrastructure, automotive power electronics, renewable energy systems, and AI photonics and optical interconnects – are placing new demands on materials, processes and device architectures. Aligning directly with these demands are the technical outputs of the cluster, realised during the support of the SIPF programme.

In 2027, South Wales will host the International Conference on Silicon Carbide and Related Materials (ICSCRM). Co-organising this is CSconnected and Swansea University, with Vishay Newport providing the principal sponsor. ICSCRM will bring the global SiC research community to the cluster for the first time. It is a marker of how far the region has come, and an indication of its ambitions for tomorrow.

FURTHER READING

➤ M. Munday *et al.* "Annual Report: Compound Semiconductor Cluster in South Wales 2025." Cardiff University Welsh Economy Research Unit (2026)

The pros and cons of PCSELs and VCSELs

While the VCSELs is a proven technology that's serving in two killer applications, it has weaknesses that are addressed by the PCSEL, a promising technology on the cusp of commercialisation

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

EDGE-EMITTING lasers are an unquestionable success. Over a number of years, they have been deployed in a wide variety of applications, including optical networks and cutting and welding, and will have generated sales worth billions and billions of dollars. But they have significant weaknesses: modulation rates are not that high; testing and packaging is far from easy; they are expensive to produce; volumes are mediocre; and the emission profile is not the desired circular beam.

Addressing all these issues are surface-emitting lasers. The most well-known and mature of these is the VCSEL, which has been manufactured in volume for many years, and has found deployment in two 'killer' applications: short-reach optical links, and a light source for facial recognition in smartphones.

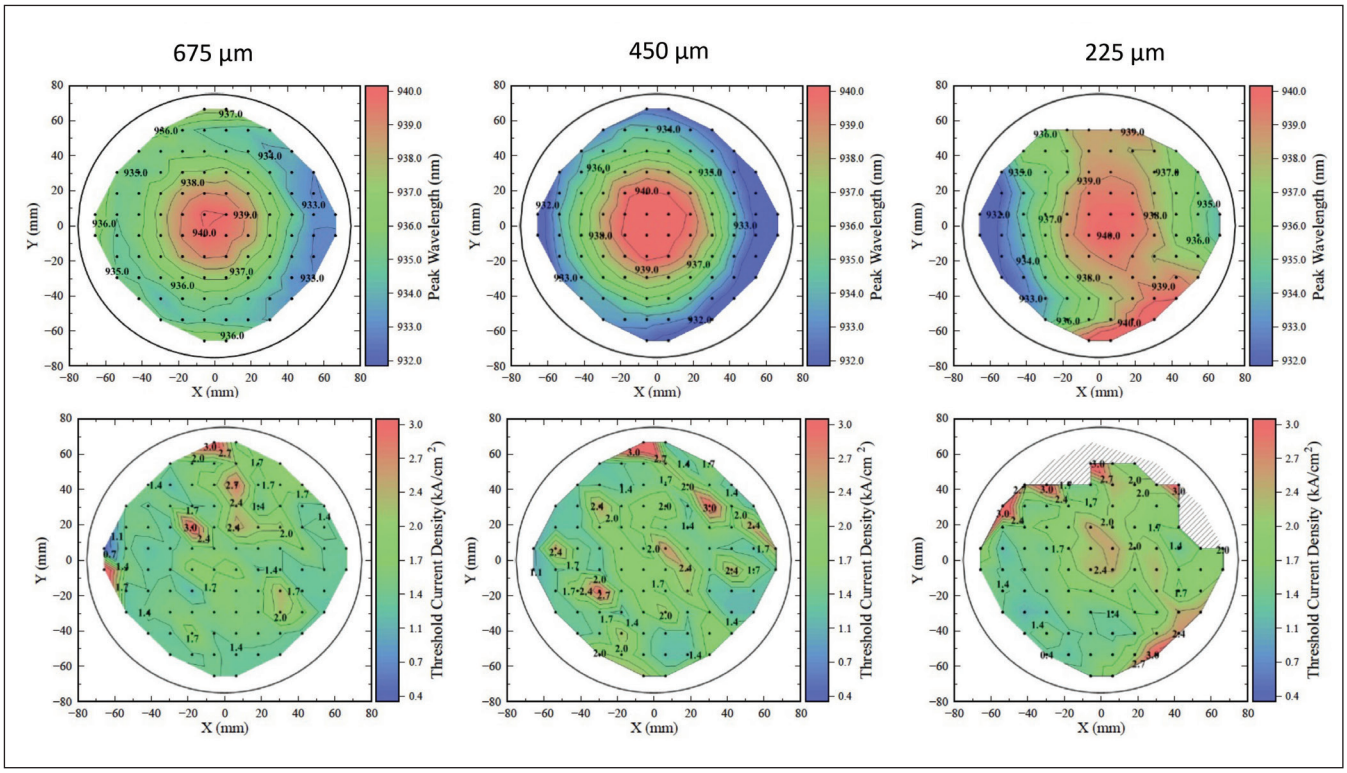
➤ Peter Smowton, an academic at Cardiff University and the Managing Director of the Institute of Compound Semiconductors, oversees efforts to improve the production of VCSELs by shifting their foundation from GaAs to germanium.

A key limitation of the VCSEL is its spectral range. High-volume products emit in the infra-red, typically at 850 nm or 980 nm, with optical gain supported by a pair of mirrors, each made from alternating layers of GaAs and AlGaAs. Expanding the spectral range involves the production of mirrors emitting in the visible or further into the infra-red, but it's challenging to find material pairings that combine conductivity with a sufficient refractive-index contrast and lattice constants close enough to ensure high-quality epilayers.

The PCSEL – short for photonic-crystal, surface-emitting laser – avoids this issue, with optical gain realised by in-plane feedback. Thanks to this design, the PCSEL provides emission over a far wider spectral range.

What's not clear is when the PCSEL will start to fulfil its promise and generate significant sales. Many applications could be served, but where is this class of laser going to make a commercial impact? Meanwhile, progress in VCSELs continues, pushing performance, with new processes that minimise strain and help to expand the spectral range.

Insights into all these matters and more were provided by speakers at this year's CS International, held on 21-22 April at Sheraton Brussels Airport Hotel. At this upbeat gathering of leaders in industry and academia, presentations detailed: the merits of switching from GaAs to germanium substrates for the production of GaAs-based VCSELs; how etching offers an attractive to solution to producing mirrors for InP VCSELs; demonstrations of the PCSEL for light-based, high-speed communication; and where the opportunities may lie for PCSELs to excel.



➤ Figure 1. Wavelength at a 5 mA drive current (top row) and threshold current density (bottom row) for GaAs VCSELs grown on 150 mm germanium substrates with different thicknesses. All VCSELs have a mesa diameter of about 49 µm and an oxide aperture of about 14 µm. For more details see S J Gillgrass *et al.* J. Phys. Photonics **7** 035033 (2025).

Switching foundations

While GaAs provides an effective foundation for the production of the GaAs-based VCSEL, it's not perfect. There is a small but significant lattice mismatch between GaAs and AlGaAs, and when the resulting strain is magnified by growing high-reflectivity distributed Bragg reflectors (DBRs) with many tens of layers, epiwafers are no longer flat. Offering an attractive alternative is the germanium substrate, which has a lattice constant sitting between that of GaAs and AlAs.

This approach has been pioneered by IQE and its collaborators. Work continues, with an update provided at CS International by the Managing Director of the Institute of Compound Semiconductors, Peter Smowton.

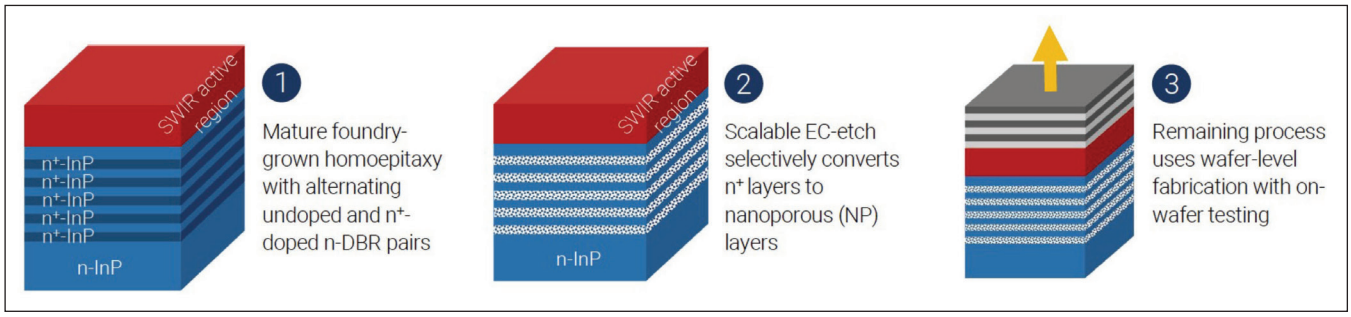
He told delegates that today's standard manufacturing platform for the VCSEL, which is in great demand for 3D sensing and communications, is the 150 mm GaAs substrate.

"We expect it to move to 200 mm, and in fact VCSEL material has been available on 200 mm substrates since 2022," said Smowton, who added that IQE is behind this breakthrough.

He pointed out that concerns associated with the GaAs substrate are not limited to epiwafer bow. "Gallium arsenide is not recycled to any large extent, and it's difficult to recycle, so that's an environmental issue. And 90 percent of gallium comes from a single country [China], with the other 10 percent coming from Russia, so that is somewhat problematic."

In comparison, while 60 percent of germanium comes from China, there are many sources, and it's possible to recycle the material. In addition, as well reducing wafer bow, germanium substrates are more robust, opening up the possibility to use

➤ Yale academic and Chief Scientist at InPhred, Jung Han, has developed an electrochemical etching technology that enables the production of lattice-matched InP DBRs.



➤ Figure 2. InPhred is pioneering the use of electro-chemical etching to produce InP-based VCSELs.

thinner substrates and reduce wafer breakage; and substrates are available in sizes up to 300 mm, offering a pathway to greater economies of scale.

However, despite all these merits, VCSEL manufacturers are reluctant to switch to germanium, which is more expensive – for the 200 mm format, prices are twice as high as those for GaAs.

Device manufacturers will not certainly not make the switch if it leads to a significant reduction in the performance of the VCSEL. And to see whether that is the case, Smowton and his colleagues have been evaluating the performance of a what is referred to as a fairly generic 940-nm-emitting structure, featuring a single oxidation layer for current confinement. VCSELs have been produced on GaAs and germanium substrates with 150 mm and 200 mm diameters.

When this VCSEL structure is grown on 150 mm GaAs, there's between 130 μm and 150 μm of wafer bow, while for the 200 mm format bow is above 200 μm. For germanium, there's warping, but the distortion is much diminished.

What's described as 'fast-fab' structures have been produced at the Institute of Compound Semiconductors, with 150,000 devices on 150 mm wafers, and 280,000 on the 200 mm format.

Comparisons of VCSELs on 150 mm substrates show that germanium provides a superior thermal impedance. When considering other metrics, these two types of emitter produce characteristics that Smowton refers to as "pretty much identical".

> "When everything is done right, you can create very, very tiny air bubbles or voids in otherwise single-crystalline perfect semiconductor," added Han. "Once you introduce these tiny nanoscale bubbles, the index of the semiconductor drops very, very quickly"

Given the relatively high price of germanium substrates compared with GaAs, Smowton and colleagues have investigated VCSEL performance on thinner foundations that could trim costs – they are two-thirds and one-third as thick. For this work, VCSELs were optimised for the thinnest substrate.

Maps of emission wavelength and threshold current density are similar for VCSELs produced on substrates with thicknesses of 675 μm and 450 μm (see Figure 1). There's a greater spread for lasers on 225 μm-thick substrates, with a region with leaky devices, due to warp that hampers processing in a conduction furnace. "If it was in a convection furnace, that wouldn't be an issue," remarked Smowton.

For investigations with 200 mm material, the team employed a VCSEL production process that's optimised for the GaAs substrate. Growth of germanium produced VCSELs with a slightly wider distribution in emission wavelength and threshold current density. When considering a threshold current of no more than 5 mA, yield on GaAs is 97 percent, while that on germanium 93 percent.

Commenting on this result, Smowton said that there's still work to do, including the need to optimise epitaxial growth for 200 mm germanium.

InP VCSELs

VCSELs emitting at wavelengths beyond 1.1 μm are attractive candidates for next-generation sensing, digital health, and data centre optical interconnects. But to reach this spectral domain, device designers have to move away from the conventional material system, based on GaAs.

For many years, effort has been directed at this issue. Progress has included VCSELs by Corning and Vertilas, featuring epitaxial DBRs that are lattice-matched to InP; VCSELs with strained active regions, such as the dilute nitrides used by Hitachi, and the InAs quantum dots pioneered by the Technical University of Berlin; and variants with an air-gap DBR on an InP substrate, a design pursued by Agilent. More recently, Vertilas has turned to double dielectric mirrors, and a number of other teams have pursued wafer fusion with AlGaAs DBRs.

Pioneering yet another approach, based on lattice-matched InP, is Yale University spin-off InPhred.

Speaking on its behalf at this year's CS International, company Chief Scientist Jung Han, who is also an academic at Yale, explained that the core technology can be traced back to work undertaken about 15 years ago, involving electrochemical etching.

According to Han, when *n*-type GaN is placed in a solution and a negative bias applied to the electrolyte, electrons are injected from the valence band to the conduction band. This creates holes on the surface, which weaken the semiconductor, leading to oxidation and etching.

"When everything is done right, you can create very, very tiny air bubbles or voids in otherwise single-crystalline perfect semiconductor," added Han. "Once you introduce these tiny nanoscale bubbles, the index of the semiconductor drops very, very quickly."

As the etching depends on the conductivity of the material, if the electrochemical process is applied to an InP stack with alternating layers that are heavily doped and undoped, the resulting structure will feature alternating low-refractive index, nano-porous layers, and high-refractive-index, pristine layers (see Figure 2).

"If the thickness is right, it will give you a DBR stopband with pretty much 99.9 percent reflectivity, and you can tune the stopband," enthused Han.

In addition to lattice-matching, mirrors benefit from relatively few alternating layers. Thanks to a refractive index contrast of up to 1.0, a reflectivity of around 99.5 percent is realised with 10 or so mirror pairs.

Han explained that the VCSEL fabrication process begins with homoepitaxial growth of the structure, which includes a tunnel junction. Engineers then form a mesa, define an aperture with ion implantation, and form an optical aperture. A side wall is then exposed, allowing electrochemical etching, prior to passivation, metallisation, and the addition of a *p*-type DBR (all these steps are illustrated in Figure 3).

Using this approach, engineers at InPhred have produced VCSELs with emission wavelengths from 1300 nm to 1700 nm using nearly identical processes. Peak power conversion exceeds 29 percent; the threshold current density for emitters with a 10 µm-diameter aperture is 1.0-1.4 kA cm^{-2}; and VCSELs have passed the Telecordia 468 reliability test, involving operation for 2,000 hrs at 85°C.

Han also presented preliminary results for linear VCSEL arrays with a handful of apertures. Encouragingly, output power is proportional to the number of apertures.

According to the Chief Scientist, the leading application for the company's InP VCSELs is 3D sensing, time-of-flight measurements. For sources beyond 1400 nm, emission is in the eye-safe regime, and the detection background quieter.

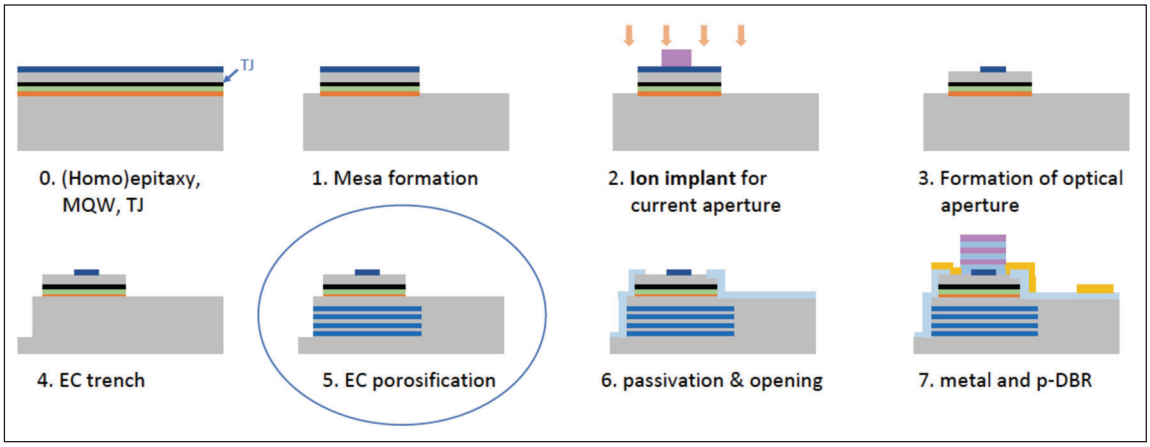
The other application that the start-up is targeting is optical interconnects, where it will compete with the likes of silicon photonics.

According to Han, InP VCSELs are strong contenders in this sector, by combining telecom-wavelength compatibility with the wafer-scale manufacturability and packaging simplicity of VCSELs. When serving in AI hardware, they promise to provide energy-efficient single-mode optical links, outperforming GaAs VCSELs and silicon photonics.

PCSELs for Li-fi...

Another speaker at this year's CS International, Vector Photonics CEO Richard Taylor, championed the merits of the PCSEL, arguing that they deliver the performance of an edge-emitter in a surface-emitting form factor. This is said to deliver several key advantages, including: wavelength flexibility; high beam quality; design of line width; and the opportunity to make large-scale, coherent arrays.

Taylor explained that Vector has a distinctive approach to producing PCSELs. "The traditional way is a void-containing structure, where you etch a grating, you do epitaxial regrowth, and you encapsulate air structures within the photonic



➤ Figure 3. The InPhred process for producing VCSELs.

crystal," remarked the Vector CEO. "What we do is very similar, except we infill the holes and have an all-semiconductor platform."

According to Taylor, removing air-filled structures from the device increases reproducibility, manufacturability, and reliability. These gains are realised, because when voids are present, they increase variability in device characteristics.

Vector has produced PCSELs with various material systems, but at CS International, Taylor only discussed breakthroughs associated with emitters made from InP. "We've got devices packaged in TO cans, we can do WDM [wavelength-division multiplexing], and we've got relatively good optical output powers compared to DFBs," said Taylor, adding that devices have been demonstrated in real-world systems.

➤ Vector Photonics, led by its CEO and co-founder Richard Taylor, has demonstrated that PCSELs can provide free-space transmission over hundreds of metres. Using a system designed and built by Fraunhofer UK, data transfer has been realised at 50 Mbit s^{-1} at a distance of 500 m. This is a real-world result, with transmission over the river Clyde, from the Glasgow Science Centre to the Clydeside Distillery.

Recently, effort has been directed at investigating the reliability of the lasers. "We previously demonstrated 2,500 hours, and more recently increased the acceleration factor to over 100 at 1,500 hours." The reason for cranking up this factor is to understand the failure mechanisms for these PCSELs. Taylor added: "If anyone knows about forcing failure modes in lasers that can help us out, please let us know, because it turns out they are very resilient."

As well as a high level of reliability, Vector's PCSELs provide excellent control of the emitted wavelength, thanks to the opportunity to tune the grating. Sub-nanometre precision is possible, alongside exceptional reproducibility, highlighted by results from a 3-inch InP wafer that provided several thousand PCSELs. "We randomly selected 60 of them across different device sizes," remarked Taylor, who added that they found a variation in emission wavelengths of just ± 0.1 nm.

One promising application for the PCSEL is laser-based free-space optical communication in challenging environments, such as war zones and disaster areas. To demonstrate the capabilities of this technology, Vector is partnering with Fraunhofer UK, to build free-space optical communication systems.

According to Taylor, PCSELs are ideal for this task, with a large emitting area enabling a high output power, and a low-divergence aiding detection of the signal.

The first system, held back by drive electronics, transmitted data over 200 m at 50 Mbit s^{-1}. Since then, speeds have increased to 700 Mbit s^{-1}, and very soon the partnership is expecting to exceed a gigabit-per-second, over 1 km.

Another application where the PCSEL has much potential is secure communication. Recently, Vector demonstrated how PCSELs can transmit orbital angular momentum, a first step in a quantum key distribution system.

According to Taylor, the traditional approach to producing a source of orbital angular momentum is to direct the emission from a laser through an external Q-plate – but this requires a large, bulky system.

Working with the UK's Compound Semiconductor Applications Catapult, Vector reduced the size of a source of orbital angular momentum, initially with a fibre-based system, and more recently, by 3D printing a waveplate. Initially printed on glass, waveplates are now directly printed on the device.

... and other applications?

Another pioneer of the PCSEL is Huawei's Bragg Research Centre, which is based in Ipswich, UK.

Speaking on behalf of this facility, CTO Graham Berry explained that it develops and manufacturers edge emitters and surface emitters. "We're relatively agnostic, and what we tend to do is choose the technology based on the performance and the packaging optics."

Berry focused on the choice of source for interconnects for AI-orientated data centres, saying that the two leading approaches are to either have high data rates at a single wavelength, or employ multiplexing and a range of wavelengths. "At the end of the day, the overall power consumption will be the prevailing winner," argued Berry.

He pointed out that PCSELs offer a low-cost packaging route, with options for data transfer

including multi-fibre push-on connectors, and fibre arrays. For these technologies, the 850 nm VCSEL is not ideal, as it is not suited to single-mode fibre – to do so demands a very small aperture – and emission is beyond the cut-off window.

For the PCSEL, the diameter of the emitter can be as small as a few microns, and potentially up to 10 mm. For all these sizes, it's single mode. "So, you have a platform for high power, mid power, and potentially some form of slow and fast," remarked Berry, who pointed out that another merit of the PCSEL is that it tends to avoid catastrophic optimal damage, thanks to power scaling with the area of the emitter.

In addition, PCSELs provide a very high beam quality and narrow beam divergence. "If you want to go lens-free and develop really small form factor micro-optics, being able to take the lenses out of that system is quite a nice win," argued Berry.

One downside of the PCSEL is its threshold current density, which tends to be higher than an edge emitter, due to scaling with area. "When you're after the last ounce of wall-plug efficiency, this threshold can come back to hurt you a little," warned Berry, who pointed out that it's not possible to produce PCSELs with apertures as small as VCSELs, because optical leakage kicks in at diameters below 20 µm.

With PCSELs, due to the limited number of devices produced so far, it's difficult to gauge reliability. "But there are no red flags at the moment," said Berry.

Discussing the potential for PCSELs to displace VCSELs in more detail, Berry considered VCSELs with apertures below 3.5 µm that provide single-mode operation, and could target 1 pJ bit^{-1}. He pointed out that while realising a bandwidth of 40 GHz with this design of VCSEL is challenging, it has been realised in the lab. However, small apertures may hamper reliability.

Link length is also a concern. For 850 nm VCSELs, connections are typically limited to 60 m, but there is the potential to extend to 100 m. Moving to 1060 nm VCSELs lengthens the link, with distances of 500 m and 2 km possible using multi-core and single-mode fibre, respectively.

Comparing these strengths and weaknesses with PCSELs, Berry remarked: "Our sweet spot on the PCSEL is between 200 and 400 microns, and it's as a high-power light source." Another merit of the PCSEL is that it's suitable for wavelength-division multiplexing. "The challenges are the slope efficiency."

PCSELs could also serve as the external light source for silicon photonics, with devices in small pluggable form factors providing between 200 mW and 400 mW.

"400 milliwatts would support something like 8 channels in silicon photonics," said Berry, who added: "If you could go to 800 milliwatts, you potentially could do all 16 channels."

For this application, Berry believes that laser efficiency needs to be at least 25 percent, a performance realised at an operating temperature of at least 50°C. The team at Huawei is not far from those requirements, with PCSELs producing potentially 300 mW over that temperature range, and recent work by Sumitomo showing that this class of laser is capable of output powers of 800 mW.

So PCSELs undoubtedly have much promise, and opportunities in many markets. But whether they'll ever enjoy sales as large as those of the VCSEL remains to be seen.

In 2027, CS International will be held on 13-14 April at the Sheraton Brussels Airport Hotel.

AI fuels phenomenal gains in valuation

Companies involved in the supply chain for optical components in AI-centric data centre are seeing staggering gains in their share price

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

SINCE its inception in 2006, there have been some astonishing figures in the yearly *Compound Semiconductor Share Price Leaderboard*, which tracks changes in valuation over a 12-month timeframe, running up to late April. Over the years, some standout numbers that will have delighted investors include Anadigics' appreciation of over 600 percent in 2006 and Veeco's increase by over 560 percent in 2010. And at the other end of the spectrum, results that will have disappointed include: the leaderboard from 2012, when the valuation of every company fell; and AXT's and Wolfspeed's plumetting valuations by just over 83 percent and 87 percent in the 12 months up to the end of April 2009 and 2025, respectively.

Against this backdrop, some of the latest results are completely off of the scale. This year, valuations of the top six have climbed by more than 400 percent – and the company out in front by an astonishing margin, AXT, has seen its share price increase by a whopping 5111 percent.

Driving these phenomenal surges in valuation, realised against headwinds of White House tariffs and a dubious war between the US and Iran, is the opportunity created by the roll-out of new generations of data-centres that will support the growth in AI.

A tremendous growth in AI is anticipated – although some fear it is a bubble that will burst – and companies playing a role in the supply chain for lasers for optical interconnects are enjoying a surge in sales. As data links shift to fibre from copper, which will only be used in the very shortest links, there are great opportunities for a ramp in revenue for makers of InP lasers and the supporting cast – that's makers of epitaxial growth systems, and InP substrates and epiwafers.

AXT's astonishing appreciation

One might easily assume that AXT's eye-watering increase in valuation to an all-time high of around $75 has been fuelled by significant hikes in sales and profitability. But that's not the case. It's all about promise, and the opportunity that will be created by ramping the production of InP substates.

AXT's current position can be seen in its most recent quarterly results, for the final fiscal quarter of 2025. For that three-month period, ending on 31 December, the company reported

a net loss of $3.5 million on sales of $23 million, with revenue held back by export restrictions on InP substrates.

While these figures are far from impressive, the great potential for the substrate supplier was clearly evident its fourth quarter earnings call on 19 February, 2026.

During that call, AXT's CFO, Gary Fischer, provided some insight into the importance of InP substrates within the company's portfolio, and the dominance of local customers. InP sales netted $8 million, compared with $7 million for GaAs and just $231,000 for germanium; and 81.5 percent of sales came from companies in the Asia Pacific, with Europe accounting for 17.5 percent and North America just 1 percent.

The breakdown by geographical region will change, as AXT has received permits in the first fiscal quarter of this year. According to CEO Morris Young, who also spoke in the February earnings call, the permits, along with data centre-build out for AI, will help to increase revenue in the first quarter of this year.

"We're also very pleased to note that we are seeing a welcome expansion of our customer base for indium phosphide," added Young, who revealed that this includes domestic and overseas makers of optical transceiver modules. For these chipmakers, which are aiming to produce optical devices operating at ever higher speeds and featuring superior sophistication, AXT is keen to showcase the merits of its InP wafers with a low etch-pitch density.

There is great demand for AXT's InP substrates. The backlog is rising, to stand at more than $60 million as of 19 February. Commenting on this, Young remarked: "Customers are planning for longer lead time by placing longer-term orders and giving us more visibility into their expected demand."

The AXT CEO also offered some perspective on the AI market: "The massive AI infrastructure build-out and planned CapEx spending by cloud services and AI platform providers in the United States is the primary driver for EML [electro-optic modulator lasers] and silicon photonics-based optical transceivers." He said that in China, while the data-centre build-out is early in its ramp, there will be rapid growth, as the world's second biggest economy moves to accelerate its data centre expansion and AI capabilities.

To support growth in global production of InP lasers, AXT is expanding its capacity for InP laser production. It plans to double capacity between Q4 of 2025 and the end of this year.

"A major focus of this expansion will be an increased investment in our six-inch indium phosphide product," remarked Young.

Helping fund this effort is a raising of $630 million this April, thanks to an over-subscribed public offering of common stock, initially planned to raise $550 million.

AXT's GaAs substrates are used for the production of VCSELs, which are widely deployed in data centres. However, while a ramp in production of this class of laser will increase substrate demand, its impact will be minimal, as these devices are small. In contrast, VCSELs for machine vision are much larger. "They also require high quality material, which we are very well positioned to supply," said Young.

Another strength of AXT is its vertical integration, with subsidiaries involved in raw material supply and the manufacture of InP crucibles.

"JinMei has begun to refine high-quality indium, which gives us direct control of a guaranteed supply of yet another critical material for our indium phosphide substrates," remarked Young.

For the first fiscal quarter of 2026, AXT is forecasting total revenue of $26 million, based on orders with a permit to ship, and those that don't require permits.

Offering some insight into the impact of permits, the VP of Business Development, Tim Bettles, explained in the investor call on 19 February that once a license is granted, AXT has a maximum of a 6-month window to deliver – and customers are often keen to receive substrates before this.

Demand shows no sign of abating. "We are talking about long-term supply agreements with a number of customers right now, and we are planning our business, according to those long-term supply agreements," said Bettles, who added: "We're seeing forecasts out beyond 2030 for many of

Compound Semiconductor Shareprice Leaderboard

Rank	Company	Ticker	Share value, April 25, 2025 ($)	Share value, April 27, 2026 ($)	% appreciation	Change in Rank
1	AXT	AXTI	1.38	71.91	5110.9	+11
2	Lumentum	LITE	58.82	855.74	1354.8	-1
3	WIN Semiconductor (Taipei)	3015.TWO	2.77*	17.65*	537.2	+4
4	IQE (London)	IQE	0.122*	0.881*	524.0	+9
5	Riber (Paris)	RIB	2.86*	16.07*	461.7	-1
6	Coherent	COHR	63.02	330.50	424.4	-4
7	Aixtron (Frankfurt)	AIX	12.39*	52.19*	321.3	+4
8	Veeco	VECO	19.00	53.63	182.3	+1
9	IPG Photonics	IPGP	57.05	125.55	120.1	-3
10	Wolfspeed	WOLF	18.00**	32.17**	78.7	4
11	ams OSRAM	AMS.SW	8.65*	15.13*	74.9	-6
12	NASDAQ composite	IXIC	17182.11	24799.64	44.3	-9
13	Qorvo	QRVO	62.54	85.53	36.8	-3
14	Skyworks	SWKS	61.02	63.70	4.4	-6

➤ * Converted to dollars using the exchange rates on 27 April of 1 EURO = 1.175 USD, 1 GBP = 1.355 USD, 1 CHF = 1.276 and 1 TWD = 0.03181. ** Wolfspeed restructured its finances on 29 September, 2025. The new share price on that date is used as the initial share price.

these customers, but those numbers are increasing on a week-by-week basis."

Lumentum's momentum

After topping last year's leaderboard with an appreciation of almost 40 percent, Lumentum, a maker of optical components, has dropped to second place, despite increasing its share price by more than 1300 percent.

Unlike AXT, Lumentum is profitable, with revenues at record levels and accelerating.

Emphasising that point when speaking to investors on 3 February 2026, in an earnings call to discuss results for second fiscal quarter of 2026, President and CEO Michael Hurlston remarked: "While we previously projected crossing $750 million in quarterly revenue by mid-2026, we now expect to comfortably surpass that milestone next quarter."

Hurlston claimed that Lumentum is a foundational engine of the AI revolution. "Virtually every AI network is powered by Lumentum technology, either through our direct hyperscaler partnerships, or as the critical component supplier that enables our network-equipment-manufacturer customers."

Lumentum, which believes that the vast majority of growth is still to happen, has identified three 'primary catalysts' for future growth: optical circuit switches, cloud transceivers, and co-packaged optics.

Discussing each in turn, Hurlston said that customer demand for optical circuit switches is intensifying, with an order backlog that's surged well past $400 million. "Barring any unforeseen manufacturing or supply chain disruptions, we are well positioned to deliver on this substantial pipeline."

Hurlston claimed that the company's execution in cloud transceivers has reached a definitive turning point. According to this CEO, Lumentum is now a leading transceiver supplier, with success coming at time when customers are transitioning networks to 1.6T speeds. "Beyond design execution, we are also improving the profitability of our transceiver business, with better yields and lower scrap rates."

Sales of Lumentum's co-packaged optics are also thriving, thanks in part to a purchase order worth hundreds of millions of dollars for the company's ultra-high-power lasers that support optical scale-out applications.

In addition to these three revenue streams – optical circuit switches, cloud transceivers, and co-packaged optics – Lumentum is eyeing an opportunity in the external light source market. Success in this sector would diversify the company's customer base.

Hurlston also discussed optical scale-up, described as a generational game-changer for the industry. "Today, data centre architectures have a clear divide," said Hurlston, who argued that optical links handle scale-out networking, connecting relatively longer links within the data centre, while ultra-short copper links are deployed within a single rack or a cluster. "While copper has long been the gold standard for scale-up for simplicity and cost, it is hitting a physical wall. An industry pivot is underway to bypass the scaling limits of copper. By late calendar 2027, we would expect our first scale-up CPO shipments, replacing longer copper connections."

To respond to surging customer demand, Lumentum is increasing capacity through tool optimisation and yield gains. Even so, Hurlston revealed that the company is not meeting all customer demand, and its capacity for EMLs is 'spoken for' in long-term agreements (LTAs). "We have very tight LTAs that run through the balance of calendar 2027."

Lumentum is working to increase its capacity. This March it announced that it had purchased a 240,000 ft^2 facility in Greensboro, NC, from Qorvo. Production at this fab is expected to ramp in mid-2028. Nvidia, which has recently invested £2 billion in Lumentum, will serve as a customer of this facility, which could employ 400 staff.

Winning WIN

In third place on this year's leaderboard, just ahead of global epiwafer supplier IQE, is the Taiwan foundry WIN Semiconductor.

WIN's share price has climbed by more than 500 percent over the last 12 months. Gains have been supported by revenue that has recently climbed. For the most recent results, for the fourth fiscal quarter of 2025 that concluded at the end of calendar 2025, sales were up 7 percent over the previous quarter, and 29 percent higher year-over-year. Manufacturing margins are also improving, in part to a favourable product mix, with a consolidated gross margin for Q4 of 31.8 percent, up 4.9 percent sequentially.

For many years, WIN has focused on providing a foundry service for wireless products. However, it is diversifying into the optical sector, a move that will improve profitability, and allow WIN to play a role in the supply chain for components for data centres.

Commenting on the revenue mix in an earnings call on 1 February, 2026, to discuss Q4, general manager Steve Chen explained that yearly cellular revenue had fallen compared with 2024, due to WIN's shift in focus to mid-high and premium models. For WiFi, per annum sales climbed by 11 percent, due to increasing adoption of WiFi 6 and WiFi 7. WIN's infrastructure sales also grew year-over-year, increasing by 5 percent, due to a rise in satellite launches and more demand for GaAs for optical drivers, according to Chen. He remarked that for WIN's optical sector, sales fells by around 15 percent from 2024 to 2025. Here, there's been a softening of the market for 3D

sensing, which initially accounted for 60 percent of WIN's optical revenue. Across all of these sectors, the most promising product for WIN is its 1.6T optical GaAs driver that can serve in AI datacentres. According to the company, demand for GaAs optical drivers will grow more than three-fold between 2025 and 2026.

Chen claimed that the company will be able to enjoy success in the optical market, due to strong relationships with tier-1 customers. Its portfolio will expand from VCSELs and InP PICs, both in mass production, to include CW lasers and EML lasers, with the broader range of sources covering optical links spanning a vast range of distances. "Right now, our CW laser and EML are undergoing qualification," remarked Chen.

Skyworks: Strong but last

For just the third time in 20 years, all companies on the leaderboard increased in valuation over the last 12 months. But for Skyworks, footing this year's table, appreciation over that timeframe was just 4.4 percent (note that its rival, Qorvo, which Skyworks is due to merge with early next year, only placed just one spot higher, indicating that makers of wireless chips are operating in a very different space from those making components that can serve in data centres).

Over the last 12 months, Skyworks' share price has not moved that much, staying above $55 and peaking just above $80, and finished at a little more than $60 at the closing date for the leaderboard. Unlike some companies that have footed the table, Skyworks financial performance is solid – and while AXT, the darling of the last 12 months is not making a profit, Skyworks is, and is putting in a strong financial performance. In its most recently reported quarter, the first fiscal quarter of 2026, which ended on 2 January, the company generated a revenue of $1.035 billion and an operating income of $104 million. Sales and gross margin, just shy of 47 percent, were above expectations.

Skyworks is well-known for its role in the mobile industry, providing front-ends that feature GaAs-based amplifiers. This sector is still Skywork's biggest earner. In Q1, 2026, mobile accounted for 62 percent of revenue, with the majority of sales associated with what's described as flagship and premium-tier devices. There's a heavy dependence on one customer, which accounts for two-thirds of Skyworks' mobile revenue.

Commenting on the company's sales to the mobile industry, in a call held on 3 February to discuss results for fiscal Q1 2026, Skyworks CEO Philip Brace remarked: "We outperformed expectations, supported by healthy sell-through and strong execution on new product launches at our top customer."

According to Brace, smartphone replacement cycles are lengthy, but beginning to shorten. "This trend is driving increased unit growth as consumers upgrade more frequently, especially with the rise of new AI-capable devices and more integrated features."

Skyworks is also shipping products used in WiFi products, with the company helping to lead advances in this technology.

"Wi-Fi 7's higher throughput, lower latency and reliability, position it as an important enabler, as AI inference moves closer to the edge," said Brace. "Design win activity remains strong, backlog is healthy, and we're already engaged with customers on early Wi-Fi 8 programmes."

Skyworks is also involved in the automotive market, where it provides device connectivity, and in data centre infrastructure, where it has products supporting timing accuracy and improving power performance.

For the next fiscal quarter, sales are forecast to fall to around $900 million, with mobile dropping by around 20 percent, which is said to be consistent with seasonality.

As well as this guidance, those on the call looked further ahead, offering views on the merger with Qorvo.

Brace remarked: "We believe this transaction is highly strategic and transformative, bringing greater scale, deeper R&D, and a broader technology portfolio. Together, this combination is expected to reduce historical mobile volatility, strengthen our competitive position, enhance our broad market capabilities, and expand our TAM into defence and aerospace, while creating a clear path to more than $500 million of synergies over time." It is expected that gross margins in the merged entity will be 50-55 percent.

If the merger is approved, and proceeds on time, the new entity will be listed on the 2027 leaderboard. Which position it will take is anyone's guess, and after the astonishing figures from this year, who knows what the future will hold. We'll just have to wait and see.

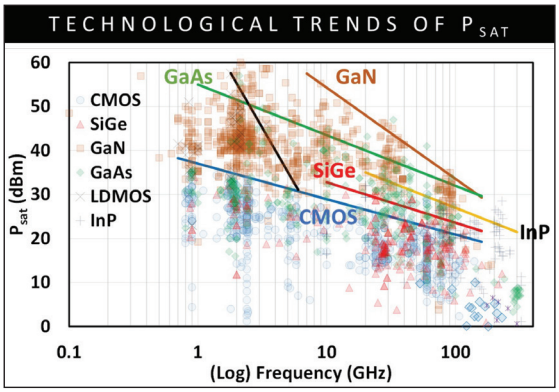
A new foundation for the InP HBT

Combining InP HBTs with Soitec's SmartCut technology creates a cost-effective, sustainable InP-on-silicon technology for advanced communication systems

BY ABHITOSH VAIS FROM IMEC

THROUGHOUT this century, communication systems have been driving the useable frequency spectrum to higher values. It's a direction of travel that facilitates higher bandwidths; and ultimately high data rates, low latency and gains in energy efficiency.

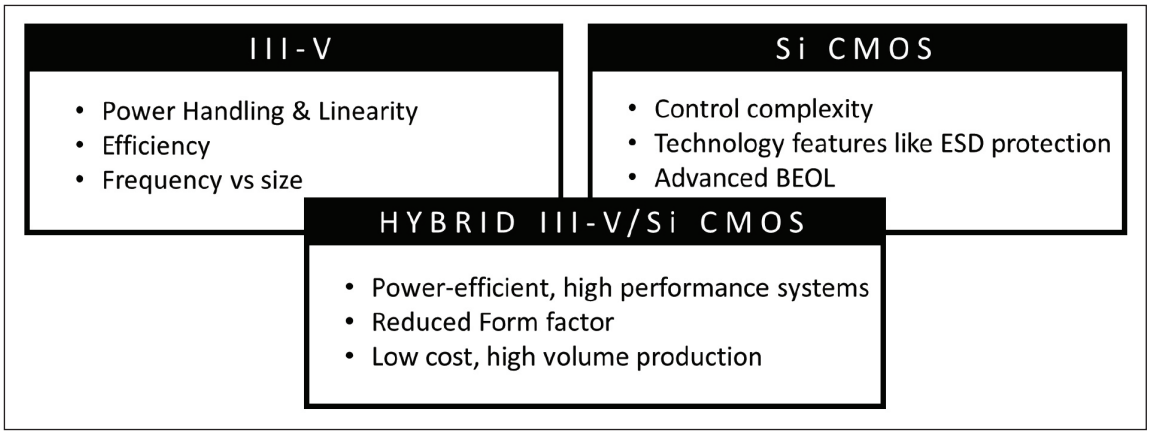
This trend shows no sign of abating, with demand strong for more and faster data connectivity. But the semiconductor technology that forms the backbone of these communication systems is now at an inflection point. The troublesome concern is that the technologies currently available for critical system components, such as power amplifier (PA) modules, are no longer meeting the performance and energy efficiency required by communication systems while operating at such high frequencies (see Figure 1). Motivated by this limitation, new materials and devices are being explored to fulfil these requirements.



➤ Figure 1. Technological trends in output power, P_{sat}, followed by different technologies with respect to operating frequencies. Solid lines are only to guide the eyes. [H. Wang *et al.*, "Power Amplifiers Performance Survey 2000-Present," [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html

Speeding communication with III-Vs-on-silicon

Within the family of compound semiconductors, III-V-based devices, and HBTs in particular, are



➤ Figure 2. III-V and silicon CMOS have their own advantages. When combined together in a hybrid technology, they can provide a solution for future RF applications.

strong contenders for next-generation high-speed communication systems. The latter class of device has generated significant sales for decades, with GaAs/InGaP HBTs grown on small size native GaAs substrates widely deployed in mobile phones, thanks to several advantages over other material combinations.

However, the technologies for high-speed communication systems, such as 6G and advanced wireline applications, require better RF performance. In particular, they need to excel when judged against a number of key metrics – they are the cut-off frequencies f_t and f_{max}, the output power (P_{out}), and the power-added efficiency (PAE) – while offering the opportunity for high-volume production at a significantly lower cost, as well as providing flexibility in circuit design, and having a smaller chip footprint.

It's possible to fulfil all these requirements with the integration of III-Vs on silicon substrates, using a state-of-the-art CMOS back-end-of-the-line (BEOL) process for routing complex control signals (see Figure 2).

When considering whether to pursue this approach, one should note that there's a significant challenge when integrating III-Vs, such as GaAs or InP, with silicon: a large lattice mismatch. Due to this issue, epitaxial growth spawns defects, with subsequent integration leading to a defective material system and unsatisfactory performance.

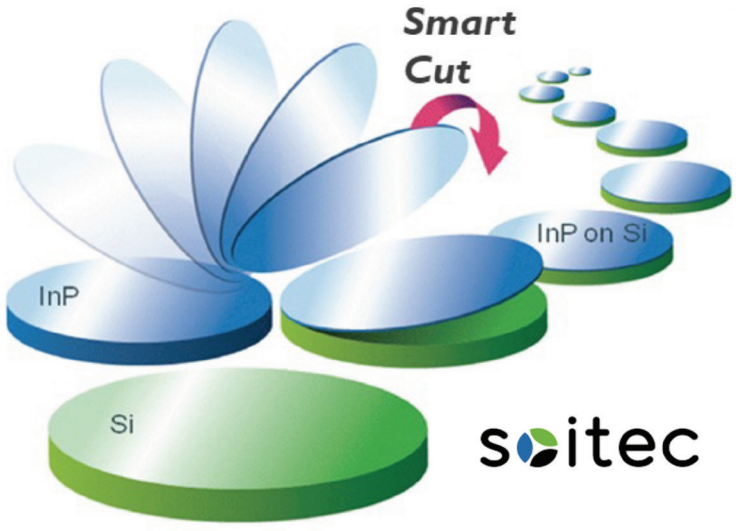
One option for circumventing this issue is a form of heterogenous integration that separates the III-V front-end-of-line (FEOL) and CMOS BEOL fabrication processes, and uses flip-chip bonding to subsequently unite the modules. It is a *modus operandi* that provides high-quality III-V devices on silicon, but at the expense of significant wastage of precious III-V material. Given the geo-political significance and scarcity of such material, the cost and sustainability of a technology will probably define its useability.

A hybrid III-V/CMOS technology

Given this concern, an attractive alternative is to transfer a thin III-V film from a native III-V substrate, instead of bonding a whole substrate to the target silicon wafer. With this approach, the thin III-V film provides a foundation for the growth of a good quality III-V device stack.

Helping those that wish to explore this approach is Soitec's recently developed process for transfering thin films of InP from native substrates to silicon target wafers. It's a technology that's scalable to 200 mm and 300 mm silicon wafers, and allows the native pseudo-donor wafer to be re-used for several cycles of transfer. Strengths of this technology include maintaining the quality of InP when it's on silicon, and consuming very little of the latter, thereby ensuring it's an environmentally sustainable solution.

At imec, our team is adopting this approach. In our case, we are working on the development of a hybrid III/V-CMOS technology that utilises InP-on-silicon wafers, employing them as a foundation for fabricating InP HBTs on 200 mm silicon wafers. Success on this front would deliver



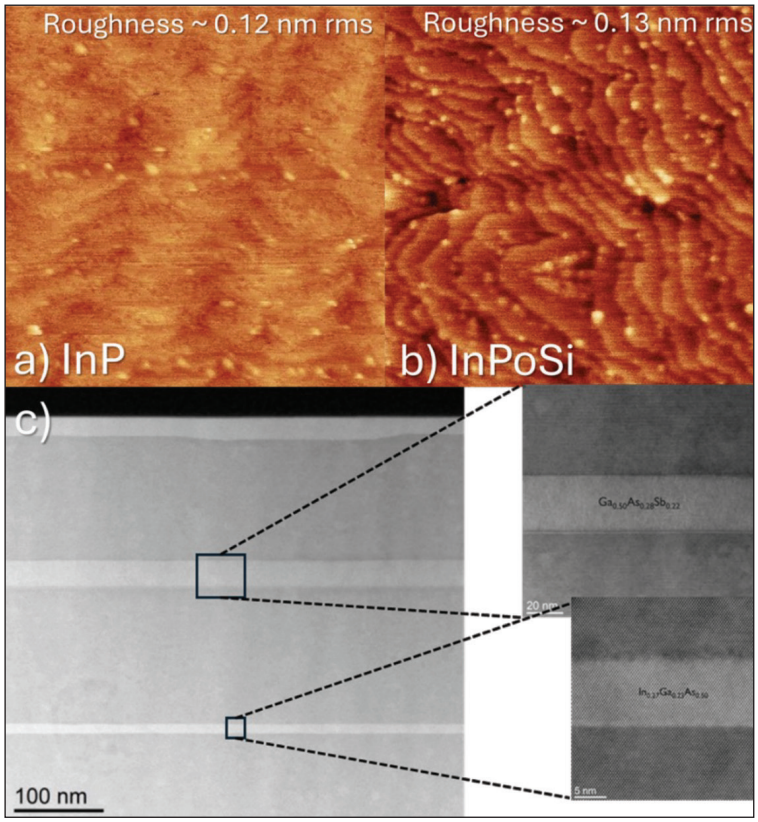
➤ Figure 3: A cartoon illustration of the Smart-Cut process of transferring thin films of InP onto a silicon substrate. [B. Ghyselen, *et al.*, Digests of 2023 International Conference on Compound Semiconductor Manufacturing Technology (2023)].

scaled process control and high-volume integration capabilities with CMOS. These attributes could be a game-changer for the InP HBT, which is currently limited by lab-like production environments. Our advance promises to provide a cost-effective solution for meeting high-performance and scalability demands of future communication applications.

Growing InP HBT stacks

The starting point for our efforts is Soitec's 100 mm InP-on-silicon substrates, which features a thin film of InP (approximately 0.5 μm) that's transferred to a 100 mm silicon wafer. We load these engineered substrates into an MOCVD chamber and grow an InP HBT stack.

To check the quality of the epilayers, we use two common characterisation techniques: atomic force microscopy (AFM), for surface quality; and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), for epitaxy quality. With AFM, we find the root-mean-square roughness, a measure of surface quality, is similar for our InP-on-silicon structures and those grown on InP. On both platforms, root-mean-square roughness is around 0.13 nm, a value that indicates good epitaxial growth (see Figure 4 (a) for AFM scans)).



➤ Figure 4. A 2 μm x 2 μm atomic force microscopy scan (a) (and corresponding root-mean-square (rms) values (b)) of the top device surface on InP and InP-on-silicon substrates. (c) A high-angle annular dark-field scanning (HAADF-S) transmission electron microscopy (TEM) image of InP HBT stack grown on InP-on-silicon with insets representing: (top), InP/GaAsSb/InP interface; (bottom), InP/InGaAs/InP interface.

Additional evidence of epitaxial growth quality is found in HAADF-STEM images (see Figure 4 (b)). Interfaces are sharp and free from defects.

We use verified, high-quality HBT stacks to fabricate our devices. These transistors are evaluated, to assess both their electrical performance and that of the epi-stack.

Our investigations have considered transfer characteristics, using the Gummel plot. Analysing this data has allowed us to extract a number of metrics, including DC current gain (β), the ideality factor of the current-voltage characteristics ($n_{base/ccollector}$), and the leakage current of the heterojunctions. Ideality factor and leakage current are good metrics for epitaxial and heterojunction evaluation, and DC current gain is a good indicator of device performance.

Benchmarking performance

When we compare the ideality factor of the base current of our device fabricated on the Soitec platform and our control, we find no clear difference. This highlights the good quality of our InP-on-silicon HBTs.

We obtained similar results when studying leakage currents, but uncovered a difference in peak DC current gain, β, at a base-emitter voltage of 1 V: a value of 30 for the HBT on the native substrate, and around 56 for that on InP-on-silicon. We attribute this variation to a difference in the effective doping of the base layer, a view supported by transmission-line measurements that determine the sheet resistance and contact resistivity of the base layer on both substrates. Differences in doping stem from variations in the effective growth temperature on the surface of InP and InP-on-silicon substrates, a consequence of the presence of a thick buried-oxide layer in the heterogeneous device. It's possible to match the gain in both forms of HBT by carefully calibrating the base doping level for epilayers grown on the InP-on-silicon substrates.

Another metric for evaluating device performance is breakdown voltage. A higher value is a valued asset, as it tends to define the operating limits of the system – and higher breakdown voltages hold the key to higher-power generation. We have not observed any discernible difference in the breakdown voltages of our HBTs on InP and InP-on-silicon substrates. This finding provides further corroboration of the quality of the epitaxial growth on the InP-on-silicon substrate.

It's not enough to evaluate a technology for RF applications with only DC metrics. RF evaluation is essential, but demands special metrology structures. In addition, it critical to undertake careful calibration of the measurement setup, using dedicated calibration structures and strategies for correct data analysis.

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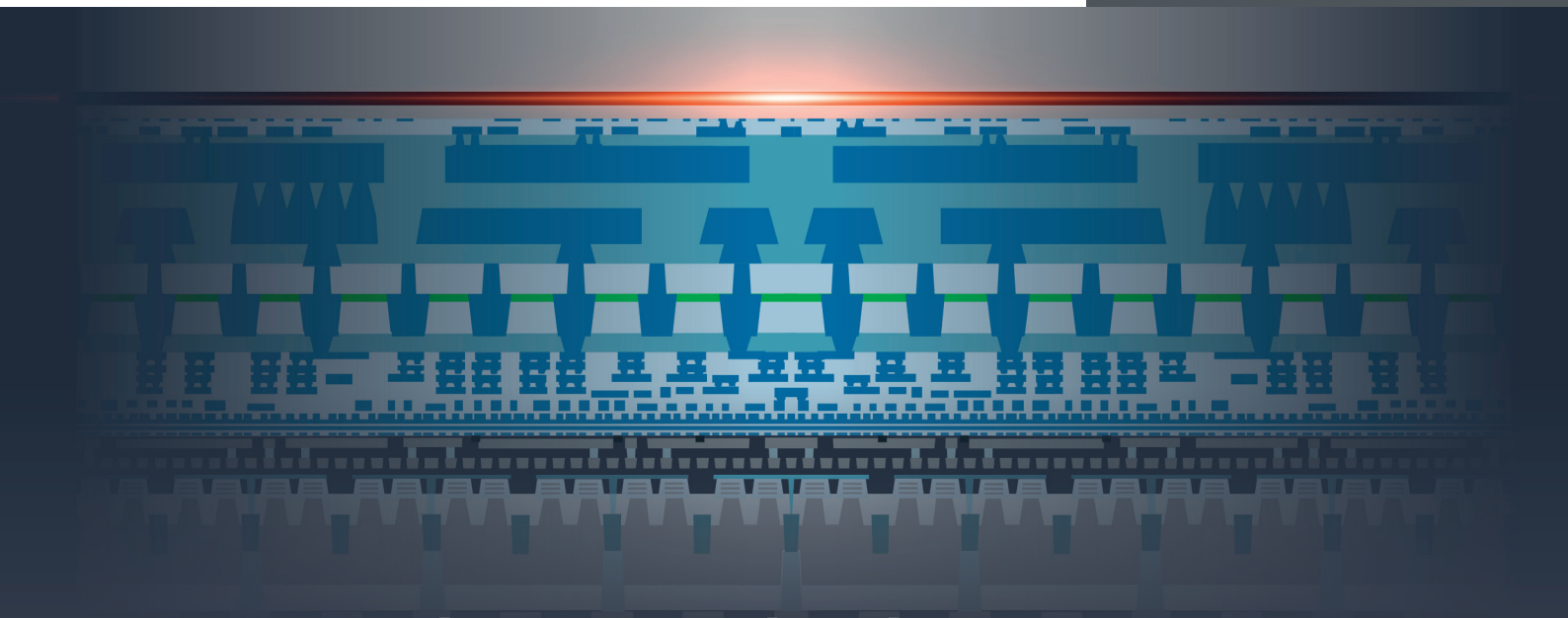

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To fulfil these criteria, we fabricated RF devices and structures on InP and InP-on-silicon substrates, for RF characterisation of our HBTs. This allows us to determine the impact of InP-on-silicon wafers on RF performance.

A key finding from this work is that HBTs on both substrates have a cut-off frequency of up to around 140 GHz. While this performance is not on a par with the state-of-the-art, it confirms that InP-on-silicon substrates provide a good alternative for the fabrication of InP HBTs, as there's no degradation in performance.

Self-heating and thermal management

HBTs have great potential to generate highly-efficient, linear power at RF and millimetre-wave frequencies. But these high output-power densities come with a catch – significant heat generation in the active device region. As temperatures rise, driven by heat generation, device performance may decline, and in the worst case, the chip can even burn. So, it's imperative to have a path for efficient heat removal from the device, and even the chip as a whole.

While GaAs- and InP-based HBTs have a superior high-speed performance with a higher drive voltage than their silicon CMOS and bipolar counterparts, they are more prone to self-heating effects. This issue stems from the relatively poor thermal conductivity of the III-V materials, including the internal III-V ternary compounds. For example, InGaP, InGaAs and GaAsSb all possess thermal conductivities that are an order of magnitude lower than those for silicon. These factors are responsible for aggravated thermal issues that threaten to degrade device performance and impact device reliability. Due to this, thermal management is key to realising high-performance InP HBT heterogeneous integration.

In addition to these issues associated with III-V materials, InP-on-silicon substrates contain a layer of SiO_2, another poor thermal conductor. There's the fear that this could exacerbate the thermal management of HBTs on InP-on-silicon substrates.

To investigate the impact of the oxide layer on the thermal performance of InP-on-silicon substrates, we have performed extensive thermal simulations, using an in-house 3D thermal simulator. This work indicates that the thickness of this oxide layer plays an important role in defining the efficiency of heat removal on InP-on-silicon substrates. We have also noticed that trimming the oxide thickness to below 50-100 nm diminishes its impact significantly, so that this structure is equivalent to that without an oxide layer.

These insights, provided by our simulations, are an important step towards achieving a thermally efficient InP-on-silicon solution for high-speed communication systems based on InP HBTs. Encouraged by these findings, we are devoting significant effort to practical implementation on InP-on-silicon substrates. The outlook appears to be positive.

We have no doubt that cost-efficient, sustainable integration of III-Vs on silicon is critical for the success of future high-speed communication systems. The current state-of-the-art on InP and/or transferred substrates might fail to satisfy some of these requirements in high-volume production applications – but InP-on-silicon substrates promise to provide a sustainable solution.

Our efforts have demonstrated that devices fabricated on InP-on-silicon can deliver a similar performance to those formed on InP; and that InP HBT technology that incorporates an InP-on-silicon foundation could be a cost-effective solution for meeting the high-performance and scalability demands of future applications.

SiC: Enhancing reliability with ion implantation

By stopping the movement of partial dislocations, high-energy ion implantation provides an approach for improving the reliability of SiC devices

BY MASASHI KATO AND TONG LI FROM NAGOYA INSTITUTE OF TECHNOLOGY, SHUNTA HARADA FROM NAGOYA UNIVERSITY, AND HITOSHI SAKANE FROM SHI-ATEX

OVER THE LAST FEW YEARS, SiC power devices have started to fulfil their tremendous potential. Sales are climbing fast, with global revenues now worth several billion dollars per annum, thanks to the deployment of these devices in trains and electric vehicles.

However, there's still substantial room for improvement in the manufacture and performance of these power devices, which tend to be produced using the 4H-SiC polytype. One issue is a high cost, which hampers penetration in hybrid electric vehicles, electric power sources for data centres, and other applications. This weakness is exacerbated by concerns surrounding manufacturing yields for devices that guarantee long-term reliability.

One phenomenon impairing the long-term reliability of SiC power semiconductor devices is bipolar degradation. This occurs when a current flows through a *p-n* junction, injecting electron-hole pairs into the material. After penetrating the drift layer, electron-hole pairs recombine in the 4H-SiC substrates at basal plane dislocations (BPDs) – they are dislocations located on the (0001) crystal plane of 4H-SiC. This is not the end of the story, as each BPD splits into two partial dislocations (PDs), which lead to the formation and expansion of stacking faults (SFs) in the epitaxial layer surrounding the PDs.

These expanded SFs are behind the degradation in performance of SiC power devices. Contributing to the electrical resistance component in the forward diode characteristics, they provide the source for the leakage current.

Complicating matters, degradation is difficult to detect during initial device operation. This is a significant issue, with reduced manufacturing yield accompanied by an increase in the cost of reliability testing.

A number of approaches have been pursued to reduce the injection of electron-hole pairs, and ultimately suppress SF expansion. One method involves the introduction of a recombination-enhancing layer between the drift layer and the 4H-SiC substrates. This addition eliminates the injected electron-hole pairs, so they no longer reach the substrate. Another strategy, explored by several

groups, is to use SiC MOSFETs with embedded Schottky barrier diodes. This combination quashes the generation of electron-hole pairs, even at active phases of diode operation. However, none of these technologies delivers a complete solution to bipolar degradation.

Offering an innovative alternative to address this problem is our team, a long-term collaboration between Nagoya Institute of Technology, Nagoya University and Shi-Atex, a company with tremendous expertise in high-energy ion implantation technology.

Our partnership draws on a strong academic background in materials science that spans semiconductors and metals. This led one of us, Shunta Harada, to introduce a new idea for preventing the degradation of SiC power devices via the intentional introduction of impurities, such as hydrogen. Critical to the success of this approach is fixing the impurities to BPDs, a step that stops the movement of PDs that make up BPDs. Once the movement of PDs is halted, expansion into SFs is prevented. Note that this is a similar concept to hardening metals, such as iron becoming steel through the introduction of carbon impurities.

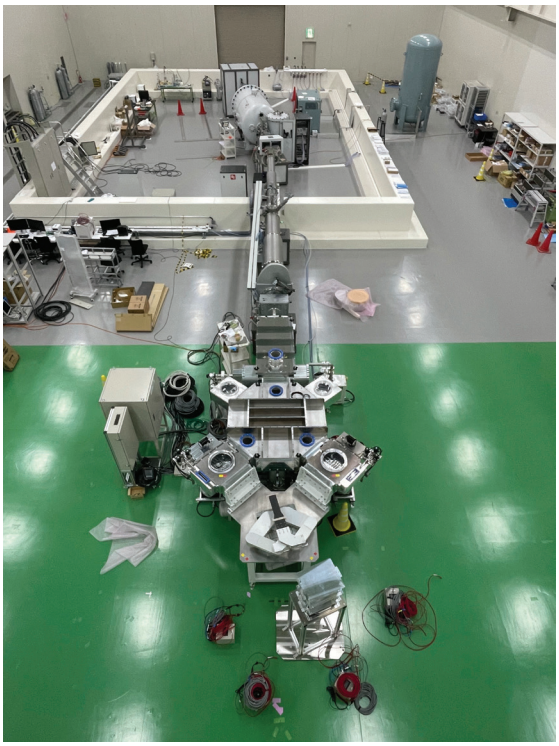
Key to our investigation is the tandem-type accelerator owned by Shi-Atex (see Figure 1). This accelerator has enabled us to apply high-energy ion implantation to SiC power devices, a step that promises to suppress bipolar degradation. Initial progress was assisted by students at Nagoya Institute of Technology, before Tong Li joined the team, supporting widespread utilisation of high-energy ion implantation for SiC power devices.

Rationale for high-energy ion implantation

During conventional ion implantation into 4H-SiC, ions reach a depth of less than 1 μm, because accelerated energies are usually below 1 MeV. To put that depth into context, note that 4H-SiC epitaxial wafers have epitaxial layer thicknesses between 5 μm and 60 μm, and a typical substrate thickness of around 350 μm.

In our case, as we want to stop the movement of PDs in the substrate near the epitaxial layer, we need the implanted ions to reach the interface of the epitaxial layer and the substrate. To fulfil this objective, we use high-energy ion implantation, shown schematically in Figure 2.

Let's consider a SiC power device with a typical voltage rating. Based on this criterion, we have selected a 1.2 kV-class device that has an epitaxial layer thickness of 10 μm. To implant hydrogen ions (protons) to the interface from the epitaxial layer surface, we require an acceleration energy of around 1 MeV; and to reach this interface from the substrate side, we need much higher energy of around 8 MeV (in fact, we have only achieved an implantation depth of around 330 μm so far, but even this is effective for our purpose). Note that even higher implantation energies are needed if we employ heavier ions. For example, implantation of helium ions to a 10 μm depth requires around 3.6 MeV.

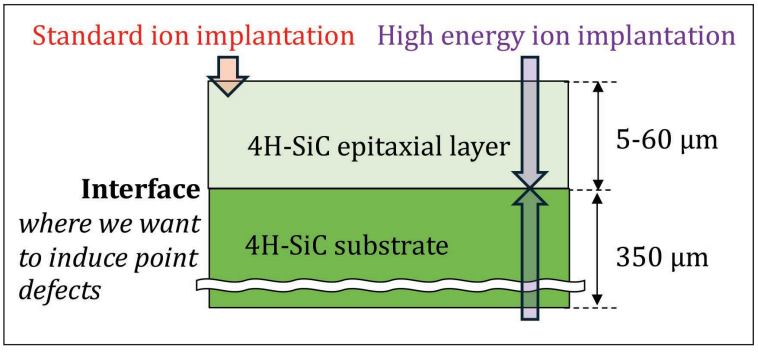


➤ Figure 1. The tandem-type accelerator in Shi-Atex for high-energy ion implantation of SiC. The accelerator is located at the top of the photo, while the wafer handling stage is located at the bottom.

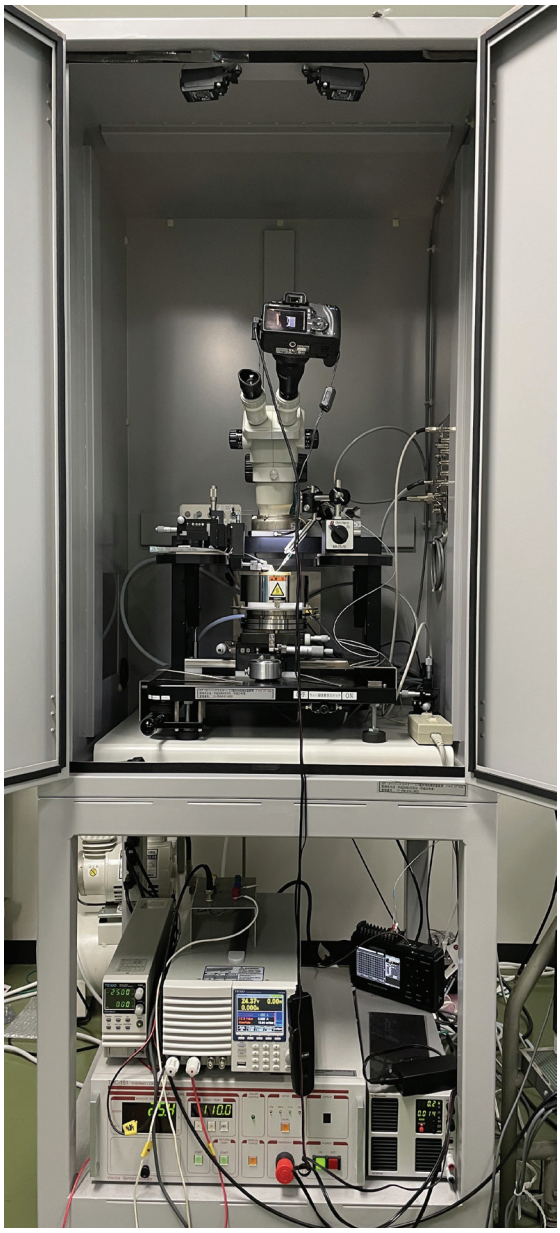
Reliability testing

We began our investigations into the effect of high-energy ion implantation on SF expansion by using UV illumination and X-ray topography to observe any changes to 4H-SiC epitaxial wafers. Without high-energy ion implantation, and prior to UV light illumination, the BPDs appear as straight lines in the X-ray topography images. But after UV light illumination, the BPDs expand into SFs in the epitaxial layers, appearing as triangles in the X-ray topography images.

With high-energy ion implantation, this situation changes markedly. In this case, the BPDs kept the



➤ Figure 2. Schematic of a SiC epitaxial wafer and depths of ion implantation. With standard ion implantation, ions cannot reach the interface of the epitaxial layer and the substrate.



➤ Figure 3. Prober (the top) with power sources and a temperature controller (the bottom) for electrical stress tests for SiC *p-i-n* diodes.

same straight lines in X-ray topography images after UV illumination. This observation confirms the effectiveness of high-energy ion implantation.

Following this confirmation, we applied our technique to devices, fabricating *p-i-n* 4H-SiC epitaxial wafers. Our process involved aluminium-ion implantation into the epitaxial layer to create a *p*-type layer on the surface. We then performed activation annealing of aluminium, an acceptor impurity, at typically 1650-1750 °C. Using photolithography and subsequent lift-off of the metal, we added metal contacts on the substrate-side and patterned metal contacts on the surface-side. Finally, we annealed the wafer, forming an ohmic contact by reaction of the metals and 4H-SiC.

We conducted high-energy ion implantation on bare 4H-SiC epitaxial wafers before forming our *p-i-n* diodes. This approach is adopted because after high-energy ion implantation, high-temperature annealing is required to recover damages caused by implantation. Without this, the *p-i-n* diodes would have a very high series resistance.

Initially, we implanted protons from the epitaxial side of the bare epitaxial wafers. Using additional wafers, we implanted helium ions from this side to assess the effects of different ions; and implanted protons from the substrate side, to determine the impact of backside implantation.

Using electrical stress tests, we investigated the reliability of our implanted and conventional *p-i-n* diodes, considering their susceptibility to bipolar degradation. Our study involved applying pulsed currents from 200-850 A cm^{-2}, with the particular value depending on diode performance.

These measurements involved a prober system with power sources and a temperature controller (see Figure 3, and Figure 4 for a photo of a *p-i-n* diode under probing). During measurements, temperature was monitored by the thermocouple and fed back to the temperature controller.

During and before/after the test, we observed SF expansion in electroluminescence images, obtained though stripes of the patterned contacts on the epitaxial layer surfaces. The dark regions observed in the electroluminescence images correspond to locations with expanded SFs.

As expected, our *p-i-n* diodes that have not benefited from high-energy ion implantation suffer from a significant number of expanded SFs. These faults are seen in the dark regions in the electroluminescence images (see Figure 5, which

Based on our results, it is clear that point defects induced by high-energy ion implantation effectively suppress bipolar degradation, thereby ensuring SiC device reliability. We believe that this technology is applicable to any SiC device: any structures, and any ratings. Thanks to ion implantation, all SiC power devices can offer high reliability, resulting in a reduction in their cost.

provides an example of uniform and nonuniform electroluminescence images for before and after stress, respectively).

In stark contrast, our *p-i-n* diodes that have the advantage of high-energy ion implantation enjoy significantly reduced SF expansion, and their electroluminescence images are relatively uniform, even after stress. This is a repeatable finding – we have obtained reproducible results, demonstrating that *p-i-n* diodes with high-energy ion implantation show a significantly smaller number of expanded SFs. Note that suppression of SF expansion is effective, irrespective of the type of implanted ions (protons or helium ions) and the implantation side.

Mechanisms and future

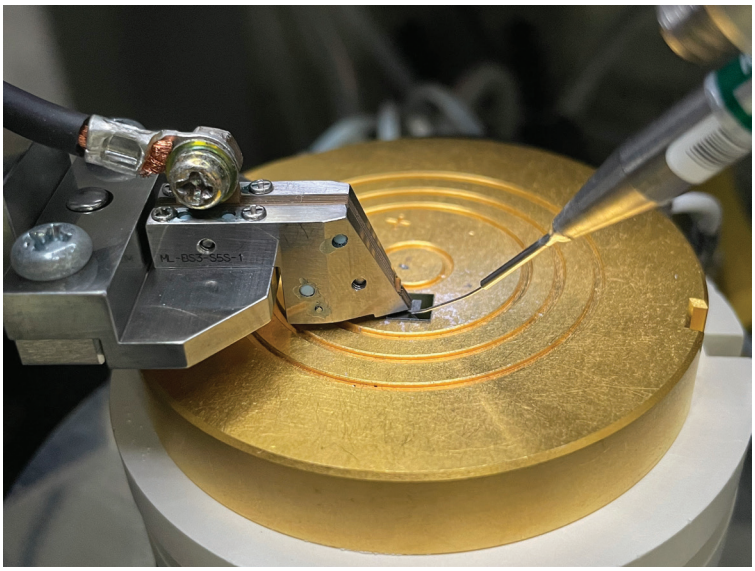
As the type of ion does not seem to play a role in suppressing SF expansion, it appears that a key factor behind our success is the presence of point defects that are induced by high-energy ion implantation, rather than the implanted species.

To delve deeper into this hypothesis, we have turned to original equipment in Kato's group to observe the distributions of point defects and carrier recombination lifetimes, using cathodoluminescence and microscopic time-resolved free-carrier absorption measurements. These techniques have confirmed that p-i-n diodes that have undergone high-energy ion implantation have point defects and a reduction in carrier recombination lifetime near the interface of the epitaxial layer and the substrate

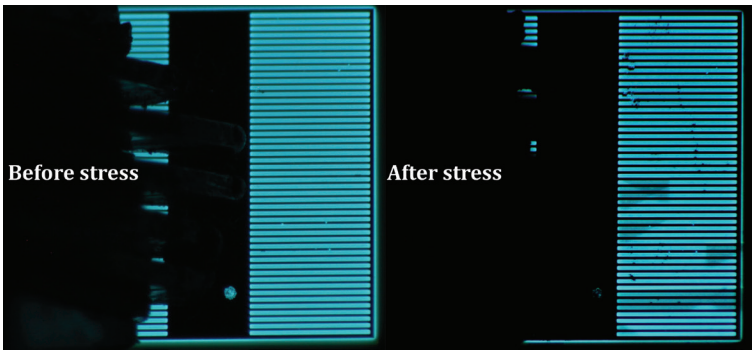
While this finding is helpful, there's still a crucial question to answer, related to the underlying mechanisms: Is the reduction in PD mobility due to point defects? Or is it due to a reduction in carrier recombination lifetime around BPDs, due to recombination centres originating from point defects? At the very least, we have already determined that the presence of point defects near interfaces plays a key role in suppressing bipolar degradation; and that implantation is effective from the substrate side, implying that our technology is applicable to device structures with any epitaxial layer thicknesses.

Based on our results, it is clear that point defects induced by high-energy ion implantation effectively suppress bipolar degradation, thereby ensuring SiC device reliability. We believe that this technology is applicable to any SiC device: any structures, and any ratings. Thanks to ion implantation, all SiC power devices can offer high reliability, resulting in a reduction in their cost.

This should open the door to the expansion of SiC power devices to a wider range of applications, leading to a reduction in humanity's energy consumption. In short, high-energy ion implantation technology promises to be a game changer.



➤ Figure 4. A diode under probing. The diode is placed at the centre of the stage, and electrical power applied to the diode from the wire at the left-hand side. The thin probe is a thermocouple, to detect the temperature of the diode.



➤ Figure 5. Electroluminescence images for diodes before (left) and after (right) electrical stress tests without high-energy ion implantation. After electrical stress tests, triangle and bar shape dark regions appear.

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SiC substrates with table-top closed-space PVT

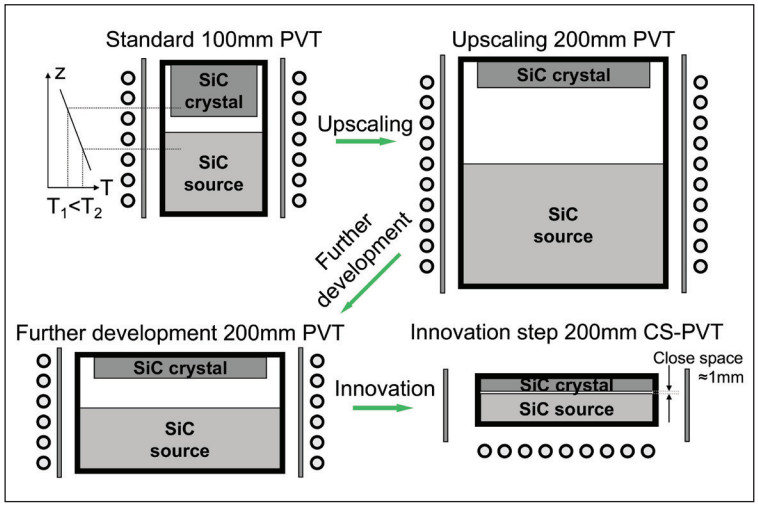
Large-area, high-quality SiC boules can be produced with a table-top closed-space PVT tool that provides ideal thermal gradients

BY PETER WELLMANN FROM THE UNIVERSITY OF ERLANGEN-NÜRNBERG (FAU)

SINCE THE TURN of the century, the commercial production of SiC has benefited from huge technological progress. Over that timeframe substrate diameters have expanded from just 50 mm to 200 mm, and the first 300 mm variants have just been demonstrated.

However, size is not everything. Quality is critical – and that's an issue for 150 mm and 200 mm SiC substrates, with defect densities, and in particular a prevalence of dislocations, hampering the performance and reliability of SiC-based power devices.

What's the origin of this troublesome issue? Well, in a nutshell, it's the excessive radial thermal gradients present during crystallisation of SiC at 2000°C in state-of-the-art physical vapour transport (PVT) reactors (for more details see Figure 1 and the pull-out box "Basics on (CS-) PVT growth of SiC"). Addressing this issue is a modified technology known as close-space (CS) PVT. With this attractive alternative, a radical design for the growth cell ensures far lower radial thermal gradients – they are an order of magnitude lower than those for standard PVT. In addition to this benefit, the axial temperature gradient, which is the driving force behind crystallisation in all PVT-based crystal growth systems, can be much greater in CS-PVT than standard PVT.



➤ Figure 1. The evolution of standard PVT, prior to the introduction of CS-PVT.

Over the years, the desired dimensions of SiC boules have shifted, aligning more closely with the capabilities of CS-PVT. As the SiC substrate diameter has increased from 100 mm to 150 mm and now 200 mm, the shape of the boules has gradually changed from cylinders to flat pucks. This is seen in the fall of the crystal-height-to-diameter ratio from 1:1 to 1:5 and less. It's a trend that's forecast to continue, with the already initiated crystal diameter enlargement to 300 mm expected to be accompanied by a further decline in the aspect ratio to 1:8 or 1:10.

While it is possible to redesign the shape of the growth cell in PVT chambers, so that it's better-suited to producing flat cylinders, there is a compelling case for switching from this crystal growth technology to CS-PVT.

To help with this transition, our team at the University of Erlangen-Nürnberg (FAU) has developed a compact, table-top CS-PVT tool (see Figure 2). This versatile growth chamber can be easily integrated into a clean-room facility for device fabrication; deployed in a larger SiC wafer production line; and added to an academic research environment.

What makes CS-PVT special?

Unlike standard PVT, which uses an inert gas for growth rate control, CS-PVT tends to employ vacuum conditions. Another key difference, which results from the geometrical design of the growth cell, is the opportunity to draw on much higher axial temperature gradients without having to alter the low radial temperature gradient. Thanks to this pair of levers, growth engineers can lower the growth temperature at the crystal growth interface – for example, reducing this from 2050°C to 1900°C – while maintaining the growth rate employed in standard PVT. Due to this, the crystalline quality realised by CS-PVT should be at least as good as standard PVT, and potentially even higher.

One feature of most CS-PVT tools is a spacer thickness of around just 1 mm between the crystal growth interface and the solid SiC source. This configuration, along with the vacuum environment and the comparably low growth temperature of around 1900°C, creates a ballistic mass-transport regime. It's a *modus operandi* that differs from that of standard PVT, where the gas phase resembles an ideal gas with Brownian molecular motion. With CS-PVT the SiC-based gas species – mainly silicon, Si_2C and SiC_2 – move from source to seed without interaction, preventing gas-phase reactions from taking place between gas species.

➤ Figure 2. Sketches of basic CS-PVT bottom heater concept (left) and TableTopCS design (right) of the newly developed growth machine at FAU dedicated to CS-PVT of SiC thick layers and bulk crystals.

Crystal growth via ballistic mass transport is advantageous, offering favourable doping conditions for volatile dopants, such as the acceptor aluminium. In an ideal gas environment, aluminium would diffuse out, due to a higher partial pressure than the SiC-based gas species. Consequently, in the ballistic growth regime all acceptors are transferred from the sublimation surface to the crystallisation interface, enabling defined and high doping concentrations.

Today's power electronics employs the so-called 4H-SiC polytype, which has a hexagonal crystal structure. That's a shift from the early days of SiC development, when the focus lay on 3C-SiC, a polytype with a cubic crystal structure. As processing of bulk 3C-SiC turned out to be particularly challenging, 4H-SiC has been pursued as the SiC polytype for power electronics. However, this situation could revert, thanks to CS-PVT – it's a growth technology that provides far higher axial gradients than its standard counterpart, and thanks to the lower growth temperature, growth conditions are favourable for stable crystallisation. While efforts surrounding CS-PVT have been directed at high-quality, cost-efficient production of 4H-SiC, in future demand for 3C-SiC could be met by this growth technology.

A new CS-PVT tool

To fully exploit the benefits of the CS-PVT process, we have developed a new machine with characteristics that exploit the strengths of this growth process. Due to the flat design of the growth cell, we incorporate a bottom heater that heats up the system with the highest efficiency. Another strength of our design, which enables the growth of high-purity SiC layers, is an ultra-high vacuum (UHV) capability – we can reach vacuum levels as low as 10^{-8} mbar. What's more, our system is a table-top set up (see Figure 2), so it can be easily integrated into a clean-room facility for device fabrication, or deployed in either a larger SiC wafer production line or an academic research environment.

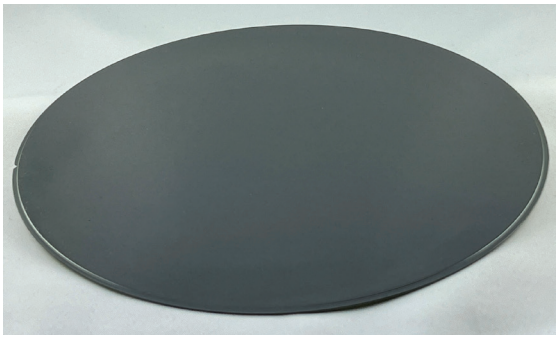
Our initial results highlight the capability of our TableTopCS system for preparing thick single-crystalline layers of *n*-type 4H-SiC (see Figure 3, which depicts a 200 mm SiC substrate with a CS-PVT-deposited *n*-type layer with a thickness of around 150 μm). This layer has been grown at a rate of approximately 300 μm hr^{-1}. We anticipate further process optimisation may lead to a reduction in growth rate to approximately 100 μm hr^{-1} to 150 μm hr^{-1}, but this is still quite a high value.

Despite a source-to-seed distance of typically 1 mm or so, it's possible to produce SiC crystals with a thickness of several millimetres with CS-PVT. To accomplish this, during consumption of the solid SiC source, its top level must be lowered synchronously as the newly grown crystal extends its height downwards into free space. With this approach, the space between the SiC source and the newly grown SiC layer or crystal remains constant.

Using this methodology, we have grown SiC crystals with a thickness beyond 6 mm. While we are still to explore the technical limit of crystal thickness, a value of 10 mm should be feasible. However, what's potentially difficult, from the point of process stability, is to reach a crystal boule height of 40 mm, a value obtainable in standard PVT.

Undercutting PVT?

Due to the potential reduction in boule height, when the CS-PVT process is employed for manufacturing SiC substrates, it requires three-to-four times as many boules as those produced by PVT to produce the same number of wafers. However, while growth rates are similar for both techniques, CS-PVT has a key advantage – far faster heating up and cooling



➤ Figure 3. Example of a 200 μm (ø196 mm) *n*-type 4H-SiC (4° offcut) CS-PVT layer on a 200 mm seed wafer.

down of the growth cell. This strength stems from the opportunity to undertake heat inflow and outflow during the heating up and cooling down steps, thanks to a minimum radial temperature gradient. The latter ensures that SiC crystal bending and cracking is unlikely in CS-PVT. Note, though, that it can be an issue in standard PVT. The upshot of all these factors is that the processing time for producing substrates by CS-PVT is roughly equal to that for PVT, and might be even shorter.

Another benefit that CS-PVT has over its conventional counterpart is a lower growth temperature. Moving from around 2050°C to 1900°C delivers significant energy savings, as well as reducing the degradation rate of the applied graphite parts of the hot-zone.

There's also the possibility of using multiple stacked growth crucibles during a single growth process. This opportunity for trimming costs strengthens the case that switching from PVT to CS-PVT will deliver a cost reduction in SiC substrate production.

Outperforming CVD?

Another opportunity for CS-PVT is to produce the thick intrinsic 4H-SiC drift layers, typically between 100 µm to 500 µm, that could lie at the heart of power electronic devices with blocking voltages above 3 kV.

Today, state-of-the-art intrinsic 4H-SiC layers for SiC power devices are formed by CVD, using growth temperatures of 1600°C to 1700°C and silane and propane precursors. Due to process instabilities, such as unintentional particle downfalls after long growth runs, drift-layer thickness is limited to 30 µm to 50 µm. Switching to CS-PVT removes this barrier, and a potential limiting factor, the purity of the drift layer. To investigate this opportunity, we are extending our exploration of CS-PVT to the epitaxial growth of intrinsic SiC layers, by equipping our new TableTopCS growth machine with a UHV capability.

Our upcoming efforts to exploit CS-PVT technology will also target the growth of SiC pucks in the several-millimetre thickness range, for the fabrication of 4H-SiC wafers; and the deposition of thin layers in the 100-300 µm range, for use in power electronic devices. A third development strategy will focus on the growth of SiC material in the 100 µm to 1 mm thickness range, for novel photonic applications, where special polytypes and dopants will be of interest.

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Basics on (CS-)PVT growth of SiC

THE ESTABLISHED process for the manufacture of SiC boules is PVT – it's basically a sublimation growth process. This technique is adopted because unlike silicon, GaAs and InP, SiC cannot be grown from a melt using a well-known and established method, such as Czochralski, Bridgman or Vertical Gradient Freeze growth.

Development of vapour growth of SiC using the PVT method can be traced back to researchers Yu Tairov and Valeri Tsvetkov. This duo introduced the technique in 1978, in a seminal paper written while they were researchers at the Institute of Electrical Engineering, Leningrad.

The PVT of SiC involves sublimation of source materials, usually SiC powder, at temperatures above 2000°C in a closed crucible, typically dense graphite. Crystallisation follows at the slightly colder interface with the seed (see Figure 1, a sketch of standard 100 mm PVT).

Critical to mass transport from the source to the crystal top of the growth interface is an axial temperature gradient. With the typical 3D-configuration of the growth cell, the high axial temperature gradient that establishes mass transport is accompanied with a radial temperature gradient. The latter is typically a few tenths of a Kelvin per centimetre, a condition supporting high-crystalline-quality via a slightly convex growth interface. If the radial temperature gradient exceeds this condition, strong thermally induced stresses on the crystal can cause cracking during wafering.

With recent increases in crystal diameter from 100 mm to 200 mm, and now reports of 300 mm development, establishment of a small radial gradient is increasingly challenging.

Addressing this issue is CS-PVT, which employs basically the same crystal growth process as standard PVT. However, the flat CS-PVT growth cell design aids the implementation of thermal conditions with small radial temperature gradients. Thanks to this valued asset, CS-PVT promises to become an important technology for large-area SiC wafer production with a high crystalline quality, essential for power electronics and novel photonics.

UV lasers: MBE trumps MOCVD

MBE provides a viable, compelling platform for fabricating low-threshold, electrically pumped mid- and deep-UV lasers

RESEARCHERS from the University of Michigan are claiming to have broken new ground in epitaxy by producing the first edge-emitting lasers operating within the UV-B or UV-C by MBE.

The team's lasers, which slash the threshold current for edge-emitters in this spectral range by more than an order of magnitude, will aid the development of on-chip UV sources for sensing, and could support metrology, water/air purification, disinfection, and quantum and defence-related photonic systems.

The success of the team may surprise many, given that MOCVD is seen as the superior growth technology for producing UVC laser diodes.

Commenting on this, group leader Zetian Mi remarks: "It has been generally believed that MBE, given its relatively low growth temperature, often leads to more defects and therefore limited performance for optoelectronic devices. However, this has changed over the last years, especially with the development of ultra-high-temperature molecular beam epitaxy by our group."

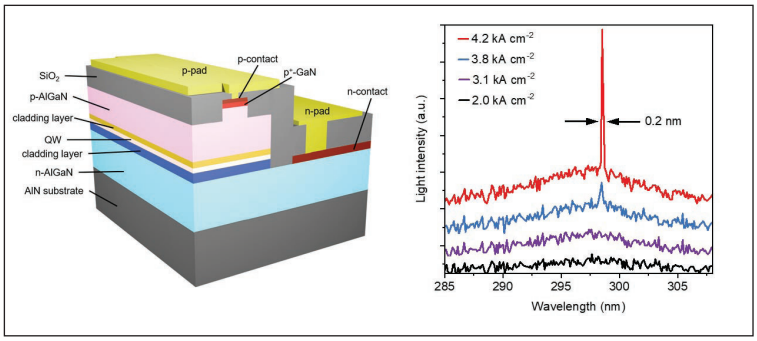
Mi and his co-workers initially used their high-temperature MBE process to produce high-quality AlN and *h*-BN, before turning their attention to AlGaN-based heterostructures for UV lasers.

According to Mi, one of the strengths of MBE for the growth of mid- and deep-UV optoelectronic devices, and in particular laser diodes, is that it proceeds under an ultrahigh high vacuum that can significantly reduce the incorporation of impurities, such as oxygen and carbon – this is a significant concern for high-aluminium-content heterostructures.

In addition, compared to MOCVD, the growth chamber is relatively free of hydrogen, enabling more efficient *p*-type dopant activation; and thanks to precise monolayer control, MBE can realise atomically sharp heterointerfaces, which reduce charge-carrier trapping and enable more-efficient radiative recombination.

Fabrication of the team's devices involved loading chemically cleaned Al-polar single-crystal AlN substrates into an MBE chamber. After thermal treatment of this material at 1000°C, growth of the AlGaN heterostructure followed under metal-rich conditions.

Mi explains that using slightly metal-rich conditions promotes a gallium-adlayer during the growth of AlGaN. "Gallium, having a lower sticking coefficient than aluminium, promotes adatom mobility, thereby resulting in a smoother surface of the epilayers. This adlayer can also be readily removed when necessary, owing to the comparatively higher desorption rate of gallium."



➤ High-temperature MBE growth under ultra-high-vacuum enabled a significant reduction in threshold current for UV lasers.

The team's lasers feature a 3 nm-thick $Al_{0.35}Ga_{0.65}N$ quantum well. It is sandwiched between a pair of 50 nm-thick undoped $Al_{0.45}Ga_{0.55}N$ guide layers, which are bounded by cladding layers. The *n*-type cladding is 300 nm-thick silicon-doped $Al_{0.35}Ga_{0.65}N$, and the *p*-type cladding is a 250 nm-thick magnesium doped layer, compositionally graded from $Al_{0.45}Ga_{0.65}N$ to $Al_{0.85}Ga_{0.15}N$.

Mi and co-workers used standard photolithography, dry and wet etching, and contact metallisation to produce ridge-waveguide lasers with a *p*-electrode width of 2 μm and a length of 600 μm.

Characterisation of the team's lasers, using 1 μs pulses and a duty cycle of 1 percent, determined a peak emission wavelength of 298.5 nm, and a threshold current density of 3.4 kA cm^{-2}. It is argued that this value – far less than that of 40-70 kA cm^{-2}, which is reported for other electrically pumped UV-B laser diodes – can be reduced by supressing non-radiative recombination, cutting internal loss, improving current confinement, and incorporating advanced cavity-engineering strategies, such as optimised distributed Bragg reflectors and index-guided ridge geometries.

Mi says that the plans for the team are to investigate the design, epitaxy, fabrication, and characterisation of AlGaN-based UV-C laser diodes, pushing the operating wavelengths down to 265 nm. "Moreover, we are working to achieve high-output-power mid- and deep- UV laser diodes for more practical applications."

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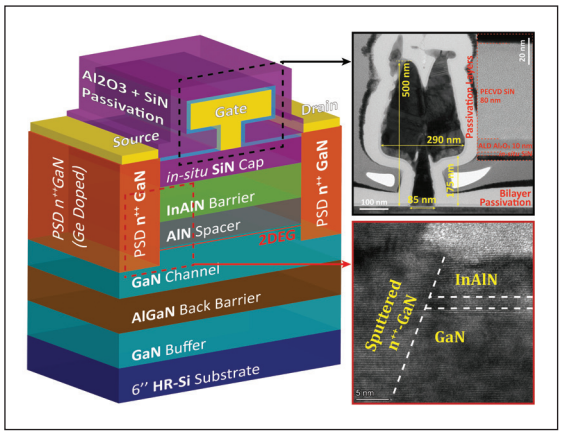
Sputtering superior ohmic contacts

Radical-enhanced reactive sputtering produces low-resistance ohmic contacts for GaN HEMTs

A COLLABORATION between researchers in Singapore and Japan has developed a sputtering technology for ohmic contacts that aids the performance of GaN HEMTs. The team argues that its approach, an attractive alternative to producing ohmic GaN contacts by MOCVD and MBE, improves the prospects for GaN HEMTs in mobile applications.

If GaN HEMTs are to be deployed in handsets and mobile infrastructure, they need to operate at around 3.3 V and 8-12 V, respectively. For these voltages, a low ohmic contact resistance is essential.

Realising this requirement is the collaboration's sputtering technology, developed by researchers from: Nanyang Technical University, Singapore; Singapore's National Semiconductor Translation and Innovation Centre for Gallium Nitride; and Nagoya University, Japan.



➤ InAlN/GaN HEMTs with a T-shaped gate and sputtered regrown *n*-type contacts, imaged with a scanning electron microscope.

One of the strengths of sputtering is its lower growth temperature, according to corresponding author Geok Ing Ng, who holds positions at both Nanyang Technical University and the National Semiconductor Translation and Innovation Centre for Gallium Nitride.

According to Ng, at around 600°C, and possibly at even lower temperatures, sputtering produces *n*-GaN with reasonable crystalline quality. In comparison, producing *n*-doped GaN by MBE and MOCVD requires growth temperatures of typically around 750°C and beyond 900°C, respectively. "Such high temperatures typically necessitate the use of an ohmic-first process, which limits process flexibility."

Another advantage of sputtering is its widespread tool availability. Today's CMOS foundries tend to have sputtering tools, but not those for growth by MBE and MOCVD. "These sputtering tools, though configured for the CMOS process, could be readily modified to support GaN sputtering," says Ng.

The team are not the first to consider sputtering *n*-type GaN, with previous efforts forming highly doped *n*-GaN ohmic contacts on GaN HEMT heterostructures

"To the best of our knowledge, this work is the first report of ohmic contact to an InAlN/GaN heterostructure, which is a strong contender for high-frequency, low-voltage GaN HEMTs," says Ng.

According to him, another breakthrough is the successful integration of sputtered ohmic contacts for scaled gate length GaN HEMTs.

Critical to success, says Ng, is ensuring a good fill of sputtered GaN, and high-quality patterning in the closely spaced source-drain regions. Engineers also had to make sure they did not damage the SiN cap, which is just 2 nm-thick.

Fabrication of the HEMTs began by loading high-resistivity silicon substrates into an MOCVD chamber and adding a carbon-doped GaN buffer, a 250 nm-thick AlGaN back barrier, an 80 nm-thick GaN channel, a 2 nm-thick AlN spacer, a 7 nm-thick InAlN barrier and a SiN cap. From this epiwafer the team produced GaN HEMTs with a source-to-drain distance of 2.5 μm and a gate length of 85 nm. To form the ohmic contact, reactive ion etching recessed this region by 50 nm, before a radical-enhanced reactive sputtering systems added 80 nm-thick germanium-doped GaN at 600°C, at a rate of 6.3 nm min^{-1}. The sputtered GaN is initially crystalline, and then polycrystalline, with the latter removed with a TMAH etch.

Characterisation determined an interfacial resistance between the *n*-type GaN and the two-dimensional electron gas of 0.06 Ω mm and an on-resistance of 0.91 Ω mm.

The HEMT produces a maximum drain current of 2.03 A mm^{-1}, and output powers at 28 GHz of 0.51 W mm^{-1}, 1.25 W mm^{-1} and 2.44 W mm^{-1}, at drain-source voltages of 3 V, 5 V and 8 V, respectively.

One of the next goals for the team is to see if they can obtain a lower contact resistance. "Secondly, we plan to implement sputtered GaN ohmic contacts in our improved low-voltage transistors with aggressive scaling, to explore the performance limits of these transistors," says Ng.

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Record forward-current for AlGaN Schottky barrier diodes

Distributed polarisation doping produces record forward currents in quasi-vertical AlGaN Schottky barrier diodes

ENGINEERS from the University of South Carolina are claiming to have broken the record for the forward current in Schottky barrier diodes based on high aluminium-content AlGaN material systems.

These quasi-vertical diodes, featuring distributed polarisation doping, deliver current densities of more than 8 kA cm^{-2} and 14 kA cm^{-2} under forward biases of 10 V and 15 V, respectively.

A key feature of the team's AlGaN diodes is their foundation, a bulk AlN substrate. This platform, lattice-matched to the diode material, offers excellent thermoconductance. "But bulk AlN crystal is a dielectric," explains corresponding author Tariq Jamil. "Making it highly conducting is a very challenging problem."

Due to this limitation, Jamil and co-workers do not try to produce vertical Schottky barriers diodes, as their fabrication is far from easy – for example, it would require the use of complex processing to etch vias in the substrate that reach the anode layer.

Jamil argues that one of the merits of aluminium-rich AlGaN quasi-vertical devices is that they can be fabricated over any substrate supporting the growth of high aluminium-content material. "In addition, quasi-vertical devices fabricated over insulating substrates allow for simple integration with many other electronic and/or optoelectronic devices."

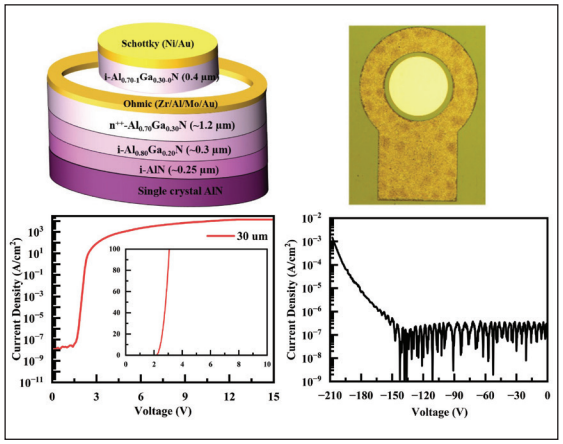
According to the team, they are the first to use distributed polarisation doping to produce an *n*-type region in quasi-vertical AlGaN Schottky barrier diodes. Note, though, that this form of doping is not new, having been proposed as far back as 2002. Since then, it's been applied to laser diodes and LEDs emitting in the UV, and to FETs and *p-n* diodes.

Fabrication of the quasi-vertical diodes began by loading a chemically cleaned bulk AlN substrate into an MOCVD reactor and, after annealing under ammonia, growing an epitaxial stack comprising a 0.25 μm-thick AlN buffer, a 0.3 μm-thick undoped layer of $Al_{0.8}Ga_{0.2}N$, a 1.2 μm-thick $Al_{0.7}Ga_{0.3}N$ heavily silicon-doped layer, and a 400 nm-thick *n*-type distributed polarisation doped layer. For the latter, aluminium content is graded from 0.7 to 1.0.

Off-axis (1012) spectra obtained by X-ray diffraction have peaks with a full width at half-maximum of around 126 arcsec for the heavily doped $Al_{0.7}Ga_{0.3}N$ layer and 70 arcsec for the AlN layer. These values indicate that the heterostructure is almost pseudomorphic.

To validate polarisation doping within the device, the team produced a similar structure, omitting the 1.2 μm-thick $Al_{0.7}Ga_{0.3}N$ heavily silicon-doped layer. Doping measurements with a mercury-probe capacitance-voltage system revealed that despite any external doping, average donor density in the distributed polarisation-doped layer is around 8.5 x 10^{17} cm^{-3}.

Jamil and co-workers fabricated Schottky barrier diodes with standard circular mesa geometry featuring an *n*-type Zr/Al/Mo/Au contact and a Ni/Au Schottky contact. Both contacts were formed by electron-beam evaporation.



➤ Engineers at the University of South Carolina have fabricated quasi-vertical Schottky barrier diodes and that deliver record forward currents. Reverse breakdown characteristics of a 30 μm-diameter diode are also provided.

Electrical measurements determined that under a 15 V forward bias, current density is 14 kA cm^{-2}, and effective current density – that's the diode area where the current actually flows – is 36 kA cm^{-2}. Reverse breakdown voltage, realised without passivation and field plates, is 210 V.

One of the team's next goals is to fabricate more advanced devices, such as multi-finger geometry devices, that ensure more uniform current spreading and ultimately enable an increase in total current capability. Another aim is to achieve the highest possible reverse voltage.

"Both high forward currents and high reverse voltages are essential for applications of these diodes in power electronics," says Jamil.

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