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FAST FEEDBACK AIDS PRODUCTION

A novel wafer-scale process aids VCSEL manufacture by providing rapid device feedback

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VIEWPOINT

BY DR RICHARD STEVENSON, EDITOR

The VCSEL's various directions

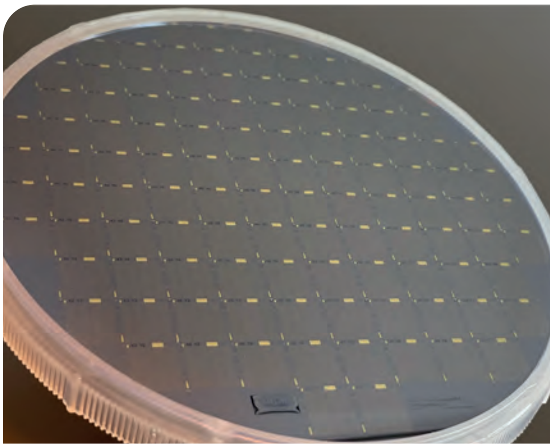
FOR VERY GOOD REASON, there's currently a great deal of interest in the VCSEL. It's on an upward trajectory: it has established itself as the key source for data communication and face-recognition systems; and it is a very promising candidate for deployment in lidar, and a range of quantum technologies, including atomic clocks and quantum gyroscopes.

In academia and industry much effort is being devoted to ensuring that the VCSEL grabs its opportunities to increase volumes and reach new applications. Work is underway to explore the capabilities of MBE for the growth of longer-wavelength VCSELs, to support manufacturing with rapid device feedback, and to introduce new architectures with superior capabilities.

The conventional VCSEL emits just inside the infrared, using emission from quantum wells made from GaAs or InGaAs. While replacing these III-Vs with a dilute nitride is a challenge, doing so shifts the wavelength further into the infrared to a domain that's eye-safe, opening the door to higher powers. Producing such a device by MOCVD is challenging, so it makes sense to switch to MBE, argues Riber (see p. 20).

In today's fabs that produce VCSELs, insights into the quality of the epiwafers are provided by a variety of tools, including those that measure optical properties, such as the reflectance profile of the mirrors. However, it's not possible to gain rapid feedback into the most valuable characteristics of all, such as the emission wavelength, the threshold current and the power-conversion efficiency.

However, a team from Cardiff University and IQE is working to right that wrong, developing a simplified strip-backed process that could fabricate a VCSEL for testing purposes within 24 hours (see p. 44). Time is saved by modifying the etching process, so that some portions are left untouched and subsequently used for electrical connections. As well as providing fast feedback, these simplified VCSELs unveil variations in oxidation, which is a key process for defining the size of the aperture of these lasers.



One of the downsides of optical sources based on the VCSEL is the complexity of the package. In addition to the chip, there's accompanying optics to transform the beam, plus connections and driver electronics that ensure eye-safety requirements are met.

At Trumpf they have developed a new generation of VCSEL that addresses this bulkiness while improving performance (see p. 30). The breakthrough comes from introducing a new device architecture: light is emitted through the substrate, and micro-optics is added to the chip by etching lenses in the III-V. The latter eliminates the need to align optics, while the higher refractive index associated with a III-V lens gives new freedom to the design.

Clearly, VCSEL design is continuing to evolve, along with technologies to support its production, ensuring that this device has a very bright future to look forward to.

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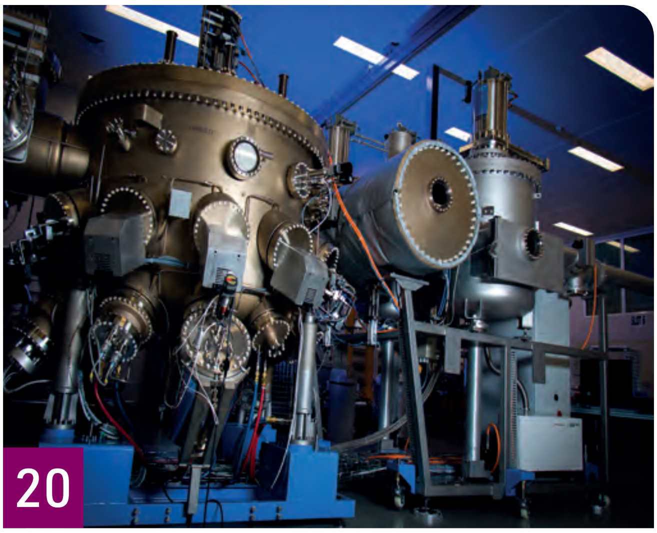

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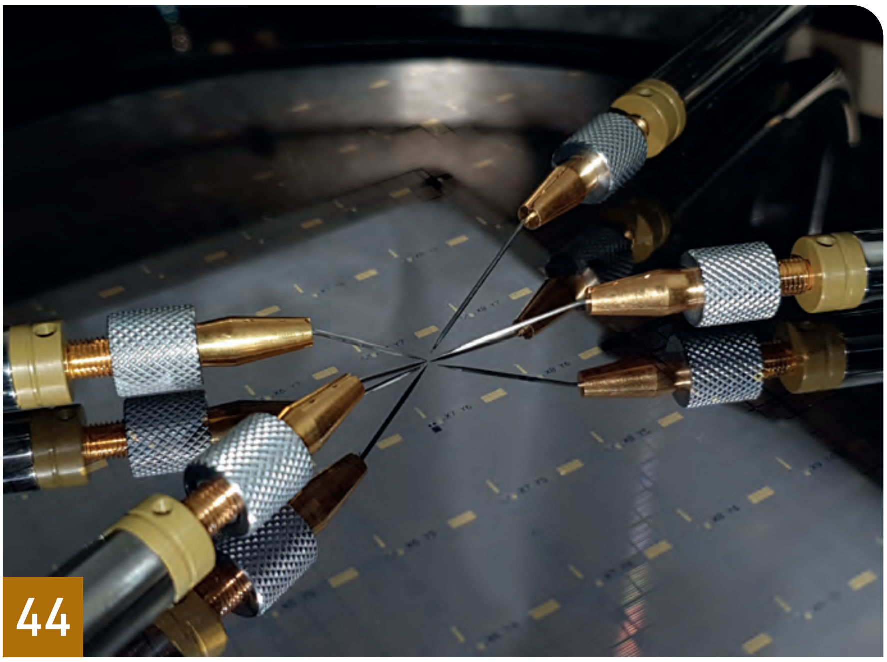

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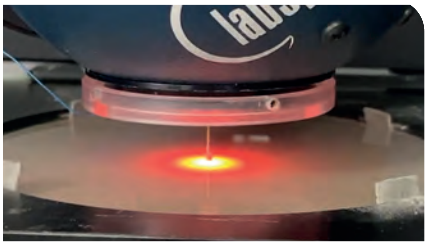

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Qorvo awarded DoD Advanced RF GaN programme

QORVO, a provider of RF solutions, has been selected by the US Department of Defense (DoD) to proceed with the *Advanced Integration Interconnection and Fabrication Growth for Domestic State of the Art* (SOTA) *Radio Frequency GaN* programme, also known as STARRY NITE, as part of the Office of Undersecretary of Defense Research & Engineering's microelectronics roadmap.

The STARRY NITE programme seeks to develop and mature domestic, open SOTA RF GaN foundries in alignment with the DoD advanced packaging ecosystem.

The Qorvo team will leverage over 30 years of technology development and a long record of successfully establishing high-performance, reliable GaN manufacturing technology to achieve several goals.

They are to offer secure, domestic high-volume manufacturing with 90 nm GaN foundry processes, along with advanced interconnect features that enable high performing, innovative, and compact solutions for next-generation military and commercial wireless communications systems.

Qorvo says that it is well-positioned to realize STARRY NITE's vision and ensure accessibility of 90 nm RF GaN and 90 nm GaN with advanced interconnects across the Defense Industrial Base (DIB), delivering manufacturing maturity with performance and advanced integration features such as copper bumps.

Philip Chesley, president of Qorvo's Infrastructure and Defense Products, said, "Qorvo looks forward to providing best-in-class advanced GaN technology that will enable high-performing, reliable and compact RF solutions for future needs through the STARRY NITE prototype project."

Qorvo is a leader in providing 5G and other commercial products that require a keen understanding of today's market requirements, as well as the advanced GaN nodes and advanced interconnects needed to support/achieve those requirements.

A commercial provider for dual-use applications, Qorvo claims to be is uniquely positioned to leverage wafer volumes to drive manufacturing process control, accelerate process and reliability maturation, and drive down costs for the entire DIB.

BluGlass ships first prototype products

AUSTRALIAN semiconductor developer BluGlass has shipped its first fully packaged laser diode prototypes to its initial customer.

BluGlass' 405 nm and 420 nm alpha products will be integrated and tested by the customer within their new product design and development cycles. An alpha product is an advanced prototype still in the design phase and is a valuable tool to collect customer feedback in real-world applications. These alpha products have undergone internal preliminary performance and life-time reliability testing and are at a stage where customers can assess the products in their own development-stage applications. The company's 405 nm and 420 nm single-mode and multi-mode products are progressing towards achieving commercial performance and reliability.

Jim Haden, BluGlass president, said: "This is a key commercialisation milestone for BluGlass, representing the first delivery of our laser diodes to an external customer. While still in the alpha (development) stage, our laser products are demonstrating significantly improved performance, and now are suitable for customers to evaluate during their product and application development process."

Haden added: "We are working with several customers wanting to trial alpha laser diodes for innovative new applications, including medical devices, sensing, quantum computing, and automotive products. The fact that we have customers anxious to receive our alpha products, ahead of our full product launch, is indicative of the significant unmet demand within the 405 nm and 420 nm wavelengths, and a testament of our improved performance."

Sony establishes space communications business

SONY has formed a new company, Sony Space Communications Corporation, to conduct space optical communications.

"Currently there are approximately 12,000 satellites in space, and the number is expected to increase in the future. The amount of data used in orbit is also increasing year by year, but the amount of available radio waves is limited," said Kyohei Iwamoto, president, Sony Space Communications Corporation.

"Low Earth orbit (LEO) satellites need to communicate with the ground, so a large number of communications facilities are required for real-time communications, which is problematic because these satellites must pass directly over a ground station to communicate with it. Additionally, the need for frequency licenses for radio waves and the requirement for lower power consumption of communication equipment needed by smaller satellites, like micro-satellites, are also issues to be addressed."

To solve these problems, SSC plans to develop small optical communications devices to provide related services to connect micro-satellites in LEO via laser beams. It says it will apply the optical disc technology it has developed for CD players and other products.

Sony has already worked with the Japan Aerospace Exploration Agency (JAXA) on space comms projects.

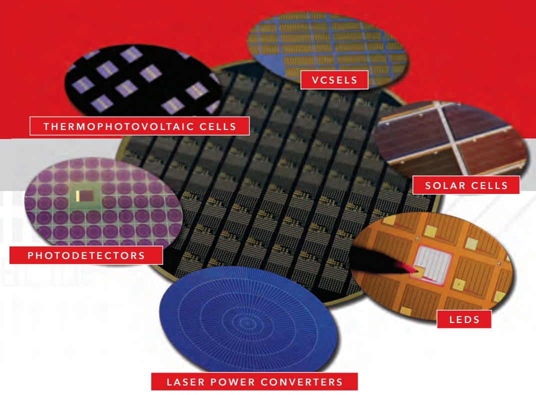
In 2020, the SOLISS (Small Optical Link for International Space Station) was installed in the Japanese Experiment Module Kibo of the International Space Station. It established a bidirectional laser communications link with a space optical communication ground station of the Japanese National Institute of Information and Communications Technology, and successfully transmitted high-definition image data via Ethernet protocols. This experiment used Sony Computer Science Lab's forward error correction – a laser-reading technique derived from Sony's Blu-ray optical disk technology. (Blu-ray technology uses a GaInN-based blue-violet laser emitting at a wavelength of 405 nm).

In 2021, the SOLISS experimental device successfully established optical downlinks from space to a commercial optical ground station of Kongsberg Satellite Services in Greece. In 2022, in collaboration with JAXA, an experiment on complete data file transfer in a simulated error-prone communications environment, which will be the technological basis for internet services through stratospheric and low-Earth orbit optical communications, was successfully conducted.

By using optical communications, SSC aims to realise high-speed communications with small devices, which are physically difficult to achieve with conventional radio communications because conventional communications require large antenna and high power output.

In addition, by constructing an optical communications network not only between satellites and the ground, but also between satellites in orbit, SSC aims to enable real-time communications from anywhere on the ground to any satellite in space.

By providing easy-to-use inter-satellite communications capabilities, SSC aims to increase the amount of communications in space and realise an internet communications network covering the earth, space, and applications such as real-time services.



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Taiwan Semiconductor Research Institute picks Veeco tool

VEECO INSTRUMENTS announced that the Taiwan Semiconductor Research Institute, National Applied Research Laboratories (TSRI, Narlabs) has selected Veeco's Propel R&D MOCVD System for advanced development and collaboration related to GaN-based power and RF devices.

According to Veeco, the single-wafer Propel platform is ideal for high-volume manufacturing and 300 mm capabilities, as well as R&D applications.

This Propel R&D system has been installed in TSRI's Hsinchu, Taiwan laboratory. It enables a joint collaborative effort to drive technology innovations, as well as develop and demonstrate technical capabilities in the emerging GaN markets.

The joint effort and collaboration aims to accelerate wide-bandgap compound semiconductor technology to high volume and low-cost applications on 200 mm and 300 mm substrates.

"Veeco's Propel R&D System is uniquely qualified to deliver the performance and flexibility required to conduct advanced development of power and RF devices," commented Chang-Hong Shen, deputy director-general, research fellow at TSRI. "We are excited to have this R&D system operating in our facility and look forward to support from the Veeco team in the years to come."

Veeco's Propel GaN MOCVD system is designed specifically for power and RF applications. Featuring a single-wafer reactor platform, the system deposits high-quality GaN films for the production of highly efficient power and RF devices.

The single-wafer reactor is based on Veeco's TurboDisc technology, including the IsoFlange and SymmHeat breakthrough technologies, which provide homogeneous laminar flow and a uniform temperature profile across the entire wafer.

"We are pleased to have our MOCVD system selected by TSRI to help develop their advanced power and RF applications," said Adrian Devasahayam, SVP, product line management. "We now have multiple technologies installed at TSRI's facility and we look forward to helping them maximise the value of our platforms and the opportunity for technology collaboration."

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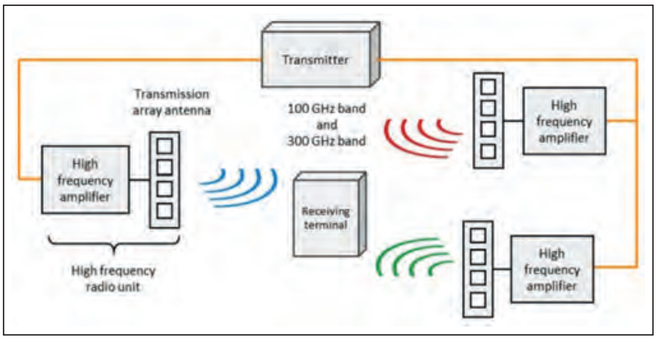
Fujitsu, NTT DOCOMO and NTT start joint 6G trials

FUJITSU will start working with NTT DOCOMO and Nippon Telegraph and Telephone Corporation (NTT) to conduct joint trials towards the realisation of practical applications for 6G.

In the joint trials, the partners will use sub-terahertz waves of 100 GHz and 300 GHz, which represent promising candidates for use in 6G . The companies further aim to develop a high-frequency wireless device based on compound semiconductor technology.

Bands of 100 GHz and above would enable communication speeds of over 100 Gbit/s, which is ten times higher than that of current 5G networks. However, radio waves at higher frequencies tend to be more easily affected by obstacles, which makes communication between distant points difficult. To address this issue, Fujitsu, DOCOMO and NTT will use distributed MIMO, a wireless communication technology where multiple sub-terahertz-wave antennas are dispersed to simultaneously emit radio waves from multiple directions to a receiving terminal.

In order to realise high-speed and large-capacity communications in the sub-terahertz domain with small size components and low power consumption, Fujitsu aims to develop high-frequency wireless devices utilising compound semiconductors, such as GaN and InP. Moving forward, Fujitsu will promote the development of technologies for the realisation of practical applications for 6G and actively engage in global 6G standardisation activities to contribute to solving societal issues through R&D.



Naoki Tani, executive VP and CTO at DOCOMO, comments: “DOCOMO has been collaborating with Fujitsu since 2014 to verify wireless technologies towards the realisation of 5G, and has leveraged the obtained know-how to provide 5G commercial services since 2020. We are delighted to collaborate with Fujitsu also towards the realisation of the 6G concept.

“DOCOMO and NTT will initiate experimental trials with Fujitsu to establish 6G wireless technologies for sub-terahertz communication using 100 GHz and 300 GHz band, and make a solid contribution to 6G commercialisation with a variety of industry partners.”

Power GaN: the next wave ...

Yole forecasts that the power GaN market will reach $2 billion in 2027. In its latest annual report, *Power GaN 2022*, Yole details the penetration of GaN devices in different applications from the system point of view.

The consumer power supply market will be worth more than $915 million by 2027, with a 52 percent CAGR between 2021 and 2027. Yole forecasts an increase in the mid term of GaN penetration in datacom/telecom as regulations become stricter. The interest in adopting 48 V-point-of-load systems in data centres to reduce power consumption and cabling volume will favour GaN for low-voltage applications.

An increasing number of power suppliers are adopting GaN in their systems. Transphorm, EPC, Texas Instruments, Infineon, and GaN Systems have all announced several design wins. Due to this, the GaN market for datacom/telecom is expected to have a 69 percent CAGR over the forecast period, to more than $617.8 million in 2027. At a lower penetration level, automotive DC-DC converters and OBCs will be part of the next wave of growth during the forecast period.

There are ever more collaborations between GaN device players, who are accelerating the automotive qualification of their products, and the Tier-1 and OEMs, who are evaluating automotive GaN solutions. The GaN automotive market is expected to exceed $227 million by 2027, with a 99 percent CAGR between 2021 and 2027.

In its *Power GaN 2022* report, Yole's analysts also highlight the dynamic supply chain with new entrants and significant investments. Indeed, since the release of the 2021 report, the market research & strategy consulting company has witnessed the entry of new players into the supply chain. Notably, Rohm is offering a 150 V GaN product for telecom/datacom applications. BelGaN, a new GaN foundry based in Belgium, has recently acquired Onsemi's fab. And on the fundraising front, Navitas went public through a SPAC business combination after an agreement valued at $1.04 billion with Live Oak Acquisition Corp.

Focusing on the Chinese ecosystem, the government has supported more investments from GaN players. Innoscience, for instance, is investing more than $400 million to expand its 8-inch wafer capacity from 10k to 70k wafers per month by 2025.

A domestic supply chain for GaN power is well developed in China, especially for the consumer market. The transition to the 8-inch platform and the consolidation of the supply chain with more players at each level are driving lower manufacturing costs, especially at the epitaxy step, which constitutes the most significant part of a GaN device's cost structure.

MIT Innovators boost millimetre-wave linearity

FINWAVE SEMICONDUCTOR (previously known as Cambridge Electronics), has announced its aim to revolutionise the future of 5G communications with next-generation 3D GaN technology.

"Today's 5G millimeter-wave networks are severely constrained by the inefficient performance of power amplifiers," commented Joe Madden, chief analyst at Mobile Experts. "RF-SOI and CMOS technologies are used today instead of GaN because of the need to integrate logic circuits with the RF front end, but this brings significant tradeoffs in power consumption and heat dissipation. High-performance GaN-on-silicon brings a new option to the table that could make 5G millimeter wave more practical."

With ten times higher breakdown electric field than silicon, high electron mobility and the ability to operate at a higher junction temperature, GaN semiconductors are poised to play a significant role for the next decade's technology revolutions. At millimetre-wave frequencies, GaN-on-silicon amplifiers excel versus alternative solutions such as silicon CMOS, GaAs pHEMTs or SiGe devices.

Finwave co-founders Tomas Palacios and Bin Lu first teamed-up at MIT to invent several of the foundational technologies for Finwave, including a novel type of GaN transistor based on a FinFET architecture. After being spun out of MIT, the company spent several years developing the technology further for manufacturing in the standard silicon CMOS fabs. By 2020, Finwave demonstrated the first GaN FinFETs fabricated with 8-inch silicon CMOS tools.

"As GaN continues to gain market share from silicon, first in 4G high-power macro base-stations, then in fast chargers for mobile phones and laptops, we are convinced that the next biggest opportunity for GaN-on-silicon will be 5G infrastructure and handset applications," said Lu. "With our unique 3DGaN technology, proprietary 8-inch CMOS-compatible manufacturing process and world-class expertise, our team at Finwave is poised to move entire industries forward and become the leading enabler of the 5G market."

Finwave's award-winning 3DGaN technology is said to significantly improve linearity, output power and efficiency in 5G millimetre-wave systems – while greatly reducing costs for carriers. By leveraging high-volume 8-inch silicon CMOS, Finwave's devices benefit from both the cost model and scalability of silicon technology.

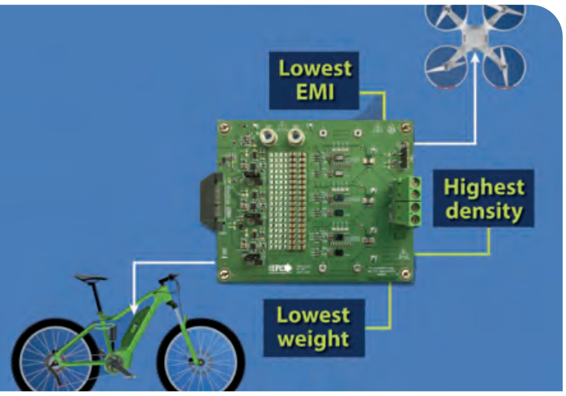
"The combination of the outstanding electrostatic control and linearity of the GaN FinFET structure, with the cost model of silicon, and the scaling ability of state-of-the-art 8-inch and, in the future, 12-inch fabs, makes 3DGaN a true game changer," commented Palacios.

EPC GaN ICs shrink motor drives for ebikes and drones

EPC ANNOUNCES the availability of the EPC9173, a 3-phase BLDC motor drive inverter using the EPC23101 eGaN IC with embedded gate driver function and a floating power GaN FET with 3.3 mΩ $R_{DS(on)}$.

The EPC9173 operates from an input supply voltage between 20 V and 85 V and can deliver up to 50 A peak (35 A_{RMS}). This voltage range and power level makes the solution suitable for a variety of motor drive applications, including e-bikes, scooters, city cars, drones and robotics.

The EPC9173 contains all the necessary critical function circuits to support a complete motor drive inverter including gate drivers, regulated auxiliary power rails for housekeeping supplies, voltage, and temperature sense, accurate current sense, and protection functions.



Major benefits of a GaN-based motor drive are exhibited with these reference design boards, including less than 30 ns deadtime for very high motor and inverter system efficiency for longer range, lower distortion for lower acoustic noise, lower current ripple for reduced magnetic loss, lower torque ripple for improved precision, and lower filtering for lower cost.

The lower weight and size of the EPC9173 solution enables incorporation of the drive into the motor housing and supports low inductance, higher power density motors. When configured for 100 kHz frequency, the input filter and the number of capacitors can be dramatically reduced, and the electrolytic capacitors can be eliminated from the board. The use of the EPC23101 integrated GaN-on-silicon device offers higher performance in a smaller footprint with significantly reduced design engineering requirements for fast time to market. The solution enables phase current sensing and leg shunt current sensing, for maximum flexibility. EPC provides full demonstration kits, which include interface boards that connect the inverter board to the controller board development tool for fast prototyping that reduce design cycle times.

The EPC9173 boards measure 130 mm x 100 mm (including connector). The boards can also be configured for multiphase DC–DC conversion topologies including buck, boost, half bridge, full bridge, or LLC converters.

"Designers can use the GaN IC to make lighter weight and more precise battery-operated motor drives for eMotion, robotic arms, and drones", said Alex Lidow, CEO of EPC. "GaN enables motor systems that are smaller, lighter, less noisy, have more torque, more range, and greater precision."

The EPC9173 reference design board is priced at $900 and is available for immediate delivery from Digi-Key. EPC says that designers interested in replacing their silicon MOSFETs with a GaN solution can use the EPC GaN Power Bench's cross-reference tool to find a suggested replacement based on their unique operating conditions.

Vitesco and Infineon cooperate on SiC

Vitesco Technologies, a supplier of drive technologies and electrification solutions, has signed a cooperation agreement with Infineon Technologies.

"Partnering-up with leading semiconductor manufacturers is important for us to master dynamic growth," said Andreas Wolf, CEO of Vitesco Technologies.

Wolf added: "We have been collaborating with Infineon on silicon for a long time. We are now expanding this with SiC power semiconductors. Jointly refining chips specifically for our applications, in the area of electromobility, will lead to highly attractive solutions."

"In SiC, Infineon is a technological and quality leader," said Stephan Zizala, head of the Automotive High Power business unit at Infineon Technologies.

"Our second SiC generation enables us to develop even more compact and efficient systems. With our decades of experience and continuous expansion of manufacturing capacities, we are well positioned for the accelerated growth of the SiC market."

"Range is a key performance characteristic in battery electric driving, higher efficiency power semiconductors such as SiC will therefore be increasingly used in the future," highlighted Thomas Stierle, member of

the executive board and head of the Electrification Technology business unit at Vitesco.

For Vitesco, this is the second partnership in SiC devices. "We have had excellent experience with the partnership already underway and have industrialized initial applications," said Stierle.

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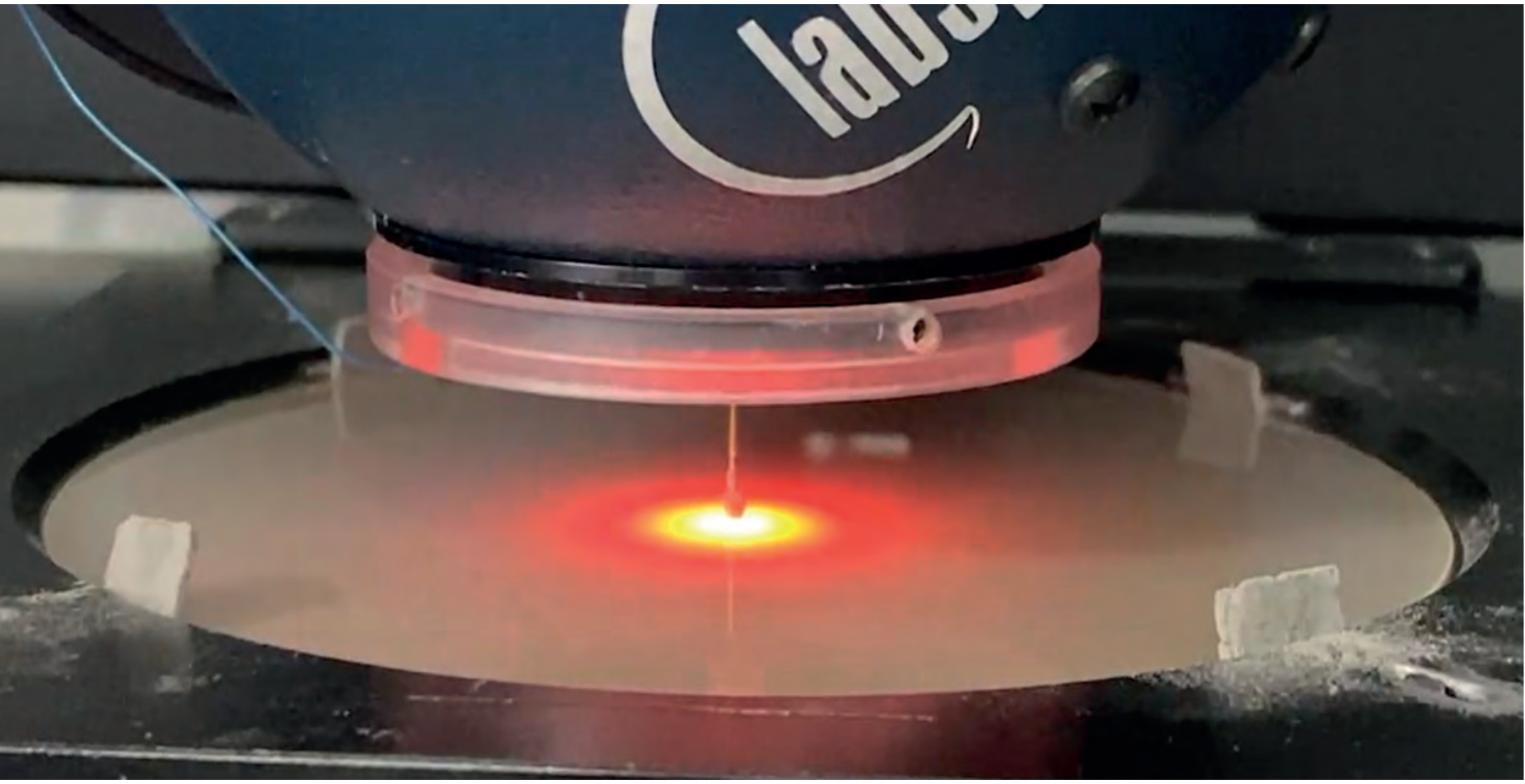


Red light success from Soft-Epi

As tech giants race to get AR headsets to market, all eyes are on a handful of companies striving to deliver reliable, bright red microLEDs. Soft-Epi is about to join the very few that think they can, reports REBECCA POOL

WHILE Soft-Epi of South Korea has been developing GaN-on-sapphire epi-wafers for blue and green LEDs for many years, late last year, company researchers discovered they could also get their GaN materials to emit red light. As James Kimoon Lee, VP of sales and marketing at Soft-Epi, tells *Compound Semiconductor*: "At the time, we just didn't know it was possible for us to do this, but our research and development engineers suddenly realised they could… Efficiency levels were good in terms of brightness, and we've been developing GaN red epi-wafers for microLEDs ever since."

The company's early sapphire-based red GaN epi-wafers had a wall plug efficiency of around 1 percent, but more recently this figure has been stretched to just over 2 percent, equivalent to 2.3 percent external quantum efficiency (EQE). So far, wall efficiency figures for red GaN-based devices have mostly hovered around 2 percent. In contrast, wall plug efficiency figures for blue and green LEDs can exceed 50 percent.

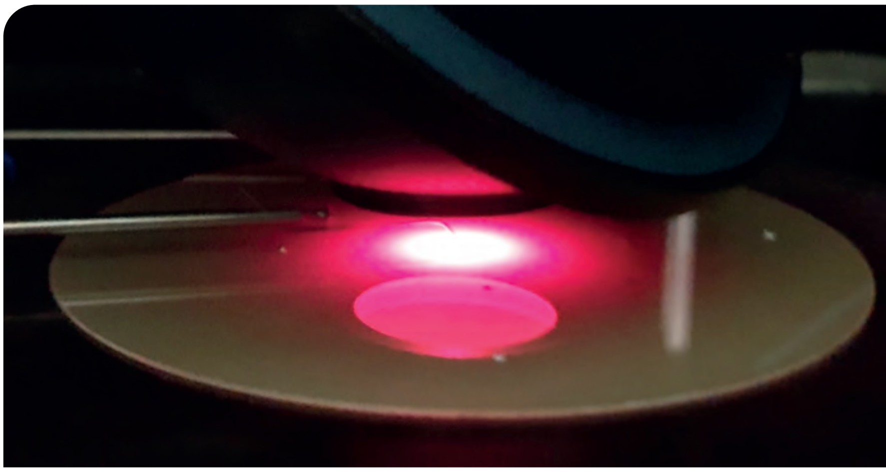
Given this, Soft-Epi researchers are currently experimenting with doping levels, new dopants and MOCVD conditions to boost their GaN red epi-wafer efficiencies. "Our work looks very promising, and by the end of this year we want to reach a figure of 3 percent," he says. "Looking at results so far, we thought now is a good time to ship our red GaN epi-wafers to those that need it."

The problem with red

While red LEDs have been successfully manufactured using AlInGaP-based materials, the same cannot be truly said for the diminutive micro-versions. High surface recombination velocities in the material lead to efficiencies plummeting as chip size decreases – researchers can address the issue with sidewall passivation, but only with partial success.

What's more, AlGaInP-based microLEDs suffer from poor thermal stability at a high temperature. Thanks to carrier leakage over the small barrier heights, efficiency droop kicks in as temperatures rise.

Given these problems, microLED manufacturers are ready for a user-friendly alternative to AlGaInP. Industry players have been experimenting



GaN red epi-wafers from Soft-Epi.

with various methods to achieve red emission, including colour conversion via nanophosphors or quantum dots, but developing native red-emitting InGaN substrates looks set to provide a more straightforward answer, compatible with existing production lines.

For example, in 2018, Soitec of France revealed InGaN substrates that could emit red light while a year later, UK-based Plessey claimed a world first with its InGaN-on-silicon-based microLEDs. Then in November 2021, Porotech, also of the UK, unveiled its red microLED display based on InGaN materials. And doing it differently, Aledia, France, has fabricated GaN nanowire microLED chips on 12-inch silicon wafers.

A flurry of other companies and research institutions have made similar microLED announcements. But as Lee points out, those touting red microLED success tend to have exclusive contracts with the likes of Meta and Google, eager to snap up the technology for AR/VR applications, wearable watches and more.

"This means [other] microLED developers are having difficulties in their R&D because they cannot get red GaN epi elsewhere," he says. "We see this as a good chance for us to inform industry on the development of red GaN, and of course, let them know what our company has done so far."

To date, Soft-Epi has been largely depositing its GaN-based red epilayers onto 4-inch and 6-inch polished and patterned sapphire substrates, but Lee is clear that the company can grow layers on SiC and silicon wafers. "In the future, we believe that GaN on silicon epiwafers are going to be very important, so we've been working on this," he says. "We're in talks with a partner that is making VR/AR technology, to pursue red GaN-on-silicon wafer development with them."

Still, it's no secret that growing GaN and InGaN layers is difficult. The large lattice mismatch and piezo-electric field between InGaN active layers and GaN layers leads to many defects and a wavelength shift within the InGaN quantum wells, which deplete a device's performance.

Lee and colleagues at Soft-Epi don't appear particularly fazed by these issues, but remain tight-lipped on how they have tackled them. "Controlling indium is key, and we can do this very precisely," says Lee. "It's very important to minimize stresses [in these layers]."

So, what now for Soft-Epi and its GaN-based red epiwafers? The company hopes to provide its technology to any company developing and manufacturing microLEDs, and is sending 4-inch and 6-inch epiwafers to customers worldwide.

NDA agreements have been signed all round. But as Lee hints: "All our customers are very advanced in the LED industry, and we've also shipped our GaN red LED epiwafers to a major South Korean customer."

Soft-Epi has also been developing monolithic RGB epiwafers, and intends to introduce these by the end of the year. Pointing to the California-based microLED start-up, Raxium, recently snapped up by Google, Lee says: "I think we have a technology that is as good, and Google is now investing huge sums of money in them."

"Every company is doing this its own way, and I hope a direct native GaN method for red, like ours, will be the champion," he adds.

The Soft-Epi team with James Kimoon Lee, VP of sales and marketing,far left.

Moving away from silicon's cast-offs

Instead of purchasing secondhand equipment from the silicon industry, new compound semiconductor lines are investing in partnerships and dedicated toolsets that will advance their capabilities

BY JOE GAUSTAD FROM CLASSONE TECHNOLOGY

WHAT DO YOU THINK is behind the current silicon chip shortage? Do you believe it is increased demand for PCs, driven by Covid-19? Or do you cite fab labour disruptions, the neon gas shortage from the war in Ukraine, the palladium shortage from banned Russian exports, or the exponential growth of IoT products?

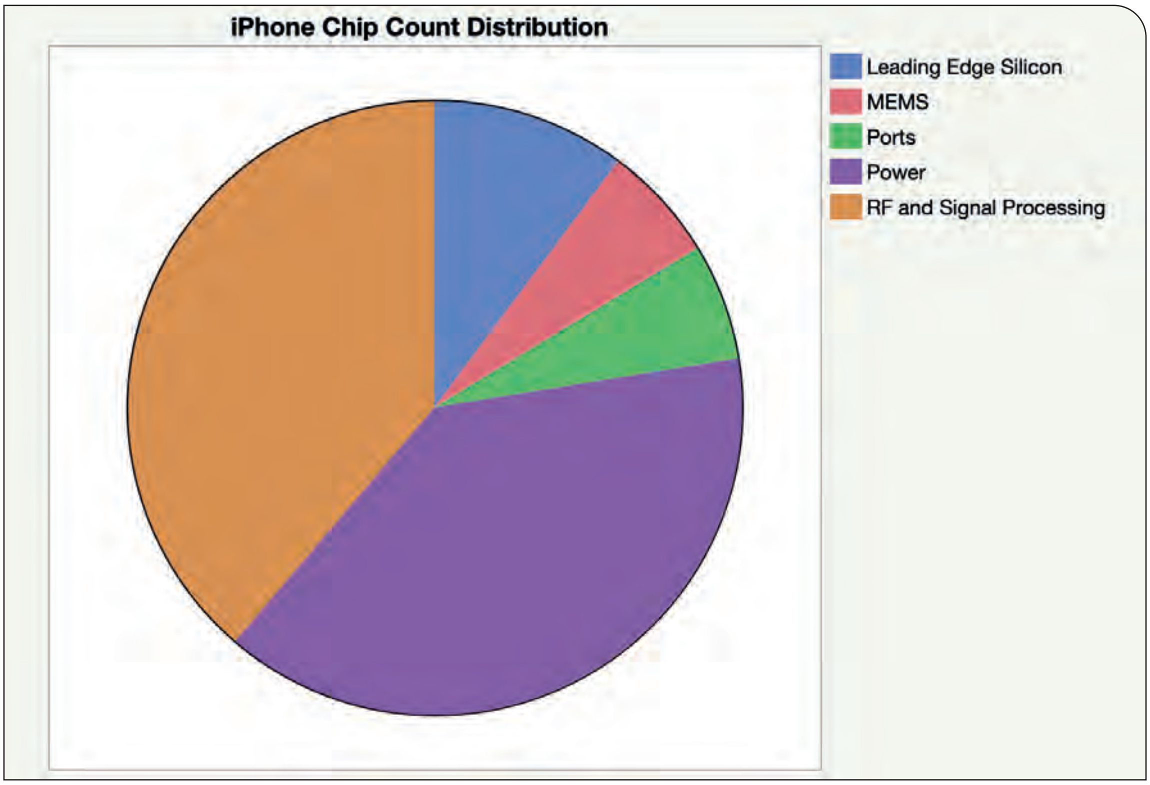
Those who have given much thought to the cause of the current chip shortage argue that it's not one factor, but a combination of them, which may influence one another. Simply blaming Covid does not stack up. While this has helped to accelerate the manufacturing deficit, the reality is that the silicon industry has been hacking away at a healthy level of spare capacity for many decades.

When evaluating this issue, it is tempting to just focus on the innovation in microelectronic technologies driven by Moore's Law. But that restricts any analysis to simply logic and memory technologies. To really get to the bottom of what's been going on, it's critical to also consider the evolution of other semiconductor technologies, as well as the lack of investment in fab construction, tool investment, process development and labour force development.

Moore's Law tech is defined as the leading node size for logic and memory technology. Those that play there need very deep pockets. Today, just a couple of companies are investing $30 billion or more to build fabs that can churn out chips at the 5 nm node or below. Supporting them is an ecosystem of tool and material suppliers that have developed the manufacturing technology for cutting-edge fabs to process wafers.

It is these IDMs, foundries, materials suppliers and tool manufacturers that are responsible for pushing the microelectronics industry forward at an incredible rate. And this leading edge is where almost all semiconductor capital investment exists. Even in the last two years, leading-edge and near-leading-edge technology has accounted for 86 percent of semiconductor capital investment, according to IHS Markit. Due to this strong focus on the capital deployment that has pushed the Moore's Law tech forward, a vacuum has been left in its wake that has opened the door to a range of alternative technologies.

These alternative technologies have benefitted from the approach of Moore's Law tech leaders, which



Relative distribution of chips in iPhone 13 Pro, per teardown by iFixit.

have shrunk nodes through innovation in device design and investment in new fabs, new tools and new process technology. As the proponents of Moore's Law have marched from one node to another, their previous generation of tech and capital equipment has been sold on. Snapping it up have been the many players in the 'More than Moore (MtM)' arena, which encompasses all devices that exist outside of logic and memory, and includes makers of compound semiconductor chips.

Sectors that are within the MtM industry include those associated with RF, power, sensors, MEMS, photonics and analogue devices. While they evolve and develop in a more conservative fashion than Moore's Law tech, that does not imply that they don't make a crucial contribution to our everyday lives. These chips are an essential ingredient in everything from cars to toothbrushes. Even phones, which tend to have the latest generation of memory and logic on board, have more chips made with MtM technologies, such as RF, power, and sensors.

Diverging toolsets

In 2022, we are seeing a shift in the interplay between those companies at the forefront of logic and memory, and those working in MtM industries. One factor at play is that leading-edge Moore's Law technology is not downcycling capital at the same rates as before. But another big change is that MtM technology, which has becoming more important and more pervasive in all our electronic devices, is now so diverged from Moore's Law tech that it requires its own specialized development. Most of the fabs that run MtM technology, including those producing compound semiconductor devices, are repurposed fabs that formerly existed on the Moore's Law frontier. After purchasing these fabs, minimal changes were required before MtM manufacturing could begin.

However, today this route is not easy to pursue by the manufacturers of MtM technology. In the last few years, the number of repurposable fabs has fallen, as silicon fabs that are multiple generations behind TSMC and Samsung continue to churn out logic and memory chips. Highlighting this point is Intel's 14 nm fabs, and foundries with 20 nm+ fabs, still operating in high-volume production. Due to this dearth of fab space, new fabs are being built specifically for MtM technology, such as Wolfspeed's Mohawk Valley 200 mm SiC facility that opened earlier this year.

Historically, when a new MtM wafer fab opened or expanded, it would be kitted out with used tools, purchased and repurposed from a Moore's Law 'junk yard'. This inspired an entire industry of resellers and refurbishers, like Moov, that have aided efficient repurposing of fab equipment down the value chain from Moore's Law tech to MtM technology. Today, many of these tools in existing MtM fabs are reaching the end of their life.

At ClassOne Technology – a provider of high-performance electroplating and wet surface preparation equipment to facilities using 200 mm and smaller wafers – we often hear of wet process and plating tools that have been running for 20 years or more. This has led many existing fabs to look for replacement equipment. At the same time, new fabs are looking for tools, a state-of-affairs that has forced MtM technology manufacturers to

The ClassOne Trident Spray Solvent Tool provides modern and affordable batch wet processing.

purchase new tools and partner with manufacturers in ways they have never done before.

As these MtM chipmakers grapple with this situation, we are on hand to offer a great deal of value to them. We offer the Batch Spray Trident system, which is a modern, cost-effective spray solvent and spray acid tool that can drop in as a direct replacement for aged tools. We also offer class-leading performance technology through our Solstice single-wafer platform, which is primarily serving compound semiconductor and other MtM customers.

By traditionally using refurbished tools, MtM technology has been bound by the design parameters of this capital. This restriction has not been faced by Moore's Law tech, which has done a great job at overcoming bottlenecks associated with processes and materials. Unfortunately, technologies such as compound semiconductors face different bottlenecks and have differing needs. With MtM technology continuing to grow, more scrutiny is being placed on these bottlenecks, on efficiency, and on process optimization constraints.

One example of these factors at play has occurred at a MtM company that has needed to advance its gold-plating process efficiency. Working with us and a chemical vendor, it has succeeded in this endeavour. Efforts could draw on gold electroplating widely used in the silicon industry, although this washed out of the Moore's Law Tech frontier more than a decade ago. Consequently, it has not been researched or optimized to the level of other materials, such as copper; and the interests of the largest of the big silicon-focused companies do not extend to these MtM domains.

Operating at the sweet spot

Against this backdrop we can be a gamechanger, as we occupy the sweet spot: we are large enough to support process development at our Technology Development Center; but we are not so large that only big Moore's Law tech can access our capability. This opportunity excites us, and we are very keen to help grow an ecosystem of technology partnerships in the MtM technology segment.

Above: The ClassOne Solstice single-wafer platform provides advanced electroplating and wet process technology.

As well as finding it hard to acquire used tools, MtM fabs are finding it tough to find experienced employees to run them and manage their facilities. This issue can be traced back to the actions of big semiconductor players, which are gobbling up talent at all levels to run their new fabs. This has forced MtM fabs to hire and train fresh graduates and new employees. Here we lend a hand, providing many of our customers with deep-dive training for their new employees on our tools and processes.

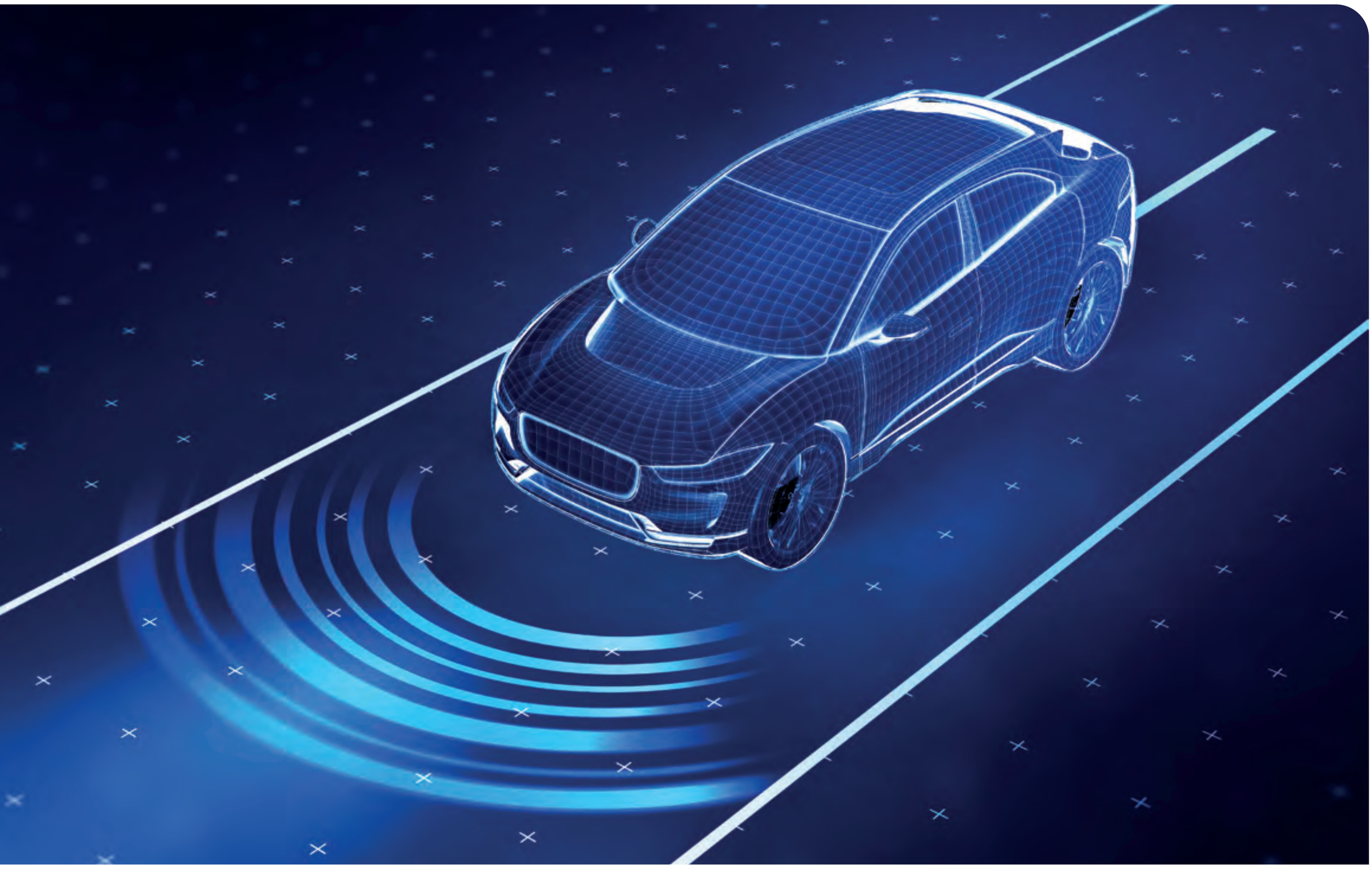
We are also assisting the smooth running of fabs through the launch of products designed for ease-

ClassOne's Technology Development Center has advanced metrology and processing capabilities used in joint development programmes and technology partnerships.

of-maintenance and automated troubleshooting. Our technology uses modern software and algorithms to limit the need for human intervention.

MtM technology is on an upward trajectory, which must continue, given that the resulting devices are important to everyday life. Key to further progress is to follow in the footsteps of the Moore's Law brigade, which has dedicated tool vendors, suppliers and fabs supporting the production of leading-edge memory and logic nodes. However, having a diversified ecosystem for MtM technologies is not, in itself, enough – there is a need for capital to build fabs; for tools that are specifically designed for unique challenges; and for technology partners who will help solve complex problems.

The good news is that there is an evolving ecosystem of solution providers focused in the MtM space, where we plan to be a model company. While the pandemic and other major events have disrupted global supply chains and taken the blame for the chip shortage, that should not obscure the reality that investment is essential for sustaining our lifestyles in MtM technologies.



Move over MOCVD

Thanks to its superior stability, MBE trumps MOCVD for the growth of long-wavelength VCSELs based on dilute nitrides

WHEN A DEVICE can do much more, it has a brighter future ahead. That's certainly the case for the VCSEL. Initially it enjoyed much success as the optical source for transmitting data over short distances, and over the last few years sales have swelled to new highs, thanks to its deployment in the facial recognition systems found in smartphones. But even higher revenues are now on the horizon. They can be realised by expanding the spectral range of this surface emitter via the introduction of dilute nitrides, such as GaInAsN(Sb), that propel emission to 1300 nm and beyond. Sources operating in this domain are highly valued, being better suited to lidar and 3D sensing. That's because light in this spectral range transmits through the glass display of the handset, and is intrinsically eye-safe, opening the door to the use of higher-power sources.

Today's commercial VCSELs, which are based on either a GaAs or InGaAs active region and tend to emit at around 850 nm or 940 nm, respectively, are manufactured using MOCVD. But this mature growth technique, which dominates the production of III-V optical devices, is not necessarily the best option for producing VCSELs that feature quantum wells with a few percent of nitrogen. Despite decades of devoted effort, repeatable growth of dilute nitride layers with a controllable composition is still incredibly challenging by MOCVD.

History attests that a far better option is to use MBE to grow layers of dilute nitrides, partly because the lower temperatures associated with this technique ensure higher sticking coefficients for indium and antimony. Just over a decade ago, Solar Junction shot to fame by breaking the record for the efficiency of multi-junction solar cells by introducing low energy junctions made from dilute nitrides. This West-coast start-up developed commercial production processes for making these devices. And more recently, Array Photonics, a developer of lasers and photodetector arrays for infrared sensing applications, has been pursuing MBE for the production of its dilute nitride devices.

It is worth noting that the choice of reactor does not have to be an 'either-or' decision. There is the option of wafer transfer, allowing some of the epitaxial stack to be grown by MBE, while other regions are produced by another process, such as MOCVD. With a two-pronged approach the mirrors of the VCSEL may be grown by MOCVD, and the dilute nitride active region by MBE.

MBE's merits

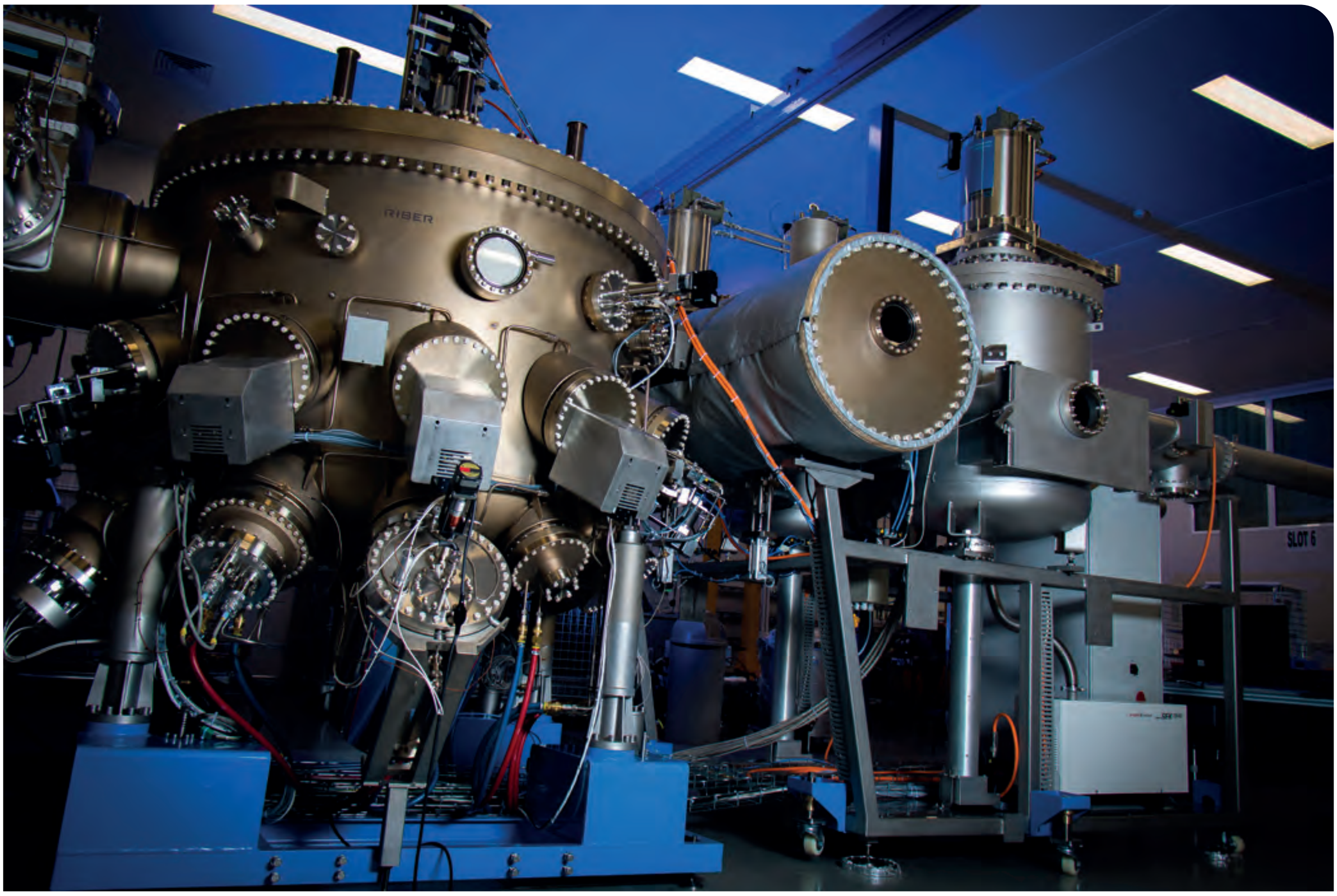
Thanks to its unique capabilities, there is much to like about MBE. It is a strong contender for the growth of all VCSELs, as it is capable of producing layers with exceptional uniformity and outstanding interface abruptness, due to the inherent atomic precision. In addition, it's possible to produce high doping levels in *p*- and *n*-type material with high purity, thanks to the absence of hydrogen incorporation. What's more, this form of epitaxy reaches a lower intrinsic background level than its rivals.

MBE is also renowned for its versatility. As well as playing a key role in the development of dilute nitrides structures, this form of epitaxy has been employed for decades for high-volume production of numerous epiwafers and various devices. MBE has been used within the RF/microwave industry by the likes of RFMD and Filtronic to produce pHEMTs; II-VI Laser Enterprise uses this growth process to make a range of lasers; and this epitaxial technique has been used to produce photodetectors, such as InP-based avalanche photodiodes and *p-i-n* structures. MBE reactors are also employed at the leading epiwafer providers, such as Intelligent Epitaxy Technology (IntelliEPI), EpiSolution and IQE's facilities in the US and Singapore.

Exactly how MBE is employed within our community continues to evolve. During the last eight years or so, it has been demonstrated that MBE lends itself very well to the formation of highly sophisticated structures for various fields of optoelectronics, such as compound semiconductor devices containing phosphorous, antimonide or nitrogen.

At Riber, we have played a key role in supporting these efforts. There are now more than 35 installations of our MBE 6000 reactor, which accommodates multiple 6-inch wafers. The uptake of this tool has firmly established MBE as a viable option for producing RF/microwave device material, and for the manufacture of optoelectronic devices.

When device makers use MBE reactors in their foundries, they are able to benefit from stable, reproducible processes that can be maintained



➤ The latest high-volume MBE reactor from Riber, the MBE 8000, accommodates eight 6-inch wafers and produces an across-platen uniformity that's less than 0.5 percent. Epistructures produced by the MBE 8000, which provides stable growth conditions over maintenance-free campaigns that can last more than 12 months, feature abrupt interfaces and have a high material purity, including the absence of hydrogen.

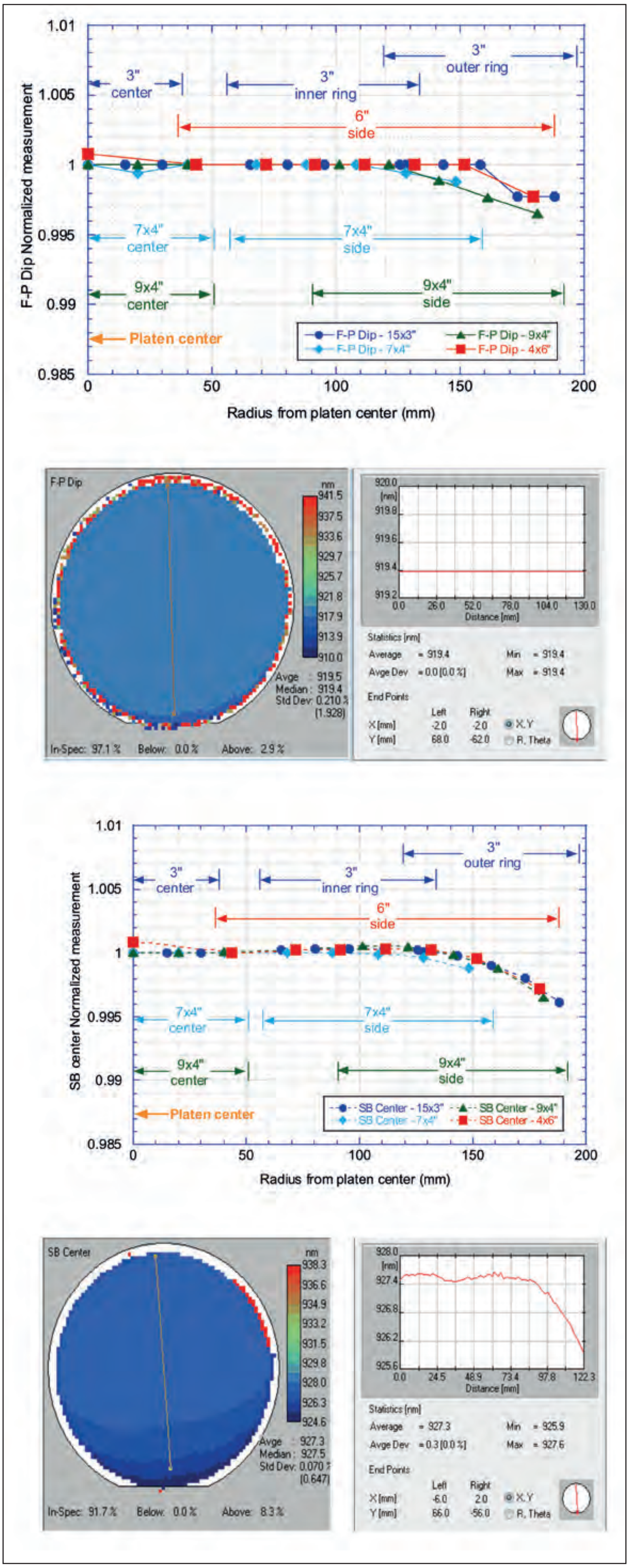
throughout a campaign that may last as long as a year or so. Those that are working there have epitaxial techniques that deliver a high yield, and are truly compatible with industrial production requirements, such as being fully automatic and having the capability to run '24/7'.

Demonstrating feasibility

For those that are considering developing production processes for dilute nitride VCSELs that involve the use of MBE, it should be noted that thanks to recent efforts, our MBE 6000 has been proven for the production of VCSEL structures, particularly for datacom applications. Results obtained by IntelliEPI have shown that this tool of ours can deliver excellent uniformity, in terms of output wavelength, across a full platen of four 6-inch wafers (see Figure 1).

Engineers at IntelliEPI have also demonstrated that with MBE, reproducibility can be close to 100 percent for the die-to-die output wavelength, for both high-specification 850 nm VCSELs for datacomms apps, and for 940 nm cousins that serve power 3D sensing. We attribute this very high level of reproducibility to exceptional thin-film uniformity provided by our correctly designed systems, such as our Riber MBE 6000.

Efforts at developing robust growth processes for producing dilute nitride VCSELs will be able to draw on a number of *in-situ* monitoring tools. Like MOCVD, MBE chambers can accommodate optical instrumentation that provides real-time monitoring of the growth process. Offering a diagnostic capability, these optical measurements can track the optical properties of the epiwafers, including their mirrors, and ensure that all wafers are precisely within the wavelength specification range. To assist process engineers, we have launched the EZ-CURVE – it provides *in-situ* curvature measurements and has shown promising results for monitoring the growth of VCSEL mirrors. Additional *in-situ* tools include those that provide measurements of the optical flux,



➤ Figure 1. (a) Normalized Fabry-Pérot dip wavelength versus radial distance from platen centre for the 15 x 3-inch, 7 x 4-inch, 9 x 4-inch and 4 x 6-inch platens in a Riber MBE 6000 reactor. (b) Reflectivity maps and radial line scans of the Fabry-Pérot dip across 940 nm VCSEL structures grown on a 6-inch GaAs substrate in a Riber MBE 6000 reactor (4 × 6-inch). The Fabry-Pérot dip variation, below 1 nm, is limited by measurement accuracy. (c) Normalized stop-band centre wavelength versus radial distance from the platen centre for the 15 x 3-inch, 7 x 4-inch, 9 x 4-inch and 4 x 6-inch platens in a Riber 6000 MBE reactor. (d) Reflectivity maps and radial line scans of the stop-band centre across 940 nm VCSEL structures grown on a 6-inch GaAs substrate in a Riber MBE 6000 reactor (4 × 6-inch). The stop-band centre variation is below 3 nm across the 6-inch wafer.

reflectivity, pyrometry and the absorption band-edge temperature. Unlike MOCVD, it is also possible to track the evolution of the crystal structure, thanks to reflection high-energy electron diffraction. By combining this suite of insightful *in-situ* instruments with the intrinsic unsurpassed crystalline precision of MBE, this growth technique can address some of the traditional issues associated with the epitaxial growth of VCSEL structures on GaAs substrates by MOCVD. Switching from MOCVD to MBE increases the proportion of the wafer where there is a matching of the wavelength of the laser's active region to the reflectivity sweet spot of the distributed Bragg reflector. In addition, the use of MBE addresses homogeneity issues and device processing yield losses, while trimming bow stemming from the GaAs/AlGaAs DBR structure.

Seizing the opportunity

Against the backdrop of increasing VCSEL consumption, there is much promise for MBE within this industry. It has proven capability, demonstrated by the successes at IntelliEPI, and much promise for driving the commercial success of the dilute nitride VCSEL. Those that wish to try and dominate the long-wavelength VCSEL market may wish to consider our ultra-high capacity MBE 8000, launched last year and developed with the production of the VCSEL specifically in mind.

With the ability to accommodate eight 6-inch wafers, the MBE 8000 has twice the capacity of the MBE 6000. The first MBE 8000 is now undergoing final qualification to validate the highest uniformities, not just in terms of effusion sources, but also substrate temperature, across the largest deposition area available in MBE. Once qualified, this tool will strengthen the compelling case MBE makes in playing a critical role in the production of dilute nitride VCSELs.

FURTHER READING

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➤ M.G. Ebski *et al*. Baseline 1300 nm dilute nitride VCSELs OSA Continuum **3** 1952 (2020)

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➤ Compound Semiconductor 2021, 6, 26

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Superjunction sparks super devices in silicon carbide

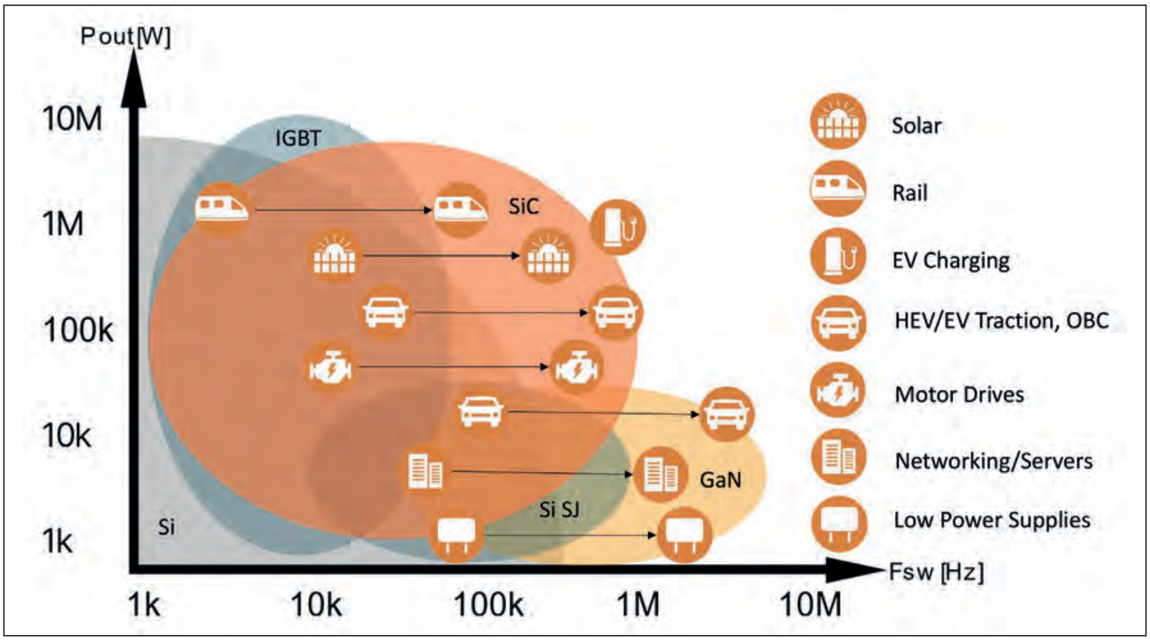
Armed with a clever charge-balance structure, SiC power devices are pushing beyond their limit

BY JAN CHOCHOL AND ROMAN MALOUSEK FROM ONSEMI

THE ENTIRE power electronics industry is buzzing with SiC activity. It's no wonder, given that SiC devices have a dielectric breakdown field strength that's ten times higher than that of silicon, as well as twice the electron saturation velocity of the incumbent, three times its bandgap, and a thermal conductivity that is better by a factor of three. All high-power applications benefit from these traits, shown in Figure 1, so it's of no surprise that vendors, fabs and OEMs are embracing the rapid adoption of SiC. All are trying to outperform, outlast and outclass their competition.

Due to all this frenetic activity, there is some turmoil in this sector, creating opportunity for all kinds of development. This has motivated our team at onsemi to explore various concepts. Against the backdrop of a maturing SiC industry, we have been able to revisit some topics that just a few years ago would be either unfeasible, too expensive or just plainly not possible with the toolset available at that time.

One such concept is the superjunction. Regardless of design, any device that is made from SiC will benefit from its unique properties. They include a large electric breakdown field that shaves tens of micrometres of epi thickness, greatly reducing the on-state resistance for a given voltage rating compared with silicon. But with the superjunction structures that we have explored, one can go a step further. Generally, this structure consists of



➤ Figure 1. Areas of application for different power electronic technologies.

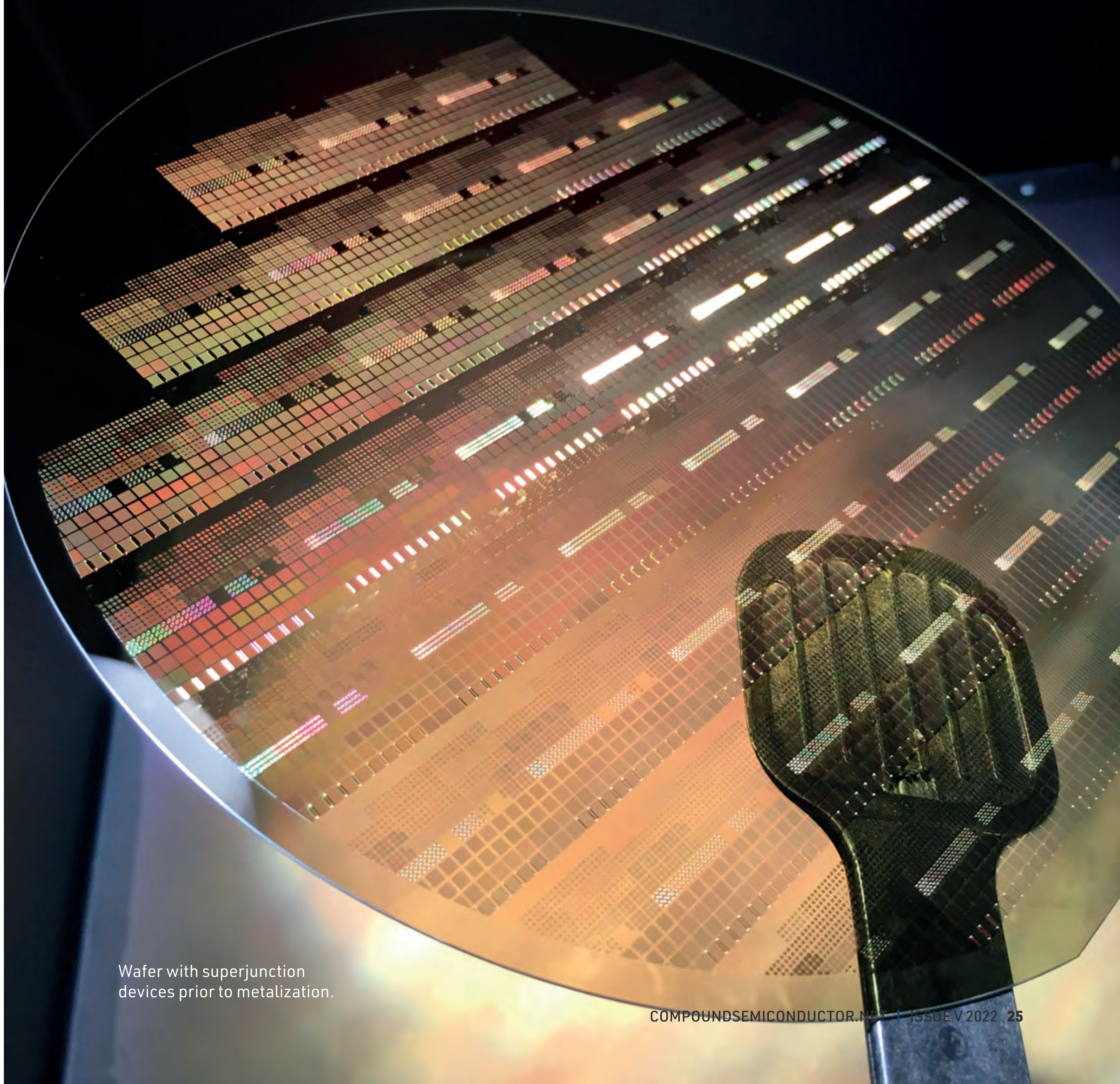
alternating regions that are highly doped, tightly spaced and with equal and opposite doping – an architecture that ensures charge balancing. With such a structure, the high doping results in superior conduction that reduces resistance. But that's not the only benefit we get – operated under reverse bias, the superjunction is fully depleted, with the electric field spread evenly in a roughly rectangular shape. Thanks to this, compared with a classical unipolar drift region, where the electric field must be trapezoidal (see Figure 2), we realise a higher breakdown field at the same drift thickness.

The real question is how can we make such a structure? We need to have defined pillars, with a controllable concentration reaching several micrometres below the surface. As each micron of superjunction depth can block about 200 V (we go on to show this), a 1200 V device needs more than 6 μm of well-controlled superjunction pillars.

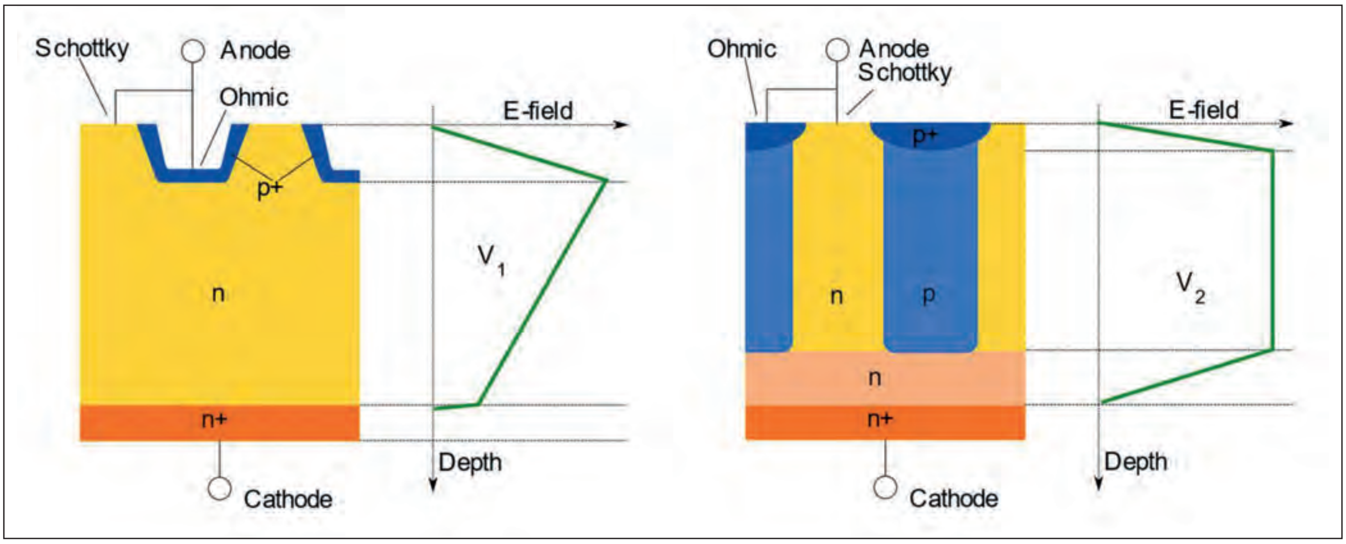
One option for forming the pillars is ion diffusion. However, those working in the SiC community don't tend to concern themselves greatly with this technique, as there is simply no way to diffuse ions in SiC. This has led some groups and companies to try other approaches, such as trench filling by CVD.

Revisiting ion implantation

But in our pilot study, we decided to take another look at ion implantation, due to the simplicity of the method and the availability of tools. We



Wafer with superjunction devices prior to metalization.

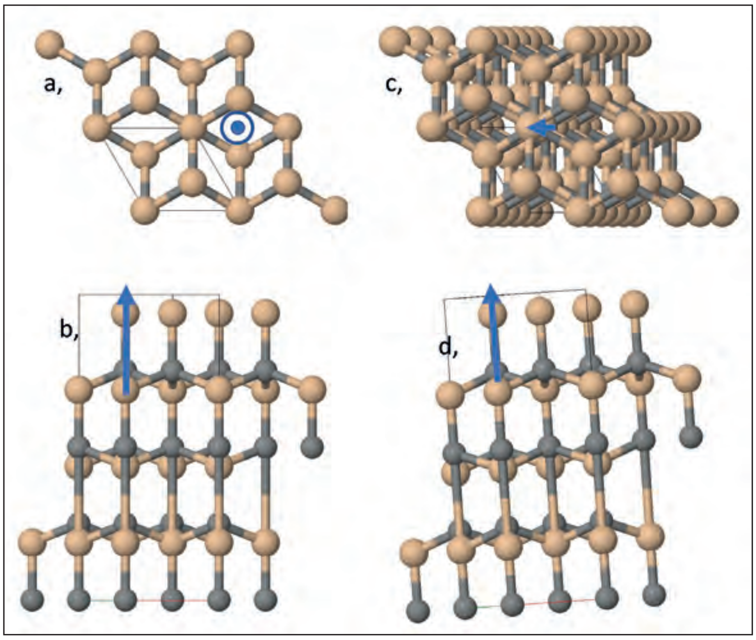


➤ Figure 2. Schematic diagram of JBS diode with unipolar drift region (left) and superjunction JBS diode (right).

have investigated two different techniques. One involves using very high energy implants. Roughly speaking, this is a brute force approach; we push the implants deep into SiC, due to their high kinetic energy. Higher energy means deeper penetration. Then, using multiple implants, we can chain the concentration profile together to create a seemingly uniform distribution. The caveat of this approach is that we have to shield the other pillar from the implantation. So one implant can be blanket, while the other must be masked and have twice the dose of the other. Success is not easy, as there is only so thick a photoresist that can block the implant.

Due to this limitation, we have also explored the channelled implant. One key characteristic of the 4H polytype of SiC, used for power applications, is that it permits ion implantation along a preferential angle, where ions 'see' through the lattice and the number of ion-lattice collisions plummets. This principle, illustrated in Figure 3, leads to a concentration profile that is far deeper and flatter than that normally possible with a random implantation direction. For example, a 900 keV non-channelled implant of aluminium reaches a depth of up to 0.7 μm, while channelling with this energy extends the depth to 3 μm.

With this approach we have produced pillars by combining a blanket high-energy nitrogen implantation, which does not require a mask, with a masked channelled aluminium implantation. The success of this scheme is seen in profiles obtained by secondary-ion mass spectrometry (see Figure 4).



➤ Figure 3. JMOL simulation of 4H-SiC lattice. Blue arrow shows the direction of *c*-axis of the crystal. (a) view through the channelling direction; (b) sideview; (c) tilted lattice; (d) tilted lattice sideview.

The channelled direction is along the 0001 direction of the crystal – this is also the direction in which the crystal is grown. As most commercial SiC crystals are cut at a 4° angle, this is the channelling angle we employ. To produce well defined pillars, it's critical that the implantation tool maintains the optimal angle across the wafer and batch-to-batch. We're grateful for the support of Nissin Ion Equipment, which helped us in this endeavour during our pilot study.

Regardless of whether we employ channelling or very-high-energy implantation, an epi re-growth step is needed to get to the desired thickness. When restarting the epi process for each new pillar layer, we tuned the conditions carefully, to minimize any potential loss of implanted material (etch back) and ensure a constant concentration throughout the epi-structure. Another challenge we have faced is to tune the alignment of the masks to the alignment marks after each epi regrowth, and to renew the marks to assure a precise position of the layers that follow. For the structures formed by very high energy implantation we undertook three epilayer growth steps, each involving a deposition of a 1.2 μm-thick layer; and for the channelled run, we used just two growths, each 2.45 µm thick. We have fabricated junction barrier Schottky diodes from both types of structure. This involved using parallel stripes as mask for the pillars. As these stripes are parallel to the wafer flat, we avoid mask shadowing when undertaking channelled implantation.

Assessing different die

To fully assess our device's behaviour, we have made both small (0.0012 cm^{-2}) and large (0.018 cm^{-2}) dies. Small dies allow us to investigate a multitude of designs, while their large siblings have properties more akin to production-line devices (the wafer with the designs can be seen in the image on p. 23).

With superjunction devices, it is essential to ensure a proper charge balance. This means that both pillars have the same concentration of dopants. With any process, factors are at play that will lead to a spread in the concentration. But it is possible to address this by varying the stripe width, as this provides a mechanism to compensate and tune the design – a wider, lower-doped pillar will behave the same as a narrower, higher doped one. We implant the top of the *p*-type pillar with a shallow, high dose of aluminium to ensure a good ohmic contact.

Contacts to our devices have been made with a standard SiC process. This added a Ti/TiN Schottky/ohmic contact to the front side. We turned to a backside grind and metal deposition for the cathode contact. Our devices feature termination, used to spread the electric field and distribute the avalanche current homogeneously in an active region. We verified this had been accomplished by electroluminescence, which shows a uniform breakdown in the active structure (see Figure 5).

Before diving into the results of our superjunction study, it is worthwhile to consider our assumptions of the expected behaviour. Key characteristics are the breakdown voltage of the diode and its on-state resistance. The ideal is to have a perfect 1:1 ratio in pillar concentrations, as this ensures a maximum achievable breakdown voltage – for a given thickness of the superjunction. Meanwhile, the on-state resistance scales linearly with the *n*-type concentration, where the conduction happens (behaviour is illustrated in Figure 6).

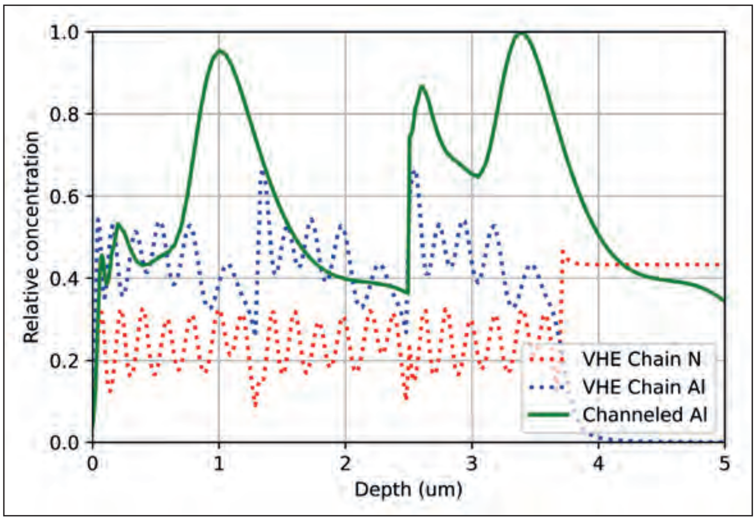


Figure 4. SIMS data on implanted profiles in the superjunction experiment.

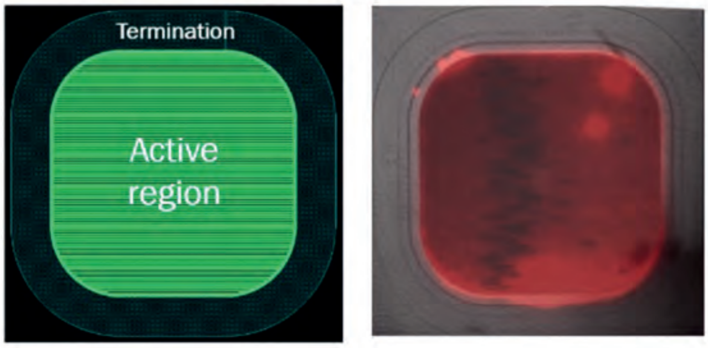


Figure 5. Left: Schematic of the device design. Right: Electroluminescence of the device in the avalanche breakdown.

The actual results of our study, shown in Figure 7, confirm our assumptions. We used three wafers for each implantation scheme, each with a slightly different dose (± 10 percent), and changed pillar ratios in the device design. Our breakdown results follow a parabolic shape, with the absolute position determined by the thickness of the superjunction. Note the spread across the wafer, with a thicker epi-structure near the flat giving a higher breakdown voltage (optimizing for uniform wafer distribution

SiC devices are also sought after for their high-temperature performance, which comes in to play in almost all their applications. It is here where the superjunction puts the 'super' in devices.

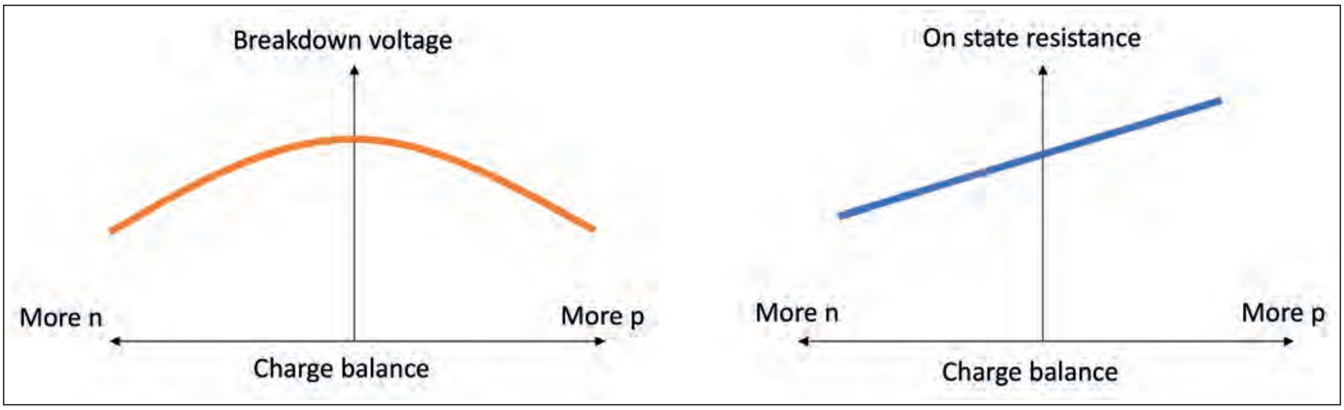


Figure 6. Predicted behaviour of the superjunction device.

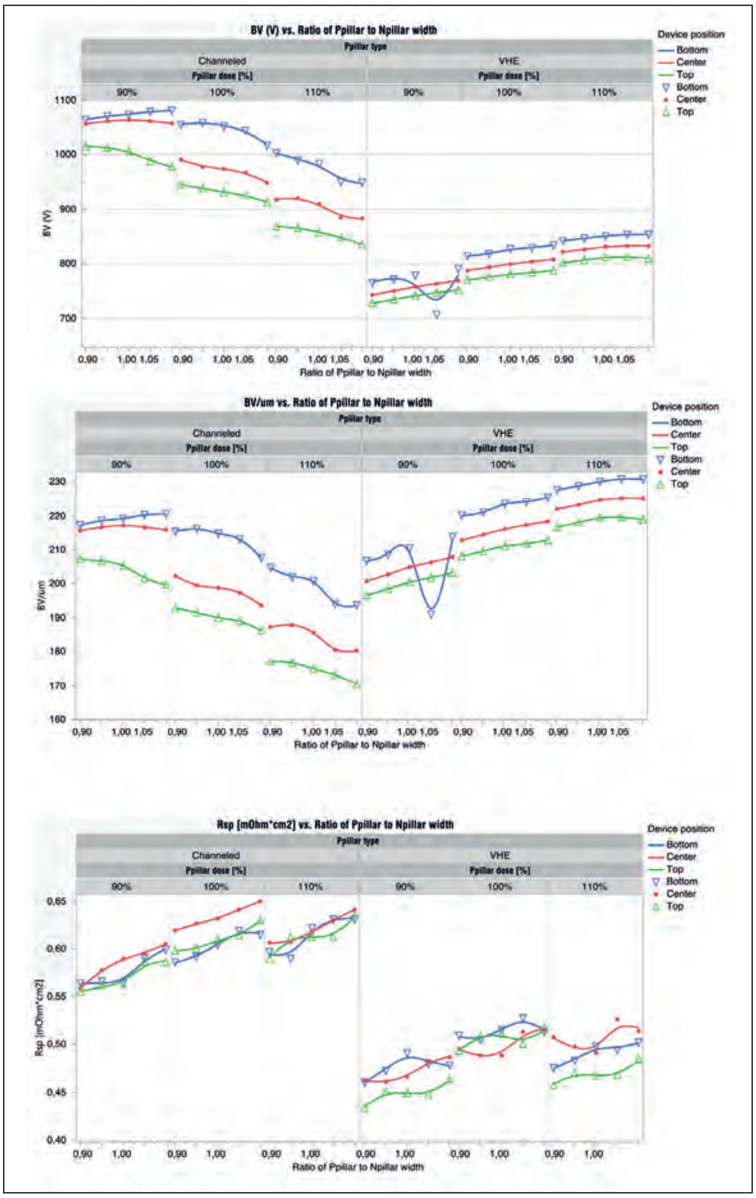


Figure 7. Electrical data from characterization of the superjunction devices characterization of the superjunction devices

was not part of the study). As expected, the on-state resistance increases with the width of the *p*-type pillar and with the epi-thickness. We have addressed the variation in the on-state resistance between the wafers to the variation of the substrate resistance.

To compare the results realised by very-high-energy implantation and channelling, we have normalized breakdown values by thickness. After omitting the epi-thickness spread, both approaches gave about 210 V/µm of breakdown. This is a crucial finding, implying that both approaches are equal, in terms of electrical performance and process stability. Where the differences lie are in the toolset needed and the number of epi steps required.

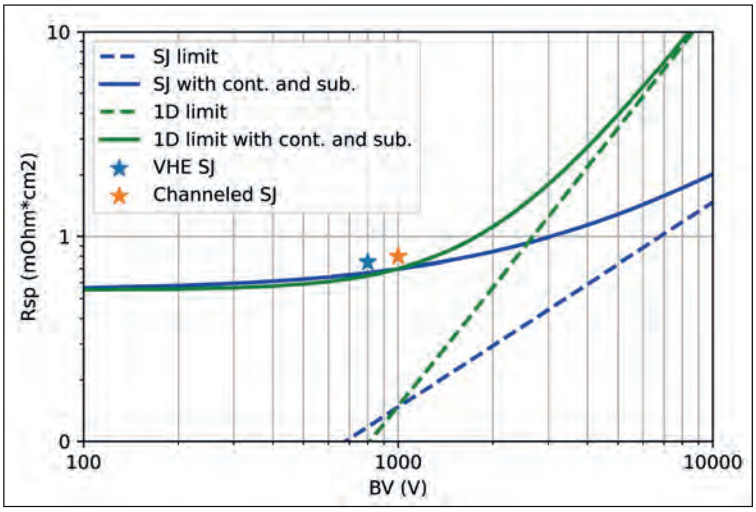
With data at hand, we can compare our devices to those with a classical architecture, including a variant with a unipolar drift region. Our evaluations, which include a plot of the one-dimensional theoretical limit of such a device, enable comparison of on-state resistance and breakdown voltage (see Figure 8). We see that with our test devices, measurements on our larger die show that we are just at the tipping point at 1000 V/0.7 mΩ cm^{-2}. Generally, the sweet spot for usage of superjunction devices is above that, in the 3 kV-5 kV region.

This, though, is only one side of the equation. SiC devices are also sought after for their high-temperature performance, which comes in to play in almost all their applications. It is here where the superjunction puts the ‘super’ in devices. The drift region, where the blocking field is spread, is the lowest doped part of the device. It is here where there is a large contributor to device resistance – but the introduction of the superjunction makes this region thinner and highly doped, changes that as we’ve seen pay off after 1000 V of blocking voltage. Thanks to high doping in this region, this device is less affected by a temperature-induced resistance increase. What happens is that the device maintains its low resistance even at higher temperatures. All the while the breakdown is largely unaffected. In fact, it increases, due to increased phonon scattering – more energy is needed to push electrons into avalanche. So, as we’ve shown, replacing the drift region with the superjunction pays dividends, transforming an ordinary device into one that excels in highly demanding applications.

The adoption of SiC devices and their related development, including the progress reported in this study, would not be possible without scaling up the entire SiC ecosystem. Whether it is the making of substrates, involving wafering, grinding, polishing; or epitaxial growth or other front-end or backend processes; every step is a demanding operation that needs to draw on hard-earned expertise and specialized tools.

SiC initially came to us at onsemi through the acquisition of Fairchild, where device technology has ever since been developed in close cooperation between: the design center in Kista, Sweden; the device and process integration teams in Bucheon, Korea; and the engineering team at South Portland, Maine, responsible for developing SiC epi technology.

Our current role includes supporting SiC development and production in key fabs, in Bucheon, South Korea and in Rožnov pod Radhoštěm, Czechia. In Rožnov, which is a small town nestled in the Beskids mountain range, materials development is gaining much attention, recognized with an award for the most innovative company in the region.



➤ Figure 8. Trade-off curves of breakdown voltage and on-state resistance for unipolar and superjunction devices with experimental data shown

With the recent acquisition of a SiC substrate manufacturer – GT Advanced Technologies – our company has increased its level of vertical integration and solidified its SiC device portfolio. These moves have strengthened our position as a significant force in the power electronics industry and sharpened the cutting edge of SiC technology.

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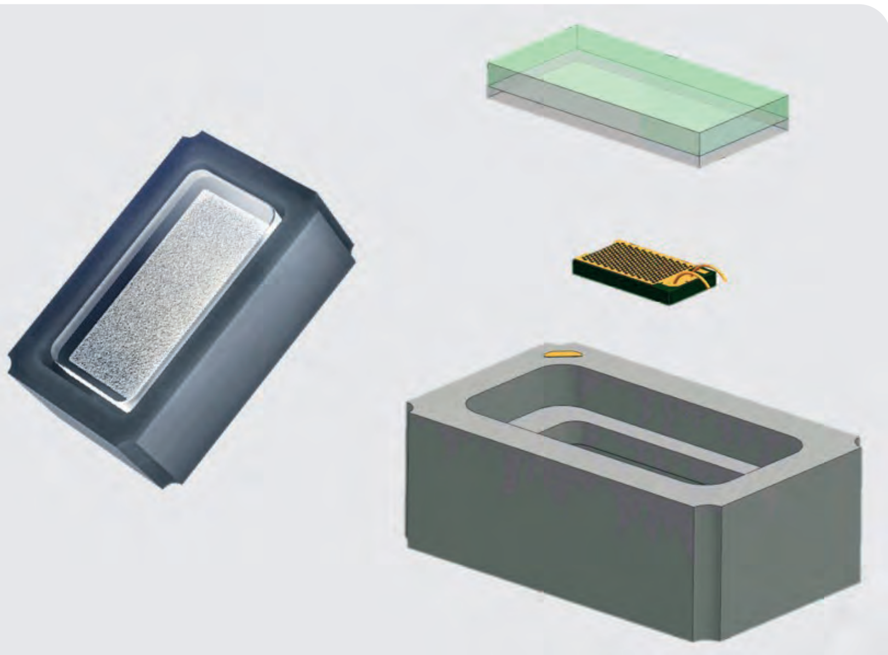
VCSELs: Integrating backside optics

Equipped with micro-optics, VCSELs are even more attractive candidates for deployment in smart glasses, face recognition systems, automotive in cabin-sensing and lidar.

BY STEPHAN GRONENBORN FROM TRUMPF PHOTONIC COMPONENTS

THE VCSEL is the ideal source for delivering infrared illumination for 3D sensing. This class of laser produces a narrow and stable spectrum, switches at very high speeds, and operates over a temperature range that spans from -40 °C to 125 °C. And when it is driven with short pulses, it enables the generation of high-resolution 3D distance maps.

Deployment of the VCSEL in consumer electronics goes back several years. Since 2015, it has been a standard component in smartphones. More recently, applications where it is seeing sales have broadened. Now, as well as assisting with time-of-flight measurements for face recognition and depth sensing in smartphones, VCSELs are serving in world-facing systems in phones, tablets and robots, and even delivering high-power levels needed in automotive and industrial heat treatment processes.



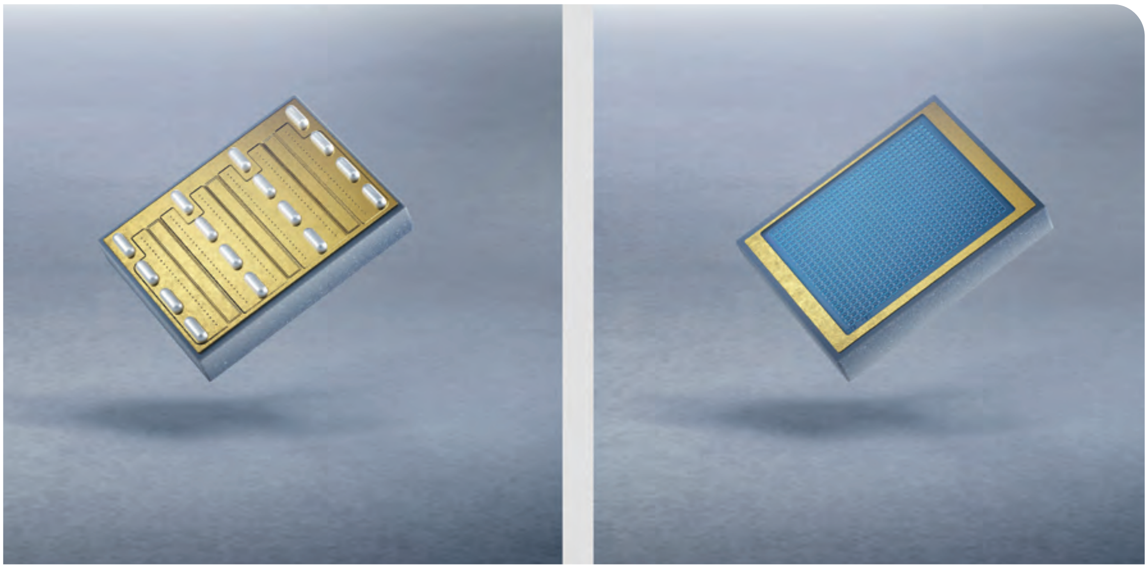
➤ Figure 1. A sketch of a state-of-the-art SMD flood illuminator.

When designers select a bare VCSEL chip, they must package this alongside accompanying optics, connections, driver electronics and safety means. Optics are essential for transforming the beam that emanates from the VCSEL into the desired illumination pattern for the scene. To ensure eye-safety, it is crucial to have correct, properly assembled optics, as well as proper driving of the VCSEL. The downside of this multi-component approach is that by having VCSELs in a separate package, it is impossible to exploit the full potential of the semiconductor production technology, in terms of both footprint and functional integration (this is illustrated in Figure 1).

The VCSEL revolution

At Trumpf Photonic Components we are addressing this shortcoming with a new technology, ViBO, which is short for VCSEL with integrated Backside Optics. Our revolutionary idea is to integrate all optical functions, currently provided by an additional package, directly into the VCSEL chip. The aim is to realise miniaturization while improving performance.

For wavelengths of 940 nm or more, vertical-cavity structures and the transparency of the carrier substrate allow the laser's emission to exit through the substrate. Adopting this architecture, rather than the conventional one with emission on the epitaxy side, offers a number of benefits that include having hardly any optical losses. Given the attractiveness of this geometry, our efforts towards miniaturization have begun by flipping the direction of the light emission. With light no longer coming out of the surface of the chip, where all the processing and contacting takes



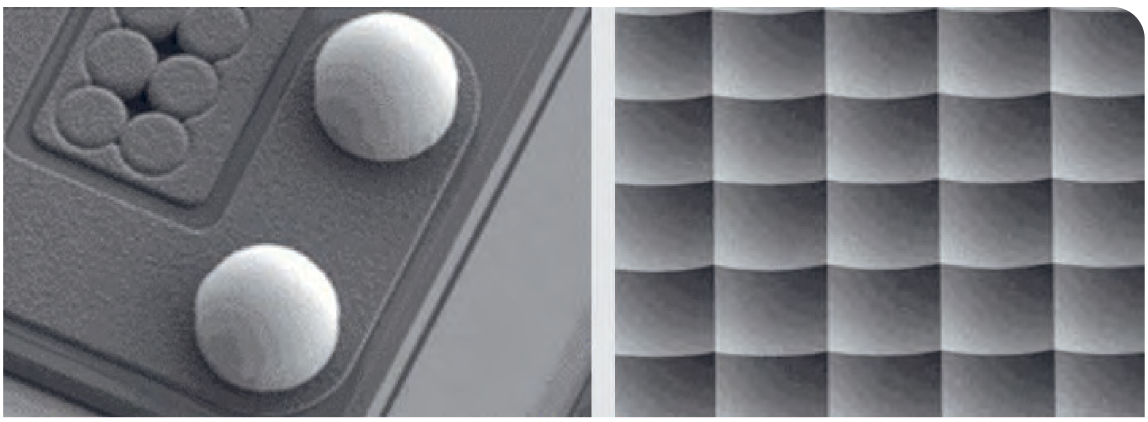
➤ Figure 2. An exemplary ViBO array with the contact side on the left and the lens side on the right.

place, but through the backside of the substrate, this part of the device is no longer just a mechanical interface but valuable real estate. It is here where we directly etch lenses into the GaAs to provide an optical function and enable extraordinary freedom of design for the customer. Note that the refractive index of the lens is as high as about 3.5, far more than the 1.5 to 2 of plastic and glass, giving much more freedom. What's more, with our revolutionary design, we eradicate the need for individual alignment of laser die and optics. Instead, the optics becomes an irremovable part of the laser die, and thus a beneficial step for long-term laser safety.

With the processed surface of the chip no longer needed for light emission, this area can be used for electrical, thermal and mechanical functions, enabling optimisation of heat removal and electrical contacts.

One option is to use large contacts on the epitaxy side, enabling direct soldering with flip-chip assembly of the die – this eliminates the need for wire bonds. Merits of this approach are superior thermal management and reduced inductivity of the system. Alternatively, contacts can take the form of slim copper pillars (see Figure 2) enabling SMD mounting to the board or driver IC. Using a large number of such contacts enables individual addressability, and therefore new functionality of the VCSEL chip.

As well as offering the same functionality as the VCSEL in a packaged solution, our ViBO technology has additional benefits that can revolutionize smart-sensing systems. First, the footprint of our ViBO source is five-to-ten times smaller than a traditional VCSEL, and its height is reduced by a similar factor – it is possible to replace a millimetre-thick package with a 150 μm-thick chip. Such miniaturization is highly valued in consumer electronics, including smartphones. Consequently, it is easier to design an entire sensing system with ViBO components, thanks to their diminutive size. Second, our ViBO technology ensures an inherently eye-safe system during the whole product lifetime, because the optics is an irremovable part of the chip. This eradicates safety hazard concerns associated with delaminating or malfunctioning optics. Third, the GaAs optics is more powerful, enabling new designs with superior efficiency. Fourth, new functionalities are possible, as more contacts are on the chip, enabling addressable segments. As these contacts are underneath the surface, the footprint remains



➤ Figure 3. Scanning-electron-microscope pictures of the copper-pillar solder bumps (left) and the lens side (right).

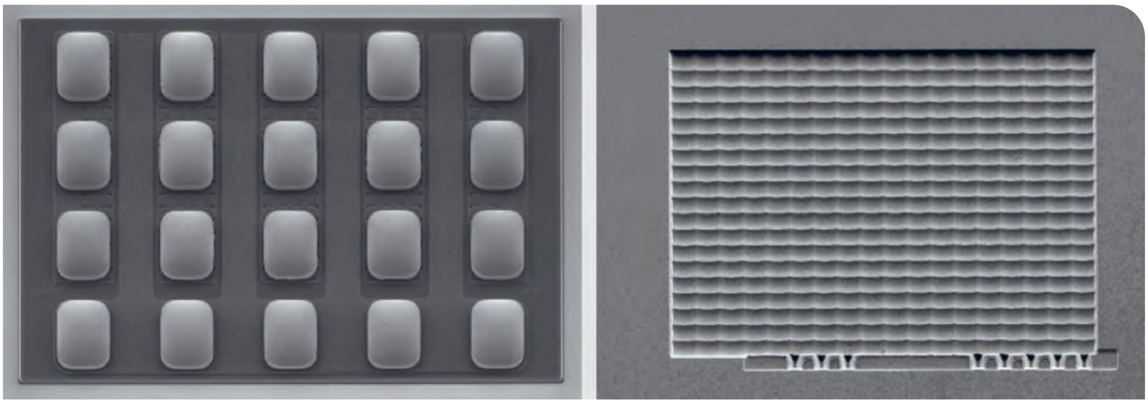


Figure 4. A scanning-electron-microscope picture of a demonstrator chip, solder side on the left, lens side on the right.

small. Fifth, our ViBO technology ensures a longer product lifetime by eliminating additional interfaces. We have eradicated unreliable glue interfaces that threaten to cause problems during the product's lifetime.

Yet another strength of our ViBO chips is that they have much in common with high-performance microelectronics. This includes the capability to integrate seamlessly with state-of-the-art silicon packaging technology.

The production of our ViBO chips is based on well-established, mass-manufacturing processes used in the semiconductor industry. We define the lens pattern with grey-tone lithography, using a wafer stepper. Thanks to the high accuracy of this approach, millions of lenses are aligned at the wafer level, rather than in subsequent production steps.

A regular lens pattern that's designed for uniform illumination of a field-of-view on a scene is shown in Figure 3. Note that no further optics is needed. With this approach illumination fields can vary from the narrow, such as 20° by 20°, to as wide as more

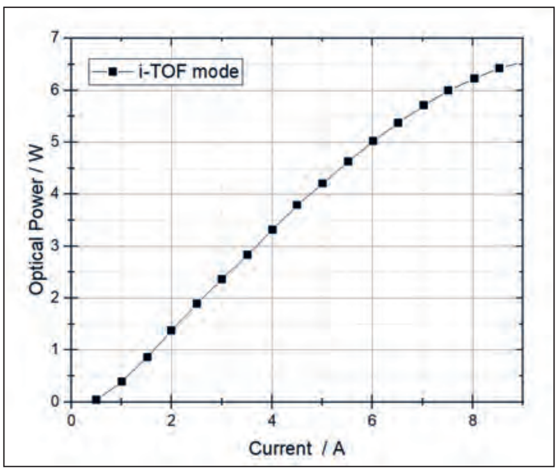


Figure 5. Optical power for different operation currents in a typical indirect time-of-flight operation mode with a pulse burst of 400 µs duration at a frequency of 50 Hz. Measurements are made at room temperature (25°C).

than 100°. It is also possible to tailor the intensity distribution within such a field, allowing more light to be directed towards notoriously dark corners.

Common within the semiconductor industry is bonding with copper pillars. For instance, they are used to create the densely packed connections of a microprocessor. ViBO technology draws on a similar approach (see Figure 3), using lithography to adjust the shape of the pillars. On top of the copper pillar is a solder depot, facilitating the assembly of the chip on ceramic and silicon interposers. Fine pitch patterns support designs with many zones, which can be addressed individually. Many individual VCSELs are grouped into a zone to provide a desired level of power. As the arrangements for the VCSELs and the contacts are independent, and may overlap, this gives more freedom. For example, it allows interlaced and addressing schemes.

Electronic designers also benefit from having both contacts available for addressing – this opportunity enables, for example, the use of a common anode configuration in the driver. Operation in this manner helps to reduce the size of the driver and its power consumption. These merits are particularly welcome in applications with short pulses and high currents, as the driver accounts for a significant part of three key budgets: size, cost and heat.

Turning to a flip-chip assembly that is back-to-back to the driver ensures the shortest connection between the VCSEL and the driver. This configuration is essential for reducing system impedance and enabling the shortest rise and fall times.

The perfect match

Using the ViBO platform, chips can be optimized as flood illuminators for indirect time-of-flight cameras. Indirect time-of-flight operation modes are characterized by bursts of pulses, each burst lasting between 100 µs and 1 ms and delivered at a frame rate of 30 Hz to 60 Hz. These requirements for the pulses, along with that for power, may be met with a chip with a surface area of 1250 µm by 940 µm and a height of just 150 µm (see Figure 4). By integrating several hundred lasers on this chip, it can produce the desired power target of 5 W. The solder bumps are separated by 60 μm to ensure a high cross section for efficient heat removal. This chip also features a regular lens array for beam shaping (see the right hand side of Figure 4), that is buried below the level of the outer rim to prevent damage to the lens array from the pick-and-place tool.

Driven at 6 A, this chip delivers the target optical power for this device of 5 W (see Figure 5). At currents beyond this, output power continues to climb.

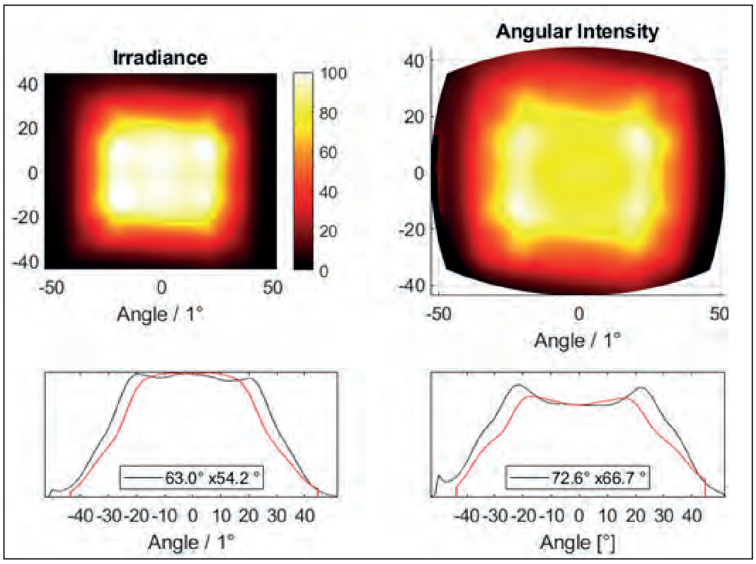
Our ViBO technology enables flood illumination of the scene that is 'laser-safe'. One example of this is a beam profile, shaped by integrated optics, that has an angular intensity in the far field with a full-angle half-maximum of 72° by 67°, and an increasing intensity up to 20° to the optical axis (see Figure 6). Emission by this chip produces a top-hat irradiance profile on a flat wall on which the camera would be looking to achieve a homogenous camera signal over the image.

In comparison, a chip with the same solder interconnect pattern and the same laser arrangement, but without integrated optics, would have a natural divergence of the laser of between 20° and 30° and a profile that tends to dip in the centre. This noteworthy difference highlights the diffusing effect of beam-shaping optics.

To address this shortcoming in the emission profile, state-of-the-art devices include an external diffusor that's based on a polymer or glass, often glued into the package. If this diffuser is removed, damaged or immersed in a liquid-like oil, this causes the beam profile to switch from the wide-angle profile of 70° by 60° to the natural divergence of the laser, just 25°. An almost seven-fold increase in intensity results, typically creating an unsafe condition for laser illumination.

With ViBO chips, the situation is markedly different. As the optic is integrated, it is impossible to remove it without destroying the laser chip. And due to the high refractive index of GaAs, if the chip is immersed in oil, the intensity only doubles. Thanks to this more modest increase, with ViBO much more power can be designed in the application while retaining laser-safe operation under the failure mode of oil immersion. Note that next-generation devices will encapsulate the ViBO chip with a transparent epoxy to protect it and negate the optical impact of immersion in a liquid.

A tremendous benefit of flip-chip assembly is that it allows for direct integration with the driver circuit (developed by our project partner iC-Haus), using only a small current loop and without bond wires. With this approach inductance is low, allowing for the very fast rise-and-fall times and steep top-hat pulse shapes that are ideally suited for time-of-flight applications. This strength is illustrated in Figure 7, which highlights the huge difference in rise and fall time for a 10 ns pulse with a 15 A pulse current. One of the four ViBO chips assembled on a driver circuit can be driven with a very rectangular pulse shape, enabling a rise time of only 0.36 ns.

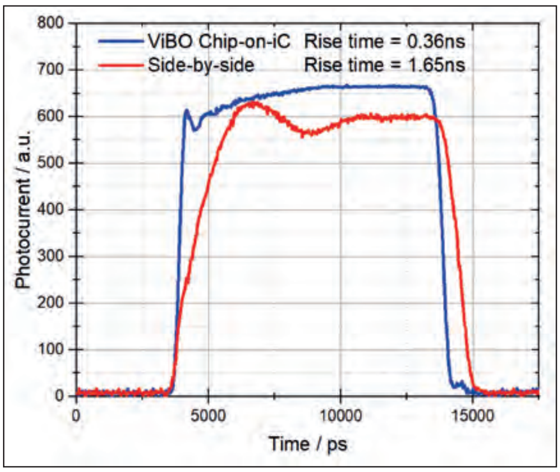


➤ Figure 6. Beam profile: Irradiance on a flat screen (left) and corresponding angular intensity (right).

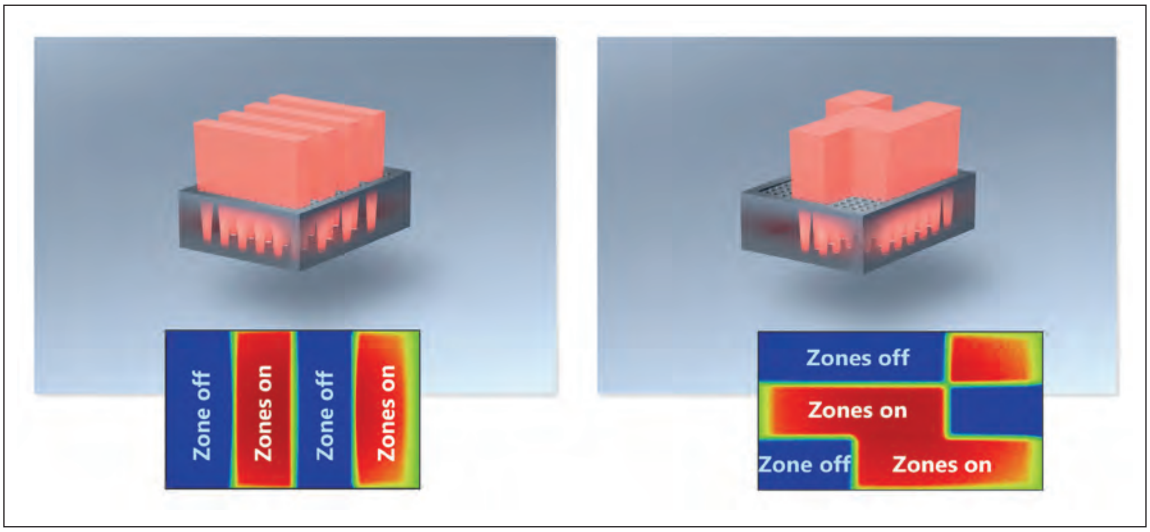
For comparison, we show a state-of-the art VCSEL array in a SMD package, assembled side-by-side to a similar driver in an QFN-package. With this configuration, for the same driving current the rise time (considered to be 10 percent to 90 percent) is 1.65 ns, which is more than 10 percent of the total pulse length. That's a concern, as for direct time-of-flight methods, a short rise time is strongly connected to the optimum measurement precision.

The future of VCSEL design

According to optical simulations, the same top-hat beam profile can be designed for many different field-of-views of 2D and 3D cameras, ranging from 20° to 80°. Even larger angles up to 150° full angle are feasible – we are currently processing demonstrator samples for all these cases.



➤ Figure 7. Pulse shapes of the ViBO chip integrated on a driver and, for comparison, a standard SMD-packaged VCSEL assembled side-by-side to a driver.

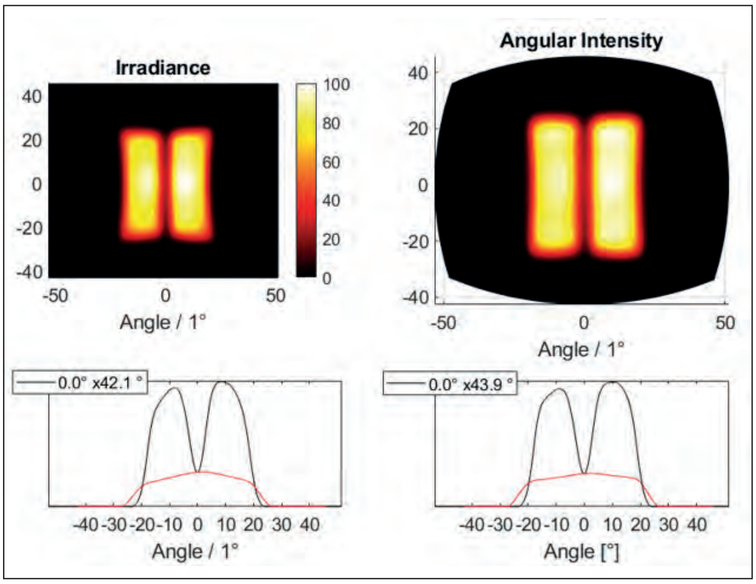


➤ Figure 8. A sketch (top) and simulated beam profiles (bottom) of exemplary laser arrays with several addressable zones to illuminate different regions of interest in the full field of view (60° by 45° in this example).

While uniform illumination of the scene is great, there are times when all the action happens in the centre. For these situations, ViBO technology facilitates addressing individual parts of the VCSEL chip, thus illuminating individual zones on the scene and switching off what is not needed (see Figure 8). As well as a hike in efficiency, this feature helps to save scarce battery power and keep the total system cool.

Further advantages of using the addressable zones of ViBO are that this can replace the mechanical beam scanners used in automotive lidar, as ViBO has no moving parts. This makes the technology more compact and more reliable. And if larger lidar systems are needed for a longer range, they can be formed by combining several ViBO chips, to increase power and resolution.

We have already tested a first example of a zone-illuminator, using a second variant of the ViBO chips.



➤ Figure 9: Beam profile of a ViBO chip illuminating two zones with 15° by 45° and 20° spacing between the zone centres.

This investigation did not allow the possibility to address different zones, because we did not include dedicated routing on the interposer and a multi-channel driver.

The measured beam profile, presented in Figure 9, shows two zones that are clearly separated, and sharp transition regions. Each zone illuminates using a top-hat profile with 15° by 45°, and the zones have a centre-to-centre pitch of 20°.

Our pioneering work demonstrates that ViBO simplifies the way that VCSELs can be deployed. This new product platform allows 3D sensing systems to be safer, more compact and more cost-efficient. We have no doubt that our ViBO technology will replace assembled VCSEL modules and expand the application scope of VCSELs with new possibilities.

Drawing on planar integration, lithographic methods and fine pitch connectors, ViBO technology is bringing VCSEL production far closer to that used for mainstream semiconductors made of silicon. With this approach, ViBO takes care of the light generation, while silicon serves as the sensor and electronic driver. These developments are destined to fuel the growth of the VCSEL, especially in smartphone and automotive applications.

This work has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826600 (project VIZTA) and from the German Federal Ministry of Education and Research under grant agreement 13N14893 (project ALLSTAR). The JU receives support from the European Union's Horizon 2020 research and innovation programme of France, Sweden, Greece, Spain, United Kingdom, Germany, Luxembourg, Latvia, Hungary. Special thanks go to colleagues from our ALLSTAR project partner iC-Haus for the development and assembly of the driver ICs with the integrated ViBO laser chips.

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UVB LEDs: Refining the design

LEDs emitting in the UVB are delivering an increase in efficiency, thanks to the introduction of grading to the hole-source layer and the electron blocking layer, and a thinning of the nickel film below the *p*-type contact

BY M. AJMAL KHAN, NORITOSHI MAEDA, JOOSUN YUN, MASAFUMI JO AND HIDEKI HIRAYAMA FROM RIKEN AND YOICHI YAMADA FROM YAMAGUCHI UNIVERSITY

THERE IS MUCH MERIT in replacing a toxic, mercury-based ultraviolet light source with LEDs emitting in the same spectral range. Recently, LEDs emitting in the UVC, a domain below 280 nm, have attracted much attention, because they can kill Severe Acute Respiratory Syndrome Coronavirus 2 (SARS-CoV-2), as well as disinfecting air, water, food, and surfaces. But there is also a great deal of opportunity for LEDs emitting in the neighbouring UVB band that is at slightly longer wavelengths. Narrow-band sources centred on 310 nm can be deployed for: cancer immunotherapy; the treatment of vulgaris, psoriasis, and atopic dermatitis; and plant growth with enriched phytochemicals (see Figure 1). In addition, emitters centred around the slightly shorter wavelength of 294 nm can be used to prevent plant diseases, attack the tomato mosaic virus, and produce vitamin D_3 in the human body.

LEDs emitting in both the UVC and the UVB are based on AlGaN. This ternary nitride alloy has many promising features, providing reasonable optical and electrical properties, and the capability to form quantum wells with a high internal quantum efficiency. However, when the most common growth technology for making GaN-based LEDs is employed – that is low-pressure MOCVD – challenges are faced. When producing AlGaN-based epistructures on *c*-plane sapphire, it is far from easy to grow a highly conductive, silicon-doped *n*-AlGaN electron-source layer, and a highly transparent, magnesium-doped *p*-AlGaN hole-source layer. Difficulties arise from the large lattice-mismatch of 13.3 percent between c-plane sapphire and the AlN epilayer, as well as the possibility of kinetic separation when forming AlGaN layers with an aluminium composition of 40-45 percent.

At Riken, our team has addressed these issues by switching to a pulsed ammonia technique. This modification allows us to produce a high-crystalline-quality AlN template with a total dislocation density as low as 5×10^8 cm^{-2} on a *c*-sapphire substrate.

We have been working with this technology for several years, using it to produce UVB LEDs. Unfortunately, even with these high-quality templates, devices have an external quantum efficiency of just 6.5 percent and a maximum light output power of 32 mW, according to room-temperature measurements on a bare wafer.

It is of no surprise that these devices are overshadowed by their blue cousins, but it is a concern that these results are inferior to those of UVC LEDs, which can realise external quantum efficiencies of up to 20 percent – although it's worth noting that this superior result is supported by the introduction of micro-patterned sapphire, a flip-chip process, and expensive rhodium-like *p*-electrodes. A farer comparison is to use the result from a bare wafer, which provides an external quantum efficiency of around 8 percent at room-temperature. But even this suggests that the performance of UVB LEDs can be improved, a goal to which we aspire – and are making good progress.

Our recent breakthroughs have come through efforts on several fronts. Part of our success has stemmed from considering the relaxation condition in the *n*-AlGaN electron-source layer underneath the active region. The nature of this relaxation strongly

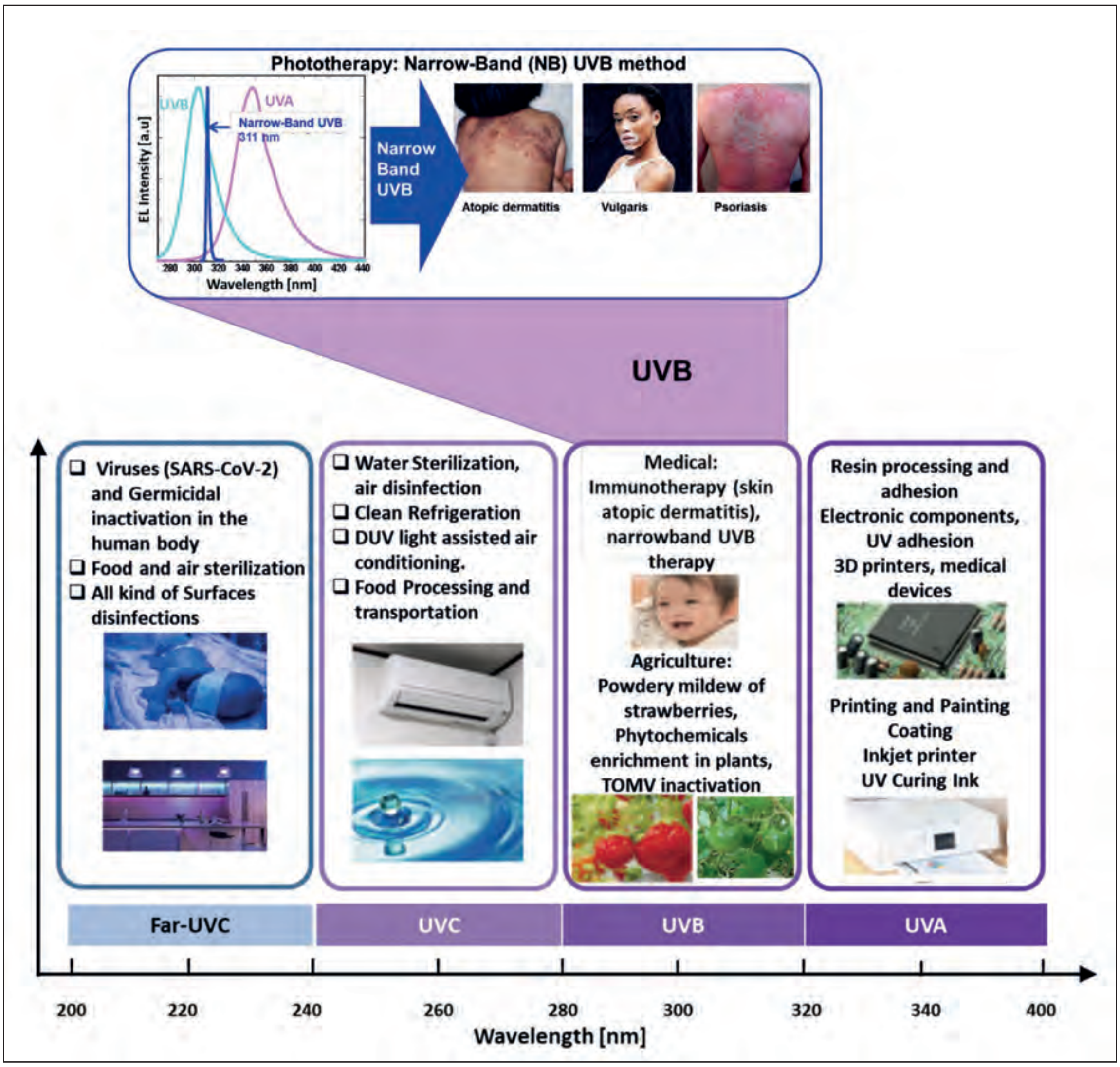
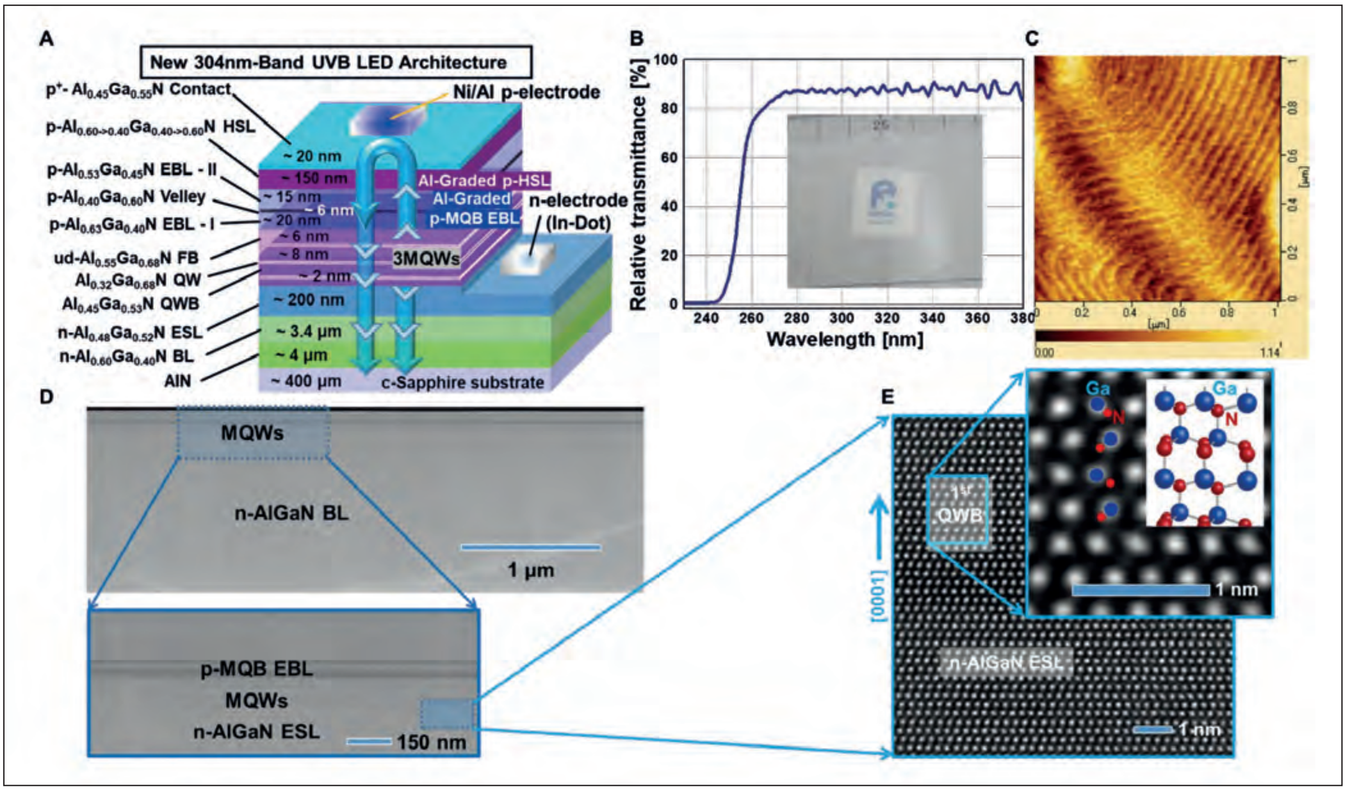


Figure 1. Some critical applications of UV light including UVB emission.



➤ Figure 2. (a) Improvements to the performance of a 304 nm-band AlGaN-based UVB LED have come from grading the hole-source layer (HSL) and the electron-blocking layer (EBL). (b) Optical characterisation of the whole UVB LED (the *p*-AlGaN-based UVB LED crystal wafer is shown in the inset). (c) Atomic force microscopy image of the final *p*-AlGaN contact layer of a UVB LED. (d) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of an LED sample. (e) Magnified HAADF-STEM image of an LED sample taken around the *n*-AlGaN electron-source layer (ESL) and the multiple-quantum well (MQW) region confirms a high-crystal-quality at the atomic level.

influences piezoelectricity, extended defects, point defects, aluminium-alloy fluctuations and non-radiative recombination centres in the multi-quantum wells, which can ultimately degrade the internal quantum efficiency.

We have taken a step forward by realising a high-crystalline-quality in the AlGaN electron-source layer underneath the active region, where we reduced the density of total dislocations to 8×10^8 cm^{-2}. Based on this figure, we can assume that the partially relaxed *n*-AlGaN electron-source layer has the potential to maintain this level of crystalline quality until the final *p*-AlGaN contact layer of the UVB LEDs. Confirming this assumption, we have found at Riken, together with Yamaguchi University, that when we insert a 3.4 µm-thick *n*-AlGaN blocking layer underneath an *n*-AlGaN electron-source layer with a relaxation ratio of about 49 percent, the density of total dislocations is as low as 7×10^8 cm^{-2} (see Figure 2 (a) to (e)). Thanks to this advance, the internal quantum efficiency in UVB active regions is as high as 80 percent, 64 percent and 54 percent, at temperatures of 100 K, 200 K and 300 K, respectively.

Another advance we have made is our development of highly transparent layers, having a relative transmittance of around 90 percent in the UVB. Such a high level of transparency has been realised in our aluminium-graded multi-quantum-barrier electron-blocking layer, our aluminium-graded hole-source layer, and our *p*-AlGaN contact-layer (see Figure 2(a) and (b)). When viewed with atomic resolution, we observe fine steps and terraces on the top *p*-AlGaN contact layer (see Figure 2 (c)).

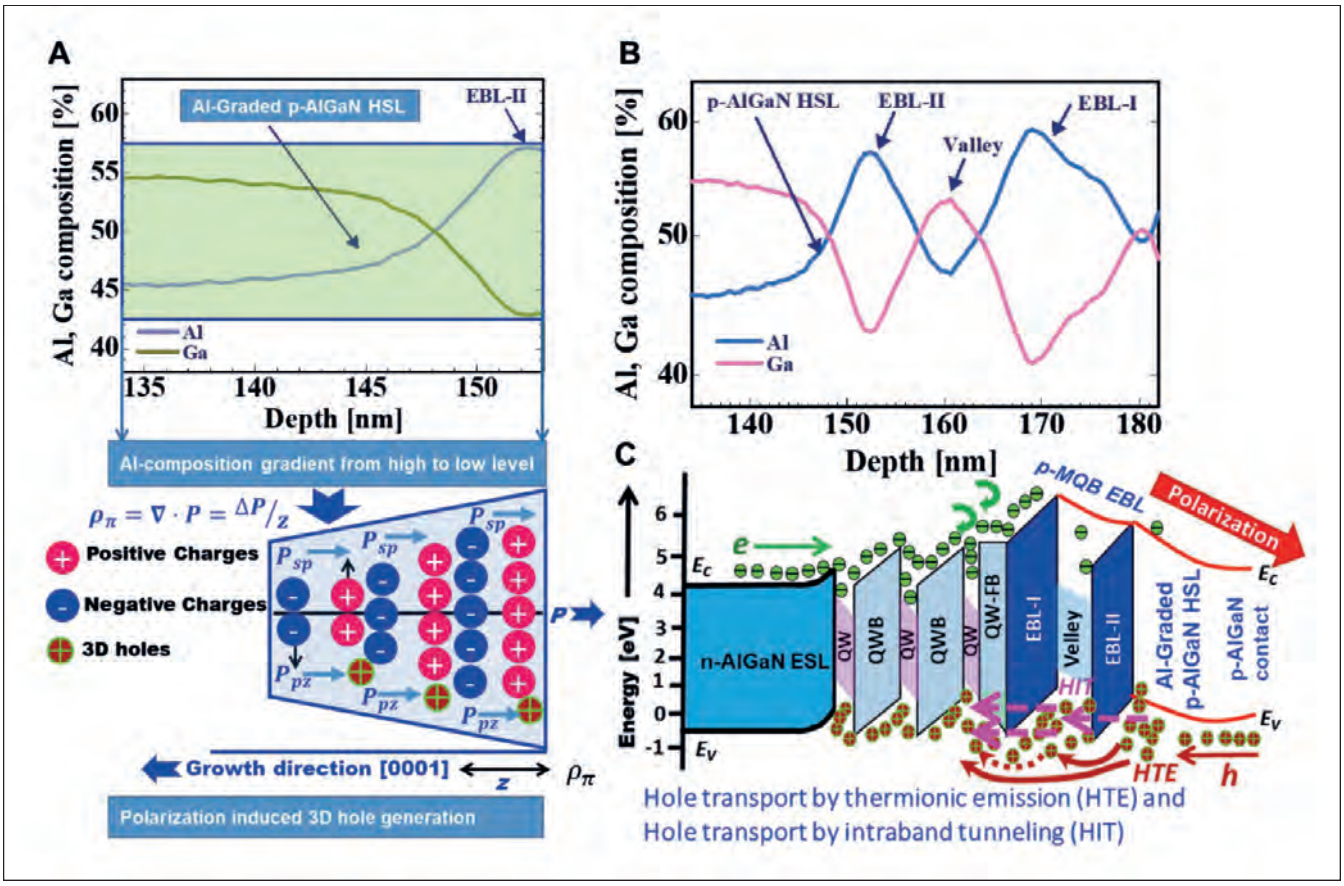
In addition to the advances already discussed, we have made even more important breakthroughs by increasing the hole-injection efficiency and increasing the light extraction associated with the *p*-type electrode. Read on to discover the details of these valuable gains.

Ensuring higher hole injection

It is well-established that the performance of UVB LEDs do not benefit from a fixed composition in the multi-quantum-barrier electron-blocking layer and the AlGaN hole-source layer, as this does not ensure a conductive *p*-type terminal and high hole injection toward the active region. One weakness of this fixed-composition design is the substantial difference between electron and hole transport towards the active region, with highly energetic electrons from shallow donor levels easily overshooting the active region and ending up in the *p*-region of the device. Performance is also hampered by diffusion of unactivated magnesium atoms in the hole-source layer that head towards the active region through the undoped AlGaN final barrier. Due to these deficiencies, present in both UVB LEDs and laser diodes, efficiency droops under high current injection and poor hole injection toward the active region, resulting in relatively poor radiative recombination.

One way to improve the carrier transport in UV devices is to generate a three-dimensional hole level. This approach, pursued by a team from the University of Notre Dame, has led to UVC LEDs that feature a polarisation effect – this comes from adjusting the aluminium composition profile from the *p*-AlGaN hole-source layer to the opaque *p*-GaN contact layer. However, this approach cannot be directly applied to UVB LEDs, as it leads to an unsuitable, opaque *p*-GaN contact layer.

To ensure success, we have modified the design, shifting to a highly transparent pure aluminium-graded *p*-AlGaN hole-source layer that has an aluminium composition ranging from a high concentration to a lower concentration (see Figures 3 (a) and 3 (b)). More recently, we have improved on this, adopting a state-of-the-art strategy of using a



➤ Figure 3. Secondary-ion mass spectrometry (SIMS) profiles of the aluminium and gallium composition in (a) an aluminium-graded *p*-$Al_{0.58}Ga_{0.42}N$ *p*-AlGaN hole-source layer (HSL). The inset illustrates the polarisation-induced 3D hole generation in the aluminium-graded *p*-AlGaN HSL structure, and the bandgap diagram of the graded layer, where the negative polarisation charge field is created by an inclination of the aluminium-profile in the magnesium-doped *p*-AlGaN HSL. When deposition starts from gallium-face crystals and is graded from GaN to AlGaN, the polarisation bound charge is positive. This induces the generation of mobile three-dimensional electrons – it is a vice-versa situation for the generation of three-dimensional holes. The total polarisation, a combination of the spontaneous and the piezoelectric polarisation, may be pictured as charged dipoles in every unit cell of the crystal. Generating 3D holes in an aluminium-graded *p*-AlGaN HSL for UVB emitters is more challenging than it is in a hybrid structure of the aluminium-graded *p*-AlGaN HSL to *p*-GaN, due to the limited availability of the aluminium variation window to keep its transparency. When the composition of the layer is graded with an increasing aluminium mole fraction, the net unbalanced bound polarisation charge is negative. Alongside the [0001]-direction (gallium-polar), the aluminium composition in the *p*-$Al_xGa_{1-x}N$ HSL gradually changes from a high aluminium content of 60 percent down to low aluminium content of 40 percent (see both (a) and (b)) and the polarisation interface charge is negative. Such polarisation-assisted interface negative charges induce a movable 3D hole gas, employed in the new LED design. (b) SIMS spectra of the aluminium and gallium composition in magnesium-doped *p*-multi-quantum-barrier (MQB) electron-blocking layer (EBL) including *p*-AlGaN HSL (new LED). (c) Estimated energy-band diagram of the newly designed *p*-AlGaN-based UVB LED (new LED). The aluminium composition of the *p*-$Al_xGa_{1-x}N$ HSL of the UVB LED gradually decreases alongside the [0001]-direction (growth direction). This may enhance the 3D hole generation near the EBL-II of the *p*-MQB EBL.

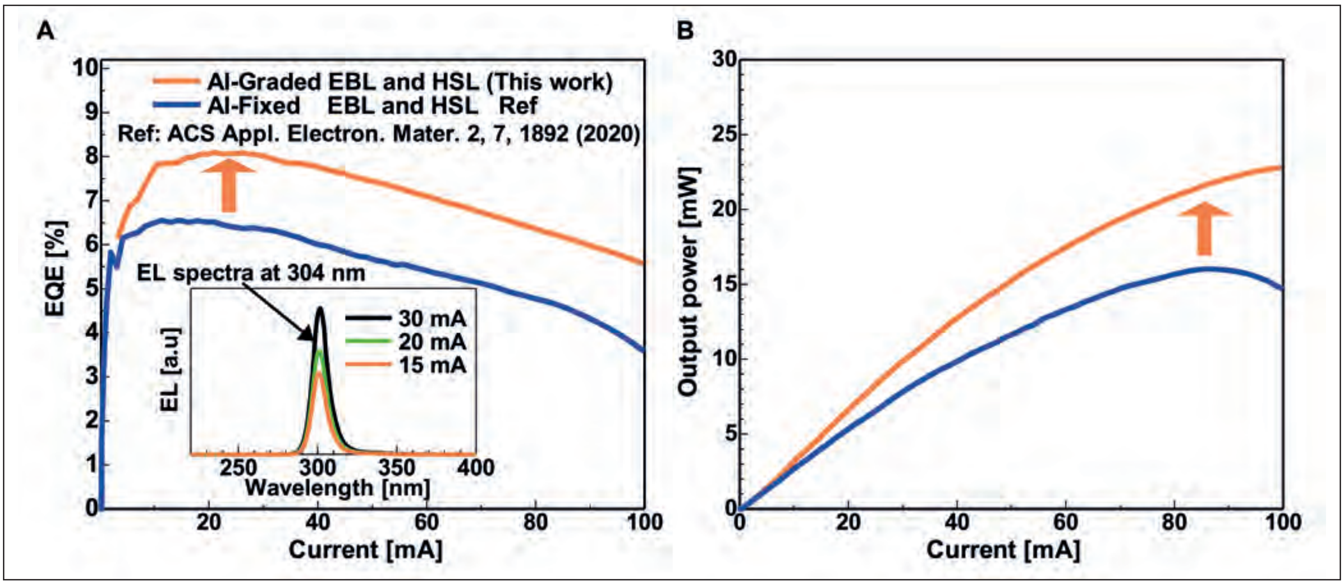


Figure 4. (a) The external-quantum efficiency of a 350 µm by 350 µm UVB LED emitting in the 304 nm-band improves with grading of the electron-blocking layer and the hole-source layer. (b) The light output rolls over in the reference design, but continues to climb in the superior variant.

moderately magnesium-doped, aluminium-graded *p*-type multi-quantum-barrier electron-blocking layer in our UVB LEDs. This design delivers three-dimensional hole generation and hole transportation via intra-band tunnelling from the aluminium-graded *p*-AlGaN hole-source layer toward the active region.

The generation of our three-dimensional hole gas originates in the gallium-polar structure, which has a net negative charge at the interface between two layers of AlGaN with different compositions. Bound charges create a built-in electric field, leading to energy-band bending that would be greater than the bandgap of the semiconductor layer if left uncompensated. To neutralise these bound charges, negative polarisation charges and holes are field-ionised from neighbouring deep magnesium-acceptor atoms. This generates a high-density mobile 3D hole gas (see Figure 3 (a), which includes a more detailed explanation of this phenomena). By adopting this approach, we have increased hole concentration to around 3×10^{16} cm^{-3}, reduced resistivity to typically 22 Ω cm, and realised a room-temperature hole mobility of 9.38 cm^2 V^{-1} s^{-1} in our moderately polarised hole-supplying layer, which has AlGaN graded from a content of 60 percent to 40 percent.

As well as improving the supply of holes, we have refined their transport to the active region by optimising the design of the electron-blocking layer. In previous work, we had introduced a pair of multi-quantum-barrier electron-blocking layers. They both had the same level of aluminium composition employed in our initial design. With our latest UVB LED we have switched to multi-quantum-barrier electron-blocking layers with a graded aluminium content (see Figure 2(a) and Figure 3(b)).

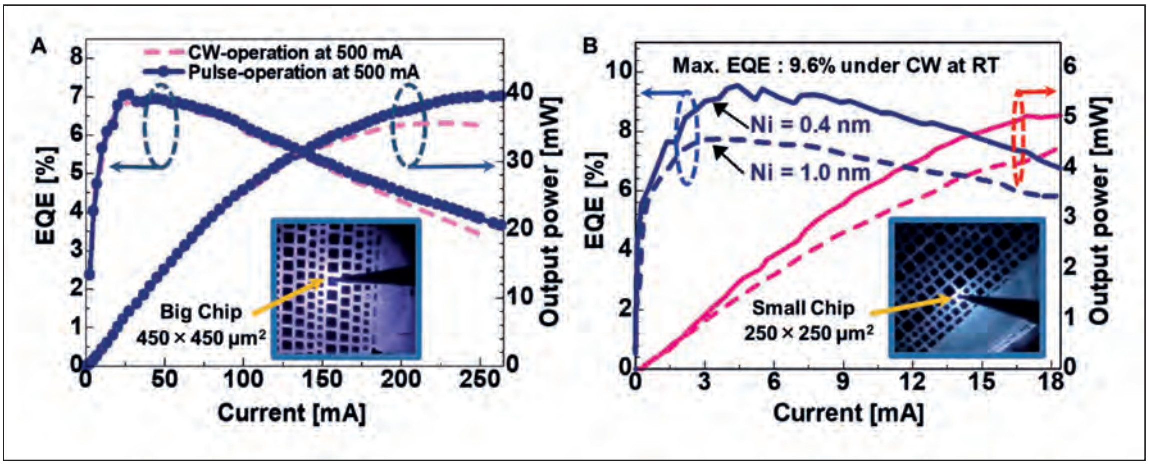


Figure 5. Characterisation of UVB LEDs with a graded electron-blocking layer and the hole-source layer under continuous-wave (CW) and pulsed operation at room temperature (RT), using bare-wafer measurements. (a) Current versus output power (I–L), and current versus external quantum efficiency (I–EQE) (the inset shows an image of a real UVB LED with a chip size of 450 µm by 450 µm during operation (b). I–L and I–EQE characteristics, highlighting the benefit of a thinning of the nickel layer (an image of a real, small-sized UVB LED during operation is shown in the inset).

With this new design, the electron-blocking layer, which is nearer to the active region, has a slightly higher aluminium content than its sibling. This architecture ensures effective blocking of high-energy electrons while supporting hole injection through intra-band tunnelling after the generation of the two-dimensional gas at the interfaces between the electron-blocking layers and the 'valley' layer between them. By selecting a relatively small bandgap for the valley layer, holes are injected into this layer from the hole-source layer by thermionic emission and intra-band tunnelling, before being easily transported to the active region.

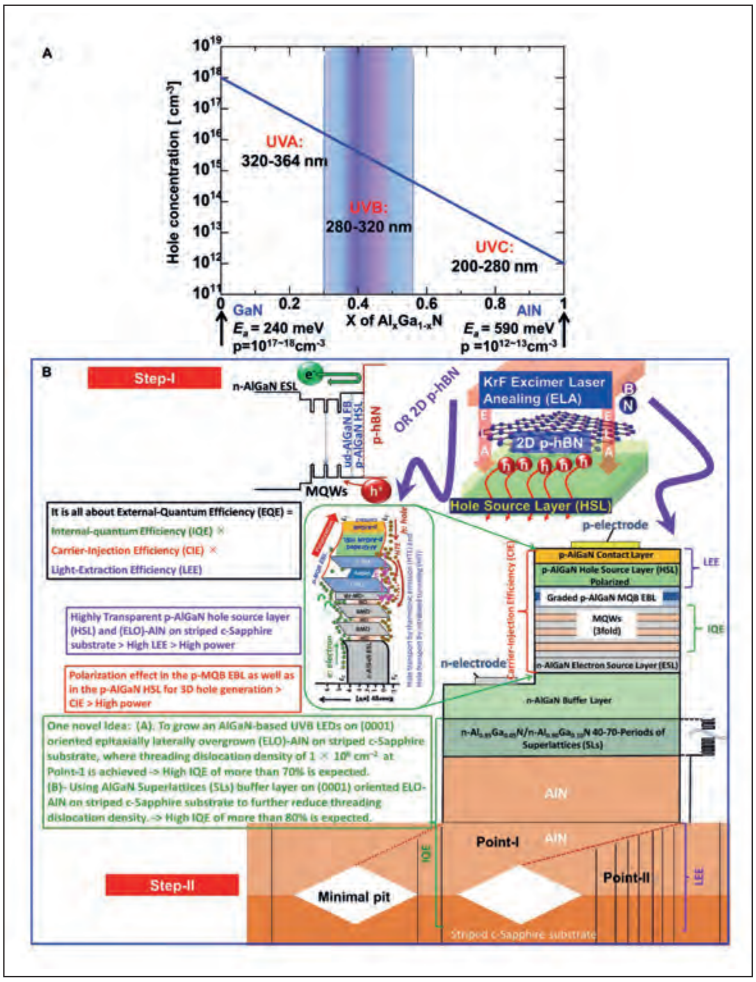
To experimentally investigate the influence of grading the electron-blocking layers and hole-supplying layers, we have fabricated UVB LEDs, which feature a *p*-electrode of 1 nm nickel, followed by 200 nm of aluminium. We have compared this to our best reference LED, which includes electron-blocking layers and hole-supplying layers with a fixed aluminium content.

Our new device produces a single electroluminescence peak at 304 nm with a full-width at half-maximum of around 10 nm (see Figure 4 (a)). For our chip that's roughly 350 μm by 350 μm in size, room-temperature bare-wafer measurements reveal a continuous-mode output power of 23 mW, up from 18 mW for the reference (see Figure 4 (b)). Additional encouraging results are a fall from 36 V to 23 V in the operating voltage for a 20 mA drive current, and an increase in maximum external quantum efficiency from 6.4 percent to 8.2 percent (see Figure 4 (a)).

Perfecting the *p*-electrode

Aluminium is known to be a good choice for the *p*-electrode, due to its high reflectivity. However, the underlying nickel film can compromise performance by absorbing UVB light and increasing the operating voltage. To address these issues, we have investigated devices with a thinner nickel layer, reducing this from 1-2 nm to just 0.4 nm, while employing an aluminium thickness of 200 nm. Devices have been fabricated with sizes of around 250 μm by 250 μm, 350 μm by 350 μm, 400 μm by 400 μm, and 450 μm by 450 μm (photos of the *p*-electrodes are shown in Figures 5 (a) and (b)).

Room-temperature bare-wafer measurements on the smallest chip reveal that reducing the thickness of the nickel film leads to an increase in the external quantum efficiency from 7.8 percent to 9.6 percent. Driven at 18 mA, this chip produces a 5 mW output. For the biggest chips, the output is as high as 40 mW, under both continuous-wave and pulsed operation. We attribute these excellent results to a thinning of the nickel layer and the introduction of aluminium grading to the electron-blocking layer and the hole-source layer.



➤ Figure 6. (a) Hole concentration versus aluminium composition in the *p*-AlGaN hole-source layer (HSL). (b) An experimental roadmap to grow *p*-type hexagonal (h) BN on a *p*-AlGaN HSL (Step-I) on AlGaN multiple quantum wells (MQWs) of UVB LEDs, and assisted by excimer laser annealing (ELA) treatment. Step-II is to grow highly efficient AlGaN superlattice-based UVB LEDs on epitaxial layer overgrowth (ELO) AlN/striped *c*-sapphire substrates.

We have confirmed the benefits of thinning the nickel layer with optical modelling, which considers an aluminium thickness of 200 nm. Simulations show an increase in light extraction of 30 percent. At normal incidence, our new design with 0.4 nm-thick nickel has a reflectance of 85 percent, while that with 2 nm-thick nickel has a reflectance of just 76 percent. As well as the higher reflectance, a thinning of the nickel trims the contact resistance. According to our calculations, if our new design were accompanied by a standard UVB LED package, a nano-patterned sapphire substrate, lenses, a photonic crystal structure, a rhodium-based *p*-electrode, a heat sink, and a flip-chip architecture – all have been adopted for UVC LEDs – then an external quantum efficiency of 21 percent should follow.

Additional opportunities

The external-quantum efficiency is the product of three factors: the internal quantum efficiency, the

For the internal quantum efficiency and the light extraction efficiency, we are targeting values in excess of 70 percent and 17 percent, respectively. One optimistic idea of ours for reaching these milestones is to grow a highly transparent *p*-AlGaN hole-source layer and an epitaxial-layer-overgrowth AlN template on a striped *c*-plane sapphire substrate

carrier-injection efficiency, and the light-extraction efficiency. We have plans for improving all three.

To increase the carrier-injection efficiency, we know that we need a hole concentration of approximately 3×10^{18} cm^{-3} and shallow acceptor energy levels in the *p*-AlGaN hole-source layer (see Figure 6 (a)). We have tried to tackle this challenge by applying an excimer laser anneal to a lightly polarized *p*-AlGaN hole-source layer. This has resulted in a hole concentration of approximately 2.6×10^{16} cm^{-3}, a hole mobility of around 9.6 cm^2 V^{-1} s^{-1} and a resistivity of 24.39 Ω-cm. While these figures are encouraging, such a *p*-AlGaN hole-source layer is incapable of matching the number of holes to the number of electrons that are delivered to the active region.

What we need to do to bolster hole injection is to switch to a new heterostructure with a new wide-bandgap material that has a highly activated *p*-dopant. Our replacement must satisfy three criteria: it must realise epitaxial growth on AlGaN and AlN; it must have a bandgap profile that aligns with AlGaN and AlN, to assist the blocking of high-energy electrons and promote hole-injection toward the active region; and it must have a lower acceptor energy level and a higher hole density than the aluminium-rich AlGaN hole-source layer (see Figure 6 (b)).

Satisfying all these conditions is hexagonal *p*-type BN. According to theoretical considerations, if we can place impurity dopants at the interstitial sites in hexagonal BN, this will create a shallow acceptor energy level of 30 meV with high hole generation in the valence band. Due to this promise, we are planning to fabricate a new form of UVB LED that features *p*-type hexagonal BN and a polarized *p*-AlGaN hole-source layer, formed by treating with an excimer laser to activate holes. We are aware that it will be challenging to produce this structure by low-pressure MOCVD at a high growth temperature.

For the internal quantum efficiency and the light extraction efficiency, we are targeting values in excess of 70 percent and 17 percent, respectively. One optimistic idea of ours for reaching these milestones is to grow a highly transparent *p*-AlGaN hole-source layer and an epitaxial-layer-overgrowth AlN template on a striped *c*-plane sapphire substrate. Such a device could be produced by growing an AlGaN-based UVB LED on (0001)-oriented epitaxially laterally overgrown AlN on a striped *c*-plane sapphire substrate. We have already shown that AlN formed by this approach has a threading dislocation density of just 1×10^6 cm^{-2}, suggesting that the active region could have an internal quantum efficiency as high as 80 percent.

Another idea of ours is to realise an even lower threading dislocation density in the active region by turning to an AlGaN superlattice buffer layer on (0001)-oriented epitaxial-overgrown AlN on striped *c*-plane sapphire. This approach should prevent threading dislocations from penetrating through the AlN buffer (see Figure 6 (b)).

Improvements can also come from introducing the standard flip-chip package, featuring a heat management module, hermetic sealing and a specially designed lens for light concentration. We have made much progress with our compositional grading of hole-source layers and electron-blocking layers, and the thinning of the nickel film – but there is still much more to explore, as we continue to refine the design of the UVB LED.

FURTHER READING

- M.A. Khan *et al*. Achieving 9.6% efficiency in 304 nm *p*-AlGaN UVB LED via increasing the holes injection and light reflectance. Sci Rep **12** 2591 (2022)
- M.A. Khan *et al*. External Quantum Efficiency of 6.5% at 300 nm Emission and 4.7% at 310 nm Emission on Bare Wafer of AlGaN-Based UVB LEDs. ACS Appl. Electron. Mater. **2** (2020)
- M.A. Khan *et al*. Impact of Mg level on lattice relaxation in a *p*-AlGaN hole-source layer and attempting excimer laser annealing on *p*-AlGaN HSL of UVB emitters. Nanotechnology **32** 055702 (2021)

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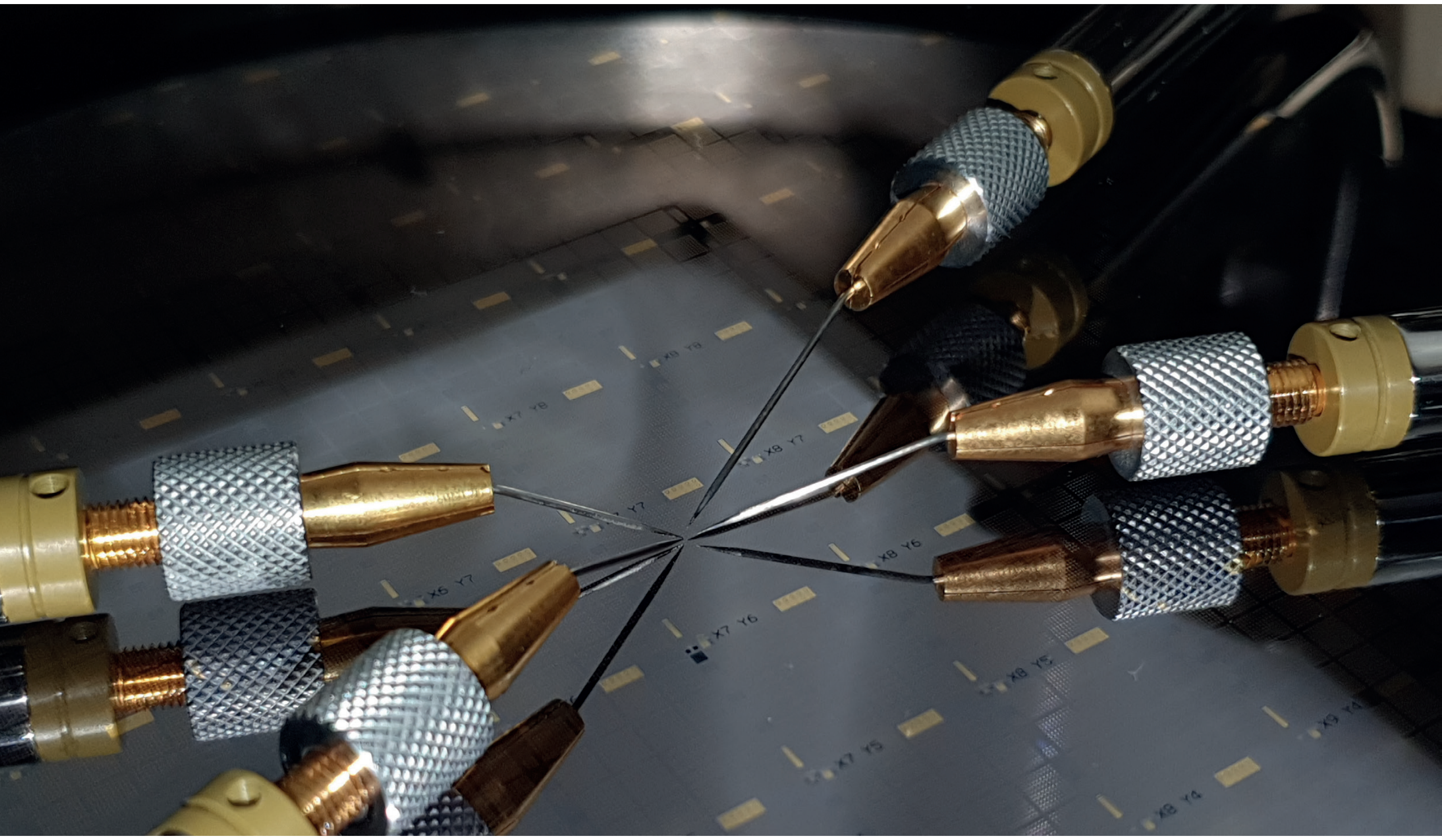


Faster feedback refines VCSEL production

A novel wafer-scale 'quick-fab' process aids VCSEL manufacture by providing rapid device feedback

BY SAMUEL SHUTTS FROM CARDIFF UNIVERSITY

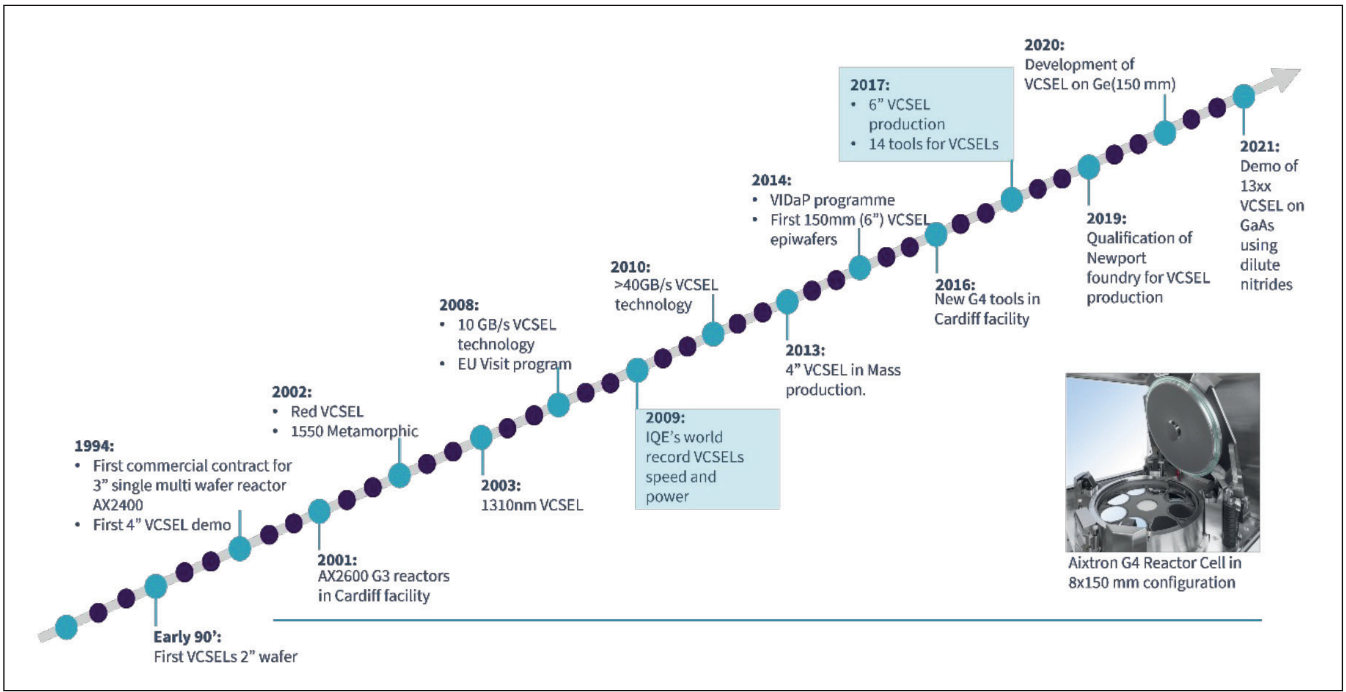
DEMAND FOR THE VCSEL shows no sign of slowing. Sales took off with deployment in wireless data communication, reached a new high when its use extended to face-and-gesture recognition systems in smartphones, and will jump again through the roll out of lidar systems in autonomous vehicles. Due to this continuous ramp in demand, VCSEL manufacturers are under increasing pressure to ship more devices.

To cater for this growing demand, makers of GaAs-based VCSELs have moved to ever larger wafer sizes – a move that as well as increasing volume, addresses the call to drive down the cost per device. As far back as 1994, the world's leading supplier of epiwafers, IQE, signed its first commercial contract for 75 mm wafers, and demonstrated its capability to produce these heterostructures on 100 mm wafers – although it wasn't until 2013 that mass-production kicked-off on this large size. Since then progress has accelerated. 150 mm wafers that are capable of providing 200,000 devices were introduced in 2014, and this May IQE introduced the world's first commercially available 200 mm VCSEL wafer, enabling further expansion of the sensing market.

The need for quick-fab

Alongside increases in the production throughput of the VCSEL, realised partly through the migration to larger wafers, there has been a tightening of tolerances to meet the more stringent demands of emerging applications. Due to this state-of-affairs, there is an ever-increasing need for device-level characterisation that delivers a rapid assessment of wafer uniformity and exposes any drift occurring during a manufacture cycle. Such a service complements the production-line characterisation toolkit by providing active device data.

Our team, a collaboration between Cardiff University and IQE, has striven to develop such a service through a project entitled ATLAS, Advanced



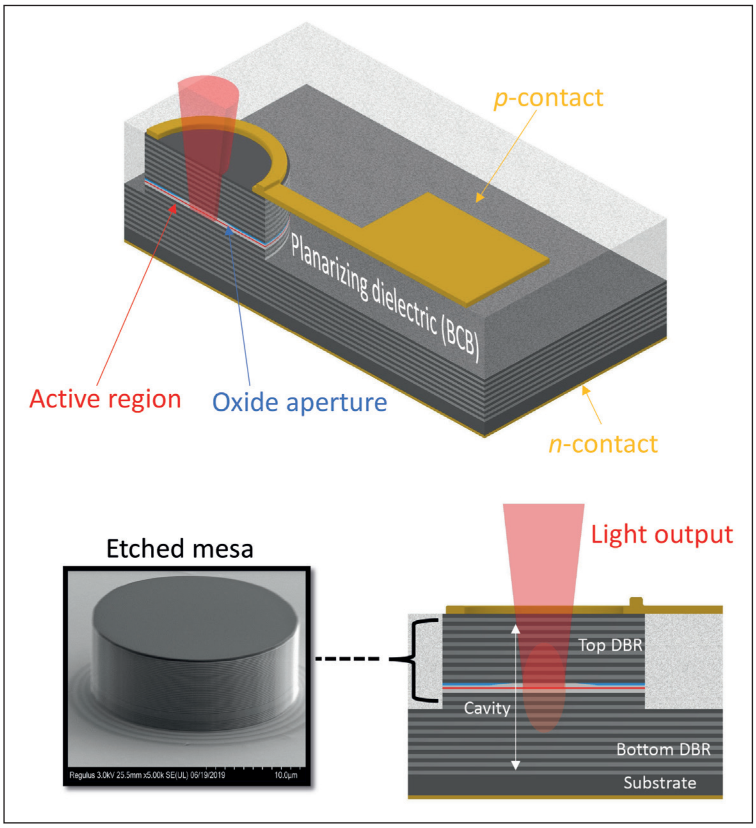
manufacturing Techniques for semiconductor LASers. This effort has focused on drastically reducing the time taken to fabricate a conventional VCSEL structure by utilising a simplified strip-backed process, which can provide fast feedback to production teams. The aim has been to complete fabrication within 24 hours.

The proposed 'quick-fab' VCSELs are not intended for packaging as individual chips, employed in end-user technology. However, they do need to be compatible with automatic wafer-level probing, which enables the mapping of various characteristics, including the VCSEL's emission spectrum and its optical output power as a function of current and voltage. From these measurements it is possible to extract key characteristics for this class of laser, such as its threshold current (the minimum current required to realise laser action), its power-conversion efficiency and its peak wavelength.

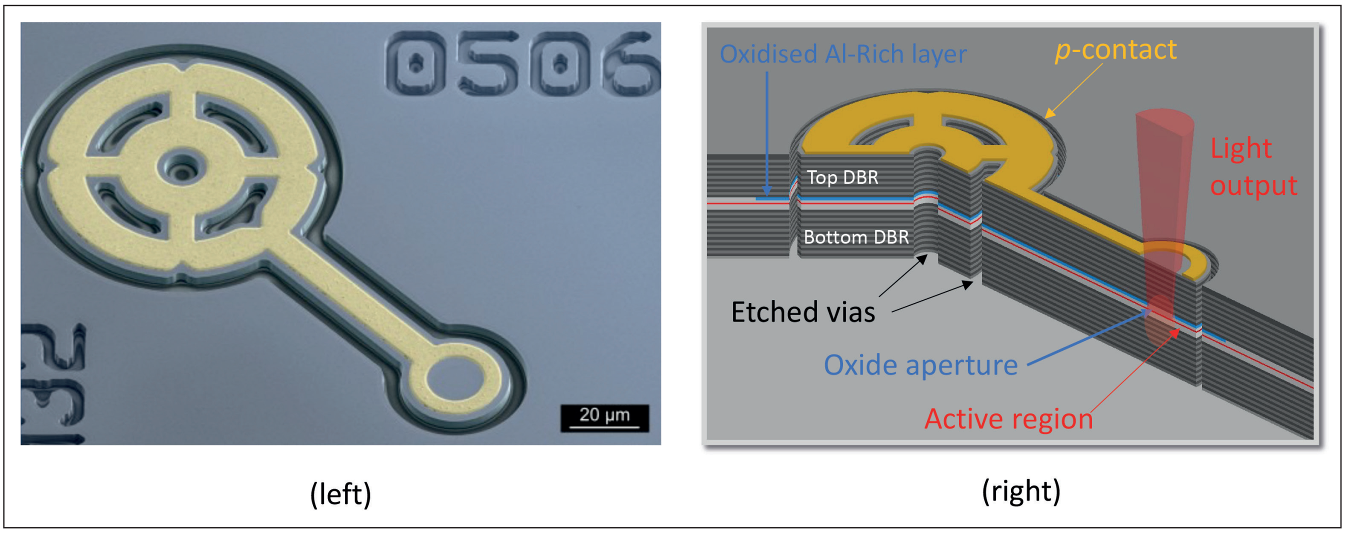
An additional benefit provided by a quick-fab service is that it allows VCSEL manufacturers and their customers to develop new products more efficiently. VCSELs are complex structures, comprising up to 200 or more layers, each with a carefully controlled composition and a thickness ranging from 1 µm down to as little as 4 nm. While simulation software supports the design of a new VCSEL, to satisfy an intended application this often has to be accompanied by a design-of-experiment. To optimise device performance, engineers tend to use several reiterations of design, epi-wafer growth and VCSEL fabrication. Our VCSEL technology quick-fab supports such endeavours, providing process monitoring and aiding R&D and product development.

Note that the benefits of VCSEL quick-fab are not limited to producing devices for large consumer markets. This form of fast-feedback also has a role to play in supporting the emergence of specialist atomic sensor technologies, such as miniature

➤ Figure 1. IQE's VCSEL production timeline. Courtesy of IQE.



➤ Right: Figure 2. Cross-section of a typical VCSEL design, with SEM image showing an etched mesa structure.



➤ Figure 3. (left) Isometric SEM micrograph of a fabricated VCSEL quick-fab device taken using a Hitachi SU8320 housed in the Cardiff's ICS cleanroom. False colour rendering has been applied to illustrate the electrical contact pad. (right) An accompanying schematic of a device cross-section.

atomic clocks, magnetometers and quantum gyroscopes. All these technologies call for stringent VCSEL specifications. For example, caesium-based atomic sensors require stable single-mode sources targeting atomic transitions at 894.6 nm and 852.347 nm. Hitting these transitions requires some current and temperature tuning, but ideally this is minimal, to ensure high efficiency and lessen the impact on the environment of the accompanying caesium vapour cell.

There is yet another benefit of VCSEL quick-fab, related to a predominant design challenge. With this class of laser it is crucial to have a healthy overlap between the optical gain spectrum and the resonant cavity mode. That's because the VCSEL cannot operate over a wide range; rather, it is constrained to emit at a particular wavelength by virtue of its optical design. To ensure efficient operation, the peak of the gain has to align with the cavity mode. This situation is analogous to shining a torch through a keyhole, where alignment is essential to enable efficient transfer of light. Sub-optimal alignment can be compensated

➤ Figure 4. Microscope image showing oxidation calibration mesas after oxidation, with the central dark spot identifying the aperture (unoxidised region).

by increasing the brightness of the torch, but this comes at the expense of consuming more energy.

Complicating matters, both the peak of the gain spectrum and the location of the cavity mode shift with temperature, and they do so at different rates. A prudent designer accounts for this, targeting the gain peak and cavity resonance to coincide at the designed temperature and operating current. Quick-fab VCSELs can speedily determine if this is actually the case.

The quick-fab concept

One of the attractive features of the VCSEL is the relative ease of large-scale manufacture. As all the light is emitted vertically from the surface, engineers undertake on-wafer testing, rather than cleaving material into individual chips, as is the case with edge-emitting lasers. However, fabricating VCSELs is not that simple. It is certainly not trivial to confine light and current in localised regions – and these are pre-requisites for efficient operation.

The widely adopted approach for ensuring localisation of electro-optical processes is to etch a mesa structure into the epiwafer to a depth that exposes an oxidation layer buried within the VCSEL structure (see Figure 2). This layer, formed from aluminium-rich AlGaAs, is partially oxidised to form an aperture or window in the centre of the mesa that defines the path for current flow. One of the merits of this approach is that it also guides light within the same region, thanks to the resulting refractive index profile.

Unfortunately, in a conventional VCSEL, it is not possible to connect an electrical wire or probe directly to the mesa, because it is too small. Due to this, the mesa is first 'planarized' with an electrically insulating material, before a feed metal interconnect and a relatively large metal contact pad are deposited. These steps eat up time. To enable VCSEL quick fab, an approach must be taken that mitigates planarization and subsequent metallisation.

Our solution involves defining a mesa structure by etching the semiconductor epiwafer, an approach that's similar to that employed for making a conventional VCSEL – but in our case we leave portions unetched, which are subsequently used to support the electrical interconnect and contact pad. We ensure that current only flows through the VCSEL aperture by etching vias to expose the aluminium-rich layer, which is subsequently oxidised in all regions, except for the area prescribed by the VCSEL aperture. Following this, we added a topside metal *p*-contact and back-side *n*-contact, before annealing to produce low-resistance ohmic contacts (see Figure 3 for an SEM image of our device and accompanying schematic showing a cross-section).

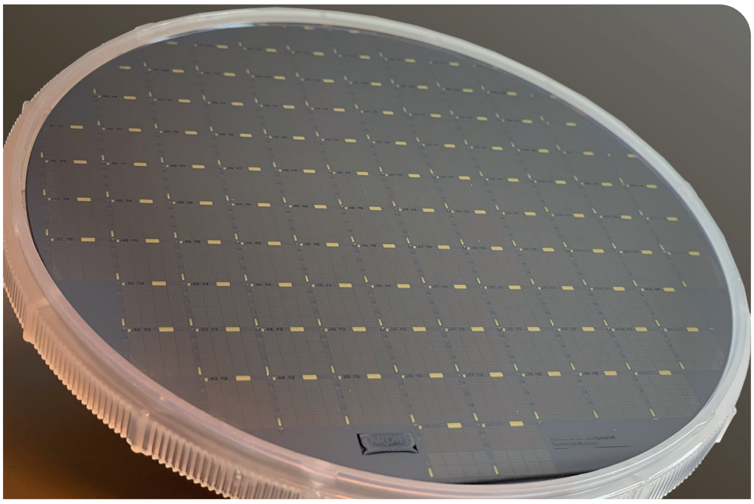
With our approach the number of steps required to produce a VCSEL is slashed from around ten to just four. Thanks to this, VCSEL quick-fab trims fabrication time by 60 percent.

For a given mesa size, the size of the oxide aperture tends to vary across the wafer. Differences in dimensions arise primarily from: compositional non-uniformities in the aluminium-rich layer, occurring during epitaxial growth; and variations in the oxidation conditions across the wafer, namely temperature. The implication is that VCSEL performance varies across a wafer.

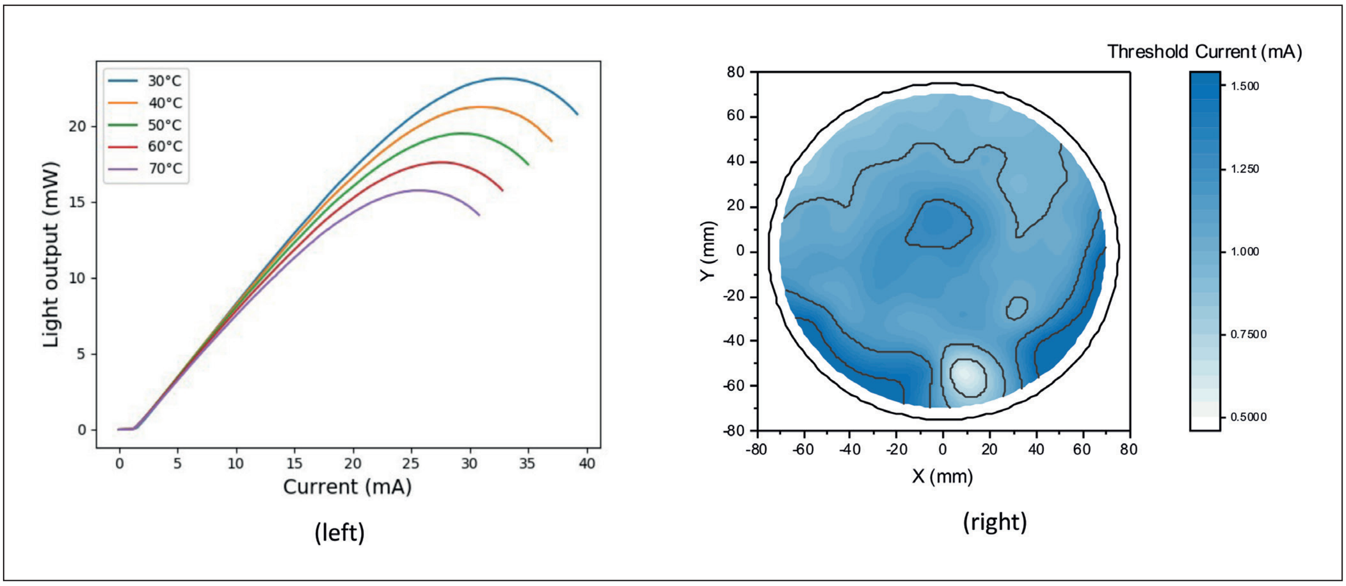
VCSEL quick-fab offers insight into this variation. What's more, by using a range of mesa sizes, the influence of variations in fabrication, such as differences in oxidation, can be disentangled from changes in device performance caused by epi-wafer growth conditions. Obviously, this is only possible when the oxidation extent across the wafer is known. We uncover this by incorporating oxidation test-structures into the quick-fab mask design (an example is shown in Figure 4, following the oxidation step). Taking this approach allows us to accurately determine the extent of oxidation via microscopy. When metal contacts are applied, we can confirm the extent of oxidation by electrical conductance measurements.

We have applied our versatile VCSEL quick-fab process to a variety of epitaxial structures. One example is a 150 mm wafer that's been grown by IQE to its 940 nm emission generic design, and been processed within the Institute for Compound Semiconductors cleanroom at Cardiff University. Full processing of one of these wafers yields more than 150,000 quick-fab VCSELs, as well as various test structures, including those for oxidation calibrations and transmission-line measurements (see Figure 5 for an image of this wafer).

With our Quick-fab VCSELs, we can map the power-current characteristics across the wafer. From this, it's possible to determine the power-conversion



➤ Figure 5. Photograph of a fabricated 150 mm VCSEL quick-fab wafer, processed in Cardiff's ICS cleanroom facility.



➤ Figure 6. Power-current characteristics of a 16 µm aperture VCSEL from 30 to 70 ˚C (left) and contour image showing variation in threshold current across a 150 mm wafer.

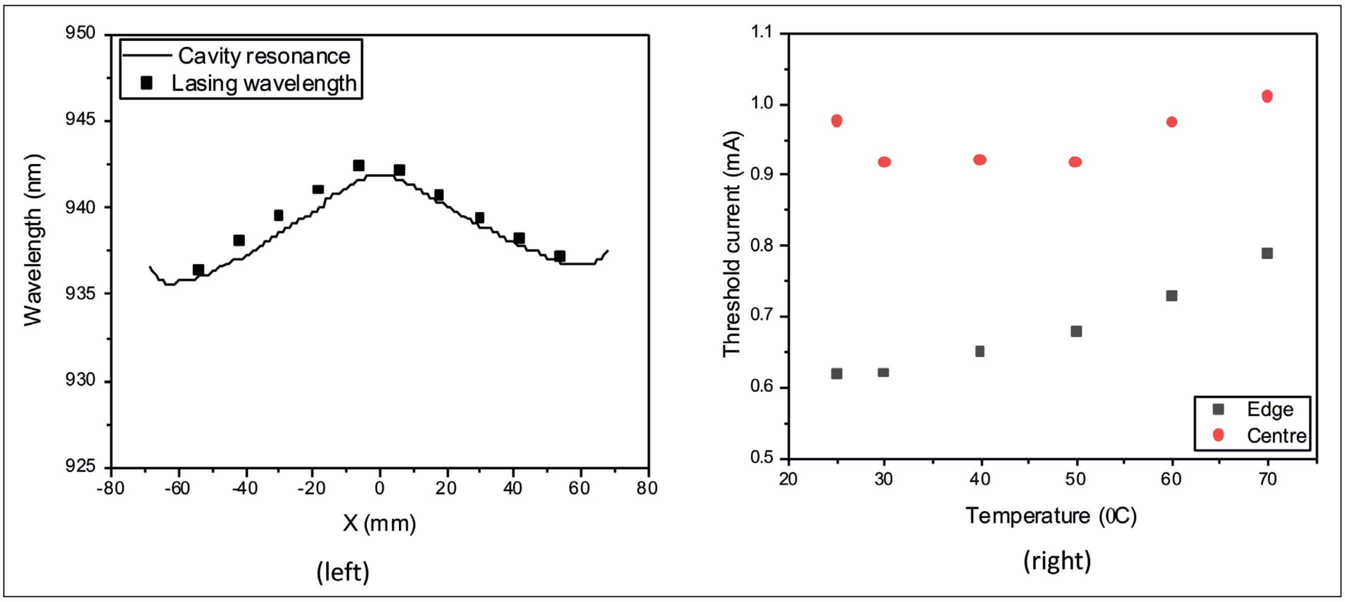


Figure 7. (Left) Comparing lasing wavelength (squares) with cavity resonance at different positions across the wafer. (Right) Threshold current versus temperature for VCSEL devices at the wafer's centre and its edge.

efficiency, the thermal rollover and the threshold current. As the oxidation extent is known at multiple points across the wafer, we are able to calculate current density.

An example of the power-current curves for a quick-fab VCSEL with a 16 μm aperture is shown in Figure 6 (left) for a temperature range of 30 - 70 °C. The wafer-scale colour map in Figure 6 (right) shows the variation in threshold current, which is concomitant with the change in oxidation extent we observe across the wafer.

Plots of the lasing wavelength of the quick-fab VCSELs and the cavity resonance wavelength show a similar trend across the wafer, albeit with a slight increase in wavelength for the quick-fab VCSELs (see Figure 7, left).

This shift to longer wavelengths is caused by Joule-heating, which must be considered in applications that are sensitive to operating wavelength, such as atomic sensors. VCSEL designers need to account for an increase in lasing wavelength of approximately 0.5 - 1 nm mA^{-1}, as well as variation due to ambient temperature of around 0.07 nm per °C. Drawing on a reference (see Figure 7, right), we have compared VCSELs with similar aperture diameters formed from the centre and the edge of a wafer, and observed a variance in the threshold current for a given temperature, with the minimum occurring at a different temperature.

This observation offers an insight into the detuning between the gain-peak and the cavity resonance wavelength, and how this changes with temperature – that's a significant advantage using quick-fab VCSELs, which provide information that cannot be obtained with standard epiwafer characterisation used in a production line.

Armed with quick-fab data, the designer, epiwafer producer, or end-user can determine whether the epi-design is optimised for the operating temperature of the intended application, and be informed of the expected variation in device performance from different regions of the wafer.

We are continuing to advance the capability and versatility of our VCSEL quick-fab progress. It is currently being used to assess epiwafers for making VCSELs for use in atomic clocks, as well mapping the performance of VCSELs grown by IQE on germanium substrates, which boast improved uniformity compared with GaAs substrates, due to a reduction of strain-induced wafer-bow.

Project ATLAS is supported by the Welsh Government's SMART Expertise programme and is part financed by the European Regional Development Fund (ERDF). Support also provided by EPSRC Future Compound Semiconductor Manufacturing Hub (EP/P006973/1) and an EPSRC-funded iCASE PhD studentship, co-sponsored by IQE plc. (EP/T517525/1) Fabrication has been carried out in the Institute for Compound Semiconductors and more details can be found on p. 35 of this issue.

FURTHER READING

- J. Baker *et al*. IEEE Photonics Journal 10.1109 JPHOT.2022.3169032

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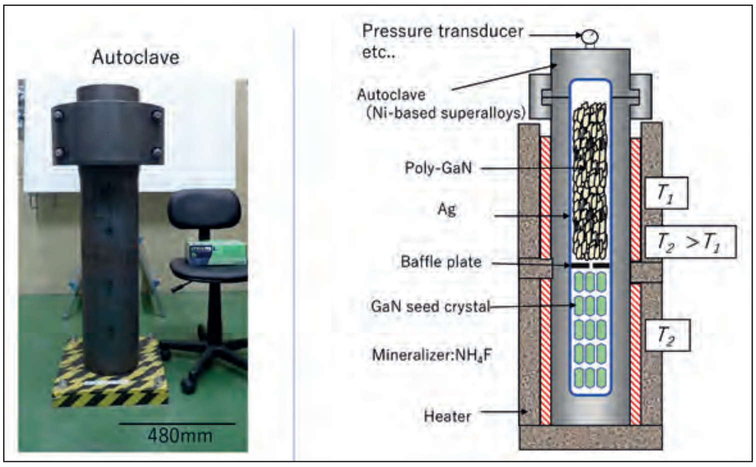
Acidic ammonothermal growth promises cheaper GaN

Switching from the conventional form of ammonothermal growth to that using acidic mineralisers offers a hike in the throughput of GaN crystal growth

DEVISING a great process for the commercial production of GaN substrates is far from easy. The incumbent technology, HVPE, delivers reasonable throughout at the expense of material quality, while the primary alternative, ammonothermal growth, majors on high crystal quality, but is impaired by a low throughout that drives up production costs. However, the limitations of ammonothermal growth could soon be addressed, thanks to a team from Japan that has boosted throughput with larger autoclaves employing acidic mineralisers.

Conventional ammonothermal growth uses basic mineralisers and temperatures of more than 600 °C. Growth takes place in autoclaves made from nickel-based superalloys that have a high strength at elevated temperatures, but the high pressures required for crystal formation restricts the size of the growth reactor.



➤ Acidic ammonothermal growth can be carried out at relatively low pressures, allowing the use of larger autoclaves with a higher throughput.

Switching from basic mineralisers to those that are acidic allows lower growth pressures, and thus larger autoclaves that provide a higher throughput.

The Japanese collaboration that's exploring this opportunity brings together researchers from Tohoku University, Mitsubishi Chemical Corporation and The Japan Steel Works, which has a great deal of expertise in producing autoclaves. This company has made more than 400 of them for the production of quartz via the hydrothermal method, and can draw on 15 years of research-based experience when producing autoclaves for basic ammonothermal growth of GaN.

Team spokesman Shigefusa Chichibu claims that they are the first to report the growth of large, flat, *c*-plane GaN using a low-pressure acidic ammonothermal process. He added: "This uses half the pressure of conventional acidic ammonothermal methods and a quarter of basic ammonothermal methods."

The team carried out GaN growth in an autoclave capable of accommodating crystals up to 4 inches in diameter. This vessel is lined with silver to prevent corrosion from a reaction between supercritical ammonia and acid.

GaN seeds were placed in the bottom half of the autoclave, where the temperature is higher. Above them, where it is cooler, the team added polycrystalline GaN, the raw material. This particular arrangement aided the growth of high-quality GaN, because the higher temperature where crystal growth occurs supressed the generation of point defects, and impurity atoms were transported to the low-temperature zone.

The researchers have studied GaN material formed after 21 days of growth on: a 2-inch diameter, HVPE-grown seed; and a 10 mm by 10 mm seed, produced by the acidic ammonothermal method. GaN grown on the HVPE seed suffered from tilt and twist mosaics, while that formed on the ammonothermal seed yielded a 3 mm-thick smooth, flat GaN crystal.

Informed by their finding, Chichibu and co-workers inserted a 60 mm by 60 mm seed produced by the ammonothermal method into the autoclave. 14 days of growth produced a 3 mm-thick, smooth, flat GaN crystal. It is almost bow free, and when assessed by X-ray diffraction, produces a peak with a full-width at half-maximum of just 13 arcsec.

Since reporting these results, the team has installed a much larger autoclave. "We are currently conducting growth experiments for 4-inch and 6-inch mass production," revealed Chichibu, who added that the next goals for the team are to produce GaN substrates grown by low-pressure acidic ammonothermal growth for customers, and to accelerate device evaluation.

REFERENCE
➤ K. Kurimoto *et al*. Appl. Phys. Express **15** 055504 (2022)

High-voltage Ga_2O_3 transistors surpass silicon's limit

4.4 kV Ga_2O_3 MESFETs with a sandwiched dielectric field plate deliver a figure of merit exceeding 100 MW cm^{-2}

A US collaboration claims to have set a new benchmark for Ga_2O_3 power transistors. A partnership between the University of Utah, the University of Buffalo, Agnitron Technology and UCSB says that its MESFETs are the first Ga_2O_3 transistors with a breakdown voltage in excess of 4 kV that surpass the theoretical unipolar figure-of-merit for silicon.

Comparing their device's performance with that of SiC is not easy, due to differences in geometry – most SiC devices are vertical, while the Ga_2O_3 MESFET has a lateral architecture.

However, initial results are encouraging. "If we compare with SiC lateral devices, our devices offer half the device footprint for a higher breakdown voltage," says Sriram Krishnamoorthy from UCSB.

However, he warns that it is still too early for meaningful comparisons between gallium oxide, which is barely a decade-old technology, and the more mature, commercial, SiC technology.

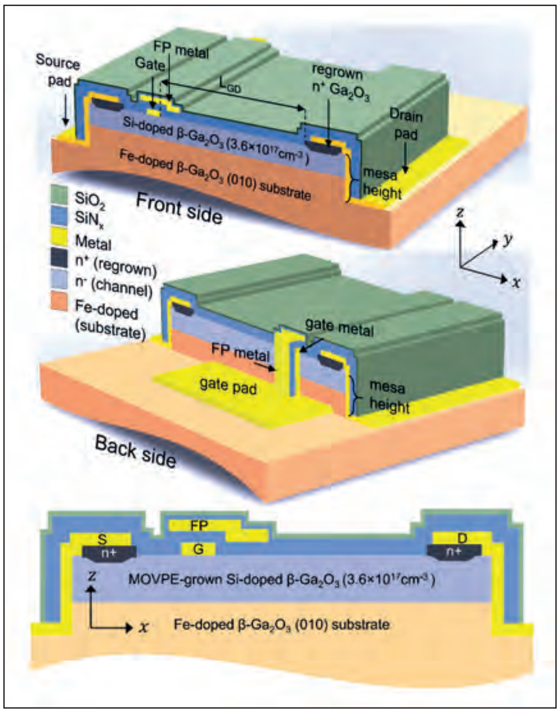
The team's success has come from avoiding etching damage in the active region, which is the area between the source and drain contacts.

Most developers of Ga_2O_3 transistors employ a field plate to reduce the peak electric field and boost the breakdown voltage. However, when they fabricate this design, it leads to etching-related damage that degrades conductivity in the active region, leading to a hike in on-resistance and a reduced on-current.

"We have employed a process flow that avoids any dry etching of the active region, except for the region where the contact layers are regrown," remarks Arkka Bhattacharyyafrom the University of Utah, adding that this ensures a low on-resistance and a high on-current.

Field plates were formed without damage to the active region through a combination of metal evaporation and plasma-enhanced CVD of SiN.

Measurements on a MESFET with a 34.5 μm gate-to-drain length, which has a gate length of 2.4 μm and a gate-to-source distance of 1.0 μm, revealed a maximum on-current of 56 mA mm^{-1}, an on-resistance of 385 Ω, a maximum transconductance of 6.2 mS mm^{-1}, and a sub-threshold swing of 186 mV dec^{-1}.



➤ The record-breaking β-Ga_2O_3 MESFETs produced by the US team incorporate a field plate (a). For devices with gate-to-drain lengths of 34.5 μm and 44.5 μm, field plate extensions are 3.2 μm and 3.5 μm, respectively. The gate field plate metal is electrically connected to the gate pad outside the mesa (b). A 2D cross-section of the device along the *x-z* plane (c).

Breakdown measurements, made by submerging the wafer in a dielectric liquid, provided values of 4415 V for the device with a 34.5 μm gate length, and 4567 V for the variant with a 44.5 μm gate length. This pair of devices had specific on-resistances of 148 mΩ cm^2 and 219 mΩ cm^2, and corresponding power figures-of-merit – defined as the square of the breakdown voltage, divide by the specific on-resistance – of 132 MW cm^{-2} and 96 MW cm^{-2}. These values surpass the theoretical limit for silicon, a feat previously restricted to devices with breakdown voltages below 4 kV, according to benchmarking by the team.

The collaboration are now planning to investigate alternative passivation materials and strategies that improve channel mobility while suppressing reverse leakage.

"One can also employ a gate oxide and operate in accumulation mode, and this can further reduce the on-resistance, via a higher current density," says Krishnamoorthy.

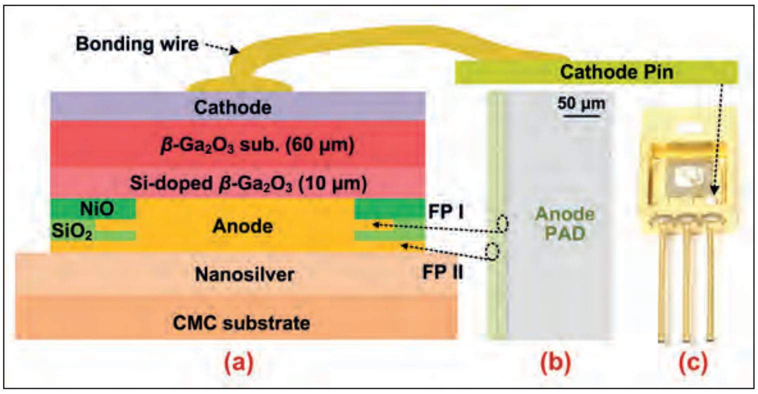
REFERENCE
➤ A. Bhattacharyya *et al.* Appl. Phys. Express **15** 061001 (2022)

Trimming the thermal resistance of Ga_2O_3 Schottky barrier diodes

Thinning the native substrate leads to a record-breaking power-conversion efficiency

THE ACHILLES HEEL of the Ga_2O_3 power device is its poor heat dissipation, attributed to the low thermal conductivity of this oxide. But this weakness can be diminished through substantial thinning of the substrate, leading to a record-breaking power conversion efficiency, according to a team from Nanjing University, China.

Those engineers point out that the body thickness of advanced Ga_2O_3 devices is typically between 400 µm and 600 µm – but with their three-step process, this is reduced below 100 µm, leading to a cut in thermal resistance for Schottky barrier diodes that then deliver better power characteristics.



➤ Schottky barrier diodes that have a thin body (a) and feature a pair of field plates (b) provide excellent conversion efficiencies in a packaged format (c).

Devices are produced by processing epiwafers made by Novel Crystal Technology, Japan. These epiwafers combine a 640 µm-thick tin-doped β-Ga_2O_3 substrate with a 10 µm-thick silicon-doped β-Ga_2O_3 drift layer, grown by HVPE. Before embarking on the thinning process, the team applied a 6 µm-thick photoresist to protect the drift layer.

The three-stage thinning process began with rapid mechanical grinding with a sharp abrasive grit that thinned the substrate to around 250 µm. Mechanical fine grinding followed, using Al_2O_3 abrasive powders mixed with distilled water to trim the thickness down to 150 µm. The final process, involving chemical mechanical polishing with a colloidal silica suspension, resulted in a body thickness as low as 70 µm.

Team spokesman Jiandong Ye told *Compound Semiconductor* that the entire thinning process took 3 hours, with most time taken on steps two and three.

The researchers had to take much care when chemical mechanical polishing, to avoid damaging devices. This step took about 90 minutes, but Ye thinks it could be shortened by improving the thinning recipes, through the likes of optimisation of the platen rotation speed and the polishing pressure.

Ye is confident that the team's three-step substrate thinning could be applied to high-volume device production. "This achievement will also be realized by fabs in the future, which may be the easiest and most effective way to overcome the shortcomings of low thermal conductivity of Ga_2O_3."

From their thinned epiwafers, Ye and co-workers produced diodes by electron beam evaporation, annealing and photolithography. The fabricated devices had a 3 mm by 3 mm contact area and a pair of field plates with lengths of 10 µm and 30 µm.

Using pressureless nanosilver sintering at 250 °C, the engineers flip-chip bonded their large-area devices to a 0.5 mm-thick copper-molybdenum-copper substrate with a high thermal conductivity.

To benchmark the performance of their diodes, the team produced a control, identical in every manner except for having a body thickness of 150 µm.

Current-voltage measurements show that both types of Schottky barrier diode have a blocking voltage of around 355 V to 380 V. These values, about three times higher than that of previous devices produced by the team, are attributed to the introduction of field plates.

Additional measurements show that the reduced body thickness cut thermal resistance from 2.71 K/W to 1.48 K/W, increased surge current from 47 A to 59 A, and propelled the power conversion efficiency to 98.9 percent. "To our best knowledge, the 98.9 percent power conversion efficiency achieved in our work is the highest among reported Ga_2O_3 power rectifiers," remarked Ye.

He has plans for optimising the body thickness of the device and enhancing its electrothermal ruggedness by improving the materials or the fabrication process. Another aim is to increase the breakdown voltage of the large-area Ga_2O_3 Schottky barrier diodes. This could be addressed with termination technologies, such as a small-angle bevelled-mesa structure.

REFERENCE

➤ H. Gong *et al.* IEEE Electron Device Lett. **43** 773 (2022)

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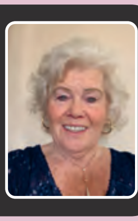

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