COMPOUND SEMICONDUCTOR

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

Streamlining SiC substrate production

HARDINGE

VOLUME 29 ISSUE V 2023

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

COMPOUNDSEMICONDUCTOR.NET

INSIDE

News, Analysis, Features, Editorial View, Research Review and much more

GaN: Excelling in the extreme

Eradicating a high defect density in GaN epilayers will allow devices to shine in extreme environments

Revolutionising GaN-on-silicon RF

GaN-on-silicon HEMTs have a great opportunity to serve in mobile applications requiring high-power millimetre waves

New opportunities for deep-UV LEDs

Higher powers and efficiencies, alongside longer lifetimes, are driving interest in the deep-UV LED within the healthcare sector

AIXTRON

What‘s Your Next Big Thing?

- Micro LED Displays
- Autonomous Driving / 3D Sensing
- Communication Infrastructure
- Solar Cells
- ...

G10-AsP

The Enabling MOCVD Solution

Fully Automated MOCVD for High Volume Production of GaAs/InP Based Materials

Cassette-to-Cassette Wafer Handling

www.aixtron.com

VIEWPOINT

By Richard Stevenson, Editor

Covid's legacies?

WHAT WILL BE the lasting legacies of Covid? Surely one of them is a shift to working from home, at least some of the time. And without the grind of the daily commute, alongside diminished social interaction during the working day, you might think that this new regime could also lead to greater participation in community activities. But my anecdotal evidence suggests otherwise. Maybe more of us are simply more used to being at home more often.

During the height of the pandemic deep-UV LEDs drew much attention, offering an elegant solution to incapacitating the virus. Market analysts predicted a surge in sales for the device, suggesting that this would be a pivotal moment in the history of this deep-UV emitter.

But while heightened interest in the deep-UV LED has been great for raising its profile, the success of the vaccination programme has dealt a blow to any long-term hike in sales in the air disinfection market. Today, when companies are trying to eke out a profit against the backdrop of rising costs and strong wage demands, there's little appetite for equipping offices with units that use deep-UV LEDs to ensure healthy air.

Yet despite the collapse of this market, there's still much good news to celebrate in the deep-UV LED sector. Take AquiSense, a provider of water treatment systems based on this solid-state source. This company's revenue is continuing to rise at great pace; it has identified many, many opportunities to vastly increase sales; and it is seeing substantial improvement at the chip level that will help to ensure further success (to discover more about the prospects for AquiSense, and its views on the progress of makers of deep-UV LEDs, take a look at "Busting market myths" on p. 16).

Another impact of the pandemic was a shift in many conferences from in-person to on-line. However, while an on-line conference is better than nothing, there's no substitute for getting a community together, hearing developments from around the world, and discussing the most significant breakthroughs with others over lunches, dinners and coffee breaks.

Like many sectors within the compound semiconductor community, those working on deep-UV LEDs are now getting back to in-person meetings. This April, more than 220 of them gathered in Berlin for the third meeting of ICULTA – that's the International Conference on UV Light-emitting Technologies and Applications.

Included in this issue is a report on ICULTA from a member of its technical committee, Michael Kneissl from TU Berlin (see p. 32). One of his lasting impressions from that meeting, which reflects the observation from AquiSense, is that the performance of the deep-UV LED is rising fast. For example, at ICULTA ams Osram revealed that its third-generation of deep-UV LEDs are producing up to 200 mW at a wall-plug efficiency of 10 percent.

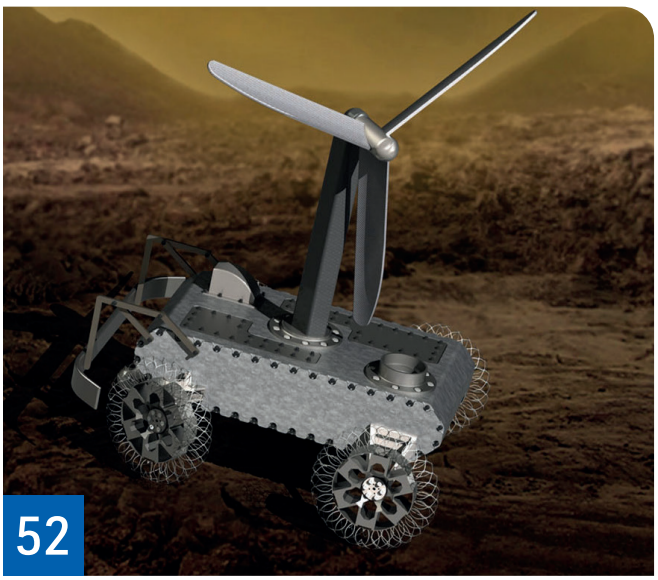
One can speculate that a contributing factor behind these impressive performance figures is a hike in investment in this device during the pandemic. But we don't know for sure. While some legacies from Covid are clear, others will be harder to identify.

Free weekly e-news roundup go to: compoundsemiconductor.net

CONTENTS

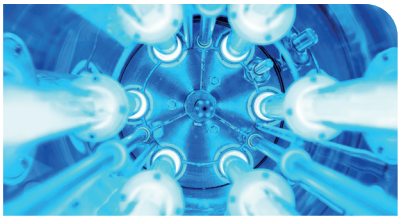
VOL. 29 ISSUE V 2023

COMPOUND SEMICONDUCTOR
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY



46

NEWS ANALYSIS



RESEARCH REVIEW

NEWS

Editor Richard Stevenson
richardstevenson@angelbc.com
+44 (0)1291 629640

News Editor Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Director of Logistics Sharon Cowley
sharon.cowley@angelbc.com
+44 (0)1923 690200

Senior Sales Executive
Jacob Caulfield
jacob.caulfield@angelbc.com
+44 (0)2476 718979

Circulation
Scott Adams
scott.adams@angelbc.com

Publisher Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

USA Representatives
Brun Media
Janice Jenkins
jjenkins@brunmedia.com
+1 724-929-3550
Tom Brun
tbrun@brunmedia.com
+1 724 539-2404

Chief Executive Officer
Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

Chief Technical Officer
Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Directors
Jackie Cannon, Sharon Cowley

Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

EPC embarks on a patent war with Innoscience

EPC takes Innoscience to court over four patents covering the design and manufacture of enhancement-mode GaN power semiconductor devices

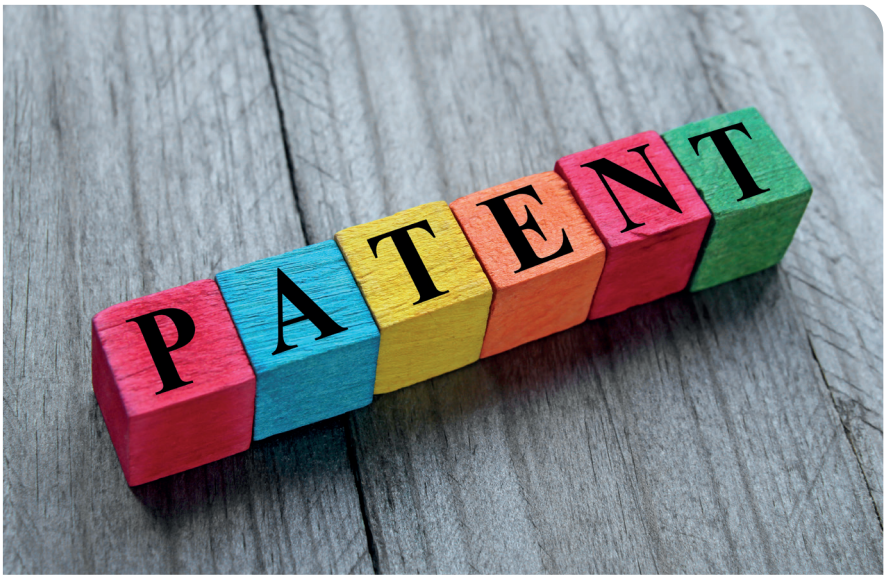
A BATTLE of intellectual property has broken out, with US-based GaN specialist Efficient Power Conversion taking Chinese GaN firm Innoscience to court over four patents related to enhancement-mode GaN power semiconductor devices.

Innoscience has responded to the charges, arguing that after it undertook a thorough analysis, it found no infringement of EPC's intellectual property rights.

EPC has filed complaints in federal court and in the US International Trade Commission (ITC), asserting four patents of its foundational patent portfolio against Innoscience (Zhuhai) Technology Company, Ltd. and its affiliates (collectively, Innoscience).

These patents are said to cover core aspects of the design and manufacturing process of EPC's proprietary enhancement-mode GaN power semiconductor devices. According to EPC, these patents encompass innovations that enabled the company's GaN-based power devices to mature from a research project to a mass-producible high-volume alternative to silicon-based transistors and ICs with GaN devices having higher efficiency, smaller size, and lower cost.

EPC began making the first mass-produced commercial GaN transistors and integrated circuits in 2010. It claims that Innoscience recruited two EPC employees to serve as its CTO and head of sales and marketing. Shortly thereafter, Innoscience is said to have introduced a suite of products visibly identical to EPC's, boasting virtually equal performance across key performance metrics. More recently, Innoscience has claimed that many of its products have 'pin-to-pin compatibility with existing products' including EPC's products, in a bold and aggressive campaign to market its suite of products to EPC's customers.



"I have always been a believer in fair cooperation as the foundation of global technology markets," said Alex Lidow, EPC's co-founder and CEO. "Only through cooperation can we unlock the potential of GaN technology and meet the world's energy security and sustainability goals. Strong protections and respect for intellectual property are essential to that trust and cooperation."

"I am confident that, through these decisive actions, we will reach a fair and reasonable resolution that levels the playing field and ensures a GaN ecosystem that works for all participants in this critical emerging technology," Lidow added.

EPC has sued Innoscience in federal court and the ITC for patent infringement, seeking damages and barring Innoscience from importing its infringing suite of GaN products into the US.

In a robust defence of its position, Innoscience has responded to EPC's filing of a patent lawsuit, with intentions to "take all legal measures to counterattack".

Innoscience says that since its establishment, it has filed 753 relevant patents globally, with 129 patents granted. It claims that the allegations of technology plagiarism, based on the job changes of a few employees, are purely speculative and lack factual basis.

The Chinese chipmakers also argues that EPC has a significant disparity in terms of business scale, scope of operations, and technological strength. It points out that it is an Integrated Device Manufacturer with its core competence lying in the full vertical integration of the semiconductor industry, including chip manufacturing.

The company adds that it is globally recognised for its pioneering 8-inch GaN mass manufacturing process. Innoscience dismisses EPC as a fabless design company, with product designs primarily relying on a 6-inch foundry process platform. The Chinese firm belittles EPC for not possessing its own wafer fabrication facilities or corresponding manufacturing processes.

Setting new standards for MBE

Riber and IntelliEPI qualify the largest MBE system for mass production of III-V compound semiconductors

EPITAXY EQUIPMENT manufacturer Riber has announced a major milestones in a joint development program with IntelliEPI for the qualification of the new MBE 8000 production platform.

Riber's new flagship product, the MBE 8000, is believed to be the highest capacity MBE production tool available on the market, able to handle batches of eight 150 mm (6 inch) or four 200 mm (8 inch) wafers. The design of this machine benefits from over 20 years' experience in production MBE systems.

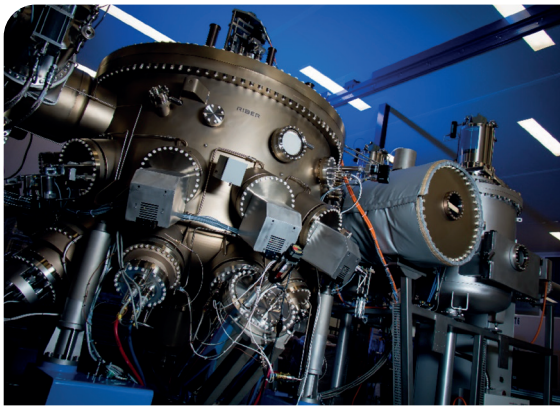
Following the delivery of the first MBE 8000 platform and after qualification work carried out in close cooperation with IntelliEPI, Riber says that the results obtained have exceeded expectations, particularly in terms of uniformities, defect densities, increasing yield, and interface abruptness, which is key for superlattice structures to achieve high performance lasers.

These performance figures combined with a high level of run-to-run repeatability control in large-scale production will enable a new generation of lasers, according to the company, in particular for VCSEL technology with significant market opportunities in the field of smartphone under-display facial recognition.

In addition to the VCSEL market, the precise control of the doping uniformity and the process stability offered by the MBE 8000 platform will enhance microelectronic device performances, such as conductivity.

Over the past few months, as results were disclosed to several industrial customers, interest for this machine has grown quickly, leading to discussions for potential purchase, says Riber.

According to Yung-Chung Kao, IntelliEPI president and CEO: "From the initial evaluation so far, this Riber MBE 8000 has shown very impressive performance in terms of being able to produce high quality epi materials over such a large substrate platen area with excellent composition and thickness uniformity across the 8x6 inch platen. With this improvement, the MBE 8000 platform offers a solution to make large-scale production MBE technology more competitive especially for high performance and high throughput market opportunities."



Christian Dupont, Riber's CEO: "Thanks to the efforts of Riber and IntelliEPI teams, we have reached a major step for MBE 8000 qualification. The results provided by the machine exceed our initial objectives. With an optimum cost-of-ownership and large capacity, the MBE 8000 equipment has strong commercial prospects. In addition, our milestone in this joint development program with IntelliEPI demonstrates the capability to bring MBE technology in high volume semiconductor industry."

ST and Sanan advance SiC ecosystem in China

Companies to create a joint venture for high-volume 200 mm SiC device manufacturing

EUROPEAN SEMICONDUCTOR giant STMicroelectronics and Sanan Optoelectronics, a Chinese compound semiconductor company, have signed an agreement to create a new 200 mm SiC device manufacturing joint venture in Chongqing, China.

The new SiC fab is targeting to start production in Q4 2025 and full buildout is anticipated in 2028, supporting the rising demand in China for car electrification as well as for industrial power and energy applications. In parallel, Sanan Optoelectronics will build and operate separately a new 200 mm SiC substrate manufacturing facility to fulfil the joint venture's needs, using its own SiC substrate process.

The joint venture will make SiC devices exclusively for STMicroelectronics, using ST proprietary SiC manufacturing process technology, and serve as a dedicated foundry to ST to support the demand of its Chinese customers.

The total amount for the full buildout of the joint venture is expected to be about $3.2 billion, including capital expenditures of about $2.4 billion over the next 5 years, which will be financed by contributions from STMicroelectronics and Sanan Optoelectronics, local government support, and loans to the joint venture.

"China is moving fast towards electrification in automotive and industrial and this is a market where ST is already well-established with many engaged customer programmes. Creating a dedicated foundry with a key local partner is the most efficient way to serve the rising demand of our Chinese customers. The combination of Sanan Optoelectronics' future 200 mm substrate manufacturing facility with the front-end joint venture and ST's existing back-end facility in Shenzhen, China, will enable ST to offer our Chinese customers a fully vertically integrated SiC value chain," said Jean-Marc Chery, president and CEO of STMicroelectronics.

"It is an important step to further scale up our global SiC manufacturing operations, coming in addition to our continuing significant investments in Italy and Singapore. This joint venture is expected to be one of the enablers of the opportunity we see to reach more than $5 billion of SiC revenues by 2030. This initiative is consistent with ST 2025-27 $20 billion plus revenue ambition and the associated financial model, previously communicated to the financial markets."

"The establishment of this joint venture will be a major driving force for the wide adoption of SiC devices on the Chinese market," said Simon Lin, CEO of Sanan Optoelectronics. "Being an international, well-known, high-quality SiC foundry service company, Sanan will also supply its SiC substrate to this new joint venture, by building a dedicated new SiC substrate factory. This is an important step for Sanan Optoelectronics' ambitions as a SiC foundry. With this new Joint Venture and the new SiC substrate capacity expansion, we are confident that we will continue to take the lead in the SiC foundry market."

The completion of the project is subject to regulatory approvals.

EVG®

invent
innovate
implement

www.EVGroup.com

FUSION AND HYBRID BONDING FOR HETEROGENEOUS INTEGRATION

- Enabling advanced 3D device stacking and chiplet integration for CMOS image sensors, memory and 3D system-on-chip (SoC)
- High-volume production equipment and process technology for Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W) hybrid bonding
- GEMINI® FB Automated Production Wafer Bonding System delivers industry leading alignment accuracy and bonding performance
- Heterogeneous Integration Competence Center™ serving as leading-edge innovation incubator for EVG customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

Ams Osram adds eye safety feature to IR VCSEL

Emitter for in-cabin sensing includes interlock loop method for safeguarding ultra-fast detection of faults

AMS OSRAM has enhanced its portfolio of infrared laser modules for automotive in-cabin sensing with the TARA2000-AUT-SAFE VCSEL family, which offers a more reliable and robust eye safety feature than existing automotive VCSEL modules.

A top-ten global car manufacturer has already selected this new product for a new design, and Ams Osram will supply it in mass production volumes starting in 2024.

The new TARA2000-AUT-SAFE, which produces a tightly controlled beam of IR light at a peak wavelength of 940 nm, is suitable for the same use cases as the existing TARA2000-AUT family: driver monitoring, gesture sensing, and interior (cabin) monitoring. It consists of an Ams Osram VCSEL chip and micro-lens array (MLA) packaged in a compact module.

The new VCSEL, which has a wide field of illumination of 116 ° x 87 °, is optimised for cabin monitoring with 2D near infrared imaging and 3D indirect time-of-flight cameras.

A forthcoming version with a narrow field of illumination of 46 ° x 41 °, the TARA2000-940-UN-AUT-SAFE, is suitable for driver monitoring. It is currently sampling with customers.

The TARA2000-AUT-SAFE family is said to offer increased reliability and simpler implementation for automotive manufacturers, due to the new, built-in interlock loop method for protecting eye safety.

The new device's resistive interlock circuitry is integrated on the MLA. Providing a near-instant response of less than 1 µs to fault conditions, the TARA2000-AUT-SAFE can directly detect faults that could compromise eye safety, such as diffuser cracking or shear-off. The TARA2000-AUT-SAFE solves various design and

implementation challenges, and at a lower cost than competing products on the market today. The fast and reliable response is in contrast to the built-in photodiode method for eye safety protection in competing automotive VCSELs. In competing products, the photodiode signal is prone to faults caused by non-eye-safety related factors such as reflective objects in front of the VCSEL module, impairing the system's ability to protect eye safety.

In addition, the interlock loop is said to be easier to integrate, as its read-out circuit only requires one AND gate or MOSFET. In comparison, the complex read-out circuit of photodiode includes an increased number of more expensive components. This means that the photodiode method results in a higher bill-of-materials cost, as well as a slower response to events that carry a risk to eye safety.

Firat Sarialtun, senior global marketing manager at Ams Osram, said: "We have been able to take our experience in other application areas and directly apply it to enhancing the TARA2000 family. Ams Osram has deep knowledge of interlock-based eye-safety designs, as we have had products that use the interlock method in mass production in other end markets, such as consumer and industrial, for many years."

Sarialtun added: "We were the first in the industry to start mass production of an AEC-Q102 and ISO26262 compliant IR VCSEL module for in-cabin sensing in Q2-2021, and now we are taking VCSEL technology a step further with the interlook loop feature. Thanks to our deep engineering expertise across the whole optical assembly, the interlock circuit has been integrated directly on the lens and package, drawing on our deep understanding of each sub-component and technology in a complete VCSEL module."

The design of the TARA2000-AUT-SAFE builds on the high performance of the TARA2000-AUT. Housed in a robust ceramic package, the new device offers a maximum operating temperature of 125°C, supporting AEC-Q102 Grade 1 qualification as well as ISO 26262 for functional safety. Peak optical power output of a 100 µs pulse at 25 °C/2 percent duty-cycle/5 A is 4 W.

The TARA2000-940-UN-AUT-SAFE and TARA2000-940-W-AUT-SAFE VCSEL emitters are sampling now.

Vitesco and Onsemi sign long-term SiC agreement

Vitesco Technologies is securing SiC supply capacity worth $1.9 billion

VITESCO TECHNOLOGIES and Onsemi have announced a 10-year long-term supply agreement worth $1.9 billion for SiC products to enable Vitesco's ramp in electrification technologies.

Vitesco, an international manufacturer of drive technologies and electrification solutions, is providing an investment of $250 million to Onsemi for new equipment for SiC boule growth, wafer production and epitaxy to secure access to SiC capacity.

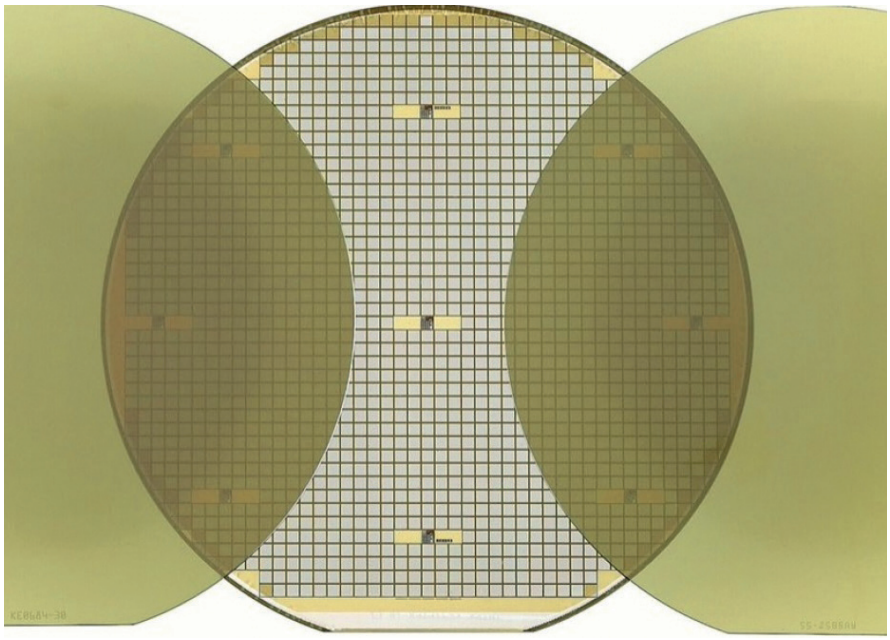
The equipment will be used to produce SiC wafers to support Vitesco's growing SiC demand.

In parallel, Onsemi, a leader in intelligent power and sensing technologies, will continue to invest substantially into the end-to-end SiC supply chain.

In addition, Vitesco and Onsemi will collaborate on optimised customer solutions for Vitesco. Onsemi's highly efficient EliteSiC MOSFETs will be used by Vitesco to execute the recent orders as well as future projects for traction inverters and electric vehicle drives.

"Energy-efficient silicon carbide power semiconductors are at the beginning of a big surge in demand. That is why it is imperative for us to get access to the complete SiC value chain together with Onsemi. With this investment we have a secure supply of a key technology over the next ten years and beyond," said Andreas Wolf, CEO of Vitesco.

Hassane El-Khoury, president and CEO of Onsemi, commented: "This collaboration will enable Vitesco to address their customers' demand for longer range and higher performance in electric vehicles. Onsemi provides superior performance and quality, supply assurance, and manufacturing at scale of SiC technologies based on decades of experience in manufacturing power semiconductor products in high-volume automotive applications."



Nuburu and GE Additive collaborate on 3D printing

INDUSTRIAL BLUE laser firm Nuburu has signed a joint technology agreement with GE Additive, to explore the speed, accuracy, and commercial benefits of blue laser-based metal 3D printing.

"As we continue to advance our proprietary blue laser technology, we have further increased both power and brightness to open up new applications," said Mark Zediker, CEO and co-founder of Nuburu.

"We've achieved key performance milestones that open new possibilities for significant advances in metal 3D printing. Working with GE Additive, and their expertise in metal additive manufacturing, will allow us to rapidly optimise our innovative area printing approach. That will accelerate the further expansion of our pioneering blue laser into innovative metal 3D printing solutions, which have the potential to change the landscape of military logistics; aerospace manufacturing; medical device fabrication, and beyond."

"As an industry leader in metal 3D printing and having been on the leading edge of qualifying parts in regulated industries, we're excited to evaluate Nuburu blue industrial laser technology and its benefits," said Chris Schuppe, general manager of engineering and technology of GE Additive.

This joint development agreement is in addition to an agreement with GE Additive to support Nuburu's previously announced AFWERX Small Business Innovation Research (SBIR) Phase II contract awarded to Nuburu in 2022.

Nexperia adds e-mode GaN FETs

Company to offer both cascode and e-mode GaN FETs for low and high voltage use

NEXPERIA has released its first power GaN FETs in e-mode (enhancement mode) configuration for low (100/150 V) and high (650 V) voltage applications.

By augmenting its cascode offering with seven new e-mode devices, Nexperia says it provides designers with the optimum choice of GaN FETs from a single supplier alongside its portfolio of silicon-based power electronics components.

Nexperia's new portfolio includes five 650 V rated e-mode GaN FETs (with $R_{DS(on)}$ values between 80 mΩ and 190 mΩ) in a choice of DFN 5 mm x 6 mm and DFN 8 mm x 8 mm packages.

They improve power conversion efficiency in high-voltage, low-power datacom/telecom, consumer charging, solar and industrial applications.

They can also be used to design brushless DC motors and micro server drives for precision with higher torque and more power.

Nexperia now also offers a 100 V (3.2 mΩ) GaN FET in a WLCSP8 package and a 150 V (7 mΩ) device in a FCLGA package.

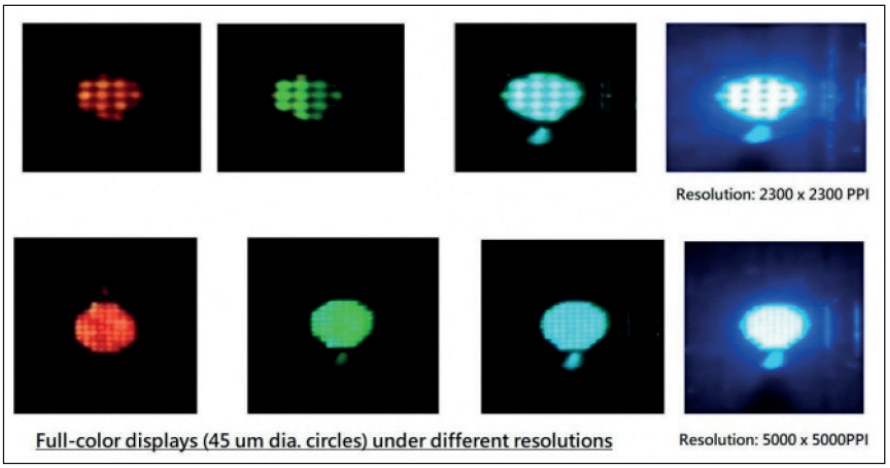
These devices are suitable for various low-voltage, high-power applications to deliver, for example, more efficient DC-DC converters in data centers, faster charging (e-mobility and USB-C), smaller lidar transceivers, lower noise class D audio amplifiers and more power dense consumer devices like mobile phones, laptops, and games consoles. GaN devices are increasingly entering mainstream power electronics markets, including server computing, industrial automation, consumer, and telecom infrastructure, thanks to their fast transition / switching capability (high dV/dt and dI/dt) and efficiency in low- and high-power conversion applications.

Q-Pixel beats world record for pixels per inch

Q-PIXEL INC, a Los-Angeles based startup, has announced the world's first full-colour, ultra-high resolution microLED display.

Using its GaN-based Polychromatic microLED technology, Q-Pixel says it has achieved a full-colour LED display with a pixel density of 5,000 pixels per inch (PPI), surpassing the current world record of 2,000 PPI held by ITRI of Taiwan.

Q-Pixel believes the technology is a game-changer for the display industry by allowing full-colour tunability across a single 4-μm pixel. It says this approach can replace single-colour LEDs and addresses several challenges to the microdisplay industry, including the need for pick-and-place, while at the same time enabling ultra-high pixel density.



Mitsubishi and Coherent sign SiC agreement

Companies to scale manufacturing of SiC power electronics on a 200 mm technology platform

MATERIALS and laser company Coherent Corp and Mitsubishi Electric have signed a memorandum of understanding (MoU) to collaborate on a programme to scale manufacturing of SiC power electronics on a 200 mm technology platform.

To meet the rapidly growing demand for SiC chips, in particular for electric vehicles, Mitsubishi Electric announced an investment of approximately $1.8 billion in the five-year period ending March 2026. A major portion of the investment, approximately $71 million, will be used to construct a new plant for SiC power devices, based on a 200 mm technology platform, and enhance related production facilities. Under the MoU, Coherent will develop a supply of 200 mm *n*-type 4H SiC substrates for Mitsubishi Electric's future SiC power devices manufactured at the new facility.

"We are excited to build on our relationship with Mitsubishi Electric, a pioneer in SiC power devices and a global market leader in SiC power modules for high-speed trains, including the famous Shinkansen in Japan," said Sohail Khan, executive VP of New Ventures & Wide-Bandgap Electronics Technologies at Coherent. "We have a long track record of supplying SiC substrates to Mitsubishi Electric and are looking forward to expanding our relationship with them to scale their new 200 mm SiC platform."

"Coherent has been for many years a reliable supplier of high-quality 150 mm SiC wafer substrates to Mitsubishi Electric," said Masayoshi Takemi, executive officer, group president, Semiconductor & Device at Mitsubishi Electric. "We are delighted to enter into this close partnership with Coherent to scale our respective SiC manufacturing platforms to 200 mm."

Coherent demonstrated the world's first 200 mm conductive substrates in 2015. In 2019, Coherent began to supply 200 mm SiC substrates under REACTION, a Horizon 2020 four-year programme funded by the European Commission. Mitsubishi Electric made history by launching the world's first SiC power modules for air conditioners in 2010, and became the first supplier of a full SiC power module for Shinkansen high-speed trains in 2015.

UK Space Agency funds SiC chip project

IceMOS to develop radiation-tolerant high-voltage superjunction SiC MOSFETs

THE UK SPACE AGENCY has awarded IceMOS Technology part of £300,000 funding in a project to develop SiC power transistors for space applications. This is in partnership with the UK space and defence trade association ADS, through the Space Technology Exploitation Programme (STEP).

The IceMOS Technology manufacturing centre of excellence located in Belfast, Northern Ireland, will focus on delivering an advanced engineered substrate, enabling a radiation-tolerant, high-voltage SiC engineered drain MOSFET for more efficient high power distribution electrical systems on spacecraft for low earth orbit, middle earth orbit and deep space exploration.

The company says the merger of a wide bandgap power MOSFET drain structure that can be tailored to be robust in harsh space radiation environments will create a new class of vertical power transistor.

Commercial applications aim to address society's increasing demand for energy conservation in systems such as AI-enabled cloud services and data centres, fast-charging stations for electric vehicles, photovoltaic energy generation and more.

"With this award IceMOS Technology is uniquely positioned to accelerate advances in the UK-space programme by making dramatic improvements in high-voltage power radiation-tolerant transistors," said Samuel Anderson, IceMOS Technology founder and chairman.

Anderson added: "It is an honour to be one of only three companies selected to participate in this prestigious programme to enhance UK space capability by developing this leading-edge technology that can lower costs and significantly improve overall systems performance."

"Creative talent and technical space expertise can be found across the length and breadth of the UK," said Paul Bate, chief executive at the UK Space Agency.

Bate believes that these projects, delivered in partnership with ADS, are brilliant examples of that from Northern Ireland's growing space sector. "They will help catalyse investment, create jobs, and develop new capabilities within the space supply chain."

Chinese team defines fast charging law

'Lichi Law' shows commercial GaN fast charging increases by 60 percent every 9 to 12 months

RESEARCHERS from South China Normal University, Red and Blue Microelectronics, Shenzhen Baseus Technology, Zhejiang University, and Shenzhen University have conducted research on GaN fast charging in the market in the past five years and found a regular trend made up of three elements.

First, the output power of commercial GaN fast charging increases by 60 percent every 9 to 12 months. Second, the output power density of commercial GaN fast charging increases by 30 percent every 6 to 9 months. And third, the output power density of commercial GaN fast charging increases by 50 percent every 20 to 24 months.

They are calling it 'Lichi Law' because the researchers gathered under a lychee tree on the Shenzhen University campus to discuss these developments.

In 2019, the technology of GaN fast-charging products was immature, resulting in a general fast charging power of only 20-30 W in the market, with a relatively large volume. This led to a power density of GaN fast charging generally being below 1 W/cm^3.

However, by 2021, market technology had matured, and the characteristics of GaN devices were successfully used to reduce the volume of fast charging, resulting in a power density of GaN fast-charging products on the market generally exceeding 1 W/cm^3.

This sparked fierce competition among major brands in the research and development of GaN fast charging. In 2023, Realme released a 240 W GaN fast charging product that was only 102 cm^3 in size. This achievement successfully pushed the power density of GaN fast charging to reach 2.36 W/cm^3, making it the highest power density in the market for GaN fast charging.

In terms of quality, Anker unveiled the market's first 30 W GaN fast charger in 2018, with a mass of 54 g and a power density of only 0.53 W/g.

As GaN fast-charging technology developed in 2022, OPPO released the first GaN fast charging product to break through 200 W. Weighing only 147 g, the OPPO 200 W charger achieved a power density of 1.36 W/g, making it the first brand in the market to exceed 1 W/g. Currently, the Realme 240 W released in 2023 boasts the fastest charging output power in the market, weighing only 166 g and achieving a power density of 1.44 W/g.

In October 2018, ANKER released the PowerPort Atom PD1, the world's first USB PD GaN charger, in New York, marking the official entry of GaN technology into the consumer market. In August 2020, Xiaomi released the Mi 10 with its accompanying 120 W GaN fast charger, making it the first mobile phone GaN charger to achieve an output power exceeding 100 W, and marking domestic manufacturers' success in the field of GaN fast charging.

In July 2022, iQOO released the iQOO 10 series of mobile phones, announcing that the fast charging technology of their mobile phones exceeded 200 W and releasing a 200 W GaN fast-charging charger, making them the first mobile phone manufacturer to achieve fast-charging power exceeding 200 W. In January 2023, Realme launched the GT Neo5 mobile phone at the MWC conference with 240 W GaN fast charging, achieving a power density of 2.36 W/cm^3 and 1.45 W/g, leading the industry in terms of technical advancements.

According to product 3C report statistics, there has been significant growth in product power density over the past five years. In 2018, Anker released the first GaN fast charger with a power density advantage of 0.56 W/cm^3. In 2022, iQOO launched a 200 W charger, achieving a power density exceeding 2 W/cm^3, reaching 2.01 W/cm^3.

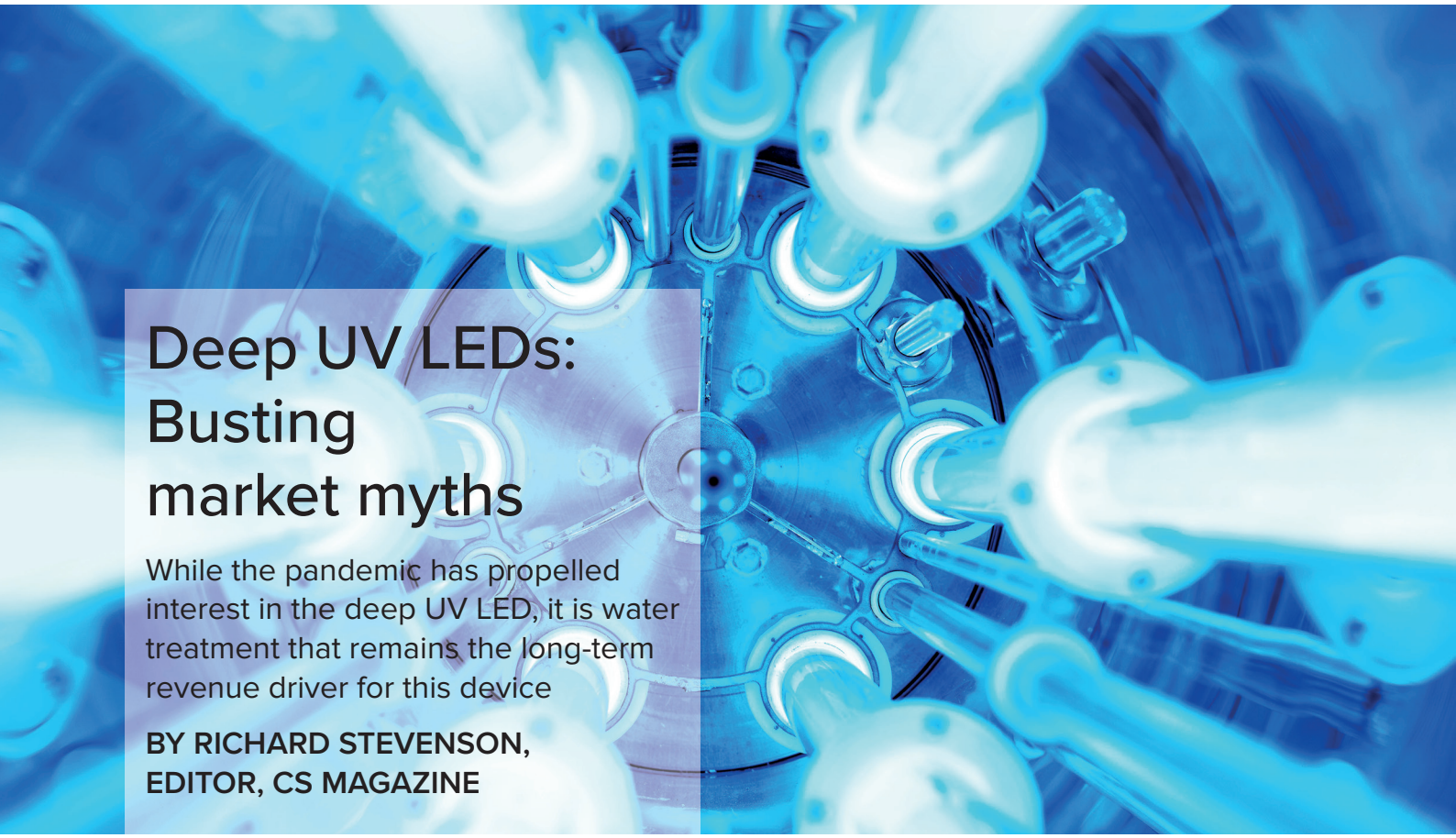
In October 2018, Anker released the first GaN fast charger with a low weight achieving a power density of 0.54 W/g. Four years later, in July 2022, iQOO launched a 200 W charger achieving a power density exceeding 1 W/g, reaching 1.36 W/g.

GaN fast charging data

The researchers say that the following three points show the key data. The interval between the launch of Anker's 30 W GaN fast charger in October 2018 and Xiaomi's 120 W GaN fast charger in August 2020 was 22 months. Subsequently, iQOO launched a 200 W GaN fast charger in July 2022, with an interval of 21 months.

Starting in October 2018, Anker released the first GaN fast charger with a power density of 0.56 W/cm^3, due to its size advantage. In October 2019, OPPO released their 65 W GaN fast charger, achieving a power density exceeding 1 W/cm^3, reaching 1.01 W/cm^3, with a 12-month interval between the two. Then, in July 2022, iQOO launched their 200 W GaN fast charger, achieving a power density exceeding 2 W/cm^3, reaching 2.01 W/cm^3, also with a 12-month interval. Overall, there was a 33-month gap between the first and last releases.

Anker released the first 30 W GaN fast charger with a power density of 0.54 W/g in October 2018, and in July 2022, iQOO released a 200 W GaN fast charger, achieving a power density exceeding 1 W/g. Over the span of 45 months, the power density increased to 1.36 W/g. In January 2023, Realme released a 240 W GaN fast charger with a power density of 1.44 W/g.



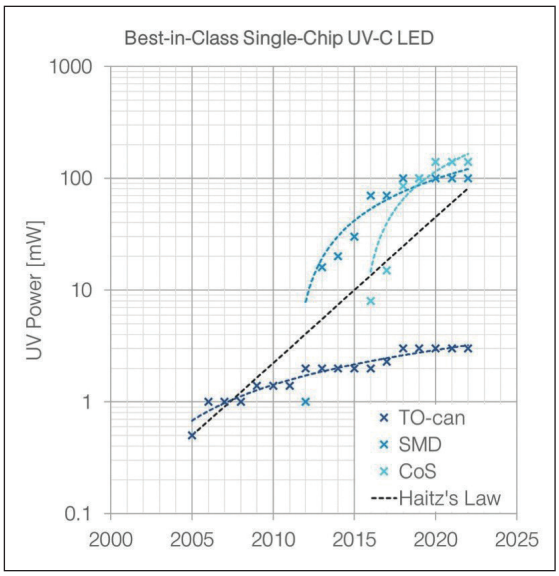
Deep UV LEDs: Busting market myths

While the pandemic has propelled interest in the deep UV LED, it is water treatment that remains the long-term revenue driver for this device

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

HOW DO YOU apply the brakes to a pandemic? One option to prevent its spread is to introduce measures such as PPE and social distancing; and another is to disarm this virus, through the likes of vaccination, chemical treatment and bombardment by radiation.

It's the latter line-of-attack that drove intense interest in the UVC LED when Covid dominated the global agenda. But has this left a lasting legacy, as many would have hoped?



➤ AquiSense's in-house measurements indicate that UV LEDs are improving at a rate that exceeds the pace of Haitz's Law. Three types of device are included: those housed in TO cans; surface-mount devices (SMDs); and chip on substrate (CoS).

Well, probably not, according to executives at AquiSense, a US-based provider of water treatment systems employing LEDs emitting in the deep UV.

The President and CEO of this company, Oliver Lawal, reasons that while many considered using deep-UV LEDs to prevent airborne transmission of Covid, device development could not move fast enough.

Looking back at that time, Lawal says that he struggled to distinguish between marketing noise and real work. "I feel like some of it was just like banging on a drum."

Due to this, he wonders whether the producers of disinfection systems based on deep-UV LEDs that switched their focus to air disinfection are regretting that decision, given the transient nature of that market.

AquiSense's CTO, Jennifer Pagán, tends to agree: "If you pivoted into making office air disinfection systems that sit on your desk, you might have seen a really big upswing during Covid, but probably no one's buying them now."

Throughout the Covid outbreak, AquiSense continued to prioritise water treatment, a strategy that has always delivered revenue growth. "We doubled in the pandemic; but we doubled in the years before the pandemic and we doubled again after it," says Lawal.

To continue to drive sales, AquiSense is expanding its portfolio, including the launch last month of the PearlAqua Deca 30C. Helping to fill a gap in its range of water purifiers, this particular product, which has attracted plenty of pre-orders, will start being shipped in a matter of days. Lawal expects that the Deca 30C will enjoy most success in the beverage and healthcare industries.

Tapping into massive markets

Opportunities to increase the company's sales are vast, given that millions of homes in North America and Europe are not connected to a municipal water supply.

It's also worth noting that for some homeowners that are connected, UV treatment still appeals, providing what Lawal describes as a "second barrier". While a wish for some, it's a necessity for the immuno-compromised, enabling sales to hospitals and care homes.

Thanks to the tremendous success of AquiSense, it's a top-three customer for many of the leading suppliers of UVC LEDs. Due to this, the company is in a great position to provide an informed view on the progress of these device makers, and the performance of their products.

Pagán says that following consolidation in the market around 2015, including the acquisition of SETi by Seoul Semiconductor, there has been an uptick in the number of players on the market over the last few years. New entrants include the likes of CrayoNano, ams Osram and Silanna, all joining the ranks of producers of high-power devices. These suppliers sit above a second tier, which includes a number of Chinese chipmakers, shipping lower-power variants.

The power of the very best devices continues to increase at good pace, with internal measurements at AquiSense indicating a rate of improvement beyond that described by Haitz's Law (see Figure). Such gains in power are highly valued, enabling water treatment at either a faster flow rate or a higher dose.

Best-in-class devices are now edging 6 percent wall-plug efficiencies, according to Pagán, along with output powers that can be as high as 150 mW. "I think the target for a lot of manufacturers is to be at the 8 percent range within another twelve months or so."

With greater powers comes the temptation to try and increase the price – but this is a threat to far greater success for all involved, warns Lawal, who argues that many makers of UVC LEDs are underestimating the competitiveness of the incumbent technology, the mercury lamp. Should sacrifices in UVC LED pricing be made, India could move completely away from the mercury lamp within just 5 years, says Lawal.

"The Indian market currently has around 3 million mercury systems a year, and we believe we're on the verge of cracking a chunk of that market. But to do that, I can't go in at a price point that I'm going in in North America."

Another key characteristic of the UVC LEDs is its lifetime, with different producers quoting different values for the time taken for the intensity to fall by different values – this might be 90 percent, 70 percent or 50 percent.

A lack of standardisation is not a major concern for those at AquiSense, partly because they manage the situation by monitoring the device as it's used. There are three levels of sensing: pass/fail; temperature monitoring; and the recording of the intensity of the UV output. "I think we're unique," argues Lawal. "We're definitely the only company that is providing that level of operational sensing." Such scrutiny shows that AquiSense is well placed to comment on where developers of UVC LEDs should direct their efforts.

"I want them to focus on epitaxial growth, efficiency and contact efficiency," says Pagán, who believes that there has been too much emphasis on packaging.

It's a clear message – and should success follow, it will accelerate humanity's access to healthy drinking water in a post-Covid era.

➤ The PearlAqua Deca 30C provides over 99.99 percent pathogen reduction at a flow rates of 15 litres per minute.

Nobel-prize-winning climate scientist Professor Donald Wuebbles unveiled a plaque to the official opening of Cardiff University's Translational Research Hub, a new home for the Institute for Compound Semiconductors

A new home for the Institute for Compound Semiconductors

Nobel-prize-winning climate scientist Donald Wuebbles opens Cardiff University's Translational Research Hub, a new home for the Institute for Compound Semiconductors

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

ONE THE CORNERSTONES of the world's first compound semiconductor cluster, situated in South Wales, is the Institute for Compound Semiconductors (ICS). Launched in 2015, the long-term plans for this driver of device development have always included a move to a new, purpose-built facility with the capability to process wafers up to 200 mm in diameter. Now finally – and to the immense relief of some of those involved – this has been accomplished, with the new facility up and running and open for business.

To mark this key milestone in the life of the ICS, which is part of Cardiff University, this institute held an official opening on Thursday 18 May. At that celebration for what is now the largest building on the Cardiff Innovation Campus, and the new home to both the ICS and Cardiff Catalysis Institute – together they form what is known as the Translational Research Hub – Nobel-prize-winning climate scientist Professor Donald Wuebbles unveiled a plaque to mark the occasion. He also delivered one of a number of talks that formed the centrepiece of this joyous occasion, showcasing the new capabilities of the ICS.

Those that spoke included Cardiff University's Pro Vice Chancellor Professor Rudolf Alleman, who discussed the many challenges associated with the construction of the Translational Research Hub, which is located on a site previously occupied by railway sidings. Initially the ICS was slated to be up and running in its new home in 2020, but who could have foreseen the problems caused by the Covid pandemic, or material supply issues associated with Brexit.

A reminder of the motivation for forming the ICS came from its Managing Director, Professor Peter Smowton. He explained that the vision for the facility, which is a resource that academia and UK

industry are able to use, came together in 2013 to address what he describes as 'the valley of death'. This phrase relates to the pitfalls that arise when trying to take a promising device technology from the fab and use it to establish a successful, high-volume product.

Smowton is well versed in the challenges of taking a bespoke device with champion results and building on this to create a high-performance, high reliability commercial product. His solution, adopted by the ICS, is that fundamental device development is undertaken with fab tools that are suitable for high-volume manufacture.

Aiding commercialisation of device development is not the only benefit of this approach, however, argues Smowton. He points out that at the heart of the research of many academics is the testing of a hypothesis, which hinges on being able to employ repeatable processes. So pure research also benefits from the highly capable, high-volume tools in the ICS, because they speed the drawing of conclusions from experimental work, as well as the level of rigour.

A diverse research portfolio

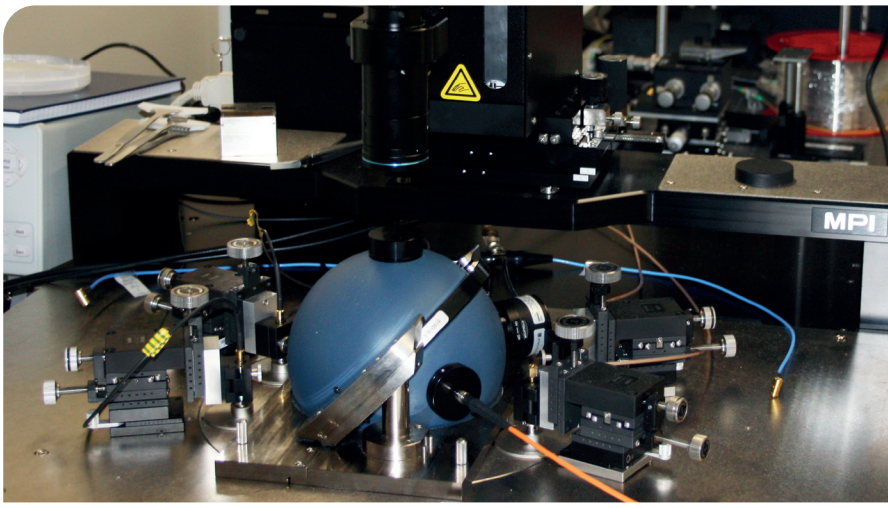
During the official opening of the ICS, this institute showcased its diversified research programme, with brief talks given by a number of academics.

Dr Naresh Gunasekar, a member of the ICS who holds a lectureship position within the Condensed Matter and Photonics Group in the School of Physics and Astronomy, explained that one of his interests relates to the manufacture of wide bandgap semiconductors. His group is concerned with the efficiency of these devices, as well as testing their reliability.

Another researcher sharing their focus, Professor Khaled Elgaid from the ICS and Cardiff University's School of Engineering, spoke about the consequences of energy consumption arising from the shift from 4G to 5G. This evolution will lead to 100 billion connected devices. Armed with tremendous expertise in high-frequency transistors based on a variety of III-Vs, he is involved in the development of GaN HEMTs that are hoped to deliver a step-change in performance.

The ICS also develops sensors for healthcare. Arathy Varghese briefly discussed efforts at developing devices based on the GaN HEMT that could detect cancers and provide personalised healthcare in homes.

Attendees at the official opening of the Translational Research Hub were also given a tour of the premises. This included a visit to the lab that provides high-frequency measurements of III-V devices, where the current focus is on investigating the characteristics of GaN RF devices. This lab has expertise in measuring very high frequencies, and identifying driving conditions that match harmonics to enable exceptional efficiencies.



Visitors were also taken to a lab that provides on-wafer optical characterisation of light-emitting devices. As well as characterising VCSELs, this group has developed techniques to investigate the performance of edge-emitters, by etching into the epiwafer.

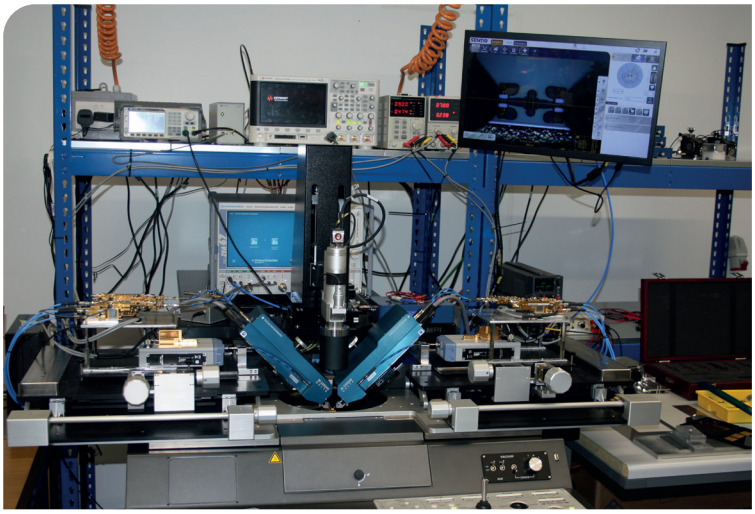
➤ On-wafer measurements of VCSELs and edge-emitting lasers are undertaken at the ICS.

In addition to the capability to measure devices, the ICS is able to make them. There's an MBE reactor within the university, and ICS partners with IQE for epiwafers produced by MOCVD, which can be grown at the company's St Mellon's facility that is now focusing on development runs.

Processing of devices into epiwafers takes place in the cleanrooms at the ICS. The institute has an extensive range of tools, with the capability to define structures, deposit contacts and add passivation materials, including via atomic layer deposition. Dimensions, defined by photolithography, could soon be extended to the nanometre scale, thanks to the delivery of an electron-beam tool.

It's clear that the move into this well-designed and equipped building is enthusing those working there. The have waited a long time – but it's been worth it.

➤ There is tremendous expertise in high-frequency measurements at the ICS.



Streamlining SiC substrate production

A breakthrough tool delivers pinpoint accuracy when producing wafer-ready SiC pucks

BY JEFF GUM FROM HARDINGE

INEFFICIENT and costly. It is those two words that best describe the traditional approach to shaping SiC boules.

However, there's now a new era for producing the wafer-ready SiC crystals. It began in late 2022, when our team at Hardinge introduced the BoulePro-200AX. With its single step dual-plane compensation capability, it is streamlining the SiC industry's process for transforming an as grown boule to a wafer-ready puck. Our launch of the BoulePro could not have come at a better time, given the incredibly high level of demand for SiC, which is the vital semiconductor material for the advancement of electric vehicles and other high growth markets.

There are a number of reasons behind the SiC industry's need for a new method for boule shaping. Concerns come from the inefficiencies of using multiple tool sets to perform different functions, as well as the need to employ several operators to work these tool sets; the time lost to gluing and de-gluing boules to carriers for different steps; the increased process variation that comes from manual material handling and setups; and a lack of best practices driving optimisation and improvement.

With 130 years of grinding and materials knowledge, our development team, supported by key SiC industry experts, has addressed all the inefficiencies of SiC boule processing by creating a comprehensive and cost-effective package. Our process optimisation enables significant cost reduction across the board, including consumables, OpEx, and CapEx.

For the last couple of years, we have been collaborating with a handful of SiC raw material suppliers to optimise the production process for fabricating a wafer-ready SiC puck. Drawing on deep experience in grinding, turning, milling, and

workholding, we have slashed costs through the optimisation of the right processing speeds, angles, workholding and machining tool types, as well as the incorporation of X-ray metrology into the machine.

Efficiency improvements

Our BoulePro 200AX, with its manufacturing capabilities, checks all the boxes for improved process flow. This fully automated, self-contained machine tool can process as-grown SiC boules to wafer-ready pucks with no gluing/fixturing, external material setup or manual intervention.

Another strength of our BoulePro is its single step, dual plane compensation capability, enabled by inclusion of integrated X-ray diffraction. Thanks to this feature, the BoulePro carries out all the steps of the boule-to-puck conversion process in a dramatically shortened period.

The traditional process flow for transforming a boule into a SiC puck can be adjusted from customer to customer, and from boule to boule. However, in general it begins with a manual or automated boule load, followed by machining the initial outside diameter, applying a rough dome grind and assessing the crystal orientation with X-ray diffraction. After this, a finish dome grind corrects the orientation, prior to handoff to a secondary workhead, seed side removal, a confirmation measurement by X-ray diffraction, the application of a final outside diameter and flat/notch, and finally manual or automated removal of the wafer ready puck (see Figure 1 for an illustration of this process).

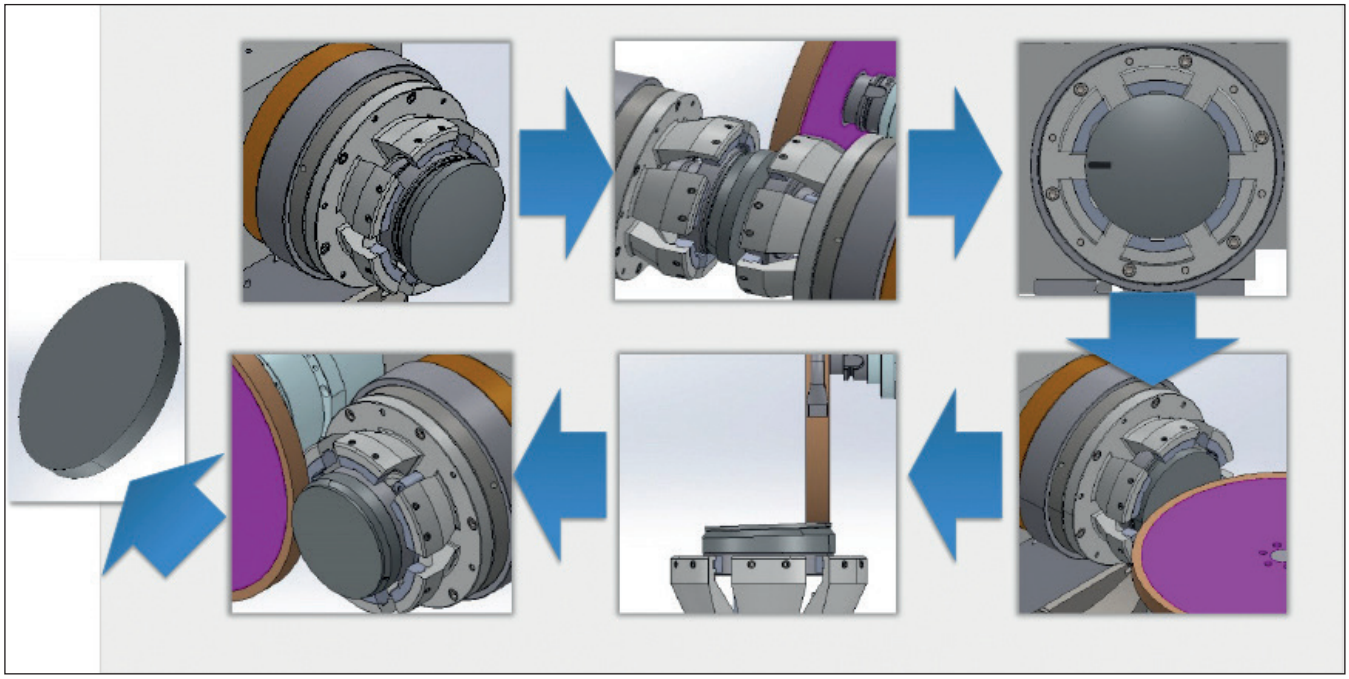
The BoulePro slashes the time it takes to process a boule into a puck. While traditional approaches take over 24 hours, with the BoulePro it's just 2-3 hours, using an automated single setup solution. This saving in time contributes to a total cost reduction of nearly 70 percent, when taking labour, manufacturing footprint, scrap, capacity efficiency, and consumables into account (for details, see Figure 2). This gain will play a key role in helping SiC producers to reduce their production costs and grow the industry utilisation of this wide bandgap material.

The secret sauce

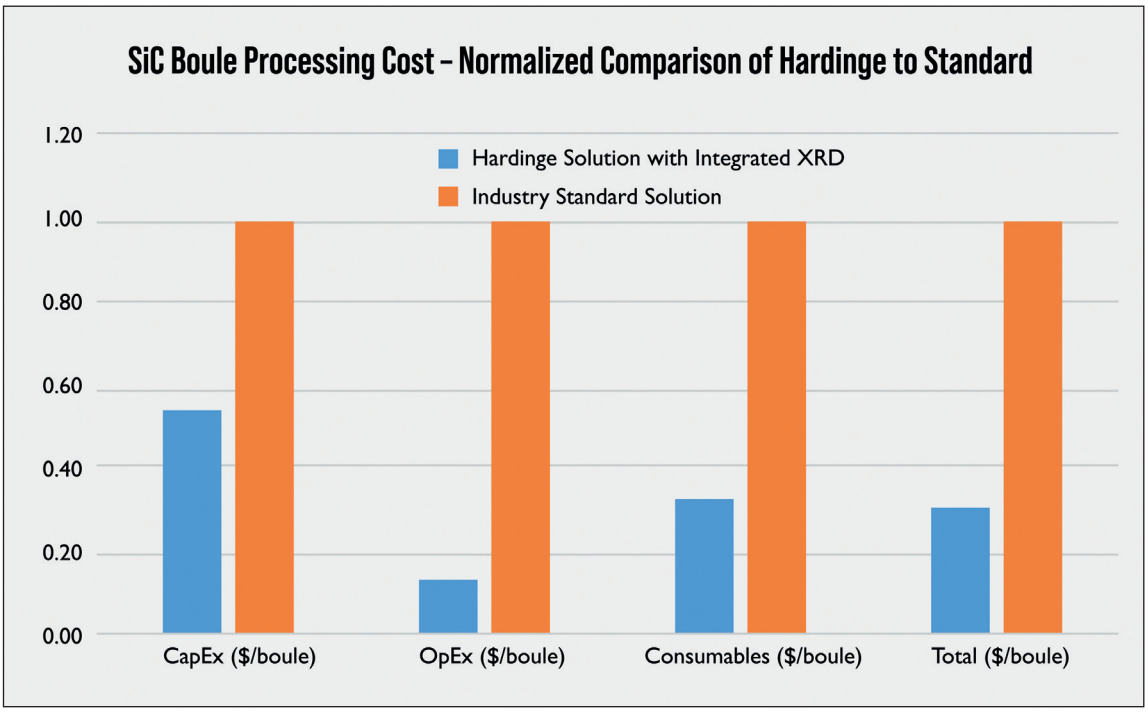
Without an industry standard Process of Record to produce wafer-ready SiC pucks, manufacturers have turned to individual approaches. In all cases, they employ a five-step process that begins by using X-ray diffraction to determine the crystal structure for the correct surface orientation, before applying a flat or notch. Outside diameter grinding follows, and then the removal of the seed side and the dome side.

Our experts have evaluated the steps in this process and their inherent inefficiencies. Drawing on our background as an international provider of customised grinding solutions, we have embarked on a clean sheet approach to an all-in-one solution, leveraging core expertise from more than a century of grinding experience.

The result of this effort, the BoulePro, is built on our industry leading USACH grinding machine platform. It features an integrated X-ray diffraction tool and



➤ Figure 1. The general process flow for producing a SiC puck is: boule load (manual or automated); application of the initial outside diameter (OD); rough dome grind; XRD taken; finishing the dome grind to the correct orientation; handoff to secondary workhead; seed side removal; XRD to confirm; a final OD and flat/notch; and removal of the wafer-ready puck (manual or automated).

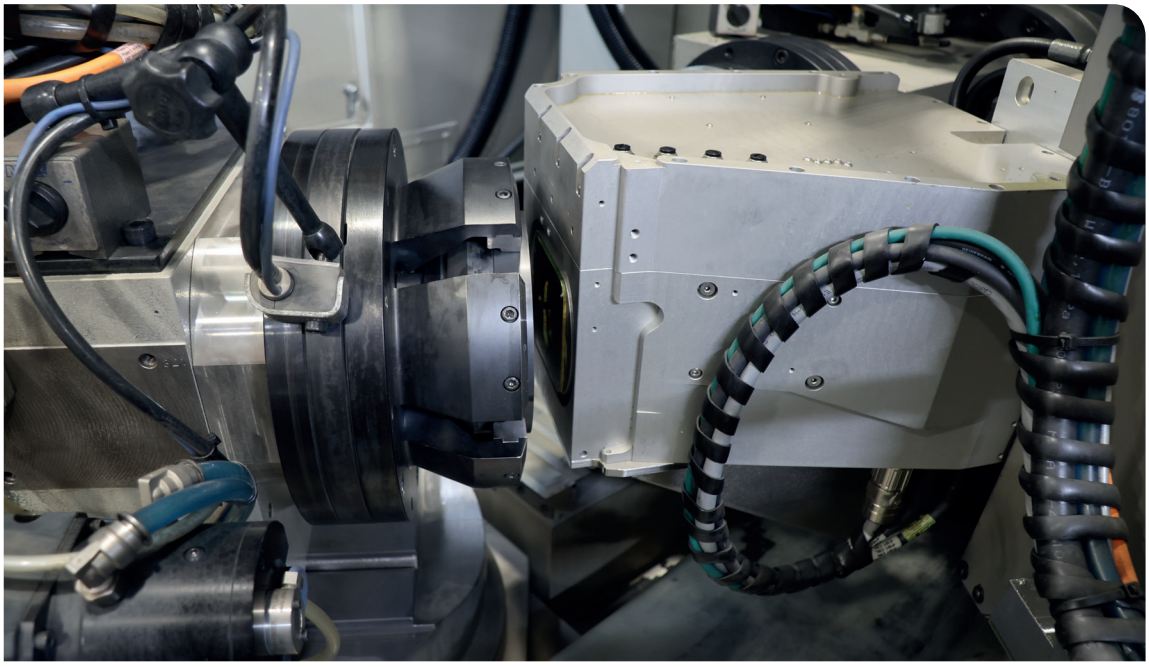


➤ Figure 2. The use of the BoulePro-200AX slashes CapExc, OpEx and costs associated with consumables.

a 5-axis capability, which enables it to orient, X-ray, grind, and/or cutoff the part to the customer's desired specifications. This is accomplished with full automation. Note that the BoulePro is capable of handling all current relevant sizes of SiC boule, including 100 mm, 150 mm and 200 mm material. Key to the exceptional efficiency of our tool is its advanced workholding of the SiC boule. There is no longer a need to glue and de-glue the boule to fixtures throughout each of the process steps – that is a major, incredibly time-consuming issue that current SiC producers face. In addition, the BoulePro eliminates the removal of the boule from one machine, along with its preparation for the next step and its installation in another tool.

An imperative component of the BoulePro is the integrated X-ray diffraction system. It's essential to identify the crystal orientation, which is needed to ensure the proper placement of the primary flat or notch, and to machine the puck with the correct compensation in all planes. By taking this approach the full puck, from end to end, yields wafers with the correct orientation and geometry. With the BoulePro, the output from the X-ray diffraction system informs the tool of the location of the flat or notch, and how much of an adjustment must be made to crystal surfaces when final machining.

Another advantage that results from having the ability to perform X-ray diffraction analysis *in situ*,



➤ The Boule in the workholding on the left and the XRD (X-ray) machine on the right. The XRD is measuring the crystal orientation so that it is known and can be corrected in subsequent grinding steps.

➤ The prototype machine in Elgin, IL that is being used for further development and customer demonstrations.

at any step the process allows, is the opportunity to switch the order of the process steps. One consequence is that the flat or notch can be applied later in the process, ensuring its orientation is highly accurate.

Additional capabilities

There's more to the BoulePro than what meets the eye. Along with its featured proficiencies, additional capabilities can be included upon request.

One of these is the identification of foreign polytypes by UV light inspection. When SiC boules are placed under UV light, certain foreign polytypes, such as 6H, show up as a different colour. Identifying the location of the 6H inclusions allows their removal by the BoulePro, ensuring that the final SiC puck contains only the desired 4H polytype.

It's also possible to add the capability to apply a laser scribe to the surface of the finished SiC puck. This allows customers to track the lot number, the boule number, and so on. It is a feature that is valued for material tracking purposes.

Another capability that can be included within the BoulePro is a vision system. This can take high end photos of the boule or puck at any stage of the process, a feature desired by some customers.

Embracing the BoulePro

This year customers from all over the world have been visiting our facility in Elgin, Illinois, to see the BoulePro in action. This facility is home to our USACH brand of specialised application grinding machines. Our team of engineers and application specialists at this facility drew on their expertise to quickly get a prototype BoulePro up and running to demonstrate this machine's capability. Visitors to the facility are now seeing how the production of SiC pucks can be undertaken with the final design of this machine, which we expect to ship later this year. Even in its prototype form, customers are eager to see the BoulePro in action, given the market's rapid expansion. These visitors want to see first-hand how the BoulePro can accommodate their unique boule geometry through a full production process. After seeing what it can do for them, they leave with a spring in their step, excited by both the flexibility of the BoulePro, and how well our engineering and application experts adjust to their demands.

One area that has amazed our customers is the precise accuracy of the BoulePro, with its built-in X-ray diffraction machine. Due to the flexibility in the order of operations for the BoulePro's process, and as all parameters are controlled extremely tightly, our machine produces the angular correction on crystal orientation up to 100 times more accurately than the manual process currently used today. What this means for SiC producers is that they can meet and even exceed customer expectations and requirements as specifications evolve.

The BoulePro's bright future

Exciting times lie ahead. We have expansion plans underway to cater for increased volumes, given the market's overwhelming excitement for the BoulePro. Demonstrations are ongoing throughout 2023, with the first batch of customer machines scheduled to ship before year-end. We will utilise our global footprint to meet customer demand and aftermarket need, to ensure that our BoulePro supply and support services match customer requirements.

SiC presents unlimited opportunities in many other growth markets as well, and our BoulePro's general configuration and capabilities enable it to be a solution for these applications. We are excited to be at the forefront of this revolution, and viewed as a reliable trusted manufacturing partner that global SiC producers can count on for their fabrication needs.

Evaluating the pros and cons of power GaN

Switching to a vertical architecture addresses concerns associated with on-resistance and capacitance, but the choice of substrate involves compromise

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE OUTLOOK for the GaN power device is incredibly positive. Spurred on by ramping revenues for power supplies in the consumer, telecom and datacom sectors, sales are sure to rocket over the next few years. According to the French market analyst Yole Intelligence, total revenue is going to eclipse $2 billion by 2027 – that's massive growth, considering sales in 2021 were worth just £126 million.

Yet despite all this success, GaN power devices are far from perfect. The harsh reality is that there are many opportunities for improvement. And while some progress might be baked into the upbeat forecast by Yole, it is clear that the more that's done to eradicate weaknesses, the better the long-term prospects for this class of power electronics.

At this year's CS Mantech, held in Orlando, Florida, in mid-May, the most noteworthy weaknesses of the GaN power device were discussed in detail by Mariko Takayanagi, a Senior Manager from Toshiba Electronic Device and Storage Corporation. Several speakers that followed Takayanagi discussed switching to a vertical architecture, which is one option for addressing some of the weaknesses of the traditional power device. Those pursuing a vertical architecture include: Travis Anderson, from the US Naval Research Lab, who detailed the scalable manufacture of planar and vertical *p-i-n* diodes; Dinesh Ramanathan from NexGen Power Systems, who outlined what is claimed to be the world's first commercially available GaN-on-GaN technology; and Eldad Bahat Treidel from FBH, Berlin, who described efforts to develop and characterise high-quality drift regions in vertical devices.

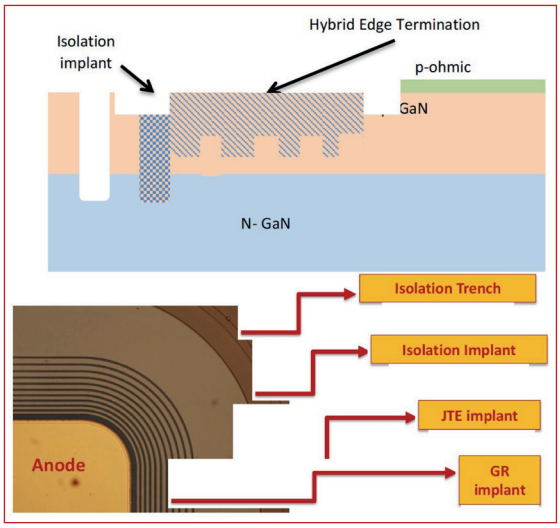
➤ Bristol University's Martin Kuball chaired this year' s CS Mantech. Taking over the reins for 2024 is Peter Ersland from MACOM.

Lateral limitations

Takayanagi, who works for one of the largest and most established makers of power devices in the world, pointed out that according to market forecasts, for the next few years sales of SiC devices will be worth far more than those for GaN, despite the latter having superior potential, based on Baliga's figure of merit. The reason for this, argues Takayanagi, is that circuit designers cannot simply swap a silicon power device for one made from GaN.

Two of the great strengths of GaN are its very high values for mobility and saturation velocity. Together, they ensure that devices made from this material switch at frequencies that are more than an order of magnitude higher than those of silicon incumbents. Switching at far higher frequencies is a very valuable asset, because it tends to enable the introduction of far smaller passive components, particularly inductors and transformers. In turn, this enables a trimming of the size of electrical units. What's more, reverse recovery losses are close to zero, thanks to the non-existence of an anti-parallel body diode. This ensures that a low switching loss is even sustained at high frequencies.

The upshot of all these merits is the possibility to produce power-conversion equipment that is relatively small, while operating at very high power densities and efficiencies. All these strengths are valued by the designers of AC adaptors, micro-invertors, server power supplies and 5G/6G base stations.



➤ Figure 1. The architecture (top) and an optical image (bottom) of the vertical *p-i-n* diodes developed at the Naval Research Laboratory, in collaboration with researchers at Vanderbilt University and Sandia National Labs.

Unfortunately, increasing the switching frequency with the introduction of GaN devices can bring its own problems. When moving to megahertz switching, electromagnetic noise may arise in regulated frequency domains. Rules are in place for good reason, as noise suppression is needed to avoid the erroneous turn-on of GaN power devices – if this were to happen, it could lead to a ground fault in power electronic equipment.

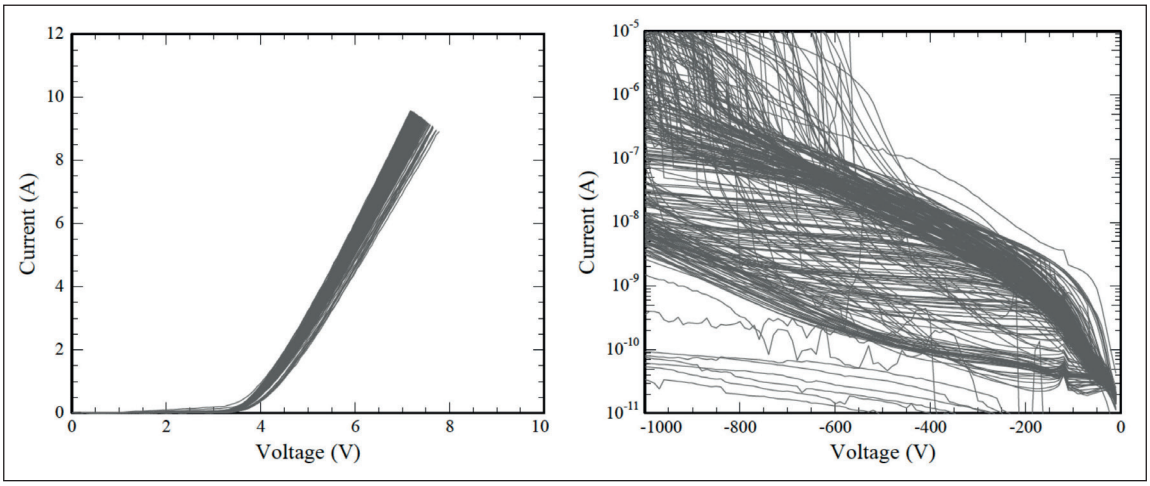
According to Takayanagi, the solution to combining a high efficiency at a high switching frequency with low noise generation is to minimise parasitic inductances and capacitances. This can be realised by placing the gate drive and the GaN power semiconductors as close to one another as possible, while minimising the parasitic inductances between the device terminals of a discrete power device.

It is a requirement that is included in what Takayanagi considers to be the three key criteria for the GaN power device, judged from an application viewpoint. These three pillars are: the need for a low on-resistance and parasitic capacitance, to ensure good switching characteristics, low energy loss and low noise; a threshold voltage that's above around 2.5 V, so that the device is immune to noise and will provide fail-safe operation; and a low overall cost.

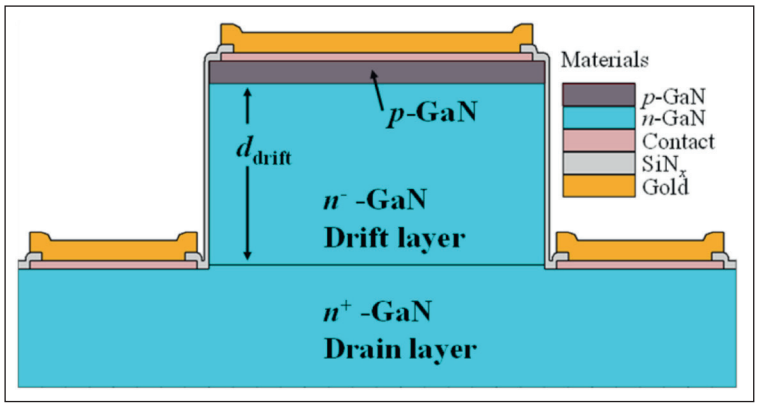
The three classes of GaN power devices on the market today are different forms of HEMT. There is the normally-on transistor, which may also be described as a depletion-mode device; the normally-off transistor, also known as an enhancement-mode device; and the cascode variant. Takayanagi has evaluated the pros and cons of these three designs of HEMT.

Merits of the normally-on transistor, which is on when the gate is biased to zero, include a very high mobility and a zero reverse recovery capacitance, traits that are preferable for high-frequency switching. However, this class of HEMT has a threshold voltage around -10 V, with less than -15 V required to ensure turn off. According to Takayanagi, having the device on at zero gate bias is fatal for power conversion applications, as it requires engineers to put great effort into designing circuitry and gate control, to ultimately ensure safety. The additional circuitry increases parasitics and costs. Due to this, normally on HEMTs are unable to provide high efficiency, high power density and low noise.

Introduced to address issues surrounding the normally-on HEMT is the variant with a cascode configuration. In this case, the normally-on HEMT is connected in series to a silicon low-voltage MOSFET – the source terminal of the MOSFET is connected to the gate terminal of the normally-on HEMT. As a commercial gate driver may be used, there are no concerns relating to cost. But there are concerns associated with the reverse recovery capacitance and the additional on-resistance of the low-voltage MOSFET. It's possible to address these weaknesses by changing the configuration of the MOSFET and HEMT, but that introduces special drivers, additional



➤ Figure 2. Vertical *p-i-n* diodes under forward and reverse bias have uniform turn-on characteristics, but a very broad distribution in breakdown behaviour.



➤ Figure 3. The reverse bias of a FBH Berlin *p-n* diode with a drift region doped to 4 x 10^{16} cm^{-3} shows avalanche behaviour.

components, a power supply and the need for sophisticated control. The third class of commercial HEMT, which is described as normally-off, promises to be the ultimate solution to all three of Takayanagi's criteria. This mode of operation may be realised with a *p*-GaN gate, which is unfortunately sensitive to over-voltage. Addressing this particular weakness is the commercially available hybrid-drain embedded gate injection transistor, which maintains zero recovery capacitance and is blessed with an on-resistance that is considerably lower than that of cascode devices. However, the threshold voltage is less than +2 V, which is just shy of what a power electronic engineer desires, according to Takayanagi. This means that there is the threat of erroneous turn-on. Additional concerns are the need for a dedicated driver to provide a current source, and some reliability issues, such as instability due to trapped charges.

➤ The winner of this year's CS Mantech 2023 Best Student Paper Award went to Yulin He for her paper *Hybrid Etching Process on Type-II GaAsSb/InP DHBT for 5G and Millimetre-Wave Power Amplification*.

To enable GaN transistors to fulfil their potential, demonstrated by their excellent value for the Baliga figure of merit, Takayanagi suggests a need to switch to a different device architecture that combines a high threshold voltage with a low on-resistance and a low capacitance.

Offering promise on all these fronts are vertical GaN transistors. Ideally they are grown on a native foundation, as they require thick drift layers, so demand lattice matching of the substrate and epistructure.

Pilot production

In the US, a collaboration that's led by the US Naval Research Laboratory and includes researchers at Vanderbilt University and Sandia National Labs, has established a pilot production line for producing vertical GaN diodes. A major motivation for this work is to address significant challenges that are holding back the mass production and widespread adoption of vertical GaN devices. According to the team, the relationship between substrate specifications and device performance is not well understood, ion implantation technology for selective-area *p*-type doping is not reliable, and there is a poor understanding of device failure mechanisms, due to a lack of large data sets from electrical stressing.

Efforts by the partnership have focused on a comprehensive study of incoming metrology and wafer mapping. The team has developed a fully planar device process for making diodes, which can be scaled to provide practical voltage and current levels – the target is 10 A and 1.2 kV.

Key accomplishments by the team include establishing pass/fail criteria for incoming epitaxial layers, and identifying the impact of substrate and epiwafer defects on device performance. To succeed in this endeavour, they are producing a large quantity of devices, with more than 500 coming from every wafer. By employing a constant process, the engineers can directly probe the effect of scaling to large-area devices and to layers designed for higher voltage operation, such as 3.3 kV.

The pilot line uses 50 mm free-standing GaN wafers. Spokesman for the team, Travis Anderson from NRL, accepts that this size is not ideal for cost-effective high-volume manufacturing. He told *Compound Semiconductor* that high volume fab infrastructure available for supporting 50 mm wafers is not really available, and yield suffers when attempting to make devices of practical size – that is, greater than 1 mm^2 – due to the limited available area.

"At 100 mm it becomes much more feasible for a

true production environment," added Anderson. "However, 50 mm is more than sufficient for a manufacturing demonstration to evaluate process stability in an R&D environment, which was the goal of our efforts."

There are concerns related to the cost, size and level of availability of GaN substrates. "I do not think the cost is prohibitive, particularly as 100 mm wafers are emerging," argues Anderson, who says that over the course of his collaboration's four-year programme, they have seen a significant shift in the economics of GaN wafers. "Even though the price has only modestly decreased, the quality and uniformity of the wafer has improved substantially, which improves our process yield." During the project, the team had no difficulty securing wafers from multiple sources. However, it should be noted that the total number of wafers they have used is not that high.

Anderson and his co-workers used their line to produce 1.2 kV diodes with an 8 μm-thick drift layer doped to 1 x 10^{16} cm^{-3}, and 3.3 kV variants with a 25 μm-thick drift layer doped to 4 x 10^{15} cm^{-3}. These devices featured an anode with dimensions varying from 300 nm to 500 nm, and a doping level from 3 x 10^{17} cm^{-3} to 2 x 10^{19} cm^{-3}.

"The *p-i-n* diode is an ideal test vehicle to understand the fundamentals of a GaN *p-n* junction," says Anderson. "Since the *p-n* junction is the building block of more complicated diodes and FETs, we chose to study the *p-i-n* diode first as a test vehicle to prove that we can reliability make high quality *p-n* junctions, evaluate edge termination processes, and study scaling to high current before moving to more complex three-terminal structures."

The metrology applied to the incoming wafers includes: C-V mapping with a mercury probe, to calculate doping and uniformity; optical profilometry; and X-ray diffraction mapping. The optical profilometry data is analysed with a machine learning algorithm that identifies bumps, pits, and regions of high roughness.

Anderson says that machine learning has been extremely helpful: "As we worked through the fabrication process, we used machine learning to correlate incoming metrology data to device performance data. By working with these data sets, we were able to develop algorithms to develop the appropriate incoming wafer and epi requirements, screen out wafers that would not yield well, and identify non-intuitive mechanisms that would impact device performance."

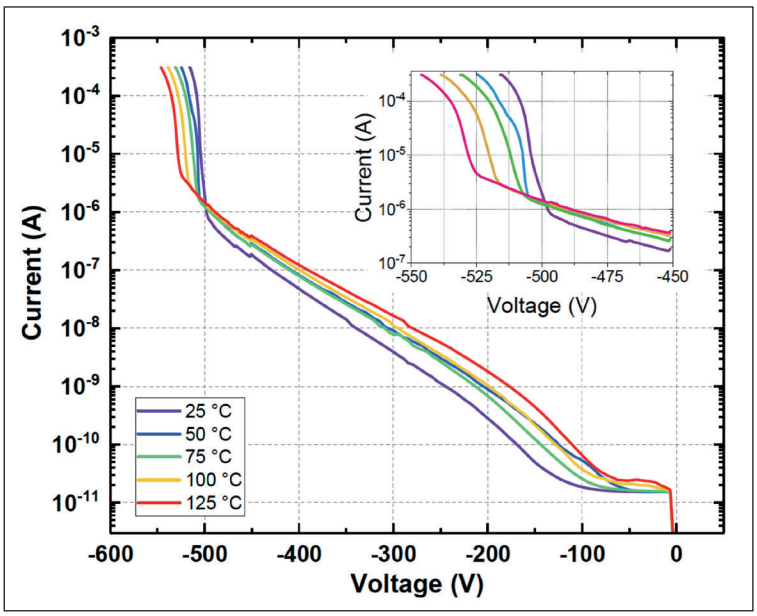
Following metrology, wafers are cleaned, before edge termination is realised using a multi-step nitrogen implant box file. This step isolates devices through the *p*-GaN layer and forms an edge termination region that utilises the hybrid structure, which consists of a junction termination extension region, with guard regions superimposed via a spacer layer (see Figure 1). After cleaning, a front side *p*-ohmic metal contact and a backside *n*-ohmic metal contact are deposited.

Electrical measurements under forward bias have produced varied results. On an exceptional wafer, diodes have a highly uniform turn on, a low leakage and high current capability (see Figure 2 (a)). This is said to be indicative of a high-quality *p-n* junction and relatively few pinholes in the film. However, on inferior wafers many devices suffer from premature turn-on, due to shorting of the anode metal to the substrate. This is caused by pinholes in the epitaxial layer, due to particles introduced in the growth process.

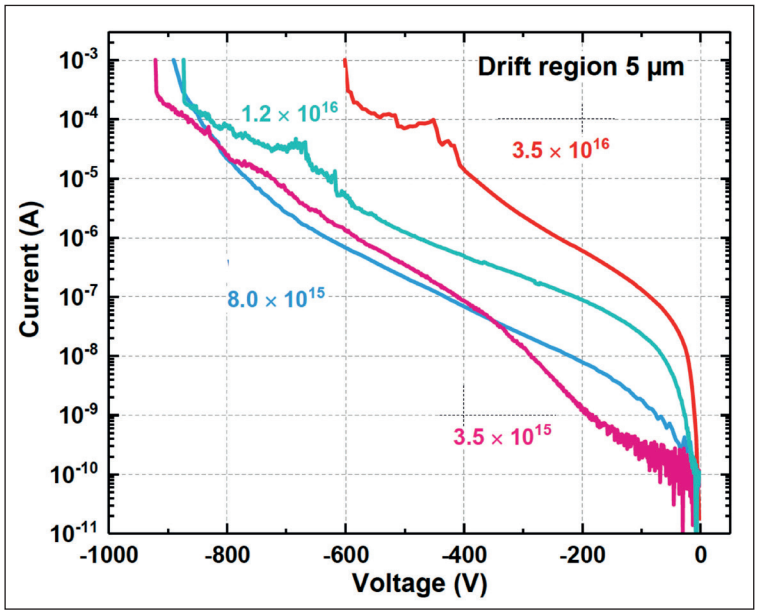
Anderson and co-workers find a very broad distribution in the breakdown behaviour of their diodes (see Figure 2 (b)). For the best discrete devices, breakdown is 1.4 kV, with a leakage below 1 nA at up to 1 kV. But there are also many devices with a high leakage at a voltage just half that of breakdown.

The team are yet to determine the mechanism behind the wide variation in breakdown behaviour. However, they speculate that it could come from localised variations in drift layer properties, arising from variations in miscut or epitaxial defects.

Efforts have been directed at optimising the edge termination design, critical to realising an abrupt avalanche breakdown. The team varied the anode thickness, which ensured a systematic variation in the thickness of the remaining *p*-GaN layer. This led them to discover that they could slash the leakage current under reverse bias by more than two orders of magnitude by thinning the underlying *p*-GaN layer to less than 10 nm.



➤ Figure 4. The reverse bias of a FBH Berlin *p-n* diode with a drift region doped to 4 x 10^{16} cm^{-3} shows avalanche behaviour.



➤ Figure 5. For *p-n* diodes with a drift region doped to 3.5 x 10^{16} cm^{-3}, plots of reverse bias reveal a hard breakdown.

Encouragingly, the team can report two observations that are consistent with avalanche breakdown. One is an increase in the breakdown voltage at elevated temperature; and the other is the moving of an electroluminescence spot from the edge of the isolation implant to the edge of the anode.

Anderson and his colleagues noted a substantial variation in diode performance from wafer-to-wafer. This is attributed to either variations in the epitaxial layers, such as drift layer doping or anode doping, or to differences in the back side of the wafer.

The team have also investigated packaged devices, developing a surface mount process using a commercially available package and outsourced mounting and wire bonding. Following packaging, devices are encapsulated with Hysol. This led to improved performance and no device degradation, benefits that are attributed to passivation.

Having completed fabrication of many devices, one of the plans for the team is to work with circuit designers to evaluate devices in practical applications.

"I am also interested in probing device reliability to understand failure mechanisms," adds Anderson. "Finally, I see large-area devices as a challenge and am interested in continuing to scale device size."

Commercialising GaN-on-GaN

Details of what is claimed to be the world's first commercial GaN-on-GaN power technology were described by co-founder of NexGen Power Systems, Dinesh Ramanathan. This Californian outfit, which is now sampling 700 V and 1200 V enhancement-mode JFETs – full production is slated for later this year – boasts that its devices have a superior breakdown voltage and current capability for a given chip area up to 4 kV, compared with any other GaN device, as well as low capacitance and switching losses. Other attributes are said to include: repeated cycle avalanche robustness, thanks in part to the *p-n* junction; a best-in-class temperature coefficient; and the smallest size, compared with other power semiconductors, for a given current rating.

Ramanathan discussed solutions to many of the challenges associated with the manufacture of GaN-on-GaN devices. To enable high-volume manufacturing, NexGen employs widely available manufacturing tools, modified to handle the transparent, fragile GaN substrates. The company is working with substrate vendors to improve substrate characteristics, such as surface finish, flatness and the level of macro-defects. In addition, efforts are directed at improving NexGen's epitaxial process, as well as etching and cleaning techniques that can aid the quality of the regrown junction, and the development of novel test structures to improve quality control.

Developing drift regions

A key element in vertical power devices is the drift layer. Evaluating its characteristics using a full device structure is a time-consuming process, so to speed this assessment a team from FBH, Berlin, have been developing approaches based on the use of process control measurement (PCM) structures.

At last year's CS Mantech FBH's Eldad Bahat Treidel outlined a PCM structure for measuring the drift region conductivity, and at this year's meeting he detailed further progress – values for the blocking strength are now possible.

Treidel told *Compound Semiconductor* that the time it takes to produce a PCM structure is just a third of what it would take to fabricate a complete transistor. What's more, it is simpler and cheaper. "For example, process and full wafer characterisation of a PCM structure would require 6 lithographic layers as compared to a full transistor process with 12 to 15 lithographic layers."

In the work described in Orlando this May, Treidel produced *p-n* diodes that target avalanche behaviour, which is a desirable attribute, as it combines the maximum blocking in the drift region with the highest conductivity.

"In addition, avalanche breakdown is controllable, repeatable, can be predicted and it's nondestructive and recoverable," adds Treidel, who points out that these strengths enable a significant reduction in the device design margin between the rated voltage and the real breakdown voltage. "Further, [avalanche] improves short-circuit robustness and ruggedness."

The team produced its *p-n* diodes on sapphire substrates. They have been developing vertical GaN-based power devices on foreign substrates, such as sapphire and silicon, through a Europen project called YESvGaN. As well as issues associated with wafer bow, substrate removal

Solutions for Compound **semiconductor passivation**

ZnSe
SiN
Oxide

RIBER's **CPS passivation tools**

UHV environment for solving the oxidation issues

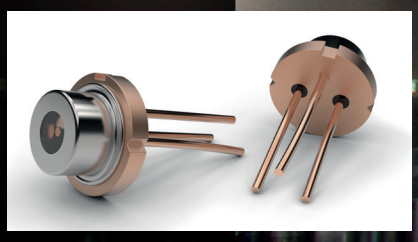
LASER FACETS PASSIVATION

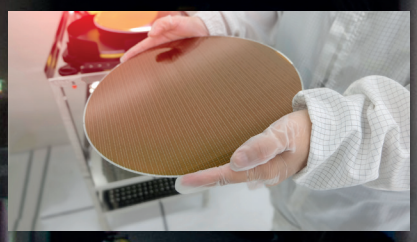
MESA-SIDEWALLS PASSIVATION

COMPOUND SEMICONDUCTORS PASSIVATION

In collaboration with

comptek solutions





RIBER

INNOVATIVE SOLUTIONS FOR SEMICONDUCTOR INDUSTRY

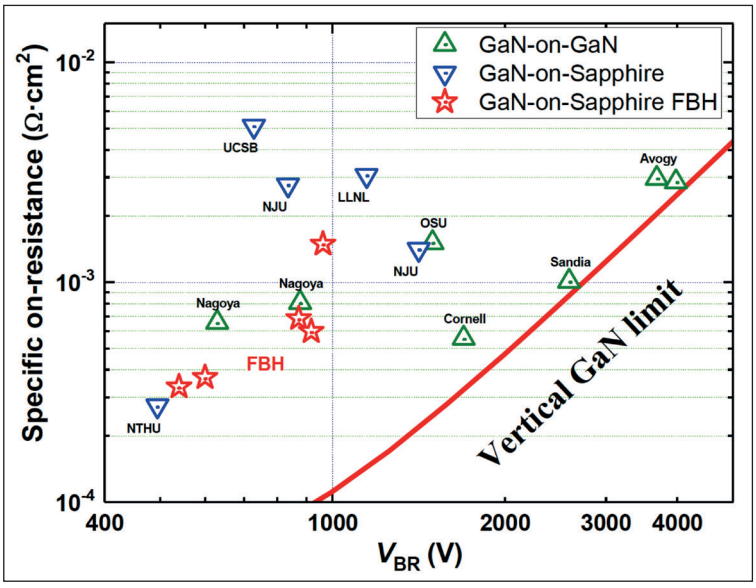
info@riber.com
www.riber.com

Those at FBH will be developing a number of gate module technologies, such as trench MOSFETs, finFETs and finJFETs. It is possible to integrate these technologies on native and foreign substrates

and processing of membranes, they have had to consider the high defect density in the drift layers that threatens to limit the blocking strength, reduce the conductivity of the drift layer and impact channel inversion.

None of these issues have proved showstoppers for Treidel and his colleagues. "In the frame of this project we have demonstrated high-quality epitaxial layers with avalanche capability and low resistivity for both GaN-on-sapphire and GaN-on-silicon."

The engineers at FBH fabricated diodes from five GaN epistructures with drift regions with different doping concentrations, all grown on 100 mm sapphire substrates. All these variants, grown by MOCVD, had epitaxial stacks consisting of a 2.2 μm-thick unintentionally doped GaN buffer layer, a 2.4 μm-thick highly conductive drain layer, and a 5 μm-thick drift layer. After determining the doping concentration of the drift layer by electrochemical capacitance-voltage measurements, these structure were loaded into another MOCVD reactor, where a 500 nm-thick layer of magnesium doped at a concentration of 1 x 10^{19} cm^{-3} was added, followed by a 30 nm-thick layer of GaN doped to 2 x 10^{19} cm^{-3}, prior to *in-situ* activation. Quasi-vertical *p-n* diodes were formed from these epiwafers by first applying rapid thermal annealing to remove hydrogen from the *p*-type layers, before using optical lithography and etching to define mesa structures. Ohmic *p*-type and *n*-type contacts were then formed, before the passivation of the mesa edges via plasm-enhanced CVD added 200 nm of SiN (see Figure 3).



➤ Figure 6. The *p-n* diodes fabricated at FBH, Berlin, deliver an impressive performance for variants that have a sapphire foundation.

Electrical measurements on all the devices determine that it is just the variant with the highest doing in the drift region – it's doped to 4 x 10^{16} cm^{-3} – that exhibits avalanche behaviour (see Figure 4). The other four, with doping in the drift region varying from 3.5 x 10^{16} cm^{-3} to 3.5 x 10^{15} cm^{-3}, undergo a non-avalanche hard breakdown (see Figure 5). According to the team, these findings indicate that as the concentration of doping in the drift region reduces, there is a shift from the parallel plane junction (avalanche) regime to the punch-through breakdown limit.

Triedel and co-workers have benchmarked their devices against other *p-n* diodes on GaN and sapphire substrates (see Figure 6). It is claimed that the device with a 1.2 x 10^{16} cm^{-3} level of doping in the drift region offers excellent blocking performance, with a hard breakdown of 920 V, a drift region specific resistance of 0.57 Ω cm^2, and a power figure of merit of 1.43 GW cm^{-2}.

One of the team's next targets is to develop the growth of GaN layers that are as thick as around 15 μm on sapphire substrates, because this will enable devices to block more than 1.5 kV while exhibiting a specific resistivity of around 1 mΩ cm^2. "For this we have developed a strategy to reduce the internal built-in strain in the substrate, and by that to reduce the wafer bow," says Treidel.

In parallel, those at FBH will be developing a number of gate module technologies, such as trench MOSFETs, finFETs and finJFETs. It is possible to integrate these technologies on native and foreign substrates.

"Our device processing activities for vertical GaN devices on native and foreign substrates will enable us to study the impact of GaN layer material quality on device performance and reliability," adds Treidel. The GaN-on-GaN will also enable the team to investigate the influence of different substrate manufacturing methods, such as HVPE and ammonothermal growth, and compare material supplied by different vendors.

Such efforts will help to advance the capabilities of vertical GaN devices, which offer many advantages over their lateral cousins. Progress on both these fronts may well be discussed at the next CS Mantech, which will take place in Tucson, AZ, from 20-23 May 2024.

HARDINGE®

TURNING | GRINDING | MILLING | HONING | WORKHOLDING | ROTARY

YOUR MACHINE TOOL COMPANY

For over 130 years, our global brands continue to provide solutions for all your precision machining & workholding needs.

Hardinge Boule Pro 200AX

SCHEDULE YOUR MACHINE DEMO TODAY:

(800) 843-8801 | HARDINGE.COM | SHOPHARDINGE.COM

JOIN US AT THESE UPCOMING EVENTS:

July 11-13, 2023
SEMICON WEST

ICSCRM2023
INTERNATIONAL CONFERENCE ON SILICON CARBIDE AND RELATED MATERIALS
SORRENTO / ITALY
17-22 SEPTEMBER 2023

LIVE DEMOS at our ELGIN, IL. FACILITY
Contact us for more details

THE HARDINGE FAMILY OF BRANDS:

BRIDGEPORT
BUCK CHUCK
FORKARDT
HAUSER
JONES & SHIPMAN
KELLENBERGER
OTW
TSCHUDIN
USACH
VOUMARD
WEISSER
WPT

Expanding horizons for deep-UV LEDs

Tremendous progress is underway with the deep-UV LED, in terms of its use in healthcare and it gains in output power, efficiency and lifetime, in both the UVC and far UVC

BY MICHAEL KNEISSL FROM TU BERLIN AND THE FERDINAND-BRAUN-INSTITUT

DEVICES THAT ATTRACT a great deal of attention tend to have breakthroughs on many fronts. As well as a hike in performance, they often undergo improvements in reliability, along with increasing interest from more applications, opened up by superior characteristics. That's certainly the case for the deep-UV LED. Its increasing power and lifetime in both the UVC and the far UVC is attracting interest for fighting hospital germs and airborne viruses.

Reports of progress in all these areas lay at the heart of the third International Conference on UV Light Emitting Technologies and Applications, known as also ICULTA 2023. Held in Berlin, Germany, from 23-26 April 2023, this year's meeting, which attracted more than 220 attendees from 27 countries, was organised by the recently established Advanced UV for Life e.V. association, together with Ferdinand-Braun-Institut (FBH), Berlin, and in collaboration with the International UV Association (IUVA).

Building better devices

Two solid-state lighting heavyweights helping to drive progress in the UVC are ams Osram and Nichia. At ICULTA 2023 representatives from both these chipmakers unveiled their latest developments in UVC-LED technologies, showcasing peak powers in the disinfection band between 260 nm and 280 nm.

Speaking on behalf of ams Osram were Project Manager Marc Hoffmann and Director of Product Management Christian Leirer. As well as outlining the company's advances, this duo delivered an excellent overview on the latest advances in UVC-LEDs, as well as their use in industrial and consumer applications. The application space is now moving from consumer to industrial applications, influencing the requirements for UVC-LEDs. To support this trend, ams Osram is improving the performance of its UVC LEDs. Current products are delivering output powers of up to 100 mW when driven at 250 mA, and have a lifetime of 10,000 hours, judged in terms of L70, which is the time it takes for the output power to fall to 70 percent of its initial value. According to the speakers, the third generation of devices from ams Osram are producing up to 200 mW at a wall-plug efficiency (WPE) of 10 percent.

The company has set itself a very ambitious goal, targeting a WPE of 20 percent by 2026, a L70 lifetime of 40,000 hours, and a pricing level that's just ten times above that of the current cost of the mercury lamp. Such a level of improvement would be revolutionary, ensuring that the cost of a UVC-LED based system is lower than that of a conventional mercury-lamp based system. This rival to the incumbent would also deliver energy savings, alongside enhanced product safety and reliability, thanks to the combination of UVC-LED and UV sensors. Note that this forecast of progress lies within the range that I gave in my presentation (see Figure 1).

Representing Nichia Europe, Managing Director Ulf Meiners offered an interesting comparison between the chronology of WPE increases for the blue and the UVC-LED, noting that both technological developments appear to be on a similar fast-paced trajectory. Meiners didn't present an extended outlook, but forecast that the WPE of Nichia's devices will hit 7.5 percent in 2024, with output power at 280 nm reaching 150 mW.

While many make a direct comparison between UVC-LEDs and mercury lamps using individual performance parameters, Meiners argued that this is not very meaningful. He emphasised the importance of studying concrete use cases that account for the specific properties of UVC-LEDs. For example, it is important to be aware of completely new, more efficient system designs that cannot be realised with conventional UV sources. Merits of deep-UV LEDs that can increase the light utilisation efficiency of the system include point source emission, which enables a tailoring of the source to fit the application, and the opportunity to trim energy consumption – UVC-LEDs are easily dimmable, and can be turned on-and-off rapidly, allowing activation only when it's needed and at the required power level. This point of view was reinforced by Alexander Wilm, Senior Key Expert Applications at ams Osram, who described several use case scenarios in which UV-C LEDs are already outperforming conventional UV-C lamps despite their lower WPE.

An interesting difference between the two heavyweights is the peak wavelength of their UVC LEDs. Nichia is sticking with its 280 nm LED technology platform, reasoning that the reliability of the UVC-LED is higher at the slightly longer wavelength, while ams Osram is focusing on LEDs centred near the germicidal efficiency peak that's around 265 nm.

Competition for the production of class-leading devices is coming from a handful of other suppliers, including Crystal IS, a subsidiary of Asahi Kasai. Delegates at ICULTA were given an update on the capability of these devices by Rajul Randive, Director, Applications Engineering, Crystal IS. Randive revealed record performance levels for the company's 265 nm LEDs, with single-chip output power now as high as 160 mW at 500 mA and maximum WPE reaching 6.5 percent. Unlike most UVC-LED products, those made by Crystal IS are grown on internally produced, low-defect-density bulk AlN substrates. Threading dislocation densities in bulk AlN are many orders of magnitude lower than those found in the heterostructures of UVC-LEDs grown on sapphire. The company attributes the far lower level of threading dislocations to superior device lifetimes. The L70 lifetimes of Crystal IS devices are already reaching 25,000 hours at a drive current of 350 mA.

Far UVC: Improving health...

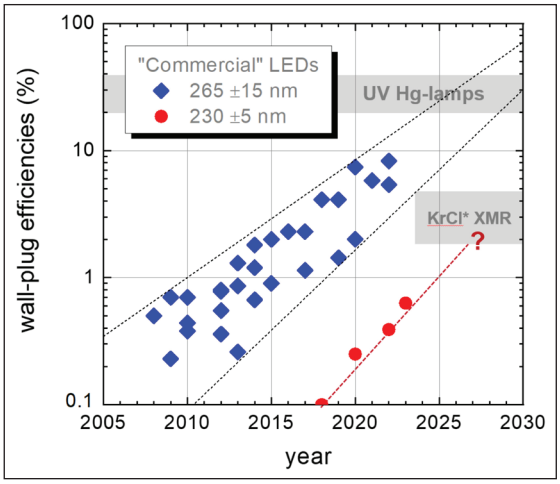
Interest in far-UVC emitters has been boosted by recent, very encouraging studies on *in-vivo* inactivation of multi-drug resistant bacteria, fungi and viruses. Reports of efforts on this front were provided at the latest ICULTA meeting by those working at Columbia University, New York, and Charité – Berlin University of Medicine.

According to David Brenner, Director at Columbia Medical Centre, Centre for Radiological Research, while the effects of the Covid-19 pandemic are fading, there are many other airborne pathogens causing significant infections and death every year, including influenza and tuberculosis. His group has shown that a dose level of just 2 mJ cm^{-2} at 222 nm reduces the viral load by several orders of magnitude for SARS-Cov-2 and other pathogens.

Several experts attending ICUTA 2023 stressed that antimicrobial resistance is one of the biggest health challenges facing humanity. In the US alone 2.8 million people are infected by multi-drug resistant germs every year, and for 35,000 of them this is fatal. Globally, the number of deaths is estimated to be around 1.2 million per year and rising.

The deep-UV LED industry is well-positioned to help save lives. Martina Meinke, Head of Experimental Skin Physiology at Charité – Berlin University of Medicine, explained that far-UVC LEDs emitting at around 233 nm can be an effective and safe tool in the fight against MRSA, MSSA, and other germs.

Meinke's team has already realised very encouraging results from clinical trials on volunteers.



➤ Figure 1. Wall-plug efficiencies for production level UVC-LEDs and engineering prototypes in the 250 nm - 280 nm and 225 nm – 235 nm wavelength bands. Credit: Michael Kneissl/TU Berlin

Left: Some of the key people responsible for organizing ICULTA 2023 were (from left to right): Martin Strassburg (ams Osram, Chairman of ICULTA 2023); Neysha Lobo-Ploch (Ferdinand-Braun-Institut, Program Chair of ICULTA 2023); Michael Kneissl (TU Berlin & Ferdinand-Braun-Institut, Chairman of Advanced UV for Life e.V.) and Sven Einfeldt (Ferdinand-Braun-Institut, Chairman of ICULTA 2021). Photo: T. Rosenthal

Typical dose levels of 40 mJ cm^{-2} show only minor DNA damage in human skin, equivalent to less than 0.1 MED (Minimal Erythema Dose), and there are no signs of DNA damage after 24 hours. Spurred on by these very promising results, Meinke and colleagues are extending the scope of their investigations to additional hazardous germs, including fungi like candida albicans. The group is also starting to investigate the treatment of other parts of the human body, in particular the oral and nasal mucosa.

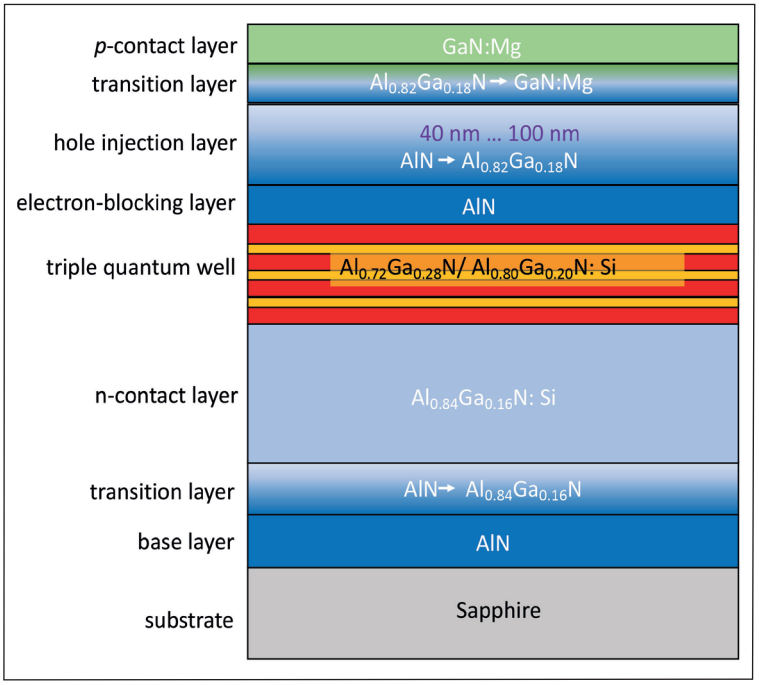


Figure 2. Schematic of a 234 nm LED heterostructure with a distributed polarization doped (DPD) AlGaN hole-injection layer. (Source: T. Kolbe *et al*. Appl. Phys. Lett. **122** 191101 (2023))

Additional work at improving healthcare includes an innovative UVC phototherapy platform for decontaminating chronic non-healing wounds. Involved in this pioneering project is Mark Gerber from Spectrum Medical Technologies. He explained that when they used 235 nm UVC-LEDs from Asahi Kasai to deliver a dose level of 80 mJ cm^{-2}, this led to a 95 percent reduction of MRSA on human skin. Gerber claimed that 235 nm emitters are better than 222 nm excimer lamps for biofilm inactivation due to the slightly deeper penetration depth, while still not causing significant skin damage. Initially, the technique will be used in nursing homes, hospitals and doctor's offices.

... and increasing output power

A number of presentations at this year's ICULTA outlined options for improving the performance of deep-UV emitters. They included a talk by Leo Schowalter, co-founder of Crystal IS and currently a designated professor at Nagoya University, who discussed the pseudomorphic growth of AlGaN heterostructures on low-defect-density bulk AlN substrates. Schowalter made the case for the native substrate, pointing out that despite the significant lattice mismatch between AlN and $Al_{1-x}Ga_xN$, which increases with gallium concentration, threading dislocation densities in the active device region of UVC LEDs grown on high-quality bulk AlN substrates are well below 10^6 cm^{-2}. The lower density of threading dislocations aids all forms of light emitter, with Schowalter arguing that it is behind major performance improvements in far-UVC LEDs, and is to thank for the demonstration of continuous-wave laser diodes emitting near 272 nm. He also mentioned recent advances in the efficiency of sub-230 nm LEDs, with EQE now as high as 0.5 percent. This work has just been published in *Applied*

Discover our NEO series

Innovative plasma-based solutions for photo resist removal, surface cleaning and isotropic etching. Fully automatic multi chamber equipment for high volume semiconductor fabs.

- High & low temperature ashing / descum
- Non critical Isotropic / lite etching
- Post DRIE polymer removal
- Sacrificial release layer removal
- UV Curing & Charge Erase

NEO 200A

NEO 2000

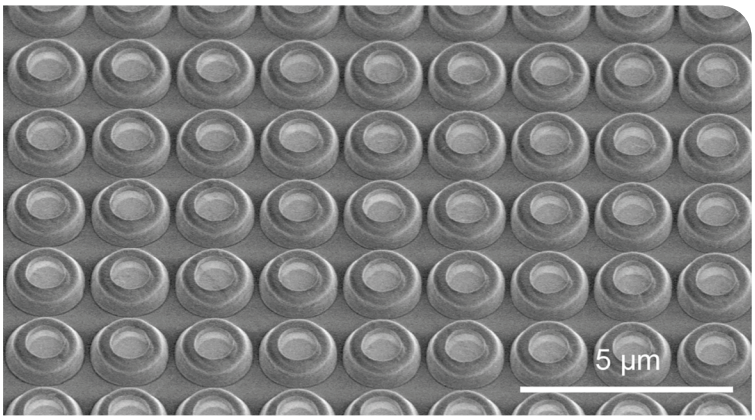
NEO 2400

NEO 3000

NEO 3400

NEO 2000UV

www.trymax-semiconductor.com



➤ Figure 3: Scanning electron micrograph image of UV microLED array with 2 µm pitch. Credit: Ferdinand-Braun-Institut (FBH), Berlin, Germany. Source: https://www.fbh-berlin.de/en/research/research-news/arrays-of-ultraviolet-micro-leds-for-production-sensing-and-communication

Physics Letters (see H. Kobayashi *et al.* Appl. Phys. Lett. **122** 101103 (2023)).

One of the challenges with deep-UV LEDs is the injection of holes into the device. An approach that addresses this and has been adopted by the Ferdinand-Braun-Institut is to employ a distributed polarization doped, hole-injection layer. Discussing devices with this feature, spokesman Tim Kolbe explained that the foundation for their LED heterostructures are MOCVD-grown 2-inch diameter AlN-on-sapphire templates with double growth and double annealing. The team estimates that the threading dislocation density in these templates is around 2.1 x 10^8 cm^{-2}, based on values for the full-width at half-maximum for (00$\bar{2}$) and (10$\bar{2}$) X-ray rocking curves. On the annealed templates the team has grown LED structures that feature an AlGaN multiple-quantum-well active region, a 2 nm thin AlN electron blocking layer, and an AlGaN distributed polarization doped hole-injection layer with an aluminium mole fraction gradient ranging from 100 percent to 82 percent (see Figure 2).

➤ Torsten Jenek from Heraeus Noblelight, the second Program Chair of ICULTA 2023, presented prizes for the best student poster. The winner was Tim Achenbach from the Technical University, Dresden, for the paper *Novel UV dosimetry for surfaces based on the interplay of oxygen and room-temperature phosphorescence* (award collected by colleague Linda Steinhäußer, FEP Dresden, far right). Sharing second place were Iman Roqan (second from the right) from KAUST (*Sub-quantum well effect on the carrier dynamics of Al-rich AlGaN/AlGaN multiple-quantum-well DUV LEC structure grown on AlN substrate*) and Silke Lohan (far left) from Charité – Berlin University of Medicine (*Radical formation in skin at different wavelengths: from UVC to NIR*). Photo: T. Rosenthal

Compared with their visible cousins, light extraction is considerably more challenging with the far-UVC LEDs. Offering a new approach to this are researchers at the Ferdinand-Braun-Institut, who are using microLED arrays to enhance the extraction of far-UVC emitters. Involved with this work is Jens Rass, who told delegates that the team applied precisely tailored plasma etching and metallisation steps to create two-dimensional arrays of UV emitters with diameters down to 1.5 µm and a spacing as short as 2 µm (see Figure 3). Since the emitted light can be redirected by the inclined mesa sidewalls, shrinking the emitter diameter leads to tremendous gains in light extraction efficiency. By carefully selecting and optimising mesa diameters, insulator materials, and mesa sidewall angles, Rass and colleagues have demonstrated record external quantum efficiencies of 1.6 percent for far-UVC microLEDs that incorporate micro-pixels with 1.5 µm diameters and a SiO_2 insulator for sidewall passivation. These 233 nm emitters are capable of output powers of 1.7 mW and 3.5 mW at 20 mA and 50 mA, respectively.

One of the newcomers in the field of far-UVC LEDs is the Australian company Silanna UV. Its team leader for MBE processing, William Lee, spoke to those attending ICULTA 2023 about the company's development of high-power, far-UVC LEDs emitting at 235 nm. The MBE tool at Silanna UV is capable of producing epiwafers up to 6 inches in diameter, and is used to grow LED heterostructures that feature short-period superlattices for the silicon-doped current-spreading layers as well as for the active region. These superlattices, comprised of alternating AlN and GaN layers, extend the spectral range of the transverse-electric-dominant emission, as well as lowering the activation energy of donors. Resistivity can be as low as 0.015 Ω.cm for an *n*-type short-period superlattice that's equivalent to $Al_{0.8}Ga_{0.2}N$. Drawing on this innovation, the team at Silanna UV has fabricated 235 nm LEDs. Driven at 200 mA, these devices deliver an output power of up to 7 mW at a WPE of 0.4 percent. Dialling back the drive current to 20 mA ensures an L70 lifetime of 2,800 hours.

The advances reported at this year's ICULTA underscore the great rate of progress in UVC and far-UVC LEDs, as well as medical treatments based on their emission. Further breakthroughs will follow, with many sure to be reported at ICULTA 2025, which is planned to be held again in Berlin.

MBE: A game changer for GaN-on-silicon RF

On the back of remarkable results at 40 GHz, GaN-on-silicon HEMTs have a tremendous opportunity to serve in mobile applications requiring high-power millimetre waves

BY ANDRE BONNARDOT, ELODIE CARNEIRO AND STEPHANIE RENNESSON FROM EASYGAN AND FABRICE SEMOND FROM UNIVERSITÉ CÔTE D'AZUR, CNRS-CRHEA

DO YOU THINK THAT GaN-on-silicon will be adopted for RF applications? If you asked that question a couple years ago, the answer could well have been along the lines of a cautious yes, tempered by the point that it's hard to know when GaN-on-silicon will have an impact, and to what extent. And there was very good reason for this caution: it is challenging to produce GaN-based heterostructures on silicon with sufficient material quality in a reproductible, reliable manner.

Helping spur the development of GaN-on-silicon RF devices are decisions related to the future of the wireless industry. In March 2022, the 3GPP (3rd Generation Partnership Project) standardisation initiative propelled the 5G millimetre wave spectrum limit to 71 GHz, exacerbating the technical challenge for device manufacturers. The reality is that while it is not going to be easy, deploying millimetre-wave bands is inexorable – that's because higher frequencies are essential for supporting the exponential increase in data traffic created by future 5G advanced networks.

The inevitable march of millimetre-wave standardisation will be challenging for pico-cell and handset vendors. They will be constrained when designing and integrating RF front-ends operating at those frequencies. In turn, this will create a new, high volume, cost sensitive RF device market opportunity for semiconductor manufacturers.

A great candidate for providing the high-power densities at high operating frequencies that's demanded by this application is the GaN HEMT. The

Substrate criteria		GaN-on-SiC	GaN-on-Si
GaN epitaxy difficulty		Medium	High
Substrate mismatch relative to GaN	Thermal Expansion	33%	116%
	Lattice	+3.5%	-17%
Thermal conductivity		4.9 W/cm.K	1.5 W/cm.K
Cost		$$$	$
Size (diameter)		Up to 150 mm	Up to 300 mm
CMOS Compatible		No	Yes
Availability		Geopolitical considerations	Commodity

➤Table 1. While there are technical challenges of using substrates made from silicon rather than SiC for GaN RF devices, there are also significant economic advantages.

most suitable form of this transistor is the GaN-on-silicon HEMT: it is the technology of choice for GaN electronics, and it is already gaining momentum in power electronics applications.

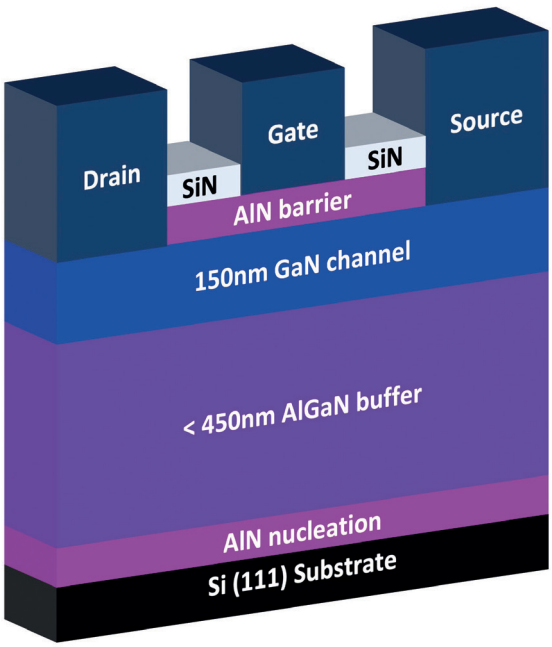
Today, however, the GaN-on-SiC form of the HEMT is the mainstay in RF applications. Compared with the silicon substrate, SiC provides a superior thermal conductivity as well as more compatible lattice and thermal expansion mismatches (see Table 1). These assets make it easier to produce a device delivering high power at high frequencies. But there are drawbacks, in terms of cost, CMOS compatibility, supply availability and large diameter feasibility. Due to this, there is no question that the GaN-on-silicon HEMT will rise to the fore for high-volume deployment, once technological barriers have been removed.

At EasyGaN, a French start-up founded in 2017 by researchers of CRHEA, a CNRS laboratory that pioneered the field of GaN hetero-epitaxy on the silicon substrate, we are helping to accelerate this switch to GaN-on-silicon. Read on to discover how we are using MBE to transform the capability of this class of GaN HEMT in the millimetre-wave domain.

Solving challenges with MBE

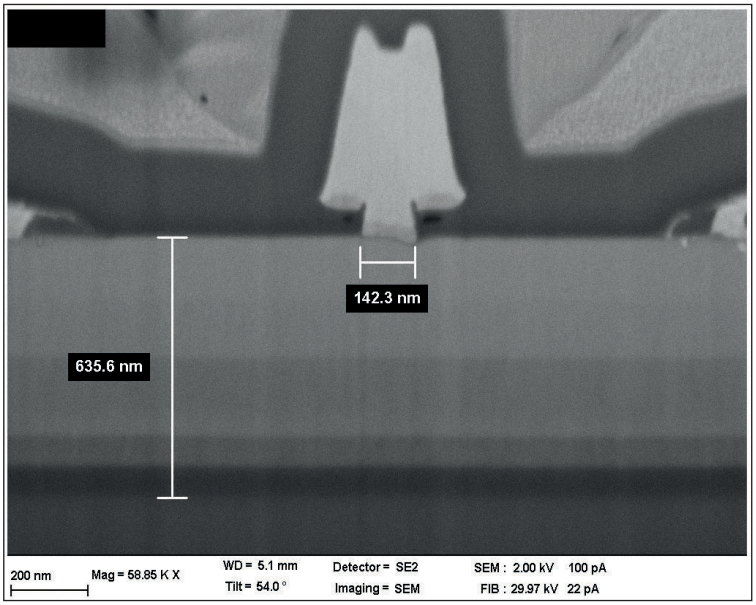
The growth of high-quality GaN-on-silicon is a challenge on a number of fronts. The most well-known difficulty comes from the large lattice and thermal expansion coefficient mismatches, which can lead to undesirable defects, such as a high density of threading dislocations and cracks. In addition, the surface of silicon is highly reactive to many chemicals involved in epitaxial growth. The presence of nitrogen leads to nitridation, gallium causes melt-back etching and aluminium diffuses into the highly resistive silicon substrate. Due to all of this, there are unintentional reactions at the interface between the buffer and silicon, as well as inside the silicon sub-surface. The unwanted consequences include parasitic charges, low buffer resistivity and insufficient thermal dissipation. All threaten to hold back the performance of the GaN HEMT – it can be impeded by RF losses, current degradation over time and reliability issues. Much progress is realised by moving the epitaxial growth technology for GaN-on-silicon from the more common MOCVD to an alternative that is well-established for many III-Vs, MBE. With the latter form of epitaxy, it is possible to obtain very good control of the AlN buffer/silicon substrate interface when using ammonia as the nitrogen source. This success is aided by low-temperature nucleation in an ultra-high-vacuum environment, which eliminates undesired pre-reactions at the surface of the silicon substrate. It is this aspect of growth that enables us to produce AlN buffers on silicon that exhibit unequalled structural quality, uniformity, and smoothness.

Back in 2020, using our unique know-how in AlN nucleation on silicon, we started measuring the resistivity of a simple MBE-grown AlN/GaN stack on silicon. Following process tuning, we were able to realise excellent results, including RF losses as low as 0.3 dB/mm at the buffer/substrate interface.

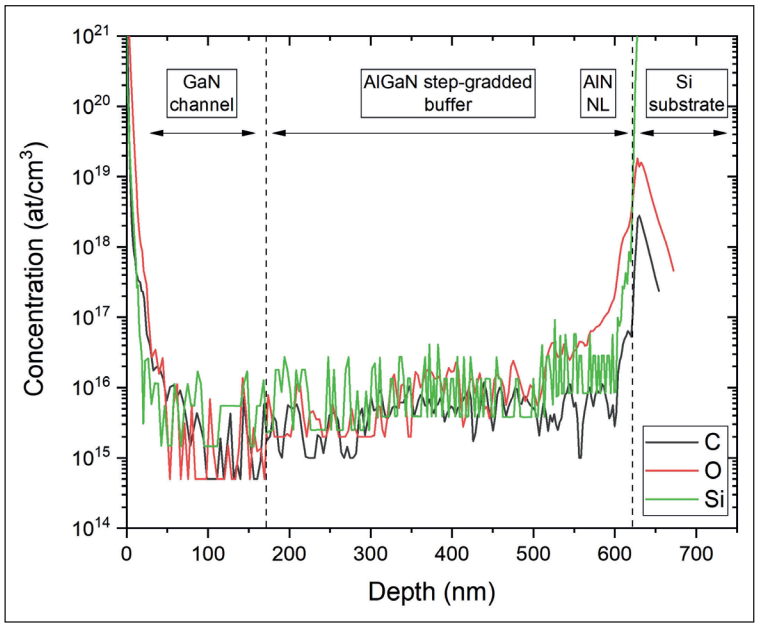


➤ Figure 1. The original epitaxial structure developed by EasyGaN.

Encouraged by this success, we joined the GaNeXT project HUGE, led by Farid Medjdoub from IEMN. This move involved a close collaboration with IEMN and CRHEA, with efforts leading to the fabrication of a complete HEMT structure. Two years in, we obtained remarkable results at the device level. Through this partnership, our team used a Riber MBE49 reactor with 3 x 4-inch configuration, located at CRHEA, to grow an epi stack on high-resistivity silicon (111) substrates. The resulting epitaxial AlN/GaN heterostructure, grown by ammonia-MBE on 4-inch silicon, features: an AlN nucleation layer; a sub-micron-thick graded and undoped AlGaN buffer, used as a back barrier to enhance both confinement of the 2DEG under a high electric field and the breakdown voltage; and a 150 nm undoped GaN channel material, covered by an ultra-thin AlN barrier (see Figure 1).



➤ Figure 2. Scanning electron microscopy cross-sectional image of an EasyGaN HEMT, showing the ultra-thin hetero-structure.



➤ Figure 3. Secondary ion mass spectrometry reveals low carbon and oxygen levels in the GaN channel and the step-graded AlGaN buffer layers.

Remarkable results at 40 GHz

Those of you that have been involved with the semiconductor industry for a while will know that development cycle times are very long. That's at odds with the wishes of a typically stakeholder, and demands a level of patience from them that they are not necessarily used to.

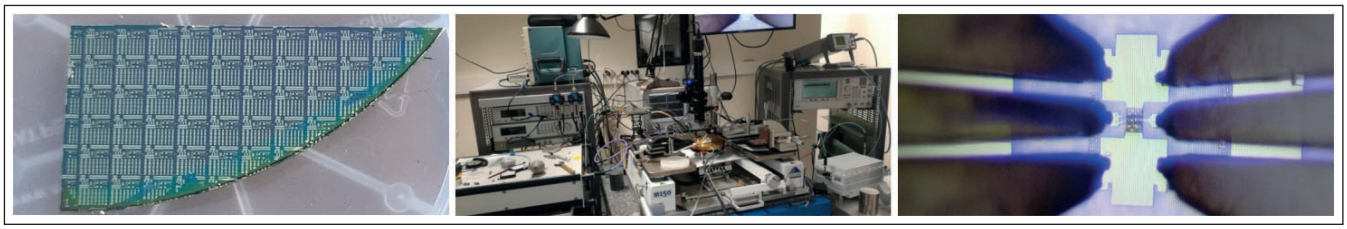
Helping to smooth over the stress at this embryonic time for any fledgling firm is the emergence of some good news from an R&D lab. In our case, this came from unveiling unmatched characteristics for each element of the stack (this is illustrated in Figure 2, which shows a cross-sectional image obtained by a scanning electron microscope).

One of the hallmarks of our epistructure, resulting from nucleation of a high-quality AlN layer at a low deposition temperature, is a high resistivity in the thin buffer that limits RF losses in the substrate. Another asset is the low level of impurities in the AlGaN buffer and GaN channel layers that minimises trapping effects (see Figure 3).

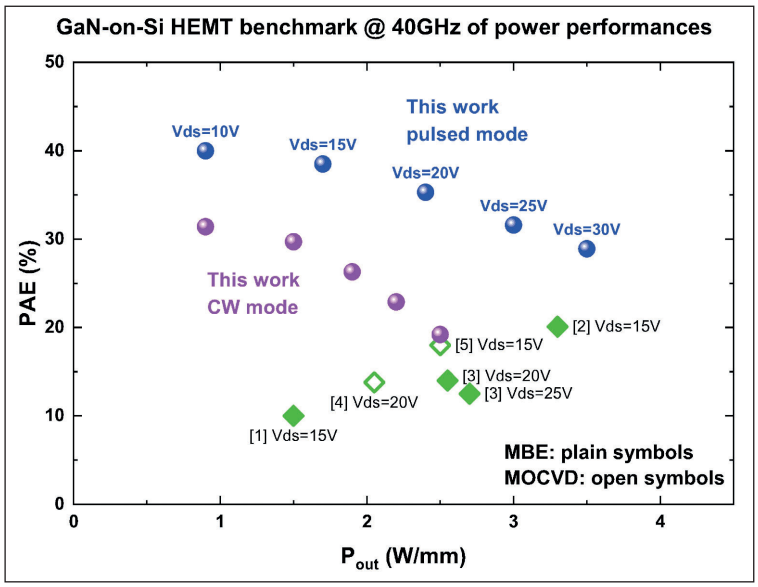
Indeed, a significant advantage of using MBE for the growth of aluminium-rich structures is that it enables relatively low levels of carbon and oxygen impurities. For example, we draw on this asset to grow epitaxial HEMT heterostructures with AlGaN channels that enable devices with a high breakdown voltage, a significant merit for power electronics. MBE is also renowned for its abrupt interface control, which ensures a very sharp interface between the barrier and channel, and in turn allows the use of a very thin AlN barrier. Such a barrier is key to doubling the density of the 2DEG, compared with a conventional AlGaN barrier.

Our team has processed these epiwafers at IEMN, fabricating short transistors that we've characterised in a load-pull configuration using a reference 40 GHz power bench (shown in Figure 4). As this bench has also been used to measure state-of-the-art GaN structures on SiC, rigorous benchmarking is assured. Device processing included formation of source and drain ohmic contacts, isolation of devices, defining of T-gates with sub-150 nm lengths by electron-beam lithography, and deposition of a SiN passivation layer.

Measurements with the power bench confirmed the excellent robustness of this heterostructure at 40 GHz. It is capable of handling extreme electric fields, and consequently enables high voltage operation without degradation after several tens of load-pull sweeps. Our device delivers 3.5 W/mm, associated with a power-added efficiency of 30 percent at a drain-source voltage of 30 V.



➤ Figure 4. A processed GaN-on-silicon epiwafer, 40 GHz power test bench at IEMN, and a device under test.



➤ Figure 5. Values of power-added efficiency versus output power for a range of GaN HEMTs. More details to be found in the *Further Reading* section.

That's a new performance benchmark for this frequency band for the GaN-on-silicon HEMT (see Figure 5).

We are also encouraged by our measurements of the maximum frequency (f_{max}) and the unity gain bandwidth (f_t). They show consistent behaviour relative to the gate length of the transistor (see Figure 6). Finally, we recorded a drain leakage current below 10 µA/mm up to a drain-source voltage of 30 V (see Figure 7).

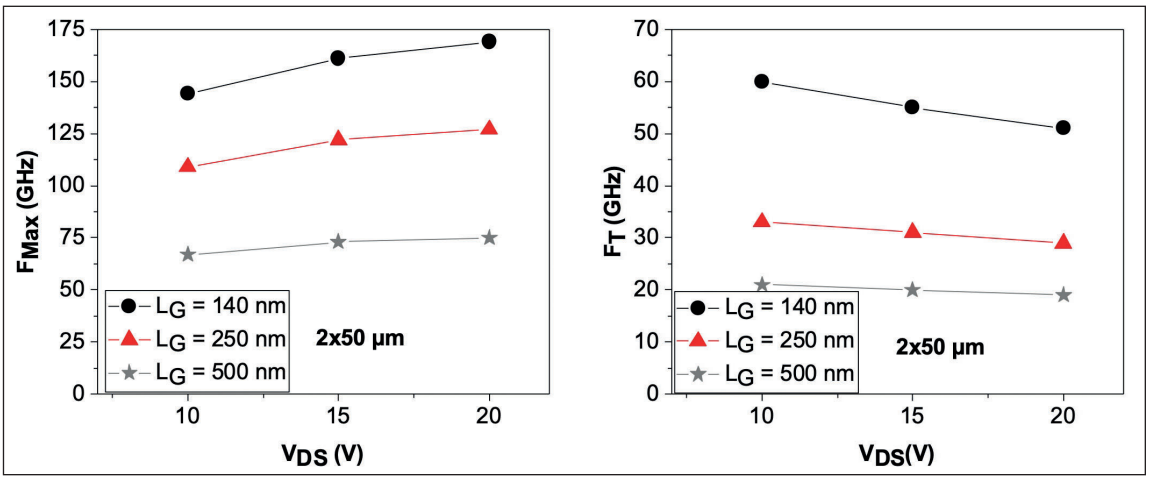
Steps to mass production

To cover the entire range of 5G advanced millimetre-wave bands with some margin, we will now work on extending the operating frequency to 94 GHz. In addition, we plan to support low-voltage operation, so that our HEMTs can serve in handsets. To meet these goals, we will increase electron mobility, enhance thermal dissipation and trim ohmic contact resistance. For the latter, we are also using MBE, an efficient approach for creating low-temperature highly doped regrown ohmic contacts.

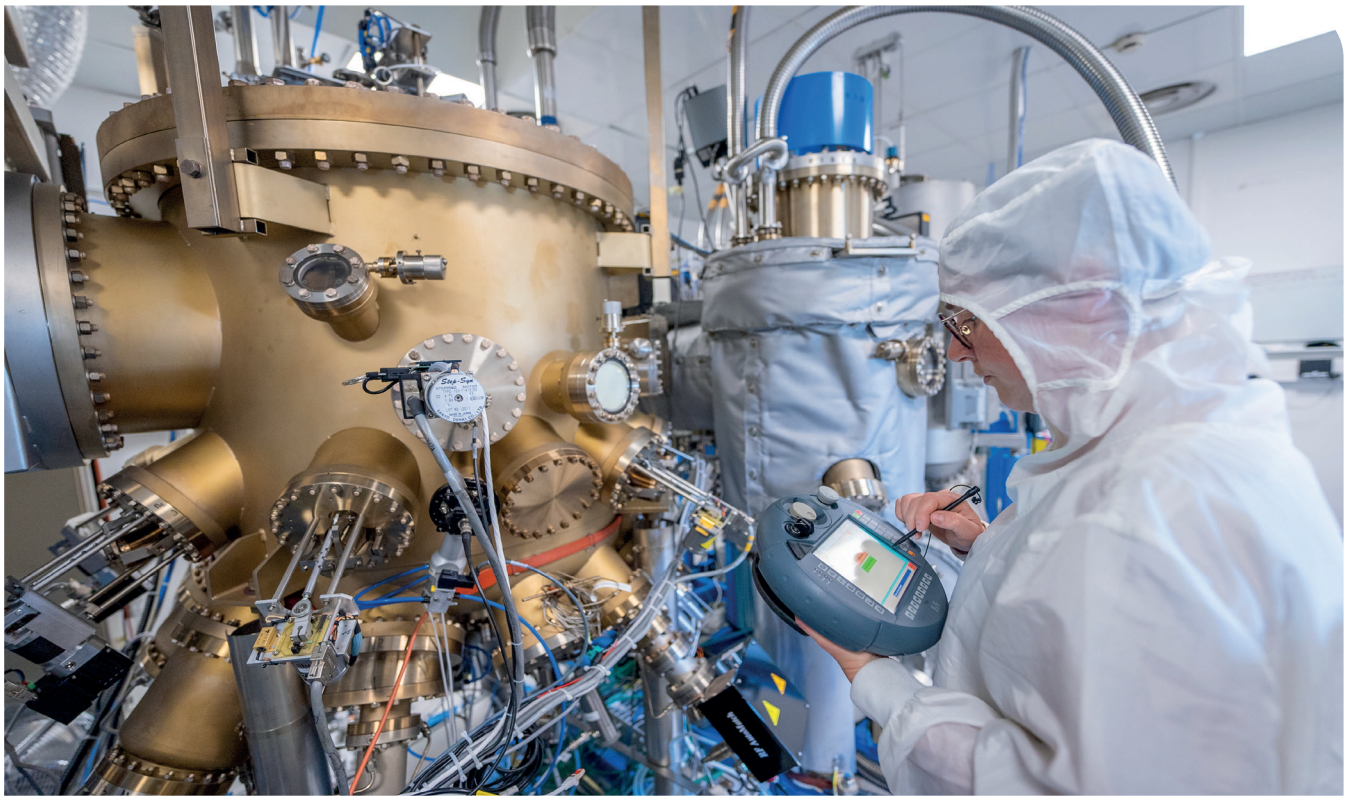
One of our next tasks is to assess the thermal properties of our HEMTs, prior to running our structure through optimisation loops. We are well aware that like any other developer of a GaN-on-silicon device, we are confronted by thermal dissipation characteristics that are poorer than those that come with structures with a SiC foundation. We expect that our sub-micron thick, simple buffer will help to minimise thermal resistance between the active area and the substrate – but we still need to prove this.

What's encouraging is that we have margins in our current design that will allow us to compromise between different parameters and tune characteristics to accommodate a wide range of RF GaN applications. One of the beauties of working with the silicon substrate is access to an arsenal of existing sophisticated techniques that will allow us to enhance thermal dissipation in the substrate.

You may wonder why we insist on making our epitaxial structures so thin. The reason is that, as well as the expected thermal benefits that we have already mentioned, thinner layers take less time to grow and lead to a low wafer bow – it is below



➤ Figure 6. Value for fmax and f_t as a function of the gate length.

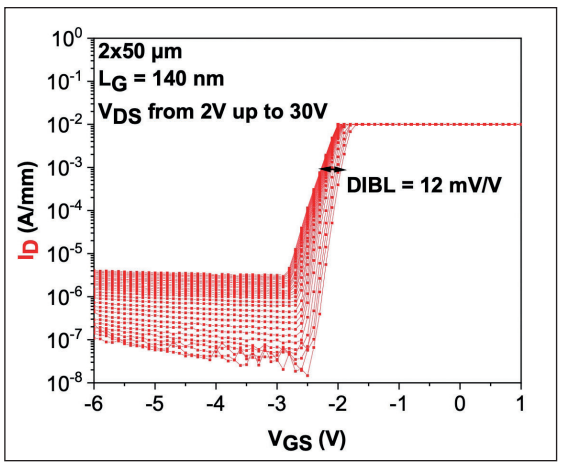


➤ The MBE49 reactor at CRHEA.

20 µm, a great asset when developing larger epiwafers. These strengths translate to a cheaper production cost and a higher yield for device manufacturers, compared with more complex MOCVD-grown structures.

We know that the adoption and deployment of GaN-on-silicon HEMTs produced by MBE will take some time. Establishing the epi design and the recipe is a first necessary step. However, in itself it is not enough. Device manufacturers demand production tools that fulfil cost and throughput requirements found in a high-volume semiconductor market. Whether the MBE systems is the only production tool employed, as is the case with an epiwafer provider, or integrated into a chip fab, key criteria are throughput, cost and yield. Those of us at EasyGaN and CRHEA are well-placed in this regard, as we are already able to manufacture GaN-on-silicon HEMT epistructures on 200 mm wafers in batch mode. For mass production, we can increase scale, moving to Riber's 300 mm silicon-fab-compatible MBE platform to deliver gains on the capacity and cost roadmap.

With our plans in place to scale manufacture of the GaN-on-silicon HEMT, and results showcasing the prowess of this transistor, it is surely destined for a bright future.



➤ Figure 7. A low value for the drain-induced barrier lowering reflects the excellent electron confinement within the 2EG.

FURTHER READING

- E. Carneiro *et al.* "Sub-Micron thick Step-Graded AlGaN Buffer on Silicon with a High Buffer Breakdown Field" Physica status solidi A 202200846 (2023)
- E. Carneiro *et al.* "Combination of low trapping effects and high blocking voltage in sub-micron thick AlN/GaN short transistors grown by MBE on silicon substrate Applied Physics Express, submitted (2023)
- R. Kabouche *et al.* "Power Measurement Setup for On-Wafer Large Signal Characterization Up to Q-Band" IEEE Microw. Wirel. Compon. Lett. **27** 419 (2017)
- K. Harrouche *et al* "Impact of undoped channel thickness and carbon concentration on AlN/GaN-on-SiC HEMT performances" Appl. Phys. Express **15** 116504 (2022)

semi

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium

SMART MANUFACTURING

SMART MOBILITY

SMART MEDTECH

SMART DATA-AI

WORKFORCE DEVELOPMENT

Global ADVOCACY

Sustainability

MIT MARKET INTELLIGENCE TEAM

1000+ STANDARDS

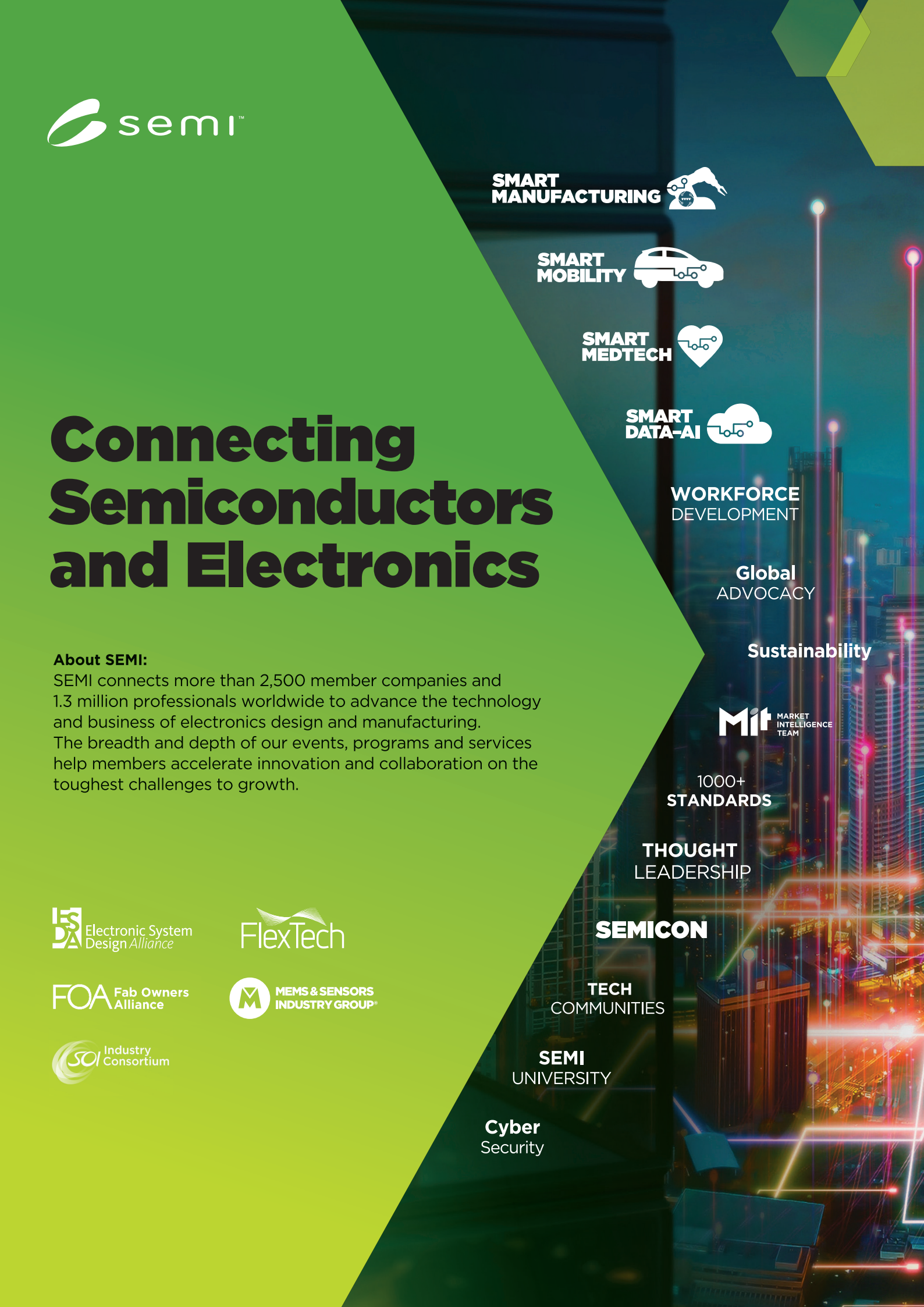
THOUGHT LEADERSHIP

SEMICON

TECH COMMUNITIES

SEMI UNIVERSITY

Cyber Security



Scaling III-V technologies for 5G and 6G

Upscaling GaN HEMTs and InP HBTs to a silicon platform and in co-integrating them with CMOS components fulfils the requirements for next-generation high-capacity wireless communication

BY NADINE COLLAERT FROM IMEC

As every year goes by, yet more data is transmitted wirelessly, driven by an ever-growing group of users. To enable this trend to continue, while making data transfer faster and more efficient, owners of mobile networks are now rolling out the fifth generation of wireless technology infrastructure – and they are already starting to consider what lies after.

Today's 5G networks are capable of peak data rates of 10 Gbit/s. When 6G follows – its deployment is slated to commence in 2030 – rates as high as 100 Gbit/s are expected. To ensure that this will be a success, researchers have much to consider. As well as figuring out how to accommodate more data and connections, efforts must be directed at investigating how the next generation of wireless communication will support new use cases, such as autonomous driving and holographic presence.

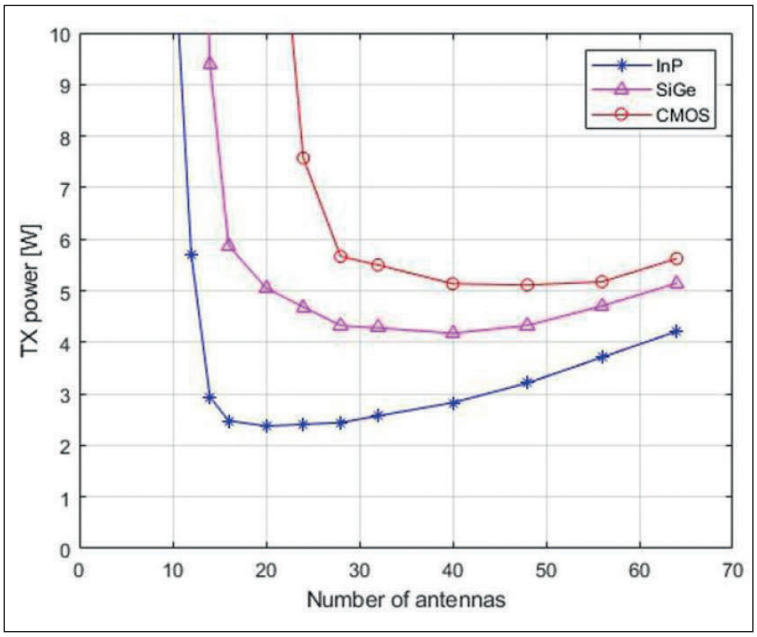
To enable exceptional data rates, the telecom industry has already been shifting wireless signals to higher frequencies. While 5G initially employed sub-6 GHz frequency bands, products targeting 28/39 GHz have been showcased. There is also growing interest in FR3 frequency bands within the 6-20 GHz domain for 5G networks, as they offer a great balance between coverage and capacity. For 6G, frequencies above 100 GHz are now being discussed.

There is much to be gained with a move to higher frequencies. One of the most significant benefits is the introduction of new frequency bands, thereby addressing the spectrum scarcity issue within

existing bands. Another advantage is that the higher the operating frequency, the easier it is to obtain a wider bandwidth. In addition to these merits, a combination of frequencies above 100 GHz and bandwidths up to 30 GHz allow telecom operators to, in principle, use lower-order modulation schemes within wireless data links. In turn, this trims power consumption.

Higher frequencies also deliver benefits coming from shorter wavelengths. As the antenna array size scales with the square of the wavelength, higher frequencies allow antenna arrays to be packed far more densely. This contributes to better beamforming, a technique that ensures that a greater proportion of transmitted energy arrives at the intended receiver.

Moving to higher frequencies is not without challenges. Today, CMOS is the preferred technology for building the critical components of transmitters and receivers, including the power amplifiers within the front-end modules that send radio-frequency signals to and from the antennas. As the operating frequency increases, CMOS-based power amplifiers struggle to deliver the required output power with a sufficiently high efficiency.



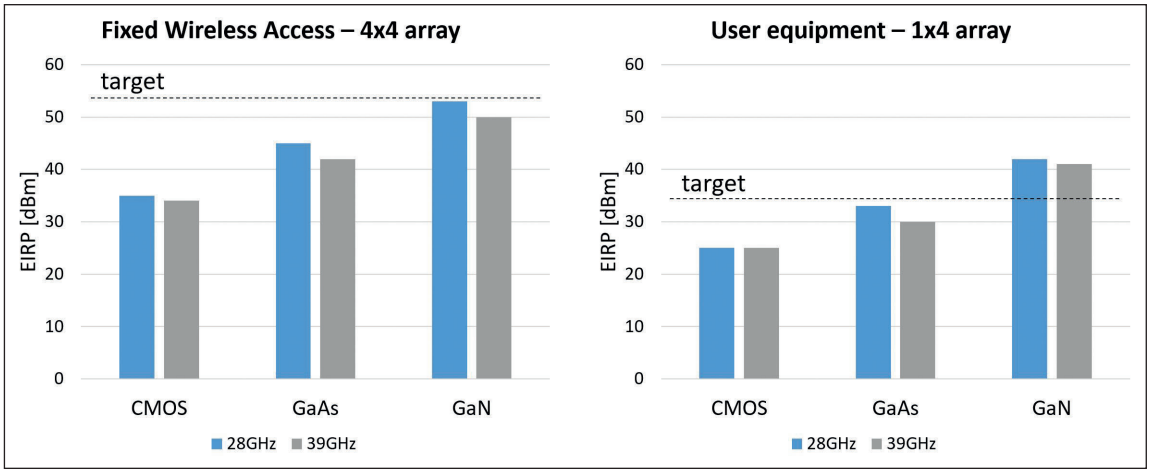
➤ Figure 1. Comparing the power consumption of CMOS, SiGe, and InP devices in transmitter architectures as a function of the number of antennas (as presented at IEDM 2022).

This is where technologies such as GaN and InP come into play. Thanks to their outstanding material properties, these III-Vs stand a far better chance of providing the required output power and efficiency at high operating frequencies. For example, GaN combines a high current density with a high electron mobility and a large breakdown voltage. The high power density also enables a small form factor, and thus a trimming of the overall system size while maintaining performance.

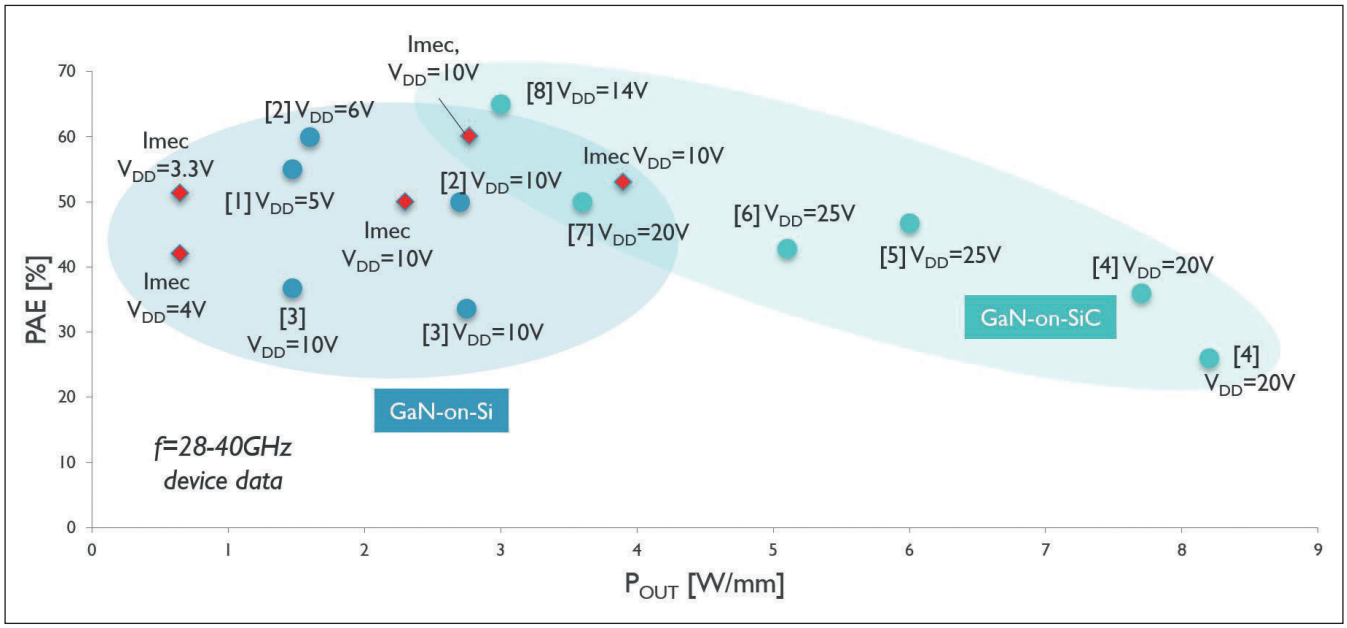
Outclassing CMOS

At imec, the internationally renowned microelectronics centre, we have been considering the opportunities for III-V technologies in tomorrow's wireless infrastructure, and the device architectures best suited for this advance. Our efforts have included a modelling exercise, where we have compared the performance of three different power amplifier implementations operating at 140 GHz: entirely CMOS; a CMOS beamformer, in combination with a SiGe HBT; and an InP HBT. The latter emerged as the clear winner, in terms of both the output power (over 20 dBm) and energy efficiency (20 to 30 percent). It's worth noting that our modelling also revealed that for InP, the optimal point for energy efficiency is obtained with relatively few antennas. This is a significant asset when real estate is at a premium, which is the case in mobile devices.

Additional modelling by our team shows that at lower millimetre-wave frequencies it is GaN that exhibits excellent performance. At both 28 GHz and 39 GHz, GaN-on-SiC HEMTs outclass CMOS-based devices and GaAs HEMTs, in terms of output power and energy efficiency. The superiority of GaN is seen in two different use cases: fixed wireless



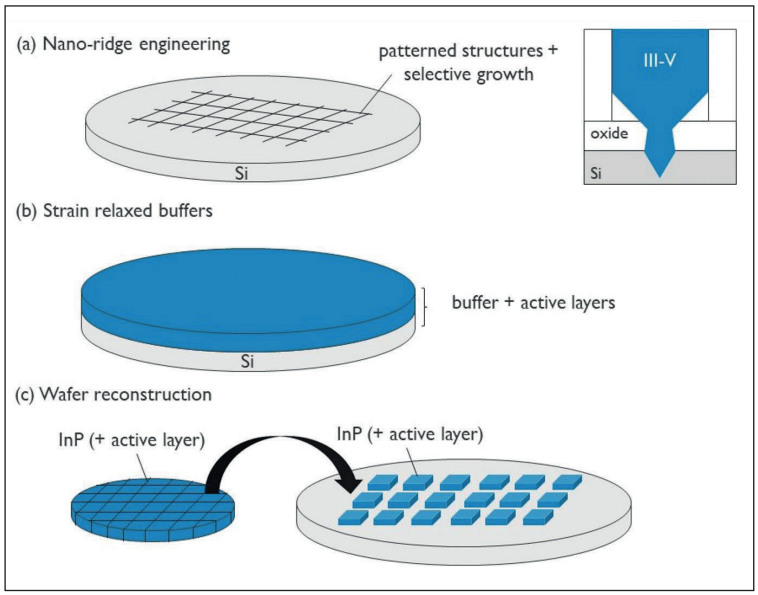
➤ Figure 2. Output power for 28 GHz and 39 GHz operating frequencies in (left) fixed wireless access (FWA) and (right) user equipment: a comparison of three different technologies (as presented at IEDM 2022).



➤ Figure 3. GaN-on-silicon benchmarking data. The imec data in red is among the best reported for GaN-on-silicon devices and comparable to GaN-on-SiC substrates (as presented at IEDM 2022). References: [1] H.W. Then *et al*. IEDM 2020; [2] H.W. Then *et al*. IEDM 2021; [3] W. Wang *et al*. J-EDS 2018; [4] Y.C. Lin *et al*. Micromachines 2020; [5] M. Mi *et al*. TED 2017; [6] Y. Zhang *et al*. EDL 2018; [7] K. Harrouche *et al*. HAL open science, 2020; [8] J.-S. Moon *et al*. MTTS 2019.

access, with 16 antennas; and user equipment, with four antennas.

The Achilles heel for III-V devices is the cost and complexity of integration – GaN and InP device technologies are not yet able to fully compete with CMOS-based technologies. III-V devices tend to be produced on small and costly non-silicon substrates, and rely on less suitable processes for high-volume manufacturing.



➤ Figure 4. Schematic representation of the different InP-on-silicon growth approaches: (a) nano-ridge engineering; (b) blanket growth with strain relaxed buffers, and (c) wafer reconstruction.

An exciting way forward is to integrate III-V devices on 200 mm or 300 mm silicon wafers. This approach promises overall optimisation while maintaining superior RF performance. As well as being much cheaper, silicon substrates open the door to CMOS-compatible processing that enables large-scale manufacturability.

Integrating GaN and InP on a silicon platform is far from trivial. It demands new approaches for transistor and circuit design, new materials, and different manufacturing techniques. One of the main challenges relates to the large lattice mismatches of the III-Vs with silicon: 8 percent for InP and 17 percent for GaN. These significant differences threaten to create many defects in the layers and ultimately degrade device performance.

Another challenge is to co-integrate the components that are based on either GaN-on-silicon or InP-on-silicon with CMOS-based components and create a complete system. Initially, GaN and InP technologies will be used to realise the power amplifiers within the front-end modules. However, there is also the possibility to improve the performance of low-noise amplifiers and switches by drawing on the unique properties of these compound semiconductors. But in the end, CMOS will still be needed for calibration, control, and beamforming.

Through our Advanced RF Program that includes contributions from industry partners, we have been exploring various ways to integrate GaN and InP devices on large-size silicon wafers, and how to enable their heterogeneous integration with CMOS

components. This work has included an assessment of the pros and cons for different use cases – infrastructure, such as fixed wireless access, as well as user equipment.

Improving RF GaN-on-silicon

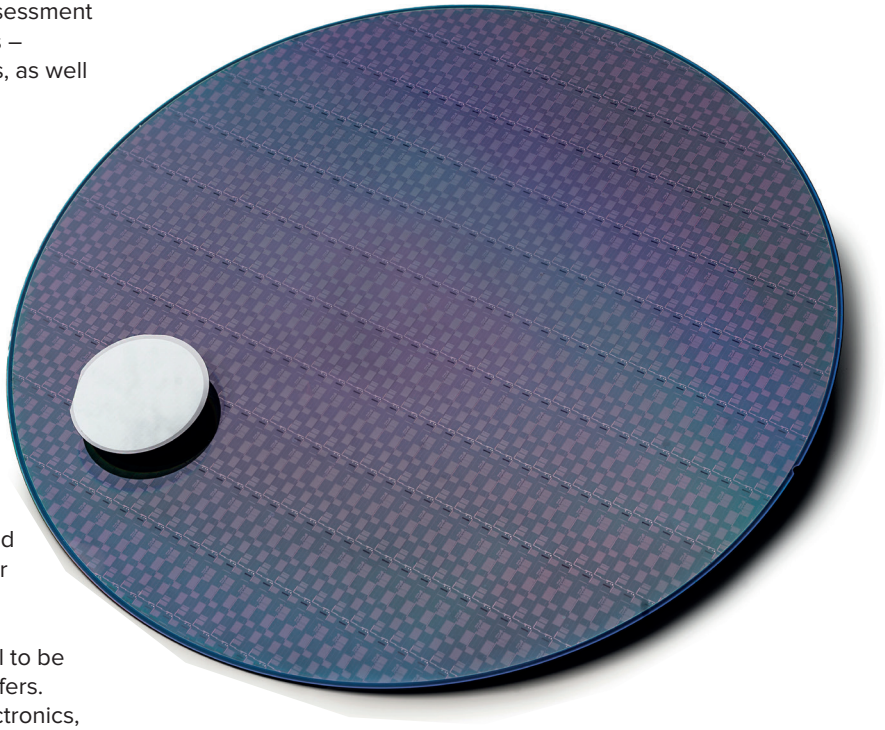
Variations in the starting substrate give rise to several flavours of GaN technology: GaN on native bulk substrates, GaN-on-SiC, and GaN-on-silicon. Of the three, today GaN-on-SiC is the most widely explored and already used for infrastructure applications, including 5G base stations. SiC substrates are more cost-efficient than bulk GaN technology, and SiC is an excellent thermal conductor – this aids heat dissipation in high-power infrastructure applications. However, SiC substrates are higher in cost than silicon and limited in size, making them less suitable for mass production.

In contrast, GaN-on-silicon has the potential to be upscaled to 200 mm and even 300 mm wafers. Thanks to years of innovation in power electronics, tremendous progress has already been made in the integration of GaN on large-size silicon substrates. However, additional improvement is needed to ensure that GaN-on-silicon technology is suitable for optimal RF performance. The main challenges are to deliver a comparable large signal and reliability performance to that of GaN-on-SiC, and to realise a higher operating frequency. Meeting these objectives requires: further innovation in material stack design and choice of materials; a reduction in the gate length of the HEMT; suppression of parasitics; and keeping RF dispersion as low as possible.

The GaN-on-silicon process flow for making RF devices at imec begins by loading 200 mm silicon substrates into an MOCVD reactor. Epitaxial growth follows, creating a structure comprising a proprietary GaN/AlGaN buffer, a GaN channel, an AlN spacer, and an AlGaN barrier. From this epiwafer we process GaN HEMTs with TiN Schottky metal gates that are subsequently integrated with a (low-temperature) 3-level copper back-end-of-line process.

We have recently realised competitive results with our GaN-on-silicon platform. Our success has brought the output power and power-added efficiency of GaN-on-silicon closer to that of GaN-on-SiC technology. Note that the power-added efficiency is a commonly used metric for evaluating the efficiency of a power amplifier, because it considers the effect of the amplifier's gain on its overall efficiency.

Our combination of technology development and modelling will ultimately help to achieve even better performance and reliability for the GaN-on-silicon HEMT. At the most recent IEDM, held last December, we unveiled a simulation framework for improving predictions of thermal transport in RF devices. These simulations revealed that the rise in peak temperature is three times higher than predicted previously. The insight provided by this modelling offers further guidance for optimising RF devices and their layouts early in the development phase.



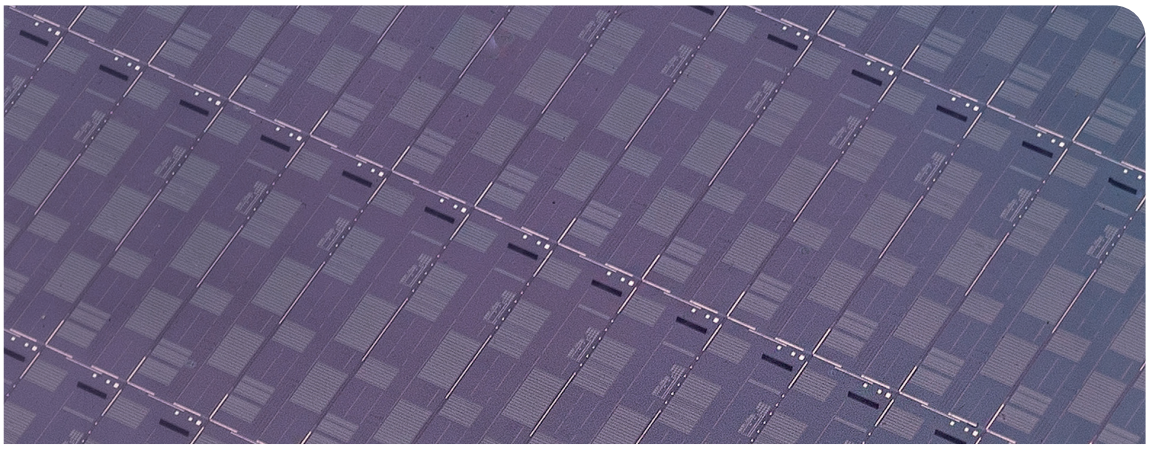
➤ Figure 5. A 2-inch InP wafer, and a 300 mm silicon wafer with a InP nano-ride engineered HBT stack.

InP-on-silicon for 6G

For higher frequencies, InP HBTs are superior to GaN HEMTs, offering a better trade-off of output power and efficiency. This technology is also well understood, with researchers knowing how to design InP HBTs for optimal RF performance. However, fabrication tends to involve InP substrates with diameters below 150 mm, and lab-like processes that are not CMOS-compatible.

Within the research community there are three approaches under consideration for upscaling. Two rely on direct growth of InP on silicon and a third is based on wafer reconstruction. All three have the potential to provide a more cost-effective approach to production than current technologies, which use small InP substrates. There are pros and cons for all three approaches, in terms of performance, cost, and heterogeneous integration potential. We have assessed the benefits and challenges of all of them for various use cases – infrastructure as well as mobile devices.

One approach that many groups pursue for making InP HBTs on silicon is to bridge the 8 percent lattice mismatch with strain-relaxed buffer layers (see Figure 4(b)). InP is grown directly on top of this buffer. The opportunity to use larger wafer sizes, particularly in cases where some of the silicon could be reused, offers a significant cost



➤ Figure 6. Zoom-in of the 300 mm silicon wafer showing the dies with the InP nano-ride engineered HBT structures.

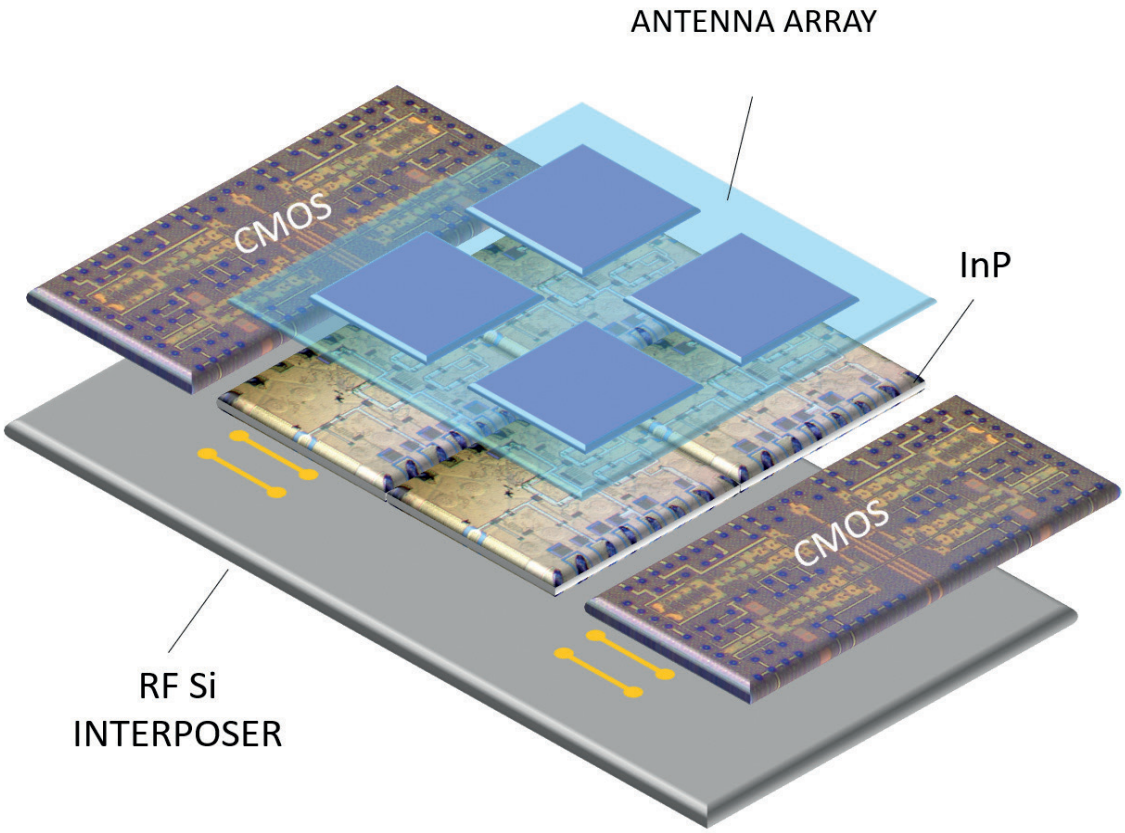
advantage. However, this approach is challenging, with optimisation needed to drive down the defect density.

We depart from this 'blanket' growth approach, proposing nano-ridge engineering, an alternative technology that deals with defects more efficiently (see Figure 4 (a)). Nano-ridge engineering involves selective growth of III-V material in pre-patterned trenches, formed in a silicon substrate. These high-aspect-ratio trenches are incredibly effective at trapping defects –imperfections are only present in the narrow bottom part of the trench – thereby enabling the growth of high-quality, low-defectivity material out of the trench. Through overgrowth the nano-ridge widens towards the top, creating a solid base for a device stack. Our insights from a GaAs/InGaP case study are guiding our optimisation of the target InGaAs/InP nano-ridge engineered HBT devices.

An alternative to direct growth is to place InP on silicon with a wafer reconstruction technology (see Figure 4 (c)). In this case, high-quality InP substrates – with or without active layers – are diced into tiles during wafer constitution. The tiles are then attached to a silicon wafer with die-to-wafer bonding. With this approach, the key challenges are associated with the efficient transfer of materials and the removal of the remaining InP substrate. Several techniques are being considered.

Towards heterogeneous integration

Ultimately, the III-V-on-silicon power amplifiers have to be combined with CMOS-based components that take care of the likes of calibration and control. We



➤ Figure 7. Schematic representation of an RF silicon interposer with integrated InP and CMOS devices and antenna array in a package.

are evaluating various heterogeneous integration options, weighing their pros and cons for a number of use cases. The most common way to integrate different RF components in a system-in-package is to use an advanced laminate substrate technology. We are optimising this to make it more suitable for higher frequencies. On top of this, we are exploring more advanced options for heterogeneous integration, including 2.5D interposer and 3D integration technologies.

Note that for frequencies beyond 100 GHz, the antenna module starts to define the area that's available for the transceiver. At such high frequencies, the antenna is smaller than the front-end module, which hardly scales in size with increasing frequency. When this is the case, one interesting option for configurations with a large antenna array is to shift the location of the RF front-end module to under the array. This is where 3D integration technologies – either die-to-wafer or wafer-to-wafer – come into play. They enable short, well-defined connections between the front-end module and the antenna modules. As great a concern for 3D integration is thermal management, which will be crucial to provide effective heatsinks. We are currently undertaking a comprehensive system-technology-co-optimisation analysis to evaluate a range of technologies for 3D integration and to guide technology choices from a system-level perspective.

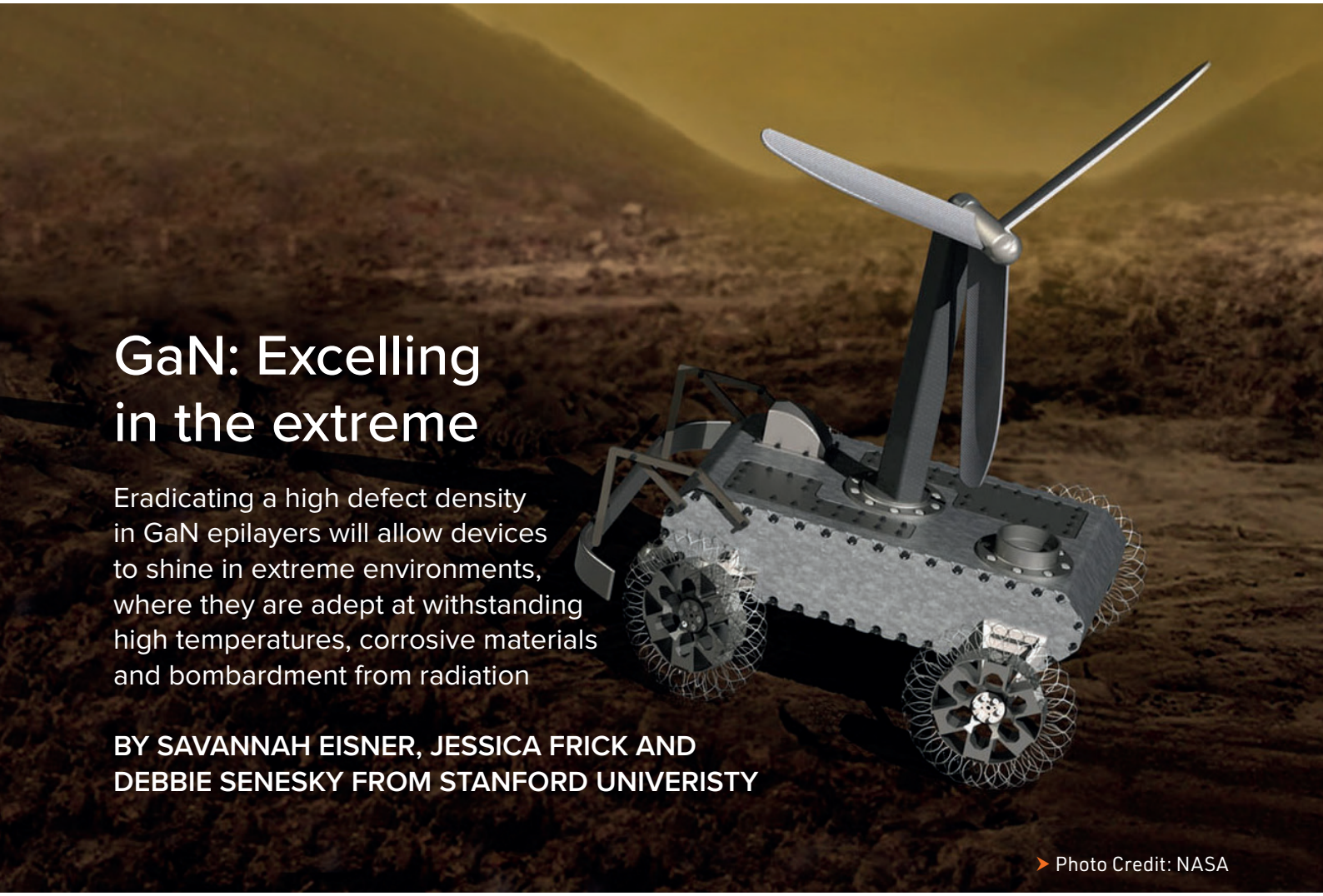
For handheld devices, where a reduced number of antennas relax constraints, an interesting approach is 2.5D interposer technology. This option for heterogeneous integration, using a layer stack with lithography-defined connections, can accommodate through-silicon vias that enable communication between the III-V and the CMOS-based components. In this situation, the III-V devices sit next to the CMOS chip, ensuring superior thermal management, because both chips can be in direct contact with a heat sink. The downside of this architecture is that it only allows for 1D beam steering.

Today we are evaluating hardware implementations of 2.5D interposer technology, looking into the most optimal combinations of substrates, dielectrics, and redistribution layers to minimise losses. Our successes on this front include a first version of an RF-tailored silicon interposer technology, using a standard silicon substrate, a copper semi-additive interconnect, and thick spin-on low-κ dielectrics that exhibit very low interconnect loss, even above 100 GHz.

Our recent upscaling and integration efforts are producing very promising results. We have shown that GaN-on-silicon and InP-on-silicon are set to become viable technologies for next-generation high-capacity wireless communication applications.

FURTHER READING

- 'Thermal modeling of GaN & InP RF devices with intrinsic account for nanoscale transport effects,' B. Vermeersch et al., 2022 International Electron Devices Meeting (IEDM)
- 'III-V/III-N technologies for next-generation high-capacity wireless communication,' N. Collaert et el., 2022 International Electron Devices Meeting,



GaN: Excelling in the extreme

Eradicating a high defect density in GaN epilayers will allow devices to shine in extreme environments, where they are adept at withstanding high temperatures, corrosive materials and bombardment from radiation

BY SAVANNAH EISNER, JESSICA FRICK AND DEBBIE SENESKY FROM STANFORD UNIVERISTY

Photo Credit: NASA

THANKS TO its remarkable properties, GaN is now a mainstay material for power and RF electronics. Its cherished strengths are its high breakdown voltage, and its high values for the mobility and the carrier saturation velocity of its two-dimensional electron gas (2DEG) channel. But what makes this material even more remarkable is that it combines these attributes with a tolerance to high temperatures and a tremendous resistance to radiation attack – it is these attributes that make GaN a very attractive material for expanding the Internet of Things (IoT) into extreme environments.

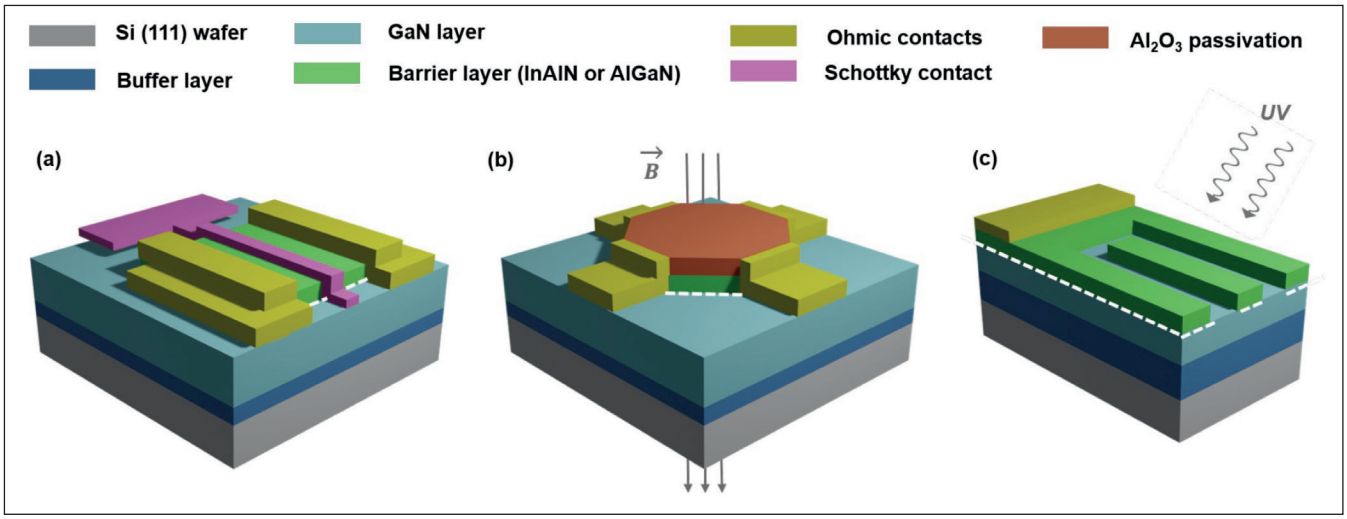
This particular promise has not gone unnoticed, with researchers already starting to explore GaN as a platform for long-range IoT communication technology in space exploration applications, as well as medium-range IoT communication technologies in terrestrial applications requiring computation, timing, and sensing within hostile conditions. There are emerging opportunities for GaN associated with geothermal, oil and gas, and hypersonics.

GaN can be harnessed for all of these opportunities because silicon, the dominant semiconductor of choice for many decades, exhibits poor performance in extreme environments. Since its invention in 1954, the scope of the silicon transistor has been fundamentally limited to benign environments.

Due to a bandgap of around just 1.2 eV, devices made from silicon are incapable of operating at temperatures above around 200 °C. This severe limitation causes silicon devices and circuits to require active cooling to operate in harsh environments.

Note, though, that moving beyond silicon offers far more than just simplifying thermal management. As electronic applications become more power dense, platforms based on a successor to silicon can cater to this need, while also functioning reliably and not requiring complex, expensive packaging. Enabling these capabilities has tremendous value, given the strict payload and cost requirements of modern-day engineering systems.

Superior alternatives to silicon are not limited to GaN, but encompass a number of other wide bandgap materials, such as SiC and diamond. All offer higher power densities, as well as lower power consumption.



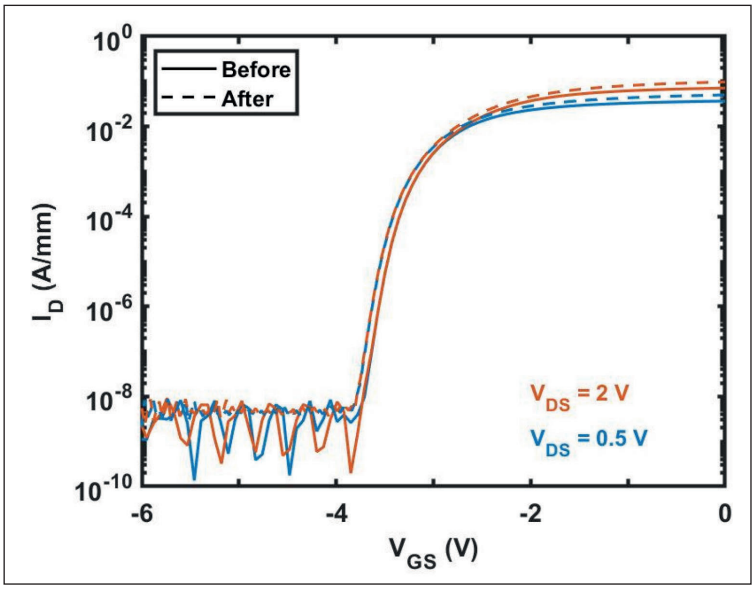
➤ Cross-sectional schematic of the (a) InAlN/GaN HEMTs, (b) InAlN/GaN Hall-effect sensors, and (c) AlGaN/GaN UV photodetectors exposed to the Venus-simulant environment. Interfaces where the 2DEG is present are represented by white dashed lines. Reproduced from S. R. Eisner *et al.*, "Extended Exposure of Gallium Nitride Heterostructure Devices to a Simulated Venus Environment," 2021 IEEE Aerospace Conference (50100), Big Sky, MT, USA, 2021, pp. 1-12.

In the case of GaN, the material attributes that enable power-efficient, high-frequency operation are also behind the compelling initial demonstrations of device operation in hot ambients. The heterostructured InAlN/GaN platform has already reached an eye-watering operating temperature of 1000 °C, a remarkable feat that's enabled by complementary high-temperature metal contacts and reduced strain relaxation effects.

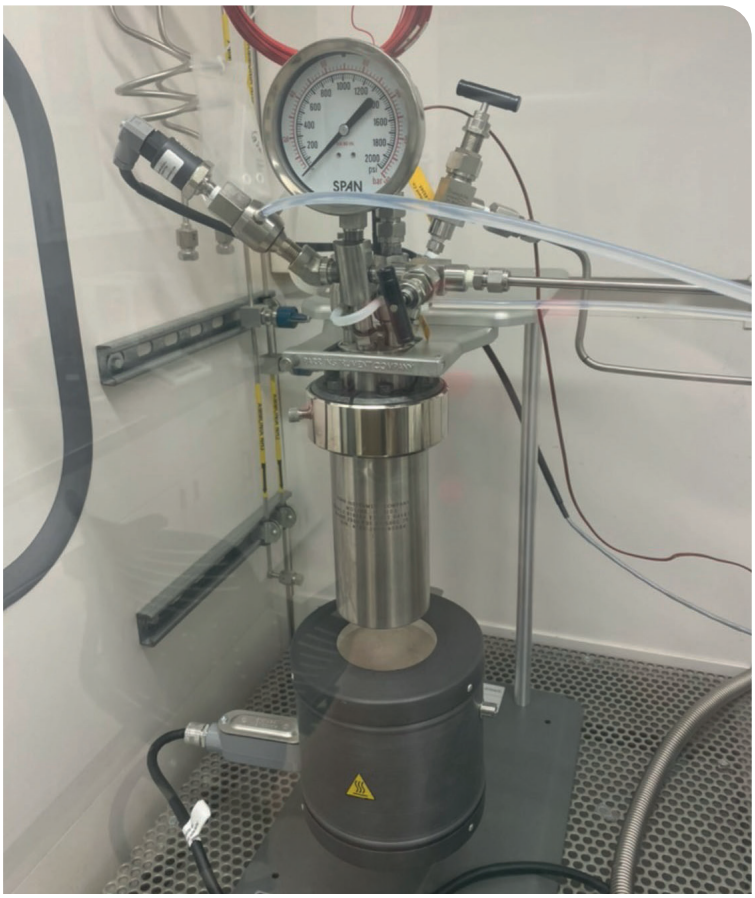
Such a performance is impossible to realise in silicon, because its intrinsic carrier concentration is too high to ensure current modulation at high temperatures. Under this condition, the carriers in silicon that are thermally activated into the conduction band would overwhelm the channel. GaN does not suffer the same fate, thanks to a bandgap that is three times wider, and a lower intrinsic carrier concentration.

A much desired, unique feature of the GaN material system is the polarisation-induced formation of the 2DEG channel at the heterointerface. Thanks to these polarisation effects, it is possible to form a conducting channel without doping. The major implication is that the channel in GaN devices is free from deleterious dopant scattering and diffusion, known to negatively impact device performance at high and low temperatures. The two-dimensional channel in GaN heterostructures can support very high electron mobilities, on the order of 2200 $cm^2 V^{-1} s^{-1}$, at room temperature.

The merits of GaN heterostructures with a 2DEG have inspired a multitude of demonstrations of solid-state and MEMS sensors at the micro- and nano-scale. Opportunities for GaN resonators that utilise a 2DEG for piezoelectric transduction include (1) deployment in harsh-environments, for infrared and chemical sensing, and (2) in oscillators, to provide stable, chip-scale clocks for a GaN-based IoT platform. Other exciting developments include: micro-pressure sensors fabricated in GaN heterostructured membranes, shown to work at up to 300 °C in air; mechanical sensors for harsh environments, such as seismometers, accelerometers, gyroscopes; and strain sensors, which can similarly benefit from strain transduction in GaN. There's also opportunity for high-gain UV photodetectors, exploiting the valence band offset in GaN heterostructure epitaxial layers, with devices formed using 2DEG interdigitated electrodes. And this list goes on - magnetic field sensing capabilities



➤ InAlN/GaN HEMT transfer characteristics before and after 10-day exposure in a Venus simulation chamber. Reproduced from S. R. Eisner *et al.* "Extended Exposure of Gallium Nitride Heterostructure Devices to a Simulated Venus Environment," 2021 IEEE Aerospace Conference (50100), Big Sky, MT, USA, 2021, pp. 1-12.



➤ Custom Venus simulation chamber for subjecting devices to realistic harsh environmental conditions in the Extreme Environment Microsystems Lab (XLab) at Stanford University.

with high sensitivities have been achieved in both AlGaN/GaN and InAlN/GaN; and heterostructured GaN has demonstrated energy harvesting capabilities in extreme environments, through thermoelectrics and betavoltaics. It's also possible to amplify signals from these sensors without having to introduce another material system, because signal amplification and logic can be performed by the well-known GaN HEMT.

Thanks to the lateral layout of the GaN heterostructure, as well as compatible microfabrication processes, the plethora of sensors that can be produced are amenable to monolithic integration. Due to this, it is possible to produce single, uncooled heterostructured GaN chips that combine sensing, communication, and power functionality; can operate for long durations in extreme environments while connecting with an IoT network; and have no need for cooling or shielding. In addition to these assets, such monolithically-integrated electronics yield lighter, cheaper IoT systems.

Venturing to Venus

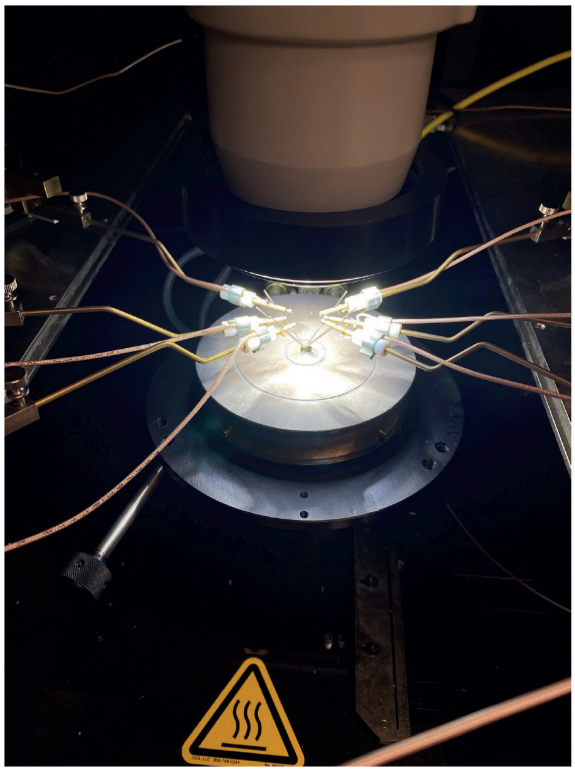
One exciting new frontier in space exploration that can be unlocked by leveraging GaN IoT technology is a long-lived mission to the hostile surface of Venus. This heavenly body is often called Earth's 'sister planet', due to its similar size, composition, and relative position in the solar system.

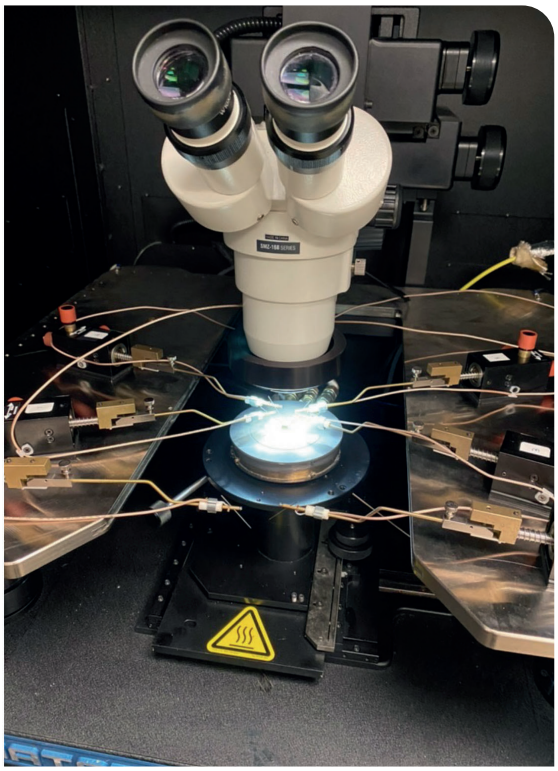
The majority of Venus surface exploration programmes date back to the 1970s and 1980s, led by the Soviet Union. Of those, the longest-lived Venus surface mission, Venera 13, lasted just over 2 hours. To put that timespan into perspective, the record lifetime of a Mars surface mission stands at 14 years and 138 days, set by NASA's Opportunity rover between 2004 and 2018.

The staggering discrepancy in the mission lengths on the surfaces of Venus and Mars is a poignant reflection of the massive technical hurdle to exploration presented by the inhospitable Venus environment. While there may be planetary similarities between Venus and Earth, the climates are utterly different. The surface of Venus is a blistering 464 °C, and atmospheric pressure is over 90 bars – that's equivalent to the pressure found at a depth of 1 km in our oceans. The content of the atmospheres is also dissimilar, with that for Venus consisting mainly of corrosive CO_2, rendered into a supercritical state by high temperature and pressure. Other constituents of Venus' atmosphere include nasty, corrosive and caustic chemical compounds, such as SO_2 and hydrofluoric and hydrochloric acids.

This toxic composition, allied to extreme physical conditions, creates a hostile surface that exceeds the operational limits of traditional silicon microelectronics, making robotic exploration missions exceptionally technologically challenging. Silicon falls well short of what's needed on many fronts, as it's chemically incompatible with Venus' atmosphere, and incapable of operating at this planet's surface temperatures, even with the introduction of strategic technologies, such as silicon-on-insulator. Applying active cooling and shielding measures makes little difference, as evidenced by the transmission failure of the silicon microelectronics on board Venera 13 after reaching ambient temperature.

Venus consists mainly of corrosive CO_2 rendered into a supercritical state by high temperature and pressure. Other constituents include nasty, corrosive and caustic chemical compounds, such as SO_2 and hydrofluoric and hydrochloric acids.





➤ GaN heterostructure devices being tested at 600 °C in air in the Extreme Environment Microsystems Lab (XLab) at Stanford University.

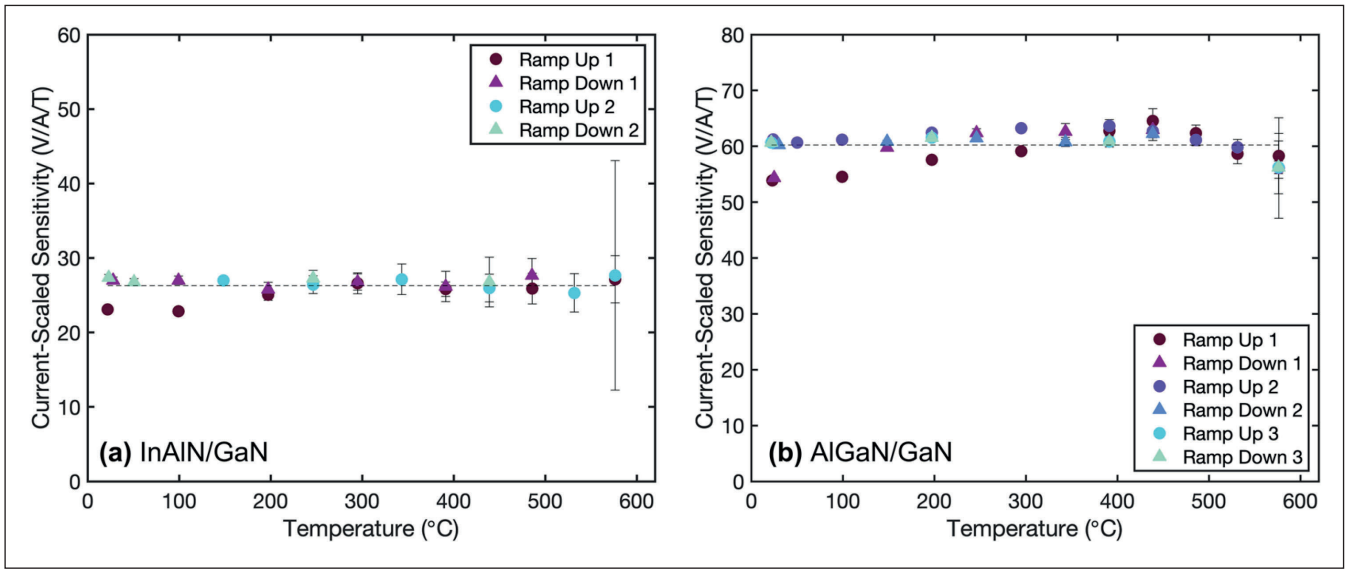
In the decades since the last dedicated Venus surface mission – the Soviet's 1985 Vega 1 mission – scientific study of this planet has focused on orbiting spacecraft and satellites, primarily on fly-by missions to other destinations. While such an approach garners useful information, insight is hampered by a very thick cloud layer that surrounds the planet and prevents scientists from answering many of the outstanding questions about Venus.

Revived by NASA

Priorities for what should be discovered on a future mission have been identified by NASA's Venus Exploration Analysis Group (VEXAG). This group has highlighted the need for studies of mineralogy, seismology, metrology, and chemical interactions between the surface and the atmosphere. To obtain sufficient information, the length of the mission needs to far exceed that of Venera 13 – the time scale should be weeks or months – to enable observations that cover various times of the day and differing weather conditions. An extended duration mission would deliver an additional benefit, as it would allow for remote, human-in-the-loop decision-making capabilities. This is the case with Mars surface rovers, with a team on Earth determining where to drill and conduct sample analysis.

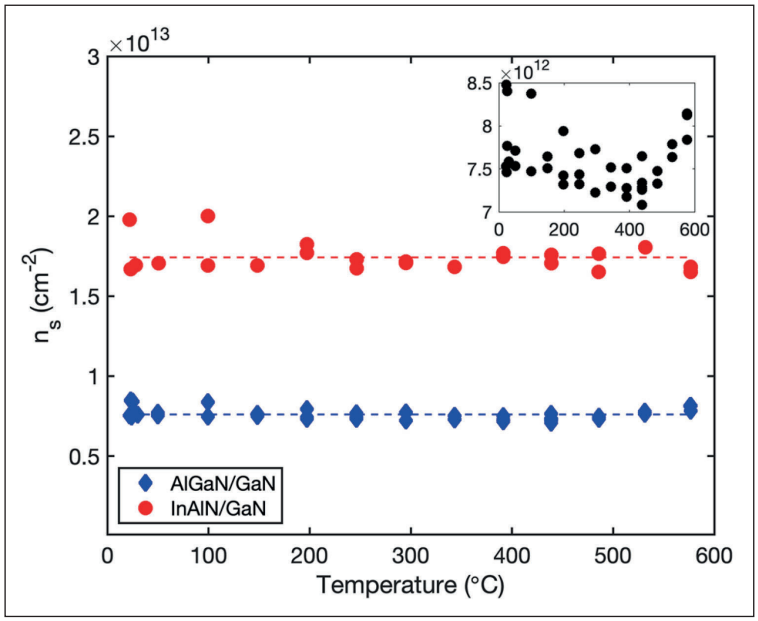
The scientific knowledge gained from such a mission is not limited to expanding our knowledge of Venus. This endeavour would also shed new light on the factors that influence diversity in planetary bodies, including greater insight into the drivers behind the divergence in the evolution of Earth and Venus, and why these two support different climates and geological features. Despite its extreme environment today, there may have been a time when Venus hosted ancient oceans, and perhaps even life on its surface. The extent and timespan of these oceans is still debated. By increasing our understanding of Venus, which suffers from a runaway greenhouse gas effect, we may resolve this debate while gaining a better understanding of similar processes, and the impact they might have here on Earth. Achieving these objectives could help shape our criteria when searching for other potentially habitable exo-planets.

➤ Savannah Eisner beside the Stanford Nanofabrication Facility's Aixtron MOCVD III-N System growing epitaxial GaN heterostructure thin films.



➤ Current-scaled sensitivity of (a) InAlN/GaN and (b) AlGaN/GaN Hall-effect magnetic field sensors between room temperature and 576 °C in air. Reproduced from H.S. Alpert *et al*. Rev Sci Instrum. **91** 025003 (2020)

For a Venus surface mission, the desired instrumentation requires multiple semiconductor devices. They are needed for: sensors and imagers; mass and laser spectrometer control and read-out electronics; low-power sample handling processors needed to command a drill; and for power system electronics, to control switching and power distribution. Thanks to the potential for monolithic integration in GaN heterostructures, a future mission to Venus may include large-scale surface exploration, carried out by multiple robotic rovers, which generate large amounts of sensor data and communicate, via the IoT, with each other and orbiting satellites.



➤ 2DEG sheet density of InAlN/GaN and AlGaN/GaN samples from room temperature to 576 °C. The inset shows the AlGaN/GaN 2DEG sheet density over temperature on tighter axes. Reproduced from H.S. Alpert *et al*. Rev Sci Instrum. **91** 025003 (2020)

The prospects of such missions are on the rise, with Venus surface exploration recently garnering increasing support. NASA has just awarded funding to two new missions to explore Venus through the Discovery programme. While neither DAVINCI+ (Deep Atmosphere Venus Investigation of Noble gases, Chemistry, and Imaging) nor VERITAS (Venus Emissivity, Radio Science, InSAR, Topography, and Spectroscopy) will lead to instrumentation on the surface of this planet, these programmes represent the beginning of what may be an exciting new chapter in Venus exploration. One hope is that they will ultimately lend credence to future surface study mission concepts demanding IoT capabilities. Efforts in this direction would have additional benefits, as they would support missions to other hot planetary bodies like Mercury or gas giants – such ventures would value uncooled instrumentation technologies enabled by heterostructured GaN.

GaN's Achilles heel

Unfortunately, the innate robustness of GaN that makes it ideal for operating in extreme environments – its tolerance to high temperatures and resistance to radiation damage and chemical attack – comes at a price. The downside is that GaN is challenging to synthesize. The promising results realised with GaN micro/nanoelectronics in terms of high power, high frequency, and high temperature tend to rely on epitaxial growth of thin films on foreign substrates, such as those made from silicon, sapphire, or SiC. Growth on these non-native foundations leads to relatively high defect densities in the epilayers that present challenges to extreme environment operation.

Shortfalls in performance, stemming from the relatively high defect densities, include compromised reliability, seen in the likes of high off-state leakage currents and trapping

related phenomenon, such as current collapse. Another downside of the high defect density and resulting traps is a transient persistent photoconductivity, which degrades the light sensing capabilities in GaN. As well as plaguing lateral heterostructured GaN 2DEG devices, defect-related issues present a challenge to vertical device architectures, which are desirable for high-power applications.

The obvious solution is to slash the defect density in devices. Switching the foundation for growth to GaN should address this, but it is challenging to realise cost-effective growth of native bulk GaN substrates and epitaxial layers.

A lack of progress on this front is not a reflection of a lack of effort. For many years, a number of research groups around the world have been pursuing the growth of single-crystal GaN substrates. But as some would say, GaN substrates remain 'hard to break, hard to make'. This state-of affairs stems from the relationship between the composite elements, Ga and N, which differ in electronegativity by 1.2 – that high value reflects the highly polar covalent nature of the bonds. Such bonding accounts for melting at the extreme conditions of around 2500 °C and 4.5 GPa. Drop below this pressure and rather than melting, GaN decomposes into liquid gallium and nitrogen gas.

To circumvent the need for extremely high processing pressures, which are incompatible with today's industrial capabilities, GaN is produced by three standard methods: halide vapor phase epitaxy (HVPE), ammonothermal, and sodium-flux. Of these three, ammonothermal is the most consistent in producing relatively large-scale bulk GaN wafers. In 2021, a partnership between the Japanese Steel Corporation and Mitsubishi Chemical Corporation reported the production of 4-inch bulk GaN wafers, the largest size grown to date using the ammonothermal method. Ammonothermal reactions are a specific subset of solvothermal synthesis – where an organic liquid phase interaction is heated in a pressure-safe vessel above its boiling point. In the case of ammonothermal reactions, ammonia provides the solvent in the presence of liquid gallium.

Like all liquid-phase reactions, ammonothermal synthesis is prone to gravity-induced phenomena. They include: container interactions, thermal convection, buoyancy, and sedimentation. All actively work against the formation of low-defect, large diameter, single crystals. The hope is that new in-space manufacturing capabilities will remove gravity from the synthesis and unlock high-quality, commercial-scale GaN wafers. Semiconductor synthesis in space is an exciting new frontier tipped to play a crucial role for many decades in the 'beyond silicon' era.

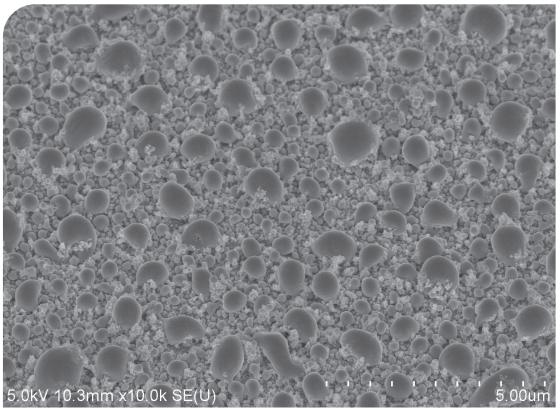
Refining GaN substrate thinning

Switching to a hydrogen-based plasma ensures high-speed etching of GaN substrates

ENGINEERS at Osaka University, Japan, are claiming to have broken new ground by thinning GaN substrates with a hydrogen-based plasma.

The team's technique, which is capable of an etching rate of up to 4 μm/minute, provides a promising approach to thinning the substrate of vertical power devices. This is needed to trim the on-resistance of vertical devices, and enable them to compete for deployment in electric vehicles.

The approach that is being pioneered by the team at Osaka University is a compelling alternative to established mechanical machining processes, such as grinding and polishing – both are used today to thin substrates. These mechanical methodologies work well when providing thinning for silicon power devices, but struggle when employed for the likes of SiC and GaN, due to issues such as cracking, chipping and warping.



➤ Scanning electron microscopy reveals gallium deposits on the surface at a flow rate of 100 sccm.

To thin GaN substrates, the engineers at Osaka University use an approach known as plasma chemical vaporisation machining (PCVM), which they have been employing and refining for more than 25 years.

"Initially we were processing silicon wafers, SOI wafers and silicon X-ray mirrors for synchrotron radiation," remarks team spokesperson Yasuhisa Sano. They started processing SiC substrates about 15 years ago, and in recent years they began to process GaN and Ga_2O_3 substrates.

One distinguising feature of PCVM is the use of a plasma pressure of several tenths of an atmosphere, which ensures a short mean path for the gas molecules and a low energy for the ions. Due to this, reactive species are not ions, but neutral radicals, which do not disrupt the atomic arrangement of the processed surface and do not warp the substrate.

Back in 2021, Sano and co-workers reported the thinning of a 2-inch SiC substrate by PCVM at a rate of 15 μm/minute, using SF_6 gas. Unfortunately, it's not possible to apply this approach directly to GaN, because SF_6 gas does not ensure etching. And chlorine-based gases, obvious contenders, are also unsuitable, because they have a corrosive nature that threatens to damage the surface of GaN devices.

These issues led the team to consider using hydrogen. Offering encouragement that this might lead to success is the use of hydrogen gas in HVPE growth of GaN, and the exitance of the gas digalane (Ga_2H_6).

Investigations involving hydrogen began with a homemade 13.56 MHz RF plasma generator, incorporating a pipe-shaped electrode with a 2 mm outer diameter and a 0.3 mm hole diameter, and a 0.4 mm-thick, 2-inch GaN substrate.

Initially, the team looked into variations in removal rate after 5 minutes, using a helium-to-hydrogen ratio of 9:1, a flow rate of 100 sccm, and RF powers of 130 W, 150 W, 180 W and 200 W. This experiment, which also considered the substrate temperature, determined that a higher power is the main driver for increasing the removal rate – it increases the number of hydrogen radicals.

Sano and co-workers went on to consider the impact of the gas flow rate, with power fixed at 180 W. They compared the etching rates at flows of 100 sccm, 500 sccm and 800 sccm, this time at a helium-to-hydrogen ratio of 19:1, shown to speed the process according to preliminary investigations. At the highest flow, etching hit 4 μm/minute, but impacted surface quality, creating what is described as a pearskin surface (see Figure).

The team attribute this morphology to spherical deposits of gallium, which may be removed by heating the surface to 40 °C and wiping it. But there is a more elegant solution: adding oxygen gas to the process. Its introduction ensured a glossy surface with a roughness of just 0.9 nm, according to atomic force microscopy.

The team are now trying to establish the process conditions for obtaining good surface roughness, according to Sano. "At the same time, efforts are being made to process a larger area, in order to bring [our technique] closer to practical application."

REFERENCE
➤ Y. Sano *et al.* Appl Phys. Express **16** 045504 (2023)

ANGELTECH

CS INTERNATIONAL CONFERENCE

PIC INTERNATIONAL CONFERENCE

PE INTERNATIONAL CONFERENCE

SAVE THE DATE

16 – 17 APRIL 2024

Sheraton Brussels Airport Hotel

To find out more about our sponsor and speaker opportunities, contact us today on: +44 (0) 2476 718970
or email:
info@csinternational.net
info@picinternational.net
info@pe-international.net

Advancing the InGaAs MOSFET

Offering greater ease of production over the HEMT, the InGaAs MOSFET is a promising candidate for very high frequency applications

RESEARCHERS from Taiwan have developed inversion-mode InGaAs MOSFETs that are claimed to produce outstanding values for transconductance and cut-off frequency (f_T).

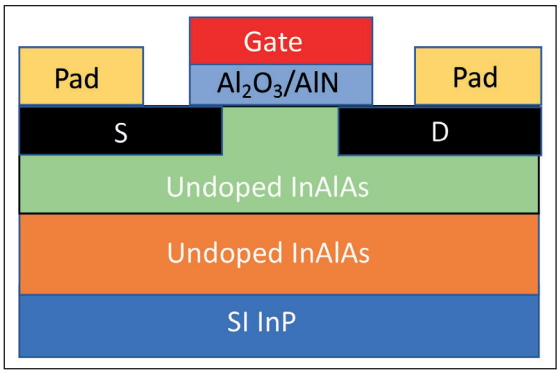
The work by the team at National Yang Ming Chiao Tung University should aid the development of sub-millimetre wave sources, which could be used in next-generation wireless communication networks and high-resolution imaging systems. According to the researchers, their transistors are an attractive alternative to GaAs-based and InP-based HEMTs that are widely used in RF applications, but are challenging to scale and require a complex epitaxial process for growth of the heterostructure.

III-V MOSFETs are said to address this concern, with those employing an InGaAs quantum-well delivering impressive results, including an f_t of 370 GHz and a maximum cut-off frequency (f_{max}) of 400 GHz.

"[But] in my opinion, quantum-well devices have an intricate epitaxial structure and complex fabrication processes," argues team spokesman Jing-Yuan Wu, who points out that their inversion-mode devices, featuring a surface channel, have a simpler structure and benefit from fabrication with a CMOS-compatible process.

While the quantum-well variants have slightly higher performance than the MOSFETs produced by Wu and co-workers, the latter is claimed to have a higher commercial value – in terms of a lower cost, as well as ease of system-on-chip integration, which is a promising feature for the future.

The team from Taiwan began the production of their transistors by loading 3-inch InP substrates into an MBE reactor and depositing a 100 nm-thick unintentionally doped InAlAs buffer, introduced to reduce signal loss, and a 50 nm-thick, lightly *p*-type doped $In_{0.53}Ga_{0.47}As$ channel. To produce devices from these epiwafers, the researchers removed the native oxide with diluted HCl, added a 10 nm Al_2O_3 cap by atomic layer deposition (ALD) that protected the $In_{0.53}Ga_{0.47}As$ surface, and used photolithography to define the active area. They then added source and drain regions by silicon implantation and rapid thermal annealing, before applying diluted HF to remove the cap, using ALD to add an AlN interfacial passivation layer and an Al_2O_3 gate dielectric, before finally introducing contacts to this structure.



➤ The InGaAs planar MOSFET fabricated by the team from National Yang Ming Chiao Tung University features a channel with a very high value for electron velocity.

Wu and co-workers compared the performance of devices with gate lengths ranging from 75 nm to 400 nm. As expected, the drain current improved with scaling, rising threefold over this range of gate lengths to peak at 816 μA/μmm under gate and drain biases of 1.0 V. The peak transconductance for the transistor with the smallest gate length, realised at a drain-source voltage of 0.7 V, is 1035 μS μm^{-1}.

Using a drain-source voltage of 0.7 V and a gate-source voltage of 0.2 V, the team combined extrapolation with a small signal model to determine values for f_t and f_{max} of 275 GHz and 75 GHz, respectively.

According to Wu, the low value for f_{max} is due to the very high resistance of the TiN gate stack. "To enhance f_{max} performance, we'll try to introduce a gold-based alloy, which has low resistance."

Values for the f_T of the team's transistor increase as the gate length decreases. Based on a TCAD simulation, they could hit 529 GHz at a 15 nm gate length.

Benchmarking with a metric that's the product of f_t and the gate length shows that the team's devices outperform silicon and other InGaAs MOSFETs.

Wu and colleagues attribute this superiority to the excellent carrier transport properties of the $In_{0.53}Ga_{0.47}As$ channel. Electron velocity in the channel is 2.88×10^7 cm s^{-1}.

According to the team, their results show that the InGaAs MOSFET has great potential for future millimetre-wave and sub-terahertz applications.

REFERENCE

➤ J.-Y. Wu *et al*. Appl. Phys. Express **16** 041007 (2023)

Improving the RF performance of β-Ga_2O_3 FETs

β-Ga_2O_3 MOSFETs realise an exceptional breakdown voltage and maximum oscillation frequency

A PARTNERSHIP between engineers at two US universities claims that to have realised a substantial improvement in the performance of β-Ga_2O_3 MOSFETs. The transistors produced by this team – a collaboration between the University at Buffalo and The Ohio State University – are said to combine a record-breaking maximum oscillation frequency (f_{max}) with a new benchmark for the field for sub-micron gate length lateral FETs.

MOSFETs made from β-Ga_2O_3 are promising devices for next-generation RF transistors, thanks to: multi-kV breakdown voltages for FETs and diodes; calculations that suggest a large saturated velocity; and many options for epitaxial growth of this oxide.

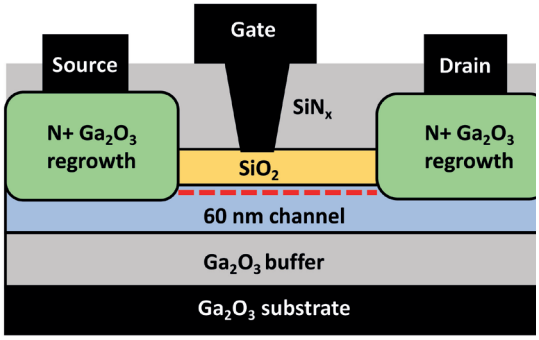
According to the team, its work could help drive the development of β-Ga_2O_3 MOSFETs that amplify signals in the L-band (1-2 GHz) and S-band (1-2 GHz). "There is potential for even higher frequency in future," adds team spokesman Uttam Singisetti from the University at Buffalo.

Back in 2021, the team reported modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ FETs with records for both f_{max} and the cut-off frequency (f_t) of 37 GHz and 30 GHz, respectively. Their devices delivered a stable RF performance up to 250 °C, but were compromised by a breakdown voltage of just 23 V.

A well-trodden approach to increasing the breakdown voltage of β-Ga_2O_3 devices involves the addition of a field plate and introduction of a larger gate length. However, while this boosts breakdown, it does so at the expense of a degraded RF performance. The larger gate length quashes the effective channel velocity, and thus leads to a longer electron transit delay. In addition, when field plates are inserted in devices with a sub-micron gate length, there's a fall in the cut-off frequency, due to parasitic capacitance.

To try and improve the breakdown of their MOSFETs without compromising RF performance, Singisetti and colleagues have turned to a highly doped contact regrowth process. Previously, this has been shown to deliver a very low contact resistance, alongside an improved transconductance and a better RF performance in β-Ga_2O_3 MESFETs and HFETs.

Fabrication of the team's highly-scaled thin-channel MOSFETs, which employ a gate oxide to realise a higher breakdown voltage, began by loading a semi-insulating native substrate into an ozone MBE chamber. They used this reactor to grow a 200 nm-thick unintentionally doped buffer layer, followed by a 60 nm-thick silicon-doped channel. Plasma-enhanced atomic layer deposition provided a 20 nm-thick layer of SiO_2 beneath a T-shaped Ni/Au gate, before regrowth by MOCVD added an n^{++} layer that provided the foundation for Ti/Au/Ni source and drain contacts added by electron-beam evaporation. Plasma-enhanced CVD of 200 nm-thick SiN ensured device passivation (see Figure).



➤ β-Ga2O3 MOSFETs produced by the University at Buffalo and The Ohio State University feature a highly scaled T-shaped gate.

DC measurements on one of the team's β-Ga_2O_3 MOSFETs with a 175 nm gate length revealed an on-resistance of 23.7 Ω mm at a gate-source voltage of 6 V, a peak transconductance of 52 mS/m at a 10 V gate bias, and a maximum drain current of 285 mA mm^{-1} – that's claimed to be comparable to the highest reported current density in Ga_2O_3 FETs.

The resistance at the interface between the re-growth layer and channel is estimated to be as high as 6.5 ± 0.6 Ω mm. This relatively large value could be due to atmospheric contaminants associated with the lack of pre-treatment, or may stem from the use of different epitaxial technologies. As fully MOCVD-grown MESFETs with low interface resistances have been reported, the team are not unduly concerned with this issue.

Biased at a gate-source voltage of -40 V, catastrophic breakdown of the MOSFETs occurred at 152 V, indicating a gate-drain breakdown voltage of 192 V and a 5.4 MV/cm average breakdown field.

High-frequency small signal measurements uncovered a record-breaking f_{max} of around 48 GHz and an f_t of 11 GHz.

One of the team's next goals to reduce the dimensions of its devices. "We plan to scale devices for more than 100 GHz f_{max}, and carry out large signal power measurements," remarks Singisetti.

REFERENCE

➤ C.N. Saho *et al*. Appl Phys. Lett. **122** 182106 (2023)

INDUSTRY SERVICES DIRECTORY

200mm Process Has Arrived

Introducing the Temescal Systems UEFC-6100

Welcome to your production future. Our UEFC-6100 is the first compound semiconductor production tool designed for 200mm lift-off processing. The world's leading manufacturers are welcoming our Auratus™ enhanced line of Temescal electron beam deposition systems, and you won't want to be left behind. We vaporize metals more efficiently. We deliver uniformity. We return unmatched savings. The results are overwhelming.

With a line of tools optimized for a range of production environments, whether 150mm or 200mm, small-batch or high-volume, this invasion could be coming your way.

Find out more before you take us to your leader. Contact Ferrotec at 1-925-371-4170 or visit temescal.ferrotec.com/200mm.

UEFC-6100
25 Wafers (200mm)

UEFC-5700
42 Wafers (150mm)
18 Wafers (200mm)

UEFC-4900
25 Wafers (150mm)

FerroTec