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VOLUME 30 ISSUE V 2024

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INSIDE

News, Analysis, Features, Editorial View, Research Review and much more

FETs: A mighty marriage

A monolithic architecture combines the merits of GaN lateral homojunctions and SiC vertical power devices

SiC: The first fully integrated facility

STMicroelectronics is building the world's first fully integrated SiC facility, partially funded by support from the EU Chips Act

Nanowires eye AR displays

The mass market seeks augmented-reality displays small enough to embed in a pair of sleek, lightweight glasses

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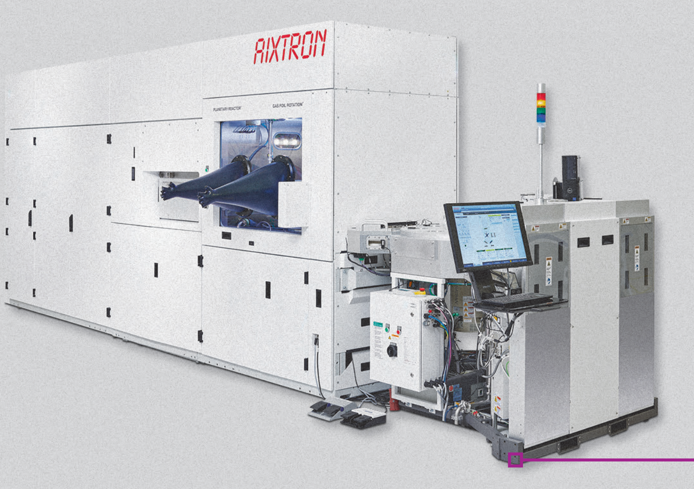

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VIEWPOINT

By Richard Stevenson, Editor

Out of our hands?

IN THE EARLY YEARS of this century, the LED industry focused its efforts on increasing the efficacy of this emitter at high drive currents. By delivering on this front, the makers of this chip would open the door to a new killer application: general lighting.

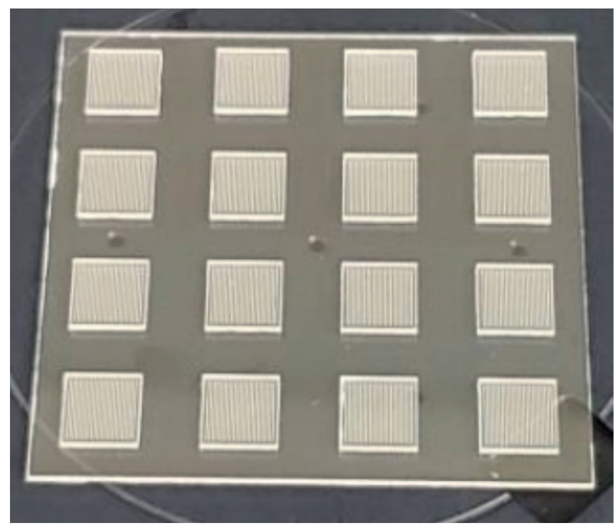
Today the focus is on shrinking the LED while retaining its efficiency. This time, success will support the commercialisation of displays based on the microLED – note that displays made from these miniature emitters are very promising candidates for a number of applications, including augmented and virtual reality, smartwatches and smartphones.

It is possible to draw parallels between then and now, with improvements to the performance of the LED helping to open up new markets. But while there is common ground, there are also crucial differences between this pair of applications for the LED.

During the development of solid-state lighting, the two biggest hurdles to commercialisation were improving the efficacy of the LED and cutting its cost. Although this form of lighting also required the optimisation of light-emitting phosphors, the development of high-performance affordable LEDs held the key to getting this product to market and ensuring its commercial success. Once the makers of LED chips started to deliver the requisite bang-per-buck, nothing stood in the way of a lighting revolution.

The same cannot be said for the microLED. It's true that it is vital to maintain the efficiency of this device during scaling, and if highly performing red LEDs could be conjured from GaN, that would substantially simplify the manufacturing process. But the reality is that whether displays based on microLEDs become a killer application is not solely in the hands of our industry.

Of the other barriers to success, the biggest is to find a way to rapidly position millions and millions of red, green and blue emitters on a backplane with sufficient precision. Over the last few years, much effort has been devoted to developing the two leading approaches, pick-and-place and laser transfer. But there are concerns over the speed of this process, as well as how to deal with



defects, ensure efficient use of material, and produce processing equipment that's affordable.

Addressing all of these concerns is a printing technique pioneered by VueReal. In this issue there's an interview with company CEO, Reza Chaji, who describes a technology involving the populating of cartridges with enough microLEDs to produce many smartwatches (see p. 14). Rather than taking these emitters from square-shaped areas of the wafer, VueReal's printing approach uses all the material, trimming costs. As this approach requires relatively low capital expenditure, the technology can also be used to pursue opportunities in smaller markets.

From our perspective, it's great to see more competition between suppliers of equipment for producing displays with microLEDs. If this printing-based method leads those focusing on other approaches to raise their game, that's good for us. How microLEDs get onto a backplane is of secondary concern – what matters is that an approach comes to the fore that enables a ramp in the production of microLED displays, and ultimately multi-billion dollar revenues for these devices.

Free weekly e-news roundup go to: compoundsemiconductor.net

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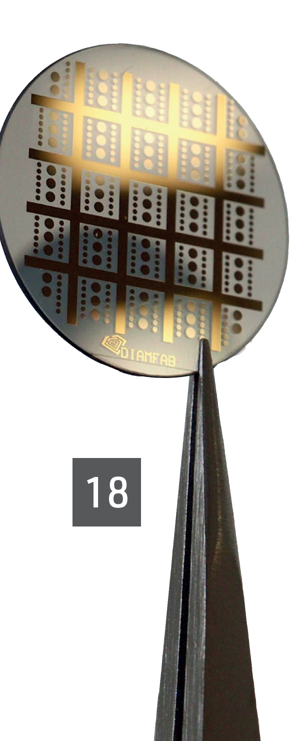

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MicroLED chip market to hit $580 million by 2028

Market will be focused on head-mounted devices and automotive applications, says TrendForce

TRENDFORCE'S *2024 MicroLED Market Trend and Cost Analysis Report* reveals that the market value of microLED chips is projected to reach $580 million by 2028, with a CAGR of 84 percent from 2023 to 2028.

Efforts to reduce the cost of microLED chips through size miniaturisation are ongoing. Companies like LGE, BOE, and Vistar continue to invest in large display applications, while AUO has been focusing on developing smartwatch products. There is also growing demand for new display applications in head-mounted devices and for automotive uses.

The inability to reduce costs and technical challenges were major factors behind the cancellation of Apple's microLED watch. Therefore, continuous optimisation of production processes remains critical for the development of the microLED industry, says TrendForce.

The evolution of mass transfer technology is expected to shift from a single to a composite technique, such as combining laser transfer with stamp transfer and potentially achieving a transfer solution with bonding capability with no stiction.

Inspection and repair processes are critical for improving yield rates and reducing microLED costs. Current electrical testing methods are being upgraded, focusing on high-precision probe cards and contactless testing. These advancements are not only leading the development of electrical testing, but also present significant business opportunities for equipment manufacturers.

The cancellation of the Apple Watch has prompted chip supplier Ams Osram to consider selling its 8-inch plant in Malaysia. If the buyer is a company within the current microLED supply chain, this could positively impact the industry's technical development and cost structure optimisation.

Considering the shift in technology routes and target markets, Chinese compound semiconductor manufacturers developing 8-inch SiC power semiconductors are also potential buyers. This would allow them to expand into international markets, providing chip manufacturers with a means to increase profitability.

Industrial opportunities for microLEDs

MicroLEDs still retains distinct advantages over competing technologies like microOLED. In AR glasses, which require light engines and high brightness and small volume, microLED light engines have now achieved sizes smaller than 0.2 cm^3.

The evolution of mass transfer technology is expected to shift from a single to a composite technique, such as combining laser transfer with stamp transfer and potentially achieving a transfer solution with bonding capability

With brightness levels advancing toward 350,000 nits, the microLED is well-suited for high-brightness, all-weather, and all-scene recognition. The rapid development of AI-assisted tools is also expected to drive demand for AR glasses with microLED displays over the next 1 to 2 years.

In the automotive sector, displays do not require extremely high PPI but demand higher contrast and reliability. MicroLED technology, with its high brightness, contrast, wide colour gamut, and fast response, can enhance the driving experience when integrated into smart cockpit display solutions with unique shapes, curves, flexibility, and feedback. This expands the potential applications of the microLED in automotive scenarios – such as AR-HUDs and P-HUDS – as well as innovative display technologies for car windows using transparent displays.

Space solar cells net $23.9 million from CHIPS Act

New Mexico-based Rocket Lab signs preliminary agreement to expand compound semiconductor solar cell production

NEW MEXICO-based Rocket Lab USA has signed a preliminary agreement with the US Department of Commerce to receive up to $23.9 million in direct funding under the CHIPS and Science Act.

The proposed investment would enable Rocket Lab to increase its production of compound semiconductor-based solar cells for spacecraft and satellites, as part of an expansion and modernisation of the company's facility in Albuquerque.

It would also help create a more robust and resilient supply of space-grade solar cells, by increasing Rocket Lab's compound semiconductor production by 50 percent within the next three years.

When Rocket Lab acquired SolAero Technologies in 2022, it became one of only two companies in the US, and three companies outside of Russia and China, that specialises in the production of radiation resistant space-grade solar cells.

The solar cells produced at Rocket Lab's facility power missions including the James Webb Space Telescope, NASA's Artemis lunar explorations, Ingenuity Mars Helicopter, and the Mars Insight Lander. Rocket Lab's technology also serves a booming commercial satellite market, such as powering the OneWeb broadband internet satellite constellation.

In addition to these proposed federal incentives, the State of New Mexico has also committed to providing financial assistance and incentives with a total value of $25.5 million to Rocket Lab in support of this effort.

"Semiconductors are central to modern life, to our economy, and to America's future. We are proud to be strengthening that future with the support of the CHIPS Office by expanding our production facilities to meet growing demand for the semiconductors that power the nation's most critical science, defense and commercial space missions," said Rocket Lab founder and CEO, Sir Peter Beck.

X-FAB and Soitec team up on SmartSiC

Partnership to bring power devices based on Soitec's SmartSiC wafers to X-FAB's fabless customers

X-FAB and semiconductor materials firm Soitec will work to offer Soitec's SmartSiC wafers for the production of SiC power devices at X-FAB's plant in Lubbock, Texas.

This collaboration follows the successful completion of the assessment phase, during which SiC power devices were manufactured at X-FAB Texas on 150 mm SmartSiC wafers. Soitec will offer X-FAB's customers easy access to the SmartSiC substrate through a joint supply chain consignment model.

SmartSiC is a proprietary Soitec technology based on the company's SmartCut process, in which a thin layer of a high-quality monocrystalline 'donor' wafer is split off and bonded to a low resistivity polycrystalline 'handle' wafer. The resulting substrate offers improved device performance and manufacturing yields. The process allows multiple re-uses of a single donor wafer, significantly reducing cost and related CO_2 emissions.

In this fast-growing market, Soitec is ramping production of SmartSiC substrates at its new plant of Bernin, near Grenoble. X-FAB is increasing production capacity for SiC devices at the Lubbock plant. The use of the SmartSiC substrate enables X-FAB's customers to design smaller devices, resulting in efficiency improvements through an increased number of dies per wafer. The benefit of reduced CO_2 emissions from the substrate manufacturing process will also contribute to X-FAB's initiative to reduce its overall carbon footprint.

Sophie Le-Guyadec, VP Procurement of X-FAB, states: "As the leading SiC foundry, we want to provide our customers the full range of opportunities to design innovative and robust SiC devices for electric vehicles, renewable power and

industrial applications. To offer the most advanced SiC processes and manufacturing capabilities, we jointly agreed to provide our customers easy access to Soitec's innovative SmartSiC via a consignment model."

Emmanuel Sabonnadiere, Soitec executive VP Automotive and Industry, comments: "Soitec's SmartSiC substrates and X-FAB's foundry services are a perfect fit to meet increasing demand for new SiC products. This cooperation is a significant milestone for the deployment of SmartSiC in the US market and internationally, thanks to X-FAB's global footprint."

DARPA awards BAE $12 million THREADS contract

THE US Defense Advanced Research Projects Agency (DARPA) has awarded BAE Systems' FAST Labs R&D organisation a $12 million contract for the *Technologies for Heat Removal in Electronics at the Device Scale* (THREADS) programme.

The DARPA THREADS program aims to overcome the temperature limits at the transistor scale inherent to power-amplifying functions. With new materials and approaches to diffusing the heat that degrades performance and mission life for MMICs, THREADS aims to resolve the thermal management challenges of today's GaN devices.

Many military systems operate at powers well below their theoretical limits because the GaN transistors

get too hot. Solving this challenge will improve the range of RF-based systems by nearly threefold. This will expand engagement distances for warfighters – taking them further out of harm's way.

"Excessive heat in electronics has been a long-standing challenge in the aerospace and defense industry," said Caprice Gray, director of Device Materials and Manufacturing Research at BAE Systems' FAST Labs. "With material and process enhancements, we are on the verge of overcoming this challenge, and doing so will unleash the hidden potential in mission critical electronic warfare and other RF-based systems."

BAE Systems will use expertise in developing and manufacturing advanced microelectronics for the program at its Microelectronics Center (MEC) located in Nashua, New Hampshire. The MEC is an accredited DoD Category 1A Trusted Supplier and manufactures GaN and GaAs integrated circuits in production quantities for critical Department of Defense programmes.

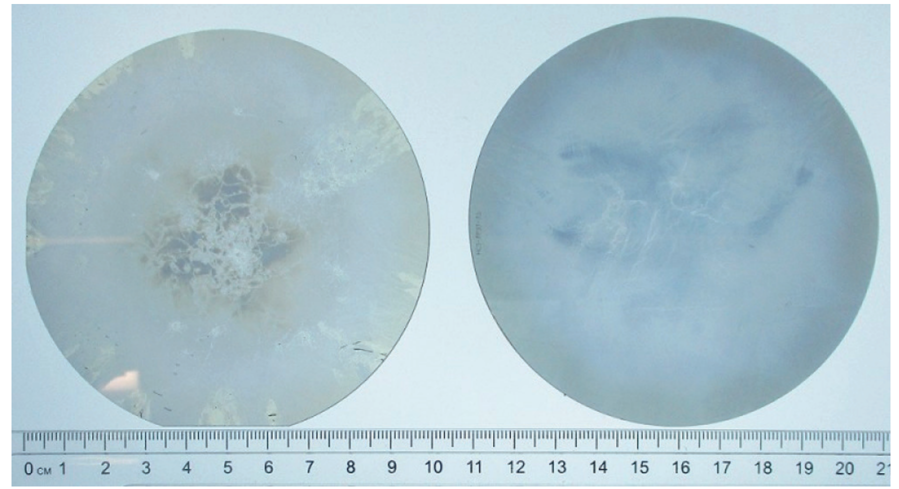
Work on the THREADS programme includes collaboration with Modern Microsystems, Penn State University, Stanford University, University of Notre Dame, and University of Texas at Dallas.

Crystal IS achieves 99% usable area on 100 mm AlN

Improved wafer quality based on specification for UVC LEDs

CRYSTAL IS, an Asahi Kasei company, has announced the successful serial production of 100 mm diameter single-crystal AlN substrates with 99 percent usable area, based on current requirements for UVC LEDs, with manufacturing to take place in the United States.

Pictured right is a comparison of Crystal IS 100 mm bulk AlN substrate from the first (left) and second (right) quarters of this year, with 90 percent and 99.3 percent usable area respectively.

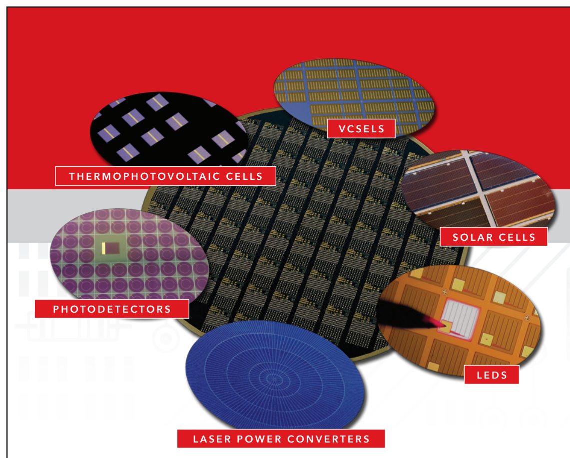


“The improvement of our large diameter substrate quality over the last nine months showcases the expertise of our team in crystal growth,” said Eoin Connolly, president and CEO of Crystal IS. “The inherent thermal benefits of AlN can enable higher performing RF and power devices in mission critical and telecom applications – we are excited to work with our partners to further develop this material to meet their needs.”

This achievement follows the company’s announcement of the first-ever recorded 100 mm diameter in August 2023, which won the Grand Prize in the category of Electronic Materials for Semiconductors in the 2024 Semiconductor of the Year Awards.

Crystal IS manufactures bulk single crystal AlN substrates at its headquarters in Green Island, New York, and began selling 2-inch diameter substrates for research and development in RF and power devices in late 2023. This 100 mm diameter milestone accelerates the development of new applications on AlN substrates as it integrates into existing fabrication lines for RF and power devices using alternative materials.

The company plans to offer 100 mm diameter substrates, which will be exclusively manufactured in its US facility, to key partners this year as they continue to expand beyond UVC LEDs.



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Infineon unveils 400 V CoolSiC MOSFETs

New family redefines power density and efficiency in AI server power supplies

INFINEON TECHNOLOGIES has extended its SiC MOSFET range to voltages below 650 V to meet the requirements of AI server power supplies.

It has now launched a 400 V CoolSiC MOSFET family, based on the second generation (G2) CoolSiC technology introduced earlier this year.

The new MOSFET portfolio was specially developed for use in the AC/DC stage of AI servers. The devices are also suitable for solar and energy storage systems, inverter motor control, industrial and auxiliary power supplies as well as solid-state circuit breakers for residential buildings.

The new family features ultra-low conduction and switching losses when compared with existing 650 V SiC and silicon MOSFETs, according to Infineon. Implemented in a multi-level PFC, the AC/DC stage of the AI Server PSU can attain a power density of more than 100 W/in^3 and is proven to reach 99.5 percent efficiency. This is an efficiency improvement of 0.3 percentage points over solutions using 650 V SiC MOSFETs.

In addition, the system solution for AI Server PSUs is completed by implementing CoolGaN transistors in the DC/DC stage. With this combination of high-performance MOSFETs and transistors, the power supply can deliver more than 8 kW with an increase in power density by a factor of more than 3 compared to current solutions.

The new MOSFET portfolio comprises a total of ten products: five $R_{DS(on)}$ classes from 11 mΩ to 45 mΩ in Kelvin-source TOLL and D^{2}PAK-7 packages with .XT package interconnect technology.

The drain-source breakdown voltage of 400 V at 25°C. makes them suitable for use in 2- and 3-level converters and for synchronous rectification. The components are 100 percent avalanche tested.

The highly robust CoolSiC technology in combination with the .XT interconnect technology enables the devices to cope with power peaks and transients caused by sudden changes in the power requirements of the AI processor.

Engineering samples of the CoolSiC MOSFET 400 V portfolio are now available and will go into series production from October 2024.

Vector Photonics raises £2.94 million

UK-BASED Vector Photonics has received £1.667 million of equity investment and £1.27 million of additional research funding, for the continued commercialisation of its unique, Surface Coupling Laser (SCL) technology.

The company believes that its SCL technology can revolutionise semiconductor laser manufacture, enhancing performance in applications as diverse as next-generation data centres, co-located optics, AI, metal and plastic printing, lidar, and optical sensing.

Neil Martin, CEO of Vector Photonics, said: "Vector Photonics' successful £1.667 million equity investment round and £1.27 million of additional research projects take its current funding total to nearly £3 million. This provides a strong financial base to continue the development and commercialisation of the company's unique and revolutionary surface-emitting laser technologies."

The equity investment comes from four companies, all of which have invested in Vector Photonics previously: Foresight WAE Technology Funds, UK Innovation & Science Seed Fund, Equity Gap and Scottish Enterprise.

The new research funding comprises two development projects. The first, FRONTIERS, is a £670k, revenue-generating, development project for free-space optics, funded by the Small Business Research Initiative.

The second, GRAPHICS, is a £600k, Innovate UK-funded grant, in collaboration with the University of Glasgow, developing GaN material processing expertise. This could lead to blue and green lasers that consume 70 percent less power than equivalent LEDs, according to Neil Martin.

Each equity investor is a next-generation technology and early-stage investment specialist. Foresight WAE Technology Funds invest in high growth-potential companies with innovative and transformational technologies; UK Innovation & Science Seed Fund is a specialist deep-tech seed fund, focused on spin outs from the UK's research base; Equity Gap is an angel investment syndicate, investing at an early stage in new technology businesses throughout Scotland; and Scottish Enterprise is Scotland's national, economic development agency and works to transform the Scottish economy by helping businesses innovate and scale.

Geely signs SiC agreement with STMicroelectronics

Multi-year contract accelerates existing cooperation around SiC devices and establishes a joint lab

STMicroelectronics and Geely Auto Group (which uses ST's third generation SiC MOSFETs in its electric traction inverters), have signed a long-term SiC supply agreement to accelerate their existing cooperation."

Under the terms of the multi-year contract, ST will provide multiple Geely Auto brands with SiC power devices for mid-to-high-end battery electric vehicles. In addition, Geely and ST have established a joint lab to exchange information and explore solutions for car electronics, such as new architectures for in-vehicle infotainment, smart cockpit systems, advanced driver assistance (ADAS), and NEVs.

As China's top automotive brand, Geely Auto sold a total of 1.68 million vehicles in 2023, with NEV sales reaching 480,000 units, accounting for 28 percent of the company's total sales for the year. This NEV sales volume represents a year-over-year increase of 48 percent.

"We are very pleased to establish a win-win cooperation with STMicroelectronics, to empower each other and fully utilise our respective advantages and resources. I believe that through the form of innovation joint lab, Geely and ST can deepen cooperation, achieve mutual benefit, and accelerate the development and implementation of innovative technologies in Geely Auto," said Li Chuanhai, president of electronic and electrical center of Geely Automotive Central Research Institute.

"Geely Auto, is a shining example of automotive innovation in China, making rapid progress in car electrification and digitalisation, while expanding its presence in the global market. This long-term SiC supply agreement and the joint lab establishment mark a significant step forward in our long-established cooperation," said Henry Cao, executive VP of sales & marketing, China Region, STMicroelectronics.

Cao added: "China is the biggest NEV market worldwide and a leading innovator. Our local competence centres and joint labs with our customers across the value chain of automotive allow ST to better support automotive innovation and transformation in China."

We cordially invite you to join the Institute of Novel Semiconductors at Shandong University

1. About Us

The Institute of Novel Semiconductors is a key academic special zone supported by Shandong University. Leveraging the solid foundation of Shandong University in the field of semiconductor material research, the institute aims at the future development direction of semiconductor material technology. It focuses on the major demands in energy, information, rail transit, and other fields, cultivating the development of new generation wide bandgap and ultra-wide bandgap semiconductor single crystal materials, enhancing breakthroughs in key technologies of semiconductor devices, and promoting application demonstrations in typical application fields.

2. Application Conditions

(A) Basic Conditions

1. Born after January 1, 1969 (inclusive);
2. In principle, should have a Ph.D. degree;
3. Have obtained a formal teaching or research position at overseas universities, research institutions, or corporate R&D institutions;
4. Have-obtained researchor technical-achievements recognized-by peers in the field,and havethepotential-to-becomea leading-academic-or-outstanding-talent-inthefield.

(B) Research Directions and Professional Fields

Growth of new generation semiconductor single crystal materials such as silicon carbide, gallium nitride, gallium oxide, diamond, aluminum nitride, boron arsenide, thin film growth, substrate processing, advanced laser technology; fabrication of power devices, optoelectronic functional devices, acoustic devices, microwave devices; and the related technology fields of packaging testing, modules, etc.

3. Compensation and Benefits

(A) **High Starting Point for Career Development:** Eligible for appointment as a professor and doctoral supervisor;
(B) **Competitive Salary:** Comprehensive annual salary not less than 600,000 RMB, with no cap on total income;
(C) **Sufficient Research Funding:** Research funding ranging from 3 to 10 million RMB during the employment period;
(D) **Excellent Working and Living Conditions:** Offers a settling-in and housing subsidy of 2.5 million RMB for the National talents;
(E) **High-Quality Team Resources:** Provides full quotas for recruiting PhD students and postdoctoral researchers during the employment period;
(F) **Additional Support:** Offers first-class medical and healthcare services for talents, and provides leading domestic basic education for the children of talents. Assistance in resolving spouse employment issues.

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Cardiff will lead UK manufacturing hub

University to share £99 million in funding to lead new compound semiconductor hub

CARDIFF UNIVERSITY will receive a share of £99 million in funding to lead a new compound semiconductor manufacturing hub.

The hub aims to capitalise on the huge opportunity of compound semiconductor manufacturing identified in the UK's national semiconductor strategy.

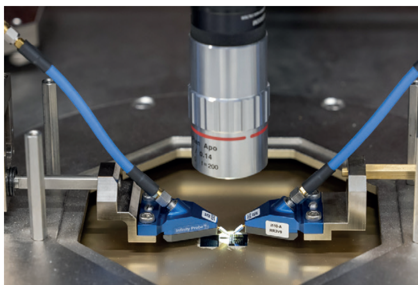
The researchers will develop energy-efficient opto-electronics for use in key emerging technologies, such as quantum, the 6G network, sensors for autonomous vehicles, the internet of things and satellite communications.

A key driver for the hub will be to expand the environmental benefits of compound semiconductors, by carrying out their research in an environmentally friendly way, developing new manufacturing processes and creating new devices that are energy efficient along the way.

Peter Smowton, the Cardiff hub lead and managing director of Cardiff University's Institute for Compound Semiconductors, said: "This award is an endorsement of our vision to establish the UK as the primary global research and manufacturing hub for compound semiconductor (CS) technologies, expanding and extending the CS Cluster here in South Wales that our previous EPSRC Manufacturing Hub initiated.

"Supported by new start-ups and inward investment into our region, the hub will be at the very heart of the cluster ensuring we can continue to develop CS technologies which enable our connected world, our health, our security and protect the environment.

"The time is right for a step-change in CS manufacturing and we can't wait to get started here in Cardiff."



The five manufacturing research hubs are supported by the Engineering and Physical Sciences Research Council (EPSRC), part of UK Research and Innovation, with an investment of £55 million. Each hub is receiving £11 million. Partner contributions, cash and in-kind, takes the total support committed to the new hubs to £99.3 million.

The hubs aim to address a wide range of challenges in commercialising early-stage research within different manufacturing sectors by reducing waste, finding alternatives to expensive or environmentally damaging materials, and speeding up processes.

Working with industry partners, the researchers will also explore different pathways to manufacture, including production scale-up and integration within the wider industrial system.

Advances in environmental sustainability across manufacturing processes are also a focus of the hubs, which hope to bolster the economy though efficiencies, such as reducing waste, emissions and pollution, and lowering production costs.

EPSRC executive chair Charlotte Deane said: "Given the scale and importance of the UK's manufacturing sector we must ensure that it is able to benefit fully from advances made across the research and innovation ecosystem.

"With their focus on innovation and sustainability, the advances made by the hubs will benefit specific sectors, the wider manufacturing sector and economy, as well as the environment."

Chris Meadows, director of CSconnected, the compound semiconductor cluster based in Wales, said: "Wales is internationally recognised for its world leading activities in compound semiconductors and has successfully attracted investment and economic growth over the last few years."

"The formation of the new institute will provide a key role in coordinating national research, development and innovation programmes, as well as addressing education and skills needs that are required to support the growth of our industry. We look forward to working closely with the new Institute"

Wyn Meredith, chair of CSconnected added: "The South Wales based CSconnected compound semiconductor cluster has a well established track record in contributing to the UK's semiconductor industry, which is demonstrated by the many initiatives and investments across the region."

Cardiff University researchers will also support the Sustainable Chemicals and Materials Manufacturing hub led by the University of Oxford and the Advanced Metrology for Sustainable Manufacturing hub led by the University of Huddersfield.

Other UK hubs announced include: the MediForge Hub led by the University of Strathclyde; and the Manufacturing Research Hub in Resource-Enabled Sustainable Circular Automation Manufacturing (RESCu-M) led by the University of Birmingham.

Pictured above: Characterisation of a GaN-based microwave monolithic integrated circuit in the labs at Cardiff University's Translational Research Hub.

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Printing microLED displays

Populating cartridges with microLEDs to print emitters on backplanes promises to drive a revolution in display technology

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

DISPLAYS based on the microLED have a great deal of potential, but face formidable challenges. The appeal of this technology is a combination of tremendous colour quality and brightness, an exceptional degree of ruggedness, and high levels of efficiency, which extend the battery life of portable devices. But producing this class of display involves positioning millions and millions of microLEDs on a backplane, followed by their connection to drive electronics – and transferring all these pixels with sufficient speed is far from trivial.

Despite several years of substantial investment, the two leading techniques for assembling microLED displays – pick-and-place and laser-based transfer – are struggling to make a significant impact. This leads one to wonder whether further effort on these fronts will reap reward. Or does it make more sense to pursue an alternative approach that avoids their weaknesses?

Arguing for the latter, and championing the production of displays with a printing process, is Reza Chaji, CEO of VueReal. He has much valuable experience in this sector, having previously led Ignis Innovation, a developer of technology that's improved the uniformity and lifetime of pixels used in OLED displays. These advances now feature in LG's OLED TVs.

In 2016, Chaji started VueReal, which has a 60-strong team that made a big splash at *Display Week 2024*. At this show, held in mid-May 2024, the company championed it printing technology and unveiled two complimentary technologies: dynamic quantum-dot patterning, and a method to increase the fidelity of displays with a liquid-crystal-on-silicon backplane.

➤ AD300Pro with panel loader

The foundation for all this promise is VueReal's proprietary cartridge technology, which allows microLEDs to be held very tightly before they are released to the display substrate by controlling electrostatic forces. The cartridges can also integrate sensors and other forms of chip, using a three-dimensional stacking approach.

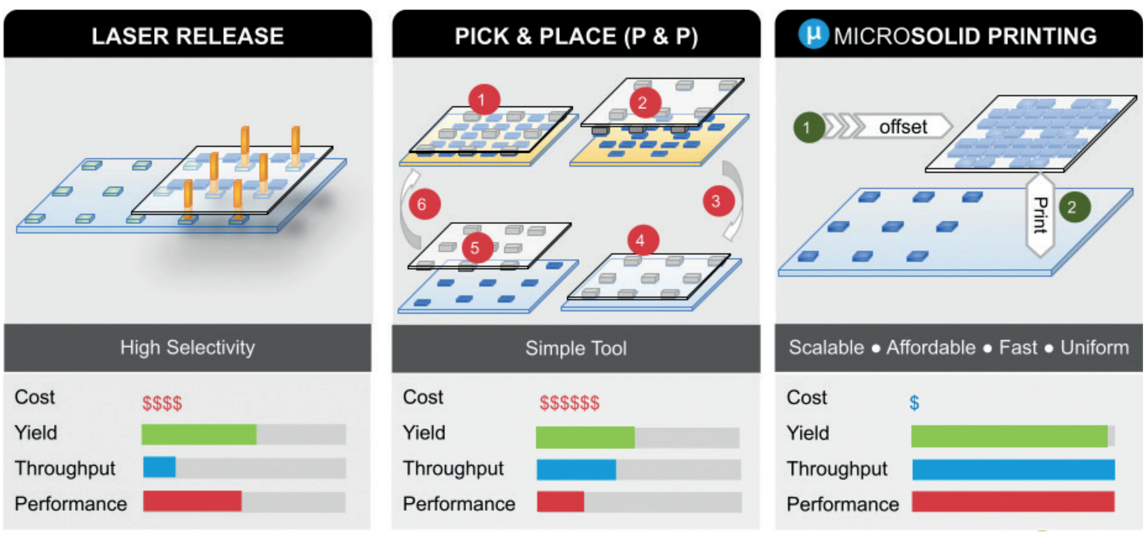
"Our main focus has been on transfer – how to integrate devices from the original wafers onto the substrate with high yield, high throughput," remarks Chaji. He argues that VueReal's laser-free process is relatively simple and low in cost.

One option for producing displays with this company's technology is to load the cartridge with one colour of microLED, print these devices, and then load and print with each of the two other primary colours. But it's also possible to populate the cartridge with all three colours of microLED, an approach demonstrated by VueReal a couple of years ago.

Today, most of the company's customers prefer to just load one colour of microLED onto the cartridge, as this approach offers greater control over colour uniformity and results in a higher yield. But as the printing process matures, Chaji expects customers to populate cartridges with red, green and blue microLEDs, to trim the time taken to produce displays. The cartridges are capable of holding millions of microLEDs. "With one cartridge, we can populate 16 smartwatches," says Chaji.

The problems of pick-and-place

Before developing the printing process, Chaji and his colleagues carefully considered the potential of both pick-and-place and laser-based transfer for high-volume production of displays. They reasoned that to make an impact, the process for transferring microLEDs to a backplane would have to be fast enough to allow this technology to be competitive with the manufacture of displays based on OLEDs, which are transferred to glass in less than 10 minutes. The team concluded that the



➤ VueReal claims that its cartridge-based approach offers cost, yield, throughput and performance benefits over the leading alternative methods.

transfer of microLEDs would have to involve multiple heads, leading to many moving parts and hampering alignment.

One advantage of printing over pick-and-place is speed, with the time taken to populate an area falling from between 15 and 25 seconds to less than 8 seconds. Another benefit is the efficient use of material. With pick-and-place, as well as laser-based transfer, microLEDs are taken from square-shaped areas, preventing many devices from ever being used. That's not the case with the VueReal printing process, which uses near all of the wafer. What's more, devices can be packed very close together – a spacing of less than 2 μm has been demonstrated.

Regardless of the transfer process, display manufacture is impeded by defects and non-uniformity in microLED wafers. But this is far less of a concern when using the VueReal approach, as losses are minimised by employing multiple, small cartridges, and scrutinising wafers with a combination of visual inspection, photoluminescence and selective electroluminescence. While some defects still get through, by driving down numbers the cost to address them is not prohibitive. "If you have hundreds of defects, it's easy to repair," says Chaji.

What may raise an eyebrow to many within our industry is that most of the defects that engineers at VueReal encounter don't come from the microLEDs, but the backplane. To address this, the company has developed an inspection tool to expose those defects, so that they can be eliminated prior to transfer.

The allure of the laser

During considerations of laser-based transfer, Chaji and his colleagues concluded that a raster-based scanning approach fails to deliver sufficient throughput, and any attempts to address this with multiple beams requires incredibly complex optics. This led the team at VueReal to invent a patented solution involving a shadow mask and mass exposure. However, even with this refinement, laser-based approaches still involve substantial capital expenditure, high operating costs, and issues associated with material costs.

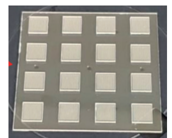
By addressing these weaknesses with its printing approach, VueReal's technology is not just suitable for high-volume production. It is also better suited for making customised products, because the tool is easy to operate, and offers low maintenance and low capital expenditure.

VueReal is not focusing on one particular market to promote its printing process. Instead, it views its user-friendly technology as suitable for the manufacture of many different products, including those that serve in the automotive, consumer electronics and healthcare sectors. The company is heavily engaged with many customers in the automotive market, where its printing technology can be used to make displays with various degrees of transparency. "MicroLEDs are inherently transparent," says Chaji, adding that if an opaque display is required, that's also possible.

The other markets offering the greatest potential today for VueReal are wearables and augmented-reality. For the latter, miniaturisation is in high demand, with an end goal of red, green and blue emitters sitting side-by-side at a 3 μm pitch.

Chaji believes that it's going to take a long time to reach that target, and that the objective might be easier to realise with VueReal's recently unveiled colour fusion technology. This combines slightly larger, more efficient microLEDs with liquid-crystal-on-silicon technology that enhances resolution. The result is a competitively priced, high-resolution display.

To help makers of displays based on the microLED trim their costs when adopting VueReal's technology, the company offers many options to its customers. It can provide all the tools for manufacture, or just the printer, if a company is already active in producing displays. This accommodating approach will be welcomed with the microLED display industry, which must now step beyond hype and start making money.



➤ At the heart of VueReal's technology is the printing of microLEDs, which are loaded on a cartridge.

The world's first fully integrated SiC facility

Backed by substantial funding from the EU Chips Act, STMicroelectronics is starting to build the world's first fully integrated SiC facility in Catania, Italy

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

TO MUCH FANFARE, the power electronics giant STMicroelectronics has unveiled plans to build a 200 mm integrated SiC facility in Catania, Italy.

ST announced this initiative, with a projected cost of €5 billion – supported by €2 billion of funding from the State of Italy in the framework of the EU Chips Act – on 31 May at a high-profile event in Catania involving many dignitaries.

President and CEO of ST, Jean-Marc Chery, opened presentations at this gathering by remarking: "I am really proud to welcome you here to share the progress we are making on investing here in ST, in Catania – but also in the future of Italy and Europe."

Chery put the latest venture in perspective by explaining that around 18 months ago, at the company's cherished site at Catania, ST showcased its ongoing work to create the first SiC substrate manufacturing facility. "We are not here to only check on the progress made on our SiC production facility, but to proudly announce the measured next step."

This next step is the construction of a vertically integrated 200 mm SiC campus that includes SiC substrate development, epitaxial growth processes, front-end wafer fabrication, module back-end assembly, and a number of R&D initiatives. Production of SiC products at this campus is set to start in 2026, and ramp to full-capacity, involving the processing of 15,000 wafers per week, by 2033.

➤ Above: ST will build the world's first fully integrated SiC facility in Catania, Italy. Here is an artist's rendering of a completed facility.

Locating this vertically integrated facility in Catania makes much sense, given the rich history of SiC development that's taken place in this region, driven by pioneers at ST, who initially worked with researchers at the University of Catania and in time with those at CNR.

Key milestones for ST that have been spearheaded by its team at Catania, include: the company's first demonstration of a SiC diode in 2002; ST's first production of SiC diodes in 2007; the launch of first-generation SiC MOSFETs and third-generation SiC diodes in 2014; and advances in SiC substrate manufacturing, with 150 mm production beginning in 2020 and 200 mm variants demonstrated the following year.

Offering greater insight into the role of local production within this global firm, Giuseppe Notarnicola, President STMicroelectronics Italy, told those gathering in Catania that this site is home to nearly 5,300 staff. He added that over one-quarter of those working at this location on the eastern side of the island of Sicily are in the R&D department, which files an average of 70 patents per year.

Notarnicola revealed that the efforts already underway to produce the SiC substrate manufacturing facility are supported by an investment of €730 million, with almost €300 million of funding coming from the European Union. This particular initiative, expected to create an additional 700 jobs, will lead to an increase in the production of SiC material, with full capacity forecast in 2026.

Since ST started volume production of SiC power electronics in 2017, it has shipped more than 500 million devices, while expanding its portfolio to now encompass MOSFETs ranging from 650 V to 2.2 kV and diodes spanning 600 V to 1.2 kV.

Today the company produces SiC devices in high volumes at its 150 mm facilities in Catania and Ang Mo Kio, Singapore. Both these sites, which are undergoing capacity expansion, are equipped with equipment that is 200 mm compatible. At Catania, the industrialisation of a 200 mm line is already underway.

In partnership with Sa'nan Optoelectronics, ST is starting to build a third hub – a 200 mm foundry in Chongqing, China. ST aims to start producing devices at this facility in late 2025, with full buildout scheduled by 2028. The plans for this joint venture are to produce SiC devices exclusively for ST using its proprietary process technologies, with products only being used to supply the local Chinese market.

Sa'nan's role in this partnership includes the building and operation of a separate 200 mm SiC plant to service the joint venture. SiC chips produced by the collaboration will be processed at ST's existing back-end facility in Shenzhen, enabling the European powerhouse to offer its Chinese customers a fully integrated SiC supply chain.

The ramp in SiC diodes and MOSFETs produced by ST will drive deployment of these devices in automotive, industrial, AI and cloud infrastructure sectors.

Automotive opportunities

Attendees at the recent event in Catania gained a perspective on the role of these wide bandgap devices in the automotive industry from a pre-recorded presentation delivered by Florian Weig, SVP Purchasing and Supplier Network Digital BMW Group.

Weig noted that BMW's portfolio of electric vehicles is expanding. Large-scale production of the group's first all-electric model, the BMW i3, began in 2013, and by the end of this year it could be offering more than 15 models, including those in the Rolls-Royce and Mini range. By 2030, it is possible that fully electric vehicles could even account for half of the company's global sales.

"Semiconductor technology plays a very important role in enabling this evolution," argued Weig, adding: "Among the technologies needed, silicon carbide is key for the creation of highly efficient electric drivetrain architectures and battery charging systems."

According to Weig, it is of high importance for BMW to have access to SiC technology from suppliers that can support and adapt to its needs during the design process, and guarantee meeting requirements for quality, reliability and volume.

"ST's investments in its Catania facilities are important for our future cooperation," claimed Weig.

"Working together with ST in Catania, we have access to an integrated site for silicon carbide with technology development, product development, and application testing labs, as well as a high-volume, fully integrated manufacturing facility."

Additional facilities operated by ST include automotive-qualified, high-volume assembly and test operations in Bouskoura, Morocco and Shenzhen, China. This gives ST a global footprint – but there is clearly much affection for its extensive roots in Catania, where efforts will continue to maintain leading-edge production of power-electronic devices.

The transistor of the future

Improvements in substrate quality and size, alongside a market primed for accepting new semiconductors, gives the diamond transistor a great chance of commercial success

BY GAUTHIER CHICOT AND IVAN LLAURADO FROM DIAMFAB

FOR DECADES, the diamond transistor has held much promise. However, its performance is yet to fulfil expectations. So why are there grounds for optimism?

That's a tricky question. One might simply respond with the slightly flippant rebuff: 'Well, why not?'. But you probably have a healthy degree of scepticism, and demand a more nuanced explanation – and I'm delighted to provide just that, by sharing the vision we have at Diamfab for this technology.

Before we dive into that, let's begin by recapping the development of diamond for technological applications. The story begins in 1954, when humanity manufactured diamond for the first time, using high-temperature high-pressure techniques. Building on this milestone, the 1980s witnessed the first growth of diamond by CVD, followed by the exploration of doping processes in the 1990s. Since then, those involved in developing synthetic diamond have expanded their knowledge of this material, in terms of characterisation, manufacturing and processing.

As we learn more about the properties of diamond as a semiconductor, the bigger its promise appears – but for some, the bigger the frustration too, as we might have expected a faster development process due to its enormous potential.

The power of diamond

As a material for power electronics, what is the promise of diamond? Well, it has an ultra-wide band gap, an exceptional carrier mobility, a breakdown voltage estimated at a tantalizing 10 MV/cm, and the best-known thermal conductivity. Thanks to these phenomenal attributes, diamond has been called the ultimate power semiconductor. Devices made from this form of carbon have the potential to boost the voltage of components while increasing their efficiency, trimming losses and cutting costs.

To illustrate the gulf in the performance of different materials, think about a basketball and its court. The ball's surface area represents a diamond component with a given resistance for a 1000 V breaking voltage capacity. And the court? Well, its surface area represents these values for silicon. So, as you can see, there's a staggering difference in the performance ratio of these two materials in the key figure of merit for power semiconductors.

At the system level, diamond promises to improve all the key characteristics that enable increased power efficiency. Gains come from: simplified thermal management; a better trade-off between increases in the component and system competitiveness/energy efficiency, and a trimming of volume and weight; and a reduction in CO_2 emissions, compared with the manufacture of SiC substrates.

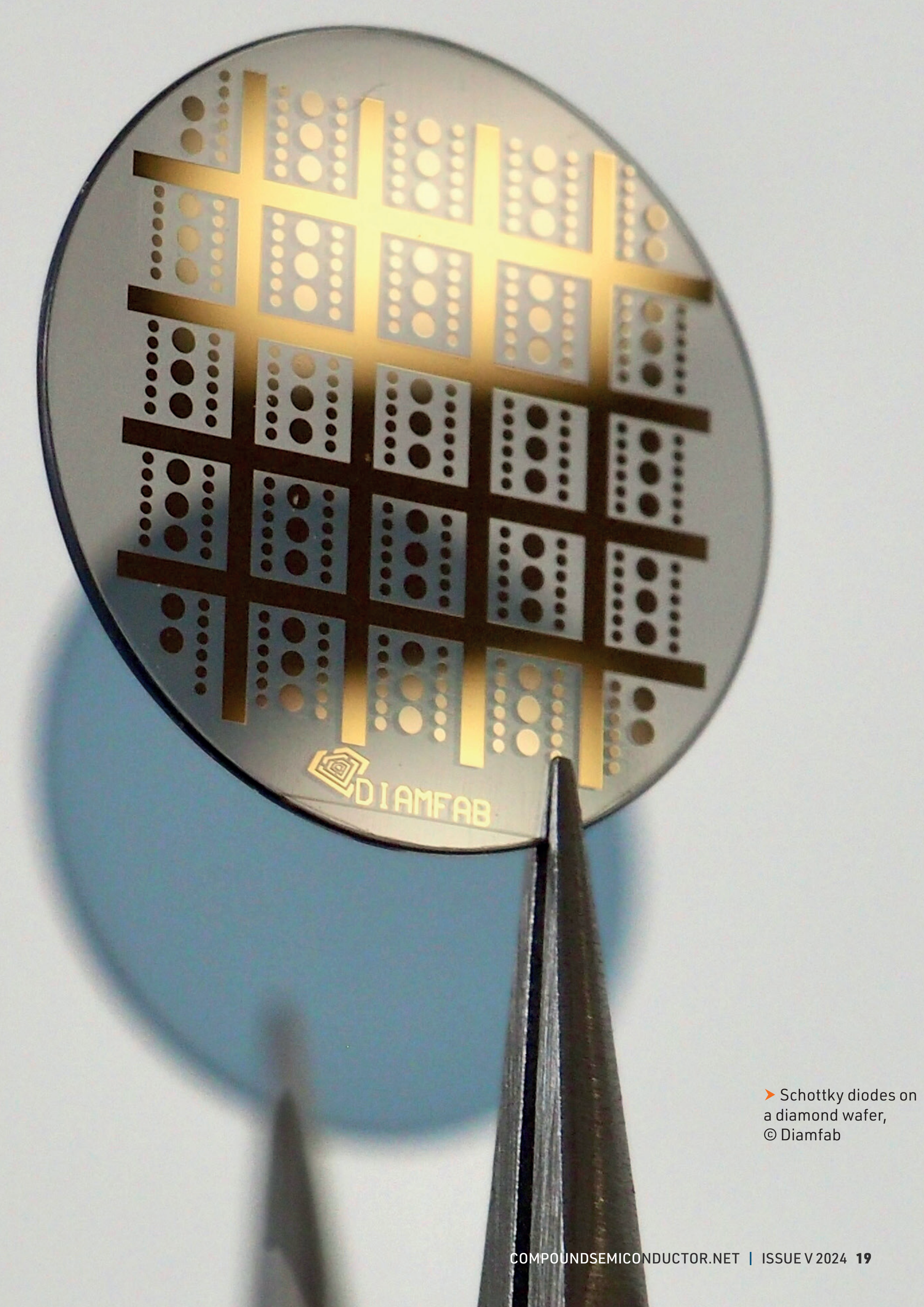
These are compelling advantages, giving good reason to be optimistic. And this positive outlook should not diminish when one considers the two biggest factors determining commercial success – the level of technological maturity, and the market situation.

When it comes to technology, three historical roadblocks have to be solved before diamond will become a commercial reality. These barriers are an increase in the size of a diamond wafer, improvements to its quality, and a better approach to doping.

The good news is that all these challenges are being addressed by the diamond industry. At Diamfab, we are making major contributions to this effort, with our development focusing on improving material quality through a reduction in the density of imperfections, and mastering doping.

It's far from easy to grow large diamond crystals, the starting point for substrate production. For other semiconductor technologies, investment in the research and development of crystal growth has come from defence applications. While that's also a source of funding for developing diamond, it's not the only one – it's also possible to leverage knowledge from other industries, such as jewellery. Drawing on all of this has ensured rapid material progress. Single-crystal wafers with a 100 mm diameter have already been demonstrated, a great advance considering that just a few years ago only 2 mm or 3 mm wafers were commercially available.

The doping of diamond is a considerable challenge. Unfortunately, diffusion and implantation are neither suitable nor recommended. Attempts to dope



Schottky diodes on a diamond wafer, © Diamfab

diamond by diffusion are thwarted by a carbon lattice so dense that potential dopants, such as boron, nitrogen and phosphorus, cannot penetrate into this material. Meanwhile, implantation is hampered by high levels of inefficiency, causing irreparable damage to the crystalline lattice.

Due to these formidable issues, doping must be undertaken *in situ*, during the growth of diamond. It's a process we've mastered at Diamfab, realising levels of doping that span from the non-intentionally doped, all the way through intermediate values to metal-like levels. We are also making good progress at improving crystal quality, and we expect to announce exciting news soon.

In a nutshell, from both a material and component manufacturing perspective, the primary technological hurdles are either overcome or there is a clear view on how to solve them. And where further progress is required, a great deal can be garnered by studying developments associated with compound semiconductor materials and devices.

In terms of market acceptance, we are living in a world that's in the midst of revolution, where major megatrends have a common factor: a quest for electrification, sustainability, and efficiency. This is driving demand for efficient power electronics. That's a stark contrast to the early years of this millennium, when trains, motor drives and UPS accounted for essentially all power electronics – and none of these sectors drove the economy.

The recent trend is highlighted in a BloombergNEF 2023 report, which claims global investment in the energy transition hit a record $1.8 trillion in 2023, up 17 percent on the previous year. With vast sums of money now flowing into the power electronics sector, commercialisation of diamond power electronics should find financial backing.

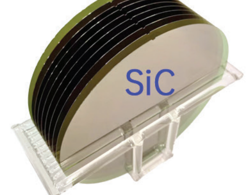
Finally, when we take a closer look at the power electronics market, we see that thanks to the emergence of SiC and GaN, engineers have now started to appreciate how the choice of semiconductor can govern a system's performance and cost. This first-hand experience of understanding the benefits of moving beyond silicon will lower the barrier to adoption of the diamond transistor.

At Diamfab, we are in no doubt that diamond will provide an alternative class of power electronics during this decade, with this semiconductor destined to fulfil its promise. Due to this, we invite everyone in the power electronic sector working with other semiconductors, from academics to integrators, to explore diamond's potential, and consider how they can contribute their know-how to this technology of tomorrow. Diamond is assured a very promising future, and there are many exciting topics well worth pursuing.

SUMMIT CRYSTAL

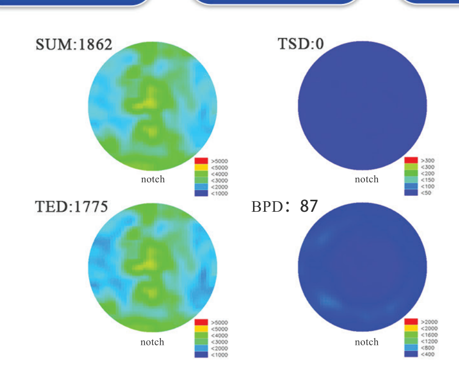
Guangzhou Summit Crystal Semiconductor Co., Ltd, a National High-Tech Enterprise, is engaged in the R&D, production and sales of Silicon Carbide (SiC) single crystal material.
The company has capability in mass production of 8-inch 4H-SiC n-type Substrate with 0 MPD, 0 TSD, 0 SF and low BPD (≤200cm^{-2}).

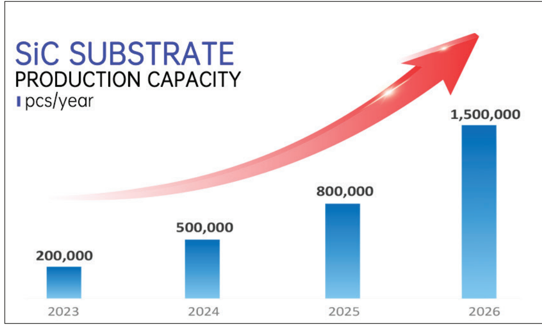
0 MPD 0 TSD 0 SF



8-inch 4H-SiC Substrate

8-inch 4H-SiC Ingot





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Optimised SiC boule fabrication

Producing SiC substrates has never been easier, thanks to the BoulePro-200AX, a versatile tool packed with various features that exposes foreign polytypes with UV light and employs X-ray diffraction to determine and correct for crystal orientation

BY JAMES CARL FROM USACH

SALES OF SiC devices are rising fast, thanks to their increasing deployment in a wide array of applications, including electric vehicles and renewable energy systems. The uptake of these devices is driven by their superior properties, such as a higher thermal conductivity, greater efficiency, and the ability to operate at higher temperatures and voltages.

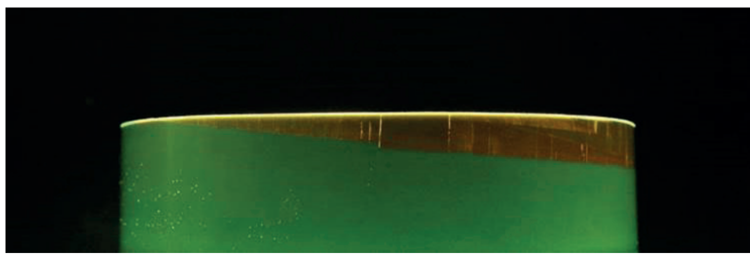
The ever-growing demand for SiC material and devices is motivating those working in this industry to innovate and enhance their production processes. Helping them in this endeavour is the BoulePro-200AX produced by our company, USACH. Designed to meet the evolving needs of the SiC industry, this industry-standard tool for fabricating boules is setting new benchmarks for efficiency and quality, while empowering manufacturers to meet the surging demand for high-quality materials. The valued strengths of the BoulePro-200AX make it an indispensable tool for every company striving to stay ahead in the dynamic SiC landscape.

Meeting growing demands

Historically, the leading producers of SiC substrates have been based in the US and Europe. But China is catching up fast, with its players making rapid advances in quantity, wafer size, and quality. Now the race is now on to establish readily available 200 mm material with a high quality that will provide chipmakers with the edge over their competition.

The growth in the number of suppliers of SiC substrates, along with an increase in the size of this material, will help meet the rise in global demand. Ideally, against this backdrop there will be an increase in the range of applications where SiC serves, and a reduction in SiC substrate costs – goals where the BoulePro-200AX technology will play a pivotal role, by ensuring that the SiC boules are manufactured with high throughput to the highest standards of quality and precision.

To meet the increasing demand for our BoulePro-200AX, we have invested more than $720,000 in upgrading our facilities in Elgin, Illinois, a move that reflects our commitment to serving SiC manufacturers with cutting-edge technology and exceptional customer service. As part of this initiative, we have added 11 new assembly bays and more than 10,000 square feet of dedicated space, initiatives that boost our production capacity by up to 200 percent. Additionally, we have established a dedicated BoulePro demo/testing showroom, allowing our customers to see their machines in action and conduct part runoffs before delivery. These investments ensure that we are well-prepared to handle the growing interest in the BoulePro-200AX, which already has multiple units in operation running both 150 mm and 200 mm capable platforms. Over the coming months we have appointments in the diary for demonstrations with several potential customers.



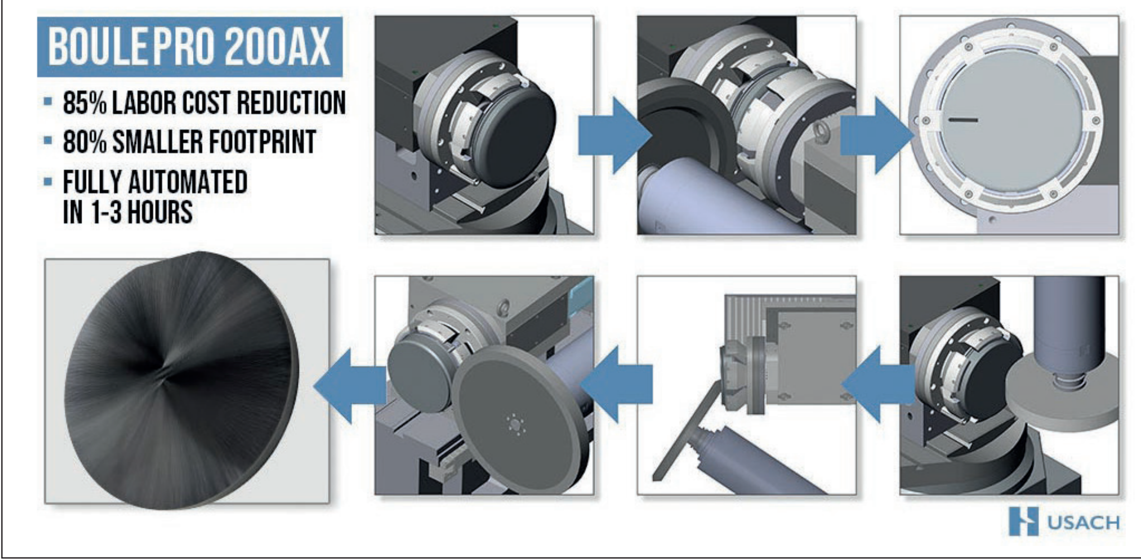
Illuminating boules with UV light exposes foreign polytypes.

Our facility upgrades are not just about increasing our capacity – they have also been introduced to enhance customer experience. Our new conference room and customer café provide a welcoming environment for our clients and help us foster stronger relationships and facilitate better communication. These improvements underscore our dedication to providing a comprehensive service that goes beyond just delivering a product, and reflect our commitment to ensuring our customers have all the support they need to maximise the benefits of the BoulePro-200AX.

Exposing foreign polytypes

Recently, we have been collaborating with several SiC producers to integrate a module that detects foreign polytypes into the BoulePro. This addition allows operators to streamline and automate the identification and elimination of unwanted foreign polytypes during the grinding process. While the core methodology – using a UV lamp to highlight different polytypes – is well-established in the industry, integrating this capability into a grinding machine is a first.

During any stage of fabrication, the boule can be sent to the foreign polytype detection module. During inspection, the boule is held in the primary workhead on the seed side, and the module covers the workholding to block ambient light. The boule



The BoulePro200AX offers many advantages over conventional approaches for processing SiC material into pucks for producing substrates.

➤ The digital twin software package helps to streamline the processing of SiC.

is rotated by the workhead inside the module containing both a UV light source and vision system that exposes and identifies the location of foreign polytypes, which are subsequently removed by additional grinding. This process can also be applied with the boule held on the dome side, to identify and remove polytypes located on the seed side.

Introducing the foreign polytype detection module, which enhances the SiC boule fabrication process by reducing the need for operator intervention, is part of our ongoing commitment to developing tools so that they remain at the cutting edge of technology. This is accomplished by anticipating future demands and providing customers with tools that will keep them competitive in a rapidly evolving market.

Speeding optimisation

As crystal growth technologies are highly proprietary, and for some producers have been developed in secret over decades, the as-grown boule can take many forms in terms of its geometry, defect location, and crystal orientation. Due to this, each customer that enters our facility brings material for a demonstration grind that requires a unique process development phase. Centred versus offset grinding, smaller or larger crystal orientation corrections, round versus non-round grinding, and the transfer of the boule from the primary chuck to the secondary chuck and vice versa during different stages of fabrication are just some of the factors that we need to consider when developing a particular customer recipe.

One new technology we are employing to streamline this process is a digital twin software package. The digital twin, an identical replica of the machine itself, allows complex sequences of events to be programmed and tested in advance of working with customer material. While there are several advantages to using the digital twin, optimisation of a particular customer material's cycle time is a primary benefit and ultimately one of the main levers to driving down costs. As the machine movements in the digital twin are on a 1:1 time scale with reality, our team can explore different sequences of fabrication, while keeping in mind customer requirements, in digital space.

This trims costs and reduces the time it takes to come to an optimised recipe for a given set of as-grown boule conditions. As boules are highly valuable – they can be worth tens of thousands of dollars per boule, depending on height – it is easy to see the advantages of turning to digital space to support process optimisation.

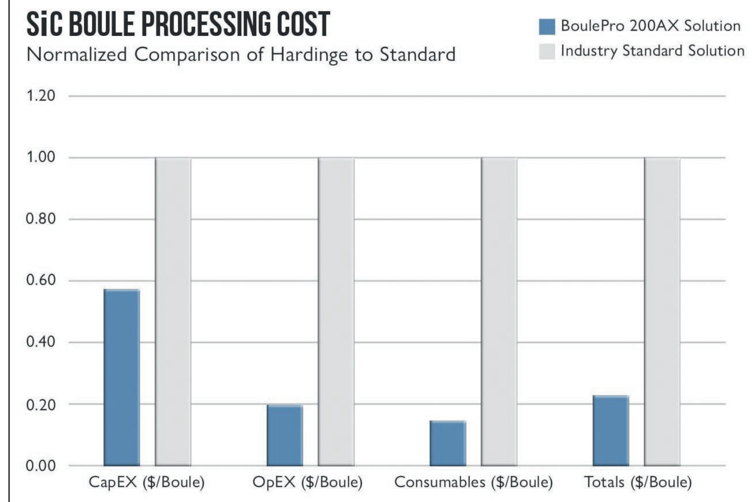
Process methodology

Our fully automated BoulePro 200AX is already revolutionising SiC manufacturing by processing as-grown SiC boules into wafer-ready pucks without the need for gluing, external material setup, or manual intervention. This single setup machine is replacing multiple tools in the traditional boule fabrication process to create a more streamlined and efficient workflow.

Dramatically shortening the boule-to-puck conversion process is the BoulePro's single-step, dual-plane compensation capability, enabled by integrating an X-ray diffraction tool. Compared with traditional methods, our BoulePro trims cycle time by up to nearly 95 percent, making it significantly more productive.

Additional strengths of the BoulePro are its automatic tool changers, and its flexible design, accommodating various boule geometries and customer requirements. These strengths make the 200AX the most efficient, flexible, and cost-effective tool for the growing SiC market.

To ensure that the boule is securely held during the grinding process, our tool employs advanced gripping techniques. Both workheads utilise vacuum technology to secure the part, while OD gripping jaws hold the outside of the part during face grinding. This dual support system enables aggressive grinding, shortening fabrication cycle times without damaging the part. In comparison,



➤ Savings on multiple fronts are possible with the BoulePro200AX.

traditional methods are cumbersome, involving gluing the part to a spindle.

By eliminating the need for multiple machines, reducing the number of handling steps, and turning to automation and integration of advanced technologies, our BoulePro minimises the risk of inadvertent damage to the part and the potential for human error during processing. This leads to higher yields and better-quality products, which are critical for the demanding applications that rely on SiC substrates. The machine's ability to perform all the necessary grinding operations in a single setup also trims the overall footprint of the manufacturing process, saving valuable space in production facilities.

The key benefits of our ground-breaking tool, including streamlined automation, enhanced process repeatability, reductions in costs and manufacturing footprint, and a higher level of accuracy, are listed in the text box "Six key strengths of the BoulePro 200AX".

Six key strengths of the BoulePro 200AX

THE USACH BoulePro 200AX is an indispensable tool for SiC manufacturers. Its strengths include:

- **Streamlined automation:** The boule-to-puck conversion process proceeds within a fully automated framework in just one-to-three hours, based on an as-grown geometry.
- **Enhanced process repeatability:** Advanced automation ensures consistent, high-quality wafer-ready SiC pucks.
- **Significant labour cost reduction:** Producers realise an 85 percent reduction in labour costs as the need for operator intervention is minimised.
- **Reduced manufacturing footprint:** Optimised space utilisation by reducing the manufacturing footprint by 80 percent.
- **Comprehensive cost reduction:** Nearly 80 percent total cost reduction compared with industry standards.
- **Higher level of accuracy:** There is precise process control and a consistent manner in which the boule is held during the crystal orientation correction. These steps result in wafer orientation that is up to 500 times more accurate than current standards.

Expanding applications

As the BoulePro gains recognition in the SiC industry and gains ground as the preferred process tool for manufacturing SiC substrates, its applications are expanding. Note that its capability to identify crystalline structures and align them for specific purposes is not limited to SiC. The BoulePro can also serve in the silicon semiconductor space, where there are opportunities for this machine to shape single-crystal silicon at the ingot level, and process other silicon-based parts. One application that's being explored is the pairing of the BoulePro with another machine tool in a fully automated cell to create critical parts for silicon crystal growth.

As other compound semiconductors garner more interest, such as the ultra-wide bandgap material AlN, the BoulePro is cementing its position as the fabrication machine of choice. Like SiC, AlN requires precise machining into wafer-ready pucks with specific orientations. The BoulePro's configuration and expertise in handling hard, brittle, and stressed materials make it ideal for shaping as-grown crystals into ready-to-wafer forms.

An industry standard

The widespread adoption of the BoulePro-200AX by leading SiC producers all over the world is underscoring its status as the premier solution for boule-to-puck conversion. From North America and Europe to emerging markets in Asia, this tool is setting benchmarks for efficiency, repeatability, and cost-effectiveness.

Its unparalleled efficiency is revolutionising traditional processes. The BoulePro streamlines production, reduces cycle times, and cuts operational costs by integrating automation, precision machining, and advanced materials handling. Consistent production of high-quality SiC pucks results, enabling manufacturers to meet stringent standards and customer demands confidently.

Thanks to its ground-breaking repeatability, the BoulePro-200AX ensures uniformity and consistency, essential traits for maintaining product integrity. Offering precise control over key parameters minimises part damage, safeguarding SiC products' reputation and reliability.

The transformative potential of the BoulePro-200AX is well understood by our parent company, Hardinge, which recognises the challenges SiC producers face in post-growth boule fabrication, as well as the need for specialised machining expertise. Current Hardinge CEO Greg Knight understands the struggles of SiC fabrication well as he was formerly the CEO of GTAT, a SiC crystal growth company that was acquired by Onsemi.

As well as meeting their immediate needs, SiC manufacturers that invest in the BoulePro-200AX are positioning themselves for long-term success. Our tool's advanced features and robust performance, coupled to our drive to continue to add innovative features and technologies to this platform, will ensure that it remains a critical component to produce SiC and other upcoming semiconductor materials for years to come.

Putting it succinctly, our BoulePro-200AX is more than just a machine – it's a catalyst for progress in the SiC industry. Offering innovative design, comprehensive capabilities and proven results, this tool is an essential asset for any SiC manufacturer looking to stay competitive in a rapidly changing market. With the BoulePro-200AX, we are not just setting the standard; we are defining the future of SiC fabrication.

Nanowires eye augmented-reality displays

The mass market seeks augmented-reality displays small enough to embed in a pair of sleek, lightweight eyeglass frames

BY SETH COE-SULLIVAN FROM NS NANOTECH

WHEN APPLE shipped its first Vision Pro headsets this February, it joined a battle with Meta and other manufacturers for a share of the emerging global market for virtual reality (VR), augmented reality (AR), and mixed reality (MR) applications. But the Vision Pro's large form factor and its hefty price tag raised as many questions as Apple answered in its presentation on the future of a new age of 'spatial computing'.

Initial reviews noted that, like the popular Meta Quest headsets, the Vision Pro is large, bulky, and generally too heavy for all-day use. And while it offers spectacular immersive video and audio experiences, this comes at a hefty price. Retailing at $3,499, the Vision Pro is four-to-five times as expensive as its competitors.

Unfortunately, all of these rivals, which are capable of demonstrating the exciting possibilities of AR, MR, and VR applications, are held back by several issues. Today they are not small enough, are limited in efficiency, not easy to manufacture, and lack the affordability that would see many consumers make them a constant companion. The mass market wants to go beyond those headsets that resemble oversized ski goggles for immersive VR and MR applications, and move to AR displays that are small enough to embed in a pair of sleek, lightweight eyeglass frames that one can comfortably wear all day.

Delivering AR displays that are this small and efficient is far from easy. It demands advances in a range of technologies, starting first and foremost with a reduction in the size of the display. The bulk required for smart AR features to be added to a normal pair of glasses is determined largely by the display size, which governs the size of the waveguides, battery, mechanical parts, and other optical components necessary to deliver satisfying AR images. Today's displays that are suitable for AR are still far too large to integrate with normal-sized eyeglasses. And because weight is largely determined by the size of the battery required, displays with greater efficiency are needed to ensure smaller power sources. Therefore, today's displays that are based on microOLED and microLED emitters, small as they are, will need to be even smaller and far more efficient.

'Bottom-up' fabrication

One promising approach to realising these much-needed size and efficiency breakthroughs is to turn

to nanowire-based LEDs. It is possible to integrate these submicron-scale emitters into displays that are small enough for a standard pair of eyeglasses (see Figure 1).

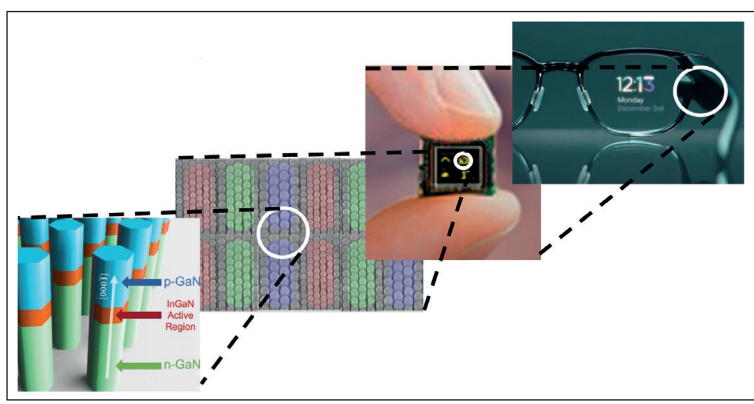
Many of the early developers of this revolutionary technology are growing GaN nanowires on silicon or sapphire substrates with a core-shell architecture featuring a *p*-GaN shell and an *n*-GaN core. It is hard to overstate the potential benefits of these efficient nanowire LEDs. Individual microscopic nanowire LEDs, bundled and working in concert on a standard semiconductor substrate, have the potential to combine an extremely high efficiency at higher brightness with much lower costs and longer lifetimes than today's LEDs and microLEDs. Allied to this, there is the use of simpler fabrication processes, offering the potential to scale-up mass production while minimising defects and delivering higher yields.

However, current nanowire LEDs and microOLEDs have yet to fulfil their promise. They are failing to deliver the brightness and efficiency that's required to meet the demanding requirements of future AR displays. What's more, they do not yet emit red or green light, and they require either filters or a layer of quantum dots to convert the blue emission to the red and green to create colour displays – and this adds to device manufacturing complexity and cost. On top of all these concerns, when the quantum dot down-conversion approach is scaled to a 1 μm pixel size, an efficiency loss results, undermining the advantages of the microLED.

But let's not throw the baby out with the bathwater. It is possible to retain nanowire LEDs, but make them even smaller, by growing nanowires from the bottom up, rather than building them out from the core to the shell. This is the approach we are trailblazing at NS Nanotech that will meet the requirements of AR displays.

Our approach, which draws on the work of Zetian Mi's group at the University of Michigan, has led to the first submicron-scale nanowire LEDs (see Figure 2). It is a technology that enables each nanowire to operate as a complete LED, all the way down to 100 nm in diameter, that can be tuned to emit any desired colour.

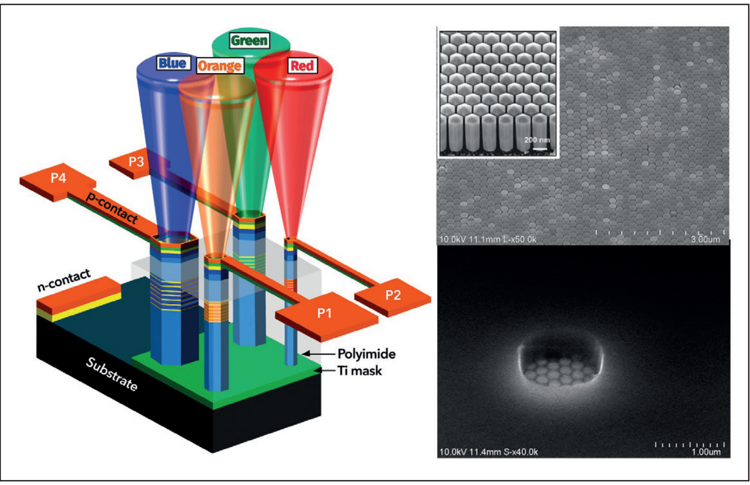
Taking a bottom-up approach represents a marked and welcome departure from traditional LED fabrication. There are downsides associated with planar LEDs, which have to battle against the challenges of materials physics, which begin with full-size LEDs and continue when trimming these emitters down in size to make them mini and eventually micro. Core-shell fabrication circumvents scaling issues through the growth of individual nanowires. However, with this architecture recombination zones are formed on sidewalls, a process that limits efficiency and colour tunability.



➤ Figure 1. A single submicron-scale nanowire can be a complete LED (left). However, in most cases tens to hundreds of nanowires will make up a single sub-pixel of a full colour display (left-centre). LEDs can then be integrated on an red-green-blue display (right-centre) that's small enough to fit unobtrusively into a standard pair of eyeglass frames (right).

The approach that's been developed by Mi avoids all these pitfalls. Device production starts from the bottom up, with a process that creates discrete, independent LED nanocrystals that are grown directly up from the substrate and utilise a layered structure that is very similar to conventional planar LEDs. This approach has enabled laboratory demonstrations of the first efficient submicron-scale red and green nanoLEDs – they deliver world-record internal and external quantum efficiencies.

To transfer these innovations from the lab to the fab, Mi co-founded NS Nanotech, which has exclusive licenses to patents from his work at University of Michigan and McGill University. Our spin-off is currently conducting further research on his novel approach to nanowire growth, while working on fabrication techniques that will provide the reproducibility and scalability required for mass manufacture of nanoscale LEDs.



➤ Figure 2. Multi-colour nanowire LEDs as small as 100 nm are grown on submicron-scale pixels (left); MBE ensures control of the growth and placement of atoms into single nanocrystals on standard substrate materials (right).

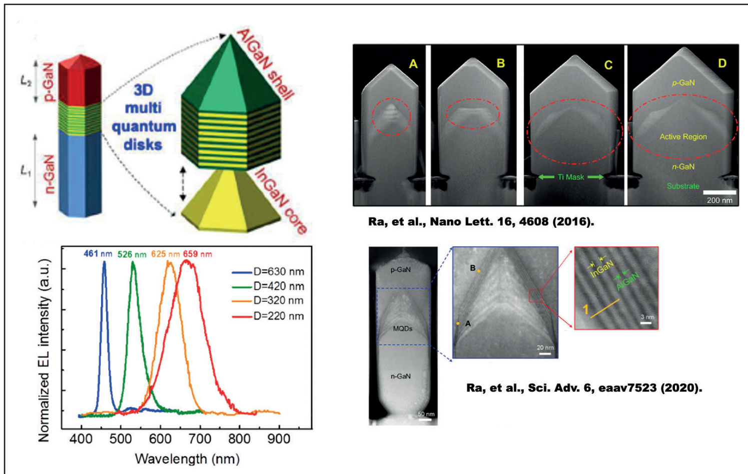


Figure 3. Nanowires grow from the bottom up without an additional process for a separate shell. While growing atomically precise quantum wells, higher bandgap material flows to the outside of each column, protecting quantum wells from the surface states and ultimately resulting in high internal quantum efficiencies (IQEs).

Four key breakthroughs

Our nanowire growth technique is underpinned by four technical breakthroughs in materials science. These breakthroughs leverage three pre-existing foundational technologies: MBE, which enables unparalleled control of the growth and the placement of atoms into single nanocrystals on standard substrate materials; nitride semiconductor technology, which provides the most stable light emitters in existence; and the nanostructures themselves.

The four materials science technology breakthroughs that come from Mi's group and build on those three pre-existing foundational technologies are catalyst-free nanocolumn growth, a disc-in-nanocolumn architecture, the use of a photonic bandgap, and monolithic integration on any substrate. We shall now discuss each in turn.

When growing nano-columns, there is an advantage to avoiding catalysts, which threaten to lead to purity problems and ultimately diminish electroluminescence efficiency. However, there are those that will tolerate this concern, pointing out that when nanowires are anchored to a surface, as opposed to being grown colloidally, it is easier to realise electroluminescence.

Fortunately, though, it's possible to enjoy the best of both worlds, thanks to Mi's development of a new method that is capable of growing high-purity nitride semiconductor material from almost any surface, while realising full doping control that allows for facile creation of LEDs. This ground-breaking technique enables the growth of GaN nanowires with regions of *p*-type and *n*-type doping, defined during epitaxy, along with alloying. Adding indium leads to visible emission, while the incorporation of aluminium ensures ultraviolet electroluminescence. Additional merits of catalyst-free nanocolumn growth are selective-area growth or selective-area epitaxy, realised with positional placement, accuracy, flexibility, and control over the packing density.

The disc-in-a-nanocolumn architectures, which are sometimes referred to as dot-in-a-wire nanostructures, offer a number of benefits. They include the reduction or elimination of crystallinity defects, surface trap states, and non-radiative emission pathways – all of which kill efficiency.

However, while the disc-in-a-nanocolumn architecture works on paper, it is complex to implement. From a perspective of chemistry process flow, there's a lot of sense to growing core-shell nanocrystals in solution, from the inside out. But growing the shell – that's the sheaths on the outside

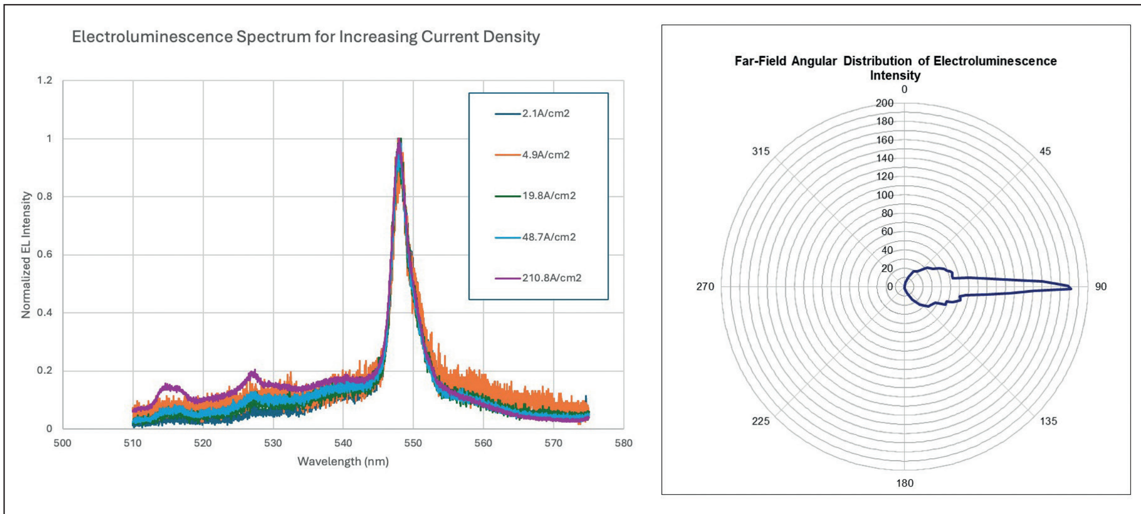


Figure 4. A periodic lattice, which has a pitch that's just a fraction of the wavelength of light that's being emitted, creates a photonic bandgap that overlays the semiconductor bandgap. The upshot is laser-quality spectral purity and directionality.

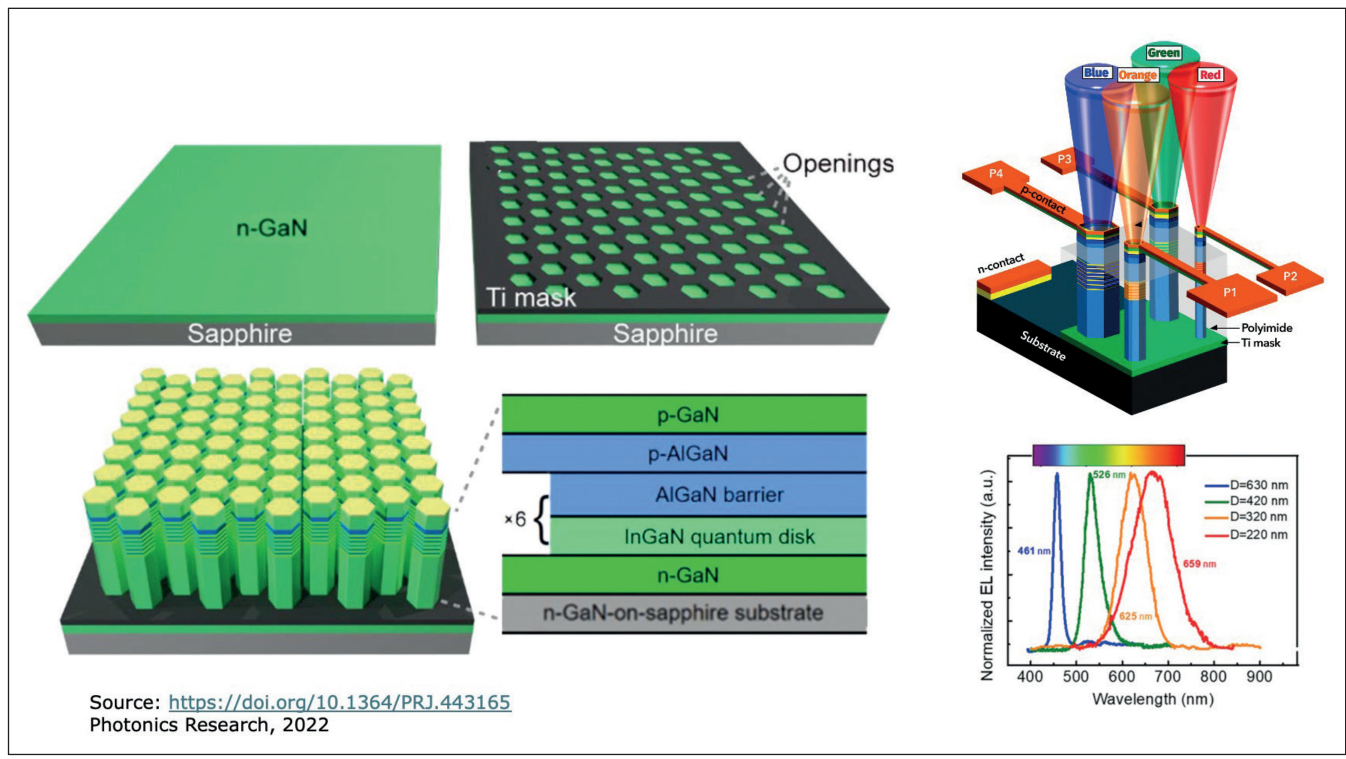


Figure 5. A lithographically defined mask enables growth of nanowires of any shape, size, and colour, in any location on the substrate (left). Adjusting the diameter of the nanowires tunes the emission wavelength and the resulting colour of light (right). Source: Photonics Research, 2022.

of the column – is extremely difficult.

One way to avoid this issue, developed by Mi's group, is to utilise the natural differences in atomic migration along the crystal surfaces. Adopting this approach enables the creation of aluminium-rich regions and indium-poor regions in the crystal, while growing the nanowire from the bottom up without an additional process for a separate shell. During the growth of atomically precise quantum wells, higher bandgap material flows to the outside of each column, protecting the wells from surface states.

The result is material with incredibly high internal quantum efficiencies, especially in the green and red. Efficient emission at these longer wavelengths stems from the use of MBE, which locks these high-indium-content wells away from thermal equilibrium, while the disc-in-a-column architecture lets them emit at high efficiency, unlike conventional nanowire or planar approaches. These innovations eliminate process steps while avoiding some of the problems presented by core-shell architectures (see Figure 3).

The photonic bandgap associated with our nanoscale LED ensures a more stable emission profile over its planar cousins. The instability stems from emission that is only governed by the semiconductor bandgap, a condition that leads to colour drift problems when the doping level isn't perfectly controlled, or when the device heats up.

Our microLEDs avoid this weakness. Our columns are smaller than the wavelength of light, and we place them with sub-nanometre accuracy, using 2D lithography. We design these columns into a periodic lattice with a pitch that's just a fraction of the wavelength of the light being produced, to create a photonic bandgap that overlays the semiconductor bandgap. Running current through the nanocolumns creates electron-hole pairs across the semiconductor bandgap that are ready for spontaneous emission and, when resonant with the photonic cavity, emit far faster and at exactly the same frequency. Photons leap out of this cavity in exactly the same cone, creating very directional

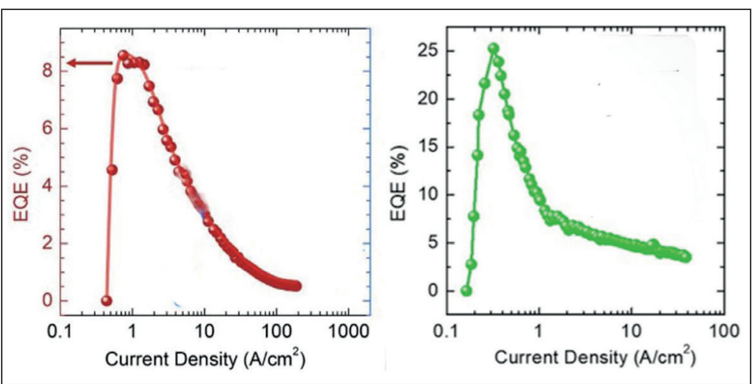


Figure 6. Nanowires grown in the lab create submicron-scale LEDs with external quantum efficiencies of 8 percent in the red and 25 percent in the green. These performance levels equal or exceed standard-size LEDs that are orders of magnitude larger.

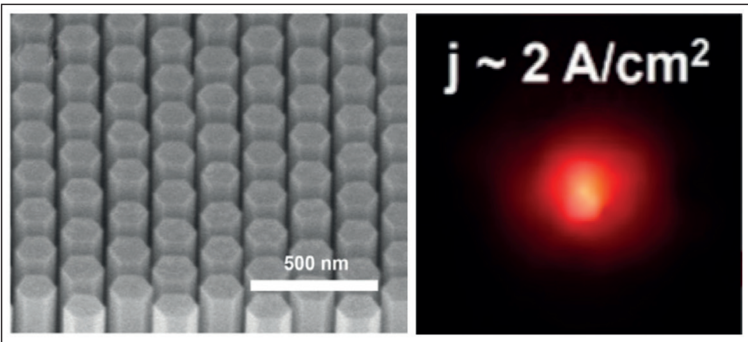


Figure 7. A single nanowire-based red LED is ten times more efficient and a million times smaller than standard red LEDs with comparable efficiency.

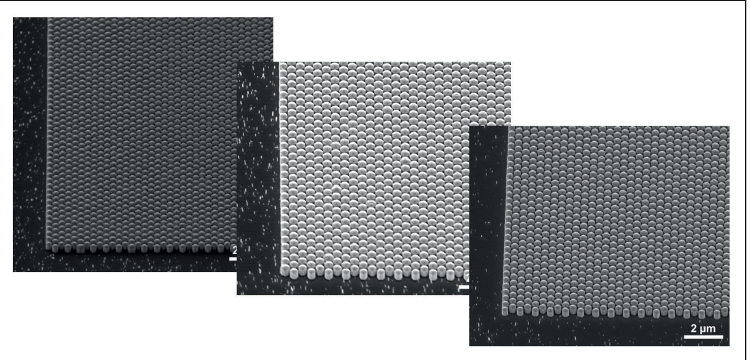


Figure 8. Separate growths of nanowires on non-consecutive days yield indistinguishable results – evidence that the nanowire LED fabrication process is repeatable, and that MBE is stable enough to perform identical processes consistently.

light without any waveguiding. The result is laser-quality directionality from a speckle-free diode (see Figure 4).

Another strength of our approach is that it enables monolithic integration on any substrate. The substrate is not an issue, as nanocolumns can grow defect-free on almost anything. Sapphire is convenient, silicon easier, and it is even possible to grow our nanowires on a metal surface or foil. On all of these foundations and more, we can place the nanocolumns arbitrarily while controlling their shape and size.

What's more, through understanding how the atoms migrate as they deposit, we can use their diameter to control their colour. We have established that wider columns incorporate less indium into their discs than narrow ones, proving another opportunity to control the emission colour in a predictable manner. Through controlled variation in the diameter of the columns, we can create red, green and blue sub-pixels on the same substrate, at the same time, in a single growth step. And by adding yellow pixels, we can grow LEDs in four colours in a single step. We have even shown that it is possible to turn-on single-wire devices of different colours, positioned adjacent to one another and located within a single square micron of area.

Contrary to typical nanowires that are randomly positioned, thanks to selective area epitaxy, we enjoy precise control of nanowire spacing, location, and diameter through lithographic patterning and growth (see Figure 5). Many advantages result from this, including an opportunity to tune the emission wavelength and the resulting colour of light by adjusting the nanowire's diameter. We gain this degree of control by adding a single lithographically defined mask step, inserted after template growth but prior to the growth of the nanowires. It is the selectivity of the mask that allows us to make nanowires where we want them, in the shape, size, and colour of our choosing. This is key to our delivery of the first true sub-micron-scale 'nano LEDs' with the potential to deliver a performance that's superior to today's LEDs, realised at much lower costs and in a small enough form factor to meet the requirements of next-generation AR displays.

Record reds and greens

Due to the nanostructure nature of our nanowire LEDs, high material quality is a given, even for indium-rich layers. And MBE enables growth at low enough temperatures to prevent indium from evaporating from the InGaN surface during growth. Taken together, these advances in materials technology are delivering the performance levels required to make nanowire-based displays commercially attractive.

Strong evidence of this capability is provided by progressive world records for the performance of devices created in the lab. We have measured green nanoLEDs with a 25 percent external quantum efficiency, a performance level on a par with today's planar LEDs that are orders of magnitude larger. For red nanowire LEDs, external quantum efficiency is 8 percent, another world record for sub-micron scale LEDs. This level of performance is well ahead of the pack, with efficiency about ten times higher than the

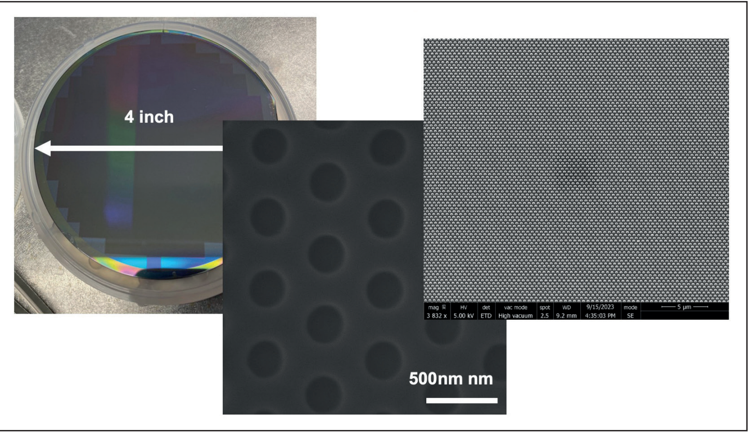
Through controlled variation in the diameter of the columns, we can create red, green and blue sub-pixels on the same substrate, at the same time, in a single growth step. And by adding yellow pixels, we can grow LEDs in four colours in a single step.

next-best red LED of the same size – and around a million times smaller than the next-best red InGaN LED at this efficiency (see Figures 6 and 7).

From lab to fab

Manufacturing nanowire-based LEDs at scale for mass markets requires scalable fabrication processes that ensure uniformity and reproducibility of nanowire growth at the wafer scale. To this end, we are determining process windows for MBE that provide repeatable, uniform results. We are encouraged by our initial efforts, demonstrating the repeatability of nanowire growth (see Figure 8).

Up until now, we have employed electron-beam lithography for the fabrication of all our laboratory-grown nanowire LEDs. However, this technique isn't easily scalable for mass production, so we are looking to introduce standard semiconductor processes. They include optical lithography, which is available and pervasive, but until our recent work has never been used to make a nanowire of this type. We have broken new ground by utilising a standard deep-UV optical lithography process on a 100 mm wafer to create a selective-area epitaxy mask. This approach has produced the first ever uniform growth of submicron-scale GaN nanowires on an optically patterned substrate (see Figure 9).



➤ Figure 9. Standard deep-UV optical lithography on a 100 mm wafer resulted in uniform growth of submicron-scale GaN nanowires.

Spurred on by our progress that has enabled us to meet the size and efficiency requirements of microLED displays, we expect nanowire LEDs to enable massive new markets for many, many years, including AR headsets, but also encompassing many other products. By developing the right hardware, including displays and optics, it will be possible to achieve the holy grail of a compelling AR device that can be worn all day – a product that will change how we all interact with computing, and enable a world where we once again turn our heads back up, rather than huddling over our phones.

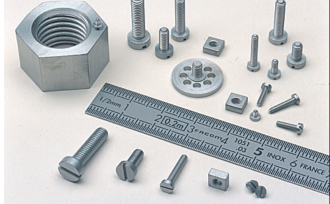
Large stock of Molybdenum and Tantalum

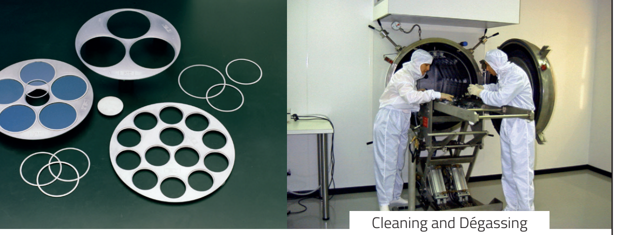
All parts made according to drawings in these materials

MICRO-MECHANICS ON STRATEGIC MATERIALS

- In stock for all vacuum and ultra vacuum applications : Molybdenum and Tantalum screw products (screws, nuts, rings) « Usable in Clean Rooms »
- In stock for laboratory machines : Standard substrate support (Molybloc)
  Dimensions :
  - 1 ½ inches
  - 2 inches
  - 3 inches

  Possibilitiy of substrate support with cavity and washer, on request and according to drawings
- Stock of platens blanks for all types of MBE from various manufacturers.
- « Usable in clean rooms » Platens and washers produced according to drawings.





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Improving the capabilities of RF GaN

Options for building better HEMTs including switching the polarity, introducing InAlN barriers and optimising buffer growth

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AS A MATERIAL for making compound semiconductor devices, GaN is peerless. It is an incredibly efficient light emitter, enabling a revolution in lighting, as well as the production of short-wavelength lasers that can read data off of discs and cut material. In addition, GaN has excellent electronic characteristics that are now being put to good use for improving the efficiency of chargers and power supplies.

With so many lucrative opportunities for GaN, one might overlook those that are not grabbing the headlines, but are still set to generate growing revenues over the coming years.

In that regard stands RF GaN, which is deployed in 4G and 5G base stations, radar and electronic warfare systems. According to market analyst Yole Group, sales of RF GaN devices for these applications are climbing, with total device revenue forecast to increase to $2 billion by 2029.

This market continues to attract investment to improve the performance of the GaN HEMT through changes to its architecture, its foundation and the epitaxial processes employed to produce this device. At this year's CS Mantech, held in Tucson, Arizona, from 20-23 May, spokesmen for makers of devices, epiwafers and MOCVD tools all reported progress on these fronts. At this conference Sumitomo Electric Industries reported record-breaking output powers for N-polar HEMTs in the Ka-band, a partnership between Mitsubishi Electric and Furuno Electric unveiled a very efficient GaN HEMT for marine radar, WIN Semiconductors explained how an optimised buffer improves GaN HEMT linearity, and a European collaboration involving Aixtron discussed the use of depleted interfaces between the substrate and epilayers for minimising RF loss in GaN-on-silicon HEMTs.

Switching polarity

The GaN HEMTs that are winning commercial deployment feature an AlGaN buffer and a Ga-polar design. To improve performance, a number of researchers have considered refining this architecture. A team from the University of California, Santa Barbara, have enjoyed much success by turning to N-polar HEMTs, realising an output power density of 8.84 W mm^{-1} at 94 GHz, at a power-added efficiency of 27 percent. Meanwhile, at team from Fujitsu has delivered a power density of 3 W mm^{-1} at 96 GHz by replacing the conventional barrier with lattice matched InAlN.

At this year's CS Mantech, Shigeki Yoshida from Sumitomo Electric Industries described efforts to combine both these valuable innovations. This team's HEMTs, with an N-polar orientation and an InAlN barrier, are claimed to deliver a record-breaking power density of 12.8 W mm^{-1} at 28 GHz. Yoshida told *Compound Semiconductor* that in comparison, the output power of the company's Ga-polar GaN HEMT product is about 4 W mm^{-1} in the Ka-band.

To produce their transistors, Yoshida and co-workers

began by loading 100 mm semi-insulating SiC substrates into an MOCVD reactor and depositing a buffer layer, followed by an InAlN back barrier, an AlN spacer, a 12 nm-thick GaN channel and a GaN cap. On this epitaxial structure they added a $HfSiO_x$ gate insulator, selected for its high values for permittivity and breakdown field – they are 13 and 8.5 MV cm^{-1}, respectively. To reduce source and drain contact resistance, the engineers introduced heavily doped *n*-type GaN selective growth regions. HEMTs were produced with a 200 nm gate length, a source-drain length of 2.5 µm, a gate-source length of 0.9 µm, and a gate-drain length of 1.4 µm.

On-wafer measurements determined an electron mobility of 928 $cm^2 V^{-1} s^{-1}$ and a surface roughness, according to atomic force microscopy, of 0.304 nm – that's the root-mean-square roughness over a 1 µm by 1 µm area. This value for roughness is lower than that for III-polar GaN HEMTs, suggesting a suppression of electron scattering and a high electron mobility. For the surface of the III-polar GaN HEMTs, pits are seen on the surface that can cause device breakdown and current collapse (see Figure 1). Note that these imperfections are not seen on the surface of the team's N-polar HEMTs.

One of the benefits of the N-polar HEMT over its conventional cousin is that the external electric field resulting from the gate voltage and the internal electric field due to the polarisation of the barrier are in opposite directions, rather than the same direction. This allows N-polar HEMTs to have a higher breakdown voltage, with Yoshida and co-workers estimating a breakdown voltage of more than 60 V, based on electrical measurements.

Additional measurements on this device have determined a maximum drain current density of 2.64 A mm^{-1}, a current gain cut-off frequency (f_t) of 30 GHz, and a maximum oscillation frequency (f_{max}) of 96 GHz.

The saturated output power for the device, 12.8 W mm^{-1} for 28 GHz load-pull power sweeps, is claimed to be the highest value ever reported for N-polar HEMTs in the Ka-band (see Figure 2). The team argues that this output power is limited by impedance tuning.

"We have to design and fabricate pre-matching circuits to improve [impedance tuning]," remarked Yoshida. However, that's not the next plan – it is to develop an AlN buffer to improve heat dissipation.

Marine radar

For GaN HEMTs for radar, the opportunities that are most often discussed are associated with defence and aviation. But there is also the option to deploy these wide bandgap devices on ships, where they can displace vacuum electron devices, such as magnetrons. Merits of GaN over the vacuum-tube-based incumbents include reductions in size and weight, a longer life and a hot-start source. The extension in lifetime is substantial, with magnetrons needing to be replaced every 5,000 hours, while GaN HEMTs have a mean-time-to-failure of over 1,000,000 hours. Another merit of the latter is that it is compatible with Doppler analysis – this ensures safe navigation by enabling the tracking of vessels and floating wreckages.

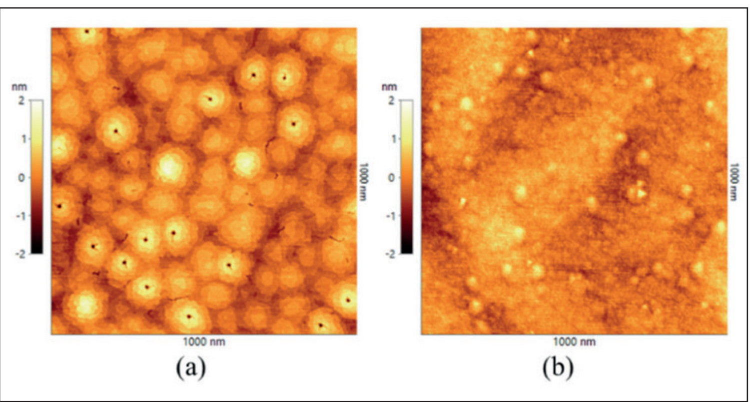


Figure 1. Atomic force microscopy uncovers pits on the surface of III-polar HEMTs that can lead to device breakdown and current collapse (a). These pits are not observed in N-polar HEMTs.

Speaking about this opportunity at this year's CS International, Eiji Yagyu from Mitsubishi Electric described the development of X-band to Ka-band GaN HEMTs with a high power-added efficiency. These transistors can be used to produce a marine radar with a range of 96 nautical miles.

This programme has involved the production of AlGaN/GaN HEMTs on SiC substrates with a gate length of 0.2 µm using what are claimed to be reliable structures and techniques. These HEMTs incorporate an iron-doped buffer layer, their fabrication involves ion-implanted isolation, and they feature a silicon-implanted ohmic contact region, a T-shaped gate and a source-connected field plate. According to the team, although these devices are ordinary HEMTs, to ensure a high power-added efficiency and reliability, they have optimised the fabrication processes, the epitaxial layers, and the electrode layout and design.

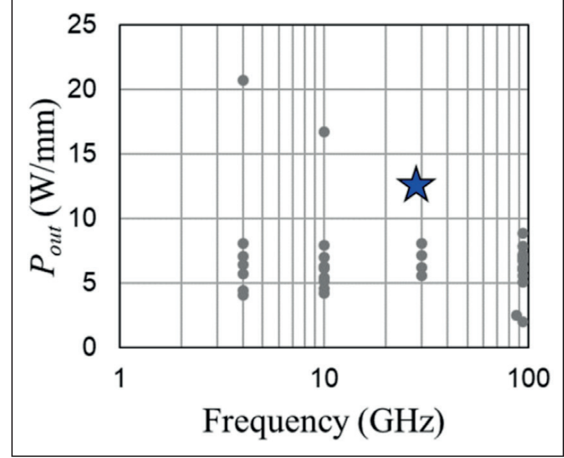


Figure 2. Engineers at Sumitomo Electric Industries have benchmarked their N-polar GaN/InGaN HEMTs (blue star) against N-polar GaN/AlGaN HEMTs.

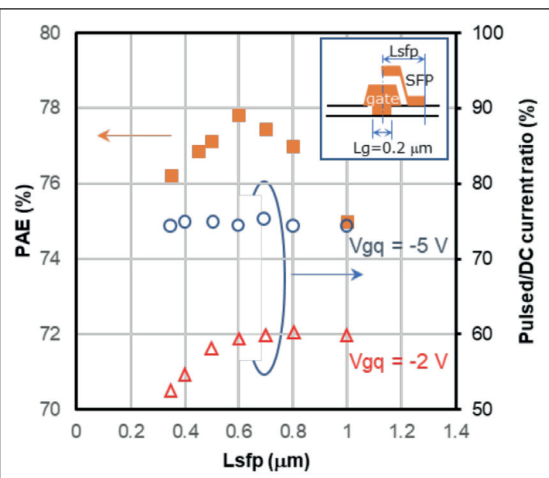


Figure 3. For HEMTs produced by Mitsubishi Electric and Furuno Electric, the length of the source-connected field plate (Lsfp) impacts the power-added efficiency (PAE), and the ratio of pulsed-to-DC current, which provides a measure of current collapse. The PAE is measured at a 9.6 GHz.

Measurements of these HEMTs reveal that there is a sweet spot for the power-added efficiency. Efficiency hits 77.8 percent at 9.6 GHz when the length for the source-connected field plate is 0.6 μm (see Figure 1). The current collapse, evaluated by the ratio of the pulsed-to-DC current, improves with the length of the field plate, but saturates at 0.6 μm. The team also notes that plots of pulsed and DC current reveal that traps working at a semi-on bias play a dominant role in determining efficiency.

Yagyu and co-workers have used their HEMTs to develop MMIC PAs. They have also made an X-band GaN HEMT with a total gate width of 29.6 mm that produces 200 W in the X-band, and they have developed an internally-matched FET PA using GaN die and input/output networks with non-uniform comb lines. The PA produces an RF output power of 240 W at a power-added efficiency of 51 percent. By combining two die, the team have produced a PA with an output power of 467 W and a power-added efficiency of 46 percent.

The solid-state PA produced by the team, delivering 200 W, is said to be equivalent to a 25 kW magnetron, but reduces power consumption from 71 W to 27 W.

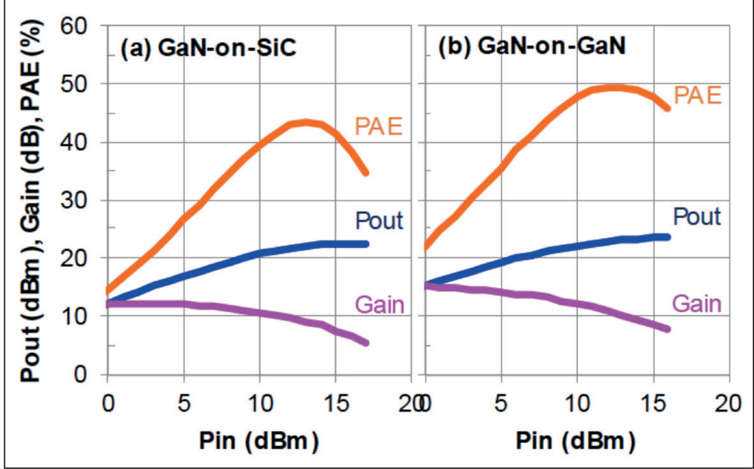


Figure 4. RF power characteristics of GaN-on-SiC HEMTs (a) and GaN-on-GaN HEMTs (b) at 2.4 GHz. The total gate width is 0.2 μm.

The frequency deviation of the solid-state PA is 0.15 MHz, 40 times smaller than that of the magnetron, and phase deviation is lower by more than a factor of 100. The combination of high-frequency stability and a low phase noise makes the radar based on GaN HEMTs far better suited to Doppler analysis.

The team have also started to investigate the potential of GaN-on-GaN HEMTs, which they argue could reduce power consumption and cost. Yagyu told *Compound Semiconductor* that although GaN substrates are currently more expensive than those made from SiC, this could change. "GaN has the possibility of a lower price than SiC, because large GaN ingots could be rapidly grown from the liquid-phase like silicon," argued Yagku, adding that SiC substrates are grown from the vapour phase.

Investigations on the use of GaN have begun by comparing the density of threading dislocations on GaN-on-SiC and GaN-on-GaN by counting etch pits. For GaN-on-GaN, this approach gave a figure of 3×10^6 counts cm^{-3}, more than 200 times lower than that for GaN-on-SiC. This led the team to reason that growth on native GaN will reduce the trapping of electrons and current collapse, and improve the power and linearity of amplification.

These engineers have produced two-finger HEMTs with a gate length of 1 μm on 15 mm by 15 mm substrates of GaN and SiC, and compared the performance of these two types of device. Using the ratio of pulsed-to-DC current to evaluate current collapse, the team observed steep degradation for transistors grown on SiC, and no significant degradation for those with a native foundation. To evaluate linearity, Yagku and co-workers considered third-order intermodulation distortion, using a centre frequency of 2.4 GHz and a spacing frequency of 2 MHz. This investigation confirmed a smaller distortion for HEMTs grown on GaN than those on SiC. The output power is also higher for HEMTs on a native substrate (see Figure 4).

Plans for Yagku and co-workers include investigating the best design of GaN-on-GaN, and demonstrating this choice of materials in other microwave applications. "As GaN-on-GaN has less-distortion in modulated signals than GaN-on-SiC, I will demonstrate this superiority in applications," remarked Yagku.

Suppressing memory effects

One of the downsides of the GaN HEMT is a memory effect that is induced by a drift in the bias current – that's the current flowing in the drain when there is DC bias and RF signal applied to the input. The memory effect degrades device performance, causing variations in gain and signal distortion. Due to this, when GaN HEMTs are used in mobile communication infrastructure, there's a need for a digital predistortion model that compensates for the memory effect. The addition of this model increases computational complexity.

To suppress this memory effect, Wayne Lin and colleagues at WIN Semiconductors have optimised buffer growth, replacing an iron-doped buffer with one that's produced with an undisclosed process, which is starting to be used in products shipped to customers.

At CS Mantech Lin presented proof of the superiority of the new process by comparing the performance of HEMTs formed on SiC that are produced using this approach with those made in a conventional way. To produce the control, the engineers at WIN grew an iron-doped GaN buffer on SiC by MOCVD, followed by a GaN channel, an AlGaN barrier and a GaN cap. The alternative has an optimised buffer. The only other difference from the control is an AlN spacer layer, inserted between the GaN channel and AlGaN barrier.

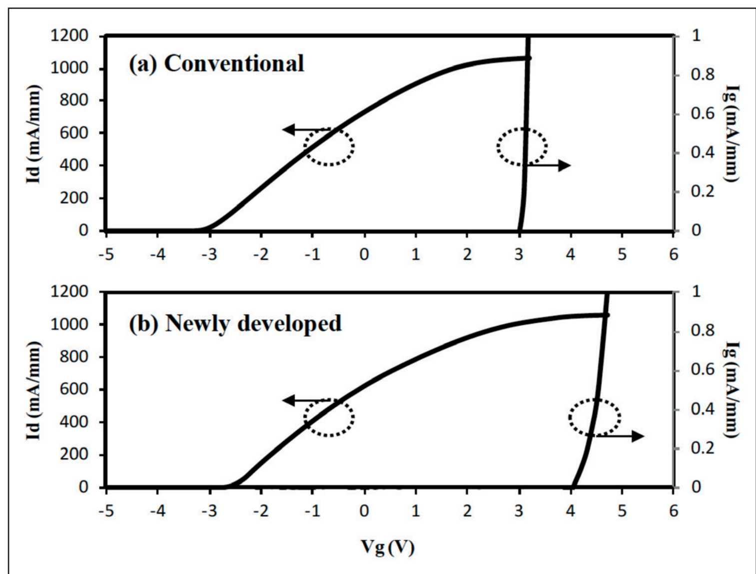
The purpose of the AlN spacer is to increase the concentration of the two-dimensional electron gas. Lin told *Compound Semiconductor* that this spacer does not improve the linearity of the HEMT. When asked if the spacer has any downsides, Lin remarked: "So far, so good." He added that WIN will collect statistical data to check if the new buffer has any drawbacks.

Fabrication of WIN's HEMTs involved defining the ohmic metal by optical lithography, followed by electron-beam evaporation of Ti/Al/Ni/Au stacks. Annealing formed the ohmic contact, before the addition of a first SiN passivation layer. After etching a gate opening, the team added a Schottky gate by evaporating Ni/Pd/Au, before depositing a second SiN layer that sits between the gate metal and a source-coupled field plate. To complete the fabrication process, the engineers added a SiN layer to protect the surface, and introduced two metal interconnection layers to enhance the HEMT's current-handling capability.

Plotting the drain current as a function of gate voltage revealed an increase in turn-on voltage for HEMTs produced with the new process (see Figure 5). This increase, which expands the dynamic range of the device, is attributed to the AlN spacer layer.

To investigate large signal performance, Lin and co-workers undertook 3.5 GHz pulsed load-pull measurements on a 10 x 125 mm device, using a drain current for what is described as deep class AB operation, and a drain voltage of 50 V, suitable for base station applications. The output power density for the design with the new buffer exceeds that of the control, delivering more than 12 W mm^{-1} (see Figure 6).

Insights into the drift in the bias current have come from measuring the transient waveform of this current in a pulsed load-pull system with a current probe. These measurements, using 36 µs pulsed RF signal excitation, reveal strong current collapse in the HEMT with the iron-doped buffer. In comparison, the HEMT with the new buffer technology has a 60 percent reduction in bias current drift and a quick recovery time.



➤ Figure 5. Transfer characteristics of HEMTs made by WIN Semiconductor reveal that the introduction of a new process has increased the dynamic range of this device.

To evaluate intermodulation distortion of RF PAs, the engineers at WIN have determined the ratio of the main channel power to that of adjacent channels. These measurements show a generally better performance for the newly developed HEMT, indicating superior linearity.

WIN has started to offer its new process to selected customers. A full release is planned during the last quarter of this year.

Minimising RF loss

For RF applications, growing the device on a silicon substrate has much appeal in terms of cost. However, SiC is easier to work with, as it offers smaller differences in lattice constant and thermal expansion coefficient with the epilayers, as well as a lower electrical conductivity. The latter strength, stemming from the wider bandgap, is a significant asset, as a lower conductivity cuts RF loss, which degrades the quality factor of passive components, the efficiency of the PA, and the linearity of switches.

To improve the capability of GaN-on-silicon devices for 5G and 6G applications, a partnership between Aixtron, imec, KU Leuven and the Free University of Brussels has investigated the role of the thermal budget on the growth of GaN layers on silicon substrates. Epitaxial process parameters can influence the conductivity of the silicon substrate, due to the diffusion of aluminium and gallium into the substrate and changes to the interface between the AlN nucleation layer and the silicon substrate. According to Aixtron's Herwig Hahn, who spoke on

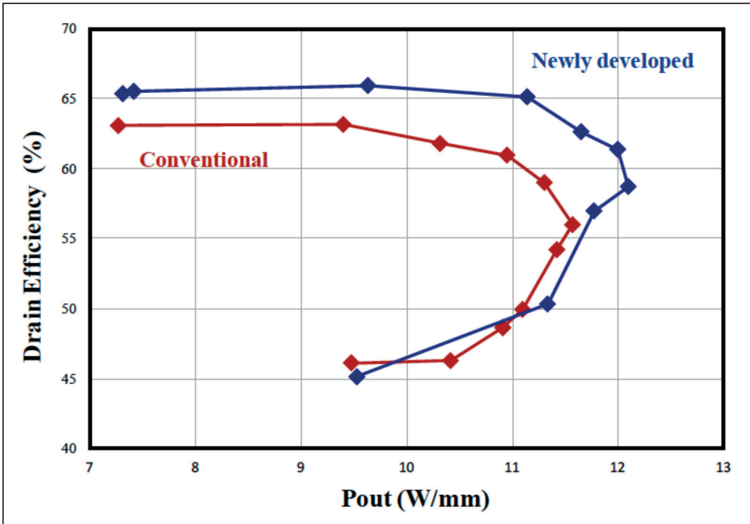


Figure 6. WIN Semiconductor's newly developed HEMT has a higher output power than its conventional equivalent, according to 3.6 GHz pulsed load-pull measurements. Each data point represents an output power (Pout) at 3 dB compression and a drain efficiency at a different output impedance.

behalf of the partnership at CS Mantech, the key finding of their investigation is that combining the leading MOCVD tool with state-of-the-art process know-how enables the use of GaN-on-silicon in applications where minimal RF loss is required.

The collaboration is convinced that a gallium/aluminium-free reactor is mandatory for minimising RF losses.

"An *in-situ* clean is key to enabling this," said Hahn. "We recommend using either a G5+ C or G10-GaN to obtain minimal RF losses."

Experiments involved *in-situ* cleaning with chlorine gas, followed by epitaxial growth on monocrystalline high-resistivity silicon that has been grown by the Czochralski method. On these substrates, which were prepared for growth by an oxide removal step under hydrogen gas at 1050°C, the team undertook an aluminium pre-dose step at between 700°C and 800°C, followed by growth of AlN between 1000°C and 1050°C. In some cases they then deposited a range of epitaxial stacks.

During these studies, the team found that a low thermal budget could not guarantee the high resistivity that's desired. Values can be as low as 800 Ω cm, which is well below substrate resistivity.

Increasing the pre-dose temperature from 700°C to 800°C produced a pronounced increase in resistivity. According to energy dispersive X-ray spectroscopy, a higher resistivity is associated the formation of a very thin SiN layer, and a SiC layer that occupies a significant part of the interfacial layer. Samplers with a lower resistivity just have a SiN layer at the interface.

Hahn and co-workers argue that predose optimisation of AlN-on-silicon slightly differs from that of a full GaN HEMT stack on silicon, and even a fully processed RF device. The researchers recommend full device processing and RF characterisation when optimising growth conditions.

The team have also considered co-planar waveguides in their study, obtaining resistivities above 10 kΩ cm with an optimised process, exceeding the value of 3.8 kΩ cm for a GaN-on-SiC reference sample.

According to these researchers, applying the optimised process to a full buffer stack will reduce resistivity, compared with that realised with a co-planar waveguide. However, they are confident that optimised epitaxial growth conditions will allow GaN-on-silicon HEMTs to enjoy a performance parity with their GaN-on-SiC cousins.

Hahn said that working with imec, those at Aixtron are continuing to optimise full GaN RF layer stacks, not only for 5G, but also for future-generation 6G applications. Such efforts will help to secure the future of GaN RF devices, throughout this decade and beyond.

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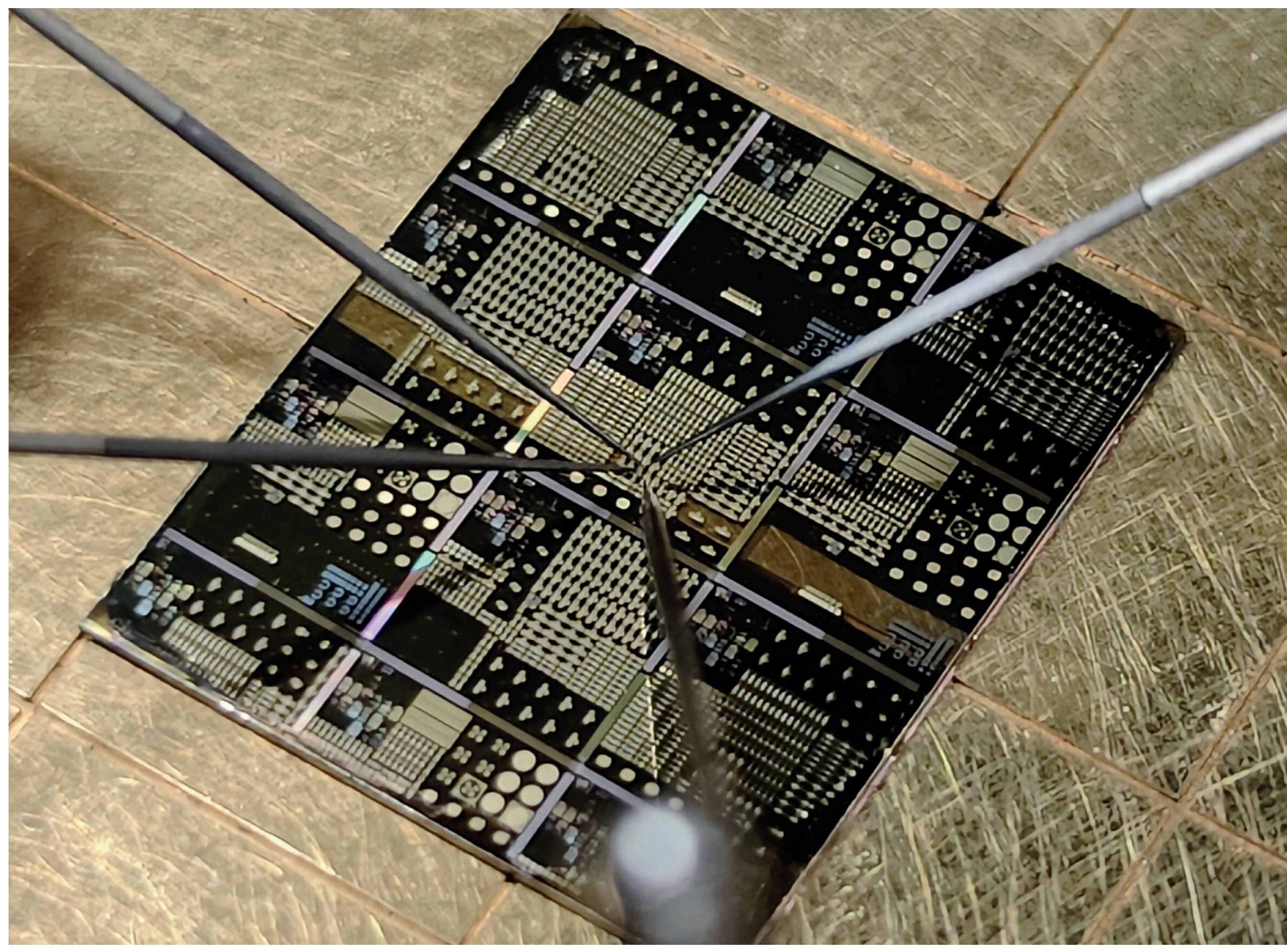


FETs: A mighty marriage

A monolithic architecture combines the complementary merits of GaN lateral heterojunctions and SiC vertical power devices

BY SIRUI FENG, ZHEYANG ZHENG AND KEVIN J CHEN FROM THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

THE REVOLUTION in power electronics is well underway. Following decades of research and development, sales of SiC and GaN devices are now soaring, and will continue to climb for many years to come. Their commercialisation is creating a pair of multi-billion-dollar markets: GaN is now extensively deployed in consumer electronics, such as fast and compact chargers for the latest smartphones and laptops; and SiC is grabbing significant market share in photovoltaic inverters, as well as motor drives for electric vehicles.

Further development of GaN and SiC power electronics technologies will inevitably lead to intense competition between these two classes of device. It's a battle that will be fought most fiercely in power range that spans 1 kW to 100 kW, due to the overlap of the power handling capabilities of GaN and SiC. While both are improving, due to efforts to increase the capability of the GaN and the SiC power transistor, is it possible that their marriage could deliver an even greater performance?

Friends or foes?

To answer this crucial question, let's begin by taking a comparative look at the prevailing structures

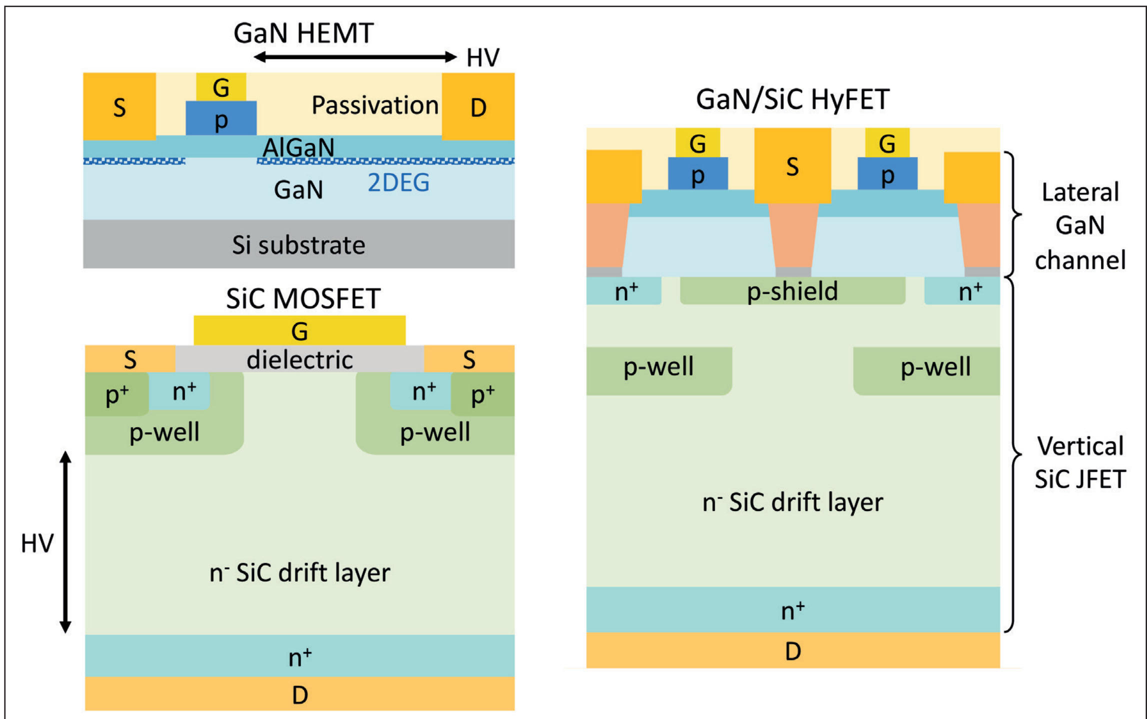


Figure 1. The device structures of the GaN HEMT, SiC MOSFET, and GaN/SiC HyFET.

of the dominant GaN and SiC power devices, as summarised in Table 1. For this evaluation, it makes sense to consider the most popular GaN and SiC power devices, namely the GaN HEMT and the SiC power MOSFET (see Figure 1).

The GaN HEMT is a lateral device with small terminal capacitances. It is renowned for its high mobility, typically 2000 $cm^2 V^{-1} s^{-1}$, associated with the polarisation-induced two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface. The small capacitance and high mobility ensure that this device is very fast. To provide enhancement-mode operation to satisfy the fail-safe requirement, a non-negotiable in power electronics applications, this class of HEMT incorporates a *p*-type GaN gate. As well as enjoying volume adoption in compact fast chargers, this design is under intensive development for industrial and automotive applications.

In contrast to the GaN HEMT, the SiC MOSFET has a vertical geometry, leading to a relatively large conduction volume. It is possible to manufacture a variety of *p-n* junctions under the MOS channel using mature and robust ion-implantation and epitaxy techniques. These processes produce devices with a high blocking voltage and avalanche capability, traits that have garnered widespread deployment in high-power applications, such as electric vehicles and photovoltaic inverters. However, while the GaN HEMT and the SiC

	Pros	Cons
GaN HEMT	High channel mobility (~2,000 $cm^2 V^{-1} s^{-1}$)) Excellent thermal stability in V_{TH}	Low area efficiency Small conduction volume Dynamic R_{ON} No avalanche
SiC MOSFET	High area efficiency Large conduction volume No dynamic R_{ON} Avalanche capability	Low channel mobility (20~50 $cm^2 V^{-1} s^{-1}$) Poor thermal stability in V_{TH}
GaN/SiC HyFET	High channel mobility (~2,000 $cm^2/(V \cdot s)$) Excellent thermal stability in V_{TH} High area efficiency Large conduction volume No dynamic R_{ON} Avalanche capability	High fabrication complexity

Table 1. Comparison between GaN HEMT, SiC MOSFET and GaN/SiC HyFET.

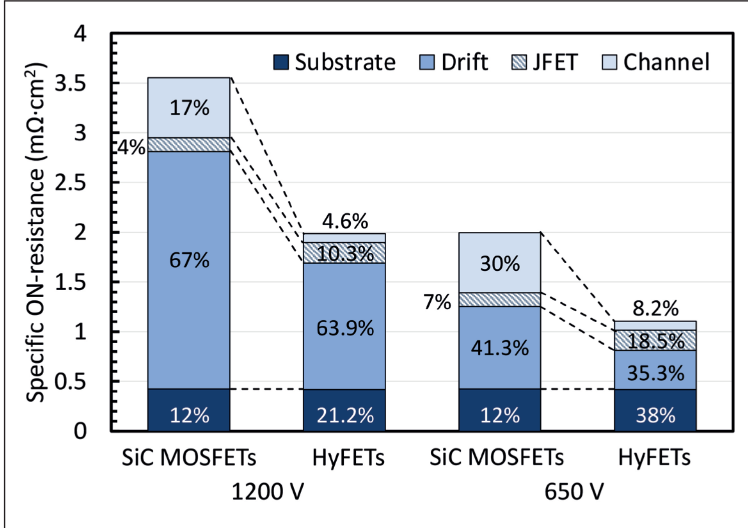


Figure 2. Projections of the contributions from the major resistances of state-of-the-art SiC MOSFETs and GaN/SiC HyFETs.

MOSFET have had unquestionable market success, this should not obscure their issues. For both devices, the full potential is still to be unleashed.

One of the significant weaknesses of the lateral GaN HEMT is that scaling of the voltage rating compromises the bang-per-buck, due to an increased terminal spacing that occupies a larger area. Another issue is that this class of transistor has a small conduction volume, with the 2DEG channel just a few nanometres thick. The small conduction volume impedes the current handling and the thermal dissipation capacity compared with a vertical structure. In addition, there is the notorious 'dynamic on-resistance' issue, induced by the trap-rich surface and buffer, that involves an unwanted increase in the on-resistance with drain bias during the switching process. The other major weakness, arising from the lack of *p*-*n* junctions in the high-field region, is an absence of avalanche capability, with HEMTs potentially undergoing permanent degradation or failure following risky events, such as unclamped inductive switching and short-circuit events. To prevent this from happening, engineers increase the headroom for the breakdown voltage, adding to the bill of materials.

For SiC MOSFETs, by far their biggest weakness is the low mobility in the MOS channel. Values are typically below 20 $cm^2 V^{-1} s^{-1}$ in planar channels and less than 35 $cm^2 V^{-1} s^{-1}$ in trench channels – in both cases, mobility falls far short of that for electrons in the SiC bulk drift region, where it is typically between 800 $cm^2 V^{-1} s^{-1}$ and 1,000 $cm^2 V^{-1} s^{-1}$. In the channel, mobility is pegged back by the high-density of carbon-cluster traps at the interface of the gate oxide and SiC. The low mobility is responsible for the large channel resistance, which accounts for close to 50 percent of the total on-resistance of a 650 V device, and makes a significant and unwanted contribution to the specific on-resistance of devices – especially those with 650 V and 1200 V ratings.

However, rather than dwelling on the negatives, one should view the GaN HEMT and the SiC MOSFET as offering complementary merits. Incorporating them together to create a heterogeneous wide bandgap power device promises to provide a compelling solution that circumvents the issues just outlined.

Initial proposal

Back in 2016, our team at The Hong Kong University of Science and Technology (HKUST) first proposed the concept of the GaN/SiC hybrid FET, based on our numerical simulations. This device consists of a GaN-heterostructure-based 2DEG channel, a SiC JFET structure, a lightly doped SiC drift layer, and through-GaN-vias that connects the GaN channel and the SiC JFET (see Figure 1(c)). This design offers E-mode operation of the 2DEG channel by incorporating a recessed gate or a *p*-GaN gate.

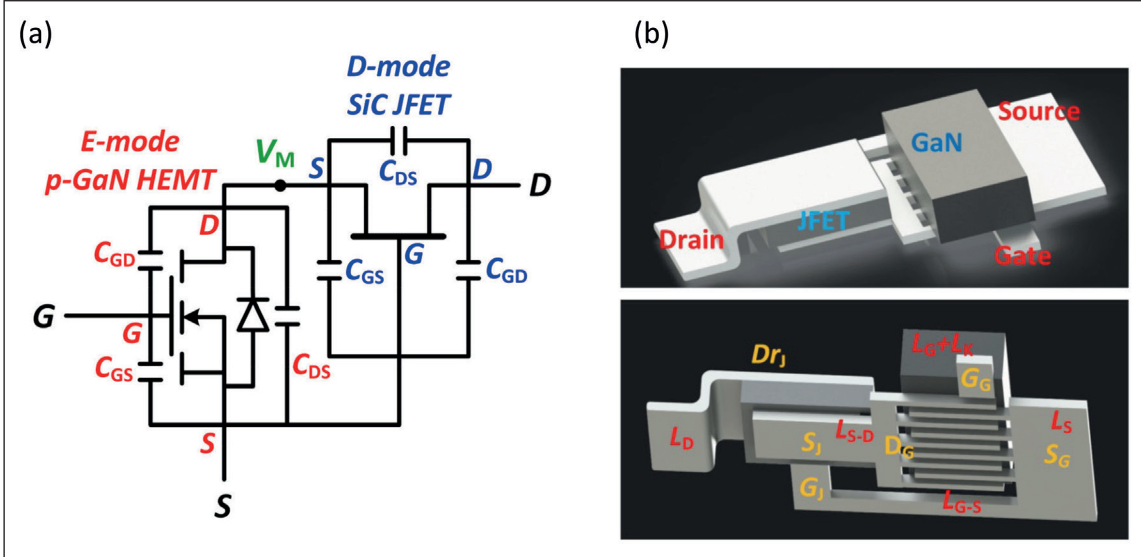
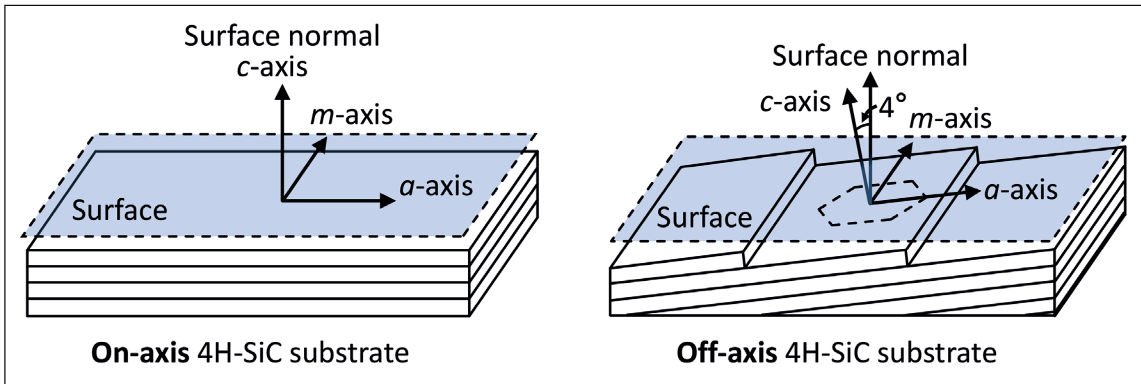


Figure 3. A GaN/SiC cascode device. (a) Circuit diagram. (b) Co-packaged GaN/SiC cascode device with reduced parasitic inductance.



➤ Figure 4. Lattice direction of the 4H-SiC substrates for epitaxy. On-axis substrates are used for GaN heteroepitaxy, while off-axis substrates are used for SiC homoepitaxy.

When this device, which we refer to as a HyFET, is in its on-state, current flows through the *n*-SiC region in the JFET, the through-GaN-vias, and the GaN 2DEG channel. In the off-state, the high electric field from the drain is effectively blocked by the *p-n* junctions in the JFET structure, a state-of-affairs that ensures excellent protection for the high-mobility GaN 2DEG channel. Thanks to the *p-n* junctions in SiC, our HyFET should offer the same avalanche capability as the SiC power MOSFET.

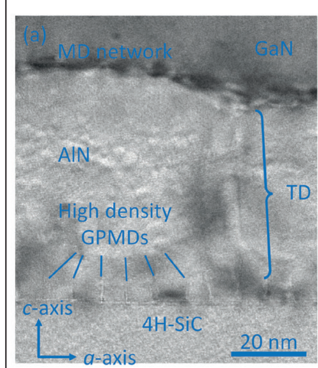
For both SiC MOSFETs and GaN/SiC HyFETs, the total specific on-resistance and its primary components (see Figure 2) has been estimated. The HyFETs offer a substantial reduction in channel resistance compared with SiC MOSFETs, thanks to far high mobility in the channel. Of even greater significance, though, is that due to an absence of the MOS channel, the HyFET is free from a problematic gate oxide, which is behind reliability concerns that have led to overdesigns in the drift region and a derating of the blocking voltage. Based on these considerations, we can reduce the drift region of the HyFET and realise a lower drift resistance.

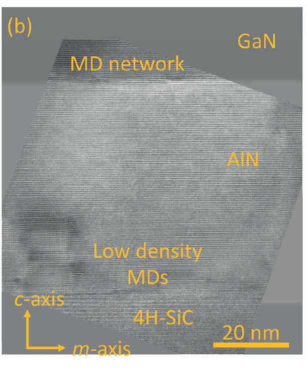
To provide an initial demonstration of the benefits of a heterogenous wide bandgap power device, we co-packaged a discrete low-voltage GaN HEMT and a discrete high-voltage SiC JFET using a cascode topology (see Figure 3). The challenge with this particular configuration is supressing parasitic inductance, occurring in the relatively long interconnects between discrete devices. This inductance is highly detrimental, leading to serious oscillation and additional loss in the switching process. The solution is to move to a more compact co-packaging scheme that trims parasitic inductance.

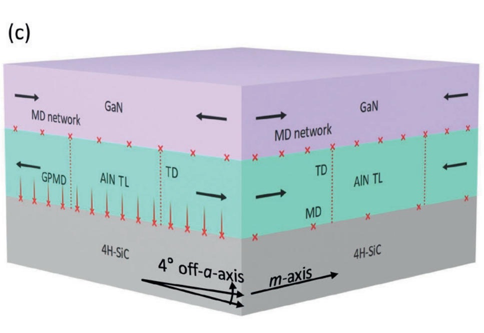
An attractive architecture that fulfils this requirement is the monolithic GaN/SiC HyFET – it has the high-mobility GaN channel and SiC JFET integrated on the sample chip. Such a design delivers incredibly low parasitics and cost competitiveness.

Material challenge

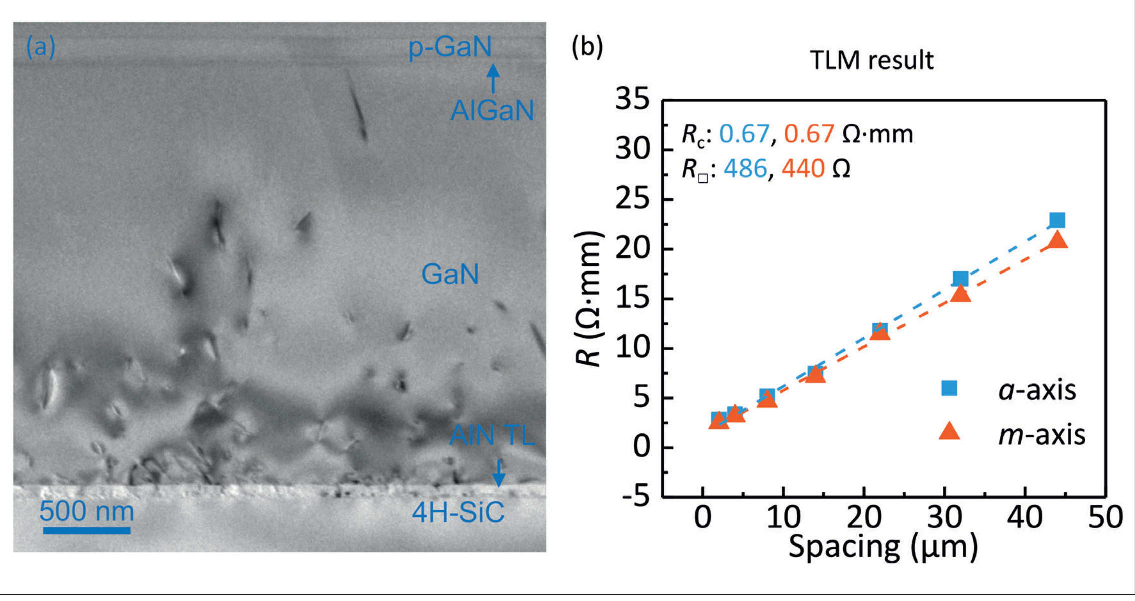
Unfortunately, it's not easy to fabricate monolithic GaN/SiC HyFETs. The biggest challenge is to grow a GaN HEMT structure on a SiC JFET. GaN-on-SiC epitaxy typically uses a 4H-SiC {0001} substrate, with the *c*-axis perpendicular to the wafer surface. However, the mainstream substrate used for the SiC JFET is a 4H-SiC wafer that is mis-cut off-axis, with the *c*-axis at an angle of 4° to the normal (see Figure 4). These mis-cut substrates have the crucial advantage of providing an atomically stepped surface that facilitates a mode of epitaxy that's referred to as step-flow growth.







➤ Figure 5. (a) *m*-plane and (b) *a*-plane view cross-sectional transmission electron microscopy near the AlN transition layer. The geometrical partial misfit dislocations (GPMDs) and misfit dislocations (MDs) at the AlN/SiC and the GaN/AlN interface are observed clearly. The empty parts of the transmission electron microscopy image have been filled with fake colour. (c) Schematics of two-step biaxial strain relaxation in the GaN/AlN transition layer (TL). The arrows show the strain induced by AlN/SiC and GaN/AlN interfaces.



➤ Figure 6. (a) Transmission electron microscopy image of the group III-nitride epilayers on off-axis SiC. Most of the threading dislocations (TDs) are annihilated at the lower part of the epilayer. (b) The transfer length method measurements results of the *a*-axis and *m*-axis GaN 2DEG channel with *p*-GaN removed. The difference in sheet resistance along *a*-axis and *m*-axis is around 10 percent.

However, while these mis-cut substrates are ideal for the single crystalline homoepitaxy of 4H-SiC, they are not well-suited to growth on overlying III-nitride layers, due to a difference in polytype. This difference is to blame for the generation of a high density of geometrical partial misfit dislocations at the III-nitride/SiC interface that tensely strain the epi along the *a*-axis. Strong anisotropic stress in the epilayer results, inducing cracks and defects, and facilitating the formation of step bunches. Concerning consequences follow, including increases in surface roughness and 2DEG sheet resistance, and severe inhomogeneity in 2DEG mobility.

The key to accommodating the anisotropic strain in the III-nitride epilayer is to simultaneously release the strain along the *a*- and *m*-axes during growth. We have devised a two-step biaxial strain release method to accomplish this task. Success comes from inserting an AlN transition layer between the GaN epistructure and the SiC substrate that separately releases the strain along the *m*- and *a*-axes at the GaN/AlN and AlN/SiC interfaces, respectively, by misfit dislocations and geometrical partial misfit dislocations (see Figure 5).

Intriguingly, in this scheme, the density of geometrical partial misfit dislocations is determined by the atomic step density, and ultimately the miscut angle at the 4H-SiC surface, while the density of misfit dislocations is predominantly governed by the lattice constant mismatch between AlN and GaN. With our novel approach, it is crucial to create sufficient misfit dislocations at the GaN/AlN interface to compromise the anisotropic strain caused by the geometrical partial misfit dislocations. However, the step-flow growth mode suppresses the formation of misfit dislocations, since the steps advance together during growth, unlike the island coalescence growth mode, where domain boundaries facilitate the formation of dislocations.

It's important to note that threading dislocations in the AlN layer are crucial for facilitating the creation of the misfit dislocation network when they terminate at the GaN/AlN interface. By adopting an AlN transition layer with an appropriate thickness that enables the threading dislocation density to be well controlled, we have been able to successfully prepare a high-quality GaN epilayer with a relatively low threading dislocation density and an isotropic electric conductivity. These beneficial characteristics are seen in transmission electron microscopy and transfer length method measurements (see Figure 6).

Monolithic HyFETs

Progress by our group, which has involved solving a variety of problems over the 8 years since we proposed the GaN/SiC HyFET, has culminated in the experimental demonstration of this novel device. During this campaign, we have collaborated with Enkris Semiconductor Inc., who prepared group III-nitride epitaxy on off-axis SiC substrates. The

It's important to note that threading dislocations in the AlN layer are crucial for facilitating the creation of the misfit dislocation network when they terminate at the GaN/AlN interface

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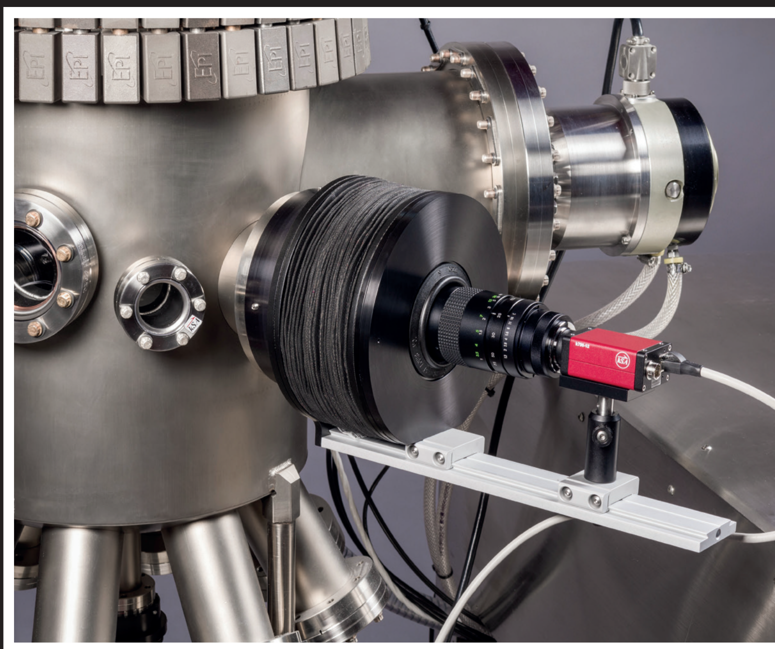

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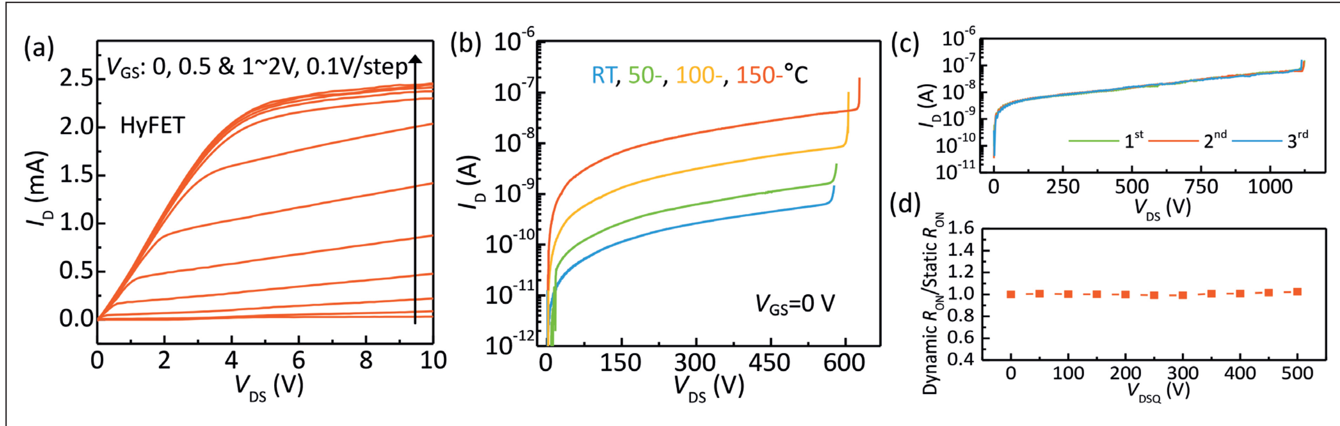

Figure 7. Characteristics of GaN/SiC HyFET. (a) Output current-voltage (I-V). (b) Temperature-dependent off-state breakdown. (c) Off-state breakdown with optimised edge termination. (d) Dynamic R_{ON}. The HyFET exhibits avalanche breakdown capability and has no dynamic R_{ON}.

remaining fabrication processes were developed in the Nanosystem Fabrication Facility and the Materials Characterization and Preparation Facility at HKUST.

In order to establish a low-resistance interconnect between the GaN channel and the SiC JFET, we developed etching techniques to form through-GaN-vias in the GaN epilayer, realised without causing any damage to the SiC JFET.

Another challenge we have addressed is controlling the thermal budget. This is needed, because the GaN surface tends to degrade during SiC metallisation. Our solution has been to develop a GaON surface reinforcement protection layer at the *p*-GaN surface that provides protection during the 900°C sintering process. Following metallisation, we use a Damascene process to create an in-cell interconnect between the SiC JFET and the GaN channel. The remaining processes involve the standard procedure for forming a *p*-GaN gate HEMT.

Our GaN/SiC HyFET is capable of avalanche breakdown, evidenced by the positive temperature coefficient of the breakdown voltage. By optimising the floating-field-limiting-rings edge termination, we have achieved a soft breakdown of 1.1 kV. Another noteworthy attribute of our HyFET is that it is free from the dynamic on-resistance issue, due to distribution of the high voltage across the SiC drift region and shielding of the GaN channel (see Figure 7).

While these results are encouraging, there is still work to do. The specific on-resistance of our HyFET is around 50 mΩ cm², a relatively high value. In comparison, specific on-resistances for state-of-the-art SiC MOSFETs with 1.2 kV and 650 V voltage ratings are typically 3 mΩ cm² and 2 mΩ cm², respectively. We attribute this high specific on-resistance to the conservative design of our JFET, which has a large pitch size to ensure the success of this proof-of-concept in our university facility.

We anticipate a significant reduction in specific on-resistance with industry processing capability, as state-of-the-art SiC JFETs with 1.2 kV and 650 V voltage ratings have values of 1.35 mΩ cm² and 0.75 mΩ cm², respectively. Thus, we see no additional obstacles to achieving a specific on-resistance below that of the SiC MOSFET, as the channel resistance of the HyFET is far lower.

The successful demonstration of the GaN/SiC HyFET, unveiled late last year at the International Electron Devices Meeting, requires expertise in both GaN and SiC. This capability, once quite rare, is now becoming far more common. It is present in some emerging wide bandgap foundries and major power semiconductor companies.

While there is still much more research and development required to realise the optimum performance in the HyFET, monolithic integration techniques described here are helping to pave the way towards the integration of GaN and SiC at an unprecedented level and will provide the impetus to propel the proliferation of heterogeneous wide bandgap semiconductor devices.

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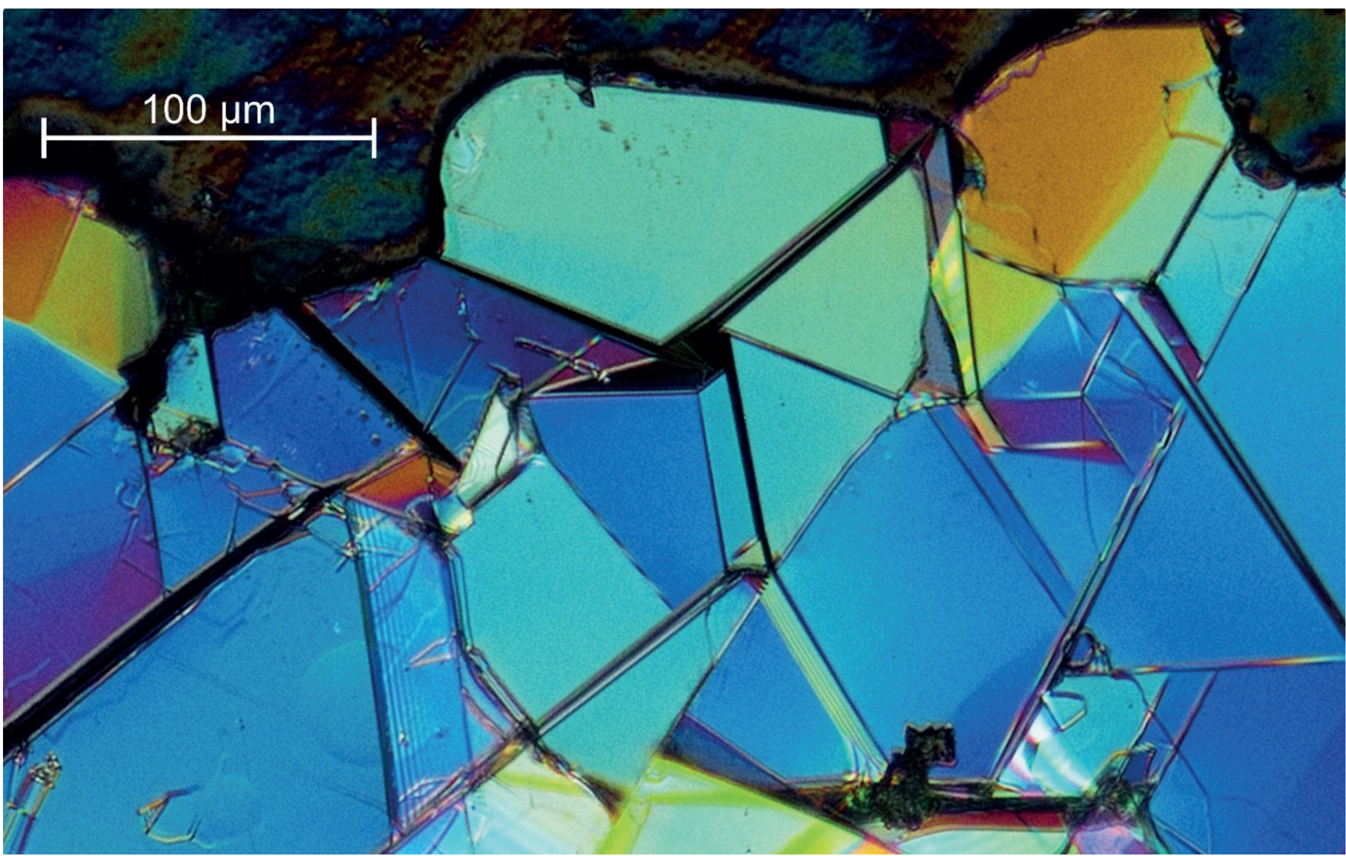


Producing high-quality hexagonal BN

The growth of high-quality hexagonal BN benefits from a sweet spot for nitrogen pressure that's well beyond one atmosphere but far lower than that used to produce diamond

BOHDAN SADOVYI, PETRO SADOVYI, SYLWESTER POROWSKI AND IZABELLA GRZEGORY FROM THE INSTITUTE OF HIGH PRESSURE PHYSICS POLISH ACADEMY OF SCIENCES, AND ANDRII NIKOLENKO FROM THE INSTITUTE OF SEMICONDUCTOR PHYSICS NATIONAL ACADEMY OF SCIENCES OF UKRAINE

SINCE THE LATE 1990s, nitrides have grown in stature within the compound semiconductor community. They shot to prominence as the foundation for efficient LEDs that are now lighting our homes, offices and communities. That's not the end of story, though, but rather the beginning. As well as a revolutionary light source, in the form of both the LED and the laser, nitride devices are playing an ever-increasing role in the power electronics and RF industries.

During the decades that have witnessed an increasing uptake of nitride devices, a miniaturisation of all semiconductor technologies has proceeded, in some cases down to the atomic scale. The discoveries of graphene, topological insulators and other novel materials have opened a whole new area, namely two-dimensional electronics. This new frontier has spurred the rediscovery of boron nitride (BN), a member of the family of III-N compounds that has much promise for modern electronics.

Of the many forms of crystalline BN, that with a hexagonal structure attracts particular interest for electronic applications. This form, referred to as hBN, is well established, having been widely deployed for many years. It has found use as a crucible material, in the form of sintered ceramics that benefit from its high thermal and chemical stability, and as a solid lubricant, thanks to its

layered structure. Now new opportunities beckon, with hBN under investigation as a potential platform for 2D electronics and quantum technology.

Crystalline considerations

Like carbon, BN forms crystalline structures with different atomic configurations at different pressure-temperature conditions. At relatively low pressures, BN is thermodynamically stable in its hexagonal graphite-like structure. This form features monoatomic layers strongly bound in a honeycomb pattern, like graphene, and inter-bonded with weak van der Waals forces. However, while graphene and hexagonal BN have similarities in their crystalline form, they differ in electrical conductivity, with hBN behaving as a strongly insulating crystal.

This strongly insulating characteristic is to be expected, given that hBN has an incredibly wide bandgap of 6 eV. In monolayer hBN this gap is direct, but it shifts to indirect as the number of layers increases. Surprisingly, regardless of whether this material has a direct or indirect band gap, the UV optical emission produced by hBN is extremely efficient.

It is possible to exploit the insulating character of hBN. Employed in its two-dimensional form as very thin structures – they may have just a monoatomic layer – hBN can be deployed as an excellent insulator or tunnelling dielectric barrier in devices based on graphene and other 2D heterostructures. In these devices, incredibly thin layers of hBN boost performance.

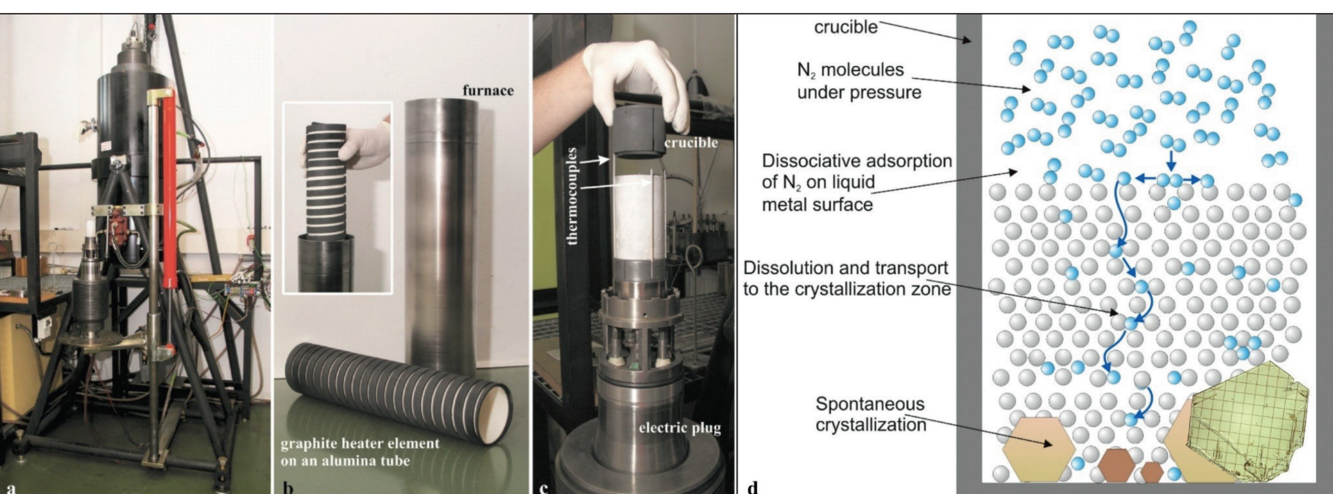
Additional opportunities arise in hBN due to defects within the material. These imperfections, often regarded as a nuisance in compound semiconductors, enable very interesting physical systems that provide single-photon emitters, or centres hosting quantum spin states with a long coherence time. Such systems are needed as the bedrock for quantum technologies.

➤ hBN flake obtained using pure nickel as the solvent

Single-crystal hexagonal BN

For both fundamental studies and the pursuit of new applications, it is critical to produce high-quality crystalline hBN, as this holds the key to uncovering its fascinating properties, as well as evaluating the predictability of theoretical models. Without access to a high-quality hBN crystal, the picture is disturbed by non-intentional defects, impurities, or strain if the crystal is deposited as an epitaxial layer on a foreign substrate.

Unfortunately, it is far from easy to grow crystalline hBN. Due to a melting temperature that exceeds 3000°C, hBN, unlike silicon and GaAs, cannot be grown from its stoichiometric melt. Due to this limitation, two leading methods have emerged for the crystallization of hBN. One of them, developed by Takashi Taniguchi and co-workers at NIMS, Japan, involves very high pressures of 5 GPa or more, and metallic solutions, containing the likes of barium, magnesium and nickel. The alternative – proposed by Yoichi Kubota from NIMS and developed by James Edgar from Kansas State University – is based on growth on the surfaces of molten transition metal alloys containing boron, and involves a flow of nitrogen gas at atmospheric



➤ Figure 1. A high gas pressure reactor with an internal diameter of 60 mm. (a) High-pressure chamber for pressures of up to 1.5 GPa. (b) Graphite heater on alumina isolating tube. (c) High-pressure plug with a crucible with thermocouples along its walls. (d) An illustration of a high-nitrogen-pressure growth from solution approach used for GaN crystallization (photo of real GaN single crystal is inserted on the right-hand side).

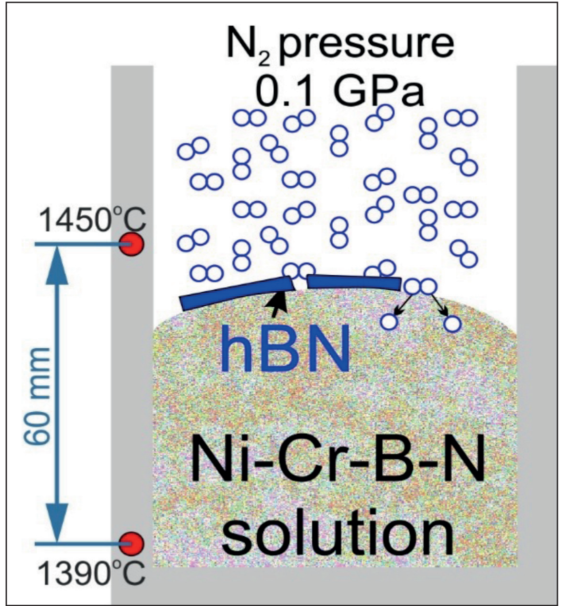


Figure 2. The hBN growth process.

pressure. For both approaches, crystals are limited to the order of 1 mm in size – although this is sufficient for a reference material for fundamental research. Another concern is the very small thickness of the hBN crystals grown on metal surfaces under atmospheric N_2 pressure.

Efforts have also been directed at growing thin layers of hBN on foreign substrates by CVD and MBE. The obvious, interesting choice of substrate for this work is highly oriented graphite, which has a similar structure – it has provided the foundation for growth of high-quality hBN layers.

It is clear that there are challenges in the crystallisation of hBN. This has motivated our team – a collaboration between the Institute of High Pressure Physics, Polish Academy of Sciences and the Institute of Semiconductor Physics, National Academy of Sciences of Ukraine – to develop a new approach to growing this exciting wide bandgap semiconductor.

Nitrogen pressure – what for?

In stark contrast to GaN and InN, hBN does not require a high nitrogen pressure to suppress its decomposition at high temperatures. Consequently, this material can be crystallised from high temperature solutions under nitrogen at atmospheric pressure. However, this approach is not as easy as it may appear at first glance, because nitrogen has an incredibly low solubility in the metals that would to be used as a growth solution for hBN. According to a paper by Yoichi Kubota and co-workers from NIMS, nitrogen solubility in pure nickel at 1550°C is as low as 0.0012 wt. percent.

Fortunately, the situation can be improved with relatively modest increases in nitrogen pressure. Recently, we have shown that it is possible to significantly enhance the nitrogen solubility in iron by increasing the free energy of nitrogen gas through compression. At atmospheric pressure and 1450°C, only 0.5 at. percent of nitrogen can be dissolved in pure iron. Increase the nitrogen pressure to 1 GPa – that's roughly 10,000 atmospheres – and the proportion of nitrogen that can be dissolved increases by over 20 times.

For high-temperature methods using atmospheric nitrogen pressure, the solubility of nitrogen in basic solutions, such as those formed by dissolving in nickel and iron, increases with additives that have a high affinity to nitrogen. For example, if pure nickel is replaced with the Ni-Cr eutectic, the solubility of nitrogen increases by 40 times. However, these additives are chemically active, complicating the growth of hBN. To avoid this, we have focused on the high N_2 pressure approach to the crystal growth of hBN. Our expectation is that through the controlled increase of nitrogen solubility in molten metals, we will enhance the growth of hBN in the c-direction in the case of surface crystallisation, and enable the production of thicker crystals.

Our ultimate goal is to establish a new approach, where in contrast to crystallisation of hBN on metal surfaces, crystals will be grown in the solution volume. That's mirroring the technique that we honed for the production of high-quality single crystals of GaN with dimensions of more than

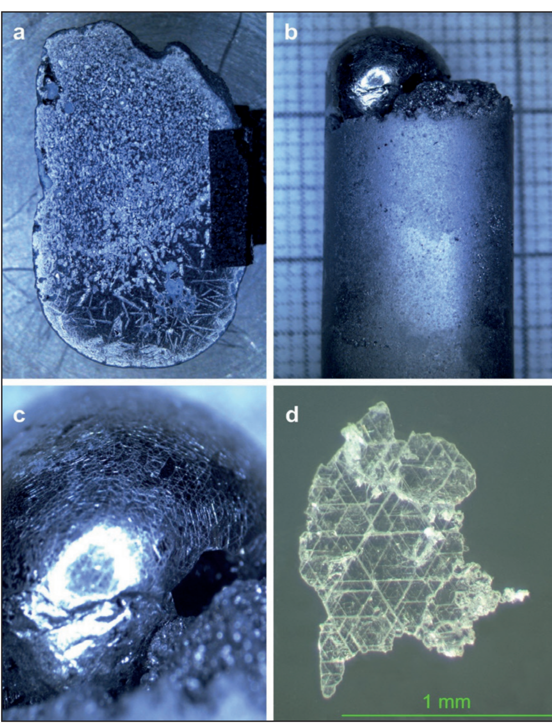


Figure 3. Results of hBN crystallization with Ni-Cr solution, at a N_2 pressure of 0.1 GPa, in a temperature gradient: (a), cross-section of the Ni-Cr-B-N ingot: CrN crystals are visible at the bottom part; (b), general view of the upper part of the ingot: a large metallic droplet emerged on the top (a very reproducible result); (c) the droplet covered with transparent hBN crystals; (d) free-standing hBN crystals exfoliated from the metal surface

1 cm (see Figure 1(d)). A driving force behind this particular methodology is the use of a temperature gradient, which enables controlled crystallisation at a constant temperature in a feed-seed configuration.

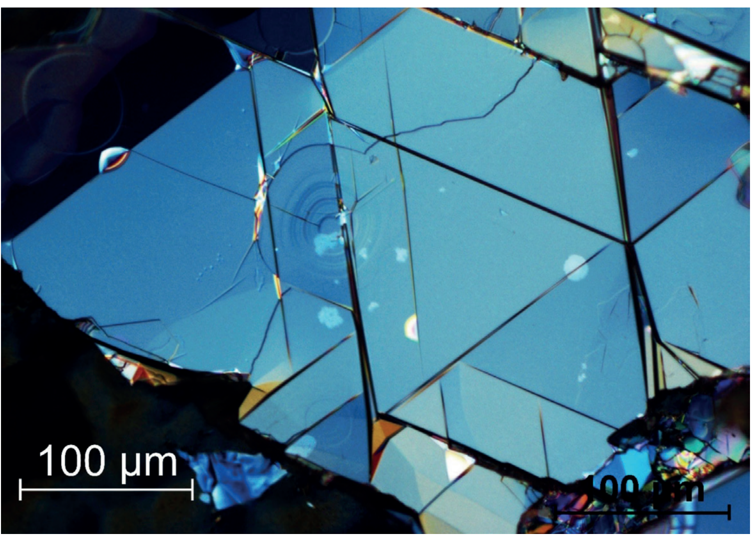
Those of us at the Institute of High Pressure Physics, Polish Academy of Sciences, work within a department that is internationally renowned for its development of reactors for crystal growth that can be monitored with a high degree of precision (see Figure 1). These reactors are capable of accommodating gas pressures as high as 1-2 GPa, temperatures in excess of 1500°C, and relatively high volumes, with internal diameters of 30 mm to 100 mm. Sets of thermocouples monitor the temperature within these reactors, allowing for precise control of temperature, temperature gradients and their changes over time. This level of control has held the key to establishing thermodynamic properties that have provided the foundation for the growth the first high-quality crystals of GaN thirty years ago. These GaN crystals, which have been extensively characterised, have been employed for homoepitaxy, thus opening this important field in GaN technology.

Initial experiments

We began investigating the growth of hBN by adopting the atmospheric pressure, high-temperature method pioneered by James Edgar. This approach involves forming a homogenised Ni-Cr eutectic mixture in an argon atmosphere at 1450°C. Quickly building on this work we added some boron, replaced argon with nitrogen gas at a pressure of 0.1 GPa, and heated this system to 1450°C to drive the dissolution of boron in the Ni-Cr melt. We established a temperature difference, varying from 1390°C at the bottom of the metal ingot to 1450°C at its top, and maintained this condition for 50 hours (see Figure 2 for an illustration of the crucible at the crystallisation phase).

These conditions led to very encouraging results regarding the growth of high-quality hBN. However, it's not been easy to interpret what happened in the crucible. We observed: efficient growth of CrN crystals at the bottom of the crucible (see Figure 3(a)); at the top of the ingot, a large droplet depleted in chromium, and containing nickel, chromium, boron and nitrogen (see Figure 3(b)); and a surface of the droplet entirely covered with colourless, transparent crystals, identified as pure hBN (see Figure 3(c) and Figure 3(d)).

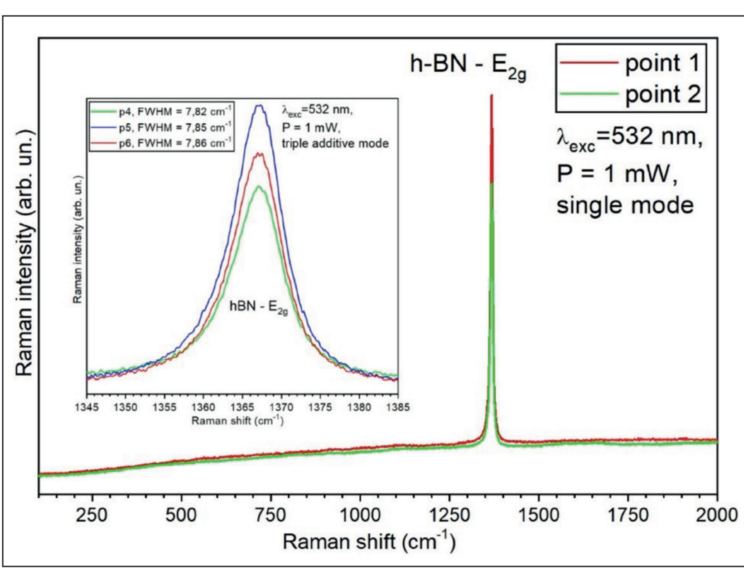
Our first crystals, which covered the metallic droplets, were fully transparent, colourless and featured mirror-like surfaces. According to energy-dispersive X-ray spectroscopy and X-ray diffraction, the hBN that we had formed had a single phase, with a c lattice parameter of 6.652 Å. The exfoliated hBN flakes, such as that shown in Figure 3(d), reached a size of a few to a few tens of mm^2. These flakes featured domains with lateral dimensions between 50 µm and 200 µm, with borderlines well-oriented along directions of the hexagonal honeycomb lattice.



➤ Figure 4. hBN crystal grown from Ni-Cr solution at 0.1 GPa N_2 pressure at 1450 °C. The growth hillock is visible in the central part, proving that growth also takes place in the direction of the *c*-axis.

Using an optical microscope to inspect the *c*-plane surface of the hBN flake adjacent to the metallic droplet during growth revealed spirals and two-dimensional growth islands that are often intersected by borderlines, which may be overgrown cracks (see Figure 4). These findings suggest that at some stages of the process, the crystal grew as a whole, prior to cracking, due to geometrical reasons, such as solidification of the metal droplet.

One of the implications of this particular growth morphology is that crystallisation on the *c*-plane of hBN probably proceeds from inside the solution. Note that this finding contrasts with the common interpretation of surface crystallisation of hBN, involving only lateral growth under constant availability of nitrogen from the gas phase. We are encourgaed by this, as it provides an opportunity to grow thicker platelets of hBN, thanks to the increased solubility of nitrogen in the growth solution.



➤ Figure 5. MicroRaman spectra of hBN.

We have also assessed the structural quality of our first hBN crystals with micro-Raman spectroscopy, with measurements at several points of the hBN flakes. In general, those spectra confirm a very high quality for our crystals, according to commonly accepted criteria. In particular, the strong and narrow E_{2g} Raman lines, with a full-width-at-half-maximum below 8 cm^{-1}, demonstrate the high perfection and uniformity of our hBN crystals (see Figure 5). It is only possible to obtain narrower peaks by turning to isotopically pure boron and nitrogen for crystallisation, an approach adopted by Edgar and co-workers.

Next steps

Our initial findings show that adding chromium to nickel significantly disrupts the Ni-Cr-B-N growth system under a N_2 pressure of 0.1 GPa and temperatures ranging from 1390°C to 1450°C. We have been able to observe excellent growth in the temperature gradient of CrN crystals, with hBN crystals forming solely on the metal surface. This led us to embark on a new set of experiments, involving the removal of chromium from the system, replaced by N_2 under high pressure. This change provides an efficient source of nitrogen, which can dissolve in molten nickel or other selected solvents.

Using this approach, we have investigated hBN growth using a relatively low pressure of 0.1 GPa and a slow cooling stage, in the 1450°C – 1350°C temperature range. These conditions result in similar surface crystallisation to our previous work with Ni-Cr. Again, transparent and colourless flakes are exfoliated from the metal surface. We have found that the dimensions of the individual crystalline hBN domains varies according to the initial concentration of boron added to the solution. These domains can be as small as 25 μm and 50-100 μm for 4 wt. percent and 2 wt. percent of boron, respectively.

We can conclude from this work that there is probably enhanced hBN nucleation on the metal surface, which is detrimental for growing large hBN crystals by this method. Similar to growth at atmospheric pressure and high temperatures, it is crucial to establish equilibrium conditions for the BN-solvent system (the liquidus curve). Doing so ensures a proper start to the supersaturation stage, by either slow cooling or the application of a temperature gradient.

Our initial experiments have determined that the enhanced nitrogen solubility, resulting from high pressure, does not in itself hold the key to obtaining thicker hBN crystals. We have also discovered that it's essential to develop a method for supplying nitrogen to the volume of the solution during the crystallisation process. This represents one of the subsequent phases in our ongoing research, focused on developing a more effective method for the crystallisation of hBN, which is without doubt a significant and intriguing material.

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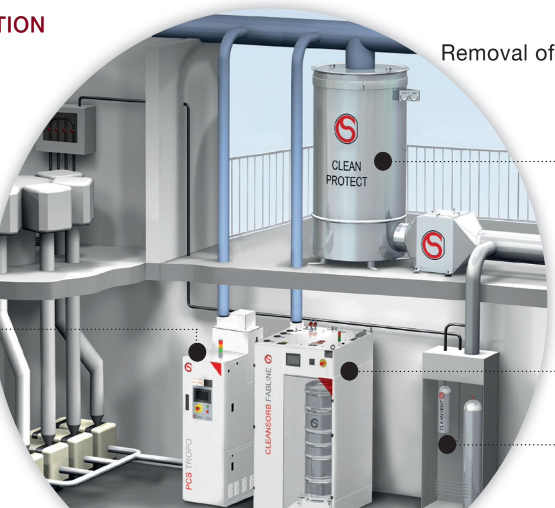

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Gaining greater insight into the GaN HEMT

A more comprehensive understanding and evaluation of the GaN HEMT comes from a rigorous model of how it is deployed and new approaches to scrutinise this device

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WHEN DEPLOYED in power electronics, the GaN HEMT delivers a great deal of bang per buck. Its strong performance stems from a number of attractive attributes, including a capability to withstand very high electric fields, an excellent electron mobility, and a high operating frequency. These strengths are realised alongside a competitive cost, thanks in part to the growth of GaN on large-diameter silicon wafers that can be processed in established lines.

The compelling performance of the GaN HEMT is driving its uptake in ever more applications. It's first taste of significant success came from its incorporation in fast-chargers for mobile devices. And over the coming years, shipments will continue to rise as it wins sales in more markets, with deployment forecast in telecommunication and data centre infrastructure, motor drives and inverters for solar panels.

However, there is still much to do to ensure that the GaN HEMT has long-term, growing success in these markets. As it will be deployed in more demanding applications and undergo a range of stresses, including those that come from hard switching and ringing, it is vital to understand the level of reliability it offers in these situations. In addition, the GaN HEMT is still a work in progress, so it's important to gain a deeper understanding of its weaknesses – they include a trapping of carriers, which can lead to an increase in on-resistance and a shift in threshold voltage. In some cases, measurements are needed on production devices, ideally undertaken on-wafer, as this saves time and money.

The good news is that progress is being made on all these fronts, with gains reported at this year's International Reliability Physics Symposium (IRPS), which took place on 14-18 April in Dallas, Texas. At this conference Sandeep Bahl from Texas Instruments outlined a more robust approach to assessing GaN reliability in various power-supply applications; on-wafer approaches to measure on-resistance, threshold voltage and degradation that have been pioneered by the University of Padova, STMicroelectronics and BelGaN, were described by two spokesmen from the university; and Yu-Shan Lin from TSMC detailed the impact of different processes on trapping in field plates.

Reliability in the field

To help ensure that power electronics offers sufficient reliability in a range of applications, standards exist for assessing device performance. This is not a new innovation, having been established for silicon technologies several decades

ago. There are documents from the mid-1990s specifying the methodology to evaluate this device, consider electrostatic discharge, and to put this package through its paces. Such standards are accompanied by documentation for accelerated test-to-failure, used to calculate lifetimes from relevant failure mechanisms.

More recently, standards have expanded to GaN HEMTs. The guideline JEP 180, published in 2020, offers guidance for calculating the switching lifetime from accelerated lifetime testing. Bahl highlighted this documentation when describing what is claimed to be the first generalised approach for determining the hard-switching lifetime of a GaN transistor.

"We first use a test-vehicle circuit appropriate for accelerating the desired switching-stress type, which was hard switching," remarked Bahl. "We then ran accelerated lifetime testing on a TI GaN part, generated a model and calculated the switching lifetime."

According to Bahl, there are three main challenges when determining the switching lifetime: the complexity of the switching transition, which involves voltages, currents, temperatures, duty cycles, frequencies and slew rates; dependence of the stress on the application circuit; and the lack of a broad modelling approach.

Bahl explained that it is desirable to have a test vehicle circuit for the stress test, and for the switching lifetime to be calculated for a broad application use: "This would allow the use of a test wafer circuit suitable for accelerating the desired failure modes. This is an important factor, because regular application boards are typically not suitable for high acceleration, and may produce false failures, or incorrectly accelerate the failure mode desired."

To evaluate lifetime, Bahl and co-workers have used a boost converter circuit, with the output tied back to the input. This provides a hard-switching stress to the device.

Claiming to break new ground, the team from TI has determined the switching stress by integrating the switching waveform, including wearout acceleration factors. This approach is said to capture the complexity of the switching waveform. To provide a generalised methodology, Bahl and co-workers have also considered the switching stress rate, which accounts for the temperature, duty cycle, frequency and the switching stress per transition. "An important advantage of this approach is that is allows the use of conventional reliability acceleration functions," added Bahl.

According to him, one advantage of the switching stress calculations is that they can be applied to any switching waveform, regardless of whether it is measured or simulated. Using both simulated and measured waveforms, the team have determined switching lifetimes for a TI part. This suggests a lifetime of more than 1 billion years for 400 V, 8 A hard-switching at 100 kHz.

"Note that the model is for hard failure due to hard switching, since that was the type of stress accelerated," remarked Bahl. "Other types of stress would be considered either independently or cumulatively, depending on whether the same failure mode is exercised."

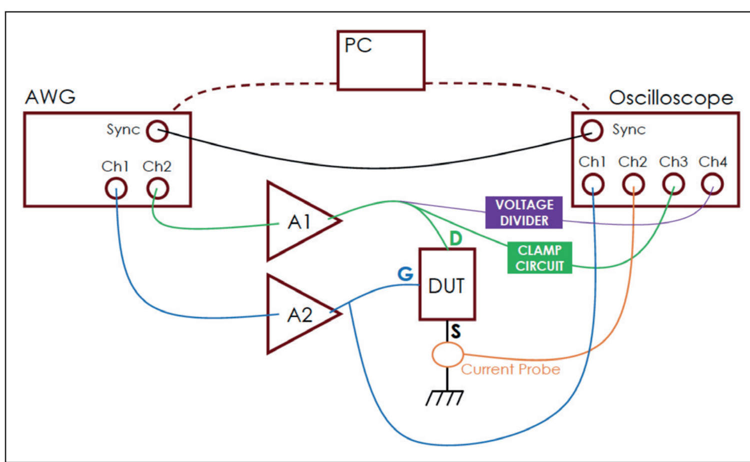


Figure 1. The set-up used by the University of Padova, in partnership with BelGaN, for on-wafer measurements of threshold voltage and on-resistance. This set-up includes an arbitrary waveform generator, two amplifiers that connect the arbitrary waveform generator to the device under test, an oscilloscope to acquire all the signals, and a clamp circuit that is needed to measure the drain voltage, in order to extract the on-resistance of the device.

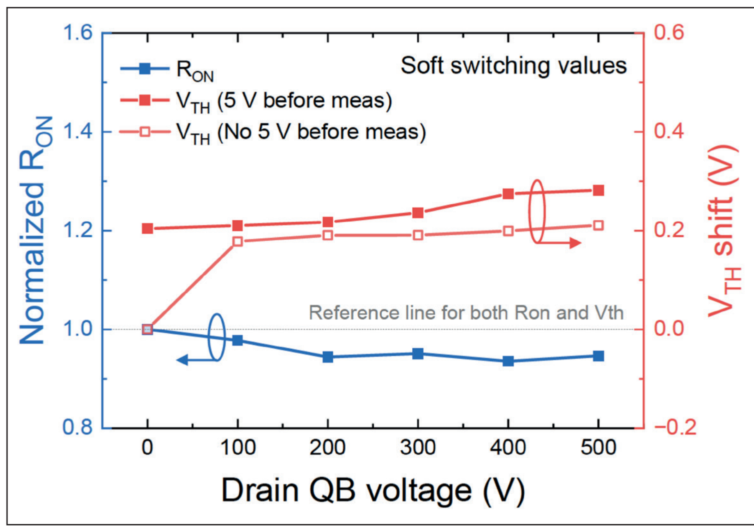
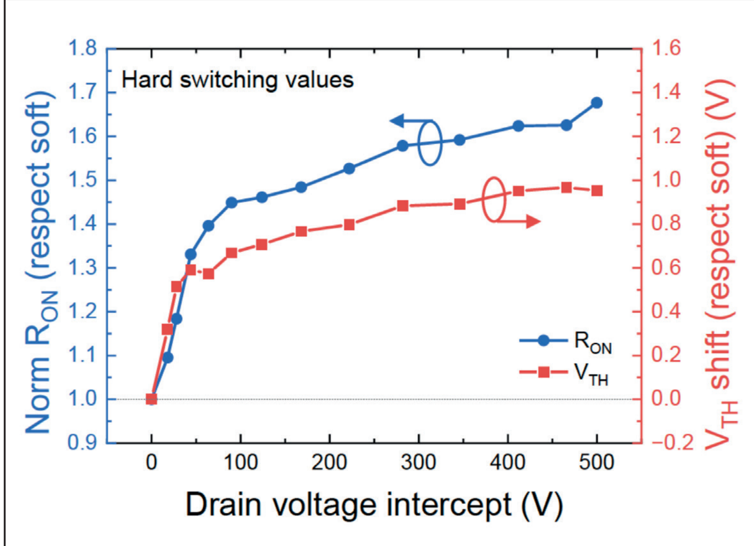


Figure 2. There are relatively small changes in the on-resistance (R_{ON}) and the threshold voltage (V_{TH}) during soft-switching.

Passivation and layout

Hard-switching conditions were also employed during on-wafer measurements by the University of Padova and BalGaN, a collaboration that considered



➤ Figure 3. Hard switching leads to significant changes in on-resistance (R_{ON}) and the threshold voltage (V_{TH}).

the impact of passivation and gate layout on both the on-resistance and the threshold voltage.

Before detailing this work at IRPS, Davide Favero from the University of Padova discussed some of the origins of the weaknesses in GaN HEMTs.

Favero remarked: "Due to the lower maturity level of the technology of *p*-GaN HEMTs compared to silicon carbide MOSFETs, these devices may suffer from instabilities, concerning both threshold voltage and on-resistance."

He pointed out that there can be a threshold voltage instability induced by the gate bias, primarily due to either the trapping of electrons or holes, or the injection of holes from the gate contact. A drain bias induced threshold voltage instability may also arise, associated with hole deficiency.

Gate and drain bias can also influence the dynamic on-resistance, according to Favero: "The most common instabilities are due to drain bias, but in literature it was shown that gate bias can induce an increase in on-resistance, because of hole traps in the AlGaN."

Under drain bias, the dynamic on-resistance can both increase and decrease. Increases can come from an injection of electrons from the substrate towards the buffer, leading to trapping; and ionisation of buffer acceptors, usually carbon, leading to a redistribution of charges in the buffer. It is also possible to have positive charges generated inside the buffer, causing a decrease in on-resistance. However, through an optimised process, it is possible to ensure a stable dynamic on-resistance.

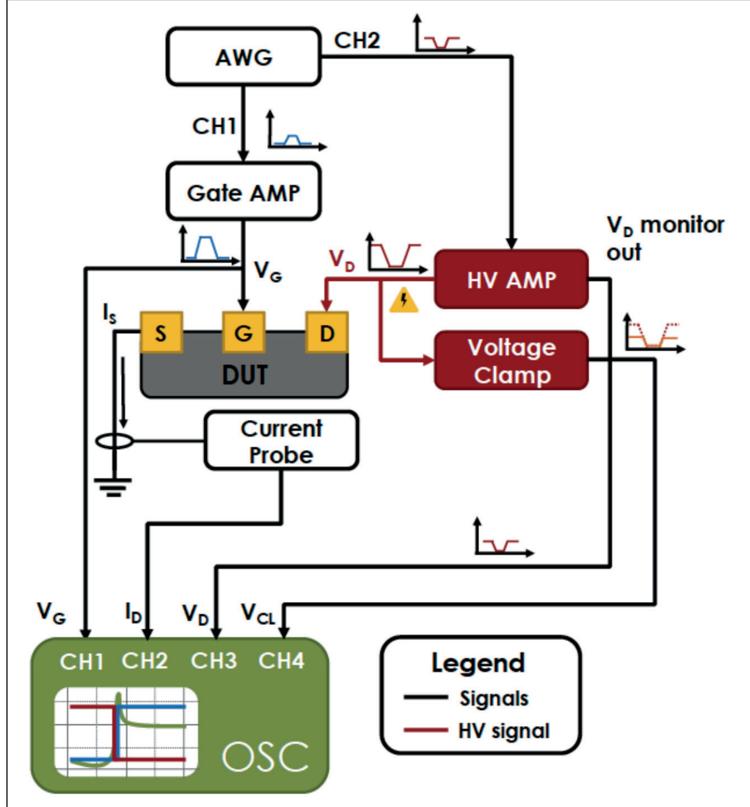
According to Favero, one significant concern for the GaN HEMT is its operation under hard switching, which enhances the trapping process through the presence of hot electrons. Trapping occurs at the gate stack, and also in the access region, where it occurs at the interface between AlGaN and the passivation layer.

"These hot electrons may lead to an increase in the on-resistance, but also to an increase in the threshold voltage, because of trapping of electrons in the gate stack", remarked Favero, before adding: "I believe it is of crucial importance to be able to distinguish between an increase in on-resistance due to an increase of the resistivity of the channel in the access region, and an increase in the on-resistance that is due to an increase in the threshold voltage."

To distinguish between these two causes, Favero and co-workers use a custom set-up, involving commercial instruments and homemade circuits (see Figure 1). This highly flexible approach offers complete control of the waveforms, and enables measurements in the microsecond range.

Using this set-up, the researchers have subjected devices to hard switching, using a range of pulsed currents and voltages. Hard-switching conditions, which are kept constant through judicious selection of the applied voltage waveforms, enable extraction of values for on-resistance and threshold voltage.

Favero and colleagues have used this approach to assess a portfolio of HEMTs with a *p*-GaN gate,



➤ Figure 4. The set-up used by the University of Padova, in partnership with STMicroelectronics, for on-wafer measurements of the degradation of GaN HEMTs.

fabricated on a 150 mm silicon substrate. Within this family of devices are transistors with shorter and longer gate lengths, and three forms of passivation.

Efforts began by assessing devices under soft switching, a condition where the architecture of the field plates and passivation do not have a significant impact on HEMT performance. Increases in the drain bias led to an increase in threshold voltage, due to hole deficiency (see Figure 2). There is also a shift in threshold voltage when applying 5 V to the gate before the measurement – this shift is due to electron trapping in the barrier.

There is minimal change in the dynamic on-resistance with drain bias, due to a balance between different mechanisms occurring in the buffer, such as the ionisation of carbon dopants and the generation of positive charges.

Under hard switching, there are significant shifts in both on-resistance and threshold voltage, with the greatest changes occurring when the drain voltage increases from 0 V to 100 V (see Figure 3).

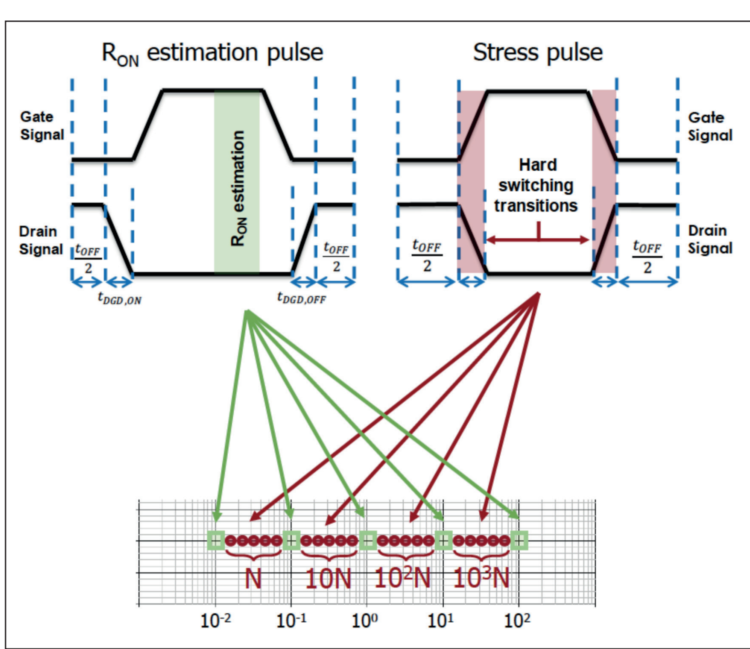
The team have studied the impact of their three different passivation processes using drain voltages between 0 V and 125 V. Differences in processes did not lead to significant variation in threshold voltage, but did lead to marked differences in on-resistance.

"Because of difference passivation, we have a different amount of defect states at the passivation-AlGaN interface that results in different on-resistance increases," explained Favero, who added that the process is completely recoverable.

He and his co-workers have also found that shorter field plates lead to a lower increase in on-resistance with voltage. According to simulations, the shorter field plate offers a better performance, thanks to a reduction in the peak electric field. Meanwhile, the threshold voltage is not affected significantly by changes to the field geometry.

Delving into dynamic on-resistance

On-wafer measurements of the on-resistance have also been carried out by Favero's colleague, Micro Boito, who reported results on an investigation by the University of Padova, in partnership with STMicrolectronics. This effort focused on studying the degradation processes associated with dynamic operation of GaN HEMTs.



➤ Figure 5. On-wafer measurements of degradation in 650 V *p*-GaN lateral GaN-on-silicon HEMTs involve on-resistance estimation pulses and stress pulses.

Boito argued that there are two leading tests or validating GaN HEMTs. One is the dynamic high-temperature operation lifetime test, which runs for 1,000 hours under specified conditions that represent all typical applications. "This usually follows the JEDEC guidelines," remarked Boito. He explained that the other test is the switching advanced life-time test – this aims to extract the main degradation mechanisms by applying more stressful conditions for a shorter period of time.

The novelty of the work of Boito and co-workers is that it offers a new way to conduct on-wafer tests (see Figure 4). Strengths of this latest approach are: the introduction of a current-sensing circuit, to evaluate the drain-current waveform during switching; and due to subjecting the drain current waveform to a large swing, improvements to the voltage sampling resolution, by adding a fast clamp circuit that limits the applied voltage to the oscilloscope channel. The team's set up allows fine tuning of the stress conditions from soft to hard switching by adjusting the overlap and the rise and fall times between the gate and drain signals.

With this set-up the team have monitored the dynamic degradation of state-of-the-art 650 V

At TSMC, engineers have investigated the correlation between defect-generation regions and field plates using capacitance-voltage analysis at high voltages. This effort, involving HEMTs and reported at IPRS, targeted improved trapping behaviour through optimisation of the production process.

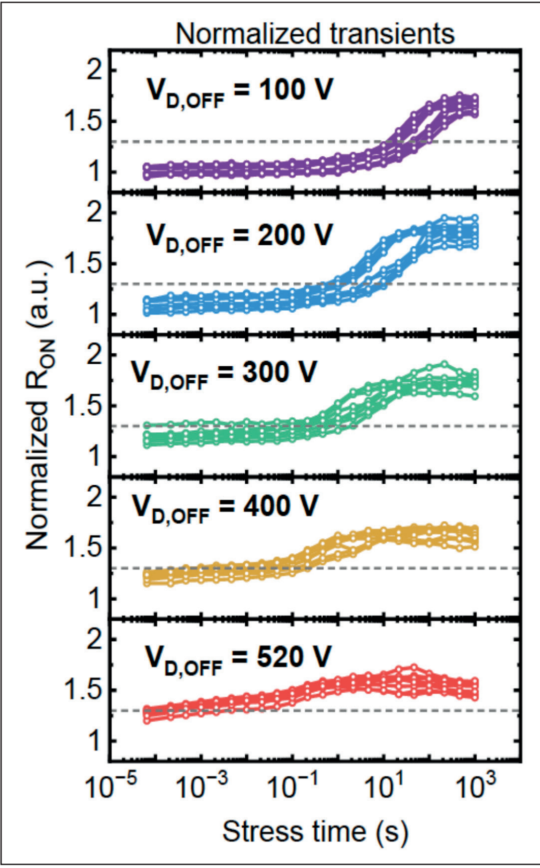


Figure 6. Trapping, probably in the buffer, is the main cause of on-resistance degradation in 650 V *p*-GaN lateral GaN-on-silicon HEMTs.

p-GaN lateral GaN-on-silicon HEMTs under hard switching and off-state stress. This work involves using two pulses: an on-resistance estimation pulse that determines the resistance via ohm's law, and a stress pulse. On-resistance estimation pulses are applied on a logarithmic time scale, with the stress pulses deployed between each of them (see Figure 5).

To distinguish between permanent and recoverable degradation, Boito and co-workers illuminate these samples with a 365 nm source. This excitation liberates traps within the device, thereby identifying recoverable degradation.

The team have undertaken voltage-step stress measurements on 10 devices, with an off-state voltage rising from 100 V to 520 V, using what is described as a cross-over level of 30 percent – that's the overlap between the gate and drain voltages. For this investigation, the switching frequency is 20 kHz.

A degradation in on-resistance is seen in these measurements, with an onset that occurs earlier at a higher off-state voltage (see Figure 6). However, for all 10 devices, the unwanted increase in on-resistance can be recovered by exposure to UV light. Based on this finding, Boito claimed that trapping, probably in the buffer, is the primary cause of on-resistance degradation. Subsequent temperature-dependent measurements supported this suggestion of trapping in the buffer.

Boito and colleagues have also collected off-state stress, so they can separate the impact of hard-switching from buffer trapping. Step stress measurements from 100 V to 600 V have uncovered two different trapping mechanisms: initially surface trapping at short stress times, associated with surface traps; and later on an exponential fall in in on-resistance, due to buffer traps (see Figure 7).

Modelling by the team explains both trapping mechanisms. The surface trapping comes from a high polarisation during the off-state that causes a leakage current, leading to ionisation of carbon acceptors in the carbon-doped region. A redistribution of the charge with the carbon-doped and unintentionally doped layers follows, causing the depletion of the two-dimensional electron gas, and ultimately a lowering of the drain current and an increase in on-resistance.

Under a longer stress time, there is band bending, due to charge storage in the unintentionally doped and carbon-doped layers that leads to an increase

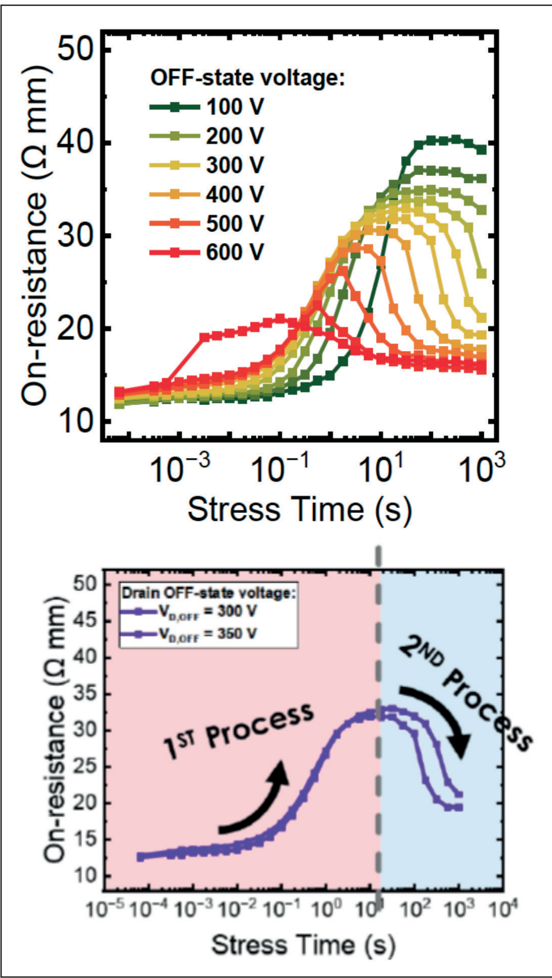


Figure 7. Step stress measurements from 100 V to 600 V have uncovered two different trapping mechanisms in 650 V *p*-GaN lateral GaN-on-silicon HEMTs (top). Processes that impact the two-dimensional electron gas can account for changes in the on-resistance (bottom).

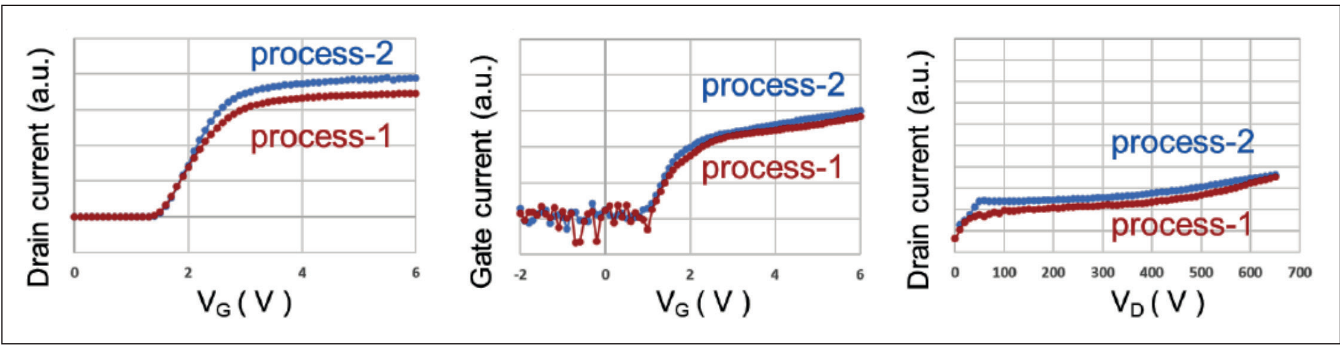


Figure 8. TSMC has studied E-mode 650 V GaN devices, housed in a TO-220 package and having the substrate connected to the source. Process-2 producing a strong polarisation that leads to a higher value for the two-dimensional electron gas.

in tunnelling probability. This leads to generation of electron-hole pairs at the interface, and in turn band-to-band tunnelling in the unintentionally doped GaN layer, alongside the generation of positive charge at the bottom of the carbon-doped layer. These processes increase the density of the two-dimensional electron gas, and lower the on-resistance.

Analysing traps

At TSMC, engineers have investigated the correlation between defect-generation regions and field plates using capacitance-voltage analysis at high voltages. This effort, involving HEMTs and reported at IRPS by Yang, targeted improved trapping behaviour through optimisation of the production process.

Yang and her co-workers have investigated 650 V E-mode HEMTs that feature two field plates, have the substrate connected to the source, and are housed in a TO-220 package. HEMTs have been formed using two processes, with what is referred to as Process-2 producing a stronger polarisation that leads to a higher value for the two-dimensional electron gas, and higher on and off currents (see Figure 8).

The team from TSMC have used a Keysight B1505A power device analyser to conduct high-voltage capacitance-voltage measurements of their devices. The goals have been to assess the processes, and to determine which one provides the best balance between performance and reliability.

To evaluate reliability, Yang and her colleagues undertook high-temperature reverse-bias measurements, employing a gate voltage of 0 V, a drain voltage of 520 V, and an elevated temperature of 150°C. Over 48 hours the team monitored changes to the linear drain current (see Figure 9).

"We found that the [linear drain current] initially improved, due to the accumulation of holes in the buffer, but after 10,000 seconds it started to degrade due to the stress," remarked Yang. She attributes initial behaviour to the test inducing vertical band bending, which results in a redistribution of electrons and holes in the carbon-doped GaN layer, explaining that electrons are drawn to the channel and collect at the drain, while holes accumulate in the buffer layer. "This accumulation of holes in the buffer layer reduces the on-resistance of the channel and enhances the two-dimensional electron gas," argued Yang. Both devices were found to have a similar level of enhancement to the linear drain current, implying that the GaN buffer layer is of consistent quality.

Another key finding by the team is that the electron trap that is responsible for the degradation in the linear drain current is located outside the buffer layer.

Support for these inferences comes from capacitance-voltage plots of HEMTs produced by both processes (see Figure 10). The behaviour of the electron trap at the first field plate during capacitance-voltage measurements indicates that the degree of electron trapping near the gate is much greater than the effect of hole trapping.

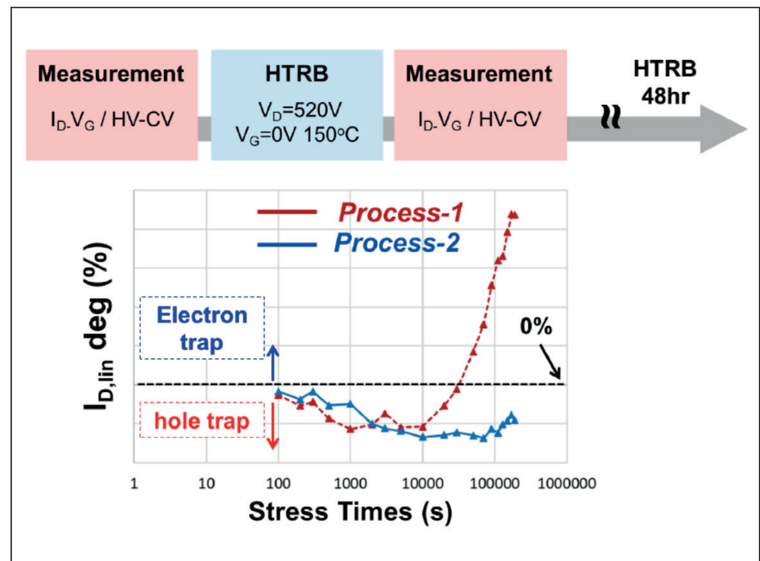


Figure 9. Engineers at TSMC studied the degradation of the linear drain current by employing a gate voltage of 0 V, a drain voltage of 520 V, and an elevated temperature of 150 °C.

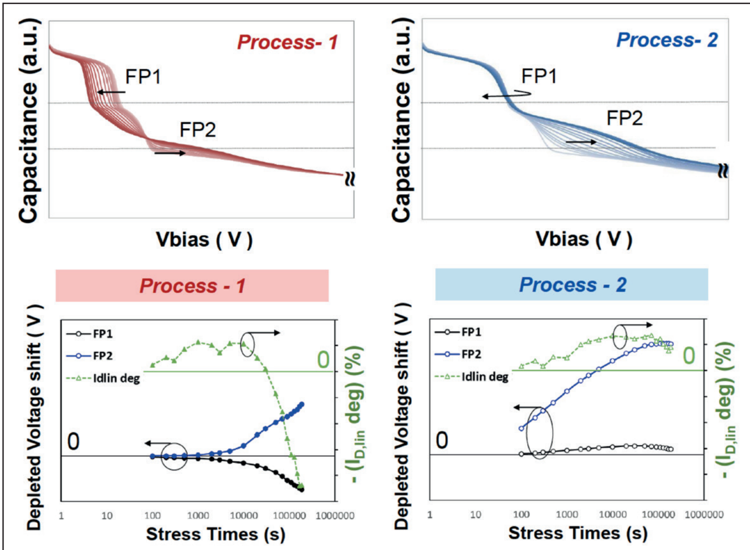


Figure 10. TSMS's capacitance-voltage plots on the HEMTs taken during high-temperature reverse-bias stress offer insight into carrier dynamics.

Note that the behaviour at the second field plate is markedly different, dominated by hole trapping.

Also shown in Figure 10 are shifts in the depletion voltage, calculated from capacitance-voltage measurements. This information uncovers both the type of trapping, and its extent – revealed by the degree of shift. Based on these profiles, Yang and co-workers have concluded that: the trap capture caused by process-2 is more stable in the field plate region; the field plate region is more susceptible to electron trapping; and that the electron trap near the gate at the field plate is improved by process-2, based on high-temperature reverse-bias measurements.

"To distinguish the effects of the bulk and dielectric layers, we modified the device design," explained Yang. This involved connecting the source and gate, while isolating the bulk.

The team used a floating bulk stress to eliminate the impact of the buffer layer, and applied a bulk stress of -650 V to mitigate the effect of the dielectric layers and emphasise the impact of bulk traps.

The key conclusion from this experiment is that holes in the bulk stress enhance the linear drain current. Based on this observation, it's argued that in addition to electron trapping, holes that accumulate in the carbon-doped GaN layer play an important role during high-temperature reverse-bias tests.

In addition, the team have carried out capacitance-voltage measurements after subjecting devices to 48 hours at a high temperature under reverse bias. This investigation revealed that the trap density is significantly reduced after the application of a high temperature and reverse bias, with the greatest gains occurring in the field plate region located near the gate. This led Yang and co-workers to speculate that improving material quality can cut the concentration of native defects, resulting in a lower trapping density.

"We hope that our findings will inspire further research in the field and contribute to the development of more efficient and reliable power devices," added Yang.

These sentiments will be held by all those at IRPS, with their progress helping to underpin the production of more competitive, higher-performance power devices that will play a key role in helping to address climate change.

Taking the power of the InP PCSEL to new highs

A double-lattice photonic crystal structure ensures powerful, incredibly narrow emission at 1550 nm

A PARTNERSHIP from Japan that includes the group that invented the photonic crystal surface-emitting laser (PCSEL) claims to have smashed the output power for this class of device at 1550 nm.

This team's InP-based laser, produced by a partnership between its pioneers at Kyoto University and engineers at Sumitomo Electric Industries, is capable of delivering a continuous output power of 300 mW. Prior to this success, the most powerful PCSELs emitting at around 1.55 μm were only capable of emitting 100 mW under pulsed operation.

The PCSEL is renowned for its single-mode operation, high optical power and high-quality narrow-divergence angle beam – and more powerful versions emitting around 1.55 μm are attractive sources for lidar, material processing and optical communication.

"We believe that 300 mW [PCSELs] can already meet requirements for some practical applications," remarked Kyoto University's Susumu Noda, who attributes the record-breaking output power of the team's PCSEL to advances in design and processing.

"Our double-lattice photonic crystal design is optimised for the 1550 nm wavelength, based on our extensive experience with GaAs-based and InP-based PCSELs," said Noda. "Additionally, our well-controlled etching and regrowth processes result in minimal damage, thereby reducing optical losses."

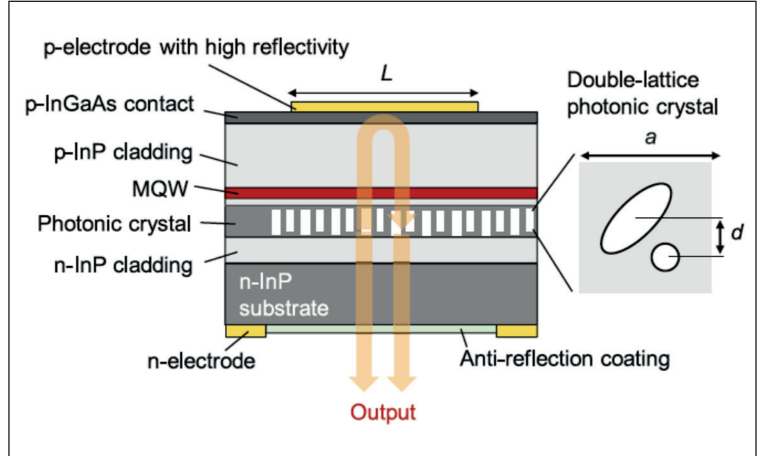
Fabrication of the team's PCSEL began with the growth of an epitaxial stack by MOCVD, followed by the formation of a photonic crystal structure, using electron-beam lithography and dry etching. Overgrowth of an InP spacer layer encapsulated air holes, prior to addition of an active region featuring four InGaAsP quantum wells, followed by a *p*-type InP cladding layer and a heavily *p*-doped GaInAs contact layer. By taking this approach, the team avoided any chance of damaging the active layer.

To complete the fabrication of their PCSEL, Noda and colleagues added electrodes. Their *n*-type electrode, which defines the size of the device and features a circular window through which the light is emitted, has a diameter of 200 μm. As well as injecting carriers, the *p*-type electrode serves as a backside reflector that enhances slope efficiency.

The InP-based PCSEL features a double-lattice photonic crystal structure, employed to realise high-power single-mode operation, that combines small circular holes with those that are larger and elliptical.

Measurements revealed a room-temperature maximum output power of 318 mW, realised at a wall-plug efficiency of 17.3 percent. At this temperature the threshold current is 230 mA, and the threshold current density 0.73 kA cm^{-2}. The latter value is only a little higher than that of 0.67 kA cm^{-2}, associated with the threshold current density of the team's 1300 nm PCSELs. The team attribute this small increase in threshold current with wavelength to a larger intrinsic loss, and an increase in Auger recombination.

The team has recorded the room-temperature spectral emission of its latest PCSEL using a drive current of 1770 mA, corresponding to the peak output power. This measurement confirmed single-mode emission, peaking at 1564 nm, and provided a value for the full-width-at-half-maximum of less than 0.02 nm, which is the resolution of the analyser.



➤ The double-lattice photonic crystal played a vital role in increasing the output power of 1.55 μm PCSELs.

Values for the side-mode suppression ratio were measured for drive currents ranging from below 1000 mA to more than 2000 mA, and for temperatures from below 20°C to 60°C. In all cases, the side-mode suppression ratio exceeded 60 dB.

Noda and co-workers have also investigated the high level of stability of the single-mode operation of their PCSEL, with calculations attributing this asset to a large threshold gain margin, as well as a moderately weakened in-plane optical coupling of the photonic crystal structure.

According to Noda, the next goals for the team are to improve their designs, including the photonic crystal, and realise watt-class operation.

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➤ T. Aoki *et al*. Appl. Phys. Express **17** 042004 (2024)

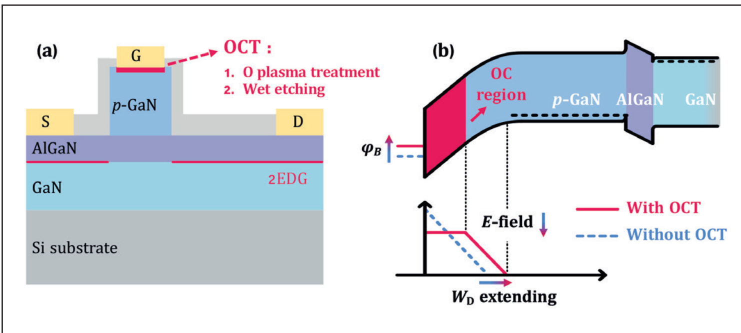
Improving HEMT reliability with oxygen plasma treatment

Oxygen compensation increases the breakdown voltage and reliability of the GaN HEMT, while supressing its gate leakage current

ENGINEERS FROM CHINA are claiming to have developed a simple, low-cost approach based on oxygen plasma treatment to improve the reliability of *p*-GaN gate HEMTs.

According to these researchers from Southern University of Science and Technology, their process extends the lifetime of Schottky-type *p*-GaN HEMTs by reducing the electric field in this device through compensation of magnesium acceptors.

This breakthrough could strengthen the competitiveness of Schottky-type *p*-GaN HEMTs, which offer excellent electrical efficiency and are already winning deployment in a number of applications, including data centres, electric vehicles and consumer electronics.



➤ Schottky-type *p*-GaN HEMTs (a) benefit from oxygen plasma treatment, which reduces the strength of the electric field (b).

Today's commercial Schottky-type *p*-GaN HEMTs suppress gate leakage, but are hampered by a narrow bias window for safe operation that stems from the time-dependent gate breakdown. Catastrophic breakdown results from degradation at the metal/*p*-GaN Schottky junction, caused by a combination of hot electron bombardment and electric field stress.

Several teams have devised ways to slow this degradation, by either increasing the robustness to hot electron bombardment or reducing the electric field strength. Introducing materials such as GaON, Ga_2O_3 and AlGaN combat electron bombardment, and the addition of an intrinsic GaN layer quashes the electric field strength. However, these approaches either require: the growth of new layers on the *p*-GaN surface, leading to concerns related to the magnesium memory effect; or high-temperature annealing, which adds to the thermal budget.

Addressing all these concerns is the process developed by engineers from Southern University of Science and Technology. According to spokesman Chengcai Wang, their team's approach has been inspired by the work of Kevin Chen's group from The Hong Kong University of Science and Technology – that team employed oxygen plasma treatment to deplete the top layer of *p*-GaN and obtain a normally-off *p*-FET. Wang says that based on that finding, he and his co-workers thought that oxygen plasma treatment might offer a simple and effective method to compensate for magnesium on the *p*-GaN gate surface and thus reduce the peak electric field.

To investigate this possibility, Wang and co-workers have used oxygen plasma treatment when producing devices. Oxygen penetrates into the *p*-GaN layer to form oxygen donors or MgO complexes that compensate for the activated magnesium dopants. A weakly doped or intrinsically doped GaN layer results, decreasing the local electric field (see figure).

According to Wang, oxygen treatment has the potential to be employed for high-volume production, because it avoids complicated equipment and the entire process is compatible with the current GaN manufacturing process. "Furthermore, a uniform oxygen plasma is usually easy to obtain," claims Wang.

The team fabricated its HEMTs by removing the *p*-GaN stack outside the gate region, adding source and drain contacts, undertaking planar isolation and depositing a passivation layer. After plasma treatment, soaking the sample in HCl removed the regions of the *p*-GaN layer that were heavily oxidised or damaged, prior to the addition of a Ni/Au gate contact, annealed at just 350°C.

Comparing the characteristics of plasma-treated and untreated HEMTs revealed that the introduction of oxygen reduced the leakage current and capacitance of the Schottky junction. Additional benefits included an increase in the room-temperature breakdown voltage from 10.4 V to 14.5 V, and an increase in the time-dependent gate breakdown. Evidence of the latter is an increase in the maximum bias from 4 V to 8.1 V, for a 1 percent failure rate for a 10-year lifetime.

"In future work, we plan to more comprehensively study the effect of oxygen plasma treatment process parameters on device performance and improve the effect of oxygen compensation technology in practical applications," said Wang.

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➤ C. Wang *et al.* Appl. Phys. Express **17** 051002 (2024)

Producing GaN substrates with pore-assisted separation

Switching from voids to pores to separate GaN could lead to cheaper substrates

ENGINEERS FROM SUMITOMO CHEMICAL are pioneering an electrochemical-based method that promises to trim the cost of producing large, high-quality, free-standing GaN substrates. By controlling the size of pores produced in GaN, the team can create free-standing substrates without the need for a high-temperature process.

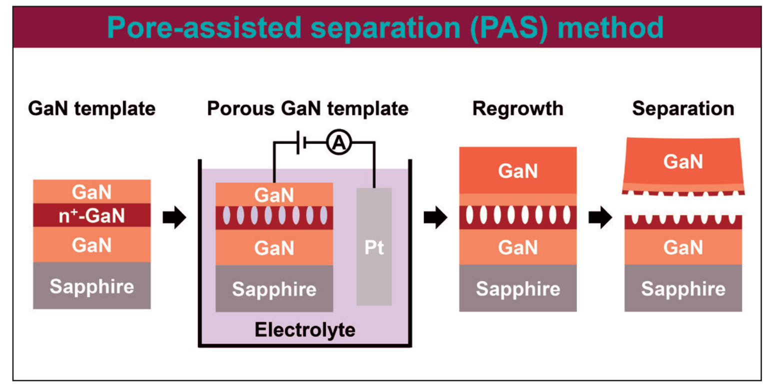
"We found that large pores allow us to fabricate free-standing GaN substrates by realising the separation of thick GaN layers from porous GaN templates," remarked team spokesman Masafumi Yokoyama. He added that in earlier work, he and his co-workers produced pores in a well-defined location, but the pore size was limited to a few tens of nanometres, which is too small for wafer separation.

Using larger pores, the engineers from Sumitomo Chemical have produced a 2-inch free-standing substrate with a material quality comparable to that of the company's commercial GaN substrates, produced using a combination of void-assisted separation and HVPE growth of GaN at rates in excess of 100 μm/hr. Those voids, used to create free-standing substrates, are formed by annealing a titanium-coated GaN template at about 1,000°C. The size and density of these voids can be adjusted through precise control of the annealing conditions.

Two weakness of the void-assisted technique are that: it is challenging to maintain uniform annealing conditions across larger wafers, limiting the size of GaN substrates to 100 mm in diameter; and that it requires two high-temperature processes, hampering throughput and increasing production costs.

With the pore-assisted approach, there is no need for high temperatures. That's avoided with an electrochemical approach, which is not new, having being used before to create pores in GaN-based distributed Bragg reflectors. However, Yokoyama and co-workers have adapted the process to make it suitable for producing substrates. Previous efforts produced pores with a size of just a few tens of nanometres – that makes them too small to survive during the growth of thick layers of GaN – but by adjusting the electrochemical conditions, pores can be sufficiently large, with diameters of more than 100 nm.

Sumitomo's pore-assisted process begins with the growth of templates, by either MOCVD or HVPE. An undoped GaN base layer at least 1 μm thick is followed by a heavily-doped *n*-type layer that has a thickness between 1 μm and 3 μm and an *n*-type cover layer with a thickness of 100 nm and 200 nm.



➤ Sumitomo Chemical's pore-assisted process involves the growth of a GaN template (a), followed by electrochemical etching (b), regrowth (c), and stress-driven separation during cooling (d).

Using a room-temperature electrochemical process involving a platinum electrode, an oxalic acid solution, and the application of between 10 V and 20 V, pores are formed in just the heavily doped *n*-type layer. On these porous GaN templates, GaN layers with thicknesses between 200 μm and 800 μm are grown by atmospheric pressure HVPE at 1,000°C. During post-growth cooling, stress resulting from differences in thermal expansion coefficients drives the separation of GaN and sapphire.

According to atomic force microscopy, the porosification process has little impact on surface morphology. Introducing pores increases the root-mean-square surface roughness from 0.36 nm to 0.45 nm, for a scan area of 5 μm by 5 μm.

Cross-sectional scanning electron microscopy reveals that pores start to form when around 5-6 V is applied in the electrochemical process. Beyond this threshold, the height and width of the pores increases almost linearly with voltage, to exceed 100 nm under application of more than 15 V.

The engineers from Sumitomo have used their pore-assisted approach to produce 2-inch substrates with thicknesses of 200 μm and 800 μm that have, according to cathodoluminescence, threading dislocation densities of around 1.4×10^7 cm^{-2} and 2.7×10^6 cm^{-2}, respectively. In addition, they have attempted to expand the diameter of substrates produced by the process, and formed a nearly 3-inch substrate.

Yokoyama says that the next goal is to use their pore-assisted technology to try and fabricate even larger substrates.

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➤ M. Yokoyama *et al.* Appl. Phys. Express **17** 055502 (2024)

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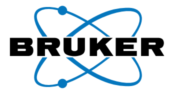

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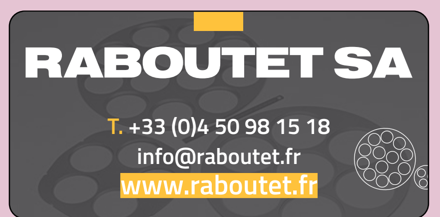

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