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VOLUME 31 ISSUE V 2025

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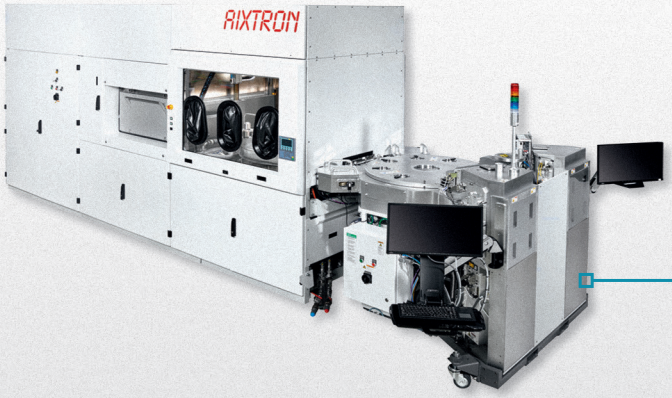

G10-SiC

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End Markets/Products:
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- 1st fully automated compact GaN MOCVD cluster designed 100 % for Si Power fabs
- Novel hardware solution for unmatched barrier uniformities and device yields

End Markets/Products:
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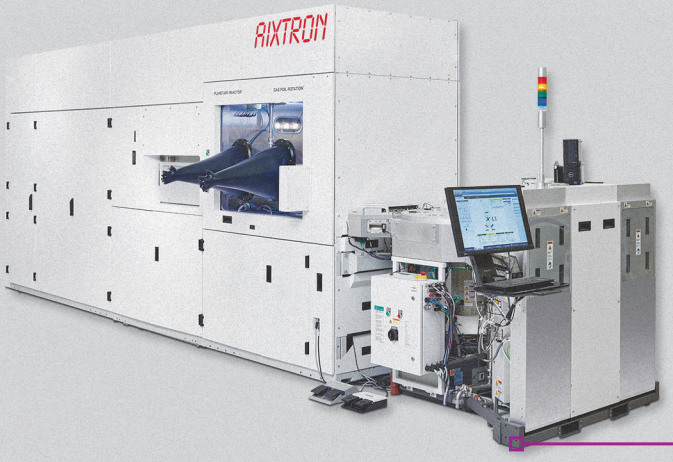

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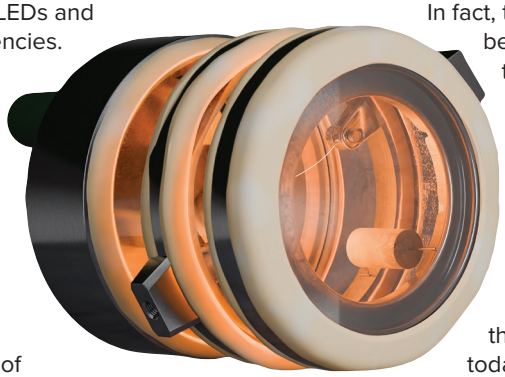
VIEWPOINT

BY RICHARD STEVENSON
EDITOR

A blast from the past

IN YOUR SPARE TIME, do you immerse yourself in technology developed in a bygone era? If so, maybe like me, you while away your hours trying to optimise the fidelity of your record player? Or maybe you help to run a steam train, or are fascinated by film-based cameras.

In our industry, it feels like it's a golden rule to never look back. Instead, we focus on the future, allured by promise of new materials and architectures that enable better-performing devices. This might involve bigger bandgaps that improve electrical conversion efficiencies, or device miniaturisation, such as smaller microLEDs and RF sources operating at higher frequencies.



Bucking this trend, and to good effect, is US start-up NS Nanotech (see p. 16). It's employing a novel approach to producing relatively powerful sources in the deep-UV that draw on technology developed for the TVs of yesteryear, which were based on cathode ray tubes.

This move comes against a backdrop of several decades of development of deep-UV LEDs, involving researchers within our community devoting a great deal of effort to increasing the efficiency and output power of these devices, and plunging new depths, in terms of wavelength. Gains in UV LED performance have been very hard to come by, due to a number of challenges, including realising reasonable values for doping and light extraction – and while today's devices are much better than their predecessors, they are pitiful when compared with their blue-emitting cousins.

Offering more power is Nanotech's alternative approach to producing solid-state sources emitting in the deep UV. Rather than using electroluminescence, it employs cathodoluminescence, with hot electrons emitted from a filament bombarding a wide bandgap semiconductor to generate UV light.

And what is this semiconductor that's whacked by countless electrons? While the obvious contender is AlN, NS Nanotech sees the situation differently, employing a material we are only just starting to hear much about, BN. It has an even bigger bandgap, with its band-edge emission delivering UV light at 215 nm, an ideal wavelength, as it avoids any concerns associated with causing harm to humanity.

In fact, the 500-microwatt sources that are being marketed by NS Nanotech are being touted as a great aid to all of us, by providing air disinfection in private cars, Ubers, ambulances and air ambulances.

By helping reduce the spread of diseases, this product can play a key role in increasing the health of nations – and it could also help to combat pandemics, an issue that matters, even if that's the last thing we want to think about today.

It's interesting to note that for those wanting higher powers than NS Nanotech can provide in this part of the deep UV – think owners of movie theatres wanting to prevent germ spreading – the leading solution is a lamp based on krypton chloride.

Tube-based technology is also key to providing high powers at very high frequencies, and in the minds of some audiophiles, is the best option for driving high-efficiency speakers. So, in some fields of engineering, the technologies of yesteryear have never gone away – and maybe that should be food for thought for our community.

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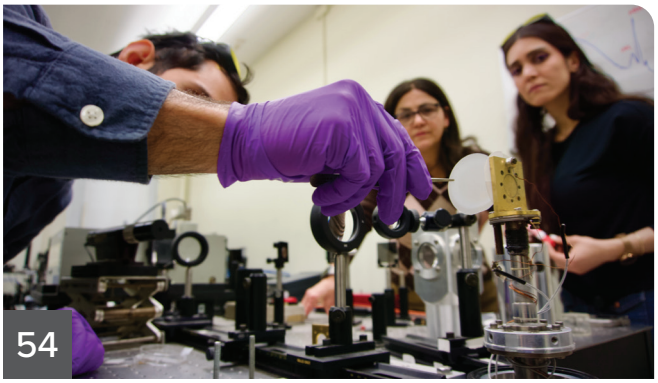

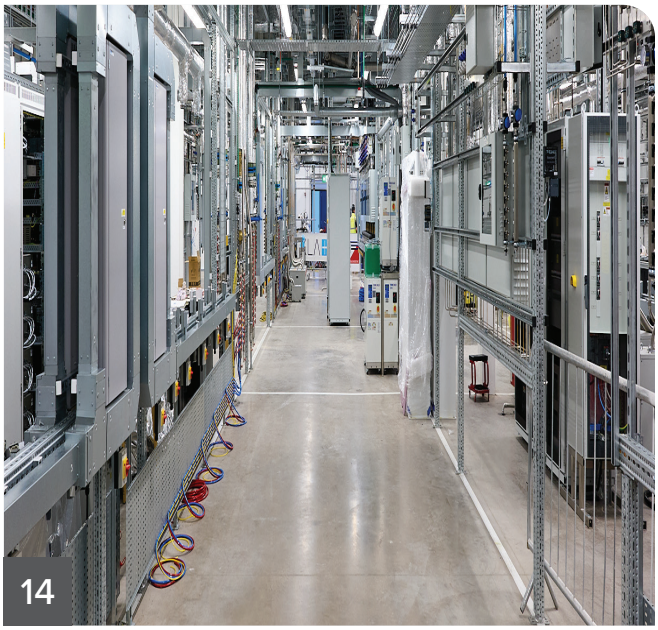

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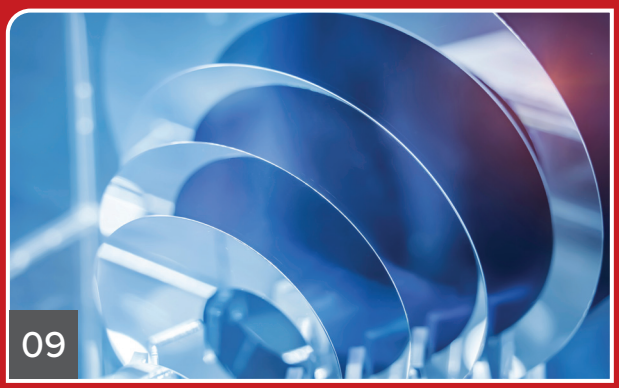

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Wolfspeed announces restructuring agreement

Proposed pre-packaged plan of reorganisation includes filing for Chapter 11

TROUBLED US SiC specialist Wolfspeed has entered into a Restructuring Support Agreement (RSA) with key lenders. These include holders of more than 97 percent of its senior secured notes; Renesas Electronics' wholly owned US subsidiary; and convertible debt holders holding more than 67 percent of the outstanding convertible notes.

The transactions envisioned by the RSA are expected to reduce the company's overall debt by around 70 percent, representing a reduction of approximately $4.6 billion, and reduce the company's annual total cash interest payments by approximately 60 percent.

As part of the RSA, the company intends to solicit approval of the pre-packaged plan of reorganisation and then file voluntary petitions for reorganisation under Chapter 11 of the US Bankruptcy Code in the near future. Wolfspeed says it expects to move through this process quickly and emerge by the end of Q3 2025.

"After evaluating potential options to strengthen our balance sheet and right-size our capital structure, we have decided to take this strategic step because we believe it will put Wolfspeed in the best position possible for the future," said Robert Feurle, Wolfspeed's CEO.

"Wolfspeed has tremendous core strengths and great potential. We are a global leader in SiC technology with an exceptional, purpose-built, fully automated 200 mm manufacturing footprint, delivering cutting-edge products for our customers."

"A stronger financial foundation will enable us to focus acutely on innovation in rapidly scaling verticals undergoing electrification where quality, durability and efficiency matter most."

Feurle continued, "As we move forward, we are grateful for the confidence and support of key lenders, who share our vision for the future and believe in our growth prospects. I also want to thank our incredibly talented team for their resilience and hard work, and our customers and partners for their ongoing support."

According to the transactions contemplated by the RSA, the company will receive $275 million of new financing in the form of second lien convertible notes, fully backstopped by certain of its existing convertible debt holders.

The RSA contemplates a paydown of its senior secured notes of $250 million at a rate of 109.875 percent, with certain modifications to reduce go-forward cash interest and minimum liquidity requirements. Another aspect of the RSA is an exchange of $5.2 billion of existing convertible notes and Renesas' existing loan for $500 million of new notes and 95 percent of the new common equity, subject to dilution from other equity issuances, with Renesas loan claims entitled to additional incremental consideration to the extent certain regulatory approvals are not obtained by an agreed upon deadline.

Pursuant to the transactions, existing equity will be cancelled, and the existing equity holders will receive their *pro rata* share of 3 percent or 5 percent of new common equity, subject to dilution from other equity issuances and potential reduction from certain events.

All other unsecured creditors are expected to be paid in the ordinary course of business.

Wolfspeed says it is continuing to operate and serve customers with SiC materials and devices throughout the process. The company plans to continue to pay vendors in the ordinary course of business for goods and services delivered throughout the restructuring process via an All-Trade Motion.

Vendors are expected to be unimpaired in the process. Wolfspeed also intends to file customary motions with the Bankruptcy Court to support ordinary-course operations including, but not limited to, continuing employee compensation and benefits programmes.

Researchers discover LED 'efficiency cliff'

University of Illinois team uncovers challenges in sub-micron LED performance

Researchers at the University of Illinois Urbana-Champaign (UIUC) have successfully fabricated InGaN blue LEDs down to 250 nm in size, a critical step for next-generation high-resolution displays and optical communications. However, their study, published in *Applied Physics Letters*, reveals a new challenge: a sharp 'efficiency cliff' when these LEDs are scaled to submicron dimensions.

The team, led by Can Bayram from the department of Electrical and Computer Engineering, who is director of the Innovative Compound semiconductoR LABoratory (ICORLAB), employed a top-down fabrication approach using electron-beam lithography on QST substrates.

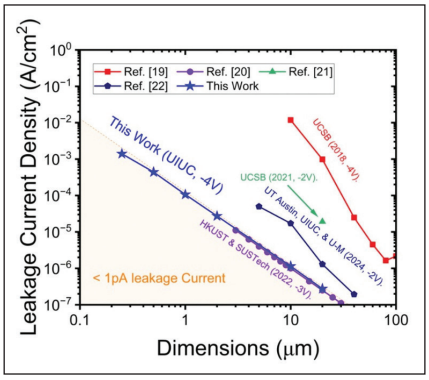
The resulting submicron LEDs, some as small as 250 nm by 250 nm, initially demonstrated promising electrical characteristics, including ideal forward voltage and remarkably low leakage current density. This suggested that the chemical treatments and passivation techniques were effective in recovering sidewall damage from the etching process.

Despite these positive indicators, the study found a dramatic decrease – approximately 70 percent – in peak external quantum efficiency (EQE) as the LEDs were scaled from 2 μm down to 250 nm. This 'efficiency cliff' is a surprising outcome, particularly as the EQE remained relatively stable for devices scaled from 20 μm down to 2 μm, according to Bayram.

"Our findings show that the conventional sidewall passivation methods, which work well for microLEDs, are not sufficient when we push the dimensions into the submicron realm," he explained. "The issue appears to be that as the LED mesa size becomes comparable to the distance carriers can diffuse laterally, the impact of the sidewalls and any associated non-radiative recombination becomes overwhelmingly dominant, even with current state-of-the-art passivation."

The research indicates that at these ultrasmall scales, the proportion of the LED's active region affected by sidewall defects significantly increases. While the team achieved good recovery of sidewall damage, evidenced by low leakage currents, the standard passivation (an atomic layer deposited bilayer of Al_2O_3 and SiO_2) could not sufficiently suppress surface recombination in these submicron devices.

This study underscores a critical hurdle for the practical implementation of top-down fabricated sub-micron LEDs, says Bayram. While the successful fabrication of 250 nm LEDs with good electricals is a promising starting point, overcoming the 'efficiency cliff' is paramount. "These results call for a fundamental rethinking of how we manage sidewall effects in these tiny light emitters," Bayram added. "Novel passivation strategies, potentially involving new materials or techniques to prevent lateral carrier diffusion, will be essential to unlock the full potential of sub-micron LEDs for future technologies."



Leakage current density compared with the literature. The device leakage current is low, around 1 pA at -5 V. This low, sidewall-limited leakage current is attributed to good passivation quality and negligible bulk leakage current.

A*STAR launches 200 mm SiC open R&D line

New initiatives and partnerships unveiled at SEMICON Southeast Asia 2025

SINGAPORE'S Agency for Science, Technology and Research (A*STAR) hosted the inaugural 'Innovate Together' event at SEMICON Southeast Asia 2025, while announcing the world's first industry-grade 200 mm SiC Open R&D Line.

"Singapore's semiconductor ecosystem is built on strong collaborations between public agencies, academia, and industry partners," said Yeo Yee Chia, deputy chief executive (Innovation & Enterprise) at A*STAR.

"The Innovate Together event exemplifies our commitment to fostering these partnerships and accelerating innovation to address industry challenges and capture new opportunities in the global semiconductor landscape."

At the heart of Innovate Together was the launch of the SiC Open R&D Line. Designed to enable joint SiC innovation between researchers and companies, the aim is for the facility to strengthen Singapore's capabilities in wide bandgap semiconductor research and address future demands for high-power applications.

In addition, A*STAR unveiled two other initiatives to strengthen Singapore's semiconductor research and innovation capabilities:

- Phase two of Lab-in-Fab, a 200 mm R&D and manufacturing line focused on piezoMEMS, involving partners STMicroelectronics, ULVAC, and the National University of Singapore. This will build on Singapore's strong R&D ecosystem to accelerate the development of new piezoelectric materials and devices.
- EDA Garage, an initiative that will provide local companies, especially start-ups and SMEs, with cost effective access to advanced electronic design automation tools. This will nurture local semiconductor companies and enable them to innovate faster and better.

To kickstart international collaborations in semiconductor training and R&D, A*STAR IME signed Memorandums of Understanding with key partners, including the Uzeltexsanoat Association, representing Uzbekistan's electronics sector, the Singapore Semiconductor Industry Association, the Indian Institute of Technology, Kharagpur, and the Fraunhofer Institute for Electronic Nano Systems ENAS.

These partnerships pave the way for internship programmes, joint research projects, and knowledge exchange through training and knowledge sharing activities.

At the sidelines of the SEMICON Southeast Asia 2025 event, A*STAR also formalised its partnerships with GlobalFoundries and Nearfield Instruments, to expand capabilities in advanced packaging and drive innovation in semiconductor metrology technologies.

Under an Memorandum of Understanding, GlobalFoundries will gain access to A*STAR's advanced R&D facilities, capabilities and technical support for technology development in advanced packaging and workforce skills enhancement.

The multi-year research collaboration between A*STAR IME and Nearfield Instruments will accelerate the development of advanced metrology solutions that enable efficient chip production.

The Innovate Together event featured expertise from other institutions on key technological areas that are important for the future of Singapore's semiconductor industry.

Speakers from A*STAR, National University of Singapore, Nanyang Technological University, Singapore, and the National Semiconductor Translation and Innovation Centre shared the latest insights on advanced packaging, photonics, MEMS, and millmetre-wave and beyond.

Renesas to abandon SiC production

Japanese giant halts SiC chip plans amid Chinese price war and Wolfspeed uncertainty

RENESAS is abandoning plans to produce SiC chips for EVs. according to *TrendForce*, citing a report by *Nikkei*.

This move by the Japanese semiconductor firm has apparently been prompted by slow growth in the EV market, coupled with a SiC chip supply glut driven by Chinese manufacturers. The decision is asociated with Renesas' SiC partner Wolfspeed, planning to file for Chapter 11 bankruptcy.

In July 2023, Renesas announced its entry to the power SiC market through a ten year partnership with Wolfspeed. The deal included a $2 billion deposit from Renasas to secure supply for both 150 mm and 200 mm SiC wafers.

Renesas had initially planned to begin manufacturing SiC power chips for EVs in early 2025 at its Takasaki plant in Gunma Prefecture. However, the company has since disbanded the SiC team at the facility, according to *Nikkei*. The latest research from *TrendForce* shows weakening demand in the automotive and industrial sectors and slow shipment growth for SiC substrates in 2024. Simultaneously, intensifying competition and sharp price declines have driven global revenue for *n*-type SiC substrates down 9 percent year-over-year to $1.04 billion.

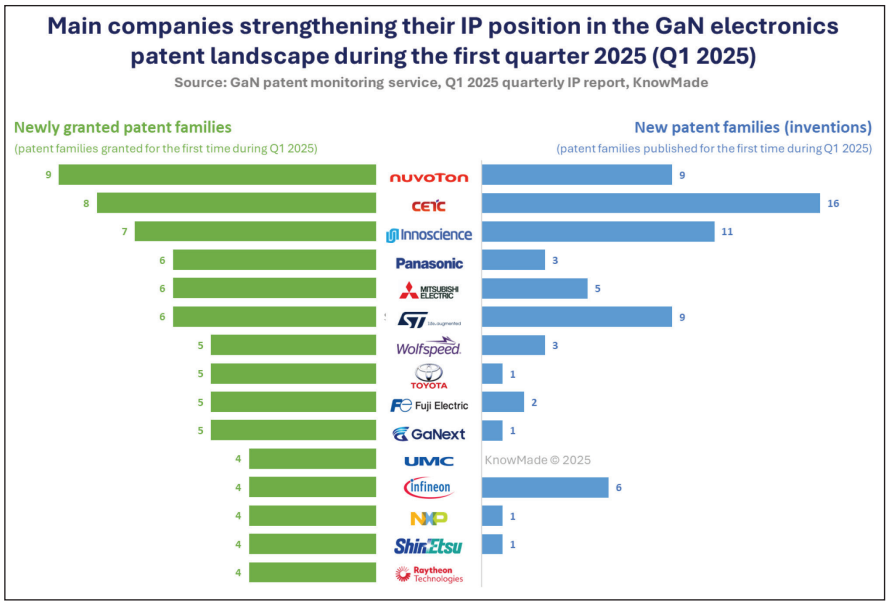
Chinese vendors TanKeBlue and SICC have risen to prominence, capturing 17.3 percent and 17.1 percent of the global market share, respectively. Price competition with Chinese rivals is expected to intensify over the medium-to-long term, making it more difficult for a late arrival like Renesas to generate profits from SiC chip production. *TrendForce* adds that while Renesas has reportedly decided to halt in-house production of SiC power chips, the company does not plan to exit the market entirely. Instead, it may continue to develop its own SiC designs while outsourcing manufacturing to foundries, then selling the finished products under its own brand.

GaN companies strengthen patent portfolios

KnowMade Q1 IP patent report shows companies are addressing critical aspects of GaN technology

KNOWMADE has published its Q1 2025 IP report on GaN electronics, highlighting robust patenting activity across both power and RF segments, amid on-going patent disputes between power GaN companies.

Recent patent filings emphasise critical aspects of power GaN technology such as gate design and packaging, resulting in sustained patent portfolio growth. Meanwhile, key RF market players keep expanding their IP activities in the RF GaN landscape, underlining the technology's role in next-generation wireless applications.



During the first quarter of 2025, a total of 540 new patent families were published, with Xidian University and major Chinese entities such as CETC and Innoscience leading the patent filings, followed by contributions from Nuvoton, STMicroelectronics, and Toshiba. Over 330 patent families were granted for the first time, notably reinforcing portfolios at Innoscience, STMicroelectronics, Infineon, Navitas, and EPC, alongside significant grants to Panasonic and TSMC. The quarter also saw more than 110 patents abandoned and over 70 patents expired, primarily from well-established patent holders including Wolfspeed, Infineon, and Fujitsu.

Approximately 10 IP collaborations (patent co-filings) were recorded, most partnerships formed between industry and academic organisations. For instance, Safran published a patent application with CNRS, CNAM and several universities in Paris, for an on-board aeronautical power circuit with active filtering. Also, Volkswagen cooperated with the University of Tennessee on GaN-based three-level active neutral point clamped power module designs, resulting in joint patent publications in Q1 2025.

Nearly 40 patent transactions took place this quarter, predominantly within China, such as the transfer of several RF GaN patents from Xidian University to Huawei and power module company Macmic Science & Technology's acquisition of a GaN device patent from UESTC.

Toshiba, Texas Instruments (TI), and Rohm each published more than six new inventions. In particular, Rohm introduced multiple innovations aimed at enhancing the reliability of normally-off GaN devices by leveraging *p*-GaN gate layer techniques and superlattice buffer structures. TI unveiled a novel gate structure incorporating a *p*-type poly-silicon layer to decouple parasitic capacitances and improve gate depletion behaviour, alongside trench-based substrate-to-source connections for GaN power devices and a HEMT design featuring a doped barrier to boost threshold voltage stability and drain current stability. Moreover, TI disclosed a packaging solution wherein a GaN FET is co-packaged with its driver for optimised half-bridge modules.

Sony, Sumitomo Electric, and Macom disclosed six, five, and four RF-focused inventions, respectively. While Sumitomo and Sony were focused on RF GaN device designs, Macom's patenting activity related to RF amplifier circuitry and advanced packaging techniques. Interestingly, Sumitomo focused on RF GaN-on-SiC devices fabricated on nitrogen-polarity GaN epitaxial structures.

Academic research also made a significant contribution on this topic with UCSB publishing an invention that improves the linearity of deep-recess GaN MIS-HEMTs through corrugation of N-polar structures. MONDE Wireless, a UCSB spin-off, also mentioned N-polar GaN HEMTs grown on miscut substrates in another Q1-2025 patent publication.

New entrants to the GaN electronics IP landscape were predominantly Chinese, with LED manufacturer Anhui GaN Semiconductor filing several epiwafer patent applications for both power and RF uses, and battery manufacturer CATL submitting its first GaN-related invention targeting battery management systems. In the US, Tesla entered the arena with a packaged IC featuring enhanced power surge heat dissipation, and Soctera, a Cornell University spin-off, proposed a GaN device structure using an AlN back barrier layer and an *in-situ* two-step passivation process to mitigate current collapse.

NICT-Sony collaboration makes laser breakthrough

Practical surface-emitting laser for 1500 nm communications uses quantum dots as gain medium

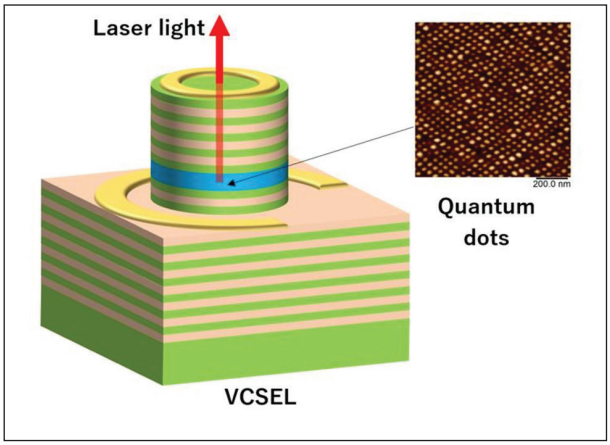
JAPAN'S National Institute of Information and Communications Technology (NICT), in collaboration with Sony Semiconductor, has developed what is claims is the world's first practical surface-emitting laser for 1550 nm communications that employs quantum dots (QD) as the optical gain medium.

The results of this research *Electrically pumped laser oscillation of C-band InAs quantum dot vertical-cavity surface-emitting lasers on InP(311)B substrate* were published in *Optics Express*, in March year.

This innovation not only facilitates the miniaturisation and reduced power consumption of light sources in optical fibre communications systems but also offers potential cost reductions through mass production and enhanced output via integration, according to the researchers.

NICT's role was to develop the reflective semiconductor multi-layer fabrication and quantum-dot crystal growth technology using MBE. Sony undertook the device design for the entire VCSEL structure and device process technology.

Fabricating a VCSEL requires growing a highly reflective semiconductor multi-layer film known as a distributed Bragg reflector to enhance light intensity; however, fabricating DBRs that operate at 1550 nm has been challenging, because the combination of materials that can be grown is limited. In this study, the NICT team developed a technology that can precisely grow DBRs by strictly controlling the ratio of materials in the crystal growth and realised a semiconductor DBR with a reflectivity exceeding 99 percent, even at 1550 nm.



In addition, strain-compensation techniques were applied to VCSEL production to accurately cancel the internal crystal strain (strain generated within the material) that occurs around the quantum dots, thereby significantly increasing the density of the quantum dots and improving the light-emitting performance.

Sony contributed a device design and fabrication process that enables highly efficient current injection employing a tunnel junction. VCSELs emit light perpendicular to the wafer surface; therefore, even if quantum dots emit light, conventional electrode placement obstructs light extraction. Sony addressed this by implementing a tunnel junction structure that permits efficient current flow while facilitating light extraction employing a precise device process.

Through the integration of these two technologies, the team succeeded in lasing VCSELs using quantum dots at 1550 nm as a light-emitting material with a small current of 13 mA (low threshold). Furthermore, polarisation fluctuations were eliminated, resulting in a stable output.

In the future, the researchers hope to develop the quantum-dot-based VCSEL technology further to enhance the capacity and reduce power consumption in optical fibre communication systems beyond 5G era.

GlobalFoundries boosts 're-shoring' investment

Company commits to a further $3 billion on next-generation GaN tech, packaging innovation, and silicon photonics

GLOBALFOUNDRIES says it is working with the Trump Administration, with support from tech companies Apple, SpaceX, AMD, Qualcomm, NXP and GM, to onshore critical components of the supply chain with a total $16 billion investment in expanding chip manufacturing and packaging across its facilities in New York and Vermont.

This latest announcement builds on the company's existing US expansion plans of more than more than $13 billion funding to both advance manufacturing of 200 mm GaN-on-silicon semiconductors at its facility in Essex Junction, Vermont; and for its recently launched New York Advanced Packaging and Photonics Center. GF is committing an additional $3 billion, which includes advanced research and development initiatives focused on next-generation GaN technologies, packaging innovation, and silicon photonics.

The company says its investment is a strategic response to the explosive growth in AI, which is accelerating demand for next-generation semiconductors designed for power efficiency and high-bandwidth performance across data centres, communications infrastructure and AI-enabled devices.

Tim Breen, CEO of GlobalFoundries said: "The AI revolution is driving strong, durable demand for GF's technologies that enable tomorrow's data centres – including GF's leading silicon photonics, as well as GaN for power applications. Meanwhile at the edge, GF's proprietary FDX technology is uniquely positioned to support AI functionality with low power consumption. With all these technologies and more manufactured right here in the US, GF is proud to play its part in accelerating America's semiconductor leadership."

"GlobalFoundries investment is a great example of the return of United States manufacturing for critical semiconductors," said US Secretary of Commerce, Howard Lutnick. "President Trump has made it a fundamental objective to bring semiconductor manufacturing home to America. Our partnership with GlobalFoundries will secure US semiconductor foundry capacity and technology capabilities for future generations."

"GlobalFoundries has supplied semiconductors for Apple products since 2010 and we're excited to see them expand right here in the United States. These chips are an essential part of Apple products like iPhone, and they're a powerful example of American manufacturing leadership," said Tim Cook, Apple's CEO

Gwynne Shotwell, president and COO at SpaceX said: "Advanced semiconductors are critical to the advanced satellite capabilities, which SpaceX has been pioneering for over two decades. We are excited by the expansion of GlobalFoundries' manufacturing base right here in the US, which is core to Starlink's growth and our commitment to manufacturing in the US, as well as our mission to deliver high-speed internet access to millions of people around the world."

"As a strategic supplier of Qualcomm, GlobalFoundries shares our vision for strengthening US chip production capacity. This commitment from GlobalFoundries will help secure a resilient semiconductor supply chain to support the next wave of US technology innovation, especially in areas vital to enabling power efficient computing, connectivity, and edge intelligence," said Cristiano Amon, president and CEO of Qualcomm Incorporated.

"This collaboration allows us to scale efficiently, expand production in the US and continue delivering for our customers. It's a strong step forward in building a resilient, high-performing semiconductor supply chain in the United States, " said Kurt Sievers, CEO of NXP Semiconductors.

"Semiconductors are critical to the future of vehicles, and their importance will only grow. GlobalFoundries' investment supports our work to secure a reliable, US-based chip supply – essential for delivering the safety, infotainment and features our customers expect," said Mark Reuss, president of General Motors.

Solutions for Compound **semiconductor passivation**

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SiN
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RIBER's **CPS passivation tools**

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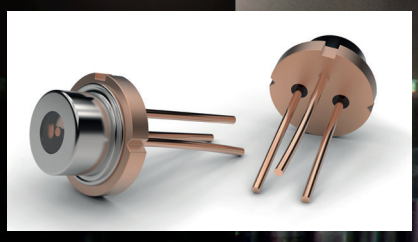

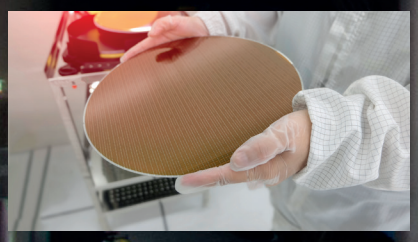

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KLA: Expanding within the CS cluster

Equipped with a demonstration lab capable of accommodating more than 100 modules, KLA's new, purpose-built facility should spur further growth of its deposition and etch tool businesses

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

RIGHT NOW, the South Wales compound semiconductor cluster is thriving. Behind those positive vibes is Vishay's investment of SiC manufacturing technology at its Newport fab, the completion of the Centre for Integrative Semiconductor Materials at Swansea University, and most recently, the opening of a tremendous new facility for the development and production of KLA Corporation's deposition and etch equipment.

Opening on 22 May to much fanfare, KLA's £138 million facility sits at the heart of the cluster, in an industrial area on the outskirts of Newport that's also home to IQE and the CS Catapult.

To mark this key day in KLA's history, the company took the opportunity to show 100 or so VIPs around its purpose-built 237,000 ft^2 three-story facility.

Accommodating up to 750 employees, this brand-new building features: more than 25,000 ft^2 of cleanroom space for R&D; more than 35,000 ft^2 for bespoke manufacturing; plenty of office space, with lots of natural light; and a canteen and a gym for all its staff.

During the opening ceremony, KLA's VP Product Marketing, SPTS Products, Dave Thomas, spoke exclusively to *Compound Semiconductor*, detailing plenty of sound reasoning behind the relocation, the trends that the company is seeing within the compound semiconductor industry, and how the new facility and the management at KLA will help to continue a ramp in sales of the company's etch and deposition tools.

Local firm, global brand

The roots of the etch and deposition division of KLA can be traced back to the days of ElectroTech, which in 1984 established a subsidiary, Special Research Systems, in Bristol – just the other side of the Severn estuary from the CS cluster. Over the years, this company re-located to South Wales, with a couple of local moves supporting expansion of the business.

In the last 15 years this venture has thrived, with sales of the SPTS etch and deposition tools rocketing from around US$50 million to US$500 million. Supporting this phenomenal growth is the acquisition by KLA in 2019, which has driven a doubling of revenue from this division and a commensurate increase in headcount. This expansion has driven demand for a bigger facility, with space not only for the expanded workforce, but also for aiding the development and demonstration of tools and processes.

Thomas believes that the acquisition by KLA came at just the right time for SPTS. "When you're going from a few hundred million towards a billion, you have to start thinking differently. You need to act more corporately, have much better control over your internal processes, and certainly be better connected with your customer base at multiple levels."

As well as offering all this, incorporating SPTS into the KLA fold has provided the finance and bold vision for building a purpose-built facility. Without doubt, this would be located in the compound semiconductor cluster, highly valued for a number of reasons.

According to Thomas, one crucial benefit of remaining within the cluster is that it enhances joint development with local companies and universities.

"There are programmes that we have running with Swansea University, where

➤ In the basement of KLA's new facility is a 'sub-fab', providing the necessary infrastructure for supporting tool assembly and the running of tools to aid and attract customers. Credit: Matt Lincoln

they're helping us to understand the link between the device and the wafer process," remarked Thomas. "Just recently, we're developing an endpoint system for silicon carbide trench etching, and we're trying to figure out how tolerant is the device to the trench characteristics."

Thomas argues that another benefit of operating within the cluster is that is helps with discussions with local and national government, because those officials have now grasped a basic understand of the importance of the compound semiconductor industry.

From MEMS to compounds

Sales of equipment to the MEMS industry provided initial success in the etch and deposition tool market. "We were the first licensees of the Bosch process," explained Thomas, adding that back in 1995, they worked with this German powerhouse to develop the deep-silicon-etching Bosch process.

Today, the MEMS sector is still valued by KLA, accounting for around 10-15 percent of sales of its etch and deposition tools. However, greater revenue is coming from the compound semiconductor industry. Here, involvement dates back several decades, with success underpinned by efforts to understand the specific characteristics of all the main materials.

Expansion into the compound semiconductor sector began with GaAs, which has some key differences to silicon from a processing perspective.

However, while it is more difficult to etch GaAs than silicon, it's still easier than InP, according to Thomas: "You've got a very heavy metal, indium, with a very light element, phosphorus. When you come to etch it, it's very easy to etch one in preference to the other, and create a rough surface. You need to move to high-temperature etching to liberate both materials."

KLA also has capabilities in wide bandgap materials, particularly SiC and GaN. "Silicon carbide is very difficult to etch because it's so tough. You have to really hit it hard," said Thomas, who explained that a markedly different approach is required for GaN, which is easily damaged. "These subtleties, they're part of our DNA now, and we understand them."

Armed with all this hard-won expertise, KLA's deposition and etch tools are winning sales in all the major compound semiconductor markets.

In the RF market, KLA's process equipment is employed for the production of various devices, including those based on GaAs, InP and GaN on both silicon and SiC.

"The RF market is in a state of recovery," said Thomas, who is expecting growth to continue over the next few years.

In the power semiconductor sector, there has been huge growth over the last few years, driven by SiC devices for electric vehicles and infrastructure. However, recently, there has been some 'softening', according to Thomas, who remarked that the company is also active in the GaN market. "We work with pretty much all customers you can think of in the GaN power space and the SiC space."

Another key sector is photonics. "This is the exciting one for me right now," revealed Thomas, who explained that makers of lasers for optical communication are enjoying tremendous growth, and there's also the promise of co-packaged optics.

For those in the silicon industry, advanced packaging is synonymous with flip-chip bumping. Technologies like TMSC's CoWoS, that unite memory and logic with interposers, have become well-established.

"The next step in that progression is to bring photonics onto that package," argued Thomas, who elaborated by explaining that progress hinges on the addition of InP or GaAs lasers onto the silicon-centric packages.

"It's such a clash of cultures, because you've got four and six-inch wafers versus twelve-inch wafers," remarked Thomas.

Along with his colleagues, Thomas is trying to bring the two camps together, drawing on KLA's strong relationships between both the makers of VCSELs and edge-emitting lasers, and the big five in silicon that employ hybrid bonding. "The marriage of the two is not going to be easy, but we're right in the middle of that and we can help."

The demo lab

One of the assets of KLA that should help in this endeavour is its new demonstration lab, able to house over 100 process modules.

"We don't really often sell anything without demonstration first," revealed Thomas, who explained that to win orders it's imperative to either prove that KLA's tools are superior to the incumbents, or are capable of being employed for a new manufacturing process. In both cases, customers tend to send wafers to KLA, which runs them through its tools and reports the data.

"We collaborate a lot during that process," said Thomas, revealing that this can involve plenty of calls, and trips to the customer's offices. "Better still, they come here, and they sit with us in those demo rooms – and they watch, they learn, they advise, and we work together." Typically, in this preferred *modus operandi*, engineers from the chipmaker will spend a week at KLA.

As well as demonstrating processes to customers, the demo room is used for R&D – this accounts for about 40 percent of activity. Efforts on this front include refining processes to make them more manufacturable, and the development of new hardware.

Managing the move

Today there are only a handful of tools in the demo lab, and office space in the new facility is populated very lightly. Over the next six-to-nine months, groups will move from one side of Newport to the other to set-up in the new facility. As this involves decommissioning and recommissioning, while meeting customer needs, it will be an exciting and challenging time. However, there's no doubt that these efforts will be rewarded.

"We will have a really engaged workforce and a really engaged set of customers who want to come here and work with us," commented Thomas, who expects that the new facility will also act as a magnet to recruiting highly capable employees.

"When I have a vacancy for a product manager, I'd like to see 10 CVs from Swansea and Cardiff universities, and local schools. I want to take local talent because, to me, if we can continue to build locally from here, I think that's a really good story for us."

Retro-tech revolutionises the deep UV

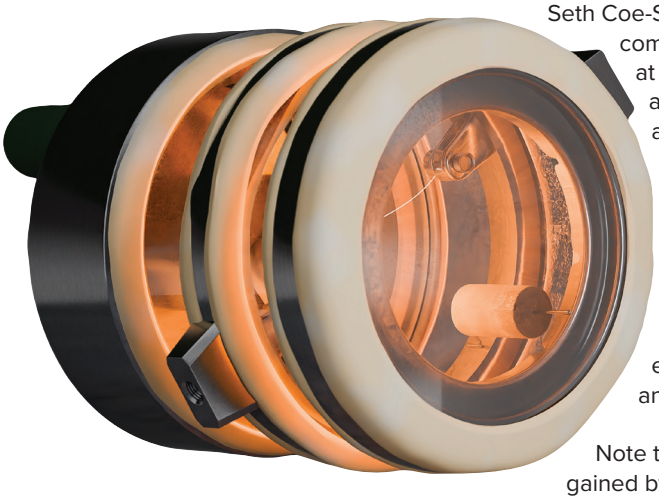
Compact sources of deep-UV emission from NS Nanotech are providing air purification through cathodoluminescence of boron nitride

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WHEN IT COMES to device design, our industry is quite insular. We focus on improving performance by optimising epitaxy or the architecture of our chips. But at times we might be missing a trick, and would benefit from approaches involving more out-of-the-box thinking.

Doing just that with considerable success is the Michigan-based start-up NS Nanotech. Drawing on cathode-ray tube technology that lies at the very heart of the televisions of yesteryear, it has just released an improved version of its cathodoluminescence-based 215 nm source that's a compelling candidate for air purification in relatively confined public spaces.

The NS Nanotech source goes deeper than AlGaN-based UV LEDs – they have been under development for decades, with developers striving to improve the efficiency and output, so that those emitters could be deployed in various applications, including curing and the purification of air, water and surfaces.



➤ Emission at 215 nm results from the bombardment of electrons into a BN powder.

Motivation for the development of deep-UV LEDs is the addressing of many weaknesses of the incumbent solution, a gas-discharge lamp that is fragile, bulky, and is some cases contains mercury, which is of great concern to humanity's health. However, while the power produced by deep-UV LEDs continues to increase, it's not that high, limiting success.

As well as offering more power, the technology from NS Nanotech produces emission at a preferable wavelength. While no light in the UV is perfectly safe to humans, the most damaging to the skin and eyes is in the range 240 nm to 280 nm.

"It's right where mercury bulbs are, where all the UVC LEDs are," says NS Nanotech CEO and co-founder Seth Coe-Sullivan. "The lowest commercial LED available is at 235, which isn't quite as bad as 240, but it's awful close."

Coe-Sullivan points out that the only two commercial sources beneath that harmful band are krypton chloride bulbs, with an emission peak at 222 nm, and NS Nanotech's source.

Note that there is little to be gained by going below 200 nm, as light in this spectral domain is absorb ed by oxygen, hampering its transmission.

Superior successor

Back in October 2024, NS Nanotech introduced its first far-UVC ShortWaveLight 215 nm emitter; and recently, it has unveiled a second-generation variant, with an output of 500 µW, 60 percent higher than its predecessor.

"Compared to any far-UVC LEDs on the planet, this is massively powerful, certainly the most powerful semiconductor device at this colour," says Coe-Sullivan.

Both generations of far-UVC ShortWaveLight 215 nm emitter are vacuum tube devices that feature semiconductor emitters. These products employ a filament, providing hot electrons that are accelerated to semiconducting material, which emits UV light via cathodoluminescence. The increase in the output power of the successor comes from optimising the vacuum tube before pinch off.

AlN versus BN

The obvious candidate material for providing cathodoluminescence is AlN, a key semiconductor for producing deep-UV LEDs. But NS Nanotech uses BN, as this has better bandgap emission when quantum wells are not employed.

"If you just buy bulk boron nitride powder, you'll get essentially zero emission at 215 nanometres," warns Coe-Sullivan. "You'll get all defect emission, which is far lower energy than the bandgap."

To avoid this fate, the team at NS Nanotech employs a refined

process for producing BN powders, involving licensing technology from Japan. The BN bulk powder is coated on a disc about a square centimetre in size, with cathodoluminescence providing 215 nm emission of the company's products, which are roughly the size of a golf ball.

The primary application for NS Nanotech's technology is reducing the spread of diseases in small, confined spaces. This approach to improving public health is known to succeed, thanks to the pioneering work of Niels Ryberg Finsen, who received the 1903 Nobel Prize for Medicine for studies into the use of deep-UV emission to disable micro-organisms.

Interest in using deep-UV sources to kill viruses rocketed during the pandemic, but has fallen away, with many wanting to simply move on from those difficult times. However, while this view is understandable, failing to learn lessons from the Covid-19 outbreak leaves humanity vulnerable to the next pandemic, which could take many forms.
Speculating on possibilities, Coe-Sullivan remarks: "Is it a measles outbreak in Texas? Is it the bird flu crossing over to humans? Is it something we can't name?"

He has no doubt that the likelihood of another pandemic is only going to increase year by year, pointing out that the planet's population is increasing, many are living closer to animals, and germ-sharing is on an upward curve.

One significant opportunity for passing on germs occurs in confined spaces, such as those found in cars. It is here that NS Nanotech is hoping to make a difference, promoting its products for deployment in private cars, Ubers, ambulances and air ambulances.

➤ The primary application for far-UVC ShortWaveLight 215 nm products made by NS Nanotech is to sterilise the air in vehicles.

"Vibration testing has been really key," claims Coe-Sullivan, revealing that one of the company's 215 nm sources has been fitted in a pick-up truck that's been driven on dirt roads for last six months. Encouragingly, this field test has not produced any degradation to the deep-UV product.

In movie theatres, there's also much interest in using sources in the 200 nm-230 nm band to kill bacteria. Here, more power is needed, so lamps based on krypton chloride that emit around 30 milliwatts are used.

"Krypton chlorine is a great product," says Coe-Sullivan. "But if you're in a car, Krypton chlorine is the wrong product, and our product is the right product."

What's also clear is that while the white-emitting filament bulb now belongs in the museum, other vacuum-based technologies are going strong, and will have a role to play in society for many more years.

CMOS: Not just for silicon

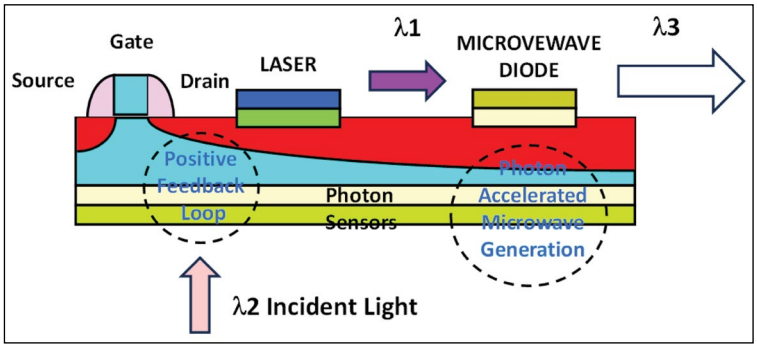
While CMOS may be synonymous with the manufacture of silicon ICs, it's a versatile process can also be applied to the production of photonic and microwave circuits employing compound semiconductors

BY JAMES PAN FROM NORTHROP GRUMMAN

SILICON ICs – invented in 1950s – are used in almost everything. Better known for their deployment in smartphones and computers, they are also integral to the operation of automobiles, washing machines, air conditioners, vacuum cleaners and so on. In all these cases, the ICs operate in total darkness, because silicon has an indirect bandgap. Due to this characteristic, silicon can absorb light, but it cannot emit it.

In our daily life, electrons and light are intertwined. We use electrons to generate light and other forms of electromagnetic radiation, such as microwaves. And while we might think of photons when we think about lasers and LEDs, they are electron devices – as are radar and lidar.

Now we need to start applying the principle of working with electrons and photons, which are intertwined, in ICs. Development is already underway, as compound semiconductors, such as GaAs, InP, and other III-V and II-VI compounds, are now used with silicon. Consider, for example, microwave photonic CMOS, which includes III-V or II-VI materials for lasers or millimetre-wave diodes, in the CMOS drain region, through a process called 'selective epitaxy'.



➤ Figure 1. Microwave photonic CMOS and image sensors. Positive feedback loops convert light to light currents. Photon-accelerated microwave generation produces modulated light wave and millimetre wave signals.

It's possible that these ideas might strike you as a little odd. I'm sure you have heard of the acronym CMOS – its full name 'complementary metal-oxide semiconductor' – and you'll know that it's a process employed to make billions of silicon ICs. But it's quite possible that this is the extent of your knowledge. And, to be fair to you, why should you know any more than this, given that many will believe that CMOS is not of any relevance to the compound semiconductor industry.

Well, I understand your position – but you are in danger of falling behind the times. Change is now afoot, thanks in part to our work at Northrop Grumman, a leader of lasers, millimetre-wave devices, and ASICs (Application Specific Integrated Circuits). We are developing a CMOS process for light-emitting structures and microwave circuits. It's a revolutionary breakthrough that will enable the integration of both compound semiconductors and silicon for almost 'all products' in the $500 billion CMOS industry, which is growing rapidly.

Our efforts are not the first to unite silicon and the compounds in ICs. Long gone are the days when silicon photonics is a new entity, having been pioneered by companies such as IBM and Intel, with products forming a small part of the IC industry. Today silicon photonics has already entered ULSI (Ultra Large-Scale Integration) markets, a point well-illustrated by the delivery of a webinar last August by Global Foundry's Anthony Yu, who gave a presentation entitled *Bringing Silicon Photonic Technology to the Forefront*). Within this development there's microwave photonic CMOS, involving modern processors that include hundreds of billions or trillions of CMOS transistors.

Based on such activities, a new trend is emerging – most, or even all of these many billions of CMOS transistors are no longer going to be fabricated only in silicon. Instead, they will incorporate GaAs, InP, or other compound semiconductors used in lasers and LEDs.

Behind this revolution is the move in modern societies to replace wireless tools with non-wireless tools, a migration observed in the uptake of smartphones, and changes to the connectivity of computers. In this particular case, the advantages of implementing compound semiconductors with silicon are wireless ULSI, and eliminating heating of the copper wires, and delays associated with their resistance and capacitance. There's the promise of replacing billions of copper wires in ULSI with wireless photonic CMOS technologies.

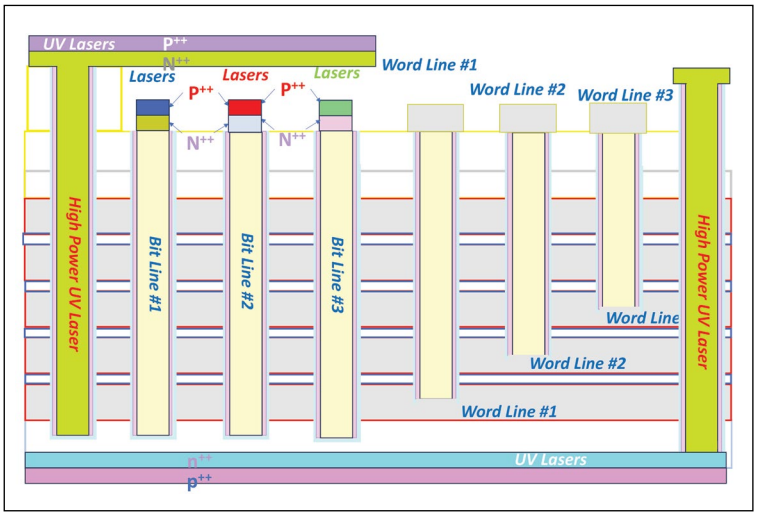
You may be wondering how III-Vs are introduced using a CMOS process. One illustrative example is the addition of GaAs in the CMOS silicon drain region, using either low-temperature selective CVD or selective epitaxy. For the former, the CVD tool includes an *in-situ* chamber in ultra-high vacuum, where native oxides on silicon are sputtered and etched, prior to sending the wafer to the CVD chamber for GaAs epitaxy. Note that all these processes proceed under high vacuum.

As GaAs is deposited right before the silicide process, in the BEOL (Back End of the Line), there are no contamination concerns, enabling the use of silicon lines (see Figure 1 for an illustration of the process integration of photonic CMOS).

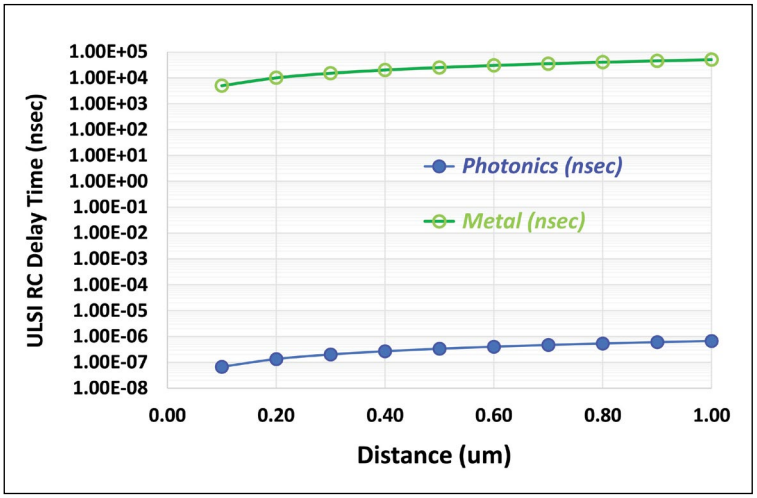
Thanks to the introduction of III-Vs, the era of microwave photonic CMOS is within our grasp. For this technology, options for the optical source include GaAs LEDs, emitting in the 800 nm to 900 nm range, threshold-less tunnel lasers on silicon, and microwave-generating devices. Note that microwave photonic CMOS can outperform traditional laser diodes, due to improved thermal reliability, higher external quantum efficiencies, and superior lasing powers.

To produce microwave photonic CMOS, an ultra-low-resistance threshold-less tunnel laser or LED is crafted in the drain region; and in either the well, channel or below the drain region, narrow-bandgap photon sensors or avalanche photodiodes are added, made from SiGe or other compound narrow bandgap materials. In addition, microwave diodes, made from silicon, SiGe, or other compound semiconductors, are added in the drain region. Note that the MOSFET, lasers, microwave diodes, and photon sensors are fabricated as one integral transistor.

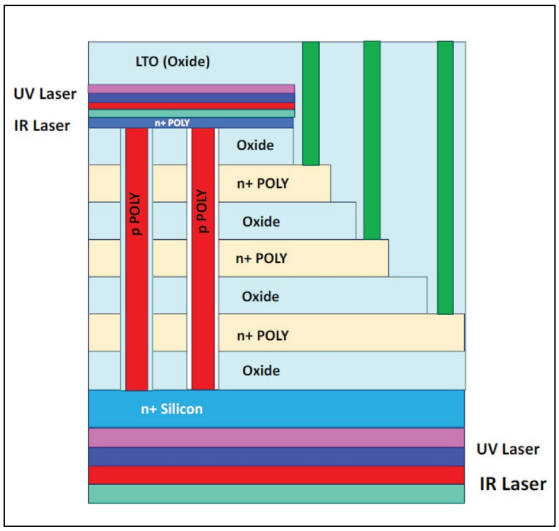
Alongside the optical sources, dielectric micro-optical waveguides are transferred that are suitable for sub-1 nm CMOS technology nodes. The dimensions of the micro-optical waveguides can be less than 100-300 nm, with guided optical signals confined with total reflection, despite the wavelength being longer than the width of the waveguide. For the sub-1 nm nodes, channel length is typically 5-20 nm, but the 'width' of the CMOS can be in the range of hundreds of nanometres, or even a few microns.



➤ Figure 2. Ultra-High-Speed Microwave Photonic Vertical NAND FLASH.



➤ Figure 3. Wireless ULSI with Photonic CMOS – significant reduction of RC delays and heat.



➤ Figure 4. An alternative method of fabricating Ultra-High Speed Microwave Photonic Vertical NAND FLASH (Vertical NAND FLASH, which has replaced NOR FLASH.

There is no doubt that these new forms of CMOS have great potential. One of their greatest assets is that the laser microwave CMOS process is 100 percent compatible with existing CMOS fabrication, and there is no threat of cross contamination. Another exciting opportunity is the introduction of far more sophisticated nonlinear optical computing. However, there are challenges – compared with photonics computing, which is already available and implemented, microwave computing needs advanced knowledge, and the development of micro-antenna, microwave filters, multiplexers, and designs.

I'm not saying that applying CMOS to the compounds is easy. But the rewards justify the endeavour.

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FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP

SOI Industry Consortium

SMART MANUFACTURING

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HRL's GaN: from innovation to qualification

Maintaining the tradition of being 'first' in technology innovation, HRL's latest T3L GaN technology delivers a world-leading high-frequency performance with a process that's manufacturable, stable, predictable and reliable

BY SATYAKI GANGULY, F. ERDEM ARKUN, ANDREA ARIAS-PURDUE, DAVE FANNING, ANDY FU, DMITRY VEKSLER, DAN DENNINGHOFF AND ANDREA CORRION FROM HRL LABORATORIES

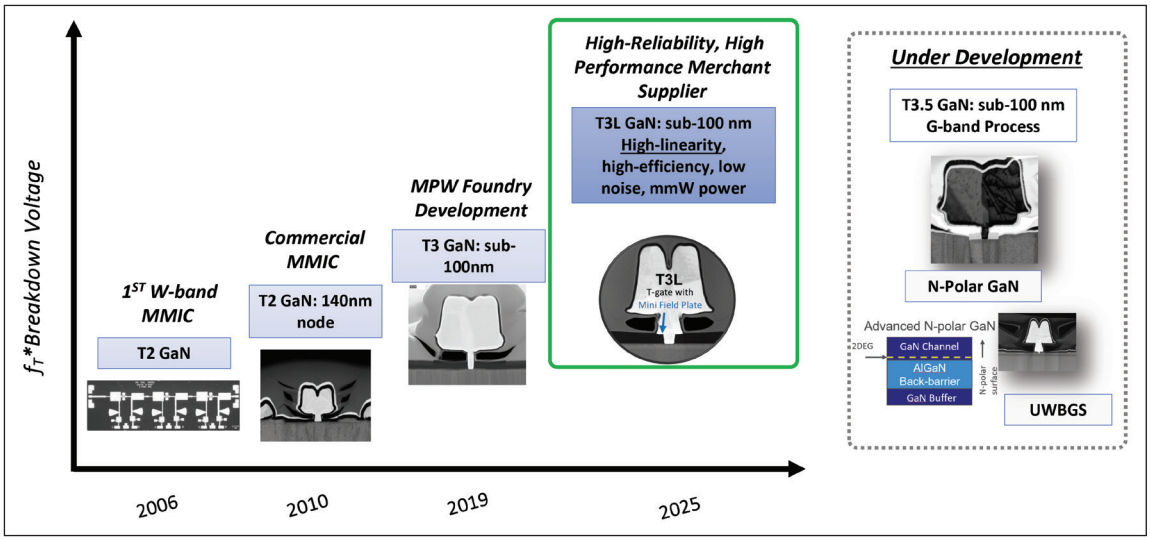
BY OFFERING increases in power, efficiency and bandwidth over other semiconductor technologies, RF GaN devices are continuing to make a substantial impact in commercial and defence applications. But to ensure the future success of this class of device, its progress must not grind to a halt. Due to the proliferation and complexity of RF signals, the electromagnetic environment is increasingly crowded, driving urgent demand for GaN technologies operating at higher frequencies – and in particular, the millimetre-wave range that spans 30 GHz to 300 GHz.

Meeting this need is not trivial. It requires a rethinking of GaN materials and fabrication approaches, including a move away from many of the standard features incorporated into lower-frequency technologies, such as standard annealed ohmic contacts, large field-plates to manage electric fields, and the standard AlGaN/GaN HEMT epitaxial structure.

Unfortunately, those that take on the challenge of moving to higher frequencies also come up against a number of trade-offs. To give just one example, when decreasing the gate length to sub-100-nm dimensions and eliminating field plates to enable high-frequency operation, peak electric fields in the device increase, impeding reliability. What's needed are out-of-the box, innovative solutions.

At HRL Laboratories, LLC, we have a long history of exceling on this front. By redefining the boundaries of what's possible today, we invent solutions to tomorrow's problems. Employing an ownership model that prioritises purpose over profit, we invest in ambitious ideas and take strategic risks on projects that significantly advance the state of the art, pursuing paths that others might overlook. This culture is reflected in our legacy of groundbreaking work on high-frequency GaN.

For many years, our portfolio of millimetre-wave GaN devices and circuits has featured cutting-edge innovations that break performance trade-offs and push the boundaries for high-frequency GaN. One of our latest technology nodes – T3L GaN – builds upon our previous successes, while adding innovations that ensure high linearity and reliability, such as a graded epitaxial structure and a gate mini-field-plate. In recent times, we have also invested tremendous effort into GaN technology maturation, qualification, model development, and external foundry services. The result is that today we are



➤ Figure 1: The evolution of HRL's millimeter-wave GaN foundry offerings over time.

offering GaN with world-leading high-frequency performance – such as T3L – to external designers via reliable, mature, open foundry offerings.

HRL GaN odyssey

We have been investing in GaN materials, transistors, and circuit development since the late 1990s, and we have a long history of 'firsts' for RF GaN MMICs, particularly in high-frequency technology demonstrations.

Our early investments associated with in-house epitaxial growth capability enabled innovations such as n^+ GaN ohmic contact regrowth by MBE, and vertically scaled layer structures necessary for high-frequency performance.

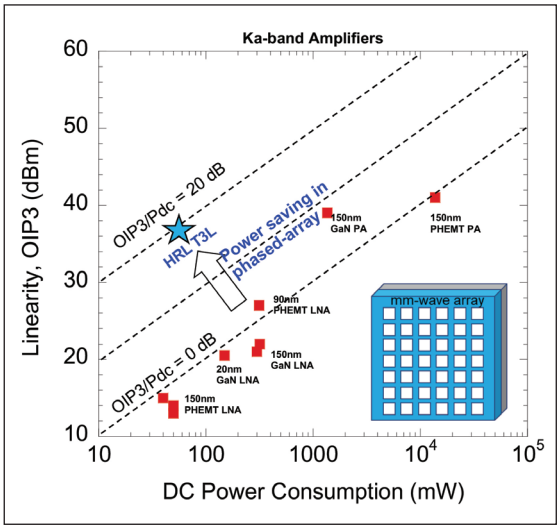
As we continue to develop and advance our GaN technology, we draw on our extensive expertise in high-frequency MMIC design and fabrication. Our background includes a strong track record as a provider of high-frequency GaAs and InP-based circuits.

Key milestones in GaN RF technology include unveiling the first Ka-band GaN MMIC power amplifier at the 2004 IEEE International Microwave Symposium, the first W-band GaN MMIC power amplifier at the 2006 International Electron Devices Meeting, and the first G-band GaN MMIC at the 2014 IEEE Symposium on Compound Semiconductor Integrated Circuits.

Over the years, our high-frequency GaN technology nodes – which have utilised 'T'-gates, as opposed to gamma- or field-plate gates – have targeted progressively higher-frequency operation (see Figure 1). Our T3L node is built upon our 40 nm-gate T3 node, but features key modifications to improve linearity and dynamic range – this results in an enviable combination of outstanding linearity, noise, output power, and efficiency for millimetre-wave applications. Much of this pioneering work in high-frequency GaN was made possible through financial support from the US government, with programmes such as DARPA WBGS, DARPA NEXT, and DARPA DREAM, among others.

HRL T3L GaN technology

Our T3L GaN HEMT technology was initially developed under DARPA's Dynamic Range-enhanced Electronics and Materials (DREaM) programme, which had the goal of developing new designs and materials for RF transistors with an unprecedented dynamic range in millimetre-wave systems. To succeed in this endeavour, we combined a graded-channel AlGaN/GaN epitaxial structure, providing precise control of transistor transconductance, with a scaled 40-nm T-gate and mini-field-plate. One of the key merits of the graded-channel epi and mini-field-plate is a



➤ Figure 2. For Ka-band amplifiers linearity versus DC power consumption with typical linearity FOM of around 0 dB has been shown. Star represents the fiducial point illustrating HRL's T3L GaN linearity that sets HRL apart. Adapted from J. -S. Moon *et al*. International Microwave Symposium - IMS 2022, pp. 302-304, 2022.

distribution of the electric field across the device's active area that improves linearity and reduces signal distortion – that's particularly beneficial for high-frequency applications, where RF signal integrity and linearity are crucial. Meanwhile, the short gate length supports a high cut-off frequency (f_T) of 170 GHz, and a maximum oscillation frequency (f_{MAX}) of 347 GHz.

Drawing on these strengths, our GaN MMICs that incorporate the T3L transistor technology and on-chip pre-matching networks have demonstrated a world-record peak power-added efficiency of 45 percent at 94 GHz, and a corresponding power density of more than 2 W mm^{-1}. These two characteristics are key performance metrics for efficient power amplifiers. The power-added efficiency of our GaN MMICs at 30 GHz is world-beating, with values as high as 70 percent.

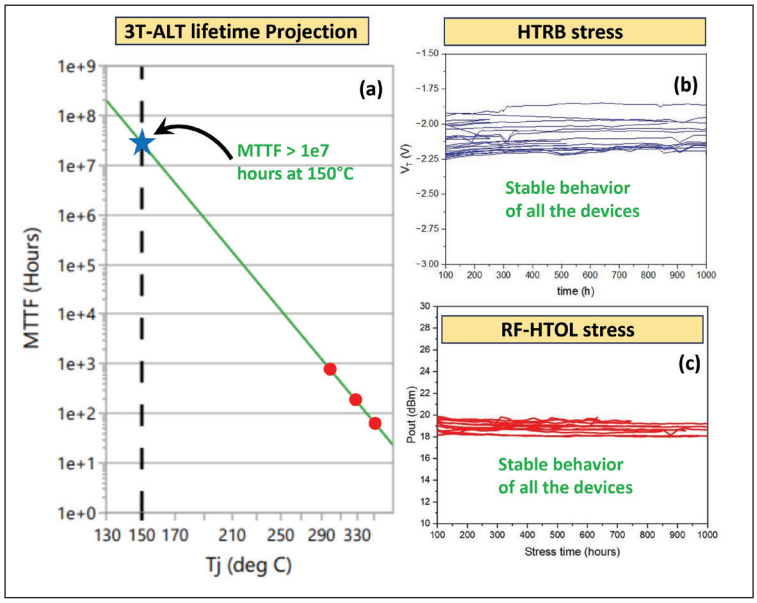
Modern-day phased arrays and high-dynamic-range RF front ends require amplifiers with high linearity. Traditionally, this linearity requirement has been fulfilled with low-noise amplifiers, operating with a higher DC power consumption, or power amplifiers that are run at a reduced power-added efficiency and power density.

Neither of these options is preferable. Industry is reluctant to meet linearity requirements by taking a hit in efficiency or consuming more power, especially as payload power needs to be allocated to increased bandwidth and newer software-defined features. Moreover, many airborne platforms are size, weight and power (SWaP) constrained.

What's urgently needed are devices with a high linearity-to-power-consumption figure-of-merit. In this regard, a common figure-of-merit for benchmarking is the ratio of the Output Third-Order Intercept Point (OIP3) (a measure of linearity) to DC power consumption. Judged against this metric, known for short as OIP3/PDC, our T3L GaN technology that employs key design and process breakthroughs delivers a record 17.5 dB at 30 GHz. That's a jaw-dropping improvement, more than 30 times better than the best previous Ka-band low-noise amplifiers featuring GaAs pHEMTs and AlGaN/GaN HEMTs (see Figure 2).

Key features of our T3L GaN technology include two-level metal interconnects with 5 µm plated airbridges, 50 Ω/sq. thin-film resistors, 300 fF mm^{-2} metal insulator metal capacitors, and 50 µm SiC with through-substrate vias and backside metal.

Our T3L GaN is well-positioned for success in a range of cutting-edge applications within the millimetre-wave domain. Deploying our technology in 5G and beyond wireless communication enables faster data transmission and improved signal quality; in high-resolution radar systems, T3L GaN provides better target detection and imaging capabilities; in electronic warfare and defence systems, T3L GaN enables robust performance in challenging environments; and last but not least, in satellite communications T3L GaN ensures reliable, efficient signal transmission over long distances.



➤ Figure 3. Three-temperature accelerated life (3T-ALT), high-temperature reverse-bias (HTRB), and RF high-temperature operating life (RF-HTOL) tests of HRL's T3L GaN. (a) Median-time-to-failure (MTTF) versus junction temperature for T3L GaN discrete devices under DC-ALT stress. Red data points represent the extracted MTTF values at the stress temperatures, while the green solid line is the fit and extrapolation as described in the text. The star represents the fiducial point to illustrate the predicted MTTF lifetime at the junction temperature, Tj, of 150 °C, of more than 1 x 10^7 hours. (b) Threshold voltage of discrete devices during HTRB stress and (c) RF output power (Pout) during HTOL stress, both showing excellent stability up to at least 1000 hours.

T3L GaN technology qualification

Recently, we have invested heavily in the qualification and maturation of our RF GaN technology, to meet the ever-growing demand and requirements of key strategic customers. Lifetime assessment is the first step towards meeting such expectations.

The first inception of our T3L GaN on the DARPA DREaM programme demonstrated the tremendous potential of our technology. Since then, by devoting much effort to technology maturation and qualification, we have been led to implement several minor proprietary changes to the epitaxial structure and fabrication processes, to further improve yield, manufacturability, and reliability.

To understand the lifetime of our first-in-class sub-100-nm GaN HEMTs, we have undertaken temperature-accelerated lifetime testing on our 4 x 37.5 µm T3L GaN discrete transistors with a dissipated power of around 4 W mm^{-1} and junction temperatures ranging from 300°C to 380°C (results are shown in Figure 3). Note that, to drive devices to failure, we have intentionally employed

stress temperatures that are far higher than the recommended operating condition, which typically ranges from 150°C to 225°C.

For this study, we defined the failure criteria as a 20 percent degradation in device on-resistance from its initial value. To determine values for the median-time-to-fail (MTTF) and lifetime, we analysed the failure time distribution with an Arrhenius temperature-accelerated lifetime model, lognormal statistics, and maximum likelihood estimation.

Based on this approach, we find that despite having one of the shortest gate lengths in the GaN industry, our T3L device lifetime is no shorter than 100 years at a junction temperature of 150°C. This is a MTTF benchmark that other GaN manufacturers typically strive for.

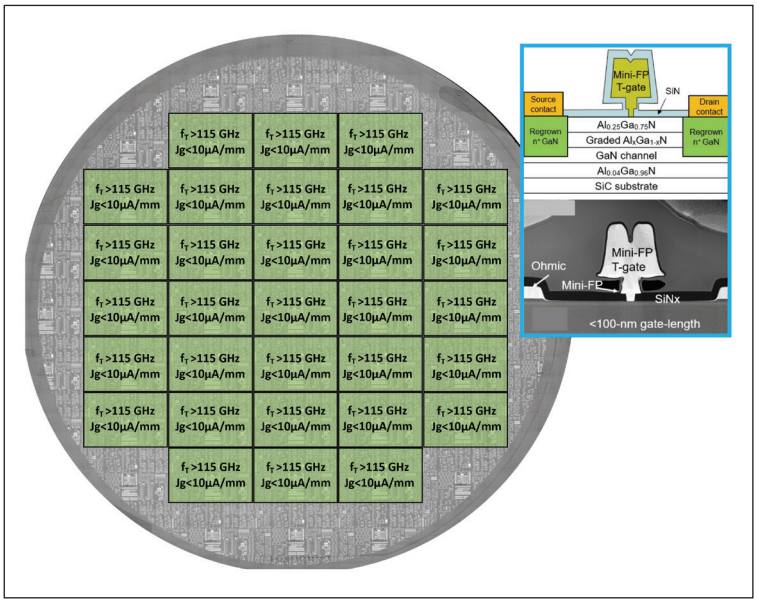
In addition to temperature-accelerated life testing, we have also performed off-state high temperature reverse-bias (HTRB) and on-state RF high temperature operating life (RF-HTOL) reliability testing on T3L devices (see Figure 3). For HTRB testing at an ambient temperature of 150°C, we stressed a group of discrete transistors from multiple wafers using a gate bias of -7 V and a drain bias of 35 V, which corresponds to 250 percent of the operating quiescent voltage (14 V). Under these conditions, we evaluated the stability of various device parameters, such as the threshold voltage.

Applying these conditions for HTRB testing, we determined that device performance is stable up to at least 1000 hours. This is a key reliability benchmark.

On-state qualification of our T3L MMICs through RF-HTOL stress also showed excellent stability, with minimal shift in critical RF-paraments after 1000 hours of stressing.

Successfully passing 1,000 hours of HTRB and RF-HTOL testing, in addition to hitting the state-of-the-art MTTF benchmark, serves as a testament to our stable, predictable, and reliable GaN T3L process.

Note that our GaN manufacturing process aligns with a remark made by one of the fathers of statistical process control, the US engineer Harold Dodge, who is famous for the phrase 'you cannot inspect quality into a product'. The implication of his statement is that it's critical to build quality and reliability into the product during the manufacturing process. Abiding by this philosophy, we do not implement any additional burn-in or screening when choosing devices for reliability testing. Instead, all our reliability results come from devices randomly picked across multiple wafers after fabrication.



➤ Figure 4. Wafer map of a typical T3L GaN (gate length less than 100 nm, source-to drain of 900 nm) showing uniform peak f_T at a V_{DS} of 5 V and gate leakage current density measured at V_{DS} = 8 V and V_{GS} = -5 V. Schematic cross section and the corresponding scanning electron microscopy image of a representative T3L GaN transistor taken from such a wafer is shown in the inset.

According to a T3L GaN wafer map of peak f_T and gate leakage current, tested on in-line process control monitors, there is excellent uniformity associated with our T3L GaN process fabricated on a 100 mm SiC wafer (see Figure 4, which has an inset that shows a schematic cross-section of a W-band capable T3L GaN transistor, as well as a corresponding scanning electron microscopy image).

Technology maturation and foundry service

We are the first fab (ISO 9001 certified) to develop and offer a sub-100 nm GaN MMIC process technology through our foundry services. With US government support, in 2019 we launched an open commercial multi-project-wafer (MPW) foundry service for our 40 nm GaN-on-SiC T3 technology, and since 2021 we have offered quarterly MPW runs. To-date, we have sold 86 MPW tiles to 30 unique customers. Our foundry services include process design kits (PDKs) in both ADS and AWR, secure

Thanks to the maturation of our sub-100 nm GaN processes, we have seen increasing demand, especially for applications in the V/W-bands. Customers are encouraged to engage with our open foundry for GaN PDK and device model access and support for low-to-moderate volume production

management of customers' design verification, wafer microfabrication, RF probing, and the delivery of singulated MMICs.

To continue to advance our T3L technology node, this year we are launching a T3L GaN MPW service, and adding advanced interconnect features, such as copper pillars for flip-chip compatibility.

Historically, our GaN foundry interests have been balanced across research institutions, companies in the aerospace and defence sector, and commercial private-sector entities. Thanks to the maturation of our sub-100 nm GaN processes, we have seen increasing demand, especially for applications in the V/W-bands. Customers are encouraged to engage with our open foundry for GaN PDK and device model access and support for low-to-moderate volume production.

Beyond T3L GaN

In addition to our T3L RF-GaN technologies, we continue to innovate, motivated by the goal of pushing the boundaries of future technologies that will be transformative for the warfighter. One such innovation is N-Polar GaN, a technology we are exploring for its potential to deliver higher power. N-Polar GaN is showing promising capabilities compared with traditional GaN, but it is still advancing through the maturity stages, supported by early government investments in both academia and industry.

We are also making strides in the Ultra-Wide Bandgap Semiconductors (UWBGS) programme that's funded by DARPA. This initiative focuses on developing key processes for realising next-generation devices, including high-efficiency UVC LEDs, laser diodes, high-power RF transistors, and power-conversion electronics.

Through these efforts, we continue to position ourselves at the forefront of technological advancements that will shape the future of military and commercial applications.

By combining world-record efficiency, output power, linearity, and noise figures with excellent device reliability, stability, and uniformity, our current GaN technology is uniquely positioned to address rapidly evolving needs in the millimetre-wave RF application space. On top of that, our heavy investment in maturation and capacity to support customer engagements is ensuring a bright future for our GaN, and helping to continue to shape the future of GaN for the broader community.

HRL Laboratories conducts contract research and development with support from various US government agencies, including DARPA, US Air Force, OUSD, and ONR. The organisation gratefully acknowledges this vital support in driving the advancement of cutting-edge technologies and scientific innovation.

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Empowering power devices

Novel material combinations and innovative architectures take GaN and Ga_2O_3 power devices closer to fulfilling their full potential

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

Look up the physical properties of a range of semiconducting materials and it's easy to understand why SiC and GaN are more attractive than silicon, and why Ga_2O_3 holds so much promise. But getting transistors and diodes made from these wide and ultra-wide bandgap materials to get close to fulfilling their true potential, rather than just outperforming silicon, is far from easy. Success demands improvements to the design of these devices, along with the processes for producing them.

Thanks to the efforts of researchers from all over the world, steady progress is being made on improving the performance of many devices made from many of the key materials that have a bandgap that's wider than that of silicon. Gains are seen in the pages of journals, as well as in the presentations delivered at many conferences, including this year's CS Mantech. At that gathering, held in New Orleans from 19 to 22 May, a number of speakers showcased advances in power electronic devices, with papers including those reporting gains from pairing GaN with tungsten and with NiO, and promising architectures, such as GaN diodes with nitrogen-ion implantation and Ga_2O_3 finFETs.

GaN-on-tungsten diodes

Within the power electronics sector of our industry, SiC generates the most significant revenue. However, sales have not soared as fast as many have been hoping for, and from a commercial perspective, GaN is receiving a great deal of attention.

GaN HEMTs have already established a 'killer' application, due to their deployment in fast chargers for mobile devices. Sales of this class of transistor involve the lateral variant, which is relatively straightforward to produce. But a switch to a vertical geometry promises substantial gains in performance, alongside reduced chip costs that come from miniaturisation.

For lower-voltage products, the compromises that come from a lateral geometry are less troublesome, with HEMTs with a 100 V rating having a typical resistance of around 3 $m\Omega\ cm^{-2}$. However, when this geometry is used for 650 V devices, the chip size increases, and resistance can be five times as high. For this voltage rating, vertical devices have much appeal, being around one-tenth of the size of their

lateral counterparts and having a resistance of just a few mΩ cm^{-2}.

At CS Mantech, a collaboration led by researchers at FBH Berlin, and involving engineers from the Fraunhofer Institute for Laser Technology and EV Group, presented their latest efforts in developing vertical GaN power devices with blocking voltages of 1 kV or more. This requirement demands *n*-type drift layers more than 10 μm-thick, which can lead to a number of issues when growth is undertaken on a foreign substrate. Due to lattice and thermal mismatch, there can be an increase in the threading dislocation density and leakage current, as well as mechanical strain and fragility.

At last year's CS Mantech, this team reported steps they had taken to address these concerns, describing the wafer bow reduction through laser stealth scribing of the sapphire substrate.

Now they have built on this previous success, removing the electrically and thermally insulating sapphire substrate from the GaN membrane electronic devices, and bonding them to tungsten.

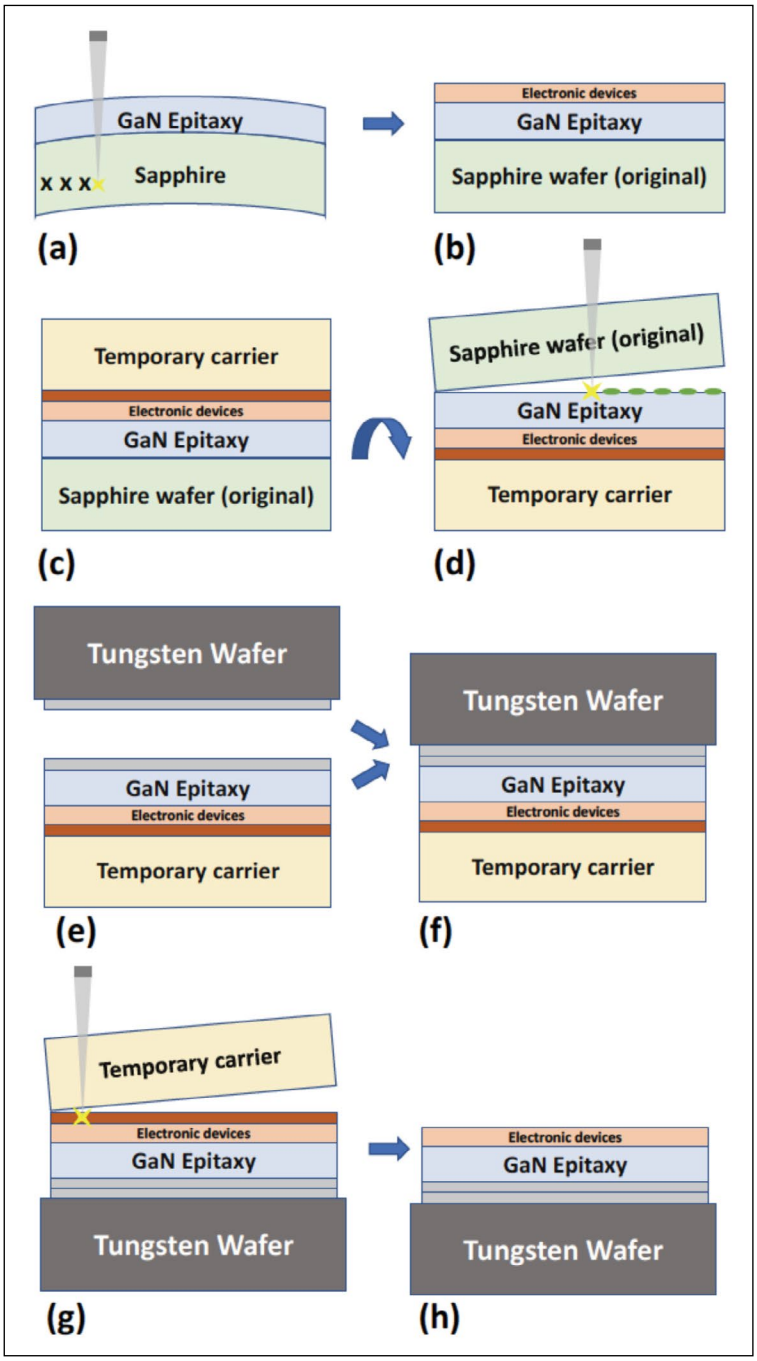
Speaking to *Compound Semiconductor* on behalf of the collaboration, Enrico Brusaterra from FBH Berlin explained that the team could have employed any conductive metal for their work. "However, we chose tungsten, as it has a thermal expansion coefficient almost identical to GaN."

Brusaterra believes that tungsten substrates offer good levels of availability and affordability. "Although more than 80 percent of the tungsten market is dominated by one country, the material itself, with a global production of about 80,000 metric tonnes, is not rare enough to be a concern." And when it comes to cost, a 4-inch tungsten wafer tends to retail for less than $100 dollars – so less than one-tenth of the price of a 2-inch GaN wafer.

To produce their GaN-on-tungsten *p-n* diodes, the team loaded a 650 μm-thick sapphire substrate into an MOCVD reactor and deposited a 2.2 μm-thick sacrificial layer, followed by a 2.4 μm-thick highly conductive cathode layer and a 10 μm-thick drift layer. Regrowth of *p*-type layers with a total thickness of 530 nm, and the *in-situ* activation of the dopants, took place in another MOCVD reactor.

Stealth laser scribing reduced wafer bow from around 300 μm to just 20 μm, prior to defining the mesa structure with lithography and etching, the addition of contacts, passivation, and etching 200 μm trenches around the chips to facilitate early chip singulation.

Before laser-lift off, the team polished the backside of its sapphire substrate, slashing roughness from around 1 μm to less than 50 nm to improve the laser lift-off process. After attaching a temporary carrier to the wafer, ultrashort pulses from a 266 nm laser



➤ Figure 1. To produce vertical GaN-on-tungsten *p-n* diodes, the German collaboration led by FBH Berlin employs a wafer back-end process that involves: (a) epitaxial wafer bow reduction, (b) front-end electronic device manufacturing, (c) temporary sapphire carrier bonding, (d) laser lift-off of the GaN epitaxy membrane from the sapphire substrate, (e) the addition of GaN backside N-face ohmic contacts and bonding metal deposition, (f) GaN membrane and tungsten wafer metal bonding, (g) temporary carrier removal, and (h) the formation of the GaN membrane on the tungsten substrate.

provided GaN decomposition, allowing removal of sapphire, prior to the addition of a tungsten wafer and the extraction of the temporary carrier (see Figure 1).

Thanks to the full conduction path through the tungsten substrate, on-resistance fell after the transfer process from 3.4 mΩ cm^{-2} to 1.7 mΩ cm^{-2}. The researchers state that the reverse characteristics are not significantly affected by the transfer process, with only a minor increase in reverse bias current at voltages of more than 400 V. The average breakdown before membrane transfer is 1015 ± 47 V, and after the full process it's 988 ± 57 V. Following substrate removal and membrane transfer, the reverse bias current at 1000 V increases from around 0.35 mA cm^{-2} to 0.75 mA cm^{-2}.

Brusaterra says that one of the drawbacks of the team's process, when it comes to commercialisation, is that it's a single-wafer process with limited throughput. "Tungsten dicing is also time consuming on large scale."

Giving GaN a NiO gate

Conventional GaN HEMTs, fabricated with growth along the (0001) axis, are described as III-polar devices. This architecture has a number of merits, most notably the creation of a two-dimensional electron gas (2DEG) at the interface of GaN and AlN, thanks to advantageous band offsets and piezoelectric and spontaneous polarisation. But even more favourable are the N-polar structures, realised through growth along the (000$\bar{1}$) direction, that allow AlGaN to act as a back barrier below the GaN channel, and ensure better control of the 2DEG, due to improved carrier confinement. What's more, with N-polar devices, it's easier to form an ohmic contact to the 2DEG, there's enhanced carrier density, thanks to a deeper quantum well, and channel mobility is higher, due to supressed alloy disorder scattering.

Unfortunately, it's not trivial to enjoy all of these benefits. It is challenging to grow high-quality N-polar GaN on all the common substrates, as compared with III-polar growth, there's a tendency for higher dislocation densities, greater surface roughness, and increased impurity incorporation. Another issue is that N-polar surfaces are chemically reactive, making interface quality and surface treatment challenging, with threats of traps and instability.

Taking on these challenges – and advancing N-polar HEMTs with GaN/AlN devices that feature the addition of a *p*-type NiO gate stack that ensures a positive threshold voltage – is a team from Bristol University that detailed their success at this year's CS Mantech.

Discussing this work with *Compound Semiconductor*, team spokesman Chengzhi Zhang explained that their device is orientated towards power applications, but it could also be deployed in some RF applications.

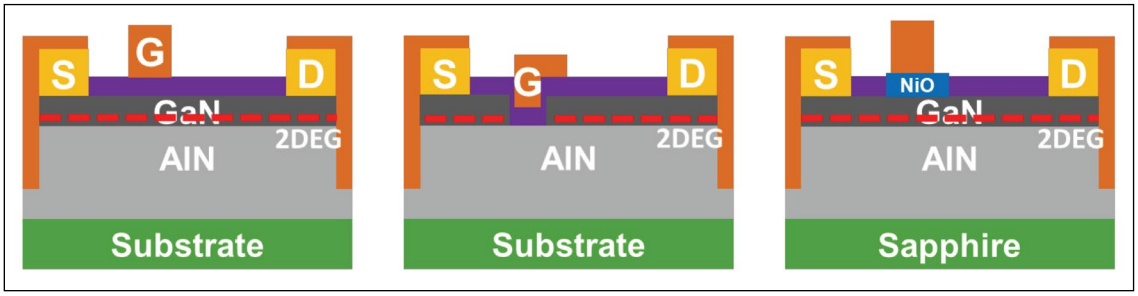
According to Zhang, the team's N-polar GaN/AlN platform enables high 2DEG channel densities, due to strong polarisation fields. "This enables high current and output power densities."

Thanks to the AlN back barrier, their HEMT benefits from enhanced channel confinement that trims buffer trapping and vertical leakage, and ultimately offers a pathway to solving reliability issues and current collapse. "These are all crucial for power electronics applications," remarks Zhang.

He points out that the use of a *p*-type NiO_x gate stack layer enhances gate control over the channel and enables normally-off (enhancement-mode) operation, which is very desirable for power switching applications. "The high breakdown field and excellent thermal conductivity of AlN also make it suitable for high-efficiency power conversion."

The attraction of using NiO is that it's naturally *p*-type, with excess oxygen creating Ni^{3+} vacancies that introduce hole conduction. Due to this, *p*-NiO is a compelling candidate for replacing *p*-GaN in HEMT gate stacks. With *p*-NiO, there's the promise of a simpler and lower-temperature synthesis process, a higher hole concentration and a work function that's comparable to *p*-GaN.

To evaluate their N-polar HEMTs with a *p*-NiO gate, the team used an N-polar GaN/AlN wafer to co-fabricate these devices, along with trench MOSFETs and MOS-HEMTs (see Figure 2). Fabricating trench MOSFETs from this epiwafer, which features a 460 nm N-polar AlN layer and a 5.4 nm GaN channel, involved using an inductively coupled plasma to etch the GaN channel and part of the AlN layer in selected regions. For all forms of HEMT, electron-beam evaporation provided the ohmic contact. Plasma-enhanced CVD added layers of SiN,



➤ Figure 2. Researchers at Bristol University have compared the electrical characteristics of (a) *p*-NiO gated HEMT (b) trench MOSFET and (c) MOS-HEMT.

and magnetron sputtering with a NiO target added a 30 nm-thick layer of NiO.

Electrical characterisation of all three forms of HEMT have shown that for the MOS-HEMT, it's not possible to realise pinch-off at even -25 V, despite the close proximity of the gate electrode to the surface 2DEG channel. Note that more negative voltages are prohibited, due to the onset of leakage currents through the gate dielectric. The team have attributed this behaviour to the large conduction band and polarisation offset at the GaN/AlN interface that confines the 2DEG to the channel and impairs depletion. Compounding this issue is the lower conduction band offset between SiN and N-polar GaN that limits the effective voltage range.

With the trench MOSFET, channel current is low over a large voltage range – or, to put it another way, the device fails to turn on. This is attributed to a low background carrier density in the AlN back barrier layer, with the Fermi level remaining below the conduction band and no channel forming.

The transfer curve for the N-polar HEMTs with a *p*-NiO gate (see Figure 3) shows that *p*-NiO plays an important role in channel control, with a threshold voltage of +1.24 V. The on-off ratio is 10^7, the subthreshold swing is 175 mV dec^{-1}, maximum transconductance 18 mS mm^{-1}, and the maximum saturation output current density 50 mA mm^{-1}.

Breakdown measurements reveal that these structures can withstand 0.8-1.0 MV cm^{-1}, leading the team to claim that N-polar GaN/AlN shows strong potential as a material platform for power electronics.

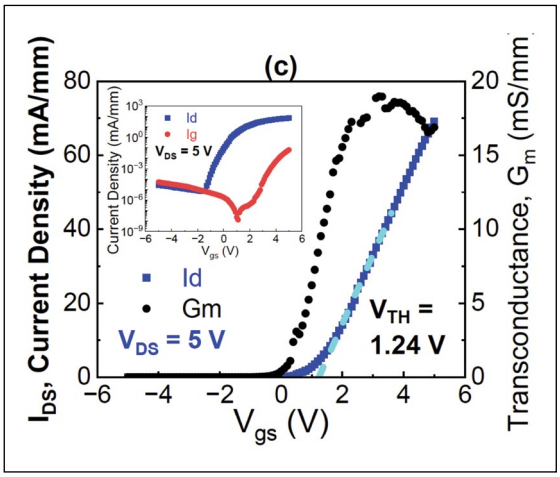
For the N-polar HEMTs with a *p*-NiO gate, Zhang and co-workers fabricated about 70 devices, with around 50 FETs working normally. "The cause of failure for the remaining devices is still under investigation."

He says that other goals for the team are to: achieve higher breakdown, by including electric field management techniques adapted from III-polar devices; to optimise growth conditions to achieve higher mobility; and to optimise device fabrication processes, to improve channel mobility and further enhance stability.

3.3 kV planar GaN diodes

Another partnership that is working to improve the performance of high-voltage GaN power devices is that led by the US Naval Research Laboratory, and supported by researchers from the University of Florida, Amentum and Sandia National Laboratories.

This team has been investigating the robustness of vertical devices, which are rapidly maturing, thanks to the widespread availability of 50 mm free-standing GaN substrates and imminent 100 mm availability. However, before these devices can enjoy significant commercial success, there's a need for detailed investigations of their lifetime and reliability under stress, as the more common lateral structures have very different degradation mechanisms. Studies on vertical studies should include the impact of ion-implanted termination of high-voltage devices, as this relies in impact-induced damage, which may be altered by high operating temperatures or stress.



➤ Figure 3. Bristol University's N-polar AlN/GaN HEMTs with a *p*-NiO gate show encouraging transfer characteristics.

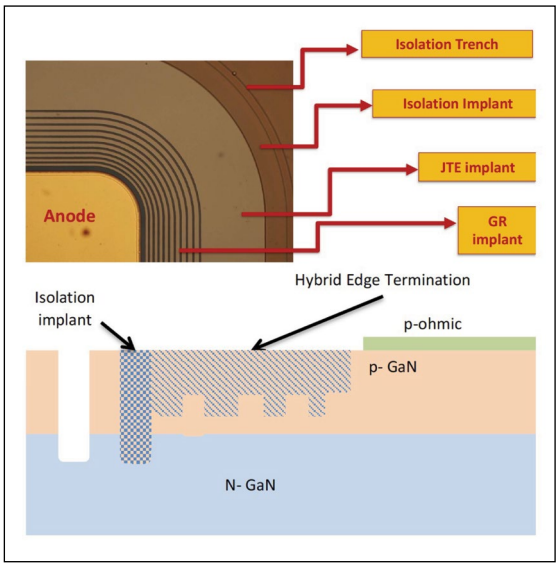
To help look into these matters, the US collaboration that's led by the US Naval Research Laboratory has been studying vertical GaN *p-i-n* diodes, produced by MOCVD on bulk GaN substrates. Using growth rates that are typically around 2 μm hr^{-1}, the team has produced epiwafers with a 25 μm-thick *n*-type GaN drift layer, a 470 nm-thick *p*-type GaN layer and a 30 nm-thick heavily doped *p*-type GaN cap, prior to the formation of terminated devices, using nitrogen implantation at up to 180 eV in a castellated structure (see Figure 4). After adding an anode and blanket cathode with electron-beam evaporation, the team did not apply a contact alloying anneal, with contacts utilised as deposited.

These devices exhibit a differential on-resistance below 5 mΩ cm^2 and a breakdown voltage of 3.2-3.4 kV, for 10 A class diodes with a size of around 1 mm^2.

To assess the robustness of their devices, the team applied high-temperature reverse-bias testing at more than 80 percent of the breakdown voltage, under vacuum and without passivation or packaging of the diodes. Periodic plots of current as a function of voltage enabled an evaluation of the degradation of the breakdown characteristics.

In addition, the team thermally stressed a cohort of 60 devices under nitrogen, using a rapid thermal anneal of 60 minutes, with sequential testing at increasing temperatures.

The researchers found that their devices exhibit a range of breakdown behaviours. As well as 'ideal' behaviour – described as low current leakage at 90 percent of breakdown, and a repeatable sharp breakdown – the team also found that



➤ Figure 4. Optical image (top) and a cross-sectional illustration of vertical GaN *p-i-n* diodes produced and investigated by a team led by the US Naval Research Laboratory, and supported by researchers from the University of Florida, Amentum and Sandia National Laboratories.

some of its devices showed: a repeated sharp breakdown with significantly elevated leakage; and a 'soft' breakdown, with a significantly elevated leakage and a less distinct increase in reverse current density at the breakdown voltage. Devices exhibiting all three forms of breakdown showed avalanche-type behaviour, with reverse electroluminescence uniformly under the anode, or visible at an anode corner spot.

When stressing at 150°C, a device exhibiting 'ideal' behaviour had a consistent low leakage of around 0.5 μA cm^{-2}, up to the end of testing – that's around 440 hours. However, periodic probing produced a softening of sharp breakdown and a slight reduction in breakdown voltage. This softening started after 88 hours of testing, and at 112 hours the breakdown voltage decreased from around 3350 V to 3275 V, before stabilising. Following 438 hours under 150°C, and then 84 hours at 200°C, degradation totalled 6 percent.

Encouragingly, after this high-temperature reverse-bias test, the diode still retained its avalanche-type behaviour. Forward behaviour did not change, and the device still maintained broad emission under the anode, when exhibiting reverse electroluminescence.

During testing of two additional diodes under a high-temperature reverse-bias test at 200°C, the team observed minimal breakdown degradation or shape change over 408 hours. According to the researchers, this divergent behaviour of the die, despite co-processing on the same wafer, highlights the need for further in-depth study.

Due to the variation in diode behaviour, and the limitation of the testing equipment to 200°C, the team annealed a cohort of five diodes for 60 minutes in 50°C steps from 250°C to 500°C.

At all temperatures, the diodes remained functional in forward and reverse, but the breakdown voltage diminished, and softened markedly after stressing at 350°C.

According to the team, the change in reverse-bias behaviour through thermal stress indicates changes to the termination structure. It is suggested that as the hybrid termination structure makes use of nitrogen implantation and the resultant damage, long-term stability of the diode may be governed by the diffusion of point defects, or the annihilation of Frenkel pairs.

The lead author of the CS Mantech paper detailing this work, Alan Jacobs, told *Compound Semiconductor* that the team continues to investigate these devices, but with less time/effort, given the programme that funded this work has completed.

"That said, the devices that are divergent are still viable, and we plan on doing further electroluminescence imaging and cathodoluminescence imaging to see if the termination structure has changed due to thermal stressing. Tracking these changes and how they modify the field distribution would improve our ability to design a more robust termination structure, and also investigate mitigation techniques for a more temperature-agnostic design."

Ga_2O_3 superjunction structures

In recent years, the ultra-wide bandgap material Ga_2O_3 has started to feature at CS Mantech. This oxide is attracting much attention, because it promises to enable the production of devices with incredibly low losses and a high electrical breakdown field. However, progress is held back by a lack of *p*-type doping, preventing the fabrication of *p-n* junctions.

To sidestep this issue and produce enhancement-mode transistors that don't require *p*-type doping, a number of different device architectures have been proposed, including finFETs. Laying the foundations for producing such devices, via simulations and etching development, is a team led by Swansea University, which has just commissioned an Aixtron close-coupled showerhead deposition system that's capable of the growth of 4-inch Ga_2O_3-based epiwafers.

Lead-author of the CS Mantech paper detailing the simulations and etching work, Swansea University's Nicholas Edwards, told *Compound Semiconductor* that team's calculations, using the Silvaco framework, outline the blueprint for realising high-breakdown, enhancement-mode devices, while also revealing the underlying operation mechanism.

One of the challenges when try to simulate the performance of Ga_2O_3 devices is a lack of consensus concerning carrier mobility models.

"It is difficult to get consensus on monoclinic crystal

structures such as beta gallium oxide, due to a lack of symmetry," says Edwards, who points out that with any next-generation material, discrepancies will exist among the available models.

"The models we implemented are based on literature and validated through experimental results, making them the most accurate to date. While absolute values may vary slightly, the key findings and design insights remain consistent and reliable."

The team's simulations show that it's possible to produce enhancement-mode β-Ga_2O_3 finFETs with a 5 kV blocking voltage using a doping concentration below 10^{16} cm^{-3} and fins with either: a width of 200 nm and a thickness of 0.8 μm; a width of 400 nm and a thickness of more than 1.2 μm; or a width of 600 nm and a thickness of more than 2 μm.

Also involved in this collaboration is KLA, another key player in the compound semiconductor cluster in South Wales.

The SPST SyapseEtch module made by KLA has been used in this investigation to etch β-Ga_2O_3, due to its high plasma density that facilitates the etching of materials with strong chemical bonds.

Using a 1 μm-thick SiN hard mask, deposited using an SPTS plasma-enhanced CVD module, the team have identified that there is a wide process window for the etching of β-Ga_2O_3.

Adjusting the applied power, which alters the etch rate, does not influence the vertical sidewall profile – this remains highly vertical, with an angle of 88°. However, the lower etch rate produces a flat trench base with rounded corners, viewed as potentially advantageous for finFET mesa fabrication, while the faster edge rate appears better-suited to edge-termination structures requiring deeper etches.

According to Mike Jennings from the Centre for Integrated Materials (CSIM) at Swansea University, work on the development of Ga_2O_3 will continue.

"This [etching] process has now been successfully transferred to the CISM fabrication facility. The next phase involves device fabrication and performance characterisation."

Such efforts will help to advance the prospects of Ga_2O_3 devices, which are likely to feature, along with their GaN and SiC cousins, at next year's CS Mantech – it will be held in Portland, Oregon, in mid-May.

Shrinking the size of LiFi through heterogeneous integration

Combining microLEDs and GaN HEMTs via transfer printing creates chip-scale systems that are opening new possibilities for visible light communication.

BY MUHAMMET GENC, ZHI LI, BRENDAN ROYCROFT AND BRIAN CORBETT FROM TYNDALL NATIONAL INSTITUTE AND SHEIKH IFATUR RAHMAN AND SIDDHARTH RAJAN FROM OHIO STATE UNIVERSITY

WITHIN THE field of wireless communication, visible light communication (VLC) has emerged as a transformative technology that's gaining increasing attention over traditional Radio Frequency (RF)-based communication methods.

At the heart of many of these VLC systems are LEDs, transmitting data at high speeds. These sources provide a promising solution to the challenges posed by crowded RF spectrums that are straining to satisfy the growing demand for higher data rates.

Migrating to the unlicensed visible light spectrum, which spans 400 THz to 800 THz, accesses a vast bandwidth, enabling VLC systems to support faster communication speeds with minimal interference, even in environments where RF signals are congested or impractical.

VLC is poised make a valuable contribution in many emerging applications, including smart cities, autonomous vehicles, the Internet of Things (IoT), and Artificial Intelligence (AI)-powered data centres. In all these examples, there is increasing need for high-speed, reliable communication systems that handle vast amounts of data. VLC offers a strong solution for addressing these demanding requirements, particularly in high-density indoor environments, such as office spaces, airports, conference halls, shopping malls and smart homes. For IoT applications, the appeal of VLC may be particularly strong compared with RF-based communication when deployed in environments where interference, limited bandwidth, or regulatory constraints make RF impractical.

In the autonomous vehicle, VLC could be a game changer, rather than just an attractive alternative. That's because VLC might facilitate real-time communication between vehicles, pedestrians, and infrastructure, and enable faster, more reliable decision-making. This could significantly enhance the safety and efficiency of transportation systems.

Meanwhile, in AI data centres VLC has the potential to revolutionise communication in chip-to-chip optical interconnects by enabling ultra-fast data transfer between components – this is essential for emerging computing technologies.

Despite much interest in the successful commercialisation of VLC systems, roll-out is held back by a number of technical challenges. While the leading candidate for the light source is clear – it's microLEDs made from GaN, which is renowned for its high efficiency, brightness, and ability to operate at high frequencies – it's far from easy to integrate these emitters with high-speed electronics that's capable of handling the modulation and control of these light sources.

Under the Tyndall National Institute/ Ohio State University Catalyst Project, led by Muhammet Genc and Siddharth Rajan from the respective insitutions, we have teamed up to address key challenges in VLC technology. Our innovative approach, which involves integrating GaN-based microLEDs with GaN HEMTs on a single chip platform, aims to simplify VLC system design while significantly reducing size and improving energy efficiency. This work holds the potential to enable scalable, cost-effective, high-speed data transmission using visible light, laying a strong foundation for the next generation of optical communication systems.

The integration challenge

In traditional VLC systems, external drivers provide the high current densities required for high-speed modulation of the microLEDs. However, these external components add size and complexity to the system, reducing overall efficiency and scalability. What's more, the power consumption of these external drivers increases the overall energy demands of VLC systems, making them less suitable for small, portable consumer devices.

Our solution to this challenge lies in the integration of GaN microLEDs with GaN HEMTs, which are well-suited for

high-speed modulation. HEMTs are capable of driving large currents with minimal resistance, and are known for their high electron mobility, making them ideal for controlling the operation of GaN microLEDs. Integrating these two components onto a single chip eliminates the need for external drivers, simplifying system architecture and reducing energy consumption. This approach has the potential to pave the way for compact, high-performance VLC systems that are more energy-efficient and scalable.

We integrate our GaN-based microLEDs and GaN HEMTs onto a single chip with a novel transfer printing technique. This ensures precise placement of microLEDs onto the GaN HEMT substrate without damaging delicate components. Our process begins by fabricating GaN microLEDs on a silicon substrate, and patterning and etching them into the desired shape – we choose dimensions of 20 µm x 10 µm. Following the preparation of our microLEDs, we release them from the silicon substrate via selective etching, with SiN tethers holding them in place during the release process (see Figure 1 (a) and (b)).

The microLEDs are then transferred to a flexible polydimethylsiloxane (PDMS) stamp, which ensures accurate alignment for transfer to the GaN HEMT wafer. Using this transfer printing process, we ensure precise placement of the microLEDs onto the HEMT substrate without the risk of damaging the components (see Figure 1 (c) and (d)). After transfer is complete, we thoroughly test the chips to assess their electrical and optical performance. Our process ensures successful integration of GaN microLEDs and GaN HEMTs, creating a single chip that combines the high-speed modulation capabilities of the HEMTs with the optical performance of the microLEDs. Ultimately, we are capable of producing a highly efficient VLC system.

We view our integration process as a significant step toward the miniaturisation of VLC systems, as it reduces the need for bulky external drivers and simplifies the overall design. The result is a compact, energy-efficient system that can be easily scaled for a wide range of applications previously discussed.

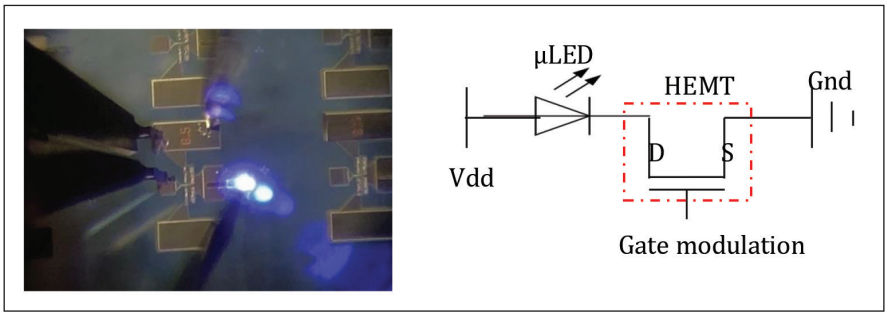


Figure 2. Modulation of microLED by GaN HEMT during operation.

Demonstrating success

After successfully integrating our GaN microLEDs and GaN HEMTs, we subjected the resulting system to rigorous testing to evaluate its performance (see Figure 2). Our efforts began by measuring the light-current-voltage characteristics of our microLEDs. These devices demonstrated a turn-on voltage of 2.6 V and a maximum optical power output of 0.24 mW at a current density of 250 A cm^{-2}. Our results confirm that these emitters are capable of efficient light emission, even at high current densities (see Figure 3 (a)).

Next, we assessed the modulation capabilities of our integrated system. By adjusting the gate voltage of the GaN HEMT, to control current flowing through the microLED, we realised precise modulation of the light emission, a key requirement for high-speed VLC. Our system successfully modulated the light emission of the microLEDs, with the drain-source current of the GaN HEMT dropping to zero at a gate voltage of -4 V, indicating that the modulation process was functioning as expected (see Figure 3 (b) and (c)).

One of our most valuable tests has involved evaluating the modulation bandwidth of the system. This determined a 3 dB modulation bandwidth of 100 MHz, which, while not yet sufficient for next-generation VLC applications, represents a promising result for this first-generation integration of microLEDs and HEMTs. The 100 MHz

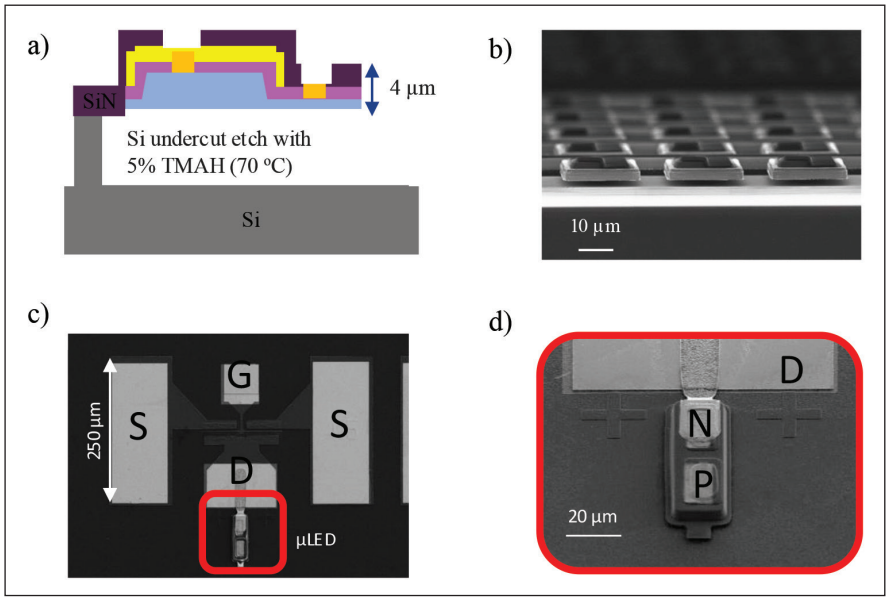
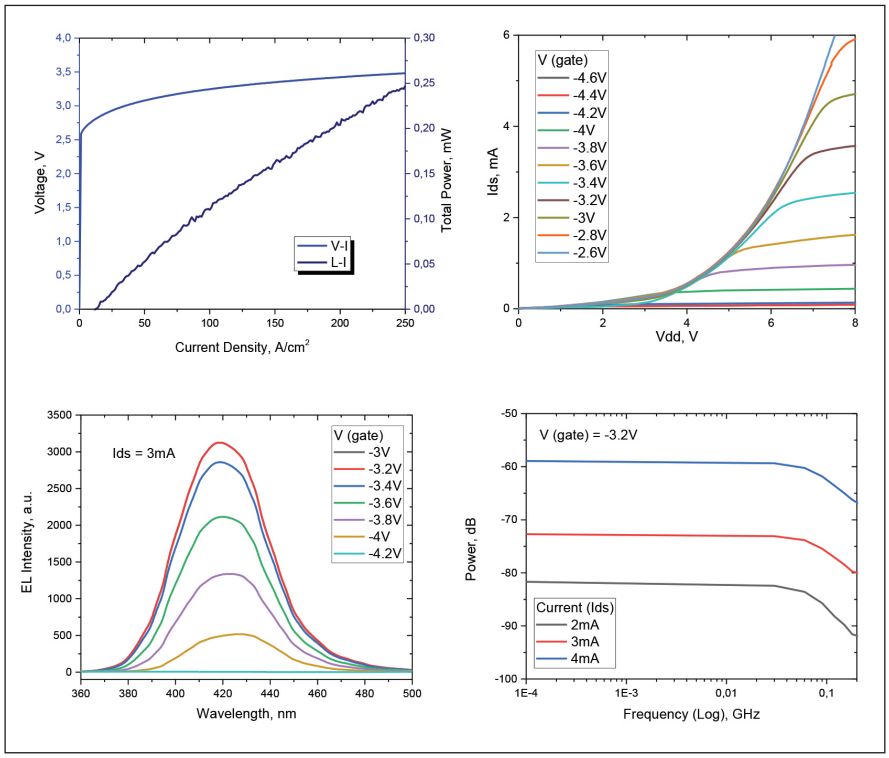


Figure 1. MicroLED release, transfer, and integration process. (a) Undercutting of microLEDs from the silicon substrate via selective etching using a tetramethylammonium hydroxide (TMAH) solution. (b) Image showing the microLEDs still securely attached to the SiN anchors following the etching process. (c) Transfer of the microLEDs onto a GaN-based HEMT structure on a SiC substrate. (d) High-magnification view of the final transfer of the microLEDs onto the GaN-based HEMT structure on the SiC substrate.



➤ Figure 3. Electro-optical and frequency characteristics of transfer-printed microLEDs integrated with GaN HEMTs on a single-chip platform. (a) Light-current-voltage (L-I-V) characteristics of a 20 x 10 μm² microLED. (b) Drain-source current (I_{ds}) as a function of supply voltage (V_{dd}) for various gate voltages, with I_{ds} reaching zero at a gate voltage of -4 V. (c) EL intensity versus gate voltage, indicating a decrease in EL intensity as the gate voltage exceeds -4.2 V, confirming the "off" state. (d) Power versus frequency (log scale) for different current levels (2 mA, 3 mA, and 4 mA) at a gate voltage of -3.2 V, showing a 3 dB modulation bandwidth of 100 MHz, demonstrating the dynamic frequency response of the integrated microLED-GaN HEMT device.

bandwidth indicates that our system is capable of high-frequency operation, providing a solid foundation for future improvements in modulation speed and overall performance (see Figure 3 (d)).

Future implications

Our successful integration of GaN-based microLEDs and GaN HEMTs onto a single chip offers several key advantages for the future of VLC. First and foremost, it eliminates the need for external drivers, significantly reducing the size, complexity, and energy consumption of VLC systems. This makes VLC a more viable option for portable devices, such as smartphones, wearable technologies, and IoT gadgets, where space and energy efficiency are critical. Additionally, our VLC technology can directly benefit advanced applications in AI data centres, where fast and reliable optical interconnects are crucial for massive data processing.

Moving forward, we will focus on increasing the modulation bandwidth of our system, with the goal of reaching speeds in the gigahertz range and beyond. If we achieve such high modulation speeds, this will allow VLC systems to handle the demanding data rates of modern communication networks, making them viable alternatives to RF-based systems for a variety of applications, including chip-to-chip optical interconnects in high-performance computing environments and AI data centres.

Another area for future development is improving the scalability of the integration process. While the transfer printing technique that we have used in this study is highly effective for integrating GaN microLEDs with HEMTs, there are opportunities to enhance the scalability of this process and make it suitable for mass production of VLC systems.

It may also be possible to increase the performance and the efficiency of our VLC systems by introducing integration techniques that incorporate other electronic components, such as photodetectors.

Our triumph – the integration of GaN-based microLEDs with GaN HEMTs onto a single chip – marks a significant milestone in the development of compact, energy-efficient VLC systems. By eliminating the need for external drivers, we have simplified system design, trimmed power consumption, and opened-up new possibilities for high-speed, interference-free communication. While the modulation bandwidth of 100 MHz is an important first step, we know that further advances in modulation speed and system scalability are necessary to unleash the full potential of VLC in a range of emerging applications, including AI data centres, chip-to-chip optical interconnects, and other high-performance communication networks. As we continue to develop this technology, this will increase its potential for shaping the future of wireless communication in a wide range of industries.

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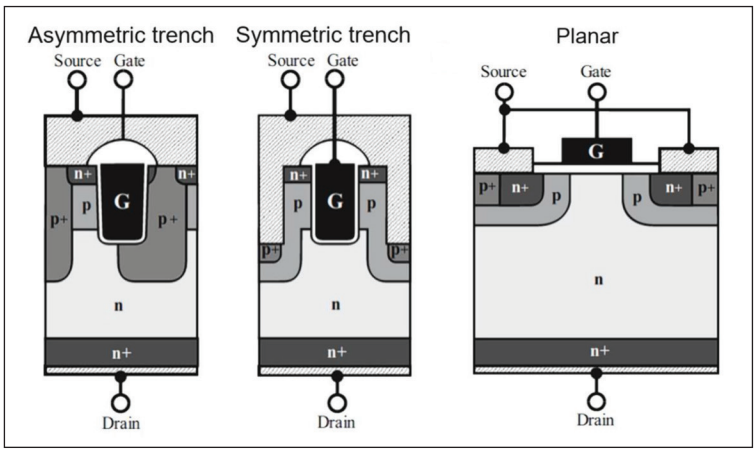
Scrutinising SiC MOSFETs

Efforts by chipmakers to improve the SiC MOSFET include investigations to understand how the design of the trench influences ruggedness, the role of the substrate on device quality, opportunities for superior screening, and the origin of shifts in threshold voltage

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

It is now 15 years since the launch of the first SiC MOSFETs by two of its pioneers, Rohm and Cree, subsequently renamed as Wolfspeed. Since then, there has been a substantial increase in the number of producers of this device, as well as an expansion in blocking voltages, improvements to performance, and a growth in sales to more than $1 billion per annum, according to many analysts.

Judged in these terms, there's no doubt that the SiC MOSFET is already a tremendous success. But there is still more to do on many fronts. To increase the supply and trim the cost of this class of transistor, more fabs are being built, and production is switching from 150 mm to 200 mm wafers. And to improve yield, performance and robustness, many leading manufacturers of the SiC MOSFET are scrutinising its behaviour.



➤ Figure 1. Infineon has compared the short-circuit ruggedness of MOSFETs with an asymmetric trench, a symmetric trench, and a planar trench.

At this year's International Reliability Physics Symposium (IRPS), held in Monterey from 30 March to 3 April, researchers from a number of the leading manufacturers of SiC MOSFETs detailed insights gained from investigations into this class of transistor. Studies of short-circuit ruggedness for different channel designs were outlined by Infineon; STMicroelectronics revealed the influence of the starting material on final device characteristics; NoMIS Power presented screening methods using high gate-voltage pulses and unclamped inductive switching; and investigations into threshold voltage shift were reported by Mitsubishi Electric.

Short-circuit ruggedness

In power-conversion systems, ruggedness and reliability are critical, particularly when short-circuit events occur. Due to this, there is a need for SiC MOSFETs to be robust under repetitive fault operating conditions.

Investigating this, a team from Infineon has compared the performance of three types of SiC MOSFET produced by four different manufacturers: that with an asymmetric trench, the technology that Infineon employs; another with a symmetric trench; and two variants with planar structures with different

oxide thickness (see Figure 1 for the device designs, and Table 1 for key details of the device structures).

Discussing this study at this year's IRPS, Andrea Piccioni noted that the active areas of the MOSFETs with a trench architecture are smaller than those with a planar geometry, enabling a lower on-resistance.

Piccioni explained that their investigation involved using normal distribution channels to purchase 15 commercial 1.2 kV devices from each of the four manufacturers. These devices, with on-resistances in the range 62 mΩ to 82 mΩ, were housed in TO247-4 pins packages, and had not been used prior to the stress test. The team decapsulated one of each of the 15 devices to analyse its characteristics in the pristine state.

The repetitive short-circuit stress test is relatively straightforward, involving the repeating of short-circuit events at a certain frequency, and ensuring that the time between each of them is long enough to avoid heating accumulation. The researchers applied 1,000 cycles at a frequency of 1 Hz, using pulses with a duration of 2 µs to provide the short-circuit. This test involved a drain-source voltage of 800 V, and values for the positive gate-source voltage varying from device to device – they ranged from 14.2 V to 15.5 V – to ensure similar values for the energy density of the four different devices.

During testing, destructive failure can occur, due to leakage from the drain to source. In addition, there can be non-destructive failure, such as leakage from the gate to source, and variations in key characteristics, such as threshold voltage.

The team had to consider how to spot all these possible issues with one unique criterion. "We decided to use short-circuit energy variation over the short-circuit cycle," explained Piccioni, who added that they considered a variation of more than 5 percent a failure.

Results of the stress tests show significant variation with device architecture (see Figure 2). All the MOSFETs with the asymmetric trench stay well within the ± 5 percent limit, as do those with the symmetric trench – although in that case there is a slight increase in short-circuit energy over the duration of the test, due to a negative shift in threshold voltage. In sharp contrast, the planar SiC MOSFETs performed poorly. All those with a thicker oxide failed the test, two from thermal runaway that led to destruction, and the remainder from an elevated gate-to-source leakage. The latter issue also led to the failure of ten planar devices with a thinner oxide.

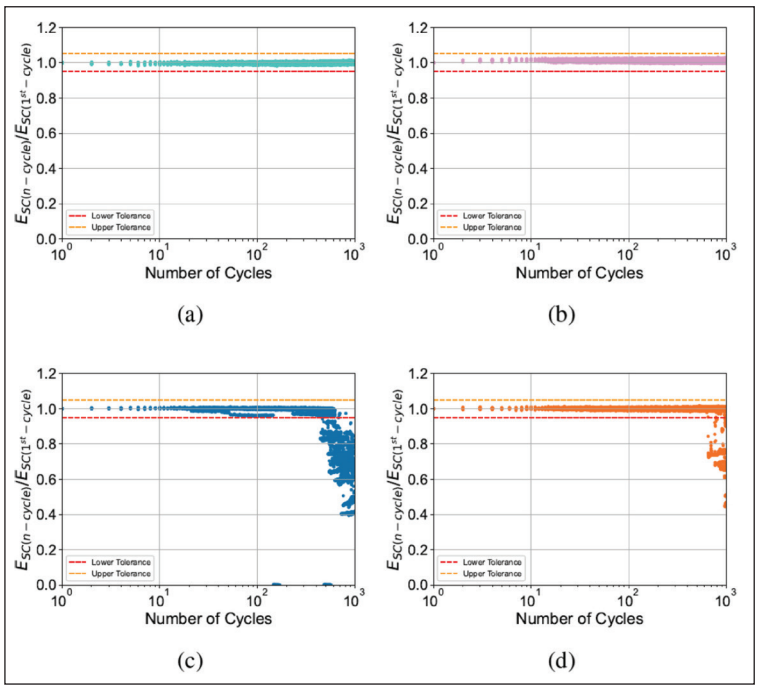
Piccioni also shared a Weibull plot, showing the probability of failure as a function of the number of cycles. This demonstrated that the gate oxide thickness in planar structures plays a pivotal role in robustness, within thinner oxides leading to greater reliability.

Param.	Channel	$^{*}R_{DS(on)}$	AA	d_{GOX}
Unit	[/]	$[m\Omega]$	$[mm^2]$	$[nm]$
M1	Asym.trench	78	2.28	~67
M2	Sym.trench	62	3.52	~50
M3	Planar	62	5.62	~50
M4	Planar	75	4.55	~35

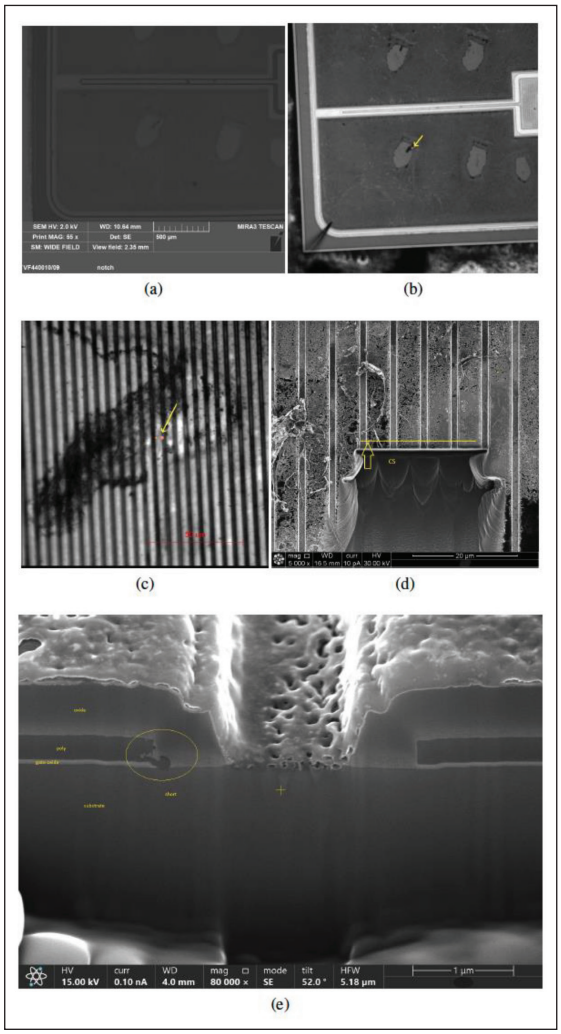
➤ Table 1. Details of the different forms of SiC MOSFET used in Infineon's study of short-circuit ruggedness. AA is the active area, and d_{GOX} is the thickness of the gate oxide.

Failure analysis has been conducted by Piccioni and co-workers, initially with decapsulation and optical inspection, before removing the top side of the device and turning to scanning electron microscopy. "After that, photo-emission microscopy helped us to locate the spot where the leakage current is flowing," remarked Piccioni, who explained that the team would then extract a cross-section, and view this using a focused ion beam. With this approach, a short is observed between the substrate and the corner of the polygate (see Figure 3).

To understand the origins of the weakness of planar devices, Piccioni and co-workers turned to Technology Computer-Aided Design (TCAD) simulations to gain an insight into the temperature profiles of different designs of MOSFET. These simulations show that compared with a trench device, that with a planar geometry has a higher temperature at the top side metallisation and at the SiC substrate. In the planar device, the hot spot occurs at 2.17 µm. Meanwhile, in the trench MOSFET,



➤ Figure 2. The short circuit energy over 1,000 cycles reveals the superior reliability of the (a) asymmetric and (b) symmetric trench MOSFETs over their planar equivalents (c) and (d).



➤ Figure 3. To uncover the origin of the failure in the planar SiC MOSFETs, the team from Infineon began by removing the top-side metal and inspecting the device with a scanning electron microscope (a). Failure localisation by photo-emission microscopy followed (b) and (c), before a focused ion beam provided a cross-section (d) and its visualisation (e), exposing a short at the edge of the gate.

the hot spot is deeper, at 3.38 μm, reducing the stress at the gate oxide.

Material considerations

A key question for the producers of any semiconductor device is this: How does the impact of the starting material influence the final device? This is far easier to answer for companies that are vertically integrated, such as STMicrolectronics, which spans powders to products.

Speaking on behalf of this European powerhouse at IRPS, Advanced Metrology Material Manager Nicolò Piluso offered some insights into this matter, by considering 650 V MOSFETs subjected to high-temperature reverse-bias tests.

SiC material is grown by physical vapour transport, with SiC powder heated at the bottom of a chamber, beneath a SiC seed crystal. The growth of SiC is imperfect, with bulk material riddled with a range of defects, including micropipes, threading screw and edge dislocations, basal plane dislocations and point defects.

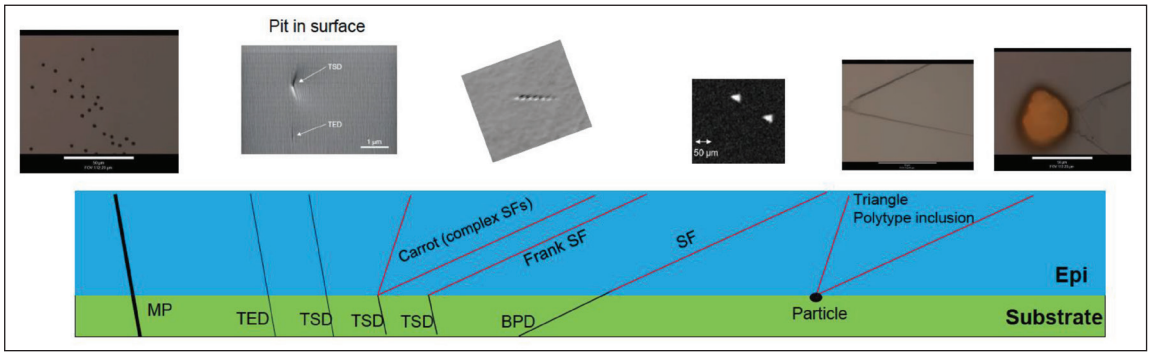
Production of SiC power devices involves growth by MOCVD on substrates that are off-axis to realise the best compromise between surface kinetics and growth rate.

“The aim is to achieve a high thickness and good doping uniformity, keeping low the defectiveness,” remarked Piluso. Due to this, there’s a need for a fast epitaxial process and repeatability.

Piluso outlined how many types of defect can propagate from the substrate to the epilayer (see Figure 4). In the case of threading screw dislocations and Basal plane dislocations, growth tends to lead to a conversion into stacking faults.

Different types of defect impact the MOSFET in different ways. Micropipes, which now have a typical density below 0.1 cm^{-2}, are destructive, while threading screw dislocations that are accompanied by a pit, and have a similar degree of prevalence, lead to reliability issues, and can cause an increase in leakage current. MOSFETs can also suffer from a significant decline in blocking voltage, caused by in-grown stacking faults, complex stacking faults and downfalls – typical densities are 0.01 cm^{-2} to 1.0 cm^{-2} for the first of these, and 0.1 cm^{-2} to 1.0 cm^{-2} for the other two.

Piluso explained that a number of techniques are used to follow the defectivity from the substrate to the epilayers. The most common are optical microscopy, light-scattering methodologies and photoluminescence. All three are relatively quick, have a high spatial resolution, and can uncover morphological defects, but are unable to reveal dislocations. This is possible with X-ray topography and atomic force microscopy, but both those approaches have a low throughput.



➤ Figure 4. SiC substrates suffer from many types of defect.

"The recent enlargement of the wafer from 150 mm to 200 mm brings several drawbacks, in terms of defects, at the beginning," remarked Piluso. He explained that stacking faults were detected near the edge of the wafer, which is symptomatic of a physical vapour transport process issue that needs to be fixed. Another concern is scratches, due to a lack of optimisation in the chemical mechanical polishing process.

"I can say that currently, such kinds of evident defects have been almost completely removed and 200 mm high-quality silicon carbide substrates are available."

A major weakness of today's metrology tools is that they are unable to detect defects that lead to failure. The likes of micropipes, nanopipes and threading screw dislocations are exposed though electrical failures.

"In such cases, electrical testing is the only way to test the quality of the material," said Piluso.

The spokesman for ST shared a map of die from a wafer, with those impacted by a defect suffering from inferior electrical characteristics, including a significant reduction in the Schottky barrier height. Raman microscopy is able to clearly identify the nature of the defect – inclusion of the 6H polytype.

Piluso also discussed electrical failure caused by a threading screw dislocation accompanied by a pit. The non-destructive optical technique emission microscopy exposed the hot spot, associated with device failure. Scanning electron microscopy then uncovered a triangular-shaped defect at this hot spot, suggesting a dislocation that originates in the substrate and propagates to the epilayer. Scrutinising this area with atomic force microscopy identified surface pitting, caused by threading screw dislocations that are clearly exposed by etching with potassium hydroxide.

The team from ST have also studied a hard failure, seen by an abrupt increase in drain leakage current after about 30 minutes. Again, emission microscopy identified the location of the device. After delayering, Piluso and co-workers applied a potassium hydroxide etch, which revealed the typical symmetry exhibited by a micropipe defect.

"It can be supposed that the defect led to a very high current density in a narrow region," remarked Piluso, adding: "The material is brought to a high temperature, exceeding the limit imposed by conductivity, and for this reason suffered corrosion and breakage."

He added that scanning electron microscopy revealed a core hole in the centre of the defect at a depth of more than 30 μm, indicating that this defect starts in the bulk and goes through the entire epilayer.

The success of the SiC MOSFET over alternatives, such as the SiC JFET and SiC BJT that got to market first, stems from providing a drop-in replacement for the silicon MOSFET. However, while both forms of MOSFET are similar, they differ in threshold voltage characteristics

When concluding his presentation, Piluso called for strong activity to improve characterisation, by enabling scanning electron microscopy, profilometery, and atomic force microscopy within standard metrology inspection at the manufacturing level.

Threshold voltage shifts

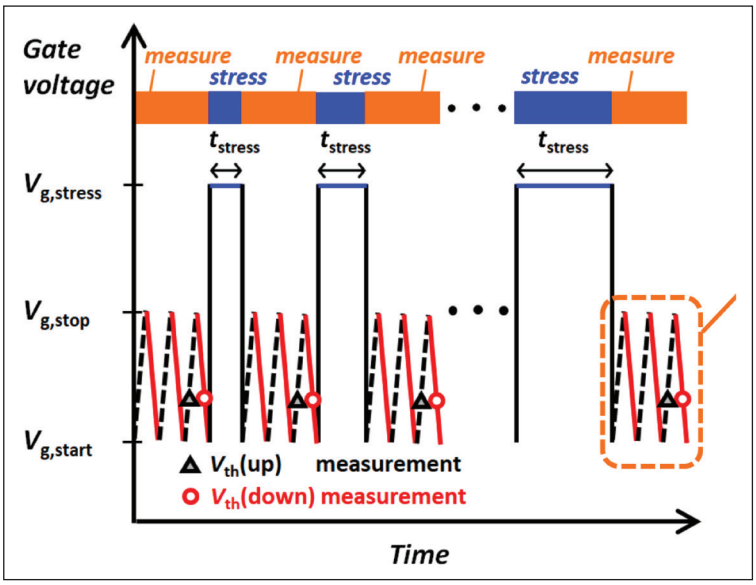
The success of the SiC MOSFET over alternatives, such as the SiC JFET and SiC BJT that got to market first, stems from providing a drop-in replacement for the silicon MOSFET. However, while both forms of MOSFET are similar, they differ in threshold voltage characteristics.

These differences in threshold voltage characteristics, seen under different temperatures and stress conditions of the oxide, are related to the SiO_2 dielectric in both types of transistor. Due to its wider bandgap, energy levels of the defects present in SiO_2 differ to those found when this oxide is paired with silicon.

Given the importance of threshold voltage – a key characteristic for any transistor – changes in the threshold voltage of SiC MOSFETs have been extensively studied. These investigations have established that the threshold voltage changes when a positive or negative electric field stress is applied to the gate oxide, as this leads to a charging of defects in the gate oxide, especially in the vicinity of the SiO_2/SiC interface.

Under a moderate electric field stress, there is a monotonic change in threshold voltage with stress time, due to the capturing of only electrons or holes, depending on the bias.

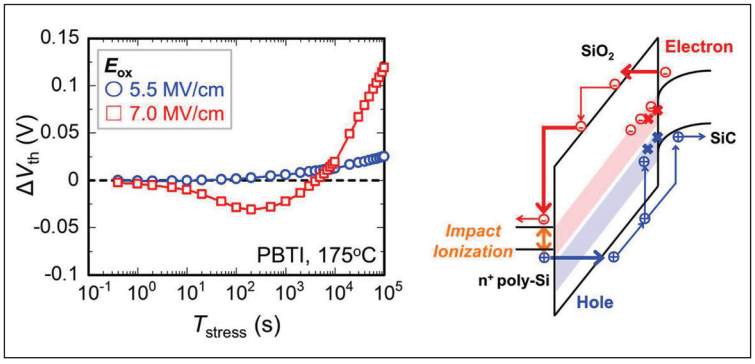
When the electric field stress is either highly positive or negative, SiC MOSFETs display a markedly different behaviour. In this case, the threshold voltage shift is initially negative, but over time it turns around and switches to positive, due to the capture of both electrons and holes in both SiO_2 and beside the SiO_2/SiC interface. Under these conditions, there's the filling of bulk traps in SiO_2, as well as interfacial traps at or near the SiO_2/SiC interface.



➤ Figure 5. Mitsubishi Electric's positive and negative bias temperature instability measurements were undertaken with measure-stress-measure sequences. Double sweeps of the gate voltage were performed three times to ensure a reducible readout of the threshold voltage.

According to Munetaka Noguchi and co-workers from Mitsubishi Electric, the influence of a high gate voltage on bias temperature instability of SiC MOSFETs has been well reported, accurately capturing the physical phenomena involved. "However, the impact of a high oxide electric field stress is not fully understood, and requires a systematic investigation." So, to shed light on this issue, they have conducted a thorough study on this, reporting results for SiC MOSFETs under a range of stresses, including both high negative and positive bias, and different temperatures.

For this work, the team from Mitsubishi used vertical planar silicon-face *n*-MOSFETs, with the gate oxide, roughly 47 nm-thick, formed by thermal oxidation and subsequent nitridation in diluted NO. On top of the oxide is n^+ poly-silicon.



➤ Figure 6. Measurements by Mitsubishi Electric of positive-bias temperature instability reveal a shift in threshold voltage under cumulative stress that depends on the applied oxide field stress. Under high oxide stress (right), electrons injected from SiC trigger impact ionisation in the n^+ poly-silicon, and holes that are generated are subsequently injected back into the SiO_2, where they are partially captured.

As well as these vertical devices, Noguchi and co-workers studied lateral devices that do not have the JFET region. Investigating these lateral devices allows evaluation of the gate leakage current and the hole current flowing into the gate oxide from the channel region.

For testing both positive- and negative-bias temperature instability, for each value of threshold voltage that's recorded, the team performed a double sweep of the gate voltage on three occasions, to ensure a reproducible readout of the threshold voltage (see Figure 5). The researchers defined the threshold voltage as the gate voltage at which the drain current reaches 1×10^{-6} A cm^{-2}, and defined the change in threshold voltage as the shift in threshold voltage in the downward sweep from its initial value.

Investigations for the positive-bias temperature instability at 175°C show that under an oxide electric field stress of 5.5 MV cm^{-1}, a condition referred to as 'not so high', there is a monotonic increase in threshold voltage with stress time, resulting from electron capture in SiO_2 (see Figure 6). But at a higher oxide electric field stress of 7 MV cm^{-1}, the change in threshold voltage exhibits turnaround behaviour, shifting from initially negative to positive. "This indicates that hole capture occurs initially, and after a while this process saturates, and in the following phase electron capture becomes dominant."

The holes that are observed during this measurement possibly result from anode hole injection. This could occur under a high positive oxide electric field stress, with some electrons injected from SiC triggering impact ionisation in the n^+ poly-silicon, and holes that are generated subsequently injected back into SiO_2, where they are partially captured.

At 175°C, under an oxide electric field stress of 7.4 MV cm^{-1}, the negative change in threshold voltage is larger than it is at 25°C, suggesting that at a lower temperature more holes are captured by SiO_2.

To delve deep into electron capture, Noguchi and co-workers have studied the change in threshold voltage after turnaround, which is considered at the starting point for these measurements. Plots (see Figure 7) show that in the region where the shift in threshold voltage is less than 0.2 V, the curves for different oxide electric field stresses have an almost parallel shift, with the slope becoming more gradual as time increases. According to the team, this gradual saturation suggests the presence of as-grown electron traps in SiO_2. Meanwhile, where the shift in threshold voltage is more than 0.4 V, the slope becomes steeper with time, suggesting the generation of

as-grown electron traps in SiO_2 and/or the interfacial region.

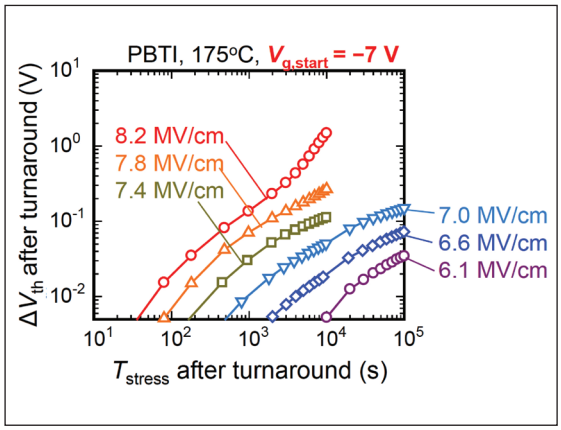
The team have also investigated the impact of the starting gate voltage on the change in threshold voltage after turnaround, comparing plots for 0 V and -7 V. Under the same oxide electric field stress, the change in threshold voltage is larger for 0 V, implying greater capture of electrons in SiO_2. This may occur because the surface potential at SiO_2/SiC is more bent at -7 V, leading to efficient emission of captured electrons.

Noguchi and colleagues have also carried out a thorough study of the shift in threshold voltage under stress under a negative bias. Similar to under positive bias, the plots at 175°C vary with the oxide electric field stress: there's a monotonic decrease observed at -5.8 MV cm^{-1}, due to hole capture in SiO_2; and, under -7.5 MV cm^{-1}, a turnaround from a decrease to an increase, attributed to electron capture in SiO_2 and/or near the interface between SiO_2 and SiC (see Figure 8).

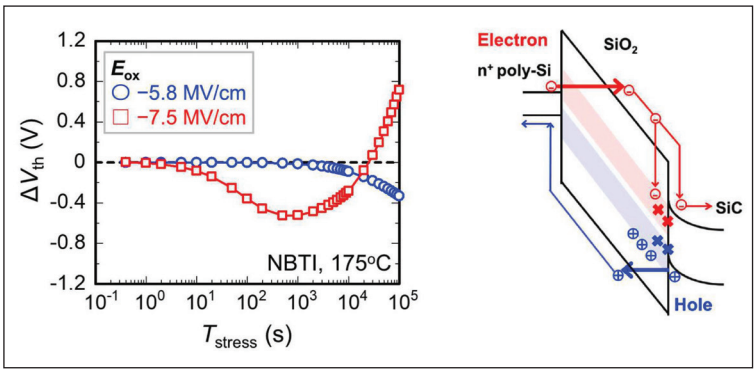
Previous studies on hole injection into SiO_2 on silicon have shown that the build-up of negative charges can be attributed to the generation of electron traps in SiO_2 and/or interfacial traps at the interface between SiO_2 and SiC.

Under a negative oxide-electric-field stress, holes injected from SiC are captured by SiO_2. It's possible that these injected holes could generate electron traps in SiO_2 and at the interface.

"To understand the phenomena, it's helpful to start the discussion with a threshold voltage shift at lower temperatures, such as 25 degrees C," remarked Noguchi.



➤ Figure 7. Measurements of the shift in threshold voltage after turnaround can be categorised into: curves with an almost parallel shift, with the slope becoming more gradual as time increases, suggesting the presence of as-grown electron traps in SiO_2; and curves that get steeper with time, suggesting the generation of as-grown electron traps in SiO_2 and/or the interfacial region.

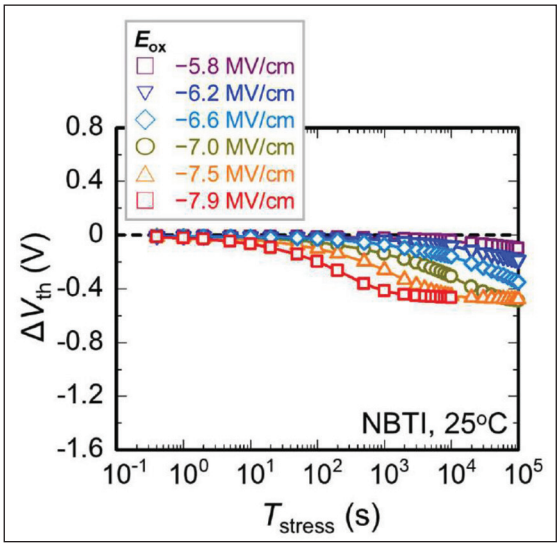


➤ Figure 8. Negative bias temperature instability measurements by Mitsubishi Electric reveal a shift in threshold voltage under cumulative stress that depends on the applied oxide field stress. The turnaround from a decrease to an increase in threshold voltage under -7.5 MV cm^{-1} is attributed to electron capture in SiO_2 and/or near the interface between SiO_2 and SiC.

Plots of this behaviour show a saturation in threshold voltage shift for all the applied oxide electric field stresses, which range from -5.8 MV cm^{-1} to -7.9 MV cm^{-1} (see Figure 9). At a higher oxide electric field stress, the change in threshold voltage is accelerated, attributed to faster hole capture.

Investigating the change in threshold voltage at -7.5 MV cm^{-1} for a range of temperatures shows that the minimum value does not change, and it is reached more quickly at higher temperatures, due to as-grown hole traps being filled more quickly, without additional generation of hole traps. Turnaround from a negative to a positive change in threshold voltage does not occur at 25°C, but does at 125°C and 175°C.

Noguchi and co-workers have investigated the change in threshold voltage after turnaround at 25°C and 175°C. "At both temperatures, the threshold voltage shift after turnaround can be universally described by the gate-injected charges after the turnaround," remarked Noguchi,



➤ Figure 9. Saturation of the threshold voltage shift, attributed to hole capture, is faster under a higher oxide electric field stress.

who pointed out that the shift is smaller at the lower temperature, and that the electron capture component of the threshold voltage shift can be attributed to the electron traps in silicon dioxide and at the interface.

To investigate these interfacial electron traps, the team studied the sub-threshold swing as a function of gate-injected charges. They found two phases in the generation of interfacial electron traps. "This indicates that the generation of interfacial electron traps on the negative oxide electric field stress partially contributes to the threshold voltage shift after turnaround."

Screening SiC MOSFETs

Over the last decade, advances in SiC substrates, epitaxial growth and the gate oxidation process have improved gate oxide reliability, but the risk of extrinsic failure in SiC devices still persists. This is an issue for the adoption of SiC MOSFETs in the electric vehicle market.

To address this concern, manufacturers of SiC power devices employ burn-in, at the package or wafer level, to provide a reasonable reduction in the 'failure-in-time' (FIT) rate – it's the number of failures per billion hours. For this task, harsher burn-in conditions enhance screening efficiency and further reduce the FIT rate, but may induce parametric shifts in the devices. What's more, the use of high-temperatures and extended testing during burn-in leads to a hike in overall production costs.

Due to these concerns, there is much interest in approaches that can cut the cost and time required to screen SiC MOSFETs.

One company developing a solution to this that's based on high gate-voltage pulses and unclamped inductive switching is NoMIS, a spin-off of the University at Albany, New York, that manufactures 1.2 kV, 1.7 kV and 3.3 kV SiC MOSFETs with worldwide foundry partners. Speaking on its behalf at this year's IRPS, Head of SiC Device Development at NoMIS Power, Seung Yup Jang, described this effort, which also involves contributions from the University at Albany and The Ohio State University.

Screening Type	Name	Conditions
High Gate Voltage Pulse (HVP)	HVP1	8.4 MV/cm, 1 s
	HVP2	8.6 MV/cm, 0.5 s
	HVP3	8.6 MV/cm, 1 s
Unclamped Inductive Switching (UIS)	UIS1	20% of Max E_{AS}
	UIS2	40% of Max E_{AS}
	UIS3	70% of Max E_{AS}
HVP + UIS	Combo	HVP1 + UIS1

➤ Table 2. NoMIS has screened SiC MOSFETs using high-voltage pulsed (HVP) and unclamped inductive switching (UIS) tests.

Jang explained that unclamped inductive switching is an effective method for identifying early failures under off-state high drain bias. While originally designed to evaluate edge termination robustness, uniform avalanche current distribution in active cells, and suppression of the parasitic bipolar junction, it has broader utility. During avalanche breakdown the maximum electric field in the gate oxide will typically exceed 3 MV cm^{-1}, and may be as high as 4 MV cm^{-1}. If a negative bias is applied during unclamped inductive switching, the oxide electric field can be even higher, causing the temperature in the active region to rise, often exceeding 500°C. "These extreme conditions impose considerable stress on the gate oxide, making unclamped inductive switching a rigorous and informative screening method."

The team has developed an approach that aims to screen out all early failures using regular, automatic testing tools, as this is a cost-effective and efficient approach. The combination of high gate-voltage pulse screening and unclamped inductive load screening has been evaluated twice – after wafer fabrication and after packaging.

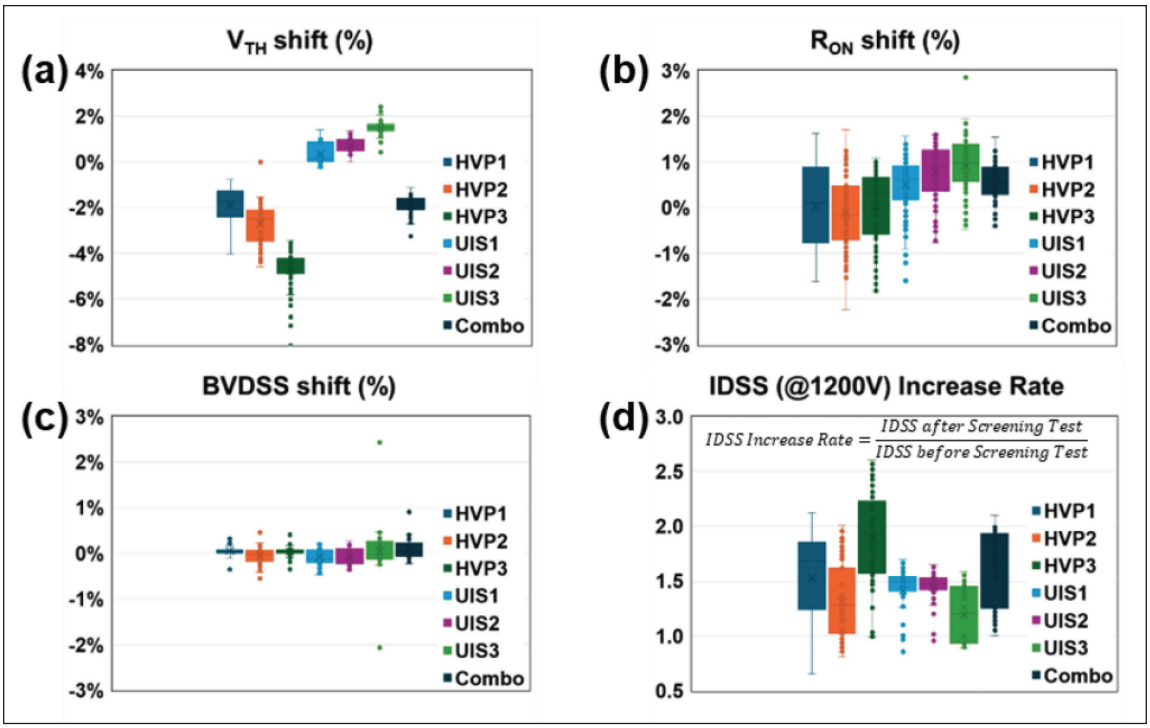
For this study, Jang and co-workers have investigated 1.2 kV, 35 mΩ and 80 mΩ planar SiC MOSFETs produced in a commercial foundry using 150 mm wafers. Gate oxides were thermally grown on 4H SiC substrates, with interface quality improved with post-oxidation annealing in nitric oxide.

To evaluate the gate oxide lifetime distribution of devices without any screening process, the team conducted constant-voltage time-dependent dielectric breakdown (TDDB) tests on 80 devices from each group.

Some devices in the 35 mΩ group failed instantly during TDDB testing, as the voltage ramped up, indicating infant failure, despite having passed prior DC testing under positive 5 MV cm^{-1} and negative 2 MV cm^{-1} pulsed gate-bias conditions.

To develop an effective screening method that minimises stress and duration conditions while addressing infant gate oxide failures, Jang and co-workers applied various screening conditions to their 35 mΩ devices (see Table 2 for details). The high-voltage pulse test conditions were devised to avoid severe degradation to the threshold voltage while providing sufficient stress, and unclamped inductive switching conditions delivered a fraction of the maximum single-event avalanche energy.

The team's testing sequence began with an initial DC test, and then more than 100 functional 35 mΩ devices were subjected to the various screening tests. 80 devices passed a second DC test, and were then subjected to TDDB tests using 9 MV cm^{-1} at 150°C.



➤ Figure 10. NoMIS has undertaken a range of screening tests: (a) threshold-voltage shift; (b) on-resistance shift; (c) avalanche breakdown voltage; and (d) drain-to-source leakage.

Results of the tests (see Figure 10) show that high-voltage pulse tests produce a shift in threshold voltage of up to 5 percent, attributed to impact ionisation in the oxide and trapping of holes in the SiO_2 and at the SiO_2/SiC interface. "This is an undesirable effect, as it may lead to the generation of new defects, and the negative threshold voltage shift is relatively permanent," remarked Jang. In comparison, the unclamped inductive switching test had a smaller impact on threshold voltage.

The changes in on-resistance mirror those in the shift in threshold voltage, but are less than 1 percent; and the avalanche breakdown voltage (BV_{DSS}) and drain-to-source leakage (I_{DSS}) do not show consistent trends.

"Overall, with the exception of the threshold voltage shift, the major parameter changes appear to be negligible," said Jang.

According to hysteresis measurements, there is no noticeable degradation of the SiO_2/SiC interface associated with the screening tests.

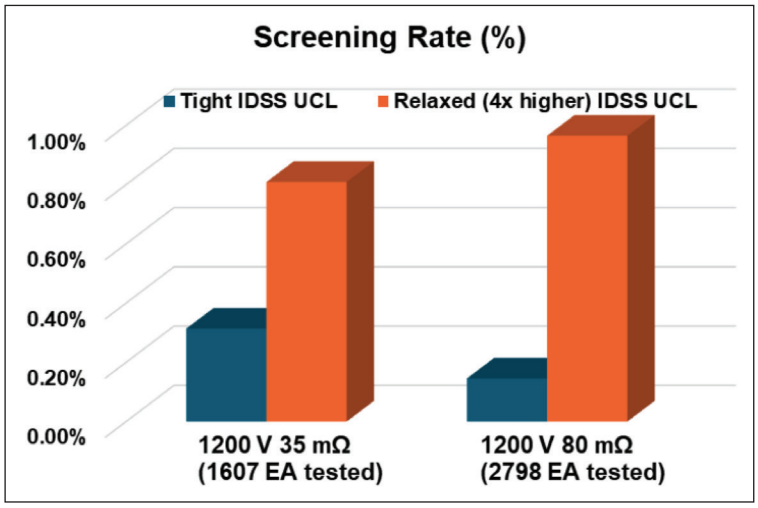
Jang and co-workers have undertaken constant-voltage TDDB tests of devices that have undergone screening, to see if this impacts infant failure, extrinsic failure, and intrinsic lifetime of the gate oxide. These investigations found that: screening did not degrade the intrinsic lifetime of the gate oxide; that after unclamped inductive switching, one infant failure in 80 devices occurred; and that no infant failures occurred after high-voltage pulse tests.

"It should be acknowledged that a sample size of 80 devices is insufficient to make definitive conclusions regarding statistical distributions, [but] the combined results from both the unclamped-inductive-switching-tested and the high-voltage-pulse-tested groups allow for a qualitative interpretation," argued Jang. "Specifically, unclamped inductive switching alone cannot screen out infant failures," added Jang, who pointed out that direct gate stressing under high-voltage pulse conditions proved to be more effective.

When it comes to extrinsic failures, the screening tests are not that effective, warned Jang, who added that only the HVP3 condition has a positive influence – that involves applying a field of 8.6 MV cm^{-1} for 1 s.

To avoid excessive negative shifts in threshold voltage and minimise excessive stress associated with unclamped inductive switching, Jang and co-workers adopted the 'combo' condition (defined in Table 2) for baseline screening. They used this to test a larger sample size, consisting of 1,607 MOSFETs with an on-resistance of 30 mΩ, and 2,798 with an 80 mΩ on-resistance.

The use of a tighter condition for screening produced a yield drop of around 1 percent compared with the more relaxed variant. This is a small trade-off against the benefit of screening-out potential risk factors.



➤ Figure 11. A comparison of the screening rate with tight and relaxed I_{DSS} unclamped inductive switching criteria.

Results (see Figure 11) show that the I_{DSS} criteria effects the screening rate. Many failures of high I_{DSS} devices during HVP1 and unclamped inductive switching indicate that leaky devices are vulnerable not only to unclamped inductive switching, but also gate oxide reliability.

Jang and colleagues have speculated that it is local defects, which contribute to a high I_{DSS} leakage, that are responsible for failures during both the high-voltage pulsed and unclamped inductive switching tests, as these defects may lead to non-uniform gate oxide formation and a non-uniform avalanche current distribution. The team plans to investigate this matter.

The use of a tighter condition for screening (see Figure 11) produced a yield drop of around 1 percent compared with the more relaxed variant. According to the team, this is a small trade-off against the benefit of screening-out potential risk factors. These insights into screening, along with the greater knowledge of the impact of oxide electric field stress, substrate material and gate oxide architecture, will help to refine the production of SiC MOSFETs. As well as the increase in availability over the coming years, customers are destined to get their hands on better products.

Strain modulation techniques for enhancing LED efficiency

By promoting the heteroepitaxy of high-efficiency LEDs in the UV and the red, strain modulation is accelerating the development of III-nitride optoelectronics

BY XINQIANG WANG FROM PEKING UNIVERSITY

GaN and its related alloys are continuing to attract tremendous attention in optoelectronics due to their excellent material properties. Strengths of these III-nitride semiconductors include a continuously tuneable bandgap, high electron mobility, superior radiation resistance, and excellent thermal stability. Such characteristics make this materials system ideal for producing a broad range of devices – and in particular light emitters, such as LEDs and lasers – that can serve in many different applications.

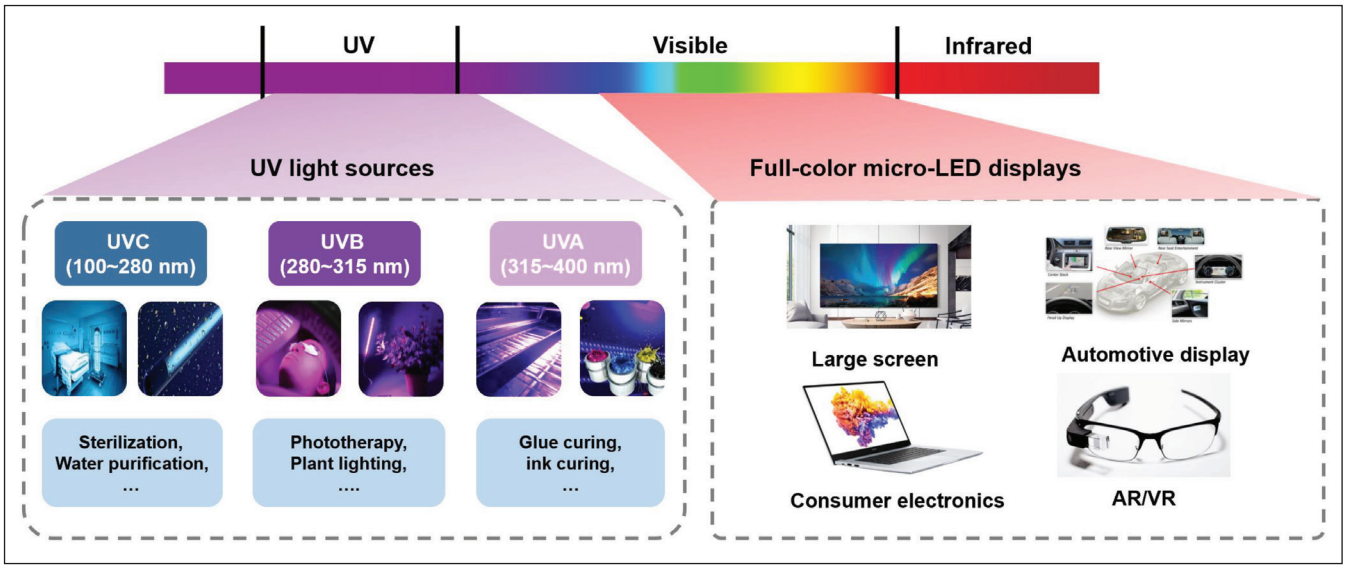
Within the III-nitride optoelectronic industry, the most notable triumph is the development of the InGaN-based blue LED. This device has revolutionised solid-state lighting, creating a market that's worth tens of billions of dollars per annum and making significant contributions to global energy conservation and carbon reduction. Beyond lighting, the applications of III-nitride optoelectronics are diversifying. Currently, this expansion is focusing more and more on AlGaN alloys and high-indium-content InGaN alloys, materials that are enabling technologies such as UV light sources and microLED displays. There is growing demand for more efficient AlGaN-based UV LEDs and InGaN-based red LEDs, a pair of goals driving much progress.

Lattice strain challenges

Compared with blue LEDs, those emitting in the red and UV are held back by greater strain in the active region. This gets more severe when increasing the gallium content in AlGaN-based UV LEDs, and increasing the indium content in InGaN red LEDs. In both cases, the strain, which degrades crystal quality, stems from differences in the lattice mismatch and the thermal expansion of the active layers and the substrate.

With AlGaN-based UV LEDs, lattice mismatch between the AlGaN layers and AlN templates generates compressive stress in the AlGaN films, leading to high dislocation densities and surface roughening in the active region. Due to these impediments, there is a reduction in the efficiency and the stability of the devices.

Similarly, for InGaN-based red LEDs, incorporating more indium results in a significant lattice strain and ultimately poor crystal quality. When these weaknesses arise, quantum efficiency plummets, the emission peak broadens, and the emitter is plagued by a severe efficiency droop. Compounding these issues, lattice strain also causes substantial wafer bowing, particularly in LEDs grown on large-sized substrates. This deformation threatens to lead to non-uniform emission wavelengths across



➤ Figure 1. The application fields for III-nitride optoelectronics are expanding to AlGaN alloys and high-indium-content InGaN alloys, such as UV light sources and microLED displays.

the wafer, and process challenges during chip fabrication.

The key to addressing these challenges is strain modulation. By carefully managing strain between the epitaxial structures and substrates, it is possible to improve the crystalline quality of the materials and enhance the overall performance of III-nitride optoelectronic devices.

Our team at Peking University is employing this strategy. By adopting this approach, we are making significant strides in improving AlGaN/AlN and InGaN/GaN systems, a critical step to increasing the efficiency of AlGaN-based UV LEDs and InGaN-based red LEDs.

AlGaN strain strategies

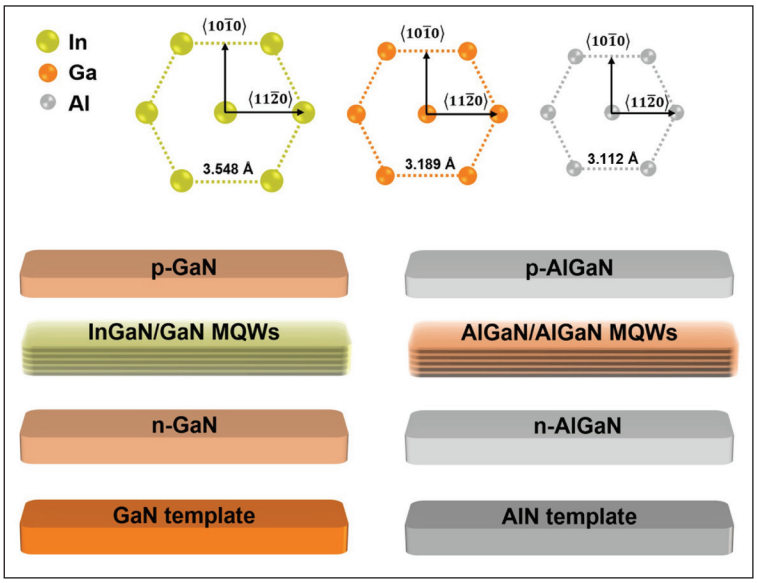
For AlGaN UV LEDs, which are typically grown on AlN templates, AlGaN strain-modulation strategies aim to mitigate the compressive stress. This can be realised by adjusting the strain state of the AlN template, and by incorporating a strain-modulation buffer layer.

We alleviate the compressive stress in our AlN templates by high-temperature annealing, in the range 1600°C to 1800°C. This annealing step enhances the recrystallisation of AlN, and improves the in-plane orientation consistency of AlN columns, which are usually fabricated by physical vapour deposition. After high-temperature annealing, the dislocation density within our AlN templates is significantly reduced, ensuring improved crystal quality.

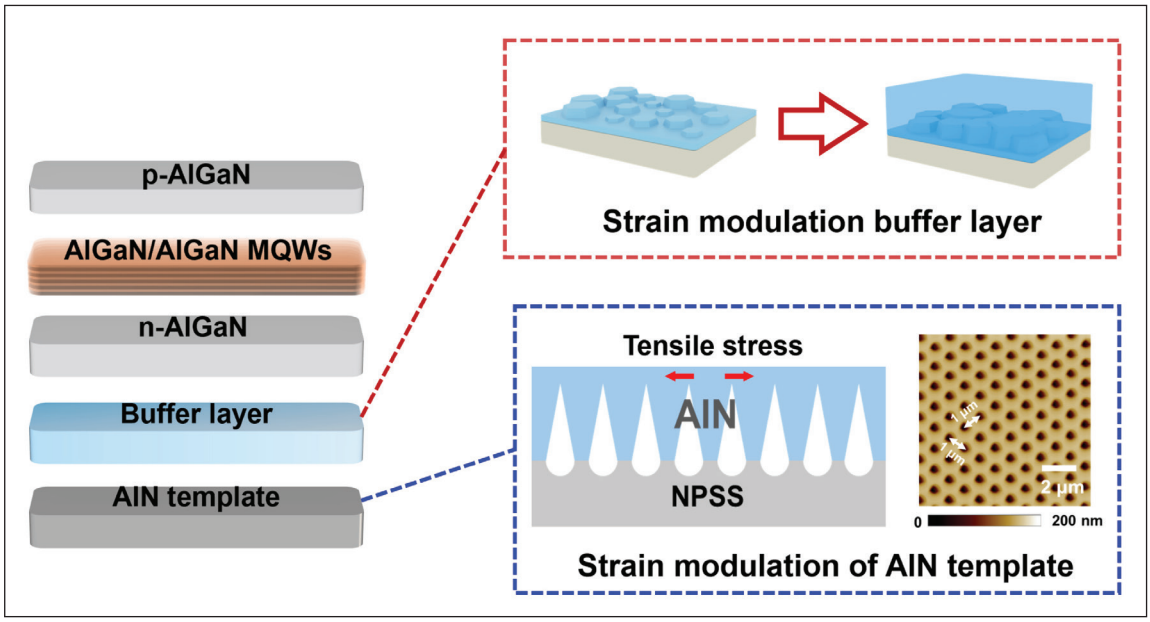
Further gains are realised by applying oxygen plasma irradiation to the sapphire substrate prior to AlN deposition, with this process improving the surface morphology of the high-temperature annealed AlN templates.

According to atomic force microscopy measurements over a 2 μm by 2 μm area, our 50 nm-thick high-temperature-annealed AlN template has a root-mean-square roughness of approximately 0.2 nm. We have also evaluated the quality of our templates with X-ray diffraction rocking curves, obtaining values for the full-width at half-maximum for the (002) and (102) planes of 51 arcsecs and 140 arcsec, respectively. These very low values highlight the superior quality of our high-temperature-annealed AlN templates, compared with conventional AlN templates.

Note that we have also shown that by adjusting the thickness of our templates, we can gradually shift



➤ Figure 2. The InGaN/GaN and AlGaN/AlN systems face similar issues of compressive stress, because both involve incorporating larger atoms into a host lattice composed of smaller atoms, such as embedding indium into GaN or gallium into AlN.



➤ Figure 3. The strain modulation strategy of AlGaN-based UV LEDs can be implemented by either adjusting the strain state of the AlN template or by introducing a strain-modulation buffer layer.

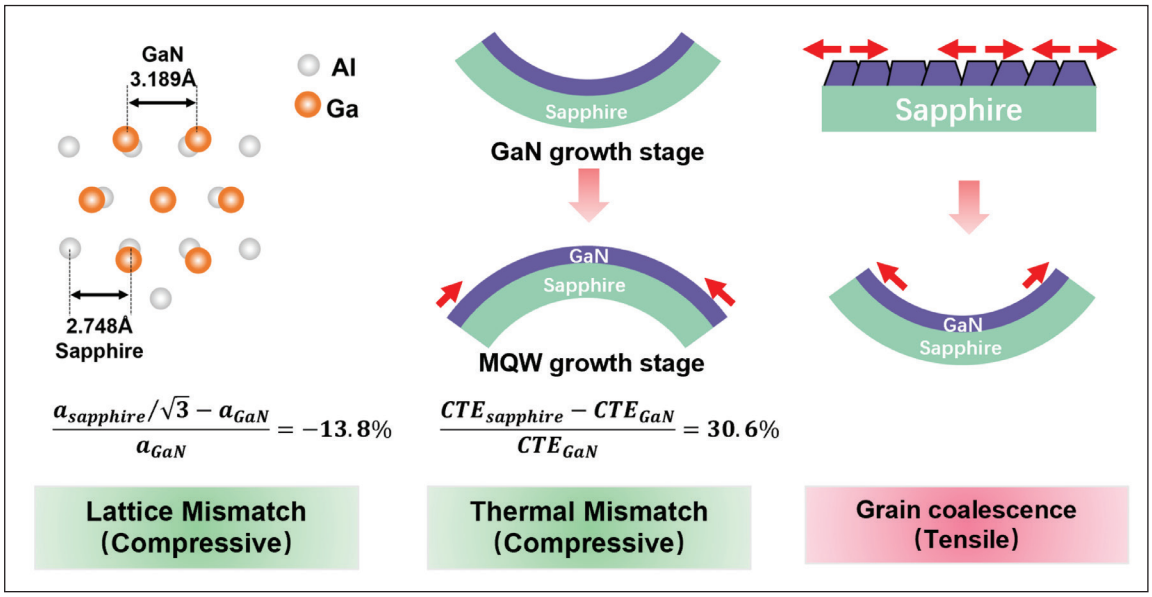
the strain state of our AlN films from compressive to tensile. This 'lever' allows us to significantly improve our surface morphology, and enhance the overall performance of our AlGaN-based UVC LEDs that we grow on this foundation.

The AlGaN UVC LEDs that we have fabricated on our ultra-thin, high-temperature-annealed AlN templates exhibit excellent luminous efficiency and reliability. By optimising the strain state and controlling the crystalline quality of this engineered platform, our 0.5 mm by 0.5 mm AlGaN UVC LED chip produces a wall-plug efficiency of 3.95 percent at a peak wavelength of 278 nm. After 1,000 hours of aging, the light output power remains at 91 percent of its initial value.

What's also appealing with this approach is that compared with traditional UVC-LED structures, we trim the epitaxial cost of this emitter by 60 percent, thanks to the use of our ultra-thin template. This significant cost saving makes our form of UVC LED more economically feasible for commercial production.

Another option for effective strain modulation in AlGaN UV LEDs involves the use of AlN templates grown on nano-patterned sapphire substrates. Introducing nano-scale patterns results in a periodically arranged array of holes or pillars in the AlN films during the early growth stages. When these AlN nanostructures coalesce, they provide a mechanism for strain modulation. Influencing the stress state within the AlN film are a number of factors, including the type and size of the pattern. We have found that using hole-textured nano-patterned sapphire substrates induces greater tensile stress during the coalescence of AlN nanostructures, compared with pillar-textured nano-patterned sapphire substrates.

For the hole-textured nano-patterned sapphire



➤ Figure 4. Lattice and thermal mismatches lead to compressive strain in heteroepitaxial GaN films on sapphire, while grain boundary coalescence induces tensile strain.

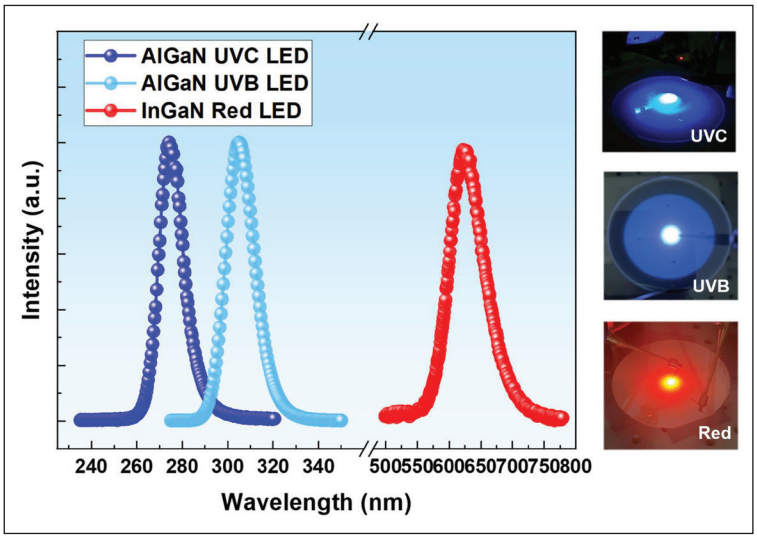
substrates, the diameter of the hole governs the stress state of the AlN template. As the size of the holes decreases from 750 nm to 550 nm, the AlN film transitions from a compressive to a tensile stress state. The nature of this stress influences surface morphology and the performance of AlGaN-based UV LEDs. By optimising the hole diameter – it is ideally 600 nm – we strike a balance between promoting a smoother surface morphology for AlGaN-based UV LEDs, and minimising crack formation in the AlN template.

We have found that the opportunity to fine-tune the hole diameter is especially beneficial for the development of high-performance AlGaN-based UV LED chips. Using hole-textured nano-patterned sapphire substrates, we have produced AlGaN-based UVB LED chips with dimensions of 0.5 mm by 0.5 mm that produce a wall-plug efficiency of 3.27 percent at a peak wavelength of 303.6 nm, and a light output power of 57.6 mW at 800 mA. The devices also have promising reliability, with an L70 lifetime of approximately 7800 hours, and the light output power retaining 83 percent of its initial value after 1,000 hours of aging. Another significant result with our hole-textured nanopatterned sapphire technology is a wall-plug efficiency exceeding 6.5 percent for our UVC LED chips. Taken together, these results highlight the significant potential of this approach for advanced optoelectronic applications.

It's also possible to use a strain modulation buffer layer to manage the strain in AlGaN-based UV LEDs. One promising approach involves an AlN transition layer, comprising a three-dimensional (3D) island-like AlN layer, followed by a two-dimensional (2D) continuous AlN recovery layer. Through homo-epitaxial growth of the 3D-2D transition layer on our high-temperature-annealed templates, we can ensure that the 3D-grown AlN islands maintain a consistent *c*-axis orientation. We observe that during the 2D AlN recovery process, tensile strain is introduced via grain coalescence, successfully converting the initial compressive strain into tensile strain. This is a valuable transformation, enhancing the surface morphology of our AlGaN-based UV LEDs. Drawing on this benefit, we have produced crack-free 4-inch UVC-LED wafers with an outstanding performance. Devices with dimensions of 0.25 mm by 0.5 mm deliver an output power of 14 mW at 275 nm, under a forward current of 100 mA. This success underscores the significant potential of the 3D-2D AlN transition layer for advancing the performance and scalability of UVC LEDs.

InGaN strain strategies

The challenges faced by engineers developing and producing AlGaN-based UV LEDs also impede the progress of the pioneers of InGaN-based red LEDs. In both cases, compressive stress is an issue, arising from the incorporation of larger atoms into a host lattice composed of smaller atoms – such as indium into GaN or gallium into AlN.



➤ Figure 5. High-efficiency UVC, UVB, and red LEDs have been realised by implementing adaptive strain-modulation strategies tailored to the AlGaN/AlN and InGaN/GaN systems.

For InGaN-based red LEDs, the strain-related issues are more severe than those for AlGaN-based UV LEDs, due to the greater lattice mismatch between InGaN and GaN. Compressive stress from the underlying GaN layers limits indium incorporation during the epitaxy of high-indium-content InGaN materials, leading to poor crystalline quality, phase separation, surface segregation, and other detrimental effects.

According to theoretical calculations, indium incorporation is more favourable when the GaN lattice is under tensile strain. Unfortunately, such conditions do not occur during heteroepitaxy on substrates such as sapphire, as this tends to induce compressive strain in GaN films, due to lattice and thermal mismatches. Consequently, the primary strategy for strain management in InGaN-based red LEDs involves either relieving compressive strain or inducing tensile strain in the underlying heteroepitaxial GaN films.

To effectively modulate the strain in heteroepitaxial GaN films, we have turned to a composite buffer structure, grown on sapphire, that leverages the tensile stress generated during grain coalescence. Our composite buffer consists of a sputtered AlN nucleation layer, followed by a low-temperature GaN layer, grown by MOCVD. The sputtered AlN nuclei exhibit excellent *c*-axis orientation, while the low-temperature GaN layer forms numerous 3D GaN islands, originating from these AlN nuclei and separated by grain boundaries. During subsequent growth, adjacent GaN islands coalesce as they seek to minimise surface-free energy, which outweighs the formation energy of the grain boundaries. This coalescence process stretches the crystallites, generating tensile stress within the low-temperature GaN buffer layer. This tensile stress significantly enhances indium incorporation in

InGaN-based red LEDs, addressing a key challenge associated with compressive strain in high-indium-content materials.

Unfortunately, simply managing strain in the underlying GaN layer is insufficient to ensure high-performance InGaN-based red LEDs, due to the significant lattice mismatch in these devices. What's also needed is additional strain modulation, realised through the structural design of the active region.

Our research reveals a substantial deterioration in the quality of InGaN-based red quantum wells when two or more are grown consecutively. To address this, one can introduce structures such as InGaN/GaN superlattices that provide strain modulation in the high-indium-content active region. This approach significantly mitigates the degradation of epitaxial quality.

As well as adopting this approach, we have developed a periodic quantum-well structure that feature alternating cycles of high- and low-indium compositions. Our experimental results confirm that this design significantly improves the performance of InGaN red LEDs.

To tackle indium surface segregation caused by stress, and to enhance the sharpness of the active region interfaces, we have introduced an AlGaN/GaN confinement layer that follows the InGaN-based red quantum well. Note that we have found that it is crucial to optimise the growth temperature of this confinement layer, as this ensures uniform confinement of indium atoms within the wells. Our investigations show that the confinement layer plays a pivotal role in enhancing the electroluminescence intensity of InGaN-based red LEDs.

Deploying these innovative strain-modulation strategies has enabled us to produce promising InGaN-based red LEDs on 4-inch sapphire substrates. Our InGaN-based red mini-LED chips operate with a working current density of around just 0.5 A cm^{-2}, have an external quantum efficiency of about 7.4 percent, and have a peak wavelength of around 629 nm. We have successfully integrated these chips into a full-colour nitride-based mini-LED display, covering 74.1 percent of the Rec. 2020 colour gamut. These results underscore the tremendous potential of InGaN-based red mini/microLEDs in high-resolution, full-colour advanced display applications.

By systematically exploring strain modulation strategies for both the AlGaN/AlN and InGaN/GaN systems, we have demonstrated high-efficiency LEDs emitting in the UVC, UVB, and red spectral domains. This success, realised by precisely tailoring the strain through substrate patterning, growth mode transitions, and epitaxial structure design, highlights the critical role of strain engineering in III-nitride semiconductor heteroepitaxy and its significance for advancing III-nitride optoelectronics.

FURTHER READING / REFERENCE

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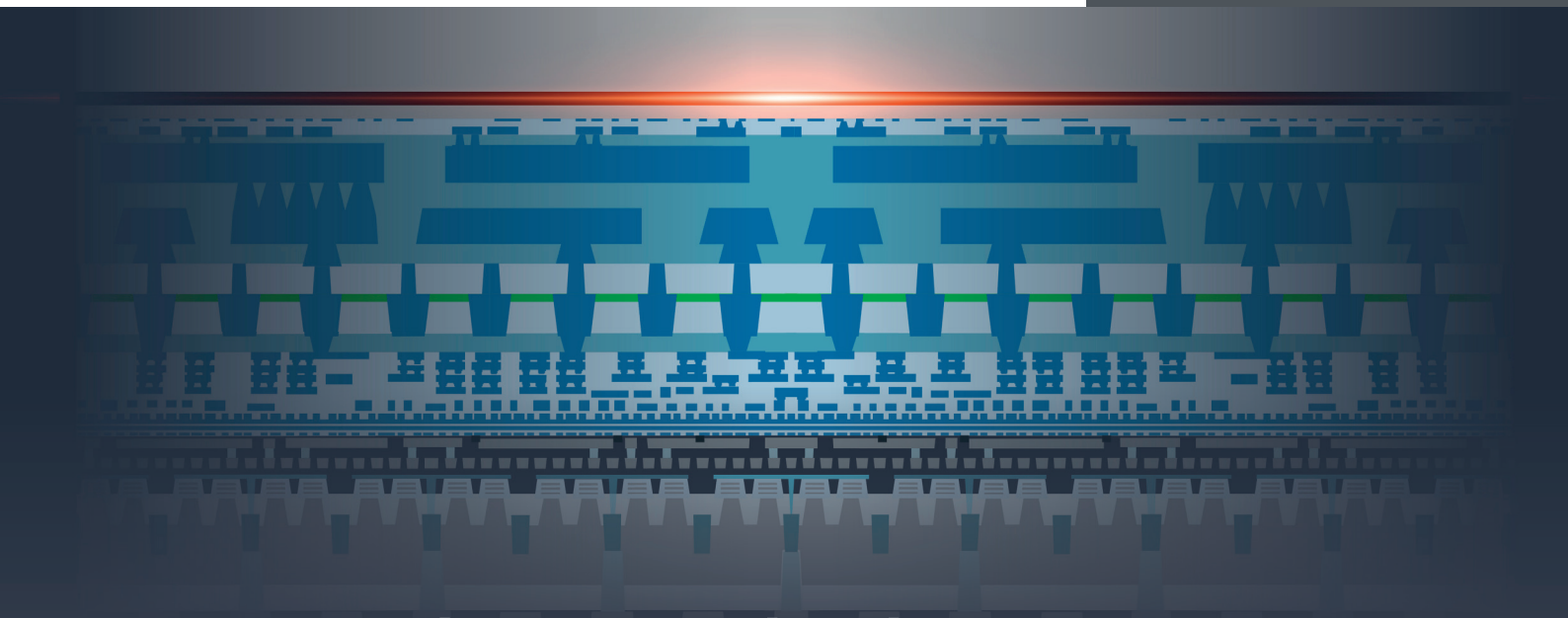

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GaN wafer under photoluminescence testing by Alireza Lajani at SUNY-Albany's Wide BandGap Optronix.

GaN: The quest for *Be*-tter *p*-doping

One promising option for enabling effective *p*-type doping in GaN and its related alloys is to introduce beryllium, possibly in the form of impurity complexes

BY F. SHADI SHAHEDIPOUR-SANDVIK AND BENJAMIN MCEWEN FROM THE STATE UNIVERSITY OF NEW YORK-ALBANY AND DENIS DEMCHENKO AND MICHAEL RESHCHIKOV FROM VIRGINIA COMMONWEALTH UNIVERSITY

SALES of GaN-based semiconductor devices are on the up, driven by increased deployment in consumer electronics and integration within the automotive industry. According to market analyst Global Market Insights, revenue from GaN devices is forecast to climb at a compound annual growth rate of 6.8 percent until 2034, from over $22 billion in 2024.

Spurring this considerable success is the great set of properties of this wide bandgap semiconductor. GaN is renowned for its high-power efficiency, its excellent thermal management, and its support for miniaturisation. Today, it's hard to imagine a world without the first multi-billion-dollar GaN device, the LED. It's certainly fair to say it would not be as bright. Without this game-changing emitter, many energy-efficient applications that humanity has been enjoying for nearly three decades would not have emerged at the same pace.

Underpinning all this progress is the work of Hiroshi Amano and his colleagues, who made a pivotal breakthrough in GaN technology, demonstrating that the *p*-type doping of GaN is possible. Realising this is a crucial step to the development of the LED, a class of *p-n* diode that put GaN on the map.

Despite the remarkable success of GaN technology from the 1990s onwards, *p*-type doping is still suboptimal. In most GaN-based devices, around just 1 percent of the magnesium acceptor dopant in the *p*-type layer produces free holes – that's two orders of magnitude lower than the total magnesium concentration. In sharp contrast, acceptors in silicon exhibit nearly complete activation at room temperature.

Note that conductive *p*-type III-nitride materials are not just needed for LEDs. Realising *p*-type doping in the family of GaN materials, which includes AlN and AlGaN alloys, is essential for next-generation bright deep-ultraviolet LEDs

(DUV LEDs), high-power electronic devices, and UV photodetectors.

DUV LEDs are particularly promising for combating pandemics, disinfecting water sources, and sterilising surfaces. However, today's commercial DUV LEDs emitting within the germicidal wavelength range, which spans 254 nm to 285 nm, have efficiencies below 5 percent and cost about 100 times more per watt than mercury vapour lamps. Meanwhile, in the wavelength range of 220 nm to 250 nm, the external quantum efficiency of DUV LEDs is even lower, below 1 percent.

A significant limitation in AlGaN-based devices, including those associated with DUV LED technology, is the absence of a low-resistivity *p*-type layer. While magnesium remains the only viable acceptor, its ionisation energy (E_A) is relatively high. In GaN, it's 0.22 eV, a value that increases with the bandgap of the III-nitride alloy, rising to 0.5-0.6 eV in AlN. Due to this, magnesium doping is inefficient.

To address this issue, some research teams have turned to alternative approaches, such as superlattice structures and polarisation-induced hole doping. However, there are downsides to these methodologies, including lower vertical conduction compared with lateral conduction. Due to these drawbacks, there is tremendous demand for uncovering a shallower acceptor in GaN, AlN, and AlGaN that offers a lower ionisation energy than magnesium.

A beryllium boost?

Offering one potential solution is the replacement of the magnesium acceptor with beryllium, which is routinely used as an acceptor dopant in other III-Vs, such as GaAs. This approach has much promise, given that theoretical and experimental evidence suggests that beryllium has a shallower acceptor level than magnesium in (Al)GaN.

Beryllium, a group II element directly above magnesium, is a divalent atom that's a suitable acceptor dopant in III-V materials when it substitutes for group III elements. According to early density functional theory calculations in the late 1990s by Fabio Bernardini and co-workers from the University of Cagliari, Italy, the beryllium acceptor level is less than 100 meV above the GaN valence band maximum. Experimental evidence broadly confirmed these predictions. However, beryllium-doped GaN, often almost exclusively grown by MBE at relatively low temperatures, tends to exhibit semi-insulating behaviour.

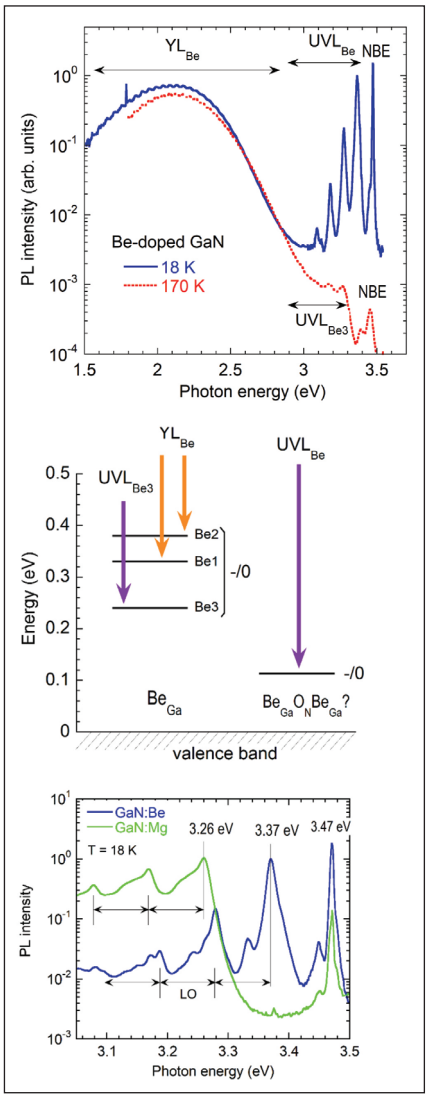
Under a National Science Foundation grant, our team from the University of Albany and Virginia Commonwealth University has pioneered a systematic approach to growing beryllium-doped GaN using MOCVD, the most widely used growth system in the manufacture of III-nitride devices. Due to higher growth temperatures compared with MBE, MOCVD-grown GaN has dislocation densities that are generally about an order of magnitude lower, making this epitaxial technology an attractive choice for the development of novel doping methods.

With MOCVD, the biggest challenge is that the beryllium source cannot simply be metallic, as is the case in MBE. What's more, due to the high toxicity of beryllium metal-organics, precursors for MOCVD are difficult to obtain, making beryllium implantation a potentially attractive doping process for those wanting to take advantage of MOCVD's good material quality, high throughput, and scalability. However, ion implantation induces material damage and donor-defects, making it extremely difficult to obtain *p*-type III-nitrides without the use of in situ doping.

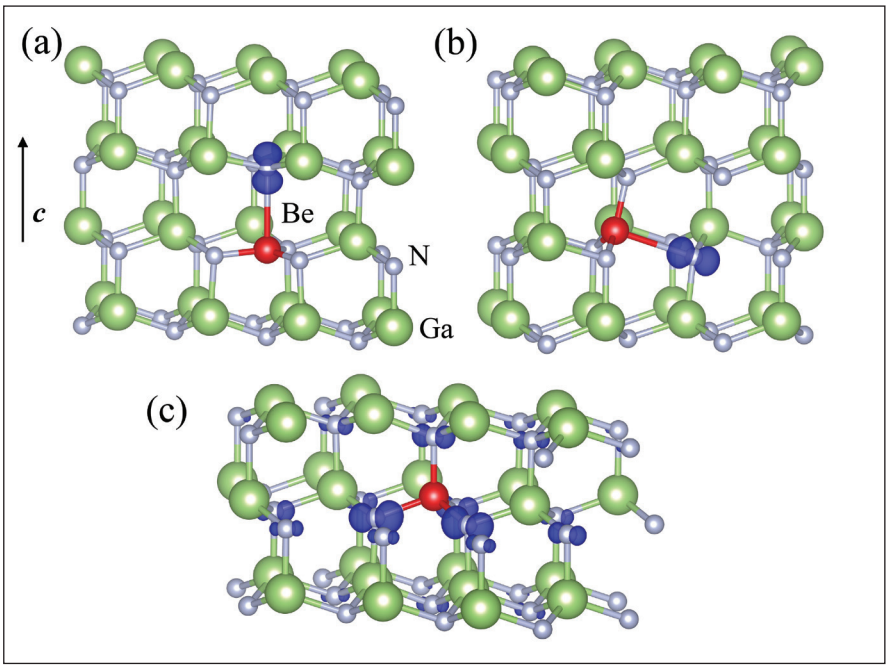
Breaking new ground, we have used beryllium acetylacetonate (Be(acac)2) as a beryllium precursor and developed MOCVD growth processes for *in situ* doping that maintain a high material quality and a relatively low compensation.

Note that we are enthused by recent work from Alan Doolittle's team from Georgia Institute of Technology, involving beryllium doping of AlN via metal-modulated MBE. This team has demonstrated conductive *p*-type AlN, realising room-temperature hole concentrations and conductivity of up to 4.4 x 10^{18} cm^{-3} and 0.045 Ωcm, respectively.

We have undertaken extensive photoluminescence studies of our MOCVD-grown, beryllium-doped samples. We routinely observed the presence of the UVL_{Be} band, indicating a beryllium-related shallow acceptor with an ionisation energy of 113 meV in our GaN. Initially, we mistakenly



➤ Figure 1. (a) Photoluminescence spectra from beryllium-doped GaN. (b) Electron transitions to beryllium-related states. The polaronic states of Be_{Ga} (Be1 and Be2) are responsible for the broad yellow luminescence (YL_{Be}) band with a maximum at about 2.15 eV, whereas transitions via the Be_{Ga} shallow state (Be3) can be observed only at temperatures above 100 K as an ultraviolet luminescence band with the zero-phonon line at around 3.26 eV (labelled UVL_{Be3}).



➤ Figure 2. Charge density of the hole localized on the neutral beryllium acceptor in GaN. (a) Deep polaronic state localized along Be-N bond in the *c*-direction of the wurtzite GaN (labeled Be2 in Figure 1); (b) in-plane deep polaronic state (labeled Be1 in Figure 1); (c) shallow state (labeled Be3 in Figure 1).

attributed this to the isolated Be_{Ga} acceptor. However, our subsequent photoluminescence studies have provided us with compelling evidence that Be_{Ga} is a dual-nature acceptor, featuring: two polaronic deep states, located at 0.38 ± 0.03 eV and 0.33 ± 0.05 eV above the valence band minimum; and a shallow state, with a delocalised hole at 0.24 ± 0.02 eV above the valence band minimum (see Figure 1).

Through photoluminescence studies of over fifty beryllium-doped GaN samples grown by MOCVD and MBE, we have demonstrated that the UVL_{Be} band at 3.38 eV – the signature of a shallow beryllium-related acceptor in GaN – cannot be attributed to isolated Be_{Ga}. Nevertheless, the defect responsible for the 3.38 eV band clearly contains beryllium and exhibits features of the shallowest acceptor in GaN. This suggests that conductive *p*-type beryllium-doped GaN is feasible, if one can understand the nature of the shallowest acceptor (E_A of 113 meV) in beryllium-doped GaN. Recently, using hybrid density functional calculations, we have proposed that this could be the $Be_{Ga}O_NBe_{Ga}$ complex (see Figure 1). Figure 2 shows the charge densities of the hole localized on the two polaronic states (a, b) and the shallow state (c) in the crystal lattice of GaN, calculated using the hybrid density functional theory.

Another promising strategy for achieving conductive *p*-type GaN is co-doping. We expect that co-doping with beryllium and oxygen could lead to an abundance of $Be_{Ga}O_NBe_{Ga}$ acceptors, with a concentration exceeding that of compensating donors. It's possible that high concentrations of mobile gallium vacancies will facilitate the formation of the complexes during MOCVD growth in nitrogen-rich conditions.

There's also a promise associated with strain-enhanced doping. For example, indium, often used as a surfactant, might induce compressive strain during growth, offsetting the tensile strain from beryllium incorporation. Due to the highly volatile nature of indium at common MOCVD GaN growth temperatures, typically more than 900°C, little to no indium incorporates into GaN, making it an excellent surfactant that affects growth without incorporating into the material.

To unlock the full potential of III-nitride semiconductors, our community must overcome the persistent challenge of *p*-type doping. Ultra-wide bandgap materials, such as AlGaN, represent a particularly promising frontier, especially given their foundational ties to the advancements already made with GaN. However, magnesium-doping alone cannot produce *p*-type aluminium-rich AlGaN or AlN, due to the high acceptor depth of magnesium in these materials.

Our preliminary research suggests that beryllium, possibly in the form of impurity complexes, could hold the key to enabling high-efficiency, conductive *p*-type (Al)GaN. Theoretical studies and experimental evidence both point toward beryllium-related shallow acceptors as a critical component in this pursuit.

While *p*-type doping in GaN and its alloys remains a complex puzzle, it's also an exciting opportunity. Advancing this field could catalyse a new wave of technological innovation, with applications ranging from next-generation displays to energy-efficient power electronics and life-saving DUV LEDs. If history has shown us anything, it's that the brightest ideas often come from solving the toughest problems – and we're optimistic that this challenge will be no exception.

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A GaN-on-silicon foundation for Ga_2O_3 transistors

GaN buffer underpins high-voltage, normally-off Ga_2O_3 transistors

ENGINEERS from King Abdullah University of Science and Technology are claiming to have unveiled the first Ga_2O_3 transistors grown on GaN-on-silicon.

According to these researchers, turning to this particular form of heterogeneous integration allows the Ga_2O_3 transistor to retain its strengths, including a very high breakdown field that makes it a very promising device for power electronics, while potentially addressing its weaknesses – it is held back by a low thermal conductivity and inefficient *p*-type doping. What's more, this combination of materials could open the door to large-scale manufacturing.

When considering the various material options for underpinning the Ga_2O_3 transistor, the team dismissed SiC. While this substrate has a high thermal conductivity, it is expensive and incompatible with silicon process technology, hampering monolithic integration

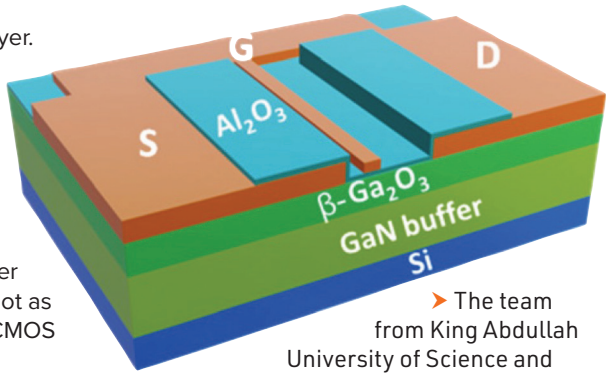
The team from Saudi Arabia view their combination of a Ga_2O_3 transistor, a GaN buffer, and a silicon substrate as a compelling one, because it is more scalable, more cost-effective, and it avoids compromising performance.

By adopting this approach, devices benefit from the strengths of GaN, including its high thermal conductivity. In addition, according to team spokesman Xiaohang Li, it's possible that *p*-type GaN might be able to tackle the poor *p*-type doping in Ga_2O_3.

Another asset of this combination is that it could create monolithic ICs that feature: high-speed control circuitry, drawing on the superior mobility of GaN; and high-power devices, produced from Ga_2O_3.

To fabricate their devices, Li and co-workers began by using pulsed laser deposition (PLD) to grow a roughly 50 nm-thick film of silicon-doped Ga_2O_3 on a semi-insulating 4.7 μm-thick GaN buffer layer.

Explaining this choice of growth technology, Li remarks: "PLD has proven to be a viable tool to grow high-quality epitaxial Ga_2O_3. MOCVD may offer moderately better materials, but MOCVD is not as compatible to the silicon CMOS process as PLD."



➤ The team from King Abdullah University of Science and Technology claim that their β-Ga_2O_3 MOSFETs break the record for breakdown voltage for this class of device on silicon substrates.

Electrical measurements determined that the film of Ga_2O_3 has an electron concentration of around 1.2×10^{18} cm^{-3}, and a mobility of just 2.1 cm^2 V^{-1} s^{-1}. Low mobility is attributed to the polycrystallinity of the Ga_2O_3 layer and defects induced by lattice mismatch.

It's claimed that mobility can be increased by adopting advanced growth techniques, such as MOCVD, and applying post-growth high-temperature annealing, which enhances crystallinity and reduces defect density.

To fabricate devices, Li and co-workers added source and drain Ti/Au terminals to their epistructure, before depositing a 25 nm-thick Al_2O_3 gate dielectric by atomic layer deposition, adding a gate metal, and then using reactive ion etching to open up source and drain pads. Transistors produced with this process have a gate length of 4 μm, a source-to-gate separation of 3 μm, and a gate-to-drain distance of 18 μm.

Electrical measurements on these devices enabled the team to calculate a sub-threshold swing of 167 mV dec^{-1} – a value that indicates a high-quality interface between Ga_2O_3 and Al_2O_3 – and determine an on-off ratio of around 10^6. At a gate-to-source voltage of 8 V, the off-state gate leakage current is around 10^{-7} mA mm^{-1}, and at a drain-source voltage of 5 V the threshold voltage is 3 V, enabling fail-safe operation.

The breakdown voltage, measured at a gate-source voltage of 0 V, has a maximum value of around 540 V. According to the team, this is the highest value for β-Ga_2O_3 MOSFETs on silicon substrates.

One alternative to the team's β-Ga_2O_3 MOSFETs on GaN-on-silicon substrates are variants produced on AlN-on-silicon. Earlier this year, such devices were reported by a collaboration led by researchers at National Chung Hsing University.

"That's a very nice work," says Li. However, he argues that there are a number of issues with β-Ga_2O_3 MOSFETs on AlN-on-silicon, including a rough surface morphology, depletion-mode operation, and a lower breakdown voltage.

"In addition, AlN-on-silicon is prone to cracks, and it is not as mature as GaN-on-silicon as a platform," adds Li. However, he believes that with more development, it is possible that AlN-on-silicon can become a good platform.

Li says that the next goals for the team include developing various power technologies associated with Ga_2O_3-on-silicon, through the use of GaN, as well as integration with *p*-GaN.

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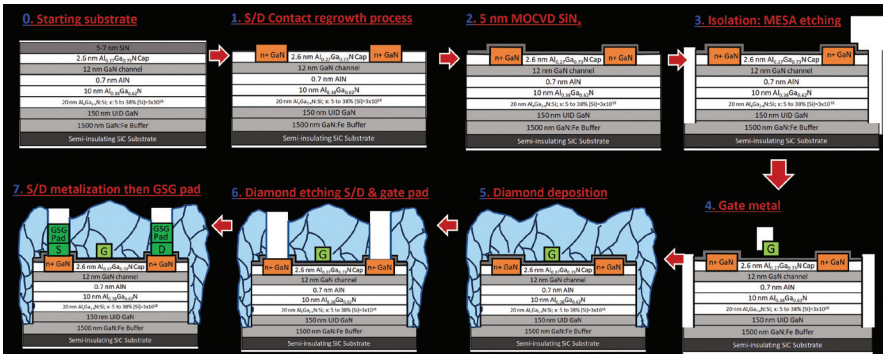
Cooling RF GaN HEMTs with all-around diamond

Low-temperature diamond growth and a gate-first approach produce devices with great potential to minimise self-heating

ENGINEERS from Stanford University are claiming to have broken new ground with the first post-process diamond integration of a GaN HEMT. It is argued that this approach, which wraps a 150 mm N-polar GaN MIS-HEMT in diamond, will provide a valuable platform for the thermal management of X-band GaN HEMTs using diamond heat spreaders.

This team's work is one of a number of approaches, developed over many years, for addressing self-heating in GaN HEMTs – this is an issue that impacts this device's performance and reliability.



➤ Stanford's latest approach to minimizing self-heating of the channel enables the fabrication of an all-around diamond N-polar GaN HEMT.

Many attempts to reduce self-heating involve trimming the thermal boundary resistance to the channel of the HEMT via backside integration of heat spreaders. Previous efforts have included growing GaN HEMT stacks on diamond substrates, transferring the substrate from sapphire to copper, and adding copper-filled micro-trenches.

One downside of all forms of backside integration is that the heat generated in the channel has to flow through the buffer and/or nucleation layers that tend to have a high thermal resistance.

To address this drawback, the team from Stanford integrates diamond on both the top and the sidewalls of the device's active area, enabling a route for heat extraction that bypasses the high-resistance buffer and/or nucleation layers.

The team's latest approach is its successor to its previous technologies, described as 'diamond first' and 'gate first'.

According to team spokesman Srabanti Chowdhury, those predecessors – the diamond-first and the gate-first processes – offer promising advantages over other approaches, and are each suited to different integration strategies.

Offering insights into both of them, Chowdhury remarks: "In the diamond-first process, lithography for the gate and other device regions must be performed directly on the diamond surface, which can be challenging – particularly at sub-micron scales."

He adds that in contrast, the gate-first process involves depositing diamond over a pre-defined gate structure, eliminating the need for gate lithography on diamond. Due to this, the gate-first process is the more manageable approach from a fabrication standpoint.

"However, the success of the gate-first approach hinges on the ability to grow diamond at sufficiently low temperatures to avoid degrading the electrical performance of the underlying gate stack," says Chowdhury. "When this condition is met, diamond integration over the gate becomes feasible and attractive."

The team's process, illustrated in the figure, begins with the formation of a GaN-on-SiC epistack by MOCVD, followed by the addition of source, gate and drain contacts, deposition of diamond, localised etching, and the addition of ground-signal-ground pads.

Chowdhury and co-workers have produced two forms of gate all-around HEMT, with diamond deposition at 500 °C and at 700 °C. "Growth at 700 °C is easier and more straightforward from a growth standpoint, but it is not practical for a gate-first process," explains Chowdhury, who points out that this temperature exceeds the thermal budget of the gate stack. "In contrast, with a 500 °C or lower temperature growth process, safe integration is achievable without such risks."

Devices produced using diamond deposition at 700 °C exhibit no gate modulation, due to a high gate leakage, stemming from the high growth temperature for diamond. Meanwhile, measurements on devices produced with diamond deposition at 500 °C reveal a threshold voltage of -8 V, an on-off ratio of 10^5, a peak transconductance of 190 mS mm^{-1}, and a drain saturation current of 0.96 mA mm^{-1}.

"Future research will focus on scaling this integration into larger device arrays and investigating long-term reliability under high-power operation," says Chowdhury, whose plans also include exploring integration with alternative gate architectures and packaging schemes, to further improve thermal and electrical co-optimisation. "Ultimately, our goal is to develop a scalable, manufacturable thermal integration strategy that enables high-power density, thermally reliable GaN devices for X-band and beyond."

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Scaling quartz-free HVPE of GaN-on-GaN epiwafers

Sumitomo Chemical targets the epiwafer market with 6-inch material produced in a quartz-free HVPE reactor that's designed for mass production

TO HELP increase the adoption of GaN power devices via a reduction in production costs, Sumitomo Chemical has developed a quartz-free HVPE reactor for mass production that can accommodate 6-inch substrates.

This latest triumph builds on previous successes by the Japanese company, which has shown that quartz-free HVPE can grow GaN layers with record room-temperature mobilities. Epilayers also feature very low background concentrations of silicon, oxygen and carbon.

Spokesman for the team, Ryota Ito, told *Compound Semiconductor* that the quartz-free HVPE technology is now very close to full optimisation. "The mobility at room temperature is close to theoretical values, and the impurity concentration is below the detection limit as measured by secondary ion mass spectrometry."

To underscore the capability of their new tool, engineers from Sumitomo Chemical have used their reactor to produce 4-inch and 6-inch GaN epiwafers. This involved the growth of a silicon-doped GaN layer, subsequently scrutinised by various characterisation techniques.

The 4-inch substrate employed in this study was produced internally, using the void-assisted separation method. This substrate had a uniform threading dislocation density of 1-3 x 10^6 cm^{-2} and an off-angle of 0.4°, tilted from the exact + *c*-plane towards the *m*-direction. "The off-cut angle is intentionally used to prevent the occurrence of hillocks," explains Ito.

For growth on 6-inch wafers, the team at Sumitomo Chemical turned to a GaN-on-sapphire template. Note, though, that 6-inch free-standing GaN substrates are under development.

Growth conditions employed included atmospheric pressure, a growth rate of approximately 1 μm min^{-1}, the use of ammonia and gallium monochloride as source gases, and a mixture of hydrogen and nitrogen for the carrier gas.

According to Fourier transform infrared spectroscopy, the silicon-doped GaN epilayer on the 4-inch native substrate has a thickness of 14.1 μm, with a standard deviation of 3.4 percent. Commenting on this, the team remarked in their paper that whereas conventional HVPE-grown GaN tended to exhibit a large thickness variation, the optimised quartz-free HVPE system led to a uniform distribution, similar to that of an MOCVD-grown epitaxial film.

For the growth of epiwafers on 6-inch templates, the thickness uniformity is a little higher, with a standard deviation of 4.4 percent.

To evaluate doping, the engineers at Sumitomo Chemical considered the difference between the density of donors and acceptors, determined by a non-contact capacitance-voltage instrument. For MOCVD-grown GaN on 100 mm free-standing GaN, the standard deviation is 14.3 percent – and for GaN grown by quartz-free HVPE on 100 mm free-standing GaN it's just 3.0 percent.

The team also conducted photoluminescence measurements on their latest GaN epilayers, and compared the spectra with that obtained for an equivalent sample produced with a prototype reactor. The film grown with the more recent reactor, designed for mass-production, produces stronger near-band-edge emission, thanks to suppression of carbon contamination. Also encouraging is a reduction in green luminescence, indicative of a reduction in the density of point defects – this is attributed to a superior reactor design that supresses the leakage of gas from/into the growth area.

To demonstrate carrier control in their quartz-free HVPE reactors, the engineers at Sumitomo Chemical varied the silicon source rate, with a step change for every 600 nm of GaN growth. Analysing the doping profile via secondary ion mass spectrometry determined that the doping level is constant in each layer, and at the interfaces there is a steep change in silicon concentration.

This investigation also showed that with the latest quartz-free HVPE reactor there is linear doping with silicon concentration, over a wide range from 1 x 10^{14} cm^{-3} to 1 x 10^{18} cm^{-3}.

As many power devices operate in the kilovolt range, controlling the carrier concentration in the range below 1 x 10^{16} cm^{-3} is critical. Excelling in this regard, Sumitomo Chemical's latest quartz-free HVPE reactor offers the capability to produce devices with breakdown voltages of 10 kV or more.

Sumitomo Chemical does not intend to produce and sell its quartz-free HVPE reactors. "We are a GaN substrate vendor, and we are planning to sell GaN-on-GaN epitaxial wafers produced by quartz-free HVPE," says Ito.

Today, Sumitomo Chemical is selling its GaN substrates with diameters of up to 4 inches, and is providing epitaxial wafers grown by quartz-free HVPE to device manufacturers and research institutions.

"Furthermore, we are developing 6-inch GaN substrates, and will soon be able to offer 6-inch GaN-on-GaN wafers," says Ito, adding: "Through this, we aim to contribute to the early establishment of the vertical GaN device market."

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