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Better blue and green lasers

Full-colour laser projectors and laser TVs are set to benefit from GaN-based lasers with impressive wall-plug efficiencies

A sound approach to cutting costs

The harnessing of acoustic energy promises to enable substrate re-use during the production of power electronics

Banishing barriers to GaN adoption

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VIEWPOINT

By Richard Stevenson, Editor

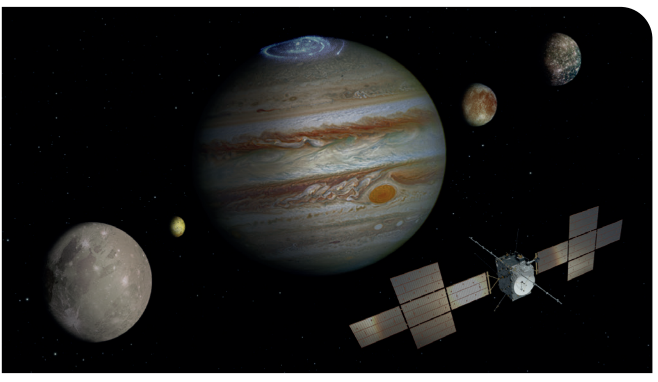
Providing the juice by Jupiter

WHEN we consider the performance of multi-junction solar cells, we tend to do so under one of two conditions. When these cells are used on Earth, we want to know how they perform under high levels of solar concentration, such as several hundred suns. And when they are deployed on a satellite orbiting the earth, we want to know what their efficiency is when they draw power from sunlight that has not travelled through our atmosphere, which causes varying degrees of attenuation.

But there's also a third condition. Right now, a craft is hurtling through space on a mission to Jupiter entitled JUICE – that's short for JUpiter Icy Moons Explorer. When this craft begins to gather data from these moons, power will come from multi-junction solar cells that are generating electricity from rays that are only around 3.5 percent of the intensity of those hitting Earth-orbiting satellites.

As well as the challenge of generating power from this weak sunlight, the maker of the cells that are going on that mission to Jupiter faced other difficulties. One is that the devices are bombarded by radiation, impairing their performance. This causes damage that is about 20 percent higher than that experienced by cells in a geo-stationary orbit, partly because the colder temperatures near Jupiter inhibit healing that comes from self-annealing. Fortunately, there's an also upside from the lower temperatures: increased efficiency, which hits 35 percent.

Providing the cells for the JUICE mission, which embarked this April and will not reach Jupiter until 2031, is Azur Space Solar Power, a company based in Germany that is now owned by the Canadian firm 5N Plus.



In this issue we talk to Azur's Director of Technology and Marketing, Wolfgang Guter, about the challenges associated with supplying the cells for this venture (see p. 14).

Given the low intensity of sunlight beside Jupiter, plenty of cells are required to generate the power that's needed for the craft. The JUICE mission involves 24,000 cells, each 30 cm^2 in size, that combine to cover an area of 85 m^2.

As well as being efficient, it is critical that every one of these cells is reliable. Azur has worked hard on this aspect, devoting much effort to gaining a thorough understanding of the degradation mechanisms of its cells when they operate under low intensity, low-temperature conditions.

Such efforts are already paying off. While it's not that surprising that a mission run by the European Space Agency (ESA) is using locally made cells, NASA is also using Azur's devices on its mission to Jupiter. So, hats off to Azur, given that the US is home to two of the world's leading makers of multi-junction solar cells.

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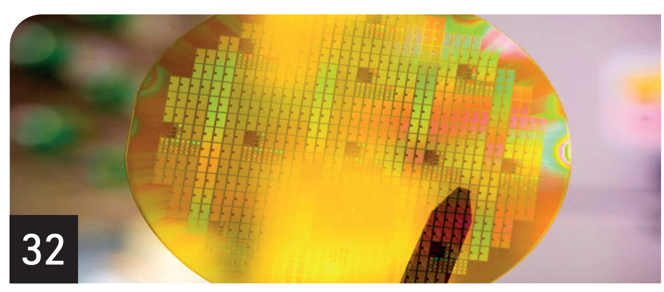

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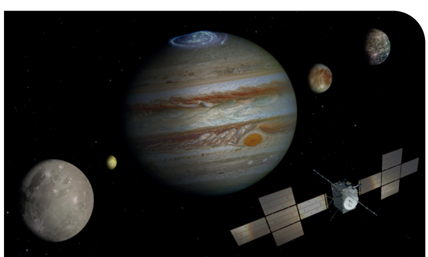

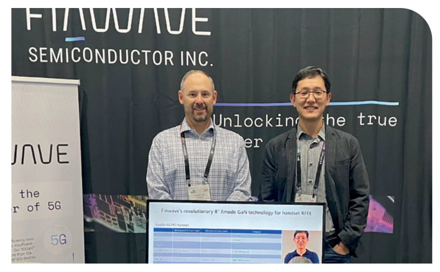

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Onsemi and Magna sign SiC deal

Magna to integrate Onsemi's EliteSiC chips into EV traction inverters

CHIP COMPANY Onsemi and automotive supplier Magna have signed a long-term supply agreement for Magna to integrate Onsemi's EliteSiC intelligent power solutions into its eDrive systems.

By integrating Onsemi's EliteSiC technology, Magna says its eDrive systems will offer better cooling performance and faster acceleration and charging rates, improving efficiency and increasing the range of electric vehicles (EVs). Additionally, Onsemi's end-to-end SiC manufacturing capability, combined with its ability to ramp production quickly, simplifies Magna's supply chain.

"With range anxiety still a top deterrent to EV adoption, our technology enables them to go further, easing the transition to an electrified future," said Asif Jakwani, senior vice president and general manager, Advanced Power Division, Onsemi. "Our latest EliteSiC MOSFET technology enables increased power density and higher efficiency in traction inverters, resulting in improved gas-equivalent miles per gallon without compromising driving dynamics and safety."

In accordance with the terms of the agreement, Magna will also invest approximately $40 million for the procurement of new SiC equipment at Onsemi's New Hampshire and Czech Republic facilities to ensure access to future supply. SiC is a wide bandgap semiconductor substrate that is ideal for high-temperature, high-power applications such as electric vehicles, but it is incredibly difficult to produce. With a limited number of manufacturers and significant demand for SiC-based designs, OEMs and automotive suppliers are increasingly looking to secure long-term, reliable supply.

"We recognise the importance of securing a stable supply of SiC material in order to continue delivering innovative and efficient eDrive systems for our customers," said Diba Ilunga, president Magna Powertrain.

"As the electric vehicle market continues to grow, we are taking proactive steps to secure access to future SiC supply to help support our electrification strategy and outpace the competition."

Onsemi and BorgWarner expand SiC collaboration

Onsemi and BorgWarner are expanding their strategic collaboration for SiC, making the total agreement worth over $1 billion in lifetime value.

BorgWarner plans to integrate Onsemi EliteSiC 1200 V and 750 V power devices into its VIPER power modules. The EliteSiC devices join a broad portfolio of Onsemi products that are part of the long-standing strategic relationship between the two companies.

"First and foremost, Onsemi's continuous and strategic investment in ramping SiC manufacturing capacity across its end-to-end supply chain gives us confidence in our ability to support the increasing demand for our solutions, now and in the future," said Stefan Demmerle, VP of BorgWarner Inc. and president and general manager, PowerDrive Systems.

BorgWarner says that its SiC traction inverters already offer higher efficiency, better cooling performance, and faster-charging rates in a more compact package than other options for EVs. By using EliteSiC technology, BorgWarner's solutions expect to benefit from increased power density and higher efficiency, which increase the range and overall performance of EVs.

"The integration of EliteSiC technology in the traction inverter enables increased gas-equivalent miles per gallon, which helps alleviate range anxiety – one of the key barriers to EV adoption," said Simon Keeton, executive VP and general manager, Power Solutions Group, Onsemi. "With Onsemi's chip-to-system level support and a track record of execution, we are able to provide industry-leading SiC-based solutions to BorgWarner at an accelerated pace to support its go-to-market requirements."

Kubos wins £700k grant for microLED tech

High-efficiency red microLED technology secures UK grant, new patent, and first customer order

CAMBRIDGE-BASED Kubos Semiconductors, a UK microLED material technology company, has won a £700,000 Future Economy Investor Partnerships (FEIP) grant from Innovate UK, the UK government's innovation agency. The grant funding is subject to completing aligned investment led by the Development Bank of Wales (DBW). The company has also been granted its first process technology patents and has received its first customer order.

The grant is for a 24-month project to achieve 5 percent efficiency for red microLEDs by deploying the company's proprietary cubic GaN process, called KubosLED. Achieving the project's goal and is said to make microLEDs viable in AR/VR applications by approximately doubling the efficiency achieved with other process technologies. Poor red microLED efficiency is currently one of the main factors constraining the AR/VR market.

Carl Griffiths, Technology Seed Fund manager for DBW, said: "We've only recently joined the FEIP and Kubos is the first company we have supported, and they have been awarded this grant. Kubos has demonstrated it has the right focus on deep tech, the right profile and momentum to secure the funding. Their exciting new technology has a clear purpose, and the market opportunity is vast."

Following successful completion of the funding round in the autumn, Kubos, as a fabless semiconductor company, will open a development office in Wales. This will enable it to continue to benefit from years of collaboration with the South Wales Compound Semiconductor cluster, specifically the Compound Semiconductor Centre (CSC, a partnership between Cardiff University and international compound semiconductor fabrication company, IQE Plc) and the Institute of Compound Semiconductors at Cardiff University, where the Kubos LEDs are processed and tested.

Kubos's core cubic GaN process and product technology patent has now been granted in China, Japan, Singapore, and the US. Its patent portfolio has also been extended to include granted patents for SiC epitaxy, which is used by Kubos as a growth substrate.

The company has also won its first customer for its KubosLED material in red microLEDs. Kubos CEO, Caroline O'Brien, commented: "We see huge demand for our technology every time we engage with potential customers and are delighted to have won our first major customer and secured further funding to ensure we reach our technology goals. These achievements underline the fact that KubosLED material technology is the leading contender to clear a major bottleneck that's been holding back AR/VR adoption."

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Aixtron raises 2023 growth guidance

GaN and SiC demand drives company's highest order intake since 2011

DEPOSITION equipment firm Aixtron has continued its growth path in Q3 2023, achieving its highest quarterly order intake in the company's history since 2011.

This momentum is driven by continued high demand from end markets and in particular for efficient power electronics based on GaN and SiC. In line with these ongoing dynamics, the executive board has raised the growth guidance for the fiscal year 2023.

In the first half of 2023, the company's order intake increased by 12 percent year-on-year to €317.7 million. In the second quarter, Aixtron's order intake was €177.8 million, 17 percent above the order intake of the previous year's period. The order backlog on June 30, 2023, increased significantly, reaching €412.5 million.

Equipment for efficient SiC and GaN power electronics accounted by far for the largest share of the order intake. The reason for the continued strong growth: Aixtron is currently supporting several major customers in setting up production facilities and enabling these important semiconductor companies to manufacture SiC and GaN devices in high volumes.

Aixtron's new G10 family of products sets the grounds for this – the G10-SiC, the G10-AsP and the G10-GaN, which will follow later this year.

"The main driver of our consistently strong growth comes from efficient power electronics based on SiC and GaN. And we expect this momentum to continue in the years to come. A very strong indication of this can be found in e-mobility, where SiC is the preferred material system. Moreover, we already know that our systems for SiC will by far be the top-selling products in our portfolio in 2023," says Felix Grawert, CEO and president of Aixtron SE.
The continuously growing demand for efficient power electronics resulted in a significant revenue increase both in the second quarter as well as the first half of the year: Aixtron's revenues in the first half of the year went up by 31 percent year-on-year to €250.7 million. In the second quarter, revenues reached €173.5 million, up 69 percent versus the same period last year.

This result was also positively impacted by the fact that a large part of the export licenses outstanding in the previous quarter have now been granted, and the corresponding equipment has been delivered.

In line with the strong revenues, the gross profit in Q2/2023 was €73.5 million, which equals a growth of 94 percent, almost doubling the results achieved in the same period of the previous year.

Due to the unabated strong demand, the executive board continues to expect significant growth with increasing margins and orders for the remainder of the financial year. Expected order intake for FY/2023 is now to be between €620.0 million and €700.0 million; and revenues are now expected to range between €600.0 million and €660.0 million.

In the first half of 2023, operating expenses amounted to €56.5 million, 34 percent higher than in the same period of the previous year. This was mainly due to increased expenses in research and development (R&D). These investments into existing as well as the development of new system generations will lay the foundation to secure and further expand Aixtron's strong market position.

Aixtron concluded the second quarter of 2023 with an operating result (EBIT) of €44.6 million and a strong EBIT margin of 26 percent, an increase of 159 percent and 9 percentage points. In the first half of the year, the operating result (EBIT) reached €48.1 million, with an EBIT margin of 19 percent.

The profit for the period in the first half of the year increased significantly by 41 percent to €43.9 million. Of this, €40.4 million was achieved in the current year's second quarter, an increase of 134 percent compared with the same period in 2022.

In the first half of 2023, Aixtron's free cash flow was €-80.1 million. This development is primarily driven by outflows to increase inventories in preparation of the planned revenue growth in the second half of 2023.

As of June 30, 2023, Aixtron reported cash and cash equivalents including other current financial assets of €210.4 million. This includes a dividend payment from May 2023 of €34.8 million.

NoMIS to develop SiC MOSFETs for US Air Force

US company to develop rugged devices for aircraft electrical power systems

ALBANY-BASED NoMIS Power has been awarded a project by the US Air Force Research Laboratory to develop rugged SiC power MOSFETs to support the electrical power systems of aircraft.

NoMIS Power will develop 1200 V SiC devices with enhanced operational lifetime as well as improved on-state and off-state efficiency at operating temperatures, resulting in lower losses for power electronics engineers to manage.

Solid-state power controllers within aircraft electrical power distribution systems require low on-state losses to enable passive cooling, as well as surge current and voltage overshoot protection during system start-up and fault interrupt. The proposed 1200 V SiC MOSFETs from NoMIS Power will provide airframers and system builders/integrators with the necessary power chips capable of high efficiency, long short-circuit withstand time, and operational ruggedness for nominal and transient conditions. Moreover, the 1200 V rating will not only support current-generation aircraft utilising 270 V_{DC} architecture, but also aircraft operating with a +/- 270 V_{DC} (i.e. 540 V_{DC} rail-to-rail) architecture, as well.

NoMIS Power says it overcomes the limitations of commercial-off-the-shelf silicon and SiC-based devices via a novel SiC device design.

As a result, NoMIS SiC devices can withstand higher voltage spikes and current surges during harsh operating conditions, enabling longer power management product lifetime through superior reliability and ruggedness.

Announcing the new award, NoMIS Power CEO Adam Morgan, said: “Our team is very excited to get the opportunity to support strategic groups working to improve the capabilities of our armed forces. We are confident this novel SiC device technology will also have a significant impact on other critical technology markets, such as electric vehicles and grid infrastructure. These efforts will directly support our company’s near-term product launch of next-generation SiC devices.”

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Agnitron installs MOCVD systems at two universities

UCSB to grow Ga_2O_3 for power and RF devices, while Notre Dame University will produce SiC chips for quantum computing

MINNESOTA-BASED MOCVD specialist Agnitron Technology has installed custom systems at two US universities this summer.

The first tool is for growing ultra-wide band gap Ga_2O_3 for power and RF devices at University of California Santa Barbara. The second is for wide bandgap SiC devices for quantum computing at Notre Dame University in Indiana.

Agnitron installed and qualified the R&D Ga_2O_3 MOCVD Agilis 100 system in July 2023 at UCSB. Agnitron and UCSB have worked together for over 5 years on similar topics, but the new installation means UCSB can grow its own materials, providing greater flexibility and innovation.

The Agnitron Agilis 100 system with six metal-organic channels, two oxidising precursor lines and silicon doping capability at UCSB can perform growths up to a 1100 °C substrate process temperature.

The system has a GEN II remote injection with a close injector showerhead add on, *in-situ* pyrometry and reflectometry for growth parameter control, and Agnitron's latest software control platform Imperium.

According to the company, the tool has demonstrated significantly reduced gas-phase reaction compared to other technologies and excellent thickness uniformity on a 2-inch diameter wafer. Furthermore, Agnitron says the Agilis 100 MOCVD platform is easily convertible to grow GaN and AlN epitaxial layers.

UCSB professor Sriram Krishnamoorthy, who is leading the Ga_2O_3 research, said: "We look forward to partnering with Agnitron to develop further epitaxial layers of ultra-wide bandgap Ga_2O_3, alloys and heterostructures and also translate that to record-breaking device performance."

"We are excited to repeat and improve upon our previous experience with an Agnitron Agilis gallium oxide MOCVD system at the University of Utah, which enabled us to achieve the highest quality epitaxial films."

VP of sales, Paul Fabiano, commented: "We are pleased to partner with UCSB on ultra-wide band gap materials. It's an important and expanding material system for future RF and power device technologies."

Also, this summer, Agnitron delivered an MOCVD/CVD tool to Notre Dame University's School of Engineering. This system, an Agilis Mini, will grow SiC devices for quantum computing.

President and CEO of Agnitron, Andrei Osinsky said: "The Agilis Mini was introduced this year by Agnitron to provide research groups with the same state-of-the-art attributes of the Agilis 100, but who have a more constrained budget. Over time the tool can be enhanced and upgraded with other technologies. However, out of the box, it can meet the current R&D needs of the customer."

Chris Hinkle of Notre Dame said: "We needed a new tool to make the highest quality SiC for quantum interconnects. We chose the Mini-Agilis from Agnitron because of the company's reputation and the tool design being able to provide the purity needed for long-lifetime qubits."

The tool is being installed in an Engineering Clean Room at the University's campus. The building houses numerous other types of semiconductor equipment and laboratories, used by students and faculty.

Renesas and Wolfspeed sign 10 year SiC wafer agreement

$2 billion deposit to Wolfspeed secures supply agreement for both 150 mm and 200 mm SiC wafers

RENESAS ELECTRONICS and Wolfspeed have announced a wafer supply agreement and $2 billion deposit by Renesas to secure a ten year supply commitment of SiC bare and epitaxial wafers from Wolfspeed.

The supply of SiC wafers from Wolfspeed will pave the way for Renesas to scale production of SiC power semiconductors starting in 2025. The signing ceremony of the agreement (pictured) was held at Renesas' headquarters in Tokyo between Hidetoshi Shibata, president and CEO of Renesas, and Gregg Lowe, president and CEO of Wolfspeed.

The decade-long supply agreement calls for Wolfspeed to provide Renesas with 150 mm SiC bare and epitaxial wafers scaling in 2025, reinforcing the companies' vision for an industry-wide transition from silicon to SiC semiconductor power devices.

The agreement also anticipates supplying Renesas with 200 mm SiC bare and epitaxial wafers after the recently announced John Palmour

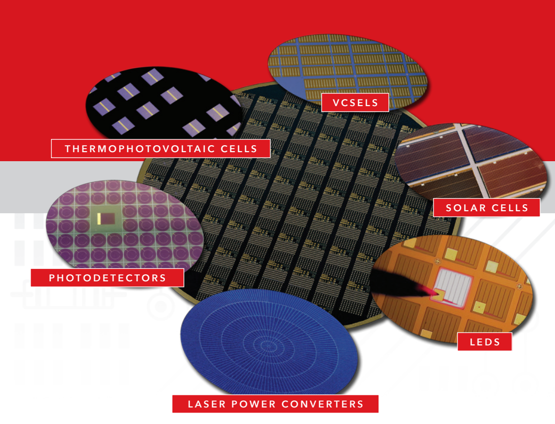
Manufacturing Center for SiC is fully operational.

Renesas is moving quickly to address the growing demand for power semiconductors by expanding its in-house manufacturing capacity. The company recently announced the restart of its Kofu Factory to produce IGBTs, and establishment of a SiC production line at its Takasaki Factory.

"The wafer supply agreement with Wolfspeed will provide Renesas with a stable, long-term supply base of high-quality SiC wafers. This empowers Renesas to scale our power semiconductor offerings to better serve customers' vast array of applications," said Hidetoshi Shibata, president and CEO of Renesas. "We are now poised to elevate ourselves as a key player in the accelerating SiC market."

"With the steepening demand for SiC across the automotive, industrial and energy sectors, it's critically important we have best-in-class power semiconductor customers like Renesas to help lead the global transition from silicon to SiC," said Gregg Lowe, President and CEO of Wolfspeed. "For more than 35 years, Wolfspeed has focused on producing SiC wafers and high-quality power devices, and this relationship marks an important step in our mission to save the world energy."

The Renesas $2 billion deposit will help support Wolfspeed's ongoing capacity construction projects including the JP, the world's largest SiC materials factory in Chatham County, North Carolina. The facility is targeted to generate a more than ten-fold increase from Wolfspeed's current SiC production capacity on its Durham, North Carolina campus.



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Indian GaN centre installs Oxford Instruments tools

GaN Ecosystem Enabling Centre and Incubator orders full suite of plasma processing solutions for power & RF pilot line

OXFORD INSTRUMENTS Plasma Technology has announced a substantial equipment shipment to the GaN Ecosystem Enabling Centre and Incubator (GEECI) located at the Centre for Nano Science and Engineering, Indian Institute of Science, in Bengaluru (formally Bangalore).

The technologies being installed in the pilot production line include atomic layer etch, two variants of inductively coupled plasma etch modules, and plasma enhanced chemical vapour deposition (PECVD).

The suite of GaN plasma processing solutions will be used to develop next generation GaN-on-silicon and GaN-on-SiC high power and high frequency power electronics and RF devices to offer improved efficiency and performance.

Positioned within India's premier high technology hub, in the city of Bengaluru and with strong links to several technology giants within the hub, GEECI is an ideal environment for technology start-ups and spin-offs.

Srinivasan Raghavan (Vasu), who is charge of setting up GEECI, said: "The equipment, ongoing process and service support, and technical collaboration with Oxford Instruments Plasma Technology, is crucial to our GaN device development programme. We are incredibly excited to partner with Oxford Instruments to establish our new GaN pilot production line to support the next generation of GaN startups and spin outs, which are critical to accelerate India's flourishing semiconductor ecosystem."

Shankar Kumar Selvaraja, the Process expert, said: "We look forward to developing new process recipes to enable GaN power and RF electronics".

Ian Wright, Plasma Technology's VP of sales and business development, Asia, commented: "We are delighted to be bringing our GaN technology to such a prestigious institution as the Indian Institute of Science. We have recently experienced a surge in interest for our solutions in India, which points toward a shift in the technology landscape for that region with momentum generated through government funding."

He added: "We have invested in an ambitious and expanding program of service and support for India, and are uniquely positioned in the region, to play an integral role in encouraging transformational semiconductor technology development and industry growth."

ST starts volume production of PowerGaN chips

STMICROELECTRONICS has begun volume production of e-mode PowerGaN HEMT devices that simplify the design of high-efficiency power-conversion systems. The STPOWER GaN transistors raise performance in applications such as wall adapters, chargers, lighting systems, industrial power supplies, renewable energy applications, and automotive electrification.

The first two products in the family, the SGT120R65AL and SGT65R65AL, are industrial-qualified 650 V normally-off G-HEMT in a PowerFLAT 5x6 HV surface-mount package. They have current ratings of 15 A and 25 A, respectively, with typical on-resistance ($R_{DS(on)}$) of 75 mΩ and 49 mΩ at 25 °C. Also, 3 nC and 5.4 nC total gate charge and low parasitic capacitances ensure minimal turn-on/turn-off energy losses. A Kelvin source connection allows optimised gate driving. In addition to the reduced size and weight of the power supplies and adapters, the two new GaN transistors provide higher efficiency, lower operating temperature, and extended life time.

In the coming months, ST will introduce new PowerGaN variants, i.e. automotive-qualified devices, as well as additional power-package options including PowerFLAT 8x8 DSC and LFPAK 12x12 for high power applications.

GaN transistors with the same breakdown voltage and $R_{DS(on)}$ as silicon alternatives can achieve lower total gate charge and parasitic capacitances, with zero reverse-recovery charge. These properties raise efficiency and enhance switching performance, allowing higher switching frequency that permits smaller passive components thereby increasing power density. Applications can therefore become smaller with higher performance.

ST has high production capacity for PowerGaN discrete products to support customer demand for a very fast ramp to volume manufacturing.

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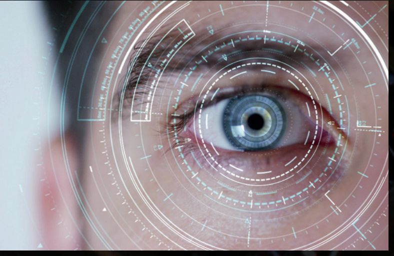

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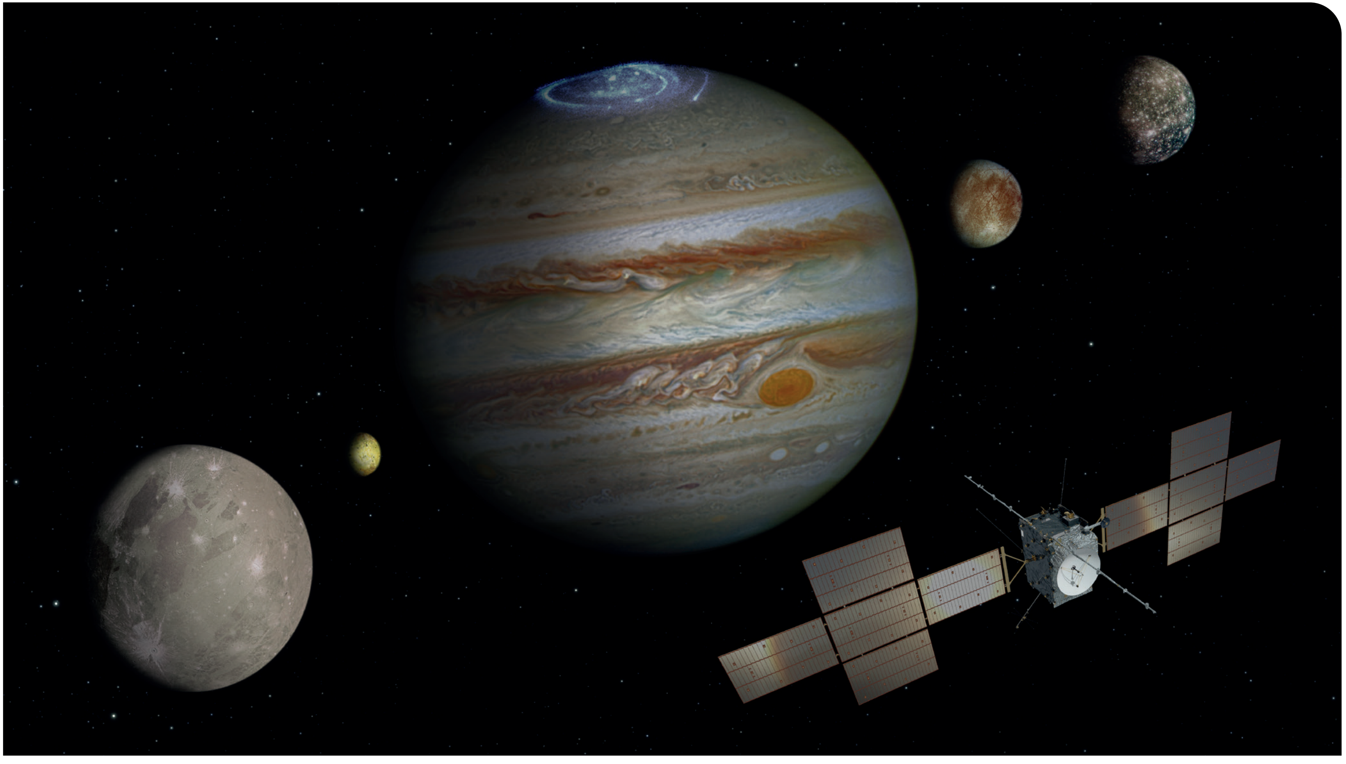

Image credit: ESA

Powering the exploration of Jupiter

The instruments on-board the latest mission to Jupiter are drawing energy from a vast array of cells produced by Azur Space Solar Power

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THINK OF SOLAR CELLS and you probably picture devices operating in sunny climes, where they convert intense rays into lots of renewable energy. But that's not their only task. Photovoltaics are also deployed on extra-terrestrial missions, where the intensity of sunlight can be far lower than it is on Earth.

Right now, a craft equipped with solar panels is hurtling through space on a mission to Jupiter, where it will study this planet and its moons. On this voyage, coordinated by the European Space Agency, detailed observations will be made of this planet and its three ocean-bearing moons by instruments powered by solar panels, receiving radiation with an intensity around just 3.5 percent of that experienced by satellites orbiting the Earth.

Providing power for this latest mission to Jupiter, known as JUICE – JUpiter Icy Moons Explorer – is a vast array of triple-junction solar cells, produced by Azur Space Solar Power, now a subsidiary of 5N Plus. These cells are considerably more efficient than those made from silicon, as well as being more robust to bombardment from radiation.

Having cells that excell in converting the Sun's rays into electricity is particular important at low levels of incident radiation, because when the intensity falls, there's a linear reduction in current and a logarithmic decline in voltage. "So just by having a lower intensity, you get a lower efficiency of the solar cell," explains Wolfgang Guter, Director of Technology and Marketing at Azur.

Another challenge facing these solar cells that are on a mission to Jupiter is that they face particularly heavy bombardment from radiation. This fluence is more than an order of magnitude higher than that for a cell orbiting the earth, and roughly equal in value to that facing a device in a geostationary orbit.

"However, the damage caused by the same fluence at Jupiter is much more severe than the damage caused by the same fluence in an orbit around Earth," remarks Guter. He says that the damage is about 20 percent greater, due to the removal of self-annealing that stems from the lower temperature.

Fortunately, the lower temperature found near Jupiter, typically just -120 °C in the sun, also has an

upside. As temperature falls, cell efficiency rises to 35 percent, a value considerably higher than that for a satellite orbiting the Earth.

A colossal undertaking

Azur's contribution to the JUICE programme involved the supply of around 24,000 cells that form a 85 m^2 array, which produces just enough power for the mission. To put that size in context, arrays on commercial constellation satellites typically cover just 10 m^2, while those on large geo-stationary communication satellites, producing around 27 kW of power, are up to 70 m^2.

For all satellites, every cell is tested before it is deployed. However, for the mission to Jupiter cells were subjected to greater scrutiny, with additional testing evaluating the dark current.

Fabrication of the cells involved the growth of complex heterostructures on germanium substrates, prior to the processing of these epiwafers into devices. The latter steps included metallisation and the addition of anti-reflection coatings. For the JUICE programme, once testing identified the cells with sufficient performance, they were sent to Leonardo, which added glass and interconnects to create solar panels. These panels were integrated to the spacecraft by Airbus.

Given the substantial work required to prepare for launch, it not that surprising that the cells on this craft, which set off for Jupiter this April, were made around eight to ten years ago. Back then all growth took place on 4-inch germanium substrates, each providing two 30 cm^2 cells. (Today Azur mainly produces cells on 6-inch germanium substrates, but 4-inch wafers are still used for some projects).

When these cells were shipped to Leonardo for the JUICE project, Azur's flagship product was the 3G28, a lattice-matched design featuring germanium, GaAs and GaInP sub-cells.

Comprehensive testing of this design determined that it is free from potential barriers within this heterostructure, even at temperatures as low at around -100 °C. That's a major asset, at it ensures a low resistivity, crucial for high-performance in space. The instruments on the JUICE programme typically require 50-100 V to operate, while the voltage produced by each cell is around 2.7 V, so they are wired in series. This scales the voltage, but current is limited by the cell with the highest resistance – hence the need for cells with minimal resistance.

The voyage to Jupiter is rather complex, exploiting gravitational slingshots to reduce the time of the journey with a route that includes a flyby of Venus. Near that planet the cell temperature could reach 160 °C, so to prevent panels from overheating, they are orientated at an angle to the sun's rays.

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As it will be 2031 by the time the craft reaches Venus, those at Azur we'll have to wait several years before claiming that this mission offers further demonstration of the capability of their cells. However, that lack of validation is not stopping them from winning contracts on other demanding and comparable missions, including NASA's Europa Clipper mission, which will investigate whether Jupiter's icy moons could have conditions suitable for life. Gutner attributes securing that contract to a thorough understanding of the performance and the degradation mechanisms of their solar cells under low intensity, low-temperatures conditions.

A new era for Finwave

Three-dimensional GaN FinFETs will ramp to production volumes under the leadership of **Pierre-Yves Lesaicherre, Finwave's new CEO**

COMPANIES THAT are spun out of universities tend to follow a similar trajectory. In their fledgling form, they recruit personnel from the accompanying research group that have specific expertise for honing the technology, and select a researcher from that background with entrepreneurial flair. But when the next phase comes, requiring the raising of substantial capital and a shift from development to production, a new leader takes over with a proven track record of delivering on these fronts.

It's an evolution that is taking place right now at Finwave, the pioneer of three-dimensional GaN FinFET technology that spun out of MIT ten years ago, initially under the name Cambridge Electronics. The company's co-founder and former CEO, Bin Lu, who helped develop the core technology while working for his PhD in Tomás Palacios' group, has now taken over the CTO role, and in his place comes industry veteran Pierre-Yves Lesaicherre.

Incredibly enthused by the tremendous potential of Finwave's technology, Lesaicherre brings with him a wealth of executive experience, having previously held a number of executive roles that include: CEO of equipment manufacturer Nanometrics, where he oversaw the merger with Rudolph Technologies; CEO of the LED manufacturer Lumileds; and several Senior Vice President and Vice President roles at NXP Semiconductors.

Lesaicherre has been appointed to scale Finwave. "The company got new investors on-board last year through Round A, and the new investors have been pretty adamant that they want to see the building of a structure that will allow the company to thrive."

➤ Pierre-Yves Lesaicherre took over from Bin Lu as CEO of Finwave this June.

Encouraging Lesaicherre to take on this challenge is what he sees as the great potential of Finwave's highly differentiated GaN technology platform, delivering an order-of-magnitude advancement in both the RF and the power domain. "I always use the analogy of a diamond. It's very difficult to find diamonds, but once you have a rough diamond, it's a lot easier to refine it and cut it and make it into a shining star than it is to develop the technology."

There's no doubt that Lesaicherre's background has equipped him with the expertise to do just that. As well as knowing how to build and structure a company, he will draw on a wide network. "I know a lot of people through the years and I think that's going to be tremendously helpful as we grow."

Early goals

To begin with, Lesaicherre will concentrate on generating sales. "We are working hard to expedite the production of our first product to meet the enthusiastic demands of our customers, as swiftly as possible."

His other goal is to secure a second round of funding to add to the Series A investment of $13.4 million, which closed in summer 2022. "That's going to come fairly quickly. We have a runway until the end of next year, so by the end of this year or early next year we're going to have to raise the Series B round."

Initially, Lesaicherre will not focus his effort on the company's strategy. That's the task for Finwave's Chief Strategy Officer, Jim Cable, who previously led Peregrine Semiconductor. Both Cable and Lu will guide Lesaicherre while he refines his understanding of the company's technology and its opportunities. However, further down the road Lesaicherre will take on the responsibility for the company's strategic direction.

Finwave has already started to target the RF market, having demonstrated its first product, an RF switch, at this year's International Microwave Symposium (IMS).

"It's a ten-watts broad-band switch that has a remarkably fast switching time and settling time," enthuses Lesaicherre. Allied to that speed – a switching time of 50 ns and a settling time of 100 ns – is a breakdown voltage of around 50 V, and a high degree of linearity and isolation.

While SOI (silicon-on-insulator) technology can match the power-handling capability of Finwave's

device, it falls short on other key metrics. SOI suffers from a slower switching speed, and with a breakdown voltage of around just 3 V, a very large number of devices must be deployed in series. Note that the other contender, GaAs, cannot offer as low a settling time as Finwave's technology, due to traps in the material.

Lesaicherre says that the unique performance of Finwave's transistors led to a very positive reception at IMS. "Now we're sampling these devices to potential customers and we are receiving very positive reactions confirming their exceptional performance."

The company is initially focusing on the 5G millimetre-wave market with a product that sets a new benchmark for power-handling capability.

"When utilised in customer premise equipment, it effectively addresses the uplink power challenge," asserts Lesaicherre. "By doing so, we can unleash the full potential of 5G millimetre-wave."

Finding a fab partner

Finwave developed its 8-inch GaN-on-silicon technology in partnership with Lincoln Labs, which has a small engineering fab in Massachusetts.

"The challenge this year and next year is to move to a high-volume eight-inch fab," says Lesaicherre. "We're in discussions with partners right now in the US and Taiwan to find a good landing spot for a high-volume, eight-inch manufacturing partner."

Negotiations are far easier than they would have been a couple of years ago, when capacity constraints were rampant.

"GaN-on-silicon will be an important factor to load these fabs," points out Lesaicherre. "So the partners we're talking to are very interested, because they see a potential long-term utiliser of their factory capacity."

Fabs with an 8-inch line, which typically have a lithographic capability that extends to 65 nm, should be capable of producing the vast majority of products that Finwave plans to manufacture. However, it's possible that if Finwave designs devices for much higher frequencies, that might require production on a 12-inch line that's capable of making devices with smaller dimensions.

Lesaicherre would like to announce an 8-inch high-volume partner within the next few months and transfer production to them. Additional aims are to expand the company's portfolio with the introduction of power amplifier products next year, and secure traction from some customers.

"Hopefully before the end of the year we're going to be able to announce utilisation of the device in specific applications and specific customers," says Lesaicherre.

These milestones should help the company secure more funding for its Series B round, which will require winning over new investors.

"When you get to Series B you attract a different type of investor," claims Lesaicherre. "I think some of our Series A investors will be staying with us and invest in Round B, but I would expect the bulk of the money to come from new investors."

Until that money comes in, they'll not be a major change in headcount, which is currently totalling around 20, but will grow slightly as a few staff are added to support the technology development, device design and marketing activities.

"We're very conscious of our burn rate, and we want to keep operating at a fairly frugal level until we get the additional funding," says Lesaicherre.

Clearly, he knows not only what needs to be done to ensure that the FinFET excels, but the right order for those many steps to success.

➤ Finwave's new switch for 5G millimetre-wave applications received a very positive reception from those attending this year's International Microwave Symposium.

> Fabs with an 8-inch line, which typically have a lithographic capability that extends to 65 nm, should be capable of producing the vast majority of products that Finwave plans to manufacture

Excelling in the etching of gallium oxide

The etching of Ga_2O_3 works best when using an MOCVD chamber to direct gallium-containing organic molecules onto epilayers

BY FIKADU ALEMA, AARON FINE, WILLIAM BRAND AND ANDREI OSINSKY FROM AGNITRON AND ABISHEK KATTA AND NIDHIN KURIAN KALARICKAL FROM ARIZONA STATE UNIVERSITY

BY TAKING RAPID STRIDES, Ga_2O_3 is now poised to shape the market for power devices. This ultra-wide bandgap semiconductor is equipped with the characteristics to enable superior devices, realised at a very competitive cost, thanks to the opportunity to make high-quality bulk substrates from the melt.

During the last decade, the performance of this class of power device has come on in leaps and bounds. Key breakthroughs have included the fabrication of devices with breakdown voltages of more than 8 kV and breakdown field strengths greater than 5 MV/cm, which is beyond the theoretical limits of SiC and GaN. However, Ga_2O_3-based devices are yet to produce a level of performance that's close to the theoretical limit. Why? Well, in part it is due to the lack of appropriate, highly controllable, damage-free etching processes.

Controllable etching and the removal of material are essential steps in the fabrication of many different types of semiconductor devices. The capability to remove material is just as important as the ability to deposit it – this pair of complementary processes enables the shaping of semiconductor materials into well-defined device architectures.

Prior to etching, the active region of many devices tends to be protected by dielectrics, such as SiO_x or SiN_x. That's also the case with Ga_2O_3-based devices. However, it's not easy to find a damage-free etch process that avoids compromising the performance or the reliability of the device.

A wide range of etch processes have been employed during the fabrication of numerous

β-Ga_2O_3 based devices. These processes include dry etching, wet etching, photochemical etching, and metal-assisted chemical etching. Unfortunately, all these forms of etching exhibit limitations, such as surface damage, the introduction of angled sidewalls, and anisotropic etching along certain crystal planes. Due to these downsides, none of these approaches are suitable for producing high-performance devices.

Offering far more promise are vapour-based *in-situ* etching techniques undertaken in the chambers of growth tools, such as those used for MBE and MOCVD. By their very nature, such approaches to epitaxial growth enable etching and re-growth of epilayers and dielectrics without breaking the vacuum, resulting in cleaner interfaces. As the quality of β-Ga_2O_3 epilayers is highest when grown by MOCVD, this type of reactor is the best choice for integrating growth and etching processes.

At Agnitron, we have a well-earned reputation as the leading provider of MOCVD reactors for the growth of β-Ga_2O_3 epilayers, with our tools now installed in a number of world-class labs. What may be less well known, however, is that our reactors can be used for the *in-situ* etching of Ga_2O_3 films, substrates, and related alloys. That's the topic for the remainder of this article, where we discuss the etching of β-Ga_2O_3 using metal organic sources containing gallium and chlorine.

Etching with MBE...

The growth of Ga_2O_3 by MOCVD involves the reaction of gallium and oxygen precursors, with the rate of deposition typically governed by the concentration of gallium that's introduced into the reactor. However, when the growth chamber is deprived of active oxygen, the gallium precursor performs a different role, etching the surface of the substrate or the epitaxial film.

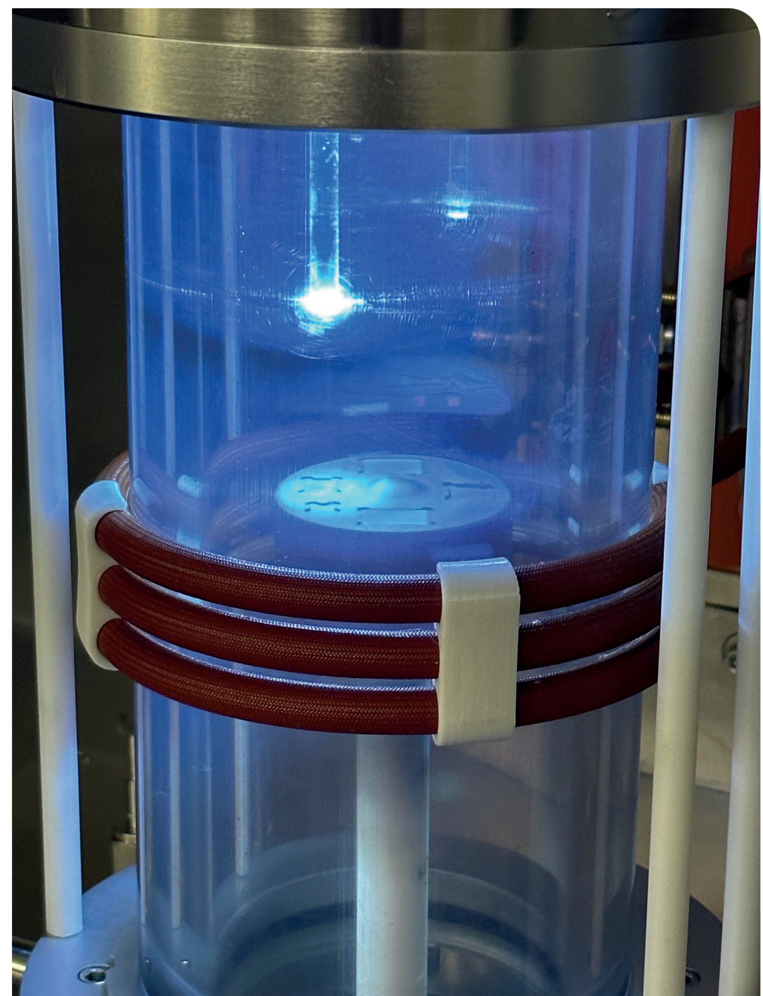
In MBE, this etching process is well-known. As the growth of Ga_2O_3 progresses, this competes with the formation of Ga_2O_3 and its volatile suboxide Ga_2O – and when higher gallium fluxes land on the substrate in an oxygen deficient environment, the rate of growth of Ga_2O_3 decreases (what's actually happening is that material is etched from the Ga_2O_3 surface, rather than growing on it).

When these conditions occur, involving oxygen deficiency, they favour formation of the extremely volatile suboxide Ga_2O, which desorbs from the surface rather than contributing to the growth of Ga_2O_3. Due to these conditions, it's impractical to accelerate the growth rate of Ga_2O_3 with standard MBE growth processes.Drawing on this phenomenon, many researchers have turned to gallium metal to etch the surface of Ga_2O_3 in an MBE chamber. According to reports, this is a low-damage etch technique, with gallium reacting with Ga_2O_3.

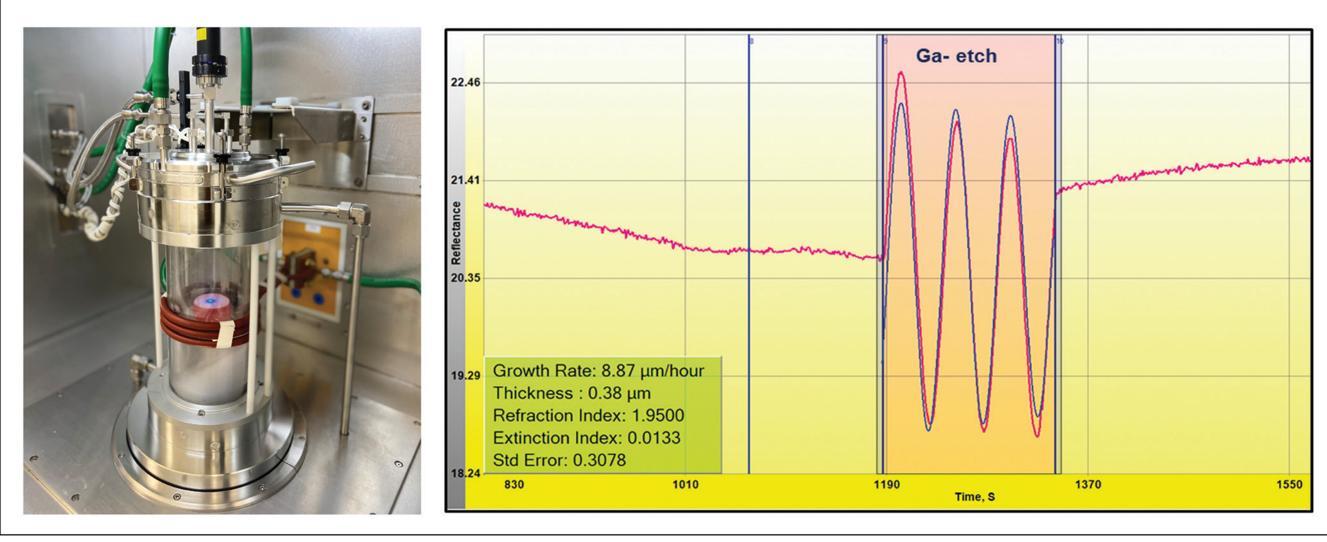
...and MOCVD

We have investigated using MOCVD to etch Ga_2O_3 in collaboration with Nidhin Kalarickal's group at ASU, who have experience of gallium etching of Ga_2O_3 in an MBE chamber. Working together, we have shown that in the absence of oxygen, metalorganic gallium-containing precursors, such as triethylgallium (TEGa), enable *in-situ* etching of Ga_2O_3 in an MOCVD chamber. Again, etching comes from the reaction of gallium with Ga_2O_3 to produce the volatile Ga_2O suboxide, but this time the process begins with the homogeneous decomposition of TEGa. Pyrolysis takes place when TEGa is exposed to a temperature of around 350 °C or more, which it gets from the substrate temperature, creating gallium adatoms that move over the surface. The stable organic ethylene by-product produced during pyrolysis is removed from the reactor through the exhaust, following minimal interaction with the substrate's surface.

To monitor the etch rate *in-situ*, we take advantage of the significant refractive index contrast between



➤ Taking customer feedback into account, Agnitron has made significant upgrades to the current UV exposure fixture. The fixture now includes a directional focused light pipe that allows precise focusing of the UV power on a specific wafer during film growth. This enhanced setup enables the growth of films under UV exposure right next to unexposed UV wafers during the same run.



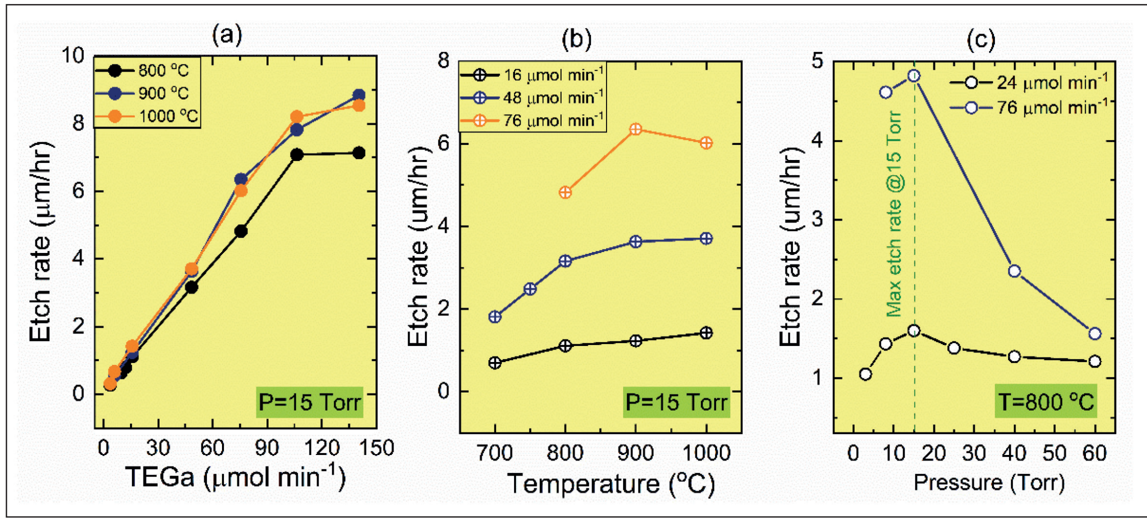
➤ Figure 1. An Agnitron MOCVD reactor with a blue LED shining at the center of a 2-inch wafer (left). (Right) The red trace is the measured reflectance data, and the blue trace fits the reflectance data from which the etch rate is estimated. An etch rate of 9 µm/hr is estimated.

the β-Ga_2O_3 film and the underlying sapphire substrate. We measure the etch rate by installing a fibreoptic reflectometer, operating at 470 nm, in our Agilis 100.

With this set-up, we have investigated the effect of various process conditions on the etch rate of $(\bar{2}01)$ oriented β-Ga_2O_3 epitaxial films grown on *c*-plane sapphire. In particular, we have studied the TEGa molar flow rate, substrate temperature, and chamber pressure. These experiments reveal that we can vary the etch rate from around 0.3 µm/hr to 9 µm/hr (see Figure 2).

We have found that for low TEGa molar flow rates – that is, values below 100 µmol/min – the etch rate increases linearly with increasing flow rate (see Figure 2(a)). However, at higher flow rates, the etching rate only increases slightly before saturating. When the etching conditions are in the linear regime, the suboxide reaction rate is high enough to consume all the gallium adatoms that are supplied from reaching the substrate surface. Due to this, the etch rate is limited by the supplied TEGa molar flow rate, resulting in the observed linear relationship. In contrast, when the number of supplied gallium adatoms is increased to the extent that they exceed what can be consumed by the suboxide reaction, the etch rate increases sub-linearly, and then saturates.

Another lever for increasing the etch rate is the substrate temperature. Higher temperatures



➤ Figure 2. Etch rate of β-Ga_2O_3 on sapphire as a function of etch parameters. (a) Etch rate versus TEGa molar flow rate at a constant pressure of 15 Torr, and a substrate temperature of 800 °C , 900 °C, and 1000 °C. (b) Etch rate versus substrate temperature at constant pressure of 15 Torr, and a TEGa molar flow rate of 16 µmol/min, 48 µmol/min, and 76 µmol/min. (c) Etch rates versus chamber pressure at a substrate temperature of 800 °C and TEGa molar flow rate of 24 µmol/min and 76 µmol/min.

accelerate the etch rate, but again only up to a point, with saturation occurring beyond 900 °C. When saturation occurs, the etch rate at saturation depends on the TEGa molar flow rate (see Figure 2(b)). At substrate temperatures below 800 °C etch rate is limited by the sub-oxide reaction rate, rather than the supplied TEGa flow. In this regime, increases in substrate temperature lead to higher etch rates, with excess gallium present on the substrate surface. It's a different state of affairs at higher temperatures, which leads to the consumption of all the supplied gallium in a sub-oxide reaction. The etch rate is then limited by the supplied TEGa flow rate, resulting in saturation of the etch rate. The pressure within the MOCVD chamber also influences the etch rate (see Figure 2 (c)). The maximum etch rate occurs at 15 Torr.

We have also used TEGa to etch $(Al_xGa_{1-x})_2O_3$. For this particular investigation, we compared the etching rate of films of Ga_2O_3, $(Al_{0.11}Ga_{0.89})_2O_3$ and $(Al_{0.22}Ga_{0.78})_2O_3$, all grown on *c*-plane sapphire substrates by MOCVD. Using a reactor pressure of 3.0 Torr, a substrate temperature of 800 °C and TEGa molar flow rate of 24 μmol/min, we determined an etch rate of around 1.0 μm/hr for Ga_2O_3, while just 0.2 μm/hr and 0.17 μm/hr for $(Al_{0.11}Ga_{0.89})_2O_3$ and $(Al_{0.22}Ga_{0.78})_2O_3$, respectively. These findings suggest that AlGaO is an etch stopper, and for this purpose $(Al_{0.11}Ga_{0.89})_2O_3$ is just as good as $(Al_{0.22}Ga_{0.78})_2O_3$.

Managing metal droplets

One limitation of *in-situ* etching of gallium is that it creates a gallium metal residue, which deposits on the etched surface. This residue, present when etching in both MBE and MOCVD chambers, has to be removed prior to subsequent steps in device processing.

A successful approach to removing the gallium residue is to etch the sample surface with hydrochloric acid. As this can only be undertaken outside the growth chamber, the etched surface has to be exposed to air, creating the threat of contamination that could impair device performance. Consequently, it is impractical to etch with hydrochloric acid, which is the only option following etching in an MBE chamber.

With MOCVD, gallium droplets can also be removed *in-situ* with halide-based metalorganic precursors. One option, which we have demonstrated, involves the use of tertiarybutylchloride (TBCl). This organic compound is also well known for *in-situ* and selective-area etching in GaN. When gallium droplets form on etched Ga_2O_3, they are converted into volatile variants of $GaCl_x$, which are liberated to leave a clean surface. Cleaning occurs at small flows of TBCl, but etching can also occur at higher flows.

Interfacial silicon

An issue that plagues the growth of Ga_2O_3 is the accumulation of silicon at the interface between the film and the substrate. Silicon is found here regardless of process conditions, the dopants in the substrate, and whether growth is by MBE or MOCVD.

Interfacial silicon is thought to come from the silica-based polishing of substrates, and probably also the exposure of Ga_2O_3 substrates to cyclic siloxanes in air. But whatever its origin, its presence is detrimental to device performance. For example, in FETs, it creates a parasitic conductive channel at the film/substrate interface, preventing devices from pinching off.

It's possible to reduce the concentration of interfacial silicon by etching the Ga_2O_3 substrates in concentrated hydrofluoric acid for about 30 minutes prior to loading into the growth chamber. This approach does not eliminate interfacial silicon but reduces its concentration, resulting in its partial compensation by the acceptor impurity (magnesium or iron), which defuses into the interface from the semi-insulating substrates during epitaxial film growth. Using this technique, we have recently produced and reported high-performance, multi-kilovolt class Ga_2O_3 MESFETs with a record power figure of merit of more than 350 MW cm^{-2}, working

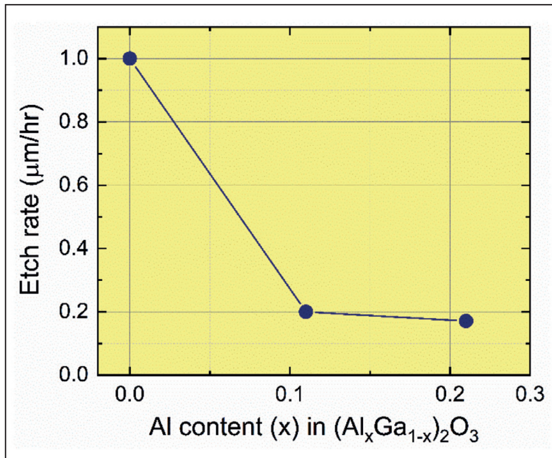


Figure 3. Etch rate of $(Al_xGa_{1-x})_2O_3$ on sapphire as a function of aluminium composition. The etch is performed at a pressure of 3 Torr, substrate temperature of 800 °C and TEGa molar flow rate of 24 μmol/min.

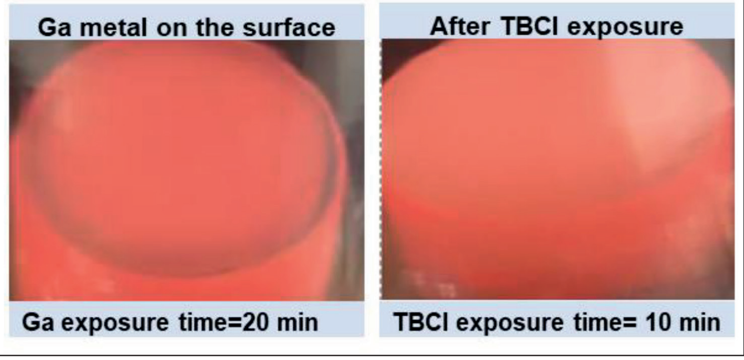


Figure 4. Images taken from outside through a transparent quartz tube reactor while undertaking etching of Ga_2O_3/sapphire. The dark coating on the surface of the wafer (left) is due to the deposit of gallium metal, and on the right the surface of the wafers after removing the gallium metal deposit.

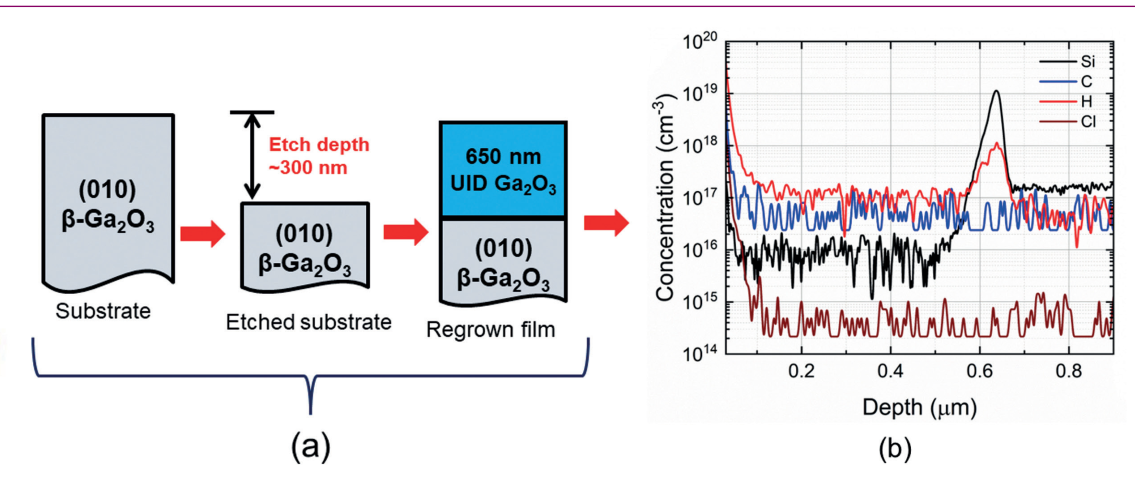


Figure 5. Etched and regrown samples (a), and a secondary ion mass spectrometry (SIMS) depth profile for silicon, carbon, hydrogen, and chlorine impurities (b).

in collaboration with Krishnamoorthy's group at the University of California, Santa Barbara.

We have also investigated whether etching with gallium can remove interfacial silicon. We etched a Ga_2O_3 substrate to a depth of about 300 nm with TEGa, before exposing the surface to TBCl to remove the gallium metal deposits and then growing an unintentionally doped β-Ga_2O_3 layer that's about 650 nm-thick. After carrying out all these steps in the same reactor without breaking the vacuum, we scrutinised our sample with secondary ion mass spectrometry (SIMS), quantifying the concentrations of silicon, carbon, hydrogen and chlorine in the unintentionally doped epilayer and interface between this film and the substrate (see Figure 5(b)). Results from SIMS indicate that the unintentionally doped epilayer is clean, with the concentration of each of the impurities below the detection limit of the instrument. No incorporation of carbon and chlorine is observed at the interface, but there is a slight uptake in the concentration of hydrogen, while that of silicon is unaffected. We attribute the persistence of the latter to the strong covalent bond that holds silicon and oxygen atoms.

We can conclude that etching with gallium is suitable for defining the dimensions of various device structures and re-growing ohmic contacts and dielectric materials, such as SiO_2 and Al_2O_3. However, the prospects of this technique for removing interfacial silicon are doomed.

Evaluating surface roughness

It is critical that when any substance etches a film or a substrate, it leaves a smooth surface. To see if that's the case with TEGa, we used this precursor to blanket-etch iron-doped (010) and tin-doped (001) β-Ga_2O_3 substrates to a depth of 350 nm.

According to atomic force microscopy maps, roughness after etching is encouragingly low, with the degree of smoothness increasing with substrate temperature (see Figure 6). Values for root-mean-square surface roughness after etching are around 3 nm. In addition, this form of microscopy uncovers parallel elongated groves, also observed on the surface of the epitaxially grown β-Ga_2O_3 film.

We have also used scanning electron microscopy to inspect our etched material. As well as using this technique to assess the morphology of films that have undergone blanket etching, we have studied structures formed by etching a patterned SiO_2 hard mask (see Figures 6 (e) and 6 (f).

Optimising process conditions, such as TEGa flow rate, substrate temperature, pressure, and the overall gas flow of the reactor, enables further improvements to surface quality. In addition, we

Figure. 6 (a) Atomic force microscopy (AFM) images of an etched (010) β-Ga_2O_3 surface, (b) AFM of an etched (001)β-Ga_2O_3 surface, (c) scanning electron microscopy (SEM) image of an etched (010) β-Ga_2O_3 surface, (d) SEM image of an etched (001) β-Ga_2O_3 surface, (e) SEM image showing a pattern-etched Ga_2O_3 (010) sample using a SiO_2 hard mask, (f) SEM image showing a pattern-etched Ga_2O_3 (001) sample using a SiO_2 hard mask (g). 2D AFM images of TEGa etched (010) β-Ga_2O_3 substrates without (g) and with (h) TBCl exposure for 20 minutes. All the AFM images were taken from scan area of 5 μm by 5 μm.

have found that exposing the TEGa-etched surface to TBCl for longer leads to a reduction in surface roughness. We discovered this when conducting an etch experiment using a pair of roughly 5 mm by 5 mm pieces of (010) iron-doped β-Ga_2O_3, cut from the same full-size substrate. For the piece that's only etched in TEGa, surface roughness is around 21 nm, while that exposed to TBCl for about 20 minutes after TEGa etching has a surface roughness of around 8 nm (see Figures 6(g) and 6(h)). We attribute the smoother surface to the effective removal of gallium droplets and gentle etching of the Ga_2O_3 surface by TBCl.

Other etchants

In addition to TEGa, we studied other organic molecules to etch Ga_2O_3. We have explored trimethylgallium (TMGa), which is expected to etch Ga_2O_3 in the same way as TEGa. However, our preliminary etching experiment using TMGa did not yield any signs of Ga_2O_3 etching. Instead, exposing the Ga_2O_3 surface to TMGa for an extended period resulted in a black coating on the surface. We believe the deposited coating is due to carbon from the methyl group, which is the by-product during TMGa pyrolysis, and blocks gallium from accessing the surface. The real mechanisms of nature of formation of coating is not understood.

TBCl, which we have shown to remove gallium metal deposits from the TEGa etched surfaces, can also etch Ga_2O_3. For a molar flow rate of just 50 μmol/min, a low value used for removing gallium metal deposits, the etch rate is too small to measure. But when this rate is increased by at least a factor of 10, etching of Ga_2O_3 by TBCl is observed, provided that the etching is conducted at a high substrate temperatures – that's more than 800 °C.

We have used a fibreoptic reflectometer to monitor the spectral reflectance during the etching, by TBCl, of Ga_2O_3 grown on sapphire (see Figure 7). For this investigation, in our Agilis 100 reactor, we employed a reactor pressure and substrate temperature of 25 Torr and 900 °C. TBCl molar flow rates of 315 μmol/min, 505 μmol/min, 1026 μmol/min, and 1450 μmol/min. As the flow rate increased the period of the spectral reflectance oscillation reduced, indicating an increase in the etch rate. For the highest flow, 1450 μmol/min, etching exceeded 2 μm/hr. This is significantly less than the fastest etch rates with TEGa, which is also a more efficient etchant, as far lower molar flow rates can be used.

We have conducted a number of experiments that are similar to those involving TEGa. We have looked into the etching rates for Ga_2O_3 films exposed to TBCl at various reactor pressures, differing TBCl molar flow rates, and a range of substrate temperatures and oxygen flow rates.

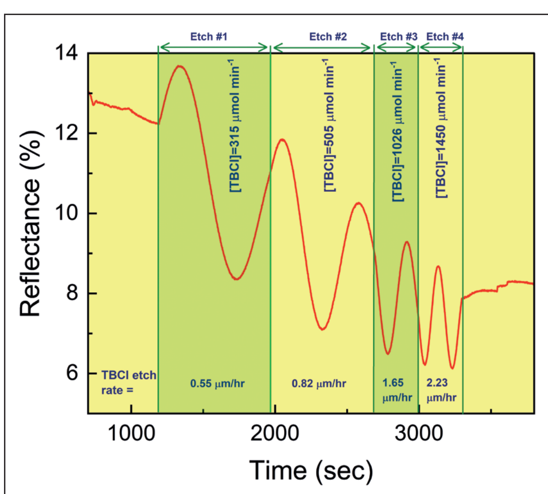
Replicating our observations for TEGa-based etching, we have found that there is an optimal reactor pressure for fast etching, in this case 25 Torr (see Figure 8(a)). For a constant pressure and temperature, etch rate increased linearly with the increase in TBCl flow rate (see Figure 8 (b)).

At higher temperatures, the etch rate of Ga_2O_3 by TBCl increases. For low substrate temperatures, it takes a significantly high flow of TBCl to obtain a measurable etch rate. For example, at a substrate temperature of 700 °C we had to use a TBCl molar flow of more than 1000 μmol/min to observe etching, and even then we only realised a rate of 0.15 μm/hr (see Figure 8 (b)). But when we upped the temperature to 900 °C, the same flow increased the etch rate to 1.65 μm/hr. While this is an improvement, it still much slower than the etch rate for TEGa, highlighting again the inefficiency of TBCl, particularly at low substrate temperatures. We have also explored the effect of introducing oxygen during etching of Ga_2O_3 by TBCl (see Figure 8(c)). This did not prove a success, reducing the etch rate, probably due to the re-deposition of Ga_2O_3 in an oxygen environment.

We have also applied TBCl to the etching of $(Al_{0.13}Ga_{0.87})_2O_3$, grown on a sapphire substrate. Similar to the TEGa etching, the presence of aluminium in the Ga_2O_3 matrix decreased the etch rate, again suggesting that AlGaO can be used as an etch stopper for TBCl.

A power portfolio

To realise the etching results just discussed, those of us at Agnitron have drawn on 15 years of innovation in the compound semiconductor field. While many of our investigations that are detailed in this article involved an Agilis 100, they could have been carried out on other platforms within our MOCVD portfolio.



➤ Figure. 7 Spectral reflectance monitoring the etching of Ga_2O_3/sapphire using TBCl at reactor pressure of 25 Torr and substrate temperature of 900 °C. TBCl flow rates varied from 315 μmol/min to 505 μmol/min, 1026 μmol/min and 1450 μmol/min in a single etch experiment, corresponding to layers labelled as Etch #1, Etch#2, Etch#3, and Etch #4. Etch rates varying between 0.55 μm/hr and 2.23 μm/hr were obtained.

Testimonials for Agnitron

Shubhra Pasayat, University of Wisconsin-Madison

"Agnitron's unparalleled experience and advanced equipment technologies have established them as one of the premier manufacturers of MOCVD systems across a wide range of material systems including dual-use systems. It is their exceptional expertise in various material systems and their ability to customise reactor designs to meet specific user needs and requirements that captured my attention and led me to choose an Agnitron MOCVD reactor for my laboratory.

I have recently acquired a dual-use GaN/Ga_2O_3 Agilis 100 reactor from Agnitron, initially configured for high-temperature nitride growth and easily convertible to Ga_2O_3. I am eager for the tool installation and start up. Throughout the entire process so far, I have been impressed by the outstanding customer support provided by Agnitron. Their team has been highly responsive, engaging in informative discussions and promptly addressing any inquiries or concerns. This positive experience has further solidified my confidence in Agnitron as a reliable and customer-oriented company.

Looking ahead, I am already making preparations to expand my laboratory with the addition of another Agnitron MOCVD reactor, possibly the Agilis Mini. Based on my interactions and experiences thus far, I have no hesitation in wholeheartedly recommending Agnitron as the ideal partner for any MOCVD needs. Their commitment to customer satisfaction, combined with their expertise and cutting-edge technologies, makes them a top choice in the industry. I am confident that their continued support will contribute significantly to the success of my research endeavours."

Hongping Zhao, Ohio State University

"I am pleased to provide a testament to my satisfaction with the two Agnitron MOCVD tools I purchased for my research at The Ohio State University. The initial tool, a first of its kind dual-chamber GaN tool delivered in 2017, and the second, a Ga_2O_3 tool delivered in 2018. The dual-chamber Agilis reactor, a GaN tool, has been used to develop both GaN and novel nitride semiconductors based on II-IV-N_2. The performance and capabilities of this tool has met my expectations. The dual-chamber GaN tool has been used to demonstrate high-quality GaN epitaxy and successful development of $ZnGeN_2$ and $ZnSnN_2$ and their heterostructure and alloys with III-N. Agnitron, for its part, continues to innovate and we're currently contemplating upgrading the tool to further enhance its utility.

The Ga_2O_3 MOCVD system has been very productive. Agnitron's Agilis 100 is an industry standard and we're appreciative of Agnitron's support of the MOCVD system and the assistance provided by their capable technical team. The tool has enabled us to do excellent work, producing world-class Ga_2O_3 material.

Agnitron's customer support to OSU has been excellent. The team is responsive, engaging, and promptly addresses concerns or questions that arise. They are a reliable partner, always there to provide guidance when needed. Based on my experiences, I am pleased with my choice of Agnitron and glad to recommend them to fellow researchers."

The Agilis 100, our most popular MOCVD/CVD system, is renowned for its compact footprint and exceptional versatility. Beyond β-Ga_2O_3, this system is a compelling option for a wide range of experiments. Featuring UV and blue range optical reflectometry integrated into Imperium analytical control software, the Agilis 100 offers real-time measurements of growth rate and thickness. Another feature is the option for UV light exposure during growth, effectively controlling Ga_2O_3 film purity by reducing residual carbon and managing point defects. What's more, the Agilis 100 – and all our other MOCVD/CVD systems – offers seamless switching between sources and gas distribution (showerhead) configurations within two hours of maintenance. Yet another feature is the ability to add precursor distribution nozzles, enabling process refinement or wafer carrier cleaning, adding to the attributes that make our tools an attractive choice across diverse applications.

To address the high cost of wafers and gas consumption in R&D, growth must be undertaken on a single large-area wafer. Our β-Ga_2O_3 MOCVD/CVD reactors, specifically the Agilis 500/700, now accommodate wafers up to 4-inch and 6-inch in diameter, respectively. These larger multi-wafer reactors have an identical footprint to the Agilis 100, aiding scientists interested in growing larger diameter wafers with a matching fab line.

At the heart of the majority of our tools is a proprietary vertical growth chamber featuring a high-speed rotating disc reactor that's capable of operating at over 1300 revolutions per minute. We minimise the chances that any deposition within the chamber will reach the wafer surface through material science and design engineering.

The unique flow dynamics in our high-speed rotating disc reactor repress particle recirculation, leaving areas above the wafer clean and free of deposition. Another asset of the high-speed rotation of our rotating disc reactor is that it allows a higher degree of control, ensuring superior thickness distribution uniformity.

Recently, we delivered the Agilis Mini to a number of universities. Earlier this year we installed one at the University of Notre Dame in Indiana, where it is going to be used to research high-purity materials for quantum computing. We have also shipped an Agilis Mini to ASU for the high-temperature growth of AlGaN/BN compounds. The appeal of this particular model is that it has the same capabilities and versatility as the Agilis 100, but with a smaller footprint and a more cost-effective price.

Our line-up continues to expand. Soon we will launch the Agnitron GOX 300, a fully automated production Ga_2O_3 MOCVD/CVD system that offers further capabilities for larger wafers. Additionally, Agnitron is proud of our commitment to continuous improvement and customer support, ensuring

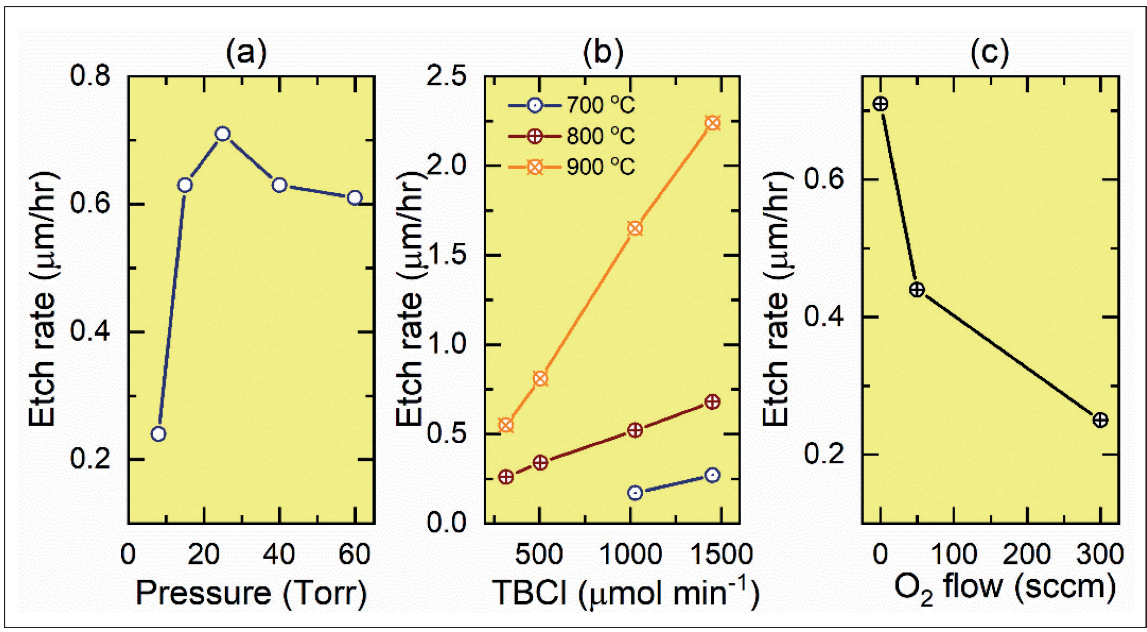


Figure 8. Etch rate of β-Ga_2O_3 on sapphire, as a function of etch parameters, using TBCl etchant. (a) Etch rate versus chamber pressure at a substrate temperature of 800 °C and a TBCl molar flow rate of 1450 μmol/min. (b) Etch rate versus TBCl molar flow rate at a constant pressure of 25 Torr and a substrate temperature of 700 °C, 800 °C, and 900 °C. (c) Etch rate versus oxygen flow rate at a constant pressure of 25 Torr, and a TBCl molar flow rate of 1026 μmol/min.

that each new generation of our Agnitron reactors provides greater reliability and versatility for process engineers. We strive to keep pushing the boundaries of semiconductor technology by collaborating with researchers and industry partners worldwide. Another significant advancement, scheduled to be introduced in the third quarter of 2023, is the first MOCVD/CVD reactor designed for research and development purposes, featuring high-temperature, low-pressure metalorganic precursor delivery. This ground-breaking innovation further expands the capabilities of MOCVD/CVD techniques. Initially, this feature will be offered on the Agnitron Agilis 100 reactor, making it the first reactor capable of delivering precursors into the chamber at temperatures of up to 200 °C. This breakthrough empowers researchers to explore the growth of new compounds and heterostructures via MOCVD/CVD, facilitating the development of novel and improved devices, as well as investigating new elements as potential dopants.

We are also proud of our patent-pending technology, which upgrades the showerhead gas distribution design. This system, in combination with the fast rotation of our rotating disc reactors, leads to superior thickness and doping uniformity of epitaxial layers.

The milestones that we have met over many years have helped us to play a key role in important projects. This includes an AFRL SBIR project to develop Ga_2O_3 growth on large-area substrates. In this project, we are planning to use Agnitron Agilis 700 and GOX 300 systems to scale up the growth of Ga_2O_3 epitaxial structures from small substrates to those that are 4-inch in diameter and beyond.

In short, Agnitron's hardware engineering department continues to make improvements to our tools, to ensure that each new generation of Agnitron reactors provides greater reliability and versatility for process engineers. In addition, we continue to support research activities, such as the efforts on etching described in this article. By supporting and driving advances in all aspects of Ga_2O_3, we are helping developers of this ultra-wide bandgap oxide to race along the path from device development to commercialisation, and embark upon a new era for high-voltage power electronics.

FURTHER READING

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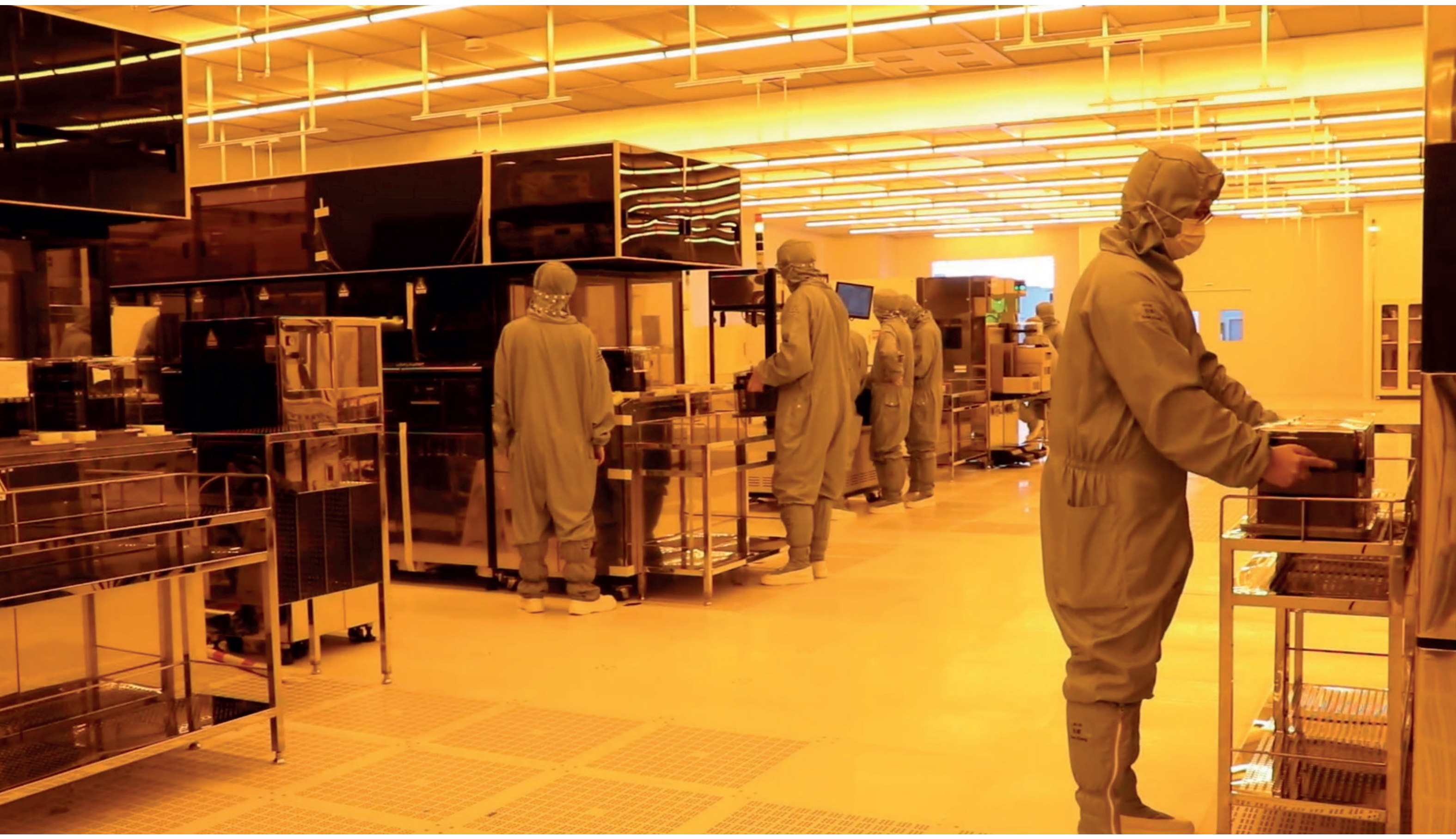


Banishing barriers to GaN adoption

With performance advantages of GaN established and the challenges of driving GaN HEMTs overcome, now is the time to address the outstanding concerns of designers, such as price, availability and reliability

BY DENIS MARCON FROM INNOSCIENCE EUROPE

IT'S NOT THAT HARD to spot the significant benefits that come from replacing silicon power devices with those made from GaN. Consider, for example, e-bike chargers, which are 75 percent smaller when they incorporate GaN, allowing them to fit in a backpack; or USB-PD laptop chargers, which are around one-third of the size of those incorporating silicon-based devices; or data centre DC/DC converters, where the introduction of GaN halves the size and delivers a substantial hike in efficiency.

There are many reasons behind the application advantages provided by GaN, which is now well known for enabling reductions in size and gains in efficiency. One significant asset of devices made from this wide bandgap semiconductor are their absence of reverse recovery current, facilitating simpler architectures. And there are additional benefits, including: GaN's ability to function at a higher frequency than silicon, thereby permitting the deployment of smaller passives; the significantly lower specific on-resistance, allowing GaN devices to be much smaller; and a 10-times-better figure of merit, based on the product of the on-resistance and the gate charge, that leads to far higher efficiencies. As a result, GaN will continue to proliferate in all application areas, including consumer, industrial, automotive and renewables, with uptake increasing the performance of all power conversion systems while trimming size, boosting efficiency and cutting costs.

GaN: the compelling case

Today, the market for GaN is buoyant, thanks to the laying to rest of previous concerns. However, that hasn't stopped some designers of power converters from harbouring doubts that are slowing the mass uptake of GaN. The reasons for this reluctance chiefly centre around price and high-volume availability, but there is also anxiety surrounding second-sourcing.

The smartphone market ably illustrates these points. Despite a slight fall in shipments, well over one billion units are still sold every year, encouraging suppliers of GaN power devices to get their products designed into phone handsets. But before this occurs, four obstacles must be overcome. First, there needs to be a clear advantage behind this move. In addition, the GaN device must replicate the very low gate leakage characteristic of silicon; sell at a competitive price; and be available in massive volumes, to sustain the billion smartphones sold per annum and to meet demand for a quick ramp, to match the 6-to-9 month cadence of new model introduction.

At Innoscience we tick all those boxes. But that's not all. We are innovating, with products such as the market's first bi-directional GaN. This technology, which we refer to as VGaN, delivers clear and compelling benefits. It enables a superior alternative to the conventional approach to blocking current in both directions, which is to use an over-voltage protection unit in a battery management system that features two back-to-back silicon MOSFETs. Thanks to our progress, this pair of transistors can be replaced with a single VGaN HEMT, delivering an alternative that's 50 percent smaller and more efficient (see Figure 1).

One of our breakthroughs has been to address concerns associated with the leakage current. Many designers are not used to having to consider this, because the oxide under the gate of a typical silicon device blocks leakage. The oxide layer is not present in GaN HEMTs, and the gate can be modelled as two back-to-back diodes (see Figure 2).

To reduce leakage, we have optimised the epitaxy, device architecture and processing. Thanks to advances on all these fronts leakage has plummeted by almost a factor of ten, falling to below 3 μA at 85 °C for the lifetime of the device. It's a level of performance that's welcomed by smartphone manufacturers, and one that ensures that VGaN HEMTs are suitable for use as the load switch within handsets.

This innovation illustrates that if a company is to be a leading GaN supplier, it must be an integrated device manufacturer. Fabless companies will struggle to innovate, because they do not have the inherent ability to optimise epitaxy, architecture and processing.

If you scrutinise price and availability, you'll soon see why GaN has failed to establish its presence in the smartphone market, despite the growing desire of both customers and suppliers. For a 10 percent market penetration of the one billion phones sold in 2022, makers of GaN power devices would need to produce 100 million units a year. To manufacture this volume requires the processing of either 3,000 8-inch wafers per month, or 5,400 6-inch wafers per month. If for a moment we ignore the capabilities of Innoscience, the total global capacity of GaN is only 16,000 6-inch wafers per month, according to market analyst Yole Intelligence. Consequently, this single application would demand about a third of the world's capacity!

It's a markedly different state of affairs once our capacity is accounted for. We are the biggest integrated device manufacturer completely focused on GaN. By using 8-inch wafers, we can produce GaN devices cost-effectively in extremely large volumes. Our capacity continues to climb, and by 2025 we will be producing 70,000 8-inch wafers every month, dwarfing the combined production of all other manufacturers.

The reliability issue

Crucial to success is reliability. For huge companies, such as the smartphone maker Oppo, GaN could never be incorporated within the handset if reliability were in doubt.

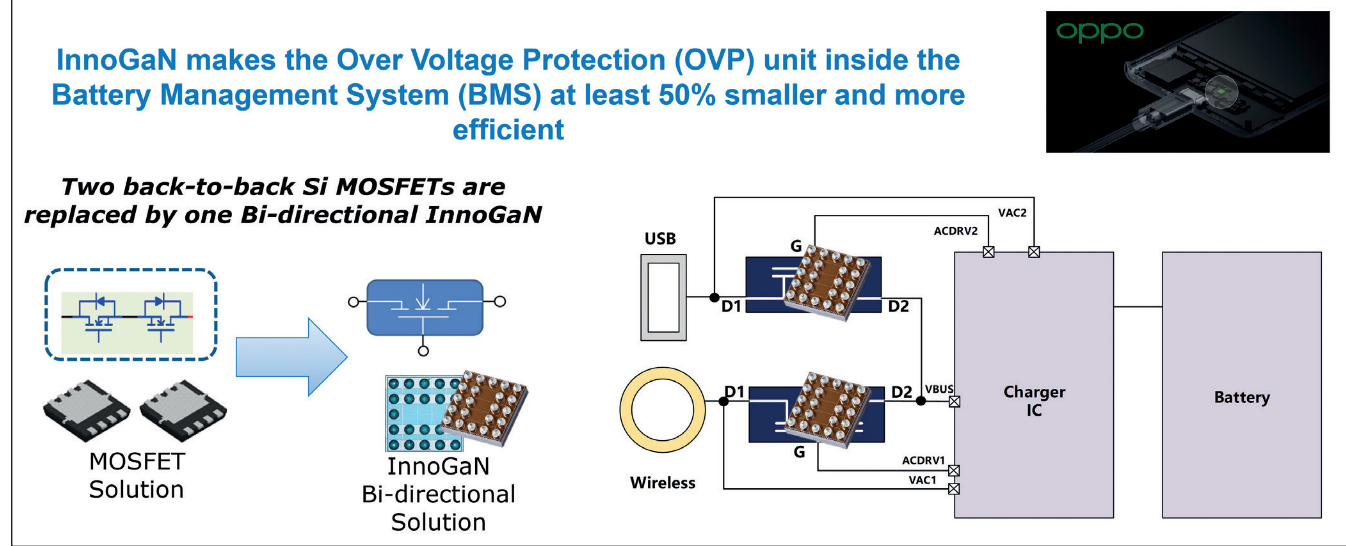


Figure 1. One VGaN can replace two back-to-back silicon MOSFETs.

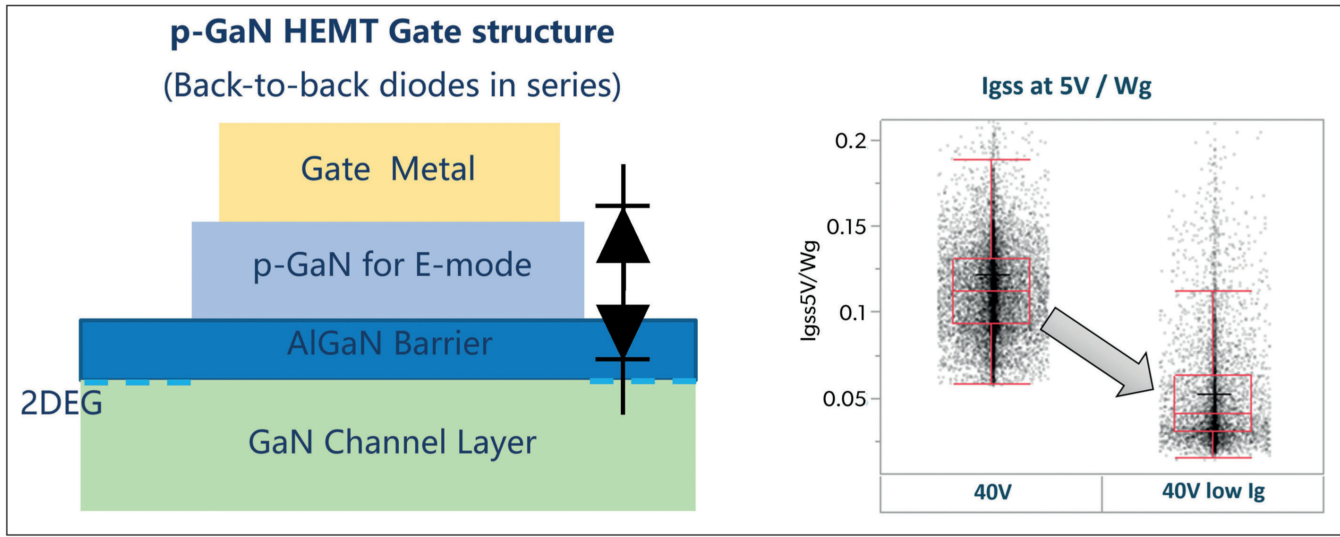


Figure 2. Optimisation reduces leakage to below 3 μA.

We have demonstrated that our devices are strong in this regard. According to evaluations described by JEDEC and accelerated life tests, we have 10-parts-per-million device failure rates for the gate acceleration factor mode that exceed 20 years (see Figure 3). The equivalent figure for the drain is more than 10,000 years.

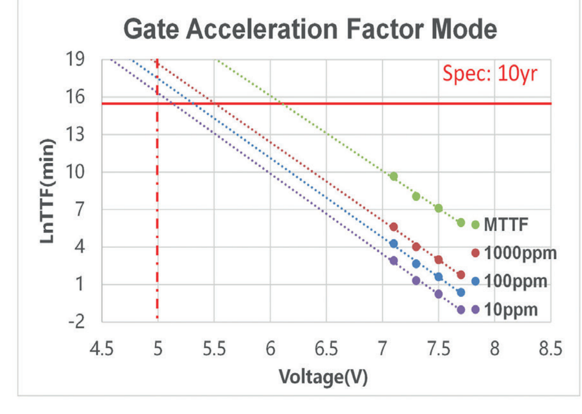
Another crucial factor is avalanche ruggedness, a vital characteristic for silicon power MOS devices. To evaluate this capability, engineers tend to perform an unclamped inductive switching test.

To carry this out, the test device is turned on, causing the inductor to charge at a linear rate. Once the drain current is high enough, the device is turned off, causing the inductor to dissipate its stored energy. This drives the device into breakdown. The avalanching capability of the test device permits the dissipation of the inductor current, therefore restricting any further increase in voltage. The test device remains in breakdown until total energy dissipation.

We translate the results of this test into values for the time-in-avalanche and the energy-in-avalanche that the device can support. If the power device does not have avalanche capability, it must offer a far higher breakdown voltage to allow complete energy discharge of the inductor. This is the case for our devices, where a high breakdown voltage fulfils the inductive switching rating. For our low-voltage devices, the breakdown voltage is more than double the device's rating, ensuring that these products handle voltage spikes safely and successfully pass such critical tests.

Data centres

Smart mobile devices are certainly not the only market for GaN. Of the other opportunities, data centres offer a huge and growing market that is exceptionally power-hungry. Here, efficiency is the number one priority. Even an increase in efficiency of just 0.1 percent provides considerable cost savings. The miniaturisation that GaN enables is also valued, with smaller power conversion systems freeing up more space for computing units.



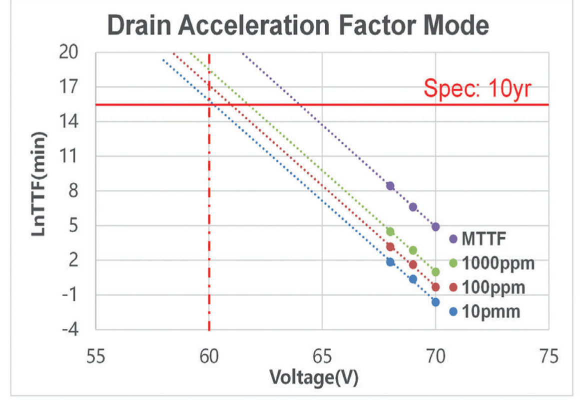
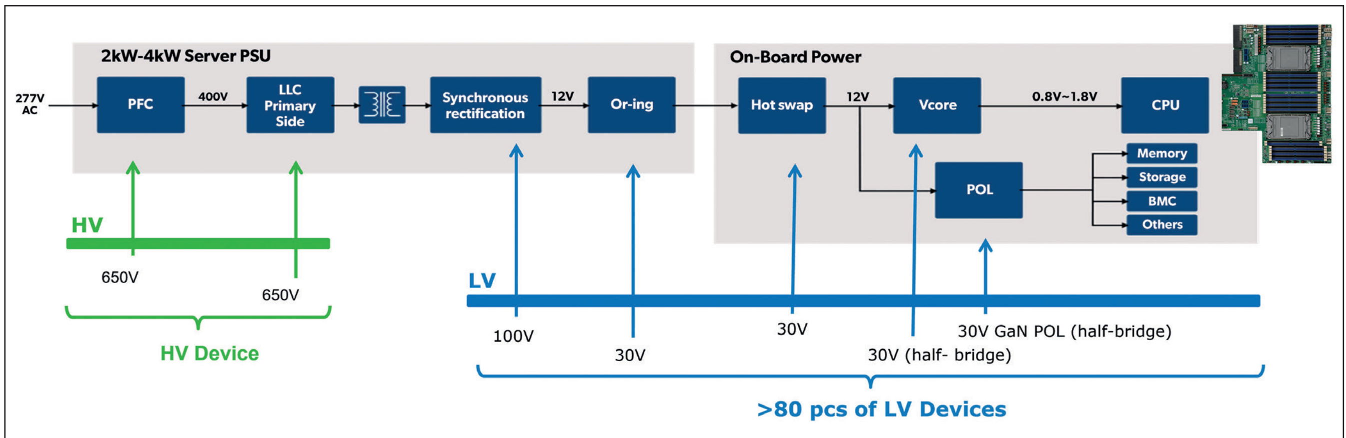


Figure 3. Accelerated life tests highlight the reliability of low-voltage VGaN.



➤ Figure 4. There is huge demand for GaN in power-hungry data centres.

However, to secure sales, GaN suppliers must also offer a large and available product capacity, as well as low prices.

Beginning with the transition from AC to DC, Figure 4 outlines the power conversion phases within a data centre. A normal design at the primary side, incorporating power factor correction and a pair of inductors alongside a capacitor, typically deploys 650 V devices. Meanwhile, on the low-voltage side, it's the norm to use 100 V and 30 V parts when getting down to point-of-load devices. Here, typically as many as 80 or more low-voltage power transistors are used for every implementation. All of these parts must be deliverable in volume and at the right price.

The benefits of our devices are illustrated in a 600 W full-bridge, constructed using a pair of inductors and a capacitor. When built using four of our 3.2 mΩ 100 V GaN INN100W032A HEMTs, the resulting design is just a quarter of the size of that based on a silicon solution, while delivering a 0.6 percent gain in efficiency. This equates to a reduction in energy consumption of almost 10 percent, ensuring significant costs savings and lower CO_2 emissions.

Integrated solutions

Further reductions in size are possible with integration. Consider, for example, our SolidGaN ISG3201, an entire half-bridge circuit that trims size by another 20 percent (see Figure 5). In this single-land-grid array package, measuring just 5 mm by 6.5 mm by 1.1 mm, there are two GaN HEMTs in half-bridge configuration, along with a driver and a bootstrap capacitor.

Note that the benefits of integration are not limited to scaling sizes. This approach also leads to higher performance, due to the package embedding connections between circuit elements. Consider once more the 600 W 48 V/12 V DC/DC converter for data centres. By introducing the ISG3201, designers can increase the power density and reach 1000 W in the same-size module at a heightened efficiency of 98.26 percent. This gives our customers the chance to choose between: a discrete solution, such as the INN100W032A, which offers greater flexibility; and an integrated solution, such as the ISG3201, which is easier to mount and use.

We have also directed our attention at the high-voltage sector with a portfolio of 650 V HEMTs with on-resistances ranging from 30 mΩ to 2.2 Ω. Again, we are aware that some designers will have concerns relating to avalanche failures due to high-voltage spikes. Once more, our approach to addressing this is to ensure headroom in the blocking voltage. Since GaN transistors – unlike those made from silicon – do not have an avalanche rating, the only way to avoid this form of failure is to select a device with a much larger breakdown voltage than the specified voltage rating. Our 650 V-rated devices can withstand non-repetitive pulses below 200 µs at up to 800 V, which is well above the maximum rating. When the duration of the repeat pulses shortens to below 100 ns, the maximum transient voltage our component can maintain falls to 750 V, both at room temperature

➤Innoscience produces devices at its 8-inch fab in Suzhou, China.

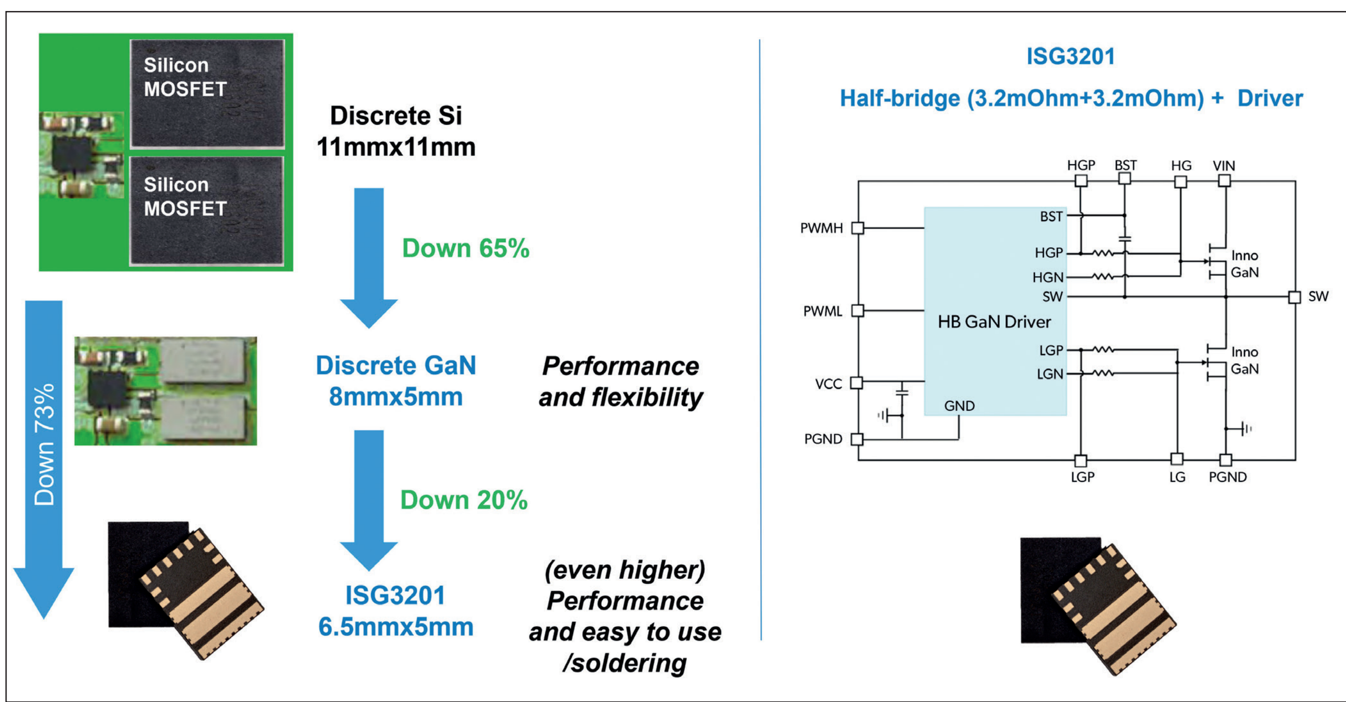


Figure 5. Integrated SolidGaN solutions offer size, performance and ease-of-use benefits.

and at 125 °C. This is still far beyond the 650 V rating, and adds to our collection of data that supports very reliable use.

Dual sourcing

For very good reason, some of our customers are reluctant to rely on a single supplier. But they don't have to, as multiple sources of GaN parts are emerging. For example, our 650 V/700 V devices in a DFN 8x8 or 5x6 package are pin-to-pin compatible with parts with a similar rating and specifications. What's clear is that there are no longer any barriers to GaN adoption in the mass power semiconductor market. Gone are the days when there would be concerns related to high-volume availability, price, compatibility between manufacturers, reliability at both low and high voltages, and avalanching. In short: the future is GaN.

Reducing the on-resistance with a strain layer

INNOSCIENCE'S GaN HEMTs are intrinsically enhancement-mode (E-mode) devices.

This much-preferred, fail-safe mode of operation, which is known as normally-off, is realised by growing a *p*-GaN layer on top of the AlGaN barrier, followed by the deposition and patterning of a gate metal and the selective recessing of the *p*-GaN layer over the AlGaN barrier. The gate metal layer forms a Schottky contact with the *p*-GaN layer and, as a consequence, the potential in the channel at the equilibrium is elevated to ensure normally-off operation.

By controlling all its manufacturing process stages in-house, Innoscience has been able to develop several technology improvements that have been key to optimising GaN HEMT manufacture for high performance and reliability, as well as mass production and cost reduction.

One of the critical parameters that determines transistor performance is $R_{DS(on)}$ – this is the total drain-source on-resistance per unit area. $R_{DS(on)}$ determines the maximum possible current rating of the switch and influences current loss, and thus efficiency. Consequently, by minimising the specific $R_{DS(on)}$, engineers can trim device size for a given on-resistance, and ultimately produce more parts per wafer, cutting costs.

To reduce specific $R_{DS(on)}$, Innoscience has developed a strain enhancement technology. A strain enhancement layer is deposited onto the wafer, immediately after the gate stack definition. Stress modulation created by this strain-enhancement layer induces additional piezoelectric polarisations; this causes the density of the two-dimensional electron gas to increase, leading to a fall in sheet resistance by 66 percent when compared with a device without the strain layer.

Crucially, since the strain enhancement layer is deposited after gate formation, it only affects the resistance in the access region. There is no impact to other device parameters, such as threshold and leakage. Thanks to this patented technology, Innoscience's GaN-on-silicon E-mode HEMTs exhibit a very low specific on-resistance.

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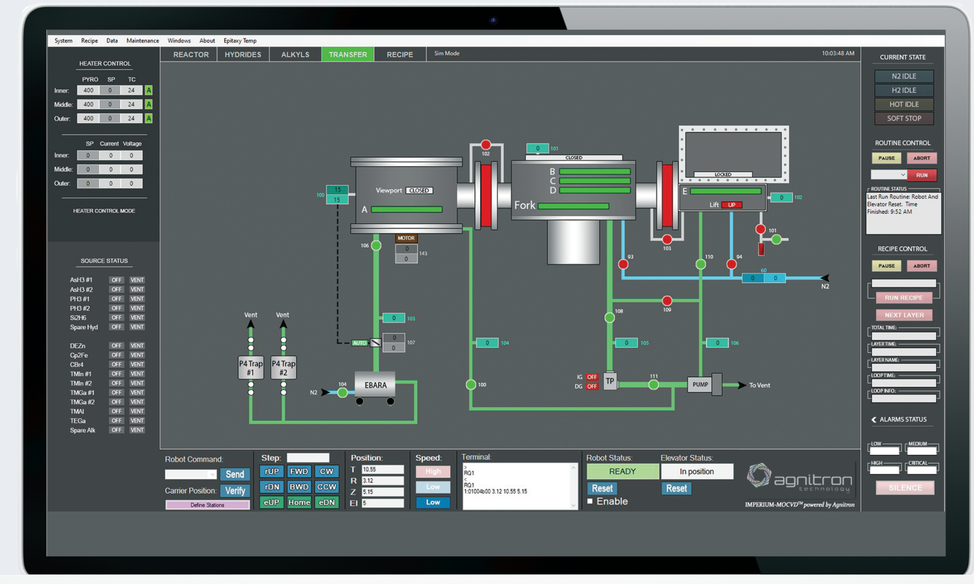

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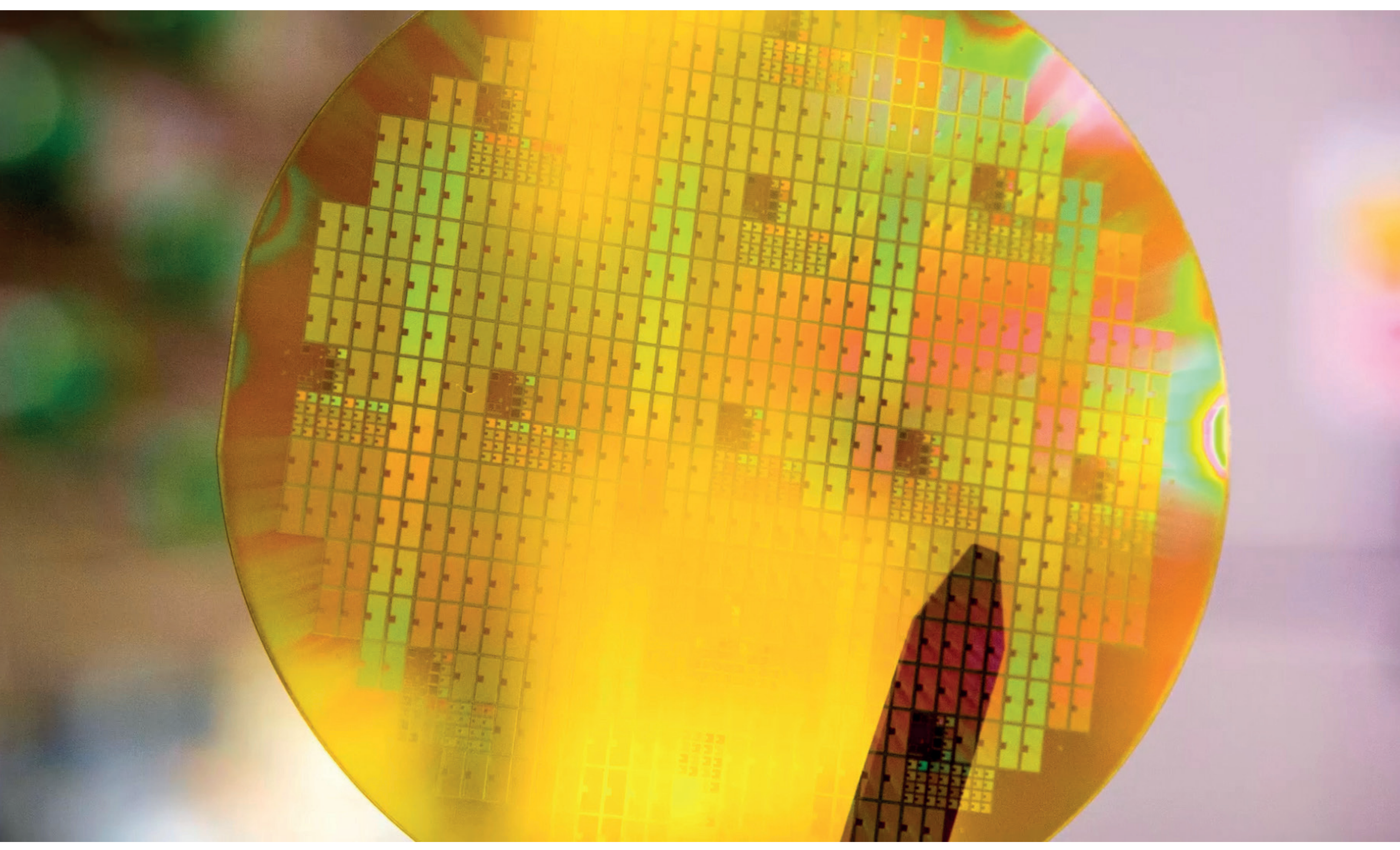


A superior process for the SiC superjunction

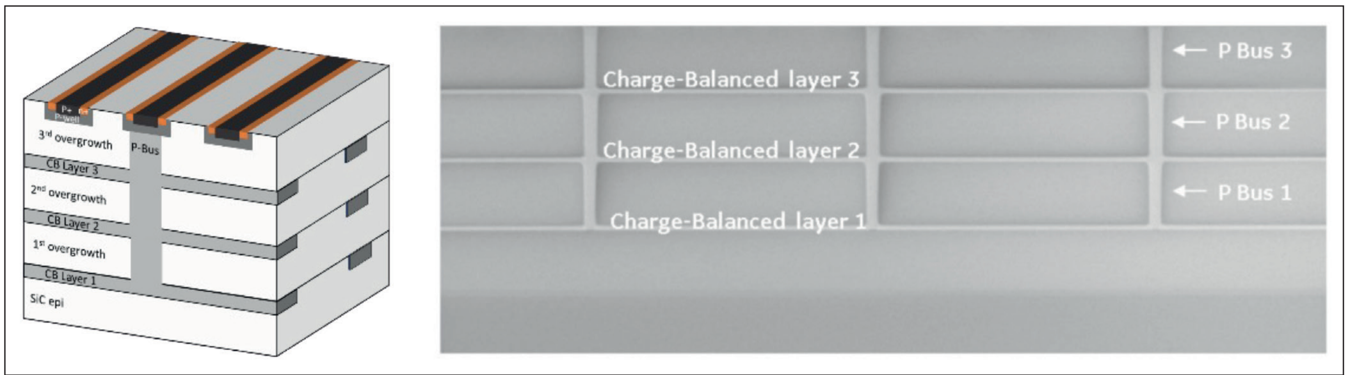
Rounds of ultra-high-energy implantation and epitaxial growth enable the realisation of devices with a SiC superjunction that block several kilovolts

BY REZA GHANDI FROM GE RESEARCH

TO TRIM the global carbon footprint much effort must be devoted at improving electrical infrastructure. As well as the most obvious priority on that front – increasing the proportion of energy that's generated from renewable sources – there needs to be an increase in the efficiency of electrical transmission, right from where power is generated to where it is used.

A key part of electrical infrastructure is the medium-voltage power-conversion system, which may be used in wind turbines, solar installations and marine converters. Operating at voltages above 3.3 kV, this class of power-conversion system is limited to switching frequencies of no more than several hundred hertz, due to losses in silicon-based solid-state switches and diodes. That's far from ideal, because at these low frequencies transformer and converter filter weights can be as high as several tons, which increases system and installation costs and limits design flexibility. What's needed is a shift to highly efficient, lightweight, multi-megawatt/multi-kilohertz power-conversion systems based on ultra-high-voltage power semiconductor devices that switch at moderate frequencies, such as 1-20 kHz.

If you are a regular reader of this publication, you will know that SiC devices can solve many of the limitations of the silicon-based incumbents. But at blocking voltages of several kilovolts, success with this approach is far from trivial. A formidable challenge arises because at blocking voltages of 3.3 kV or more, SiC unipolar switches and diodes suffer from high conduction losses at elevated temperatures, while SiC bipolar devices, such as IGBTs, exhibit a prohibitive high forward-voltage drop of 3 V. Therefore, in these systems, the advantages of SiC technology over that of the silicon IGBT are diminished.

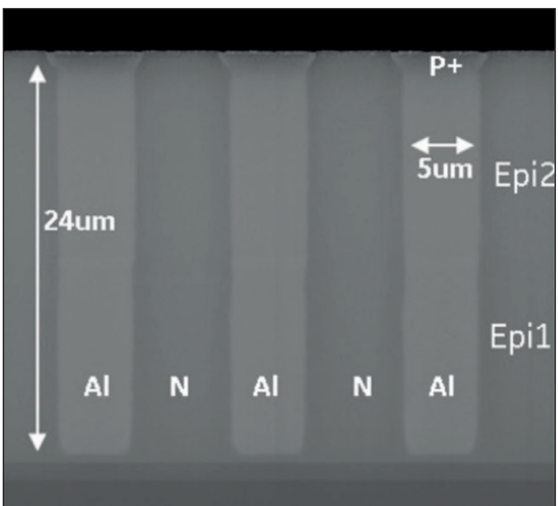


➤ Figure 1. Schematic view (left) and scanning electron microscopy, cross-sectional view (right) of GE's 4.5kV SiC charge-balanced (CB) MOSFET. These switches implement epitaxial regrowth and high-energy implantation similar to SJ devices.

One solution that's attracted interest is the SiC superjunction. This architecture breaks the unipolar conduction limit and offers an improved trade-off between the specific on-resistance and the blocking voltage in medium-voltage-class applications.

To date, there have been a few demonstrations of this device. They include multi-epitaxial SiC superjunction devices that span 1.2- 3.3 kV, and are formed with a multi-epitaxial approach. Fabricating such devices is not straightforward, as it requires several iterations of epi regrowth, due to the shallow projectile depth of implanted atoms in SiC using conventional process tools. An alternative is to make a trench-refill SiC superjunction device. However, although that device can handle 6.5 kV, it suffers from excessive leakage at high blocking voltages, due to crystallographic defects from a complex refill process.

At GE Research we are currently exploring a novel, third fabrication architecture for producing devices operating above 3.3 kV, based on ultra-high-energy implantation and epitaxial growth. This technology draws on our pioneering capabilities in SiC charge-balanced device fabrication, developed from a recently completed project funded by ARPA-E (the ARPA-E DE- AR0000674 "SiC charge balanced FETs for Breakthrough Power Conversion" programme). In that programme, we developed a superjunction intermediate charge-balanced technology. This involved the implementation of a novel drift layer architecture, to create buried charge-balanced *p*-type regions, which are electrically connected to the top body contact through mega-electron-volt, high-energy implanted regions (denoted P-Bus, as shown in Figure 1). As is the case with superjunction pillars, if the charge-balanced regions are designed with the optimum implanted *p*-type dose and spacing, they deplete surrounding areas during blocking and act as electric field dividers. The key implication is that for a given breakdown voltage, it is possible to use a drift layer with higher doping than that in a traditional design, that enables a lower on-resistance in forward conduction mode and obliterates the conventional, one-dimensional limits for the specific on-resistance as a function of breakdown voltage.



➤ Figure 2. World's first 3.5 kV deep-implanted SiC superjunction, junction barrier Schottky (JBS) diode with two rounds of epitaxial overgrowth and ultra-high-energy implantations fabricated at GE Research.

Using this approach, we began by producing devices that have a comparable performance to that of a 20 μm pitch SiC superjunction – and are significantly better than state-of-the art high-voltage SiC approaches. Recent highlights from that effort include the first experimental demonstration of charge-balanced MOSFETs with a differential specific on-resistance of 10 mΩ cm^2 and a blocking voltage of more than 4.5 kV. This value for the specific on-resistance is below the one-dimensional specific on-resistance as a function of blocking voltage, and is nearly 20 percent below that for conventional 4.5 kV SiC FETs reported. To our knowledge, this is the highest breakdown voltage for any SiC charge-balanced device demonstrated to date, and the lowest on-state loss for any 4.5 kV-class MOSFET reported.

While we are encouraged by this success, we know it's just a start. One downside of this device is that due to its stacked nature for charge balancing, and the charge carrier redistribution required

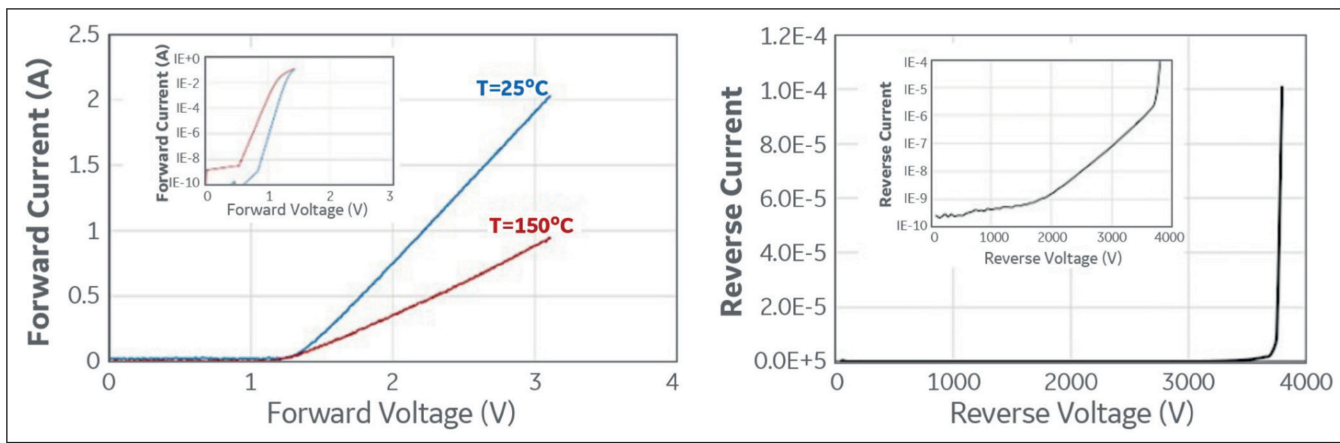


Figure 3. Forward and reverse current-voltage (I-V) characteristics of 3.5 kV deep-implanted SiC superjunction, junction barrier Schottky (SJ JBS) diode. The specific on-resistance, $R_{on,sp}$ is 4.5 mW cm^2 (45 percent below SiC unipolar limit).

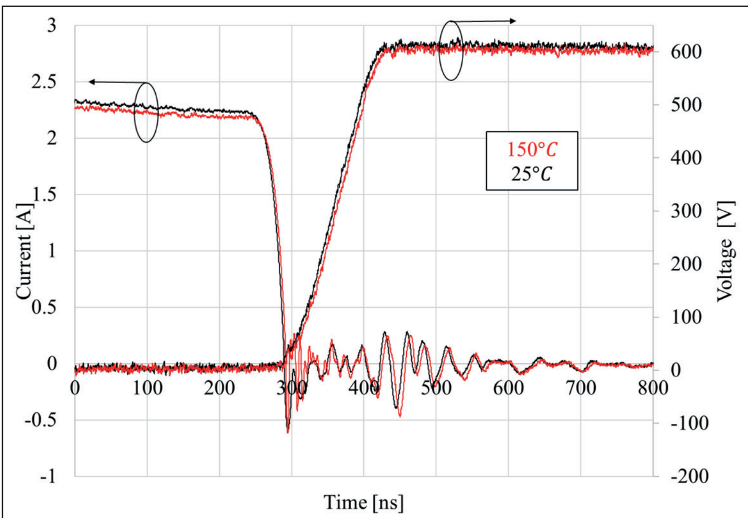


Figure 4. Reverse recovery characteristics of 3.5 kV SiC deep-implanted superjunction, junction barrier Schottky (SJ JBS) diodes at room temperature and 150°C.

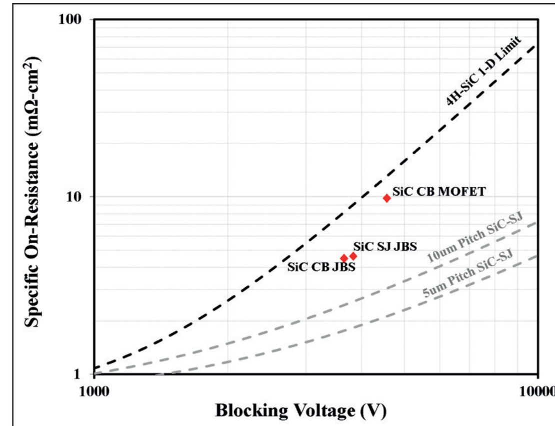


Figure 5. Comparison between GE's reported charge-balanced and deep-implanted superjunction devices, together with the 4H-SiC unipolar and superjunction limits.

during switching, there are switching delays, which increase with each additional layer. These delays are prohibitive when scaling SiC charge-balancing devices beyond 4.5 kV.

To build on our initial efforts, we are now extending our charge-balance architecture to full superjunction devices, supported by further funding from ARPA (ARPA-E DE-AR0001007 "Advanced Medium Voltage SiC-SJ FETs with Ultra-Low On-resistance"). Our latest work involves the fabrication of full superjunction devices based on deep implanted pillars, developed for charge-balance devices to overcome the limitations imposed by the charge-balance carrier distribution delay.

Breaking new ground, our team has demonstrated the world's first 3.5 kV SiC superjunction deep-implanted junction barrier Schottky (JBS) diodes (see Figure 2). These devices, a significant milestone for SiC, will provide a stepping stone for our development of 3.3 kV SiC SJ MOSFETs.

The deep-implanted superjunction diodes that we have produced are formed using two rounds of epitaxial overgrowth (12 μm each), leading to a total drift layer thickness of 24 μm. The *p*-doped and *n*-doped pillars were created using two rounds of high-energy implantations (MeV), enabling a maximum junction depth of 12 μm.

We have measured the forward and reverse current-voltage characteristics of our superjunction JBS diode (see Figure 3). This device turns on at 1.4 V and has a specific on-resistance of 4.5 mΩ cm^2 at room temperature and 9.6 mΩ cm^2 at 150 °C, which is about 45 percent below the SiC unipolar limit. Breakdown voltage is 3.8 kV. We have observed low leakage prior to breakdown, suggesting that there is low defectivity following high-energy implantation, epitaxial overgrowth and an activation anneal at 2,000 °C.

Using the ITC57300/57220 from AGVA Technologies (see Figure 4), we have carried

out reverse recovery measurements of SiC superjunction diodes. We did not observe any change in the turn-off current and voltage waveform when increasing the junction temperature from ambient to 150 °C. We estimate the total capacitive charge to be below 700 nC/cm^2.

Benchmarking our charge-balanced and superjunction devices against 4H-SiC unipolar devices and superjunction limits demonstrates the effectiveness of both our technologies (see Figure 5). They are an attractive alternative to the multi-epitaxial and trench-refill approaches to making superjunction devices, and they offer a scalable solution towards the realisation of medium-voltage-class, high-frequency, solid-state switches.

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DEAR0000674 and DEAR0001007 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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Building better blue and green lasers

Full-colour laser projectors and laser TVs are set to benefit from blue and green laser diodes with very impressive wall-plug efficiencies

BY YOSHITAKA NAKATSU, TSUYOSHI HIRAO, TOMONORI MORIZUMI, YOJI NAGAO, SHINGO MASUI, TOMOYA YANAMOTO AND SHIN-ICHI NAGAHAMA FROM NICHIA CORPORATION

FOUNDED IN 1956 and headquartered in Anan, Japan, our company, Nichia, is a well-known manufacturer of chemical materials, LEDs and laser diodes. For more than 50 years we have been playing an active role in the business related to displays. Back in 1970, we started to manufacture phosphors for colour TVs, and a year on we began to produce phosphors that are used in our customer's high-pressure mercury lamps, a key element in projection displays. We shot to worldwide fame in the 1990s with the invention of the high-brightness blue LED, which we started to manufacture in 1993. Building on this success, in 1995 we produced the world's first electron-injection InGaN-based laser diodes. That particular success has played a pivotal role in the development of

laser-based displays, such as laser projectors and laser TVs. The market for these displays, which employ lasers emitting the three primary colours of red, green, and blue, continues to grow.

A direct emission portfolio

As well as being the pioneer of the blue laser diode, we are the first company to commercialise watt-class green laser diodes. Both feature in our laser diode portfolio, which has sources spanning 375 nm in the UV to 532 nm in the green. Makers of displays can use our lasers alongside red laser diodes, which are commercially produced by a number of other companies.

The combination of red, green and blue lasers has much promise for projectors, thanks to its prowess on the colour diagram. When united, these three sources produce an expanded colour gamut, ensuring that a wider variety of colours are produced, ultimately making it possible to create images that stimulate the senses. There is also an appeal from a business standpoint: laser diodes can offer a low power consumption and a long life, helping to trim the running costs of a cinema.

Here we detail the latest developments in our blue and green laser diodes. When these sources, plus variants in the red, emit narrow wavelengths, this enables the creation of displays that express extremely rich colours. In terms of maturity, red and blue lasers are out in front, with mass production well established. The most common green source is actually one based on the second-harmonic-generation of a 1064 nm laser – the result is a complex contraption with a power conversion efficiency for a commercial device of typically only about 6.5 percent. Due to this shortfall in performance, high-efficiency green laser diodes are eagerly anticipated for driving the deployment of laser projectors.

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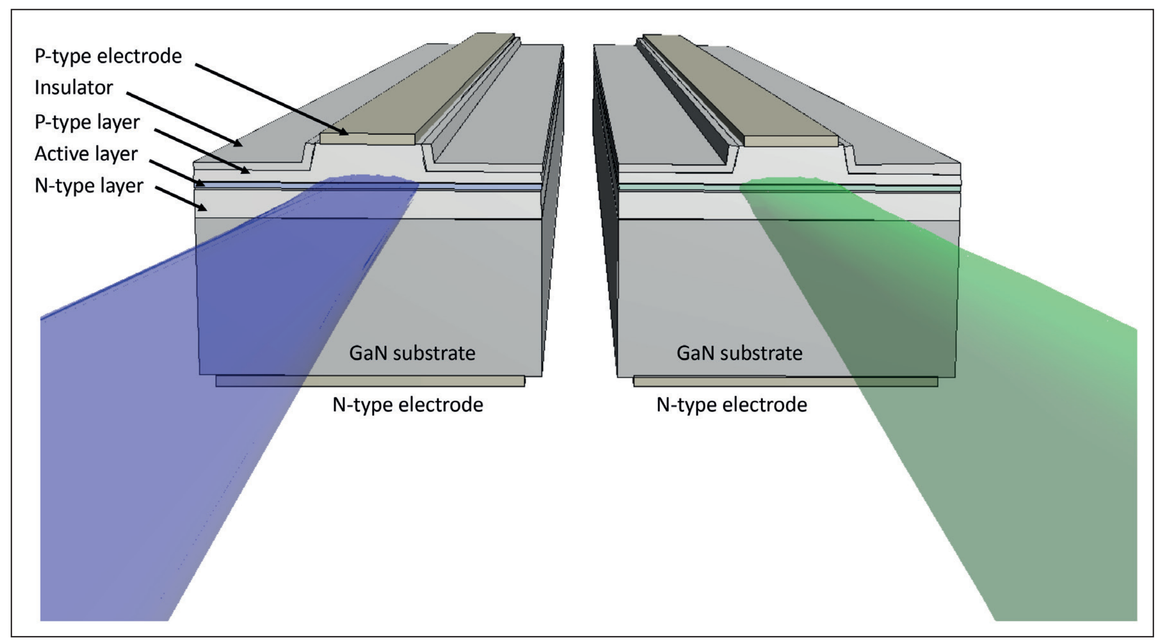
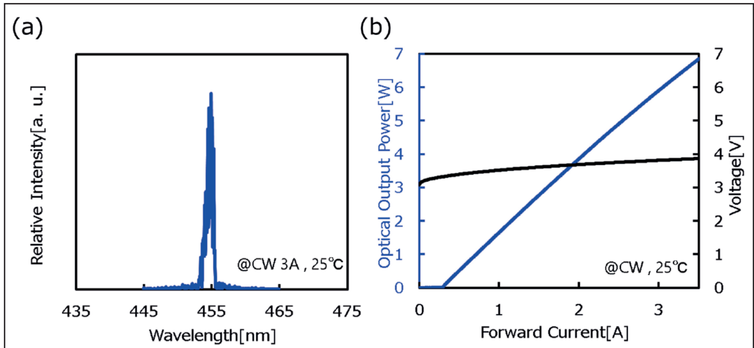
Recording-breaking blues and greens

Why is it so difficult to make a green laser diode? If your starting point is its blue cousin, you have to shift emission to the green by increasing the indium content in the quantum well, because this narrows the bandgap. Unfortunately, there is a downside to this move, with strain introduced into the active region due to InN having a much bigger lattice constant than GaN. Strain leads to degradation, hampering the radiative recombination between electrons and holes in the quantum wells. What's more, piezoelectric polarisation is introduced, as the indium content increases due to the distortion of the crystal structure, and this alters the profile of the energy band structure. Impacts include a shift in the emission wavelength, and a decrease in luminescence efficiency that stems from a reduction in the carrier recombination probability.

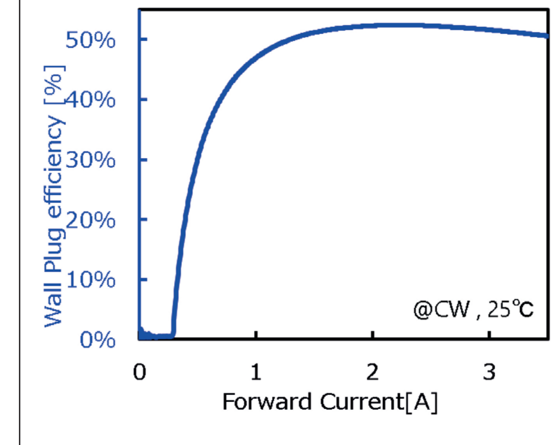
To suppress the piezoelectric field, some groups turn to non-polar GaN substrates, which are limited



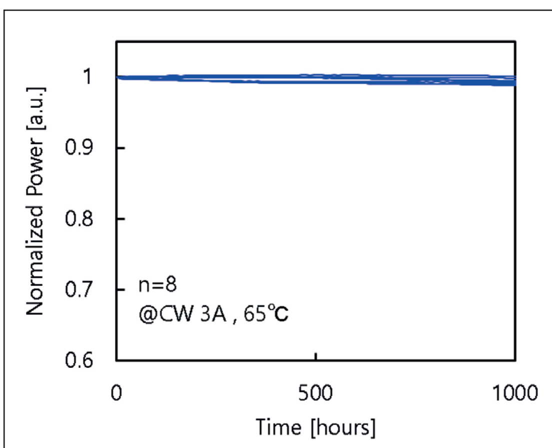
➤ Figure 1. Nichia's multi-mode blue and green laser diodes.



➤ Figure 2. (a) The emission spectrum under 3 A CW and (b) current-light (I-L) and current-voltage (I-V) characteristics of a Nichia blue laser diode under CW operation at 25 °C.



➤ Figure 3. Current-WPE (I-WPE) characteristics for a Nichia blue laser diode under CW operation at 25 °C



➤ Figure 4. Lifetime test results of Nichia's blue laser diodes under an automatic current control of 3.0 A CW operation at a case temperature of 65 °C. Operating current is normalised by its initial value.

in size and availability. We prefer an alternative approach with greater commercial viability, involving a thinning of the quantum wells to realise better uniformity and a greater overlap of electron and hole wavefunctions. Through changes to the epitaxial structure and the device design, we have produced laser diodes with a high wall-plug efficiency.

We grow the epitaxial layer structures of our lasers by MOCVD. Their production involves loading 2-inch *c*-plane free-standing GaN substrates into an MOCVD reactor and depositing *n*-type, active and *p*-type layers. We process these epiwafers into devices by using etching to form a ridge structure on the *p*-side, before adding *n*-type and *p*-type electrodes to the top and bottom of the chip (see Figure (1)). The mirrors at the ends of these edge-emitting structures are created by cleaving the wafer and then coating the bare facets with dielectric mirrors. To reduce optical absorption losses, we gave much care to the design of the optical confinement structures of the epitaxial stack. The fabrication of our lasers finishes by mounting the chip, with a junction down method, in a TO-can package that suppresses thermal resistance.

Blues beyond 50 percent

Back in 2001, we reported a key milestone for the blue laser diode: the first milliwatt output power for this device. Rapid progress came over the next few years, leading us to unveil the first watt-class laser diode in 2007. Recently, we have broken another noteworthy barrier, realising a WPE of 50 percent. For our blue lasers emitting at 455 nm, spectral width is typically 2 nm, implying that all the light energy exists in only about one-tenth of the spectral width of an LED. It is quite astonishing that half of the electrical input power is converted into laser light spanning just a 2 nm range. Note, though, that this level of efficiency is below that of the best GaAs-based and InP-based laser diodes, so we can expect further improvements in efficiency in the future.

Earlier this year we revealed an optical output of 5.90 W and a WPE of 51.6 percent from a 455 nm blue laser driven at 3 A (see Figures 2 and 3). These laser diodes have raised the bar for output power and efficiency through advances in chip design. Specifically, improved performance has come from suppressing absorption losses inside the laser diode element, increasing the carrier injection efficiency and trimming the operating voltage via resistance reduction.

An important characteristic of our blue lasers is their exceptional reliability. They have demonstrated this merit in a 30,000 hour lifetime test at the rated 3 A (see Figure 4). Thanks to this attribute, we can expect our blue laser diodes to serve in projector displays for several years or more – that's much longer than conventional lamp light sources, which need to be replaced after several thousand hours.

To reach any desired output power, we can mount a number of our blue laser diodes together in a package. Using this approach, we have produced sources with optical output powers from 20 W to 100 W.

In recent years, there has been a global shift from lamps to solid-state light sources. This trend will continue as products are replaced. At the centre of this transformation is the laser diode. There's no doubt that laser diodes will become mainstream, with the shift from lamps to lasers spreading to all markets.

Watt-class greens

Another recent triumph for us is increasing the WPE of our 525 nm green laser diode to nearly 24 percent. This laser is capable of completely covering the standard for digital cinema in the green region. To realise such success, we have combatted the challenges associated with piezoelectric polarisation, which reduces the overlap of electrons and holes and thus the radiative efficiency. Our solution is to reduce the active layer thickness. While piezoelectric polarisation still occurs, by turning to a very thin active layer thickness, we suppress the decrease of luminescence

Characterisation of our green laser diodes, which have a ridge width of 20 μm and a cavity length of 1200 μm, underline the benefits of thinner quantum wells. Our 525 nm-emitting devices deliver 1.86 W at a WPE of 23.8 percent when driven at 1.9 A, while benefitting from a low threshold current (see Figure (5)). We have also produced a direct alternative to the incumbent 532 nm laser that's based on second-harmonic generation. Driven at 1.9 A, our 532 nm laser produces an optical output of 1.64 W and a WPE of 20.2 percent (see Figure (6)). Note that our green lasers produce even higher WPEs at lower output powers. The peak WPE for our 525 nm laser is 25.9 percent, associated with a 1 A drive current; and our 532 nm laser has a maximum WPE of 21.9 percent, when delivering an optical output power of 1 W (see Figure (7)).

Our efforts will accelerate the shift to combining existing red laser diodes with new, more powerful and efficient blue and green cousins, to create compelling light sources for projectors. This will enable a new generation of projectors with a wide colour gamut. Note that the merits of higher efficiency extend beyond the trimming of electricity bills, as they simplify thermal management, which is of great importance. We are breaking new ground, as we are the only company to have commercialised watt-class, 532 nm laser diodes. They provide a light source that fully satisfies the BT.2020 high-definition standard. The higher efficiency is not just valued for projector applications as it will be an asset in other markets, including processing and industrial applications.

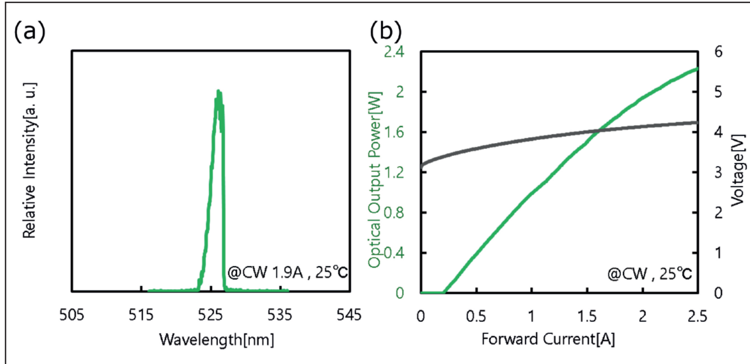


Figure 5. (a) The emission spectrum of Nichia's 525 nm green laser diodes under 1.9 A CW operation at a case temperature of 25 °C. (b) Current-light (I-L) and current-voltage (I-V) characteristics of a green laser diode under CW operation at 25 °C.

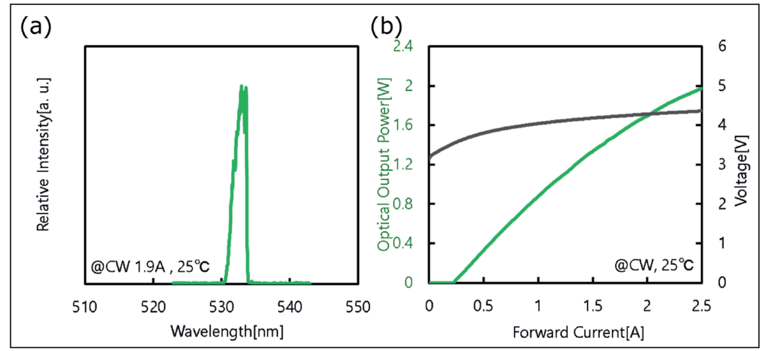


Figure 6. (a) The emission spectrum of Nichia's 532 nm green laser diodes under 1.9 A CW operation at a case temperature of 25 °C. (b) Current-light (I-L) and current-voltage (I-V) characteristics of a green laser diode under CW operation at 25 °C.

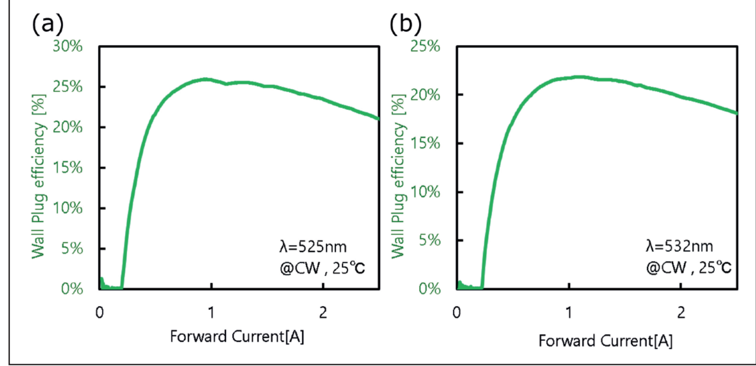


Figure 7. Current-WPE (I-WPE) characteristics of Nichia's (a) 525 nm and (b) 532 nm green laser diodes under CW operation at 25 °C.

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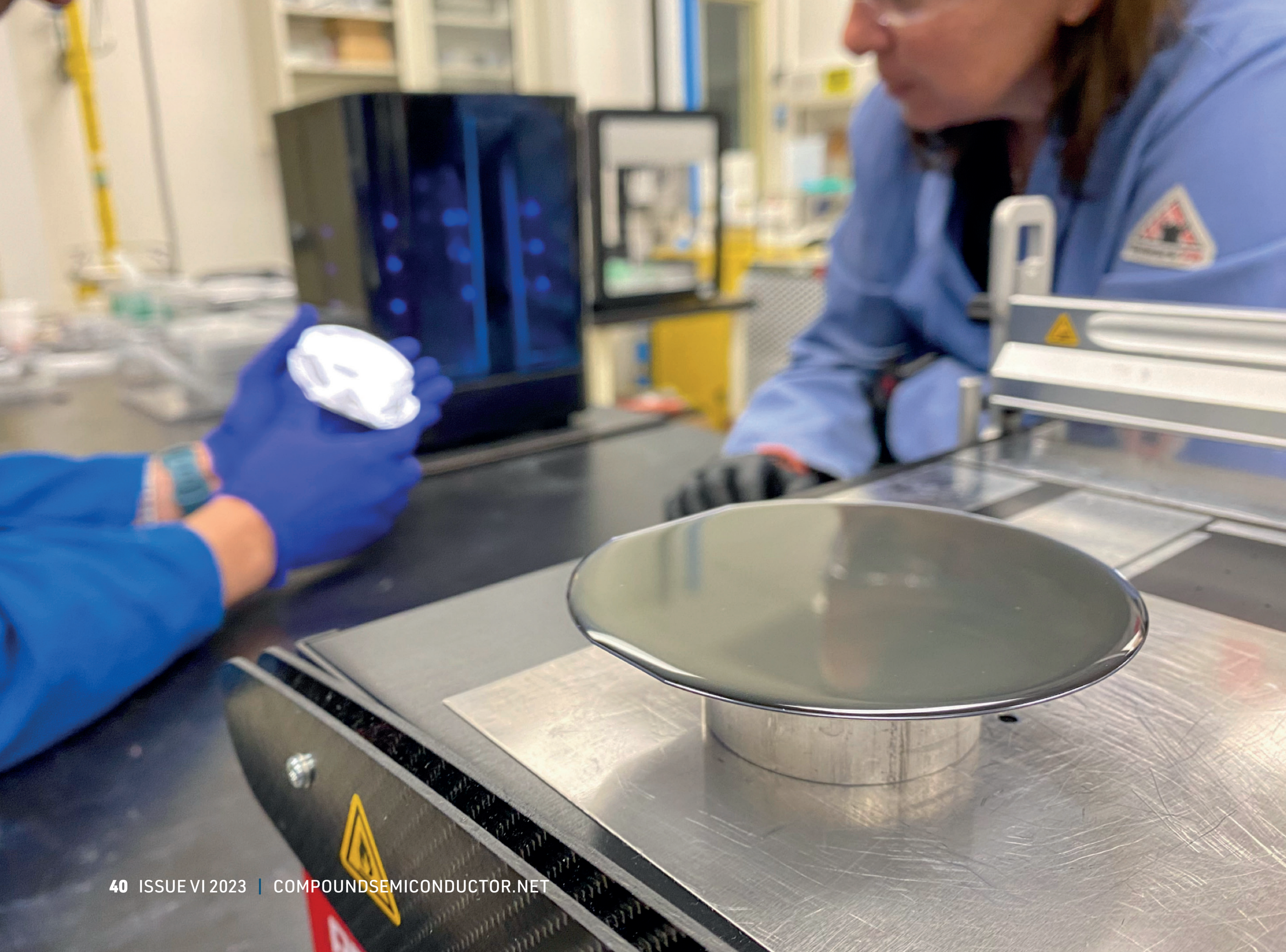
A sound approach to cutting costs

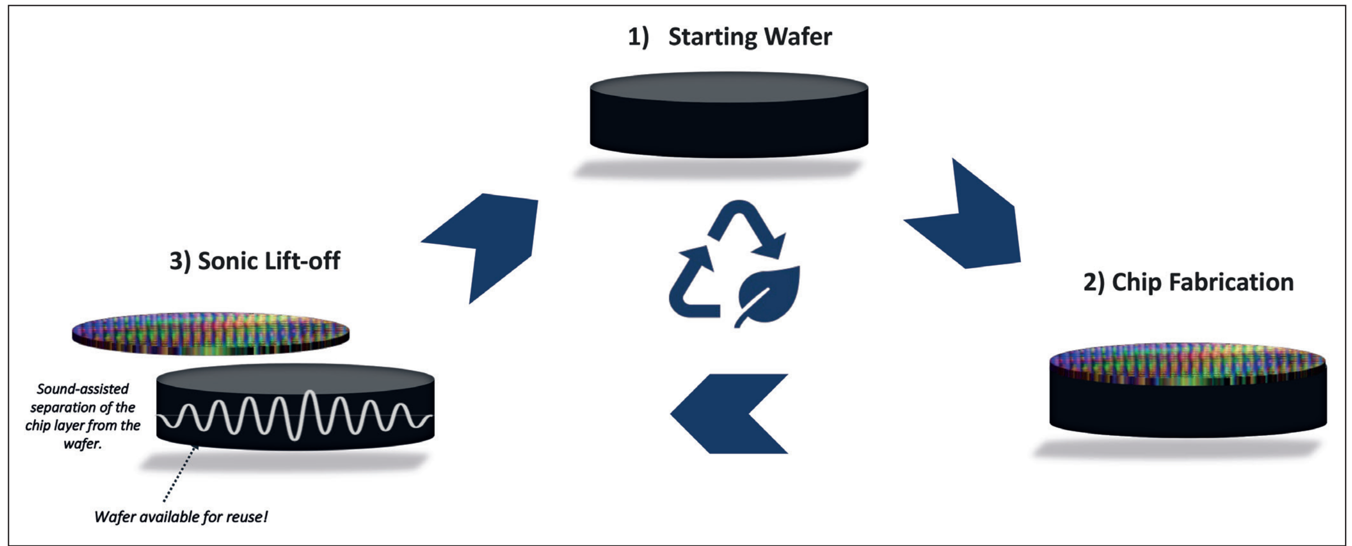
The harnessing of acoustic energy promises to enable substrate re-use during the production of wide bandgap power electronics

BY ARNO MERKLE FROM CRYSTAL SONIC

There's no doubt that compound semiconductor devices are on a long-established upward trajectory. Even as far back as the end of the twentieth century they were playing a number of crucial roles in our lives: they were a key ingredient in telecommunication networks; they were providing the optical source for the CD player; and they performed two essential roles in handsets – lighting keypads and amplifying RF signals. During the last two decades sales of these devices have continued to climb, due in part to deployment in lightbulbs and chargers. And growth is sure to continue, as revenues ramp through the electrification of transportation, the roll-out of 5G and the launch of countless satellites.

However, despite great performance advantages that have driven the success of compound





➤ Figure 1. Sonic Lift-off workflow, enabling substrate re-use for wide bandgap materials.

semiconductor devices, their potential is yet to be fully realised. Holding this back are three related constraints in the manufacturing supply chain: a large demand-supply gap, particularly for wide bandgap devices based on SiC and GaN; high cost; and waste. Let's analyse these three issues, one by one.

First, there is a large and increasing gap between the demand for wide bandgap devices and their supply. For example, the Canaccord Genuity Group estimates that the demand for SiC-based power devices, driven by thirst for the likes of electric mobility, charging stations, industrial motors and solar inverters, is leading to approximately a three-fold shortage in SiC wafer supply over the course of this decade.

Second, wide bandgap materials are costly to produce, due to the inherent difficulty required to produce high-quality wafers with limited crystalline defects. Unlike silicon, crystals of GaN and SiC cannot be grown from the melt, leading to the need for a far higher energy input and greater challenges for process control. Another factor at play is that the industrial know-how for producing such materials, while broadening somewhat, is still relatively concentrated, especially for GaN and AlN. Due to these difficulties, it's not surprising that the substrate prices for GaN, AlN and SiC are at least one or two orders of magnitude higher than those for silicon. As a result, their cost can account for about half of total device manufacturing cost – and this is not expected to appreciably change. Forecasts by PGC Consultancy indicate that wide bandgap substrates will remain the dominant manufacturing cost contributor, bottoming out at around 35-45 percent of SiC die cost in the coming decade as wafer production ramps up.

Third, waste in semiconductor manufacturing is abundant. Typically, discussions on this topic focus on either water waste and recycling strategies, or ways to limit the use of toxic chemicals, gases, and other consumables during chip manufacturing. But this strategy overlooks a more basic issue: waste of the wafer material itself. This really matters, as it's not uncommon to waste at least 95 percent of wafer material during today's conventional manufacturing process. With quite some effort, this material is literally ground into dust during two key steps in the manufacturing process. The first time this happens is during the slicing of large boules of wafer-grade crystals into wafers with a wire-saw, which is essentially a glorified bread slicer. During this step, known as 'wafering', approximately 50 percent of the material is lost to sawdust. The second step that wastes a great deal of material is the processing of wafers into chips, when they are typically thinned by mechanical back grinding. In this case, a sanding device provides 'device thinning', a step that eliminates up to another 90 percent of the substrate material, again to dust.

Over the past decade attempts to improve wafering have emerged that move beyond wire-sawing. These approaches, including those involving lasers, are capable of decreasing the waste associated with this step by around 50 percent. However, it is still challenging to reduce waste at the thinning step. While various attempts have been made, there are no lasting solutions that are suitable for producing wide bandgap bulk substrates of the highest quality.

A sound solution

At Crystal Sonic of Phoenix, AZ, we are breaking this deadlock with a novel technology that's based on the use of sound energy. With this approach we are opening the door to thin device lift-off and substrate re-use, overcoming barriers encountered by previous efforts in this domain.

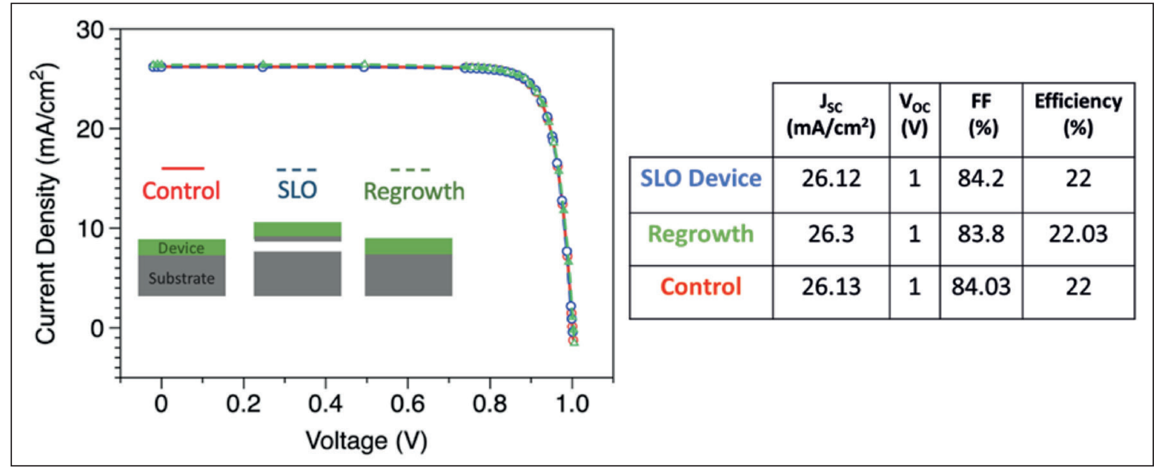
Our technology provides a pathway for simple, multiple wafer reuse that reduces the substrate cost proportionally with the number of wafer reuses. To deliver these savings, we combine a removable stressor that defines the depth of the cut with a highly tuneable acoustic source (see Figure 1 for

Figure 2. 4-inch GaAs wafers split by Sonic Lift-off, at Crystal Sonic laboratories in Phoenix, Arizona.

an illustration of how our patented technology harnesses the power of sound to separate thin devices from semiconductor substrates, thus enabling substrate re-use).

A key advantage of our approach is that a crack front is guided smoothly through a substrate at a controlled speed. This results in a chip that is ready for postprocessing, while leaving the substrate surface ready for reprocessing, with either minimal or no conditioning required. Note that we have already undertaken successful feasibility demonstrations on small diameter wafers made from silicon, GaAs, SiC, GaN and AlN.

The approach that we have developed, which we refer to as Sonic Lift-off, is an improved variation of thermal spalling – a technique that uses acoustic energy to control crack motion across a wafer. In thermal spalling, the stress that's imparted to the



	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	Efficiency (%)
SLO Device	26.12	1	84.2	22
Regrowth	26.3	1	83.8	22.03
Control	26.13	1	84.03	22

Figure 3. Current-voltgae (I-V) plots for devices grown on 2-inch GaAs (control-Red), after Sonic Lift-off (blue) and a regrowth on the remainder substrate (green). Device performance comparison between growth on a pristine substrate (red), a Sonic Lift-off device (blue) and re-growth on a re-used substrate (green). All device growth done by Rochester Institute of Technology and supported by DoE under contract number DE-EE0008973.

wafer originates from the difference between the thermal expansion coefficients of the substrate and the stressor layer upon heating or cooling. With this approach, undesirable results can come from coupling of crack initiation and crack propagation. Problems stem from the need to use far more energy to move a crack front successfully through the full diameter of a wafer, compared with that required to initiate the crack. This energy surplus directly translates into uncontrollable crack velocities and, subsequently, high values for surface roughness and the total thickness variation. And, as one would expect, this issue is accentuated when transitioning to larger diameters.

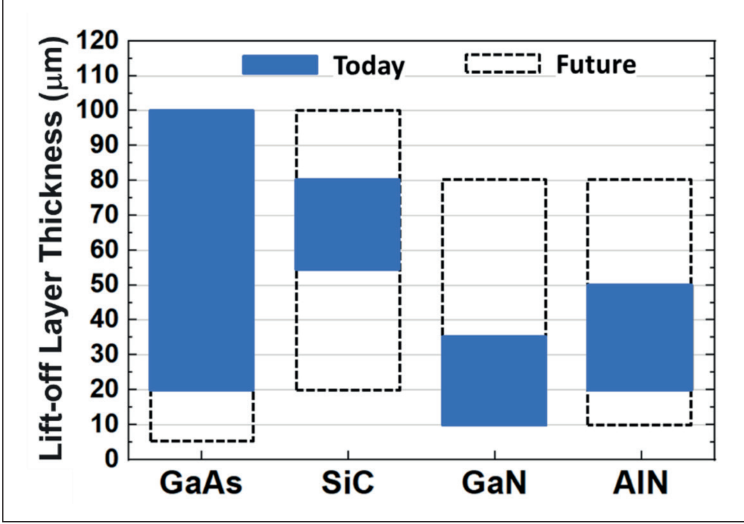
We overcome these problems with acoustics. Thanks to this modification, we successfully decouple crack initiation from crack propagation. By introducing acoustics, we enable process tuning, which in turn allows for crack velocity control that has a direct and positive impact on surface quality.

Great lift-off

Working in partnership with the National Renewable Energy Laboratory, Arizona State University, and the Rochester Institute of Technology, we have demonstrated that photovoltaic devices – they could be thought of as a proxy for any vertical optoelectronic technology – retain their performance after Sonic Lift-off. This effort, involving inverted and upright devices grown by MOCVD on (100) GaAs substrates, has determined that lift-off leads to no loss in current or voltage compared with the 'control' device.

Our investigation continued with light conditioning of the remaining substrate, followed by the growth of new devices. Results from this regrowth show that these devices have an almost identical performance to both the control and the first photovoltaic produced by Sonic Lift-off (see Figure 3). This finding offers extremely encouraging evidence that Sonic Lift-off is an optimal non-destructive technique for lifting off thin devices.

It's important to note that our technology is not just applicable to GaAs. It also has a major role to play with wide-bandgap semiconductors – such as SiC, GaN and AlN – which are projected to grow significantly in the coming years, due to increasing demand for energy-efficient and high-performance electronic devices. These materials can serve in a wide range of applications in power electronics, including electric vehicles, renewable energy systems and data centres. In addition, they can be used in high-frequency RF/microwave devices and optoelectronics, such as: RF power amplifiers for the telecommunications industry; and in UVC-LEDs, a promising source of radiation in healthcare, providing disinfection of surfaces, water, and air. The majority of these applications suffer from an even higher substrate-cost constraint than that for GaAs, so would be clear beneficiaries of substrate re-use technologies.



➤ Figure 4. Current and future expected lift-off layer thickness ranges estimated for various wide bandgap substrates. Specific thicknesses may be targeted within approximately 5 µm.

We expect our Sonic Lift-off technology to be applicable to most, if not all, single-crystal semiconductor substrates. Right now work is underway to further optimise process conditions for materials such as SiC and GaN. Development efforts are split between materials compatibility and tool upscaling. The former focuses on isolating appropriate process parameters suitable to each material type, while the latter is directed at optimising acoustic and other tool-related design elements required to extend lift-off areas to 6-inch and 8-inch wafers.

Early work on GaN and SiC has yielded promising results that are in line with our previous experience with GaAs. According to our models, there is a material dependent process window of lift-off thicknesses, in the range of approximately 10-100 µm ± 5 µm (see Figure 4). Specific ranges are in line with current limits of mechanical back grinding, and extend to thinner layers. We have found that due to the relative lack of surface damage or introduction of microcracks, our Sonic Lift-off technology is well suited to maximising substrate material utilisation by minimising lift-off layer thicknesses.

We are confident that our Sonic Lift-off technology will open the door to substrate re-use, and ultimately supply the fuel that's needed to grow the deployment of wide bandgap semiconductor devices. Success on this front will help all of us to enjoy a brighter, more powerful and efficient future.

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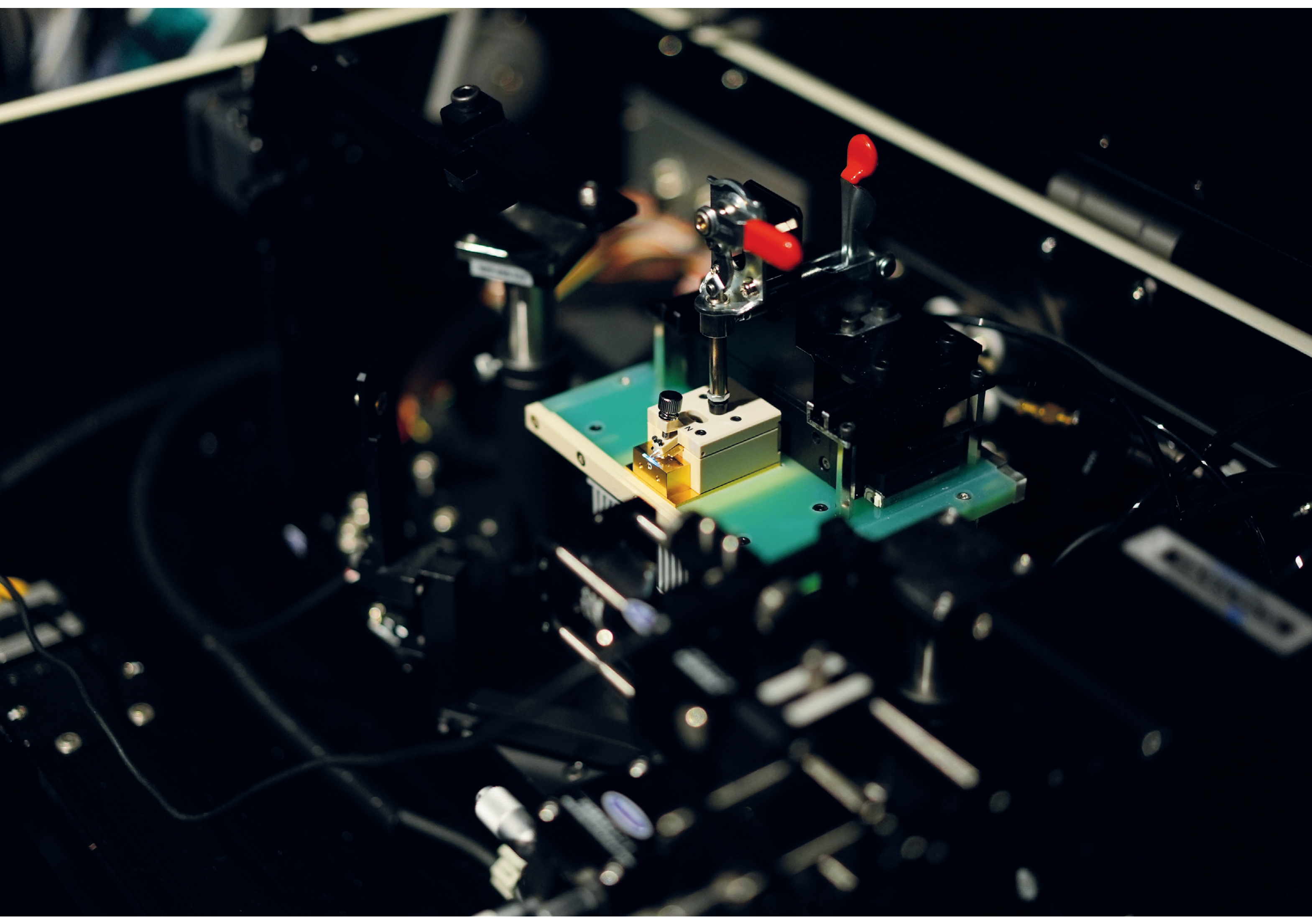


The power of pseudomorphic nitrides

Pseudomorphic AlGaN/AlN promises to enhance the performance of UVC lasers, far-UVC emitters and high-power solid-state devices

BY LEO SCHOWALTER FROM NAGOYA UNIVERSITY AND LIT THINKING AND MAKI KUSHIMOTO, ZIYI ZHANG, AKIRA YOSHIKAWA AND HIROSHI AMANO FROM NAGOYA UNIVERSITY

RECENTLY, and for good reason, our community has been showing much interest in ultrawide bandgap semiconductors. Part of their appeal is their potential to create optoelectronic devices emitting in the UVC, a spectral domain associated with wavelengths below 280 nm (see Figure 1). But in addition, this class of semiconductors is a strong candidate for creating higher performance, high-power RF devices, and for increasing the power density and performance of power devices and power switches.

Unfortunately, ultrawide bandgap semiconductors are challenging for the very reasons that make them attractive. It's the norm that very large bandgaps go hand-in-hand with very strong chemical bonds, leading to very high temperatures for crystal growth. Likewise, the large bandgaps hamper controlled doping of *p*-type and *n*-type carriers.

This is so severe that in the not so distant past, what we now call ultrawide bandgap semiconductors were listed as insulators! And even now, aside from a few special cases, it is incredibly challenging to realise reliable hole and electron conductivity in these materials.

One example of an ultrawide bandgap semiconductor is high-aluminium-content $Al_{1-x}Ga_xN$. When the aluminium content in this alloy exceeds about 50 percent – that is, when the value of *x* is less than 0.5 – its bandgap monotonically increases with aluminium concentration from about 4.4 eV to 6.1 eV, when pure AlN is reached.

Related to high-aluminium-content $Al_{1-x}Ga_xN$ is GaN, as well as the alloys of $Al_{1-x}Ga_xN$ and AlInGaN with bandgaps less than 3.5 eV. These materials have enjoyed much success, so it's natural to try and builid on what has been accomplished by progressing the capabilities of ultrawide bandgap alloys of $Al_{1-x}Ga_xN$ with values for *x* that are less than 0.5.

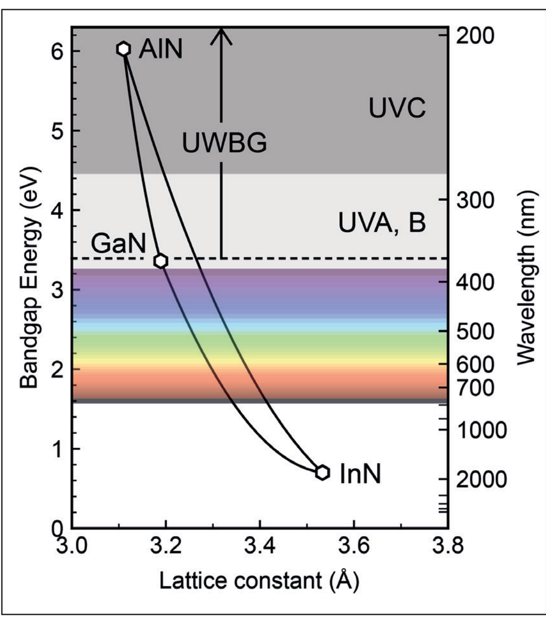
While this may sound simple, the reality is far from that, with two major obstacles blocking the path to success. One is that the epitaxial growth of high-quality, high-aluminium-content AlGaN is relatively difficult on foreign substrates. It is much easier to undertake epitaxial growth on native bulk AlN, particularly at high aluminium concentrations, but progress has been held back by the lack of high-quality substrates.

The other major issue is the difficulty in doping high-aluminium-content AlGaN. Until recently, the most common approach to doping has been the addition of silicon, to produce *n*-type material. This dopant works quite well at aluminium concentrations below 85 percent and, very recently, researchers at Georgia Tech have even shown successful *n*-type doping of AlN. However, producing *p*-type doping is much more problematic.

Breaking new ground by overcoming both these issues is our team at Nagoya University, which has been working in partnership with Asahi Kasei/ Crystal IS. Our recent demonstration of UVC laser diodes highlights that we have established a clear path past these issues that can unlock the door to allowing high-aluminium-content AlGaN to play a much bigger role in ultrawide bandgap device applications (see Figure 1).

Our work is an important milestone in the development of the UVC laser diode, a device that has been intensely pursued for more than 20 years. The commercialisation of a low-cost laser diode in the UVC will revolutionise portable, cost-effective chemical and particle detectors, medical instrumentation, and surface monitoring and machining. All these applications draw on short-wavelength high-energy photons and their very short absorption length in most materials.

However, despite the great demand for such a source that inspired numerous development efforts, the shortest wavelength laser diode developed prior to our successful demonstration of a 271 nm laser diode in October 2019 only reached down to a wavelength of 315 nm (see Figure 2).



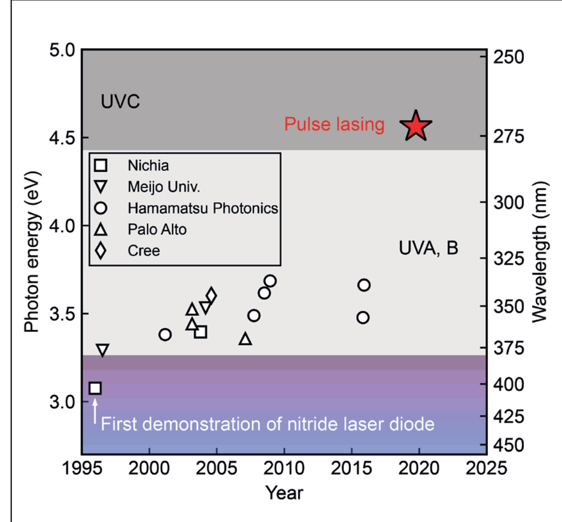
➤ Figure 1. Nagoya University, working in partnership with Asahi Kasei/Crystal IS, has demonstrated the first UVC laser diodes

There are two keys to our success. One is the availability of pseudomorphic $Al_{1-x}Ga_xN$ on high-quality AlN substrates, and the other is the use of distributed polarisation doping. With this form of doping it's possible to realise low-resistivity hole injection without the use of impurity doping in the *p*-type laser cladding layer.

What is pseudomorphic AlGaN/AlN?

Due to progress in bulk crystal growth of AlN, several companies, including Crystal IS, are now supplying substrates. This foundation for epi-growth comes from slicing material from AlN crystals with very low defect densities.

During the growth of nitride semiconductor heterostructures, one defect that arises in the epilayers is the so-called threading dislocation. High densities of this type of dislocation tend to arise during growth on foreign substrates, such as sapphire, SiC or silicon, due to lattice mismatch. As these threading dislocations degrade device performance, the nitride community has devoted



➤ Figure 2. Nagoya University, working in partnership with Asahi Kasei/ Crystal IS, has demonstrated the first UVC laser diodes.

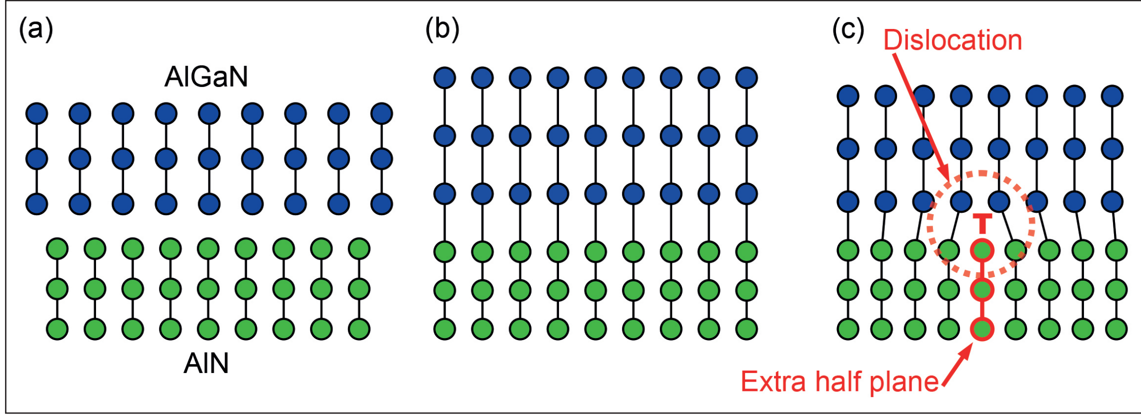


Figure 3. In high-aluminium-content AlGaN, misfit dislocations may form along the interface.

much effort to reducing their density, as well as mitigating the impact that they have on devices. But despite all this work, it still takes a great deal of care to bring the threading dislocations in high-aluminium-content AlGaN below 10^8 cm^{-2}, leading to a high cost. The good news is that 2-inch AlN substrates with threading dislocation densities of less than 10^3 cm^{-2} are now available from a couple of suppliers, and there are more producers on the horizon. When the surfaces of these substrates are properly prepared (most typically, the Al-polar c-face), AlN homoepitaxy with threading dislocation densities below 10^4 cm^{-2} are routinely produced.

Crucially, AlN substrates can also provide the foundation for AlGaN alloys with very low threading dislocation densities. Since the crystal structure of GaN, AlN and related alloys is identical, one would hope that a well-prepared surface of native AlN would act as a good template for the growth of all AlGaN alloys. Unfortunately there is a significant lattice mismatch between bulk GaN and AlN – it is as high as 2.4 percent. Thus, if GaN is grown on AlN using the *c*-face crystal surface as a template, the epitaxial GaN layer is compressively strained in the *c*-plane by 2.4 percent. This results in an enormous strain energy, increasing linearly with the thickness of the GaN layer. Eventually, this strain has to be relieved in some way.

As epitaxial growers are well aware, there are a number of mechanisms for strain relief, including forming islands and roughening the surface. However, the mechanism that is most significant for high-aluminium-content AlGaN is the formation of a misfit dislocation along the interface (see Figure 3). As shown in that figure, an edge misfit dislocation forms when a plane of atoms is skipped along the interface, leading to a reduction in the compression of the GaN epitaxial layer that fits onto the underlying AlN lattice.

At the core of the misfit dislocation is a row of atoms with dangling bonds. That's not the only concern, however, as there is an inhomogeneous strain field surrounding the misfit dislocation. Together, they result in a 'core energy' associated with each misfit dislocation and additional strain energy that arises from non-uniformity. For more than half a century it has been known that the extra energy introduced by an array of misfit dislocations can be balanced by a reduced elastic strain energy that results from the misfit array once the strained epitaxial layer exceeds a critical thickness.

If the thickness of the layer is below the critical thickness, the epitaxial film is in a lower energy state and pseudomorphically strained to exactly match the lattice parameter of the underlying substrate. For the growth of GaN on AlN, the critical thickness is only a few nanometres. Using Vegard's law, it is possible to estimate the lattice mismatch between AlGaN and AlN. This approach, involving linear interpolation, determines that for $Al_{0.6}Ga_{0.4}N$ the lattice mismatch is still almost 1 percent – and roughly speaking, the critical thickness is only increased by a factor of 2.5, far short of what's needed for most device structures.

Fortunately, the reality is better than these predictions. Back in 2009 our colleagues at Crystal IS showed that it is possible to grow a 0.5 μm-thick layer of $Al_{0.6}Ga_{0.4}N$ pseudomorphically on the *c*-face of an AlN substrate. Since then, even thicker pseudomorphic layers have been demonstrated for layers of AlGaN with a higher aluminium content.

While this was a very surprising result at the time,

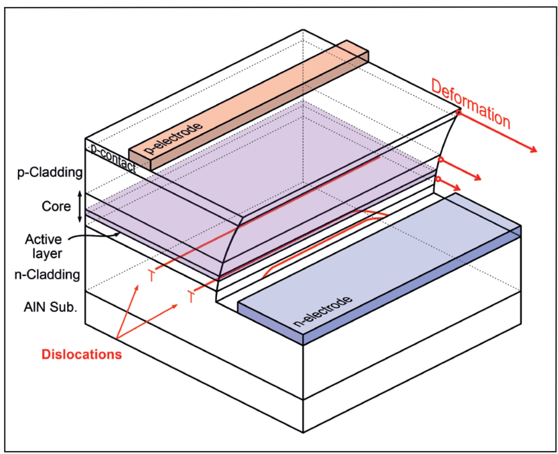


Figure 4. In this pseudomorphic UVC laser diode the top edge of the etched mesa is no longer strained while the bottom corner of the mesa remains fully strained.

it can be explained. While the strain energy in the epitaxial layer would be reduced by forming a misfit network of dislocations, there are no easy glide planes. That matters because without these glide planes, dislocations, which form on the surface of the epitaxial layer, cannot be pushed down to the AlGaN /AlN interface to relieve the strain. As a result, the strain energy in the epitaxial layer can become much, much larger than equilibrium models predict.

P-type polarisation doping

A rather special feature of nitride semiconductors is that it is possible, at least in principle, to create regions of *n*-type or *p*-type carriers by simply changing the alloy composition at an interface. Exploiting this phenomenon are the high-performance GaN HEMTs that are serving in the RF and power industries. Their success is built on efforts in the 1990s, which showed that a two-dimensional electron gas can be created at the interface between GaN and AlGaN. This gas, formed without doping with any extrinsic impurity, results from the growth in the metal-polar direction of a layer of AlGaN on top of GaN.

Note that this is a very different state of affairs from that found in cubic semiconductors. For instance, to create a two-dimensional electron gas at the interface of GaAs and AlGaAs, an *n*-type impurity dopant, typically silicon, must be introduced in the wider bandgap AlGaAs epitaxial layer.

With the nitrides, the creation of a two-dimensional electron gas at an interface is not limited to the pairing of AlGaN and GaN. This gas arises at any interface where the aluminium concentration of AlGaN is stepped up when growing on a metal-polar *c*-face substrate, so long as the defect density is not too high. What's more – as demonstrated by researchers at the University of California, Santa Barbara, back in 2002 – even grading an epitaxial layer from a lower to a higher aluminium concentration yields a distributed electron gas without extrinsic impurity doping. Note that this type of doping is referred to as distributed polarisation doping.

What about grading in the opposite direction – that is, from a high to a low aluminium concentration, when growing on a metal-polar c-face substrate? This was predicted to produce a distributed *p*-type semiconductor without the use of any extrinsic impurity doping. However, experimental demonstration did not immediately follow, although an increase in the hole concentration was observed in extrinsically doped *p*-type material, typically doped with magnesium, over what would be expected from just extrinsic doping. The barrier to forming a hole gas without extrinsic doping in this earlier work appears to have been a high density of defects. These defects trap holes, which must be saturated before the effect of distributed polarisation doping can be observed.

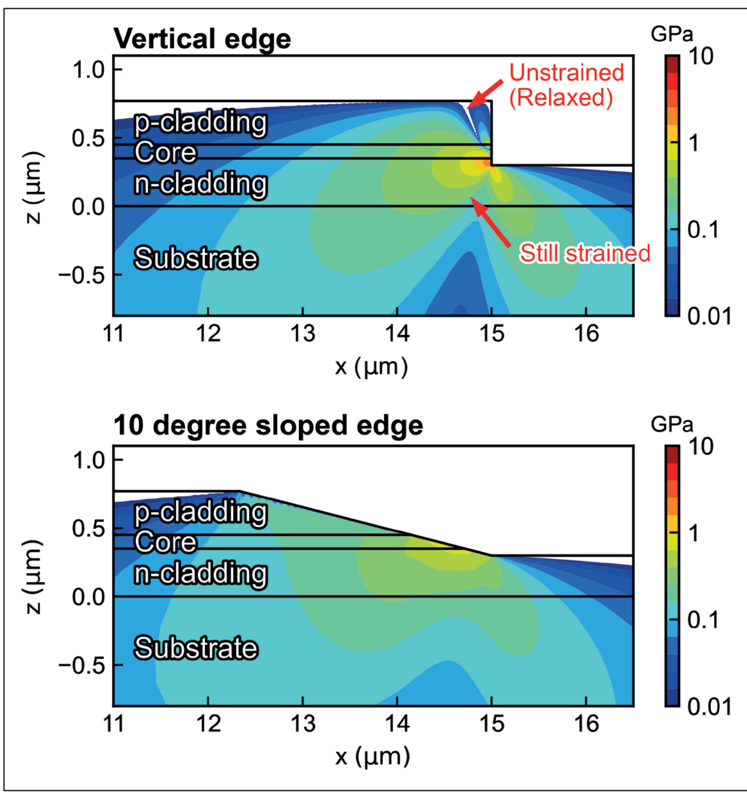


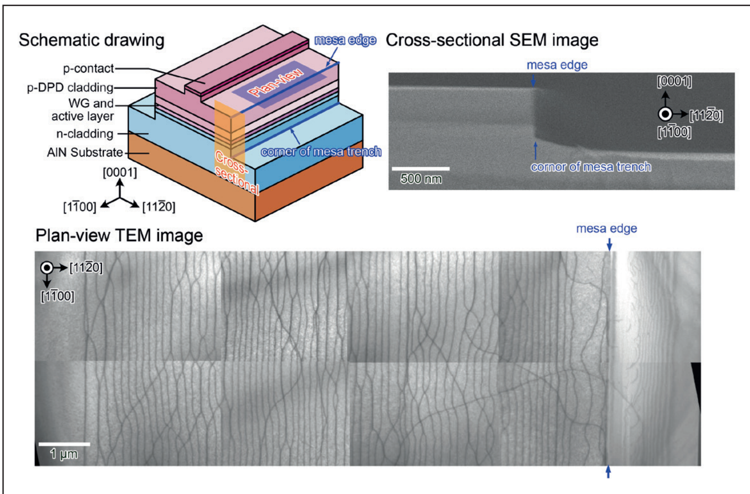
Figure 5. Severe strain inhomogeneity can generate very large shear stresses at the corner of the mesa that drive misfit dislocations in from the sides of the structures.

Against this backdrop, our demonstration of the first UVC laser diode has to be viewed as incredibly encouraging. To produce this device, we realised high hole conductivity in a distributed polarisation-doped *p*-side cladding layer. Here there is no use of extrinsic dopants, and the aluminium concentration is increased to 63 percent. Another key to this breakthrough in laser performance is the very low density of threading dislocations that results from pseudomorphic growth. We view our development of pseudomorphic AlGaN /AlN as crucial to the realisation of distributed polarisation doping in our devices.

A price to be paid

It's rare that any technology is free from downsides. In that respect, pseudomorphic epitaxial growth conforms to the norm, with its many benefits having to be weighed against a couple of problems that need addressing.

One weakness is that while the thickness of the pseudomorphic layers can be remarkably high, it is still finite. While it is possible for epitaxial growers to modify their process conditions and exceed the limits predicted by equilibrium models by at least three orders of magnitude, even then the constraints are rather limiting, especially when the gallium concentration of some of the epitaxial layers is increased. In general, there will be a roughening of the epitaxial layer once the pseudomorphic limit is exceeded. As this limit depends on the epitaxial conditions, a formal model of the limit is yet to be developed. This hampers efforts to account for the impact of the epitaxial process on the quality of the heterostructure, which influences considerations



➤ Figure 6. Dislocations injected from the mesa edge are visible by various forms of electron microscopy.

associated with device design. The other limitation is not so obvious. Producing devices involves etching into highly strained epitaxial layers, which breaks the two-dimensional symmetry. Rather than being uniformly compressed to fit onto the underlying AlN lattice, all local three-dimensional features have strains that are not uniform in the plane, with the non-uniformity giving rise to locally high stresses.

This high degree of local stress occurs at the corners of a mesa created by etching. Consider, for example, Figure 4, illustrating the etching of pseudomorphic layers of a UVC laser diode. In this particular case, the top edge of the etched mesa is no longer strained while the bottom corner of the mesa remains fully strained. This severe strain inhomogeneity is certainly cause for concern, because it generates very large shear stresses at the corner of the mesa that can drive misfit dislocations in from the sides of the structures – in this case, the mesa walls (this is illustrated in Figure 5). If these dislocations reach the active region of the device, including regions of high current density, they will degrade device performance.

We have observed this mechanical instability in the etched epitaxial layers when fabricating laser diode structures. Our device designers wanted to put the *n*- and *p*-contacts as close to one another as possible to reduce the laser's electrical resistance. This must be minimised to trim resultant Joule heating, which threatens to hike the threshold current required for lasing. To position the *n*- and *p*-contacts as close to one another as possible, we etched the vertical wall mesas and positioned our *p*-type metallisation that sits at the top of the mesa and our *n*-metallisation that's located at the bottom of the mesa as close to the mesa wall as possible. Unfortunately, the vertical mesa walls resulted in the injection of misfit dislocations into the device structure (shown schematically in Figure 4) during thermal annealing of the metal contacts. Compounding our problems, the high temperatures that we employed for annealing reduced the Peierls stress required for dislocation motion, causing AlGaN to plastically deform. The dislocations injected from the mesa edge, visible in a plane-view transmission electron microscopy image (see Figure 6), created an effective dead region near the sidewalls and forced the *p*-contacts to be moved further from the sidewalls to avoid this dislocated region. Moving the *p*-contact away from the mesa wall has pros and cons. It improves the laser performance, by reducing the threshold current and increasing device lifetime, but it also increases resistivity – this led to self-heating that prevented room-temperature CW operation, because the threshold current increased too rapidly.

Our solution is to engineer the side walls of the etched mesa to ensure a reduction in the build-up of shear stress. By introducing a sloped mesa wall, we significantly reduce the maximum shear stress present in the etched structure (see Figure 5). With this new architecture, annealing of our device does not induce misfit dislocations, and our *p*-metal can be placed much closer to the mesa edge, enabling a reduction in the resistance of the laser diode.

The key point here is that it is possible to engineer the stress in the sidewalls in a manner that avoids exceeding the minimum shear stress that will result in misfit dislocation injection, even at elevated temperatures. This is a major breakthrough for the practical application of pseudomorphic epitaxial structures.

Where next?

As well as UVC laser diodes, there are other exciting opportunities for ultrawide bandgap semiconductors, which can be used to solve several of society's problems. For instance, this class of materials can be used to develop solid-state sources of far-UVC radiation, emitting below 235 nm – this corresponds to a photon energy of more than 5.3 eV. At such short wavelengths, radiation is so strongly absorbed by protein and other organic molecules that it is unable to penetrate the skin or the surface of the eye, preventing damage to the DNA in living

Our solution is to engineer the side walls of the etched mesa to ensure a reduction in the build-up of shear stress. By introducing a sloped mesa wall, we significantly reduce the maximum shear stress present in the etched structure

cells. Meanwhile, viruses and bacterial pathogens have no such protection, and will be neutralised by relatively small exposures to such radiation. Thanks to this, it is possible to safely disinfect rooms where humans are present.

It's worth noting that gas sources of far-UVC radiation are available. However, as they are rather inefficient and expensive, far-UVC LEDs promise to be an attractive alternative, offering a much lower cost and superior robustness. Within the family of ultrawide bandgap semiconductors, the pseudomorphic high-aluminium-content AlGaN / AlN system offers potential: it has a bandgap that approaches 6.1 eV, and can form *p*-type material with distributed polarisation doping.

Additional opportunities for ultrawide bandgap semiconductors are associated with electrical grids, which need to evolve to handle future demands, resulting from distributed power generation and storage. As we shift to a world with a lower carbon footprint, we will move away from the centralised mega-power generators, which depend on fossil fuels, to many sources of relatively small, renewable power generation. These greener alternatives are often neither continuous nor 'on-demand', necessitating a hike in energy storage capability. What's required is a 'smart-grid' that handles power regulation without having to put up power substations in every square block – at least, not the large, unsightly and vulnerable kind currently used. Amongst the ultrawide bandgap semiconductors that can help in this particular endeavour is AlN, which has the potential to enable the development of power control systems that handle much higher power densities reliably, while shrinking the volume to enable a substation in a box. With any ultrawide bandgap semiconductor there have always been challenges in realising *p*-type and *n*-type carriers; but distributed polarisation doping presents an extremely useful new tool to accomplishing this for the high-power device designer, who also benefits from pseudomorphic growth, key to realising the low defect densities that ensure long-term reliable operation.

What is abundantly clear is that the potential for pseudomorphic, high-aluminium-content AlGaN/GaN is very high.

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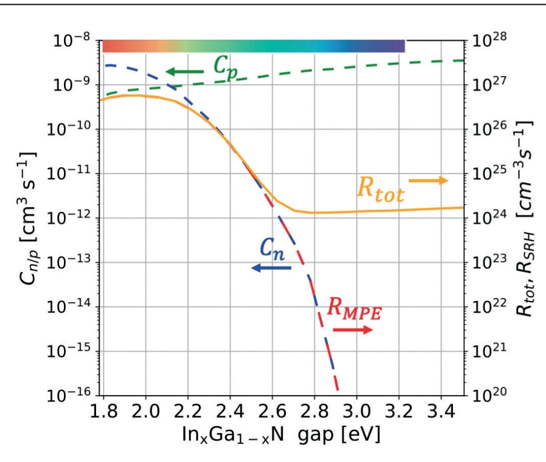
A new insight into non-radiative mechanisms

A trap-assisted process is behind defect-related losses in shorter wavelength GaN-based LEDs

ONE OF THE GREAT MYSTERIES of the LED is this: how do defects impact efficiency at ever shorter wavelengths? For many decades, it's been common knowledge that LEDs emitting in the red and green are held back by a non-radiative recombination process located at defects and involving multi-phonon emission. But as this process exponentially decreases with bandgap, what is the defect-related mechanism that matters for blue and UV emitters?

Offering an answer to this intriguing question is a team of computational scientists at the University of California, Santa Barbara, led by Chris Van de Walle. "Our newly developed methodology reveals that the trap-assisted Auger-Meitner effect can produce loss rates that are orders of magnitude greater than the mechanism based on multi-phonon emission alone, thus resolving the puzzle of how defects can cause loss in materials with wide bandgaps," remarks Van de Walle.



➤ The multi-phonon emission process, denoted R_{MPE}, cannot account for defect-related losses in short-wavelength LEDs. To explain this loss, trap-assisted Auger-Meitner processes must be included, as they are in R_{TOT}.

This new loss mechanism is a cousin of what has often been referred to as the Auger process, reported by Pierre Auger in 1923, but also described in 1922 by Lise Meitner, a female physicist with many accomplishments who is only just starting to get the recognition she deserves. Accepted by many as the cause of LED droop, the Auger-Meitner process involves an electron combining with a hole to promote a second electron or hole to a higher energy state. Meanwhile, the related trap-assisted Auger-Meitner process, which the UCSB team has just identified as playing a key role in short-wavelength LEDs, involves the localisation of an electron or hole at a defect or impurity.

As extended defects, such as threading dislocations, are present in high densities in GaN-based LEDs, they seem to have little direct impact on the internal quantum efficiency of these devices. Thus, in order to increase device efficiency, there's a need to focus on point defects, such as native defects or impurities, which are the class of defects considered by Van de Walle and his colleagues.

This team considered calcium impurities in their calculations. Calcium has been identified as an impurity in GaN LEDs grown by MBE, with the interloper introduced during wafer polishing. During growth by MBE, calcium appears to ride the surface until the deposition of the InGaN layer. However, this impurity does not seem to hamper LEDs grown by MOCVD, either because the different epitaxial conditions prevent calcium from riding the surface, or because it is caught in the InGaN layer beneath the active region.

According to the team's calculations, for a calcium impurity in GaN, defect-assisted recombination with the trap-assisted Auger-Meitner process is eleven orders of magnitude faster than recombination based on multi-phonon emission alone (see Figure).

At high current densities, the bulk Auger-Meitner process dominates, because this scales with the third power of the carrier density. But at a more modest carrier density, trap-assisted recombination is the most significant loss mechanism.

While some researchers may be tempted to add a non-radiative 'B' term to the ABC model that describes LED behaviour, Van de Walle warns that this is an over-simplification. "To fully describe nonradiative recombination at a trap, one needs to include both electron capture and hole capture. The most common scenario will be that one of these capture processes happens by trap-assisted Auger-Meitner, and the other still happens by multi-phonon emission." Consequently, both a linear and a quadratic contribution are at play.

Van de Walle and his co-workers are now building on this work, by re-examining candidate defects and impurities that may be responsible for efficiency loss in wider-bandgap materials, but were previously dismissed because rates based on multi-phonon emission alone were too low. In addition, the researchers are investigating trap-assisted Auger-Meitner processes where the trap has more than one bound state. "Again, when only multi-phonon emission is considered, such defects show low nonradiative recombination rates, and we are curious to examine whether including trap-assisted Auger-Meitner changes this," explains Van de Walle.

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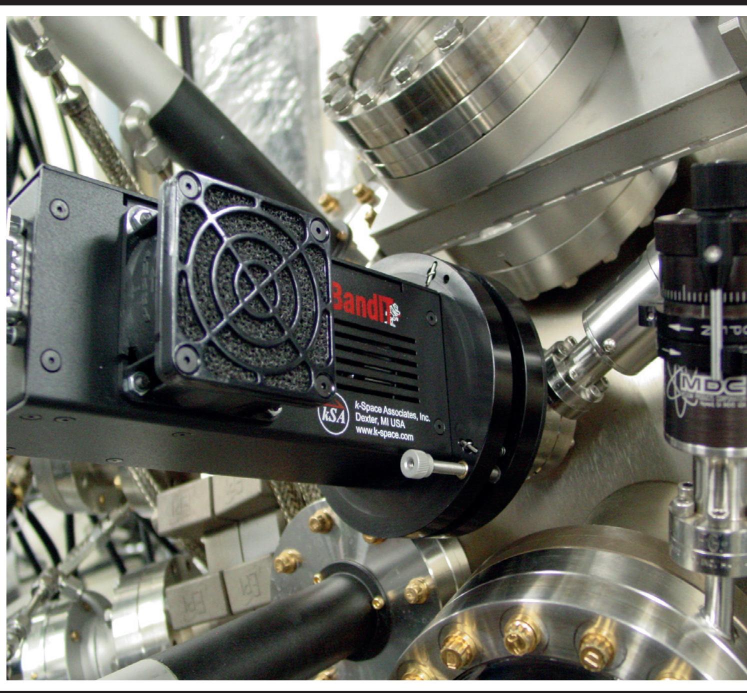

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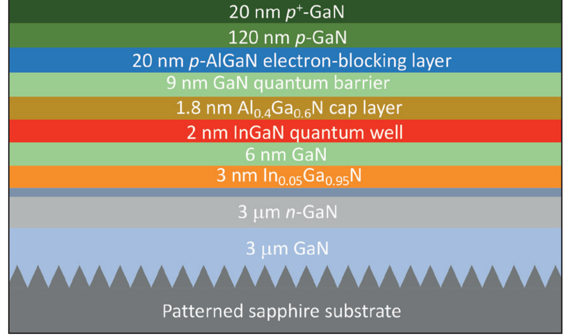
Advancing amber microLEDs

Passivated emitters with capped quantum wells set a new benchmark for the efficiency of long-wavelength GaN-based LEDs

A TEAM from the University of California, Santa Barbara, is claiming to have made major strides towards the development of ultra-small, highly-efficient red LEDs.

The researcher's InGaN-based microLEDs, which have dimensions of 10 μm by 10 μm and a peak emission wavelength of 601 nm, produce a peak external quantum efficiency of 5.5 percent and a maximum wall-plug efficiency of 3.2 percent. What's also encouraging is that the efficiency droop of these devices scales in a very similar manner to that of comparable devices with dimensions of 100 μm by 100 μm.

This work is an important step towards the development of efficient microLEDs emitting in the red, green and blue. Augmented reality and virtual reality displays need these three sources, each with dimensions below 10 μm, to produce high-quality colour images.



➤ The epistructure of InGaN microLEDs produced by UCSB.

One candidate material for the red microLED is AlInGaP. However, this alloy that is employed in traditional red LEDs has a high surface recombination velocity, causing efficiency to plummet as device dimensions shrink. While red AlInGaP LEDs with a size of around 0.1 mm^2 have an external quantum efficiency of around 20 percent, this falls to just 3 percent for variants with dimensions of 10 μm.

Much innovation has been directed at improving the performance of red-emitting GaN-based LEDs, which are far less sensitive to scaling than their AlInGaP siblings when proper sidewall passivation and treatment is employed. However, these nitride-based emitters are held back by two significant issues: a strong internal electric field, which impairs radiative recombination; and a significant lattice mismatch between the InGaN quantum wells and GaN layers, giving rise to a high density of light-quenching defects.

Novel approaches to improving the performance of red InGaN LEDs include the UCSB group's growth of the epistructure on a nano-porous GaN substrate. In 2021, they reported 6 μm microLEDs with an external quantum efficiency of 0.2 percent that incorporated this technolgy. That year, using pattern sapphire, a team from King Abdullah University of Science and Technology announced in external quantum efficiency of 0.56 percent in 47 μm red microLEDs, while partnership between researchers at the University of Grenoble-Alpes and Soitec reported an external quantum efficiency of 0.14 percent for 47 μm amber microLEDs on a relaxed pseudo-substrate. More impressive results have come from a collaboration led by National Yang Ming Chiao Tung University: last year that team reported a peak external quantum efficiency of 2.91 percent for amber LEDs, but even this is overshadowed by the latest claims from UCSB.

Their latest devices have been produced by loading patterned sapphire substrates into an MOCVD chamber and depositing an epitaxial stack featuring a 6-period active region with InGaN wells, AlGaN cap layers and GaN barriers (see figure for details). Fabrication of devices began with the deposition of a 110 nm-thick layer of ITO on these epiwafers, followed by the formation of mesas via stepper lithography and reactive-ion etching. After sidewall treatment with potassium hydroxide and the addition of a reflective dielectric stack by ion-beam deposition, atomic layer deposition of a 30 nm-thick layer of SiO_2 ensured sidewall passivation, before evaporation added metal contacts.

Measurements of these microLEDs reveal a turn-on voltage of 2.6 V at 1 A cm^{-2} and a reverse current of just a nanoamp at -3 V. According to the team, these findings imply good quality for the epitaxial materials, the etching process and the passivation.

Peak electrical efficiency at 1 A cm^{-2} is 0.83, exceeding the group's previous value for red InGaN microLEDs. This improvement is attributed to optimisation of the active region and sidewall chemical treatment. As the drive current increases from 0.5 A cm^{-2} to 80 A cm^{-2}, the peak emission shortens from 614 nm to 593 nm. This shift, stemming from screening of the electric field and band filling of localised states, is claimed to be smaller than that for most red and amber microLEDs.

The researchers believe that their work paves the way for the realisation of highly efficient red microLEDs with sizes down to 1 μm and below.

REFERENCE
➤ P. Li *et al.* Appl. Phys. Express **16** 064002 (2023)

Better FETs with bulk AlN

A native foundation equips nitride FETs with a higher drain current and lower thermal impedance

ENGINEERS from the University of South Carolina are claiming to have raised the bar for the performance of nitride FETs with an aluminium-rich AlGaN channel.

The team's devices, grown on bulk AlN, are said to break the record for the Baliga's figure-of-merit for this class of transistor. For that metric – the square of the breakdown voltage, divided by the specific on-resistance – the researcher's FETs have a value of 460 MW cm^{-2}.

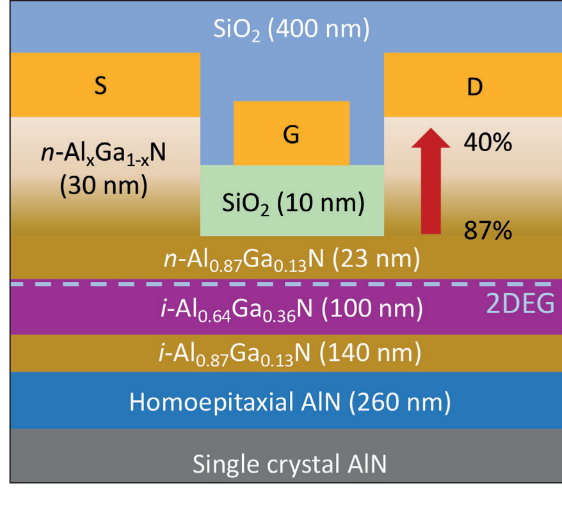
According to these engineers, their devices could improve the performance of nitride-based transistors in consumer chargers and next-generation electric vehicles. Advances have come from addressing thermal limitations with AlN substrates, which are blessed with a high thermal conductivity.

Metal-oxide-semiconductor FETs were fabricated on a 400 µm-thick single-crystal AlN substrate grown by physical vapour transport and purchased from HexaTech. Engineers loaded this substrate into a low-pressure MOCVD reactor and deposited an epitaxial stack consisting of a 260 nm-thick AlN layer, a 140 nm-thick $Al_{0.87}Ga_{0.13}N$ back-barrier, a 100 nm-thick $Al_{0.64}Ga_{0.36}N$ channel, a 23-nm thick *n*-type $Al_{0.87}Ga_{0.13}N$ barrier, and a 30 nm-thick graded AlGaN layer that's silicon-doped and designed to support the formation of ohmic contacts.

Device fabrication began by using reactive-ion etching to form a mesa. Electron-beam evaporation added source and drain contacts, which were annealed, before a second etching step removed the graded layer from the access region, prior to the introduction of a 10 nm-thick layer of SiO_2 that serves as the gate oxide. After electron-beam evaporation added gate and probe pads, devices were embedded in a 400 nm-thick SiO_2 film by plasma-enhanced CVD to relieve the surface electric field during breakdown measurements. To provide a control, identical structures were fabricated on an AlN template, formed by depositing a 3 µm-thick layer of AlN on sapphire.

Electrical measurements on FETs with a gate length of 1.8 µm, a gate-to-source distance of 1.2 µm, and a gate-to-drain distance of 2.64 µm, exhibited clear saturation and pinch-off. Peak currents of 610 mA mm^{-1} and 410 mA mm^{-1} were recorded for devices on the native substrate and template, respectively.

Thermal droop is seen in the FET with the sapphire foundation, but not in the variant built on AlN. The lack of droop is said to result from superior thermal management. Thermal impedance measurements reveal a value of 10 K mm W^{-1} for the device on AlN, and 31 K mm W^{-1} for that on sapphire.



➤ Fabricated on single-crystal AlN, the nitride FET produced at the University of South Carolina has a thermal impedance of just 10 K mm W^{-1}.

The team attributes the far lower thermal impedance, which is supported by an 8-fold higher thermal conductivity for AlN than sapphire, to the higher value for the peak current.

Due to the presence of the SiO_2 gate insulator, the team did not expect to see any difference in reverse leakage current between the two types of device. But leakage in the sapphire-based device is noticeably higher at positive gate voltages, a finding that is said to require further study.

The peak value for transconductance – the product of channel mobility and gate capacitance – hit 45 mS mm^{-1} in the FET on AlN, compared with 34 mS mm^{-1} for the variant on sapphire. As the gate capacitance is similar in both devices, the superior transconductance in the device on the native foundation is thought to be associated with an inferior mobility, which gives rise to thermal droop.

At a gate-source voltage of -30 V, device breakdown is 959 V, leading to a 'conservative' estimate for Baliga's figure-of-merit of 460 MW cm^{-2}. It is argued that because the annealed contacts are unlikely to produce an isotropic in-plane two-dimensional electron gas, a reasonable upper bound for the figure of merit is more than 750 MW cm^{-2} – that's claimed to be ten times higher than other results for FETs on AlN, and represents the state-of-the-art.

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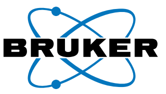

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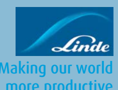

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