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VOLUME 30 ISSUE VI 2024
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
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INSIDE
News, Analysis, Features, Editorial View, Research Review and much more

All GaN power integration
Bipolar transport overcomes the inherent barriers of GaN *p*-FETs to pave the way to higher current densities

One tipping point at a time
The growth of GaN is inevitable as it displaces the silicon MOSFET in one application after another

GaN switches and CMOS drivers
Monolithic integration of GaN and silicon CMOS on 300 mm wafers will support power delivery in tomorrow's networks

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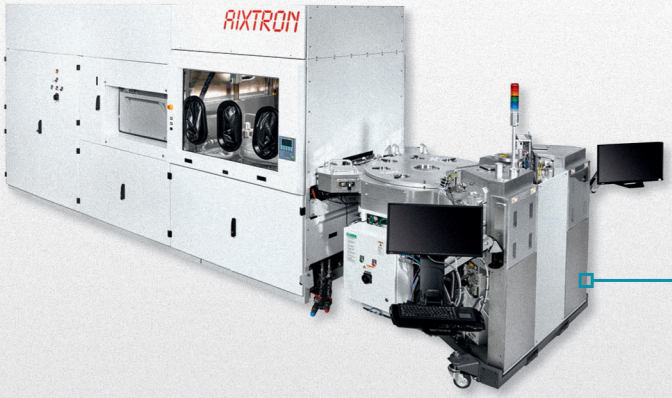

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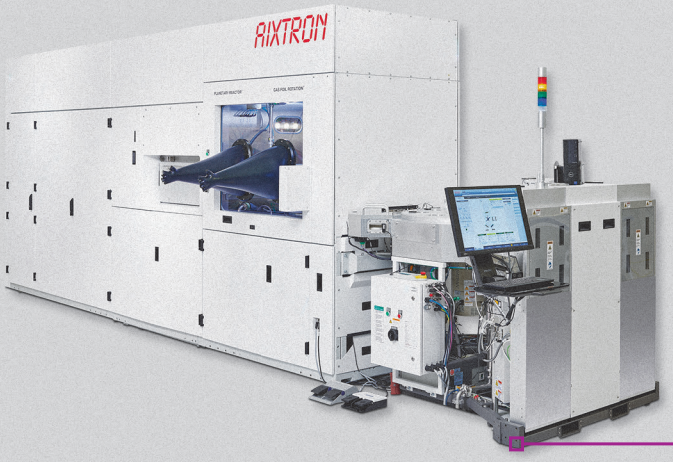

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VIEWPOINT

By Richard Stevenson, Editor

The optimal sweet spot

One of the questions that continues to pop up within our industry is this: What is the most appropriate level of vertical integration?

Throughout the late 1990s and the early 2000s, when production of GaAs-based transistors for mobile phones attracted a great deal of attention, a well-publicised debate centred on whether to outsource the epitaxial process. Beyond question, however, was the production of boules and substrates, which would be carried out by a company focusing on crystal growth.

That's not the case with the material of the moment, SiC. Within the big five – that's Wolfspeed, STMicroelectronics, Onsemi, Infineon and Rohm – the extent of vertical integration is expanding, beginning in some cases with the production of boules from powders and concluding with the shipping of packaged devices.

However, while this *modus operandi* makes much sense for companies that can invest hundreds of millions of dollars in their infrastructure, smaller firms need to identify a different sweet spot for their optimal operation within the SiC industry.

That includes SMC Diode Solutions, an American-owned company that has just opened a second fab in Nanjing, China. This chipmaker cut its teeth by producing silicon devices for makers of power supplies, and expanded its portfolio with SiC diodes in 2019, followed more recently by a range of MOSFETs.

Discussing the opening of this new 300,000 ft^2 fab that's created 300 jobs, company CEO and chairwomen Yunji Corcoran told *Compound Semiconductor* that when it comes to SiC, SMC would continue to focus on what it does best – making power devices from semiconductor epiwafers (see p. 14).

While this approach has much going for it, the downside is that there is a need to work within a supply chain, and possibly deal with the consequences of delays outside of SMC's control.

For the production of SiC Schottky barrier diodes, SMC is partnering with local producers. Corcoran says that the quality of the material that they are receiving is 'pretty good'.

To produce MOSFETs, a more complex structure, SMC sources its epiwafers from further afield. However, drawing on its internal analysis of defects in SiC, Corocan believes that local suppliers are improving, which is good news for both SMC and the global SiC industry.

The efforts of SMC show that there is space for plenty of smaller players in the SiC industry. Their efforts help to strengthen supply chains and increase the availability and deployment of this compelling class of power electronics.

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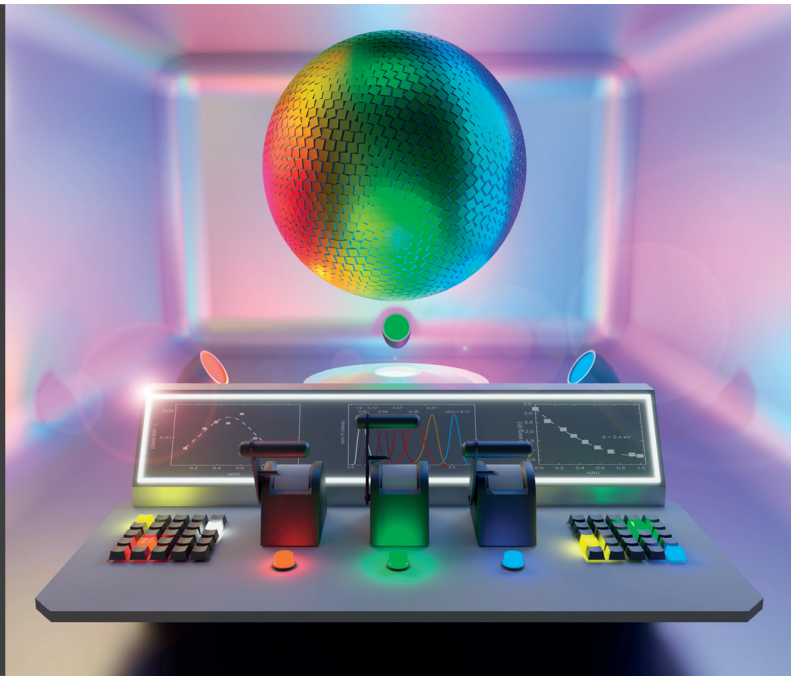

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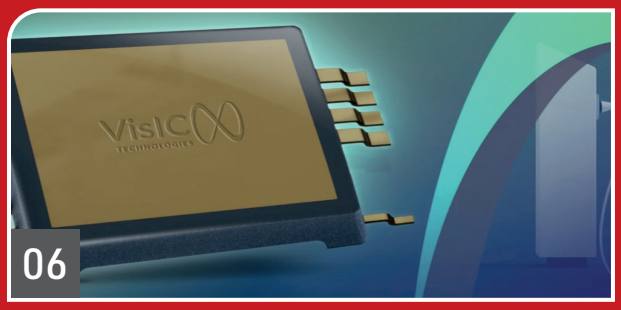

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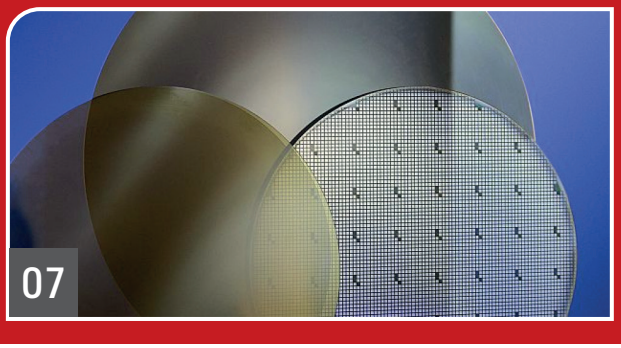
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Nokia to acquire Infinera for $2.3 billion

Creates global optical business with increased in-house capabilities and vertical integration

NOKIA will acquire the optical networking and chip company Infinera for $2.3 billion.

Nokia and Infinera see a significant opportunity in merging to improve scale and profitability. The transaction also aligns strongly with Nokia's strategy to strengthen the company's technology leadership in optical and increase exposure to webscale customers, the fastest growing segment of the market.

The combined business will have significant in-house capabilities, including an expanded digital signal processor development team, expertise across silicon photonics and InP-based semiconductor material sciences, and deeper competency in photonic integrated circuit (PIC) technology.

Pekka Lundmark, president and CEO of Nokia, said: "In 2021 we increased our organic investment in optical networks with a view to improving our competitiveness. That decision has paid off and has delivered improved customer recognition, strong sales growth and increased profitability. We believe now is the right time to take a compelling inorganic step to further expand Nokia's scale in optical networks. The combined businesses have a strong strategic fit given their highly complementary customer, geographic and technology profiles. With the opportunity to deliver over 10 percent comparable earnings-per-share accretion, we believe this will create significant value for shareholders."

David Heard, CEO of Infinera, said: "We are really excited about the value this combination will bring to our global customers. We believe Nokia is an excellent partner and together we will have greater scale and deeper resources to set the pace of innovation and address rapidly changing customer needs at a time when optics are more important than ever – across telecom networks, inter-data centre applications, and now inside the data centre."

Heard added: "This combination will further leverage our vertically integrated optical semiconductor technologies. Furthermore, our stakeholders will have the opportunity to participate in the upside of a global leader in optical networking solutions."

VisIC, Heraeus and Pink collaborate on GaN EV module

GaN COMPANY VisIC Technologies has partnered with materials company Heraeus Electronics, and sintering equipment firm Pink, to develop an advanced power module using D3GaN technology.

This combination of VisIC's D3GaN technology with Heraeus' sintering paste and Pink's silver and copper sintering process and sintering equipment is claimed to set a new benchmark for power module performance in the EV market. The partners expect it to drive the adoption of GaN technology in this field.

The module – based on a Si_3N_4 ceramic substrate, an innovative silver sintering process and advanced top side interconnects – is claimed to deliver high reliability and performance for battery electric vehicles (BEVs).

The use of a Si_3N_4 metal ceramic substrate is a key innovation. Si_3N_4 is known for its high thermal conductivity, mechanical strength, and reliability under high-temperature conditions.

The adoption of the silver sintering process by Pink enhances the thermal and electrical conductivity of the module. Silver sintering is a low-temperature bonding process that creates robust and reliable connections between components, improving the module's overall durability and efficiency. This process is said to be critical for the high reliability required in EV powertrains, where consistent performance is non-negotiable.

The resulting power module is designed to meet the stringent reliability and performance standards of the EV industry. It can deliver the high-power density of over 500 A_{rms}/650 V and the efficiency needed for modern BEVs, while also offering long-term reliability and durability at a cost point near silicon devices.

Tamara Baksht, CEO of VisIC, stated: "We are thrilled to work with the leading manufacturer of sintering processes of Heraeus Electronics and Pink and adapt their experience into GaN-based power modules to develop the next generation of power module for high-volume automotive inverter applications."

Andrea Pink, CEO of Pink, remarked: "We are excited to work with such a future driven company as VisIC, together with our long-term partner Heraeus Electronics, supporting the newest product innovation for GaN applications."

Heraeus Electronics Michael Jörger, EVP Head of Business Line Power Electronic Materials, added: "With our materials, application know-how and engineering services we are glad to work with our partners on speeding up the innovative approach of highly efficient GaN modules for automotive applications."

Nexperia to invest $200 million in Hamburg site

Expansion will focus on the next generation of wide bandgap semiconductors SiC and GaN

SEMICONDUCTOR manufacturer Nexperia will invest $200 million to develop the next generation of wide bandgap (WBG) semiconductors, SiC and GaN, and to establish production infrastructure at its Hamburg site in Germany.

At the same time, wafer fab capacity for silicon diodes and transistors will be increased. The investments are jointly announced with Hamburg's Minister for Economic Affairs, Melanie Leonhard, on the occasion of the 100-year anniversary of the production site.

"This investment strengthens our position as a leading supplier of energy-efficient semiconductors and enables us to utilise available electrical energy more responsibly," comments Achim Kempe, COO and managing director at Nexperia Germany.

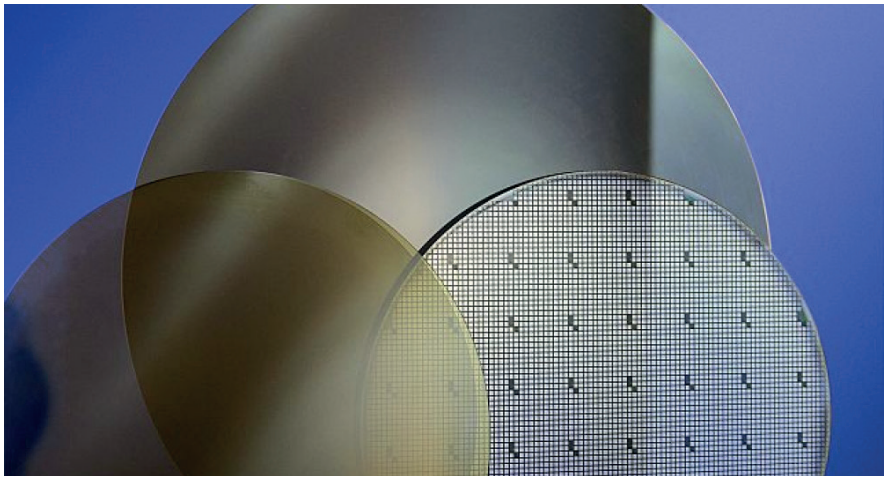
"In the future, our Hamburg fab will cover the complete range of WBG semiconductors, while still being the largest factory for small signal diodes and transistors. We remain committed to our strategy of producing high-quality, cost-efficient semiconductors for standard applications and power-intensive applications, while addressing one of the greatest challenges of our generation: meeting the growing demand for energy, while reducing the environmental footprint."

First production lines for high-voltage GaN D-Mode transistors and SiC diodes started in June 2024. The next milestone will be modern and cost-efficient 200 mm production lines for SiC MOSFETs and low-voltage GaN HEMTs. These will be established at the Hamburg factory over the next two years.

At the same time, the investment will help to further automate the existing infrastructure at the Hamburg site and expand silicon production capacity by systematically converting to 200 mm wafers. Following the expansion of the clean room areas, new R&D laboratories are being built to continue to ensure a seamless transition from research to production in the future.

"The planned investment enables us to bring WBG chip design and production to Hamburg. However, SiC and GaN are by no means new territory for Nexperia. GaN FETs have been part of our portfolio since 2019, and in 2023 we expanded our range of products to include SiC diodes and SiC MOSFETs, the latter in collaboration with Mitsubishi Electric," said Stefan Tilger, CFO and managing director at Nexperia Germany

Tilger dded: "Nexperia is one of the few suppliers to offer a comprehensive range of semiconductor technologies, including silicon, SiC, and GaN in both E-mode and D-mode. This means, we offer our customers a one-stop shop for all their semiconductor needs."



Infineon steps up battle with Innoscience

GERMAN chip maker Infineon has expanded its GaN patent battle with China's Innoscience Technology, adding three patents to infringement allegations.

The amended complaint (filed in the US District Court for the Northern District of California) alleges that as many as 88 of Innoscience's GaN-based chips infringe Infineon patents. These include US Patent numbers 8,686,562; 9,070,755; and 8,264,003.

Earlier this year, Infineon Technologies Austria sued Innoscience alleging that 30 of its products infringed US Patent No. 9,899,481. A subsequent injunction stopped Innoscience from showing its GaN devices at last month's PCIM trade exhibition, held in Nuremberg, Germany, June 11th-13th.

Innoscience has since challenged both the validity of the original patent and the injunction, saying it only applies to the tradeshow.

Meanwhile, EPC is involved in a US court case with Innoscience about the validity of another GaN patent, '294, which EPC describes as its foundational patent.

Onsemi takes next step in SiC innovation

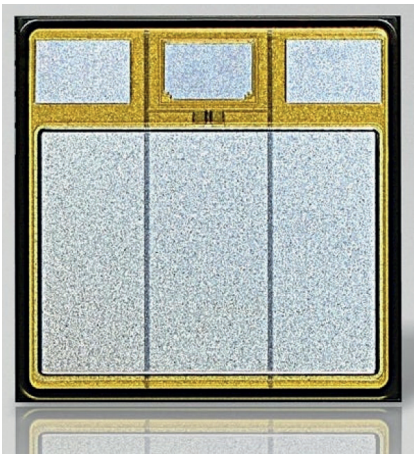
Introduces latest generation EliteSiC M3e MOSFETs

ONSEMI has introduced its latest generation SiC technology platform, EliteSiC M3e MOSFETs. The company also disclosed plans to release multiple additional generations through 2030.

According to Onsemi, the EliteSiC M3e MOSFETs achieve a significant reduction in both conduction and switching losses. Compared with previous generations, the platform can reduce conduction losses by 30 percent and turn-off losses by up to 50 percent.

The EliteSiC M3e MOSFETs are also claimed to offer the industry's lowest specific on-resistance with short circuit capability, which is critical for the traction inverter market that dominates SiC volume.

Packaged in Onsemi's discrete and power modules, the 1200V M3e die delivers substantially more phase current than previous EliteSiC technology, resulting in approximately 20 percent more output power in the same traction inverter housing.



Conversely, a fixed power level can now be designed with 20 percent less SiC content, saving costs while enabling the design of smaller, lighter and more reliable systems.

Onsemi says that with each new generation of SiC, cell structures will be optimised to efficiently push more current through a smaller area, increasing power density.

Moreover the company says it can develop multiple generations in parallel and accelerate its roadmap to bring several new EliteSiC products to market at an accelerated pace through 2030.

"We are applying our decades of experience in power semiconductors to push the boundaries of speed and innovation in our engineering and manufacturing capabilities to meet the rising global energy demands," said Mrinal Das, senior director of technical marketing, Power Solutions Group, Onsemi.

"There is a huge technical interdependency between the materials, device and package in SiC," added Das. "Having full ownership over these key aspects allows us to have control over the design and manufacturing process and bring new generations to market much faster."

Onsemi provides gate drivers, DC-DC converters, e-Fuses and more to pair with the EliteSiC M3e platform. The EliteSiC M3e MOSFET in the industry-standard TO-247-4L package is now sampling.

GlobalFoundries acquires Tagore GaN IP

GLOBALFOUNDRIES has acquired Tagore Technology's proprietary GaN IP portfolio, a high-power density solution designed to push the boundaries of efficiency and performance in a wide range of power applications in automotive, internet of things (IoT) and AI data centres.

As a part of the acquisition, a team of experienced engineers from Tagore, dedicated to the development of GaN technology, will be joining GF.

"We are committed to being the foundation of our customers' power applications today and for decades to come," said Niels Anderskouv, chief business officer at GF. "With this acquisition, GF takes another step toward accelerating the availability of GaN and empowering our customers to build the next generation of power management solutions that will reshape the future of mobility, connectivity and intelligence."

Amitava Das, co-founder and chief operating officer of Tagore Technology, added: "The accelerating demand for more power efficient semiconductors is dramatically increasing, and Tagore has been at the forefront of developing disruptive solutions using GaN technology for a wide range of power devices. The team and I are excited to join GlobalFoundries to increase our focus on market-leading IP that will help address power design challenges and support the continued evolution of automotive, industrial and AI datacenter power delivery systems."

In February 2024, GF was awarded $1.5 billion in direct funding under the US CHIPS and Science Act, part of that investment is targeted towards enabling the high-volume manufacturing of critical technologies including GaN to securely produce more essential chips.

Combining this manufacturing capacity with the technical know-how of the Tagore team, GF hopes to transform AI system efficiency, especially in edge or IoT devices, where reduced power consumption is critical.

Russian venture targets SiC power

Element and St. Petersburg Electrotechnical University form joint power chip company

RUSSIAN microelectronics company PJSC Element and St. Petersburg Electrotechnical University LETI (ETU LETI) have formed a joint venture called Letiel LLC, according to a story on Interfax, a news agency covering Russia.

"We plan to actively develop the area of high-tech power semiconductor devices and in future take leading positions among global manufacturers of SiC devices," Element president Ilya Ivantsov told Interfax.

"The objective of the joint venture with LETI will be to develop and research technologies to produce SiC devices, on the basis of which we will be able to build a modern and competitive power electronics product and technology line for various sectors of industry," Ivantsov said.

The new company will do research and development on SiC-based power devices, which are used in the production of modern electric vehicles, aircraft navigation systems and other sectors.

The venture, which is 51 percent owned by Element and 49 percent by LETI, also plans to study and design photonic integrated circuits. These components are used in equipment for cellular networks, satellite systems and radio location.

"Mass production of solutions in the area of the electronic component base for power electronics and photonic integrated circuits will be rolled out at the facilities of Element Group's new plant in Zelenograd," the company said.

The partners have not specified how much they are investing in the venture, which is headed by Element technology development director Konstantin Okunev.

Element was formed in 2019 with 19 microelectronics design, development and manufacturing assets belonging to investment group Sistema PJSFC and state corporation Rostec. Element's key portfolio companies are chip factory Mikron and microchip, molecular electronics research institute NIIME and electronics research institute NIIET. The group now includes about 30 enterprises.

Over £1 million for IQE to commercialise ultraRAM

IQE to develop capability for growth of gallium antimonide and aluminium antimonide in Innovate UK project

AN INNOVATE UK project worth £1.1 milion has been awarded to the Lancaster University spinout firm Quinas, IQE and the universities of Lancaster and Cardiff.

Quinas will coordinate the project, which is the first step towards volume production of the universal computer memory ultraRAM invented by Lancaster University academic Manus Hayne.

UltraRAM, which exploits quantum resonant tunnelling, combines the non-volatility of a data storage memory, like flash, with the speed, energy-efficiency, and endurance of a working memory, like DRAM.

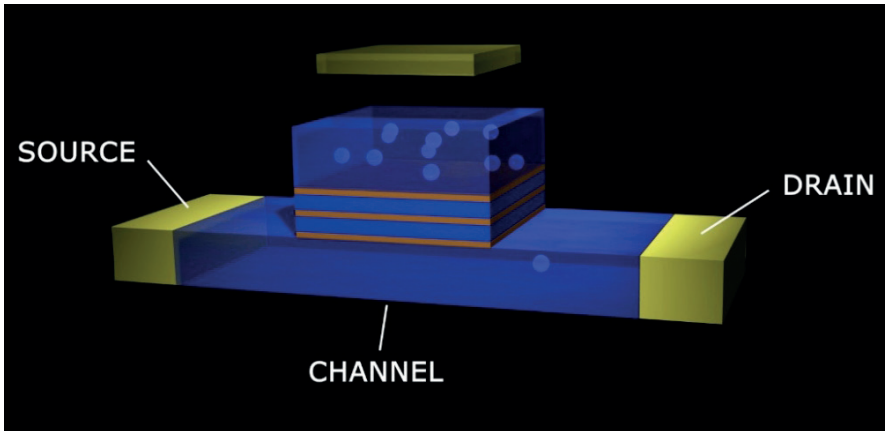
Most of the funding for the one-year project will be spent at IQE, which will scale up the manufacture of compound semiconductor layers from Lancaster University to an industrial process at the Cardiff-based firm. This will involve IQE developing advanced capability for growth of GaSb and AlSb for the first time.

The project follows significant investment to boost the UK semiconductor industry and the establishment of the world's first compound semiconductor cluster in South Wales.

Manus Hayne, who is the Lancaster team lead, co-founder and chief scientific officer at Quinas, said: "We are delighted that Innovate UK is supporting this ambitious project, and that IQE has committed to developing the first part of ultraRAM mass production."

It is estimated that the global memory chip market will be worth about $320 billion by 2030, but the UK currently has no stake in it.

Hayne said: "UltraRAM represents a tremendous economic opportunity for the UK, and the efficiencies it could bring to computing at all scales has the potential for huge energy savings and carbon emission reduction."



Jessica Wenmouth, Lancaster University's head of research commercialisation said: "I am delighted to support our spinout Quinas on its journey to scale this Lancaster-led innovation to an industrial process suitable for a semiconductor foundry 'fab,' thereby generating impact from research through commercialisation.

Wenmouth added: "This project not only aligns with Lancaster University's strategy to foster impactful research and innovation but also demonstrates the effective utilisation of strategic grant funding alongside private equity investment. Such collaborations are crucial for bringing new products to market and driving significant investment into the UK for emerging technologies, enhancing our national and global standing in cutting-edge fields."

The goal of the one-year project to industrialise the process involves scaling up ultraRAM wafer diameters from 75 mm at Lancaster to 150 mm at IQE. This will be achieved by MOCVD rather than MBE, which is typically used at universities.

The goal of the one-year project to industrialise the process involves scaling up ultraRAM wafer diameters from 75 mm at Lancaster to 150 mm at IQE. This will be achieved by MOCVD rather than MBE, which is typically used at universities.

Hayne said: "Lancaster will do some initial MBE as a control/template for the industrial growth. Our key role will be to characterise the antimonide material grown at IQE, and once sufficient quality is confirmed, we will fabricate and test ultraRAM on small areas of the wafers from IQE."

"In parallel with this, Lancaster will continue to work on ultraRAM scaling, by reducing the size of individual devices ('Moore's law') and making larger and larger arrays. Once devices are small enough and arrays are large enough, the following stage will be to demonstrate fabrication on a complete 8-inch wafer, and then to translate the process to an industrial one, suitable for a semiconductor foundry 'fab'."

VueReal and RiTdisplay forge microLED partnership

Collaboration aims to accelerate the adoption of microLED displays into consumer markets and augmented reality

VUEREAL, the Canadian company behind MicroSolid Printing technology, has announced a partnership with Taiwanese emissive display firm RiTdisplay Corporation.

The companies have already worked together on automotive display and interior/exterior lighting systems.

Now they are expanding into consumer markets and augmented reality, using RiTdisplay's backplane process and VueReal's MicroSolid Printing platform, which enables the transfer of microLEDs.

"VueReal's technology is revolutionising the microLED space," said Reza Chaji, CEO of VueReal. "Our collaboration with RiTdisplay will not only accelerate the adoption of microLED displays, but also deliver unmatched performance and value to our customers, setting new industry standards."

"RiTdisplay is thrilled to partner with VueReal," said Robert Chen, general manager of RiTdisplay. "This collaboration allows us to combine our extensive expertise in emissive display production with VueReal's groundbreaking MicroSolid Printing technology."

Chen added: "Together, we are uniquely positioned to deliver cutting-edge displays that not only meet but exceed the evolving needs of our customers, offering innovative and commercially viable solutions that will redefine the display market."

This announcement follows VueReal recent plans to double its manufacturing space and introduce a new production line capable of producing displays.

CSconnected: Maintaining momentum

Under leadership of its new managing director CSconnected will continue to focus on realising a high level of visibility and maintaining close relationships, while developing skills and strengthening supply chains

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

ANYONE TAKING OVER the leadership of any organisation will be tempted to exert their new authority by announcing big and bold plans. But if the current direction of travel is working well, there's a strong argument for simply keeping going, while looking to make small and meaningful changes.

The latter approach is the one being adopted by Howard Rupprecht, the new managing director of CSconnected, a not-for-profit focusing on strengthening the reach and capabilities of the world's first compound semiconductor cluster, located in south Wales, UK.

"We're really building on a strong foundation," enthuses Rupprecht, who applauds all those that work at CSconnected for raising this cluster's international profile and visibility.

According to Rupprecht, his organisation is already incredibly well connected to many people and organisations, both in the compound semiconductor industry and in south Wales. "Our primary goal is to maintain that level of visibility and these relationships."

While focusing on those tasks, Rupprecht and his colleagues are looking to assist in developing skills and strengthening supply chains.

Skills development has been a part of CSconnected's mission for many years. Since 2017, it has been leading an educational group to co-ordinate activities and content. Now the not-for-profit is stepping up its efforts on this front, thanks to winning funding specifically earmarked for skills development from the Cardiff Capital Region.

When it comes to strengthening supply chains, the focus is on specialty components and services.

"We have multiple businesses using many, many local suppliers," remarks Rupprecht, adding: "We have secured funding to help local suppliers increase their business with the cluster companies through grants that help to increase their capacity or capabilities."

A broad background

Trained as mechanical engineer in the 1980s, Rupprecht has accumulated a broad range of expertise over his career. He views this diversity as a key asset for running a small organisation, such as CSconnected, that works with a variety of stakeholders operating in different sectors.

For more than the last 20 years, Rupprecht has held senior management roles in tech companies. Over those decades he has experienced diversity in technology, ranging from photonics to MEMS, compound semiconductors and PCB assembly, as well as the nature of the role – at times Rupprecht has led sales, product marketing, business development, operations and business management. However, while he sees this range of skills as important, he puts even more value on having experience in working in both the public and private sector.

To ensure a smooth transition in the leadership of CSconnected, Rupprecht, who joined this not-for-profit in January, and has spent the last few months working closely with its founder, Chris Meadows.

Motivation for parting company with his former employer, Rockley Photonics, has come from a desire to grow the entire industry and support the local community. "It feels like I'm waving the flag both for the region and the industry," reasons Rupprecht.

Valuing Vishay

In any industry, uncertainty impedes progress. This issue has hampered the cluster over the last few years, with

➤ Howard Rupprecht, recently appointed as the managing director at CSconnected, has held many senior management positions within the technology sector. Prior to joining CSconnected, Rupprecht held the role of senior director of operations strategy at Rockley Photonics.

differing decisions surrounding the ownership of a jewel in the crown, the 200 mm fab in Newport. This facility, built by Inmos in 1980 and previously owned by several multi-national chipmakers, including Infineon, went into the hands of Nexperia in summer 2021. This takeover by a firm with a Chinese parent company initially had the backing of the British government, before it launched an enquiry and eventually reversed its decision, creating almost three years of disruption and uncertainty.

Commenting on this matter, Rupprecht remarks: "Clarity of policy and greater transparency is needed to avoid future debacles."

Rupprecht sees this fab, one of the biggest employers in the cluster, as an important facility for developing SiC and GaN power electronic capability in south Wales. However, this foundry is capable of making additional contributions, for example, its expertise in deep trench etching would also be valuable for the production of MEMS and photonic devices.

Since its launch in 2017, CSconnected has benefited from financial support from various sources. It is now coming to the end of a 55-month *Strength in Places* programme, which began in November 2020 and raised £25 million from the UK Research Initiative, alongside an additional £18 million from project partners. Another significant supporter of CSconnected is the Cardiff Capital Region, which has just secured £160 million to support local economic growth through the semiconductor investment zone.

For roughly the next three years CSconnected has core funding secured for a range of activities. As Rupprecht looks to strengthen support over that timeframe and beyond, he is keen to avoid dependency on a single project or a single activity, and is keen to pursue various sources of funding.

Seeking sovereignty

When the compound semiconductor cluster launched, its backers often argued for efforts that established strong supply chains within south Wales. Related to this cause, Rupprecht is keen to distinguish between sovereign independence and sovereign capability.

"I do think it's important that we have companies operating at different points in the value chain," says Rupprecht, arguing that much of this is now in place. For example, at one end of the spectrum is KLA, producing production equipment, and at the other is Microchip, shipping completed modules.

Over the coming years, it is possible that a supply chain forms in south Wales that begins with a SiC wafer and finishes by supplying a UK automotive company with a power module.

"That concept has already been demonstrated in a programme called Escape," reveals Rupprecht, adding: "But rather than having an integrated vertical UK supply chain, having all the companies exporting their products to multiple competing customers around the world is more important."

➤ While attending this year's CS Mantech, Howard Rupprecht (centre) explored an anechoic chamber at the University of Arizona with colleagues from the south Wales cluster. To the far left is Richard Shaddick from the Welsh Government, to the left is Chris Meadows, founder of CSconnected, to the right is Mike Jennings, an academic at Swansea University, and to the far right is Camille Colombier, marketing manager at CSconnected.

Moving over

One sign that the cluster is thriving is that start-ups within the UK are relocating to this region to draw on its support and expertise.

Kubos, a pioneer of microLEDs based on cubic GaN, moved to within the cluster earlier this year, so that it can use the fab at the Translational Research Hub at Cardiff University to scale its technology in a cost-effective way.

Within the region, there is also a fab at Swansea University, more suited to the development of power devices.

During the launch of the cluster, much was made of the economic benefits it would deliver, in terms of jobs and income generation. It would be easy to put these promises to one side after securing investment, but the cluster is taking these projections very seriously, with evaluations led by Max Munday's group within the Welsh Economic Research Unit at Cardiff University.

Quoting some findings from Munday and co-workers, Rupprecht says that since 2020 there has been a 28 percent increase in direct cluster company employment, and a 27 percent rise in sales over that time frame. "But the real big, big growth was gross added value, which has seen 122 percent growth over the same period."

These encouraging figures underscore the great momentum of the south Wales cluster, which Rupprecht will help to continue, while refining the support that's provided by CSconnected.

Swelling SiC shipments with a second fab

Opening an additional fab in Nanjing will help to grow sales of SMC Diode Solution's SiC products to around half the company's revenue

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN OUR INDUSTRY, one of the biggest trends is the growth in sales of SiC devices by companies with a strong pedigree in producing silicon power electronics. Of the current big five in SiC, Wolfspeed is the only player producing just wideband materials and devices, while STMicroelectronics, Onsemi, Infineon and Rohm have branched out into SiC after establishing a strong portfolio of silicon-based power electronics.

This direction of travel is also being pursued by some of the smaller players, such as SMC Diode Solutions, an American-led company that produces silicon and SiC power devices and has just opened its second fab in Nanjing, China. Opening this 300,000 square foot facility, which cost $3 billion RMB (US $410 million) and is creating 300 new jobs, will enable the company to boost production by 1.2 million silicon wafers and 60,000 SiC wafers per year – that equates to more than a quadrupling of the company's annual output.

➤ SMC's chairwomen and CEO Yunji Corcoran grew up in Nanjing before moving to the US to study for a PhD in Materials Science and Engineering at Stony Brook University. She has held the role of CEO at SMC since its founding in 1997.

Founded in 1997, SMC started considering the expansion of its power portfolio to include SiC products in 2014. Back then, when far fewer producers of these power devices competed for sales, SMC's chairwomen and CEO Yunji Corcoran reasoned that expanding into this area would enable her small-to-medium-sized company to expand its range of products and potentially target new applications.

At that time, Corcoran considered diversifying into either SiC or GaN. However, she felt that the pioneers of SiC, particularly Cree, offered a better-defined product. If SMC manufactured these devices, Corcoran believed that it would have a great opportunity to sell them to its existing customers, predominantly large power-supply companies. According to her, compared with GaN power devices, those based on SiC are much closer to SMC's silicon power rectifier family.

SMC started its commercial expansion into SiC with the production of Schottky rectifiers, shipping from 2019 onwards. Beginning its SiC offering with this product made much sense. "We are a silicon diode company," argues Corcoran, pointing out that by starting with a SiC Schottky rectifier, it's been easier to find customers for its first range of products.

Once SMC starting working with SiC, Corcoran and her colleagues could see the tremendous potential for the SiC MOSFET.

Today the company produces both classes of power device. Its SiC Schottky barrier diode portfolio has products with blocking voltages from 600 V to 3.3 kV, and a wide range of current ratings, which can include those that target a customer's particular needs.

The family of SiC MOSFETs is not as broad. There are 1.2 kV MOSFETs with on-resistances ranging from 16 mΩ to 160 mΩ, as well as a recently introduced a 1.7 kV variant. However, there are plans to expand the range. "We are working on the 650 and the 3300 at this moment," enthuses Corcoran.

Silicon products are dominating SMC's sales today, with those based on SiC only accounting for 10 percent of revenue. Corcoran attributes this modest but growing proportion to working with large and rigorous customers that are thorough when designing and evaluating prototypes.

Just a small fraction of the products that SMC makes in China are sold on the domestic market. 90 percent of business comes from sales oversees. Accounting for this, Corcoran explains that while her home town is Nanjing, she moved to the US to study and work, and it is there that she acquired her business acumen.

Given current tensions between the US and China, one might expect it's not easy for a company to have a fab in Nanjing that ships most of its products overseas. But somewhat surprisingly, SMC's activities have not been impacted by trade wars.

"When the US applied the duties, we were very concerned," admits Corcoran. "But in the end, it did not decrease our sales much, because it's not that easy to source our product outside China." However, the situation may differ surrounding the SiC MOSFET.

Outsourcing growth

For the leading manufacturers of SiC diodes and MOSFETs, there is a tendency to shift to greater degrees of vertical integration. Now some companies are beginning with the production of SiC boules from powders and concluding with the shipping of packaged devices.

For SMC, there's little sense in trying to emulate these bigger players. Instead, the company is focusing on what it is good at.

"We are not doing the epi, we're not doing the substrates, and we don't even do the packaging," says Corcoran, who explains that SMC's two fabs are used to process epiwafers into power devices. For the company's silicon products, there is a plant that can package the chips into modules. In the future, the plan is to use this facility to produce modules from SiC MOSFETs made in-house.

SMC uses suppliers based in China for its SiC Schottky-barrier-diode epiwafers, with Corcoran describing the quality as "pretty good".

For MOSFETs, a more complicated structure, the local supply is not as strong. "But we're testing the Chinese substrates," says Corcoran. "I think they are coming along."

She explains that SMC is devoting much effort to understanding which kinds of defect impact the MOSFET. Equipped with that insight, the company will be better prepared to assess the quality of Chinese SiC MOSFET epiwafers, and ensure that when they switch to them, there is no reduction in device performance.

Given current tensions between the US and China, one might expect it's not easy for a company to have a fab in Nanjing that ships most of its products overseas. But somewhat surprisingly, SMC's activities have not been impacted by trade wars

According to Corcoran, there are many good reasons for selecting Nanjing for its a second fab. As well as the advantage of being close to the first fab, this location benefits from: strong universities nearby; a good education system; a cost-of-living lower than that found in the cities on the east coast, such as Shanghai; and plenty of engineers with relevant expertise, partly due to a very large, local TMSC fab.

Today, SMC's fabs produce devices from 150 mm SiC epiwafers. However, the tools could be converted to handle 200 mm material – that's a move that is planned when the cost-per-unit-area of the larger format falls.

Another change may be an increase in the proportion of SiC devices produced in the fabs.

"We invested a lot of money in silicon carbide, and I hope we will have more than 50 percent of silicon carbide as our total revenue," says Corcoran. While sales of silicon devices are steadily increasing, she anticipates far faster growth for SiC products.

As well as shifting the balance of the product portfolio, SMC plans to penetrate new markets. The aim is to expand from simply serving the power supply sector to winning sales in renewable energy markets, including electric vehicles.

With more chipmakers with a silicon heritage now pursuing SiC, the chances that supply will satisfy demand are improving, helping humanity's efforts to try and curb its carbon footprint.

➤ Built in just 21 months, SMC Diode Solution's second fab will increase this chipmaker's production capacity by 1.2 million silicon wafers and 60,000 SiC wafers per year.

Crushing MOSFETs one tipping point at a time

The growth of GaN is inevitable as it displaces the MOSFET in one application after another

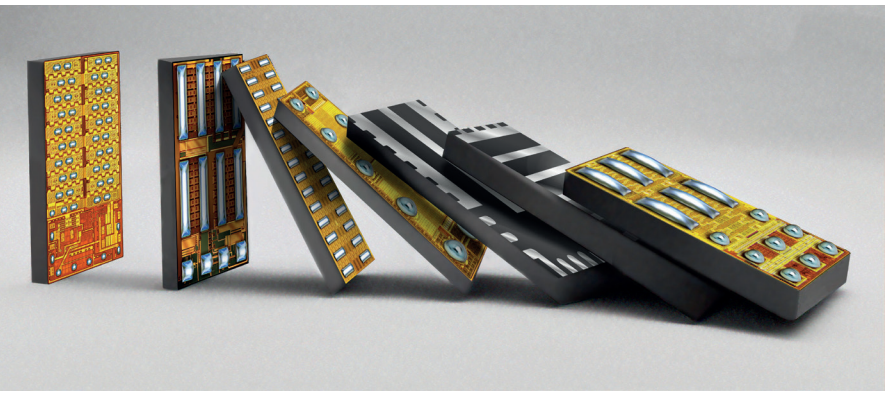
BY ALEX LIDOW FROM EFFICIENT POWER CONVERSION

GaN POWER TRANSISTORS are at a tipping point. It's a juncture where any small change or action leads to significant and often irreversible effects, and the future of these devices has reached a point of no return, where the dynamics of the situation shift dramatically.

This tipping point is following more than a decade of volume production of the GaN transistor. Since our company, Efficient Power Conversion (EPC), starting producing them in March 2010, they have repeatedly been touted as the replacement for the aging power MOSFET. Fourteen years on, the promise that GaN will crush silicon is now being realised.

To understand the changing rate of adoption of GaN, one can draw lessons from the 45-year-old power MOSFET. It's a device I know intimately, having been one of its first developers, as well as an instrumental player in the launch of the first product in November 1978. Back then the bipolar transistor was the incumbent power transistor. Despite being ten times slower, it was much cheaper than the MOSFET.

MOSFETs eventually crushed bipolar transistors. This did not occur overnight, but one application at a time. The first tipping point came from desktop computers, with Apple and IBM turning to the MOSFET for their AC-DC power supplies.



By adopting the superior transistor of the day, these tech giants could shrink their power supplies enough to fit inside desktop housings, a breakthrough that played a crucial role in widespread adoption of these computers.

Following this breakthrough, our MOSFETs continued to increase their deployment in high-performance applications while we focused on reducing costs and accelerating the learning curve as quickly as possible. Initially adoption took time, but jumps occurred whenever a new application ramped successfully. With each new tipping point for an application, the benefits to the business would extend beyond this individual triumph to trim the time and increase the likelihood of subsequent successes. Motor drives for high-speed plotters ramped in 1982. Anti-lock brakes ramped in 1985.

By 1988, thanks to higher volumes and significant capital investments, the manufacturing cost for the MOSFET had plummeted to below that of the bipolar transistor. Since then, the world never looked back. At that point in time the MOSFET had officially reached its tipping point. And that's exactly where GaN stands today.

GaN has already been adopted in several disruptive technologies, to the point where MOSFETs are no longer even considered for new designs. Each novel application for GaN can be thought of as having crossed an individual tipping point. This roadmap for ever-expanding adoption includes lidar, fast chargers, satellite electronics, AI, DC-DC power supplies, and humanoid robots.

With nearly fifty years of experience to guide us, we can identify four key factors that have played a crucial role in ensuring that GaN reaches its tipping point and finally surpass the MOSFET. These four factors, which exist in addition to all the cost, performance, and reliability requirements, are as follows: the design community now clearly

understands the large value derived from GaN; the targeted application is facing a changing landscape that leads to many open design windows; the adoption of GaN is being pursued by user community leaders, who are enjoying subsequent business success; and the existence of well-trained technical talent has emerged, which is capable of working with GaN and efficiently extracting its benefits.

For GaN technology, lidar provided the first application for crossing the tipping point. The simple reason behind this success is that GaN is capable of operating at far faster speeds than the MOSFET. Dave Hall, the visionary founder of Velodyne and the father of modern lidar, fully appreciated this benefit, realising that GaN technology enables a car sensor to see farther and with higher resolution than radar. Hall developed a spinning lidar system using EPC's first-generation GaN transistors, sparking the birth of the autonomous car.

Considering lidar from the perspective of tipping point elements, one can conclude that: Hall had a clear understanding of the substantial value derived from GaN; lidar opened many new design windows as it became an essential sensor for autonomous vehicles; Velodyne had huge success, attracting lots of customers and competitors; and Hall, with some assistance from EPC's engineers, knew how to extract the maximum performance from of these transistors.

The second application to reach a tipping point is the satellite power supply. As well as outperforming the MOSFETs, GaN is virtually immune from degradation caused by radiation in space. The key champion in helping to reach this particular tipping point is Dan Sable, CEO and founder of VPT. Today, just four years after initial deployment in this application, GaN transistors account for 30 percent of the satellite market for MOSFETs, and are on track to take the final 70 percent as legacy designs become obsolete or uneconomical.

Providing the third tipping point for GaN is the fast charger. Here the standout is Gene Sheridan, CEO and co-founder of Navitas Semiconductor. Today, virtually all fast chargers use GaN, thanks to its capability to deliver high powers and recharge power-hungry cell phones, tablets and laptops in a fraction of the time that silicon-based chargers would take.

Following all this success, we are now standing on the precipice of one of the most significant tipping points in recent history: AI. Servers for AI, such as those made by Nvidia, have crossed a crucial threshold, with virtually all of them utilising GaN in the on-board 48 V – 12 V (or in some cases 5 V) DC-DC converters.

While the full impact of the AI revolution is only beginning to be fathomed, one inevitable outcome is related to the tipping point of humanoid robots. These robots, equipped with 40 or more high-performance motors, rely heavily on GaN technology for higher torque density, higher power efficiency, less noise, and a more compact design. It is a set of requirements that is making silicon obsolete and GaN indispensable.

Taking a step back from specific successes, one can see that the tipping points for GaN are occurring with greater speed and a higher frequency. As has been the case for the MOSFET, every new development is educating the user community on GaN's unique value and accelerating its inevitable adoption in additional applications. And with each new positive experience and business success resulting from GaN, global implementation is rising, creating more and more design-window opportunities. Additional gains are the emergence of new GaN advocates within the user community, and new sources of capital. Over the last few years, thousands of trained design and manufacturing engineers have gone up the learning curve, and now know how to extract the additional efficiencies of GaN. Adding to these factors, GaN is proven to be more reliable than silicon, across a wide range of power levels, with a price that is comparable to the MOSFET. Due to all these compelling factors, it is inevitable that GaN's adoption will only accelerate, consuming the $12 billion MOSFET market while creating new markets of its own. In sum, GaN's tipping point is here.

What does the future hold for the compound semiconductor industry?

Growth is forecast for all leading forms of compound semiconductor device, driven in part by demand for more data, an uptake in AI, increasing opportunities for satellite communication and growing sales of electric vehicles

BY ALI JAFFAL, TAHA AYARI AND AYMEN GHORBEL FROM YOLE GROUP

THE COMPOUND SEMICONDUCTOR industry is now booming, having established itself as a significant player alongside silicon-based semiconductors, bringing not only superior performance but also new functionalities that silicon cannot achieve, such as light emission. These semiconductors are becoming increasingly popular in power electronics, RF, photonics, and microLED displays. For power applications, sales are dominated by SiC and GaN devices; for RF applications, GaAs and GaN devices lead the way; for photonics, InP and GaAs are the leading material systems; and for LED/display applications, GaAs and sapphire are the key substrate materials.

The compound semiconductor industry is well-established, having formed an entire ecosystem, with its own equipment for crystal growth, wafer manufacturing, front-end manufacturing, testing and packaging. According to recent market research by our company, Yole Group, the value of compound semiconductor substrates is rising at a compound annual growth rate of 17 percent over the 2023 to 2029 timeframe, to reach US$3.3 billion[1]. Underpinning this growth is an expansion in key facilities that are supporting a transition to larger substrates. There is a migration to 200 mm wafers for SiC and GaN-on-silicon, driven by power electronics growth in the automotive and consumer markets; in the photonics sector, the use of 150 mm InP is on the rise, spurred on by the datacom market; and in the microLED displays market, there is increasing use of 200 mm GaAs and sapphire. However, the latter application has been hit badly by Apple, who closed its microLED project earlier this year, after being the main player pushing for 200 mm substrates with it partner ams-Osram[2].

Looking in more detail at the substrate market, a number of SiC substrate makers, including Coherent, Wolfspeed, SK Siltron, SICC and TankeBlue, are actively working on the 200 mm format, with initial volume shipments starting late last year. The Chinese SiC substrate supply is growing rapidly, and is fiercely competing with the US[8].

For GaN-on-silicon for power applications, for the last 2-3 years volume production has involved 200 mm wafers, the format employed by the massive Chinese company Innoscience. All recent investments and capacity expansions are focused on this platform, including Infineon's GaN fabs in Villach and Kulim.

When it comes to InP, the mainstream substrate size is still 75 mm. However, market leaders such as Sumitomo Electric and AXT have the capability to produce good-quality 150 mm InP substrates, and this year they are shipping significant volumes for R&D. Sales of higher volumes are expected over the next few years.

Regarding GaAs, 150 mm substrates continue to dominate photonics and RF applications. Here the market is dominated by Sumitomo Electric and Freiberger.

As well as high-quality substrates, optimal devices demand high-quality epitaxy. This leaves chipmakers with one of two choices – to adopt the captive approach, and undertake epitaxy in-house; or to use an 'open' approach, drawing on the epitaxial services

of a number of players, including IQE, Landmark, VPEC, IntelliEPI and Sumitomo Chemical. We estimate that between 2023 and 2029 the open epiwafer market will expand at a compound annual growth rate of 19 percent to hit US$2.5 billion. Sales from the SiC open epiwafer market are already soaring, and will climb to account for 64 percent of that total by 2029.

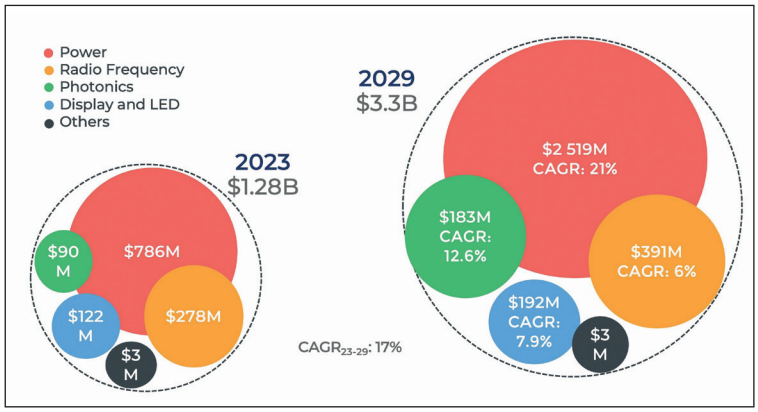
EVs and fast chargers are gaining

Since 2017-2018, sales of SiC and GaN devices have experienced rapid growth. Helping this has been Tesla's adoption of SiC in its inverters, a move that marked significant disruption in the EV market. Here SiC plays a crucial role in 800 V fast charging, significantly reducing the time it takes to accomplish this task. Today, high-volume EVs, such as BYD's Han and Hyundai's Ioniq 5, are being shipped with SiC technology. Sales to automakers have ramped the revenue of leading device manufacturers like STMicroelectronics, onsemi, Infineon, Wolfspeed, and Rohm. These pioneers of high-volume SiC power device production all realised record revenue in 2023, and are on track to net sales from these products of US$1 billion by 2024-2025. We forecast that by 2029 the total market for SiC devices will exceed US$9.6 billion[3], with ramping revenue not only driven by the EV market – sales growth will also come from industrial, energy, and rail applications. Supporting this substantial hike in revenue is capacity expansion, business integration, and innovative business models.

Meanwhile, in the power GaN market the primary drivers of growth are still consumer applications. Recent trends include chargers with higher power capacities of up to 300 W, along with power supplies and motor drives for home appliances that offer a higher efficiency and compactness. We are foreseeing two additional catalysts for power GaN growth: automotive and data-centre applications. Due to these contributions, the power GaN market will be propelled to more than US$2.25 billion by 2029[3].

Evolutions in RF

In the RF domain, GaAs technology is a well-established building block for RF front-end modules in smartphones, and is showing growth opportunities in automotive applications. The other key material in RF is GaN-on-SiC. Over the last two decades this has been used to develop power amplifiers for defence and aerospace applications, with efforts given much support by the US government. With the advent of 5G, new macro base stations are adopting GaN technology over existing silicon LDMOS, a move that enables more complex architectures at higher frequencies with greater efficiency. RF GaN technology is also expanding into markets such as satellite communication and RF energy. According to our recent analysis, the total RF GaN device market will grow from US$1.1 billion in 2023 to US$2.07 billion by 2029[4,7].



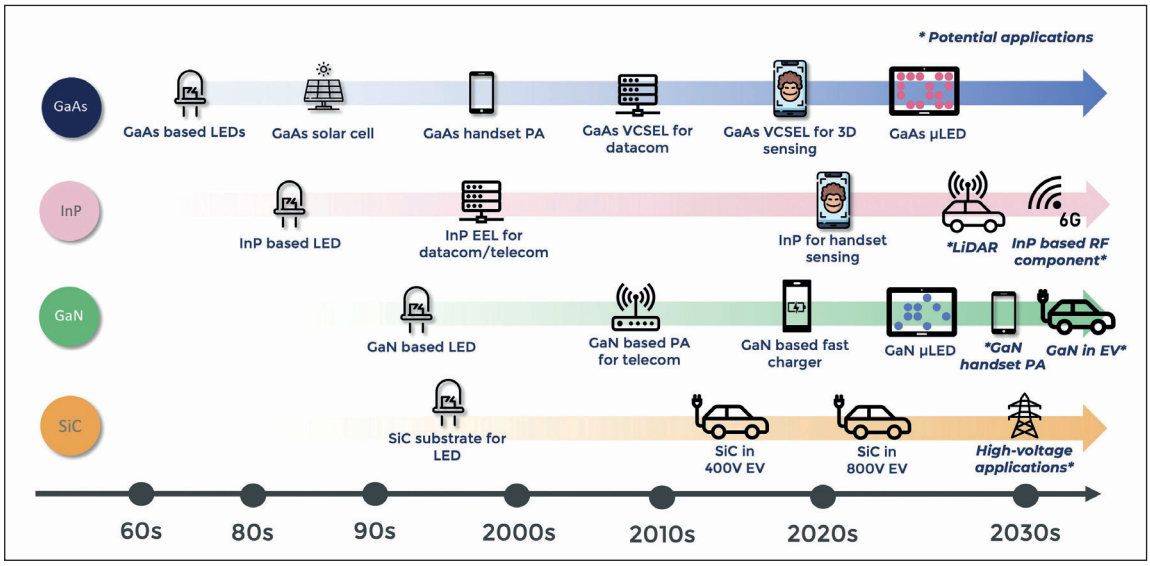
➤ 2023-2029 compound semiconductor substrate market by application ($M). Source: *Status of the Compound Semiconductor Industry* report, Yole Intelligence, 2024. Credit: Yole Intelligence.

An alternative material system for RF devices that has garnered interest in recent years is GaN-on-silicon. Last year Infineon introduced a GaN-on-silicon power amplifier module processed on 200 mm wafers to the telecom infrastructure market, directly competing with GaN-on-SiC technology. With the potential to scale to 300 mm, RF GaN-on-silicon could offer performance and cost benefits to compete with GaAs technology for 6G PAs. Other companies exploring RF GaN-on-silicon technology include UMC, STMicroelectronics, GlobalFoundries, Sony and Finwave. As these newcomers invest in power GaN-on-silicon, they are able to use 200 mm facilities to enter RF applications without having to make risky investments.

A pioneer of 150 mm RF GaN-on-silicon technology is Macom. This US chipmaker has secured design wins for military tactical radios for over a decade. Last year Macom expanded into satellite communication by acquiring Ommic SAS, and enhanced its GaN-on-SiC portfolio by buying Wolfspeed's RF business. These acquisitions have elevated Macom to one of today's top four RF GaN device players.

AI drives photonics growth

The other major applications within the compound semiconductor industry are based on photonics. A significant market here is the GaAs VCSEL for 3D sensing in smartphones. This application began in 2017 with Apple, followed by Android makers like Huawei and Xiaomi. While US-China sanctions have slowed uptake, there has been a re-adoption of GaAs VCSELs for 3D sensing, with Chinese OEMs such as Huawei, in this case using this technology in its Mate 60 Pro model. This leads one to wonder whether we will now see more Chinese OEMs adopting GaAs VCSELs in the consumer market – and whether these chipmakers will be able to meet the cost target for low-end smartphones. What is beyond question is that GaAs VCSEL supply is growing in China, with several players demonstrating excellent capabilities, including Vertilite, Everbright photonics, RaySea, and QM lasers. This expertise will aid the adoption of VCSELs for automotive lidar in China. Note that China represents the biggest market for automotive lidar.



➤ Evolution of compound semiconductor applications – inflection points. Source: *Status of the Compound Semiconductor Industry* report, Yole Intelligence, 2024. Credit: Yole Intelligence.

In the optical communications sector, AI is driving GaAs VCSEL adoption in data centres. These emitters are being deployed in optical transceivers that transmit and receive data at 800G and beyond. Key to such high speeds are 100G/lane VCSELs. Coherent and Broadcom are already mass-producing these devices, and Lumentum is set to follow later this year. Development of 200G/lane VCSELs for 1.6Tb pluggables is underway, with mass production forecast for 2026-2027. This begs the question: What technology will be used in 1.6Tb optical transceivers for short-reach applications between 2024 and 2026?

Also driven by AI are sales of InP edge-emitting lasers, with shipments to this application dominated by 100G and 200G/lane InP electro-absorption-modulated lasers and high-power continuous-wave distributed-feedback lasers that are enabling 800G and 1.6T optical transceivers in long-reach applications.

Back in 2023, AI had yet to make a significant impact, and that year was a challenging one for the InP business. Headwinds came from a slowdown and increased inventories from hyperscalers and cloud service providers, as well as reduced consumer market adoption when Apple reverted to the GaAs VCSEL for proximity sensors, instead of using InP edge-emitting lasers.

Since the beginning of this year, the situation in the InP market has improved significantly. This is especially true for the datacom sector, which is driving growth in substrates, epiwafers, and devices. Several encouraging signs have emerged, such as Lumentum's acquisition of Cloudlight to ensure full vertical integration in its datacom business. However, the most significant development is the announcement of a 150 mm InP fab at Coherent. Will we now see other players adopting the 150 mm InP platform to reduce costs and meet market demand, especially if InP re-enters the consumer market in the short term and 6G in the long term?

After weighing up all the likely scenarios, we forecast that the GaAs and InP photonic bare die markets will reach US$1.94 billion and US$.3.5 billion, respectively, in 2029[5].

What's next?

To push performance and cost limits, the compound semiconductor industry continues to explore new materials, platforms and designs. Now one critical question is this: Which emerging semiconductor substrate will be the next game changer? The answer is not obvious, as material scientists and industrial players are developing a number of new foundations for epitaxial growth, including Ga_2O_3, diamond, bulk GaN, GaSb, InSb, bulk AlN, smart-SiC, and an engineered substrate based on polycrystalline AlN. We are projecting that the emerging substrate market will grow to US$264.5 million by 2028[6], driven by power applications, particularly using engineered substrates.

Considering all these advances, the compound semiconductor market is set for sustained growth, especially in sectors where silicon falls short. The future of technology will undoubtedly be shaped by the ongoing evolution and impact of compound semiconductors.

FURTHER READING / REFERENCE

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- [7] RF GaN 2024
- [8] Power SiC Manufacturing 2024

Bipolar *p*-FETs enable all-GaN power integration

Bipolar transport overcomes the inherent barriers of GaN *p*-FETs to pave the way to higher current densities

BY MENGYUAN HUA FROM SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

GaN POWER DEVICES have many attributes. They are renowned for their exceptional switching efficiency and high power density, strengths that are driving the development of miniaturised, energy-saving power systems. Thanks to a wide bandgap and stable material properties, GaN-based power devices are also capable of maintaining a good performance in challenging environments, such as extreme temperatures and irradiation conditions. And in addition to these capabilities, GaN power devices are revolutionising power systems towards higher levels of integration and intelligence. Given all this, it's of no surprise that GaN-based HEMTs have rapidly surpassed traditional silicon devices to play an indispensable role in a number of fields, ranging from consumer electronics to industrial power supplies.

However, while much progress has been made to date, there is still much more to do. In this regard, one important area for improvement is the GaN power IC – today there is a significant challenge in realising the seamless integration of power devices with low-voltage peripheral circuits. In the latest approaches to hybrid integration, the silicon-based circuits that are used for driving, sensing and protecting functions, are integrated with GaN power devices through packaging. This results in non-negligible parasitic inductance, which can lead to gate ringing, particularly during high-power fast-switching transients. Two downsides of this are a limited switching speed and a compromised system reliability. What's more, the silicon devices in these hybrid designs fail to handle extreme environments as well as GaN devices, narrowing the

application scope. Consequently, moving to an all-GaN integration strategy has much appeal, including liberation from parasitic issues and the constraints of silicon-based devices, as well as the opportunity to unleash the full potential of GaN power ICs.

There are several straightforward approaches for all-GaN integration, such as leveraging established *n*-channel device technology, resistor-transistor logic and direct-coupled FET logic. However, all these methods are impaired by excessive power consumption, due to a significant static current that diminishes the efficiency of the power IC and necessitates enhanced heat dissipation strategies.

A promising solution to effectively blocking the static current is the GaN-based complementary logic IC, incorporating both the *p*-FET and the *n*-FET. In this design, the existing *p*-GaN layer on the E-mode GaN HEMT platform is used to fabricate the *p*-FET.

The simplicity of this approach has attracted much attention, leading to efforts directed at boosting *p*-FET performance via strategies that include reducing interface trap states, downscaling the device, and engineering the gate dielectric. But even with these refinements, the current density of the *p*-FET falls far short of that of the GaN HEMT. This gap in current density between the GaN *p*-FET and its *n*-FET sibling poses a significant hurdle for progressing GaN CMOS technology.

Limiting the current density of the GaN *p*-FET is the low conductivity of the *p*-GaN layer. Due to a considerable effective mass and strong scattering, the mobility of holes is nearly two orders of magnitude lower than it is for electrons. Compounding this issue, magnesium is the only effective dopant available for *p*-type GaN. Unfortunately, it's far from an ideal dopant, being held back by a low activation ratio and a deep energy level that restricts the hole concentration in the *p*-GaN layer to 10^{18} cm^{-3}. While innovative epi-structure designs involving N-polar GaN, AlN and GaN heterostructures, superlattices, and InGaN insert layers are able to enhance hole mobility or density, these approaches are incompatible with the existing commercial *p*-GaN gate HEMT platform.

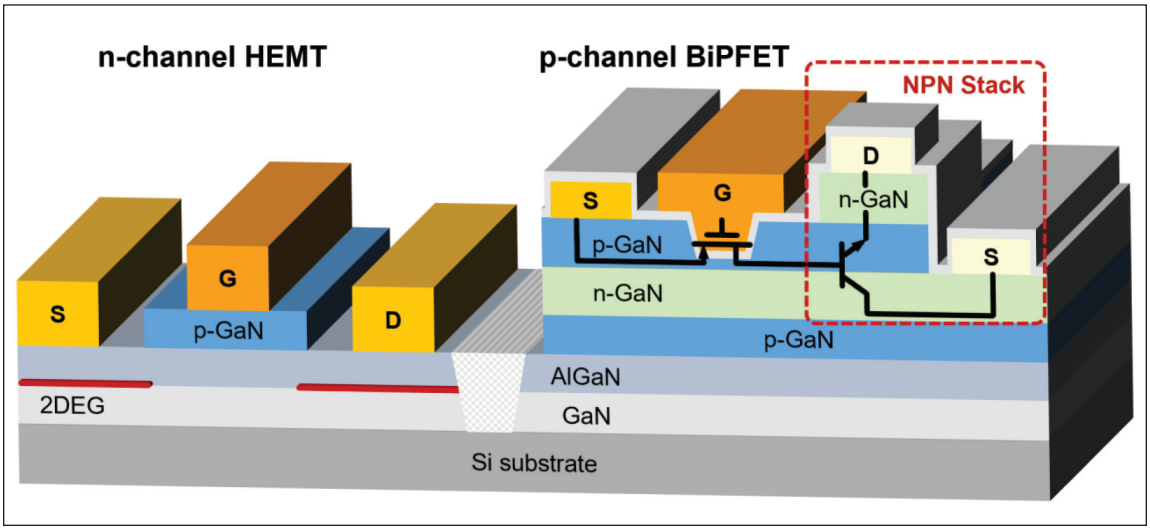
To overcome this challenge, our team at the Southern University of Science and Technology is pursuing an innovative GaN *p*-FET architecture endowed with a bipolar transportation capability (see Figure 1). This bipolar *p*-FET (BiPFET) features a conventional *p*-FET gate for maintaining *p*-type control logic, as well as an additional *n*-*p*-*n* GaN stack, which functions as a bipolar junction transistor that amplifies the current density. Operating in the on state, the *p*-channel turns on with a gate voltage below the threshold voltage. In this state, a minor hole current flows through the *p*-channel, and is injected into the base region of the *n*-*p*-*n* stack, initiating a substantial electron current. With electrons serving as majority carriers, the current density of the BiPFET is no longer confined by holes.

In addition to its remarkable conduction capability, the BiPFET inherently ensures a more stable threshold voltage and a higher drain-to-source breakdown voltage. When in the off-state, the bottom *n*-GaN region acts as a back-side field plate, extending the depletion region from the *p*-FET gate to the drain side. Thanks to this there is a more uniform electric field distribution, alleviating stress on the *p*-FET gate and improving the off-state breakdown voltage.

Another advantage of the BiPFET technology is that it is ready for integration with GaN HEMTs, thereby demonstrating outstanding compatibility and feasibility. The *n*-*p*-*n* stack can be realised through MOCVD growth, and the process flow of the BiPFET aligns well with that of the standard *p*-GaN gate HEMT. These strengths underscore the promising potential of the BiFET for the development of all-GaN ICs.

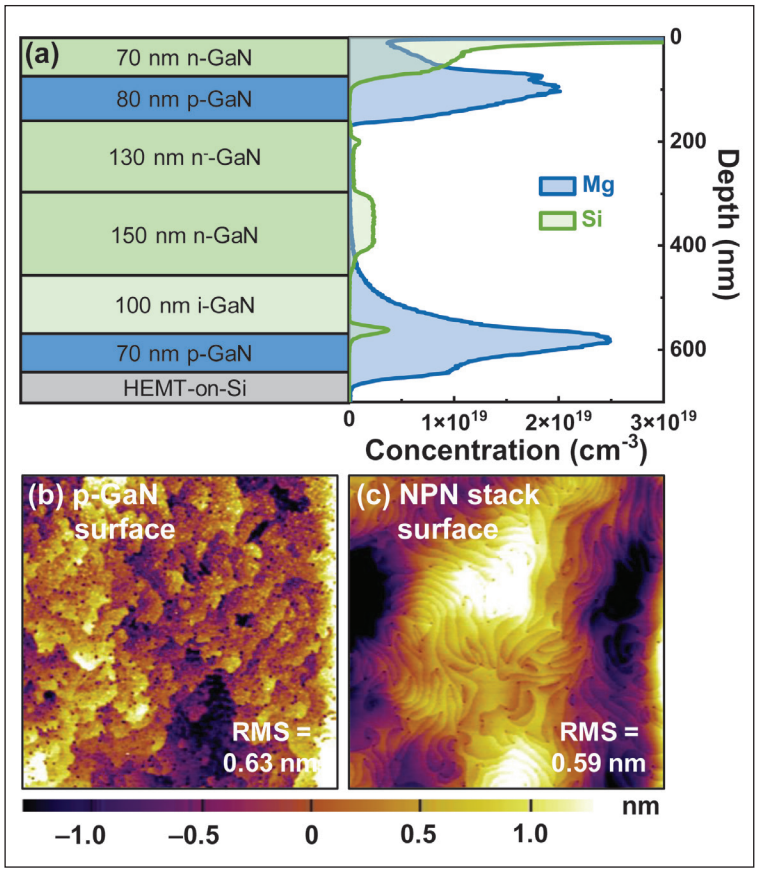
Demonstrating the concept

We have investigated the capability of our BiPFETs by producing these devices from a commercial



➤ Figure 1. A promising option for GaN integration is the combination of the *p*-GaN gate HEMT and the bipolar *p*-FET.

p-GaN HEMT platform featuring a 4.2 μm-thick GaN buffer layer, a 420 nm-thick undoped GaN channel layer, a 15 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 75 nm-thick *p*-GaN layer with magnesium doping at a concentration of 2.5×10^{19} cm^{-3}. Using this platform, our partners at Suzhou Institute of Nano-tech and Nano-bionics, Chinese Academy of Sciences, led by Qian Sun, selectively grew the *n*-*p*-*n* stack by MOCVD. This stack comprises a 150 nm-thick bottom *n*-GaN collector layer with a silicon doping concentration of 3×10^{18} cm^{-3}, a 130 nm-thick *n*-GaN layer with a silicon doping concentration of 5×10^{17} cm^{-3} to enhance voltage blocking capability, an 80 nm-thick *p*-GaN base layer with a magnesium doping concentration of 2×10^{19} cm^{-3}, and a 70 nm top *n*-GaN emitter layer with a silicon doping concentration of 10^{19} cm^{-3} (see Figure 2(a)).



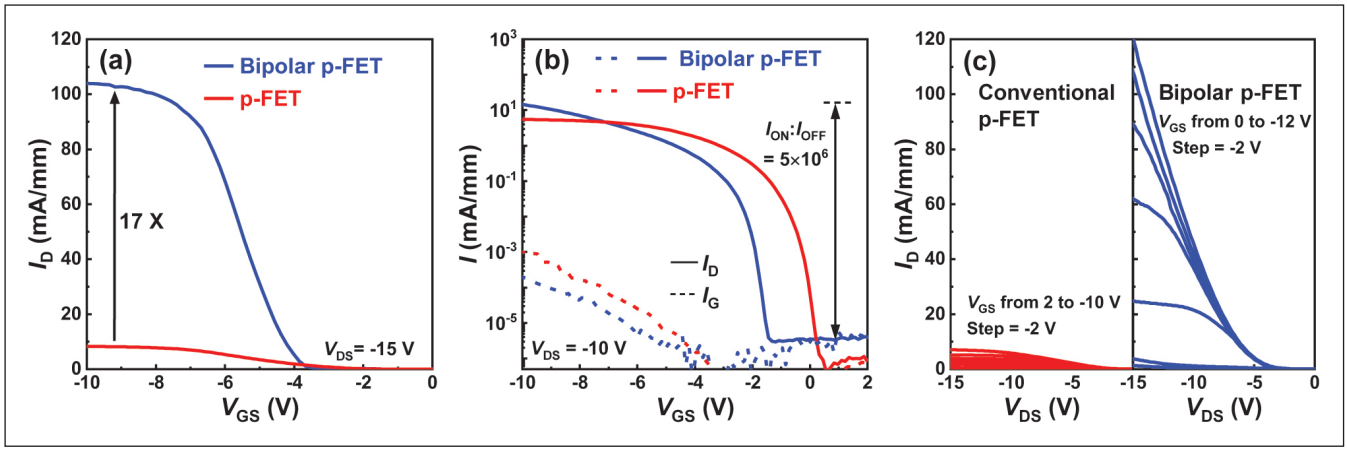
➤ Figure 2. (a) An *n*-*p*-*n* epi-structure on the conventional *p*-GaN HEMT platform and a secondary ion mass spectrometry depth profile of magnesium and silicon dopants. Atomic force microscopy images of the (b) initial *p*-GaN surface and (c) GaN surface after *n*-*p*-*n* stack growth on the E-mode GaN HEMT platform.

Note that we insert a 100-nm undoped GaN layer between the bottom *n*-GaN and *p*-GaN layers to mitigate the impact of the magnesium memory effect. Encouragingly, this *n*-*p*-*n* epi-stack preserves the favourable surface morphology of the original *p*-GaN, with clear atomic steps (see Figure 2(b) and (c)).

The fabrication of our BiPFETs starts with two-step etching, using a chlorine-based inductively coupled plasma recipe. The first step involves etching the collector region to remove the *n*-GaN layer, part of the *p*-GaN base layer, and then the hard mask SiO_2 in the *p*-FET region. During the second step, we simultaneously etch the top *n*-GaN in the *p*-FET region and the remaining *p*-GaN in the collector region until we reach the target depth. After removing the hard mask, we activate dopants in the *p*-GaN layer by annealing our samples under nitrogen gas at 750°C for 30 minutes.

Following dopant activation, we add *p*- and *n*-ohmic contacts. To ensure an excellent *p*-ohmic contact on the etched *p*-GaN surface, we sputter a 50 nm-thick layer of magnesium on the contact region, prior to annealing at 600°C, to diffuse this metal into the GaN layer. After removing the annealed magnesium layer, we form *p*-ohmic contacts with conventional evaporation and annealing processes.

According to electrical measurements, the contact and sheet resistance for our *p*-ohmic contacts are 57 Ω mm and 65 kΩ/sq, respectively. These values are comparable to those for a fresh bare *p*-GaN layer without any etching.



➤ Figure 3. (a) Linear-scale transfer, (b) log-scale transfer and gate leakage current, and (c) output characteristics of BiPFETs compared with conventional *p*-FETs.

Our next step is to form *n*-ohmic contacts on upper and lower *n*-GaN layers through photolithography, evaporation, lift-off, and annealing.

Following contact formation, we undertake slow inductively coupled plasma etching to gradually recess the gate trench. By going slow, we minimise plasma-induced damage. Then, using atomic layer deposition, we add a layer of Al_2O_3 that is approximately 22 nm-thick and serves as the *p*-FET gate dielectric. Evaporation of the gate electrodes follows, before we finalise the fabrication by defining contact vias and probing pads.

Improved current density ...

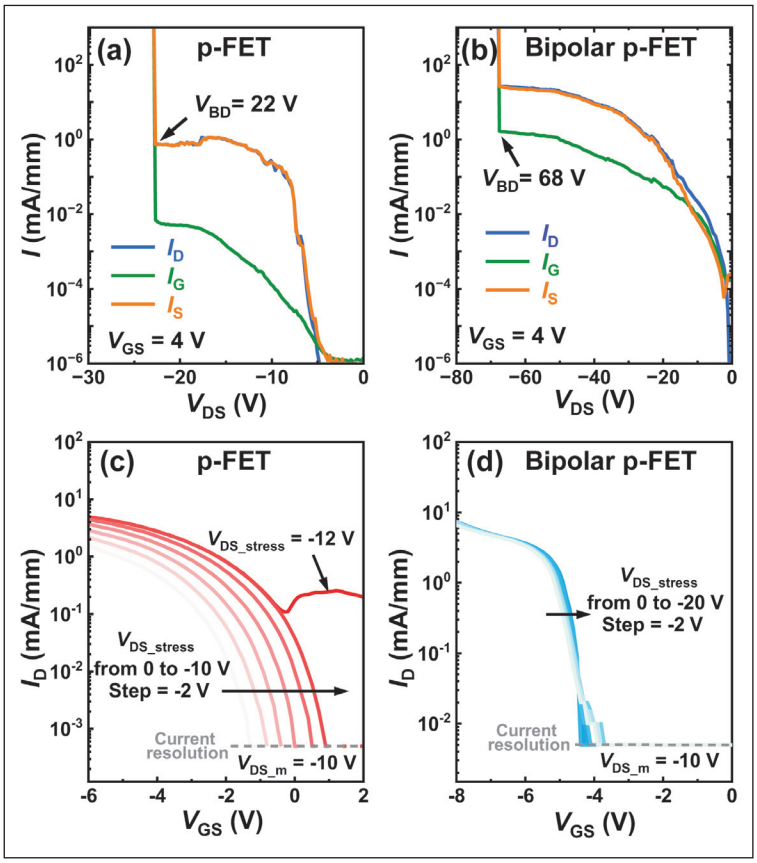
By integrating the *n*-*p*-*n* stack into the *p*-FET, we realise a substantial increase in the current density of the GaN *p*-FET. With identical MIS-gate dimensions as the *p*-FET, our BiPFET delivers a 17-fold hike in current density to more than 100 mA mm^{-1} (see Figure 3). This enhancement in current density is particularly pronounced when comparing output characteristics.

It's worth noting that this substantial increase in current density is realised without compromising the performance of the MIS-gate. Our BiPFET maintains a high current on-off ratio and exhibits a low gate-leakage current, signifying the well-preserved performance of the MIS gate (see Figure 3(b)). With moderate device scaling, we anticipate an increase in current density.

... and enhanced stability

As well as significantly enhancing the current density, the incorporation of the *n*-*p*-*n* stack offers the additional advantage of mitigating the voltage drop on the *p*-channel MIS-gate. When operating in the off-state, a depletion region forms in the reversely biased *p*-GaN/bottom *n*-GaN junction, creating a depletion region that homogenises the electric field distribution and alleviates stress on the MIS gate. The introduction of the *n*-*p*-*n* stack elevates the off-state breakdown voltage from 22 V to 68 V (see Figure 4(a) and (b)).

The strengths of our BiPFET extend to exhibiting a more stable threshold voltage under pulsed drain-bias stress, a merit that's attributed to a reduced voltage stress on the *p*-channel MIS gate. Pulsed tests, conducted on both the *p*-FET and BiPFET, show that the latter has a significantly lower drain-induced threshold voltage shift (see Figure 4(c) and (d)). In the BiPFET, the *n*-*p*-*n* stack shares the drain stress and safeguards the gate region. Even under a high drain stress of up to 20 V, we do not uncover any degradation in our pulsed transfer curves.



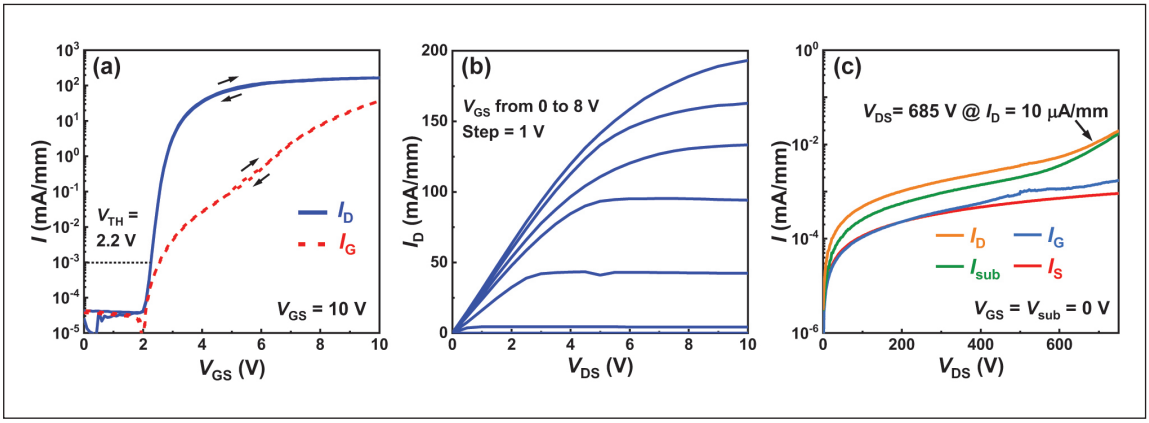
➤ Figure 4. (a) Off-state leakage current and breakdown characteristics of (a) the conventional *p*-FET and (b) bipolar *p*-FET. Plots of pulsed drain current as a function of gate-source voltage (I_D-V_{GS}) of (c) the *p*-FET and (d) the BiPFET measured with various drain-source stress voltages (V_{DS_stress}).

Integration capability

To assess the integration capability of our BiPFET, we concurrently fabricated a *p*-GaN gate HEMT on the same epitaxial wafer. This *p*-GaN gate HEMT demonstrates E-mode operation and a high on-off ratio, confirming the continued activation of the *p*-GaN layer after regrowth of the *n*-*p*-*n* stack (see Figure 5(a)).

We measure a saturation drain current density for our fabricated *p*-GaN gate HEMT of 200 mA mm^{-1},

The strengths of our BiPFET extend to exhibiting a more stable threshold voltage under pulsed drain-bias stress, a merit that's attributed to a reduced voltage stress on the *p*-channel MIS gate. Pulsed tests, conducted on both the *p*-FET and BiPFET, show that the latter has a significantly lower drain-induced threshold voltage shift



➤ Figure 5. (a) Transfer and gate leakage, (b) output and (c) off-state leakage characteristics of the E-mode *p*-GaN gate HEMT on the same platform with the BiPFET.

a value comparable to that of conventional *p*-GaN gate HEMTs (see Figure 5(a) and (b)). This robust conduction capability indicates that the 2DEG channel is not significantly impacted by regrowth of the *n*-*p*-*n* stack.

Another encouraging finding is that after regrowth, the buffer and channel layers still exhibit excellent blocking capability (see Figure 5(c)). The off-state breakdown voltage of the fabricated *p*-GaN gate HEMT achieves 685 V, validating the feasibility of integrating *n*-channel devices with BiPFETs for the realisation of GaN CMOS and power ICs.

The key strengths of our BiPFET are its exceptionally high current density and its enhanced stability, attributes that enable this class of transistor to be a very promising candidate for seamless integration with GaN HEMTs. This breakthrough paves the way for the design and fabrication of GaN CMOS and power ICs, laying the foundation for tomorrow's advanced power systems.

FURTHER READING / REFERENCE

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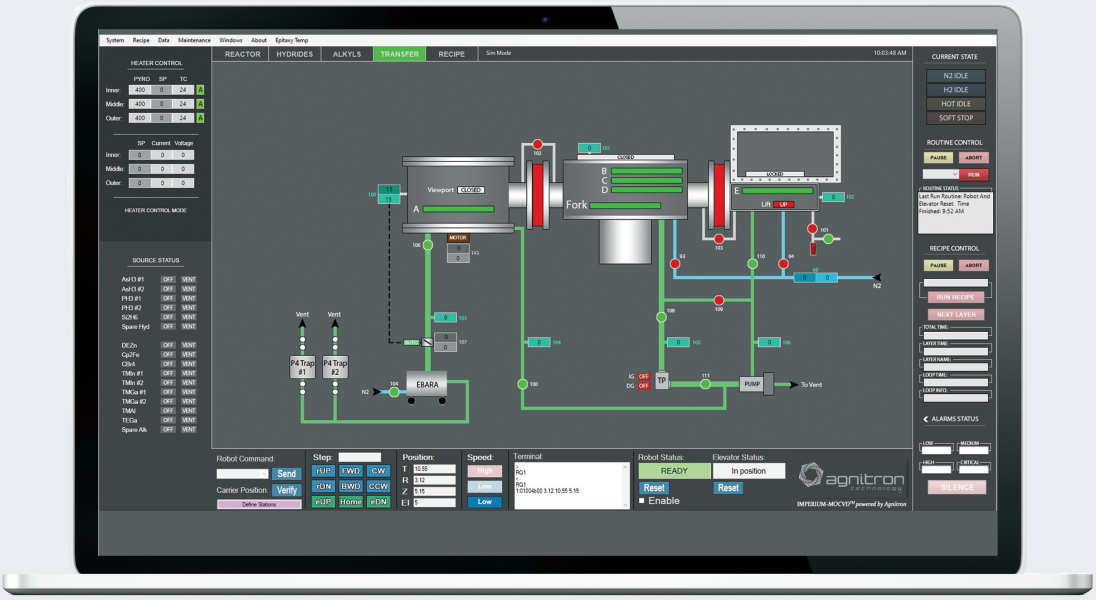

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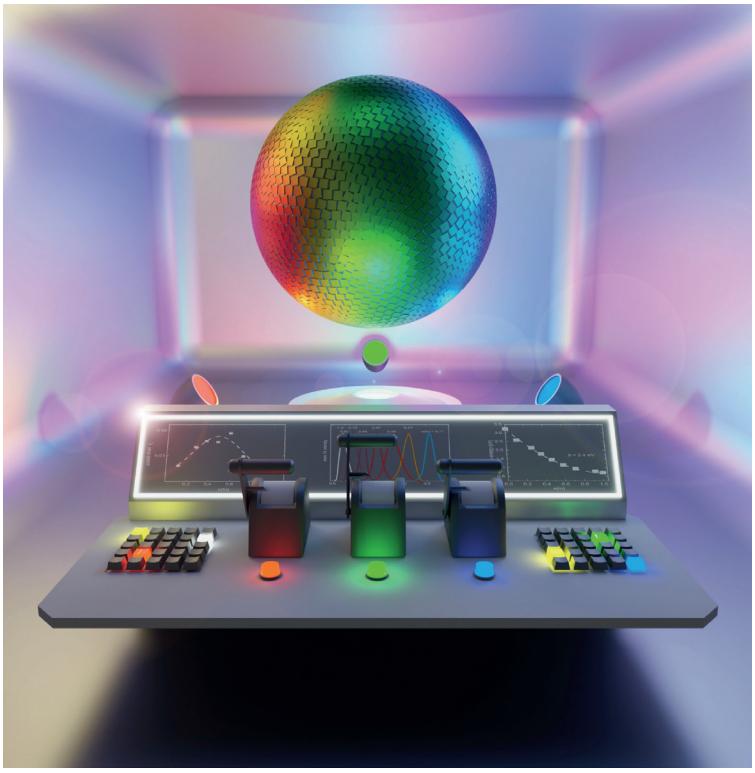
Tackling the amber emission challenge with cubic nitrides

The growth of cubic nitride by MBE promises to enable the production of microLEDs that span the entire visible range

BY JÖRG SCHÖRMANN, MARIO ZSCHERP, SILAS JENTSCH AND SANGAM CHATTERJEE FROM JUSTUS LIEBIG UNIVERSITY GIESSEN AND VITALII LIDER, ANDREAS BEYER AND KERSTIN VOLZ FROM PHILIPPS-UNIVERSITY MARBURG

WHAT SOUNDED LIKE science fiction a mere two decades ago is starting to become part of our everyday life: virtual elements enriching the real world. This is evident in the on-going trend of companies and organisations turning to immersive technologies to benefit from the advantages of extended reality, such as augmented reality (AR) or mixed reality (MR). However, while much progress has been made with these technologies, there are still a few hurdles to overcome.

One of the biggest is to address the poor visibility of displays under bright ambient conditions, such as sunlight. A promising candidate for tackling this weakness is the microLED. However, this emitter, with dimensions well below 10 μm, needs to deliver an improved performance – as well as, ideally, the emergence of a unified materials platform covering the whole visible spectrum.



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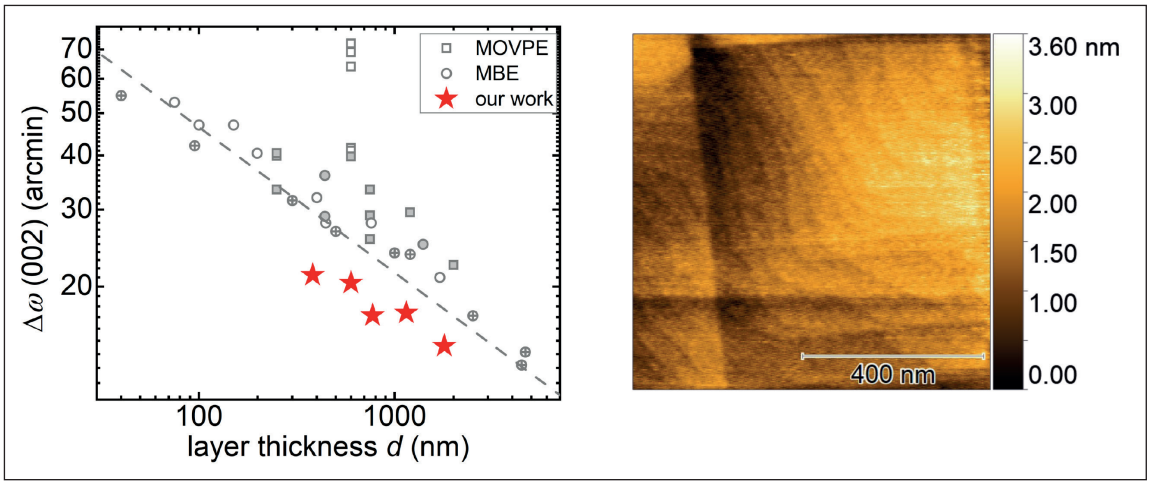
Addressing the latter issue requires some radical changes to LED production. Today, efficient, large-area white and blue LEDs employ hexagonal nitride technology, while their red counterparts are based on AlGaInP multilayers with a different crystal structure. Regardless of the approach, these devices are held back by a decrease or 'droop' in efficiency as the emission wavelength is extended to the green/amber range. This flaw is commonly known as the 'green gap'.

Of these two classes of semiconducting materials, the group-III nitrides – they include AlN, GaN, InN and their alloys – are preferred, being viewed as the crucial semiconductor materials for the current and next-generation of optoelectronic technologies. Up until now, all relevant devices made from this material system are based on the thermodynamically stable hexagonal phase.

At the very heart of these III-nitride devices, which emit in the blue and green, are InGaN multilayer structures that incur inherent internal electric fields. This gives rise to the quantum confined Stark effect (QCSE), which result from the interplay of the spontaneous polarisation that arises from the inherent asymmetry of the hexagonal crystal structure, and the piezoelectric polarisation, an undesirable effect of strain in this crystal structure. One culmination of the QCSE, which impedes radiative recombination, is a spatial separation of the electrons and holes in the quantum wells.



➤ Figure 1. The quality of material can be evaluated by considering values provided by ω-scans, produced by X-ray diffraction. The general trend is a decreasing value for Δω with increasing layer thicknesses. Grey squares and circles refer to other c-GaN layers grown by MOCVD and MBE on comparable 3C-SiC substrates (left). An atomic force microscopy image offers insight into surface morphology, uncovering mono-atomic steps across the smooth surface of c-GaN (right).

These issues are particularly prevalent at longer wavelengths. To propel emission from the blue to the green and beyond, the indium content in the InGaN quantum wells has to increase. But this induces even more strain in the active region, enhancing the QCSE and driving down the radiative recombination rate.

Another side effect of the increase in indium richness in the wells is a screening of the QCSE under high injection conditions. A decrease in colour stability results – although this can be turned into an advantage, if there is a need for colour tuning.

For phosphide LEDs there is a different set of issues at play. When miniaturising these devices, surface recombination drags down efficiency, due to an increased surface-to-volume ratio. While it might be possible to address this concern, there is also a more fundamental one that cannot be overcome. With this material system, as the composition is adjusted to shift the emission towards the green, the bandgap switches from direct to indirect. This causes efficiency to plummet, and prevents the use of phosphides for the manufacture of blue and green LEDs.

The cubic advantage

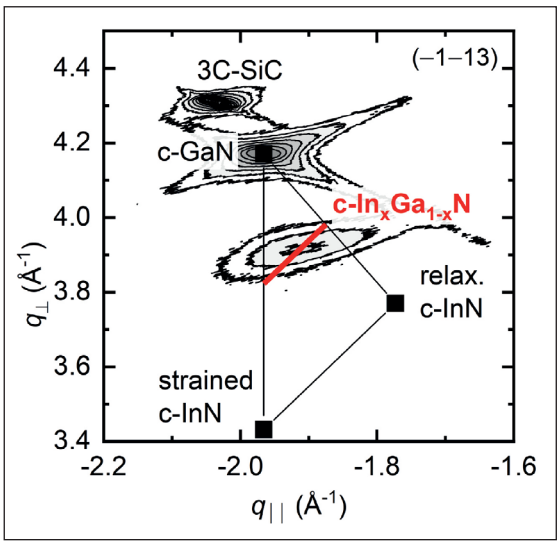
Intriguingly, group III-nitrides can also crystallise in the metastable cubic structure. This form promises several advantages, stemming from a polarisation-free material system that is inherent, thanks to cubic crystal symmetry. The most prominent merit of such a structure is that it is free from the QCSE, equipping LEDs with superior colour stability at higher injection currents. Additional advantages of c-GaN over its hexagonal counterpart include a high carrier mobility, a high *p*-type conductivity and a high electron drift velocity.

As well as all these attributes, c-GaN has a bandgap of 3.2 eV. That's 0.2 eV lower than h-GaN, reducing the necessary indium content by about 10 percent for targeting a particular emission wavelength in the red.

Due to the combination of an absence of the QCSE and a lower bandgap, cubic nitrides promise to provide a material platform for LEDs spanning the entire visible range. The opportunity to produce powerful blue, green, and red emitters from this material system is incredibly attractive for cost-efficient integration schemes, in particular, once ported onto 300 mm silicon wafer technology.

Another niche for MBE?

Today, virtually all nitride devices on the market are produced by MOCVD. While this may be desirable for commercial reasons, MBE has advantages for the metastable cubic phase: the extreme nonequilibrium



➤ Figure 2. X-ray diffraction of the asymmetric ($\bar{1}\bar{1}3$) reflection of c-GaN. The reciprocal space map reveals a pure cubic phase and a single, partially strained c-$In_{0.47}Ga_{0.53}N$ layer.

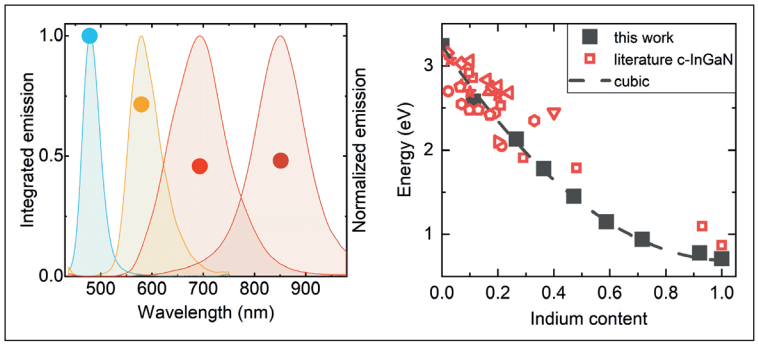
When we scrutinise the surfaces of our epistructures with atomic force microscopy, we identify atomic steps. We view this observation as a hallmark of the great quality of our c-GaN as a template for subsequent growth of c-InGaN.

growth conditions associated with this form of epitaxy include a larger temperature window. In particular, the potential for growth at lower temperatures may be superior for future CMOS-compatibility. Additional advantages of MBE include the virtual elimination of hexagonal inclusions, and the ability to incorporate more indium into the epilayer; the latter helps to shift emission to longer wavelengths.

Together with our partners from Phillips-University Marburg, our team at Justus-Liebig University Giessen has produced cubic III-nitride structures on 3C-SiC/silicon(001) substrates using plasma-assisted MBE. This platform for the growth of c-GaN has a lattice mismatch of 3.4 percent, currently the lowest of all commercially available substrates. The samples we have produced clearly exhibit superiority structural qualities compared with other growth techniques (see Figure 1) and substrates.

To assess the crystal quality of our material, we use X-ray diffraction rocking curves (ω-scans), considering values for the full-width at half-maximum. This metric provides a direct insight into the density of structural defects. What's more, this approach is extremely robust, providing reproducible measurements that are commonly reported in most publications featuring epitaxial growth.

Using this methodology, we have benchmarked our material against that of values in the literature for other cubic GaN layers grown on comparable 3C-SiC/silicon substrates. This exercise showcases the superiority of our process. It should be noted that there is a trend of a decrease in the width of the diffraction peak as the thickness of the epilayer increases. In general, this phenomenon is associated with the coalescence of threading dislocations.



➤ Figure 3. Normalised low-temperature photoluminescence spectra of c-$In_xGa_{1-x}N$ with values for x ranging from 0.1 to 0.5. The spectrally integrated intensity is shown as dots (left). Peak emission energy versus indium content, where black squares denote data points of this work and red symbols refer to the emission energies of bulk c-$In_xGa_{1-x}N$ (right).

Another important characteristic associated with epitaxial growth is the roughness of the film – it must be minimised to ensure high-quality growth of multi-layered heterostructures. Following optimisation, we are able to produce c-GaN layers that feature very smooth surfaces. When we scrutinise the surfaces of our epistructures with atomic force microscopy, we identify atomic steps (see the right-hand panel of Figure 1). We view this observation as a hallmark of the great quality of our c-GaN as a template for subsequent growth of c-InGaN.

Spanning the spectrum

It is challenging to grow metastable cubic $In_xGa_{1-x}N$ with good epitaxial quality, due primarily to differences in lattice constant, and the need for a significant difference in growth temperatures for the two binary compounds. Consequently, there are few reports of $In_xGa_{1-x}N$ alloys with an indium content of more than 0.3. Note that our search in the literature also uncovered publications that report spinodal decomposition for InGaN with intermediate indium contents.

Against this backdrop we have had considerable success, demonstrating the growth of metastable, phase-pure cubic InGaN layers across the entire composition range. By being able to produce all compositions of InGaN, from InN through to GaN, we are able to continuously tune the emission energy from 0.7 eV to 3.2 eV. To span this domain, we carefully adjust the relevant growth parameters while maintaining successful strain management.

Following the growth of our range of InGaN thin-film samples, we evaluated their composition, phase purity, and degree of strain relaxation with asymmetric reciprocal space maps. Ultimately, these maps uncover the relationship between the amount of indium incorporated in an epilayer and its residual strain. The latter strongly influences the alloys' miscibility and, thus, the impact on the optical properties.

It should be noted that substrate-induced strain leads to slight differences in the in-plane and out-of-plane lattice constants. Our reciprocal space maps allow us to determine all lattice constants

and consequently quantify the residual strain of the $In_xGa_{1-x}N$ layers. We find that all c-$In_xGa_{1-x}N$ layers grown on c-GaN are partially strained. This is a particularly important observation, because theoretical calculations predict enhanced miscibility, due to the suppression of spinodal decomposition in strained layers. We have observed that uniaxial strain is highest for intermediate indium compositions. This strain counteracts spinodal decomposition and is thus responsible for the full miscibility found in our c-$In_xGa_{1-x}N$ layers.

We have measured the photoluminescence of our samples at cryogenic temperatures (see Figure 3). Spectra for compositions with an indium content ranging from $In_{0.11}Ga_{0.89}N$ to $In_{0.5}Ga_{0.5}N$ are broad, with a single peak. Notably, the spectrally integrated emission intensity only quenches by a factor of two across the complete visible range – this is much less than that observed for currently established technologies.

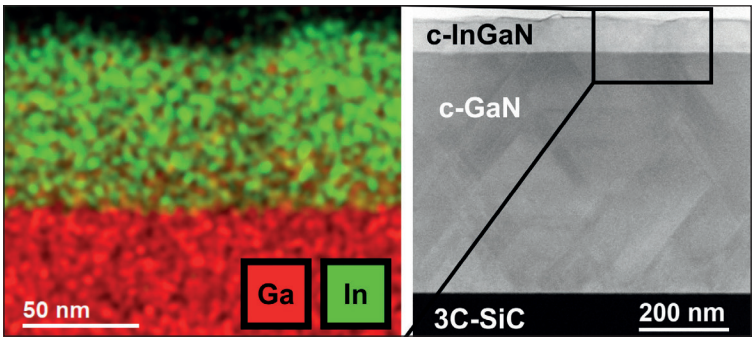
As we are able to produce alloys of c-InGaN across the whole composition range, we have the opportunity to span an emission range from below 400 nm to beyond 1.55 μm. All our samples stretching over this domain produce photoluminescence, and we find a bowing of the emission energy with indium content. These results are a rarity, given that reports associated with InGaN with a high indium content are few and far between. In general, either the materials are not realised – potentially due to presumed spinodal decomposition – or reports are limited to structural properties, with no emission data provided.

Confirmation of the high structural quality of our layers comes from transmission electron microscopy. One example of this, shown in Figure 4, is a characteristic image of a c-GaN/c-$In_{0.47}Ga_{0.53}N$ sample. According to energy-dispersive X-ray spectrometry data, also shown in Figure 4, there is no evidence of any spinodal decomposition.

Remaining challenges

Significantly threatening the performance of optoelectronic devices are extended defects, such as stacking faults. That's a concern for us, as there are numerous stacking faults in our c-$In_xGa_{1-x}N$ on c-GaN samples, according to defect-sensitive low-angle annular dark-field scanning transmission electron microscopy.

However, this situation may not be as concerning as it first appears. The majority of stacking faults in our c-$In_xGa_{1-x}N$ layer originate in the c-GaN layer, forming at the substrate interfaces during the nucleation of GaN on 3C-SiC. If these faults are not annihilated, they will penetrate the $In_xGa_{1-x}N$/GaN interface and propagate through the entire epitaxial layer. To reduce the number of stacking faults in c-GaN, one can incorporate a thin c-AlN buffer. Its addition drives down the concentration of stacking faults in the c-$In_xGa_{1-x}N$ layer.



➤ Figure 4. Characteristic energy-dispersive X-ray spectrometry (left) and scanning transmission electron microscopy (right) of a c-$In_{0.47}Ga_{0.53}N$ sample. The cross section of energy-dispersive X-ray spectrometry shows a very homogeneous distribution of the elements gallium (red) and indium (green). This is a noteworthy finding, as a sample with this indium content lies at the heart of the often literature-perceived miscibility gap.

The progress that we have made provides a solid foundation for further development of cubic nitride technology. While we have made much progress, more is needed, including improvement to material quality. Such efforts must include the development of successful doping strategies and high-quality quantum structures, goals that will demand optimised growth conditions and possibly the use of alternative substrate technologies. The latter may tackle challenges related to anti-phase domains, which originate from the interface between the group IV material and the cubic nitrides.

While microLEDs for AR and MR are showing much promise, they are struggling to make significant breakthroughs. Cubic GaN can be game changer. Its growth is not trivial, but much can be accomplished with MBE.

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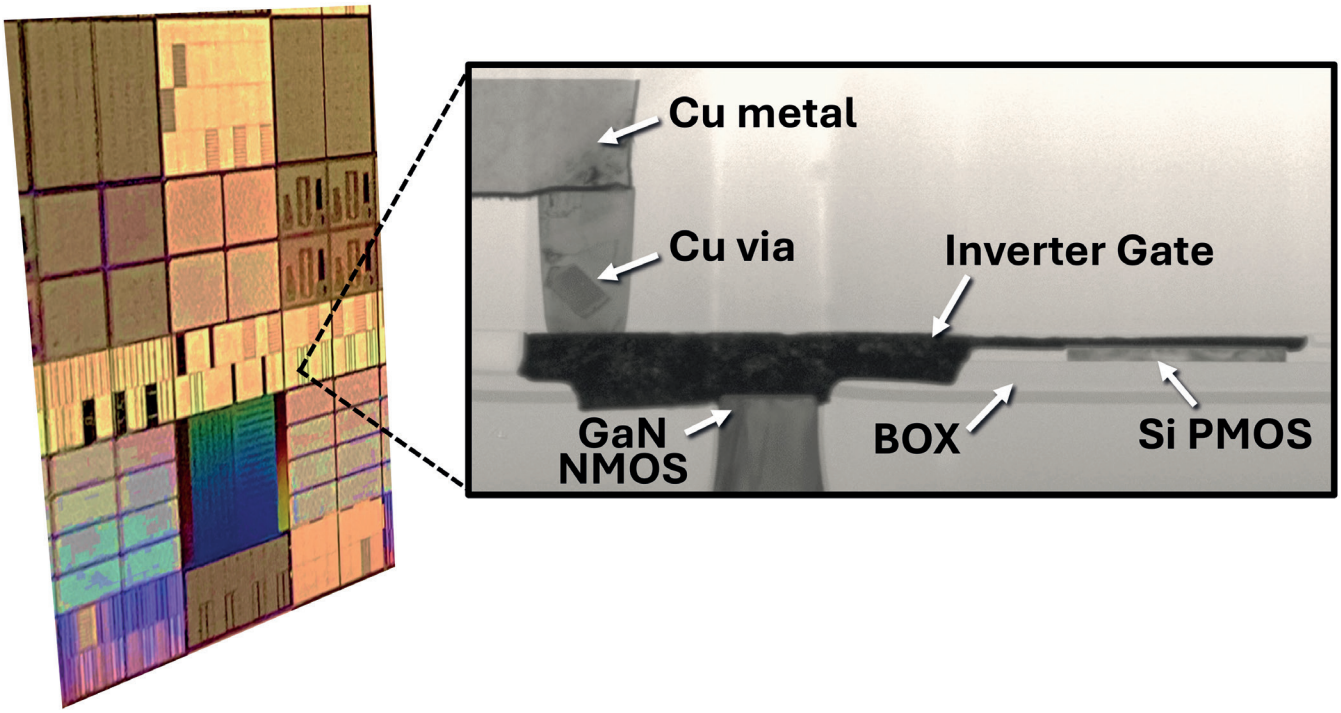


Combining a CMOS driver and a GaN power switch on 300 mm silicon

Intel's DrGaN technology, involving the monolithic integration of GaN and silicon CMOS on 300 mm wafers, will support power delivery in tomorrow's data infrastructure and communication networks

BY HAN WUI THEN FROM INTEL CORPORATION

THE NUMBER of power-hungry applications involving massive computation is on the rise, due to growth in datacenters, AI, wafer-scale compute, supercomputers and 5G/6G networks. Due to this, there is a need for the ICs that power these applications to combine a superior level of performance with greater energy efficiency and higher densities.

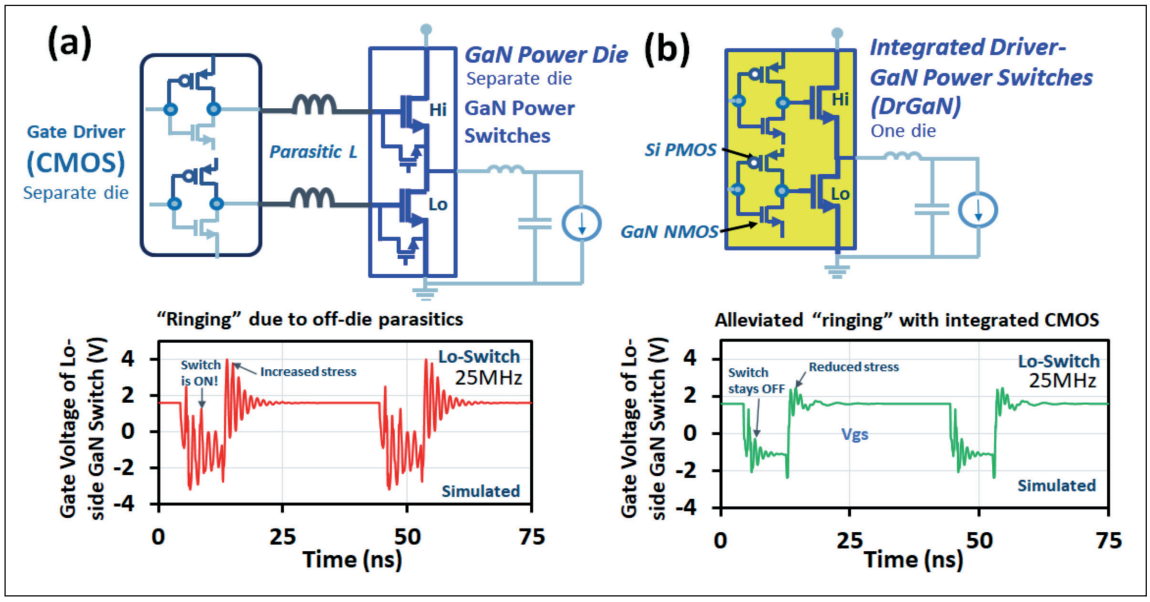
Our team at Intel Technology Research has anticipated these trends and has already devoted many years to addressing them. Back in 2019 we developed the industry's first enhancement-mode (E-mode) GaN transistor, enabled by high-κ dielectric metal gate technology; and we pioneered monolithic three-dimensional stacking integration of GaN and silicon transistor technology, all using 300 mm silicon wafers. During these efforts, we pursued the use of GaN because this high-mobility wide-bandgap semiconductor can operate at high frequencies and high power densities. These assets make this particular technology the best-in-class for power delivery and RF applications. We have focused on combining the advantages of GaN and silicon CMOS on a single chip to realise best-in-class performance, high efficiency and high density (small form-factor), as well as to integrate functionalities beyond what is possible with an *n*-channel only GaN technology.

Recently, we have taken our research a step further, employing an improved version of this process. At the most recent *International Electron Devices Meeting*, held last December in San Francisco, we unveiled what we refer to as 'DrGaN': it is a large-scale integrated CMOS driver-GaN power switch technology, realised on a 300 mm GaN-on-silicon wafer.

A single die solution

Our DrGaN technology breaks new ground. It is the first time that a GaN power transistor technology has been enhanced with an integrated CMOS driver on the same die. In comparison, other state-of-the-art GaN technologies of today employ a separate CMOS driver die that accompanies a GaN die, with the driver signal from the CMOS die routed through the package to the GaN die. This routing through the package incurs parasitic inductance

➤ Above. Intel's CMOS DrGaN Technology



➤ Figure 1. (a) A typical state-of-the-art solution involves a co-packaged two-die implementation: a separate CMOS driver die and power GaN die, where the driver signal from the CMOS die is routed through the package (represented by parasitic inductance, L) to the power GaN die. One downside of this approach is that it causes extreme ringing, visible in the simulation (inset). (b) A new approach facilitated by DrGaN, with a fully integrated CMOS driver on the power GaN die, enables a low-inductance path from the CMOS driver output to the GaN power switches. This technology suppresses the large ringing in (a).

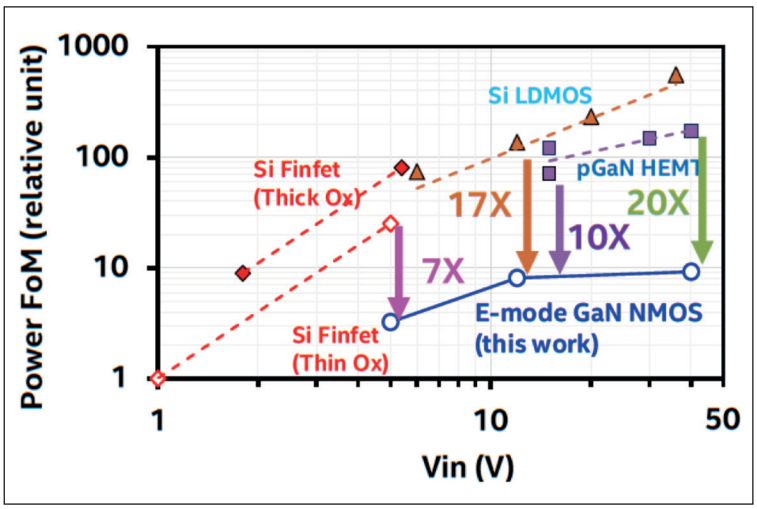
(see Figure 1(a)), which limits performance, with extreme 'ringing' at high switching speeds (this is visible in the simulation trace, shown in the inset of Figure 1(a)).

This ringing is detrimental, limiting the switching speed and the performance, in terms of the conversion efficiency. Due to this ringing, it's not possible to exploit a key advantage of the GaN transistor, which can switch far faster than its silicon sibling, evidenced by a figure-of-merit around 10-20 times higher (see Figure 2).

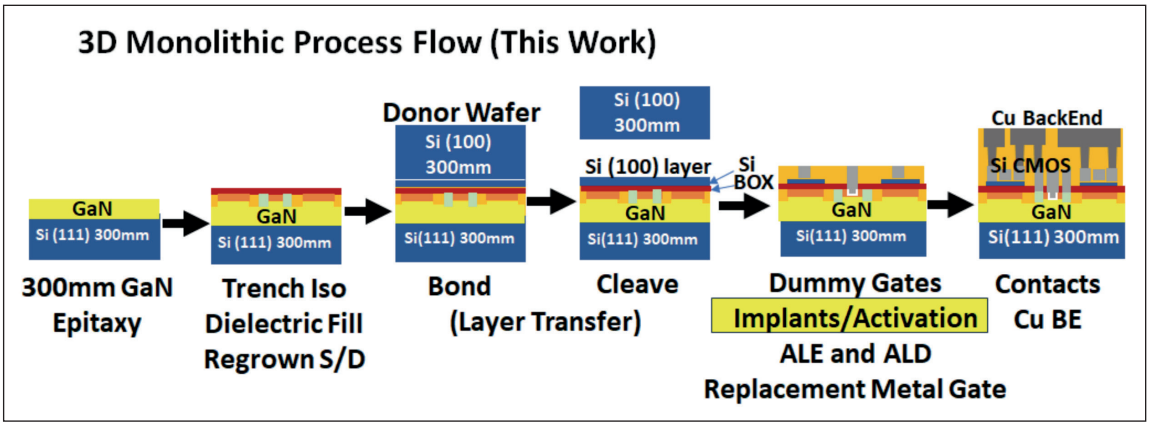
In addition, pairing a GaN die with a CMOS die leads to voltage 'overshoot'. Two issues result from this: an increase in the stress subjected to both the CMOS and GaN transistors; and inadvertent activation of the GaN power switch during the off-interval.

There is no doubt that a two-die solution fails to realise the full potential of the figure-of-merit gains offered by GaN. Overcoming this limitation is our DrGaN technology. By offering a fully integrated CMOS driver on the GaN die, our approach enables the realisation of a low-inductance path from the driver output to the GaN power gate, thereby suppressing the substantial ringing. The upshot is higher frequency operation, alongside a higher efficiency and improved reliability. The higher switching frequencies are cherished, as they open the door to smaller passives, such as smaller inductors. Shrinking the size of the power delivery unit follows, enabling higher power densities – that is, power delivery occupies less space-per-unit-power delivered, while maintaining high performance. Note that what we have just described is an instance of Moore's law in action for the power delivery solutions provided by DrGaN technology.

Our company has a long and strong track record in driver and MOSFET integration. Back in 2004 we introduced 'DrMOS' – driver and MOSFET integration for the silicon MOSFET. Our motivation for this breakthrough came from the need to keep pace with increasing microprocessor power density



➤ Figure 2. Benchmarking the power figure-of-merit ($R_{ON}xQ_{GG}$) of the GaN transistor of this work shows: a performance that's around a 20-fold better than the *p*GaN HEMT and around a 30-fold better than silicon LDMOS at 40 V; a 10-17-fold better performance than silicon LDMOS and a *p*GaN HEMT at 12-15 V, and 7-fold better performance than a silicon finFET at 5 V.



➤ Figure 3. The process flow used for DrGaN technology, which involves three-dimensional monolithic integration of GaN and silicon CMOS by layer transfer on 300 mm silicon wafers.

and efficiency demands associated with the leading PCs and laptops of that era. Since then, DrMOS has become the gold standard for point-of-load power delivery solutions for CPUs and GPUs.

One of the trailblazers for GaN is Navitas Semiconductor, which introduced integrated enhancement-depletion (E-D) mode *n*-channel drivers for high-voltage GaN power ICs. This particular architecture has been adopted because standard GaN processes cannot produce *p*-channel or CMOS devices.

The E-D mode driver is suitable for high-voltage scenarios. However, this form of driver is far too leaky – and thus not efficient enough – for lower voltage, point-of-load applications, such as those below 48 V. Turning to CMOS addresses this, while enabling efficient, high-density integration of other functionalities, including control logic and telemetry circuitries, such as current and temperature sensors. It is a broad range of features, challenging to realise with a standard GaN *n*-channel only process.

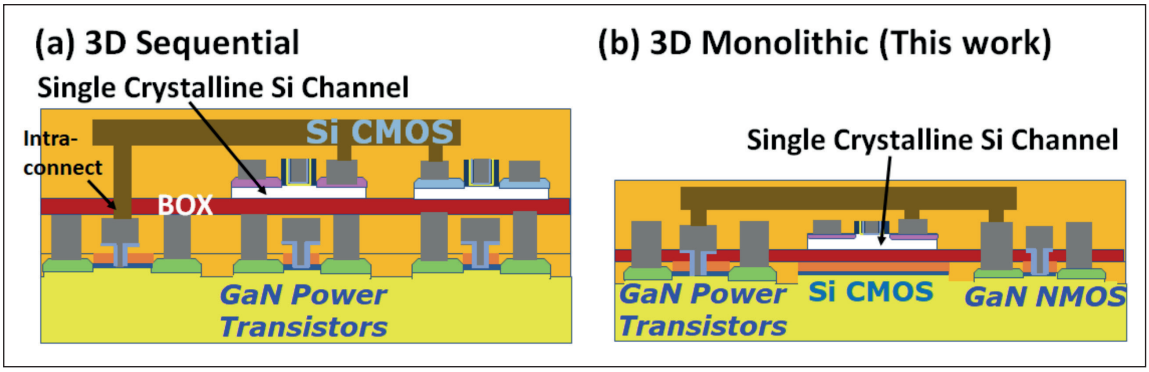
With our DrGaN technology, we accomplish the monolithic integration of GaN and silicon CMOS with a new process flow (see Figure 3), using a technique called layer transfer. We begin by bonding a donor silicon wafer to a GaN wafer. Upon separation, the silicon donor wafer cleaves along a weakened crystal plane throughout the wafer, to leave a thin layer of silicon channel material bonded onto the GaN wafer.

Our latest approach involves introducing implants and high-temperature activation steps, for the fabrication of the silicon CMOS transistors, prior to formation of the high-κ gate dielectric of the GaN transistors. From there onwards, we only perform low-temperature steps. That's critical, because high temperatures threaten to degrade the quality and reliability of the high-κ gate dielectric used for GaN transistors. By arranging our process flow in such a manner, this truly gate-last process overcomes a major hurdle in three-dimensional monolithic integration of GaN NMOS and silicon CMOS transistors.

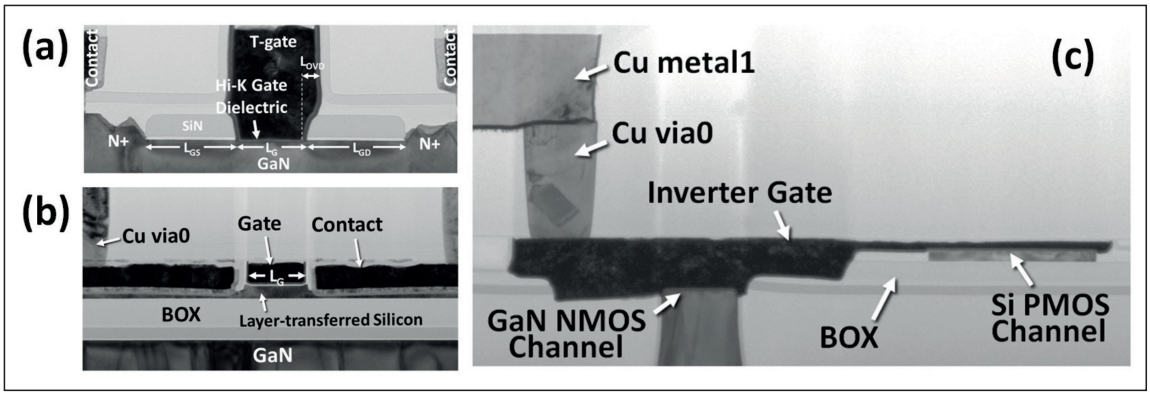
Proven superiority

The benefits of our latest process are seen in the measurements of silicon PMOS transistors fabricated by both approaches (see Figure 4). Previously, PMOS transistors were fabricated sequential, only after the GaN transistors were completed. This sequence exposed the gate dielectric of the GaN transistor to the high-temperature steps of silicon transistor processing.

Another downside of our previous approach is that this sequential process flow employed intra-connects to establish electrical connectivity



➤ Figure 4. (a) Intel's prior work involved the three-dimensional sequential monolithic integration of GaN and silicon CMOS by a layer transfer process, with silicon PMOS/NMOS transistors fabricated after completing fabrication of the GaN transistors. (b) For Intel's latest work, DrGaN technology, GaN and silicon PMOS/NMOS transistors are fabricated in such a way that the high-temperature activation steps are completed before the deposition of the gate dielectric of the GaN transistors.



➤ Figure 5. Transmission electron microscopy of the completed (a) GaN transistor, (b) silicon PMOS transistor and (c) CMOS inverter, fabricated in this process on a 300 mm wafer.

between the silicon and GaN transistors. As well as necessitating additional fabrication steps and masks, these intra-connects added path resistance when accessing the underlying GaN transistors. In contrast, our latest process for producing GaN and silicon CMOS transistors leads to a shared backend copper interconnect stack, eliminating the need for additional intra-connects and masks.

To inspect our completed devices – the GaN transistor, silicon PMOS transistor and hybrid GaN/silicon CMOS inverter – we have used a transmission electron microscope (see Figure 5). These devices, fabricated with our latest process on a 300 mm wafer, are used to construct the DrGaN.

We have undertaken a number of electrical measurements on our devices. Transfer current-voltage (I-V) characteristics for a typical GaN transistor with a channel length of 90 nm are shown in Figure 6 (a). Strengths of this device include an excellent on-off ratio of around 10^{10}, a low on-resistance of 422 Ω μm, a high drain-current drive of 1.2 mA μm^{-1}, and gate leakage below 1 pA μm^{-1}. Equally impressive are the I-V characteristics of our silicon PMOS transistor, which has a channel length of 180 nm (see Figure 6(b)). In this case the on-off ratio is around 10^6, the on-resistance 1780 Ω μm, the drain current drive 0.43 mA μm^{-1}, and the gate leakage around 1 pA μm^{-1}. Note that these are some of the best numbers ever reported for GaN and silicon PMOS transistors at comparable channel lengths. In particular, the GaN transistors show a best-in-class figure-of-merit for the reciprocal of the product of on-resistance and gate charge of 0.59 $m\Omega^{-1}$ nC^{-1}, measured from the shortest channel length of 30 nm (see Figure 7).

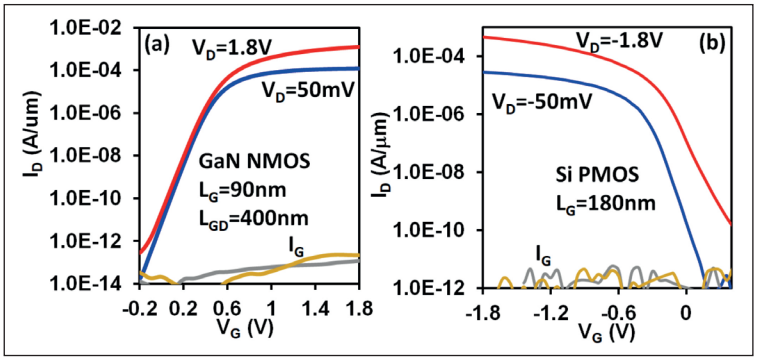
Through judicious selection of gate-to-drain separation, which can be varied from 200 nm to 1000 nm, we can obtain a breakdown voltage of up to around 60 V for our GaN transistor (see Figure 7). This enables us to target a range of use cases and application voltages.

Our DrGaN technology enables the construction of a large-scale IC from a massive array of repeated unit cells. Each of these cells, 40 μm by 10 μm in size, consists of four blocks: a silicon PMOS driver block, a GaN NMOS driver block, and two symmetrical GaN power switch blocks. The layout for these cells is outlined in Figure 8, along with a circuit schematic that illustrates the electrical connections between the silicon PMOS, GaN NMOS and GaN power switch transistors.

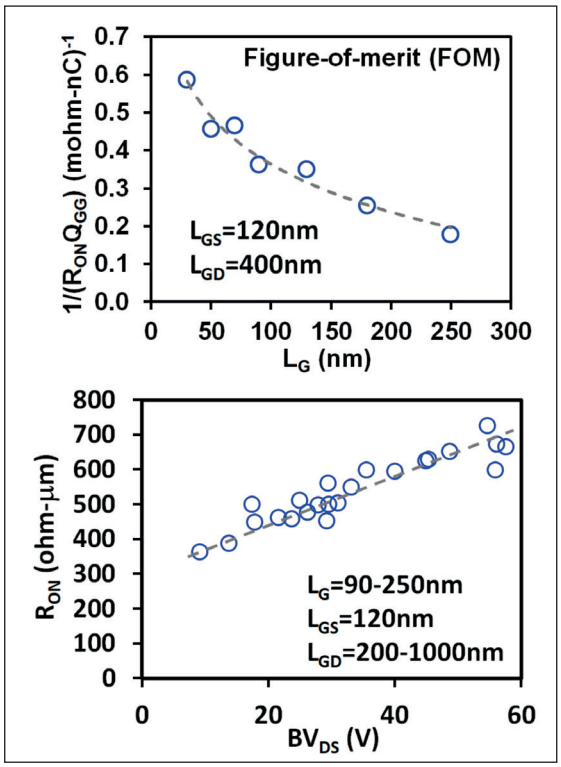
The DrGaN unit cell is arrayed over an area of 0.8 mm^2 to realise a desired total width of 421.1 mm for the GaN power switch, 49.54 mm for the GaN NMOS (driver) and 27.19 mm for the silicon PMOS (driver). The aggregate total width of all the transistors is 497.83 mm.

To demonstrate the full functionality of this 497.83 mm wide DrGaN, we have measured its steady-state electrical characteristics. To record the transfer characteristics of the GaN power switch S, which has a total width of 421.1 mm, in DrGaN, we use a probe to apply a bias voltage to the gate node of this switch (see Figure 9(a)). For this GaN power switch we have measured an on-resistance of 1 mΩ and determined leakage characteristics, with the switch turned off by applying a bias voltage of either (c) 0 V directly at the gate node of S; or (d) 1.8 V at the gate driver node of P and Q. Drain and gate leakage currents are well below 0.1 mA for the 421.1 mm-wide power switch. Also shown in Figure 9 are the transfer characteristics of silicon PMOS, P (width of 27.19 mm) (e) and the leakage characteristics of GaN NMOS, Q (width of 49.54 mm), in the gate driver (f).

We have also assessed the inverting characteristics



➤ Figure 6. The current-voltage (I-V) characteristics of (a) GaN transistor, and a (b) silicon PMOS transistor produced by the DrGaN process.



➤ Figure 7. (a) The figure-of-merit $1/(R_{ON}Q_{GG})$ for the GaN transistors produced by the DrGaN process, for channel lengths, L_G, ranging from 30 nm to 250 nm. (b) The on-resistance, R_{ON}, and breakdown voltage, BV_{DS}, for GaN transistors produced by this process. Gate-to-drain lengths, L_{GD}, are between 200 nm and 1000 nm.

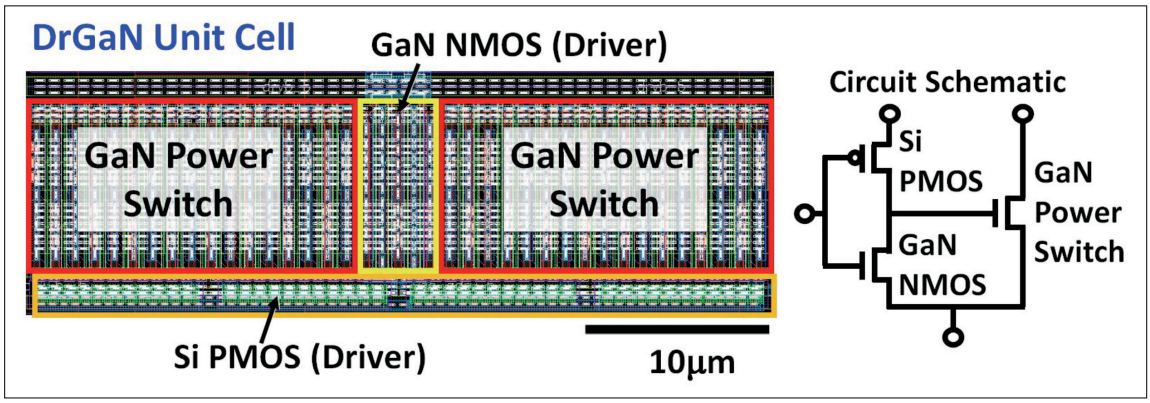
of the combined GaN-silicon CMOS driver (P and Q). Figure 10 shows the steady-state transfer characteristics with DrGaN. Modulation of the GaN power switch, S, is driven by the integrated GaN-silicon CMOS driver (P and Q).

This final measurement completes full functionality testing of our DrGaN technology, which has multiple merits. We view our realisation of a large-scale, 497.83 mm-wide DrGaN is an important milestone towards demonstrating the viability of our 300 mm GaN-on-silicon process with three-dimensional monolithically integrated GaN and silicon CMOS, brought together by layer transfer. Our efforts break new ground, showing for the first time that this process can produce large-scale integrated circuits comprising GaN and silicon CMOS transistors on the same chip.

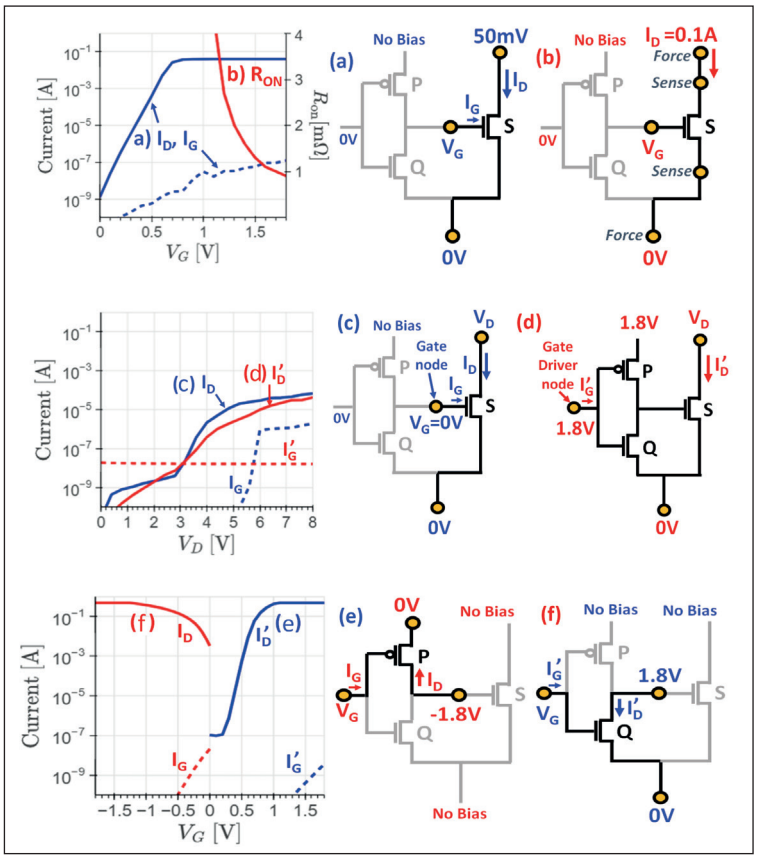
Our development of DrGaN demonstrates that the monolithic three-dimensional integration of GaN NMOS and silicon PMOS transistors is a powerful way to integrate two dissimilar best-in-class semiconductor technologies on the same silicon and deliver optimal performance, improved density, and more functionalities. Our accomplishments include the industry's first CMOS DrGaN technology fabricated in 300 mm GaN-on-silicon technology. Through the use of enhancement-mode high-κ dielectric GaN MOSHEMT technology for the GaN transistor, our DrGaN ICs set new benchmarks for performance and leakage. Another significant advance is the new improved truly gate-last process flow, resolving a major hurdle in three-dimensional monolithic integration of GaN NMOS and silicon CMOS transistors.

Thanks to our efforts, there has been a significant advance in 300 mm GaN-on-silicon technology. But that's far from all that the demonstration of DrGaN has accomplished. This technology holds the key to tomorrow's efficient, highly integrated, high-density point-of-load power delivery solutions for future high-performance compute in datacenters, AI and 5G/6G networks. DrGaN is clearly destined to deliver many great things.

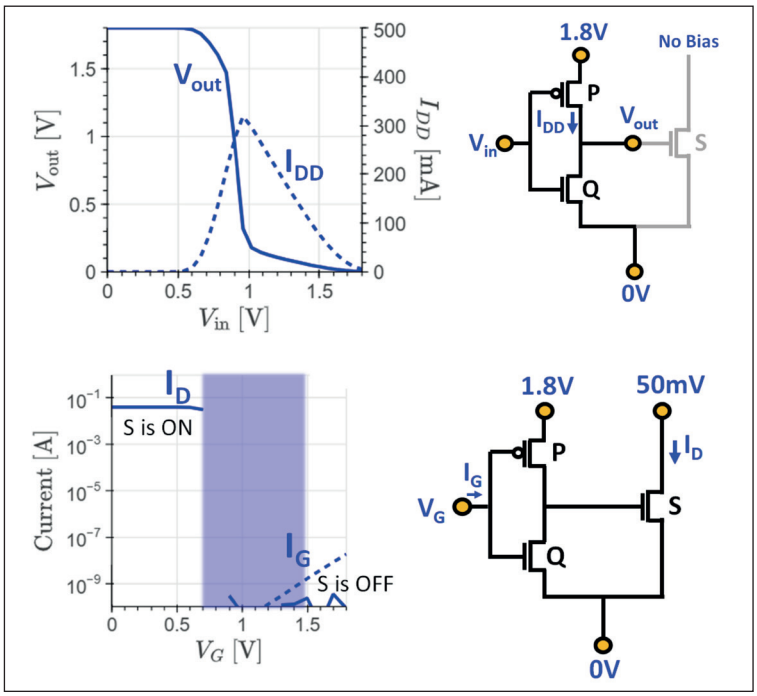
The author, Han Wui Then, would like to thank team members and contributors: M. Radosavljevic, S. Bader, A. Zubair, H. Vora, N. Nair, P. Koirala, M. Beumer, P. Nordeen, A. Vyatskikh, T. Hoff, J. Peck, R. Nahm, T. Michaelos, E. Khora, R. Jordan, C. Hoffman, N. Franco, A. Oni, S. Beach, D. Garg, D. Frolov, A. Latorre-rey, A. Mitaenko, J. Rangaswamy, S. Sarkar, S. Ahmed, V. Rayappa, H. Chiu, A. Hubert, S. Brophy, N. Arefin, N. Desai, H. Krishnamurthy, J. Yu, K. Ravichandran, and P. Fischer.



➤ Figure 8. The layout of a 40 μm by 10 μm DrGaN unit cell consisting of silicon PMOS and GaN NMOS driver blocks, and two GaN power switch transistor blocks. The inset shows the circuit schematic of the electrical connections between the silicon PMOS, GaN NMOS and GaN power switch transistors. In the driver block, the silicon PMOS has a channel length, L_G, of 180 nm, and a total width per unit cell of 19.76 μm, while the GaN NMOS has the same channel length of 180 nm and total width-per-unit-cell of 36 μm. The GaN power switch transistors have a similar channel length of 180 nm, but a larger total width-per-unit-cell of 306 μm, and a longer gate-to-drain length, L_{GD}, of 400 nm, in order to withstand a higher operating voltage.



➤ Figure 9. (Top) the transfer characteristics of the GaN power switch S with a total width of 421.1 mm in DrGaN, demonstrating transistor operation. The normalized R_{DSON} is 0.8 mΩ mm^2. (Middle) The leakage characteristics, I_D-I_G-V_D and I_D'-I_G'-V_D of the GaN power switch S in DrGaN, in the off-state accomplished by either applying a bias voltage, V_G, of (c) 0 V directly at the gate node of S; or (d) 1.8 V at the gate driver node of P and Q. (Bottom) The I-V transfer characteristics of the (e) silicon PMOS, P, and (f) GaN NMOS, Q, in the gate driver of DrGaN.



➤ Figure 10. (Top) Transfer characteristics, V_{out}-V_{in}, of the GaN-silicon CMOS driver, P and Q, in DrGaN technology. (Bottom) The steady-state transfer characteristics of DrGaN. The switching of the GaN power switch, S, is driven by the integrated GaN-silicon CMOS driver (P and Q). Turning on involves a driver pull-up to a V_G rail of 1.8 V, and turning off involves a driver pull-down to a V_G rail of 0 V.

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Raising the bar for power amplification

The performance of GaN-based amplifiers operating in the X- and Ka-bands record new highs through the introduction of an AlN buffer

BY YANG LING, HAO LU, BIN HOU, FUCHUN JIA, XIAOHUA MA AND YUE HAO FROM XIDIAN UNIVERSITY

IN COMMUNICATION infrastructure and radar systems, there is much demand for more powerful power amplifiers (PAs). By increasing the strength of signal through greater amplification, more powerful PAs can open the door to improving the design and the capability of wireless networks, and the resolution and reach of radar.

A compelling approach to increasing the power of the PA is to enhance the buffer design. One option is to switch to compensation doping in the GaN buffer – this boosts the resistance of this layer, leading to a reduction in RF insertion loss, and in turn a hike in the operating voltage of the GaN device.

However, while this approach sounds easy, success is far from trivial. Our team from Xidian University initially tried to succeed in this manner, with efforts beginning by exploring compensation doping in GaN buffers. Through the integration of deep-level impurities such as either iron or carbon, we aimed to significantly increase the buffer's resistivity, and ultimately the breakdown and power characteristics of the PA. But we came up against a number of hurdles, including the unintended introduction of carbon-related buffer traps and an iron-related doping tail effect – both threaten to degrade device performance. In addition, we found our quest for optimal material quality to be hampered by limitations in thermal management, originating from the thickness of the doped GaN buffer layer.

In response to these challenges, we switched to an AlN buffer. It's a formidable solution: boasting a high thermal conductivity and an ultra-wide bandgap, this form of buffer has emerged as a beacon

of innovation, poised to redefine the standards of PA design. We have deployed this buffer as the foundation for recording-breaking levels of amplification in the X- and Ka-bands.

Inserting AlN buffers

Fabrication of these devices began by loading a 75 mm semi-insulated SiC substrate into an MOCVD reactor and growing a ultrathin AlN buffer layer at high-temperature, followed by an unintentionally doped GaN channel layer, an AlN insert layer, and a $Al_{0.25}Ga_{0.75}N$ barrier layer (see Figure 1).

To uncover the doping profiles in this design, we scrutinised our epitaxial structure with secondary ion mass spectrometry (see Figure 2). This technique revealed a sharp profile for the iron concentration at the interface between the undoped GaN and AlN, indicating the elimination of the iron-doping tail effect, thanks to incorporation of the AlN buffer.

We have investigated the interface between the SiC substrate and AlN buffer with high-angle dark-field scanning transmission electron microscopy and energy-dispersive X-ray spectrometry (see Figures 2 and 3). This pair of techniques revealed a continuous sharp boundary, as well as no element inter-diffusion between the AlN buffer and the substrate.

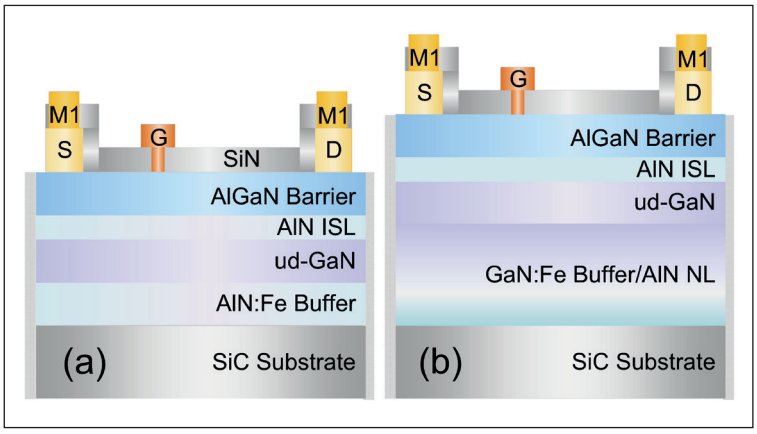
To produce GaN-based HEMTs with two types of buffer layer structures from our epiwafers, we began by adding an alloyed source/drain ohmic contact, prior to deposition of a 120 nm SiN_x passivation layer. Subsequent electrical isolation resulted from planar nitrogen-ion implantation, followed by the removal of SiN_x passivation under the gate stem and the formation of Ni/Au gate electrodes for the Schottky contact.

Devices with two types of epitaxial heterostructure were produced using the same process flow and device geometry. These HEMTs have a 0.5 μm gate length and a 3.1 μm gate-drain spacing. We have also fabricated transistors for millimetre-wave applications – that's frequencies of more than 30 GHz – by scaling down the AlN buffer device using the same process platform to produce a HEMT with a 150 nm gate length.

Better breakdown

By switching from GaN to AlN, our buffer has a higher thermal conductivity that eradicates heat dissipation issues in this region of the device. The AlN buffer also improves channel conductivity and transport properties by eliminating the iron doping-tail effect.

These benefits of the AlN buffer are seen in our measurements of DC and small-signal characteristics. Thanks to a high field-effect mobility, we see higher values for the transconductance in our AlN buffer device, alongside superior values

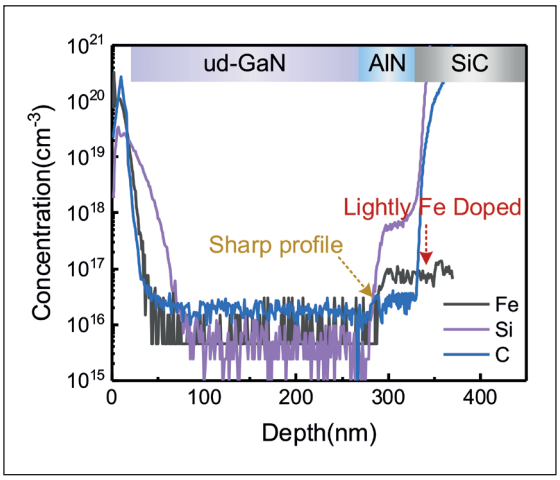


➤ Figure 1. Improvements in RF performance are realised by introducing an iron-doped AlN buffer (a). This design is superior to the conventional iron-doped GaN heterostructure (b). Note that these illustrations are not to scale.

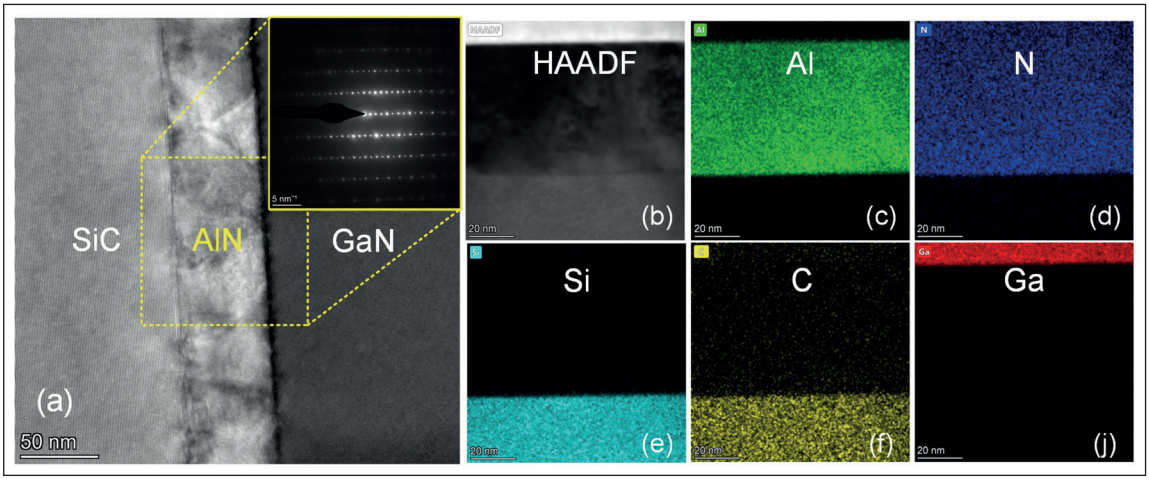
for the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}). These findings have been drawn from our studies of small-signal characteristics for devices with AlN and GaN buffers, operating under a drain-source voltage of 10 V.

We have recorded values for f_T and f_{max} of 29.1 GHz and 50.7 GHz, respectively, for our HEMTs with an AlN buffer. These devices, which have a breakdown voltage that is linearly related to the gate-drain spacing, have a breakdown voltage more than 100 V higher than that of variants with the conventional GaN buffer. According to plots of breakdown voltage as a function of source-drain distance, our devices have an average breakdown field of 0.87 MV cm^{-1}. We have also measured the double-pulsed current-voltage characteristics of HEMTs with an AlN buffer, and those with a GaN buffer. These plots show that the introduction of the AlN buffer effectively suppresses current collapse, and trims the current-collapse ratio by nearly 13.2 percent.

Encouraging results have also been obtained for our scaled-down device that's targeting the Ka-band. This 150 nm HEMT has a breakdown-field of 0.76 MV cm^{-1}, and values for f_T and f_{max} of 50 GHz



➤ Figure 2. Secondary ion mass spectrometry provides profiles of the iron, silicon and carbon elements in GaN/AlN/SiC hetero-structures.



➤ Figure 3. Transmission electron micrograph of the iron-doped AlN buffer structure.

and 145 GHz, respectively. Meanwhile, simulations suggest that the channel temperature is lower with an AlN buffer, than a GaN buffer, and RF loss is significantly reduced.

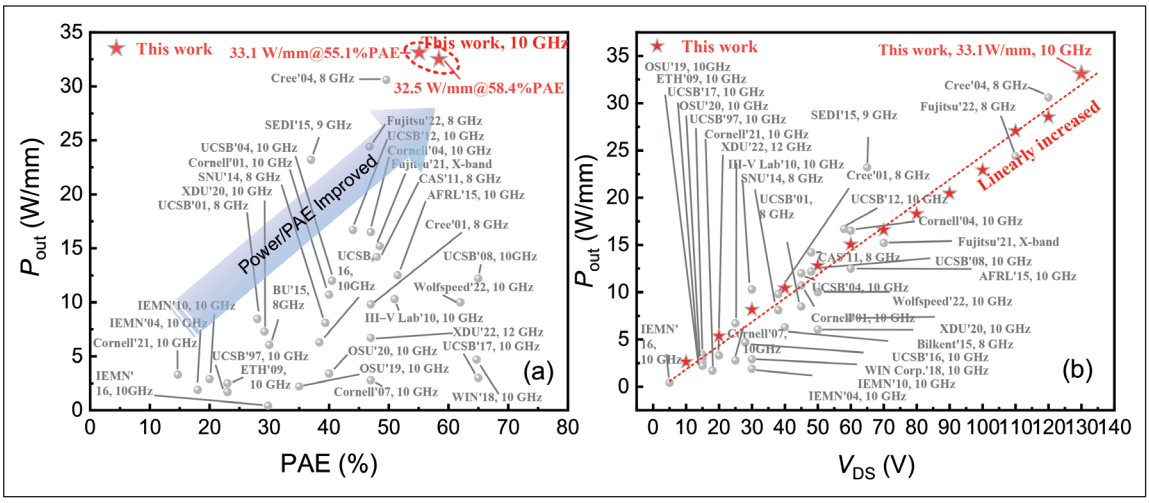
Record-breaking power densities

The X-band is renowned for electromagnetic waves with strong reflectivity and a short wavelength. Due to these traits, the X-band is widely used for wireless communication, as well as a number of other applications. For wireless links, the PA's power performance is crucial, as it directly affects the operating performance. The PA must deliver sufficient power to ensure that signals are transmitted effectively over long distances, while offering a high level of efficiency that enables minimal heat generation and power consumption. Amplifiers also need to provide good linearity, as this ensures signal integrity and minimises distortion.

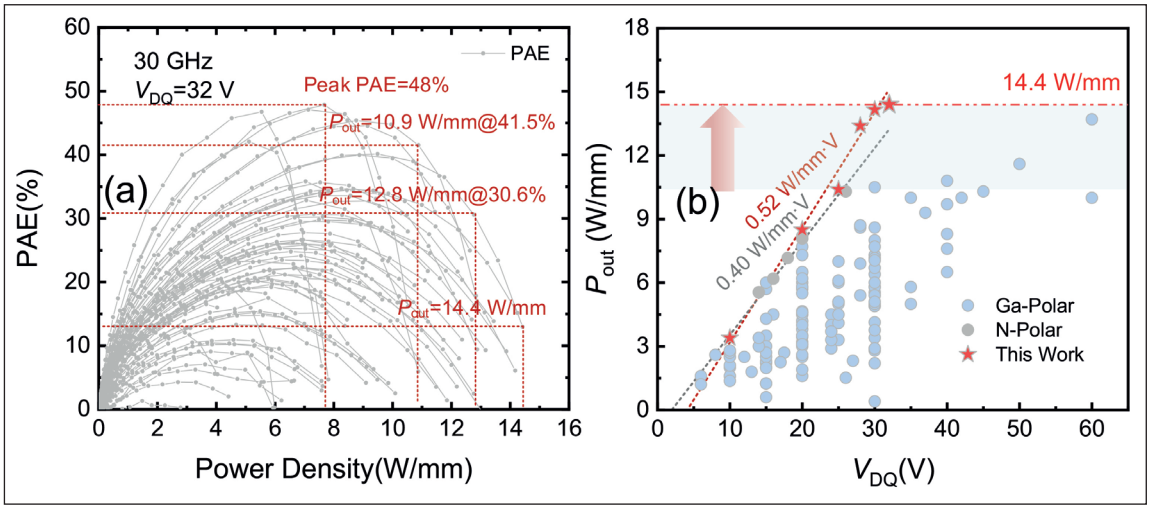
To perform large-signal power characterisation at 10 GHz in pulsed mode, we employed an active load-pull system. Operating in the X-band, our devices produced an output power of 33.1 W mm^{-1}, and under optimum output power tuning, a peak power-added efficiency of 55.1 percent. Meanwhile, under optimum power-added efficiency tuning, our HEMTs delivered a maximum power-added efficiency of 62.9 percent, realised at an output power density of 32.5 W mm^{-1}.

For PAs, the two key characteristics for benchmarking are the output power as a function of power-added efficiency, and the output power as a function of drain-source voltage. Using these criteria, we benchmarked our HEMTs against state-of-the-art results (see Figure 4). This exercise shows that our design achieves high efficiency at high output power density, and the output power of this portfolio of devices tends to increase linearly with increasing drain-source voltage, even within a wide drain voltage range, spanning 10 V to 130 V.

We have also studied our devices that amplify in the Ka-band, which ranges from 26.5 GHz to 40 GHz. This band is used for satellite communication, including high-speed satellite broadband, as well as ground wave tracking, collecting weather information and visible/infrared imaging. Compared with the X-band, wavelengths are shorter, enabling higher resolution – and there is the opportunity for broadcasting services to cover larger geographical areas. While operational power performance is vital for any amplifier, in higher frequency bands like the Ka-band, it is also crucial to handle amplified signals without introducing excessive noise or distortion. This implies the need for robust thermal management solutions and a low RF loss, to ensure the clarity and quality of the amplified signal.



➤ Figure 4. Comparison of X-band power results from various reports for (a) output power (P_{out}) versus power added efficiency (PAE); (b) P_{out} versus drain-source voltage (V_{DS}).



➤ Figure 5. (a) Active load-pull test results at Ka-band for the scaled-down HEMT. (b) Benchmark of millimetre-wave power performance from various reports for P_{out} versus V_{DS}.

Scaling our devices to a 150 nm gate length so that they operate in the Ka-band leads to a record power density of 14.4 W mm^{-1} and a maximum power-added efficiency of 48 percent. We benchmarked this device, considering output power as a function of the drain-source voltage. For this evaluation, we determined that for our devices the power-voltage ratio – a measure of the modulation ability of the drain-source voltage on the output power – is 0.52 W mm^{-1} V^{-1}. According to this metric, our devices even outperform N-polar GaN devices, with further gains promised by increasing the drain-source voltage and employing a strong-polarisation thin-barrier design in the Ga-polar material system. This shows that devices with the AlN buffer also have plenty of potential for millimetre-wave applications.

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Broadening the nitride palette with AlYN

AlYN provides a promising material for pioneering sustainable high-performance applications and green technologies

BY STEFANO LEONE, ISABEL STREICHER, PATRIK STRAŇÁK AND LUTZ KIRSTE FROM FRAUNHOFER IAF, FREIBURG,GERMANY

IN TODAY'S digitally connected society, characterised by the relentless demand for high-energy data computing that's needed to power artificial intelligence (AI) applications, one key question is this: What must be done to keep up with the pace? Reflecting on this at the recent World Economic Forum Annual Meeting in Davos, OpenAI's CEO, Sam Altman, issued a poignant warning, leaving no-one in any doubt that the future of AI hinges upon breakthroughs in energy efficiency, essential for accommodating the escalating demands for power consumption. Altman's cautionary note is resonating deeply within the tech community, sparking a critical dialogue on the need for innovation in energy-efficient computing.

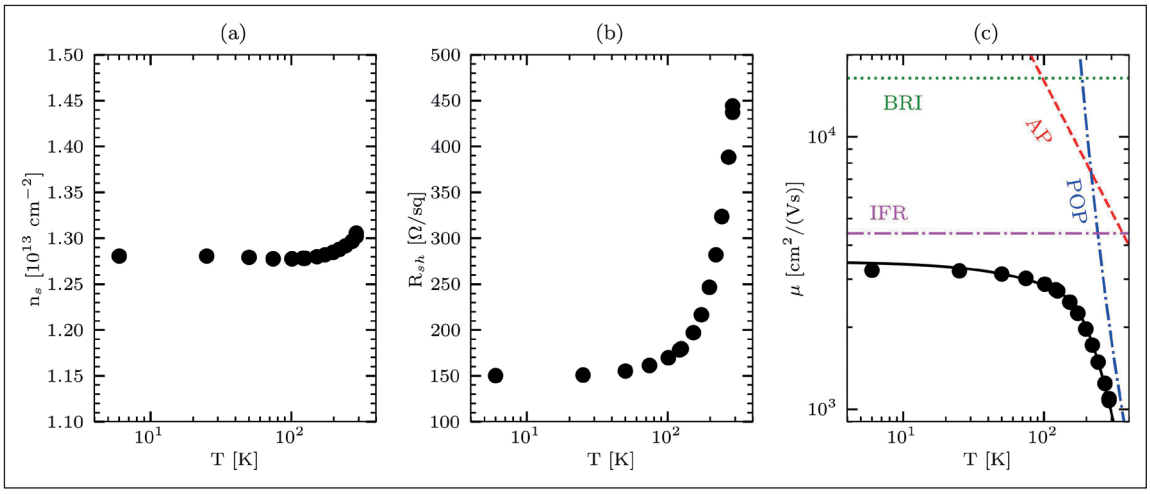
➤ Scientists Lutz Kirste, Isabel Streicher and Stefano Leone from Fraunhofer IAF, Freiburg, discuss on the stability of AlYN's wurtzite crystal structure and the challenges posed by cubic inclusions, highlighting ongoing efforts to overcome material hurdles and advance semiconductor technology.

A new way of thinking is needed to ensure success on this front. Traditionally, efforts have focused on increasing power capacity to meet burgeoning computational requirements. Now, though, there is a need to shift to optimising existing technologies for efficiency. This paradigm shift, promoting the value of sustainability, is particularly pertinent in compound semiconductor materials, where advances in materials science are already unlocking new possibilities for enhancing performance while minimising energy consumption.

One notable innovation in this regard is the development of AlYN, a novel nitride, by our team at the Fraunhofer Institute for Applied Solid State Physics IAF in Freiburg, Germany. Grown by MOCVD, AlYN holds immense promise as a key enabler in more efficient digital communication and energy-efficient computing.

We are not the only trailblazer of this nitride. Work by Zetian Mi's group at the University of Michigan has demonstrated that AlYN exhibits ferroelectric properties, akin to its counterpart, AlScN. This discovery opens up exciting avenues for exploring AlYN's potential in novel applications, including non-volatile memories.

Within the worldwide research community, efforts to explore the use of AlYN for fabricating HEMTs are ongoing. While these transistors are still to be realised, significant strides have been made in demonstrating the epitaxial heterostructure



➤ Figure 1. Temperature-dependent Hall measurement of the $Al_{1-x}Y_xN$/GaN heterostructure with a value for x of 0.082. (a) Electron density (n_s), (b) sheet resistance (R_{sh}) and (c) mobility (μ). Calculated background residual impurity scattering (BRI), interface roughness scattering (IFR), acoustic phonon scattering (AP) and polar optical phonon scattering (POP) limited mobilities are indicated.

necessary for their fabrication. Both MBE and MOCVD techniques have been employed to grow epitaxial AlYN/GaN heterostructures, showcasing the feasibility of integrating AlYN into HEMTs. It should be noted that while AlYN's ferroelectric nature provides potential for non-volatile memory, there has been no conclusive evidence of its functionality in this capacity. Nevertheless, ongoing research endeavours are diligently exploring the suitability of this novel nitride for non-volatile memory applications, propelled by its tantalising material properties and potential benefits for energy-efficient computing.

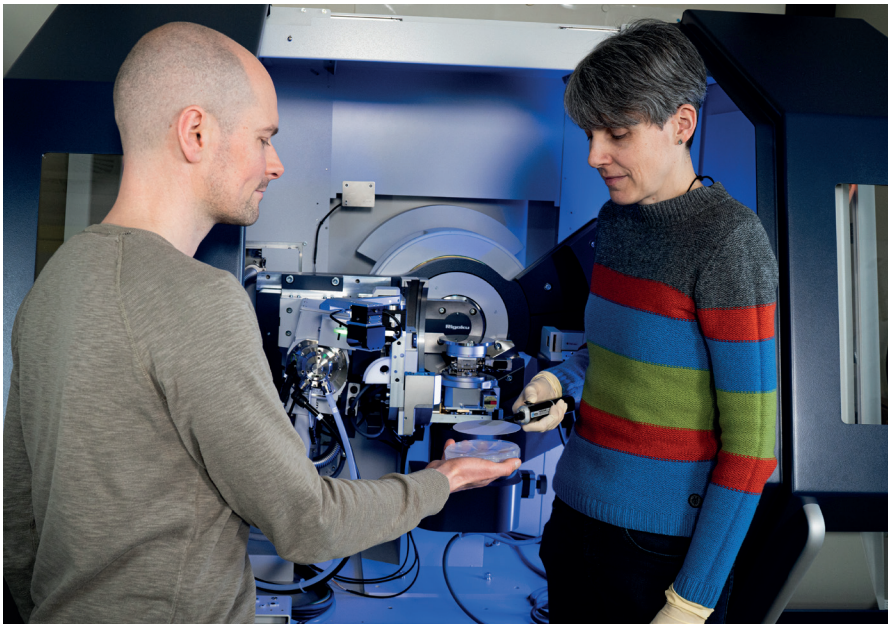
Unveiling the potential of AlYN

Back in 2019, we realised a significant milestone, cultivating the first AlScN by MOCVD. This provided a pivotal moment in our journey to producing AlScN, which is blessed with exceptional physical properties that could revolutionise various sectors, from digital communication to power conversion. This nitride is renowned for its prowess in enhancing the performance of GaN-based HEMTs, an appeal that's captivating the interest of researchers worldwide.

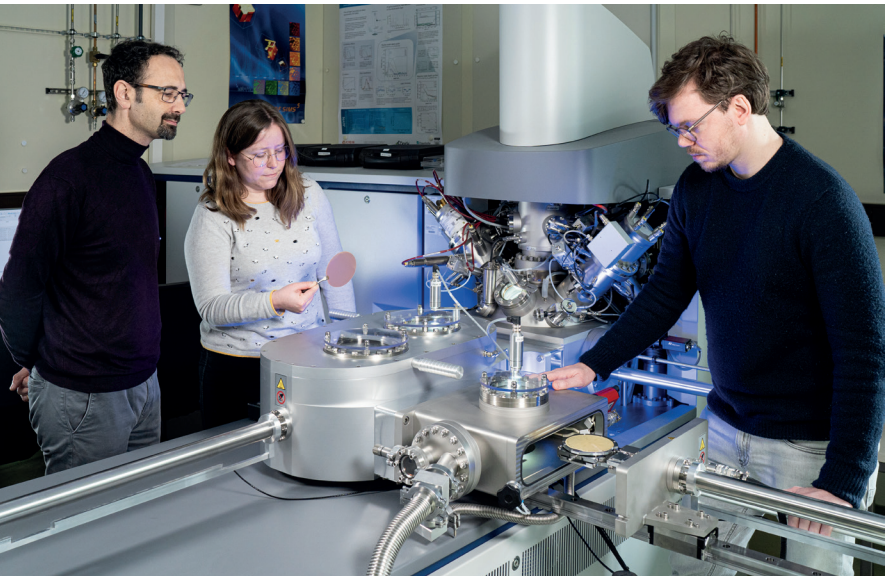
Surrounded by the fervour associated with AlScN, last year many delegates experienced an unexpected twist at the ICNS conference in Fukuoka, Japan. Sandwiched between a plethora of discussions centred on AlScN, our team had the chance to present not on AlScN, but AlYN. While some of the researchers at the conference might have thought that there had been a typographical error, it was actually the culmination of our pioneering efforts in semiconductor alloys – AlYN had entered the spotlight.

The genesis of our fascination with AlYN traces back to 2019, following our success with AlScN. This rationale was multifaceted: AlYN, stable in the wurtzite phase with higher yttrium concentrations, boasts distinct advantages over its counterparts. Notably, AlYN demands a lower yttrium content than scandium to realise lattice-matching with GaN, enabling enhanced performance and reliability. This alignment with GaN may offer many benefits, including a superior HEMT durability and the alleviation of constraints in layer thickness, crucial for ferroelectric applications in non-volatile memories.

Promoting the direction of our research are discussions surrounding the scarcity of scandium.



➤ In the X-ray diffraction lab at Fraunhofer IAF, Freiburg, scientists Mario Prescher and Nadine Brückner meticulously analyse the crystallographic structure of AlYN layers, providing essential data for optimising material quality and understanding its relationship with underlying GaN layers.



The time-of-flight secondary ion mass spectrometry tool operated by Patrik Straňák provides invaluable insights into the composition of AlYN layers, allowing analysis of interfaces and the detection of impurities.

This encouraged us to pivot our attention to yttrium, an abundant alternative coursing through the Earth's crust. The accessibility of this transition metal, coupled with a significantly lower cost than scandium, makes it an enticing prospect for industrial applications. Yet, as with any innovation, we embarked on our efforts with a shadow of scepticism lingering over us: Would yttrium's propensity for oxidation prove a hindrance?

Back to 2012

Note that we are not the first to produce AlYN. That accolade belongs to Agnė Žukauskaitė from Linköping University, who, in 2012, provided the first report of this nitride, deposited by sputtering. Since then there has been sporadic interest in AlYN, followed by a notable surge in attention in 2023.

Recent research highlights include advancements in bulk acoustic wave resonators, enhanced piezoelectricity through alloying, and thermal conductivity measurements. MBE studies have demonstrated the ferroelectricity of AlYN and its ability to induce a two-dimensional electron gas in heterostructures. However, further exploration is needed to fully understand and optimise the properties of AlYN/GaN heterostructures.

We reported our first ground-breaking results concerning the growth of AlYN by MOCVD in April 2023. In our paper we detailed our growth of AlYN using the liquid precursor $(EtCp)_2$(iPr-amd)Y, to realise pure wurtzite layers with a yttrium content that exceeds 30 percent. Despite challenges, including cubic phase formation, we successfully deposited a 600 nm-thick $Al_{0.73}Y_{0.27}$ film, a pure wurtzite layer with an unprecedented yttrium concentration.

At the most recent International Conference on Nitride Semiconductors, held last November, we unveiled subsequent progress. At that meeting in Fukuoka, Japan, we announced our investigations with a purified solid precursor $(MCp)_3Y$ – these results have been recently published in *APL Materials*. This work involved the fabrication of AlYN/GaN heterostructures with a precisely tuneable yttrium concentration that exhibited excellent structural quality and electrical characteristics.

During this particular study, we attained yttrium concentrations up to 16 percent, and determined that the optimal properties for the two-dimensional electron gas occurred for a yttrium concentration of 8.2 percent. At this concentration the room-temperature sheet resistance is 444 Ω/sq, the electron density 1.30 x 10^{13} cm^{-2}, and the electron mobility 1079 cm^2 V^{-1} s^{-1} (see Figure 1). At the cryogenic temperature 7K, the electron mobility increases to 3234 cm^2 V^{-1} s^{-1}, the highest value reported for AlYN/GaN heterostructures. These results underscore AlYN's potential for next-generation HEMTs, which promise to offer enhanced digital communication systems and usher in a new era of semiconductor technology.

Our recent study is a comprehensive exploration of the growth, characterisation and optimisation of AlYN/GaN heterostructures formed by MOCVD. This effort elucidates the intricate interplay between structural parameters, such as yttrium incorporation and barrier thickness, and the resulting electrical properties – particularly the formation and optimisation of the two-dimensional electron gas, which is crucial for high-performance semiconductor devices.

This latest investigation began with surface morphology analysis, using atomic force microscopy. We meticulously examined the epitaxial quality of the heterostructures, determining a value for the root-mean-square roughness for a 10 μm^2 scan area of 0.28 nm. This low value indicates that our films are suitable for high-quality device fabrication.

We turned to the combination of high-resolution X-ray diffractometry and X-ray reflectometry to determine the barrier and cap layer thicknesses of our heterostructures. These techniques provided crucial insights into the structural integrity of the layers, essential for optimising device performance. We measured AlYN barrier and SiN_x cap layer thicknesses of 3 nm to 20 nm with an accuracy of ± 0.5 nm.

Concurrently, we undertook reciprocal space mapping, to assess the strain state of the AlYN barrier relative to the GaN substrate. This mapping shed light on the lattice-matching conditions – they seem to occur at a yttrium content of 8 percent to 10 percent – that are critical for minimising defects and enhancing carrier mobility.

In addition, we have carried out: phase analysis (2θ/θ-scan); azimuthal Φ-scans, which enable us to easily identify the presence of cubic inclusions; and pole figures, which allow us to estimate the presence of textures or twisting. By routinely performing these measurements, we have been able to understand the formation of cubic inclusions taking place in samples grown with a yttrium content above 20 percent, and a growth temperature higher than 1100°C.

To gain a deeper understanding of the chemical composition and depth profiles within our heterostructures, we have employed time-of-flight secondary ion mass spectrometry. This technique can uncover atom interdiffusion between the layers grown at higher temperatures, and, with the help of calibration standards, quantify yttrium concentrations (see Figure 2). We have observed a higher incorporation of yttrium in AlYN layers deposited on more lattice-compliant GaN layers, rather than on AlN layers.

We have also undertaken electrical characterisation of our films, including measurements of eddy-current sheet resistance and contactless Hall measurements. This has provided a comprehensive overview of the 2DEG properties, revealing key insights into carrier density, mobility, and electron transport mechanisms within our heterostructures. Through meticulous analysis of temperature-dependent Hall measurements, we have observed significant enhancements in electron mobility at lower temperatures, indicative of the potential for high-speed and high-frequency device applications (see Figure 3).

Another aspect of our work is the growth and evaluation of AlYN/GaN heterostructures on 4-inch SiC substrates. Our films on this foundation have an electron mobility close to 1400 $cm^2 V^{-1} s^{-1}$. This funding demonstrates the scalability and structural uniformity of these heterostructures, further underscoring their potential for large-scale semiconductor device fabrication. Through detailed morphological and structural analysis, coupled with comprehensive electrical characterisation, we have showcased the exceptional promise of AlYN/GaN heterostructures for next-generation HEMTs and advanced digital communication systems.

Next steps

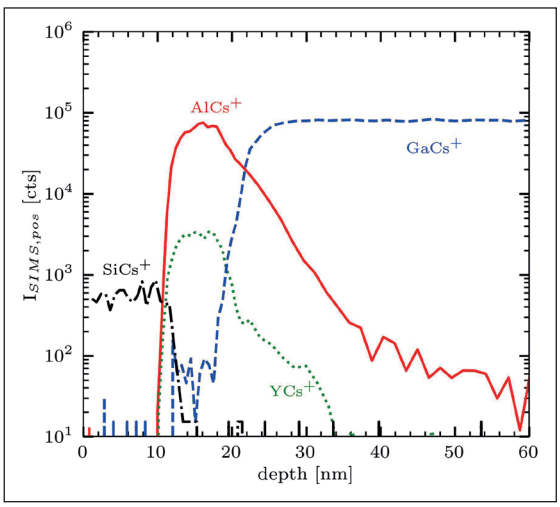
When navigating the complexities of our digitally driven society, it is paramount to pursue energy-efficient computing solutions. In this regard, much consideration must be given to the transformative potential of materials such as AlYN, as well as advancing cutting-edge technologies, such as HEMTs and non-volatile memories. These promising technologies allow humanity to chart a course towards a more sustainable, resilient future for digitally interconnected society and AI-powered computing.

Looking ahead, our next steps involve fostering cooperation across the globe to establish an international network dedicated to harnessing the full potential of AlYN/GaN heterostructures for transistor applications. By collaborating with researchers and industry partners worldwide, we aim to accelerate the translation of our findings into practical devices for the semiconductor industry.

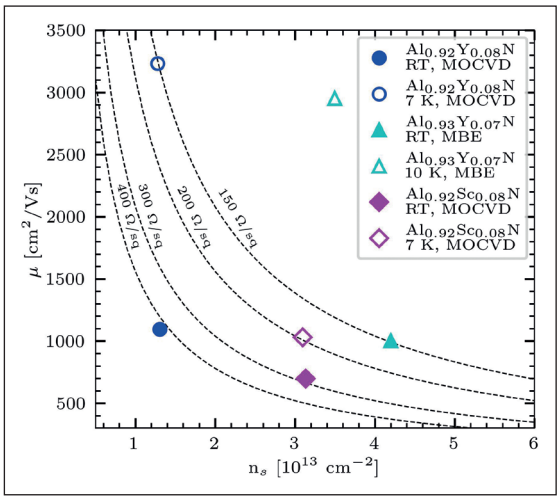
Our research marks a milestone in developing semiconductor devices that could deliver an improved performance, by switching to AlYN/GaN heterostructures. We have unravelled the intricate interplay between structural characteristics and electrical properties through meticulous experimentation and analysis. This effort lays the groundwork for realising advanced electronic devices with unprecedented performance and functionality.

Looking ahead, our next steps involve fostering cooperation across the globe to establish an international network dedicated to harnessing the full potential of AlYN/GaN heterostructures for transistor applications. By collaborating with researchers and industry partners worldwide, we aim to accelerate the translation of our findings into practical devices for the semiconductor industry.

In addition, our ongoing efforts will include exploring the ferroelectric properties of thick AlYN layers, which offer exciting prospects for non-volatile memory applications. By testing the viability of



➤ Figure 2. Secondary ion mass spectrometry analysis of an AlYN/GaN heterostructure suitable for a HEMT.



➤ Figure 3. Mobility and electron density obtained at room temperature and 7 K for MOCVD-grown AlScN and AlYN, compared with AlYN grown by MBE.

AlYN-based memories, we envision a future where sustainable, energy-efficient data storage solutions will power the next generation of interconnected devices.

Our vision encompasses the creation of sustainable, energy-efficient yttrium-based devices, driving innovation and connectivity in our interconnected society. By harnessing the power of AlYN/GaN heterostructures, we aspire to seamlessly integrate data storage and processing, facilitating transformative advancements in computing architectures.

While our research has unveiled the potential of AlYN in semiconductor technology, it is imperative to address concerns regarding its susceptibility to oxidation. This challenge poses a significant hurdle that may impact the material's viability for specific electronic applications. By openly acknowledging this issue, we reaffirm our commitment to transparency and responsible research practices.

Moving forward, it is essential to continue investigating strategies to mitigate or overcome limitations associated with oxidation, such as developing ultrapure precursors, implementing protective coatings and introducing innovative fabrication techniques. By addressing these challenges head-on, we ensure that our research efforts remain focused on areas with the most significant potential for success.

While the road ahead may present obstacles, our dedication to advancing semiconductor technology remains unwavering. By embracing challenges and fostering collaboration, we will navigate the complexities of AlYN and pave the way for a more interconnected, sustainable future in electronics.

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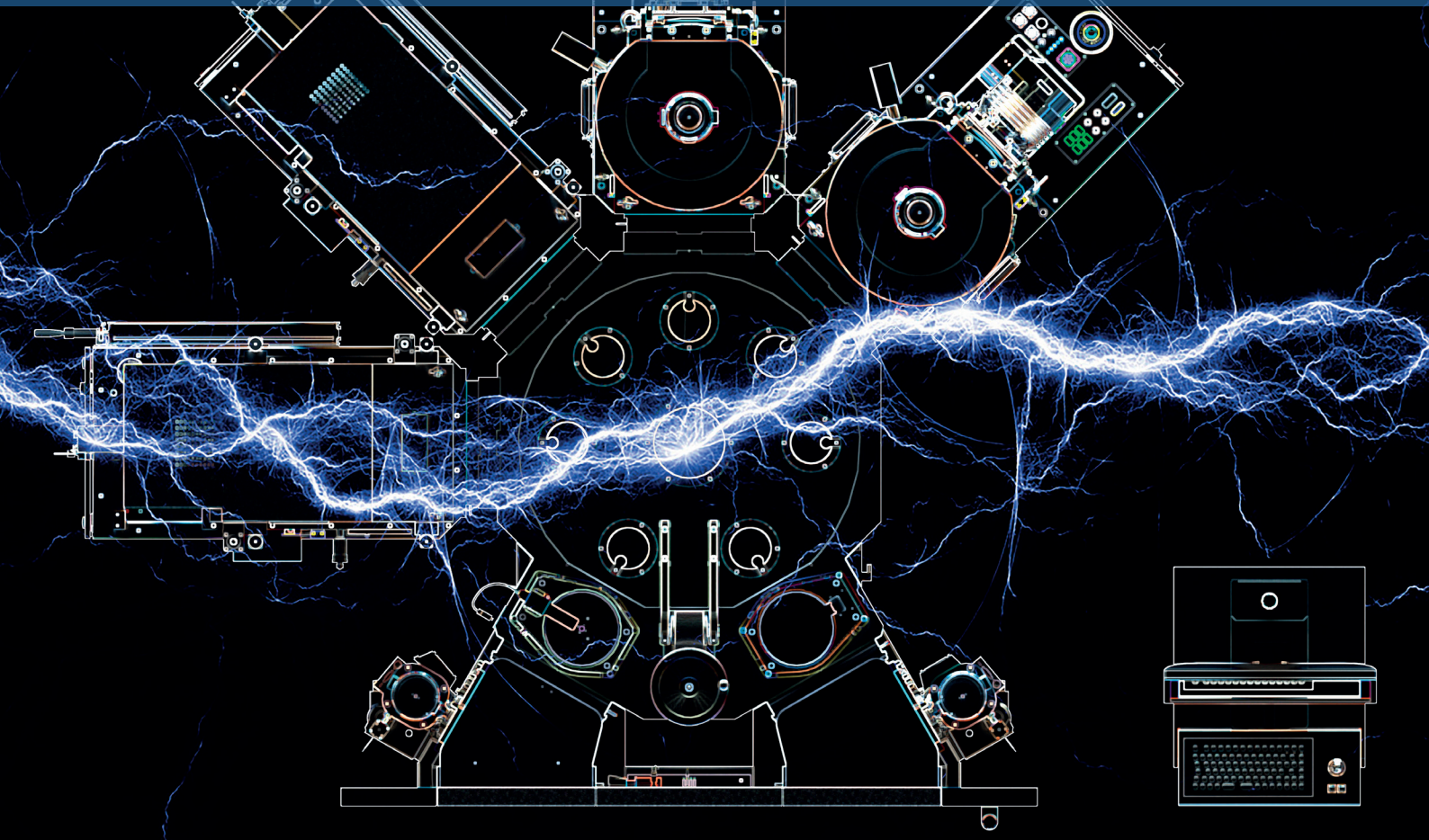

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Raising the bar for β-Ga_2O_3 diodes

Heterojunction barrier Schottky diodes combine a low turn-on voltage with a high breakdown

TO UNLEASH the potential increase in rectifier efficiency with β-Ga_2O_3 diodes, these devices need to combine a lower turn-on voltage and a diminished on-resistance with superior suppression of the reverse leakage current.

Addressing this challenge is a team from the University of Science and Technology of China that has unveiled a β-Ga_2O_3 heterojunction barrier Schottky diode equipped with a tungsten Schottky contact.

According to team spokesperson Quiyan Li, the most significant breakthrough associated with their recent work is the validation that a low-work-function metal leads to a low Schottky barrier height for β-Ga_2O_3, significantly reducing the turn-on voltage of these devices.

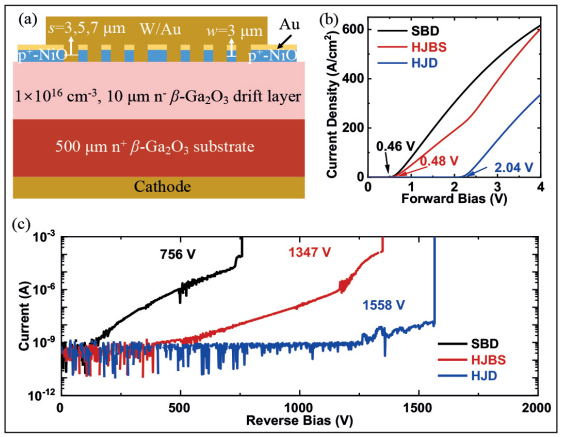
Typically, β-Ga_2O_3 diodes employ high-work-function metals for Schottky contacts, such as nickel and platinum, resulting in a turn-on voltage of 0.8 V. And even higher values of up to 2 V are realised when metal oxides, such as PtO_x and NiO, are introduced to trim the reverse leakage current. In stark contrast, the diodes made by Li and co-workers, featuring a tungsten Schottky contact, have a turn-on voltage of just 0.48 V.

Another important aspect of the devices pioneered by Li and co-workers is the use of *p*-type NiO to supress the reverse leakage current.

"As a result, we fabricated a unipolar diode with a breakdown voltage exceeding 1.3 kV," says Li.

To quantify the capabilities of this particular design, Li and co-workers evaluated the performance of heterojunction barrier Schottky diodes, Schottky barrier diodes, and heterojunction diodes. All three were fabricated from epiwafers purchased from Novel Crystal Technology that contained a 10 μm-thick, lightly-doped β-Ga_2O_3 layer grown by HVPE.

Production of devices from the HVPE-grown epiwafer began by chemical cleaning the surface and adding a Ti/Al/Ni/Au contact to the backside of the wafer. Formation of the top contact included using lithography to define spacer widths, and sputtering to deposit heavily-doped regions of 220 nm-thick NiO coated with 50 nm-thick gold. To form the anode, the team added a 50 nm-thick layer of tungsten and a 150 nm-thick layer of gold (see Figure for the resulting device architecture).



➤ Heterojunction barrier Schottky diodes almost match Schottky diodes for turn-on characteristics, while providing the highest breakdown voltages.

Measurements of the on-voltage, determined for a forward current density of 100 mA cm^{-2}, provided a value of 0.48 V for the heterojunction barrier Schottky diode, compared with 0.46 V for the Schottky barrier diode and 2.04 V for the heterojunction diode. For the heterojunction barrier Schottky diode, the forward-current density increases at a faster rate for voltages beyond the turn-on voltage for the heterojunction diode, thanks to a switch to bipolar operation.

The breakdown voltage of the heterojunction barrier Schottky diodes is 1558 V, significantly higher than that for the Schottky barrier diode and heterojunction diode, which have values for this key metric of 756 V and 1347 V, respectively. However, even the heterojunction barrier Schottky diode breaks down at a field strength of 2.46 MV cm^{-1}, far short of the maximum field strength for β-Ga_2O_3 of 8 MV cm^{-1}.

One of the next goals for Li and co-workers is to employ an embedded NiO for the junction barrier Schottky structure with stronger depletion capability to suppress the reverse leakage current. "However, this structure will bring challenges in repairing sidewall etching damage," says Li.

"After that, we will further optimise the parameters of the epitaxial layer, such as adopting a double-layer drift layer, in order to achieve low on-resistance while maintaining low surface electric field, low reverse leakage, and good breakdown capability."

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Irradiation-hardened GaN HEMTs

Enhancement-mode *p*-GaN HEMTs with a source-connected buried metal structure deliver robust single-event radiation hardness

A COLLABORATION between engineers at Nanjing University and CorEnergy Semiconductor is claiming to have broken new ground by demonstrating robust radiation hardness in novel *p*-GaN HEMTs.

According to team spokesman Feng Zhou from Nanjing University, this triumph could open up new and lucrative markets for the GaN HEMT. "We believe that GaN devices have a very broad market in radiation environments, which could reach hundreds of millions of US dollars or more," argues Zhou, who claims that there is an urgent need for advanced wide bandgap semiconductors in orbital satellites, spacecraft, and weapons facilities.

To demonstrate the superior radiation hardness of their *p*-GaN HEMTs, which remove holes accumulated under radiation, Zhou and co-workers have benchmarked their devices against conventional GaN HEMTs using the value for single-event burnout at a linear energy transfer of around 78 MeV cm^2 mg^{-1}. Linear energy transfer is the average radiation energy deposited per unit path length along the track of an ionizing particle.

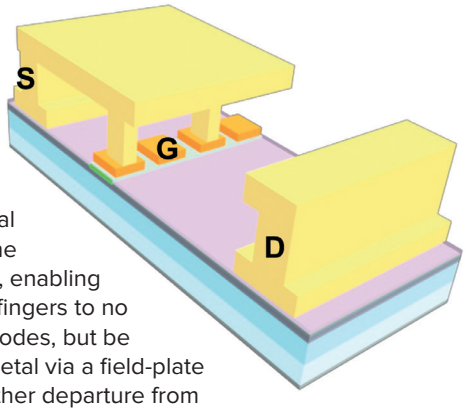
"The linear energy transfer describes the energy-deposition density of a particular type of radiation, which largely determines the adverse consequence of radiation exposure, such as degradation of electrical properties and radiation damage," explains Zhou.

For the team's *p*-GaN HEMTs, single-event burnout at a linear energy transfer of around 78 MeV cm^2 mg^{-1} occurs at 558 V. In stark comparison, typical GaN HEMTs have values of between 100 V and 200 V.

Another important aspect of the work of Zhou and colleagues is the development of an ultraviolet pulsed laser irradiation system that enables the evaluation of the dynamic characteristics of devices through integrated power switching circuits. According to Zhou, this novel alternative to a heavy-ion accelerator has enabled the first measurements that assess the power-conversion efficiency of GaN power devices under radiation.

Prior to the fabrication of their *p*-GaN HEMTs, Zhou and co-workers modelled the conventional form of this device. They found that radiation-induced holes accumulate in the channel/buffer regions near the gate stack, due to the reverse blocking of the *p-i-n* junction, which is composed of *p*-GaN/AlGaN/GaN in the gate stack of the *p*-GaN HEMT.

Based on this insight, the team introduced a partitioned design of the gate stack that safely dissipates accumulated holes and improves tolerance to single-electron burnout.



➤ Fabrication of radiation-hard HEMTs involves removal of the *p*-GaN layer in the non-gate region and source-connected buried metal region, followed by deposition of a Ti/Al/TiN metal stack in the patterned source and drain region, as well as the source-connected buried metal region.

Their novel HEMT architecture is realised by patterning the gate metal layer that's deposited on the *p*-GaN layer into segments, enabling some of the spaced metal fingers to no longer serve as gate electrodes, but be connected to the source metal via a field-plate interconnect process. Another departure from the norm is the etching of the middle region of *p*-GaN beneath the source-connected metals, so that these metals can be deposited directly on top of the AlGaN layer to form an ohmic contact. With this approach, the source-connected-metal/AlGaN/GaN ohmic contact contributes to the dissipation of holes.

Electrical measurements, comparing the radiation-hard HEMT with a control, reveal that the former has a higher threshold voltage and on-resistance – 3.3 V, rather than 3.0 V; and 223 mΩ, compared with 188 mΩ. Both increases are attributed to the source-connected buried metal structure that occupies part of the original gate region and weakens the current conduction capability.

Heavy-ion accelerator-based irradiation experiments using linear energy transfers of around 76 MeV cm^2 mg^{-1} and 86 MeV cm^2 mg^{-1} led to average values for the single-event burnout voltages of 558 V and 467 V, respectively, for the radiation-hard HEMT. In comparison, the equivalent values for the conventional HEMT were just 217 V and 89 V, respectively.

Operating under laser irradiation, a 300 W power factor conversion system has been found to have an efficiency of 95 percent under a linear energy transfer of around 76 MeV cm^2 mg^{-1}, compared with 91 percent for an equivalent system featuring a radiation-hardened 400 V vertical double-diffusion silicon MOSFET.

Zhou says that the next goal is to apply their radiation-hardened devices to circuit systems and conduct application verification for aerospace electronic systems.

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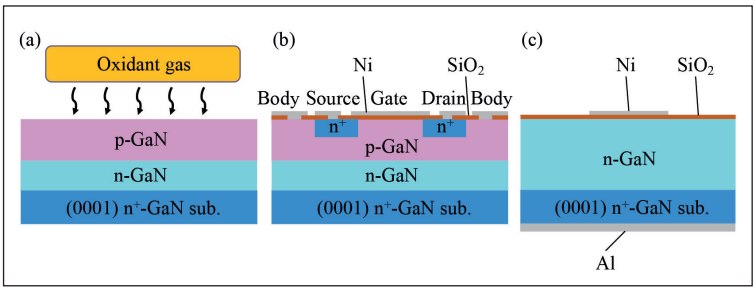
➤ F. Zhou *et al.* IEEE Electron Dev. Lett **45** 976 (2024)

Enhancing mobility with mist CVD

Depositing the gate oxide of GaN MOSFETs by mist CVD delivers a hike in field-effect mobility

SALES OF SiC MOSFETs are soaring, because they extend the driving range of electric vehicles by delivering a higher switching efficiency than silicon equivalents. Strengths of these vertical transistors include a high threshold voltage and a high current-handling capability, but losses are not as low as they might be, due to a channel mobility of around just 100 $cm^2 V^{-1} s^{-1}$.

However, this limited mobility could be addressed by turning to GaN MOSFETs with a SiO_2 gate oxide grown by mist CVD, according to a partnership between Mirise Technologies and Kochi University of Technology. According to recent work by this team from Japan, GaN MOSFETs produced with this deposition technology combines a high threshold voltage with a mobility of more than 250 $cm^2 V^{-1} s^{-1}$.



➤ The researchers from Mirise Technologies and Kochi University of Technology produced: (a), an epitaxial layer for oxidation evaluation; (b), a lateral MOSFET for determining channel mobility; and (c), an *n*-type MOS capacitor for finding the density of interface states.

For GaN MOSFETs, another requirement is a high threshold voltage, as this ensures that if these devices were deployed in inverters in electric vehicles, they would provide fail-safe operation. Spokesman for the team, Kauki Miyake, told *Compound Semiconductor* that data sheets for SiC MOSFETs reveal a threshold voltage of around 4 V for this device, leading one to assume that a similar value is needed if a GaN variant is to be competitive.

Miyake and co-workers are not the first to investigate the mobility of GaN MOSFETs. Previous studies have shown that GaO_x at the interface impacts GaN MOSFET mobility, and the thickness of this oxide is influenced by the gases that are used, as well as the oxidation time and temperature. Earlier work also considered the channel mobility of GaN MOSFETs with SiO_2 deposited by various techniques, but efforts to enhance mobility via oxidation control had limited success.

The researchers from Japan have addressed that issue, reducing GaN surface oxidation with plasma-enhanced CVD, atomic layer deposition (ALD), and mist CVD, which is a cost-effective method that does not require a vacuum system. In addition, the team have investigated the level of GaN surface oxidation in their samples, as well as measuring channel mobility and the interface state density.

To assess the capability of all three deposition techniques, Miyake and co-workers have applied oxidant gas to epitaxial layers; produced lateral MOSFETs to assess channel mobility; and made *n*-type MOS capacitors, to determine the density of interface states (see Figure).

Analysis of X-ray photoelectron spectroscopy offers an insight into the oxidation ratio of various samples under different oxidation conditions. For all three growth techniques, a long oxidation time increases the oxidation ratio. This ratio also increases within the ALD samples by moving from H_2O to O_3 and then to an O_2 plasma.

Samples produced by mist CVD have a lower oxidation ratio than those produced by ALD using the same oxidation time and same oxidant gas, O_3. The team attributes this to variations in O_3 concentration, differences in the heater configuration in the deposition equipment, and variations in gas flow through the chamber.

Measurements on the lateral MOSFETs reveal values for the threshold voltage, defined as the voltage at a current of 1×10^{-8} A, of 4.4 V for growth by plasma enhanced CVD, -9.0 V for ALD, and 4.8 V for mist CVD. The later technique, using O_3, led to the highest field mobility of 266 $cm^2 V^{-1} s^{-1}$ – that's more than twice that of the GaN MOSFETs produced by other techniques.

Scrutinising the interface of these lateral MOSFETs by cross-sectional scanning transmission microscopy, and applying electron-energy-loss spectroscopy, show that the nitrogen-to-gallium ratio decreased in the ALD-grown device at the interface of SiO_2 and GaN, indicating the presence of thick GaO_x. This technique also revealed that mist CVD using O_3 is an effective SiO_2 deposition method for supressing GaO_x.

Plots of capacitance-voltage provided a value of just 8×10^{10} $cm^{-2} eV^{-1}$ for the interface state density of the capacitor produced by mist CVD using O_3. In comparison, values for capacitors produced by plasma-enhanced CVD and ALD were 1.2×10^{12} $cm^{-2} eV^{-1}$ and 2.1×10^{12} $cm^{-2} eV^{-1}$, respectively.

Miyake says that the team will now apply mist CVD to the fabrication of vertical GaN MOSFETs.

REFERENCE

➤ K. Ikeyamam *et al.* Appl. Phys. Express **17** 064002 (2024)

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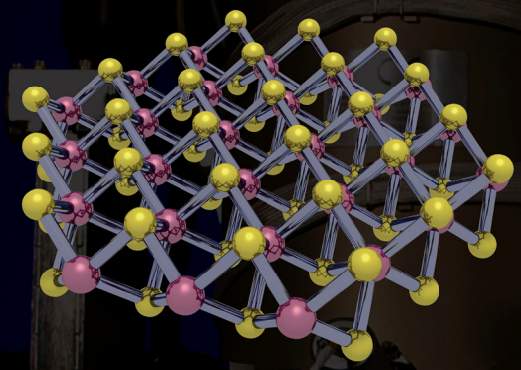

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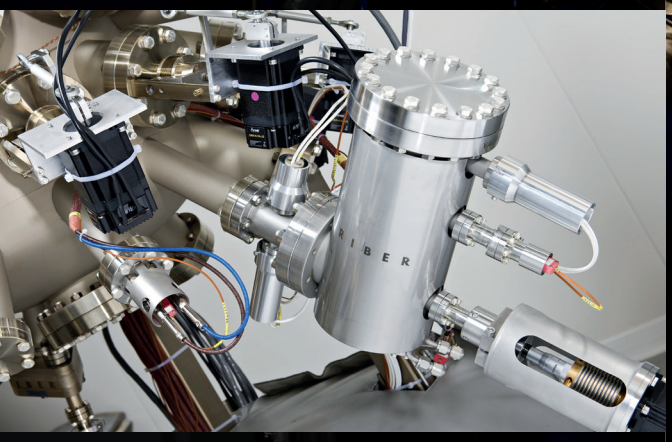

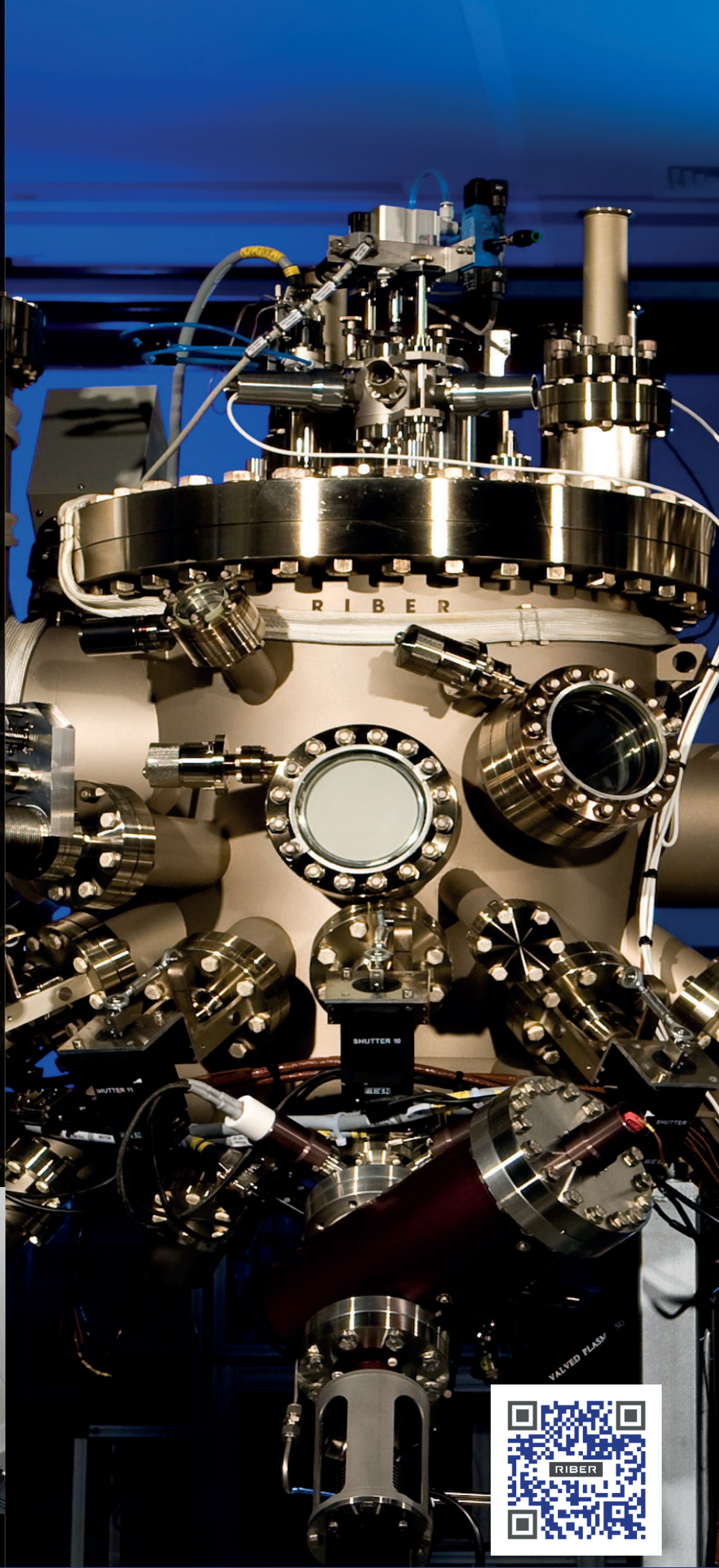

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