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VIEWPOINT

BY RICHARD STEVENSON
EDITOR

A new chapter for Wolfspeed

FOR a number of reasons, I'm a long-time admirer of Wolfspeed, formerly Cree.

To me, part of its appeal is the fascinating story of its founding and early years. The company, spun out of Bob Davis' group at North Carolina State University, began when a handful of incredibly ambitious graduates got together, lived in each other's pockets, and worked around the clock to exploit the opportunities provided by crystalline SiC. To do so, they had to overcome substantial technological and financial difficulties. When it came to the former, they managed to secure investment from a McDonald's franchisee, following the removal of established sources of venture capital in the wake of the 1987 Black Monday stock crash. And when it came to the big technical challenge, mastering epitaxy, they sought support by whirling a rubber chicken above their reactor. While it's hard to believe that this action paid dividends, after several years of hard work the team were one of the first to enter the high-brightness LED market.

Cree will always be remembered as a pioneer of commercial LEDs. As one of the big five – along with Lumileds, Osram, Nichia and Toyoda Gosei – this firm made billions from seeing its solid-state emitters deployed in mobiles, larger screens, and finally the light bulb.

As well as that success, the company deserves plenty of plaudits for looking ahead and adjusting its priorities. As margins in the LED industry plummeted, slashing profitability, its efforts have shifted to power electronics, with the company planning to play a key role in the revolution in transportation. With electric vehicle sales on an upward trajectory throughout this decade and beyond, Wolfspeed has recently been building its hopes on ramping shipments of SiC MOSFETs.

When companies try to cash in on an emerging opportunity, they often fall short by failing to move fast enough, and never catch up. But with Wolfspeed, it's quite the opposite – it went too hard and too fast, and it is now paying the penalty (for more details on this, see p. 16). Compounding Wolfspeed's current woes are a softening of the electric vehicle market,

and increased competition for sales of SiC substrates that have tumbled in price over the last year or so. While the company is still in pole position, it no longer has a vice-like grip on this sector.

After borrowing big to finance a colossal expansion in capacity that's yet to be matched by orders, Wolfspeed has spent the last few years under a very black cloud, with debt at troublesome levels. That's alarmed the investment community, and led to a fall in share price from north of $140 in late 2021 to single digits, with trading sometimes even falling below a dollar.

To seek refuge from its crippling debt, Wolfspeed recently filed for Chapter 11 bankruptcy protection. It's an action that forms part of a restructuring effort that's included the conversion of a substantial loan from Renesas into shares, due to mature in summer 2031.

Hopefully these steps, and others that will follow, will ensure the survival of Wolfspeed. And if they can they go on to thrive from this incredibly difficult position, I will not be alone in admiring the next chapter in their history.

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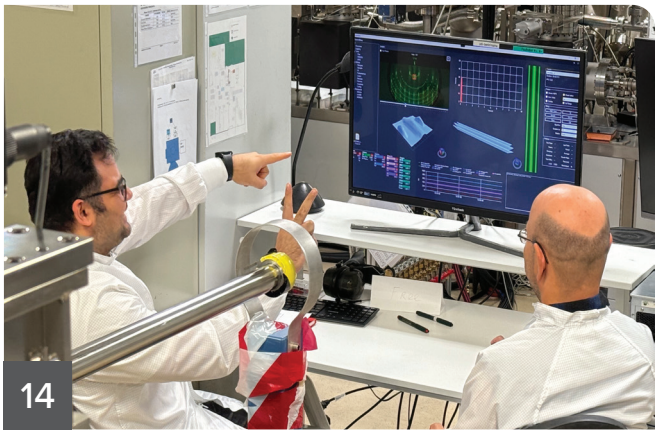

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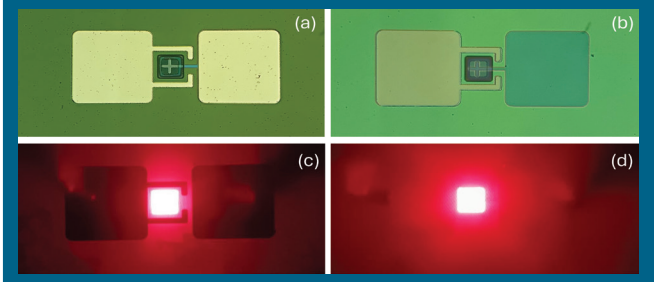

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RF to be a $70 billion market by 2030

Growing RF market enters a new era of integration and global competition, says latest Yole report

IN ITS FIRST *Status of the RF Industry* report, the Yole Group's forecasts a $70 billion RF market by 2030, growing from $51.3 billion in 2024. This 4.5 percent CAGR will be driven by 5G, consumer connectivity, and emerging 6G technologies.

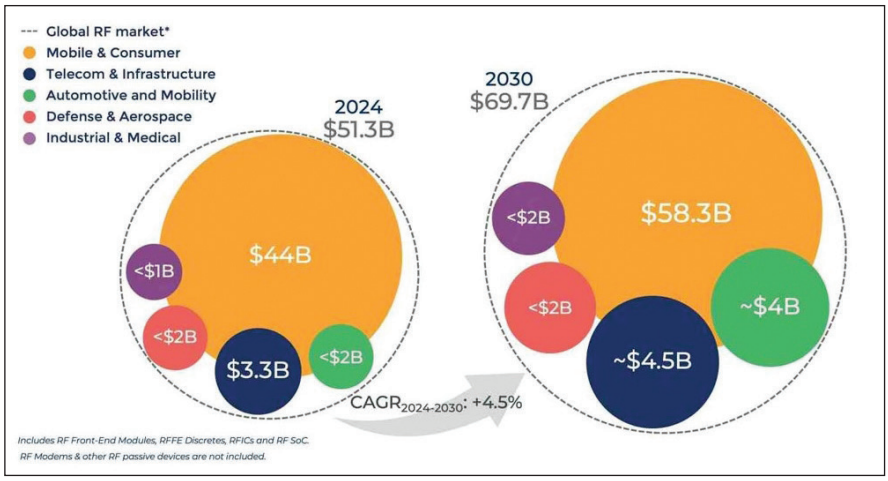
Cyril Buey, senior technology & market analyst for RF at Yole Group said: "RF technologies are everywhere, from your smartphone to your car, and from telecom towers to defense radars. This first report synthesizes decades of RF innovation and provides forward-looking guidance for an industry under major transformation."

The mobile and consumer segments lead the RF market, accounting for the highest share in both revenue and volume. US giants like Qualcomm, Broadcom, Skyworks, and Qorvo dominate, offering advanced RFFE modules and RF SoCs for smartphones and connected devices. In parallel, Samsung and MediaTek serve high-volume markets across Asia, with varied integration strategies.

Chinese RF companies are also a key part of the mix. Moreover, they are accelerating efforts to reduce foreign dependency, through leading players like Maxscend, Vanchip, and Smarter Micro. HiSilicon also confirms its return with dedicated in-house RFFE and SoC solutions.

Yole's analysts forecast two fast-growing subsegments by 2030: RFFE modules, more than $ 17 billion; and RF SoCs for cellular and Wi-Fi/Bluetooth/GNSS, exceeding $23 billion. Discrete RF devices, including PAs, LNAs, switches and filters, with almost $14 billion, are also part of this RF landscape.

Filters represent the most dynamic segment and the second largest part of the RF front-end market in terms of value.



Telecoms, automotive, and defence

In telecom infrastructure, GaN technology is gradually replacing LDMOS in massive MIMO base stations. Companies such as NXP, Qorvo, SEDI, and Analog Devices lead this market segment internationally. However, China is scaling up domestic production of GaN-based RF solutions and LDMOS with suppliers like Sanan IC, Wuatek, and Dynax.

The global 6G race is now a critical driver of RF sovereignty strategies, with government-backed programmes underway in the US, China, Japan, Korea, and Europe.

Chinese RF companies are also a key part of the mix. Moreover they are accelerating efforts to reduce foreign dependency, through leading players like Maxscend, Vanchip, and Smarter Micro. HiSilicon also confirms its return with dedicated in-house RFFE and SoC solutions

RF is becoming essential in automotive ADAS, infotainment, and connectivity. NXP and Infineon Technologies lead with SiGe, CMOS solutions, and GaAs-based radar ICs. In parallel, UWB adoption is accelerating, with Apple, Qorvo, and NXP anchoring the ecosystem across smartphones, smart homes, and vehicles.

In defence, RF innovation focuses on high-power broadband systems for radar, satcom, and EW. Once again, GaN-based designs dominate this market segment. Meanwhile, industrial and medical applications prioritise reliability and low power, but have long certification cycles.

Yole Group will be on-site to share its market expertise and connect with key players shaping the future of high-frequency technologies at European Microwave Week (EuMW) 2025.

It will also participate in the Automotive Forum, with a dedicated presentation on September 23, focused on automotive radar markets and technologies, by Hassan Saleh, senior technology and market analyst, RF, at Yole Group.

Coherent opens SiC facility in Vietnam

New plant will play a pivotal role in boosting capabilities in SiC and optics, says Coherent

COHERENT, the US-based semiconductor and optoelectronics firm, opened a new facility in Vietnam on July 28, 2025. The $127 million plant, in Nhon Trach Industrial Park in Dong Nai province, will make SiC semiconductors, optical glass, and advanced optoelectronic components.

Speaking at the opening ceremony, deputy prime minister Nguyen Chi Dung, underscored the move by Coherent as compelling evidence of the growing confidence that leading global tech firms are placing in Vietnam's investment environment and development potential.

"Vietnam is actively developing key strategic industries, including semiconductors. Today's event is a concrete step in implementing the Joint Statement on upgrading Vietnam-US relations to a Comprehensive Strategic Partnership. Coherent is expected to make a meaningful contribution to Vietnam's emergence as a key link and future hub in the global semiconductor supply chain," said Dung.

Coherent entered Vietnam in 2005, establishing its first factory at VSIP1 Industrial Park in former Binh Duong province, specialising in thermoelectric coolers, technical ceramics, wafers, advanced optics, and laser services. In the late 2010s, Coherent expanded to the north, and in 2019 opened a facility at Yen Phong Industrial Park (IP) in Bac Ninh province.

In 2023, Coherent met with Dong Nai provincial leaders to propose three high-tech projects at Nhon Trach 1 & 2 IPs, including SiC, semiconductor manufacturing, advanced optics, and the M-Cubed project for measurement, testing, and semiconductor component production.

Gan YC, director of Nhon Trach 1 Factory, said: "This new facility is designed with scalability, flexibility, and sustainability at its core, to meet the rising global demand for advanced technologies. It plays a pivotal role in enhancing our capabilities in SiC and optics, both essential to the transformation of industrial systems, high-speed communications, and data centre infrastructure. Equipped with smart manufacturing systems and a high-quality local workforce, the factory strengthens our supply chain, reduces lead times, and brings us closer to key markets across Asia. This is not merely a factor, it is a strategic platform for innovation, growth, and long-term competitiveness," said YC.

Nguyen Minh Man, general director of Coherent Vietnam (Dong Nai) believes the inauguration of Coherent Corporation's new factory in Vietnam marks a significant step forward in its global growth strategy. "It reinforces our long-term commitment to Southeast Asia, a vital region for advanced manufacturing, technological innovation, and talent development," said Man.

Macom completes takeover of Wolfspeed RF wafer fab

MACOM TECHNOLOGY has assumed full control of the GaN-on-SiC wafer fab it acquired from Wolfspeed in 2023 for $125 million.

Located in Research Triangle Park, North Carolina, the fab specialises in RF and microwave GaN-on-SiC process technologies for telecommunication system infrastructure and defence electronics.

The facility is an accredited United States Department of Defense Trusted Foundry.

"This transfer is occurring approximately six months ahead of schedule," said Stephen G. Daly, Macom's president and CEO. "Our leadership and management team are focused on opportunities to improve the fab's performance and key operational metrics. The best results are yet to come."

Far-UVC LEDs deliver record-breaking performance

FBH microLED development paves the way towards compact medical light sources that can inactivate pathogens in body cavities

EACH year thousands of people die from multidrug-resistant organisms (MDROs), such as MSRA, acquired in hospitals. But one potential approach to killing these harmful microorganisms is the use of far-UVC wavelengths below 235 nm.

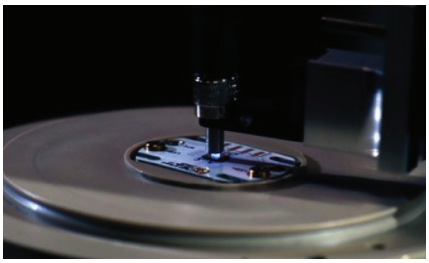
Now the Ferdinand-Braun-Institut (FBH) in Berlin has reported exceeding an important threshold in making this technology more widely applicable. It has announced 1 milliwatt of output power using far-UVC LED light sources in continuous wave (CW) operation from a single fibre – an international record that was recently presented at a conference.

The breakthrough research, driven primarily by the work of Jens Rass, was achieved using 235 nm UV microLEDs arranged in a dense array, allowing five times more light to be coupled into the fibre than with conventional far-UVC LEDs. The microLEDs themselves, of which up to 125,000 are arranged on a chip measuring one square millimetre, are compact, with diameters of only around 1.5 μm. Importantly, the light source is also directional.

Sven Einfeldt, research group leader at the FBH, who has many years of experience in the development of UVC LEDs for medical applications, explains: "With these very short-wave LEDs, we were able to demonstrate international record values in terms of efficiency and performance – a real breakthrough. Together with partners, we now want to take the next step from the laboratory to practical application with a prototype."

The Berlin-based institute has already developed 233 nm UVC LEDs for panel irradiation systems that have been applied directly to human skin. Extensive studies conducted within two BMFTR-funded projects at University hospital in Berlin and the University in Greifswald have confirmed the effectiveness of the treatment and that it does not cause any lasting damage to the skin.

The longterm vision is to be able to make light sources for disinfecting the nasopharyngeal cavity for eradicating



multi-resistant germs and also for disinfection in other body cavities. One milliwatt LED irradiation sources, according to the researchers, could provide irradiation times of around five minutes without significant heat generation.

"This would allow us to inactivate MDROs in their habitats, which have been difficult to reach until now. After disinfecting the entire body with special washing lotions and mouthwashes, it would be possible, for example, to completely eliminate MRSA bacteria," explained Martina Meinke, head of the Centre for Skin Physiology at University hospital in Berlin's Department of Dermatology, Venereology, and Allergology.

Singapore opens GaN innovation centre

SINGAPORE has opened the National Semiconductor Translation and Innovation Centre for GaN; the country's first national facility dedicated to GaN semiconductors.

The centre addresses common challenges faced by companies and researchers – such as limited local access to advanced facilities and the need for closer collaboration.

NSTIC (GaN) is the first facility in Singapore to host both 6-inch GaN-on-SiC and 8-inch GaN-on-silicon wafer fabrication lines. It will also offer advanced GaN technology with gate lengths below 0.1 μm and operation frequencies above 100 GHz, suitable for chips used in satcoms and a range of future communication and instrumentation technologies.

NSTIC (GaN) will begin offering commercial foundry services from mid-2026.

First set up in 2023 as the National GaN Technology Centre (NGTC), NSTIC (GaN) is a partnership between the Agency for Science, Technology and Research (A*STAR), DSO National Laboratories, and Nanyang Technological University, Singapore.

NSTIC (GaN) is part of the broader National Semiconductor Translation and Innovation Centre initiative led by A*STAR, which supports national efforts to deepen semiconductor R&D and innovation across priority domains, such as photonics and advanced packaging.

"NSTIC (GaN) is not just a facility – it is a national platform for innovation and a catalyst for future technologies," said Cheong Chee Hoo, chairman of the NSTIC (GaN) Steering Committee.

"Our goal is to build deep capabilities in GaN manufacturing and research, so that Singapore can help define the future of high-performance semiconductors."

Q-Pixel launches Q-Transfer technology enabling microLED transfer

Q-Pixel debuts Q-Transfer technology that enables incredibly high yield microLED transfer

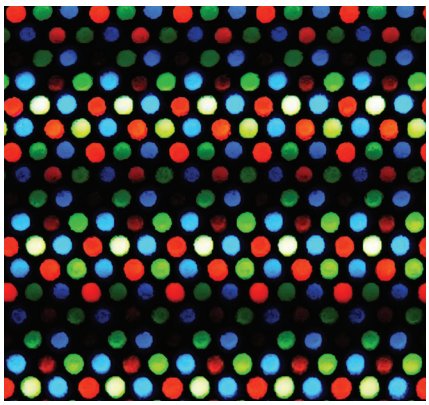
MicroLED DISPLAY startup Q-Pixel Inc. has debuted Q Transfer, a microLED display technology that directly addresses the pixel transfer challenge long faced by the microLED display industry.

The low yield of conventional mass transfer processes (below 99.99 percent) leads to prohibitively high repair and manufacturing costs and remains a major barrier for scaling microLED displays towards mass production. As a result, only limited high-end microLED products are available in the market.

Q-Transfer radically improves microLED transfer yield while maintaining high resolution and superb alignment accuracy, thus enabling the production of large-area, high-quality microLED displays, such as wearables, mobile devices, and transparent displays, at affordable prices.

Q-Transfer was implemented by a patented process using Q-Pixel's tuneable polychromatic microLEDs (TP-microLEDs) to successfully demonstrate color display prototypes. These displays consist of 10 μm pixels with over 500 pixel-per-inch (PPI) densities, and most notably, zero missing pixels in the transfer process for more than 99.9995 percent transfer yield – over an order of magnitude improvement over existing transfer approaches.

The debut of Q-Transfer marks a new breakthrough in Q-Pixel's microLED display technology portfolio. Q-Pixel's achievements in microLED technology include world records for



the highest resolution colour active-matrix display (6,800 PPI), highest resolution full-colour display (10,000 PPI), and world's smallest full colour pixel (1 μm) diameter based on their tunable polychromatic LED (TP-LED) epitaxial material.

Microchip partners with Delta on SiC

Agreement builds on Microchip's mSiC technology and Delta's smart energy solutions

MICROCHIP TECHNOLOGY has announced that under a new partnership with power management company Delta Electronics the companies will collaborate to use Microchip's mSiC products and technology in Delta's designs.

The synergies between the companies aim to accelerate the development of SiC-based energy-saving products and systems.

Delta intends to use both Microchip's experience in SiC and digital control to accelerate time to market of its solutions for AI, mobility, automation and infrastructure.

"SiC is increasingly important in sustainable power solutions because of its wide-bandgap properties, which enable smaller and more efficient designs for high-voltage, high-power applications at a lower system cost," said Clayton Pillion, vice president of Microchip's high-power solutions business unit.

"We look forward to forging an impactful path with Delta Electronics on innovating SiC solutions to meet the rising demand of the electrification of everything."

Other key advantages of the agreement are top-tier design support, including technical training.

Navitas plans 200 mm GaN production with PSMC

NAVITAS SEMICONDUCTOR has announced a strategic partnership with Powerchip Semiconductor Manufacturing Corporation (PSMC or Powerchip), to start production and continue development of 200 mm GaN-on-silicon technology.

Navitas' GaN IC portfolio is expected to use Powerchip's 200 mm Fab 8B, located in Zhunan Science Park, Taiwan. The fab has been operational since 2019 and supports various high-volume manufacturing processes for GaN, ranging from microLEDs to RF GaN devices.

Powerchip's capabilities include an improved 180 nm CMOS process, offering smaller and more advanced geometries, which bring improvements in performance, power efficiency, integration, and cost.

"200 mm GaN-on-silicon production on a 180 nm process node enables us to continue innovating higher-power-density, faster, and more-efficient devices while simultaneously improving cost, scale, and manufacturing yields", said Sid Sundaresan, SVP of WBG Technology Platforms at Navitas.

Powerchip is expected to manufacture Navitas' GaN portfolio with voltage ratings from 100 V to 650 V, supporting the growing demand for GaN for 48 V infrastructure, including hyper-scale AI data centers and EVs. Qualification of initial devices is expected in Q4 2025.

The 100 V family is expected to start production first at Powerchip in the first half of 2026, while the company expects 650 V devices will transition from Navitas' existing supplier, TSMC, to Powerchip over the next 12-24 months.

Navitas recently made several announcements in the AI data centre, EV, and solar markets, including its collaboration with NVIDIA to support GaN and SiC technologies for 800 V high-voltage DC architectures for 1 MW IT racks and beyond.

Enphase announced that its next-generation IQ9 would include Navitas' 650 V bi-directional GaNFast ICs, and Changan Automobile announced its first commercial GaN-based OBC (on-board charger) using Navitas' GaNSafe technology.

"We are proud to partner with Powerchip to advance high-volume 200 mm GaN-on-silicon production and look forward to driving continued innovation together in the years ahead", said Gene Sheridan, CEO and co-founder of Navitas. "

Nexperia and TU Hamburg endow chair in WBG research

New professorship to accelerate wide bandgap semiconductor research and train next-generation talent

NEXPERIA and the Hamburg University of Technology (TU Hamburg) have launched an endowed professorship in power electronic devices with a focus on wide bandgap semiconductors, including SiC, GaN and AlScN.

The position, held by Holger Kapels, will drive research into next-generation semiconductor components and train engineers at TU Hamburg's School of Electrical Engineering, Computer Science and Mathematics.

As part of this initiative, Kapels will also lead the newly founded Institute for Power Electronic Devices.

In his inaugural lecture, 'Innovative Power Semiconductor Devices as a Key Technology for an Electrified Future' Kapels outlined how compound semiconductors based on SiC and GaN are enabling transformative improvements in energy efficiency – particularly in electric vehicles, industrial systems, and data centres.

The new institute will focus on aspects such as new device architectures, including vertical GaN structures, and machine-learning-based fault prediction systems. Additional research priorities include modeling the reliability and

ruggedness of power devices under extreme operating conditions.

Opening remarks at the event were delivered by TU Hamburg president Andreas Timm-Giel.

Representing the Hamburg Senate, state secretary for science Eva Gümbel emphasised the broader impact of the new chair: "This endowed professorship addresses one of the most important enabling technologies of our time. Power electronics are vital to sustainable energy supply and industrial innovation. With Prof. Kapels, TU Hamburg gains a leading researcher who will shape both science and education in this strategic field."

Ansgar Thorns, VP R&D at Nexperia Germany, highlighted the professorship's significance for the company and the broader innovation ecosystem: "This professorship is an investment in future technologies, in local talent, and in Hamburg as a center for semiconductor excellence. Fostering innovation and developing the next generation of engineers go hand-in-hand – and both are critical to strengthening our deep-tech ecosystem."

Nexperia has a manufacturing legacy in Hamburg that dates back over a century to the founding of the Valvo radio tube factory in 1924 – a pioneering site in German electronics history.

Today, Nexperia's Hamburg facility produces approximately 25 percent of the world's small-signal diodes and transistors. Since 2017, the site has expanded from 950 to around 1,600 employees and undergone significant technological modernisation, including a strategic expansion into power semiconductors.

"This is Nexperia's first endowed professorship and a milestone for our engagement with research and education," Thorns added. "We're proud to partner with TU Hamburg – a strong academic institution – to shape the future of energy-efficient semiconductor technologies in Germany and beyond."

Japanese team prepares to make SiC from chip waste

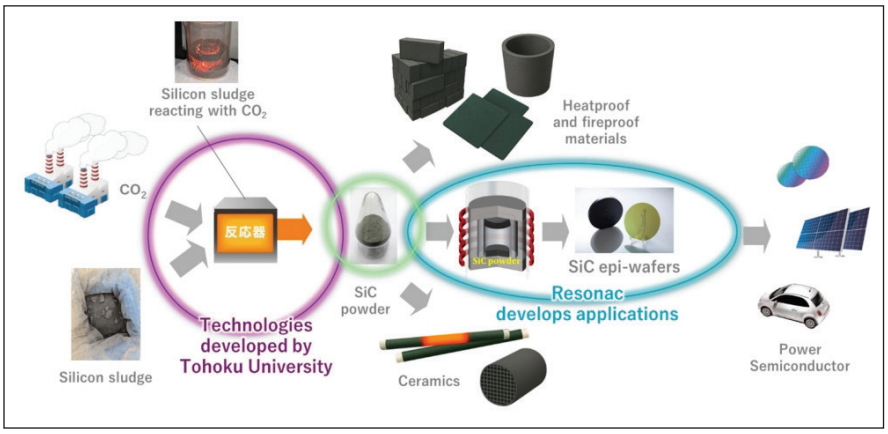
Resonac and Tohoku University are looking to apply carbon recycling to silicon sludge and CO_2

Japanese chemical company Resonac and Tohoku University have been exploring using SiC powder, produced from sludge generated during silicon wafer manufacturing and carbon dioxide, as a raw material for the growth of SiC single-crystal materials.

The team say they have now completed this basic research phase and have started full-scale studies aimed at practical applications.

If this technology is successfully commercialised, SiC power devices will not only contribute to energy conservation as products, but also enable reductions in CO_2 emissions during manufacturing, the recycling of silicon sludge and CO_2, and the overall reduction of environmental impact throughout their lifecycle.

The researchers estimate that the CO_2 reduction effect per 100 tonnes of SiC powder will reach the equivalent of 110 tonness of CO_2. This is expected to significantly contribute to the further promotion and widespread adoption



of SiC power devices, which enable energy conservation and CO_2 reduction.

For the fundamental research, Tohoku University synthesised SiC powder by heating silicon sludge and CO_2 with microwaves at its carbon recycling demonstration research hub, while Resonac worked on applying the SiC powder to SiC single-crystal substrates.

Jun Fukushima from Tohoku University remarked: “The key feature of this process lies in its ability to transform CO_2, which is stable gas, into high-purity SiC with low energy consumption, offering a promising solution to both waste management and greenhouse gas reduction.”

Diverse fields, such as electric vehicles and renewable energy sectors, could benefit. “By accumulating practical demonstrations, we seek to enhance industrial competitiveness and present concrete measures toward achieving carbon neutrality and a circular economy by 2050,” said Fukushima.

EU project to provide 4-inch AlN crystals

THREE leading players in semiconductor research and development – the Leibniz Institute for Crystal Growth (IKZ), PVA TePla AG, and Siltronic – are combining their expertise in a pioneering project to scale up AlN crystal growth.

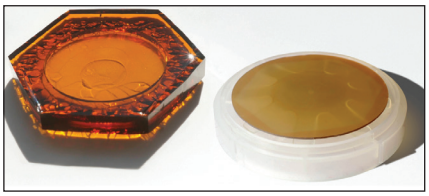
The project focuses on the fabrication of 4-inch AlN substrates to enable applications in high-power electronics and ultraviolet photonics.

The project’s focus on scaling AlN crystal diameters from 2 to 4 inches addresses a fundamental requirement for transitioning this key material from research-scale to industrial manufacturing environments.

The Leibniz Institute for Crystal Growth (IKZ) brings its long-standing expertise in growing AlN crystals to the project and has a proven 2-inch AlN crystal growth platform.

Siltronic. a producer of silicon wafers (using both Czochralski and Float Zone methods), contributes its experience in the R&D of substrates for power electronics and in precision metrology.

PVA TePla AG provides solutions in materials and metrology with decades of experience in manufacturing crystal



growing systems. With its expertise in the Physical Vapour Transport (PVT) method, particularly in the SiC market, PVA TePla provides the equipment for growth process for bulk AlN crystals.

“The expansion from 2-inch to 4-inch is a crucial milestone in making AlN accessible for mass production”, the project partners explain. “Thanks to the synergies among the partners, we can overcome the technological barriers.”

A holistic approach to growing with AI

Bizmuth MBE is advancing thin-film growth by drawing on the capabilities of the latest AI technology

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

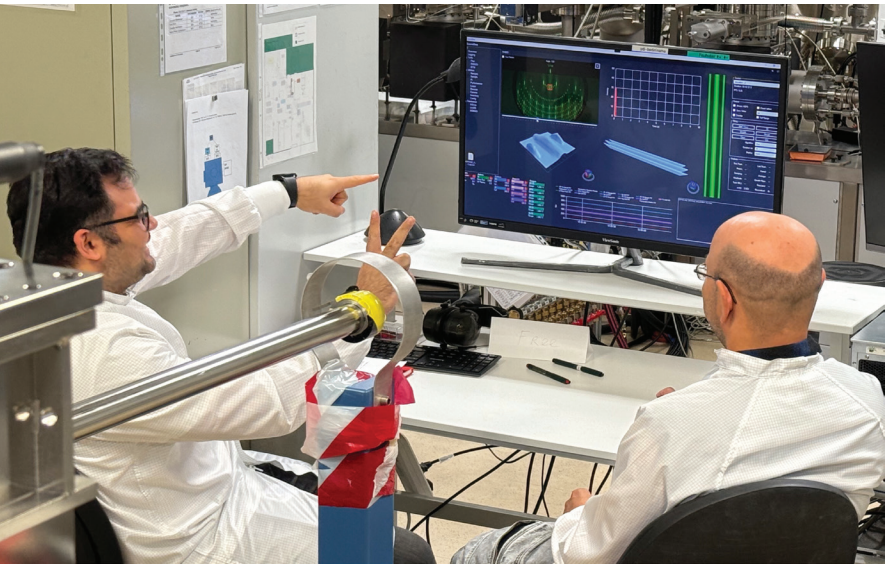
IT'S OFTEN SAID that the devil is in the detail. And that's certainly the case when turning to AI to optimise the production of compound semiconductor devices.

While AI is grabbing headlines in today's mainstream media for its transformative potential, it's not a new technology. Its initial development dates back many decades, and includes the pioneering efforts of the brilliant British mathematician Alun Turing, who published a seminal paper in the 1950s.

In recent times AI has grabbed much attention in our industry as a tool for classifying defects and aiding epitaxy, and when it comes to the later, one should not assume the support provided by AI is fixed. It's not: it's evolving, with capabilities that are sure to grow over many years.

Although some of the AI advances within our industry may be hidden from view, as the downside of patenting IP is that it discloses ideas, it is well known that IVWorks has been promoting the use of AI for many years. Based in South Korea, this provider of GaN epiwafers has put thin-film AI on the map, drawing on this technology since at least 2019.

However, while deep learning was at the forefront of AI a few years ago, the technology has moved on. Now the new kid on the block is the large-language model, which allows AI to draw on all information that's publicly available, including every journal paper, text book, and all material on the internet. Within this model is a multimodal feature, enabling AI to understand the make-up of images – this allows for comprehension of the reflection high-energy electron diffraction (RHEED) images provided by *in-situ* tools during MBE growth that are key to monitoring epitaxial processes.



IVWorks hinted that they will be working towards the introduction of these new AI technologies at their foundry. But they are by no means alone, with London-based start-up Bizmuth MBE striving to get there faster, with an AI toolkit that operates at the system level and will be available to all.

Founded just a year ago, Bizmuth has a tremendous track record in software-related innovation to support MBE, having established relationships with the University of Sheffield and HRL, and just started a ground-breaking project with the Paul Drude Institute (PDI), a world-renowned pioneer of MBE.

The duo behind Bizmuth are its CEO, the third-generation entrepreneur and environmental scientist Isabella Lorente, and CTO Faebian Bastiman, who has a PhD in MBE and passion for coding. This pair are working together to offer the world an AI technology for thin-film growth that will ultimately operate at the system level, delivering what is essentially a lab operating system.

Bizmuth has not pursued external funding. "Everything that we have accumulated has been earned, not raised," says Bastiman, explaining that revenue has been generated through sales of software and fees from delivering seminars covering many matters related to MBE. One of the merits of this approach is that Bizmuth is making its own plans, rather than having to compromise to placate investors.

Bastiman sums up the company's philosophy as this: "We want to walk before we run, and then we want to still be running for decades to come, building really ambitious tech, grounded in sustainable business sense."
Bizmuth is developing an entire ecosystem in a very

structured, logical manner, building on software produced by Bastiman over many years.

More than a decade ago he created a piece of software called Epic, designed to control MBE equipment.

"It was everything that I'd been missing from 2004 to 2012 as a grower," explains Bastiman. "I wanted automation. I wanted automatic flux checks. I wanted to know the composition of what I was growing, etc. I wanted to know how much material is left in my cell."

After offering all these features to others through Epic, Bastiman introduced a pair of software packages: Nexus, which is MBE control software that's built on Epic; and a RHEED analysis software called Pulse.

"The reason why I made Pulse is that there was no other RHEED software that you could talk to," says Bastiman, who explains that with this breakthrough growth software can instruct RHEED software to undertake oscillation checks, thereby determining growth rates and automatically calibrating the MBE tool.

Following on from the introduction of an expanded software portfolio has been the MBE Academy. It's a practical guide to this growth technology that's emerged from a collection of blog posts from a dozen years or more. This source of knowledge, designed to make it easier for engineers to develop the expertise required for thin-film growth, addresses the omission of formal training for MBE.

Within the academy are interactive teaching tools, including one called Crystalmatic. "It's essentially just ball-and-stick models in 3D that you can spin around, go down to the unit cell, and come back up and build a structure for the common semiconductors," says Bastiman. There's also a RHEED simulator that allows users to input a crystal structure, calculate the reciprocal space equivalent, and see the resulting diffraction pattern.

A can-do attitude

Helping Bizmuth to get off the ground and generate an income is its willingness to serve its customers by providing solutions to whatever problem they have.

"We love a challenge," says Bastiman, who is incredibly keen to modify software to address the needs of its users: "They didn't just buy a product. They bought a lifestyle. I want them to enjoy this lifestyle."

The support provided by Bizmuth to researchers at the University of Sheffield has injected new life into legacy hardware, which is perfectly functional, but would not interface with software. According to Bastiman, by engaging with the services of Bizmuth, process engineers are avoiding 'vendor lock-in' and continuing to use their growth tool.

What's in a name: Bizmuth MBE

A number of reasons lie behind the moniker Bizmuth. This element, known for its iridescence and multi-layered nature, has parallels with the company, as well as a special place in the hearts of its founders. CEO Isabella Lorente has a lifelong love of minerals, with Bismuth her favourite, and CTO Faebian Bastiman investigated one of its promises when pursuing his PhD, evaluating its addition to GaAs to form dilute bismides. Another great characteristic of bismuth is that it has the longest half-life of any non-radioactive element, reflecting the aims of the founders to create a company that endures. And why the 'z', not an 's'? It's a play on words, reflecting that the company is a business.

"We allowed them to get several PhDs worth of results at a time where they would have been blocked and delayed by traditional methods."

Bastiman says that when working with HRL, efforts have focused on delivering software that integrates with workflow and optimises proficiency.

This June, Bizmuth announced that it has just started an extremely ambitious project with PDI. Bastiman is tight-lipped when it comes to the details of this "multimodal mesh" technology that's being deployed, but he is willing to talk more freely about the aim of the project: It's to determine the growth window for GaN on one MBE system, and then replicate this on two other systems.

"Finding the gallium nitride growth window is non-trivial," argues Bastiman. "Anyone that's growing gallium nitride knows it's zero or one. You either get nucleation and material or you do not."

The results of this project will have tremendous ramifications, claims Bastiman. "This is the proving ground for AI material science." According to him, success will open the door to applying AI to all other growth technologies – including CVD, ALD, and PVD – as well as characterisation equipment.

Bizmuth's ultimate goal, which it is working towards with a step-by-step approach, is to employ AI as a lab operating system.

"We're going to expand to other meteorology tools, *in-situ* tools, and *ex-situ* characterisation tools, and then other deposition techniques," says Bastiman, who explains that this effort will go hand-in-hand with an expansion of the MBE Academy to the Thin-film Academy, which will also offer expertise in MOCVD, PVD and ALD technologies.

"The overall goal is that every scientific lab in the world can have access to advanced AI tools and cutting-edge knowledge in their industry, with a low barrier to entry," claims Bastiman. They are laudable goals, promising to transform our industry.

Wolfspeed: Rejuvenated by restructuring?

After starting to address its colossal debt by converting loans into shares and filing for chapter 11 bankruptcy protection, has Wolfspeed taken the first steps to a revival?

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WOLFSPEED, and in its former guise Cree, has been at the very forefront of our industry for decades. Building on its initial expertise in SiC, this spin-out of North Carolina State University, founded in the late 1980s, has trailblazed SiC substrates, high-brightness LEDs and power and RF electronics.

In recent times, driven by the vision of Wolfspeed's former CEO, Gregg Lowe, the company has streamlined its business, first carving out its LED division and then selling its RF business to Macom in December 2023.

While these moves – they have shifted the focus to SiC substrates, epiwafers and power devices – make much sense, given that the current portfolio is aligned with an electric vehicle market that is sure to climb over the coming years, it's not prevented Wolfspeed from finding itself trapped in a particularly ferocious storm. Peril has resulted from borrowing big to try and fully exploit growth in softening SiC markets, while facing increasingly stiff competition from Chinese makers of SiC substrates that are slashing prices to win sales in a sector suffering from overcapacity.

Now Wolfspeed is trying to extricate itself from this precarious position by starting to convert billion-dollar cash injections from BorgWarner, ZF and Renesas into shares, filing for Chapter 11 bankruptcy protection in late June, and trimming its wage bill by laying off 20 percent of its workforce.

But will this be enough? And even if Wolfspeed soldiers on, has it already been inflicted with irreparable damage?

Offering insight into all this and more, including crucial details into why Wolfspeed has got itself into such dire straits, is Yole Group's Principal Technology & Market Analyst for Compound Semiconductors, Poshun Chiu, who has been sharing his thoughts with *Compound Semiconductor*.

According to Chiu, Wolfspeed's problems have been exacerbated by its incredibly aggressive investment in capacity expansion, spurred on by an outlook based on design-ins rather than design wins, and optimistic forecasts. "They targeted a larger market size, much higher than Yole's numbers at the time."

Driven by these enthusiastic predictions, Wolfspeed has been spent billions and billions expanding its capacity. In North Carolina, home of its materials and epiwafer businesses, Wolfspeed's recently complemented a well-established facility with the John Palmour Manufacturing Center. Topped out last March, this latter addition, designed for the production 200 mm SiC wafers, cost $5 billion.

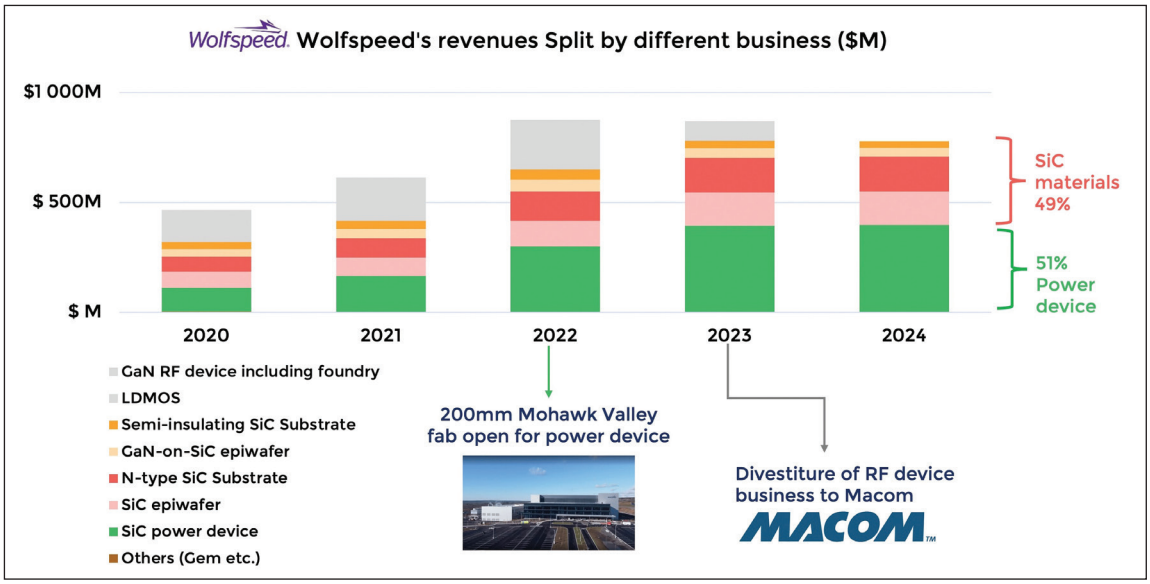
Some device production also occurs in North Carolina, using 6-inch material, but this is being phased out. "In the coming quarters they want to have 100 percent device manufacturing in Mohawk Valley," says Chiu, explaining that the plan has been to add tools to this facility – opened in 2022 as the world's first 200 mm SiC fab – over a number of years.

Underscoring how fast Wolfspeed intended to grow its business, the company also planned to build a second 200 mm fab in Mohawk Valley, plus another in Germany, with financial support from ZF.

It's not yet clear exactly how ZF, and another financial backer, BorgWarner, will recoup their substantial investments. But Wolfspeed has just announced a deal struck with Renesas, which in July 2023 loaned Wolfspeed $2 billion and agreed to a 10-year wafer supply contract. Now that loan has been converted into Wolfspeed shares, maturing in June 2031. Chiu expects similar outcomes for ZF and BorgWarner, given the lack of alternative options.

From substrates to devices

Within Wolfspeed's current portfolio of SiC substrates, epiwafers and devices, over the last few years emphasis has shifted to the production of power electronics. Yole Group estimates that back in 2020, sales of SiC power devices netted around $100 million – about a fifth of the company's revenue – and by 2024 this figure had climbed to nearly $400 million, positioning Wolfspeed as the fourth biggest supplier of this class of device. Note that this astonishing growth has been far from linear, with Wolfspeed's sales of SiC power devices flat-lining from 2023 to 2024.



➤ Wolfspeed's strategic transition in the last five years. Source: *SiC - Markets & Applications 2025* report, Yole Group.

The company's growth in SiC power devices over the last five years is crucial to its long-term prospects, given that Wolfspeed's stranglehold on the substrate market is loosening fast. As well as using substrates for internal production, the company has been selling to many of the leading producers of power electronics for decades, but its share of this market is in decline, and is now less than 30 percent, compared with around 50 percent in 2021, according to Yole Group

"The Chinese companies have improved quality a lot, and the price compared to the international players is much lower," says Chiu, explaining the additional capacity provided by Chinese SiC substrates makers contributed to overcapacity in 2024, and a price drop of 30 percent.

Chiu says that the Chinese companies are striving to win market share by compromising gross margin. Some new entrants are even selling the substrate at a price below cost. Despite this aggressive approach, prices are not expected to fall as fast in the near future – Chiu is expecting reductions of around roughly 10 percent per annum – because all the players in the SiC market are currently managing cash very carefully.

In Wolfspeed's favour is the high quality of its substrates, particularly valued for producing MOSFETs for the automotive industry. The quality of Chinese material was not as high, arguably making it better-suited for less demanding Schottky barrier diode production. However, the quality of substrates from Chinese players is getting better and better, spurred on by competition between Chinese suppliers, and the diameter of these wafes is getting larger. In 2025, at Semicon China, many domestic producers of SiC boules demonstrated 300 mm wafers. This size could unlock an opportunity to use SiC as the backplane in AR glasses, an application that promises to drive volumes to new highs.

As a device manufacturer, Wolfspeed is focusing on the most demanding application, electric vehicles, and supplying MOSFETs for use in inverters. Here, Chiu argues that Wolfspeed is competitive, with a 10 percent share of the SiC power electronics market.

"What Wolfspeed has achieved is quite significant, but it's not enough to sustain or support their ambitions, like to build a huge fab in the US, and another fab in Germany," says Chiu. "They have achieved a certain level of revenue, but somehow it's not sufficient compared to the level of investment announced."

Those now in charge of Wolfspeed will be hoping to retain existing customers and find new ones, while restructuring capital to ensure a cash flow that provides a sustainable business.

In Wolfspeed's favour is that when it comes to chip manufacture, it's still the market leader for device production on a 200 mm line. Thanks to this edge over its rivals, Chiu believes that if Wolfspeed can navigate through these difficult times, it could grow its revenue, or at least its shipments, over the next few years.

While such success would be very modest when judged against the big and bold plans of yesteryear, it might allow the company to turn a page and eventually provide some good news for its investors. They have suffered in recent years, seeing shares tumble from over $140 in late 2021 to trade below a dollar, reflecting the severe downturn in fortunes. And although the recent chapter 11 filing went down well with markets, helping to deliver some significant hikes in valuation, existing equity holders are going to have their shares cancelled, and receive 3 percent to 5 percent of the new equity. They will be hoping that Wolfspeed's survives – and on its new footing, they have good reason to be hopeful – but whether it will ever thrive again is hard to say.

Beyond disinfection: Unlocking the full potential of the UV LED

Advances in LED technology across the UVA, UVB, and UVC bands are opening transformative opportunities in manufacturing, sensing, healthcare, and beyond

BY PRATIBHA SHARMA AND SAYA HAN FROM VIOLUMAS

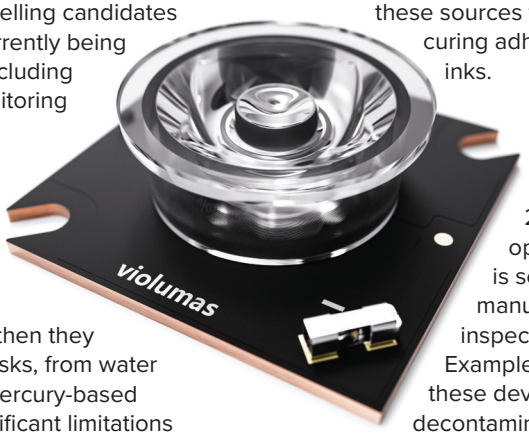
DURING the last decade, and fuelled by the Covid-19 pandemic, UVC LEDs have become synonymous with the disinfection of air, water, and surfaces. These solid-state sources, which are renowned for being compact, mercury-free and instantly switchable, have garnered a great deal of attention in public healthcare, spurring a surge in new product development.

However, since the height of the pandemic, the initial enthusiasm in the UV LED has waned. This has led makers of these devices to start targeting more mature and purposeful applications, and foster a long-term vision that's based on replacing mercury lamps and new product development. Due to their flexible form factor, narrow spectral width and high reliability, UV LEDs are now compelling candidates for many applications, and are currently being deployed in a number of fields, including spectroscopy, environmental monitoring and medical devices.

Since the late 1800s, it's been well established that UV light offers health benefits, by killing bacteria and viruses. UV lamps based on mercury vapour were launched in the 1930s, and since then they have been used for a variety of tasks, from water purification to curing. But these mercury-based lamps are far from ideal, with significant limitations that include bulky form factors, hazardous materials, limited spectral control, and long warm-up times. Due to these weaknesses, they are unsuitable for many demanding industries.

The introduction of UV LEDs has opened new doors, with this promising alternative enabling more flexible designs. Initially, these emitters struggled to match the optical performance of mercury lamps, falling short in output power and lifetime, particularly for shorter wavelengths. But with significant advances in epitaxy, packaging, and thermal management, UV LEDs are now hitting performance levels once considered unattainable.

A key strength of the UV LED over the mercury lamp is that its emission profile can be tailored to a particular application. For tasks such as curing and 3D printing, mercury lamps were once the source of choice – but in order to realise sufficient spectral purity, they must be combined with expensive filters. What's more, as lamps have long warm-up times, they have to be left on, leading to excessive energy consumption. Turning to UV LEDs addresses these drawbacks, while enabling faster production cycles, reduced thermal budgets, the elimination of start-up times and delivery of uniform exposure. Moreover, controlling the LED at the chip level allows dosage to be precisely managed, enabling consistent curing. Alongside these strengths, UV LEDs have flexible form factors that ease integration, making these sources the global standard for curing adhesives, coatings, and inks.



➤ Above: VioBeam Ultra-Narrow Beam UV LED module with integrated optics for focused 10° beam, designed for precision industrial applications

One area where the development of high-power 265 nm and 255 nm UV LEDs is opening new possibilities is semiconductor manufacturing and inspection equipment. Examples of the uses of these devices include surface decontamination in cleanroom environments, wafer edge cleaning, and lithography-related processes benefitting from precise, localised UV exposure.

In the photovoltaic industry, UV LEDs are also being used for numerous applications. They include deployment in spectrum-tailored applications, such as designing solar simulators to emulate the solar spectrum. UV LEDs are also being used for solar panel inspection, to detect contamination.

Yet another application for today's UV LEDs are as the key light sources in absorption and fluorescence spectroscopy systems. These sources are helping

to detect pollutants such as ozone, sulphur dioxide, aromatics, and many other organic compounds, with precision and scalability. Here, the motivation behind the steady replacement of mercury lamps with UV LEDs is not limited to environmental concerns, but extends to the merits of superior control, stability, and operational efficiency. Note that thanks to a lower cost-of-ownership, UV LEDs are increasingly explored as viable alternatives to UV lasers as well.

In addition to all these industrial applications, UV LEDs are being deployed in various medical applications that are not associated with disinfection. Narrowband UVB LEDs are being used to treat skin conditions, such as psoriasis and vitiligo, offering safer and more portable alternatives to conventional phototherapy equipment; and those emitting in the UVA are enabling progress in photodynamic therapy, where light-activated drugs selectively target tissues.

In terms of longevity, the UVC LED has improved a great deal over the past decade. What was once a major limitation is no more, with typical lifetimes now 10,000 to 20,000 hours, which is acceptable for many of today's applications. And further gains on this front, under real-world conditions, are to be expected, given the continued advances in material quality, chip design, and packaging. Devices are also expected to benefit from advanced thermal management technologies that will improve performance.

Helping to increase the competitiveness of UV LEDs is a reduction in their price. That for UVA LEDs has dropped substantially with volume production, and prices for UVB and UVC LEDs are continuing to fall, encouraging early adoption. As manufacturing techniques mature and production yields improve, the trend of a fall in the cost-per-milliwatt should continue.

During the initial adoption phase of UV LEDs, many will overlook the importance of system integration – but it is a key consideration. To produce the best possible UV systems, they have to be holistically designed to optimise optical distribution, manage thermal budgets, and ensure reliability. Additional factors are that materials exposed to deep-UV must be long-lasting, and appropriate shielding or interlocks must be incorporated to protect users. In this regard, the companies that are offering complete, ready-to-integrate UV LED solutions – including optics, drivers, thermal management, and safety features – will have a distinct advantage as adoption continues to grow.

Given the progress of the UV LED over the past five years, it is clear that we are now approaching a critical inflection point. Disinfection provided the catalyst that introduced UV LEDs to a broad market, but their future adoption extends much further. While the pandemic drove a surge in consumer products based on the UV LED, adoption of these sources has evolved as they start to serve in more long-term solutions targeting healthcare environments, such as mobile units and surgical rooms.

In the coming decade, UV LEDs are on course to drive innovations in high-precision manufacturing, real-time environmental monitoring, next-generation medical therapies, and scientific research. Their capability to deliver targeted, efficient, and sustainable optical power aligns perfectly with the global push for smarter, greener technologies. Thanks to the current AI boom, UV LEDs are destined to work hand-in-hand with machine learning technologies to drive development of smart systems. For example, AI-enabled systems could dynamically control UV LED arrays to fine-tune curing processes in advanced manufacturing, optimise UV dosage in real-time water monitoring, and personalise phototherapy treatments, based-on patient data. As materials science, photonics, and data science converge, UV LEDs are poised to become not just components, but core enablers of intelligent, responsive systems across multiple sectors.

At Violumas, a producer of UV LEDs, we are excited about the role that these sources can play in reshaping industries and enabling solutions once considered out of reach. Through continued innovation, collaboration, and investment, UV LEDs are poised not merely to illuminate the future, but transform it.

Sealing tech to balance performance, maintenance and lifecycle value

Greene Tweed's high-performance seals enable compound semiconductor manufacturers to thrive in a volatile market by optimising the total cost of ownership while providing robust protection against harsh processing conditions

BY ALAN MAHER AND PRAGATI VERMA FROM GREENE TWEED

THE compound semiconductor industry is entering a period of promise and disruption. Sales are projected to hit $25 billion by 2030, spurred on by an average annual growth rate of almost 13 percent, according to semiconductor market research analyst Yole Group. What is fuelling this surge? It's the booming demand for GaN and SiC, driven by the rise of electric vehicles, 5G networks, and renewable energy tech.

While this growth is welcome, it comes with challenges. There's a backdrop of tightening global regulations, fluctuating tariffs, export bans and geopolitical tensions – factors that disrupt the supply of GaN and SiC. And on top of that, there's the cyclical nature of market demand, threatening to turn forecasts upside down.

For businesses in this space, managing risk and profitability often comes down to one question: how do we enhance our operations while controlling costs, especially amidst volatility?

Why cost-of-ownership matters in uncertain times

One of the keys to thriving in an unpredictable market is to give a lot of consideration to the total cost of ownership for compound semiconductor manufacturing tools and processes. The production of compound semiconductor epiwafers and devices tends to require specialised equipment, unique materials and complex processing steps, all of which drive up initial investment and ongoing operational costs.

Due to all these factors, manufacturers must look beyond upfront costs of major equipment to consider long-term expenses associated with even the smallest components, such as the elastomeric seals in their equipment and tools.

At Greene Tweed, we assist with this task by engineering sealing solutions that outperform and outlast in the world's harshest semiconductor manufacturing applications. Many prominent chipmakers depend on our portfolio of perfluororoelastomer (FFKM) Chemraz and fluoroelastomer (FKM) Fusion seals to manufacture silicon and compound semiconductor devices.

As the total cost of ownership becomes a central concern, our portfolio of advanced seals strikes the ideal balance between performance, maintenance, and lifecycle value. By focusing on enhancing maintenance cycles and ensuring higher equipment uptime, our seals help compound semiconductor manufacturers realise better yields and profitability, even

during challenging times. The crucial balance between performance, maintenance, and lifecycle value is even more crucial for tools and processes exposed to extreme plasma and chemical environments, such as those found in etching and deposition chambers, where seals often bear the brunt of these costs. Faulty or inefficient seals are highly detrimental, as they can lead to equipment failures, unplanned downtime, and ultimately suboptimal yields.

When it can't fail

To understand the critical importance of seals in the compound semiconductor industry, consider the pendulum valve. Located inside etch and deposition chambers in fabs, it is an indispensable component in compound semiconductor manufacturing processes involving 200 mm wafers. The roles of these sophisticated valves are to regulate critical gas flow and help maintain the vacuum conditions required for precise wafer processing. Success on these fronts ensures efficient etching or deposition.

The performance and the longevity of pendulum valves heavily relies on their seals. Harsh chemicals and plasma environments can rapidly degrade seals, leading to erosion, sticking, and cracking. Seal quality can also diminish through constant dynamic motion, such as compression, decompression, and rotation, as this creates friction, accelerates wear and reduces lifespan. Add the extreme heat from wafer fabrication, and challenges faced by seals skyrockets. Even the smallest of failures can disrupt valve operation, leading to costly delays, unplanned downtime, and expensive repairs.

➤ High-performance Fusion seals, built to withstand extreme temperatures, high pressures, corrosive chemicals, and volatile fluids.

The good news is that our high-performance seals, such as Fusion – and in particular Fusion F07 – are built to withstand extreme temperatures, high pressures, corrosive chemicals, and volatile fluids. These strengths enable manufacturers to improve the performance and the lifespan of their pendulum valves in demanding vacuum applications.

But what happens if a seal in a pendulum valve fails? The consequences are dire, as the entire valve goes down with it. One ramification is that the vacuum needed for wafer processing collapses, leading to chamber contamination and ruined wafers. There's also the distinct possibility of a catastrophic chain reaction, involving material scrapping, production delays, and equipment damage. Persistent failures can even destroy other high-cost components or compromise the entire tool, sending repair costs through the roof. What's abundantly clear is that seal reliability is a non-negotiable, ensuring that these valves perform flawlessly during semiconductor plasma processing.

Fusion: Balancing performance and costs

Pendulum valves aren't alone. There are a number of tools and processes, including lid seals and slit valve seals in fabs, that rely on our Fusion sealing solutions to deliver certainty during crucial operations.

Engineered to bridge the gap between performance and cost, Fusion F07 is a dependable FKM solution that's tailored for the compound semiconductor and legacy semiconductor market.

➤ For compound semiconductor fabs, Chemraz G-Series prevent contamination while withstanding aggressive conditions.

For compound semiconductor fabs managing legacy equipment for chip production, the Chemraz G-Series delivers exceptional versatility, and the performance needed to meet demanding manufacturing challenges

The material used to produce this seal ensures an ideal balance between affordability and chemical resistance, making F07 a natural choice for 200 mm and smaller wafers widely used to make a vast range of compound semiconductor devices. Operating continuously at temperatures of up to 180°C, and including excursion service temperatures of up to 220°C, F07 has a minimum expected lifetime of six months, outperforming standard FKM seals in these applications. Additionally, F07 has a lower total-cost-of-ownership than a number of premium materials, making it an economical yet high-performing solution.

Developed specifically for CVD and dry plasma etch equipment that's used in the manufacture of flat panel displays, the 707 family of seals ensures exceptional chemical resistance while maintaining reliability and minimising contamination. For plasma equipment applications, there's also the Fusion 706, a versatile option that handles everything from etch and plasma-enhanced CVD to plasma ashing processes. Note that the 706 is also suitable for systems requiring low sealing force materials, such as bonded slit valve gates.

Our Fusion products can assist with efforts to trim chip production costs by upgrading from 150 mm to 200 mm wafers. Compared with the production of silicon devices, manufacturing those that are based on compound semiconductors, such SiC, is inherently more expensive, due to high material costs, complex processes, and lower yields. Many companies aim to cut expenses by retrofitting older tools with software and component upgrades, instead of investing in entirely new equipment. For these efforts, we offer upgraded seal kits, to enhance the performance of outdated tools.

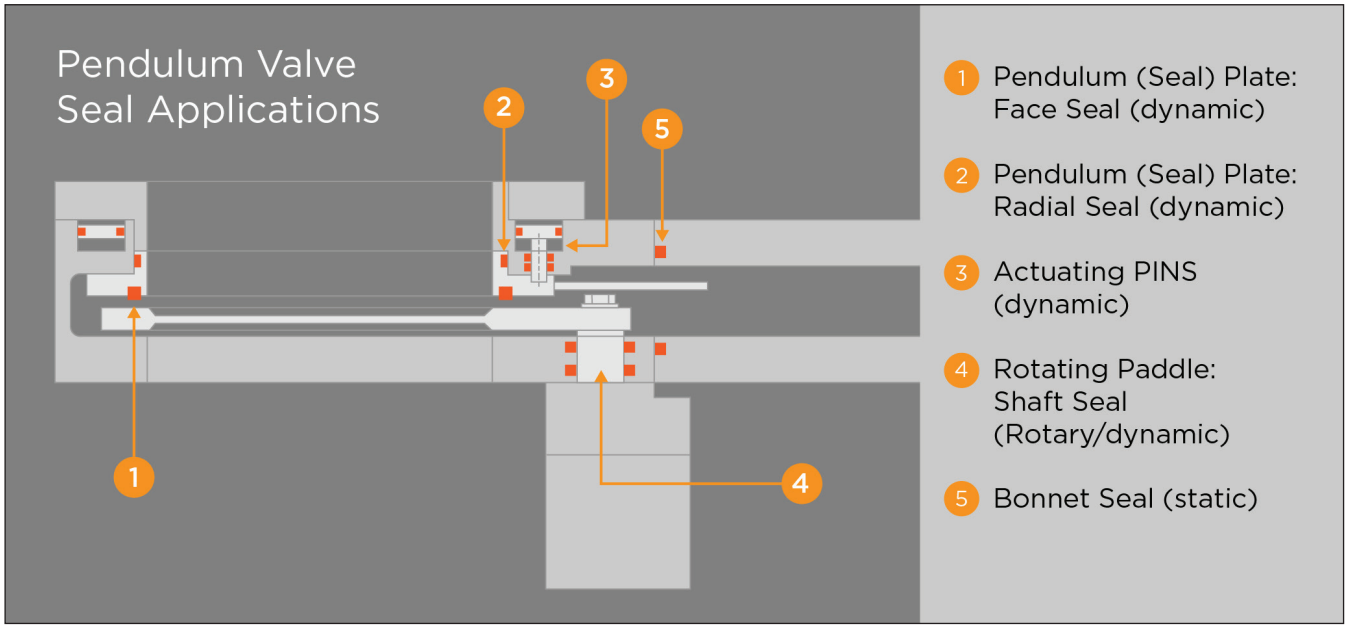
By integrating advanced sealing solutions, these chipmakers can optimise older refurbished equipment, preventing contamination and maintaining cleanroom standards. As well as increasing throughput and yield, this approach supports the growing demand for compound semiconductors while maximising profitability.

Chemraz: Outperforming in the harshest conditions

Manufacturers of compound semiconductor devices often operate in incredibly demanding industrial conditions, which may involve extreme temperatures, aggressive chemicals, and a plasma environment. These conditions place significant stress on seals and other components. In such applications, prominent chipmakers tend to turn to our Chemraz FFKM seals to prevent contamination while withstanding aggressive conditions. These seals play a critical role in chip production, where anything less than the best simply won't do.

For compound semiconductor fabs managing legacy equipment for chip production, the Chemraz G-Series delivers exceptional versatility, and the performance needed to meet demanding manufacturing challenges. This FFKM material is engineered to excel in aggressive plasma chemistries and dynamic sealing applications, making it a reliable choice for demanding manufacturing environments.

The Chemraz G-Series stands out for its superior plasma resistance, performing reliably in oxygen and fluorine-rich environments. Its ability to withstand such harsh conditions ensures



➤ Located inside etch and deposition chambers in fabs, pendulum valves regulate critical gas flows and help maintain vacuum conditions required for precise wafer processing.

consistent performance, even in the most demanding applications. Whether used as a door seal or an actuator O-ring, Chemraz significantly reduces particulation while boosting operational uptime, contributing to smoother and more efficient manufacturing processes.

Working in tandem, the Chemraz FFKM and Fusion FKM series provide a complete range of sealing solutions for compound semiconductor manufacturers. Designed for both legacy systems and the latest tools, these materials offer the durability and flexibility needed to support every stage of production. The goal is simple: ensuring efficiency and reliability throughout the entire manufacturing process.

If you are searching for the right seal for your application, Greene Tweed's Elastomer Selection Guide makes it very easy by simplifying the process of choosing the most suitable seal for every application.

This proven process considers key factors, such as material compatibility, seal geometry and operating conditions, to develop solutions tailored to the specific needs of semiconductor manufacturing. By aligning seal types with precise engineering criteria, the Right Seal Pyramid methodology addresses key challenges, like chemical resistance, mechanical stress and installation accuracy, to ensure reliable performance in the harshest semiconductor manufacturing environments.

Prepare for the next upswing

Selecting the right components and optimising the total cost of ownership can pay dividends in an uncertain market. After all, the cyclical nature of the semiconductor industry is no secret. While the timing and breadth of these cycles are increasingly difficult to predict, it is critical to be ready for the next upswing. Navigating uncertainty, whether from tariffs, supply chain shocks or technological disruption, demands strategic investment in the right materials and designs for components such as seals.

For over 160 years, our company, Greene Tweed, has been applying our expertise in materials science and engineering to support innovation in the industries we serve.

By focusing on reliable processes, high-quality sealing solutions and advanced technologies, we are helping semiconductor manufacturers improve their operations and scale efficiently. Our support plays a key role in fostering long-term growth and ensuring the reliability of critical components in the semiconductor industry.

As the compound semiconductor industry braces for a year of typical shifts and unpredictable headwinds, one thing is clear.

In this environment, those taking a strategic approach to managing the total-cost-of-ownership by factoring in not just purchase price but also the reliability, flexibility, and resilience of small indispensable components, such as seals, will be better positioned to weather volatility and maintain profitability.

Elegant approaches for equipping PICs with lasers

At this year's European Conference on Integrated Optics, researchers outlined a number of sophisticated strategies for the monolithic integration of lasers and photonic integrated circuits.

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

FOR OUR industry, AI is a massive win-win. On the one hand, by drawing on this technology, we get to run labs and fabs more efficiently, benefitting from the likes of streamlined processes and the opportunity to detect and classify defects with more consistency. And on the other hand, we get to grow our revenues by supporting the roll-out of this new form of intelligence, via the supply of wide bandgap power electronics that trims the electricity bills of AI data centres, and the shipment of laser diodes, a key component in high-data-rate optical links.

Without doubt, the biggest name in AI at the component level is Nvidia, currently worth more $3 trillion. It has a roadmap for advancing its technology that includes the release of a silicon photonics chip operating at 1.6T, now slated for early 2026.

While at first glance Nvidia's plans might appear as another milestone in the increasing integration of compound semiconductor devices, that's not the case – the laser that's providing the light source for optical communication is an external device. And from a historical perspective, that's not surprising. Consider these four pioneers of silicon photonics: Luxtera, Kotura, Mellanox and Ayar Labs. All have developed ground-breaking photonic integrated circuits (PICs) with external lasers.

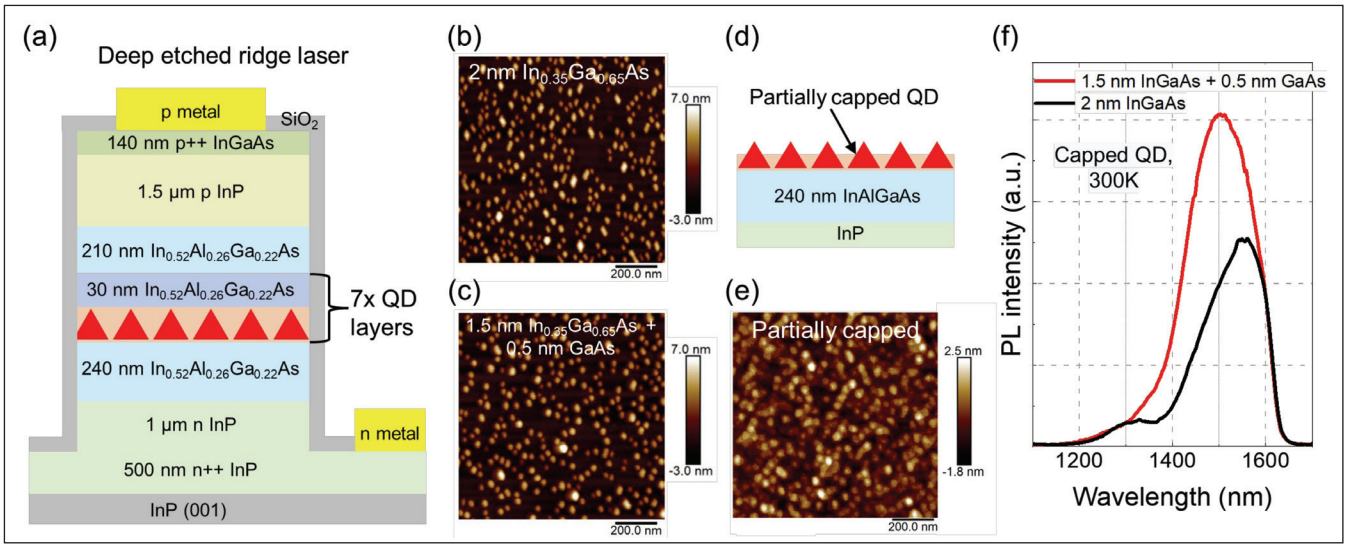
This type of approach is not the neatest of solutions, as having the laser on the chip leads to a smaller footprint and supports optical chip-to-chip communication, which is faster than that based on electrons and copper wires.

Significant progress on this front has come from the group of John Bowers at the University of California, Santa Barbara. More than a decade ago Bowers and his co-workers united InP-based lasers with silicon chips using die-to-wafer bonding, with the technology commercialised by Intel and now in the hands of Jabil, which is manufacturing 800G products.

As well as die-to-wafer bonding, there are a number of other approaches to equipping PICs with an on-chip laser. Alternatives include flip-chip technologies, micro-transfer methods that offer parallel processing, and arguably the most elegant solution of all, monolithic integration.

Efforts at fabricating lasers in this most attractive manner, which could help advance PIC technology, featured at this year's European Conference on Integrated Optics (ECIO), held in Cardiff, UK, between 10-12 June. At this meeting, researchers from academia championed the promise of InAs quantum dots grown on InP, rather than the more common foundation, GaAs, and also discussed the promise of GeSn lasers.

Compared with their quantum-well counterparts, quantum-dot lasers have a number of advantages. In addition to a lower threshold current, temperature insensitivity, and a stronger carrier confinement that ensures enhanced tolerance to optical reflectance, they include the mitigation of dislocation-induced performance degradation when integrated on silicon-based platforms, commonly used to produce PICs.



➤ Figure 1. (a) A team from Cardiff University and University College London has produced a portfolio of deep-etched ridge-waveguide quantum-dot lasers. (b) and (c) Atomic force microscopy offers insight into the morphology of the quantum dots, produced using different pre-layers. (d) and (e) An illustration and an atomic force microscopy image of partially capped quantum dots. (f) Photoluminescence spectra of uncapped quantum dots.

Now reasonably mature, lasers based on InAs-on-GaAs quantum dots are capable of providing emission at around 1.3 μm. But they are not able to reach longer wavelengths, such as those that are found in the C- and L-bands, and employed for a variety of applications – they include fibre-optic communication and eye-safe optical sensing, and further into the infra-red, the detection of gases and biomolecules.

A compelling candidate for reaching these longer wavelengths is an ensemble of InAs quantum dots grown on InP, rather than GaAs. However, switching from a GaAs to InP foundation reduces strain from around 7 percent to 3 percent, making it more challenging to produce high-quality dots.

Optimising pre-layers

One partnership working on this problem is a collaboration between Cardiff University and University College London. This team has produced a portfolio of deep-etched ridge-waveguide lasers on InP substrates, with structures grown using a close-coupled MOCVD tool.

Detailing this work at this year's ECIO, Zhao Yan from Cardiff University explained that he and his co-workers had investigated three quantum-dot configurations: uncapped, partially capped and fully capped.

Their study began by comparing uncapped quantum dots grown on two-different pre-layers: 2 nm-thick $In_{0.35}Ga_{0.65}As$; and the pairing of 1.5 nm-thick $In_{0.35}Ga_{0.65}As$, followed by 0.5 nm-thick GaAs.

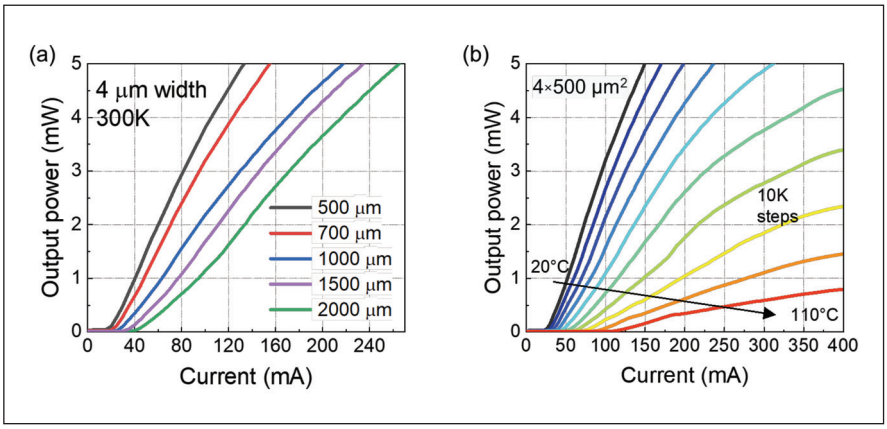
Sharing atomic force microscopy images of both samples with delegates in the auditorium (see Figure 1), Yan remarked: "As you can see, by adding the gallium arsenide layer you can achieve more in-plane symmetry."

Additional insights provided by atomic force microscopy are that the quantum-dot density is about 3.4 x 10^{10} cm^{-2}, and that a partial capping process retains the morphology of these nanostructures.

Photoluminescence measurements underscore the superiority of the pre-layer comprising 1.5 nm-thick $In_{0.35}Ga_{0.65}As$ followed by 0.5 nm-thick GaAs, with quantum dots on that foundation producing a more intense signal.

Yan and co-workers have produced a portfolio of deep-etched ridge-waveguide lasers that feature seven layers of InAs quantum dots. These devices have been fabricated from epiwafers with a very smooth surface, thanks to step flow growth.

The team's edge-emitters, produced with a top-contact metal configuration and SiO_2 passivation, have ridge widths varying from 4 μm to 10 μm. Fabrication



➤ Figure 2. (a) Ridge-waveguide InAs quantum-dot lasers produced by a team from Cardiff University and University College London have an output power of several milliwatts. (b) Lasing occurs over a wide temperature range for an edge-emitter with dimensions of 4 μm by 500 μm.

included thinning the substrates, and cleaving into laser bars with cavity lengths of 300 μm to 2000 μm. Facets were left uncoated.

"The lasing yield is more than 98 percent," remarked Yan, who pointed out that these emitters have a low threshold current. Driven in pulsed mode, using a pulsed width of 1 μs and a duty cycle of 1 percent, lasers with a 300 μm cavity have a threshold current of 17 mA, while those with a 1000 μm cavity have a threshold current of 28 mA. According to the team, these values are considerably lower than those for comparable lasers grown by MOCVD.

Yan and co-workers have recorded output powers of several milliwatts for their devices, and lasing at up to 120°C for an edge-emitter with dimensions of 4 μm by 500 μm (see Figure 2).

The team are also working on the growth of their lasers on silicon substrates. For this effort, they are collaborating with researchers at CEA-Leti, who are providing initial buffer layers, grown on 300 mm silicon substrates without any off-cut. Stacking faults can be an issue when using this platform, but Yan explained that these imperfections can be reduced by minimising strain through optimisation of the epistructure.

Indium flushing

One of the weaknesses of InAs-on-InP dots, stemming from the relatively small lattice mismatch and the anisotropic surface diffusion of indium atoms, is the formation of elongated nanostructures with a significant size dispersion. This morphology is far from ideal, leading to broad photoluminescence and ultimately lasers impaired by insufficient gain, a high threshold current density and limited high-temperature performance.

To address these concerns, an indium-flush technique has been developed by a collaboration led by Jiajing Yuan and co-workers from UCL, and supported by researchers from Swansea University, SuperSTEM, the University of York, Cardiff University, University Grenoble Alpes and the University of Leeds.

Yuan and co-workers assessed the impact of indium flushing by producing epistructures with and without this approach, before scrutinising them, fabricating lasers and recording their emission characteristics.

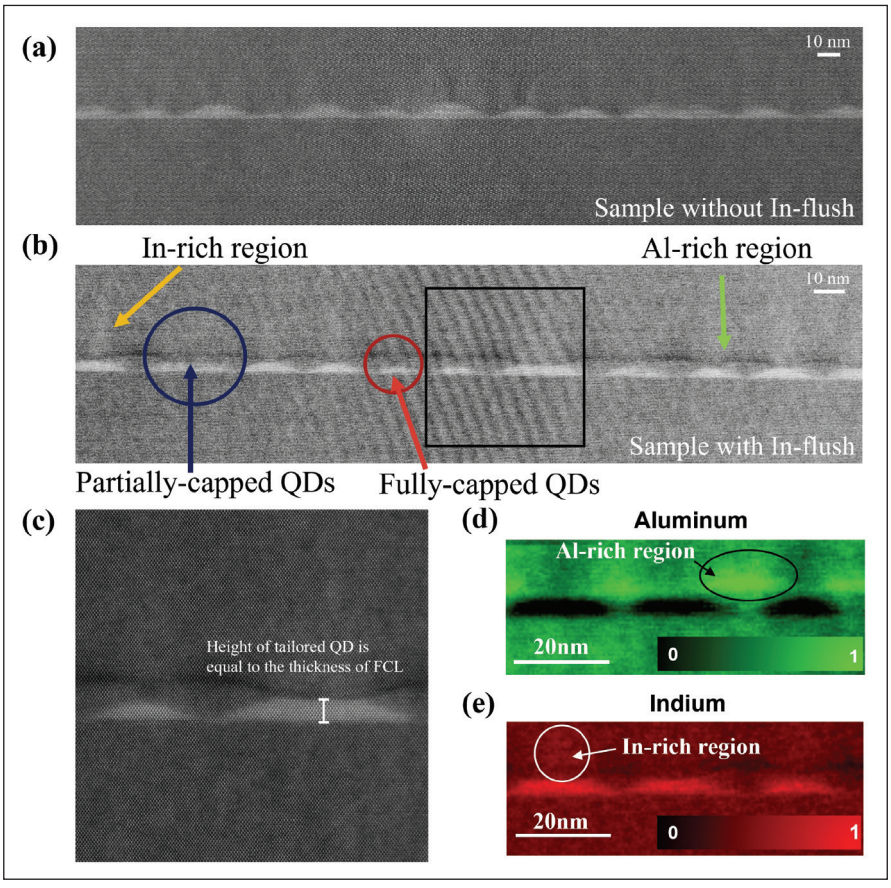
For this work, InP substrates were loaded into an MBE reactor, prior to the growth of a lattice-matched InAl(Ga)As buffer, and the growth of nanostructures – they tended to be quantum dots rather than elongated quantum dashes, thanks to optimisation of the growth parameters. A thin InAl(Ga)As capping layer followed the growth of the quantum dots, before annealing enhanced quantum dot uniformity, by means of indium flushing. All quantum dots were encapsulated with a second InAl(Ga)As capping layer, to fully cover these nanostructures.

Yuan shared high-angular dark-field images of as-grown quantum-dot samples with and without the indium flush (see Figure 3).

"You can see that for samples without the indium flush, the average height of the quantum dots varies," remarked Yuan. "But for the samples with indium flush, most of the quantum dots are truncated to the same height as the first capping layer thickness."

The researchers have also investigated their samples with electron-energy-loss spectroscopy, identifying indium-rich and aluminium-rich regions, arising from strain redistribution and segregation/desorption of indium from the first capping layer, during the annealing step.

Yuan and co-workers have fabricated laser structures that feature seven stacks of quantum dots with a process that includes indium flushing and growth by both MBE and MOCVD. Epitaxy begins by loading InP substrates in the MBE chamber and depositing a 200 nm-



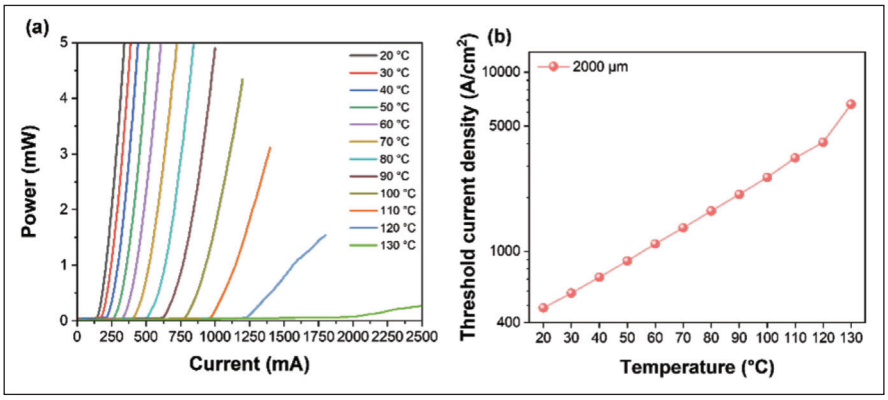
➤ Figure 3. A collaboration led by researchers from University College London has considered the impact of indium flushing during MBE growth of InAs nanostructures. High-angular dark-field images (a) and (b), as well as (c) – that's the area of the black box in (b) – show that with indium flushing, quantum dots shorter than the first capping layer are fully encapsulated, while taller dots have a height that's governed by the thickness of the first capping layer. (d) and (e) Electron-energy-loss spectroscopy identifies indium-rich and aluminium-rich regions, resulting from strain redistribution and the segregation/desorption of indium from the first capping layer during annealing.

thick *n*-type $In_{0.524}Al_{0.476}As$ buffer, an $In_{0.528}Al_{0.238}As$ spacer layer that provides a lattice-matched foundation, and a seven-layer stack of quantum dots, formed by depositing 6.8 monolayers of InAs. To manipulate dot morphology and control the strain distribution, this structure includes 2 nm-thick $In_{0.359}Al_{0.323}Ga_{0.318}As$ stressor layers, followed by annealing at 515°C under arsenic overpressure, as part of the indium flush. A *p*-type $In_{0.528}Al_{0.238}Ga_{0.234}As$ layer and an $In_{0.524}Al_{0.476}As$ layer are then added, plus a 10 nm-thick InGaAs protection layer, prior to the transfer to an MOCVD tool, used to add a 1700 nm-thick zinc-doped InP cladding layer and a 200 nm-thick zinc-doped InP contact layer.

These epiwafers were processed into Fabry-Pérot lasers with a 15 μm-wide ridge, a cavity length of 2000 μm, and an emission wavelength of around 1.6 μm. Photolithography and wet-etching defined the ridge waveguides, and a 400 nm-thick SiO_2 layer provided passivation. After adding ohmic contacts, laser bars with a cavity length of 2000 μm were formed by cleaving.

Characterisation of these lasers, which do not include facet coatings, included driving them with 1 μs pulses at a duty cycle of 1 percent. This determined a threshold current density of only 69 A cm^{-2} per quantum-dot layer.

"This is the lowest threshold current density per quantum-dot-layer for C-to-L-band InAs-on-InP quantum dot lasers on InP (001) substrates," remarked Yuan, who added that the team's lasers have a linear relationship between threshold current density and temperature up to 120°C (see Figure 4).



➤ Figure 4. (a) Fabry-Pérot quantum-dot lasers produced by a collaboration led by researchers at University College London can operate at up to 130 °C, when driven by 1 μs pulses at a duty cycle of 1 percent. (b) The threshold current density of these lasers has a linear increase with temperature up to 120 °C.

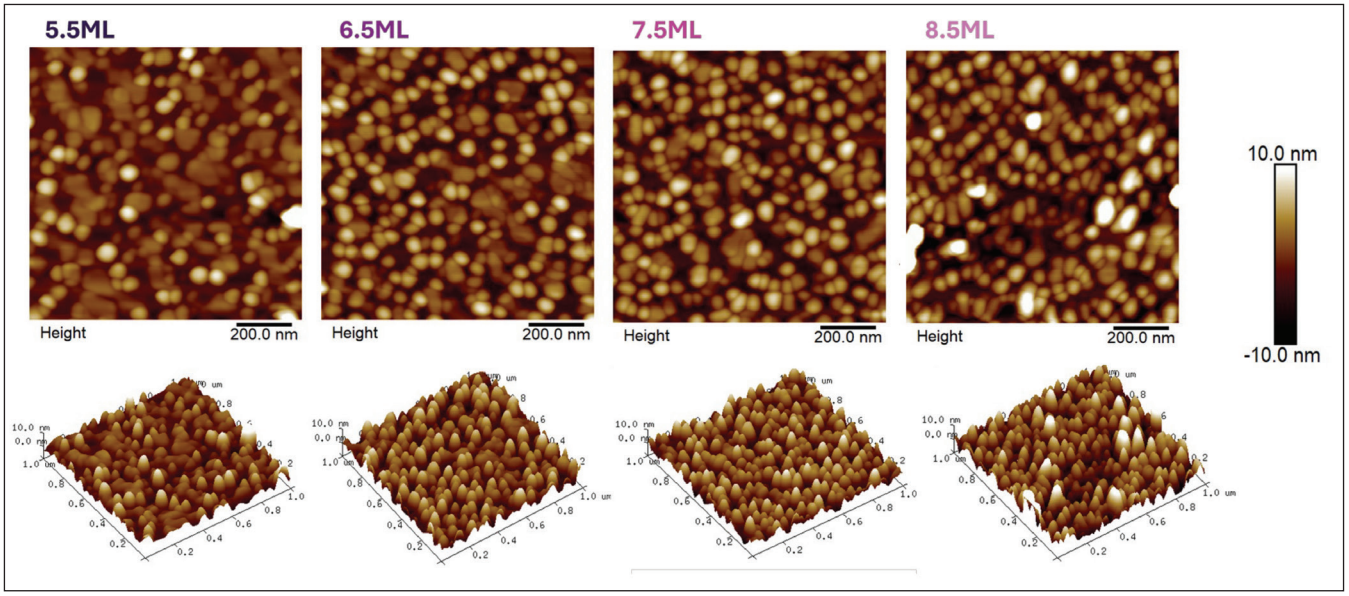
Stretching to the mid-infrared

It's possible for the emission of InAs-on-InP quantum dots to reach 2 μm or more, allowing them to be deployed in a range of applications, including the light source for lidar, as well as the detection of biomolecules and gases such as CO, CO_2, N_2O and CH_4.

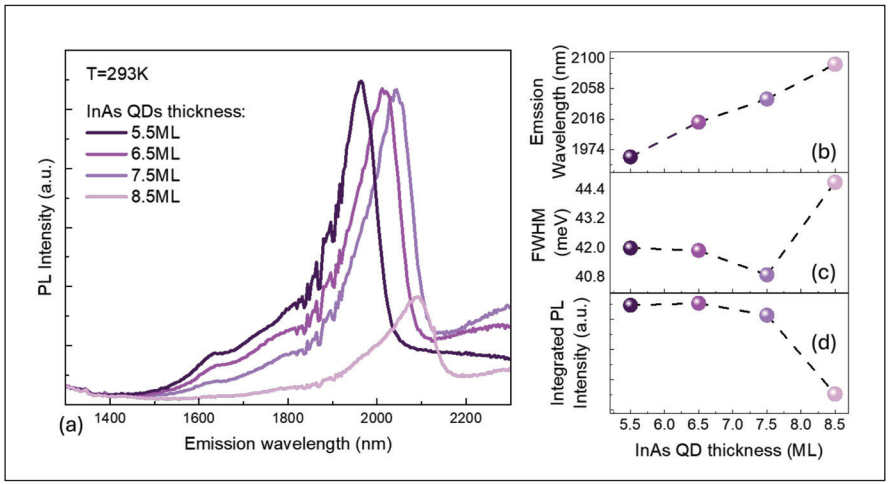
At this year's ECIO, Yangqian Wang from UCL discussed this opportunity and described the devices she has produced in collaboration with departmental colleagues and researchers at the University of Glasgow, Lancaster University and Cardiff University.

Producing high-quality quantum dots that emit at these wavelengths is not easy, as these nanostructures tend to be elongated, forming what's known as quantum dashes.

"Even though people have done a really good job, none of them have done a 2 μm laser source," according to Wang, who claimed that they are now breaking through this barrier by supressing anisotropic diffusion with a high InAs growth rate, arsenic overpressure, and a low growth temperature.



➤ Figure 5. A partnership between University College London, the University of Glasgow, Lancaster University and Cardiff University used atomic force microscopy to compare the morphology of mid-infrared InAs quantum dots with 5.5, 6.5, 7.5 and 8.5 monolayers of InAs.



➤ Figure 6. (a) Room-temperature photoluminescence of mid-infrared InAs quantum dots, along with plots of (b) emission wavelength, (c) full-width at half-maximum, and (d) integrated photoluminescence intensity.

Wang and co-workers have used atomic force microscopy to evaluate the quality of dots produced with the deposition of 5.5, 6.5, 7.5 and 8.5 monolayers of InAs (see Figure 5). This work showed that as the number of monolayers increased from 5.5 to 7.5, the dots exhibited improved shape uniformity, and an increase in density, rising from 9.4×10^9 cm^{-2} to 2.01×10^{10} cm^{-2}.

Increasing the number of monolayers to 8.5 led to a deterioration in quality, highlighted by a reduction in photoluminescence intensity.

Building on this, Wang and co-workers have optimised their III-V ratio and growth temperature, with the best results obtained at values of 27 and 495°C.

➤ This year's European Conference on Integrated Optics included an hour-long session entitled 'European Research Council Funding/ Networking'. Credit: Chris Hodges.

These optimised conditions have been employed to produce lasers with a five-layer stack of InAs quantum dots. According to transmission electron microscopy images, these structures are quantum dots rather than dashes – but the fifth layer has a reduced density of dots, which are larger. Wang says that this suggests that the team needs to devote more effort to optimising the structure.

Measurements on Fabry-Pérot devices with uncoated facets have allowed the team to claim the first room-temperature InAs quantum-dot lasers with an emission beyond 2 μm. The team's device, capable of operating at up to 50°C and having a threshold current density of 589 A cm^{-2}, has an emission wavelength of 2.018 μm.

The promise of GeSn lasers

While it's possible to introduce III-Vs into silicon lines to equip silicon PICs with a laser, it's preferable to use a material system that's less different. With germanium already used in detectors, it offers a great deal of compatibility – and while it's naturally indirect, under significant strain it exhibits a direct bandgap.

Looking into the possibilities of germanium and its related alloys for making lasers is Donguk Nam from KAIST, who discussed the progress of his team, and this field, at ECIO.

Nam explained that if germanium is subjected to about 2 percent of biaxial strain, it can transition from an indirect to a direct bandgap material. However, while 2 percent may not initially sound that high, it is, with Nam warning that a strain of just 0.2 percent can cause a wafer to break.

To realise a sufficiently high degree of strain to ensure a direct bandgap, in the 2010s Nam initially pursued nanobridge structures, before turning to strained wires.

"We put [them] in a cavity, and we got pretty nice single-mode lasing [under optical pumping]," explained Nam, who added that other groups have been able to replicate this success.

However, while these results were promising at the time, theoretical work has indicated that it would be very challenging to realise practical lasers.

Due to this, Nam started to consider adding tin to germanium, a move inspired by work from a team at the Jülich Research Centre, Germany that produced optical lasing from this material system.

While initial thresholds for pumping were very high, they have plummeted over the years. Helping with this success is Nam and his colleagues, who have developed a process involving deposition of initially amorphous GeSn, and the use of aspect ratio trapping, which localises defects at the neck of the structure to enable the growth of high-quality single-crystal GeSn on top of an insulator. This material provides lasing under optical pumping, with a threshold of around 1 kW cm^{-2}. Nam and co-workers have also been able to tune the emission of their lasers, by exploiting the mechanical resonance of their structures.

Other groups have reported electrically-pumped GeSn lasers, but they require cryogenic temperatures, so this class of device is unlikely to provide an on-chip light source in the foreseeable future. Lasers based on quantum dots are clearly far more advanced, and as the work at ECIO shows, they continue to progress. When they will make an impact in the PIC industry is not yet clear – but with interest in AI rocketing, maybe these devices will soon be in the right place at the right time.

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Cost-effective SiC

Novel 150 mm SiC engineered substrates, produced using dummy-grade material reuse, unlock the door to cost-effective manufacture of 1200 V SiC MOSFETs

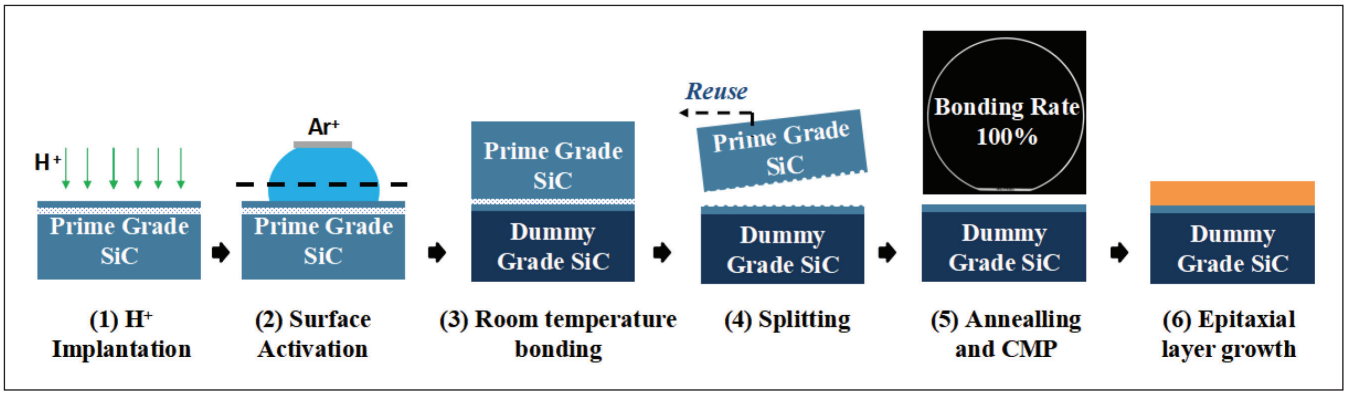
BY XINHUA WANG AND XINYU LIU FROM INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCE, YUHAO ZHANG FROM VIRGINIA TECH, AND FENWEN MU FROM TJ INNOVATIVE SEMICONDUCTOR SUBSTRATE TECHNOLOGY COMPANY

WITHIN the SiC industry, there's an urgent need for expanded production capacity of SiC substrates, to support the growth of this sector. Hampering efforts to fulfil this demand is the low yield of nearly defect-free substrates suitable for MOSFET manufacture – yield for 'prime-grade' material is typically just 40-60 percent. Falling short and leading to significant manufacturing inefficiencies are the inferior low-grade 'dummy' substrates, which are naturally produced during the growth and refining of 6-8 inch SiC and often disposed of. Due to these inefficiencies, alongside the complexity, high-energy requirements and challenges associated with the growth of bulk SiC, these substrates have a number of weaknesses. They are renowned for their high carbon footprint and high production cost, often accounting for more than 50 percent of the cost of the MOSFET.

To address this bottleneck, our partnership between the Institute of Microelectronics at the Chinese Academy of Science, Virginia Tech, and TJ Innovative Semiconductor Substrate Technology Company has introduced a novel 150 mm single-crystal SiC-SiC composite substrate, realised with surface-active bonding (SAB) technology. By turning to this engineered substrate, it's possible to re-use dummy-grade SiC substrates and recycle each prime-grade wafer over 30 times – or, to put it another way, we can extract over 30 thin layers from each prime-grade wafer.

One of the key merits of this approach is that our engineered substrate is capable of potentially cutting costs by 40 percent, compared with prime substrates. In addition, our technology is more sustainable than other approaches, thanks to waste material reuse that avoids the need for new materials. Note that there is no use of poly-SiC substrates with our methodology.

To illustrate the performance and the strengths of our new engineered-substrate technology, we have undertaken a holistic set of experiments, from substrate bonding and epitaxial growth to device fabrication and circuit testing. We have carried out this work using an industrially relevant scale, involving



➤ Figure 1. The main steps in the fabrication process for 6-inch SiC-SiC bonding. The prime-grade SiC substrate is selected for MOSFET fabrication. The dummy-grade SiC substrate is usually adopted in low-grade SiC diode fabrication or treated as waste. The re-use of prime grade SiC allows a reduction in wafer cost. Soft Ar^+ bombardment and intentional soft doping activated the SiC surface. After bonding, high-temperate annealing induced a splitting of the prime-grade SiC. Then, ultra-high temperature annealing repaired damage generated during the H^+ implantation and interface bonding. A high bonding and transfer rate of 100 percent was achieved, excluding the 1 mm region from the wafer edge. Note that it is very challenging for chemical-mechanical polishing technology to control the uniformity for a high-quality surface layer with several hundred nanometres.

device fabrication from 150 mm wafers at wafer scale, and extensive 150 mm wafer mapping, to characterise both material and devices.

Highlights that have emerged from this effort – and read on to discover all the crucial details – include engineered substrates with a low defect density and a low thermal boundary resistance, and the fabrication of robust, reliable devices with a very high yield. This impressive collection of results underscores the great potential of our new substrate technology for opening the door to more economical and sustainable SiC power electronics.

Superior substrates

In general, the current approach that's adopted within the SiC industry is to reserve prime-grade SiC substrates for high-performance MOSFETs, and to use dummy-grade SiC substrates – characterised by lower crystalline quality and a higher defect density – for low-cost diode production, or to discard as waste.

We are not alone in using engineered substrates to address this weakness in material efficiency. However, while we use surface-activation bonding to integrate a thin layer of prime-grade SiC onto a dummy-grade SiC substrate, the approach taken by Soitec and Sumitomo differs, involving the bonding of a prime-grade SiC thin layer onto a polycrystalline SiC substrate.

To fabricate our SiC-SiC composite substrates, we begin by bombarding prime-grade wafers with H^+ ions, with implantation at 90 keV using a fluence of 6×10^{16} cm^{-2}. After this initial step, which forms a pre-fractionation layer, we bond prime- and dummy-grade substrates at room temperature under high vacuum, after activating the surface with an energy ion beam and intentional doping. Subsequent annealing at more than 870°C splits the pre-fractionation layer, allowing transfer of a prime-grade SiC film around 410 nm-thick to a dummy-grade handle wafer. Finally, annealing at more than 1700°C repairs the bonding interface, before we apply a handful of finishing steps to improve the roughness and thermal stability of the epi-ready surface (all these steps for fabricating our SiC-SiC composite substrates are illustrated in Figure 1).

We are not alone in forming engineered wafers via the application of a high-quality film on one material to a thicker, lower-quality foundation. To assess our results, we have benchmarked our composite wafer against others with a 150 mm diameter, an exercise that reveals a record low thickness deviation for our material (see Figure 2).

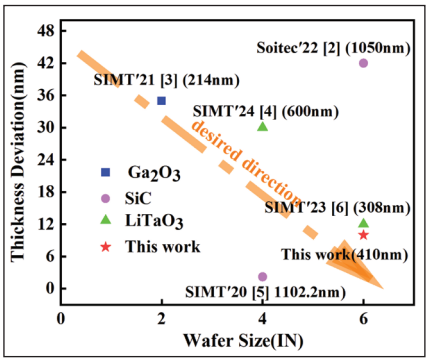
Another encouraging result is that, according to defect mapping, while the number of defects – including pits, micropipes, and bar-shaped stacking faults– totals 206 in a typical dummy-grade substrate, it's just 59 in our engineered substrate.

Evaluating the boundaries

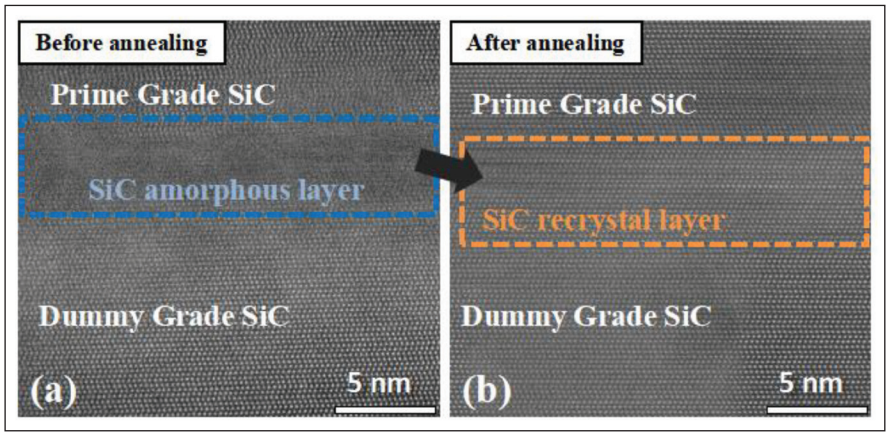
According to transmission electron microscopy images of the bonding interface before and after annealing (see Figure 3), this step recrystallises the amorphous SiC layer that's 2-3 nm thick, and formed in the prior step of surface activation. Thanks to this, interface quality improves.

We have turned to electrostatic force microscopy to characterise the electric-field distribution and potential barrier at the bonding interface – both play critical roles in high-current conduction.

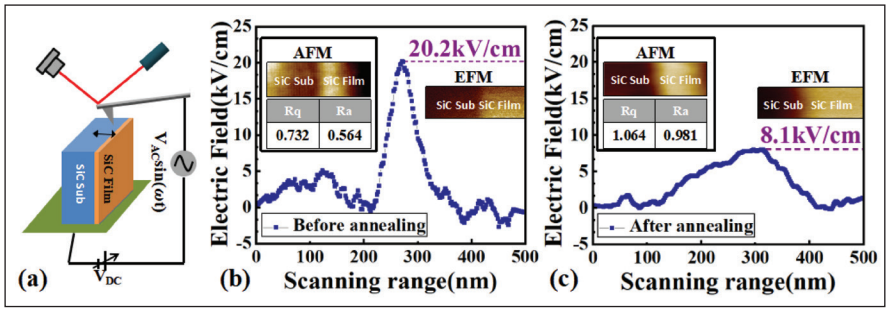
The principle of electrostatic force microscopy is a scanning process to measure the cross-sectional potential variation, with the signal amplified by tuning DC and AC biases (see Figure 4 (a)).



➤ Figure 2. Benchmarking of the thickness deviation of the transferred semiconductor film as a function of wafer size.



➤ Figure 3. Cross-sectional high-resolution transmission electron microscopy images of the SiC-SiC bonding interface (a) before and (b) after annealing. The amorphous layer generated during bonding is well recrystallised by ultra-high-temperature annealing, with only a slight twist due to the wafer alignment in plane.



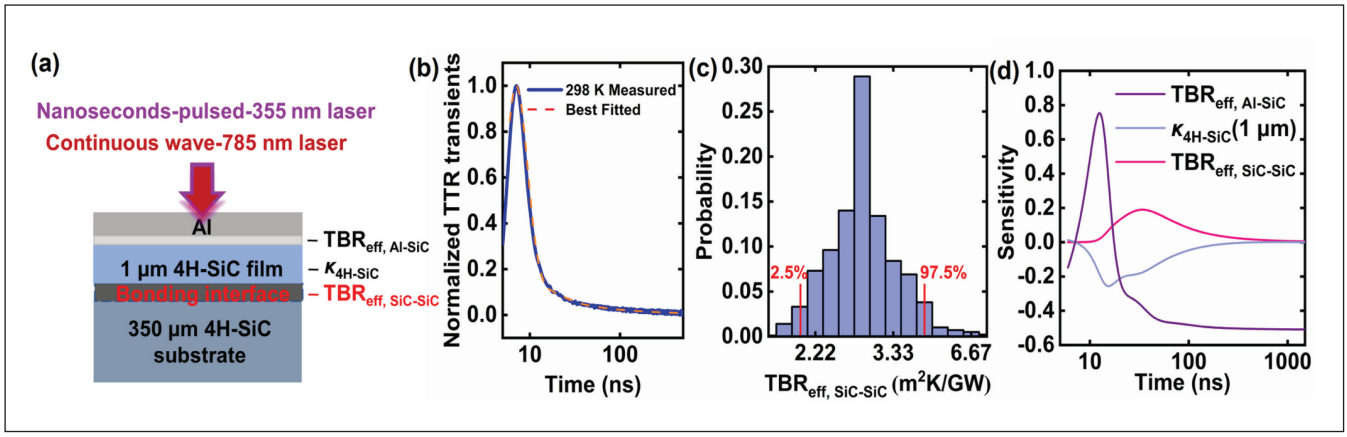
➤ Figure 4. (a) An illustration of electrostatic force microscopy (EFM) scanning at the SiC-film/SiC-sub bonding cross-sectional interface. The derived electric-field profile images (b) before and (c) after annealing, respectively, as well as cross-sectional topography and corresponding apparent surface-potential images in the inset. Set V_{DC} of 5V, V_{AC} of 0.5V for EFM scanning. Note the potential data shown in the inset are after signal amplification. The derived potential barrier is below 130 mV, allowing easy tunnelling by electrons in the n^{++} SiC.

With this technique we have determined that annealing produces a reduction in the peak electric field at the bonding interface, which falls from 20.2 kV cm^{-1} to 8.1 kV cm^{-1} (see Figure 4 (b) and (c)). Reducing the peak electric field ensures a smaller barrier for carrier flow across the bonding interface. Further evidence for annealing producing a smaller barrier to carrier transport across the bonding interface comes from an ohmic current-voltage test structure, which maintains linear current-voltage characteristics, even at temperatures up to 175°C. This confirms the robust ohmic contact through the bonded interface.

To determine the thermal boundary resistance of our bonding interface, we have employed transient thermo-reflectance (see Figure 5 (a)). We have a high degree of confidence in this measurement, based on good fitting (see Figure 5 (b)), the Monte-Carlo analysis histogram (see Figure 5 (c)), and sensitivity analysis (see Figure 5 (d)). We have measured a thermal boundary resistance at the SiC-SiC bonding interface of 2.8 +1.4/-0.7 m^2 K GW^{-1} at 25°C. Benchmarking indicates that our thermal boundary resistance is amongst the lowest values reported for the SiC interfaces bonded with SiC, GaN, and Ga_2O_3.

Demonstrating devices

We have used our 150 mm engineered substrates to produce industrial-standard 1.2 kV SiC devices. Following epitaxy, we employed a Candela



➤ Figure 5. (a) Schematic of a transient thermo-reflectance (TTR) measurement of bonded SiC-on-SiC. Pump beam is a 3 ns, 355 nm pulsed laser and the probe beam is chosen with a 785 nm continuous-wavelength laser. (b) TTR signals for bonding interface and the best-fitted curve from the analytical model. (c) Monte-Carlo analysis histogram of thermal boundary resistance (TBR), measured at room temperature. (d) Sensitivity of the TTR signal to the TBR signals of SiC-SiC and SiC-Al interfaces and the SiC thermal conductivity (κ_{4H-SiC}). The sensitivities to three free variables do not significantly overlap in the time windows and are suitable for simultaneous fitting. Here the aluminium electrode acts as the metal transducer.

Our work has showcased the prowess of our novel 150 mm single-crystal SiC engineered substrate produced by surface-active bonding that enables dummy-grade material reuse and prime-grade material recycling. The bonding interface shows the lowest thermal boundary resistance for all SiC bonding reports, and the epiwafers grown on this substrate have achieved a high killer-defect-free yield of 99.2 percent

metrology tool to map our 2 mm x 2 mm die and identify killer defects, including downfalls, micropipes, triangular and carrot defects. Based on this mapping, our killer-defect-free epi yield is very high – it's 99.2 percent (see Figure 6).

From this epiwafer we have fabricated 1.2kV planar-gate SiC MOSFETs with an on-resistance of 20mΩ. To evaluate these devices, we have considered the key signatures of extrinsic reliability: the gate leakage current (I_{GSS}) and the drain leakage current (I_{DSS}). Mapping for both characteristics, using a gate-source voltage of -4 V for I_{GSS} and a drain-source voltage of 1200 V for I_{DSS}, has allowed us to probe 550 devices across our entire 150 mm wafer. Applying the very stringent standard of an I_{GSS} of below 20 nA and an I_{DSS} of less than 2 μA, determined yields for I_{GSS} and I_{DSS} of 90 percent and 70 percent, respectively (see Figures 7). Such high device yields validate the high quality of our SiC epilayers on our engineered substrates.

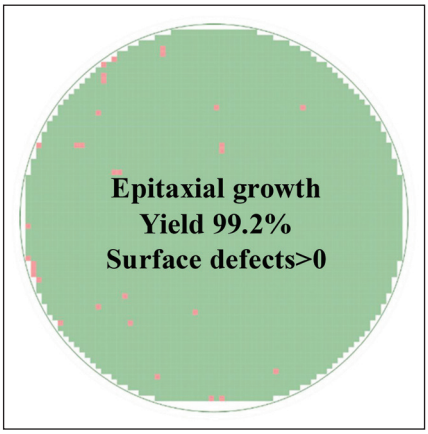
We have also recorded the output current-voltage characteristics of our MOSFETs up to 100 A, at 25 °C and 125 °C. From these plots we extracted a specific on-resistance of 3.5 mΩ cm^2, which contains a contribution of about 15 percent from the engineered substrate – it has a resistivity of 0.25 Ω mm, and a thickness of 200 μm. At 125°C, there is an increase in on-resistance by around just 20 percent, from a low I_{DS} up to 150 A. This small increase is superior to some reference products on the market.

These results validate the stability of our engineered substrate under high I_{DS} at high temperatures. We are also encouraged by the off-state characteristics of our devices at up to 175 °C under 1 μA test compliance. These measurements reveal an I_{DSS} of around 10^{-8} A up to 800 V at 175°C. This validates the low epiwafer defect density.

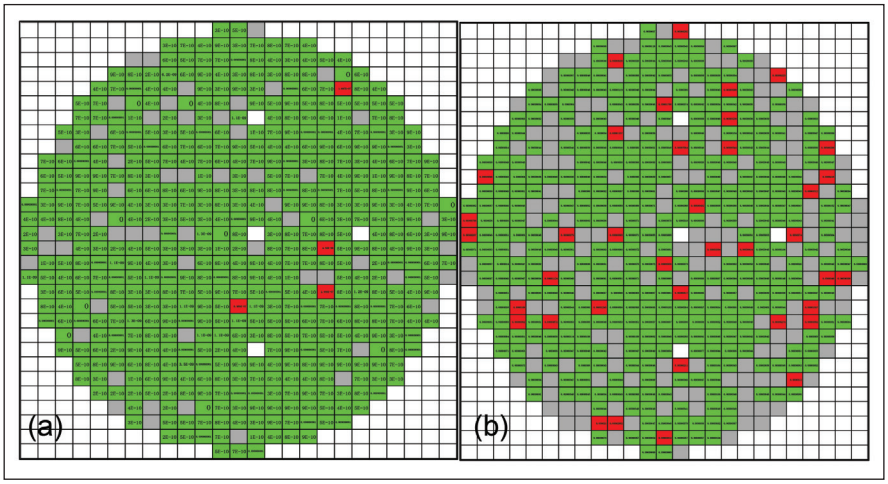
We have also undertaken a hard turn-on and turn-off assessment of our devices, using a 800 V/50 A double-pulse test. The zoom-in waveform allows us to extract rise and fall times of 18.79 ns and 16.97 ns, respectively. These values are comparable to, or even superior to, those for similarly-rated commercial products fabricated on prime-grade substrates reported under a similar double-pulse test condition.

Reliability and robustness

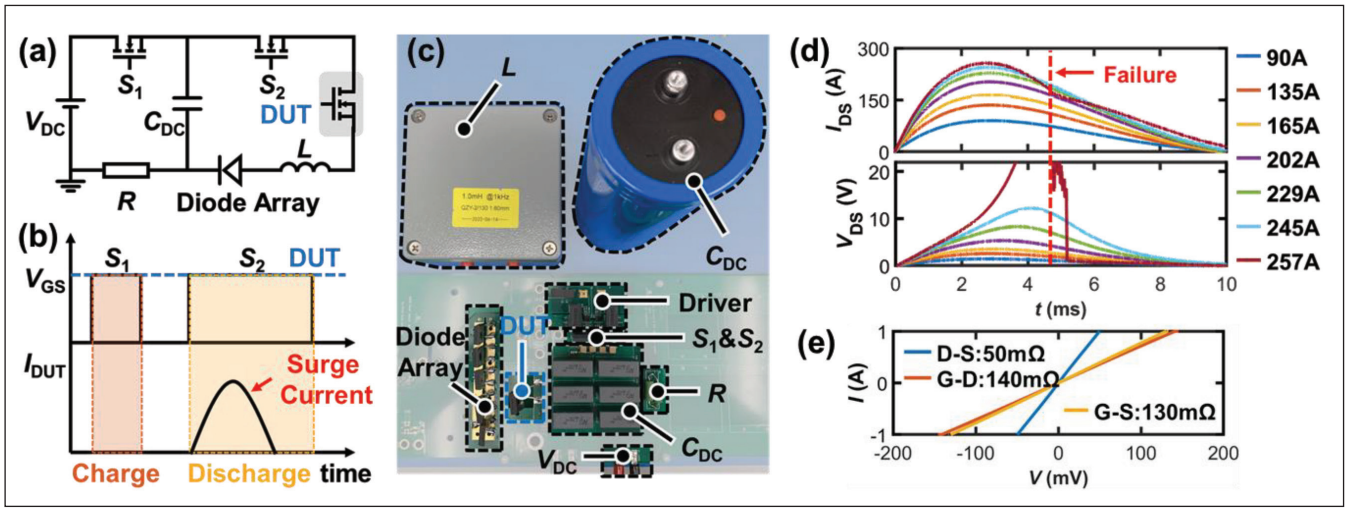
To evaluate the reliability of the epilayers and the devices that we have produced on our engineered substrate, we have performed high-temperature reverse-bias tests on multiple devices, using a V_{DS} of 960 V and a temperature of 175°C for 168 hours. This investigation considered four critical device metrics: on-resistance, threshold voltage, blocking voltage and I_{GSS}, both before and after the 168-hour stress. This stress resulted in very small shifts



➤ Figure 6. 2 mm x 2 mm die map with an estimated 99.2 percent die yield of a 6-inch wafer after epitaxial growth. Morphological defects include downfalls, micropipes, triangular defects and carrot defects.



➤ Figure 7. (a) I_{GSS} mapping of devices fabricated on 6-inch wafer at V_{GS} of -4 V. Yield is 90 percent. I_{GSS} less than 20 nA (green, pass), between 20 nA and 1 μA (red, failed), more than 1 μA (grey, failed). (b) I_{DSS} mapping of devices fabricated on 6-inch wafer at a V_{DS} of 1200 V. Yield is 70 percent. I_{DSS} less than 2 μA (green, pass), between 2 μA and 99 μA (red, failed), more than 99 μA (grey, failed).



➤ Figure 8. (a) Circuit schematic, (d) ideal waveforms and (c) photograph of surge current test setup. S_1 is first turned on to charge C_{DC} (10 mF), followed by S_2 turn-on to produce a inductor-capacitor resonance (L of 1 mH) to generate a 10 ms-width half-sine current waveform for the device under test (DUT). Two 1200V/16mΩ SiC MOSFETs (C3M0016120D) (i.e., S1 and S2) and ten paralleled 1200 V/10 A SBD (C4D10120D) are applied to guarantee higher surge current capability than the DUT. (d) DUT's current and voltage waveforms under various surge current levels. (e) Pin-to-pin resistances of the failed DUT.

in the four critical metrics: on-resistance, threshold voltage, and blocking voltage changed by less than 1.3 percent; and I_{GSS} shifted by less than 10 percent. While the bonded substrate does not 'see' the high electric field, it does have to pass current between the source and drain. Due to this requirement, its surge-current robustness is critical. To evaluate this, we have used a circuit setup (see (Figure 8 (a)-(c)) that produces a 10 ms-wide half-sine surge current, according to the JEDEC standard. This surge current is generated by an inductance-capacitance resonance, with the peak current controlled by the bus voltage.

We have recorded the current and voltage waveforms of our devices under surge-current levels ranging from 90 A to 257 A (see Figure 8 (d)). After each test, we comprehensively characterised the SiC MOSFET. We found that this device survived the 245 A surge current test with no degradation, before failing the 257 A test. When inspecting the pin-to-pin resistance of the failed device, we uncovered a gate-source short failure. Investigating this revealed that the ohmic current-voltage behaviour is retained between the drain-source and the drain-gate, suggesting no failure at the bonding interface. If failure occurred here, this would give rise to a potential barrier at the bonding interface, jeopardising the device's ohmic behaviour.

To conclude, our work has showcased the prowess of our novel 150 mm single-crystal SiC engineered substrate produced by surface-active bonding that enables dummy-grade material reuse and prime-grade material recycling. The bonding interface shows the lowest thermal boundary resistance for all SiC bonding reports, and the epiwafers grown on this substrate have achieved a high killer-defect-free yield of 99.2 percent.

Additional highlights include 1.2 kV SiC MOSFETs that combine a high yield with good performance and reliability, and surge-current robustness for both device and substrate.

Due to all these encouraging results, we have no doubt that our technology can address the key challenge currently facing the SiC wafer industry, and enable more economical, sustainable SiC power electronics.

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Unleashing the potential of nanoimprint lithography

Now a mature technology, nanoimprint lithography is ready to support the production of PCSELs and augmented-reality glasses incorporating SiC

BY WANG NANG WANG, CHUNG-HSIANG LIN AND KANG YUAN LEE FROM QUANTUM NIL CORPORATION AND HAO CHUNG KUO, CHIN WEI SHER AND WEN-CHENG HSU FROM THE HON HAI RESEARCH INSTITUTE, SEMICONDUCTOR RESEARCH CENTER

FOR ALL classes of semiconductor device, their dimensions dictate their performance. For transistors deployed in microprocessors and RF amplification, the length of the gate governs capability, while for lasers, critical characteristics depend on the width of the cavity and the aperture size.

Today, the most aggressively scaled devices are silicon MOSFETs, used in the ICs in every laptop, tablet, desktop and smartphone. Their production involves extreme UV lithography, which provides sub-2 nm linewidth manufacture on 300 mm silicon substrates. However, such scaling, which pushes the boundaries of semiconductor miniaturisation, comes with significant challenges, including exceptionally high manufacturing costs, substantial energy consumption, and more stringent substrate and material requirements. Note that these constraints have widespread limitations, impairing flexibility for heterogeneous material integration and preventing cost-effective scalability across diverse semiconductor applications.

➤ Figure 1. 3D dot projection image by a fabricated PCSELs array.

Making a big impression within this field is the rapid progress of AI-driven design methodologies. This has led to the generation of highly intricate and quasi-random design architectures that optimise system integration and performance. These designs are something of a double-edged sword, offering superior efficiency and functionality, but at the expense of significant challenges for photolithography, which struggles to accommodate their complexity without extensive process adaptation, hampering their use in production.

Beyond the silicon world, there are other opportunities requiring the definition of dimensions at very small scales. Augmented reality (AR), advanced 3D sensing and high-bandwidth datacom/telecom all require stringent and complex nano-patterns integrated in devices. Also fuelling demand for additional nanostructure fabrication are biotechnology devices – also known as biochips – that tend to rely on biocompatible materials at the micro- or nano-scale.

Amongst the various lithography technologies competing to achieve these goals, nano-imprint lithography (NIL) has much promise, with the potential to revolutionise the field of nanotechnology. Due to the flexibility of the entire process, NIL is insensitive to material types and specifications, and is a competent manufacturing technique for the production of next-generation complex heterogenous devices.

NIL is now a well-established, replication-based mechanical process. At its heart is the pressing of a

patterned template or mould into a polymer or resist layer, to enable the transfer of the pattern. Thanks to this approach, NIL, which is not limited by optics, is an attractive option for large-scale manufacturing of nanostructures, as it avoids multiple optical proximity correction requirements. What's more, it has the upper-hand over traditional lithography on a number of fronts: it does not demand expensive equipment and extensive processing, making it an ideal technology for research and development; and it consumes far less energy and gases compared with deep-UV and extreme-UV processes, for similar critical dimensions.

Defining incredibly small feature sizes is possible with NIL. Back in 2006, this technique demonstrated the critical dimension resolution of 2 nm using a mould formed from single-wall carbon nanotubes.

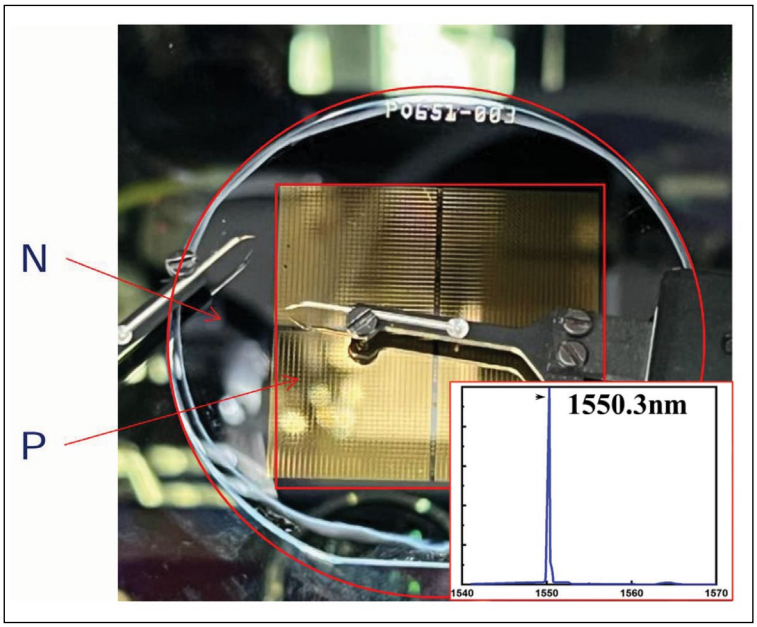
Thanks to the versatility of the mechanical pattern transfer process, NIL is compatible with a very wide range of materials and substrates – biopolymers, thermal and photo resists, metals, plastics, glasses, compound semiconductors, metal oxides, composites and bio-functional materials. This long list contains many materials that are not compatible with silicon-based semiconductor equipment and processes, highlighting that one of the strengths of NIL is that it can be applied to deformed templates – such as those with bowing, warping, or large thickness variations – as well as non-flat and curved surfaces.

One field where NIL is attracting much attention is biomedical, with this form of lithography viewed as a strong candidate for creating bio-functional surfaces, biosensors, and drug delivery systems. The precise control over surface topography and chemistry offered by NIL on biocompatible materials at the micro- or nano-scale makes it a powerful tool for engineering biomaterials and studying cellular interactions at the molecule level.

NIL is also generating much interest in emerging technologies, by driving advances in plasmonics, metamaterials, and quantum photonics. This class of lithography has been employed for the creation of precise arrays of quantum dots, which trap and manipulate individual electrons, allowing for the creation of quantum bits – they are the crucial building blocks for quantum computing. In addition, NIL has been used to create on-chip integrated sources of entangled photon pairs, which are key elements in quantum communication and cryptography protocols.

Unfortunately, there are still several challenges associated with the implementation of NIL, discussed below, that are particularly significant compared with state-of art silicon-based semiconductor device fabrication.

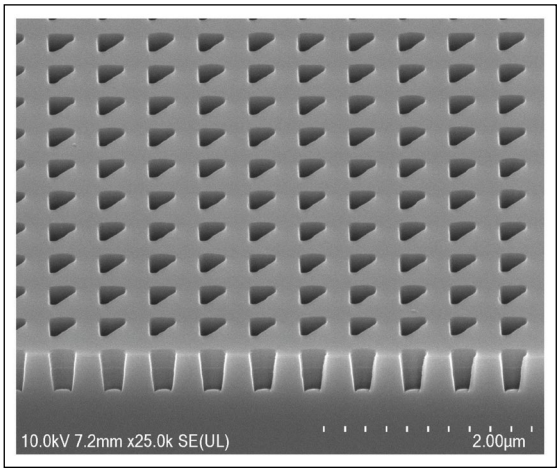
These challenges include realising sufficient uniformity and reproducibility across large areas,



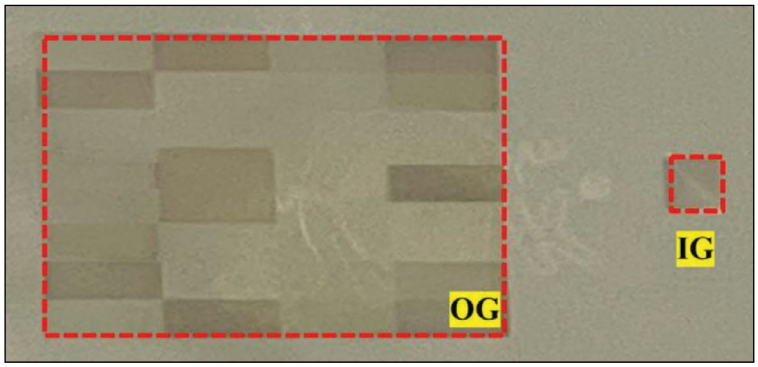
➤ Figure 2. A full NIL-patterned InP PCSEL wafer undergoing full device pre-testing.

such as 300 mm substrates. Impeding success are a variety of factors, including pressure distribution, material flow dynamics, and residual layer thickness variation. Efforts can also be hampered by the production of complex structures, which might collapse or deform during the NIL demoulding process. Another factor threatening to hit yield is the thickness of the residual layer left behind after imprinting, as this impacts subsequent processes. Note that realising a consistent residual layer thickness can be difficult, especially for complex pattern features.

While NIL can be applied to many classes of materials, it's still important to consider material compatibility. During the NIL process, materials must flow and conform to the imprint mould. It can be challenging to select suitable materials with desired properties, such as a low viscosity, high fidelity, and good release characteristics. Another consideration is that due to the 1:1 process scale, it can be costly and time-consuming to fabricate high-quality, defect-free imprint moulds with the desired feature sizes and shapes. These imprint moulds must have a precise alignment and registration with



➤ Figure 3. Scanning electron microscopy image of a photonic-crystal pattern fabricated on a 4-inch InP PCSEL wafer.



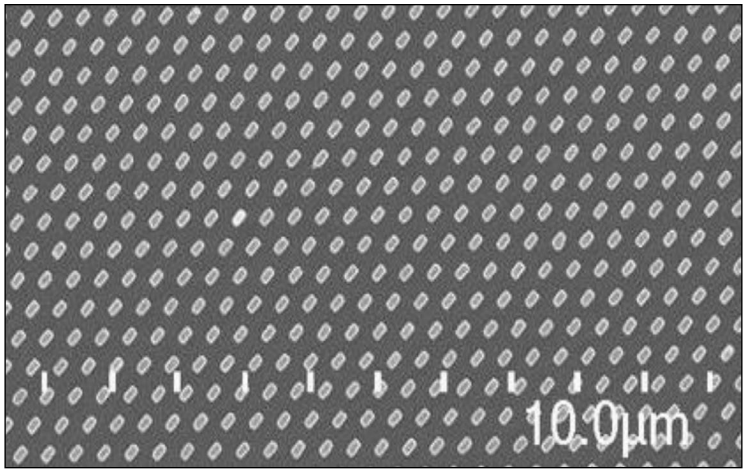
➤ Figure 4. A preliminary type of SiC AR glass with a waveguiding architecture. IG and OG represent input-coupling grating and output-coupling grating, respectively.

the substrate to ensure pattern fidelity – any out-of-window misalignment can lead to defects or pattern distortions, especially for multilayer structures.

Finally, unlike parallel techniques, such as photolithography, NIL is typically a serial process. This limits throughput, and makes it challenging to scale up NIL for mass production while maintaining high resolution and throughput.

Within the NIL community, much effort has been devoted to addressing all the challenges just described. Highlights of progress-to-date include the development of step and flash nanoimprint lithography, along with in-line or cluster tools using small defect-free NIL moulds that may offer better reproducibility when working with larger substrates.

There has also been a significant milestone in NIL's commercial adoption, with Canon's introduction of an NIL system tailored for manufacturing flash memory. This breakthrough could unlock the door to the deployment of NIL in the manufacture of next-generation electronics and photonic devices. In particular, Canon's technology could be used for complex and AI-optimised architectures that demand high-precision, cost-effective patterning solutions.



➤ Figure 5. Scanning electron microscopy image of an out-coupling grating (OG) component of the SiC AR glass.

Bridging the gap

Providing a pioneering force in the commercialisation of NIL is our team at Quantum NIL Corporation (QTNIL), which based in the Hsinchu Science Park, Taiwan and supported by researchers at Hon Hai Research Institute (HHRI) Semiconductor Research Centre. Our efforts on this front have provided significant contributions to continuous advancements in research and industry, and date back to 2007, long-before QTNIL founded in 2022.

Our key technology is the seamless integration of NIL with conventional photolithography to form unique hybrid NIL solutions that effectively bridge the gap between these two techniques, and enable the application of NIL for the manufacture of a broad range of semiconductor and photonic devices. Thanks to our trailblazing efforts, NIL can be applied to mass production of micro/nano-patterned substrates for multi-functional compound semiconductor devices, including photonic integrated circuits (PICs), high-speed datacom lasers, and biomedical chips.

Our company is establishing itself as a leading material engineering foundry specialising in hybrid NIL process flows. We are already offering tailored solutions to meet industry's increasing demand for advanced pattern engineering techniques. With extensive experience in NIL materials, process optimisation, optical alignment, and equipment modification, our foundry solution is compatible with most compound semiconductor and optical materials.

We have a strategic vision that revolves around expanding industry collaboration with Tier 1 companies and leading research institutions, targeting high-value applications in data communications, quantum photonics, and autonomous systems. To increase our competitiveness, we are spearheading advancements in NIL manufacturing technology through AI-driven optimisation, machine learning-enhanced process control, and the development of next-generation multi-function process design kits (PDKs). This progress will streamline the adoption of NIL in semiconductors and photonic fabrication for applications in quantum science, and position our company at the forefront of NIL commercialisation, driving innovations in AI, quantum sensing, photonics, and computing.

Producing PCSELs

The PCSEL, or to give it its full name the photonic-crystal surface-emitting laser, offers advantages over both incumbent laser technologies: edge-emitting lasers and VCSELs. Merits of the PCSEL include: its capability to produce a high output power while radiating light vertically; and a scalability of size and power, making this device applicable to high-power applications and long-distance detection. Another hallmark, which sets the PCSEL apart from conventional lasers, is single-mode operation with a high output power while maintaining a very narrow optical-beam-divergence angle. Through engineering of the photonic crystal, PCSELs can realise a superior system efficiency, an enhanced

NIL is now a most promising nanofabrication technique for meeting the critical demand of aggressively scaled down silicon MOSFET memories/microprocessors, and compound semiconductor devices with sub-wavelength features. These devices are crucial in driving advancements in AI and quantum computing

sensing resolution, and a compact module footprint, making these devices highly suitable for advanced applications, such as autonomous navigation, long-range optical communication and high-precision optical sensing. Multi-integrated photonic crystals can be further programmed for PIC applications.

In 2024, Hon Hai Research Institute (HHRI) Semiconductor Research Center demonstrated a new method for fabricating PCSEL arrays, involving the definition of an isolation pattern (see Figure 1, which illustrates the dot projection image by a PCSELs array when applied to a 3D sensing system). When compared with the conventional 3D depth sensing system, this new PCSEL system demonstrates a higher dot projection number – 44 percent higher and a much wider field-of-view of 158°. These results highlight the capability of the PCSEL to deliver a higher sensing resolution, an extended detection range, and improved environmental adaptability, key metrics for high-accuracy lidar.

We are now working to further extend the wavelength of the PCSEL and investigate the feasibility of manufacturing this class of laser (see Figure 2 for the full NIL patterned InP PCSEL wafer undergoing full device pre-testing, and Figure 3 for a scanning electron microscopy image of a photonic crystal pattern fabricated on a 4-inch InP PCSEL wafer using our NIL foundry process). These PCSELs feature photonic-crystal structures with a right-angled triangular pattern, designed to facilitate an asymmetrical approach in photon behaviour manipulation.

The characterisation of these PCSELs showcases the strength of our foundry solution, which is capable of providing a straightforward implementation of an asymmetrical geometry onto any kind of substrate. This ability to fabricate precise photonic-crystal patterns at scale paves the way for mass adoption of PCSELs in applications such as next-generation automotive lidar, high-speed optical communication, and 3D sensing.

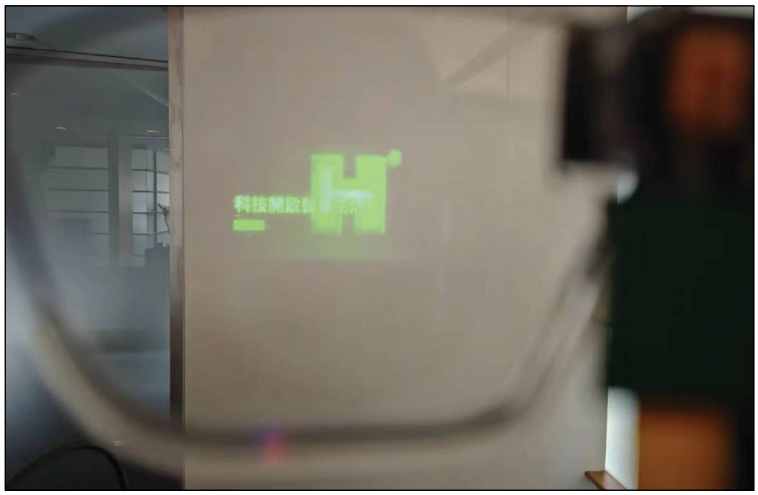
SiC augmented-reality glass

Meta recently announced the Orion AR glass, leveraging SiC as a core material and marking a significant step forward in AR display technology. The selection of SiC for this task reflects its exceptional optical properties, which include its high refractive index and superior thermal conductivity. These strengths contribute to enhanced AR display performance, by providing a broader field-of-view, superior optical clarity, increased durability, and better thermal stability. According to research, SiC-based AR waveguides are capable of fields of view of up to 80°, significantly outpacing traditional high-refractive-index glass solutions, which are typically limited to 40°.

To draw on the benefits of SiC, those that are working with this material must overcome its manufacturing challenges. It is an intrinsically hard material, a characteristic that complicates precision etching and fabrication.

Taking on this challenge, we are actively developing SiC-based AR glass for full-colour displays, with efforts directed at advanced process integration and design adaptation (see Figure 4 for a preliminary type of SiC AR glass with a waveguiding architecture, where IG and OG represent input-coupling grating and output-coupling grating, respectively).

For this work, we have used 6-inch substrates, and considered a footprint of SiC AR glass of about 2.8 cm x 5.5 cm. By leveraging NIL and optimised etching techniques, our aim has been to enhance the manufacturability of SiC while maintaining its superior optical performance. Our results have included a SiC etch with an aspect ratio of about 1.5 and a fabricated minimum dimension of about 80 nm (see Figure 5, showing a scanning electron microscopy image of the output-coupling grating).



➤ Figure 6. The preliminary display result by a single wavelength of 525 nm.

We have demonstrated a preliminary display, using a single wavelength (see Figure 6). Due to the design complexity of the grating, our hybrid NIL solution is fully adopted for device and process implementation.

NIL is now a most promising nanofabrication technique for meeting the critical demand of aggressively scaled down silicon MOSFET memories/microprocessors, and compound semiconductor devices with sub-wavelength features. These devices are crucial in driving advancements in AI and quantum computing. With its innovative NIL solutions, we are pushing the boundaries of optical component fabrication, quantum photonic chips, and sub-wavelength structures. As NIL technology matures, its adoption into the manufacturing of all classes of semiconductor device will accelerate, shaping the future of high-performance electronic and photonic devices.

The authors thank Professor Martin Charlton at the University of Southampton for his support in the e-beam system capability study and JORJIN Technology Inc. for assisting with AR glass feature assembly.

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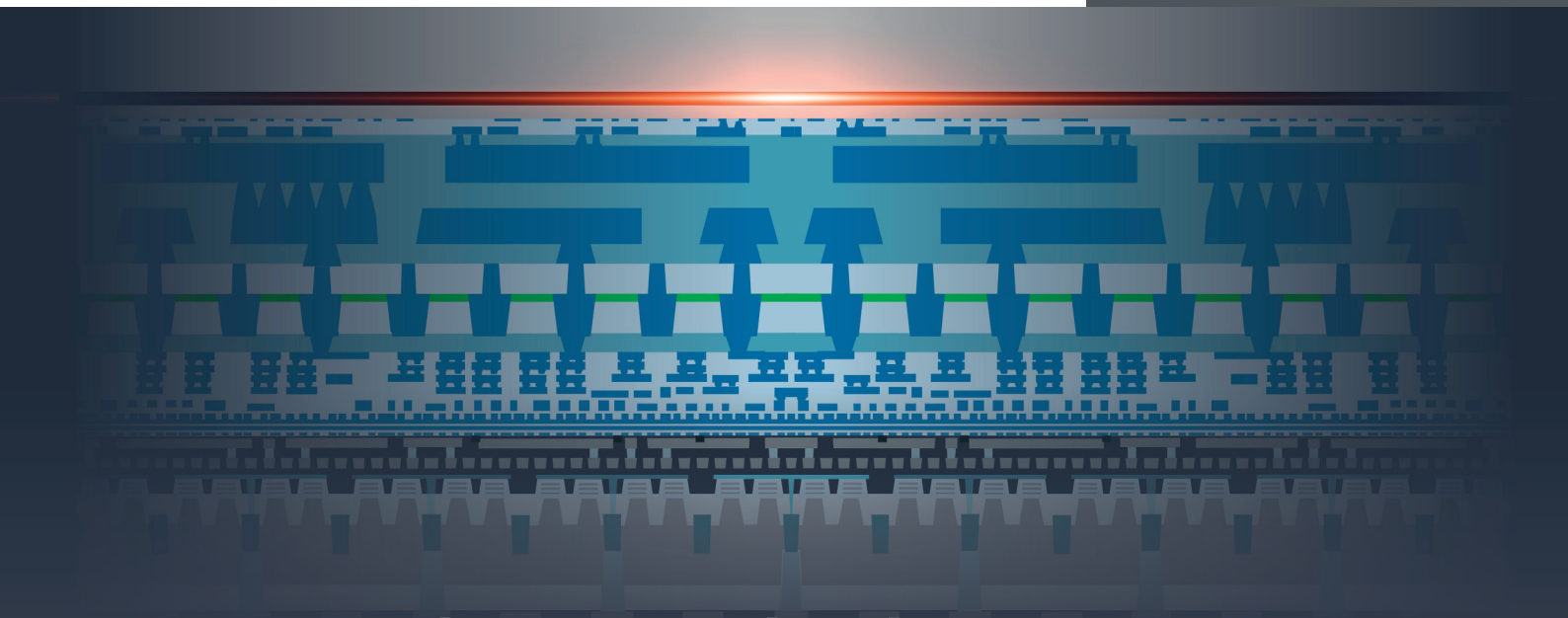

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Boron alloys for nitride optoelectronics?

Can boron-containing III-Nitride alloys unleash the potential of deep-UV solid-state light sources and provide a red solution for microLED displays?

BY PETER PARBROOK AND STEFAN SCHULZ FROM TYNDALL NATIONAL INSTITUTE

LEDs are renowned for their extreme efficiency, long lifetime and environmental compatibility. Thanks to these strengths, they have transformed the way we generate and control light. Amongst their successes, LEDs have revolutionised the lighting industry, and all forms of display, from mobile phones to laptops and TVs.

However, there are still some applications where the advantages of LED technology are yet to make an impact. One is emission at wavelengths deep within the UV, and another is making ultra-small LEDs for pixels in visible displays.

The traditional approach to reaching these wavelengths is to build upon the GaN-based blue-emitting LED, and to stretch the emission wavelength, by either adding more indium to reach the red, or inserting more aluminium to plunge the depths of the UV. But to date, success on these fronts has been limited, suggesting that new approaches are needed. Our team at the Tyndall National Institute at University College Cork is starting to offer just this, investigating the potential of boron alloys in these spectral domains.

The UV challenge

One of the potential benefits of our work is that it could help to improve the performance of solid-state UV sources, which are one of the most effective ways to provide sterilisation. Wavelengths below 280 nm are key to UV disinfection, because this part of the solar spectrum is blocked by the Earth's atmosphere. Without this global shield, living organisms would struggle to survive. This weakness allows UV sources operating below 280 nm to provide a 'clean' route to destroying harmful bacteria, parasites and viruses, such as MRSA and Covid-19. Such solutions remove, or at least reduce, the need for chemical treatments.

Today, UV sterilisation usually involves mercury-based lamps. However, they are potentially fragile, their efficiency is not high, and the toxicity of mercury creates serious end-of-life disposal issues. Furthermore, emission from these lamps is limited to a small number of wavelengths, linked to atomic mercury transitions.

UV LEDs offer an ideal alternative. They are potentially efficient, non-toxic and robust, and have

a freely tuneable wavelength, limited only by the choice of semiconductor material. With AlGaN alloys it's possible to cover the wavelength range down to 210 nm. However, this potential is yet to be fully realised, and producing sources at the very shortest wavelengths is particularly challenging, with the fundamental properties of the material hampering light extraction.

The micro-pixel challenge

The visible display market is huge, and climbing. According to Precedence Research it's already worth well in excess of $177 billion. At one end of this sector are displays with diagonals of many metres, used in stadia, and at the other are smart watches and even potentially smart contact lenses, requiring micron-scale emitters.

Competing for success in the display market are a number of technologies. However, in all cases inorganic LEDs have inherent advantages, in terms of pixel brightness, contrast and efficiency. Their major drawback, when deployed as microLEDs in displays, is cost of implementation. But with new processing and packaging techniques, this commercial feasibility is improving.

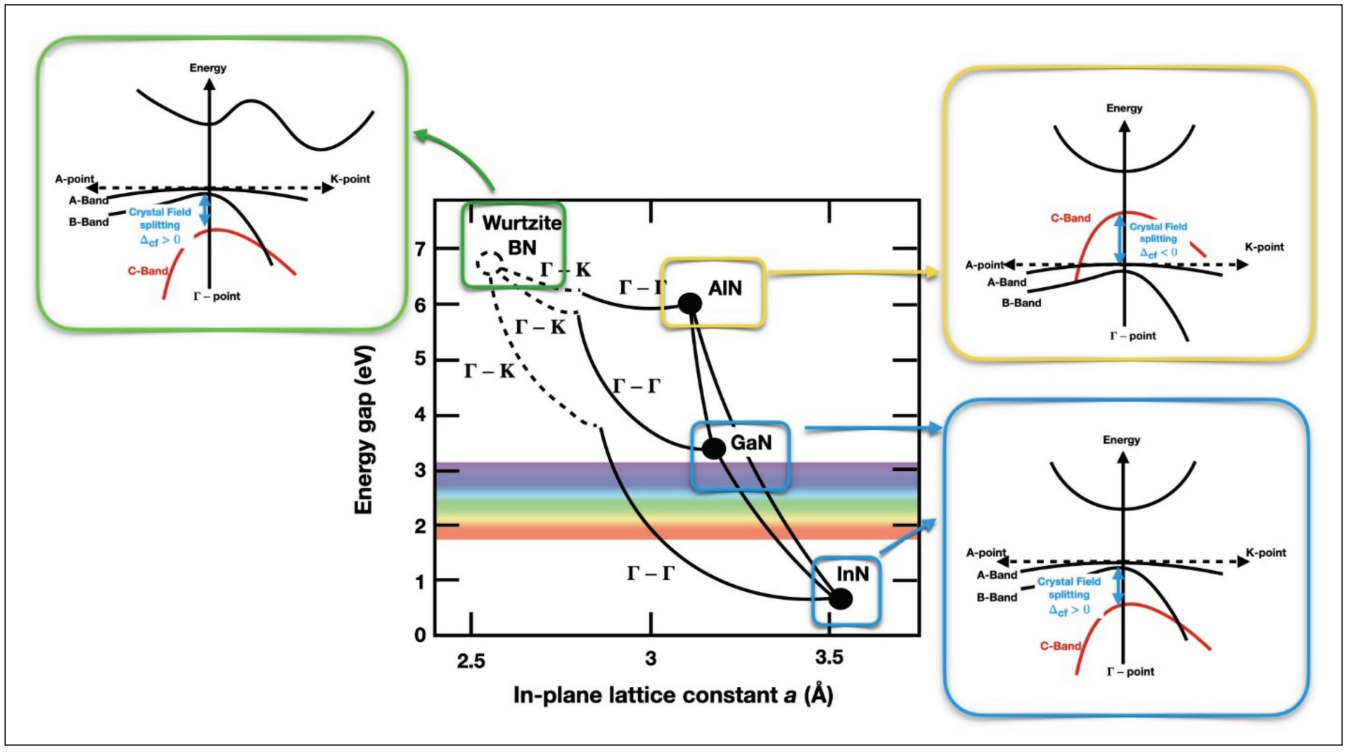
The technological challenge is to shrink the size of the inorganic LED pixel to suit the application. Devices need to be smaller than 20 microns in diameter, and in some cases scaled to the near sub-micron level. At these dimensions, non-radiative surface recombination at the edges of the device can slash efficiency. In general, III-nitride LEDs featuring InGaN quantum wells are remarkably robust to this effect, ensuring that they are suitable for blue and green pixels. But conventional red emitters, made from the InGaAlP material system, suffer from a rapid reduction in brightness as their pixel size shrinks. What's required is an alternative solution, ideally based on III-nitrides.

A boron-based solution?

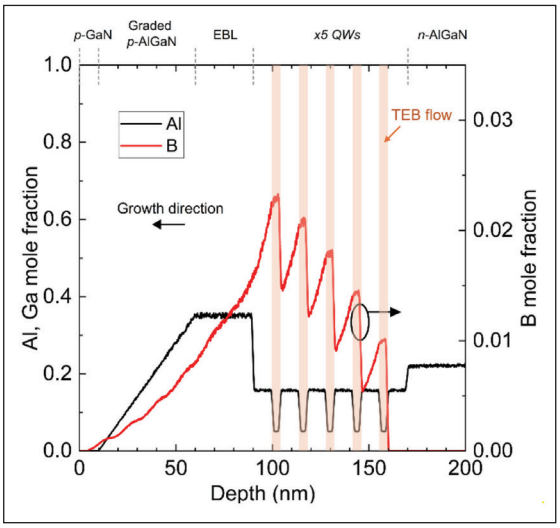
Against this backdrop, boron is a potential game changer. It is blessed with a small atom size, and the capability to alter the fundamental electronic properties of III-N alloys for the better, to enable improved device performance. However, to exploit the full potential of such alloys in device heterostructures, it is key to begin by gaining theoretical and experimental insights into the impact of boron on III-N's fundamental properties.

There has already been some interest in the use of boron in III-N alloys, with previous work targeting boron-containing thick epitaxial layers. Creating such layers is challenging, with an intrinsic bond-length mismatch leading to miscibility issues. However, studies have not included a significant examination of the extremely thin layers that are used in quantum wells.

When boron is added to InGaN and AlGaN quantum wells, this ingredient has the potential to adjust the lattice constant, reducing strain in the device's active region. For instance, if boron is added to InGaN quantum wells during their growth, this promises to shrink the lattice mismatch with the GaN barriers,



➤ Bandgap schematic of the variation of III-nitride alloys as a function of lattice constant. It should be noted that wurtzite BN is an indirect bandgap material, with a 'direct' bandgap transition of around 13 eV. Insets show the valence band ordering for each binary compound. The red 'C-Band' is highest for AlN, which leads to light extraction issues in LEDs.



➤ Secondary ion mass spectrometry of an LED structure with BAlGaN quantum wells, showing sharp increase in boron at each lower quantum well interface with an extended tail in the growth direction.

and hence reduce the formation of strain-induced defects in red-emitting LEDs.

Another benefit that could come from reducing the lattice mismatch in BInGaN/GaN and BAlGaN/AlGaN quantum wells is a decrease in the strain-induced piezoelectric response. This would pay dividends, as piezoelectric polarisation is detrimental to LED efficiency, reducing the probability of light-generating radiative recombination.

In the case of deep-UV LEDs, light extraction is hampered by a peculiarity in the electronic properties of AlN. Specifically, there is a different symmetry of the valence band edge for AlN and GaN, resulting in a change in the optical polarisation of the photons that are generated. Due to this, photons with the shortest emission wavelength, emanating from AlGaN with the highest AlN alloy content, are directed laterally towards the device edges, where they can be reabsorbed or lost, rather than towards the top (or bottom) surface of the device, where they lead to emission. Adding boron into AlGaN quantum wells promises to change this state-of-affairs, by pushing the symmetry transition to higher AlN content, and ultimately improving light extraction at these very short UV wavelengths.

Understanding boron's influence

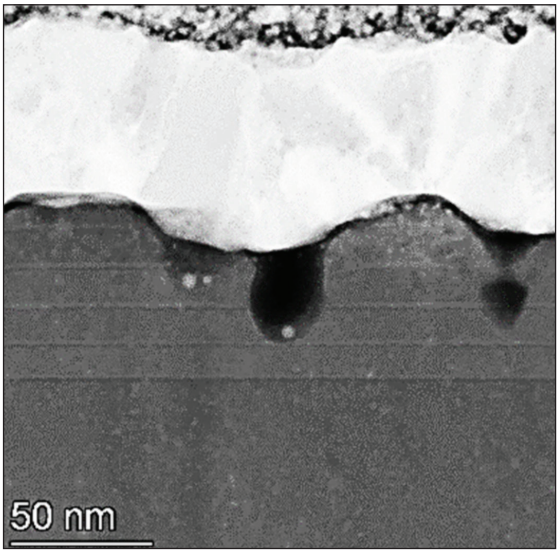
While there are clear potential advantages associated with the addition of boron, work is needed to understand whether it is possible to enjoy this potential benefit. Specifically, it is known that it's challenging to include significantly smaller atoms, such as boron, into an alloy with larger atoms (or *vice-versa*).

Within the compound semiconductor community, there have already been a number of efforts involving the introduction of atoms of a size that differs significantly from the host lattice, with their addition altering the electronic bandstructure, which may then exhibit unusual behaviours. A well-known instance of this is the addition of nitrogen to GaAs, an introduction that leads to the formation of additional defect states within the conduction band. Just a few percent of nitrogen leads to a dramatic reduction in bandgap, with that for GaAsN alloys deviating from the widely observed quadratic behaviour found in 'conventional' semiconductor alloys, as nitrogen content increases. A similar observation is found in AlInN, due the large lattice mismatch in the alloy.

One topic that requires further study is whether boron induces such defect states, and if so, under what circumstances. Answering this question requires detailed theoretical studies, particularly related to the importance of the alloy microstructure – that is, does boron atom clustering take place? According to initial theoretical studies, the presence of such clusters could lead to localised states in the bandgap of BGaN alloys, and potentially provide recombination centres in light-emitting devices.

As part of our investigations associated with boron, we have prepared B(Al)GaN samples with a boron content of around 1 percent. Photoluminescence spectra, obtained at temperatures from 10K to 300K, exhibit dramatic changes compared with boron-free reference samples. This behaviour is observed in both thick layers, with a thickness of around 100 nm, and in quantum wells, just 2-3 nm-thick. In general, we have found additional peaks at lower photon energies, consistent with the concept of carrier localisation playing a role, particularly as the boron content increases.

Another area to be addressed is the relatively poorly understood nature of boron incorporation into the material. The most common form of boron nitride



➤ Transmission electron microscope image of BAlGaN quantum wells showing smooth wells disrupted by void structures, attributed to nano-masking effects (Acknowledgement to Dr Miryam Arredondo-Arechavala of Queens University Belfast, UK, for the electron microscopy)

is a two-dimensional 'graphitic'-like structure that's markedly different from that for AlN, InN and GaN – they all have a wurtzite crystal structure. Due to this striking contrast, as well as the very different atom size, incorporating boron into (Al)GaN lattices is non-trivial.

Like other groups, we have come across these difficulties during the growth of layers with a thickness of more than 100 nm. When increasing boron incorporation beyond a particular critical boron flow, we found that the BGaN surface becomes self-masking, and the growth rate falls to zero. We attribute this to boron accumulation on the surface, which can prevent gallium incorporation.

For BAlGaN quantum well structures, we observe different findings. Grown using lower boron flow rates, surface accumulation results in a long boron tail into the cap material, according to secondary ion mass spectrometry. Within the quantum wells are micro-voids, observed by transmission electron microscopy, that are indicative of local boron surface concentrations creating nano-masking features.

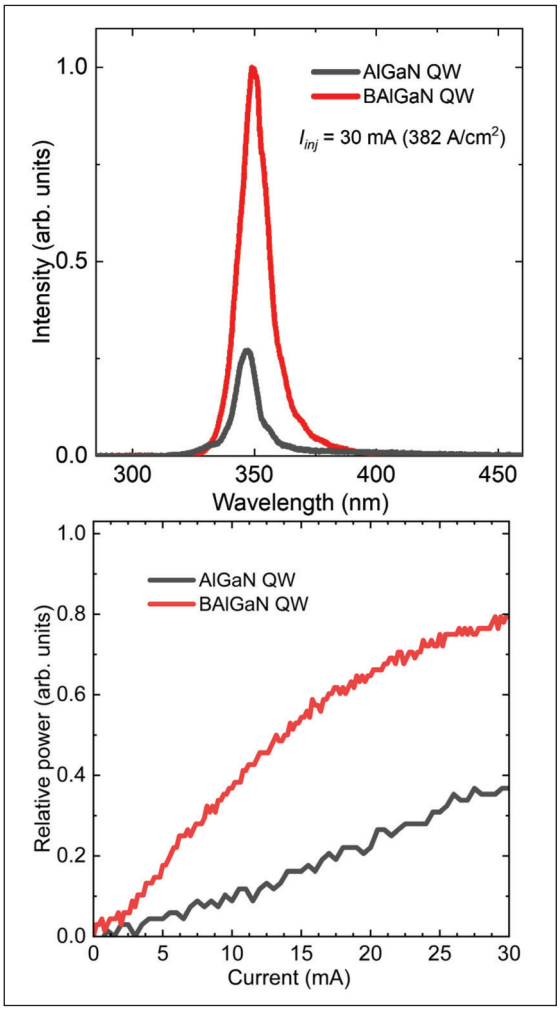
Towards light emission

Despite these challenges, we have successfully realised the world's first BN-containing quantum-well LED. We targeted emission within the UVA at 340 nm, a wavelength suitable for a biophotonics diagnostic application. For this work, we prepared two identical diode structures: one with no boron in the AlGaN quantum well, and a second with around 1 percent boron targeted.

Characterisation of the epistructures shows that, according to secondary ion mass spectrometry, there is a sharp increase in boron content at each lower quantum-well interface, as well as a tail towards the top surface, as previously discussed. We also uncovered voids in the quantum-well region, overgrown to a smooth surface for the *p*-contact.

Using a standard device fabrication process, we produced LEDs from our epiwafers. Under test, our devices that feature boron in the wells show enhanced luminescence for equivalent current injection. We also observed a small redshift, and increased broadening in the luminescence in our boron-containing sample. These features might be attributable to bandgap bowing and increased alloy disorder at low boron concentrations.

As expected, the addition of boron into 'conventional' III-nitride semiconductors is complex. We find this particularly when our boron-containing material is within the optically active part of the device structure, such as the quantum wells of an LED. However, we have shown that boron can be used advantageously in such devices, presenting a pathway to improved performance. In future, we plan to use this to study its potential for boron-containing devices at the extreme wavelength limits that III-nitride semiconductors can practicably address, specifically deep-UV (sub 250 nm) emission for skin-safe sterilisation and red emitters for displays based on microLEDs.



➤ (Upper) LED spectral output and (lower) light output versus current characteristic for BAlGaN quantum well device (red) and boron-free reference sample (black) showing improve performance in the boron containing case.

We acknowledge funding from Taighde Éireann - Research Ireland (formerly Science Foundation Ireland) under Grants 12/RC/2276 P2; 21/FFP-A/9014 and SFI-18/EPSRC-CDT/3585-PIADS. We acknowledge the support of our colleagues and students, in particular Dr Thomas O'Connor, Peter Milner, Dr Cara-Lena Nies and Dr Vitaly Zubialevich.

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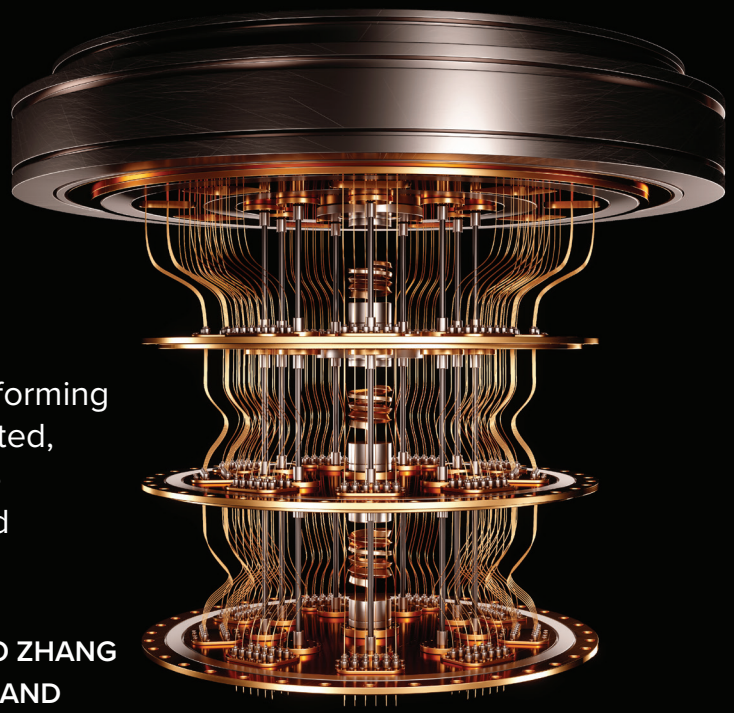
Powering quantum and space technologies



Cutting-edge power devices are performing in the coldest environments ever tested, unlocking new possibilities for space exploration, quantum computing, and energy systems.

BY XIN YANG, ZINENG YANG AND YUHAO ZHANG FROM THE UNIVERSITY OF HONG KONG AND LINBO SHAO FROM VIRGINIA TECH

IN THE shadowed craters of the Moon, inside quantum computers, and within futuristic superconducting power grids, electronics faces a common enemy: extreme cold. Temperatures below 4 Kelvin, that's less than -269°C, are not just harsh – they're a fundamental barrier. When exposed to these conditions, most materials grind to a halt, with electrons 'freezing' in place and refusing to move. Yet, these frigid environments are precisely where tomorrow's technologies will thrive.

For quantum computers, temperatures that are very close to absolute zero are needed to stabilise qubits. Incredibly low temperatures will also be endured by spacecraft sent to explore Pluto or Mars, with electronics having to survive -230°C. And futuristic energy grids, relying on superconducting cables, will demand power converters that operate in the cold. Until now, one critical question has lingered: Can power semiconductors – the backbone technology of energy conversion – function in these extremes?

Answering this question is the groundbreaking study by our team from Virginia Tech and the University of Hong Kong. We have been testing silicon, SiC, and GaN power devices down to 0.1 K, which is colder than the vacuum of space. These investigations have provided the first ever insight into how power devices perform deep within the cryogenic regime, using evaluations based on switching tests and static characterisations (see Figure 1). Our results, obtained using tools employed in quantum physics research, reveal a new frontier for power electronics.

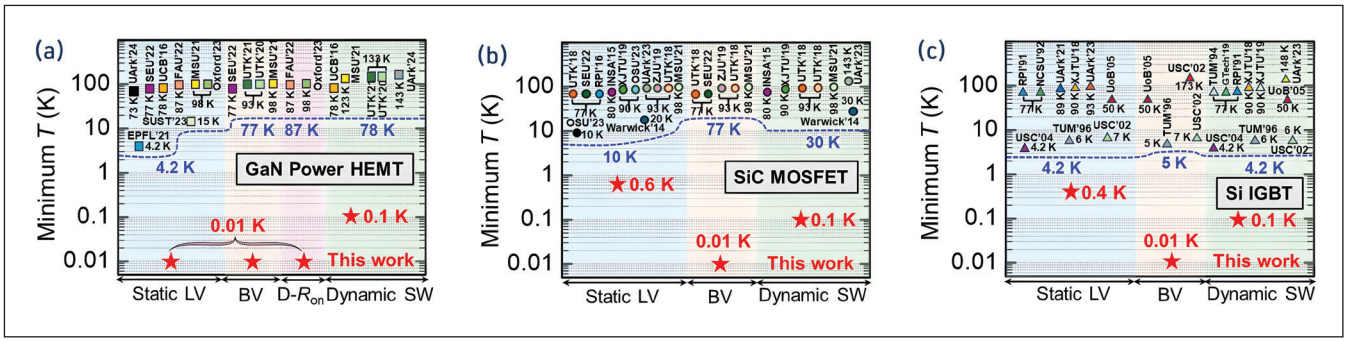
Breaking the ice

Our investigation has involved the use of a dilution refrigerator, originally designed for quantum physics experiments, and repurposed for power electronics testing (see Figure 2). Unlike conventional refrigerators, our high-tech 'freezer' uses helium isotopes to cool samples to 0.1 K – a staggering 10,000 times colder than liquid nitrogen.

The cooling process begins with a pulse tube cryocooler, lowering the temperature to 3 K using helium gas. The dilution unit then takes over, leveraging a quantum cooling mechanism where helium-3 and helium-4 isotopes separate into two phases below 0.87 K, with helium-3 extracting heat as it moves between them. The mixing chamber, the coldest point at 10 mK, serves as the mounting location for test devices.

Adapting this system for power electronics, which operate at high voltages, high currents, and fast switching speeds, posed a number of challenges, including increased measurement noise and potential thermal instability.

To overcome them, we engineered a custom setup, featuring: a daughter board mounted at 10 mK; superconducting cables to carry high currents without resistance; and a dynamic test circuit, to simulate real-world switching conditions. Using this setup, we undertake reliable performance evaluation in extreme cold.



➤ Figure 1: Reported cryogenic studies of (a) GaN power HEMT, (b) SiC MOSFET and (c) silicon IGBT, highlighting the unexplored range in the prior literature. The lowest temperature, research institute, and year of each report are marked. Studies are grouped into the static low-voltage (LV) test, breakdown voltage (BV) test, dynamic on-resistance (D-R_{ON}) test, and dynamic switching (SW) test. The lowest temperature for device characterisation in this work is marked in star symbols for different types of tests.

To accurately assess the performance of power semiconductors at cryogenic temperatures, we use two complementary measurement systems: a dynamic switching test and static current-voltage sweeps. For our double-pulse test, we pulse devices on and off within microseconds, allowing us to capture turn-on/off speeds and dynamic resistance with high precision. To combat signal distortion, we use a noise-cancelling model to filter out cable-induced interference.

For measurements of steady-state characteristics, we connect a Keysight B1505A curve tracer to the dilution fridge. This instrument maps voltage thresholds, leakage currents, and breakdown limits of devices at 0.1 K. To prevent thermal instability, we limit the maximum test current to 1 A.

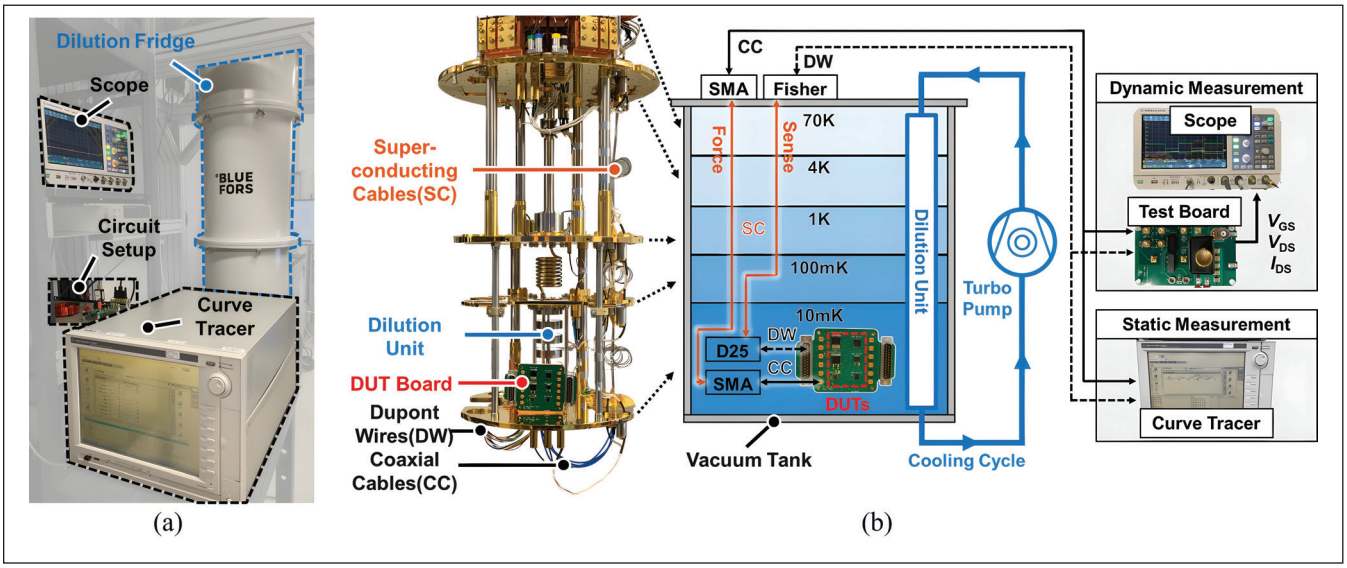
We have tested three industry-standard power devices rated at 650 V: a GaN HEMT, a SiC MOSFET, and a silicon IGBT. As well as spanning three mainstream power semiconductor materials, this selection included both unipolar and bipolar devices.

Our ultimate goal has been to determine whether these devices block high voltages, switch efficiently, and avoid catastrophic failure in the extreme cold – essential for future cryogenic power systems.

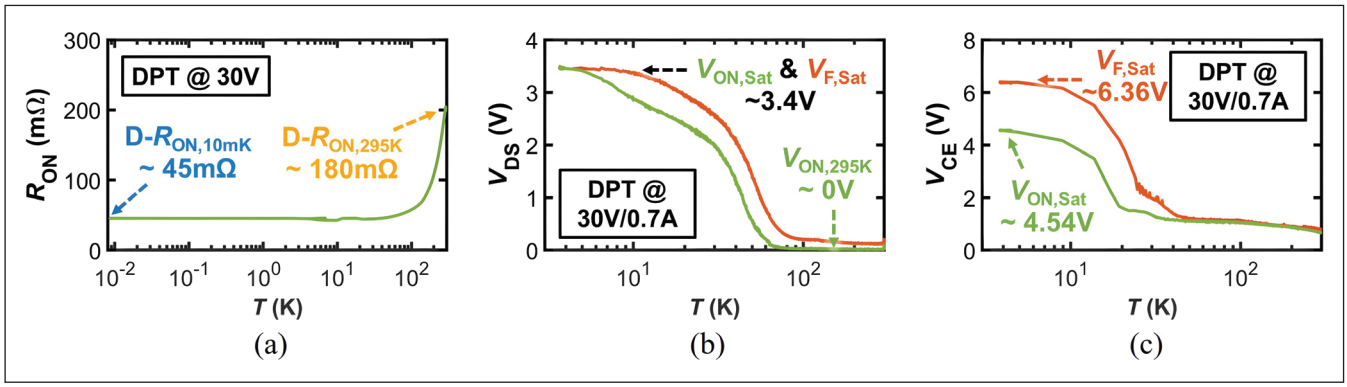
GaN: The cryogenic champion

Among the three classes of device tested, the GaN HEMT demonstrates remarkable performance improvements at cryogenic temperatures (see Figure 3 (a)). At 0.1 K, on-resistance drops by 4.5 times, significantly reducing conduction losses. This benefit comes from avoiding the trapping-induced degradation under switching stress that occurs at room temperature, with exhibited dynamic on-resistance-free behaviour – a long-sought breakthrough in power electronics. Another encouraging result is that the GaN HEMT maintains a robust breakdown voltage over 1129 V, well beyond its 650 V rating, confirming ruggedness in extreme cold.

The secret behind GaN's cryogenic prowess lies in its two-dimensional electron-gas conduction channel, formed by atomic-level polarisation rather than chemical doping. This unique mechanism renders GaN immune to carrier freeze-out, a phenomenon that traps charge carriers in doped semiconductors at low temperatures.



➤ Figure 2: (a) Photograph and (b) an illustration of a cryogenic test setup, which consists of a BlueFors dilution fridge, a Keysight B1505 curve tracer, and a customised circuit test setup. The daughter board with the device under tests (DUTs) is mounted on the 10 mK plate, and other components and equipment are placed outside the fridge.



➤ Figure 3: Extracted dynamic R_{ON}, on-state voltage (V_{ON}) and forward voltage (V_F) of (a) GaN HEMT, (b) SiC MOSFET and (c) silicon IGBT as a function of temperature down to 10 mK. The V_{ON} is defined as the device voltage at a current of 100 mA, while V_F represents the device voltage at 1 A.

Our findings unlock new possibilities for cryogenic electronics. GaN has the capability to enable compact, efficient power supplies for quantum computers, where precise, low-noise control circuits are essential. It could also be deployed in space missions, where lightweight cryogenic converters built with GaN could replace bulky resistive heaters, offering more-efficient power management in deep-space environments.

SiC and silicon: Functional, but higher loss

While the SiC MOSFETs and silicon IGBTs successfully block beyond their rating of 650 V, with values of 830 V for SiC and 619 V for silicon at 0.1 K, conduction losses ramp up as temperatures drop (see Figure 3 (b) and (c)). We found that SiC MOSFETs lose their ohmic current-voltage characteristics and exhibit a 3.4 V turn-on voltage, requiring extra voltage to start conducting, while silicon IGBTs exhibit a two-step turn-on, demanding 6 V to fully activate.

The root cause of this inefficiency lies in the drift layer, a lightly doped region responsible for blocking voltage. At cryogenic temperatures, this layer becomes nearly insulating, preventing electrons from flowing freely – until quantum mechanics kicks in. Two effects help to restore conduction: electron tunnelling, where electrons bypass energy barriers; and shallow-level impact ionisation, where high-energy electrons knock loose additional charge carriers from frozen donor atoms, triggering a microscopic chain reaction.

Unfortunately, the current flow that's enabled by shallow-level impact ionisation is accompanied by higher voltages, leading to significant energy losses. For SiC and silicon, operating at cryogenic temperatures comes at a steep efficiency cost, positioning these candidates as far less viable ones for ultra-cold power electronics, compared with GaN.

The road ahead

Our results open the door to many opportunities in quantum computing, space exploration, and energy grids.

Considering these opportunities one by one, modern quantum computers rely on room-temperature electronics, with extensive cabling required to connect qubits to external power supplies. Such a setup introduces noise and signal degradation, limiting system performance. If cryogenic GaN power converters are integrated directly within the low-temperature environment, this would ensure power delivery just inches from the qubits, drastically reducing noise and improving computational accuracy. This advancement could hold the key to unlocking more stable, scalable quantum processors.

For future space missions, including NASA's Artemis programme, one can envision lunar bases equipped with superconducting magnets for radiation shielding. These systems require efficient cryogenic power management, which currently demands heavy shielding and resistive cooling to maintain functionality. Introducing GaN-based power converters could provide a lightweight and energy-efficient alternative, operating reliably at 0.1 K without the need for additional cooling. Such a solution is ideal for deep-space applications, where efficiency and weight savings are critical.

The third opportunity at ultra-cold temperatures, next-generation superconducting power grids, could see GaN helping to revolutionise energy transmission by enabling lossless electrical transport. However, to maintain superconducting states, there has to be continuous cryogenic cooling. Pairing these power grids with GaN-based converters could enhance overall system efficiency by providing compact, low-loss power conversion at ultra-low temperatures. This integration could pave the way to more sustainable, energy-efficient infrastructure.

To help to fulfil all these new opportunities, our team at Virginia Tech and the University of Hong Kong is currently working towards a circuit- and system-level demonstration of deep cryogenic power electronics.

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Pulsed MOCVD promises to improve AlN-based power devices

Quasi-vertical Schottky barrier diodes highlight the capability of pulsed MOCVD for growing high-quality *n*-type material

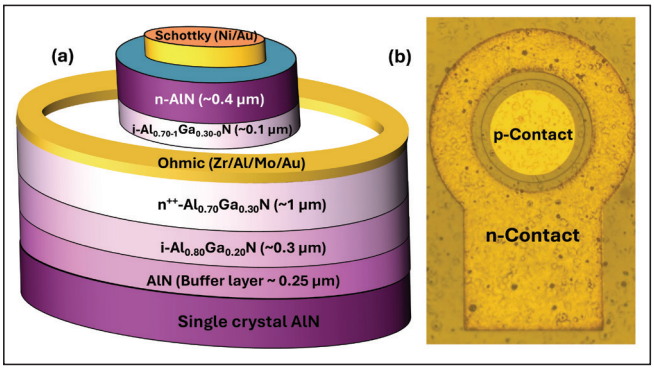
AlN has tremendous potential as a material for power electronics, with a key metric, the Baliga figure of merit, exceeding that for all other ultra-wide-bandgap semiconductors. However, device performance is held back by difficulties associated with doping, including high ionisation energies and the formation of self-compensating defects.

But much progress is possible by moving from conventional growth methods to pulsed MOCVD, according to a team of engineers from the University of South Carolina. These researchers are claiming that pulsed MOCVD enables more efficient doping of AlN, alongside a lower ionisation energy and superior doping control.

As the difficulties associated with doping AlN are well known, the nitride community has investigated a number of innovative techniques to try and address this issue. Efforts include the use of metal-modulated MBE, undertaken at low temperatures that reduce the formation of self-compensating defects; and the addition of a UV source during the MOCVD process, a solution that's difficult to implement, but enables Fermi-level control and mitigates self-compensation. With the latter technique, silicon-doped AlN layers have a doping density of 2 x 10^{15} cm^{-3} and a mobility of 160 cm^2 V^{-1} s^{-1}.

The team from the University of South Carolina argues that their pulsed MOCVD is simpler to implement than that involving a UV source. Earlier this year they reported that switching from conventional to pulsed MOCVD enables an increase in the conductivity of AlN by an order of magnitude, and now they are demonstrating the capability of this growth technology for fabricating quasi-vertical Schottky barrier diodes.

To produce these power diodes, the team began by taking an AlN substrate and using conventional MOCVD to grow a 250 nm-thick undoped AlN buffer layer, followed by an unintentionally doped $Al_{0.8}Ga_{0.2}N$ layer, a 1 µm-thick silicon-doped $Al_{0.7}Ga_{0.3}N$ layer for contact formation, and a 100 nm-thick undoped graded layer, with the aluminium mole fraction increasing from 70 percent to 100 percent.



➤ Engineers from the University of South Carolina have demonstrated the prowess of pulsed MOCVD for AlN growth by using this technology to produced quasi-vertical Schottky barrier diodes (a). The top view of the fabricated device (b).

Co-author of the paper detailing this work, Abdullah Al Mamum Mazumder, told *Compound Semiconductor* that they use conventional MOCVD for the growth of these layers, because it is capable of combining efficiency with high growth rates.

"To grow doped AlN layers, the use of pulsed MOCVD offers important advantages in terms of achievable dopant incorporation and smaller donor ionisation levels. This is why in this work we used pulsed MOCVD to grow the active AlN layer only."

The engineers produced quasi-vertical Schottky barrier diodes with a circular geometry from their epiwafers. To form these devices, they used standard photolithography and inductively coupled plasma reactive ion etching to define mesas and access the $Al_{0.7}Ga_{0.3}N$ layer – on this layer they formed the *n*-type contact, using electron-beam evaporation. Schottky contacts were added by electron-beam evaporation. This completed fabrication of the diodes, which had a 10 µm gap between the Schottky and ohmic contacts.

Electrical measurements revealed that the team's Schottky barrier diodes have a breakdown voltage of around 395 V. According to simulations, the peak electric-field-breakdown is 9.9 MV cm^{-1}. The engineers point out that incorporating passivation and field-plating would allow the electric field at breakdown to get close to the critical field for AlN – that's 12-15 MV cm^{-1}.

The team's Schottky barrier diodes have a turn-on of around 2.2 V and an ideality factor of 2.4, due to oxide formation on the AlN surface and an imperfect metal-AlN interface. "We are planning to address these issues in our future work," says team member Tariq Jamil.

Other goals include systematic studies of pulsed MOCVD growth of AlN and AlGaN materials with a very high aluminium content.

"Our tasks include increasing doping levels, material quality optimisation, and mobility and current transport analysis and optimisation," says Mazumder. "We are also working on developing new devices using pulsed MOCVD. These include vertical and quasi-vertical Schottky and *p-n* diodes, as well as transistors."

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➤ A. A. M. Mazumder *et al*. Appl. Phys. Express. **18** 065501 (2025)

Red InGaN microLEDs: Boosting efficiency with all-ITO contacts

Replacing a metallic *p*-type contact pad and *n*-type electrode with those based on ITO boosts the extraction efficiency of red microLEDs

ENGINEERS from King Abdullah University of Science and Technology (KAUST), Saudi Arabia, have substantially increased the performance of their microLEDs by using ITO for all the contacts.

By retaining the *p*-type ITO electrode and using this oxide for the *n*-type electrode and *p*-contact in their red-emitting InGaN devices, the team have increased external quantum efficiency by 60 percent and wall-plug efficiency by 50 percent.

These gains could aid the development of full-colour GaN-based microLED displays, which are promising candidates for augmented- and virtual-reality headsets, smartphones and watches.

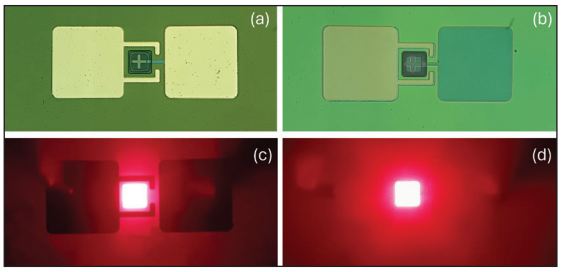
Red LEDs that are based on InGaN are far less efficient than their blue cousins, due to the increase in indium content in the quantum wells that introduces substantial strain and crystal imperfection. Due to these drawbacks, it is paramount to optimise the light extraction efficiency of these emitters.

Light generated within an LED can fail to exit the device due to absorption, total internal reflection and shading from opaque electrodes.

It is well known that metallic *p*-electrodes, typically positioned on the top surface, significantly block light extraction. Previously, the team from KAUST addressed this weakness in red and green microLEDs, without compromising electrical performance, by replacing metal *p*-type electrodes with those made from ITO. This switch increased light extraction efficiency, light output power, external quantum efficiency and wall-plug efficiency.

Now the team has turned its attention to *n*-type electrodes and *p*-contact pads – positioned around the periphery of the active mesa region, they enable contact probing and effective current injection.

As light can be reflected within the device, the *n*-type electrodes and *p*-contact pads can lead to absorption or additional reflection, and ultimately reduce the light extraction efficiency. One option to address these losses is to replace the metal *n*-type electrodes and *p*-contact pads with transparent ones based on ITO.



➤ Comparing the optical microscope images, (a) and (b), with the light emission images (c) and (d), highlights the benefits of using ITO for all the contacts of a microLED.

To quantify the benefits of *n*-type electrodes and *p*-contact pads made from ITO, the researchers from KAUST have compared the performance of two forms of red-emitting microLED: one that combines *p*-type ITO with metallic *n*-type electrodes and *p*-contact pads; and another that employs ITO for all contacts.

Both forms of microLED were produced by growing an epitaxial structure on a patterned sapphire substrate by MOCVD. Devices were produced from the epiwafer with a number of steps that include photolithography and etching to define mesas, passivation through the addition of SiO_2 on the sidewalls, and the deposition of ITO by electron-beam deposition.

Electroluminescence imaging reveals that the ITO electrodes enable higher light extraction in the electrode region, with metal contacts significantly blocking the emitted light (see figure).

The emission from the all-ITO LED has a peak in its electroluminescence at 653 nm at a drive current density of 1 A cm^{-2}, compared with 648 nm for the variant that incorporates metal contacts. The team attributes this slight difference to fluctuations in indium composition.

At first glance, the wavelength of these microLEDs appears to be longer than that required in colour displays, given that the red sources employed in high-definition TVs and augmented-reality displays have a dominant wavelength of around 610 nm, and red LEDs for ultra-high-definition TVs and virtual-reality headsets have a dominant wavelength of around 630 nm. However, according to KAUST spokesman Kazuhiro Ohkawa, the team's all-ITO red microLEDs with a 653 nm peak wavelength have a full-width at half maximum of 53 nm and a dominant wavelength of 630 nm.

"If you look in other literature, you will find so-called red LEDs with peak wavelengths around 600-620 nm or less," explains Ohkawa. "Their colour appears orange to the human eye. Our LEDs are true red."

According to on wafer-measurements, peak external quantum efficiency with the all-ITO microLED is 2.1 percent, and maximum wall-plug efficiency hits 1.7 percent. Packaging these LEDs and measuring their output with an integrating sphere would lead to higher values for these key metrics, says Ohkawa. "The peak absolute external quantum efficiency and wall-plug efficiency of our red LEDs with packaging are expected to be 7 percent and 6 percent, respectively."

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➤ C. Altinkaya *et al.* Appl. Phys. Express **18** 061001 (2025)

AlGaN deep-UV LEDs: Less is more

Thicker layers of n-type AlGaN fail to enhance the optical performance and material quality of AlGaN quantum wells grown on AlN templates, formed by face-to-face annealing

A JAPANESE collaboration has demonstrated that it should be possible to produce high-quality deep-UV LEDs with minimal MOCVD growth, using face-to-face annealed templates.

This work by researchers from Mie University, Tohuku University and the University of Tsukuba offers a promising approach to lowering the cost of production for deep-UV LEDs.

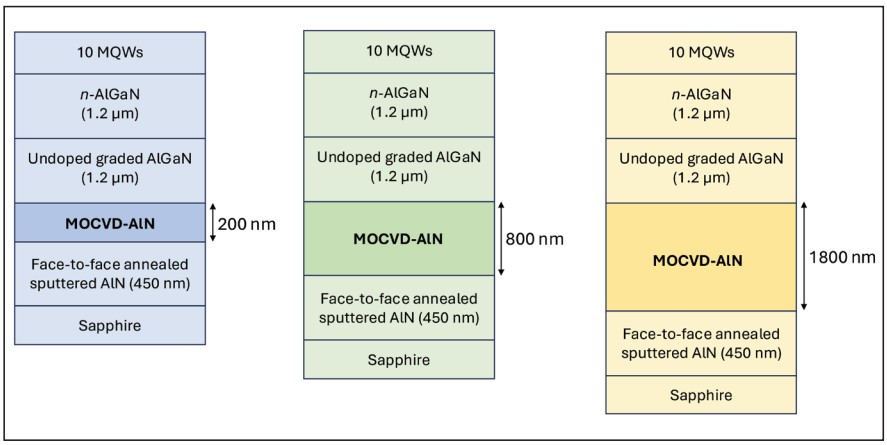
The team's latest effort builds on its previous work, involving the development of high-quality templates with dislocation densities of less than 10^8 cm^{-2}, produced via face-to-face annealing of sputter-deposited AlN. UVC LEDs produced on these templates and emitting at 263 nm have an external quantum efficiency of 8 percent.

According to the team, this is a record for external quantum efficiency – and it should be attributed to the switch from conventional MOCVD-grown AlN templates to those produced by face-to-face annealing of sputter-deposited AlN.

Initial work by the researchers employed MOCVD-grown AlN with a thickness of just 200 nm on the novel templates. The latest effort has considered the impact of thicker layers, which could lead to a reduction in dislocation densities within the device and ultimately a higher internal quantum efficiency.

For this investigation the researchers used three 450 μm-thick AlN films, created by RF sputtering on *c*-plane sapphire with a 2° off-cut relative to the *m*-axis. These films were annealed for 3 hours at 1700°C, under nitrogen gas with a face-to-face configuration.

Using MOCVD, the team deposited an 800 nm-thick AlN layer on one of these samples and added an 1800 nm-thick layer of AlN on another. To provide a benchmark, they decided not to grow any AlN on their third sample.



➤ A thorough study of the material quality and emission characteristics of three different samples shows that there's no significant benefit from the growth of thicker AlN layers.

Following storage under nitrogen, all three samples were placed in an MOCVD chamber, used to grow an epistructure featuring an active region with ten 2 nm-thick $Al_{0.69}Ga_{0.31}N$ quantum wells sandwiched between 3.6 nm-thick $Al_{0.44}Ga_{0.56}N$ barriers (see figure for details of the structure).

Drawing on information provided by X-ray rocking curves, the team determined that the increase in AlN thickness led to an increase in the edge-type dislocation density from 3.5×10^8 cm^{-2} to 6.4×10^8 cm^{-2}. Screw-dislocations are far less prevalent, with a density of just 1.6×10^6 cm^{-2}.

Scrutinising samples with cross-sectional scanning transmission microscopy confirmed results obtained X-ray rocking curves, with an increase in the thickness of AlN from 200 nm to 2000 nm causing the density of edge-type dislocations to increase from 2.1×10^8 cm^{-2} to 6.4×10^8 cm^{-2}.

To investigate point defects, the researchers turned to the positron annihilation method. This approach determined that the type and the concentration of vacancy-type defects, at least in the upper part of *n*-type AlGaN, is identical for different thicknesses of AlN.

Plots of photoluminescence efficiency are similar for all three samples, indicating that changes to the thickness of AlN only have a slight impact on emission characteristics.

To try and uncover any differences in internal quantum efficiency between the samples, the team employed time-resolved photoluminescence measurements. This study found long lifetimes of over 2 ns under weak excitation, a result comparable to that for quantum wells on AlN substrates, highlighting the high quality of all three samples. Efforts also determined that the internal quantum efficiency is the same in all three samples.

Based on their findings, the team concluded that when employing face-to-face annealed templates, it's possible to produce high-quality quantum wells on MOCVD-grown AlN with a thickness of just 200 nm.

REFERENCE
➤ R. Akaike *et al.* Appl. Phys Express **18** 065503 (2025)

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