



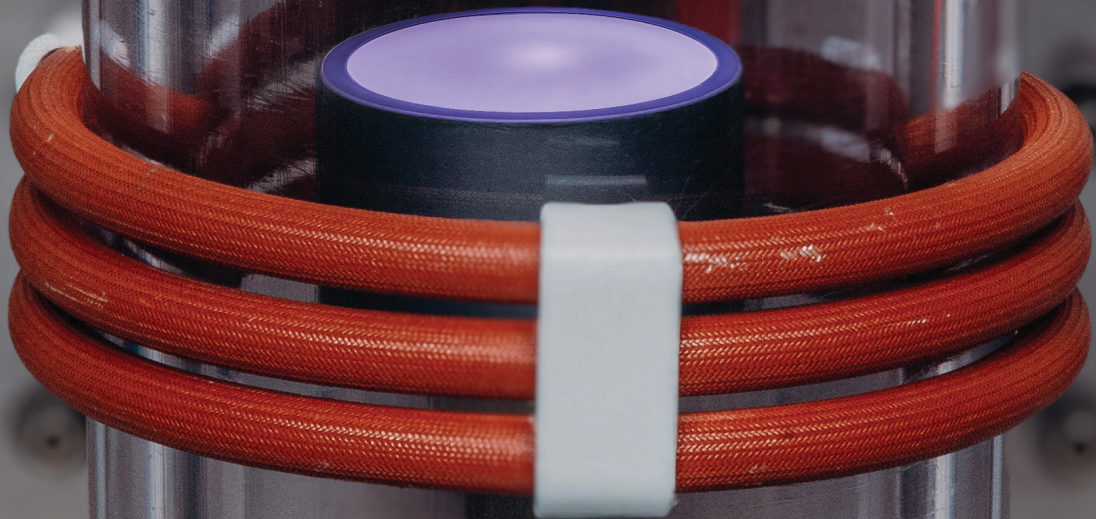
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VIEWPOINT

BY RICHARD STEVENSON, EDITOR



From the vault

FOR MANY DECADES, this publication has been leading the way in reporting all matters related to the compound semiconductor community. Launched in print form in 1995, we have expanded our approach over many years, adding digital versions of the magazine and a website that now combines news and views with videos.

While this rich legacy has much value, you have not been able to access all of. On our website, magazines produced under Angel Business Communications have been accessible, but much content dating back further has not been available.

It's an omission that's been nagging away at me – and one that I've started to address. While I don't have copies of all early print editions, I'm fortunate to not live that far from a former editor who does, Tim Whittaker. So, I have been borrowing his collection, and helping to ensure that you can access this content.

It's a time-consuming process to archive our early editions. Whether we scan or photograph, there are thousands and thousands of pages to capture, and then assemble as magazines.

If you take a look on our website, you'll see that we have made some progress. You can now read a number of editions from the mid-1990s and beyond, covering some fascinating topics. This includes the demise of Cray, a pioneer of supercomputers that could see much merit in using GaAs rather than silicon for microprocesses; and reports relating to the development of MBE in space, where a superior vacuum aids epitaxy.



Over the coming months, we'll be adding more editions. You'll be able to read how the dot.com boom and subsequent bust fuelled and rocked our industry, as well as learning about the birth of SiC power devices and the early successes of the LED industry.

By the time we have added all our early content, you will have access to every edition from 1995 to 2003; and from 2005 onwards. But what about the issues from 2004, the year I started to work on this publication? Well, I have the magazines from when I began – that's the June issue onwards – but neither Tim nor I have the first four issues for that year.

Maybe you can help us? Do you happen to keep all your print copies, and would allow us to borrow those missing from our collection, to add to our archive? If so, please get in touch, and help this community access more of its rich history. Just send an e-mail to me: Richard.Stevenson@angelbc.com

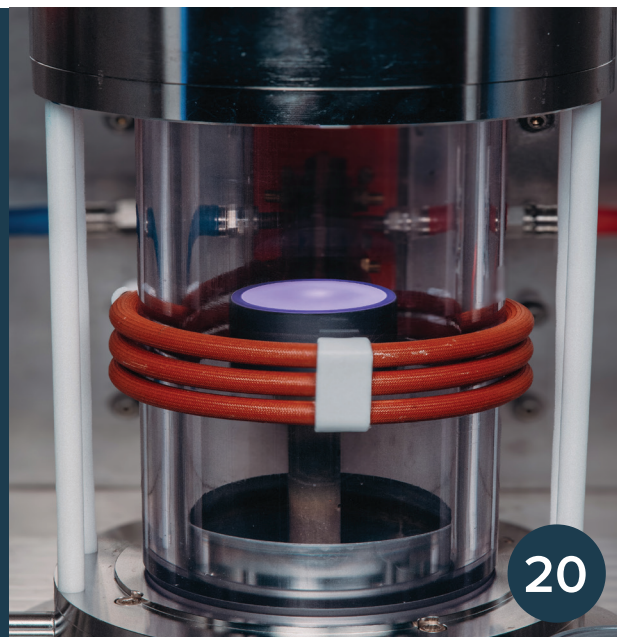
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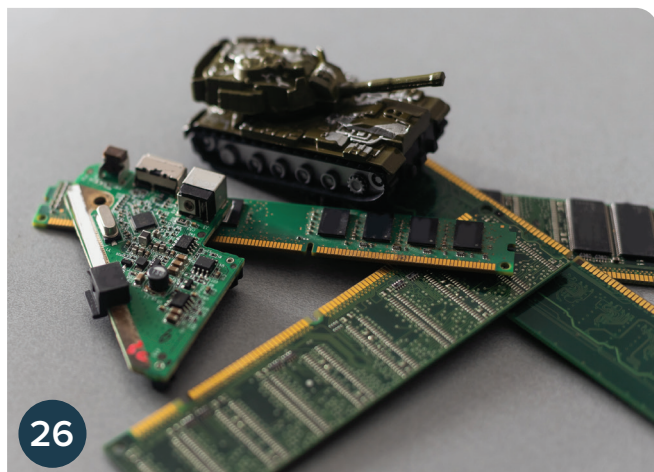
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Power electronics at a turning point, says Yole

Leaders remain dominant for now, but challengers emerging in an environment shaped by overcapacity, pricing pressure and geopolitical tensions

THE global power electronics industry is entering a new phase, according to Yole Group's latest report, 'Status of the Power Electronics Industry 2026'.

After years of rapid expansion fuelled by electrification and renewable energy, companies are now navigating a more complex environment shaped by overcapacity, pricing pressure, geopolitical tensions, and intensifying competition.

Following a turbulent 2024-2025 period marked by geopolitical uncertainty, lower-than-expected EV demand, and significant manufacturing overcapacity, the power electronics industry is entering a new phase focused on consolidation, cost optimisation, and competitive positioning.

Despite these challenges, Yole Group forecasts the power device market to continue growing at a 7.1 percent CAGR between 2025 and 2031, reaching \$41.3 billion by 2031. While growth prospects remain robust, industry priorities are changing.

Milan Rosina, Yole's principal technology and market analyst for power electronics & battery, said: "The power electronics industry is entering a new phase: growth continues, but the focus has shifted from expansion to

TOP 20 POWER DEVICE MANUFACTURERS' REVENUE: 2025 RANKING AND POSITIONING ON DIFFERENT DEVICE TECHNOLOGIES

Source: Status of the Power Electronics Industry 2026 report, Yole Group



competitiveness, cost optimisation, and market share."

One of the main messages delivered by Yole Group's analysts is the accelerating rise of Chinese players across the power electronics value chain. Supported by strong domestic demand in EVs, photovoltaics, wind energy, and battery storage systems, Chinese companies are rapidly expanding their presence in SiC wafers, power devices, and industrial power modules, increasing competitive pressure on established global suppliers. Xiran Zuo, Yole's technology and

market analyst for power electronics, said: "Power electronics is entering a new chapter. Companies are moving from capacity expansion to profitability, operational excellence, and long-term market positioning."

With electrification, renewable energy deployment, AI-driven infrastructure expansion, and automation continuing to drive demand, Yole says that understanding the evolution of the power electronics industry has never been more critical for device manufacturers, material suppliers, equipment providers, system integrators, and investors.

SK Siltron to close Michigan SiC fab

THE Korean company SK Siltron announced it is winding down its Michigan SiC plant, citing 'market conditions' as the reason for closing its doors, affecting all 140 employees on site within 60 days.

In an article on the *Michigan Public NPR* website, SK Siltron spokesman Joe Guy Collier is quoted as saying the company originally expanded manufacturing in

the US to meet what was then growing customer demand for a specialised product used in electric vehicles. "Significant changes in the EV market have created sustained challenges for the SiC wafer business," said Collier.

In October 2024, SK Siltron closed a deal to get a \$544 million loan, now repaid, financed through the US Department of Energy to expand



American manufacturing of high-quality SiC wafers for EV power electronics.

EU approves €353 million for Element 3-5 SiC facility

Element 3-5 receives one of four direct grants through German state aid to develop first-of-a-kind semiconductor facilities

THE EUROPEAN COMMISSION has approved €659 million in direct grants through German state aid to develop four first-of-a-kind semiconductor facilities.

€353 million of this will go to the compound semiconductor company Element 3-5 GmbH for a facility in Baesweiler, North Rhine-Westphalia, to manufacture SiC epiwafers.

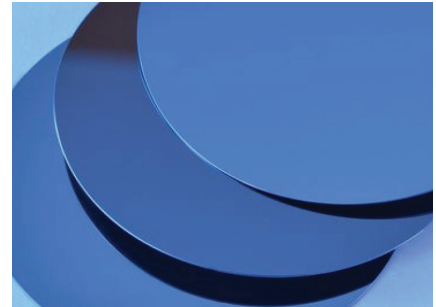
Element 3-5's SiCnature epiwafers have a very thin, high-quality layer added on top to improve their performance compared to standard SiC wafers.

The new type of wafers are expected to be used in end applications

across various sectors, including automotive, industrial, telecommunications and energy.

The project involves major improvements, notably in the manufacturing process. It will improve energy efficiency, yield and manufacturing efficiency, compared with conventional hot-wall chemical vapour deposition.

The other recipients of grants are: Vishay (€214 million) to establish more manufacturing capacity in Itzehoe, Schleswig-Holstein, for making next-generation power MOSFETs; KLA (€74.4 million) for a facility in Weilburg, Hesse, for manufacturing optical



overlay and film metrology equipment; and Ketek (€17.9 million) to construct two production lines for specialised silicon chips: Silicon Drift Detector (SDD) chips and graphene radiation entry window chips, which are key components of the SDD detectors Ketek already builds.

UK microLED start-up Pixel-Flo raises £5.25 million

PIXEL-FLO, a spinout from the University of Sheffield's School of Electrical and Electronic Engineering, has secured £5.25 million funding to enhance microLED technology manufacturing, helping to cut costs and speed up current production methods.

MicroLEDs offer higher brightness and low power consumption for smartwatches, car dashboard displays, TVs and PC monitors. However, they are difficult to mass produce, due to the challenge of moving the millions of microscopic LEDs from the wafer to the display backplane.

Pixel-Flo has developed an entirely new mass-transfer process that could enable microLED displays to be manufactured at industrial scale and more cost effectively by unlocking economies of scale, making them much faster and significantly cheaper to produce.

The funding, led by Northern Gritstone,



an investment company dedicated to supporting ambitious science and technology businesses in the North of England, with additional investment from SCVC, the Parkwalk Northern Universities Venture Fund, and German investment firm, HTGF, will support Pixel-Flo's transition from laboratory development towards industrial scale-up, expanding their team and relocating to new lab and office space.

Pixel-Flo was founded by Rick Smith, Suneal Ghataora, and Simon Jones. The company builds on novel semiconductor photonics research from Ghataora in Smith's lab, drawing on long-running LED research from the University of Sheffield's School of

Electrical and Electronic Engineering, and Simon Jones's extensive display-industry commercial experience.

Rick Smith, CEO and co-founder of Pixel-Flo, said: "This investment allows us to expand our team and demonstrate our unique technology on a commercial coating system, enabling partnership and evaluation by display manufacturing partners. We are proud to have a fantastic international consortium of complementary investors led by Northern Gritstone supporting our international ambitions to enable huge new market opportunities for microLED."

Sue Hartley, VP for Research and Innovation at the University of Sheffield, said: "The company's approach to addressing a critical bottleneck in industry together with its international growth ambitions are an inspiration to other spin-out companies emerging from the North of England. I am excited to see the company grow following this new investment."

Wolfspeed files patent lawsuit against Navitas

Company takes action to protect its GaN and SiC IP

WOLFSPEED has filed a patent infringement lawsuit in the United States District Court for the District of Delaware against Navitas Semiconductor.

The lawsuit asserts that a broad range of Navitas products infringes multiple Wolfspeed patents, including US Patent Nos. 8,169,005, 10,998,418, 10,886,396, 10,749,443, and 11,888,392.

Products accused of infringement encompass major product lines of Navitas, including its GaN-based FETs — such as the GaNFast, GaNSlim, and GaNSafe product families — as well as Navitas's GeneSiC MOSFETs and SiCPAK modules.

“Wolfspeed’s foundational technology helped create this industry, and we are deeply committed to defending the intellectual property that represents decades of innovation and R&D



investment. We respect the IP rights of others, and we expect the same respect in return,” said Robert Feurle, Wolfspeed’s CEO.

“Protecting our patent portfolio is a strategic priority for the company and our shareholders. This action reflects

our commitment to enforcing our rights and protecting continued investment in next-generation SiC and GaN technologies.”

Navitas’ CEO, Christopher Alexandre, has commented on Wolfspeed’s actions in a Q2 earnings call (see p. 9).

Renesas sues Navitas over trade secrets

THE Japanese semiconductor company Renesas is suing US-based Navitas in the California federal court, claiming the company poached its employees to steal trade secrets for developing next-generation GaN chips.

According to a Reuters report on 22nd July 2026, Renesas alleges that California-based Navitas’ CEO Christopher Alexandre and executive Felicia Cheng stole confidential Renesas information for Navitas related to GaN-based chips for data centres.

“Within a short period of time after Alexandre assumed the role of CEO, Navitas announced a new ‘2.0’ strategy that directly mirrored Renesas’ confidential plans – targeting the same customers, the same technologies, and the same market opportunities reflected in the stolen materials,” Renesas said in its complaint.



The complaint said that Alexandre and Cheng took confidential PowerPoint presentations to Navitas that contained Renesas trade secrets.

“Any Renesas competitor (like Navitas) could use the information in these presentations to engineer the same

secret product specifications Renesas has designed, knowing Renesas’ timelines, to beat Renesas to market to steal billion-dollar contracts,” the lawsuit said.

Renesas is seeking monetary damages and an order blocking Navitas from misusing its secrets.

Navitas CEO makes robust response to patent lawsuits

CEO Christopher Alexandre describes a “campaign of harassment and intimidation.”

NAVITAS CEO Christopher Alexandre has responded to actions taken by Wolfspeed and Navitas Semiconductor regarding IP.

Initial moves in this controversy involved: SiC specialist Wolfspeed filing a patent lawsuit against Navitas Semiconductor over GaN and SiC chips; and Japanese chip firm Renesas (which has a stake in Wolfspeed) alleging that Navitas misappropriated GaN chip trade-secrets by poaching Renesas employees (see p. 8 for details surrounding both stories).

During an upbeat Q2 earnings call on 27th July, Navitas CEO Christopher Alexandre (pictured right) commented on the litigation for the first time, describing the Wolfspeed case as “the last step in a campaign of harassment and intimidation.”

The Wolfspeed lawsuit asserts that Navitas’ GaN-based FETs, GeneSiC MOSFETs and SiCPAK modules infringe multiple Wolfspeed patents.

Renesas alleges that Alexandre, and Navitas executive Feili Cheng, diverted Renesas’s confidential information concerning GaN chips to Navitas.

Alexandre joined Navitas in September 2025. Prior to that, he served as SVP and general manager of the Power Division at Renesas Electronics, where he oversaw the company’s \$2.5 billion power management business.

Putting context around the two cases, Alexandre said: “Wolfspeed already sued us because we stopped buying wafers from them a while back. Then they sued two of our employees that worked at Wolfspeed in the past, including one that they had RIF’d [lost their job due to a Reduction in Force], in their cost reduction effort a while back.”



He added that Wolfspeed then tried to litigate and failed when third-party recruiters were calling Wolfspeed employees for job positions Navitas had online on the web.

On the Renesas case he said: “Based on the public record, Renesas would own up to 39 percent of Wolfspeed. So, is all this a coincidence, the week before the earnings call?” (The beneficial ownership percentage refers to an SEC filing from 31 March 2026).

He added: “You don’t start litigation like this if you are winning market share, [and] your technology is superior.”

Alexandre concluded: “We respect IP and technology. Actually, the company is a result of decades of innovation coming from start-ups in both GaN and SiC. We let everybody draw their own conclusion on why now Wolfspeed and their major shareholder are running to the courthouse instead of competing in a fair way in the marketplace.”



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EYEQ Lab reveals 200 mm SiC wafer

Korea's first mass-produced SiC wafers showcased at KEMS 2026

EYEQ Lab, a Korean power semiconductor company, has recently unveiled Korea's first mass-produced 8-inch (200 mm) SiC power semiconductor wafer at the 2026 Korean Institute of Electrical and Electronic Material Engineers (KEMS 2026), held from June 24-26 at BEXCO in Busan.

The company exhibited its production-ready 8-inch SiC wafers, manufactured at its recently established 8-inch SiC dedicated fabrication facility in Busan, marking a milestone for Korea's power semiconductor industry.

Alongside the wafer exhibit, EYEQ Lab exhibited a range of application products powered by its proprietary Q-Device SiC technology, including a 65 W SiC quick charger, a high-efficiency SiC power module, and intelligent power modules for industrial and consumer applications.

Last year, EYEQ Lab completed Korea's first dedicated 8-inch SiC fabrication

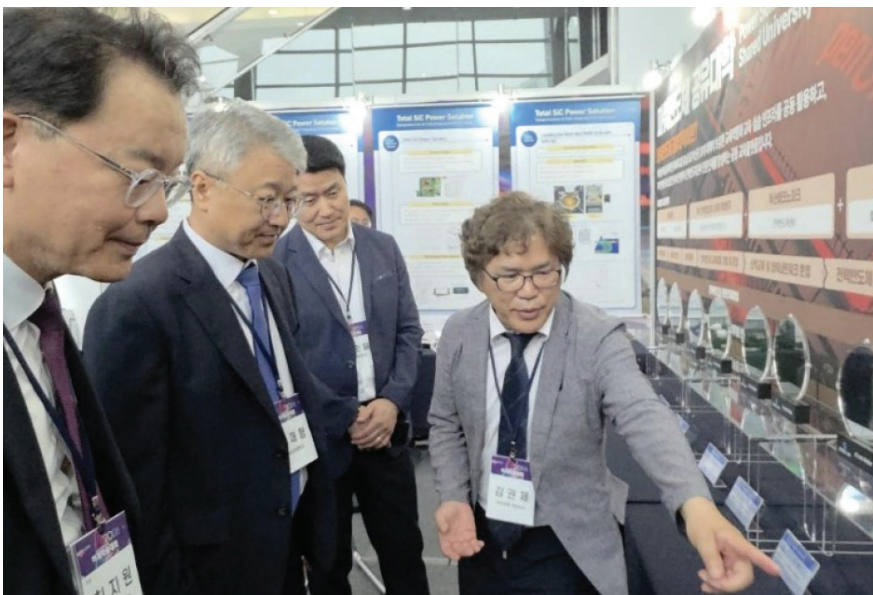
facility within the Busan Power Semiconductor Materials, Components and Equipment Cluster.

The company has since focused on process stabilisation and yield optimisation and is now advancing towards full-scale mass production.

"This exhibition represents the first official public presentation of Korea's first mass-produced 8-inch SiC wafers," said an EYEQ Lab spokesperson.

"Through our Q-Device-based power semiconductor solutions, we aim to enhance the competitiveness of Korea's power semiconductor industry while expanding our presence in the global market."

The company's 8-inch SiC fabrication facility in Jangan-eup, Gijang-gun, Busan, has an annual production capacity of up to 30,000 wafers, and EYEQ Lab says it is expanding commercial supply to customers worldwide.

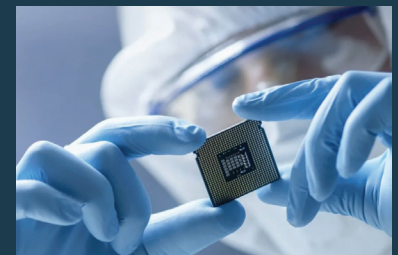


Palomino Labs ships microLED light engine prototypes

Palomino Laboratories, a US microLED start-up, has announced that it has shipped its first-gen microLED light engine prototypes, with second-generation sampling planned by Q3 FY26.

The company has also just signed an agreement to acquire Vega Links, which it says will transform Palomino Labs into a next-generation AI interconnect company supporting copper, microVCSELs and microLEDs.

The firm has a mission to replace copper with microLED in data centres to reduce energy consumption related to interconnects by 6x, combined with 10x higher shoreline density.



It is targeting around 10 Tbps/mm – a step-change in data throughput for AI and next-generation compute, using patented wavelength-division multiplexing that enables two or more wavelengths per microLED.

Along with its own IP, Palomino Labs has licensed 15 patents from the University of California, Santa Barbara.

Academic partners include the University of California on GaN photonics and University of Central Florida CREOL on optical coupling.

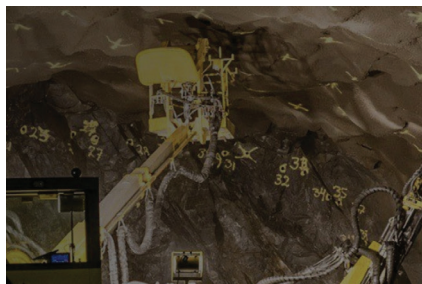
\$250 million CHIPS award for I-Pulse

US pulsed-power specialist gets funding for further development of SiC-powered drilling technology

I-PULSE has announced an agreement with the US Department of Commerce's CHIPS Research and Development Office for a \$250 million award for the further development of I-Pulse's proprietary SiC-based pulsed-power technology.

The CHIPS funding is for R&D to advance the company's semiconductor and pulsed-power drilling technology with the aim of unlocking untapped resources of geothermal power within the United States.

I-Pulse will develop SiC semiconductors



in partnership with US national laboratories, universities, and specialised manufacturers. The company will also commercialise high-temperature, high-current, high-

voltage solid-state switches designed for applications such as underground mining, rock crushing, manufacturing, and defence systems.

I-Pulse co-founder Robert Friedland said: "We are excited to partner with the US government to advance our unique, American technology suite to benefit our great nation. This award supports the development of world-leading critical components in the pulsed-power technology stack, with profound implications for energy security and national defence."

IQE lifts year-on-year growth forecast to 30 percent

Compound semiconductor wafer company IQE has provided a trading update for the six months ended 30 June 2026, with expectations to deliver a full year 2026 revenue growth in excess of 30 percent year-on-year, resulting in an adjusted EBITDA of low-teens of millions of pounds.

Trading in H1 2026 exceeded management expectations, with strong demand across all of the group's core segments. This is expected to result in first half revenue of at least £64 million.

Demand for IQE's InP solutions is continuing to accelerate due to

their critical role in enabling optical photonics products for data centres and AI infrastructure. Revenue growth was also supported by ongoing strength in aerospace and defence segments, as well as robust demand for both 3D sensing and wireless products.

Jutta Meier, CEO of IQE, commented: "I am very pleased that H1 trading exceeded our expectations. Our long-established leadership in InP and other key material systems means we are critically embedded in supply chains enabling industry trends that will continue to deliver further progress in H2. I remain extremely excited about



the significant opportunities ahead for the transformed IQE, and look forward to sharing our continued progress."

IQE remains bank-debt free with a cash position as at 30 June 2026 of £41.6 million.

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IVWorks reGaN tech enables World's first 742 GHz GaN HEMT

Results presented at VLSI Symposium 2026 show that GaN is viable for future sub-terahertz and terahertz electronic systems

Korean company IVWorks' is claiming that its proprietary reGaN selective regrowth technology has played a key role in the world's first GaN transistor to achieve a maximum frequency ($f_{\max}$) exceeding 700 GHz.

This achievement was demonstrated through a 45 nm GaN HEMT device developed by Daehyun Kim's research team in the school of electronics engineering at Kyungpook National University in Korea. It was unveiled on June 18 at the VLSI Symposium 2026.

The research team fabricated a GaN transistor with a 45 nm gate length and achieved an $f_{\max}$ of 742 GHz, said to establish a new benchmark for RF performance in GaN transistor technology. It is claimed that the device also achieved a record average frequency metric (f_{avg}) of 497 GHz, the highest value reported to date for any GaN transistor technology.

These results demonstrate that GaN semiconductors possess sufficient performance competitiveness, even in the ultra-high-frequency regime, and can serve as a viable platform for future sub-terahertz and terahertz electronic systems.

While InP-based transistors have long dominated the sub-terahertz frequency regime, due to their exceptional electron transport properties, their relatively low breakdown voltage limits output power and system scalability.

In contrast, GaN semiconductors offer a unique combination of high breakdown electric field, high power density, and excellent thermal robustness, making them attractive candidates for next-generation high-frequency and high-power applications. However, achieving ultra-high-frequency performance with GaN has remained a significant



challenge. To overcome these limitations, the research team employed an advanced 45 nm gate process and optimised device architecture to maximise high-frequency performance.

A key enabler of this achievement was IVWorks' proprietary reGaN selective regrowth technology. Developed exclusively by IVWorks, reGaN selectively regrows heavily doped n -type GaN in the source and drain regions, significantly reducing contact resistance.

As a co-research partner in this study, IVWorks demonstrated excellent process uniformity across the entire 4-inch wafer and achieved outstanding reproducibility. Furthermore, the company reduced regrowth interface resistance to 0.027 Ω mm, approaching the theoretical limit achievable at the corresponding carrier concentration.

Daehyun Kim of Kyungpook National University commented: "This research pushes the RF performance limits of GaN HEMTs to a new level and demonstrates the potential of GaN semiconductors for ultra-high-frequency applications through the world's first demonstration of a GaN HEMT with an $f_{\max}$ exceeding 700 GHz."

Kim added: "The study is particularly meaningful as a successful example of industry-academia collaboration, combining advanced epitaxial growth and regrowth technologies from industry with the university's expertise in device and circuit research."

Building on this achievement, Kim and co-workers plan to further accelerate the development of next-generation GaN electronic devices targeting terahertz-frequency applications for 6G communications and advanced defence technologies.

The achievement further highlights the growing potential of GaN technology to expand beyond traditional RF and power electronics into emerging sub-terahertz and terahertz applications, including 6G communications, advanced radar systems, satellite communications, and next-generation defence electronics.

Young-kyun Noh, CEO of IVWorks, said: "reGaN is a core technology that has already passed quality qualification at a major foundry and has been adopted for volume production. This achievement demonstrates that our hybrid-MBE-based reGaN platform is not only manufacturing-ready, but also a key enabling technology for next-generation sub-terahertz and terahertz GaN electronics. We are proud to see IVWorks technology contribute to a world-leading research milestone."

Innoscence: Its take on the Munich rulings

Innoscence's says that the current products are not affected by both rulings of the Munich Regional Court.

IN THE long-running patent battle between Infineon and Innoscence, the Chinese chipmaker is taking a positive view, regarding a recent pair of rulings from the Munich Regional Court.

Innoscence says that its GaN power device products fall outside the scope of Infineon's asserted German patents and may be commercialised in Germany without restriction.

According to Innoscence, these rulings are fully consistent with the final determination issued last month by the US International Trade Commission ("ITC"), which found that Innoscence's current products do not infringe Infineon's asserted US patent relating to packaging design (US Patent No. 9,899,481).

The Munich case concerns the German counterparts of that same patent family, says Innoscence, which claims that in line with the ITC's findings, the Munich Court found infringement only with respect to a limited set of legacy products – they are some packaged



650-700 V transistors that had already been discontinued.

Due to this, Innoscence argues that any injunction granted would not apply to its current product portfolio. As a result, it claims that there is no impact to ongoing operations or its customers' use of its products in Germany.

According to Innoscence, the decisions mark another significant milestone in its string of favourable outcomes across major jurisdictions. It is claimed that these outcomes follow recent success in China, where the company secured an injunction and damages award against Infineon, as well as its decisive victory at the ITC in the United States

last month. Together, these rulings are said to reaffirm the legality of Innoscence's current product portfolio and its ability to operate freely in key global markets.

While proceedings in Germany remain ongoing, including Innoscence's invalidity challenges to the asserted German patent, the growing body of decisions across China, the United States, and Germany

underscores that the global litigation campaign initiated by Infineon has not altered the competitive position of Innoscence's core products, says the Chinese chipmaker. It says: To the contrary, independent judicial findings across multiple jurisdictions have consistently validated the robustness of Innoscence's technology and reinforced market confidence in the company's product compliance and innovation capabilities.

Innoscence says it remains committed to advancing its technology leadership and expanding its global footprint, delivering cutting-edge GaN solutions to customers worldwide in a fair and competitive marketplace.



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Tunable SiC Epi System

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MOCVD for AlN Growth

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- 3G 1x6inch 1x4inch 6x2inch
- 4G 1x8inch 3x4inch 14x2inch

• Crystal Quality for AlN

- (XRD FWHM)
- : (002) < 220arcsec
- : (102) < 370arcsec

• Crack-Free AlN

- : Fast Gas Switchable Reactor

• Application

- AlN, AlGaIn Growth
- (Far)UV, UVB, UVA LED: 220~350nm
- Power Device (AlN, High Al-Content AlGaIn, RF GaN)
- Photodetector (AlGaIn-based)



HESTIA

Aixtron announces Malaysian facility

Company's wide-bandgap technologies to power Malaysia's next semiconductor chapter

DEPOSITION equipment company Aixtron has announced that it is building a state-of-the-art facility in Penang, Malaysia, with both manufacturing and engineering capabilities.

The investment establishes two key enabling technology areas for AI infrastructure in Malaysia.

First, Aixtron says, its wide-bandgap semiconductor technologies, which include include GaN, InP and SiC, help address the 'AI Power Wall' by enabling more efficient power conversion for data centres, energy infrastructure and electric vehicles.

Second, Aixtron's products offer solutions for the 'AI Data Wall' by enabling high-performance optical interconnects with high bandwidth, fast data transmission and reduced energy demand.

Together, these technologies address two of the central challenges facing the continued growth of AI: the need for more energy-efficient computing infrastructure and the need to move



ever-larger volumes of data at high speed.

On July 22, 2026, Datuk Sikh Shamsul Ibrahim Sikh Abdul Majid, CEO of the Malaysian Investment Development Authority (MIDA), visited Aixtron in Herzogenrath, Germany, to gain first-hand insight into the manufacturing and development of Aixtron products.

He said: "Aixtron's investment in Penang is fully aligned with Malaysia's national strategy to strengthen its position in the global semiconductor industry. The presence of a front-end equipment manufacturer of Aixtron's caliber will directly support Malaysia's National Semiconductor Strategy, its

high-value and digital economy agenda, and its national target of developing 60,000 high-skilled semiconductor professionals by 2030. Aixtron will contribute to this goal by recruiting locally and developing the skills of its new Penang workforce, and its products will play a pivotal role in improving energy sustainability and transforming the country toward a greener future."

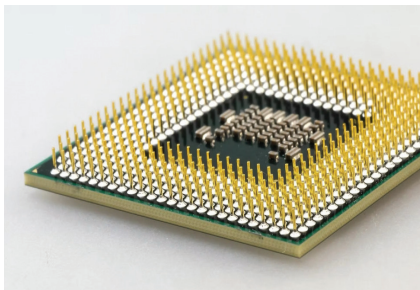
Felix Grawert, (pictured) CEO of Aixtron, added: "Malaysia is becoming an important location for advanced semiconductor technology, and Aixtron is proud to contribute to this development. With our new site in Penang, we are bringing front-end equipment manufacturing, engineering capabilities and our new customer service support centre closer to one of the world's most dynamic semiconductor ecosystems. Our technologies are at the heart of the transition to third-generation semiconductors and help overcome both the 'AI Power Wall' and the 'AI Data Wall' – two key challenges for the next phase of AI growth."

Gallium oxide startup NextGO Epi raises €2 million

NEXTGO Epi, a Berlin-based startup developing Ga₂O₃ epitaxial wafers for next-generation power semiconductor devices, has secured a €2 million pre-seed funding round.

The round, its first institutional backing, was led by Vireo Ventures, with participation from Ultratech Capital Partners, IBB Ventures, and angel investor Boris Habets.

Founded in 2025 by Ta-Shun Chou, Andreas Popp, and Andreas Fiedler, the company is a spin-off from the Leibniz-Institut für Kristallzüchtung (IKZ) and claims to be the only European company producing Ga₂O₃ epitaxial wafers at



industrial quality up to 4 inches.

Ga₂O₃ offers a significant efficiency boost compared to the widely used SiC. The German startup notes that it is 10 times more power-efficient, handles up to 6 times higher voltage density, and

can be produced for up to 75 percent less cost.

The company is already in production, generating revenue, and serving customers across three continents.

The most immediate application is EV fast charging. NextGO Epi says its product can fully charge a vehicle in just 10 minutes, compared to the usual 60 minutes, according to the company.

NextGO Epi plans to use this fresh capital to accelerate product development, grow the team, and strengthen the company's commercial presence across Europe and beyond.

Kubos raises \$2.1 million to advance cubic GaN microLEDs for optical interconnects

Kubos will use the funding to accelerate development of cubic GaN microLEDs for high-speed optical interconnects targeting AI and data centre applications

KUBOS SEMICONDUCTORS has secured more than \$2.1 million in new funding to accelerate development of its patented cubic GaN technology for next-generation microLEDs aimed at high-speed optical interconnects.

The investment includes a Growth Catalyst grant from Innovate UK, matched by funding from the Development Bank of Wales, the Low Carbon Innovation Fund 3 (LCIF3), S4C Digital Media and existing shareholders.

The latest round brings Kubos' total funding to more than \$8 million. The funded project will investigate the



use of cubic GaN microLEDs capable of gigahertz switching speeds while operating at low power, supporting optical communications for AI and data centre infrastructure. The company plans to enter the microLED market

within three years through an IP licensing model.

Susan Gormley, CEO of Kubos, said the project complements the company's wider programme to develop high-efficiency microLEDs across the visible spectrum while strengthening its commercialisation roadmap for AI infrastructure, next-generation displays and solid-state lighting.

Based in Cardiff and Cambridge, Kubos is developing cubic GaN materials to improve the performance and manufacturability of microLED devices for emerging photonics applications.

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A revitalising reboot

IQE has got its mojo back, thanks to substantial investment from Macom, which has signed two long-term supply deals

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THOSE running companies within our industry often focus on commercialising trailblazing tech and ramping volumes. But they are not the only matters keeping them awake at night. Leaders must also concern themselves with their balance sheets. If they have debt, how do they plan to pay it off?

For a number of years, debt-related concerns have hung over the world's leading supplier of epiwafers, IQE. But not anymore – this April it secured investment totalling £81 million (\$107 million), in a deal involving Macom that IQE's CEO Jutta Meier describes as 'transformational'.

The lion's share of this investment comes directly from Macom. There £30 million in cash, which Meier describes as a 'true equity investment', and another £15 million in the form of a convertible loan note.

Commenting on these contributions, Meier remarks: "The investment needed to really make the debt structure was roughly £30 million." The additional £15 million provides headroom for investment and an increase in capital expenditure.

During the financial restructuring of IQE, there were negotiations with existing convertible loan holders, who are reinvesting in the company. This secured around £23 million. And there's a fourth element to the £81 million figure: the raising of a further £13 million from existing shareholders, a move supported by Macom.

According to Meier, IQE is now in a very strong position to weather any



➤ In September 2017, IQE announced the creation of a new state-of-the-art mega foundry in Newport, Wales. Since taking on the lease of the 30,000 m² building, IQE has completed the first phase of construction of cleanrooms and services.

upcoming storms, while supporting growth.

Discussions between the two companies began over the supply of epiwafers. "[Macom] were obviously extremely happy with our technology, and they wanted assurance that we are going to be able to supply that technology for the longer future," says Meier. Macom and IQE have now established two long-term supply agreements.

Strengthening ties between the two companies is the introduction of two Macom executives on IQE's board.

"That means that we are going to benefit from their experience in

manufacturing," says Meier, who is keen to stress that this investor will not be calling the shots. "We're not a Macom house. It's really more advice sharing."

Happy days

IQE's re-financing has reinvigorated the company, and its interactions with its customer base. "What we're really seeing right now is a pure excitement to work with IQE," enthuses Meier.

That's not been the case in the recent past, when the company had to devise a plan for addressing its rolling credit facility with its bank, HSBC. Debt stood at \$30 million, day-to-day operations could not reduce this figure, and a renewal date of September 2026 loomed over IQE.

When internal discussions on a solution began in summer 2024, an IPO for the Taiwan site emerged as the front runner. This facility focuses on the manufacture of GaAs-based epiwafers for the wireless sector. “It’s really quite separate from our growth opportunities,” argues Meier.

By the end of 2024, IQE discarded that option, due to a weakening wireless market and difficulties associated with an IPO. “You have to be listed on the emerging market for six months before you can actually complete an IPO there,” explains Meier.

IQE then considered the sale of its the Taiwan facility. This could clear debts and potentially support growth of the remaining business. But would this be the best way forward? To answer this question, IQE launched a strategic review, considering its options as it conversed with investors, customers, and other players in the eco-system.

These deliberations considered whether IQE could have a role to play in a vertically integrated company, through a sale of part or even all of its business.

“It was always difficult to pinpoint which technologies could be vertically integrated, versus what would just be left stranded,” explains Meier, who says that there are other matters demanding consideration: the integrity of both the portfolio and the company, and its geographical footprint. “Breaking it out and then integrating it into other components wouldn’t quite yield the same value as keeping the company intact.”

During internal discussions, Meier and colleagues concluded that the best role for IQE is to be core supplier to vertically integrated companies, supporting them with product and technical expertise. And while they did consider selling IQE, they failed to find an interested party that valued the company in the right way.

IQE’s management also considered the ideal make-up of its order books. “You can run very low batch volume, however, you need to have a premium pricing associated with that. I think that’s something that we haven’t been doing enough in the past,” remarks Meier. According to her, high-volume orders are also crucial. “We’re

optimising our portfolio to have enough of a scale to drive profitability, but not lose that bespoke quality of the offering.”

When striking deals, IQE has not always been in a strong position. “Given our financial situation in the past, we were always on the back foot of negotiations,” admits Meier. But that’s changing, with IQE planning to sign long-term supply agreements that will improve visibility surrounding future demand.

During the strategic review, uncertainty over IQE’s future paralysed the company. Customers expected to strike a good deal with IQE, but it made little sense for them to build or strengthen their relationships with this supplier of epiwafers, given its vulnerability.

IQE’s results for 2025 reflects this state-of-affairs, with annual sales just £97 million. This relatively low revenue results from uncertainty holding back IQE’s business and extenuating circumstances. In the wireless sector, customers built up inventory in 2024, then drew on that in the following year; and product orders from the US suffered very lengthy delays, due to a change of administration and a slow release of military and defence budgets.

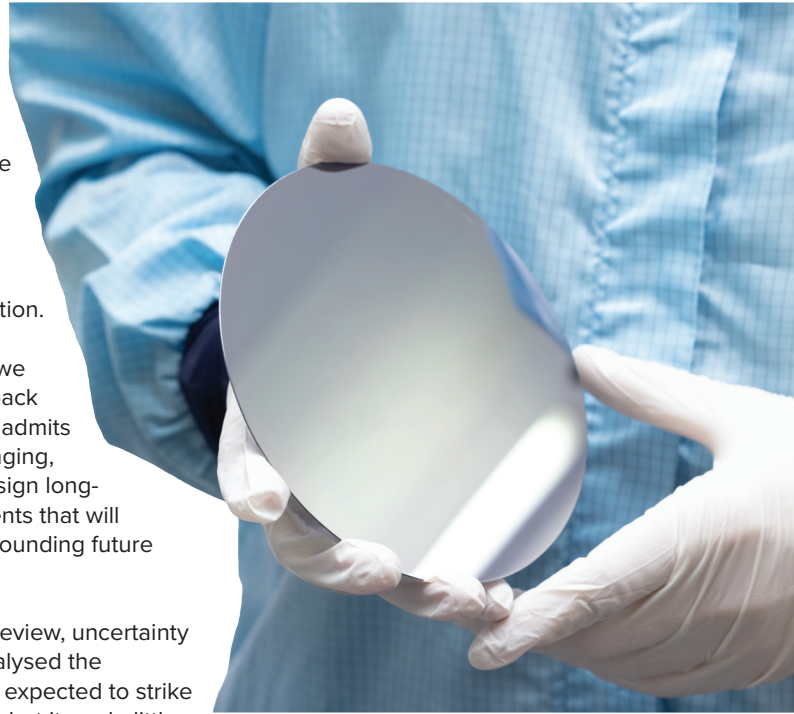
Poor sales and uncertainty weighed heavily on IQE’s share price, which headed south through 2025, finishing the year at around 5p.

For this year, sales are forecast to be up year-over-year by 20 percent. And further ahead, even better figures should be delivered, supported in part by a multi-year InP epiwafer supply agreement signed this June with Tower Semiconductor. Note that this deal will not impact revenue immediately, due to qualification.

Learning from history

Meier is keen to avoid repeating errors made by IQE.

“Additional capacity increases will have to be coupled with very concrete



customer commitments and customer co-funding. We will not just build capacity and hope that we will receive customer commitments.”

IQE fell into this particular trap during the VCSEL boom, which initially generated massive orders for the epiwafer supplier. “Once the devices shrunk and the yield increased, the demand of the wafers really subsided.”

While IQE will continue to respond to surges in market demand, the focus is for a balanced portfolio. Although devices based on InP and GaN are currently attracting a great deal of interest, due to the rapid buildout of AI infrastructure, IQE will not neglect business activities associated with GaSb and GaAs epiwafers, used in infrared sensing and wireless markets, respectively.

Adopting this approach should help ensure a steady growth in sales. But will this lead to profitability, which has alluded IQE for many years?

“People ask me that all the time,” admits Meier, who points out that it’s possible to define profitability in multiple ways. “I’m not going to commit to a time when we are going to be cash accretive, but ultimately, I think that that is truly the goal. And looking at the growth rates right now, that goal will be achieved sooner than later.”

GaN: No knockouts in the patents war

While four years of fighting over intellectual property has driven changes in device design, it's failed to force any settlements or cross-licensing agreement

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

FOR MOST OF US, when we read a company's press release related to a ruling of a patent dispute, we'll conclude that this firm emerged largely victorious. But if we had instead read the release of their adversary, we'd think that the outcome had ruled in their favour.

While both conclusions can't be right, it's incredibly difficult to uncover the truth. What's needed is the view of an unbiased expert in patent law with expertise in the critical technologies.

Offering this in the ongoing GaN IP war is David Radulescu, head of the patent litigation boutique firm Radulescu LLP. He discussed details of patents wars between EPC, Innoscience and Infineon in a July 29 webinar. Alongside his commentary, industry expert Ralf Higgelke provided yet more welcome insight, discussing the implications of various rulings on purchasers of GaN power electronics.

One key point made by Radulescu is that after just over four years of fighting,

there's still no licensing. "It does tell you that the asserted patents and the cases that have been filed have not created enough pressure."

While no side has had a breakthrough, there have been skirmishes on many fronts (see Figure for an overview). They include cases filed in the US International Trade Commission (ITC) for import bans, costing around \$8-12 million per side, with an outcome taking typically 16 months or so. Invalidation petitions have also been filed in the US Patent and Trademark Appeal Board, an action costing less than \$1 million per patent, and involving an 18-month validity review. Infineon has also used German courts, where it's possible to obtain a preliminary injunction within a few days. "You can get a full sales injunction in 9 to 12 months, and you're also paying a bond to cover if you're wrong," explains Radulescu. In addition, there are courts in China that may rule in favour of a nationwide injunction for 12 months, as well providing fast-track patents.

To fight an effective war, companies

must carefully optimise all these options.

ITC rulings

The GaN patents war began in summer 2023, when EPC announced it had taken legal action against Innoscience for infringing four of its patents; and in March 2024, Infineon joined in, also taking to court claims of infringement of four patents.

"Within months, half the patents were dropped," said Radulescu. "It's probably because the claims of infringement were just too weak."

The two remaining EPC's patents were: the '508 patent, which describes a multi-step process that uses three different photoresist patterns to produce a self-aligned gate; and the '294 patent, entitled 'Compensated Gate MISFET'.

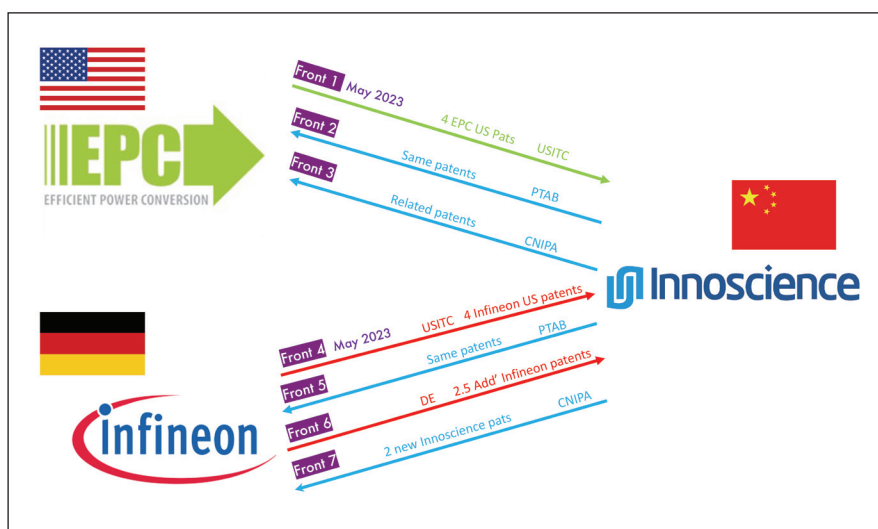
For Infineon, it's remaining duo were: the '481 patent, involving a Kelvin source, added so that parasitic elements associated with the packaging and connections have a reduced impact on overall system performance; and the '755 patent, detailing a non-coplanar drain finger.

The ITC determined infringement on two of these four: EPC's '294 patent and Infineon's '481 patent.

Differing views

Although the ITC found violation on two claims concerning the '294 patent, Innoscience convinced the US Patent Office that the relevant claims are invalid.

In patent cases, either filed in district court, the Patent Office, or the ITC, parties appeal to the US Court of



“The counterattack in China is faster than what happens in the US, It flips the table, because of the tremendous pressure that you can get with these injunctions. The goal, from a patent litigation perspective, is leverage. You want to force a return to the negotiating table”

Appeals for the Federal Circuit, a specialised appeals court. When the Patent Office is involved, the appeals court tends to side with them quite often, according to Radulescu. The appeals argument will be heard in October 2026 at the earliest, and a decision typically issues several months later, depending on the issues presented.

However, to cater for an unfavourable outcome from its perspective, Innoscience has launched new families of products that distance themselves from the technology described in the '294 patent. Now, after epitaxy, there's an anneal to drive out hydrogen and ensure conductivity just comes from the magnesium dopant. The latest approach, which is widely employed for manufacturing LEDs, is reflected in new model numbers, featuring an added suffix AD.

According to Higgelke, the introduction of this new process will have required a lot of investment. As well as optimising material properties and manufacturing processes, Innoscience will have had to generate reliability data from scratch.

Another downside, argues Radulescu, is the additional time for the epiwafers in the MOCVD chamber. "It's requiring Innoscience to add 15 minutes to its epitaxy process, to theoretically out the hydrogen, which I believe was driven out elsewhere, and probably not a lot to start with."

The third leg

When ruling on the Infineon's '481 patent, related to the Kelvin source, the administrative law judge concluded that just two claims were infringed and not invalid. One, claim 4, describes planar contact surfaces and leads exposed on the bottom; and the other, claim 17,

details a voltage of at least 400 V, and a frequency of at least 100 kHz.

Due to this ruling, Innoscience was hit by a cease-and-desist order, and had to pay 100 percent bond for importation.

Innoscience responded to Infineon's action by redesigning its packages. "If you remove that pin, you're out from under the '481 patent," said Radulescu.

However, the redesign degrades performance, according to Higgelke, who explained that the Kelvin source pin is a performance feature. Without it, the device suffers from slower switching, additional losses and instability. In short, the advantages of using GaN are negated.

So, the pin is an important technology that will apply pressure to Innoscience, and may lead to a settlement or cross-license.

A counterattack

Innoscience has pushed back against its adversaries, partly by taking action in its own backyard, where it has won injunctions against Infineon from the Chinese courts.

"The counterattack in China is faster than what happens in the US," remarked Radulescu. "It flips the table, because of the tremendous pressure that you can get with these injunctions. The goal, from a patent litigation perspective, is leverage. You want to force a return to the negotiating table."

The Chinese chipmaker filed two patents with the Chinese patent office. One concerns the passivation layer on the gate, and is directed at the ratio of sidewall thickness to the thickness in the drift region; and the other concerns a field plate with rounded corners.

Actions in Germany

To strengthen Infineon's IP, it has a counterpart of the '481 patent filed in Germany – the '947 patent, which is related to a Kelvin-source sense lead.

There are also three related patents: '691, involving a third lead that provides source sense functionality; the '465, covering interleaved elongated source-drain pad metallisation over the non-active regions of a lateral GaN transistor; and the '054, concerning a GaN die with a deliberate vertical leakage structure.

"They had 4 first-instance wins in Munich Regional Court," remarked Radulescu, who added that Innoscience is saying all these ruling only apply to discontinued legacy packaged parts.

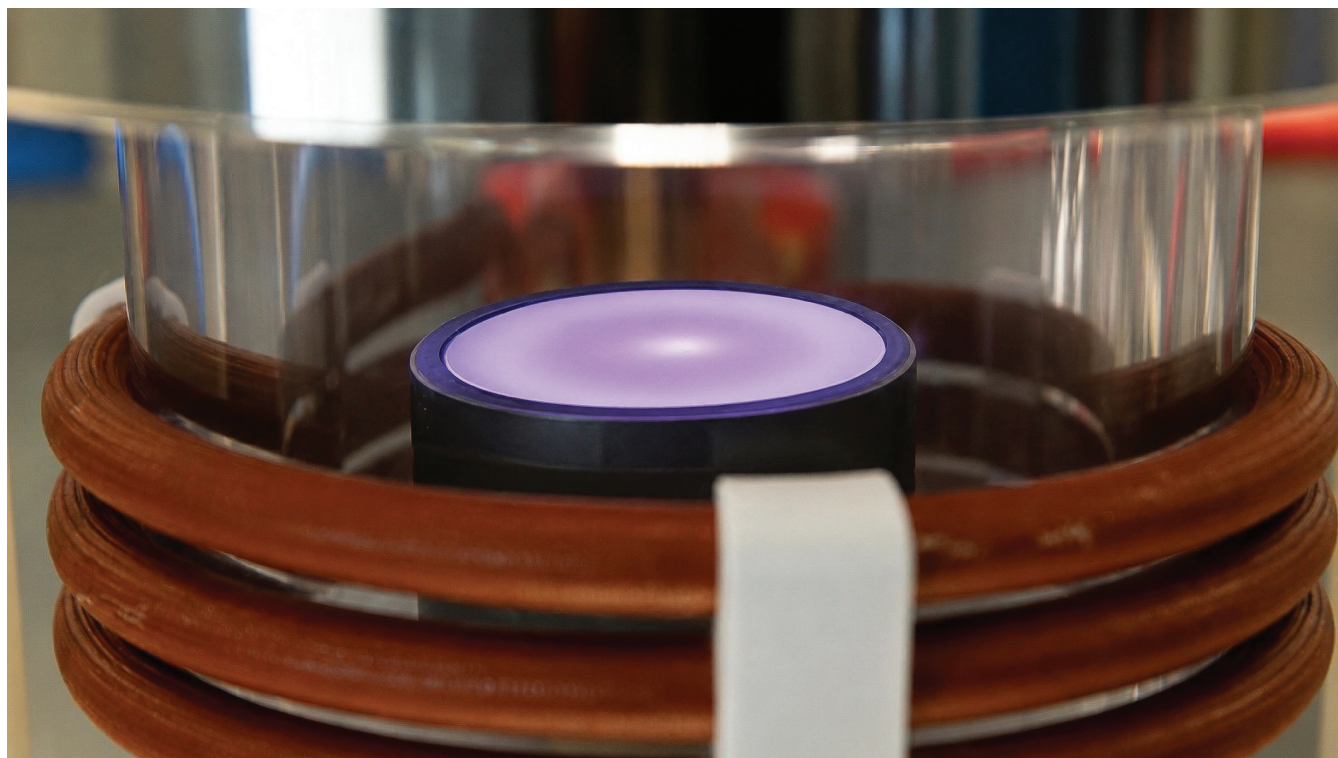
State of play?

Based on the various actions of EPC, Infineon and Innoscience, are there any winners?

According to Radulescu, little pressure has been created during the EPC-Innoscience battle. "It looks like the appeals are just going to run their course, and I assume the campaign's just going to fizzle out."

That's unlikely to happen in the battle between Infineon and Innoscience, which Radulescu views as currently a draw. "Innoscience and Infineon are in a position with a balanced pressure, to possibly enter into some type of cross-license."

As this may take some time, don't be surprised to first see more propaganda-ridden press releases, claiming final victories for the companies involved.



Efficacious excitation aids *n*-type AlN

Illuminating the MOCVD chamber with a source that emits deep within the UV boosts the mobility of silicon-doped AlN and its free-electron concentration

**BY FIKADU ALEMA, WILLIAM BRAND, VITALI SOUKHOVEEV, AARON FINE
AND ANDREI OSINSKY FROM AGNITRON TECHNOLOGY**

WITHIN THE FAMILY of ultra-wide-bandgap semiconductors, AlN has much appeal. Its strengths include a bandgap of around 6.2 eV, a critical breakdown field that exceeds 15 MV cm^{-1} , and a thermal conductivity of almost $340 \text{ W m}^{-1} \text{ K}^{-1}$. What's more, native substrates are commercially available, giving AlN a route to low-defect-density epitaxy that's not available for every emerging wide-bandgap material. Thanks to all these attributes, AlN is an incredibly attractive candidate for next-generation power electronics and deep-ultraviolet optoelectronics.

However, there's a critical issue: realising conductive, *n*-type AlN layers with sufficient free-electron concentrations and adequate mobility. Simply injecting more silicon, the most common donor in III-nitrides, is not a solution. While high levels of silicon are effective in GaN and gallium-rich AlGaIn, where this impurity behaves as a shallow donor, in AlN silicon activation is far less efficient. Adding this donor creates a number of imperfections, including silicon-related

DX centres, aluminium vacancies, vacancy-silicon complexes and background impurities – all can trap or compensate electrons. While increases in silicon doping initially produce a rise in free-electron concentration, mobility often collapses, with compensation eventually limiting further improvement [1-3].

Recently, our team at Agnitron has refined the MOCVD process to attack this problem from two directions. One is chemical potential control – using growth pressure, temperature, V/III ratio and precursor delivery to influence point defect formation during growth. And our second direction is defect quasi-Fermi-level control, realised by using above-bandgap illumination to alter the carrier population and suppress the formation of compensating defects during the epitaxial process [4, 5].

In the pages of this publication we previously reported how these strategies hold much promise for the growth of high-quality silicon-doped AlN and

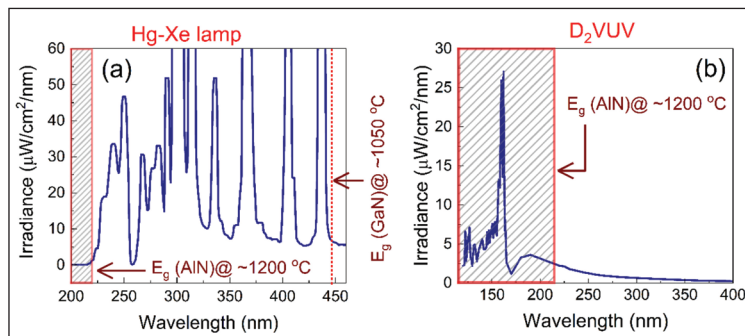
aluminium-rich AlGaIn [6, 7]. Now we are adding another control knob: deuterium vacuum-ultraviolet (D_2 -VUV) illumination during growth of silicon-doped AlN by MOCVD.

Influencing defect formation

During defect quasi-Fermi-level control, we control the incorporation of point defects with UV-assisted epitaxy. This involves using a source of above-bandgap photons to generate carriers near the growth surface that shift quasi-Fermi levels and change the formation energies of charged point defects. Under these conditions, it's possible to reduce the incorporation of compensating defects in AlN, and increase the fraction of silicon donors that contribute free electrons.

Note that this approach is strongly material dependent. UV sources that work well for GaN may fail to provide photons with enough energy for AlN, which has a much larger bandgap and requires much shorter wavelengths. For this reason, spectral matching is critical. For growth of AlN, mercury-xenon lamps, which emit strongly across many UV wavelengths and have been useful in III-nitride growth studies, are not ideal – much of their output is at wavelengths too long to efficiently excite AlN under growth conditions. Far better are D_2 -VUV sources, which provide strong emission near 160 nm and deliver higher-energy photons that interact more effectively with the growing AlN surface (see Figure 1).

Initially, we evaluated UV-assisted growth using a mercury-xenon source. Investigations involved growth on Crystal IS AlN substrates in an Agnitron Agilis 100 MOCVD reactor equipped with a remote-injection showerhead. Trimethylaluminum, ammonia and silane provided the aluminum, nitrogen and

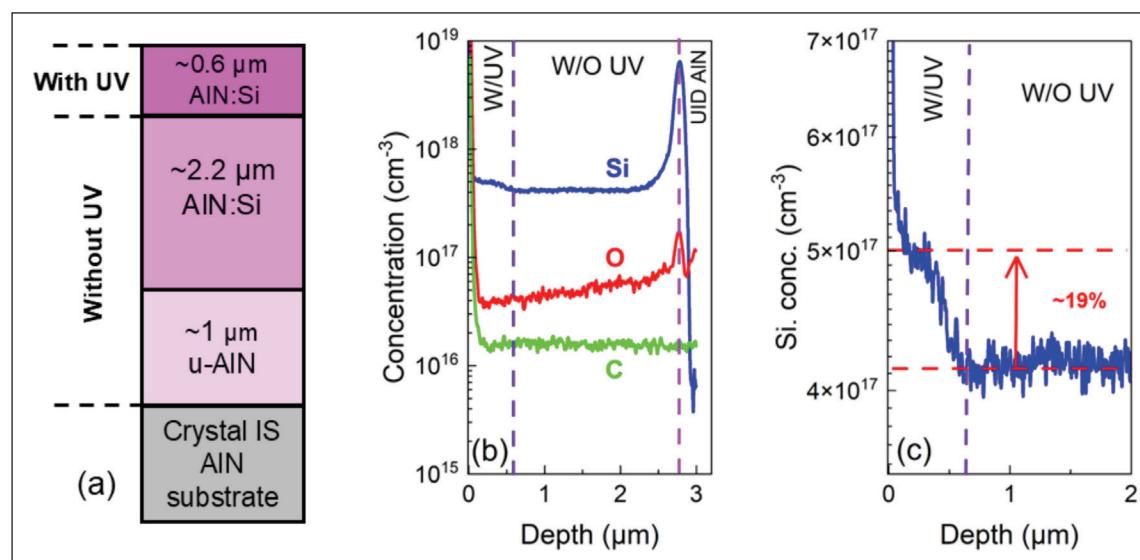


➤ Figure 1. Spectral comparison of the mercury-xenon lamp (a) and the deuterium vacuum-ultraviolet source (b) used for UV-assisted MOCVD. The D_2 -VUV source provides stronger short-wavelength emission near 160 nm, making it a better match for above-bandgap excitation of AlN than the Hg-Xe lamp.

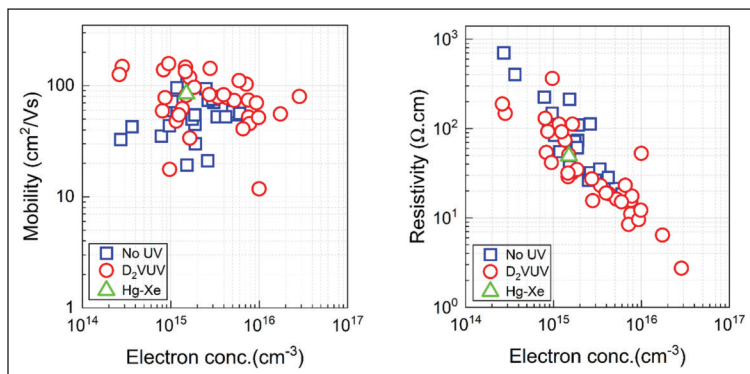
silicon precursors, respectively. To isolate the effect of UV exposure, we grew pairs of silicon-doped AlN layers under identical process conditions. For UV-assisted samples, we only switched the Hg-Xe lamp on during growth of the silicon-doped AlN layer.

Measurements of our samples showed that ultraviolet exposure influences AlN growth. However, benefits are limited with the mercury-xenon source. Using this form of UV illumination, the free-electron concentration increased from about $8 \times 10^{14} \text{ cm}^{-3}$ to $1.5 \times 10^{15} \text{ cm}^{-3}$, electron mobility fell from around $107 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ to roughly $90 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and bulk resistivity fell from about $73 \Omega \text{ cm}$ to around $49 \Omega \text{ cm}$.

Secondary-ion mass spectrometry (SIMS) offered valuable insight into these changes. Under Hg-Xe exposure, silicon incorporation increased from approximately $6.5 \times 10^{17} \text{ cm}^{-3}$ to $7.7 \times 10^{17} \text{ cm}^{-3}$.



➤ Figure 2. Secondary-ion mass spectrometry (SIMS) analysis of silicon-doped AlN grown on a Crystal IS AlN substrate with and without D_2 -VUV exposure. (a) SIMS test structure. (b) Depth profiles of silicon, oxygen and carbon. (c) Linear-scale silicon profile showing an approximately 19 percent increase in silicon incorporation under D_2 -VUV exposure.



► Figure 3. Electrical performance of silicon-doped AlN grown on Crystal IS substrates. Electron mobility (left) and bulk resistivity (right) are plotted as functions of Hall-measured free-electron concentration. D₂-VUV-assisted growth extends the free-electron concentration above the non-UV range while preserving useful mobility, and it shifts the films into a lower-resistivity regime. The best sample combines a free-electron concentration of $3 \times 10^{16} \text{ cm}^{-3}$ with a mobility of around $80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, giving resistivity of $2.7 \Omega \text{ cm}$.

— that's a rise of about 19 percent. Meanwhile, carbon and oxygen concentrations remained essentially unchanged. These results suggest that donor activation efficiency increased slightly, from roughly 0.15 percent without UV exposure to about 0.20 percent with Hg-Xe exposure. We concluded from these findings that Hg-Xe illumination measurably affects silicon-doped AlN growth, primarily by increasing silicon incorporation and carrier concentration, but these are only small gains in donor activation, highlighting insufficient spectral matching between the UV source and the material. Due to this limitation, we integrated a D₂-VUV source into our Agilis 100 MOCVD reactor. With strong emission deep within the UV, this source provides a better spectral match to AlN, and ensures more effective above-bandgap excitation during growth.

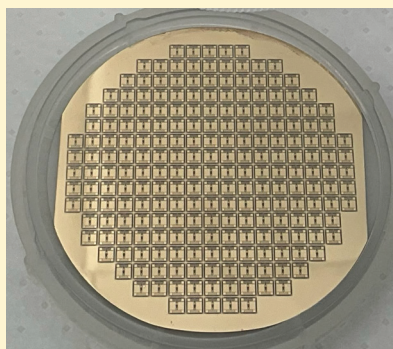
We direct the VUV light at the growing surface via a custom remote-injection showerhead with a central optical-access region. With this design, our

Scaling nitrogen-buffered β -Ga₂O₃ FETs

BUILDING on the nitrogen-doped Ga₂O₃ buffer work reported on a 1-inch (010) β -Ga₂O₃ wafer in this year's issue III of *Compound Semiconductor* magazine [7], Agnitron extended this approach to 2-inch (010) β -Ga₂O₃ wafers as part of its Direct-to-Phase II programme with AFRL. The goal is to determine whether nitrogen-buffered FET structures can provide reproducible wafer-scale suppression of the parasitic silicon-related conduction channel, which often forms at the substrate-epilayer interface.

For lateral β -Ga₂O₃ devices, interfacial silicon accumulation is a major challenge. It threatens to create an unwanted secondary conduction path, increase reverse-bias leakage, and contribute to threshold-voltage variability in MOSFETs. While pre-growth HF etching can reduce this silicon peak, it introduces processing complexity, and may not fully remove the interfacial contribution. Nitrogen compensation is an attractive alternative, offering a more direct epitaxial approach that places a nitrogen-doped buffer between the substrate interface and active device channel.

To assess repeatability, Agnitron grew nitrogen-buffered FET structures on three 2-inch (010) β -Ga₂O₃ wafers and evaluated wafer-to-wafer and run-to-



► Figure 4. Photograph of a fully fabricated 2-inch β -Ga₂O₃ FET wafer grown by Agilis 700 MOCVD on a nitrogen-doped buffer layer using a Synoptics (010) iron-doped β -Ga₂O₃ substrate. The nitrogen-doped buffer suppresses parasitic interfacial silicon conduction while enabling uniform wafer-scale device fabrication.

run consistency (see Figure 4). Two wafers were co-loaded into the Agilis 700 reactor to assess wafer-to-wafer repeatability, and a third grown using the same process to evaluate run-to-run reproducibility. Capacitance-voltage measurements showed consistent profiles across 2-inch wafers. The silicon-doped channel charge was comparable from wafer to wafer, with channel concentrations generally in the range of approximately

1.5×10^{18} to $3.0 \times 10^{18} \text{ cm}^{-3}$. Profiles decreased smoothly with depth, to reach below approximately $1 \times 10^{16} \text{ cm}^{-3}$ in the buffer region, indicating effective compensation by the nitrogen-doped layer and strong suppression of parasitic interface conduction (see Figure 5).

Wafer-scale Hall mapping provided additional confirmation of reproducible electrical properties across the nitrogen-buffer FET structures grown on 2-inch wafers (see Figure 6). Average mobility values were tightly grouped near $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, with mobility non-uniformity ranging from 2.5 percent to 8.1 percent. Average free-carrier concentration ranged from 9.1×10^{17} to $1.3 \times 10^{18} \text{ cm}^{-3}$, close to the target silicon-doped channel concentration of about $1 \times 10^{18} \text{ cm}^{-3}$.

Carrier concentration non-uniformity was higher, ranging from 10.5 percent to 19.5 percent, but the overall doping level remained well controlled across the wafers. Fabricated devices exhibited functional normally-on β -Ga₂O₃ FET behaviour, with drain current at a gate voltage of 0 V ranging from 2.1 mA mm^{-1} to 5.1 mA mm^{-1} and average threshold voltage ranging from -7.4 to -4.4 V .

Although the Hall measurements

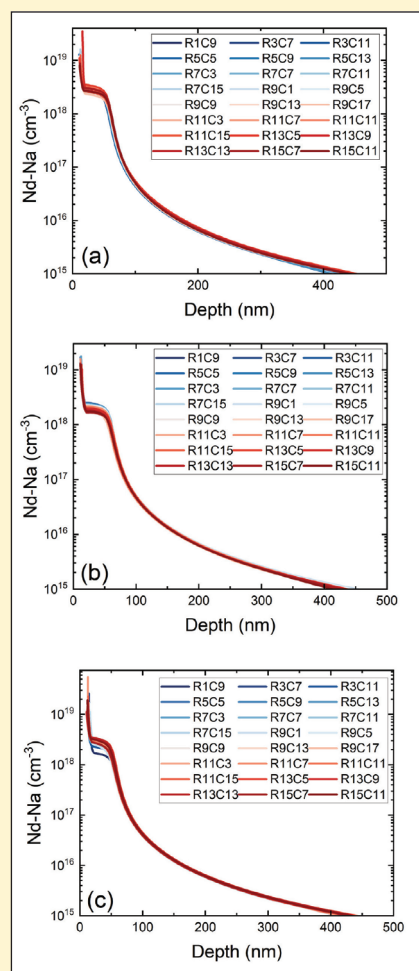
compact D₂-VUV source is mounted directly above the reactor and optically coupled to the growth surface. Ammonia is introduced through the central region, and metalorganic precursors delivered through an annular region surrounding the optical access.

With D₂-VUV exposure, there's a similar increase in silicon incorporation to the Hg-Xe lamp, but a much larger electrical payoff. According to SIMS, silicon concentration increases from about $4.2 \times 10^{17} \text{ cm}^{-3}$ to roughly $5.0 \times 10^{17} \text{ cm}^{-3}$ with D₂-VUV exposure, corresponding to an increase of about 19 percent (see Figure 2). The concentration of carbon remains near the SIMS detection limit, while oxygen decreases through the film, and does not show dependence on the UV exposure.

Another important observation is that the illumination of the surface with UV reduces the growth rate. Our view is that the increase in silicon concentration under UV exposure may be partly

linked to growth-rate-mediated surface kinetics: a slower AlN deposition increases the effective residence time of silicon-containing species at the growth surface, enhancing their probability of incorporation.

When conducting additional growth-rate experiments on AlN/sapphire templates, we uncovered a striking trend. Without UV, the growth rate increases with V/III ratio in the custom showerhead. But with D₂-VUV exposure, this relationship reverses, with growth rate decreasing as V/III ratio increases. This shows that VUV illumination should not be thought of as the addition of passive light to an otherwise unchanged MOCVD process – rather, D₂-VUV illumination is part of the growth chemistry, probably altering ammonia photodissociation, gas-phase precursor reactions, surface reaction pathways, or some combination of these effects. While the detailed mechanism requires further study, it's clear that VUV illumination changes how AlN grows.

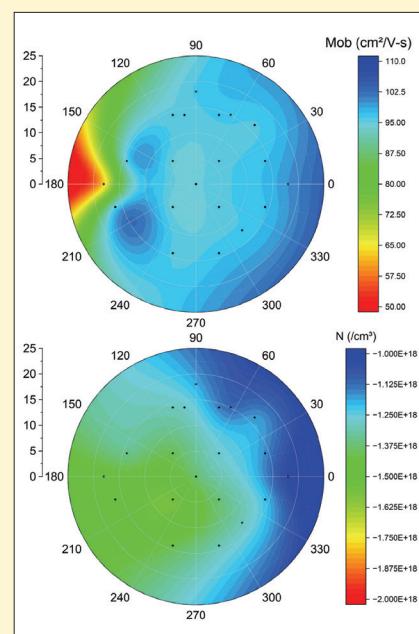


➤ Figure 5. N_d-N_a profiles for three 2-inch nitrogen-buffered $\beta\text{-Ga}_2\text{O}_3$ FET wafers. Panels (a) and (b) show co-loaded wafers to assess wafer-to-wafer repeatability, while (c) shows a repeat growth for run-to-run reproducibility. The closely overlapping profiles show reproducible silicon-doped channel charge and a smooth decrease of N_d-N_a into the nitrogen-doped buffer, indicating effective suppression of parasitic interface conduction.

from the channel properties alone. This discrepancy indicates that the device current is not primarily limited by the nitrogen-buffer FET structure. Instead, it's strongly influenced by source/drain access resistance and contact resistance. Probably a significant contribution to this limitation is the absence of an ohmic contact regrowth layer, as this increases the effective series resistance at the contacts. As a result, the measured drain current should be considered a lower-bound result, with substantial improvement expected from optimised regrown ohmic contact regions.

Overall, the 2-inch results demonstrate that nitrogen-buffered $\beta\text{-Ga}_2\text{O}_3$ FET structures can be grown reproducibly at wafer scale while effectively suppressing parasitic interface conduction. The successful fabrication

indicate that the epitaxial channel has suitable mobility and carrier concentration near the target doping level, the measured drain current is a concern – it's lower than expected



➤ Figure 6. Representative wafer-scale maps of mobility (top) and channel electron concentration (bottom) for a 2-inch $\beta\text{-Ga}_2\text{O}_3$ FET sample grown on a nitrogen-doped buffer layer.

of normally-on devices across the wafers provides a strong foundation for further optimisation. Future work will focus on source/drain contact engineering, including regrown ohmic contact regions, which should reduce series resistance and increase drain current, uniformity and overall device performance.

Breaking trade-offs

With D₂-VUV-assisted growth, the overwhelming advantage is the superior trade-off between mobility and carrier concentration in silicon-doped AlN. Using this technology, AlN now has a high enough carrier concentration to reduce resistance, while retaining sufficient mobility to avoid the severe transport penalty normally associated with heavy compensation.

Measurements reveal that with the introduction of D₂-VUV exposure, electron mobilities increase from 20-110 cm² V⁻¹ s⁻¹ to 100-160 cm² V⁻¹ s⁻¹, and free-electron concentration climbs from 6 × 10¹⁵ cm⁻³ to 1 × 10¹⁶ cm⁻³ (see Figure 3, left). One of our best results – highlighting our breakthrough – is a free-electron concentration of about 3 × 10¹⁶ cm⁻³, combined with an electron mobility of about 80 cm² V⁻¹ s⁻¹.

Another important characteristic is resistivity. Several of our D₂-VUV-grown AlN samples have values below 10 Ω cm, with the best film reaching a bulk resistivity of about 2.7 Ω cm (see Figure 3, right). This value, which is lower than previously reported bulk resistivities for MOCVD-grown silicon-doped AlN, showcases the significant improvement in the conductivity of AlN grown by MOCVD [2].

Record activation efficiencies

To estimate the donor activation efficiency of our most conductive D₂-VUV-grown film, we have compared the Hall-measured free-electron concentration with the SIMS-measured silicon concentration. For the sample with a free-electron concentration of approximately 3 × 10¹⁶ cm⁻³, the silicon concentration is about 1.3 × 10¹⁷ cm⁻³, implying

a donor activation efficiency of roughly 22 percent. That's a very impressive figure – it's more than 100 times higher than the value estimated for the Hg-Xe-exposed film, and nearly two orders of magnitude higher than typical values reported for MOCVD-grown silicon-doped AlN.

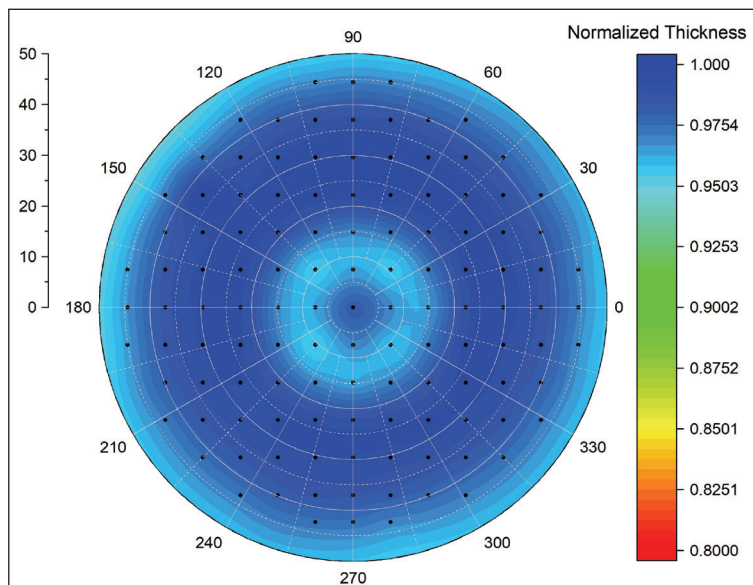
A careful look at our SIMS results uncovers an important clue concerning the mechanism associated with D₂-VUV exposure. As there's no reduction in carbon or oxygen incorporation, it's unlikely that the dramatic improvement in conductivity results from lower impurity levels. Instead, the results point to improved donor activation and reduced compensation by point defects during growth. Since VUV exposure changes the growth-rate behaviour, we have deduced that the most likely cause of overall improvement is a combination of modified growth chemistry and defect quasi-Fermi-level control.

We have also investigated whether D₂-VUV-assisted MOCVD aids the growth of high-aluminium-content AlGa_{0.87}N_{0.13}. Using D₂-VUV exposure, we produced Al_{0.87}Ga_{0.13}N that is conductive, and has Hall-measured electron concentrations reaching 3.1 × 10¹⁹ cm⁻³. Specific contact resistivity reaches up to 7.5 × 10⁻⁵ Ω cm², compared with 1.7 × 10⁻⁴ Ω cm² for a comparable layer grown without D₂-VUV exposure. That corresponds to a reduction in specific contact resistivity of approximately 57 percent. Based on these results, the benefits of D₂-VUV illumination are not limited to binary AlN – they support improved conductivity and contact behaviour in high-aluminium-content AlGa_{0.87}N.

Deep UV exposure capability

Playing a key role in the success of our recent UV-assisted AlN work is the Agilis 100, our most widely adopted OEM R&D MOCVD platform. This flexible reactor is a highly configurable research tool, supporting both remote-injection showerhead and close-injection showerhead operation – this allows researchers to select the reactor geometry best suited to their material system and growth objectives. Thanks to this flexibility, our platform is particularly useful for wide-bandgap and ultra-wide-bandgap materials research, where growth chemistry, precursor delivery, thermal environment, and *in-situ* process control often need to be adapted as science evolves.

For the UV-assisted AlN results presented in this article, we employed a newly engineered showerhead/gas distribution flange that integrates a high-power D₂-VUV source directly into the reactor. Rather than relying on an external lamp, viewport coupling, or a long optical light pipe, by adopting this approach VUV exposure is delivered directly to the wafer carrier and growth surface. That's valuable, as it allows the photon flux to interact with the growth environment where it is needed most, while only infringing minimally on gas delivery, to ensure high-quality growth by MOCVD.



► Figure 7. Thickness uniformity map of a Ga₂O₃ film grown on a 4-inch sapphire substrate in the Agilis 700 using Dynamic Sweep Gas Modulation. The sweep-modulated growth achieved approximately 1 percent 1σ thickness non-uniformity.

Another recent breakthrough is our demonstration of a new uniformity-control approach on our larger-format Agilis 700 platform – this is one of our most capable MOCVD systems for developing advanced oxides, including β -Ga₂O₃ and related materials. On platforms supporting larger wafers, it is critical to maintain uniformity across larger substrates.

Our development of integrated D₂-VUV hardware reflects our broader approach to reactor design: using an MOCVD platform as not only a growth tool, but an adaptable experimental environment for testing new process physics. By integrating the UV source into the showerhead region, we have created a practical path for above-bandgap exposure during the growth of ultra-wide-bandgap materials, such as AlN.

Dynamic sweep gas modulation

Another recent breakthrough is our demonstration of a new uniformity-control approach on our larger-format Agilis 700 platform – this is one of our most capable MOCVD systems for developing advanced oxides, including β -Ga₂O₃ and related materials. On platforms supporting larger wafers, it is critical to maintain uniformity across larger substrates. Building on observations made during the development of our horizontal AgniGaN 400 reactor, we have developed Dynamic Sweep Gas Modulation technology. This patent-pending technology (US Patent Application No. 19/715,791) actively tunes the spatial distribution of precursor flux during growth.

To realise this, we modulate selected push-gas or injection-zone flows during a growth step, rather than holding them at fixed values. Modulation may be defined through recipe parameters, such as baseline flow, amplitude, frequency, phase, duty cycle and waveform shape. By selecting fixed high-flow and low-flow conditions, process engineers may bias deposition toward different regions of the wafer or carrier. Using dynamical sweeping of the gas flow during growth, our reactor time-averages these spatial biases to produce a more uniform film. Adopting this approach in our horizontal reactor reduced the 1 σ thickness non-uniformity of AlN grown on 4-inch sapphire from about 2.5 percent to approximately 0.5 percent.

Recent work with our Agilis 700 shows that we can apply the same concept to a vertical reactor configuration. In one of our sets of experiments, we compared two fixed alkyl/metalorganic-zone flow conditions, 1500 sccm and 500 sccm, with a third condition using Dynamic Sweep Gas Modulation. Fixed-flow conditions produced distinct spatial deposition profiles, while the sweep-modulated condition significantly improved uniformity, reaching approximately 1 percent 1 σ non-uniformity on a

4-inch substrate (see Figure 7). These results show that Dynamic Sweep Gas Modulation is not limited to horizontal flow reactors – it can also improve vertical MOCVD platforms where gas distribution, wafer rotation, precursor utilisation and wafer-scale uniformity are tightly coupled. These improvements to uniformity, alongside advances in silicon-doping with sources deep within the UV, strengthen our position as a pioneer of high-quality ultra-wide-bandgap epilayers.

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The quiet war beneath our electronic chips

Export controls and conflicts are placing compound semiconductor manufacturing at risk

BY SC LENNY KOH FROM THE UNIVERSITY OF SHEFFIELD AND
PETER SMOWTON FROM CARDIFF UNIVERSITY, AND BOTH FROM
THE UKRI COMPOUND SEMICONDUCTOR HUB

OUR INDUSTRY underwent a profound change on 3rd July 2023. That day, a routine announcement from China's Ministry of Commerce and General Administration of Customs informed exporters of gallium and germanium – and their compounds – that they would now need to apply for licences before shipping. No advance notice. No transition period. No named targets. And the control measures were imminent, imposed from the 1st of August.

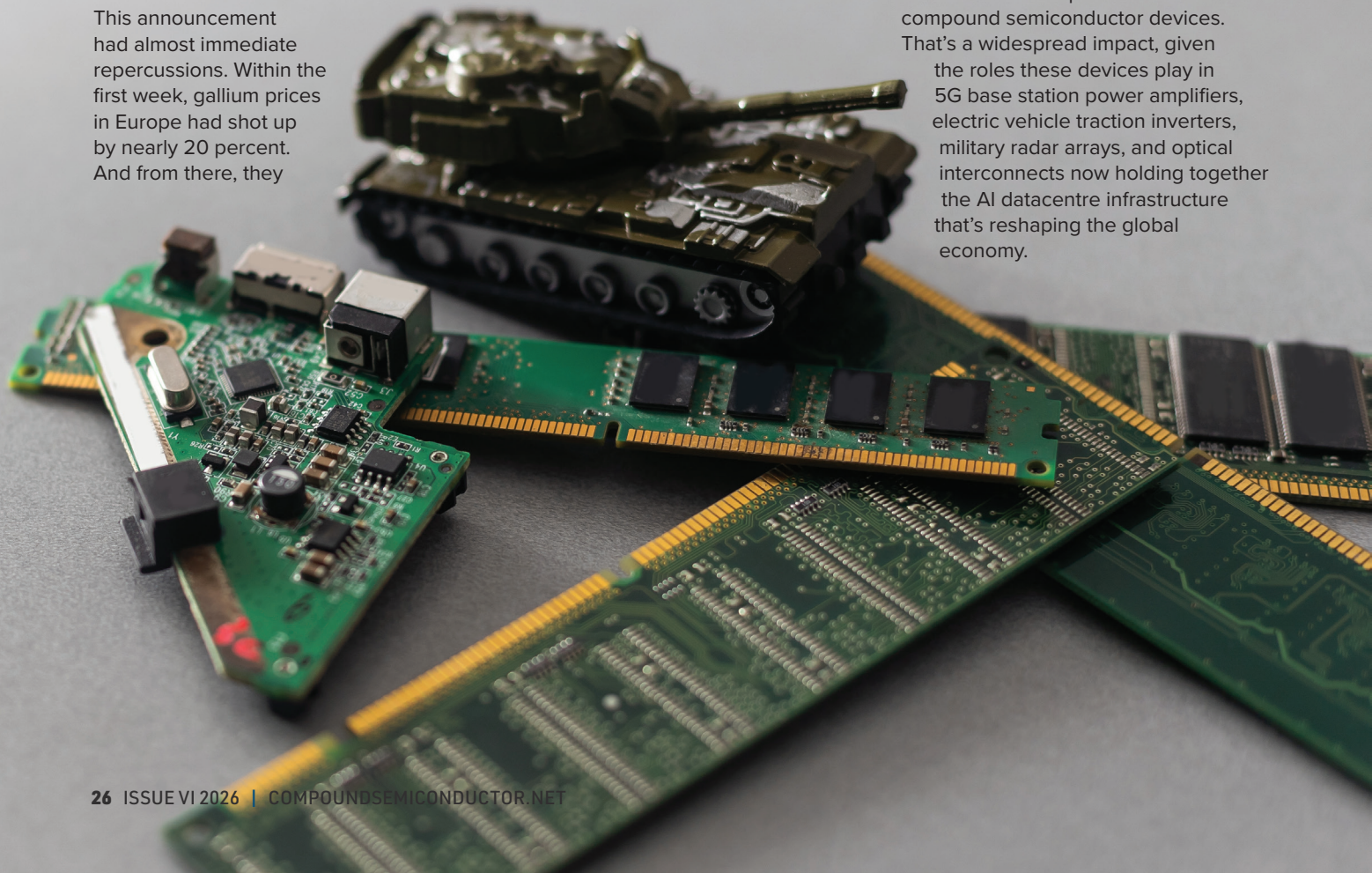
This announcement had almost immediate repercussions. Within the first week, gallium prices in Europe had shot up by nearly 20 percent. And from there, they

continued to climb. By mid-August 2023, the spot price for gallium had spiked by roughly 50 percent from its June baseline; and the trend continued, with Rotterdam gallium prices climbing by nearly 150 percent from the pre-control time to May 2025. Similarly, by the end of 2024, the year-over-year germanium prices had rocketed by nearly 90 percent in Europe.

This is what supply chain weaponisation looks like. It's not an

embargo announced with fanfare, but a licensing regime tightened incrementally – from cautious signal, to export ban, to extraterritorial jurisdiction clause – until the supply chain of an entire technology class is effectively held hostage.

As we are sure you can figure out, these restrictions on germanium, gallium and their compounds – and since 4 February, 2025, you can add indium into that mix – have had substantial implications on all compound semiconductor devices. That's a widespread impact, given the roles these devices play in 5G base station power amplifiers, electric vehicle traction inverters, military radar arrays, and optical interconnects now holding together the AI datacentre infrastructure that's reshaping the global economy.



Compound Semiconductor Supply Chain Resilience Risk Matrix

Materials	Conflicts	Export Controls	Sanctions	Natural Disasters	Energy Crises	Concentration Risk	Average Risk
Gallium	Critical	Critical	High	Low	Medium	Critical	4.0
Germanium	High	Critical	High	Low	Medium	Critical	3.8
Rare-earths	High	Critical	Critical	Low	Low	Critical	3.8
Indium	Medium	High	Medium	Low	Medium	High	3.2
Arsine/ Phosphine	Medium	Medium	High	Medium	Medium	Medium	3.2
Sapphire Substrate	Medium	Medium	Medium	Low	Low	Medium	2.7

Risk Scores: Authors' analysis using CSIS, SEMI, USGS, SIA/BCG data

5 4 3 2 1

A supply chain unlike silicon

Compound semiconductor supply chains are short, steep, and extraordinarily concentrated. While silicon chips are made from one of the most abundant elements on Earth, compound semiconductors are markedly different: they are built from binary and ternary combinations of elements that are scarce, geographically concentrated, and in most cases extracted as byproducts of entirely different industrial processes. Due to scarcity and accessibility, these elements are defined as critical minerals. This underscores their strategic importance.

Production of gallium involves recovery from residues of aluminium smelting. Germanium comes from zinc refining and coal fly ash, and indium is a byproduct of zinc production. In other words, for the three most important metals in our industry, there's no primary mine; so simply mining more is not an option when prices rise. It is also worth noting that China produces approximately 98 percent of the world's low-purity gallium – not because it holds a monopoly on deposits, but because it has built an unmatched refining infrastructure over three decades, largely beneath the radar of Western industrial policy.

From raw material to finished devices, the compound semiconductor

supply chain traverses four layers: raw materials and process gases; substrate and epitaxial growth; device fabrication; and end-use sectors. An illustration of this interconnectedness is trimethylgallium, the organometallic precursor that carries gallium into MOCVD reactors for GaN and GaAs epitaxy. It is synthesised from Chinese-refined gallium metal and supplied through key regions, including the US, China, Europe, Japan, South Korea, and India.

Disruption vectors

The compound semiconductor supply chain faces four threats: export controls, war and geopolitical conflict, energy supply crises, and climate and water risk.

Export controls account for the most acute near-term threat. In December 2024, China prohibited exports of gallium, germanium and antimony to the US, a direct retaliation of US semiconductor export restrictions. For China, critical mineral supply control is a strategic leverage. Following a US-China trade truce in November 2025, these controls have been suspended under a licensing regime until November 2026. However, the ban on military end-uses remains fully in place, with Beijing retaining the complete legal architecture to reimpose restrictions at any point. The controls are paused, not resolved. Meanwhile, the extra-

territorial provisions introduced in December 2024 – extending Chinese legal authority to third-country re-exporters – have not been rescinded. Trans-shipment routes via Germany, Belgium and Japan remain closed in law, even as direct trade partially resumes. The structural dependency ensuring that the ban would be effective has not been reduced. China also bans imports of some Nvidia chips from the US, supporting local production of advanced AI chips, in line to develop a full end-to-end advanced semiconductor supply chain.

War and geopolitical conflict introduce a different risk profile: a faster onset, and a more indiscriminate cascade. The 2022 Russian invasion of Ukraine immediately disrupted neon and krypton supply. Prior to the conflict, Ukraine supplied roughly half of global semiconductor-grade neon – this is one of the critical gases used in high-end lithography tools, and while it is primarily employed in the silicon industry, it is starting to impact compound semiconductor manufacturing.

Another potential disrupter is an energy supply crisis. Restrictions in electricity and gas threaten and directly impact the sustainability of substrate epitaxial growth, wafer production and device fabrication. This occurs, due to the energy intensiveness of these

processes – and our industry must take this fragility seriously.

Climate and water risk is the least visible, but most structurally embedded vector. Recurrent drought conditions in Taiwan have had implications for compound semiconductor fab operations, addressed by emergency water-trucking. Epitaxial growth processes are particularly water-intensive, causing water management to become a strategic variable alongside geopolitical risk.

What can be done?

Given the ramifications of restrictions to the flow of compound semiconductor materials, the obvious question to ask is what to do about it at various levels.

For companies, the priority is to move from reactive procurement to structural resilience. Chipmakers should be dual-qualifying every critical input across at least two geopolitically distinct suppliers (if possible) – a process that takes 12-24 months and must begin before a crisis, not during one. Alongside this move, there must be a redesign of inventory strategy: as a 90-day gallium buffer proved insufficient by late 2023, a 180-day reserve for non-substitutable inputs is now a reasonable baseline.

It's also crucial to invest in renewable substrates, critical material and rare-earth recycling: companies generating gallium-bearing epi polish waste are sitting on a recovery opportunity that reduces cost exposure and geopolitical

Given the ramifications of restrictions to the flow of compound semiconductor materials, the obvious question to ask is what to do about it at various levels

dependency simultaneously, and can directly contribute to the circular economy.

For policy makers and nations, there are four important opportunities to exploit, forming part of modern industrial strategy and national security. One of these four is the strategic on-shoring and scale up gallium, indium and germanium (and antimony) refining capacity. Another prudent move is the mandatory supply chain disclosure of critical mineral and rare earth inputs in semiconductor manufacturing: requiring fabs to report Tier 1 and Tier 2 input geographies, which would transform visibility for both industry and government. A third objective is to derisk, through the substitution of materials and reshoring semiconductor manufacturing to a stable, sustainable eco-system. And last but by no means least, there's a need for design security, resilience and circularity, for the photonics, electronics and semiconductor manufacturing supply chains.

The decade ahead

Due to recent events, the semiconductor industry is undergoing a fundamental transformation from a model that's been optimised for global

efficiency to one that must prioritise resilience and security. The four levers to succeed in this quest are strategic stockpiling, geographic diversification of processing, recycling investment and material substitution R&D. All are underinvested relative to the strategic exposure they address. The US CHIPS Act, the EU Chips Joint Undertaking, the EU/UK/USGS Critical Raw Materials Act, the UK Semiconductor Strategy, and the allied-nation supply agreements represent a real, if belated, beginning.

But the pace must accelerate. So far, our industry's responses to supply chain shocks have been reactive, although long-term resiliency strategies are gaining speed. However, the next shock may provide no warning.

We live in turbulent times, where structural changes in the global world order are fast and frantic. Over the last few years, supply chains have become increasingly uncertain, as an evenly-poised battlefield outcome. The compound semiconductor industry's ability to recognise that fact – and act on it with the urgency the situation dictates – will define the technology security landscape of the 2030s.



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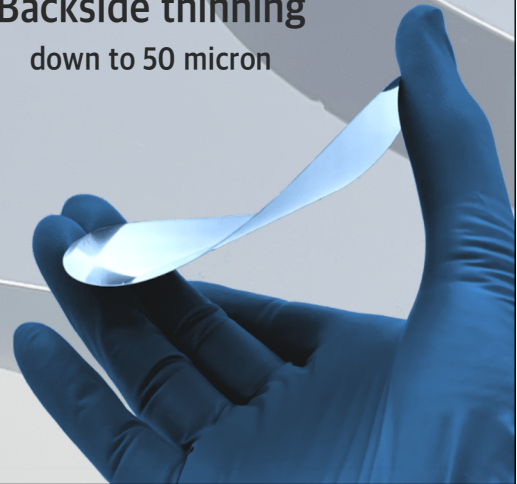
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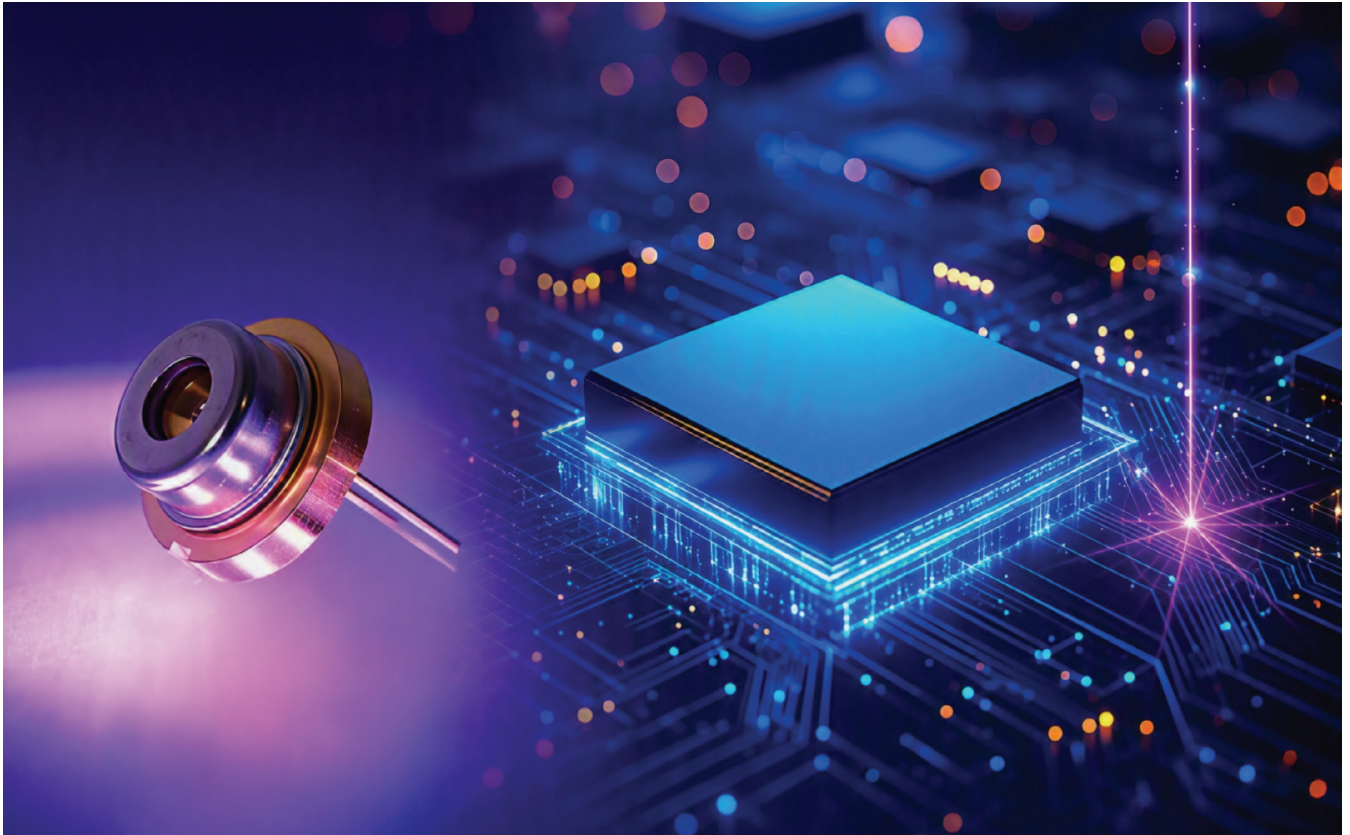


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**BY SHINJI YOSHIDA AND COLLEAGUES FROM
NUVOTON TECHNOLOGY CORPORATION JAPAN**

THROUGHOUT the history of the semiconductor industry, there's been a relentless drive to improve semiconductor performance. As well as reshaping device architectures, this eternal goal refines the way that chips are packaged and manufactured. Within the silicon industry, conventional transistor scaling is approaching fundamental limits. Due to this, innovation is increasingly shifting towards advanced packaging, where processors, memory devices and specialised chips are assembled three-dimensionally and interconnected by extremely fine patterning. This transition is placing an unprecedented demand on manufacturing equipment, and in particular on the lithographic technologies employed to form redistribution layers and high-density interconnects on large-area substrates.

Packaging at the forefront

There are a number of requirements associated with advanced semiconductor packages. They include finer features and resolutions, a higher overlay accuracy between multiple layers, large substrates and high productivity.

Efforts to excel on these fronts are stretching the capabilities of traditional steppers using photomasks. While the photolithography equipment that relies on ultraviolet radiation from mercury lamps and solid photomasks has served the silicon industry well, there are intrinsic challenges when substrate sizes grow and product variants multiply. Mask preparation is now costly and time consuming, as it is increasingly difficult to ensure a high overlay accuracy across large areas, because patterns on solid photomasks are fixed and fail to compensate for distortion and deformation of the substrate.

Due to these constraints, there's renewed attention in laser direct imaging (LDI). This is a maskless exposure technique, with circuit patterns written directly by scanning a focused laser beam. Thanks to elimination of photomasks, LDI enables rapid design changes, excellent resolution and overlay accuracy, and efficient support for high-mix manufacturing. In addition, this solution complies with a global trend for regulating and phasing out mercury-based light sources.

Despite these advantages, today's adoption of LDI for next-generation semiconductor packaging is limited to pilot-line equipment. Holding back full-scale industrial deployment of LDI are concerns over throughput, which is governed by the power of the laser light source. Existing semiconductor lasers emitting in the UV or violet have enabled early deployment of LDI systems, but their output powers are insufficient for high-volume production of advanced semiconductor packages.

The light-source bottleneck

In practical LDI systems, laser diodes must deliver a high continuous-wave output power while maintaining a stable emission wavelength and delivering reliable long-term operation. Simply increasing drive current is not a viable solution, as this increases self-heating, in turn increases the junction temperature of the laser diode, and leads to degradation of laser performance and an acceleration of output power degradation during long-term operation. To overcome this bottleneck, there must be a holistic approach, addressing both the laser diode and the thermal path that removes heat from the active region.

At Nuvoton Technology Corporation Japan we are addressing these issues during our development of a high-power InGaN-based edge-emitting laser diode that emits at 405 nm – that's a wavelength well matched to photoresist sensitivity, and widely used in LDI systems. By jointly optimising the device geometry, epitaxial waveguide structure and package thermal design, we have realised a high-output power and an improved wall-plug efficiency. These strengths have enabled improved long-term reliability through suppression of the junction temperature in violet laser diodes.

Managing heat at its source

A major limitation of the high-power operation of InGaN-based laser diodes is the rise in junction temperature at high current densities. Elevated junction temperatures increase carrier leakage from the quantum well, leading to a higher threshold current and a reduced slope efficiency. In addition, high junction temperatures accelerate device degradation during aging, due to the thermally activated formation of defects, which act as non-radiative recombination centres.

Compounding these matters, the unwanted loss mechanisms are amplified in violet and UV lasers, due to reduced band offsets in the III-N quantum well and increased internal optical loss, making high-power operation particularly sensitive to junction temperature. Consequently, it is imperative to suppress the rise in junction temperature under high-power operation, as this holds the key to high performance and long-term reliability.

One of our key design choices when working towards this objective is our laser chip geometry. We employ a wide stripe and a long cavity. By

expanding stripe width and extending the cavity length, we reduce the optical power density at the facet and the current density in the cavity – and ultimately distribute heat generation over a larger volume. There's a reduction in the thermal resistance of the laser chip, helping to suppress the rise in junction temperature.

For the devices described in this article, stripe widths are up to 45 μm , and cavity lengths up to 1400 μm . In addition to enabling a higher output power, this geometry mitigates degradation mechanisms exacerbated at high optical intensities. As emission heads towards the violet and UV, thermal management is increasingly critical in InGaN-based lasers. Shorter wavelengths are accompanied by higher photon energies, and typically higher operating voltages – both contribute to increased heat generation for a given optical output. At the same time, it is more challenging to ensure carrier confinement in the quantum well, due to reduced band-offsets, making device performance particularly sensitive to junction temperature.

There's a strong interplay between key laser characteristics. As the temperature rises, more carriers spill over from the active region, leading to an increase in threshold current and a rapid deterioration in slope efficiency. In high-power operation, this detrimental feedback loop between temperature and laser performance threatens to dominate device behaviour, and incremental design changes are insufficient for addressing these concerns. This issue is one of the reasons why high-power scaling of violet laser diodes has historically lagged behind that of devices emitting at longer wavelengths.

Our approach to improving the performance of violet lasers involves trimming its current density and thermal resistance through a widening of the stripe and an extension of the cavity length. However, just making these geometrical changes does not guarantee high-power performance. In short-wavelength lasers, internal optical loss plays an outsized role in determining wall-plug efficiency. There's the possibility that free-carrier absorption in heavily doped cladding and guiding layers, as well as scattering losses associated with imperfect optical confinement, offset gains resulting from a reduced current density and a lower thermal resistance of the laser chip.

To address this, we treat waveguide optimisation and thermal design as interdependent challenges. We know that reducing internal loss not only improves efficiency directly – it also cuts dissipated power for a given output, thereby alleviating the thermal load on the package. Meanwhile, if we lower the thermal resistance of the entire device, including the package, we will preserve the optical and electrical benefits of the optimised waveguide under practical operating conditions. Due to this strong coupling

between optical design and thermal management, it is critical for progress at the device level to be matched by advances in packaging.

Optimising the waveguide

Thermal management alone is insufficient to ensure success; a high wall-plug efficiency requires low internal optical loss and strong confinement of carriers and photons. We meet these requirements with a laser structure employing a single quantum-well active region to minimise threshold current, surrounded by carefully engineered guiding layers. The heterostructure features high-refractive-index InGaN waveguide layers to confine the optical mode, and AlGaIn cladding layers to provide carrier confinement and minimise optical leakage.

Our design also addresses free-carrier absorption. Arising from dopants and impurities in the waveguide, this impediment to efficiency is a major source of internal loss in short-wavelength lasers. We mitigate this with a design that minimises the spatial overlap between the optical mode and highly doped regions. It's a strategy that reduces free-carrier absorption without compromising carrier injection. Through optimisation of dopant concentrations and impurity profiles during growth of the heterostructure, produced by MOCVD, internal losses are reduced without compromising electrical performance. Our emitters also incorporate an electron-blocking layer – this helps suppress carrier overflow from the active region, and supports high efficiency, even at elevated drive currents.

Rethinking the package

While device-level optimisation improves intrinsic performance, it is the package that governs how effectively heat is extracted. In industrial laser applications, TO-CAN packages, such as TO9, are widely used. They provide a compact form factor and ease of integration. However, these packages have traditionally suffered from relatively high thermal resistance. Moving to much larger packages could address this issue, but it will complicate system design, so we have focused on trimming thermal resistance within the TO9 footprint.

To accomplish this, we redesigned the package as a monolithic copper structure, replacing conventional iron-based base plates and minimising internal thermal interfaces (see Figure 1). With this redesign, package thermal resistance is roughly two-thirds of that of a conventional iron-based TO-9 package. Behind this reduction is a substantially higher thermal conductivity, realised by replacing iron-based materials with copper.

We have made further gains by mounting the laser chip *p*-side down, as this shortens the heat path from the active region to the submount. Note that the choice of submount material is equally critical. We have evaluated various high-thermal-conductivity materials, and found that a diamond submount provides a substantial reduction in thermal resistance compared with conventional ceramic materials. Our use of a diamond submount, offering a thermal conductivity several times higher than that of typical ceramic materials, delivered an additional reduction in junction-to-case thermal resistance.

Taken together, the redesigned copper package and *p*-side mounting on diamond have doubled the overall heat extraction capability of the laser, and enabled stable high-power operation within a compact TO-9 package.

Power performance and efficiency

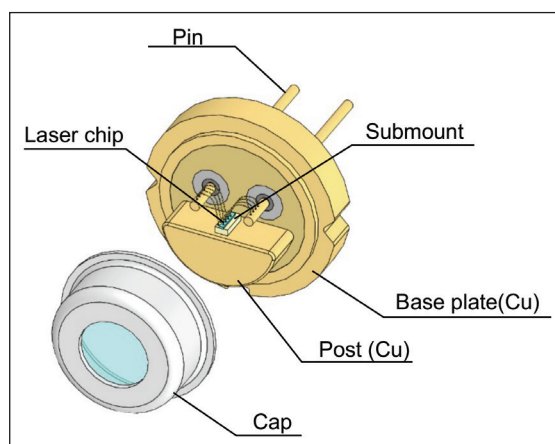
As one would expect, the combined effect of a tailored device geometry, waveguide optimisation, and a low-thermal-resistance package has produced marked improvement in high-power performance. Operating at a case temperature of 25°C, our 405 nm lasers deliver a continuous-wave output exceeding 12 W (see Figure 2). When the output is 5.2 W, wall-plug efficiency is 43.9 percent.

For industrial applications, high efficiency must be maintained at elevated temperatures. We find that even at a case temperature of 50°C, our devices exhibit wall-plug efficiencies above 40 percent, when delivering an output power of more than 5 W. Behind this success is the device's thermal robustness, essential for integration into compact LDI modules, where active cooling capacity is limited and there may be fluctuations in ambient temperature.

In addition to enabling high output powers and thermal robustness, our work highlights the flexibility of our device platform, which can be optimised for various performance priorities.

If we design devices with a reduced stripe width, we can enhance wall-plug efficiency by decreasing the threshold current – but this goes hand-in-hand with a fall in the maximum output power, due to increased current density and a higher thermal resistance. When making this trade-off, the laser geometry must be tailored to specific application requirements. While a high output power is essential for an LDI system seeking maximum throughput, applications

► Figure 1. Schematic of the low-thermal-resistance TO-9 package, featuring a monolithic copper base, *p*-side-down mounting, and a diamond submount, designed to enhance heat extraction from the laser chip.





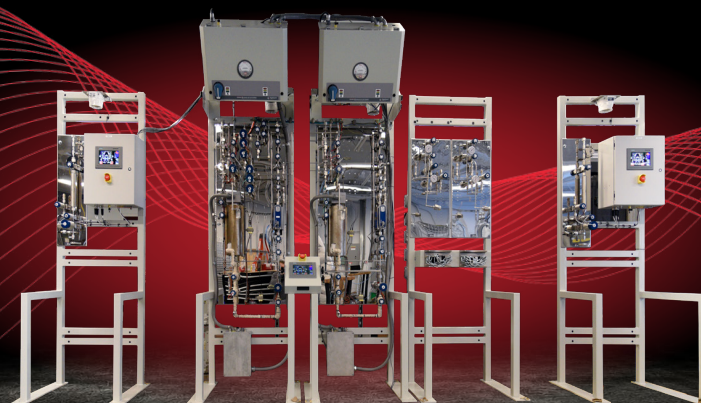
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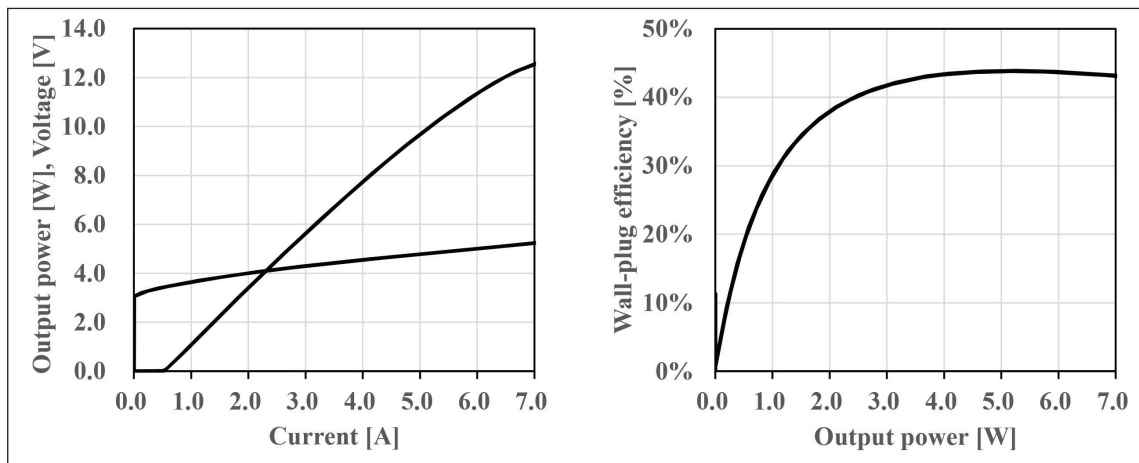
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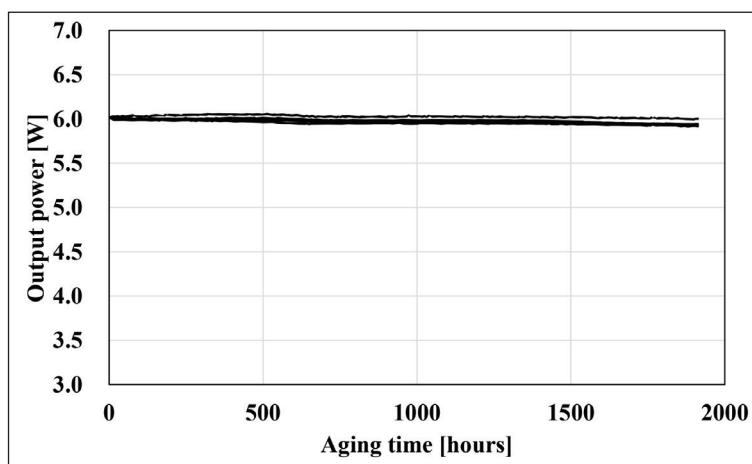
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► Figure 2. Optical output power and wall-plug efficiency measured under continuous-wave operation at a case temperature of 25°C for a 405 nm InGaN-based laser diode with a cavity length of 1400 μm and a stripe width of 45 μm .



► Figure 3. Long-term output stability of the laser diode during aging at 6 W and a case temperature of 25°C, demonstrating stable operation without catastrophic optical damage.

requiring a moderate output power are better served with geometries optimised for peak efficiency.

The key message is that our underlying design principles can support both high-power, thermally robust operation and high-efficient operation at lower output powers. What's required is to optimise the device geometry for the required characteristics.

Reliability at high power

When laser diodes operate at high output powers, there's severe stress on their facets and internal structures. This raises concerns related to long-term reliability. To look into this matter, we conducted aging tests under automatic current control, involving an initial output power of 6 W and a case temperature of 25°C. These conditions are representative of demanding industrial operation beyond typical commercial levels.

During extended operation, exceeding 1900 hours, we did not observe any catastrophic optical damage, and recorded minimal output degradation (see Figure 3). Based on the low degradation rate during our investigation, we can conclude that our device design provides a sufficient margin for long-term operation at this power level. These results underscore the importance of reducing optical and thermal stress through appropriate design of the device and its package.

Implications for LDI and beyond

The performance of our lasers overcomes a key barrier to the wider adoption of LDI in advanced semiconductor packaging. By delivering a substantially higher optical power from a compact semiconductor laser, we are enabling engineers in silicon fabs to shorten exposure times and boost throughput, without sacrificing system stability or lifetime. This leads to a step change in productivity, allowing LDI to provide the throughput required for industrial-scale manufacturing on large substrates.

Beyond LDI, there are opportunities for high-power, high-efficiency violet laser diodes in a number of other industrial applications, including additive manufacturing, precision processing and illumination systems – all benefit from short-wavelength, compact light sources.

As semiconductor manufacturing continues to evolve, the demands placed on light sources are only going to increase. Meeting them is our next step. We are targeting further improvements in efficiency, extension to other ultraviolet and visible wavelengths, and integration into application-optimised modules. Such efforts will build on successes to date, demonstrating that a coordinated approach – spanning epitaxial design, device geometry and thermal packaging – will enable semiconductor laser diodes to meet the stringent requirements of next-generation manufacturing technologies.

FURTHER READING

- S. Yoshida *et al.* "High-efficiency and high-power InGaN-based laser diode at a wavelength of 405 nm" *Proc. SPIE* **13896** 138960H (2026)

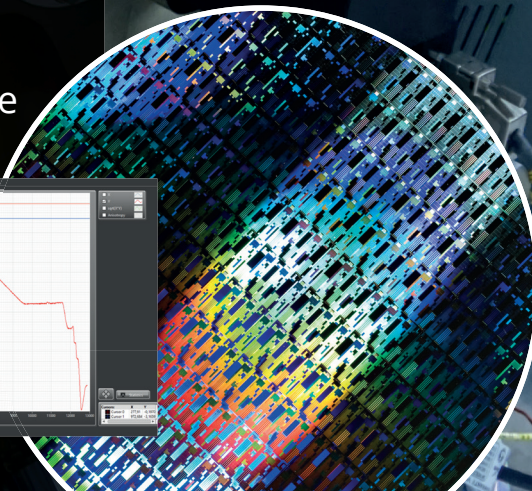
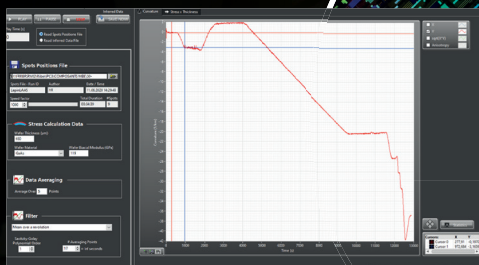
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A breakthrough for the bidirectional switch

By exceeding a blocking voltage of 5 kV while keeping conduction loss and reliability in check, a new generation of monolithic GaN bidirectional switches promise efficient, more compact medium-voltage AC power conversion

BY YUAN QIN FROM UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA, MING XIAO FROM XIDIAN UNIVERSITY, KAI CHENG FROM ENKRIS SEMICONDUCTOR, AND YUHAO ZHANG FROM THE UNIVERSITY OF HONG KONG

With minimal fanfare, power electronics is becoming the enabling layer for a number of converging transitions: electrified transport and industry, the build-out of renewable generation and storage, and the expansion of energy-intensive digital infrastructure. For all these cases, higher efficiency and a higher power density are no longer optional – instead, they directly translate into smaller passive components, simplified thermal management and a lower lifetime cost. The introduction of wide-bandgap semiconductors has already shifted the landscape, with GaN's success story told through unidirectional HEMTs, powering compact, high-frequency converters from 30 V to 400 V.

But many of the next frontiers for GaN are inherently AC-facing, so switches will have to handle current reversal and bipolar off-state voltages. While it is workable to implement that bidirectional capability

with anti-series devices, that solution scales poorly as voltage rises: chip area grows, parasitic capacitances stack, and gate-drive and layout complexity multiply.

A better approach is to attack this problem at its root, using a monolithic bidirectional switch. This form of switch shares the high-voltage region inside one device, and preserves efficiency while simplifying the circuit.

Taking the performance of these switches to a new realm, by delivering a hike in the voltage-handling capability, is our team from University of Science and Technology of China, Xidian University, Enkris Semiconductor and the University of Hong Kong. Our breakthrough promises to open the door to the deployment of this device in medium-voltage AC applications.

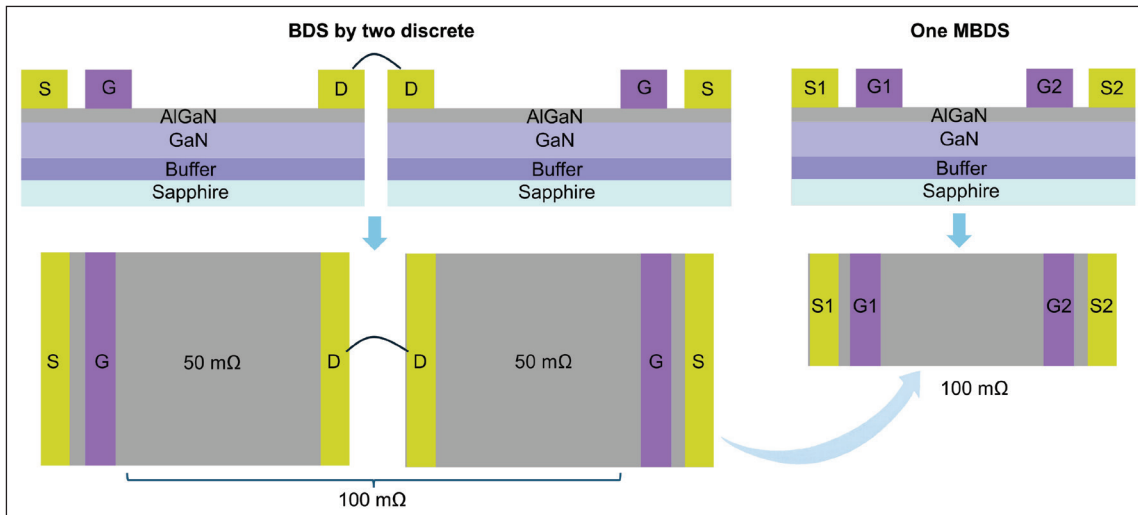
Motivation for our efforts has come from considering three questions: Why does bidirectional switching matter in real converters? Why do monolithic implementations offer such a strong advantage? And how is it possible to reach a high voltage with a bidirectional switch?

Why bidirectional?

The applications most in need of a bidirectional switch are those that involve a converter having to connect and disconnect an AC node efficiently. Matrix converters and current-source inverters are classic examples. In these circuits, the switch must handle current in both directions, as the load current and the instantaneous line voltage are not necessarily aligned. In addition, the same device must often sustain positive and negative blocking voltages, as switching states change over a line cycle.

Bidirectional switches are also valuable in solid-state transformers. They are a critical component in Nvidia's next-generation 800 V power delivery





➤ Figure 1. Conceptual comparison between a bidirectional switch realised using two discrete GaN transistors in anti-series and a single monolithic bidirectional switch sharing one drift region.

architecture in AI data centres, as well as in medium-voltage motor drives, and emerging AC distribution and protection concepts, where fast, controllable bidirectional elements can replace bulky passive components. For all these examples there tends to be a common economic driver: if a bidirectional function can be implemented with fewer devices, the overall system can be smaller, faster and more efficient.

At medium voltages, strong opportunity for the deployment of the bidirectional switch is in the AC-DC front end, used in data centres, rail traction and industrial power supplies. Here, design engineers are using three-phase active rectifiers and solid-state transformer stages to increasingly target higher switching frequencies and shrink magnetics.

In these systems, the bidirectional function is often realised with anti-series device pairs, a compromised solution that increases the active device count and stacks parasitic capacitances and stored charge. With this approach there's a higher commutation energy penalty on every transition, making it harder to push up the switching frequency without sacrificing efficiency.

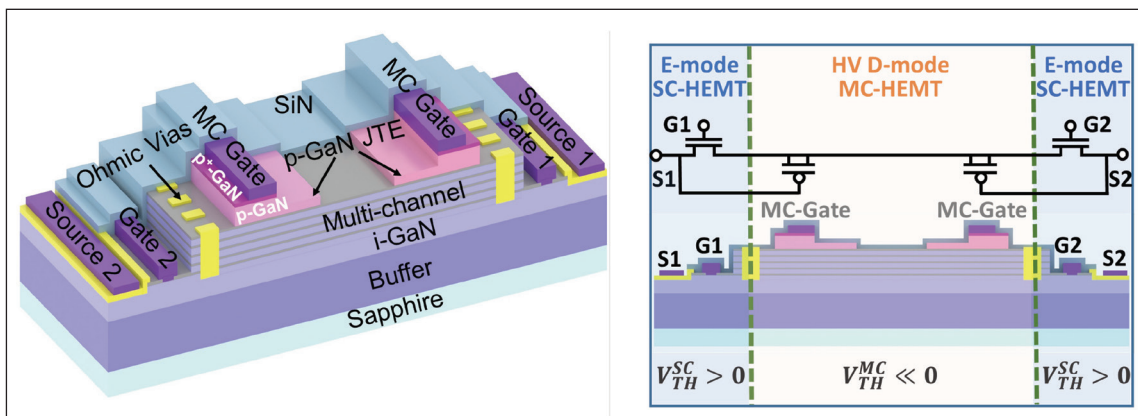
Additional examples associated with the potential deployment of bidirectional switches are medium-voltage motor drives and variable-

speed compressors. In these cases, introducing bidirectional switches enables matrix-converter and current-source topologies that remove the bulky DC-link electrolytic capacitor. Eliminating or downsizing the DC link improves lifetime and power density. However, to ensure success, the bidirectional switch must block bipolar voltages safely and repeatedly under fast switching, elevated temperature and rapidly changing voltages.

The monolithic advantage

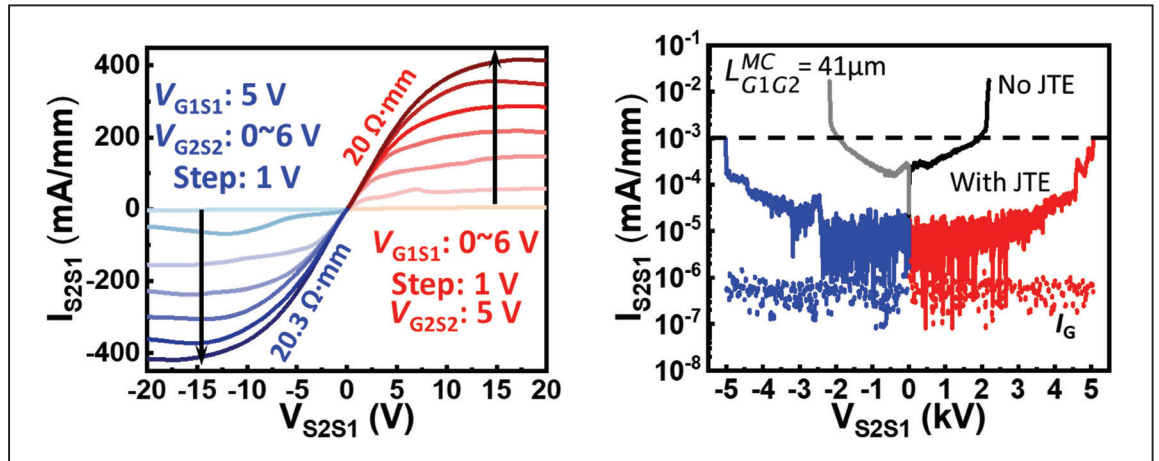
When a brute-force anti-series architecture is adopted, this doubles the number of active devices. That's not an elegant solution – as each device contributes roughly half the total on-resistance, there is a potential quadrupling of chip area to realise the same conduction loss as a single unidirectional transistor. At the system level, the penalty can be even more severe, with extra devices introducing additional capacitance, which must be charged and discharged for every switching cycle.

Introducing monolithic bidirectional switches reduces this overhead by placing two gated channels on one shared drift region – this avoids duplication in the high-voltage region (see Figure 1). At lower voltages, monolithic GaN bidirectional switches are already appearing as engineering samples in industry, pointing to a path for adoption.



➤ Figure 2. Device schematic and equivalent circuit model of multi-channel GaN monolithic bidirectional switch demonstrated at IEDM 2025.

➤ Figure 3. Bidirectional forward and blocking characteristics of the multi-channel GaN monolithic bidirectional switch.



One pertinent question is whether it's possible to preserve these monolithic advantages when shifting the voltage rating into the kilovolt class. In this regime, electric-field management, buffer breakdown, and reliability could be limiting factors.

Taming fields

In a bidirectional device, the high-voltage stress does not sit at a single drain edge in a fixed direction. Instead, the peak field can move, depending on the polarity of the blocked voltage, and it can couple to multiple gate stacks. Due to this, edge termination and field shaping are central design problems.

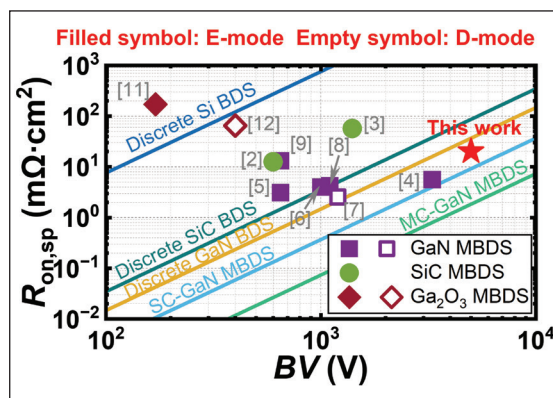
When we recently produced a 3.3 kV enhancement-mode monolithic bidirectional switch, we demonstrated one way to tackle this challenge. Working on a mature *p*-GaN gate platform on sapphire, the dual junction termination extension held the key to our success, with implementation in the *p*-GaN layer of the standard gate stack, without epitaxial regrowth. Our devices delivered a breakdown voltage exceeding 3.3 kV in both polarities, a threshold voltage around 0.6 V, and a specific on-resistance of $5.6 \text{ m}\Omega \text{ cm}^2$, while maintaining symmetric conduction in both directions.

Looking beyond the headline numbers, the junction termination extension concept is worthy of consideration. This refinement provides a field-shaping knob that does not rely solely on long field plates. Instead, by balancing field peaks at the gate edge and the termination edge, it allows the average lateral field to be pushed beyond what is typical in field-plated lateral GaN devices, while maintaining a low leakage current under bipolar blocking.

Multi-channel leap

Our 3.3 kV device established a high-voltage foundation. But it's just a starting point, as medium-voltage power conversion often demands higher voltages and higher currents. Ideally, this is realised without compromise, but in lateral GaN that's not easy, as efforts to reach to higher voltages tend to drive the drift region longer and the specific on-resistance higher, unless there's a reduction in channel and access resistances. One way to address this is to move to multi-channel AlGaIn/GaN materials, because multiple parallel channels can combine a high current capacity with a low sheet resistance.

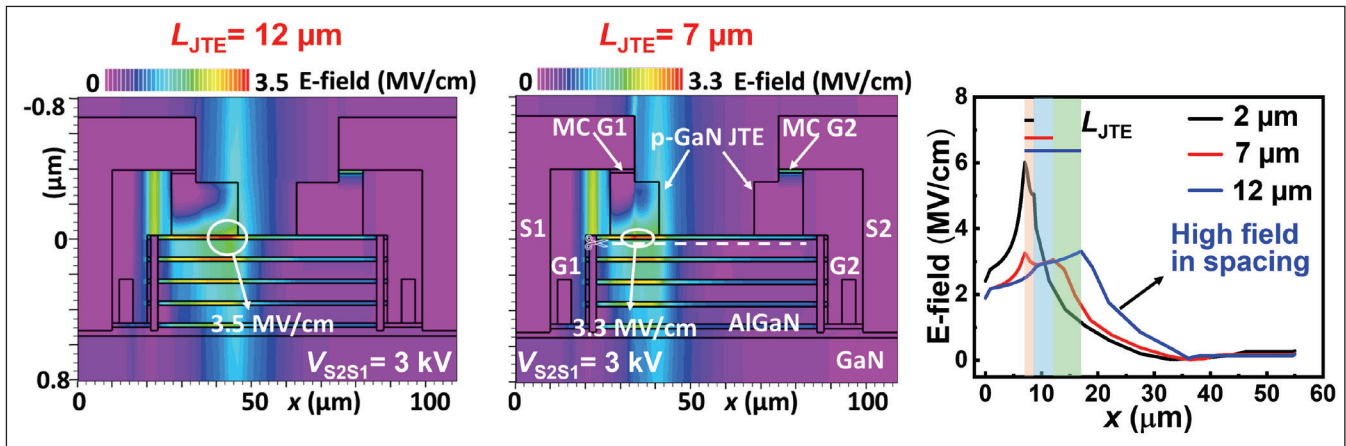
Late last year, at the International Electron Devices Meeting (IEDM), we unveiled the first multi-channel GaN monolithic bidirectional switch. It's a five-channel device, fabricated on a 150 mm GaN-on-sapphire wafer grown by Enkris Semiconductor (see Figure 2).



➤ Figure 4. Benchmarking state-of-the-art (ultra-) wide-bandgap monolithic bidirectional devices and the practical performance limits of discrete anti-series implementations.

Strengths of this switch include a symmetric blocking of up to 5 kV in both polarities, a specific on-resistance of around $20 \text{ m}\Omega \text{ cm}^2$ and a threshold voltage of about 0.8 V (see Figure 3). To our knowledge, 5 kV is the highest breakdown voltage ever reported for a monolithic bidirectional switch (see Figure 4).

Our device architecture combines two important ideas (see Figure 2). First, by employing a dual-junction termination extension, connected to the two high-voltage gates, it provides effective electric-field management in the central multi-channel region. Second, it realises enhancement-mode operation using a monolithic dual-cascode architecture. By integrating two low-voltage, single-channel



➤ Figure 5. Electric-field management using a *p*-GaN dual junction termination extension: simulated E-field contours illustrating the impact of the junction-termination extension (JTE) length and the risk of field crowding in the spacing region for an overlong termination.

enhancement-mode HEMTs on either side of the multi-channel bidirectional region, the overall switch behaves as an enhancement-mode device while the high-voltage multi-channel section retains its natural depletion-mode characteristics.

Optimising the termination length is particularly important in a bidirectional device (see Figure 5). When a high-voltage GaN switch is unidirectional, device designers may turn to a long *p*-GaN reduced-surface-field region to aid voltage scaling. But that's not an attractive option in a bidirectional structure with two terminations facing one another, as long termination on the high-side cannot necessarily be depleted in a helpful way – instead, there's the threat of failing to take advantage of the footprint and crowding the field in the spacing between the two terminations.

Based on simulations that suggest an optimal termination length that balances these effects, we implemented a termination length that supports 5 kV bipolar blocking. We recorded no destructive breakdown under our measurement compliance.

Reliability focus

A high voltage is only half the story. Reliability also matters, requiring serious consideration. In bidirectional devices, the stress differs from that found in a conventional transistor, because the blocked polarity alternates in normal operation and the second gate can sit at a non-trivial potential relative to the substrate. These factors raise practical questions about dynamic on-resistance, threshold stability and the right stress protocols for qualification.

Our multi-channel bidirectional switch shows encouraging signs, regarding reliability. In our paper from IEDM 2025, we described a comparison of our multi-channel 5 kV device and a single-channel bidirectional device with a similar termination concept. Under a high-temperature reverse-bias

stress at 150 °C, our multi-channel device underwent a shift in on-resistance of less than a 5 percent after 1,000 s of stress at 1.7 kV. In contrast, the single-channel device exhibited substantially larger on-resistance shifts under comparable stress conditions (see Figure 6).

Equally encouraging for system designers, we have found that our multi-channel device is relatively insensitive to substrate bias over our testing range. It's known that substrate bias management is a challenge for GaN-on-silicon bidirectional devices in practical circuits, because the substrate and buffer can couple to the switching node. By moving to an insulating sapphire substrate and exploiting a multi-channel stack, our device offers a proven robustness to substrate bias that's attractive for real converter environments.

To interpret our observed stability, we have proposed a physical picture, in which the multiple channels provide an inherent shielding effect. Our view is that in a single-channel device, charge trapped at the surface or in the buffer directly modulates only the conduction channel, leading to larger dynamic and stress-induced resistance shifts. Meanwhile, in a multi-channel structure, the top channel screens the influence of surface traps and the bottom channel screens the influence of buffer traps, to leave the middle channels less perturbed. The upshot is a smaller change in on-resistance after stress (see Figure 7).

Where next?

Thanks to a combination of 5 kV bipolar blocking, enhancement-mode control, and improved dynamic stability, our monolithic GaN bidirectional switches are compelling candidates for medium-voltage AC power conversion. Here, their established rivals are silicon or SiC solutions.

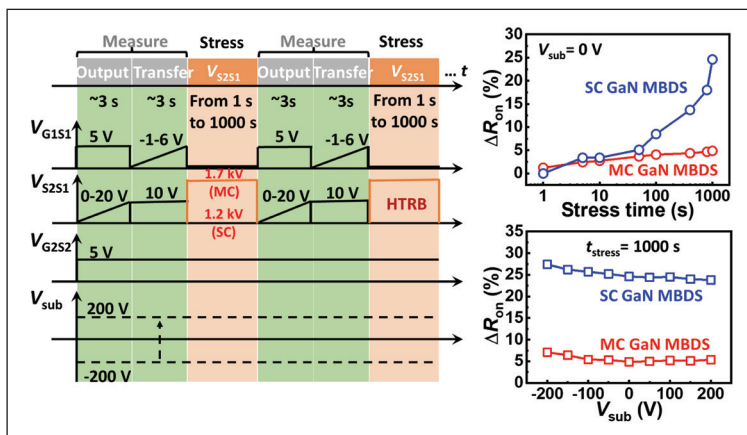
At the device level, the next steps are clear: a further reduction in specific on-resistance, realised through

layout and material optimisation; refinement to termination designs, to scale blocking voltage while maintaining controlled leakage; and a broadening of reliability evaluation, beyond static stress, to include circuit-relevant dynamic and switching tests. In practice, that means characterising dynamic on-resistance, switching energy and gate/termination bias sensitivities under realistic temperature conditions, while considering derivatives of voltage and current with respect to time. In addition, these measurements must be correlated with long-duration stress, to isolate and uncover dominant trapping and degradation mechanisms.

Once that device- and circuit-level understanding is in place, efforts can be directed at the system-level, re-thinking topologies constrained by cost and the

parasitics of anti-series device pairs. A genuinely compact monolithic bidirectional switch has the potential to simplify gate driving, reduce the energy stored in parasitic capacitances, and raise switching frequency without an equivalent penalty in loss. If these benefits are realised at scale, they could translate into smaller passive components, a higher power density, and increased efficiency in the medium-voltage converters underpinning electrified transport, renewable integration and industrial automation.

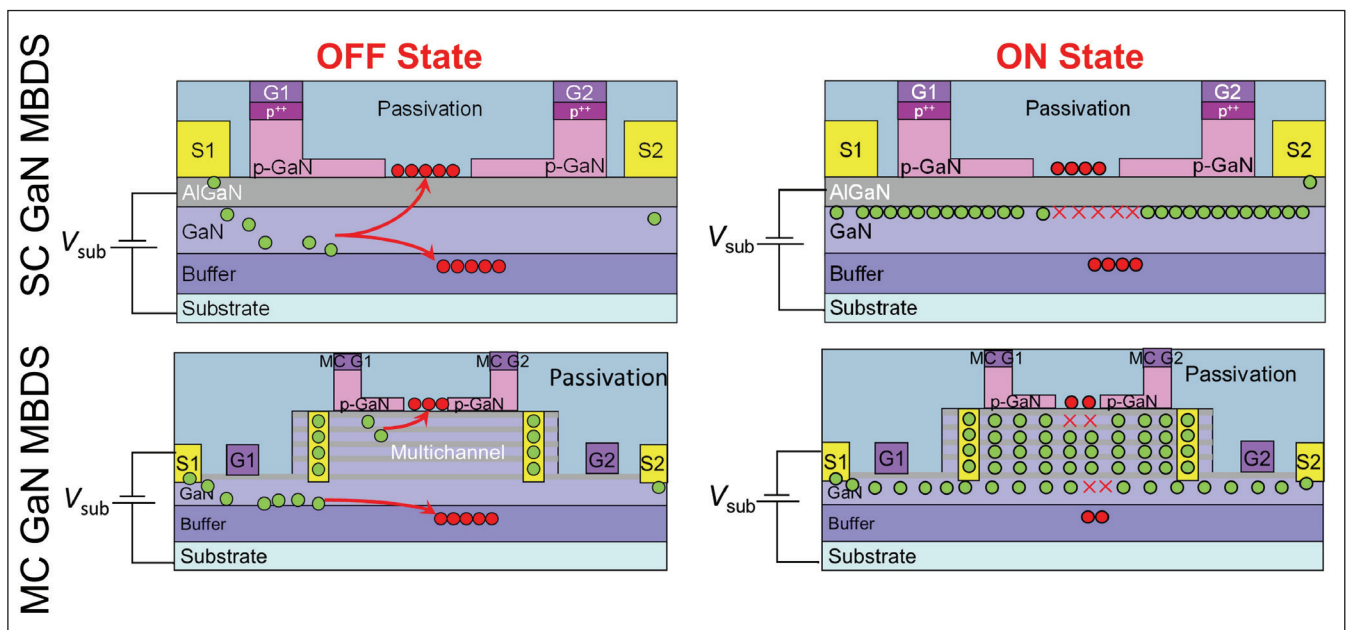
While bidirectional switching is not a new functional requirement in power electronics, it is becoming a more urgent one as systems shift towards higher-frequency operation and tighter volumetric constraints. Given the great progress in moving from 650 V to 5 kV in GaN monolithic bidirectional switches, alongside a growing understanding of their unique reliability physics, there is good reason to think that this technology is moving from an academic curiosity to a platform that will meaningfully reshape medium-voltage converter design.



➤ Figure 6. Device reliability: high-temperature reverse-bias stress sequence, and the evolution of on-resistance shift for single-channel versus multi-channel devices.

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- Y. Qin *et al.*, “5 kV, 20 mΩ·cm² Enhancement-Mode Multi-Channel GaN Monolithic Bidirectional Switch,” 2025 IEDM, pp. 1-4, 2025.



➤ Figure 7. Schematic illustration of device physics: impacts of interface and buffer traps on middle channels are shielded by top and bottom channels, reducing the dynamic on-resistance shift for the multi-channel GaN monolithic bidirectional switch.



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Transferable thin-film GaN LEDs

Electrochemical etching lifts membranes of III-nitride LEDs, opening the door to scalable integration into CMOS-based photonics

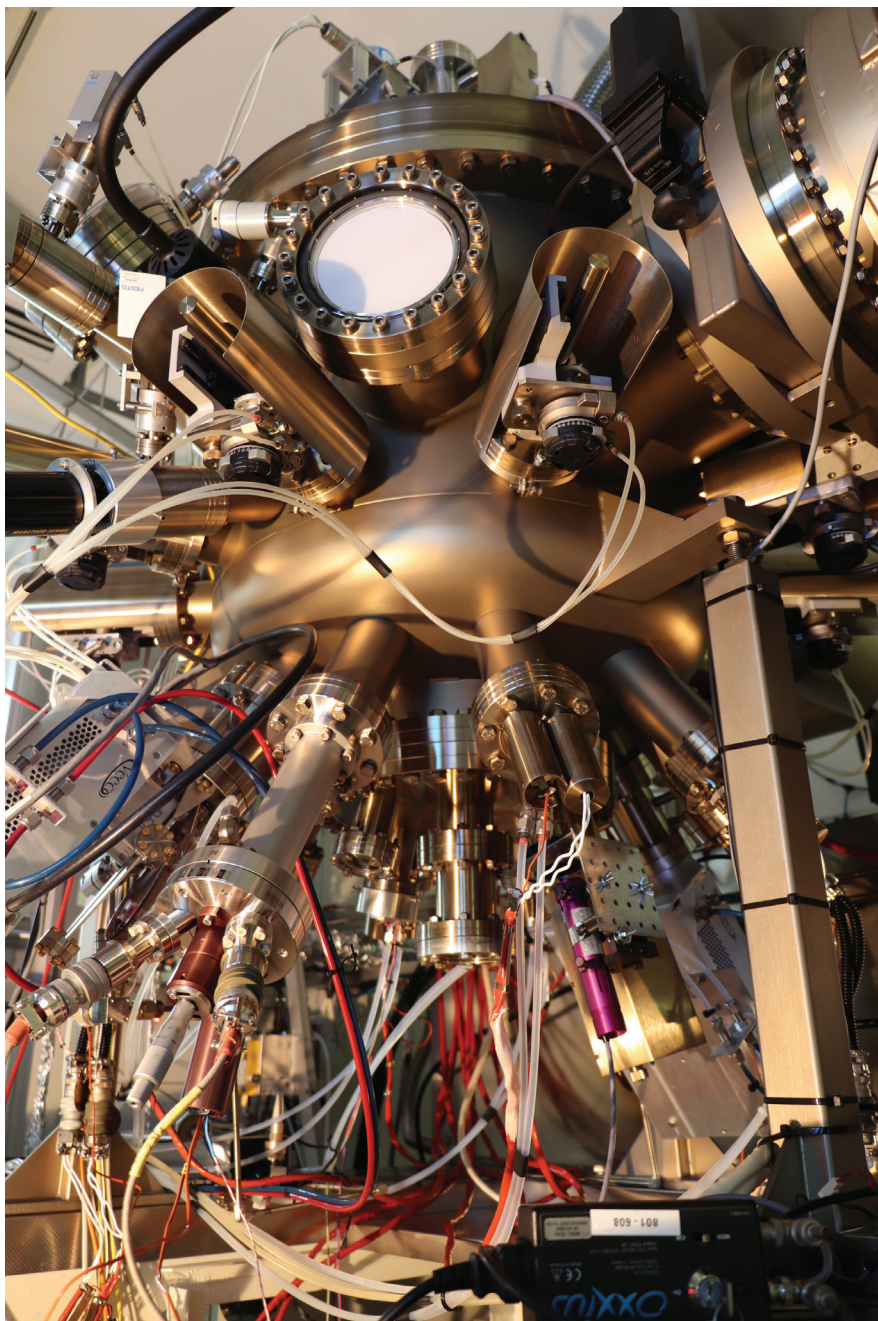
BY MIKOŁAJ CHLIPAŁA AND HENRYK TURSKI FROM THE INSTITUTE OF HIGH PRESSURE PHYSICS OF THE POLISH ACADEMY OF SCIENCES

GENERATION of visible light has been transformed by GaN. From solid-state lighting to backlighting displays, optical communication and sensing, GaN-based devices are deeply embedded in today's technology. Yet as optoelectronic systems become more complex, another key requirement is coming sharply into focus: the ability to integrate high-quality light sources onto CMOS-compatible substrates.

This particular task is far from trivial. The trait that ensures the success of GaN devices – their excellent quality when grown on native bulk GaN substrates – has a downside, as it makes them stubbornly difficult to integrate with other technologies. And as well as being technically demanding, GaN substrates are expensive, reinforcing the need to use the material as efficiently as possible.

Moreover, bulk GaN is poorly suited for integration with with photonic integrated circuits, silicon electronics and flexible electronic platforms. All three of these technologies demand substrates that are inexpensive, available in large sizes and supported by mature fabrication ecosystems –

➤ Figure 1. A plasma-assisted MBE system at Institute of High Pressure Polish Academy of Science used for GaN LED growth. Gallium and other group-III elements are supplied from thermal evaporation sources, while active nitrogen is provided by a radio-frequency plasma source, enabling low-temperature growth of high-quality III-nitride epitaxial layers. Photo Dr. Grzegorz Muzioł.



criteria that bulk GaN fails to fulfil. And one potential solution, substrate re-use, is not easy. For GaN devices grown homoepitaxially on bulk substrates, it's been a formidable challenge to detach the active device without damaging it.

The good news is that a promising solution is emerging, thanks to our efforts at the Institute of High Pressure Physics of the Polish Academy of Sciences. By combining epitaxial design with low-voltage electrochemical etching, we cleanly release ultra-thin GaN LED membranes, incorporating nanometre-smooth back surfaces. From there we integrate these membranes on foreign substrates by micro-transfer printing, while retaining electrical and optical performance. This approach provides a practical pathway to heterogeneous integration of high-quality GaN light sources, accomplished without sacrificing the exceptional strengths of these emitters.

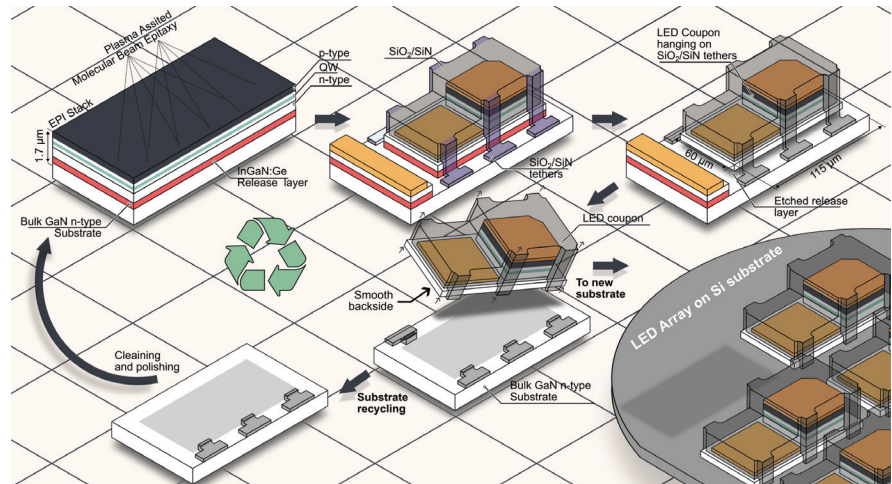
The value of native substrates

For the growth of GaN LEDs, a native substrate is superior to both sapphire and silicon, as it enables a significantly lower threading dislocation density. Thanks to this, devices have higher current handling, higher efficiency, enhanced reliability and a higher yield per wafer. These attributes are particularly important when LEDs are driven at high current densities, or deployed in demanding applications.

Due to the crystallographic compatibility of GaN-on-GaN LEDs, established escape routes for device release are unavailable. It's not possible to employ laser lift off, which works well for GaN-on-sapphire, thanks to the absorption of laser energy at the interface; and wet etching, a common option for devices grown on silicon, is not viable.

Against this backdrop, electrochemical etching has much appeal. This technique enables selective removal of layers with specific doping concentrations, and leaves device layers intact. However, several obstacles are limiting the usefulness of this etching technique for micro-transfer printing applications.

Of these, the biggest obstacle is surface quality. For micro-transfer printing, interfaces must be extremely flat to ensure good mechanical contact and sufficient adhesion to the target



► Figure 2. Simplified process flow for thin-film LED transfer. The process begins with MBE, followed by standard LED device processing. Electrochemical etching selectively removes the sacrificial release layer (shown in red), leaving the LED coupon suspended. At this stage the device is supported only by a SiO₂/SiN tethers, which are subsequently broken during the transfer step to release the thin-film LED onto a target substrate. The substrate can be cleaned and reused.

wafer. Any residual roughness on the backside of a released device could compromise yield and reliability. To preserve device integrity, another matter to address is the suppression of parasitic etching paths, which can occur through dislocations, sidewalls or metal contacts.

Initial efforts involving electrochemical or photoelectrochemical lift-off tended to suffer from at least one of these issues. Common problems included backside roughness that remained too high, and inadequate device protection for fully processed LED structures. It's imperative to show that electrochemical etching not merely works – it must be refined into a robust, transferable process.

The role of the sacrificial layer

Behind our success is the realisation that backside smoothness is determined as much by epitaxial design as electrochemistry. Rather than relying on aggressive etching, our strategy is to ensure that the sacrificial layer is easy to remove in a uniform, selective and gentle way.

We realise this by introducing an InGaN release layer, heavily doped with germanium, that's inserted beneath the LED structure. Germanium is a great choice, as it allows extremely high electron concentrations, while avoiding severe degradation of the crystal structure and surface morphology.

Using plasma-assisted MBE, we produce carrier densities as high as $6 \times 10^{20} \text{ cm}^{-3}$ – that's far beyond what is typically possible with silicon doping.

Our second trick is to use a release structure that consists of two layers. This duo combines a thicker, germanium-doped InGaN layer that provides electrochemical access with a thinner, even more heavily doped top layer that ensures complete, uniform removal. With this pairing, the total thickness of the etched material is around 300 nm. Above this sacrificial region sits an *n*-type GaN layer – it has a doping level that's lower than the sacrificial layer, and supports current spreading – followed by a thick, single quantum-well active region, and then *p*-type layers.

Crucially, the rest of the device stack remains electrochemically inert under our etching conditions. Key to this is the separation of roles by doping. We have a sacrificial layer that's heavily doped, and device layers that are only moderately doped. This contrast ensures that electrochemical etching at a low bias selectively targets the release layer, dramatically reducing the risk of surface roughening or unintended damage to the active device structure.

From wafer to coupon

Even with a well-designed release layer, electrochemical etching of fully

processed devices is not trivial. There are a number of potential failure points, including metal contacts, mesa sidewalls and exposed semiconductor surfaces. Preventing failure requires a careful sequence of processing and protection steps.

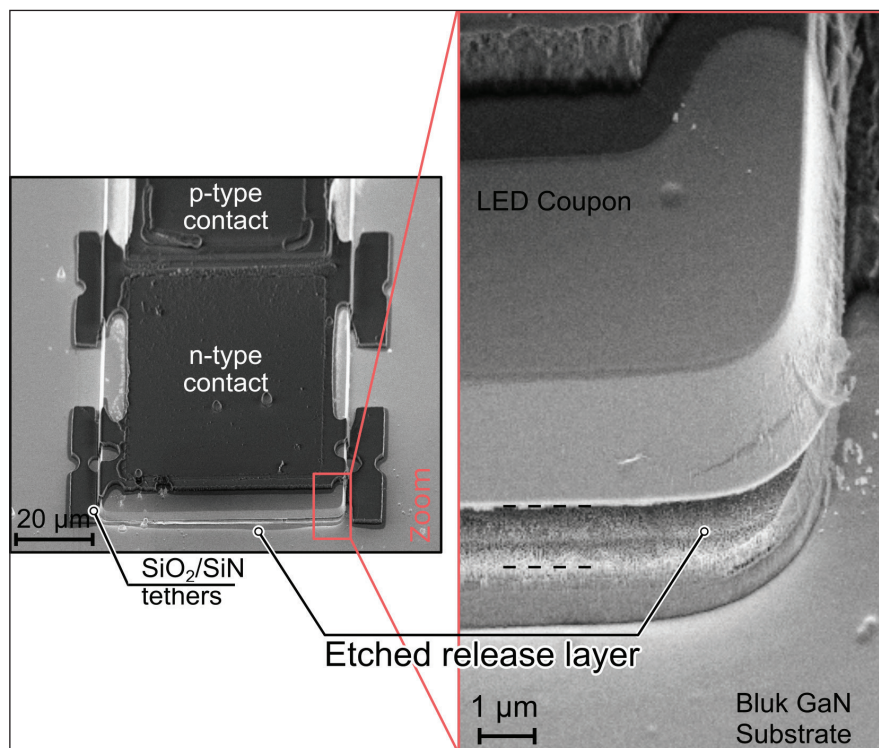
Following standard LED fabrication, which includes mesa definition and the formation of *p*- and *n*-type contacts, we introduce an additional metal layer that provides electrical access for etching bias. Our devices are then fully encapsulated in a dielectric stack, comprising alternating layers of SiO₂ and SiN. This encapsulation serves multiple purposes: it shields metal contacts from the electrolyte, it blocks parasitic etching, and it mechanically reinforces the structure during release.

Our next step involves using photolithography and dry etching to pattern the dielectric into narrow tethers, which anchor each LED coupon to the parent wafer. It's crucial that these tethers strike a careful balance: they must be stiff enough to hold the coupons in place during processing and shipping, yet fragile enough to break cleanly during transfer printing.

Finally, we apply a thick photoresist, to control the direction of the etching front. This enables the exposure of only one edge of the sacrificial layer per coupon. Once this preparation is complete, we submerge the entire wafer in an oxalic acid electrolyte, biased at 3 V. Over several hours, the heavily doped InGaN layer is selectively removed, undercutting the LED coupons, to leave them suspended above the bulk GaN substrate. The coupons are held by dielectric tethers.

Nanometre scale flatness

If our approach is to be a success, there must be minimal roughness after etching. According to surface



➤ Figure 3. Scanning electron microscopy of an LED coupon with an etched release layer beneath and attached by a SiO₂/SiN/SiO₂ multilayer to a substrate. A magnified view shows separation at the coupon-substrate interface. For more information see ACS Applied Electronic Materials 7 4814 (2025).

profiling by atomic force microscopy, we are able to realise that, as there's the same degree of roughness on our calibration samples, consisting of only a release layer, and on the backside of our released LED coupons. What's really encouraging is that the surface morphology of this backside closely mirrors that of the original release layer, indicating that our electrochemical process faithfully reproduces the epitaxial interface, rather than introducing new damage.

For micro-transfer printing, this level of smoothness is crucial. It enables a perfect contact with the adhesive layers on target wafers, reduces the risk of voids or delamination, and thanks to

this sub-nanometre roughness, it's possible to precisely and reliably align the height of the device after transfer. The last trait is crucial for integration into a photonic circuit, where it is critical to align the light source with waveguides.

How to move LEDs?

Realising great surface quality is of little value, if it's accompanied by a device performance that's compromised during release. To look into this matter, we explored two transfer approaches.

The first of them is not gentle, involving the removal of individual LEDs with a micromanipulator. What's pleasing is that electrical measurements confirm that these devices continue to operate as they did before transfer, even after conversion into ultra-thin, free-standing membranes by this crude handling method.

While micromanipulator transfer provides a useful proof of concept, to enable scalable integration, a more versatile approach is needed. We accomplish this with micro-transfer printing. Using polydimethylsiloxane (PDMS) stamps, we pick up multiple

While micromanipulator transfer provides a useful proof of concept, to enable scalable integration, a more versatile approach is needed. We accomplish this with micro-transfer printing. Using polydimethylsiloxane stamps, we pick up multiple released LED coupons, in parallel from the source wafer.

released LED coupons, in parallel from the source wafer. During this step dielectric tethers fracture. These coupons are then printed onto a foreign substrate, in this case silicon pre-coated with a thin adhesive layer. Measurements across multiple printed LEDs show remarkably consistent current-voltage characteristics, confirming that our process is reproducible and scalable. Our sequence – release, pick up, printing and connecting – illustrates how electrochemically released GaN LEDs can be embedded into different systems.

We have employed this approach to interconnect multiple LEDs on a target wafer and form a simple array. This technique is particularly attractive for future display technologies, given that III-nitride materials have an emission envelope spanning the UV to the red. Note, though, that our demonstrated devices are still too large for deployment in portable or high-resolution consumer displays, highlighting the need for further down-scaling of the process.

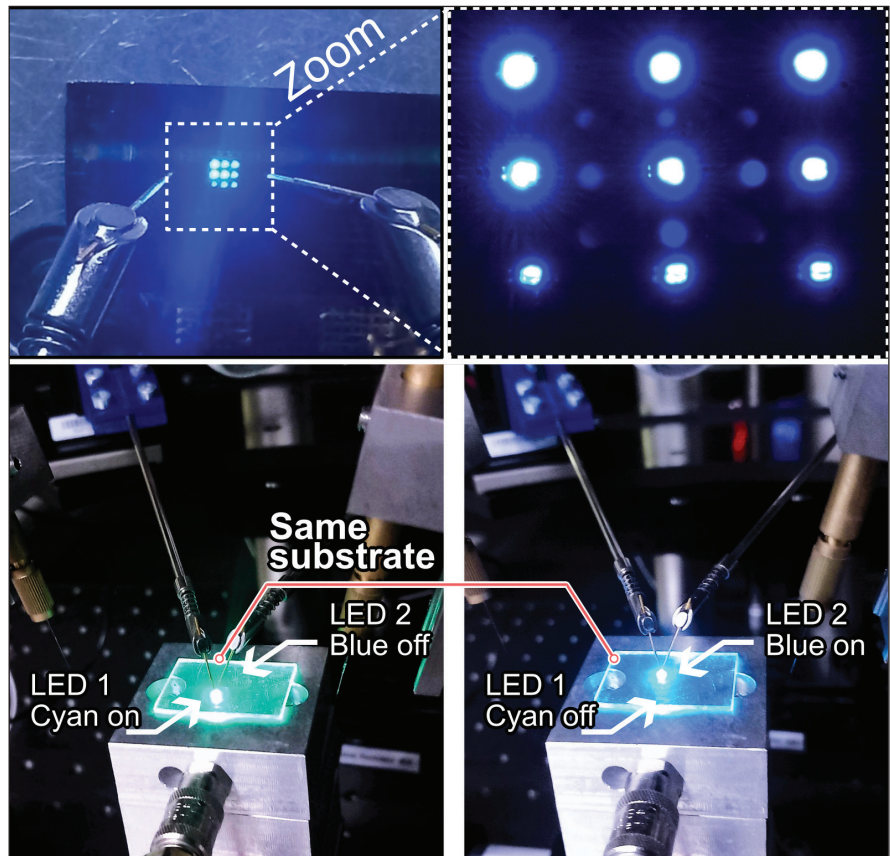
Beyond LEDs?

Although our work has focused on visible LEDs, its implications reach far wider. By combining bulk GaN material quality with heterogeneous integration, we are opening a new design space across III-N technology.

One class of technology that could benefit is the photonic integrated circuit. Our efforts enable on-chip, high-performance GaN light sources, without the need for direct epitaxial growth. It's also possible to transfer power devices to CMOS-compatible substrates with our approach.

When evaluating our efforts, one should not overlook the significant advantage that comes from substrate reuse. As the bulk GaN wafer remains intact after electrochemical undercutting, it can, in principle, be reclaimed and reused – this helps offset the high cost of native substrates.

At the wafer scale, our release process removes around just 300 nm of material when freeing LED coupons. For a 2-inch wafer, this corresponds to a total gallium loss of a few milligrams. Such minimal loss is valuable, as it's important to drive down gallium consumption, given its limited supply, energy intensive



➤ Figure 4. (Top) Photograph of an LED array consisting of nine devices, connected in parallel, that have been transferred to silicon wafer. (Bottom) An example of single substrate, on which LEDs emitting in different colours were transferred. Photo: Konstantinos Akritidis.

extraction, and growing demand across power electronics, photonics and defence applications. Approaches that ensure material efficiency, while preserving substrate integrity, could deliver a decisive economic benefit in a manufacturing environment.

Note that while our approach employs plasma-assisted MBE to produce extreme germanium-doping levels, our underlying concept is not limited to a single growth technique. It's possible that following further optimisation, lower doping concentrations – accessible by other epitaxial methods – may also enable a similarly smooth release.

Our work promises to play a significant role over the coming years, since

device integration will become increasingly central to photonics and electronics. We view techniques to decouple material quality from substrate choice as essential, and consider our electrochemical release as an attractive solution for this task.

By addressing the long-standing challenges of backside roughness, device protection and scalability, our approach is transforming electrochemical etching from a laboratory curiosity to a practical manufacturing tool. It allows the best attributes of bulk GaN LEDs to be retained and redeployed wherever needed, while allowing reuse of the expensive bulk substrate.

FURTHER READING

- M. Chlipała et al. "Electrochemical release of transfer ready III nitride LEDs from bulk substrates" *ACS Appl. Electron. Mater.* **7** 4814 (2025)

Enhancing HgCdTe detectors with plasmonics

With the addition of plasmonic nanostructures, HgCdTe infrared detectors can benefit from stronger signals and provide several advantages at the system level

BY NAGENDRABABU VANAMALA FROM TENNESSEE STATE UNIVERSITY

WHILE they are often unseen, infrared detectors are all around us, underpinning many applications. They are deployed for night vision, surveillance and environmental monitoring, and advanced defence systems.

For detection in the infrared, the established material of choice is HgCdTe. Merits of this ternary include its tuneable bandgap, and its high sensitivity across a wide spectral range.

While these advantages are valued, there's a fundamental challenge with HgCdTe. When incident infrared radiation impinges on this detector's active region, the resulting interaction may not be strong enough to generate a large population of charge carriers. This weakness stems from an optical absorption that is not that high, holds back signal strength, and ultimately constrains detector sensitivity and resolution.

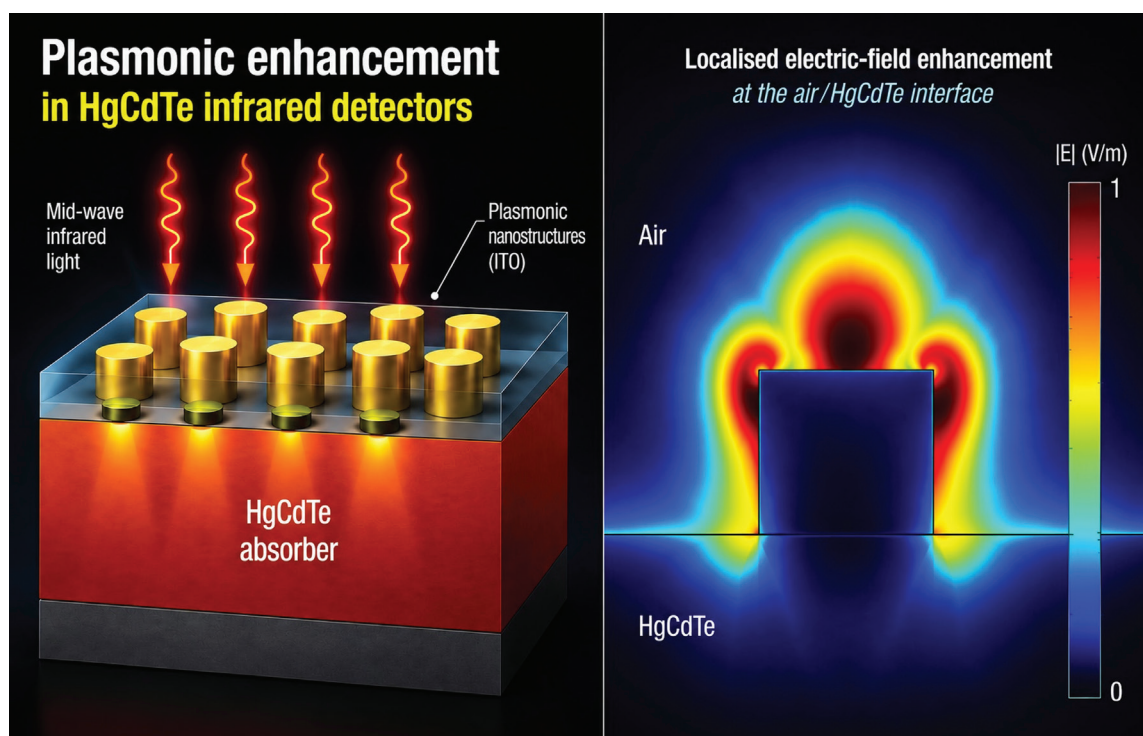
Due to this limitation, strategies for improving detector performance must focus on enhancing the light-matter interaction within the absorber. An attractive way to realise this is to strengthen the local electric-field intensity, as this increases the efficiency for the conversion of incoming photons into electrical signals, without having to increase absorber thickness or adjust semiconductor composition.

HgCdTe foundations

By altering the composition of HgCdTe, detection can span the short-wave, mid-wave, and long-wave spectral regions. This flexibility makes this alloy indispensable for multispectral and broadband sensing systems operating across atmospheric transmission windows.

Traditionally, to ensure strong absorption, the designers of detectors employ relatively thick

➤ Plasmonic enhancement in HgCdTe infrared detectors. Schematic illustration of plasmonic nanostructures integrated with a HgCdTe absorber, together with a simulated electric-field distribution showing localised field enhancement at the air/HgCdTe interface.



absorber layers. While this strategy enables effective capture of photons, thicker material may exacerbate recombination effects and impose constraints on performance, manufacturability and cost. All this matters – there's demand for infrared systems with superior sensitivities and greater efficiencies, so enhancing absorption without increasing material thickness is a central challenge.

Approaches to tackling this need to enhance absorption include modifying the semiconducting material. But there's also a more elegant solution, involving engineering of the optical environment at the detector surface.

That's the methodology we're pursuing at Tennessee State University. Our efforts demonstrate that it's possible to significantly enhance midwave infrared absorption in HgCdTe by integrating plasmonic nanostructures at the detector interface. By adding carefully designed metallic or dielectric nanostructures, our design concentrates optical fields near the surface, strengthening the light-matter interaction and increasing absorption within the active region.

Field enhancement

When infrared radiation interacts with our nanostructures, this generates collective oscillations of free electrons, known as surface plasmons. These resonances introduce highly localised electromagnetic fields in the vicinity of the nanostructures. In turn, there's an increase in the optical energy density inside the HgCdTe absorber, boosting photon absorption within thinner layers. According to numerical modelling by our team, optimised plasmonic structures enhance midwave infrared absorption by approximately 15-18 percent, with higher gains achievable for specific geometries. Crucially, this enhancement comes without increasing absorber thickness or modifying the semiconductor material.

We employ what's referred to as an effective-medium approach to model the optical response of nanostructured HgCdTe systems. Although structures involve nanoscale features, so quantum effects influence carrier behaviour, one can treat the interaction with infrared radiation with classical electromagnetic theory.

The structures we have considered include periodic nanostructure arrays, consisting of materials such as indium tin oxide embedded in air – it's a combination that forms an effective optical layer, with a refractive index depending on geometry, spacing, and scattering characteristics. The effective index, which is strongly dependent on feature size, periodicity, and geometry, governs the resulting electric-field distribution, quantum efficiency, and absorption behaviour.

To ensure plasmonic enhancement, nanostructured material must exhibit a negative real permittivity at

From a manufacturing standpoint, periodic nanostructures are particularly attractive, because they are compatible with standard lithographic techniques, and they tolerate realistic dimensional variations

the detector's operating wavelength. In the mid-wave infrared, there are a number of transparent conducting oxides satisfying this condition, behaving as metallic media while maintaining a comparatively low optical loss. When this happens, localised surface plasmons are excited at the interface with HgCdTe, producing intense near-field confinement and a strong coupling of optical energy into the absorber. This allows transparent conducting oxides to serve as effective plasmonic materials in spectral domains where conventional noble metals are less suitable.

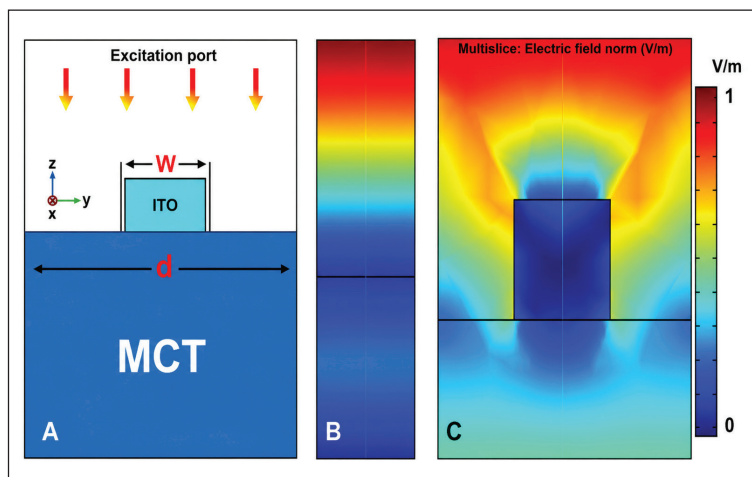
The negative permittivity, needed to ensure a plasmonic resonance, governs how electromagnetic waves are confined and guided at the nanostructure interface. A negative permittivity ensures that the material supports surface-bound modes – they remain tightly confined near the interface rather than propagating into free space. Thanks to this confinement, there's a significant increase in the local density of optical states, allowing more-efficient coupling of incident radiation into the absorber region.

From a device perspective, this behaviour is ideal, as it enhances the probability that photons contribute to carrier generation, and it reduces the likelihood that they are reflected or transmitted. The upshot is more efficient optical-to-electrical conversion, even in thin absorbers. It's an improvement that's particularly important in HgCdTe systems, where absorption, noise figures, and detector sensitivity are strongly linked to absorber thickness.

During our development of HgCdTe detectors that are enhanced with plasmonics, we uncovered small deviations between our measured and simulated values for absorption near the band edge, arising primarily from temperature sensitivity and detector operating conditions. Note that HgCdTe devices are typically optimised for low-temperature operation, and measurements performed under ambient conditions introduce fluctuations in detector response. This is particularly significant near the absorption edge, where small temperature variations may lead to noticeable differences in measured absorbance.

Why geometry matters

Details associated with geometry play a crucial role in determining how effectively plasmonic



► Figure 1. HgCdTe detector structures benefit from plasmonic nanostructures. This illustration highlights key geometric parameters and optical excitation.

structures enhance absorption. We have shown that while the choice of material sets the fundamental electromagnetic response, the spatial distribution and intensity of the near field are governed by the shape and periodic arrangement of the nanostructures.

Through systematic modelling we have uncovered some clear trends. Adopting symmetric structures, such as rings and cylinders, produces a relatively uniform field enhancement and reduced polarisation sensitivity, traits that are valued when constructing a detector. If highly asymmetric shapes are deployed, this can generate stronger localised fields – but potentially at the expense of

an increased sensitivity to fabrication tolerances and illumination conditions.

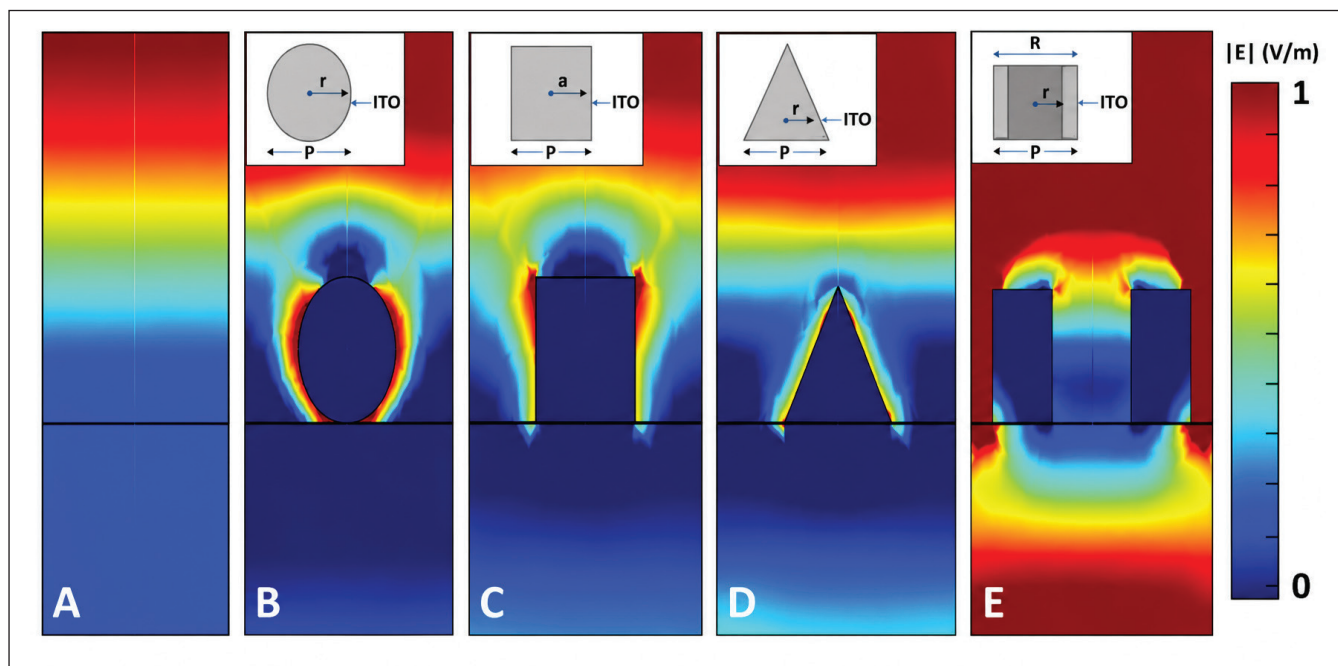
The benefits of the plasmonic structure are significant, due to enhanced fields extending several micrometres into the HgCdTe absorber – that's comparable to the thickness of conventional mid-wave absorbing layers. Thanks to this extension, there's enhanced absorption, removing the need to resort to thicker material stacks.

Optimised structures

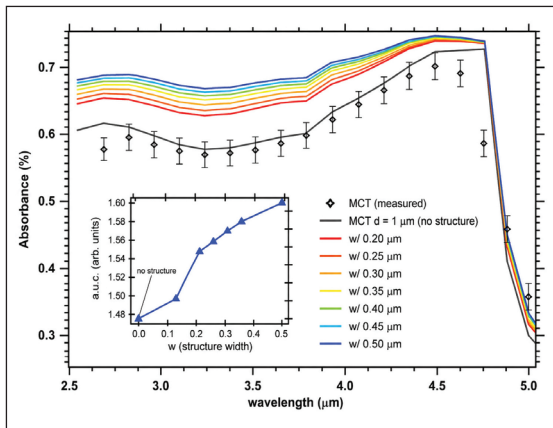
Our efforts to optimise plasmonic structures have been systematic, considering shapes that include rings, cylinders, and pyramids. This extensive investigation has revealed that the shape, size, and periodicity of the nanostructure have a decisive influence on absorption efficiency.

By tuning these parameters, we engineer absorption enhancement across the midwave infrared while retaining established semiconductor fabrication processes. We have found that transparent conducting oxides, such as indium tin oxide, are particularly attractive in this context. They offer metal-like optical behaviour with comparatively low loss in the infrared.

Our work has also highlighted practical trade offs. We have found that designs for maximising peak enhancement at a single wavelength may not perform as well across the broader spectral range required for imaging applications. This finding shows that what's needed is to identify geometries that balance absorption gain with robustness and manufacturability.



► Figure 2. Simulated electric-field distributions at the air/HgCdTe interface for different plasmonic nanostructure geometries: (A) reference structure without nanostructures, (B) spheres, (C) cylinder, (D) cones, and (E) rings. The simulations illustrate how nanostructure geometry influences localised field confinement and optical absorption behaviour. Insets show the optimisation parameters corresponding to each geometry.



➤ Figure 3. Measured and simulated optical absorbance of HgCdTe in the mid-wave infrared spectral region for varying nanostructure widths, demonstrating enhanced absorption compared with conventional structures without plasmonic enhancement.

For our modelling, we use periodic boundary conditions to represent extended nanostructure arrays, allowing a single unit cell to capture the collective optical behaviour of large-area patterned surfaces (see Figure 1 and Figure 2).

The impact of these design choices on measured and simulated absorbance is evident (see Figure 3)

Practical considerations

If plasmon-enhanced HgCdTe detectors are to be produced in volume, in addition to a strong optical performance, they must be manufacturable and reliable. Fortunately, these conditions should not be that demanding, as plasmonic elements can be implemented as surface features. This allows the introduction of electromagnetic field engineering without having to alter the underlying semiconductor growth process.

From a manufacturing standpoint, periodic nanostructures are particularly attractive, because they are compatible with standard lithographic techniques, and they tolerate realistic dimensional variations. But care is needed – we have identified that plasmonic enhancement introduces design trade-offs that must be managed. As mentioned before, while high absorption at targeted wavelengths is possible with strongly localised resonances, if the spectral response is overly narrow, this might not suit broadband imaging applications.

Another challenge is to control optical loss, so that there's no excessive heating or impaired efficiency. Helping to fulfil this objective are transparent conducting oxides, which provide negative permittivity with a comparatively low loss in the infrared, and enable robust field confinement while preserving overall detector performance. By balancing these factors,

plasmonic field engineering delivers meaningful gains, and builds on simulations to construct large-area, practical infrared detector systems.

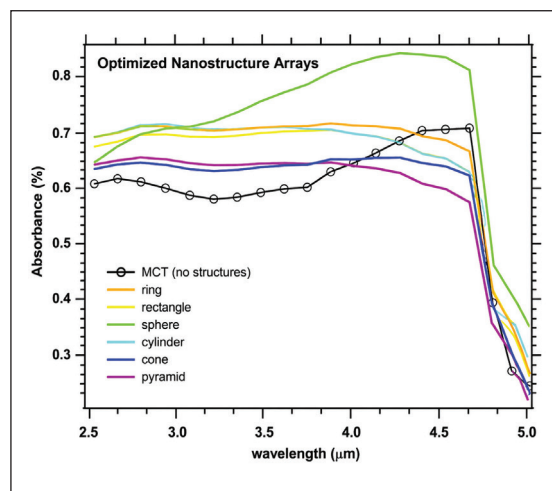
The overall improvement in absorbance achieved through geometric optimisation is illustrated (see Figure 4).

Broader adoption

What began as an effort to enhance light-matter interaction in HgCdTe detectors has evolved into a broader design philosophy that's been adopted and extended by other research groups across infrared photonics and optoelectronics. Our technology for enhancing optical absorption by engineering the electromagnetic environment has been shown to be robust and transferable across different materials, device architectures, and operating regimes.

Drawing on our efforts, researchers at the Army Research Laboratory have used gold-based plasmonic nanostructures to enhance infrared absorption in HgCdTe detectors. Although they employed noble metals, rather than transparent conducting oxides, they are also using localised surface resonances to increase the electric-field intensity at the detector interface and strengthen absorption in thin HgCdTe layers. Their success shows that our field-enhancement framework is not restricted to a specific material system, and can be implemented with different plasmonic platforms, depending on design constraints and fabrication considerations.

Extending these concepts beyond plasmonic materials, Mohammad Ariful Hoque Sojib and co-workers from Virginia Commonwealth University have shown that dielectric-grating-based architectures enhance the absorption in sub-wavelength HgCdTe layers by increasing the lateral optical propagation within the absorber. Although these designs do not rely on metallic plasmonics, they apply the same underlying mechanism of nanostructure-mediated light confinement we



➤ Figure 4. Optimised plasmonic nanostructure arrays showing enhanced optical absorbance across the mid-wave infrared spectral range after geometric optimisation of the nanostructure parameters.

Why transparent conducting oxides matter

IN PLASMONIC infrared design, material choice is as important as geometry. Transparent conducting oxides have much appeal, as they exhibit metallike optical behaviour in the infrared while remaining compatible with standard semiconductor processing.

The optical response of transparent conducting oxides may be tuned through free-carrier concentration, to align resonances with specific infrared wavelength bands. For HgCdTe detectors, where absorber thickness and operating temperature are closely linked, introducing oxide nanostructures allows architectures to recover absorption in thinner layers and reduce cooling requirements without compromising sensitivity.

introduced to compensate for reduced absorber thickness.

More advanced plasmonic implementations by Marco Vallone and co-workers from the Polytechnic University of Turin have involved investigating plasmonic cavity architectures for high-operating-temperature HgCdTe infrared detectors. Efforts by these researchers show that engineered resonances can improve absorption efficiency and detector performance at elevated temperatures.

Beyond device-level implementations, there's work by researchers at Regensburg University, the Ioffe Institute, Poland's Institute for High-Pressure Physics, and the Rzhnev Institute of Semiconductor Physics. Together, they examined symmetry-dependent transitions and photogalvanic effects in HgCdTe. This effort – relying on the underlying understanding of light-matter interaction and electromagnetic field distribution that underpins our modelling approach – shows that the impact of our original framework extends beyond device design into broader optoelectronic physics.

Taken together, these developments show that the research community is increasingly adopting electromagnetic field engineering as a primary strategy for improving infrared detector performance. The foundation for these investigations is the concepts introduced in our work.

Towards HOT detectors

Where the plasmonic enhancement may have the

biggest impact is in high-operating-temperature (HOT) infrared detectors. At the system level, even modest improvements in absorption, resulting from the introduction of plasmonic nanostructures, may diminish cooling requirements, trim power consumption, and simplify architectures. For aerospace and defence platforms, where size, weight and energy budgets are tightly constrained, these gains could deliver an impact that's well beyond the improvement in the detector itself. For example, the thinner absorber architectures that have a reduced cooling demand also offer a superior detector uniformity and an improved long-term stability. In addition, thanks to a reduced material volume, there can be a reduction in thermally activated noise sources and mitigation of mechanical stress introduced during repeated temperature cycling. For large infrared focal-plane arrays, these gains contribute to improved pixel-to-pixel consistency and reduced calibration overhead.

From a systems engineering perspective, if absorbers maintain a strong performance while operating closer to ambient temperature, this simplifies packaging requirements and broadens deployment options. Thanks to these advantages, detectors can be integrated into platforms where space, weight, and power constraints previously limited infrared capability.

Future directions

One promising direction that builds on our work is to integrate plasmonic nanostructures with advanced detector architectures, including multi-layer designs and hybrid photonic systems. There's also the possibility of combining nanophotonics with computational optimisation techniques, and exploring increasingly large design spaces more efficiently.

Our plans include examining the behaviour of plasmon-enhanced HgCdTe structures under low-temperature operation, where changes in free-carrier concentration strengthen local field confinement and boost absorption efficiency. In parallel, we intend to investigate alternative transparent conducting oxides with higher carrier densities, such as fluorine-doped cadmium oxide and copper-doped aluminium oxide. These oxides should extend plasmonic enhancement across a broader range of operating conditions.

There's also the possibility of turning to machine-learning-assisted design frameworks, which may accelerate identification of optimal nanostructure configurations and enable faster development cycles and improved detector performance. Taken together, these advances could position plasmonic HgCdTe detectors as a promising platform for next-generation infrared sensing technologies.

Ultimately, the engineering of infrared detectors will evolve, due to the convergence of plasmonics, advanced materials, and electromagnetic design.

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- N. Vanamala *et al.* "Geometric optimisation of plasmonic nanostructures on HgCdTe" *AIP Advances* **10** 065006 (2020)

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AI accelerates power design

By slashing the time it takes for electro-thermal simulations of wide-bandgap devices by a factor of more than 5,000, a new physics-informed graph neural network is unlocking rapid structural optimisation and SPICE parameter extraction

BY LI ZHENG, XINHONG CHENG AND COLLEAGUES FROM SHANGHAI INSTITUTE OF MICROSYSTEM AND INFORMATION TECHNOLOGY, CHINESE ACADEMY OF SCIENCES

THERE'S MUCH in favour of a relentless push towards higher power densities in modern electronics. Gains on the front save space, thanks to smaller footprints, and may trim weight. What's more, there's the opportunity for product miniaturisation, faster charging rates, and lower operational costs.

Holding the key to realising higher power densities are wide-bandgap semiconductors, in particular GaN and SiC. Introducing these devices in place of silicon incumbents delivers a hike in efficiency. However, this goes hand-in-hand with formidable challenges associated with thermal management.

When devices fail under stressful conditions, such as short-circuits, the fundamental weakness is often related to a thermal phenomenon. Due to this, accurate electro-thermal analysis is non-negotiable for reliability.

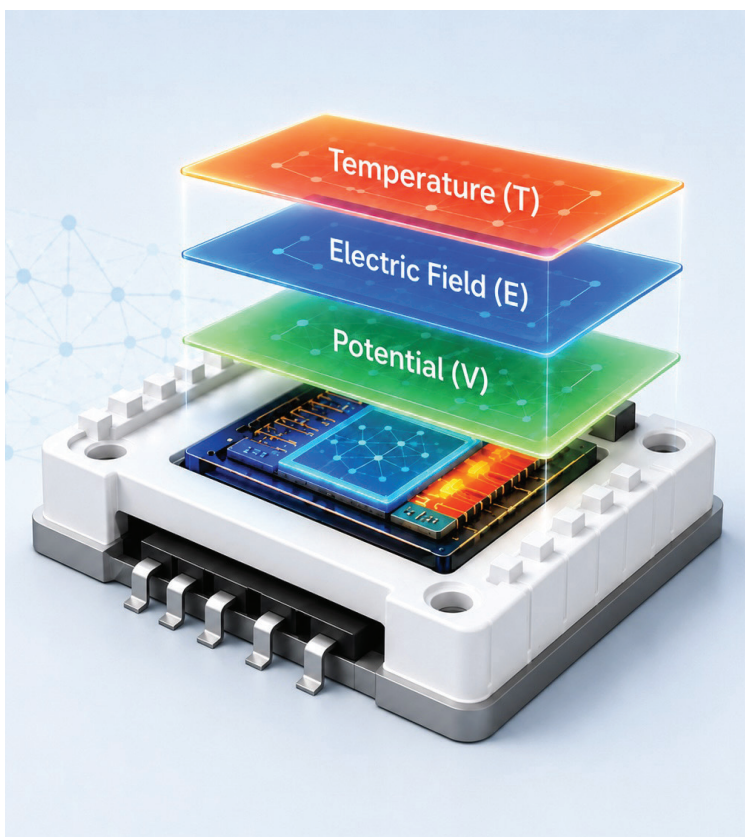
Unfortunately, traditional simulation methods are painfully slow, creating a bottleneck in the design cycle. Every iteration can cost days of computational time. This delay is a severe impediment to progress: it stifles innovation, it forces designers to rely on approximations, and it limits exploration of optimal device structures and accurate system-level models. Given these issues, there's an urgent need for a paradigm shift that will equip design engineers with the opportunity to maintain high-fidelity physics without suffering from crippling computational overheads.

The modelling challenge

One of the weaknesses of conventional electro-thermal analysis, which is typically performed with finite element methods (FEM), is that it struggles with multi-scale complexity. Due to this, simulating an entire power die that contains thousands of parallel cells is prohibitively expensive. So, engineers are often forced to settle for simplified, less accurate models.

It's not overstating the issue to claim that this gap between detailed device physics and system-level circuit simulation is a major hurdle. It should also be noted that when designing critical structures, such as field-limiting rings for high-voltage devices, an iterative trial-and-error process must be adopted, consuming vast amounts of engineering time and resources. What's clear is that the need for a unified, fast, scalable modelling framework has never been more acute.

Overcoming this challenge is critical in applications that pursue higher efficiencies and power densities. For instance, in electric vehicle traction inverters and data centre power supplies, power modules



have a compact layout, making thermal interactions extremely complex. When traditional simulation tools are employed to deal with problems associated with ‘system-level’ electro-thermal coupling, they fall far short of what’s required. They are either insufficiently accurate, or they require computation times spanning weeks, a timescale utterly incompatible with agile development cycles. Due to these severe limitations, many in academia and industry have a shared goal: the development of a method that delves into the microscopic structure of a device while rapidly deducing the macroscopic thermal behaviour of an entire chip, or even a module.

AI solution

Our team is offering a powerful solution, which marries deep learning with fundamental physics: the Physics-Informed Graph Neural Network (PIGNN). This framework represents a device’s mesh – that’s the digital grid used for simulation – as a graph. Points are nodes, and their connections are edges.

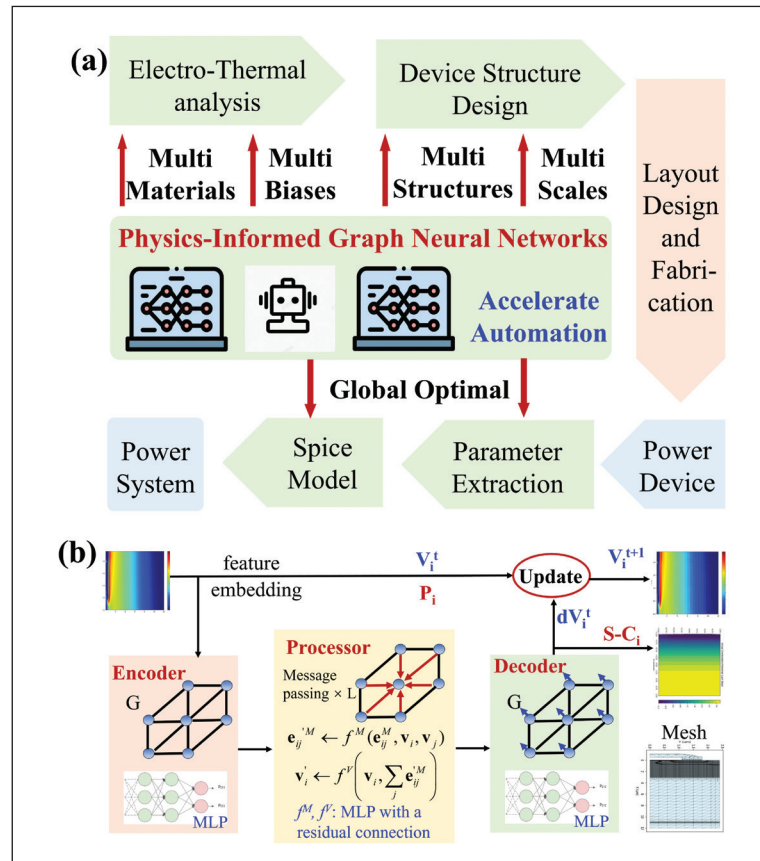
The innovation in our approach lies in how we train this network. It learns not just from the data generated by traditional simulators, such as Sentaurus, but by directly incorporating the governing physical equations into its learning process. So, our network draws on Poisson’s equation, and those for carrier continuity, drift-diffusion and heat conduction. By incorporating a physics-informed approach, our model respects the underlying laws of nature, and makes robust predictions, even for conditions not explicitly seen during training.

The core advantage of PIGNN is the flexibility of its ‘graph structure’, combined with the constraints of ‘physical information’. The graph structure is naturally suited to representing irregular meshes and non-uniform material distributions, a strength that enables seamless handling of multi-scale geometries, from nanometre-scale channels to millimetre-scale substrates. Thanks to an embedding of physical equations, predictions are not based on mere data fitting, but result from physically consistent reasoning. With this design, after the model has been trained on one device structure and a range of operating conditions, it may be generalised to accommodate new geometries and bias voltages through its ‘transductive learning’ capability. Accomplished without retraining, this vastly expands the application scope.

Speed and accuracy

Our performance gains are transformative. According to benchmarking, the PIGNN framework can predict both static and transient electro-thermal responses over 5,000 times faster than conventional Sentaurus FEM simulations. Crucially, this speed is not at the expense of an inferior accuracy. When predicting short-circuit thermal transients, our model maintains an error below 1.5 percent.

This combination of speed and accuracy completely



➤ Figure 1. (a) A universal PIGNN modelling framework as a AI Accelerated model for E-T analysis, structural parameter auto-design of power devices and global optimal extraction of spice parameters. (b) The PIGNN model adopts a supervised encoder-processor-decoder framework, encoder converts grid data into a graph, processor updates node/edge embeddings through L message-passing layers and decoder extracts node features.

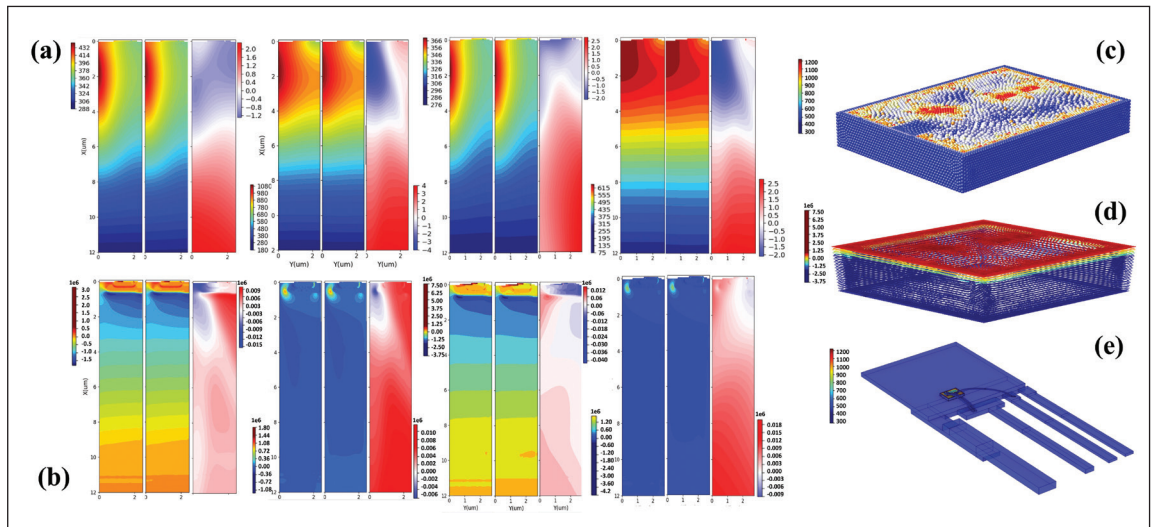
redefines the boundaries of design exploration. Previously, engineers, constrained by time, may have evaluated just a few dozen design variants. Now, by leveraging PIGNN’s rapid inference capability, they can screen and optimise thousands of structural parameter combinations within hours, uncovering optimal ‘sweet spots’ overlooked by traditional methods. As well as pushing the performance limits of the final product, this transformation significantly enhances the foresight and reliability of the design process.

Designing with AI

The true power of this accelerated model comes from its application to real-world design problems. We have demonstrated this strength by automating the design of field-limiting rings (FLRs) for a GaN vertical power device. Within the PIGNN framework, ring spacing and width have become learnable parameters. We tailored the model’s loss function to maximise the breakdown voltage by optimising electric-field uniformity.

After training, our AI-based approach has proposed an optimised FLR structure with a breakdown

► Figure 2. PIGNN's multi-scale modelling for a SiC short circuit. (a) Cell-level temperature under different bias at various times. (b) Cell-level electric field components. (c) (d) Temperature, electric-field distribution across the die. (e) Temperature characteristics of the packaged device.



voltage of 2000 V. Subsequent validation in Sentaurus provided excellent agreement, proving the framework's capability as a powerful design accelerator that can converge to reliable, high-performance solutions.

This process mimics and dramatically accelerates the decision-making of a seasoned engineer. Rather than blindly attempting changes with every iteration, our AI model intelligently adjusts structural parameters based on feedback from physical laws (via partial differential equation loss) and guidance from performance objectives (via custom loss). This model 'understands' how changing the width of one ring affects the electric field profile across the entire depletion region. Based on these changes, the model seeks a global optimum.

More diverse design tasks can be pursued with this approach, such as termination structure optimisation, the best cell layout for reduced thermal coupling, and even the exploration of novel voltage-withstanding structures.

Universal parameter extraction

As well as supporting structural design, our framework bridges the gap to circuit simulation. We are able to perform global optimisation for SPICE model parameter extraction for both SiC MOSFETs and GaN HEMTs. By treating device terminals as a graph, and incorporating temperature as a global node, the PIGNN can learn a unified set of SPICE parameters, valid across a wide temperature range that spans -40°C to 125°C.

Results with this approach show excellent, non-piecewise fitting of key capacitance curves, and highly precise replication of DC output characteristics. This demonstrates that we can thus provide circuit designers with accurate models derived directly from physics.

To fully appreciate the extent of this success, be aware that the traditional parameter extraction methods tend to rely on piecewise fitting for

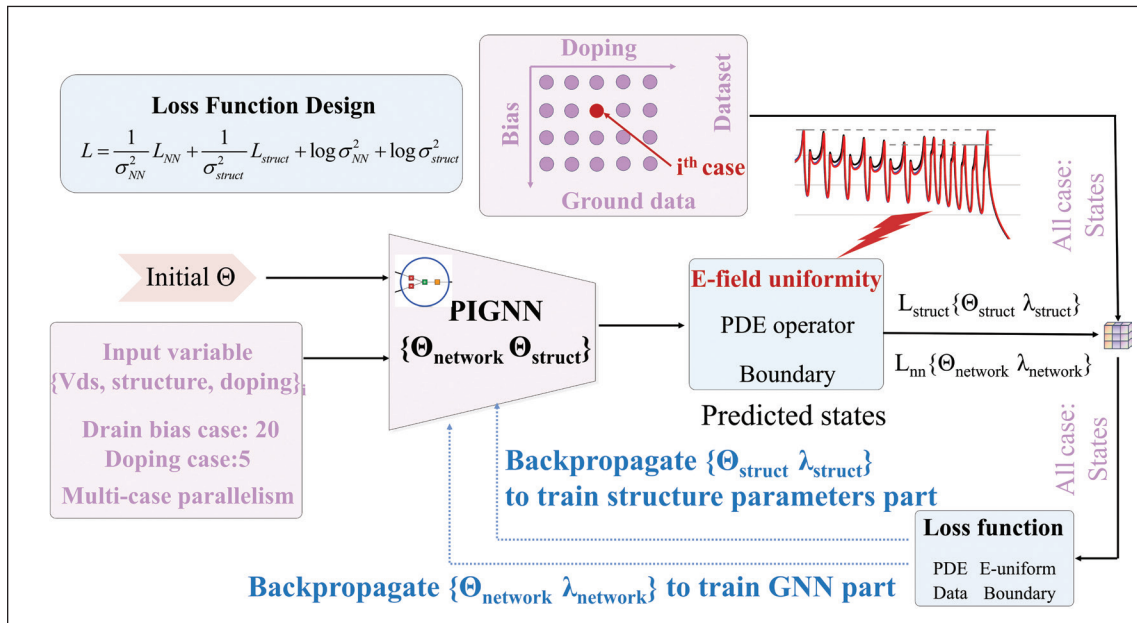
specific operating points, where parameters lack physical correlation. This weakness leads to model inaccuracies during extrapolation, or under extreme conditions.

Our framework is fundamentally different. It unifies a device's internal physics with its external terminal characteristics through the graph model. The parameter set extracted via a single global optimisation inherently reflects the device's intrinsic physical mechanisms. Consequently, the resulting SPICE model is not only accurate within the training data range, but exhibits higher credibility when predicting complex switching transients or thermal coupling effects never directly tested.

Stable and scalable

With any optimisation system, a critical concern is stability. Does the system reliably converge to a good solution? We have rigorously tested the robustness of our PIGNN framework, by evaluating it from 25 different sets of initial parameters, for both the FLR design and SPICE extraction tasks.

Encouragingly, our framework demonstrates robust convergence every time, proving its suitability for automated design workflows. What's more, while traditional FEM simulation time scales linearly with problem size, our trained PIGNN model maintains inference times on the order of seconds, regardless of scale, enabling full-die thermal analysis, a task previously considered impractical. This stability and scalability pave the way for building 'digital twins' and enabling 'real-time health management'. One can imagine a future where a critical power module has a virtual model based on PIGNN that updates synchronously with its physical counterpart. The system controller could use this ultra-fast model to predict internal hot spots and stress distributions in real-time, based on actual operating conditions. It's an insight that opens the door to proactive adjustment-control strategies, which extend lifespan or prevent failure. This marks a leap in reliability design from *post-facto* verification towards real-time predictive maintenance.



► Figure 3. Schematic of PIGNN-based device design: Structural parameters are incorporated as learnable variables, with Electric-Field uniformity of rings added to loss function for global optimisation.

Future enabled

Our work is not simply showcasing an incredibly speedy simulator; it offers a new methodology for power device engineering. By integrating multi-scale physics with the adaptive learning capability of graph neural networks, we have created a tool that dramatically accelerates the two most time-consuming phases of development: device structural optimisation and compact model generation. Our AI-accelerated framework promises to shorten design cycles, enable more innovative device architectures, and improve the reliability of next-generation power electronics by making high-fidelity electro-thermal analysis a practical part of the iterative design process.

Looking ahead, the potential of this framework goes far beyond silicon-based and wide-bandgap power devices. Its core idea – the integration of physical equations with graph neural networks – is transferable to the design and modelling of multi-physics coupled systems, such as photonic devices, MEMS sensors, and even bio-chips. As chip integration continues to increase and heterogeneous integration technologies advance, design complexity is growing exponentially. The co-design paradigm, using physics as a guide and AI as an acceleration engine, is emerging as the key to confronting this challenge and unleashing the full potential of next-generation semiconductor technologies. Our work is a solid step towards that future.

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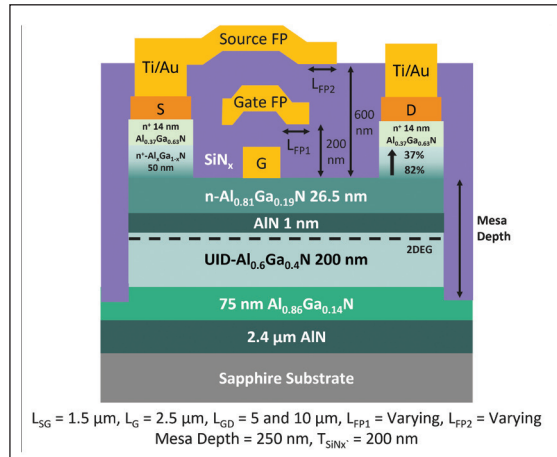
A new benchmark for AlGaN-on-sapphire HEMTs

Electric-field engineering delivers a three-fold hike in the key figure of merit for AlGa_N-on-sapphire HEMTs

ENGINEERS from the University of Wisconsin-Madison are claiming to have produced passivated AlGa_N-on-sapphire HEMTs that combine impressive breakdown fields with a record Baliga's figure of merit.

According to the team, their field-plated $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ HEMTs can withstand up to 2.33 kV, and have a Baliga's figure of merit of 654 MW cm^{-2} . This latter metric, calculated by squaring the breakdown voltage and dividing that figure by the on-resistance, is more than three times higher than the previous best for AlGaIn-on-sapphire HEMTs.

- Record-breaking AlGaN-on-sapphire HEMTs feature SiN passivations and source and gate field plates.



The engineers point out that the performance of the latest HEMTs even surpasses that of their previous devices produced on bulk AlN. Success is attributed to careful electric-field engineering.

When discussing the pros and cons of different foundations for the HEMT, spokesman for the team, Khush Gohel, remarked: “Bulk AlN substrates can provide better thermal conductivity and a higher-quality epitaxial structure, but the lack of large-diameter substrates – 6-inch and 8-inch – makes AlN unsuitable for scaling the technology in the near future. Substrate cost is a particularly strong driver in the power semiconductor industry, which is highly cost-sensitive, so for now, the gain from AlN doesn’t justify the cost.”

Gohel and co-workers produced their devices by loading AlN-on-sapphire templates into an MOCVD reactor and depositing an AlGaIn heterostructure with an *n*-doped Al_{0.81}Ga_{0.19}N barrier, included to increase the electron concentration in the two-

dimensional electron gas channel (see Figure for details of the epistructure).

Fabrication of the HEMTs included metal deposition, etching, passivation and the addition of field plates. These transistors have a gate length of 2 μm , a source-to-gate spacing of 1.5 μm , and a device width of 100 μm . Gate-to-drain distances varied from 5.5 μm to 10.3 μm , the length of the first field plate ranged from 0.5 μm to 2.0 μm , and the source field plate dimensions varied from 1.0 μm to 2.5 μm .

According to Gohel, on-state characteristics of the team's HEMTs are approaching the performance of GaN-based transistors. But they are not quite there yet, mainly due to lower electron mobility in AlGaIn and the difficulty of achieving a high average electric field in the gate-drain access region.

For devices with a breakdown voltage more than 2 kV, on-resistance is 8.3 mΩ cm². Commenting on the latter, Gohel remarked: “I believe this can be improved significantly by reducing channel sheet resistance and improving field spreading, which would allow us to block the same voltage with a smaller gate-to-drain spacing.”

When measuring breakdown voltage, the team immersed their HEMTs in Fluorinert FC-40 to suppress premature air breakdown. Higher breakdown fields resulted from the addition of two field plates, which are claimed to spread the field in the gate drain access region.

A HEMT with a 1 μm gate field plate and a 2.5 μm source field plate produced the most impressive results – a breakdown voltage of 2334 V and an average breakdown field of 2.26 MV cm^{-1} .

Gohel says that as the critical field for $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ exceeds 10 MV cm^{-1} , there's "clear room" to improve the spreading of the electric field in the gate-drain access region.

“As for passivation, we’re still investigating its role, along with material quality and processing effects, since several factors beyond the field plate design likely limit the breakdown field, and we don’t yet have a complete picture of their individual contributions.”

Plans for the team include a further reduction in on-resistance, while simultaneously optimising the electric field in the gate-drain access region. “We also want to shift focus toward the device’s dynamic performance, rather than just its static/DC characteristics.”

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Terbium-doped AlGaN eyes microLED displays

Full-colour, monolithic displays from microLEDs could be realised by turning to the ultra-stable electroluminescence of terbium-doped AlGaN LEDs

RESEARCHERS from The University of Osaka and Ritsumeikan University are claiming to have provided the first demonstration of electroluminescence from terbium-doped AlGaN-based LEDs.

This breakthrough could aid the development of monolithic microLEDs for displays, according to Shuhei Ichikawa from The University of Osaka.

Ichikawa points out that as conventional microLEDs rely on inter-band transitions, the emission colour is fixed after epitaxy – and the production of a full-colour display requires either a stacking of multiple emission layers or a lateral arrangement of sub-pixels.

“A major advantage of this terbium-doped AlGaN light-emitting diode is its ability to generate four colours solely through terbium-ion emission, eliminating the need for the complex integration structures typical of conventional microLEDs.”

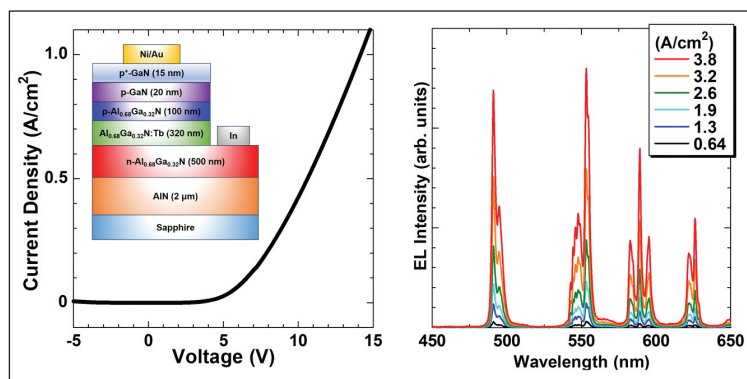
Production of the team’s devices began by forming AlGaN-on-sapphire heterostructure in a Taiyo Nippon Sanso SR-200 MOCVD reactor. Devices were fabricated with terbium-doped layers with AlGaN compositions of $\text{Al}_{0.36}\text{Ga}_{0.64}\text{N}$, $\text{Al}_{0.53}\text{Ga}_{0.47}\text{N}$, $\text{Al}_{0.59}\text{Ga}_{0.41}\text{N}$ and $\text{Al}_{0.62}\text{Ga}_{0.38}\text{N}$.

It is claimed that high-volume production of these devices would be no more challenging than that of conventional LEDs. “The terbium metal organic precursor has a melting point in the range of 40-80°C; by controlling the bottle temperature, it can be maintained in a liquid state and used for bubbling in the same manner as conventional precursors,” argues Ichikawa.

According to secondary ion mass spectrometry, the terbium concentration in the active region slightly decreases from $2.0 \times 10^{19} \text{ cm}^{-3}$ to $1.5 \times 10^{19} \text{ cm}^{-3}$ as the aluminium content increases.

External quantum efficiency (EQE) of these novel emitters increases with aluminium concentration – it is just over 10 times higher for $\text{Al}_{0.62}\text{Ga}_{0.38}\text{N}$ than $\text{Al}_{0.36}\text{Ga}_{0.64}\text{N}$. While an increase in aluminium concentration degrades the electrical properties, Tb^{3+} emission is much stronger, due to enhanced energy transfer from the alloy to the dopant.

These LEDs produce incredibly stable electroluminescent emission peaks at around 620 nm, 580 nm, 550 nm and 490 nm, due to $^5\text{D}_4 - ^7\text{F}_j$ ($j = 3, 4, 5, 6$) transitions.



➤ With the addition of the terbium dopant, AlGaN LEDs produce sharp electroluminescent peaks at around 620 nm, 580 nm, 550 nm and 490 nm.

One option for realising single-colour emission from terbium-doped LEDs – a critical requirement for making full-colour displays – is to place bandpass filters over the devices. However, this is viewed as impractical, as it limits EQE. According to Ichikawa, a far better solution is to control the branching ratio: “Fortunately, the emission of all four visible colours is governed by the relaxation process from the same excited state of the terbium ion – the $^5\text{D}_4$ state.”

There is a strong possibility that a single emission colour can be made to dominate, argues Ichikawa, by shortening the radiative lifetime. This could be accomplished by coupling a specific emission wavelength, with architectures involving plasmon resonance or resonant cavities. “It is known that in materials like terbium-doped glass, green emission becomes the dominant component.”

Efforts must also be directed at increasing EQE. Values for the latest devices are below 0.01 percent.

“Our group has already achieved a peak EQE approaching 10 percent with europium-doped GaN red LEDs; similarly, we anticipate significant EQE improvements in terbium-doped AlGaN through the optimisation of crystal growth conditions,” says Ichikawa.

He points out that with europium-doped GaN, the breakthrough came with co-doping with oxygen atoms. “I believe that developing a co-doping technique using different impurities will be the crucial factor for terbium-doped AlGaN as well.”

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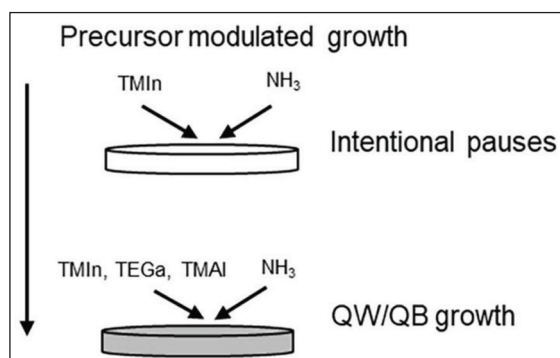
Precursor-modulated wells boost the efficiency of UVA LEDs

LEDs emitting at 380 nm combine low droop with an efficiency exceeding 40 percent

RESEARCHERS at the University of California, Santa Barbara (UCSB), have improved the performance of UVA LEDs through the growth of precursor-modulated quantum wells.

The team's low-droop devices, emitting at 380 nm with an efficiency above 40 percent, support development of solid-state sources for a number of applications, including i-line photolithography, industrial curing, and quantum technologies. LEDs provide an attractive alternative to the incumbent source of UV emission, the mercury lamp, as they are smaller, have a superior energy efficiency, and a longer operational lifetime.

➤ Modulating the growth of the active region improves the performance of UVA LEDs.



One weakness of LEDs emitting in the UVA – that's the spectral domain from 315 nm to 400 nm – is the bandstructure, which features InGa_N quantum wells with a relatively low indium composition, typically 5 percent. Due to this, offsets between conduction and valence bands are smaller than those in blue LEDs, leading to inferior carrier confinement. Compounding this issue, UVA LEDs are more sensitive than their blue-emitting cousins to interface quality.

To address both issues, the team from UCSB have drawn on earlier work involving AlGa_N LEDs. "We found that the growth pause during the temperature ramp of quantum well growth could noticeably affect device performance, although the underlying mechanism was not fully understood at that stage," remarks team spokesman Yifan Yao. "This motivated us to investigate the effect of precursor modulation more systematically in UVA LEDs."

Yao and co-workers produced their devices by loading Ga_N-on-patterned-sapphire substrates into an MOCVD chamber and growing an epistructure featuring a 3 μm-thick *n*-type Ga_N buffer layer, a 200 nm-thick

n-type Al_{0.06}Ga_{0.94}N layer, an active region with two quantum wells, a 15 nm-thick Al_{0.2}Ga_{0.8}N electron-blocking layer, a 300 nm-thick *p*-type Al_{0.06}Ga_{0.94}N layer, and a 15 nm-thick *p*-type contact layer.

When an active region is grown with a conventional approach, layers are deposited continuously, and there are no extended pauses. But in this work, there are intentional growth pauses. Between the growth of the well and the barrier there's a pause for 8 minutes under a nitrogen gas ambient, with flows of just ammonia and a small amount of indium.

"The time was optimised for best device performance and repeatability," remarks Yao. "We tried to pause for a shorter time, like 30 seconds or 1 minute, but this effect is less noticeable on device performance."

During on-wafer electroluminescence measurements, the UVA LED with an active region grown with precursor modulation produced three times the output power of a reference device, grown conventionally. The more powerful device also suppressed broad defect luminescence and had a narrower emission linewidth, thanks to improved carrier confinement.

To investigate the compositional fluctuations across the active region, the team employed scanning transmission electron microscopy energy-dispersive X-ray spectroscopy. This uncovered an aluminium-enriched interfacial layer, roughly 2 nm-thick, formed at well-barrier transitions.

The team also produced top-emitting LEDs with sides ranging from 300 μm to 20 μm. Sidewalls were passivated by dielectric layers.

These devices exhibit a size-dependent droop that decreases with dimensions, due to reductions in localised heating and current crowding.

According to pulsed measurements with a 1 percent duty cycle, packaged 40 μm devices produce a peak external quantum efficiency above 41 percent, and maintain a value of 40 percent up to 200 A cm⁻².

Yao says that the efficiency and the optical power of these devices are good enough for typical uses in many applications, including photolithography, curing, and photocatalysis.

Recently, the team applied its precursor modulation technology to the growth of laser diodes. This work will soon be published.

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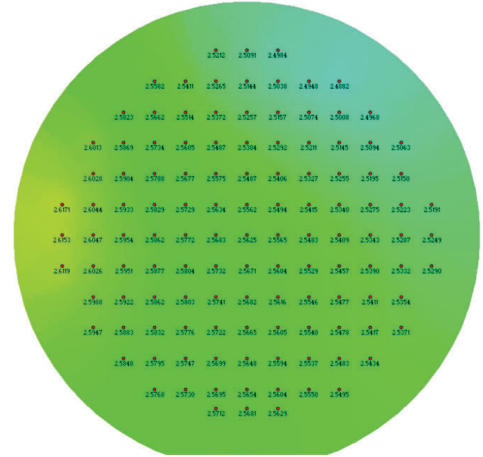
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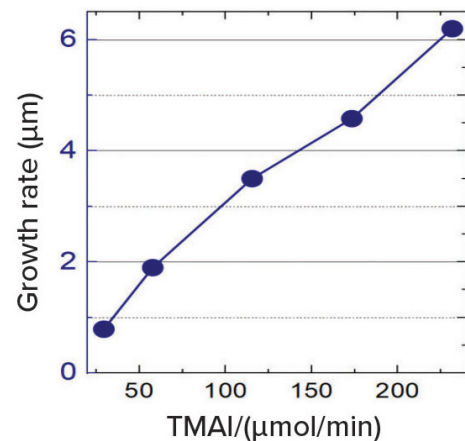
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