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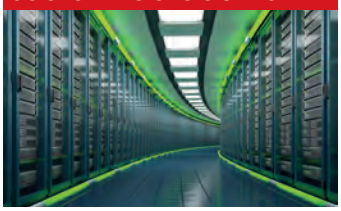
SiC: Evaluating the MOSFET and the IGBT

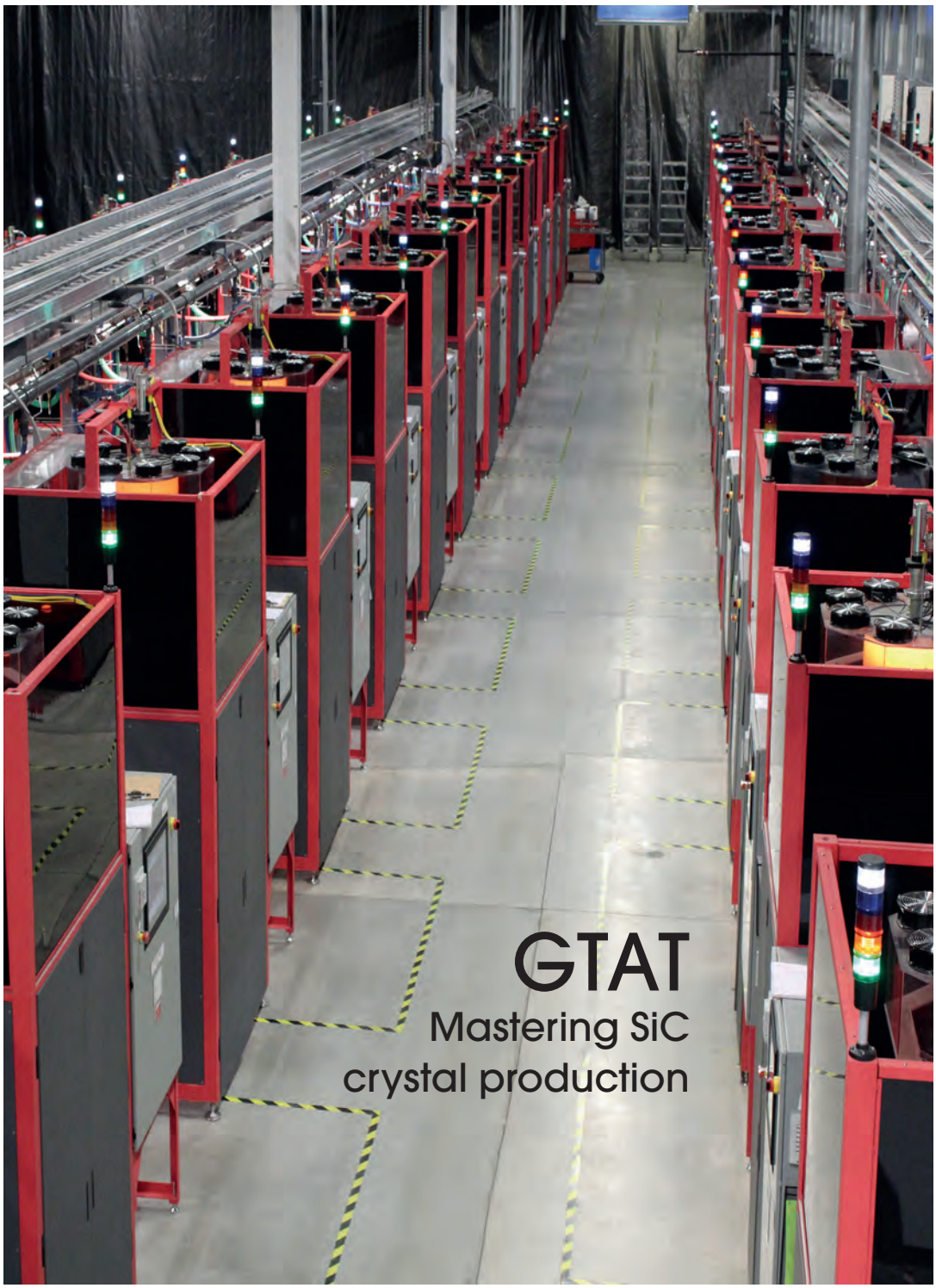
GaN HEMTs offer a new level for linearity

Cubic GaN garners glorious green LEDs

Surface-emitting superluminescent LEDs

Joint venture delivers scale in datacoms





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Mastering SiC crystal production

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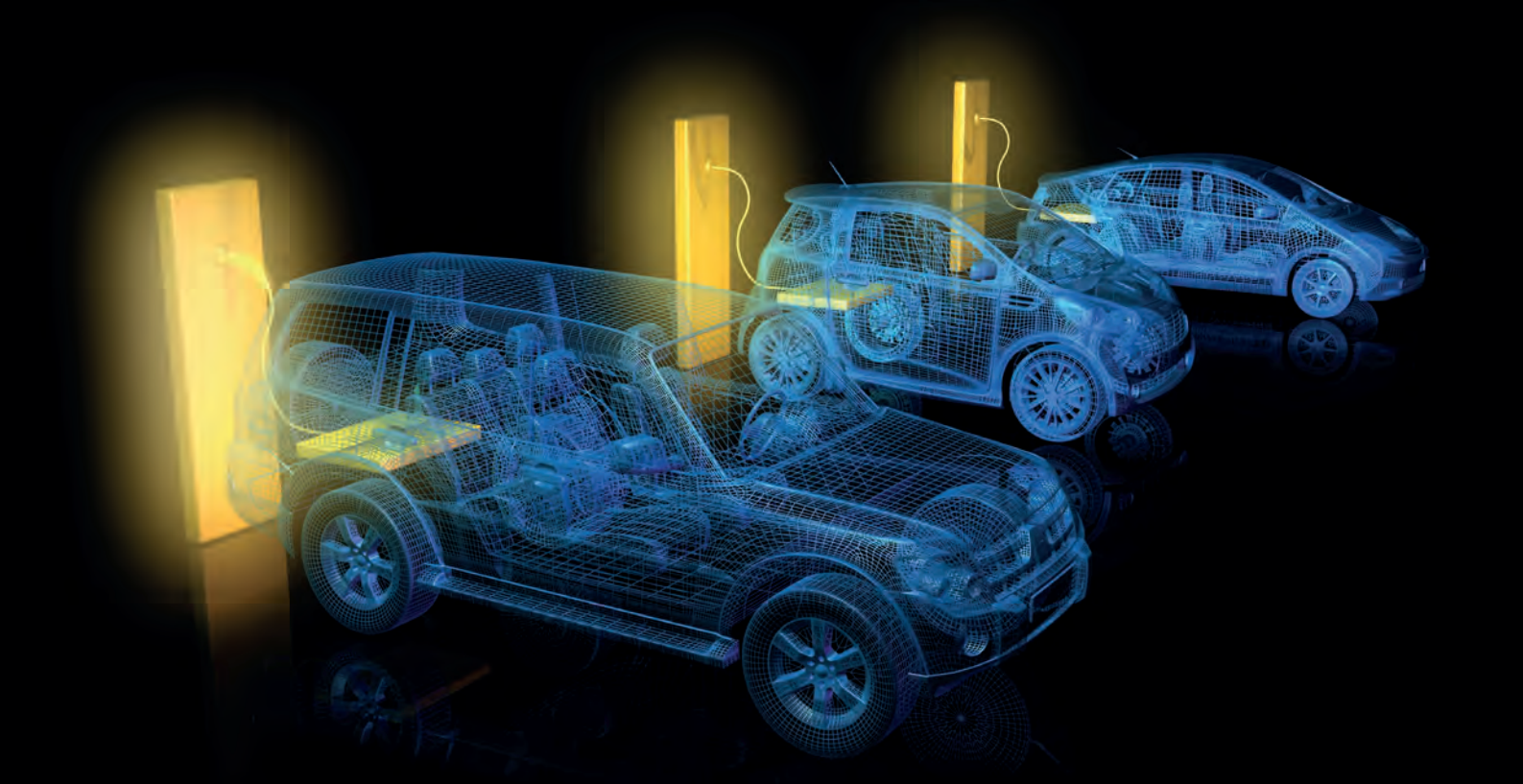

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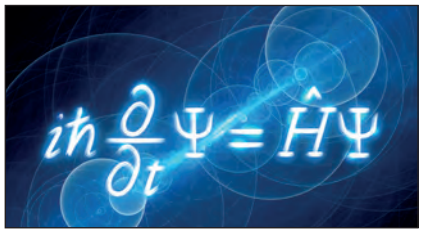
Viewpoint

By Dr Richard Stevenson, Editor

Getting the best out of GaN

INTERNAL ELECTRIC FIELDS found in conventional III-Nitrides are a blessing and a curse. By pulling apart electrons and holes in quantum wells, they inhibit radiative recombination; but by allowing a high-quality two-dimensional electron gas to form at an interface between AlGaN and GaN, they are key to the operation of the GaN HEMT.



In the pages that follow, we look at a handful of approaches that impact these fields and deliver improvements to a range of devices.

For more than a decade researchers have been investigating semi-polar and non-polar planes, as they quash or eliminate internal electric fields in GaN LEDs and laser diodes. The foundation for these devices are miniature pieces of GaN that command astronomical prices.

To slash the price of real estate for light emitters with reduced internal electric fields, a team from China has produced a portfolio of GaN-based semi-polar active regions on pattered sapphire (see p. 58). Encouragingly, wells emitting at around 460 nm have an internal quantum efficiency exceeding 50 percent.

An alternative approach to combatting these internal electric fields is to switch from conventional to cubic GaN. Developing LEDs of this ilk is Kubos Semiconductors. This spin-off of the University of Cambridge starts with a silicon substrate and adds a layer of SiC that provides a foundation for subsequent growth of cubic GaN (see p. 42). This form of GaN has two major assets: it has a narrower bandgap than conventional GaN, making it easier to produce bright LEDs that address the green gap; and it is free from internal electric fields, allowing the growth of wider quantum wells that provide efficient recombination while minimising Auger recombination, a cause of LED droop.

When it comes to GaN HEMTs, internal fields are cherished, helping to create devices with unprecedented efficiencies and power densities in the RF. But the two-dimensional electron gas has a flaw: adjustments to gate bias alter electron density, in turn changing the velocity of this charge carrier and ultimately the gain of the transistors. Variations in gain degrade linearity, a much-needed characteristic in 5G networks. One way to address this, pursued by a partnership between researchers at Qorvo and The Ohio State University, is to turn to a three-dimensional gas, formed by grading (see p. 34).

Such efforts, plus those on semi-polar planes and involving cubic GaN, show that we are only just starting to unlock the full potential of this material.

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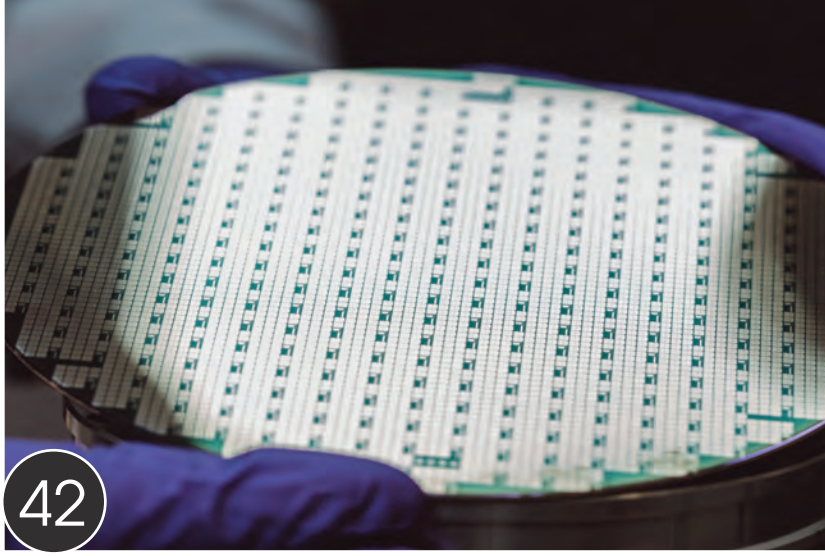

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SemiNex laser diode enables 250 m range LiDAR

SEMINEX CORPORATION has announced a patent-pending, multi-junction, semiconductor laser diode at eye-safe wavelengths between 1310 nm and 1550 nm. According to the company, the laser diode has more than 20 times the photons/second and over three times the range of 905 nm LiDAR systems.

The new laser diode enables autonomous LiDAR systems to reach greater than 250 m. Present solutions limit visibility to 100 m, requiring a vehicles speed to be at 25 mph or less.

For the past ten years LiDAR manufacturers have taken two laser approaches for time-of-flight LiDAR systems: 905 nm laser diodes or 1550 nm fibre lasers. The 905 nm laser diodes suffer from limited range due to eye-safety regulations and the 1550 nm fibre lasers are impractical for mass-market deployment because of their size and cost. Until now, there was no solution that offered the low-cost, small size, and efficiency of 905 nm laser diodes with the eye-safety and extended range of 1550 nm fibre lasers.

"The SemiNex multi-junction laser diode changes everything," states Ed McIntyre, SemiNex director of sales and marketing. "Now there is a low-cost, long-range, eye-safe alternative to 9XX nm diodes and 1550 nm fibre lasers."

"The SemiNex multi-junction laser diodes will allow vehicles to autonomously navigate at higher speeds that can't be achieved with the existing technology; this could finally enable driverless cars to be a reality within the next five years," adds McIntyre.

The multi-junction laser diode is a drop-in replacement for most compact laser drivers used for existing 9XX nm diode systems. It makes use of three monolithic solid-state laser junctions that produce 80 watts at 1550 nm with 95 μm aperture width and yield more than three times the power of current laser diodes at this wavelength. Product samples are available immediately and the multi-junction is ready for immediate high-volume production.

Typical time-of-flight LiDAR systems using multi-junction 905 nm lasers are limited to a range of 100 m due to eye safety acceptable emission limits of International Electrotechnical Commission regulations, thus limiting their use to niche applications such as private security systems, warehouse automation, and limited-use public driving functionality.

"SemiNex invested three years in research and development to create a long-range and cost-effective solution to overcome the short-range limitations of existing technologies. We see this as a major game changer and believe it will revolutionise the way major LiDAR companies approach this challenge," said David Bean, CEO of SemiNex Corporation.

Today, the LiDAR market for automotive and industrial applications is expected to be $981 million and limited to short-range applications. However, with improvements in technology and broader acceptance, the market is expected to grow to $2.8 billion by 2025.

A major challenge with the existing LiDAR technology for autonomous vehicles has been to find a cost-effective semiconductor laser diode that can provide high peak power at eye-safe wavelengths for long range applications. The SemiNex device can be operated at pulse widths between 2 ns and 100 ns at 200 kHz to 400 kHz pulse repetition rate.

The multi-junction device is available in double and triple junction configurations in various packaging and submount configurations. Samples in either TO-9 or bare die configuration at 1550 nm are available for immediate delivery.

LiDAR: dropping prices and low volumes

LiDAR has seen a massive price drop in the past three years according to market research consultants Yole Développement. However, it's not the result of mass-production, because volumes have not grown significantly and mass adoption of LiDAR is yet to happen. Instead, it's due to the strategies of different companies.

In this complex and rapidly evolving environment, Yole's analysts predict that the LiDAR market for automotive and industrial applications will be $1.7 billion in 2020. Growth is expected to be 19 percent. Yole's forecast is a revenue of $3.8 billion in 2025.

Automotive applications are expected to be the main driver for LiDAR in the next five years, providing $1.8 billion growth between 2019 and 2025. With several partnerships between LiDAR manufacturers and car manufacturers, Yole expects 3.2 percent of personal cars to adopt LiDAR by 2025.

The impact of robotic cars on LiDAR will be modest due to lower deployment of robotic cars than once expected.

LiDAR for personal cars could also be jeopardized. The Covid-19 crisis is putting financial pressure on car manufacturers. Regulations imposing reduced carbon emissions are pushing investments towards electrification.

Finally, the ambition of Tesla to rapidly achieve autonomous cars without LiDAR could make LiDAR less essential in the coming years.

Alexis Debray, technology and market analyst, MEMS, Sensors & Photonics at Yole says: "A new trend in the LiDAR business appeared a few years ago, which might dramatically change the shape of the LiDAR market, namely dropping prices. Velodyne has announced a plan to reach an average unit price of $600 by 2024, from $17,900 in 2017".

Chinese LiDAR companies, which usually have LiDAR unit prices one-fifth of that of other companies and usually below $1,000, are gaining market share and expanding their business. LiDAR with lower unit prices is expected to enter new industrial applications including factory, logistics and security. However, because of lower LiDAR unit prices, the industrial segment is expected to have moderate growth between 2019 and 2025, expanding from $390 million to $567 million.

"LiDAR technologies could be adopted for most robots and smart facilities", says Pierrick Boulay, technology and market analyst, Solid-state Lighting at Yole Développement.

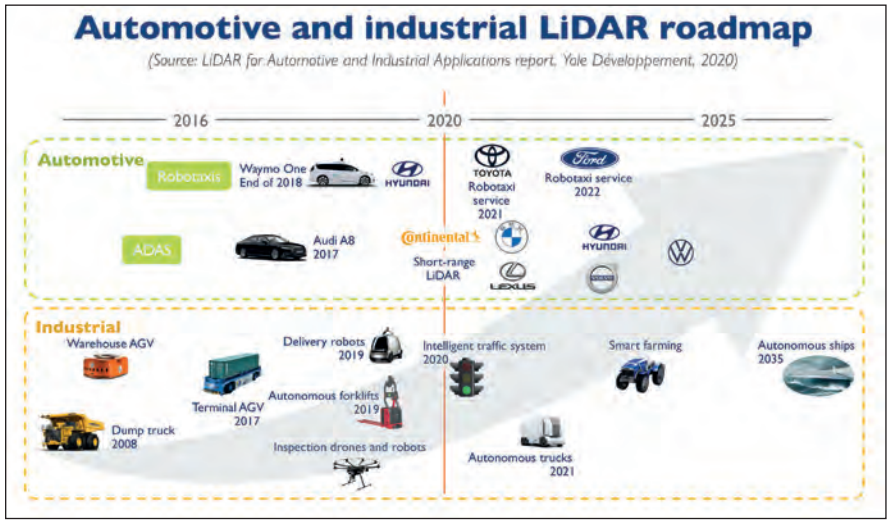
Since the 2005 DARPA Grand Challenge, vehicles have been a major application for 3D real-time LiDAR. In 2017, Audi equipped some of its cars with the Valeo Scala, a long-range LiDAR. At the end of 2018, Waymo launched Waymo One, its robo-taxi service equipped with its own mid-range and long-range LiDAR. Continental has announced short-range flash LiDAR for 2020. Aimed at ADAS cars, it could also equip robo-taxis or even industrial platforms. Other LiDAR manufacturers that have partnerships with car manufacturers, such as Innoviz, Velodyne and Luminar, are targeting long-range applications.

As a key player in the LiDAR industry, Hamamatsu has developed photodiodes and lasers for Livox's Horizon LiDAR. According to Sylvain Hallereau, project manager Integrated Circuits, Power Semiconductors and LEDs at System Plus Consulting and author of the *Hamamatsu Photodiode and Laser in Livox's Horizon LiDAR* report: "LiDARs are manufactured around four main components: the pulsed laser diode, avalanche photodiodes, opto-mechanical system (to scan the environment in front of the car), and the processor".

The Livox LiDAR sensing module includes a custom six-photodiode array die from Hamamatsu, specifically developed for LiDAR applications. The photodiode dies are assembled in a package with a 905 nm narrow-bandpass filter.

Industrial applications of LiDAR have a longer history, with topographic applications dating from 1970s. This business is well-established and operated by large companies, explains Yole in its 2020 LiDAR report. Mining applications started to develop in 2008 with Komatsu and Caterpillar offering autonomous dump trucks. Their positions as solution and service providers have helped them operate these fleets.

Recently, many new industrial applications have been emerging for LiDAR, including warehouse AGVs, terminal AGVs, delivery robots and drones, autonomous forklifts, inspection robots and drones, intelligent traffic systems, security and soon to come autonomous trucks and smart farming. Yole announced a 31 percent volume CAGR between 2020 and 2025 for logistics and other industrial applications.



SETi and Seoul Viosys ramp UV LED production

SENSOR ELECTRONIC TECHNOLOGY, INC. (SETi) and Seoul Viosys, providers of UV LED technology and subsidiaries of Seoul Semiconductor, have started mass production of UV LED modules designed to sterilise 99.9 percent of the coronavirus in 3 seconds using Violeds, a UV LED technology developed by Seoul.

Seoul Viosys is also developing a Photon Shower device that applies the UV LED technology to contribute to the safety of medical staff and patients who have been struggling amid the Covid-19 pandemic.

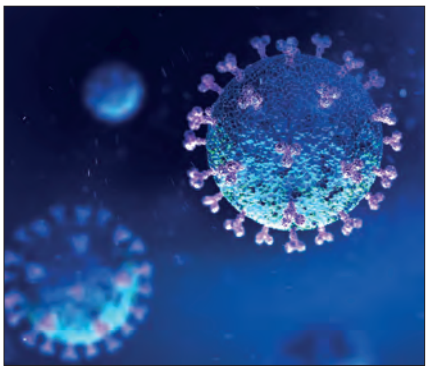
The BIO research team at Seoul Viosys has conducted numerous research and development projects with in-house laboratories, cultivating and sterilising various bacteria and viruses.

In April 2020, a Violeds sterilisation test conducted with a research group at Korea University demonstrated that Violeds sterilises coronavirus.

The Photon Shower device is a whole-body sterilisation solution that uses only light to sterilise various germs on the surface of peoples' clothing in seconds. This sterilisation function can also be added to conventional air shower devices, which are used for dust removal only. The Photon Shower using Violeds technology is expected to contribute to minimising infections in hospitals in the future. According to the US Centers for Disease Control and Prevention statistics, more than 14,000 people die annually from hospital infections in the US alone.

"There are countless industrial fields where the Violeds UV LED module, which sterilises 99.9 percent of viruses on the surface of everyday objects in just three seconds, can be applied," said Mike Berens, director of sales for SETi. "It has been supplied to US escalator manufacturers to be applied to escalator handle sterilisation solutions, and we expect global customer demand to increase in the future."

Violeds is a UV LED technology jointly developed by SETi and Seoul Viosys through more than 20 years of research and development. It uses only light to sterilise, and can be optimally designed depending on the application by considering the following five factors:



wavelengths from 200 nm to 400 nm, distance to objects, light irradiation time, brightness of light (intensity), angle, and area of the irradiation surface.

This technology has already been applied to the International Space Station of the National Aeronautics and Space Administration (NASA), and is also applied to various home appliances and automobiles, including air conditioners, air purifiers, water purifiers and dishwashers.

Applying this technology, Seoul Viosys is also producing an air purifier, designed to filter and sterilise 99.9 percent of bacteria and virus particles in 30 seconds.

AMF and DenseLight develop optical engine with integrated InP lasers

ADVANCED MICRO FOUNDRY (AMF), a silicon specialty foundry and DenseLight Semiconductor, an InP laser provider with its own InP MOCVD technology and wafer fab in Singapore, have entered into a Memorandum of Understanding (MoU) to develop silicon photonics solutions with integrated lasers.

The data traffic within data centres is projected to grow rapidly over the next five years due to an economy increasingly relying on online solutions and the deployment of 5G technology. This will lead to a higher demand for high-speed data centre interconnect. Silicon photonics (SiP) technology is uniquely placed to support these requirements and silicon-photonics based solutions started being deployed to support the transition from 100G to 400G.

However, silicon photonics chips for these applications require the subsequent attachment of an InP based external laser light source and the challenges associated can impact the final optical performance and cost of the interconnects. By joining forces, AMF and DenseLight are combining their respective expertise in silicon photonics manufacturing and laser development to develop an integrated 'low loss – low cost' SiP optical engine with integrated laser light source.

Rather than off-the-shelf modules with a limited range of specifications, the companies will focus on the development of laser-on-chip integration solutions that can be applied directly onto customer PIC designs. The solutions will then be offered through the pure-play foundry services of AMF with DenseLight's matching laser integration as part of the AMF Process Design Kits.

The availability of such made-to-order turnkey SiP optical engine solutions with integrated light sources will contribute to lower assembly costs and shorten development cycle times of transceivers (400G/800G) and fibre sensing products.

Patrick Lo, president of AMF mentioned that "for the first time, two Singapore companies are working together to locally develop unique solutions that will promote the widespread adoption of silicon photonics by the data communication industry and by other emerging technologies".

"This MoU creates a unique partnership between two synergistic Singapore based companies to deliver turnkey SiP-based solutions to both datacom and fibre sensing customers. Our proprietary DPHI technology enables the integration of InP-based photonics devices to SiP platforms for efficient light coupling into waveguides" said Rajan Rajgopal, president and CEO of DenseLight.

STMicroelectronics pioneers smaller, faster chargers

STMICROELECTRONICS, a global semiconductor leader serving customers across the spectrum of electronics applications, has unveiled MasterGaN, the world-first platform embedding a half-bridge driver based on silicon technology along with a pair of GaN transistors.

The combination will accelerate the creation of next-generation compact and efficient chargers and power adapters for consumer and industrial applications up to 400 W.

The company's in-house GaN technology enables these devices to handle more power even as they become smaller, more lightweight, and more energy efficient. These improvements will make a difference for smartphone ultra-fast chargers and wireless chargers, USB-PD compact adapters for PCs and gaming, as well as in industrial applications like solar-energy storage systems, uninterruptible power supplies, or high-end OLED TVs and server cloud.

Today's GaN market is typically served by discrete power transistors and driver ICs that require designers to learn how to make them work together for best performance.

ST's MasterGaN approach bypasses that challenge, resulting in faster time to market and assured performance, together with a smaller footprint, simplified

assembly, and increased reliability with fewer components. With GaN technology and the advantages of ST's integrated products, chargers and adapters can cut 80 percent of the size and 70 percent of the weight of ordinary silicon-based solutions.

"ST's market-unique MasterGaN platform builds on our proven expertise and power-design skills to combine high-voltage smart-power BCD process with GaN technology, to accelerate the creation of space-saving and power-efficient products that are kinder to the environment," said Matteo Lo Presti, Executive VP and General Manager Analog Sub-Group, STMicroelectronics.

ST is launching the new platform with MasterGaN1, which contains two GaN power transistors connected as a half bridge with integrated high-side and low-side drivers.

MasterGaN1 is in production now, in a 9 mm x 9 mm GQFN package only 1 mm high. Priced at $7 for orders of 1,000 units, it is available from distributors.

An evaluation board is also available to help jump-start customers' power projects.

SMI and SUNY Poly partner on DoE GaN project

STRUCTURED MATERIALS INDUSTRIES (SMI) has been awarded a Phase I Small Business Technology Transfer Research contract by the US Department of Energy to develop manufacturing infrastructure for GaN qualified for vehicle power electronics. The project is in partnership with the State University of New York Polytechnic Institute (SUNY Poly).

SMI and SUNY Poly researchers will address issues related to the production of uniform quality GaN materials on large area substrates (4 inches and beyond). They will also design and develop power devices that will perform at currents of more than 20 A and voltages exceeding 600 V for electric drive vehicle electronics.

SMI's focus will be developing novel reactor concepts to increase the GaN material quality/uniformity across large wafer sizes. SUNY will use reactor technology to optimise materials and device structures on 4-inch substrates. SMI will help with the commercialisation of both device and reactor technology.

Shahedipour-Sandvik, SMI's partner at SUNY Poly, an expert in growth of III-N materials and device fabrication, was the first to report enhancement operation in AlGaN/GaN HEMTs. The SUNY Poly team has recently reported on a novel integrated body-diode AlGaN/GaN HEMT power device that enables dynamic tuning of V_{on} and substantially reduces I_{off} current.

Principal investigator and SMI research scientist, Arul Arjunan, commented: "We are designing a concept MOCVD system to improve the yield and quality of GaN devices for vehicle power electronics."

"The concept system will lead to the growth of films with both thickness and quality uniformity. In addition to this, we will aim to improve the quality of the film to achieve better devices than that currently existing. The success of this programme will increase the efficiency of the hybrid electric and electric vehicles".

In Phase I the team will demonstrate GaN power devices at the 100 mm wafer scale, which can operate at >600 V and > 10 A. (The Phase I reach goal is >20 A and >600 V).

At the end of the Phase I programme, the team will define the product scale-up pathways for 100 mm, 150 mm and 200 mm wafer production and packaged device production in addition to firming up potential customers.

"SMI's team is very happy to be contributing to the advancement of nitride power technology", said SMI's president and CEO, Gary Tompa, adding: "Improving power efficiency and lowering costs will help bring greater numbers of more environmentally friendly vehicles to market sooner."

In the past, SMI has worked on several different III-N funded research programs and has built tools for research and development of III-Nitrides.

NXP opens GaN fab in Arizona

NXP SEMICONDUCTORS has opened an 150 mm (6-inch) RF GaN fab in Chandler, Arizona. The new factory, which will support the expansion of 5G base stations and advanced communications infrastructure, is thought to be the most advanced GaN fab for RF in the US.

The opening ceremony was marked by keynote addresses and remarks by NXP executives plus federal, state and local government officials. In his keynote address, Kurt Sievers, NXP CEO said: "Today marks a critical milestone for NXP. By building this incredible facility and tapping key talent in Arizona, we are able to bring focus to GaN technology as part of driving the next generation of 5G base station infrastructure."

NXP has nearly 20 years of GaN development expertise and extensive wireless communication industry knowledge. The company has optimised its GaN technology to improve the electron trapping in the semiconductor to deliver high efficiency and gain with high linearity.

Joakim Sorelius, head of development Unit Networks at Ericsson, a longstanding NXP customer, commented: "We strive to deliver industry leading products that provide maximum value to our customers, where power amplifiers play an important part of the radio technology. Similar to Ericsson's recent US investments, we are pleased to see NXP's investments in the US semiconductor process development with the continuous focus on improving RF system performance for future high-demanding radio networks. I am excited by the opening of our new facility in Chandler as it underscores NXP's decades-long commitment to GaN and the communications infrastructure market," said Paul Hart, executive VP and GM of the Radio Power Group at NXP.

"I would like to thank our customers for their collaboration throughout the years and the entire NXP team that has been instrumental in creating the world's most advanced RF GaN fab, which is designed and ready to scale to 6G and beyond."

The fab is set to ramp quickly with NXP using its Chandler-based team and their long-standing expertise in compound semiconductor manufacturing. Arizona Governor Doug Ducey added: "With this new state-of-the-art manufacturing facility in Chandler, Arizona is set to expand its reputation as a high-tech manufacturing hub and a pioneer in 5G innovation. We're grateful to NXP for bringing more jobs and investment to our state."

The internal factory will serve as an innovation hub that facilitates collaboration between the fab and NXP's onsite R&D team. NXP engineers can now more rapidly develop, validate and protect inventions for current and future generations of GaN devices, resulting in shorter cycle times for NXP GaN innovations.

NXP's new Chandler-based GaN fab is qualified now, with initial products ramping in the market and expected to reach full capacity by the end of 2020.

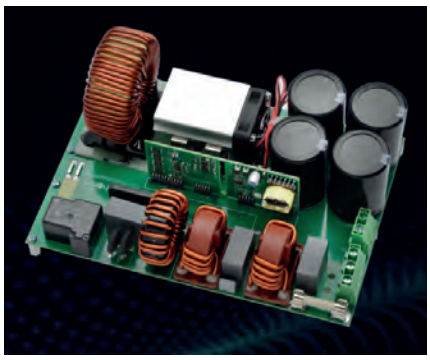
Transphorm releases new 4 kW eval board

TRANSPHORM has announced availability of its newest evaluation board, the TDTTP4000W065AN. Designed for single-phase AC-to-DC power conversion up to 4 kW, this board uses the bridgeless totem-pole power factor correction topology with a traditional analogue control.

This pairing provides fast and easy access to the top-notch conversion efficiency made possible by Transphorm's latest SuperGaN FETs without the need for firmware development required when using digital signal controllers.

Maintenance power – power required to support basic functionality such as powering up and supplying chipsets – is a relatively fixed amount in any system. Therefore, as an application's power level decreases, the maintenance power becomes a larger percentage of the system's overall power loss.

When compared to a DSP solution, Transphorm's analogue board requires lower maintenance power at the onset, thereby increasing overall system efficiency, according to the company.



For engineers requiring more design flexibility, Transphorm released the TDTTP4000W066C earlier this year. This DSC-based 4 kW AC-to-DC board also uses the bridgeless totem-pole PFC with the company's SuperGaN FETs. However, it integrates a dsPIC33CK DSC board from Microchip that has been pre-programmed and is backed by dedicated firmware support.

"Transphorm's analogue evaluation board provides an unprecedented opportunity to access our highly efficient GaN in the easiest way possible. Much like the preceding digital board, it gives power system engineers a choice that the high-voltage device market was previously lacking," said Philip Zuk, VP of worldwide technical marketing and North American sales, Transphorm. "Regardless of the end application's targeted value proposition, we have the diverse toolset and the most robust GaN possible to help you succeed."

The TDTTP4000W065AN employs Transphorm's SuperGaN Gen IV TP65H035G4WS FETs in the board as the fast-switching leg with low-resistance silicon MOSFETs in the slow-switching leg. The resulting performance is similar to that of its digitally controlled counterpart, the TDTTP4000W066C.

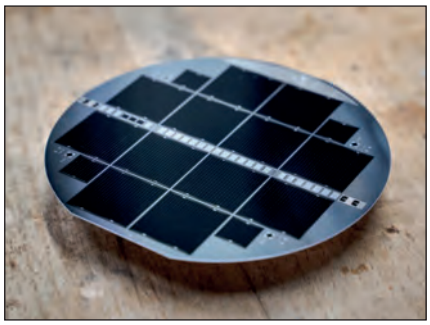
The TP65H035G4WS is a 650 V device with a 35 mΩ on-resistance in a TO-247 through-hole package with an inherently high thermal dissipation ability. This feature eliminates the need to parallel devices for higher power output; a design method required by competitive surface-mount GaN solutions. And, as with all other Transphorm GaN devices, the SuperGaN FETs can be driven with a threshold voltage of 4 V and standard off-the-shelf gate driver operating from 0 to 12 V.

Aixtron and partners continue to push tandem cell efficiencies

AIXTRON has announced its involvement in a project that has so far achieved an efficiency of 25.9 percent with a multi-junction solar cell grown directly on a silicon substrate.

This figure was achieved by researchers at the Fraunhofer Institute for Solar Energy Systems ISE in close cooperation with the Technical University of Ilmenau, the Philipps University of Marburg and epitaxy experts at Aixtron SE, as part of the funded MehrSi project.

"For the first time we have now been able to realise a tandem solar cell based on a silicon wafer with such high efficiency," comments Dietmar Schmitz, VP corporate technology transfer at Aixtron. Until now, the production of III-V multi-junction solar cells has been based on a more expensive substrate material, such as a compound semiconductor material.



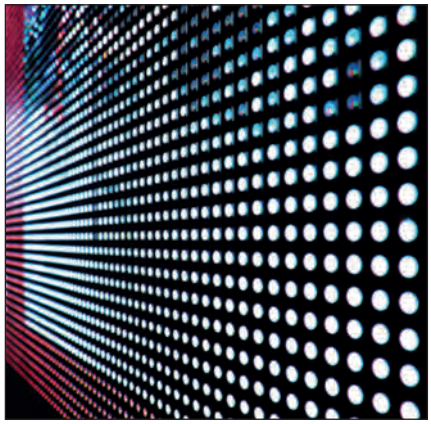
Schmitz explains what is special about this basic research: "The gallium and phosphorus atoms must occupy the correct lattice positions at the interface with silicon. To achieve this, we have to control the atomic structure very well. This requires exceptionally high precision."

"In addition, to achieve the necessary high quality of the epi-wafers, it is crucial that a high crystal quality of all layers is achieved during epitaxial growth. This was achieved in the project thanks to the improved system technology developed by Aixtron and the good cooperation with the project partners".

Now the alliance partners are working to further increase efficiency and reduce manufacturing costs. To this end, the deposition of the layers is to be realised even faster, with higher throughput and thus more cost-optimised. In addition, the efficiency of the solar cells is to be further improved.

"Specifically, the dislocation density in the III-V solar cell layers is to be reduced from 10^8 cm^{-2} to the range of 1-5 x 10^6 cm^{-2} in order to increase the efficiencies to more than 30 percent. And last but not least, the cost-effectiveness of the epitaxy processes is to be further optimised," explains Michael Heuken, VP corporate R&D at Aixtron.

Samsung to galvanize growth of mini LED backlight TVs



AT THE MOMENT, TV brands are focusing on 4K resolution and OLED displays as the primary selling points in their high-end product strategies.

However, Samsung is hoping to increase the market share of its QLED TVs, which are much more cost-competitive than OLED TVs, via the integration of mini LED backlights, which can significantly raise the level of contrast and image detail through multiple dimming zones in addition to its WCG (wide colour gamut) capabilities.

TrendForce indicates that Samsung's lineup of mini LED backlight TVs in 2021 will include 55-inch, 65-inch, 75-inch, and 85-inch display sizes, 4K resolution, and multiple mini LED local dimming zones, which produce contrast ratios of 1,000,000:1, a significant improvement over the current market mainstream of 10,000:1. Since such high contrast ratios are only possible if the display backlight contains at least 100 local dimming zones, the corresponding number of mini LED chips used for backlighting will skyrocket as well, with between 8,000 and 30,000 mini LED chips used for each TV.

By combining high-resolution display panels and multiple local dimming zones, Samsung's mini LED TVs are set to deliver a superior visual experience for the end-user.

The upcoming release of Samsung's mini LED TVs will inject considerable momentum into the LED supply chain.

Samsung's new mini LED backlight TVs are expected to feature HV LED chips as their light source. Thanks to their mini LED backlights, these TVs deliver improved display performances via dimming ratio and WCG functionalities.

Samsung's adoption of HV LED chips requires an extremely large-scale, fast, and stringent testing and sorting process for LED chips according to chip wavelengths and specs, and related companies such as San'an Optoelectronics, Epistar/Lextar, FitTech, Saultech, Apex, and Macroblock have all moved to participate in Samsung's mini LED supply chain. TrendForce believes that, although most of the above companies are still currently in the sampling stage without any finalised contracts, competition in the LED supply chain will likely intensify once again.

Osram LEDs ensure greater safety when driving

IN A FEW YEARS, LEDs will be the predominant light source in car headlights, according to Osram Opto Semiconductors. Their compactness, brightness and energy efficiency in particular are major advantages over conventional technologies.

Osram Opto Semiconductors has been working on its LED solutions for the automotive sector, with significant leaps in performance in the Oslon Black Flat and Oslon Compact product families.

It is also launching a new generation of one to four-chip versions in the Oslon Compact PL range. Like their predecessors, the ceramic components have an electrically insulated pad that makes it much easier to dissipate heat from the package.

As a result, a higher current is possible, which allows the one-chip version to achieve a high brightness value of 395 lumens at 1A with a chip area of 1mm^2. Thanks to the very small dimensions of 1.9 mm x 1.5 mm x 0.73 mm, the product is suitable for ADB (Adaptive Driving Beam) systems and in space-saving designs.

In addition, the Oslon Black Flat S family expands to include a one and a two-chip version. The special lead-frame-based components feature highest contrast values (>1:200) and very low thermal resistance – which allows for higher currents. The one-chip variant reaches 395 lm at 1 A. The square lighting surface of the UX:3 chip makes optical design particularly easy for headlight manufacturers. The different technology concepts of the Oslon Black Flat S and Oslon Compact PL enable customers to choose the best possible combination of LED and PCB for their systems. Due to the product family's high efficiency values of up to 130 lm/W at 1 A, headlights with smaller or even without heatsinks are conceivable in the future – leading to a potential reduction in system costs.

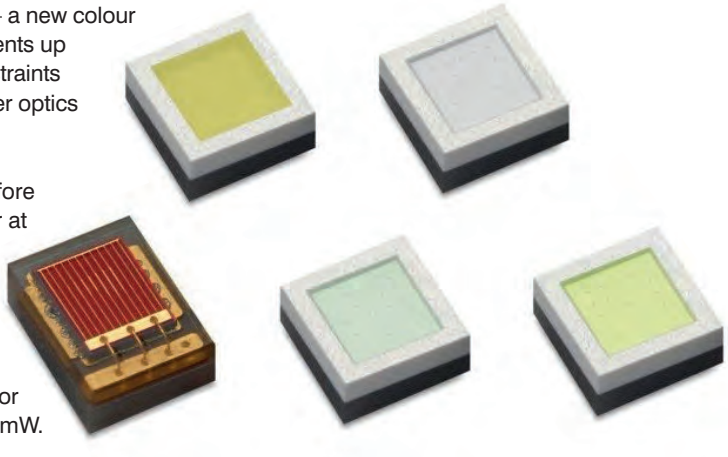
"LEDs such as the Oslon Compact PL and the Oslon Black Flat S will lead to an increasingly high penetration rate in vehicles, including small and mid-sized cars," explains Florian Fink, marketing manager automotive exterior at Osram Opto Semiconductors.

"We always work in close cooperation with our customers to constantly improve our established product families and to push the limits of achievable brightness values even further in future".

The package dimensions remain the same in the new product generations of the Oslon Compact PL and Oslon Black Flat S, which allows headlamp manufacturers to easily exchange the products.

Lumileds releases Luxeon rubix colour LED building blocks

LUMILEDS has released the very small and powerful Luxeon Rubix – a new colour LED building block – designed to deliver maximum flux at drive currents up to 3 A. With Luxeon Rubix, engineers are freed from the design constraints of pre-configured modules and can create custom arrays with smaller optics supporting smaller size luminaires, according to the company.



"Luxeon Rubix introduces a size and power ratio that has never before existed for colour LEDs," said LP Liew, product marketing manager at Lumileds. "Think of Luxeon Rubix as pixel-like – uniquely shaped arrays are possible, optics can be smaller, and exceptionally high light density allows solutions across a broad range of lighting segments to take new forms and increase their value."

Each Luxeon Rubix delivers high flux performance. Typical output for red is 85 lm, green is 310 lm, blue is 112 lm and royal blue is 1635 mW. Typical output for white is 440 lm at 93 lm/W.

IGaN epi centre aims to boost GaN ecosystem in Asia

FOLLOWING successes in customer pilot lines, Singapore-based IGSS GaN, a company focused on GaN-on-silicon/SiC technology, has set up a 4-inch to 8-inch MOCVD GaN Epi Centre which is expected to be operational mid-2021.

The Epi Centre brings together customers, universities, research institutes and tool vendors to collaborate in the future development of GaN technologies as the quality of epiwafers are critical to GaN device manufacturing, according to Raj Kumar, IGaN's CEO and founder of its holding company IGSS Ventures.

IGaN, IGSS Ventures and select partners have invested some $73 million to expand GaN epi production capacity and to mass produce 8-inch GaN fabrication technologies.

"What the industry lacks today is a concerted effort to enhance the overall GaN ecosystem to lower cost barriers so that technology adoption can happen at the pace the market is moving."

"We projected more than nine years' ago that at 8-inch wafer dimensions, GaN-on-silicon capabilities becomes a competitive and powerful solution to create the right balance between superior performances and cost competitiveness," said Kumar.

"A commercial centre and joint lab hosting several top specialist brands and leading vendors is a timely market response to creating strategic partnerships that fast-track innovation, growth, and customer value."

"Capitalising on the recognisable Singapore-brand, second-to-none IPs standards, its known semiconductor infrastructure and IGaN's in-house expertise, I truly believe we can set standards, create benchmarks and lead the global movement in GaN adoption," he added.

Ambitions for the Epi Centre is indicative of the growing excitement in GaN technology that sits at the intersection of power-efficient electronics, AI, 5G and IoT, charging systems/powertrain management, green energy and smart city demands.

Azur Space orders tool from 3D-Micromac

3D-MICROMAC AG, a maker of laser micromachining and roll-to-roll laser systems for photovoltaics, medical devices and electronics, has announced the order of microPRO XS laser system for processing of III–V (GaAs) solar cells from Azur Space Solar Power GmbH based in Heilbronn.

Azur Space is developing III–V (GaAs) solar cells for satellites and terrestrial concentrative solar systems. More than 550 satellites have been equipped with Azur Space cells. The order of the microPRO XS is to increase production.

"During the assessment of different laser systems for our solar cell production, 3D-Micromac's microPRO XS has convinced us with its smart machine concept in combination with the achievable throughput rates," said Jürgen Heizmann, CEO of Azur Space. "We are looking forward to installing this system on our production site."

3D-Micromac's microPRO XS is an adaptable laser micromachining system that is mainly used in industrial manufacturing settings. Due to its high flexibility it is ideally suited for all applications of laser structuring, laser cutting, laser drilling and laser welding.

Depending on the chosen process module and the installed laser source, a variety of materials can be processed.

Axus and CP partner on microLED AR displays

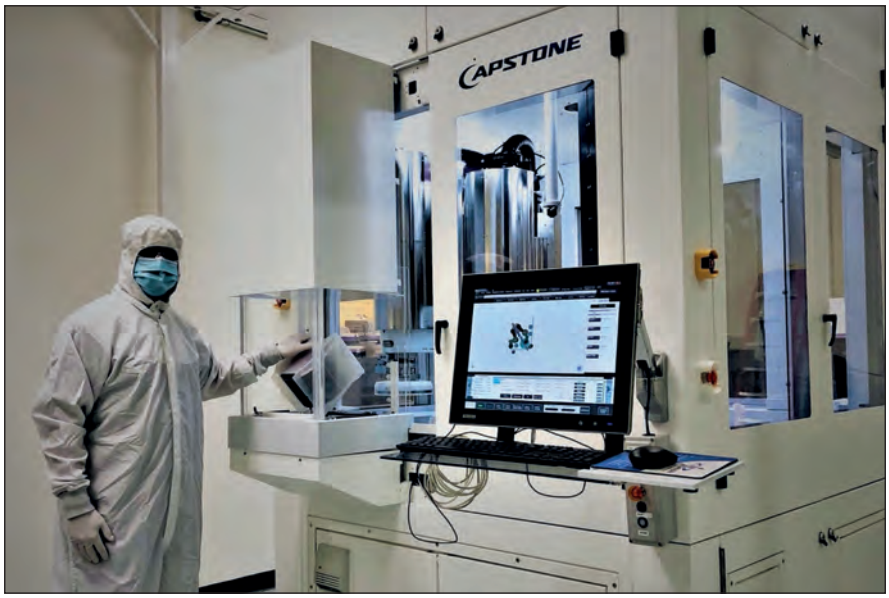
ARIZONA-BASED Axus Technology, a provider of CMP, wafer thinning and wafer polishing surface-processing solutions, has announced a partnership with Compound Photonics US Corporation (also known as CP Display), a provider of microdisplay solutions for augmented and mixed reality (AR/MR), to accelerate sub 5 μm pixel microLED development to the mass market.

Axus and CP will work together to integrate critical wafer-scale processes needed for mass-production scale up of CP's 2 μm pixel, 1080p microLED displays for next-generation AR glasses. Specifically, Axus will deploy its state-of-the-art Capstone CMP system with integrated post-CMP clean to enable wafer planarisation and surface preparation process solutions for successful wafer-scale bonding of microLED wafers to high-performance CMOS backplanes.

To accelerate development, Axus and CP will set up in CP's MicroLED Innovation Center for Augmented Reality Acceleration (MiARA) located in Chandler, Arizona.

The approximately 15,000-square-foot, Class 100 clean room facility provides the infrastructure for Axus, CP and other capital equipment suppliers to conduct advanced process development in Silicon Desert within proximity to global leading semiconductor manufacturers.

Axus's CMP processing capability is said to be key to enabling CP's proprietary, small pixel, epi-substrate agnostic microLED integration process scheme. The Capstone CMP system provides the repeatability over multiple wafers and planarity performance within die/wafer to reliably enable bonding of multiple-million micron scale electrical contacts between microLED and CMOS backplane wafers. This addresses a critical mass-production process requirement for consistently yielding microdisplay modules with required visual uniformity, which is needed for compact, low power, high brightness AR/MR near-eye applications.



Axus and CP have collaborated since early 2020 to develop wafer-scale bonding process integration between microLED array and CMOS backplane wafers.

Dan Trojan, president of Axus Technology, commented: "Given the tremendous growth potential and exciting technological advances associated with microLED development and commercialisation, I'm very pleased that Axus Technology has the opportunity to support many, if not most, of the technology companies working in this area.

"Axus is the leader in CMP-related advanced technology and process innovations to enable microLED and its solutions. With the introduction of our new, state-of-the-art Capstone CMP system, we also now offer the equipment best suited for implementing such processes in R&D, pilot production, and high-volume manufacturing applications. We're thankful for the opportunity to continue, and extend, our relationship and interaction with Compound Photonics, which we recognise as a leader and pioneer in this exciting field."

Peter Wrschka, process technology director of Axus Technology, added: "The synergies between Axus and CP will yield display devices of unprecedented speed and performance. Axus offers years of experience in the surface preparation for wafer bonding and subsequent substrate removal, which is needed to successfully build the next-gen miniature displays. The partnership will significantly shorten the time-to-market for monolithically integrated microLED displays."

Julie Chao, product development Director of CP Display, commented: "We are thrilled to work with Axus to develop CMP and cleaning solutions that enable bonding CP's CMOS backplane to any sub 5 μm pixel microLED wafer. By working together in MiARA, process improvement cycles are naturally accelerated. This is imperative in meeting the market schedule from developers to end customers."

MicroLED is continuing to emerge as the most potential display solution to meet the critical requirements of AR/MR applications.

Innovations in manufacturing process are critical in enabling cost reductions and volume productions for AR/MR headset commercialisation.

Correction: On page 59 of the August / September 2020 edition of *Compound Semiconductor*, it was incorrectly stated that Union Minière is now known as United Materials. Union Minière actually changed its name to Umicore.

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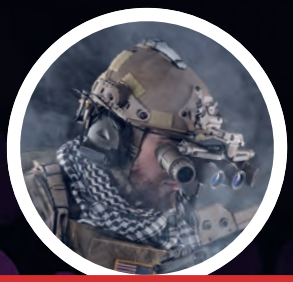


Infrared

Solar

CMOS++

Power

Delivering scale in datacoms

A joint venture between POET Technologies and Sanan IC is set to supply the huge volumes of optical engines that cloud data centres crave, reports Rebecca Pool.

IN LATE JUNE, this year, Canada-based POET Technologies signed a deal with Sanan IC, China, to form a $50 million joint venture that could significantly ease the manufacture of optical engines for datacoms applications.

By combining POET's CMOS-compatible optical interposer platform and Sanan IC's customised lasers and photodiodes, the partners will design and manufacture 100G, 200G and 400G optical engines in large volumes for high-speed datacoms markets.

As POET chairman and chief executive, Suresh Venkatesan, said at the time: "This joint venture has the potential to have a breakthrough in technological innovation as well as product competitiveness... [We will] offer the market the highest performance optical engines at a competitive price."

POET's optical interposer is based on a multi-layer CMOS-based platform. Passive components such as optical waveguides and filters are integrated into the interposer via CMOS processing while active devices such as lasers, detectors, and modulators are aligned and placed within the top layers of the interposer. The platform's lower layers are home to high-speed metal traces that connect with electronics components, such as drivers and processors, enabling high-speed communication between electronic and photonic devices. The optical interposer platform also enables co-packaged optics, essential for higher capacity switches.

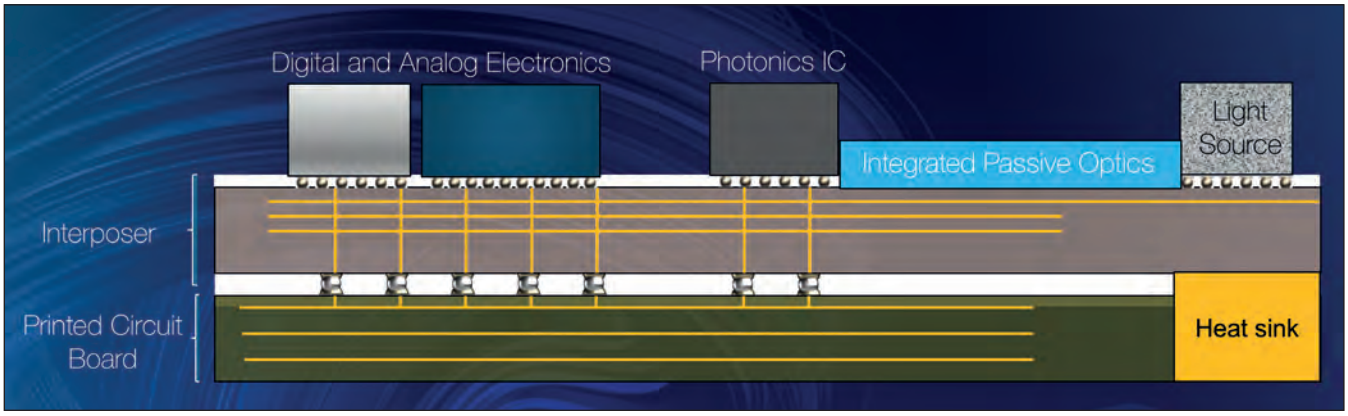
CMOS compatibility allows wafer-scale processing, opening the door to the high-volume manufacture of optoelectronic devices that datacom players are demanding in droves. And herein lies the reason why the POET-Sanan IC venture is such a big deal.

Sanan IC's parent company, Sanan Optoelectronics, is the world's largest manufacturer of LED epiwafers and chips, delivering around 50 percent of all chips. Sanan IC, itself, currently provides dedicated capacity for GaAs and InP epi-growth and epiwafer fabrication on 2,4, 6 and 8 inch platforms.

Earlier this year, the foundry announced it would better serve global optical markets by expanding services to include the manufacture of VCSELs, DFB lasers and other optical communications components. For datacom players, vying to scale data centre operations in line with market growth, this spells good news.

Scale matters

Prior to the SARS-CoV-2 pandemic, POET president and general manager Vivek Rajgarhia and colleagues visited the Sanan IC foundry in the High-Tech Industrial Development Zone of Xiamen, China, and left astounded. "We knew that Sanan IC was the largest compound manufacturer in the world, but their facility certainly had a level of scale that I had never seen before, even from my days at MACOM, Hitachi OpNext (now Lumentum) and Lucent Microelectronics," highlights Rajgarhia.



"The facility contains 400 MOCVD reactors and is making more than 20 million compound semiconductor wafers annually," he adds. "And it is now expanding into RF GaAs and GaN as well as InP optics."

This latest move, which triggered the POET-Sanan IC joint venture, is set to enable the low-cost, high-scale integration of optical engines that lie at the heart of the all-important datacoms transceiver module used in cloud data centres.

As part of the joint venture, POET will supply optical interposers, manufactured by semiconductor wafer fab partner, SilTerra, at its 8 inch foundry in Kulim, Malaysia. Meanwhile Sanan IC will provide lasers, photodetectors and other active devices, which will then be integrated into the optical interposers at the joint venture's facility in Xiamen, to form optical engines.

Along the way, POET has emphasised that none of its optical interposer's fundamental process or design IP will be transferred to Sanan IC during the joint venture. Once the joint venture starts volume production of the optical engines, POET will own 47 percent and Sanan IC will own 53 percent of the equity.

Intellectual property aside, thanks to the set-up's wafer-level processing, POET is confident that the joint venture will slash the labour and materials costs of optical engine manufacture by up to 40 percent, and capital expenditure by around ten times, compared with that required for conventional transceiver sub-assemblies. And of course, this will please potential customers such as Huawei, ZTE, Cisco, Juniper, ADVA, Delta, Innolight and EOptolink, and more, that require ever-greater volumes of optical engines for servicing cloud data centre customers.

"For cloud data centres to adopt our products, we need to provide enough manufacturing scale for our offering to be meaningful," points out Rajgarhia. "The joint venture provides confidence to our end-customers that there is a supply chain with robust scaling – without this, data centre expansion could become limited."

The POET president is also certain that critical optical engine fabrication steps, such as optics alignment and packaging, can take place seamlessly in a volume manufacturing environment. "The joint venture with Sanan IC is a huge endorsement of our technology – we've spent years working on alignment, testing and so on, so know how to do this," he says. "I've seen these optical engines made in a more conventional way and you really do need a lot of patience to watch them being aligned and assembled – it takes time and is very expensive."

So what now for the joint venture? According to Rajgarhia, the current worldwide pandemic hasn't significantly slowed operations, so POET and Sanan IC are busy working on optical engines for customers

that manufacture 100G, 200G and 400G transceiver modules. Potential customers also include system integrators and data centre operators that specify the suppliers and components that make up these modules.

Production of 100G and 200G optical engines is scheduled to be up and running by the third quarter of 2021 for customers around the world. Meanwhile, production of 400G-related products, including light engines and receivers, is set to come online by the end of 2021, with optical engine production following in 2022. Sales of 400G optical engines by the joint venture will be directed at the Greater China Territory.

"We will soon populate a facility in China with the necessary equipment relating to the joint venture," says Rajgarhia. "POET is also opening its own subsidiary in Shenzhen, and is currently looking for talent there."

Cash-wise, the future also looks bright. Based on the number of Ethernet ports shipped and optical transceiver modules sold, POET has calculated the total available market for all optical transceivers to be some $2.5 billion this year, growing to $7 billion come 2025. Of this, the company reckons the joint venture can serve a market worth around $1.5 billion in 2020 and $3.5 billion in 2025, and anticipates associated revenues to exceed more than $250 million in 2024 to 2025.

These figures don't actually take into account POET's activities outside of the joint venture. The company also hopes to expand into other markets including artificial intelligence and 5G telecommunications. Indeed, Sanan Optoelectronics currently has a huge presence in 5G, so this market could be a natural extension for POET and the joint venture.

"In five years' time we'd like to have seen the optical interposer transform the optical industry in the same way that transistors transformed the electronics industry," says Rajgarhia. "This may be a big goal, but that's the impact that we want."

Opening up **SiC substrate** production

A manufacturer of crystal growth equipment pivots to materials manufacturing, creating a more competitive supply chain for the production of SiC power electronics

BY SANTHANARAGHAVAN PARTHASARATHY FROM GT ADVANCED TECHNOLOGIES

SILICON, the most widely used material across the entire electronics industry, has dominated power electronics for decades. But its vice-like grip is slipping. The silicon power devices used in all forms of power conversion – that includes AC-DC rectifiers, AC-AC transformers, DC-DC converters and DC-AC inverters – are struggling to keep up with demands for higher power ratings, faster switching frequencies and elevated operating temperatures. Failing to fulfil these requirements has undesirable implications, as circuits then need additional cooling and take up much more space, because they require large 'passive' components, such as inductors and capacitors.

Addressing all these weaknesses is a portfolio of materials with wider bandgaps, such as SiC. The wider bandgap is a wonderful attribute, delivering multiple benefits. For SiC, the bandgap is three times

that of silicon, providing a breakdown field ten times that of the incumbent (see table 1). Additional merits of SiC devices are efficient switching at far higher frequencies than silicon equivalents, enabling the use of far smaller passives, and a thermal conductivity three times better than silicon. Drawing on all these attributes allows SiC to hold the key to smaller, lighter circuits that are more efficient, handle higher voltages, and have reduced requirements for thermal management.

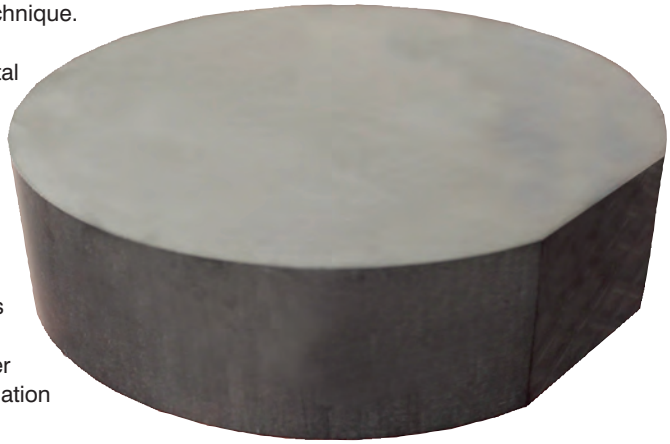
Such circuits are in growing demand as markets and applications push toward the 'electrification of everything'. Although this is most evident in the electric-vehicle industry, which is literally driving the transition from traditionally used silicon-based power electronics to SiC, other industries are also benefitting from this wide bandgap material. They include: power conversion systems featuring in other forms of transport, such as electrified trains, ships and aircraft; renewable energy applications, including solar photovoltaics and wind energy; and industrial/commercial applications, such as power supplies for servers, uninterruptible power supplies for data centres, motor drives and medical imaging systems.

In addition to all of these all-SiC devices, SiC provides the foundation to a variety of devices based on GaN. High-frequency GaN-on-SiC transistors are deployed in 5G telecommunication systems, such as repeater stations; and also in digital TV, radar and optoelectronic devices. In 5G applications, the combination of GaN epilayers and a semi-insulating SiC substrate creates devices that are superior to silicon LDMOS, and deliver increased capacity and coverage. Switching from silicon LDMOS to GaN-on-SiC doubles the number of users per tower and increases data transmission by more than an order of magnitude.

Substrate supply

As awareness of the superior properties of SiC grows, the demand for power electronics made from this material is ramping fast. Only a few companies are meeting this demand by growing high-quality SiC crystals, which begs the question: why aren't SiC crystals produced in volume?

The answer is multifaceted, and relates to the challenges of growing SiC. The wide bandgap material cannot be produced by the melt growth processes used to make boules of elemental semiconductors, such as silicon, which is manufactured by the Czochralski method. That's because a stochiometric melt is not realised under normal conditions. Instead of melting, SiC sublimes at about 2100 °C. For this reason, the growth of SiC requires a vapour-phase crystal growth process – generally a physical vapour transport or sublimation technique.



The fundamental crystal growth steps are essentially the same for vapour growth and melt growth. The process begins by generating reactants, either through sublimation or melting, and

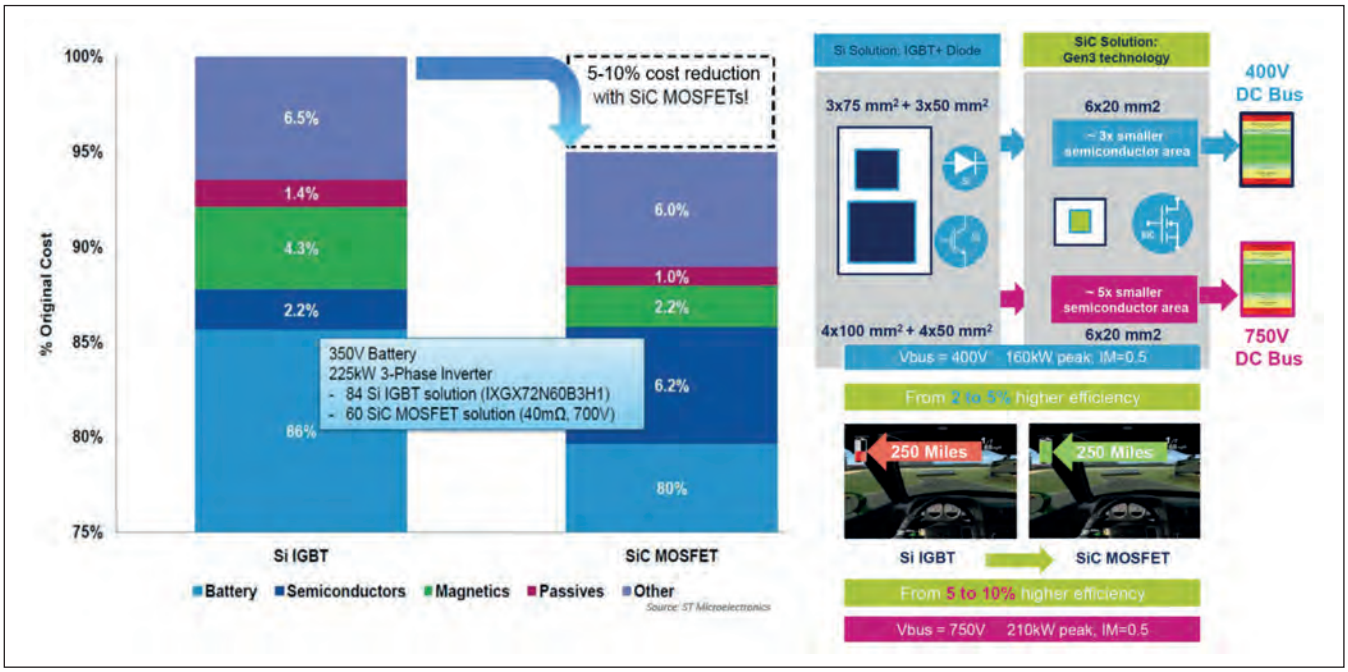


Figure 1. Switching from silicon to SiC offers savings at the system level. Source: ST Microelectronics

transporting them to the growth surface using specific temperature gradients. After this adsorption occurs at the growth surface – known as supersaturation – nucleation takes place, followed by crystal growth, which proceeds via either the advancement of the gas-solid interface or the solid-liquid interface.

Differences in the processes used for SiC and silicon boule growth are behind differences in the cost, size and availability of these substrates. For silicon, ingots produced in state-of-the-art crystal growth equipment have a diameter of 450 mm and a length exceeding 2 m, and are realised at a growth rate of around 100 mm/hour. Growth is initiated using a thin seed with a 10 mm by 10 mm cross section.

In contrast, SiC crystals are grown with a diameter of 150 mm, and have a length up to 50 mm, with growth proceeding far more slowly – it occurs at 100-300 μm/hour. This process begins with a starting seed that has a diameter of 150 mm or more and a thickness of 1-2 mm.

One significant barrier to entry for any company wanting to manufacture SiC substrates is that the high-quality starting seeds, which are needed to initiate the process, are not commercially available. Trying to get around this by using a commercial substrate as a seed for bulk crystal growth is not an option, as this is prohibited by SiC wafer manufacturers. Hence any new entrants to this market must spend considerable development time and resources generating high-quality seeds.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration.

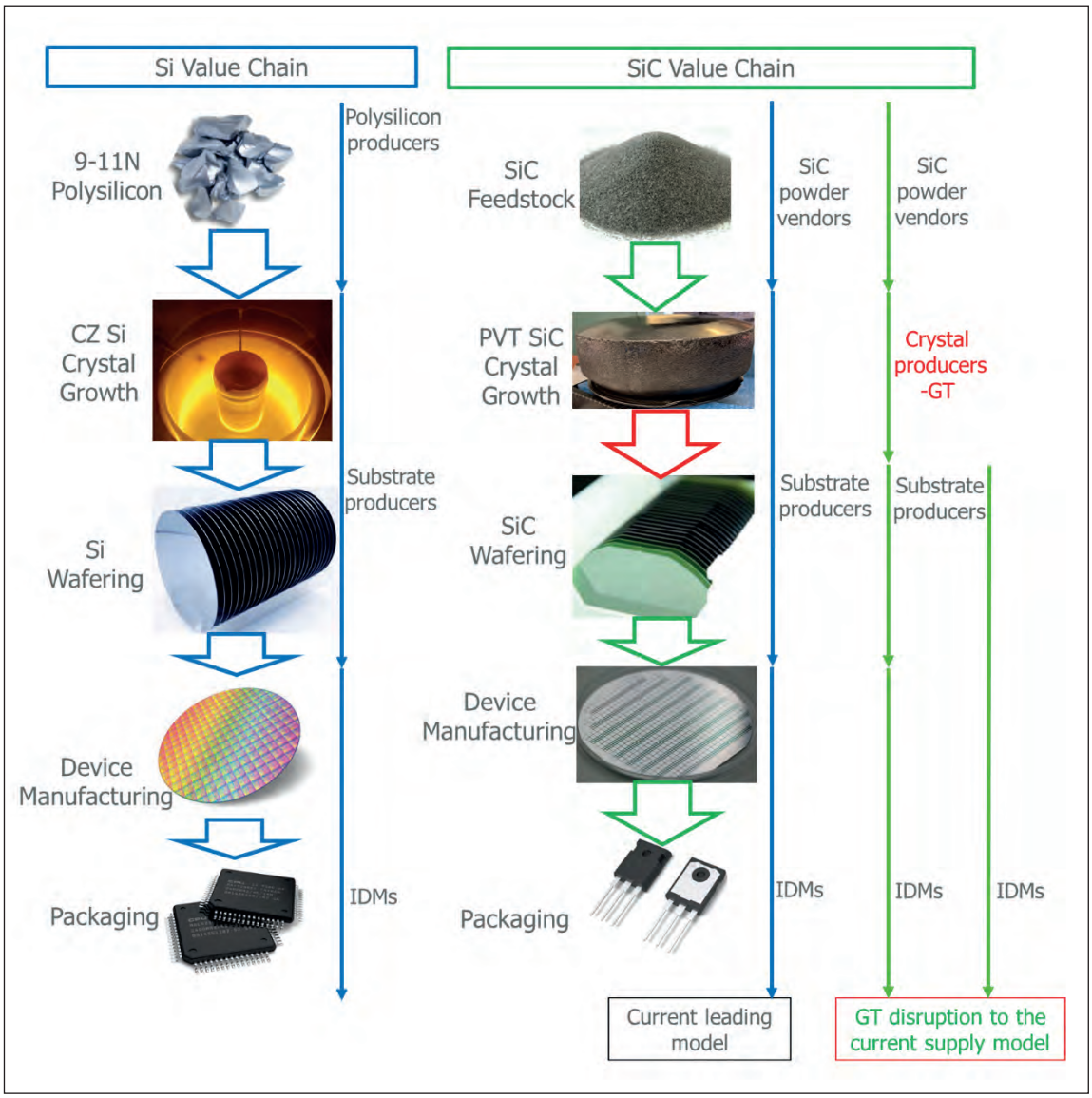


Figure 2. The SiC value chain has different challenges to that for silicon.

Along with slow growth rates and limitations to crystal size, difficulties associated with yield in the vapour growth process account for the far higher production costs of SiC crystals, compared with those made from silicon. Yet, despite the far higher substrate cost, even today a circuit designer that switches from using silicon devices to those made from SiC gets a 5-10 percent cost reduction at the system level. So the material already pays for itself, and its winning margin is only going to grow as the costs of SiC substrates and devices fall significantly over time. Note that in addition to the cost savings, SiC devices enable smaller, lighter systems, primarily due to their higher power densities (see Figure 1 for details of cost savings).

Another challenge associated with SiC relates to the many forms of this material. There are three crystal structures – cubic (3C), rhombohedral (15R) and hexagonal (2H, 4H, 6H, etc.) – and the number of polytypes exceeds 200. The 4H polytype of SiC, used for power electronics, accounts for around 60 percent of the SiC market. Devices are made on *n*-type SiC, produced by doping with nitrogen gas. This results in a resistivity in the 0.015 to 0.025 Ω cm range – it is typically 0.020-0.022 Ω cm. Sales of substrates for making RF devices account for 40 percent of the SiC market. These devices involve the growth of GaN-based heterostructures on 4H semi-insulating substrates. Produced by either doping with vanadium, or the absence of doping, they have a resistivity exceeding 10,000 Ω cm. For opto electronic device application, 6H polytype is used.

The quality of SiC lags that of silicon. The latter can be grown free of defects, while SiC suffers from fundamental issues associated with vapour-phase growth, multiple polytypes and a spiral growth mechanism. Part of the problem is that the stacking fault energy needed for the atoms to migrate to, and sit in, the right place is far lower in SiC than silicon. This introduces a wide range of defects,

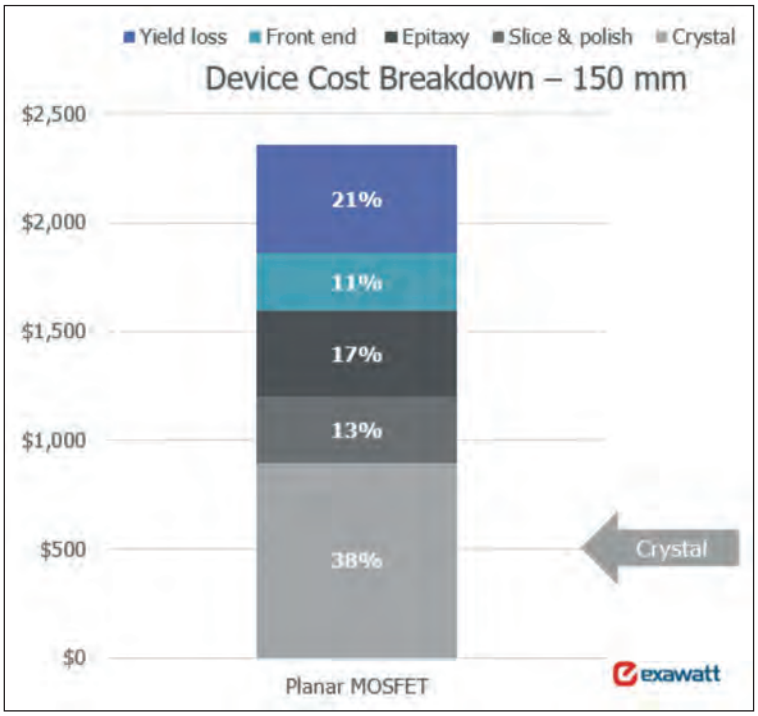


Figure 3. The cost breakdown for a SiC MOSFET produced on a 150 mm wafer. Source: Exawatt

including micropipes, carbon inclusions, and extended crystal defects, such as threading screw dislocations, threading edge dislocations, basal planar defects and stacking faults. Mitigating these defects is not easy, requiring a combination of equipment expertise and process knowhow. Just one without the other is insufficient for delivering the results demanded by high-growth markets.

Accelerating cost parity

At GT Advanced Technologies, also known as GT, we have developed and refined a high-yielding crystal growth process for large-volume, low-cost SiC boule production. This is helping us meet our primary objectives of accelerating cost parity between silicon and SiC, and greatly increasing the supply of this high-demand material.

Our efforts have enabled us to produce 150 mm diameter SiC substrates using mainstream production processes. As the availability of larger-diameter wafers is key to lowering device cost and improving die yields, we have also started development work on 200 mm boules.

The price of the SiC substrate is governed by the costs associated with the furnace architecture and infrastructure – factors such as the cooling water supply, the cost and need for uninterruptible power, the space occupied, the exhaust system and HVAC. There are two options for creating the high temperatures needed for SiC sublimation: a resistively heated furnace, with heat transferred from the heater to the crucible by radiation; and inductive heating of the crucible, which acts as the heater. One downside of resistive furnaces is a high fixed cost profile, stemming from equipment capex, the large footprint and infrastructure. Using this form of heating, there is limited opportunity to trim costs through operational and technical improvements. The promise of savings is far greater with inductive platforms. They offer a much lower fixed cost burden, due to lower capex, higher productivity, a lower electrical consumption, and a smaller footprint.

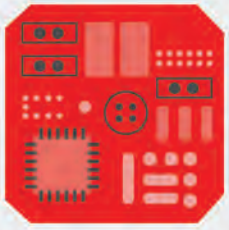
By adopting the inductive approach for reasons just outlined, we have positioned ourselves as a cost leader today, with a tremendous headroom for further improvements. Our production process enables high yields, high-quality and low cost, thanks to extensive thermal modelling skills, combined with excelled equipment design and process control innovations. The boules we produce have low defects, both for micropipes and other crystalline defects, and are manufactured in a cost-effective manner, due to a very high run-to-run reproducibility.

We are also able to draw on established supply-chain resources, equipment design and build capabilities, and process expertise. These strengths put us in a great position to scale quickly with demand and further improve our production processes over time. This will steadily increase our competitiveness in providing a low-cost, high-volume supply of SiC bulk materials.

The challenges of SiC substrate production are not limited to crystal growth. Processing boules into wafers is not easy, due to in-built thermal stresses arising from the growth process and a high material hardness – it is second only to diamond. Substrate production begins by grinding the SiC crystal to a specific diameter and then undertaking multi-wire sawing, using either a diamond slurry, a diamond-fixed abrasive wire, or laser-based wafering. This is followed by coarse and fine grinding of the surface, edge grinding and chemical-mechanical polishing.

Device makers will take the epi-ready substrates, load them into an MOCVD chamber, heat this to 1600 °C, and grow an epilayer using propane as the source of carbon and silane or trichlorosilane as the source for silicon. Depending upon the intended device breakdown voltage, the thickness of this drift layer will be somewhere between 5 μm and 100 μm (the drift layer thickness is approximately 1 μm per 100V, so for a 11 kV device, the epilayer thickness needs to exceed 100 μm).

To realise excellent reliability and drive improvements in yield and cost, device production may draw on recent refinements, such as gate oxide and thermal oxidation processes. Such techniques have helped expand the portfolio of SiC devices, which include Schottky barrier diodes, MOSFETs, HEMTs, MesFETs, JFETs, cascodes and BJTs, with operating voltages spanning 600 V to 30 kV. Power modules have also been produced from SiC devices, using developments



	Ge	Si	GaAs	4H SiC	4H SiC comments
Bandgap (eV)	0.67	1.1	1.4	3.3	Larger bandgap, lower leakage current, higher operating temperature and radiation resistance
Breakdown field E_c (MV/cm)	0.1	0.3	0.4	2.5	Higher breakdown field, lower on-resistance and higher blocking voltage
Thermal conductivity W cm^{-1} C^{-1}	0.58	1.3	0.55	3.7	Higher thermal conductivity, which increases heat spreading and power density
Relative dielectric constant ε	16	11.8	12.9	9.7	Lower dielectric constant – less parasitics
Electron velocity υ_s (cm/s) x 10^7	0.6	0.9	1	1.5	High electron saturation drift velocity leads to smaller devices
Electron mobility μ (cm^2Vs^{-1})	3900	1400	8000	1000	
Johnson Figure of Merit (Maximize Frequency and Voltage)	1	5	7	63	
Baliga Figure of Merit (Minimize conduction losses)	1	7	106	2429	

Table 1. Physical properties of germanium, silicon, GaAs and SiC.

in packaging technology, such as direct-bonded copper and direct-bonded aluminium-on-AlN. These modules can operate at temperatures beyond 200 °C.

The supply chain for SiC power electronics is markedly different from that for silicon (Figure 2). The former is held back by the limited availability of SiC crystal, a major bottleneck that we are eliminating through our supply chain strategy. In comparison, integrated device manufacturers (IDMs) in the silicon industry are buying material from multiple substrate producers. Complicating matters, the leading incumbent SiC substrate vendors also make their own devices, so they compete against their downstream customers.

Like silicon, the SiC industry needs 'pure play' material suppliers. GT's supply chain strategy will enable this, opening up opportunities for existing silicon substrate providers to add SiC to their portfolios, leveraging established scale, mature value chains and established relationships with the IDMs who buy silicon substrates. Similarly, IDMs can rapidly add wafer capacity and increase their level of vertical integration. In either case, costs should rapidly decline as scale is added and industry freed from its dependency on just a few merchant suppliers.

This transformation of the SiC industry will deliver much success in the power electronic industry. Today, a single epi-ready 150 mm SiC substrate retails for $800-$1,100, accounting for a significant proportion of the device cost (the cost breakdown of a MOSFET is given in Figure 3). The cost of this substrate can tumble – we expect it to fall to just $300 in the years to come. One of the keys to this price reduction is increasing the useable height of the grown crystal, as run costs are relatively independent of crystal height.

Additional drivers are lowering capex, reducing operating costs, increasing productivity, tightening process control and increasing factory yield – crystal growth yield must be pushed above 98 percent, while crystal fabrication yields needs to go beyond 95 percent.

Our expertise in SiC crystal growth has led us to make the strategic decision to focus solely on this, drawing on our knowledge and experience in crystal growth equipment and SiC growth. We are offering the world's wafer producers a large supply of high-quality SiC crystal. This offering broadens and deepens the global supply of SiC wafers, helping drive down costs.

The power device industry is already welcoming these market developments. Illustrating this, in August 2019 GTAT signed a long-term agreement with GlobalWafers to supply its CrystX SiC crystal, and in early 2020 signed a long-term supply agreement with ON Semiconductor, one of the leading IDMs.

Stretching the bandwidth of GaN power amplifiers

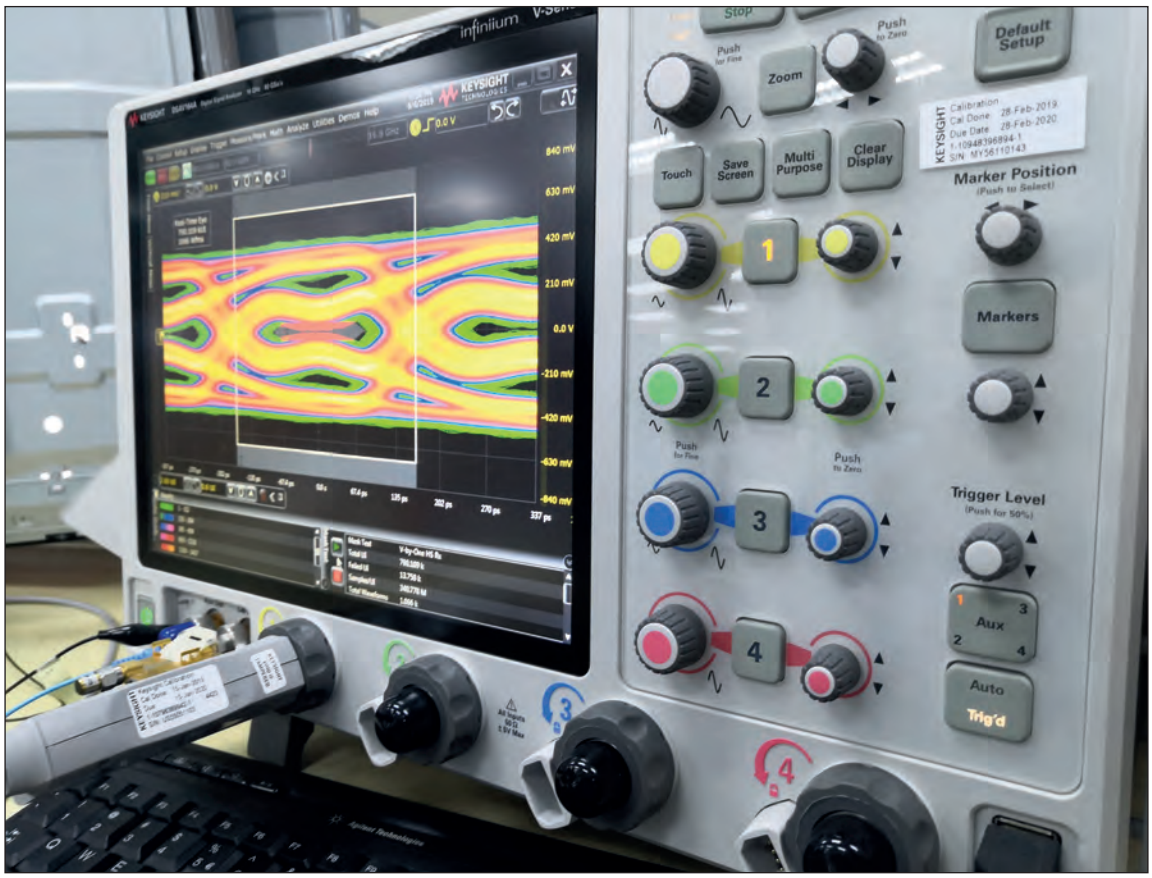
Broadband performance reaches a new level by enhancing the coupling within amplifiers that are based on the GaN HEMT

BY RICHARD STEVENSON

WHAT DO YOU VIEW as the key priorities for an amplifier? Whether it is boosting signals to drive a pair of loudspeakers, increasing the reach of a base station or engaging in electronic warfare, sufficient gain must be vying for the top of the list. Linearity will also command a premium, as this ensures the waveforms are reproduced faithfully; and efficiency is definitely an asset, driving down cooling requirements and trimming electricity bills.

Within this list of highly valued attributes, there is also the desire for bandwidth. Applications often require amplification over a wide range of frequencies, and this is ideally realised without having to employ several amplifiers for different frequency domains, as that adds to complexity and cost.

Several different approaches for improving the bandwidth of amplification at various frequencies



were outlined at this year's IEEE MTT-S International Microwave Symposium, held online from 4-6 August. Here we describe the highlights of a handful of papers presented at that meeting, outlining progress at frequencies spanning sub-gigahertz to beyond 200 GHz.

All of these papers describe the use of high-quality GaN transistors for the construction of wide-band, high-performance amplifiers. Note, however, that simply selecting these devices does not guarantee success. How they interact with surrounding components is critical, and consideration must be given to the likes of the interconnect technology and impedance matching.

Transmission-line transformers

Doing just that are Yoshitaka Niida and co-workers from Fujitsu Laboratories. They have enjoyed much success, with progress leading to a claim to have set a new benchmark for the bandwidth of GaN PAs with an output of over 200 W.

At the heart of Fujitsu's amplifier, which spans the range 0.5 GHz to 2.1 GHz, is a transmission-line-transformer-based combining architecture. This draws on a well-established approach, the transmission-line transformer, which is a class of wideband impedance transformer. Rather than a conventional impendence transformer, which transfers energy by magnetic coupling, energy is transferred by a transverse transmission-line-mode. This results in the realisation of an ultra-wideband impedance transformer.

A significant challenge facing designers of amplifiers is how to convert the transistor's impedance, which is typically just a few ohms, up to a value of 50 Ω by the matching circuit. Using a large impedance conversion ratio for the matching circuit is not a great solution as this narrows the bandwidth.

To address this concern, Niida and colleagues add a impedance conversion function to the power combiner. With this approach, impedance converted by the matching circuit is up to 12.5 Ω, reducing the impedance conversion ratio.

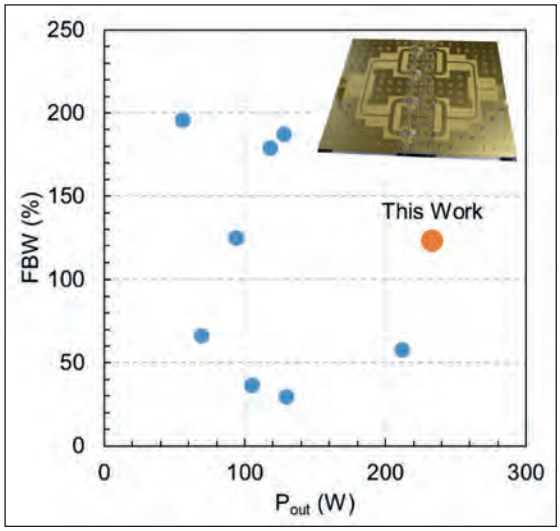


Figure 1. An evaluation of Fujitsu's amplifier, which features a transmission-line-transformer-based combining technique, indicates that it sets a new benchmark for bandwidth. The inset shows the fabricated PA.

The power-combiner produced by the team has four input ports, each with an impedance of 12.5 Ω. The first stage transforms impedances from 12.5 Ω to 25 Ω, and the second takes it from 25 Ω to 50 Ω.

Fabrication of the transmission line involves the creation of metallic structures, facilitating strong coupling, on the top and bottom of a 0.5 mm-thick substrate with a dielectric constant of 3.4. Metallised through-holes are formed in the substrate, and the bottom and top layer electrically connected, to create a transmission-line-transformer-based power combiner that is 22 cm by 11 cm in size.

The team formed a wideband power amplifier by placing four GaN HEMTs PAs, each with 12.5 Ω input and output impedances, between a four-way power divider and a four-way power combiner. The HEMTs, sporting a 16 mm gate width, were produced in-house using a 0.25 μm AlGaN/GaN HEMT technology. Small signal measurements on the amplifier, measuring 22 cm by 27 cm by 1.5 cm, revealed a gain of over 9.7 dB and an input return loss

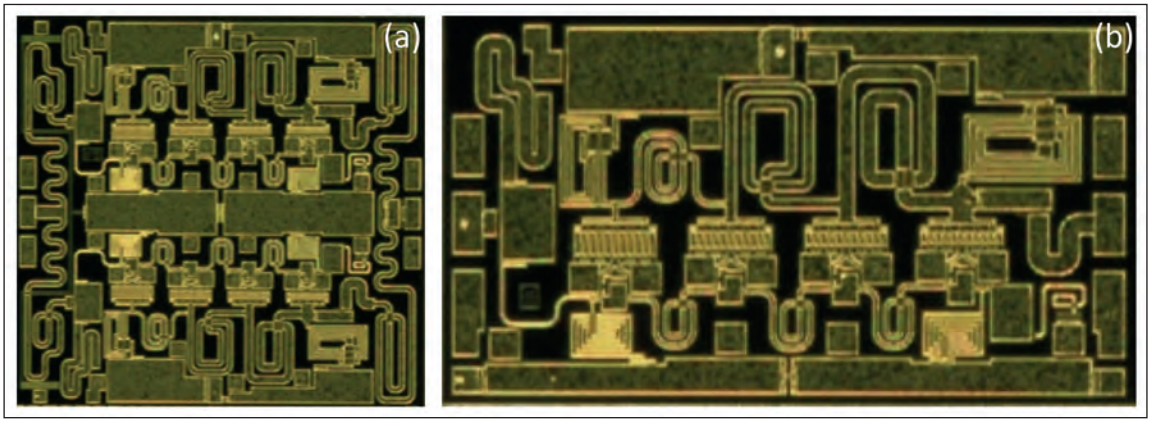


Figure 2. Researchers at Mitsubishi Electric Corporation have produced a single-ended (a) and two-way combined (b) high-power amplifier featuring a band-pass filter.

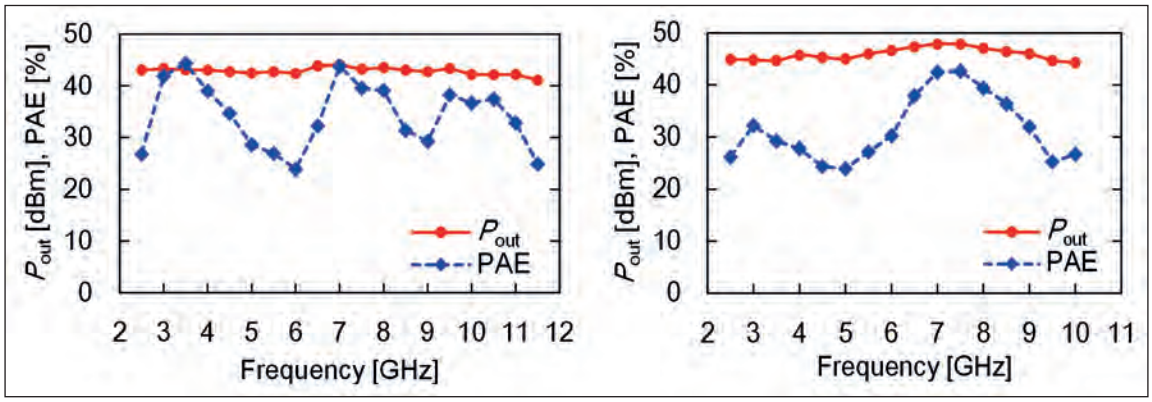


Figure 3. Mitsubishi's two-way combined GaN MMIC high-power amplifier has a higher output power (right) than the single-ended variant (left).

below -7.9 dB over the 0.5-2.1 GHz range, using a drain voltage of 50 V.

The same voltage is used for large-signal measurements involving 10 μs pulses and a 1 percent duty cycle. For an input power of 44 dBm, the amplifier produced an output of 53.4 dB ± 1.6 dB at a power-added efficiency of 42.3 percent ± 19.4 percent over the range 0.5-2.1 GHz. The output power peaked at a frequency of 1.3 GHz, hitting 55.0 dBm, which equates to 315 W.

Niida and co-workers have benchmarked their results using a metric known as fractional bandwidth – it is the difference between the highest and lowest frequency, divided by the centre frequency. Based on this figure, the team claims that their power amplifier has the highest bandwidth of any reported PA with an output power exceeding 200 W.

One of the next goals for Niida and co-workers is to examine whether this technology can be applied to higher frequencies.

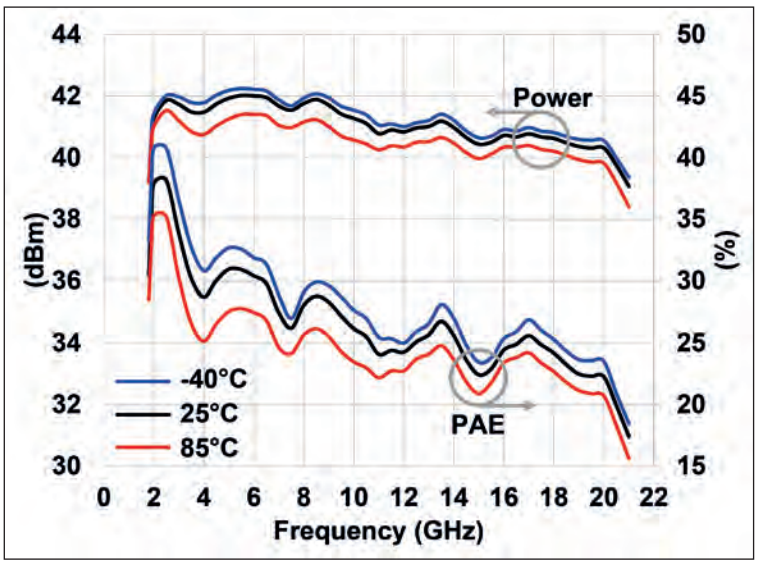


Figure 4. Qorvo's TGA2962 is a 10 W 2-20 GHz GaN MMIC with a chip size of just 10.5 mm². It produces an output power between 40.3 dBm to 42 dBm over the 2-20 GHz range, for an input power of 27 dBm.

Non-uniform distributed PAs

A popular option for delivering amplification in wide-band microwave systems serving commercial and defence markets is the GaN non-uniform distributed PA. It has the capability to combine a very wide bandwidth with a healthy output power and a good power-added efficiency.

Jun Kamioka and co-workers from the Information Technology R&D Centre at Mitsubishi Electric Corporation claim to have broken new ground by constructing the first non-uniform distributed PA that incorporates band-pass filters. They believe their design has delivered some of the highest ever output powers for wideband amplifiers.

With conventional distributed amplifiers that use an artificial transmission-line configuration for the first cell, there is a trade-off between the cut-off frequency and the output power for each of the FETs. Increase the gate periphery of the FET and its output power increases at the expense of its cut-off frequency.

One workaround with this circuit design is to add an additional capacitor to the first cell, but this increases cut-off frequency while compromising gain. A better option, according to Kamioka and colleagues, is to insert a band-pass filter. This increases the higher cut-off frequency, but also introduces a lower cut-off frequency.

The team have investigated this design by building single-ended and a two-way combined GaN MMIC high-power amplifiers, using the company's in-house 0.25 μm GaN-on-SiC MMIC technology (see Figure 2).

The single-ended variant is a 2.8 mm by 1.5 mm chip featuring four FETs. These transistors have gate peripheries of 1.0 mm, 0.7 mm , 0.6 mm and 0.5 mm, with band-pass artificial transmission lines applied to the first and last FET. Using a DC drain voltage of 50 V and a quiescent drain current of 50 mA, small-signal gain exceeds 12 dB over a 2.5 GHz to 11 GHz frequency range. Large signal measurements, under a pulsed gate bias with a 10 percent duty cycle, produce a power-added efficiency varying between 24

percent and 44 percent and an output ranging from 42.2 dBm to 44.1 dBm over the 2.5 GHz to 11 GHz range (see Figure 3).

The two-way combined MMIC is a significantly bigger chip, measuring 3.2 mm by 3.0 mm. Using the same measurement conditions, over the 2.5 GHz to 10 GHz range this amplifier produces a small-signal gain of over 11 dB, a power-added efficiency varying between 24 percent and 33 percent, and an output ranging from 44.3 dBm to 47.9 dBm – that equates to 27 W to 61 W.

Kamioka says that one of the goals for the team is to try and expand the bandwidth while maintaining the large output power.

Amplifiers with an even wider bandwidth have been produced by engineers from Qorvo. In a pair of papers presented at this year's IMS conference, developers at the company's Infrastructure & Defense Products division claim to have made two-stage GaN amplifiers with the widest bandwidth, for amplifiers that produce more than 10 W and are based on non-uniform distributed PAs. The team's 2-20 GHz GaN MMIC amplifiers, which feature a decade bandwidth transformer-based power combiner, deliver an output of up to 20 W.

According to the engineers from Qorvo, up until now output power over the 2-20 GHz band has been limited by the output power of a single PA, due to the lack of a low-loss combiner over this bandwidth. To address this limitation, the team developed two-stage amplifiers featuring a decade bandwidth on-chip transformer-based power combiner. The combiner is based on a broadside-coupled transformer, which is "quite novel", according to lead author Michael Roberg. He says that some of the intellectual property involved in the design and fabrication is patent pending, so he is unable to disclose more information at this time."

Amplifiers have been fabricated using Qorvo's QGAN15 process, which involves growth on SiC substrates, then thinned to 100 μm. Thinning is partly undertaken to improve the thermal management of the MMIC, says Roberg, who adds: "The thinning of the substrate is also critical for minimising the device source inductance, enabling high performance, high frequency operation."

It is usual to drive amplifiers operating at microwave frequencies at 28 V or more, but the MMICs made from Qorvo have been run at just 22 V, thanks to the introduction of the decade-bandwidth broadside-coupled transformer. Roberg says that moving to this lower voltage is a big deal, as it delivers several benefits: "Over a broad bandwidth, GaN devices have a better power-added efficiency at lower voltage. In addition, even if the power-added efficiency were identical at lower voltage, the GaN device has less dissipation at lower voltage."

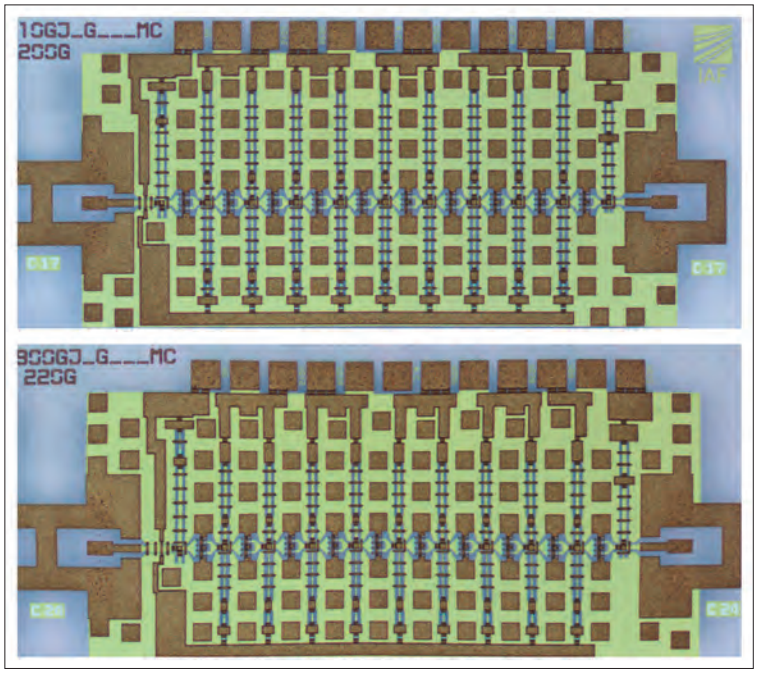


Figure 5. Researchers at Fraunhofer IAF are setting a new benchmark for the performance of GaN MMICs at frequencies of around 200 GHz. The team's ten-stage MMICs are capable of more than 15 dB of small signal gain over 145 GHz to 205 GHz (top), and 10 dB of gain from 162 GHz to 217 GHz (bottom).

Operating at a lower voltage also introduces merits associated with monolithic processes. By reducing the voltage, there is a reduction in the voltage swing across capacitors and active devices. "It is true that the higher current is traded for lower voltage to achieve the performance," says Roberg, "but every conductor is able to be properly designed, in order to ensure there are no electro-migration issues."

He and his co-workers have evaluated the performance of two different MMICs, which are both commercially available. The TGA2962 is a 10 W 2-20 GHz GaN MMIC with a chip size of just 10.5 mm^2, and its 20 W cousin, with a chip size of 25.8 mm^2, is the part QPA2966D.

Operating at a 22 V bias point, a gate voltage set for a quiescent current of 1680 mA, and using an input power of 27 dBm, the smaller chip produces an output of 40.3 dBm to 42 dBm over the 2-20 GHz range, and a corresponding large signal gain of 13.3 dB to 15 dB (see Figure 4). Power-added efficiency peaks at 38.2 percent at 2.5 GHz.

Driven under identical bias, but with quiescent current of 3360 mA and using an input power of 31 dBm, the output power of the larger chip fluctuates between 42.6 dBm and 44.9 dBm over the 2-20 GHz range, and has a large signal gain of 11.6 dB to 13.9 dB. There is a degradation in output power at the high end of the band, attributed to inaccuracies in the transformer-based combiner modelling. Roberg says that one of the next goals is to produce a full portfolio of wide

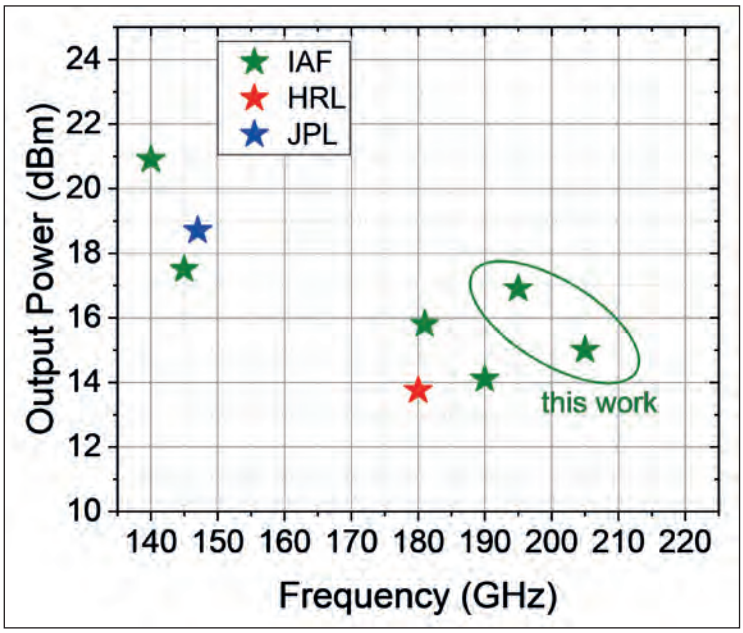


Figure 6. The performance of GaN MMICs produced at Fraunhofer IAF compares favourably with those made at HRL Laboratories and NASA's JPL.

bandwidth, high-power amplifiers from 1-40 GHz that will leverage the broadside-coupled transformer to achieve world-class output power and power-added efficiency.

Gains in the G-band

Focusing on far higher frequencies, engineers at Fraunhofer IAF presented a paper at IMS claiming to have produced the first G-band broadband power amplifier MMICs operating beyond 200 GHz.

Efforts by this team include the fabrication of a ten-stage amplifier providing a small-signal gain of more than 15 dB between 145 GHz and 205 GHz, which is a large proportion of the G Band that spans 140 GHz to 220 GHz. There is much interest in the atmospheric windows within this band because they ensure reduced propagation losses for next-generation high-data-rate wireless communication links and high-resolution imaging systems.

Maciej Ćwikliński, lead author of the paper detailing the performance of this high-frequency MMIC, plus another providing gain at a slightly different frequency range, says that the team's amplifiers have been fabricated using an enhanced version of their baseline in-house 100 nm process. Refinements include the capability to produce 70 nm gates, employed in the G-band amplifiers.

According to Ćwikliński, what makes the Fraunhofer IAF process unique is that it combines great high-frequency performance – that is a high f_T and f_{max} – with a good yield and uniformity for the transistors.

Fabrication of the amplifiers began by loading 100 mm 4H-SiC substrates into an MOCVD chamber and depositing a GaN-based heterostructure that included a thin AlN interlayer to reduce alloy scattering and increase the mobility of the two-dimensional electron gas. The engineers used silicon implantation to trim contact resistance, and electron-beam lithography to define the dimensions of the 70 nm gate. They realised a reduction of parasitic resistances by optimising the deposition of metal-insulator-metal structures, and completed fabrication by thinning the SiC to 75 μm and processing 30 μm by 30 m via holes.

One of the features of the HEMTs produced by Ćwikliński and his co-workers is an asymmetric gate-source and gate-drain spacing, with the length between gate and drain exceeding that between gate and source.

"The main purpose of extending the gate-drain spacing is to improve the high-frequency gain of the HEMTs, which can be associated with the reduced gate-drain feedback capacitance," explains Ćwikliński.

He and his co-workers form matching networks for the MMIC using a coplanar waveguide, and use a ground-ground spacing of 25 μm. Due to the high number of gain stages in this amplifier, the inter-stage matching network governs performance. It is realised as a double-stub tuning network, with both stubs DC-separated, allowing them to be used as bias injection points. To minimise the amplifier's footprint, the inter-stage matching network is compact. The drain feeder is connected to the top plate of the metal-insulator-metal-capacitor and routed further upwards via the drain-bias stub, and the gate feeder and the gate-bias stub are connected via the bottom plate of the metal-insulator-metal-capacitor. By positioning the drain feeder just 45 μm from the gate feeder of the following HEMT, a relatively dense layout is realised for the MMICs.

The team's first ten-stage amplifier, with a chip size of just 1.55 mm by 0.8 mm, has a peak in small signal gain of 30 dB at 155 GHz and delivers more than 15 dB between 145 GHz and 205 GHz. According to Ćwikliński, the homogeneity of the small-signal response over the wafer is excellent for such a high-frequency design. The RF yield is impressive, hitting 73 percent. Cell-to-cell variability in small-signal gain over the band of operation is just ± 1 dB over the entire wafer.

A second amplifier made by the team, measuring 1.5 mm by 0.75 mm, provides an average of 10 dB of small-signal gain from 162 GHz to 217 GHz. The gain remains above 7 dB up to 220 GHz. For this amplifier RF yield is 81 percent and homogeneity ± 2 dB.

Large-signal measurements have been undertaken on both designs. Using an input sweep at 195 GHz, the first MMIC provides up to 16.9 dB of power at a power density of 613 mW/mm. Power-added efficiency is 1.7 percent. For an input power of 8 dBm, output exceeds 14 dBm from 185 GHz to 205 GHz. The

second amp delivers up to 15 dBm of power at a power density of 439 mW/mm, with a corresponding power-added efficiency of 1.1 percent. An output exceeding 12 dB can be produced over the 170 GHz to 220 GHz band, using an input of 7 dBm.

Ćwikliński and co-workers have benchmarked the performance of their amplifiers against those made by teams at HRL Laboratories and NASA's JPL (see Figure 6). MMICs made at Fraunhofer IAF compare favourably, having the upper hand in both output powers and high frequencies.

Despite this progress, GaN MMICs are still to catch up with the performance of those based on InP. According to Ćwikliński, inferiority stems from the relatively low high-frequency gain of GaN HEMTs compared with InP-based transistors.

"Of course, it is hard to fight physics and make GaN transistors with higher gain than their InP counterparts," says Ćwikliński. "However, we still see some room for improvement, both technology-wise as well as circuit-design-wise."

He believes that GaN MMICs have the capability to outperform InP MMICs. To make this happen, high-performance HEMTs must be produced with a good degree of uniformity using a high-yield process. This will unlock the door to a substantial improvement in high-frequency power amplifiers, formed with multiple stages and multi-way combining.

Ćwikliński points out that state-of-the-art numbers for InP MMICs operating at 200 GHz involve combining 16 transistors in the output stage. "In the work shown at IMS2020, the output power is five times lower, but achieved only with a single GaN transistor in the output stage."

He also suggests that InP technology seems to be approaching its on-chip combining limit at high frequencies. One of the goals for the team is to introduce further improvements to its GaN process, enabling it to become an attractive candidate for MMICs operating above 100 GHz, mainly for applications in next-generation communication networks beyond 5G.

"The long-term goal is to put our GaN HEMT process as the dominating technology for power amplifier MMICs within the whole millimetre-wave spectrum – that is, up to at least 300 GHz."

Such efforts will help to increase the attractiveness of GaN amplifiers. Already renowned for their high power densities and power-added efficiency, an impressive bandwidth is not far behind.

A new level for linearity

Taking the electron-gas into the third dimension increases the linearity of power amplifiers, while retaining their efficiency and power density

BY SHAHADAT SOHEL AND SIDDHARTH RAJAN FROM OHIO STATE UNIVERSITY, AND ANDY XIE, EDWARD BEAM AND YU CAO FROM QORVO

ONE OF THE KEY CHALLENGES for the engineers that construct circuits for millimetre-wave communication is the design of the transmitter power amplifier, which is used in base stations and repeaters. A very promising candidate for these amplifiers is the GaN HEMT. Thanks to the material's large breakdown field and high saturation velocity, GaN HEMTs are delivering unprecedented efficiencies and power densities in the millimetre-wave frequency bands that are just starting to deliver ultra-fast data rates in the emerging 5G networks, and will do so in the 6G networks that follow.

In addition to high efficiencies and power densities, amplifiers must excel on a third front: linearity. Ensuring a high degree of linearity is critical to realising many communication channels at closely spaced frequencies. High-quality data transmission demands minimal crosstalk between multiple frequency signals, a condition realised by using an amplifier with a very high degree of linearity (see Figure 1). Today, this is not a strong suit for the GaN HEMT, predominantly because up until recently, development efforts for this class of transistor have majored on increasing gain and power density.

However, during the past few years the emphasis has started to shift, with significant effort directed at increasing the linearity of GaN RF transistors. This work has borne much fruit, with engineers making progress through innovative approaches at the epitaxial and device level. Success has not come easy, because linearity is influenced by many device and circuit parameters, including the bias dependence of transconductance, the output conductance, and bulk and interface traps.

Attempts to increase linearity must consider the two-dimensional electron gas (2DEG) that lies at the heart of a conventional GaN HEMT and is located at

the interface between a layer of AlGaN and the GaN channel. The velocity of these localised electrons governs the gain of the transistor, with recent work showing that this velocity depends on the electron density in the channel, and thus the gate bias. Changes in electron velocity are detrimental, leading to variations in the transconductance and gain of the device as a function of bias. This results in deviations from an 'ideal' field-effect transistor behavior, leading to non-linearity in key device characteristics.

Into the third dimension

The good news is that these problems are not insurmountable. One of the great strengths of the III-Nitride material system is that it offers significant design flexibility beyond the 2DEG. In an AlGaN/GaN HEMT, polarization discontinuity at the interface leads to a sheet electron gas. By spreading variations in polarization over some distance through a grading of the AlGaN composition, it is possible to spread out the electron charge.

By doing this, when the gate bias is changed the depletion width in the device changes, but the electron density remains the same – and in turn the velocity, which determines gain, is kept constant. Our team at Ohio State University and Qorvo had developed devices featuring this modification to the HEMT, and shown that they realise near-ideal constant/flat transconductance profiles (see Figure 2).

These compositionally graded transistors we are helping to pioneer are commonly known as polarization-graded FETs (PolFETs). As is the case in AlGaN/GaN HEMTs, electrons in the channel of the PolFET are generated from polarization charges only – there is no external doping involved. Due to this characteristic, impurity scattering is quashed, enabling a very high electron mobility. This attribute gives the PolFET the upper hand over the impurity-doped MESFET, which is impaired by dopant-related impurity scattering that diminishes mobility.

We have carried out detailed simulations to understand the influence of device transconductance on large-signal linearity. This has involved a 2D TCAD Silvaco simulation to extract bias-dependent small-signal parameters of the device, before drawing on these bias-dependent results to predict power and linearity performance using circuit-level Advanced Design System simulations.

One of the insights provided by these simulations is that flattening the transconductance propels the

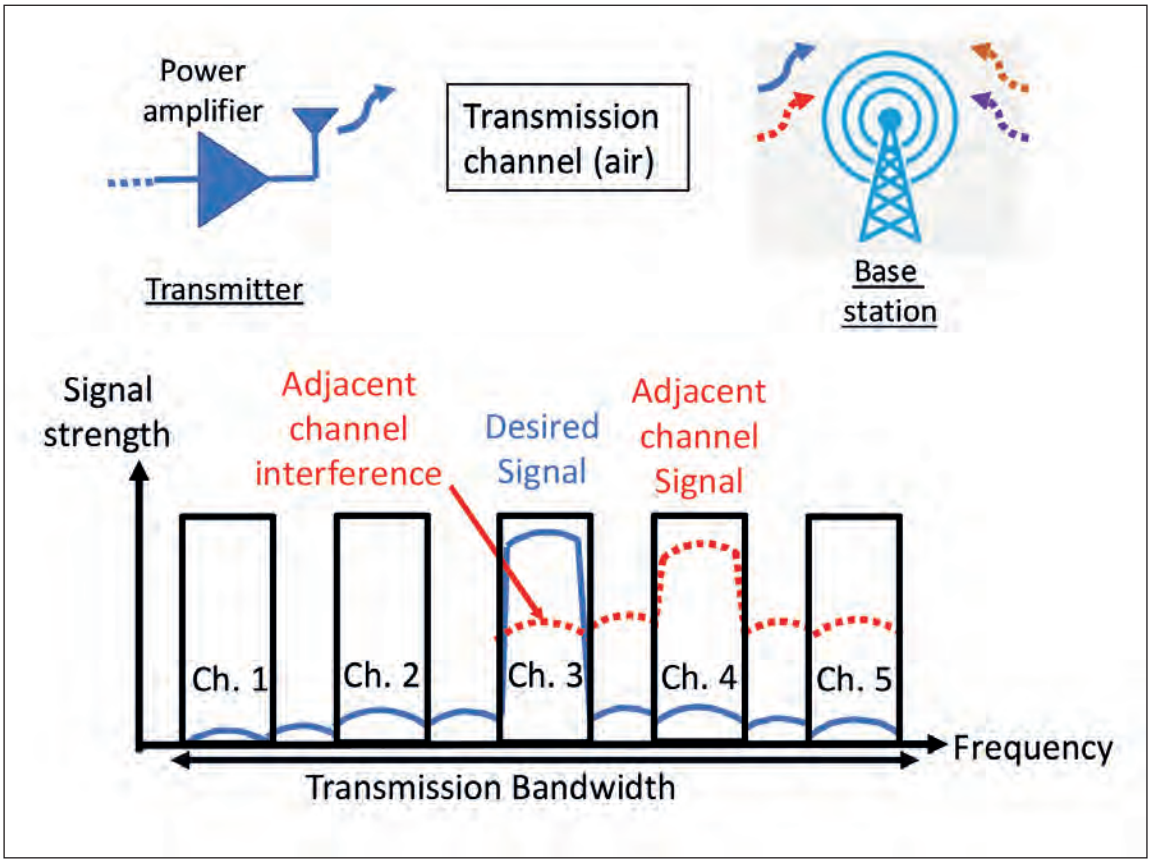


Figure 1. In a communication system, the transmitter contains a power amplifier that helps to transmit the signal into the transmission channel. The base station receives signals from many different transmitters. Each transmitter has a specific channel (bandwidth). If the power amplifier is non-linear for a specific transmitter (red), signal from other channels (blue) is distorted.

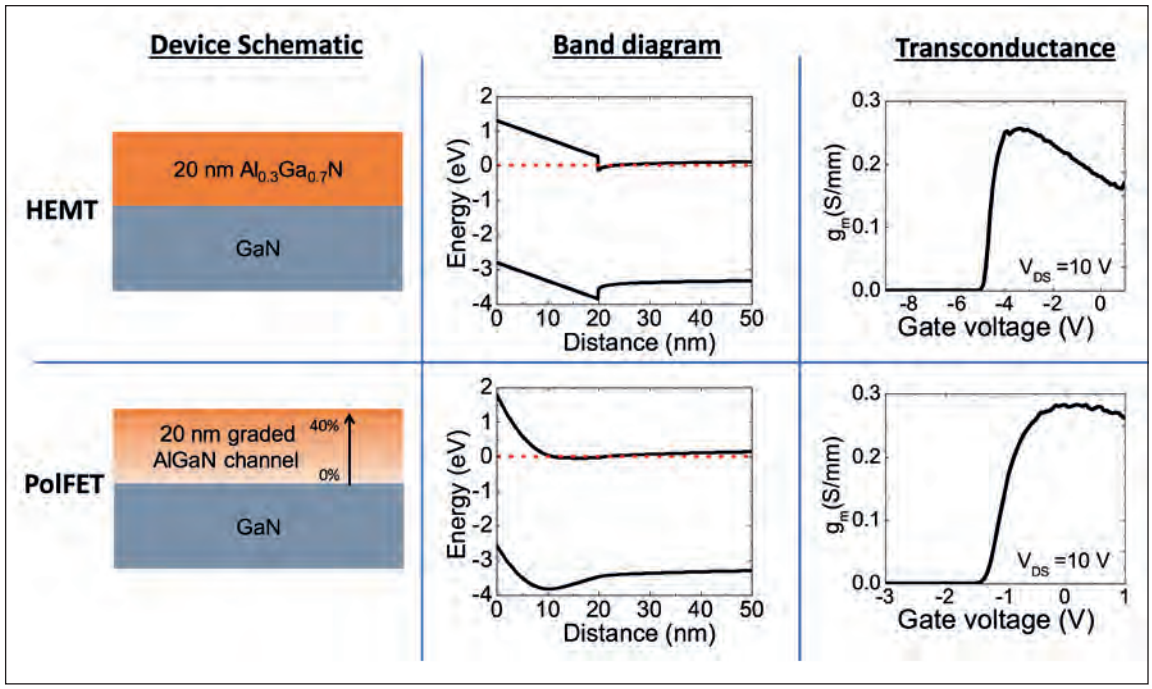


Figure 2. Differences between the bandstructure of the HEMT and the PolFET account for the difference in the transconductance (g_m) profile. The graded-channel PolFETs produce a flatter g_m profile.

performance of the PolFET to a level well beyond that of the HEMT. The promise of graded-channel devices for realising more linear circuits is underscored by plotting, as a function of input power, the ratio of the fundamental power to the third-order harmonic power (see Figure 3).

To see if the PolFET can live up to its promise, we have fabricated a portfolio of devices. These PolFETs feature linearly graded AlGaN channels with composition varying from 0 percent to 40 percent over 20 nm (see Figure 4).

Measurements on these PolFETs reveal that the current density, transconductance, and small-signal performance are comparable to that for HEMTs based on an AlGaN/GaN 2DEG (values are 720 mA/mm; 285 mS/mm; and 23 GHz and 65 GHz for f_T and f_{max}, respectively). The superiority of the PolFET shines through in the transconductance profile, which drops by just 10 percent over the bias range. In comparison, the comparable figure for the AlGaN/GaN HEMT is a fall by more than 40 percent.

A downside of these first-generation devices is their significant dispersion. We attribute this to the use of plasma-assisted CVD to passivate the devices. To overcome this weakness, we have explored an alternative method for depositing SiN – low-pressure CVD. It is a growth technology that is widely used in the silicon industry, and while it requires a higher thermal budget, it prevents plasma damage to the surface, so it can lead to significantly higher-quality SiN films.

We have combined this passivation-first process with the introduction of a field plate that reduces peak fields at the edge of the gate. Together these changes greatly improve the dispersion behaviour, with a low knee-walkout and minimal current collapse (see Figure 5). Small-signal performance is also encouraging, with an almost flat f_{max} across the entire current range (see Figure 6). This observation confirms that the small-signal power gain of the device is independent of the gate bias. That is in stark contrast to conventional AlGaN/GaN HEMTs, which exhibit a significant drop in the f_{max}/power gain across the gate bias range.

	Transistor type	OIP3 (dBm)	OIP3/P_{DC} (dB)
UCSB	N-polar GaN HEMT	-	12
HRL	GaN NDPA	43	4.8
OSU	**PolFET w/ LPCVD SiN_x**	**39**	**13.3**

Table 1. Comparison of device-level linearity figure-of-merit in X-band from literature.

Thanks to the improved RF-DC dispersion, we have realised a good large-signal performance from our PolFET. Using on-wafer load-pull measurements at 10 GHz and a biasing of the device in class A configuration, we have realised a power density of 3.4 W/mm at a drain bias of 15 V, along with a corresponding power-added efficiency of 40 percent. Linearity is excellent, setting a new benchmark in the X-band for the OIP3/PDC of 13.3 dB (see Figure 6 and Table 1).

Promising pathways

While these results are very promising, already matching state-of-art device performance, there are many avenues for further improvements worthy of exploration.

So far, our devices have a relatively long gate length – it is 0.7 μm – and further scaling promises significant improvements in high-frequency performance and linearity. Recent work by Jeong-Sun Moon and co-workers at HRL Laboratories has shown exciting results in this direction.

Further improvements are also possible by using different grading schemes beyond the linear grade that we have pursued. One team that has taken that approach is that of Mario Ancona and colleagues from the Naval Research Laboratories. These researchers have investigated the impact of different grading functional schemes on large-signal linearity. Options in this vein that could offer additional flexibility in design include the introduction of channels that incorporate 2D and 3D electron gases. This has the potential to allow the designer to tailor capacitance and transconductance profiles in the III-Nitride system while maintaining high mobility due to polarization-induced doping. Such a high degree of flexibility provides a truly unique advantage when compared with other material systems.

Another exciting area of research is the use of graded channels in 3D architectures. They include the superlattice castellated FET, pioneered by Northrop Grumman; and the BridgeFET, trailblazed by Teledyne Systems.

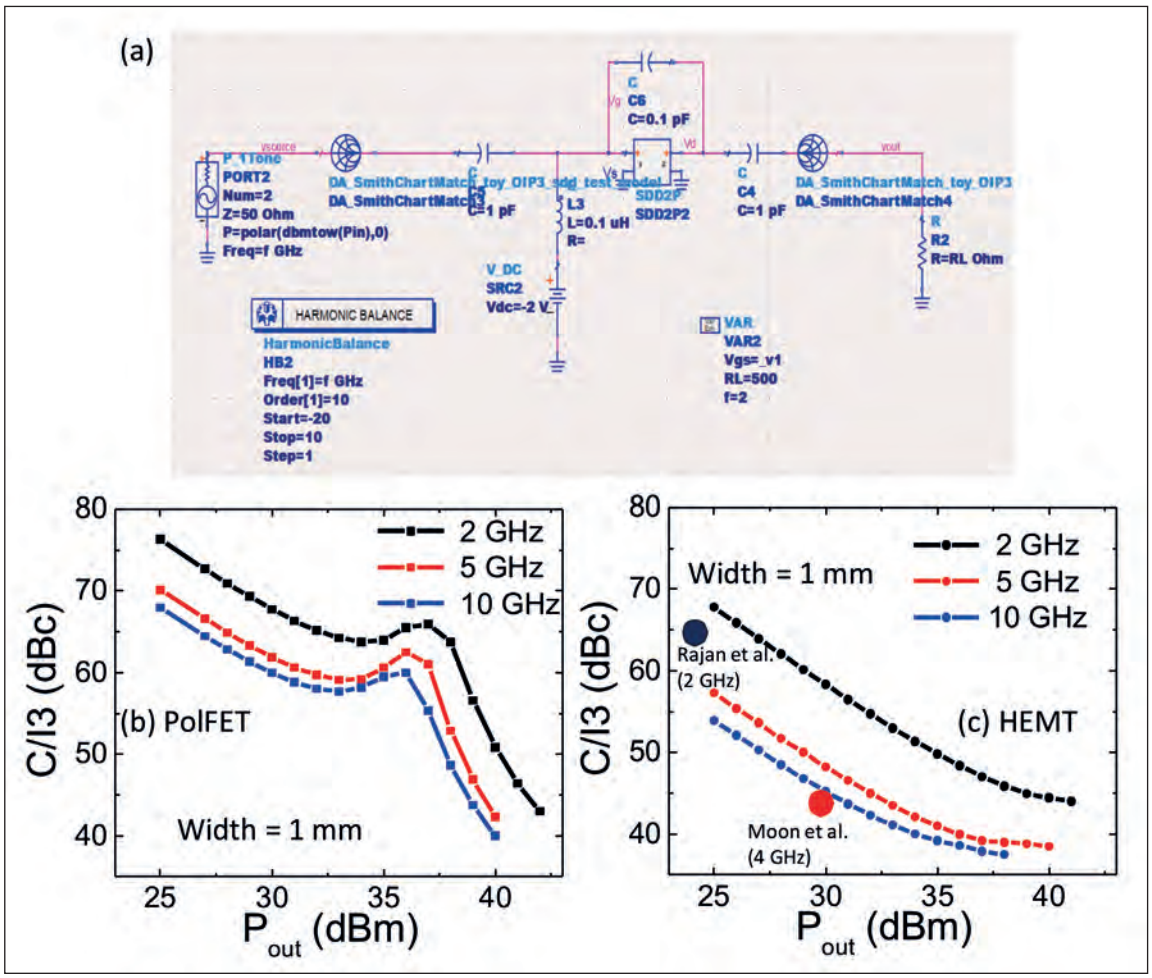


Figure 3. (a) Keysight ADS large signal simulation setup for calculating linearity. The transistors are modelled using the symbolically defined device (SDD2P) tool with small signal parameters calculated using TCAD simulation. Simulation show that PolFETs (b) provide a better C/I3 (harmonic suppression) than HEMTs (c). (For more details, see Proceedings of Int. conf. on Compound Semiconductors Manufacturing Tech., Austin, TX, 2018).

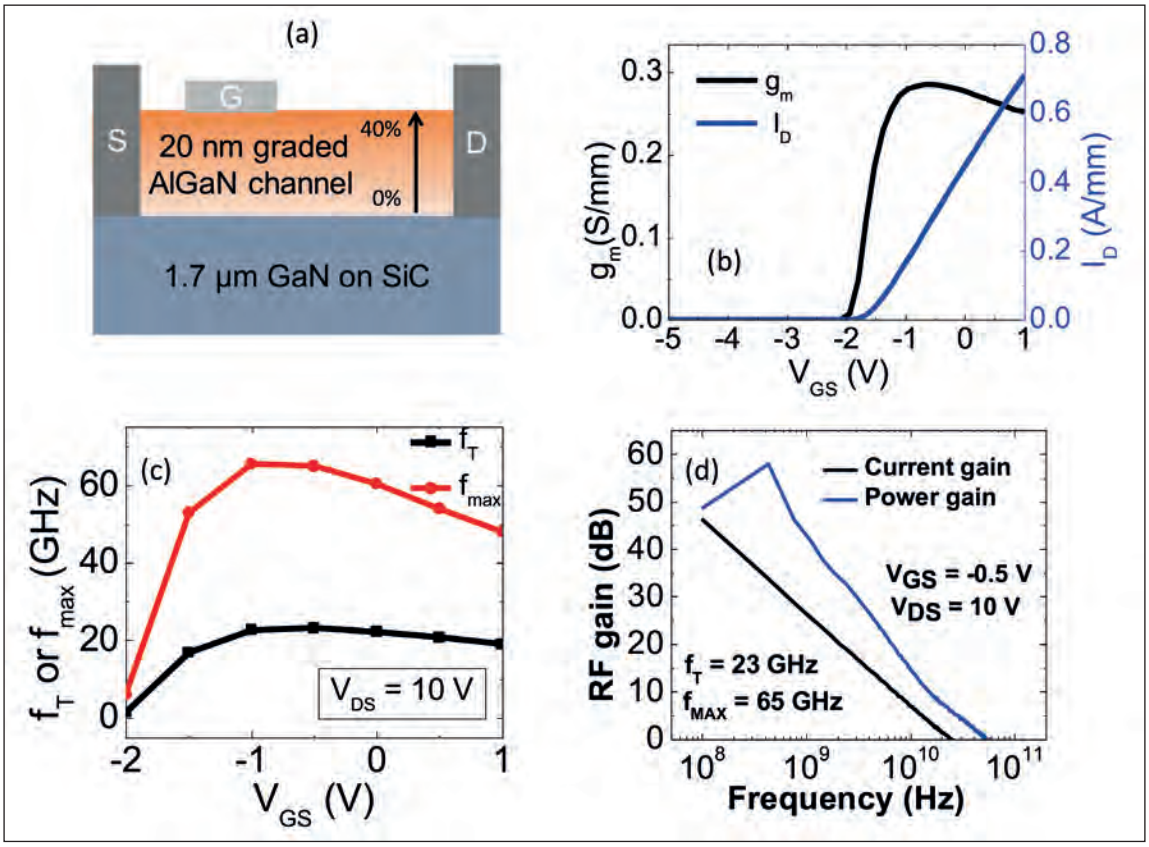


Figure 4. (a) Schematic diagram of a fully processed PolFET. (b) Transfer characteristics and (c) a current gain and power gain cut-off frequency (f_T-f_{max}) plot as a function of gate bias show the expected linear behaviour from PolFETs (d) Results from a two-tone linearity measurement at 10 GHz show an OIP3 (intersection of fundamental and third harmonic power) of 33 dB (S. H. Sohel *et al.* IEEE Electron Dev. Lett. **39** 1884 (2018)).

Switching to ultra-wide bandgap materials, such as AlGaN, offers yet another avenue for graded-channel transistors. The larger breakdown fields associated with these devices could enable a higher Johnson figure-of-merit. Early work on these devices has already been reported by a team at Sandia National Laboratories.

Given the tremendous sensitivity of linearity to dispersion, there is a need to research more effective surface passivation schemes. Efforts on that front include work by our team showing that epitaxial passivation schemes can create graded-channel devices, and effectively suppress surface-related dispersion.

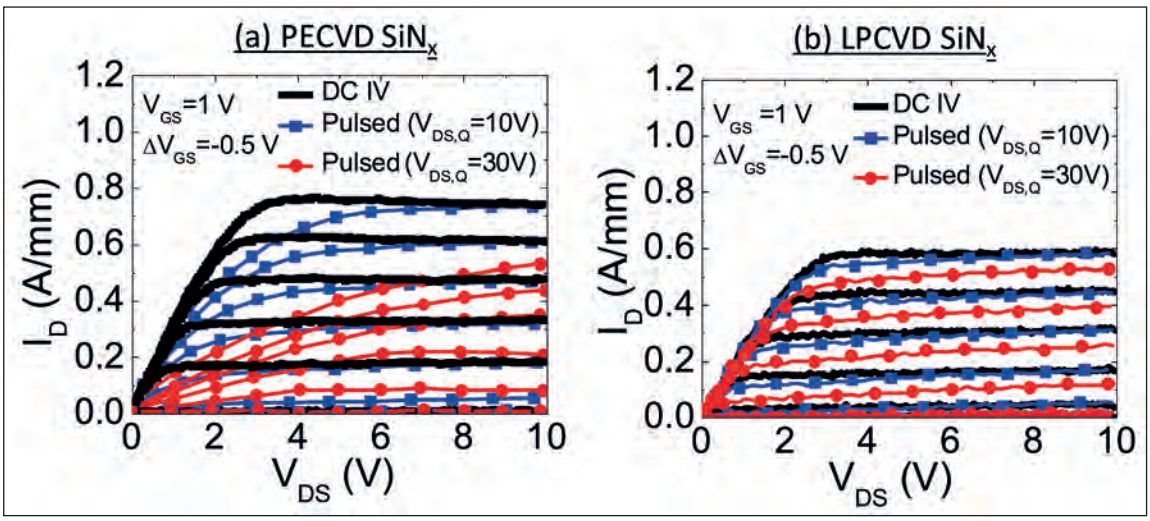


Figure 5. A comparison between measured pulsed current-voltage characteristics for PECVD and LPCVD SiNx passivated PolFETs. These results show significant improvement for the DC-RF dispersion in terms of both current collapse and knee-walkout for LPCVD SiN_x passivation. The current collapse at 30 V drain quiescent condition reduced to 8 percent (LPCVD) from 25 percent (PECVD) and knee voltage walkout reduced to around 1 V (LPCVD) from around 8 V (S. H. Sohel *et al*. IEEE Electron Dev. Lett. **41** 19 (2020)).

02.11 2020

Main event:
Monday 2 November
10am GMT
(Greenwich Mean Time)

China Taiwan Time Recorded Event:
Wednesday 4 November
10am CTT, (GMT +8 hrs)

Pacific Standard Time Recorded Event:
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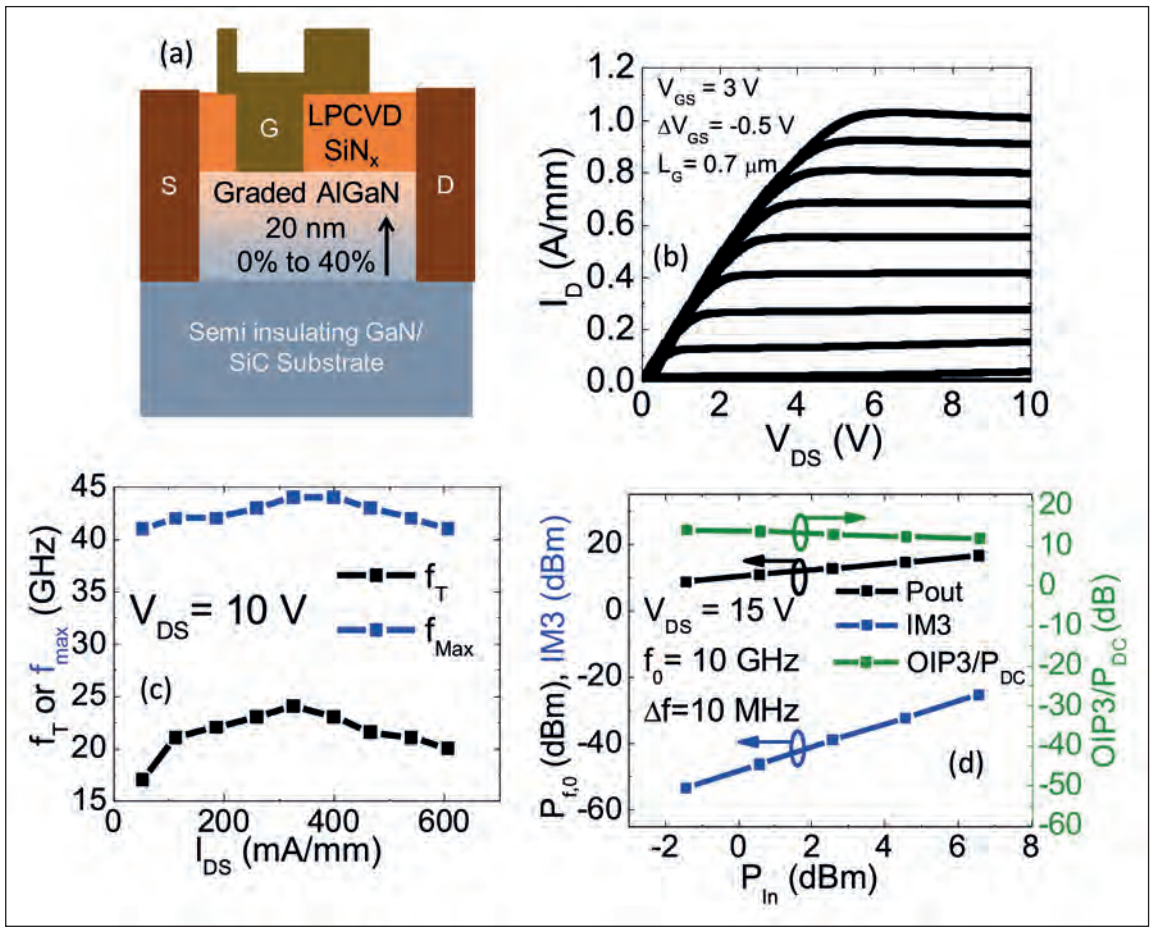

Figure 6. (a) Schematic diagram of a fully processed PolFET with LPCVD SiN_x passivation, (b) output characteristics, (c) f_T and f_{max} as a function of output current, and (d) two-tone linearity measurement at 10 GHz (S. H. Sohel *et al.* IEEE Electron Dev. Lett. **41** 19 (2020)).

Further reading

S. H. Sohel *et al*. IEEE Electron Dev. Lett. **39** 1884 (2018)

S. H. Sohel *et al*. IEEE Electron Dev. Lett. **40** 522 (2019)

S. H. Sohel *et al*. IEEE Electron Dev. Lett. **41** 19 (2020)

S. H. Sohel *et al*. Appl. Phys. Express **13** 036502 (2020)

M. Ancona *et al*. IEEE Transactions on Electron Devices **66** 2151 (2019)

J. Chang *et al*. IEEE Electron Device Letters **40** 1048 (2019)

K. Shinohara 2019 IEEE MTT-S International Microwave Symposium (IMS). IEEE, 2019, pp. 1133-1135, doi: 10.1109/MWSYM.2019.8700845.

A. Armstrong *et al*. Appl. Phys. Lett. **114** 052103 (2019)

S. Sohel *et al*. Applied Physics Express **13** 036502 (2020)

P.S. Park *et al*. IEEE Electron Dev. Lett. **36** 226 (2015)

Finally, the graded channel approach could be uniquely suited to integration with silicon, due to the ability to realise very low-resistance non-alloyed contacts. A value of just 0.2 Ω-mm has been reported by Pil Sung Park and co-workers from Ohio State University.

This body of work, which we have contributed to, shows that graded-channel devices provide unique flexibility to device and circuit designers for future millimetre-wave amplifiers. Demonstration of excellent DC, small-signal, and large-signal performance during the last few years highlights that application-specific epitaxial design could enable significantly improved functionality and performance for III-Nitride devices. We believe that future research, both by our team and those working in various research groups around the world, will provide exciting breakthroughs that could unlock the door to future commercial and military applications for these devices with tailored electron-gas profiles.

The work at Ohio State University was funded by the Office of Naval Research (Program manager: Dr. Paul Maki). We would like to acknowledge our collaborators at Ohio State University (Hao Xue, Prof. Wu Lu) and Naval Research Laboratory (Jason Roussos, Dr. David Meyer).

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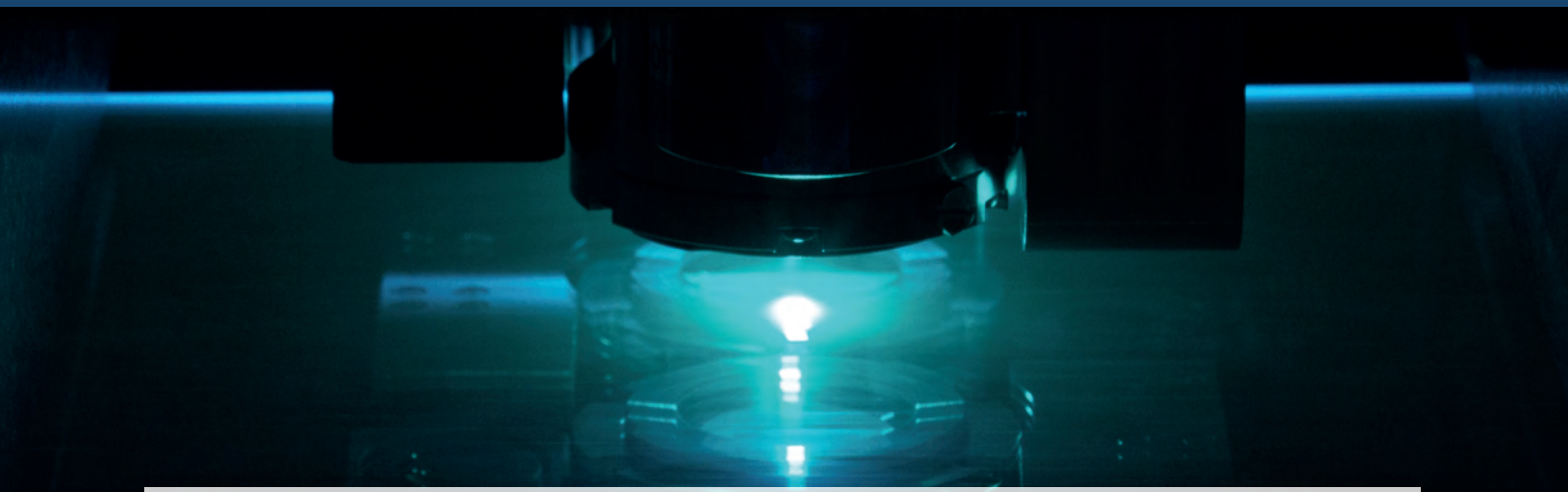

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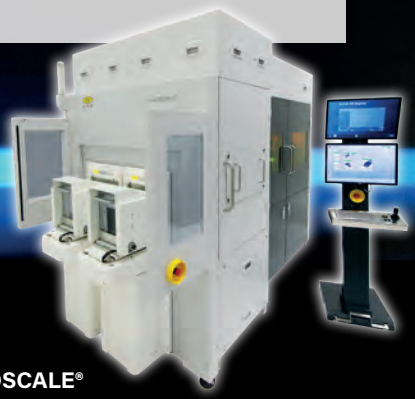

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Cubic GaN garners a glorious green

Manufacture of efficient green LEDs is now within reach, thanks to proprietary growth conditions that yield cubic GaN on silicon substrates

BY MARTIN LAMB, MENNO KAPPERS, LATA SAHONTA AND DAVID WALLIS FROM KUBOS SEMICONDUCTORS

DESPITE HUGE INVESTMENT in the last decade, the LED industry has failed to close the 'green gap', the weakness associated with the relatively low efficiency of green LEDs compared with their red and blue cousins. The repercussions of this inferiority are immense and include holding back the performance of solid-state lighting. Once the green gap is addressed, tremendous energy savings will follow. In addition, there will be a substantial cut to the carbon impact of lighting and an increase in demand for connected LED lighting – it could climb by as much as 14 percent, according to the US Department of Energy's Energy Savings Forecast of Solid-State Lighting in General Illumination Applications.

Fortunately, there is a technology that offers a great solution to the green gap: cubic GaN. This is now poised to revolutionise solid-state lighting, thanks

to the development and commercialisation of LEDs employing this form of GaN by our team at British start-up Kubos Semiconductors, using technology originally spun out of the University of Cambridge.

Our technology will provide a new impetus to LED-based lighting, which has undergone explosive growth over the last ten-to-twenty years. While commercial success will undoubtedly continue, with LEDs destined to become the dominant technology across most lighting applications, there is still room for improvement. According to the US Department of Energy's 2019 Lighting R&D Opportunities report, published at the start of this year, the efficacy of LED-based solid-state lighting remains open to significant further improvement. A number of key areas of opportunity were identified in that document, as well as goals for research and development. Realising success on these fronts would stimulate further accelerated growth.

To date, the solid-state lighting industry enjoyed most success with phosphor-converted LEDs. In these devices, white light comes from applying a phosphor coating to a high-efficiency, blue LED that is based on hexagonal crystalline GaN. Turn on this device and some of the light emitted by the chip pumps the phosphor that luminesces across a broad yellow band, with white light resulting from the combination of this emission and that from the blue LED.

Widespread uptake of LED lighting demonstrates the success of this approach. However, this modus operandi has its drawbacks and can be improved. Colour management of white light is a challenge, and you get a trade-off between efficiency and the colour palette. Adjust the design to increase efficiency and a harsh, unflattering cool white hue results, stemming from the large underlying blue component in the emission. When viewed from a thermodynamic perspective, a further flaw emerges: the phosphor conversion process is inherently inefficient, placing a practical limit on the overall efficiency of the device.

Thanks to advances in phosphor-converted LEDs, designers are already getting close to this efficiency limit. While it is true that further incremental progress is still possible, an alternative approach to solid-state lighting must be adopted if significant additional energy savings are to be realised.

One well-trodden route to far higher efficiencies and greater energy savings is to produce white light by colour mixing the direct emission from LEDs emitting different colours. One option is to mix red, green and blue, while a better colour quality is realised by combining red, amber, green and blue. An additional benefit of this phosphor-free approach is that it allows simple colour-tuning of light sources. This feature is desirable for mood lighting, and offers health and well-being benefits, by allowing artificial light to mimic natural daylight.

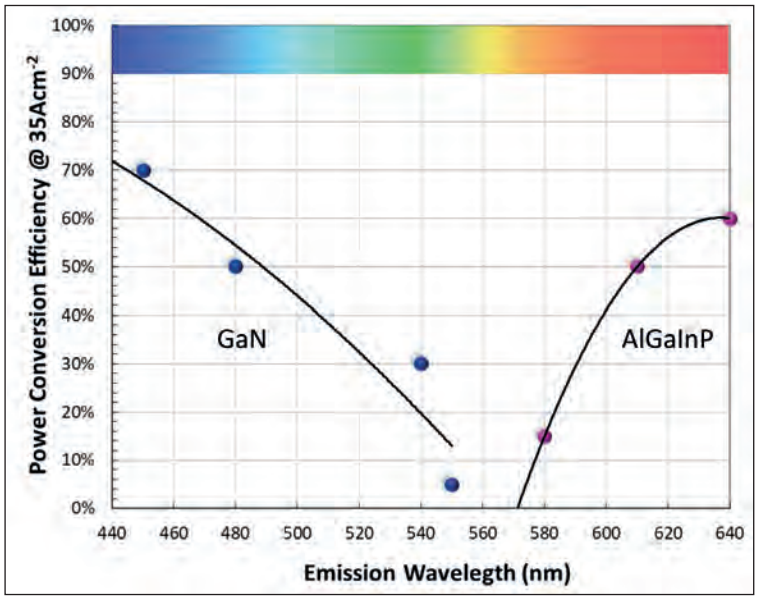

Figure 1: Power conversion efficiency for current state-of-the-art hexagonal-nitride and cubic-phosphide based LEDs.

The lighting industry is well aware of the revolutionary potential for colour-mixed LED architectures. Today, though, it remains a work in progress due to technical reasons, not least of which is the 'green gap' (illustrated in Figure 1, this is the substantial fall in efficiency in the green and amber regions of the spectrum spanning 500 nm to 600 nm). While blue LEDs based upon hexagonal InGaN and red LEDs based on cubic AlInGaP produce power-conversion efficiencies up to 70 percent, state-of-the-art green and amber devices are well behind, floundering in the 15 percent to 30 percent range.

LEDs based on the hexagonal InGaN system can, in principle, be flexed to produce emission not only in the green, but also the yellow, orange and red. However, once the indium content is increased to shift emission to 500 nm and beyond, efficiency tumbles due to the quantum-confined Stark effect. As the wavelength gets longer, built-in electric fields strengthen, pulling apart carriers and inhibiting radiative recombination.

While it's hard to get to the green when approaching this problem from the blue, at least it is possible. That's not the case when trying to go from red to green, using the cubic AlInGaP system, which is commonly used to manufacture highly efficient red LEDs. When the composition of this alloy is adjusted to try to deliver shorter wavelengths, the bandgap switches from direct to indirect, quashing light emission.

The inferior efficiency of green and amber LEDs is not so low that it prevents successfully implementation of white sources based on colour mixing. But the approach is far from ideal, as it requires more green and/or amber emitters, a solution that sacrifices the efficiency of the overall white device. Note that it's not a good idea to crank up the current through green and amber LEDs to boost their output power to that of the blue and red emitters, as droop is more prevalent, sending efficiencies even lower.

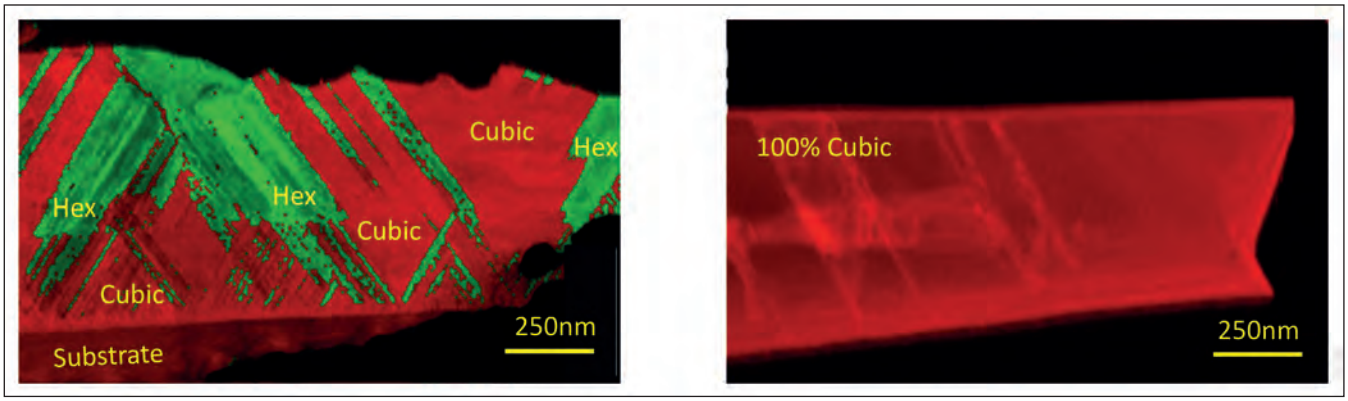

Figure 2. Nano-diffraction images, showing mapping (10 nm resolution) of the crystal phase of wafers produced using standard growth conditions (a) and Kubos's proprietary growth conditions (b). The red coloured pixels denote the cubic phase while those that are green denote the hexagonal phase. The growth starts predominantly cubic at the interface with the substrate, but under standard conditions growth breaks down, with increasing amounts of the hexagonal phase creeping in as the layer thickness increases. Using Kubos's proprietary growth conditions, growth can be managed to produce a single-phase cubic layer.

So, as you can see, the green gap is detrimental to the overall efficiency of any putative colour-mixing LED architecture for solid-state lighting, and until a viable solution is identified it is unlikely to be widely adopted. But despite these issues, this technology is still well worth pursuing. The US Department of Energy is encouraging its development, due to the potential for significant energy savings and carbon impact reductions, and has set a target of realising a 540 nm LED with an efficiency of 50 percent by 2025.

Filling the green gap

Efforts at addressing the green gap have tended to focus on combatting the quantum-confined Stark effect. Progress has resulted from reducing the impact of these electric fields, realised by rotating the crystal structure with respect to the LED stack. By growing the LED on substrates that have a surface parallel to a plane with a different crystal orientation – so-called non-polar or semi-polar orientations – the impact of the fields on device performance is eliminated or reduced. This leads to some improvements, but the efficiency and manufacturability of green LEDs remains problematic for solid-state lighting applications.

Our approach is more radical, using a fundamental change to the crystal structure of GaN to eliminate built-in electric fields. In conventional LEDs, GaN and InGaN form thermodynamically stable crystals with a hexagonal atomic structure. But these materials can also be produced in a cubic crystalline form, which is similar to the norm for the arsenides, phosphides and antimonides of gallium and indium. This cubic structure is inherently less prone to built-in electric fields and polarisation that blight the hexagonal system. So, if nitrides can be reliably produced with the cubic structure, cubic InGaN offers a potential solution to the green gap.

In addition to this benefit, there is another. For hexagonal GaN the near-band-edge emission is around 365 nm, while for cubic GaN it is around 387 nm. This means that less indium is needed in the

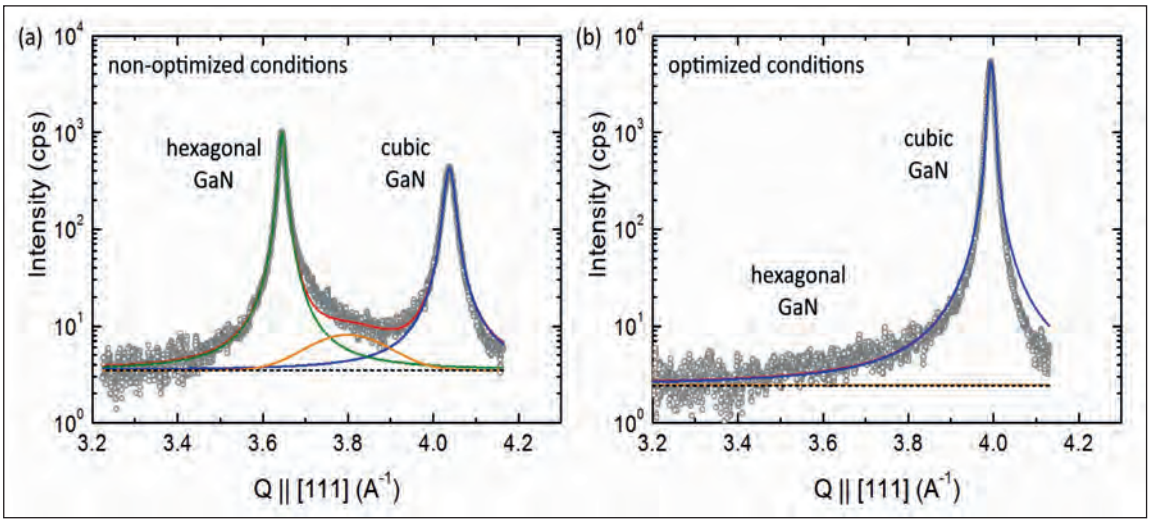

Figure 3. X-ray diffraction measurements using standard growth conditions (a) and Kubos's proprietary growth conditions (b).

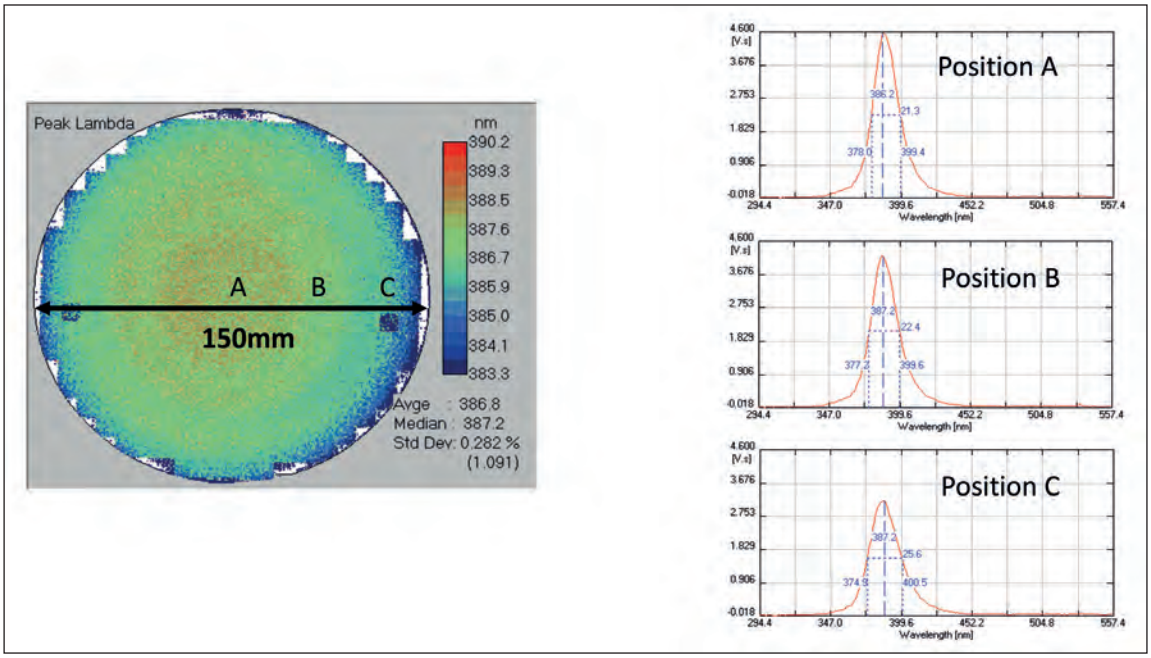

Figure 4. Photoluminescence map of near-band-edge emission from *n*-type cubic GaN grown on a 150 mm diameter wafer.

quantum wells of cubic green LEDs than in hexagonal LEDs made on conventional, non-polar and semi-polar planes.

It's rare to get advantages without a snag. With cubic GaN, the drawback is that it is hard to produce, due to the meta-stability of this crystalline form. But that is not a show-stopper – using a variety of means, several research groups have shown that is it possible to produce cubic GaN, albeit on small-area wafers. All these teams have benefited from a fortunate situation: although the energy difference between the hexagonal and cubic phases is small, the energy barrier to convert between them is very large. Consequently, once the crystal is locked into the cubic phase it is very difficult to convert it to the hexagonal phase. This is akin to the situation for graphite, the hexagonal form of carbon; and diamond, its cubic form: once diamond is formed it is not trivial to convert it to graphite.

Efforts at developing cubic GaN have been conducted on a variety of different substrates. Developers look for a foundation that combines a cubic symmetry with a relatively small lattice mismatch between the substrate and the GaN, because this stabilises the growth of the cubic phase.

Our approach is to take vicinal (001) silicon and grow a high-quality layer of 3C-SiC, which is the cubic and lowest-temperature polytype of SiC. With this choice of substrate the lattice mismatch is just 3.4 percent, and scaling production of LEDs is relatively straightforward – we can already use wafers up to 150 mm in diameter, with the possibility of being ported to 200 mm or larger in due course.

Given the propensity for GaN to form its usual hexagonal structure, the first challenge we faced was to confirm that the cubic phase could be reliably grown in a controlled fashion using industry-standard GaN MOCVD epitaxy equipment. Cross-sectional nano-diffraction images demonstrate that our proprietary growth conditions are able to yield a single-phase cubic layer (see Figure 2).

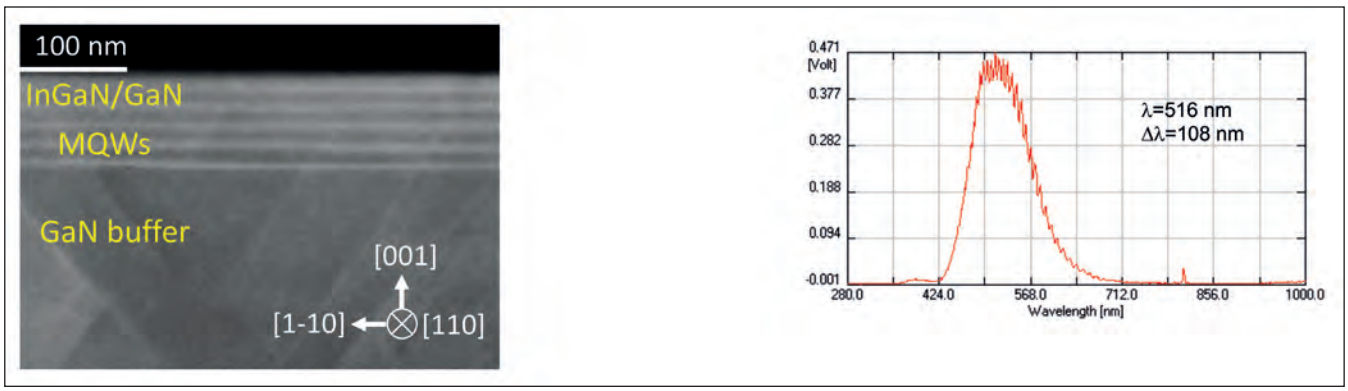

Figure 5. (a) Transmission electron microscopy image of cubic InGaN quantum wells and b) photoluminescence spectrum showing emission in the green gap region.

Further evidence of the success wrought by our proprietary growth conditions is provided by X-ray diffraction measurements that evaluate a rather more macroscopic volume of the sample by considering an area of several mm^2 (see Figure 3). Material produced with standard growth conditions features a strong hexagonal GaN peak in addition to the intended cubic GaN signature, while that produced with our proprietary conditions contains no evidence of hexagonal GaN.

Drawing on this success, we have applied our growth technology to the production of what we believe is the world's first pure cubic GaN film on a 150 mm diameter wafer. Photoluminescence mapping of this *n*-type cubic layer reveals that over almost the entire wafer there is the near-band-edge signature of cubic GaN with a peak at around 387 nm (see Figure 4). While there is still work to be done on optimising uniformity, this early result shows that cubic GaN can be reliably produced on large-area substrates using standard MOCVD growth equipment.

Building on these early steps we have continued to develop our technology and explore its potential, investigating its capability to deliver the game-changing benefits that theory predicts.

Such efforts include the growth and evaluation of InGaN multi-quantum wells grown in the cubic system (see Figure 5(a), which shows a cross-sectional electron micrograph of this structure). Under photoexcitation, the active region produces strong green emission centred on 516 nm, well into the green gap (see Figure 5(b)). Note that the indium content in the InGaN alloys in the quantum wells is far lower than would be required to achieve a similar emission wavelength in an equivalent hexagonal structure, confirming the promise offered by theory.

We have also investigated the impact of increasing quantum well thickness. In the hexagonal system, the quantum-confined Stark effect results in a significant decline in radiative recombination once the thickness of the quantum wells exceeds about 4 nm. To see if that issue occurs in the cubic material system, we produced a portfolio of samples with quantum-well thicknesses ranging from 2 nm to 10 nm, while maintaining a constant alloy composition. Photoluminescence measurements show that as

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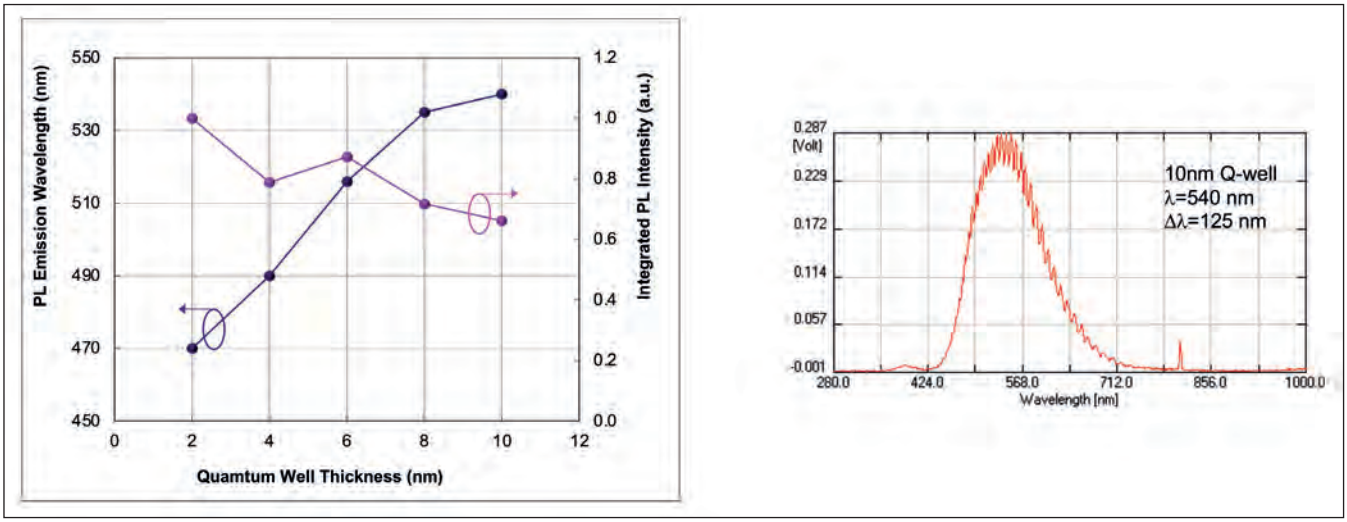

Figure 6. (a) The effect of cubic InGaN quantum well thickness on the emission wavelength and photoluminescence intensity. (b) The photoluminescence spectrum of 10 nm-thick InGaN quantum wells with a peak emission at 540 nm.

expected, the emission wavelength increases from around 470 nm for quantum wells 2 nm-thick up to 540 nm for a well thickness of 10 nm (see Figure 6). Encouragingly, as the well gets thicker, there is only a relatively small reduction in photoluminescence emission intensity.

Another challenge for conventional hexagonal GaN LEDs is 'efficiency droop'. This is a roll-off in efficiency as the drive current of a device is cranked up to increase the light output. There has been much debate about the origins of droop in conventional LEDs, and the consensus of opinion is currently that droop is caused by Auger processes leading to the non-radiative recombination of some of the carriers. Irrespective of the exact mechanism, the key to reducing efficiency droop is reducing the carrier density in the quantum wells at a given drive current and again the cubic form of GaN has the potential to address this.

Removal of the QCSE means that carrier lifetimes are much shorter in cubic GaN quantum wells, reducing carrier density. Also, the higher symmetry of the cubic crystal should mean that the Auger coefficient, which determines what fraction of carriers undergo Auger recombination, is lower than in hexagonal GaN. Although this benefit is yet to be demonstrated this is another reason why cubic GaN LEDs are of great interest.

From wells to devices

Recently, our efforts have turned to developing full LED structures in the cubic GaN system, with the aim of demonstrating electroluminescence from a cubic InGaN LED. Early prototypes show very promising results, highlighting the potential of producing GaN-based LEDs emitters across the full colour range from blue to red.

We expect to share results demonstrating green LEDs later in this year, ahead of a planned major funding round in early 2021. Ultimately, our aim is to produce a portfolio of intellectual property for licence. This will allow chipmakers to manufacture a full InGaN LED stack in the cubic system using a readily scalable technology on industry-compatible equipment platforms.

Although some tasks still need completing, the signs are that this unique technology could be the key that unlocks the solid-state lighting market for colour-matched LEDs, a move that will deliver energy savings that the world so craves.

Further reading

Energy Savings Forecast of Solid-State Lighting in General Illumination Applications published in December 2019 by DoE: www.energy.gov/sites/prod/files/2019/12/f69/2019_ssl-energy-savings-forecast.pdf

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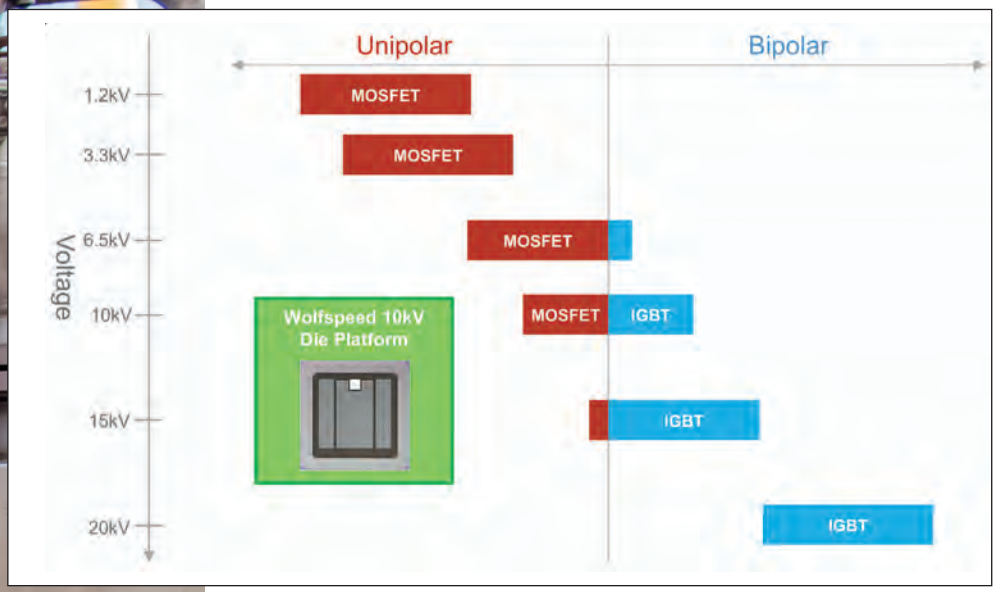
Evaluating the MOSFET and the IGBT

With a higher current than the SiC MOSFET but a need to be paired with a junction barrier diode, will the SiC IGBT see significant deployment in medium-voltage applications?

BY EDWARD VAN BRUNT FROM WOLFSPEED, A CREE COMPANY

RESEARCHERS have been enamoured with 4H-SiC high-voltage power devices for almost as long as high-quality monocrystalline material has been available on the market. Although the power industry is tending to focus on applications requiring devices with blocking-voltage ratings of 1200 V and below, the promise of efficient 4H-SiC medium-voltage power devices – that is, roughly in the range of 3.3 kV to 10 kV – is continuing to drive device development in this voltage space.

4H-SiC devices operating in this domain are seeing increased interest in applications that include medium-voltage motor drives, railway power transmission and direct grid connection of renewable resources. A virtuous circle is underway, with this interest driving more research in 4H-SiC medium-voltage transistors, with a focus on increasing the current rating of modules incorporating these novel power devices.



As the blocking voltage increases, the SiC IGBT offers a more suitable set of characteristics than the SiC MOSFET.

Well known in the silicon world, one option for boosting the current rating of power semiconductor devices is to switch from a unipolar power device to a bipolar variant. This move, which could be from a MOSFET to an IGBT, is being pursued in SiC, with success taking slightly longer than it did for silicon. Back in 2014 our team at Wolfspeed spearheaded the development of bipolar stable 4H-SiC power devices, and in 2018 we obtained qualification results for bipolar drift for 3.3 kV and 10 kV MOSFETs, clearing the final bar for commercialisation of medium-voltage 4H-SiC power devices.

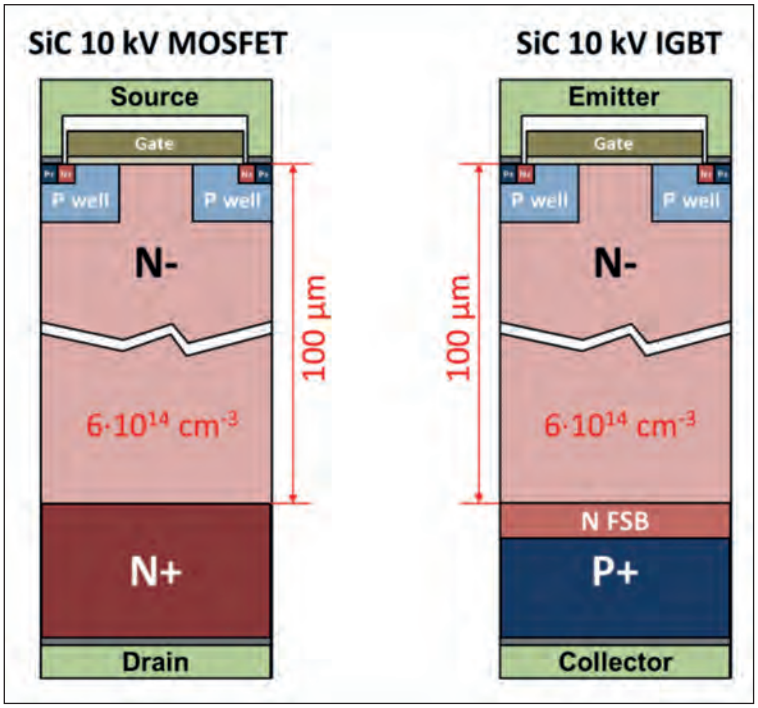
With all the technical and reliability hurdles cleared, the main question that remains is this: which device structure is better suited for medium-voltage applications, the MOSFET or the IGBT? It turns out that the answer isn't so clear-cut, just like it is for silicon power devices.

Making the switch to bipolar

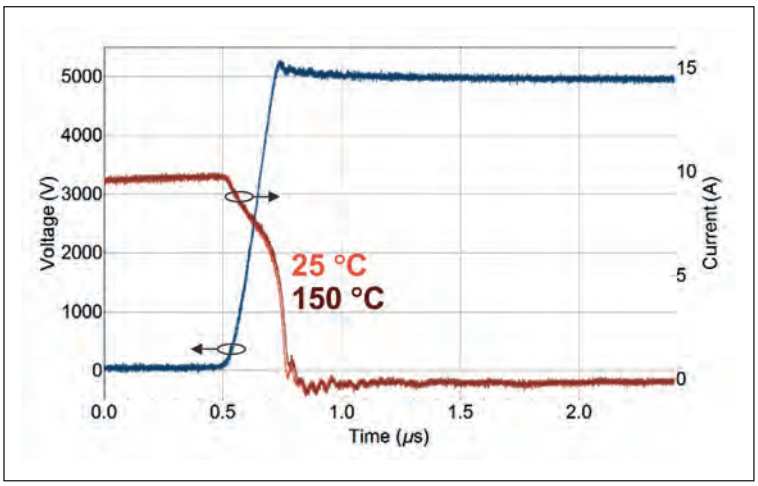
The transition voltage for making the switch to bipolar power devices in 4H-SiC is not based on a specific number or a cut-off mark. Instead, it depends on performance, and takes into account the relevant strengths and weaknesses of mature unipolar and bipolar SiC devices. MOSFETs are fast, so for low-voltage applications they will always be the best candidate. Meanwhile, at ultra-high voltages IGBTs are preferred, thanks to their low conduction loss that outweighs their slow speed. So, at both ends of the spectrum the ideal solution is clear. But what about the middle of the road, where the decision between using an IGBT or MOSFET is more complex?

If we make a 'back of the envelope calculation' to determine the voltage rating for the dividing line between the 4H-SiC unipolar MOSFET and the bipolar IGBT, and we appropriate a bit from silicon, we get a figure of 6.5 kV – that's ten times the voltage that silicon power devices start to gain a benefit from the IGBT. However, 6.5 kV might be a bit low. The unipolar resistance for SiC is 200 times lower than silicon, not 100 times lower; the SiC junction potential is 2.7 V, compared with 0.7 V in silicon; and the technology maturities are vastly different – silicon IGBTs are now in their seventh generation, while the SiC IGBT is still a R&D technology. So confounding factors are at play, indicating that a more in-depth analysis is required to understand where to mark the boundary. To shed some light on this, we have chosen an empirical approach, fabricating a 10 kV 4H-SiC IGBT and comparing its performance to that of our existing 10 kV 4H-SiC MOSFET.

Our 10 kV SiC IGBT is the first of its kind. When we designed this transistor, we used the exact same mask layout and blocking layer as the 10 kV MOSFET, with the exception of the drain/collector. This produced, as expected, the same blocking performance; however, in comparison to the 10 kV MOSFET, the 10 kV IGBT



Wolfspeed's 10 kV IGBTs were produced using the exact same mask layout and blocking layer as the 10 kV MOSFET, with the exception of the drain/collector.



The speed of turn-on (red) and turn-off (blue) is determined by the capacitance in the anti-parallel diode used alongside the SiC IGBT.

had a slightly negative temperature coefficient and a much higher DC current capability – it delivered 220 A cm^{-2}, compared with 70 A cm^{-2} for a MOSFET. Also, as anticipated, switching losses for the IGBT were higher, by almost a factor of 15, due primarily to the bulk stored charge and high emitter efficiency. Notably, the IGBTs have a very manageable change in voltage with time (the dV/dt is roughly 12 kV/µs). Operation in this manner dispels the notion that high-voltage SiC devices induce unmanageable electromagnetic interference due to their extreme speed. Another key consideration is that IGBTs do not have built-in antiparallel diodes like MOSFETs, so when evaluating these devices, it is essential to consider more than the switch itself.

A look at antiparallel diodes

One of the features of the 4H-SiC MOSFET body diode is its weak emitter-injection coefficient, which is an asset when it comes to switching loss. This means that a 4H-SiC MOSFET has a high-quality built-in antiparallel diode that can be used for switching purposes, unlike a silicon super-junction MOSFET, which suffers from high switching losses.

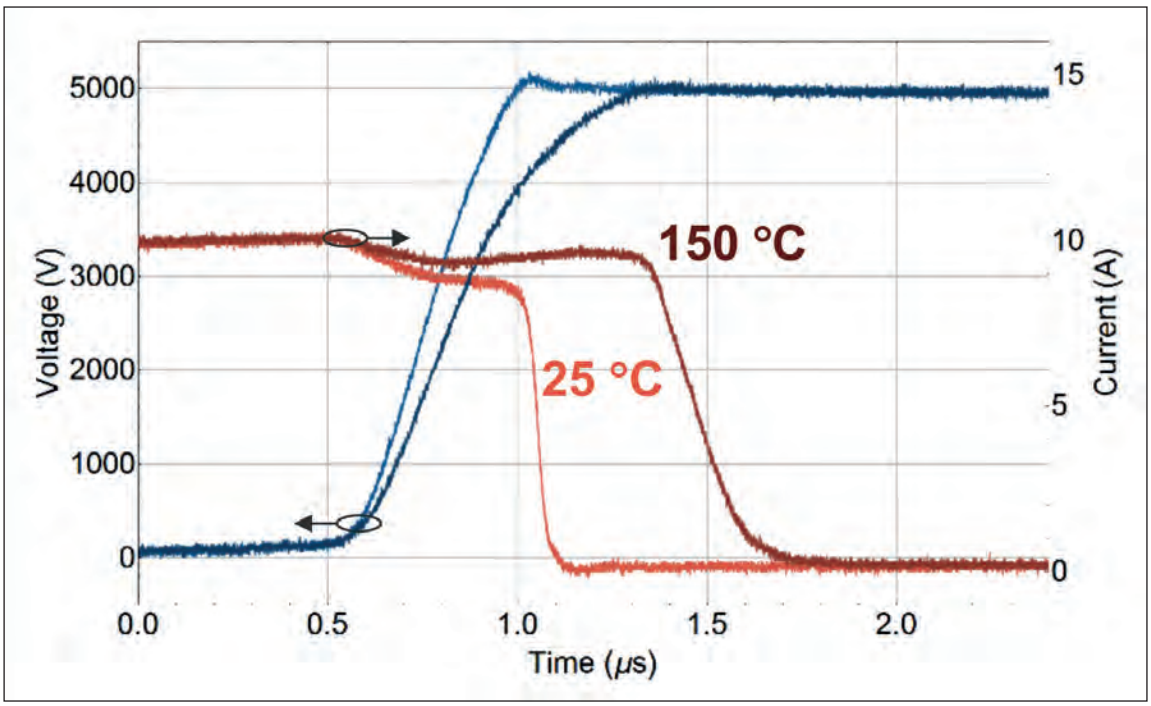
The 4H-SiC IGBT does not have a built-in antiparallel diode. Consequently, an additional antiparallel diode must be added, which is where a 4H-SiC JBS (junction barrier Schottky) diode comes into play. We have fabricated JBS diodes that have the same drift region as MOSFETs, but have a slightly larger active area and conduct current through an entirely unipolar mechanism.

High speeds and low switching losses are provided by both the built-in antiparallel diodes of the 4H-SiC MOSFET and the 4H-SiC JBS diode. The JBS diode switches incredibly fast, while the MOSFET is only just behind, having a slightly higher stored charge because of the weak emitter; and the JBS diode has a turn-on loss of 11.3 mJ, compared with 13.5 mJ for the MOSFET body diode. However, the MOSFET body diode has the upper hand when it comes to a higher current rating. Based on these characteristics, the MOSFET body diode should be viewed as great power diode, combining a high current rating with a switching performance that gives away very little to the IGBT.

Which is better?

The above characteristics – in isolation – provide a sense of what is going on. However, to put together a more comprehensive picture requires a model application, identifying the criteria where the 10 kV 4H-SiC IGBT may have an edge over the 10 kV MOSFET.

One leading application for 10 kV 4H-SiC devices is the medium-voltage motor drive, and in particular systems operating at 4160 V. Uses of these medium-voltage motor drives include performing vital tasks in energy production, industrial manufacturing and transportation. Motor drives based on 10 kV 4H-SiC



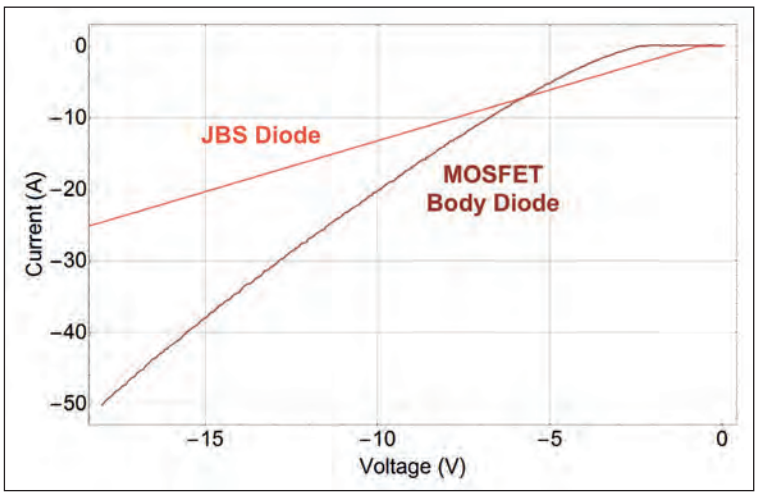
The SiC IGBT exhibits a very manageable dV/dt of roughly 12 kV/μs at room temperature (light red trace). Switching loss is dominated by bulk storage charge and high emitter efficiency as well as a very small current tail due to a low buffer lifetime.

devices promise to increase the efficiency of these systems, while trimming their size and weight. Given these opportunities, we have selected a three-phase inverter to model device losses for our 4H-SiC MOSFET and IGBT.

If you have a model application with various switching data for a 5 kV bus voltage at different operating currents you can use these data points with the current-voltage curves to model overall losses in an application. Notably, the MOSFET comes with its own diode. While the IGBT results in a higher current out of the active switch, based on the data of this particular model, it requires additional 0.64 mm^2 diodes (rather than using two MOSFETs and zero diodes, designers will need one IGBT and two diodes). Due to this, the MOSFET will continue to appear attractive as a high current device at the 10 kV voltage rating. This claim contrasts our 'back of the envelope' calculation and traditional wisdom gathered from silicon – that unipolar devices have long exhausted their worth at voltage ratings beyond 650 V.

Move to a lower system frequency design, and the active switch area required for an IGBT-based design is reduced. However, there is a trade-off, which is the area of the power module that must be dedicated to antiparallel diodes. As SiC MOSFETs have excellent body diodes, which is a strong selling point for these devices, compact high-frequency systems will assuredly use medium-voltage SiC MOSFETs. But even lower frequency systems can still benefit from MOSFET-only approaches, because they don't require additional diodes.

Our brief look at the needs of different applications has highlighted that the best approach must consider the details of a specific system. Both IGBTs and MOSFETs have attributes that make them attractive candidates for deployment in medium-voltage applications. The best choice depends on a variety of factors. Developments in SiC IGBTs will continue, making them an increasingly competitive option, especially at higher switching speeds, and with the development of additional technologies such as reverse-conduction capability, the balance of technologies employing 4H-SiC medium-voltage MOSFET technology may shift towards bipolar devices. For the last 30 years the silicon power device industry has continued to innovate its unipolar and bipolar technologies, and there are no signs this will stop. We should expect the same to hold true for 4H-SiC medium-voltage devices.



The MOSFET body diode (dark red) has a better current than the JBS diode. Current ratings: 30.6 A at T_J = 175 °C for 10 kV SiC MOSFET body diode; 17 A at T_J = 175 °C for 10 kV SiC JBS diode.

Surface-emitting superluminescent LEDs

Superluminescent LEDs that emit from the surface are easy to produce and combine laser-like quality with broadband emission, making them the ideal source for virtual and augmented reality applications

BY BERND WITZIGMANN FROM UNIVERSITÄT KASSEL, ALEXANDER TONKIKH AND ALVARO GOMEZ-IGLESIAS FROM OSRAM OPTO SEMICONDUCTORS, AND BRUNO JENTZSCH, AFFILATED TO BOTH THESE ORGANISATIONS

TABLETS AND SMARTPHONES are now multi-functional devices. Their latest models are equipped with an increasing number of virtual and augmented reality applications, supported by an advanced hardware environment. Key to providing these virtual and augmented reality functions are specialised output devices, such as head-mounted displays and pico-projectors; and input devices, such as tracking sensors and motion controllers.

The majority of these sensing and imaging functions are based on optics. An essential ingredient is an efficient, compact, high-power light source, which should be low in cost and widely available. Depending on the purpose, this source may be specified to operate in the infrared, the red, or to deliver emission in the yellow, green or blue.

For such applications, designers can select from a wide variety of semiconductor-based light sources. What they are looking for is emission from the surface, as this enables seamless integration into a system, alongside a narrow beam profile and the output of powerful pulses.

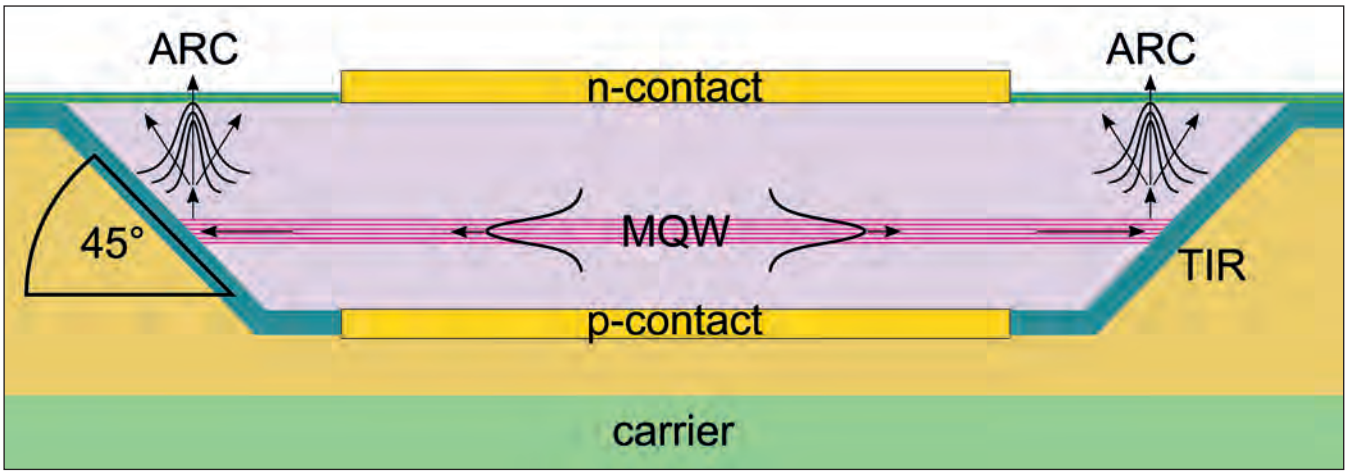


Figure 1. A cross-section of a surface-emitting superluminescent diode with two anti-reflection-coated emission windows. Using total internal reflection, 45°-mirrors deflect in-plane amplified optical modes out of the waveguide.

Fulfilling some of these criteria is the LED. It is a low-cost surface emitter, driven by spontaneous emission that determines the optical bandwidth and switching dynamics. Increasing the size of this chip boosts its output power. However, beam quality is poor.

An alternative is the vertical-cavity surface-emitting laser diode. It produces narrow far-fields, but requires sophisticated lateral-mode control. Due to this restriction, power is scaled by arranging multiple low-power emitters in a matrix, a solution that adds complexity. Additional pros and cons are a high power density, fast turn-on/-off transients, and a coherent output that adds speckle in interferometric sensors and imaging systems.

A far better option, sporting the merits of the laser and the LED, is a device known as the superluminescent LED (SLED). It combines laser-like beam properties with broadband emission similar to an LED; produces high output power densities; and has a short coherence length, much needed for visualization and sensing applications.

One drawback of the typical SLED is that it is designed as an edge emitter. This architecture dictates that the fabrication process must be similar to that of a laser diode and include wafer cleaving, followed by coating the facets. Producing devices with this approach requires the handling and testing of individual stripes or bars. This elaborate fabrication process adds cost, and has applied the brakes to growth of commercial sales of the SLED.

Success of the SLED has also been hindered by the need to suppress lasing – hence optical feedback at the mirrors is critical. Lasing is restricted by maximising light out-coupling and reducing feedback by engineering the level of losses. One upshot is that the typical SLED has a relatively low efficiency.

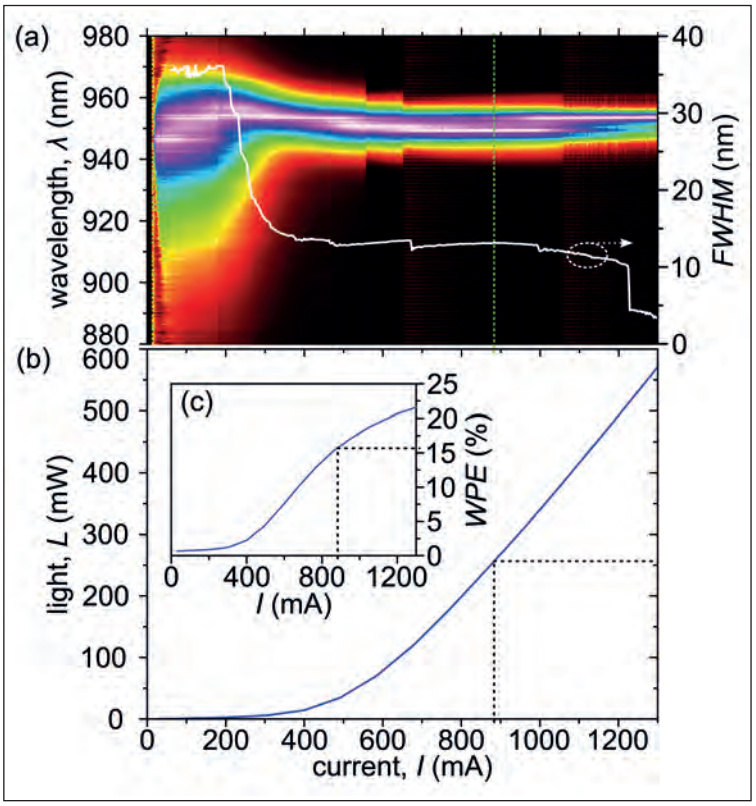


Figure 2. (a) Spectral evolution, (b) light-current curve and (c) wall-plug efficiency of a surface-emitting SLED with two micro-mirrors and anti-reflection-coated emission windows. Dotted lines mark the onset of lasing.

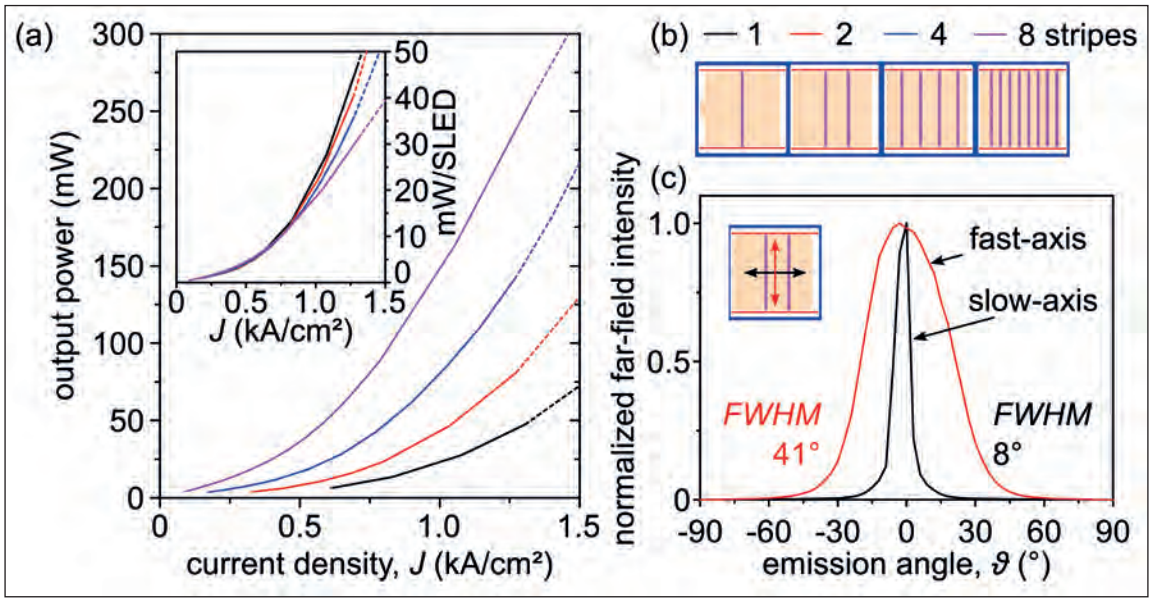


Figure 3. (a) Output power and (inset of (a)) output power per stripe for parallel aligned surface-emitting SLED arrays. The onset of lasing is marked by the dotted lines. (b) Top view illustration of investigated devices. (c) Far-field distribution of an array with two stripes measured in the directions of fast- and slow-axis.

Slashing costs

Our team from the Universität Kassel and Osram Opto Semiconductors have addressed several drawbacks of the conventional SLED by pioneering a design based on surface emission. This allows the device to be fabricated in a similar way to that of an inexpensive LED.

To amplify the spontaneous emission in our SLEDs, we have turned to an in-plane waveguide to ensure interaction of stimulated emission with a guided optical mode. This is similar to the approach employed in an edge-emitting device.

Another feature of our design is the termination of the waveguide by integrated micro-mirrors, which deflect in-plane optical modes via total internal reflection towards the surface of the chip. We form these mirrors with a conventional wafer-scale, dry-etching process.

The fabrication of our devices also involves bonding of the epiwafer to a new carrier, which is flipped prior to substrate removal. All other processing steps – including out-coupling surface treatments and final testing – are undertaken at the wafer-level, replicating the approach associated with thin-film LED production.

We mount our surface-emitting SLED chip *p*-side down on a carrier with a high thermal conductivity (see Figure 1). To minimise feedback into the in-plane waveguide containing multiple quantum-wells, we cover the outcoupling windows on the chip's surface with an anti-reflective coating. In principle, one side of the surface coating can be made highly reflective, to create a more compact chip with dual pass light propagation.

The epitaxial layers between the multiple quantum wells and the *n*-contact require careful design: they have to be thick enough to ensure current spreading to the unpumped mirror regions, but thin enough to prevent excessive beam broadening from the outcoupling mirror to the surface coating. Drawing on numerical simulation, we identified an optimum layer configuration. This has led to the fabrication of near-infrared emitters with a 500 μm cavity length and 50 μm waveguide that have promising electro-optical characteristics (see Figure 2 for details).

One feature of this design is the outcoupling of the optical power at both ends of the waveguide. This trims losses. Amplified spontaneous emission is maintained up to 250 mW, realised at a wall-plug efficiency exceeding 15 percent. The spectral width of this amplified spontaneous emission is around 10 nm.

When the drive current exceeds 900 mA, our device operates in lasing mode, thanks to the feedback of the surface out-coupler into the waveguide. This lasing threshold, realised for first-generation devices, will

Merits of our technology include the possibility to scale power and add further control of the far-field by producing arrays of surface-emitting SLEDs – this can be accomplished without any additional processing steps

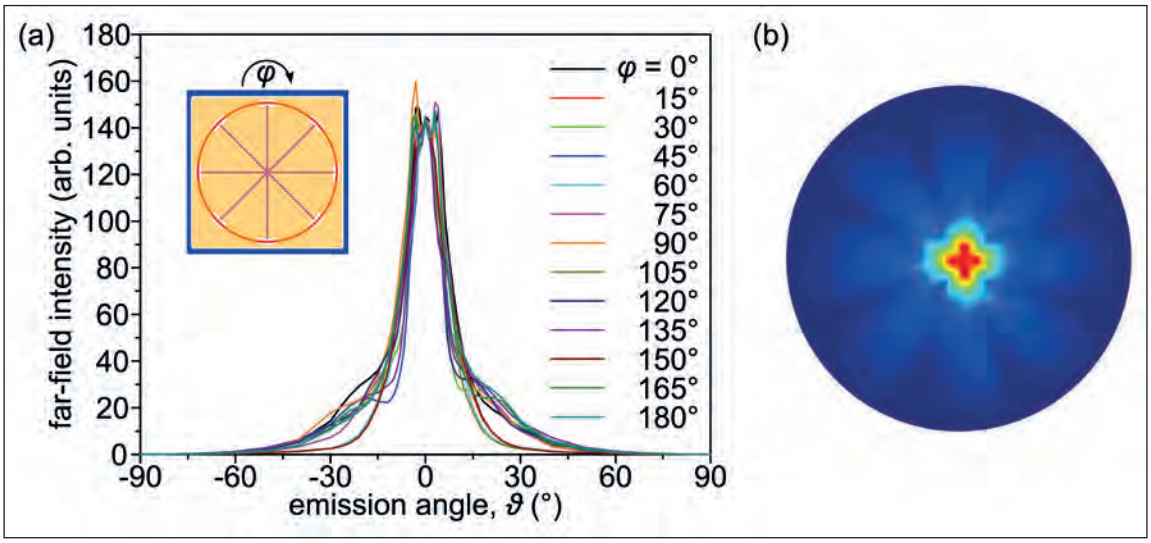


Figure 4. (a) Far-field pattern obtained at 15°-steps of a radial array with four overlapping waveguides. (Inset of (a)) Top-view schematic of the surface-emitting array. (b) Overview of the resulting radial symmetrical far-field.

increase as we optimise our anti-reflective coating. If we introduce small deviations in the outcoupling mirror angle from the 45° angle, this also reduces feedback, similar to curved waveguides for edge-emitting SLEDs.

We have also investigated pulsed, high-power operation. Initial experiments indicate rise- and fall times of just 3 ns and 2 ns, respectively. These values are shorter than those associated with LEDs, due to faster stimulated emission rates.

Promising profiles

Recording the far-field profiles from the two outcoupling windows at the ends of the surface emitting SLED reveal that the output profile, optical out-coupling and wall-plug efficiencies are comparable to that of a conventional edge-emitting device. To assess the efficiency of the surface outcoupling, we have carried out a direct comparison between as-cleaved edge-emitting devices and uncoated surface-emitting chips. Both designs deliver identical output powers, demonstrating the high quality and efficiency of the micro-mirrors, which are based on total internal reflection.

Merits of our technology include the possibility to scale power and add further control of the far-field by producing arrays of surface-emitting SLEDs – this can be accomplished without any additional processing steps. We have demonstrated linear and circular arrangement of SLEDs that offer power scaling (see Figure 3).

Due to heating and non-optimized current-spreading of our SLEDs, the power produced does not scale linearly with the number of waveguides on the chip. However, we do see a significant power increase in the regime where amplified spontaneous emission occurs. We have examined the far-field characteristics of a parallel surface-emitter array with two waveguide stripes, finding that the fast-axis has a Gaussian shape containing a full-width at half-maximum of 41°, and is symmetric to the surface normal of the chip. The profile of the slow-axis is markedly different, with a full-width at half-maximum from the array of just 8°. These values are comparable with those of a single-waveguide device, with the emission pattern of the individual stripes forming a well-matching, superposition-based beam profile.

We have created a symmetric optical far-field by arranging the waveguides of four SLEDs in a circular fashion on the wafer. The outcoupled optical power is located along a circle, with far-field measurements exhibiting circular symmetry (see Figure 4). A single top contact provides simultaneous electrical injection into all four waveguides. Thanks to the surface-emitting capability of our SLEDs, more advanced arrangements of contacts and waveguides are possible.

Our efforts show that surface-emitting SLEDs, featuring etched micromirrors for light outcoupling, are capable of meeting demands of advanced input and output devices for AR/VR technologies. Attributes of these devices include a good beam quality, low coherence, and a high power. While epitaxy required to produce our devices resembles that employed for the production of an edge-emitting laser, chip processing is compatible with large-scale LED processing, including mirror etching, bonding and the fabrication of a testing step. Highlights to date include a wall-plug efficiency exceeding 15 percent and a 250 mW output power for our 950 nm SLED. Operation at other wavelengths is sure to follow.

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Efficient, affordable semi-polar GaN

Patterned sapphire provides the foundation for low-cost semi-polar GaN with an internal quantum efficiency exceeding 50 percent

SEMI-POLAR PLANES of GaN are renowned for their combination of weak internal electric fields that aid radiative recombination, and the relative ease of forming indium-rich quantum wells, needed for green-emitting devices.

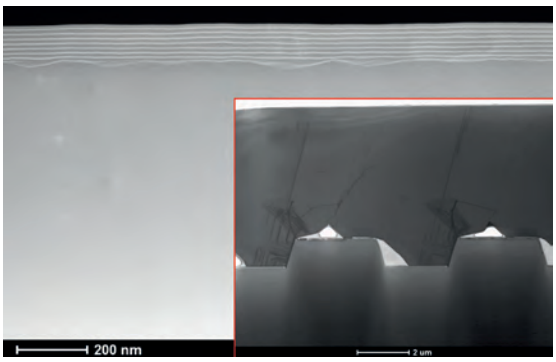
The downside of semi-polar is the astronomical price of native substrates – but the good news is that far cheaper sapphire-based variants are now showing much promise, thanks to the work of a Chinese team.

These researchers, working at Nanjing University, Hefei University of Technology and Jiangsu University, have produced semi-polar InGaN quantum wells on sapphire substrates with an internal quantum efficiency of more than 50 percent. Such a high value is encouraging for the realisation of efficient, affordable green LEDs and lasers.

"The quantum wells we obtained have a high crystal quality with low defect density, which is essential for a high internal quantum efficiency," says team spokesman Bin Liu from Nanjing University. "We should acknowledge the cooperation from Saphlux for the semi-polar GaN template."

Another attribute of these semi-polar quantum wells is that they produce a photoluminescence lifetime of just 0.5 ns, highlighting their potential as a source for high-speed communication. According to calculations, a -3 dB modulation bandwidth of 1.4 GHz is achievable – and even higher data rates could be realised with advanced modulation schemes. However, Liu says that today the modulation bandwidth is limited to around 500 MHz, because device quality is insufficient for handling high injection currents.

He and his co-workers produced a portfolio of samples by taking sapphire substrates patterned with 3 μm-wide, 1 μm-thick grooves, loading them into an MOCVD chamber, and growing heterostructures featuring eight quantum wells. By employing a range of temperatures for the growth of the wells, their composition varied.



Transmission electron microscopy (TEM) cross-sectional image of a semi-polar (20$\bar{2}$1) InGaN/GaN multiple quantum-well sample. The inset is a TEM cross-sectional image of the semi-polar (20$\bar{2}$1) GaN template.

Examining these structures by cross-sectional transmission-electron-microscopy revealed a blurred interface for the first quantum well, followed by seven quantum wells with straight, clear interfaces (see Figure). According to the team, the blurred interface is probably caused by the non-smooth surface of the underlying GaN.

By conducting photoluminescence measurements at a range of temperatures, the team deduced values for internal quantum efficiency of 33 percent, 52 percent and 25 percent for the semi-polar (20$\bar{2}$1) samples with emission peaks at 404 nm, 460 nm and 497 nm, respectively.

Liu and co-workers have proposed a model to account for these variations in internal quantum efficiency. It is suggested that localisation centres are deeper in the 460 nm sample than that emitting at 404 nm, decreasing the likelihood that carriers will reach non-radiative centres. Despite having even deeper localisation centres in the 497 nm sample, the higher indium content leads to degradation of crystal quality, and in turn increases defects and quashes radiative recombination.

One of the next goals for the team is to increase the crystal quality of its semi-polar GaN, especially in the range 530 nm to 560 nm.

"Based on semi-polar orientations, we plan to realise microLEDs that are used for full colour display, with the characteristics of high reliability and high speed," says Liu.

This effort will build on work undertaken last year, which realised microLEDs with minor colour shifts, minimal droop, and an external quantum efficiencies of 62 percent at a drive current of nearly 800 A cm^{-2}.

Liu and colleagues will also develop VCSELs with very short carrier lifetimes. "We plan to reach a semi-polar light source with a modulation bandwidth larger than 1 GHz."

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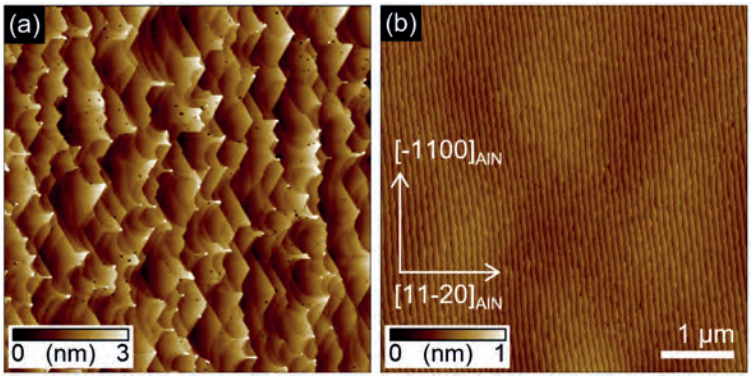
Double sputtering enhances AlN

A sputtering and annealing process yields AlN films with a very low threading dislocation density

RESEARCHERS at Mie University, Japan, are claiming to have set a new benchmark for the material quality of AlN films grown on sapphire.

Spokesman for this team, Hideto Miyake, says that their AlN films, produced by a combination of sputtering and annealing have a threading dislocation density of around 4 x 10^7 cm^{-2}.

Miyake believes that these films provide one of the best options for making deep-UV LEDs, which are attractive candidates for medical and biochemical treatment, water purification and solar-blind detection. Using AlN with a lower threading dislocation density as a foundation for device growth enables higher external quantum efficiencies and superior reliability.



Atomic force microscopy reveals: (a) bunched steps structures in sputtered AlN films that have been annealed; and (b) smooth epilayers with atomic steps for the AlN epilayers grown on these templates.

The more common method for growing AlN films on sapphire, MOCVD, is inferior. Threading dislocation densities are typically 2-3 x 10^8 cm^{-2}, and although patterning sapphire can reduce this, gains are modest.

"In any case, for achieving sufficiently low threading dislocation densities with MOCVD, engineers need to grow relatively thick AlN films, typically a few micrometres," says Miyake.

In comparison, the combination of sputtering and high-temperature annealing yields far thinner films with a superior material quality.

Fabrication of the films began by sputtering a 600 nm-thick layer of AlN. After this, the researchers placed the surface of this AlN up against another AlN-on-sapphire template, prior to annealing at 1725 °C for 3 hours.

"With this configuration, the AlN films can be effectively protected against temperatures as high as 1700 °C," explains Miyake.

Without this face-to-face method, nitrogen gas with a pressure of thousands to tens of thousands of atmospheres would be needed to suppress desorption of nitrogen atoms.

Sputtering of a second AlN film that is also 600 nm-thick followed, prior to a second face-to-face annealing step at 1725 °C for 9 hours.

Atomic force microscopy revealed that annealing converted the columnar AlN formed by sputtering to bunched stepped structures (see figure).

Miyake and co-workers used MOCVD to deposit a 200 nm-thick AlN film on their template. According to measurements made by atomic force microscopy, this epilayer has clear atomic steps and a root-mean-square roughness of just 0.1 nm over a 2 μm by 2 μm area.

X-ray diffraction measurements on the sputtered and annealed film produced peaks that enabled an estimate for the total dislocation density of 5.9 x 10^7 cm^{-2}. Similar measurements on samples with a 200 nm-thick layer of MOCVD-grown AlN produced values indicating that the low threading dislocation density in the sputtered film is retained in the MOCVD-grown AlN epilayer.

The team have also scrutinised their material with plan-view transmission electron microscopy. Inspecting an area of 8 μm by 8 μm provided a figure for the dislocation density of 4.3 x 10^7 cm^{-2}. The team attribute the difference between this lower value and that obtained by X-ray diffraction to a blocking effect around the interface between the first and second growth of the sputtered AlN film.

Using high-angle annular dark-field scanning transmission-electron-microscopy, Miyake and colleagues uncovered a high concentration of oxygen at the interface between the two growths of AlN.

This oxygen-rich region is thought to create a polarity inversion that terminates, or possibly bends, some dislocations formed during the first growth of AlN.

The team are now using their templates to develop deep-UV LEDs. They are also keen to investigate whether their foundation could enhance other devices, including high-power, high-frequency HEMTs.

Reference

D. Wang *et al.* Appl. Phys. Express **13** 095501 (2020)

Pioneering AlInN power diodes

Fabrication of the first AlInN diodes provides an initial step towards a leap in performance for power switching

Researchers at Lehigh University have broken new ground by reporting the first results for power devices based on AlInN. This team, led by Nelson Tansu and Jonathan Weirer, has fabricated a quasi-vertical bipolar diode containing highly doped *p*-type GaN and a low-doped *n*-type $Al_{0.82}In_{0.18}N$ drift layer.

Efforts by these researchers are building on the development of GaN-based vertical power devices, which offer a superior alternative to those made from silicon and SiC. GaN-based vertical power devices have the upper hand on many fronts, including the capability to handle higher power densities and operating temperatures, switch at higher speeds, and provide higher blocking voltages.

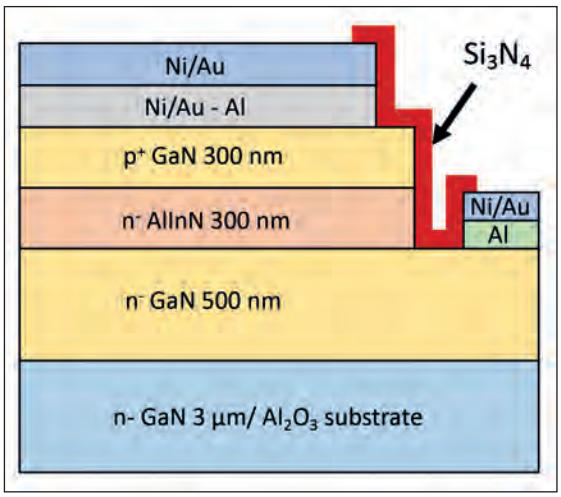
Introducing $Al_{0.82}In_{0.18}N$ propels the GaN-based vertical power device into the ultra-wideband gap realm, where it competes alongside the likes of AlGaN, Ga_2O_3, diamond and cubic BN.

For devices operating at low switching frequencies, a useful metric for comparing performance is Baliga's figure of merit. This yardstick – defined as the square of the blocking voltage, divide by the specific on-resistance – is 33 GW cm^{-2} for $Al_{0.82}In_{0.18}N$, thanks to a bandgap of around 4.4 eV and an electron mobility of 450 $cm^2 V^{-1} s^{-1}$. In comparison, the figure of merit for GaN is just 14 GW cm^{-2}, while values for Ga_2O_3 and AlGaN are 37 GW cm^{-2} and 41 GW cm^{-2}, respectively.

Although $Al_{0.82}In_{0.18}N$ is slightly behind Ga_2O_3 and AlGaN when judged in terms of Baliga's figure of merit, it has the upper hand when it comes to doping – both *n*-type and *p*-type doping are proven.

Development of the team's AlInN power devices began by evaluating the growth of an AlInN epilayer on *n*-type GaN-on-sapphire templates. A 300 nm-thick AlInN layer had a root-mean-square roughness of 3.5 nm, a typical value for this ternary that is known to be plagued with V-defects and threading dislocations. According to Hall measurements, the *n*-type carrier concentration of this team's AlN-on-sapphire template is 2 x 10^{17} cm^{-3}, and it has an electron mobility of 370 $cm^2 V^{-1} s^{-1}$.

This low-doped, latticed-matched $Al_{0.82}In_{0.18}N$ has been incorporated into the heterostructure of a power diode (see figure). Device fabrication began by forming a 60 μm-diameter *p*-contact by electron-beam lithography and etching, and then annealing under nitrogen gas for 60 s to ensure ohmic behaviour. Etching with an inductively coupled plasma created a 60 μm-diameter mesa, exposing the underlying



A highly doped *p*-type GaN layer and a lightly doped *n*-type AlIN drift layer form the main junction of the AlIN power diode.

n-type GaN contact layer, before addition of a 2 μm-thick layer of aluminium created the cathode contact surrounding the circular mesa.

To aid probing, the researchers deposited and patterned a Ni/Al film on both metal contacts. The addition of a Si_3N_4 passivation layer by plasma-enhanced CVD and the removal of the metal from the contact areas by etching completed device fabrication.

Measurements on the diodes revealed a breakdown voltage of around 60 V, limited by leakage current; and a specific on-resistance of 0.53 mΩ cm^{-2}, held back by the spreading resistance within the *n*-type GaN contact layer and at the interface between the *n*-type AlInN and *n*-type GaN.

Under forward bias, the team's diode produced strong photoluminescence at 2.51 eV to 2.67 eV. This emission, well below the bandgaps of GaN and AlInN, is thought to originate from an unintentional quantum well created by the diffusion of indium from AlIN to *p*-type GaN.

Eliminating this well through better control of the growth of *p*-type GaN, as well as switching to a GaN substrate, should reduce the reverse leakage current and increase the breakdown voltage. Introducing a GaN substrate should also eliminate lateral current spreading and trim the specific on-resistance, which could fall further through the incorporation of interlayer and doping designs that reduce resistances from the AlInN/GaN heterojunction.

Reference

M. Peart *et al.* Appl. Phys. Express **13** 091006 (2020)

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