Shifting to 200 mm silicon carbide

GT ADVANCED TECHNOLOGIES

200 mm

150 mm

76 mm

100 mm

50 mm

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INSIDE
News, Analysis, Features, Editorial View, Research Review and much more

II-VI'S GOLDEN ANNIVERSARY

A candid interview with II-VI co-founder Carl Johnson offers a wonderful insight into the early years

PROBLEMATIC POINT DEFECTS

The intrinsic light-quenching point defect is dragging down the efficiency of GaN-based LEDs

MORE MARKETS FOR MICROLEDS

Many opportunities beckon for light engines made with microLEDs that vary in pitch, size and wavelength

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VIEWPOINT

By Dr Richard Stevenson, Editor

Crystal clear objectives

In general, our industry is propelled by advances in device design, as this opens up new markets and swells sales. However, there are times when progress comes from other breakthroughs. Examples include the development of a new metrology techniques offering valuable insight, computational software that holds the key to designing a better chip, and the growth of larger crystals that unlock the door to producing more devices at lower cost.

During the latter years of the twentieth century, engineers devoted much effort to increasing the size of the GaAs substrate, as this supported a ramp in volumes of devices for switching and amplifying RF signals in mobile phones. By the turn of the millennia, leading fabs had installed 150 mm lines, which are still at the forefront of production today.

Now it is SiC that is seeing a shift to larger substrates to support an increase in the production of power devices, including those deployed in electric vehicles. Twenty years ago, producers of this foundation could only offer a limited supply of 50 mm substrates, but today 150 mm is the norm, and there are well-publicised moves to manufacture diodes and MOSFETs on a 200 mm variant. Cree's Wolfspeed arm is already building a massive fab for that dimension, and this summer STMicroelectronics joined the ranks of companies that can fabricate SiC substrates of this size.

One company helping the growers of SiC material to upgrade their output to the larger size is GT Advanced Technologies. Its contribution is welcome, because scaling of SiC is not easy, due to the lack of growth from the melt. Several alternative technologies are available, offering differing levels of maturity, with physical vapour transport leading the way (to find out why, head to p. 20).

A major supplier of SiC is II-VI, which lay claim to producing the world's first 200 mm SiC substrate back in 2015. This multi-national, celebrating its fiftieth anniversary this year, has crystal growth in its DNA. Just turn to p. 28 to hear directly from the company's first leader, Carl Johnson, on how his PhD work on cadmium telluride in the late 1960s led him to meet his co-founder, a crystal grower named James Hawkey, and go on to start a company.

To ensure the success of this start-up, the founders had to master the growth of cadmium telluride, a material needed for carbon dioxide lasers. The duo went through some tricky times, blowing up furnaces far too frequently, but by drawing on their complementary skills and staying positive, they got through this setback and began to grow the company.

As well as his great business acumen, Johnson must be admired for what he's giving back to our industry. Through the II-VI Foundation that he's initiated and funded, he is helping to bring on a new generation of scientists and engineers. Who knows, some might even go on to be the crystal growers of tomorrow, underpinning further advances within our industry.

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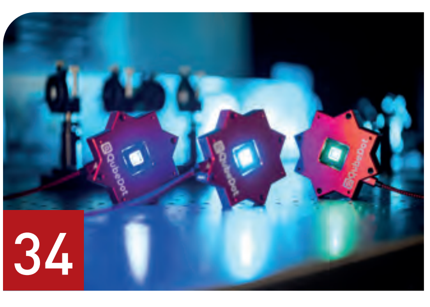

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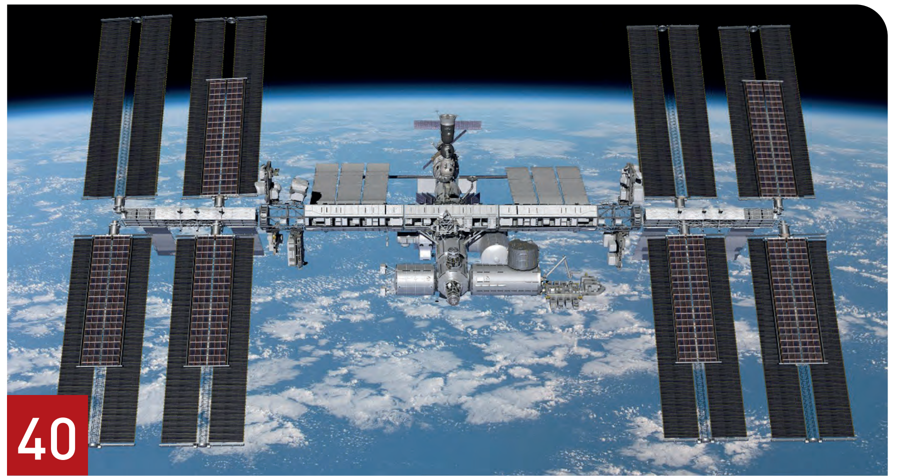
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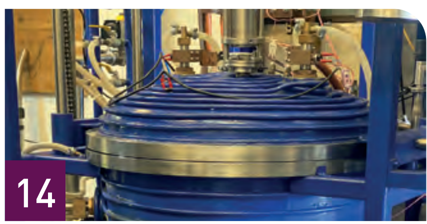
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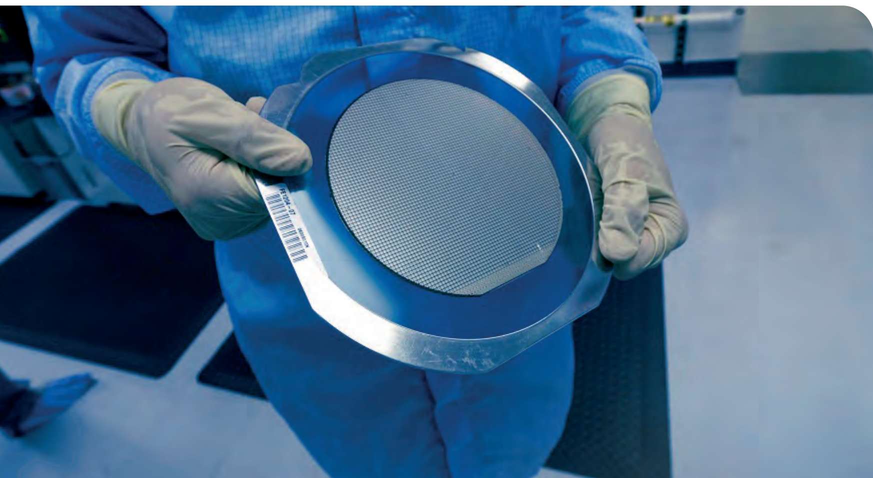
Cree and ST expand SiC wafer agreement

CREE (through its Wolfspeed business) and STMicroelectronics have announced the expansion of an existing multi-year, long-term SiC wafer supply agreement. The amended agreement, which calls for Cree to supply ST with 150 mm SiC bare and epitaxial wafers over the next several years, is now worth more than $800 million.



“This latest expansion to our long-term wafer supply agreement with Cree will continue to contribute to the flexibility of our global SiC substrate supply. It will continue to contribute importantly to our global SiC supply, complementing the other external capacity we have secured and the internal capacity we are ramping. The agreement will help meet the high volumes required by our product manufacturing operations in the next years, with a large number of automotive and industrial customer programmes in high volumes or ramping up,” said Jean-Marc Chery, president and CEO of STMicroelectronics.

The adoption of SiC-based power solutions is rapidly growing across the automotive market as the industry moves from internal combustion engines to electric vehicles, enabling greater system efficiencies that result in electric cars with longer range and faster charging, while reducing cost, lowering weight and conserving space. In the industrial market, SiC solutions enable smaller, lighter and more cost-effective designs, converting energy more efficiently to unlock new clean energy applications.

To better support these growing markets, device manufacturers are interested in securing access to high-quality SiC substrates to support their customers. “We are very pleased that STMicroelectronics will continue to leverage Wolfspeed SiC materials as part of their supply strategy for the next several years,” said Cree CEO Gregg Lowe. “Our long-term wafer supply agreements with device manufacturers now total more than $1.3 billion and help support our efforts to drive the industry transition from silicon to SiC.”

Lowe added: “Our partnerships and significant investments in increased production capacity ensure we are well positioned to capitalize on what we believe to be is a multi-decade growth opportunity for SiC-based applications.”

Infineon and Panasonic accelerate GaN development

INFINEON TECHNOLOGIES and Panasonic have signed an agreement for the joint development and production of the second generation (Gen2) of their proven GaN technology, offering higher efficiency and power density levels.

The high performance and reliability combined with the capability of 200 mm GaN-on-silicon wafer production mark Infineon’s strategic outreach to the growing demand for GaN power semiconductors.

In accordance with market requirements, Gen2 will be developed as 650 V GaN HEMT. The devices will allow for ease of use and provide an improved price-performance ratio, targeting, amongst others, high- and low-power SMPS applications, renewables, motor drive applications.

“In addition to the same high-reliability standards as for Gen 1, next-generation customers will benefit from even easier control of the transistor as well as a significantly improved cost position, thanks to moving to an 8-inch wafer manufacturing,” says Andreas Urschitz, president of Infineon’s Power and Sensor Systems Division.

Like the jointly developed Gen 1 devices, known as Infineon’s CoolGaN and Panasonic’s X-GaN, the second generation will be based on the normally-off GaN-on-silicon transistor structure.

This, in combination with the unmatched robustness of the hybrid-drain-embedded gate injection transistor structure, is claimed to make these components the product of choice and one of the most long-term reliable solutions in the market.

“We are delighted to extend our partnership and collaboration with Infineon on GaN components. Within the joint approach, we will be able to apply Gen1 and Gen2 devices on high quality and based on latest innovation developments”, says Tetsuzo Ueda, associate director of Engineering Division, Industrial Solutions.

The market launch of the new 650 V GaN Gen2 devices is planned for the first half of 2023.

AlScN project wins German innovation prize

THE Fraunhofer Institutes IAF and IIS together with the University of Freiburg/ INATECH netted second place with their joint project *EdgeLimit – Evaluation of Power Electronics in Modern Edge Cloud Systems* in the innovation competition *Electronics for Energy-Saving Information and Communications Technology* launched by the German Federal Ministry of Education and Research (BMBF).

The project EdgeLimit presents a concept for the use of novel power semiconductors for high-frequency amplifiers in 5G base stations for the new millimetre-wave frequency range at 26-34 GHz based on aluminum scandium nitride (AlScN). The project not only offers enormous potential savings in energy consumption and CO_2 emissions, but also an extraordinary level of innovation in the field of high-frequency electronics with a major leverage effect for microelectronics in Germany. This finds expression in the significant participation of industry in the second phase of the project, with a planned cooperation with Nokia Bell Labs, United Monolithic Semiconductors, Deutsche Telekom and Nokia Solutions and Networks.

Modern networked ICT systems increasingly have capacities for collecting and processing information at the edge of the network in addition to the central data-processing infrastructures (cloud), as well as systems for transferring data between cloud and edge.

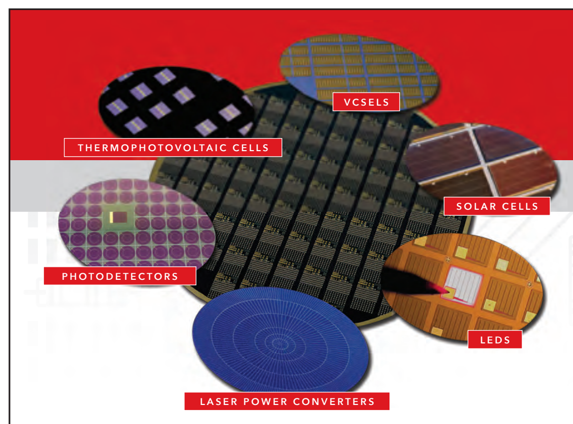
"This is where the EdgeLimit project comes in," says project coordinator Rüdiger Quay. "Our goal is to realize a complete antenna system, a so-called Remote Radio Head (RRH), which will enable more energy-efficient transmission in the millimeter-wave range of 5G while halving losses at the same time."

"We are working, for example, on intelligent edge solutions that take energy consumption into account during the design phase and reduce it to a minimum," says Albert Heuberger, Director of the Fraunhofer Institute for Integrated Circuits. By looking at the energy consumption of the radio units (massive MIMO antennas) in the 5G Testbed Industry 4.0 at Fraunhofer IIS, energy-efficient, distributed, secure edge cloud systems can be built and tested.

"The semiconductor technology we are pursuing, with which we have already gained a lot of experience at IAF, has the potential to fundamentally increase power efficiency in integrated circuits (MMICs) through better matching, higher gain and higher power density," elucidates Quay. Due to its high current-carrying capacity, AlScN allows significant advantages over established semiconductors such as silicon, GaAs and AlGaN/GaN. Based on this material, EdgeLimit aims to at least double power efficiency at the amplifier-level in new cellular frequencies as well as halve losses in power converters. More energy-efficient electronics alone cannot counter the exponentially increasing energy consumption of ICT. The horizon of physical energy efficiency is closer than that of the realizable data throughput, which is growing faster and thus promoting a rebound effect. One solution is the intelligent and adaptive management of mobile communications systems, which ensures that energy is used as needed – an approach with enormous energy-saving potential.

To enable smart ICT, innovative power electronics architectures are required that allow electronics to be switched on and off as needed without compromising the latency of data transmissions.

"At the network level, large amounts of energy should be saved by intelligently networking transmission modules and antennas with on-demand control, for example in factory networks such as the new Bosch semiconductor fab in Dresden or for fast video transmission to cars," says Quay. "For this purpose, we are developing the necessary high-frequency electronics in EdgeLimit that are capable of being connected to intelligent network management. Because one thing is certain: In the further development of ICT, we must give resource efficiency at least the same priority as performance enhancement. This is the only way to reduce CO_2 emissions as digitization advances."



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Onsemi acquires GT Advanced Technologies for $415 million

ONSEMI, a US supplier of intelligent power and sensing technologies, and GT Advanced Technologies, a US producer of SiC, have announced that they have entered into a definitive agreement under which Onsemi will acquire GTAT for $415 million in cash.

The transaction is expected to better position Onsemi to secure and grow supply of SiC and meet rapidly growing customer demand for SiC-based solutions in the sustainable ecosystem, including EVs, EV charging and energy infrastructure.

Founded in 1994 in Hudson, New Hampshire, GTAT manufactures SiC and sapphire materials for high-growth markets.

Combining Onsemi's manufacturing capabilities with GTAT's technical expertise will accelerate SiC development and position Onsemi to better serve customers as the sustainable ecosystem rapidly ramps up over the next decade. This enhanced SiC capability will allow Onsemi to assure customers of supply of critical components and to further commercialize intelligent power technologies.

"This transaction reflects our confidence and stated commitment to meaningfully invest in SiC solutions to support the creation of intelligent power and sensing technologies to help build a sustainable future," said Hassane El-Khoury, president and chief executive officer of Onsemi.

"We are focused on deepening our leadership and innovation in game-changing technologies that support the automotive and industrial sectors, and GTAT brings outstanding technical capabilities and expertise in developing wafering-ready SiC, which we intend to accelerate and expand to better empower customers in our high-growth end markets. We look forward to welcoming GTAT's talented employees to the Onsemi team and driving innovation together."

"Today's announcement marks the start of a new chapter for GTAT and is a testament to the value created by the hard work and strength of our team," said Greg Knight, president and chief executive officer of GTAT. "Onsemi is strategically positioned to scale our capabilities, providing the resources and platform to maximize the potential of our cutting-edge production techniques and ensure we remain on the forefront of advanced crystalline growth."

The acquisition also reinforces Onsemi's commitment to make substantial investments in disruptive, high-growth technologies, consistent with the company's recently announced 2025 target financial model described during its Analyst Day presentation. As Onsemi previously stated, capital expenditures are expected to be approximately 12 percent of revenue in 2022 and 2023, as Onsemi invests to drive differentiation and leadership, including in SiC. The transaction is not expected to impact the company's 2025 target financial model.

Onsemi plans to invest in expanding GTAT's research and development efforts to advance 150 mm and 200 mm SiC crystal growth technology, while also investing in the broader SiC supply chain, including fab capacity and packaging.

The transaction, which has been unanimously approved by the Boards of Directors of Onsemi and GTAT, is expected to close in the first half of 2022. Completion of the transaction is subject to regulatory approvals and other customary closing conditions. Approval of Onsemi's stockholders is not required in connection with the proposed transaction.

Onsemi intends to fund the transaction through cash on hand and available capacity under its existing revolving credit facility. The company expects the transaction to be marginally dilutive to its non-GAAP earnings per share in the immediate term and to be accretive within one year after close.

Vector Photonics receives £600,000 for TITAN project

VECTOR PHOTONICS has received £600k for the newly awarded project called TITAN: PhoTonIc CrysTal LAsers for EtherNet applications. The funding will drive the development of PCSELs for low-power consumption optical interconnections between servers in hyperscale data centres. Of the total project value, £300,000 has come from Innovate UK's Investor Partnership Programme. This has been match-funded by private investment from UKI2S, a specialist, deep-tech seed fund for UK-based, research spinouts; the Scottish Growth Scheme; and Equity Gap.

Neil Martin, CEO of Vector Photonics, said: "The rising power usage of hyperscale data centres is being driven by escalating demand from network-connected devices, such as smartphones, PCs and the IoT. Hyperscale data centres currently rely on high-performance lasers for the optical interconnects between servers."

These lasers require so much electrical power to operate that it is the heat they create, and the energy used by the systems cooling them, that have become the limiting factors to any increases in optical performance.

"The TITAN project will fund the early-stage development of PCSELs, which aim to solve this major heat problem. PCSELs require only half the electrical power of the incumbent lasers, for the equivalent system performance. Less heat is produced and less energy is used for cooling. Since we anticipate the system optical performance requirements of next-generation, hyperscale data centres increasing in future, it is only low-power consumption systems using PCSELs that can realistically facilitate this increase."

Trumpf unveils new VCSEL laser platform

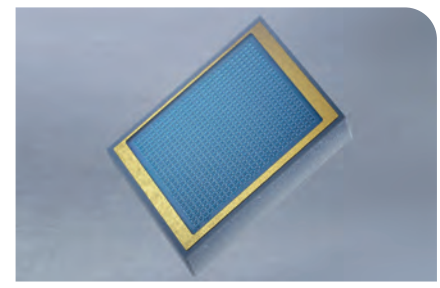
TRUMPF PHOTONIC COMPONENTS has revealed a new product platform called ViBO: VCSEL with integrated Backside Optics.

This VCSEL array technology supports a new generation of illumination devices that are inherently eye-safe over the whole product lifetime as the diffusor optics are monolithically incorporated into the laser array. This allows easy interfacing with the new platform and enhances reliability. Also, the form factor is significantly reduced compared to present hybrid VCSEL package solutions. ViBO can be directly SMD mounted onto a board or driver IC without additional wire bonding. This supports, for instance, easier integration under smartphone displays.

"ViBO has superior properties as well as cost advantages compared with standard top-emitting devices that are combined with external optics. Using ViBO as light source for 3D sensing applications offers more flexibility and freedom in design for its integration, as the footprint and the height are significantly smaller than hybrid solutions. This is especially interesting for consumer electronics such as smartphones or AR glasses", says Ralph Gudde, VP of marketing and sales.

"The smart combination of our high-performance VCSELs with unique, patented lens forms directly etched into the GaAs-substrate, gives our customers unprecedented benefits in creating tailored illumination profiles needed in advanced 3D sensing applications," adds Ralph Gudde. As well as flood and spot illumination, addressable zones can create linear and individual illumination profiles, as the emitting zones can be flexibly turned on and off.

In the first generation products, Trumpf focuses on the realization of illumination devices incorporating various diffusor designs for a wide range of emission angles to support various flood illumination applications for consumer and automotive. Having shipped millions of hybrid packaged products containing separate VCSEL arrays and diffusors, these widely used flood illuminators are viewed as the logical candidates for the company's ViBO technology. With coplanar contact designs, the devices can be flip-chip mounted, yielding the most compact integration with the shortest electrical path and thus minimum electrical inductance. This design setup allows short pulses, high modulation speed and the flexibility of addressing multiple channels or even selected segments on the chip.



X-FAB to offer heterogeneous integration using micro-transfer printing

X-FAB Silicon Foundries, a foundry for analogue/mixed-signal and specialty semiconductor solutions, is now able to support volume heterogeneous integration via micro-transfer printing (MTP), thanks to a licensing agreement that has just been secured with X-Celeprint.

This will mean that a diverse range of semiconductor technologies may be combined together, each being optimised for particular functional requirements. These technologies will include SOI, GaN, GaAs and InP, as well as MEMS.

In order to become the first foundry to provide customers with MTP-based heterogeneous integration, X-FAB has made substantial investments over the last two years. It has also established new optimised workflows and cleanroom protocols. This will allow customers to work with the foundry on heterogeneous design projects – benefitting from a low-risk and fully scalable business model that offers a clear migration to volume production.

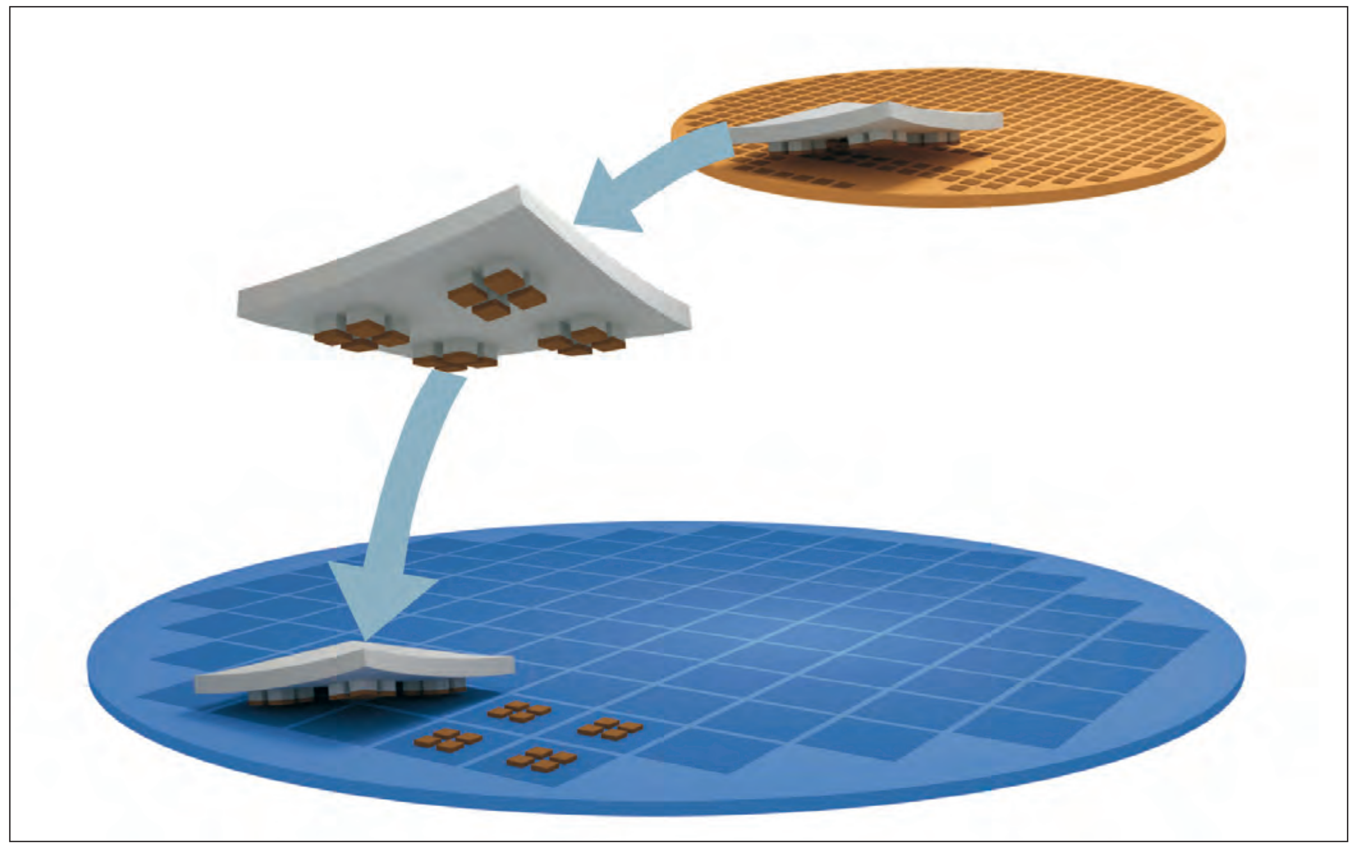
X-Celeprint's proprietary massively-parallel pick-and-place MTP technology stacks and fans-out ultra-thin dies based on different process nodes, technologies, and wafer sizes. It results in the formation of virtually monolithic 3D stacked ICs, which have enhanced performance, greater power efficiency, and take up less space. Furthermore, all this can be achieved at an accelerated rate, thereby significantly shortening time-to-market.

"By licensing X-Celeprint's disruptive MTP technology, we are uniquely positioned in our ability to facilitate the incorporation of numerous different semiconductor technologies. X-FAB customers will be able to utilize a technology that no other foundry is offering, and existing X-Celeprint customers may now tap into capacity levels that will easily meet their future demands," Volker Herbig, VP of X-FAB's MEMS business unit, explains.

"As a result, we can assist customers looking to implement complete multifunctional subsystems at the wafer level, even when there are high degrees of complexity involved. Signal conditioning, power, RF, MEMS, and CMOS sensors, optoelectronic devices, optical filters, and countless other possibilities will all be covered."

"Our agreement with X-FAB represents a major milestone in the commercialization of MTP technology, broadening the number of customers and applications," states Kyle Benkendorfer, X-Celeprint's CEO.

"High-volume heterogeneous integration of elements derived from various different source wafers will provide the semiconductor industry with significant new capabilities, including access to higher density devices with more functionality, fabricated at high yields and lower cost, within shorter timeframes."



GaN Systems signs capacity agreement with BMW for power transistors

GaN SYSTEMS has signed a capacity agreement with BMW Group for GaN Systems' high-performance, automotive-grade GaN power transistors, which increase the efficiency and power density of critical applications in electric vehicles.

GaN power semiconductors are a key ingredient to achieve the small size, lightweight, and high efficiency required in the next generation of high-performance electric vehicles. Under the terms of the agreement, GaN Systems will provide capacity for multiple applications in series production. The guaranteed volumes by GaN Systems are a key building block for reliability in the supply chain for automotive players like BMW.

"Electric vehicles represent the future of transportation, and we are delighted to continue to support BMW with our design and production capacity," stated Jim Witham, CEO of GaN Systems. "This multi-hundred-million dollar agreement demonstrates BMW's commitment to innovation and sustainability."

BMW's relationship with GaN Systems began more than four years ago when BMW's engineers found that small size, lightweight, low-cost onboard chargers, DC/DC converters, and traction inverters were enabled by GaN. This led to investment from BMW's venture capital firm, BMW I Ventures, to support and accelerate the automotive qualification of the GaN technology.

"The close collaboration among GaN Systems and BMW's engineers has helped to solidify the technology for automotive series production, resulting in the most advanced GaN power transistors in the marketplace today," said Kasper Sage, managing partner BMW i Ventures.

"As electric vehicles become more prominent, the demand for critical semiconductor components is only going to increase, thereby making strategic partnerships with suppliers like GaN Systems even more important."

NSF to fund new US centre for optoelectronic and quantum tech

THE US National Science Foundation has announced it will fund a new endeavour to bring atomic-level precision to the devices and technologies that underpin much of modern life, and will transform fields like information technology in the decades to come. The five-year, $25 million Science and Technology centre grant will found the centre for Integration of Modern Optoelectronic Materials on Demand – or IMOD – a collaboration of scientists and engineers at 11 universities led by the University of Washington.

IMOD research will centre on new semiconductor materials and scalable manufacturing processes for new optoelectronic devices for applications ranging from displays and sensors to a technological revolution, under development today, that's based on harnessing the principles of quantum mechanics.

"In the early days of electronics, a computer would fill an entire room. Now we all carry around smartphones that are millions of times more powerful in our pockets," said IMOD director David Ginger (pictured above), the Alvin L. and Verla R. Kwiram Endowed Professor of Chemistry at the UW, chief scientist at the UW Clean Energy Institute and co-director of NW IMPACT.

"Today, we see an opportunity for advances in materials and scalable manufacturing to do the same thing for optoelectronics: Can we take a quantum optics experiment that fills an entire room, and fit thousands – or even millions – of them on a chip, enabling a new revolution? Along the way we anticipate IMOD's science will help with a few more familiar challenges, like improving the display of the cell phone you already have in your pocket so the battery lasts longer."

Building on advances in the synthesis of semiconductor quantum dots and halide perovskites, the centre will integrate the work of scientists and engineers from diverse backgrounds, including: chemists with expertise in atomically precise colloidal synthesis, characterization and theory, which consist of engineered systems of nanoparticles suspended in a medium; materials scientists and mechanical engineers developing methods for the integration, processing and additive manufacturing of semiconductor devices; and electrical engineers and physicists who are developing new nanoscale photonic structures and investigating the performance limits of these materials for optical quantum communication and computing.

"NSF Science and Technology centres are integrative not only in the sense that they span traditional academic disciplines, but also in the sense that they seek to benefit society by connecting academic research with industrial and governmental needs, while also educating a diverse STEM workforce," said Ginger. "To this end, we're extremely lucky to have had the support of an amazing list of external partners across the fields of industry, government and education."

A partial list of IMOD's external partners includes companies such as Amazon, Applied Materials, Corning Incorporated, Microsoft, Nanosys and FOM Technologies, Inc.; government organszations like the National Renewable Energy Laboratory, the Pacific Northwest National Laboratory and the Washington State Department of Commerce; and educational partners including GEAR UP at UW, Catalyst @ Penn GSE and the centre for Education Integrating Science, Mathematics and Computing at Georgia Tech.

The centre will launch a series of mentorship, team science training and internship programmes for participants, including students from under-represented groups in STEM and first-generation students. centre scientists will also work with high-school teachers on curriculum development programmes aligned with the next-generation science standards and act as 'ambassadors' to K-12 students, introducing them to STEM careers.

"In partnership with UW QuantumX and the Northwest Quantum Nexus, IMOD is launching a Quantum Training Testbed facility to provide cutting edge training and workforce development opportunities for students from across IMOD's participating sites and partners," said Kai-Mei Fu, associate professor of physics and of electrical and computer engineering at the UW, who is IMOD's associate director of quantum workforce development.

"We're excited to have such strong support from our partners in the region, allowing us to build on the investments that Washington state has already made in the Washington Clean Energy Testbeds to support workforce training and economic development. For example, Microsoft plans to donate a cryostat that will allow our students to cool samples down to within a few degrees of absolute zero to study phenomena such as quantum spin physics and decoherence, and we have plans to do so much more for our trainees. Right now, we're asking the question: 'What is the equipment we wish we had been able to experiment with as students?'"

The 11 academic institutions that make up IMOD are the University of Washington; the University of Maryland, College Park; the University of Pennsylvania; Lehigh University; Columbia University; Georgia Institute of Technology; Northwestern University; the City College of New York; the University of Chicago; University of Colorado at Boulder; and the University of Maryland, Baltimore County.

Applied Materials helps SiC chipmakers to move to 200 millimetre production

APPLIED MATERIALS has announced new products that help enable SiC chipmakers transition from 150 mm wafer production to 200 mm production, which approximately doubles die output per wafer, to help satisfy the world's growing demand for premium electric vehicle powertrains.

"To fuel the computer revolution, chipmakers moved to ever-larger wafer sizes, dramatically increasing chip output to satisfy burgeoning global demand," said Sundar Ramamurthy, group VP and general manager of the ICAPS group at Applied Materials.

"Today we are in the early stages of another revolution that will benefit from Applied's expertise in materials engineering at an industrial scale."

According to Gregg Lowe, president and CEO of Cree, electrification of the transportation industry is a rising trend. "We are accelerating this inflection point by leading the global transition from silicon to SiC with our Wolfspeed technology. Delivering the highest-performing SiC power devices on larger 200 mm wafers enables us to increase end-customer value and meet growing demand."

"Applied's support in helping speed qualification of 200 millimetre processes in Albany and multi-equipment installations at our Mohawk Valley Fab is expediting this transition," Lowe added. "Moreover, new technologies being developed by Applied's ICAPS team, such as hot implant, have broadened and deepened our technical collaboration and helped accelerate our power technology roadmap."

SiC wafer surface quality is critically important to SiC device fabrication as any defects on the surface of the wafer will migrate through the subsequent layers. To produce uniform wafers with the highest quality surfaces, Applied has developed the Mirra Durum CMP* system, which integrates polishing, measurement of material removal, cleaning and drying in a single system.

The new system has demonstrated a 50X reduction in finished wafer surface roughness as compared with mechanically grinded SiC wafers and a 3X reduction in roughness compared to batch CMP processing systems.

During SiC chip fabrication, ion implantation places dopants within the material to help enable and direct the flow of current within the high power producing circuits. The density and hardness of SiC material makes

it extremely challenging to inject, accurately place and activate the dopants while minimizing damage to the crystal lattice, which reduces performance and power efficiency.

Applied has solved this challenge with its new VIISta 900 3D hot ion implant system for 150 mm and 200 mm SiC wafers. The hot implant technology injects ions with minimal damage to the lattice structure, resulting in a more than 40X reduction in resistivity compared with implant at room temperature.

Applied's ICAPS (IoT, Communications, Automotive, Power and Sensors) business is developing additional products for the SiC power chip market including in PVD, CVD, etch and process control.

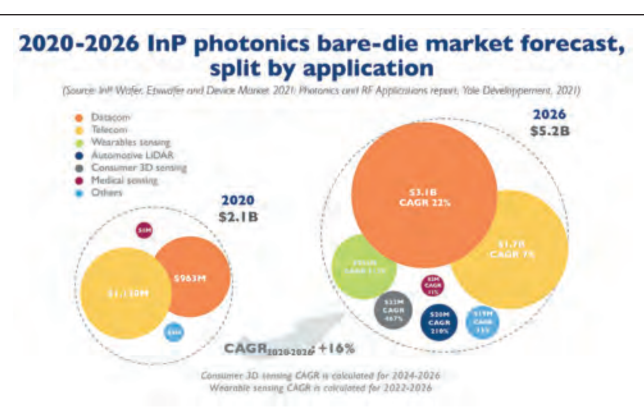
InP bare die market offering opportunities and profits

"AT YOLE, we expect an initial slight market penetration of InP in 2022 in wearables, followed by a significant increase to $255 million in 2026 with a CAGR 2022-2026 of 112 percent." asserts Ahmed Ben Slimane, technology & market analyst, Compound Semiconductors and Emerging Substrates at Yole Développement. He adds: "For LiDAR applications, InP could be promising, enabling eye safety at higher wavelengths. Leading companies such as Volvo, ZF, Continental, Daimler, etc. are interested in adopting InP-based LiDAR ."

For smartphones, OLED displays are transparent at wavelengths in the range of 13xx to 15xx nm, explains Yole's analyst. OEMs interested in removing the camera notch on mobile phone screens and integrating the 3D-sensing modules under OLED displays are considering moving to InP edge-emitting lasers, replacing the current GaAs VCSELs. Even though this trend is currently in an early R&D phase, Yole sees a strong interest from several players, such as ams, Infineon Technologies, STMicroelectronics and several laser manufacturers and sensor players.

The *InP Wafer, Epiwafer and Device Market 2021: Photonics and RF Application* report delivers a comprehensive and detailed understanding of the InP industry, covering markets from wafers and epiwafers to bare dies. Including market trends and forecasts, supply chain, technology trends, technical insights and challenges analysis, take away and outlook, this study proposes an in-depth description of the ecosystem and main players' strategies.

As analysed by Yole's team in the new *InP Wafer, Epiwafer and Device Market 2021: Photonics and RF Application* report, as an indispensable building block for high-speed and long-range optical transceivers, InP laser diodes remain the best choice for telecom and datacom photonic applications. However, following the Covid-19 outbreak and the US-China trade tensions, telecom infrastructure deployment was disrupted, resulting in a minor InP market slowdown in 2020. The requirement for more data transfer at higher speed in datacom is increasing, with technology migrating to single InP lasers targeting state-of-the-art 100 Gbit/s output, making them preferable in 400 Gbit/s and 800 Gbit/s transceivers. Driven by high-volume adoption of high-data-rate lasers, the datacom bare die market reached around $963 million in 2020. It is expected to be worth $3.1 billion in 2026, due to a 22 percent CAGR during this period.



Meanwhile, the cyclic InP telecom market will continue its growth thanks to 5G deployment. Yole sees a comfortable increase from $1.1 billion in 2020 to $1.7 billion in 2026 at a CAGR2020-2026 of 7 percent. The InP industry is a dynamic market with lots of opportunities for legacy players and new entrants. In its InP technology and market analysis, Yole reports a fragmented market, with numerous companies, especially at the device level.

According to Ahmed Ben Slimane from Yole: "Two American players are leading the InP market: II-VI and Lumentum. Both have increased their market share and strengthened their position thanks to strategic mergers and acquisitions. Indeed, II-VI acquired Finisar in 2019, and Lumentum acquired Oclaro in 2018." II-VI and Lumentum have both vertically integrated business models: they generate revenues at bare die, device, and module-level. II-VI also offers epiwafer products. Their combined bare die market share is around 30 percent.

Facing II-VI and Lumentum, Yole identifies major Chinese players like Hisense and Accelink. Both companies are in the global top five and are increasing step-by-step their share of the market. The two Chinese companies take advantage of the US-China trade tensions and the massive 5G transceiver deployment in Asia, explain Yole's analysts in the InP report. Sensing applications targeting the mass consumer and automotive markets are attracting new players.

Yole has identified several players interested in entering this market:

- Vertically integrated InP players with the know-how and an already established structure, as they can easily switch to sensing applications as soon as the market becomes bigger. II-VI and Lumentum are part of this segment.
- GaAs players with foundry capabilities could leverage the existing GaAs tools to switch to similar InP processes. Yole sees for example, ams and Trumpf.
- Emerging foundries or companies already working on InP-based solutions.

According to Poshun Chiu, technology & market analyst, Compound Semiconductors & Emerging Materials at Yole: "In the last category, we witnessed an increase in private investments and SPACs in the last year. These include, in Q4-2020, Luminar raised $590 million and went public, then acquired OptoGration; in Q2-2021, Aeva went public with an initial valuation of $1.7 billion; and in Q2-2021, Rockley Photonics announced its intention to go public at an initial valuation of $1.2 billion with an Apple supported project for smartwatches."

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AFTech:
Creating the killer coating

A new coating for the incredibly expensive graphite parts in MOCVD reactors is set to slash the costs of SiC epitaxy. **REBECCA POOL** talks to the **ZOE TOLKIEN, THE RESEARCH DIRECTOR AT AFTECH** that is making this happen

EARLIER THIS YEAR, UK-based MOCVD services provider, Advanced Furnace Technology, won more than £1 million in funds from UK Research and Innovation (UKRI) to develop a novel coating method for the lesser-known but eye-wateringly expensive graphite parts that are instrumental to epi-wafer growth.

From wafer carriers and exhaust collectors to ceilings and susceptors, the graphite 'furniture' found in MOCVD reactors is coated with highly stable SiC to prevent wafer contamination. But while the SiC coat works well for most III-V semiconductor wafer production, issues emerge when working with SiC materials.

According to Zoe Tolkien, director of research at AFTech, SiC-coated graphite internal furniture is integral to all MOCVD processes as it withstands the fast radiative heat cycles without cracking. What's more, cleaning these pricey parts to extend lifespan is critical to keeping manufacturing costs down.

"After a few runs, manufacturers of, say GaN wafers, pack up these parts and send them to us so we can clean them – this has become a booming business for us," she says. "But cleaning the silicon carbide deposits off a silicon-carbide coat part while leaving that coating intact is difficult."

"To our knowledge, no-one has managed to do this for a high-throughput, high-yield SiC commercial process – you just end up cleaning the coating off as well, which means the parts then need re-coating," she explains. "So a silicon carbide coat is just not practical for silicon carbide epi-growth."

Left: Tantalum carbide experimental CVD furnace chamber.

The AFTech researchers developing the tantalum carbide coating for graphite furniture. Zoe Tolkien is third from the left.

But tantalum carbide (TaC) could provide the answer. The metal carbide has already attracted worldwide interest as a graphite coating; it provides a highly uniform coat, is stable at SiC's extreme epitaxial growth temperatures, can suppress impurity migration from the graphite part and can extend the graphite component life. Indeed, in June this year, US-based industry analyst Persistence Market Research estimated that the TaC coating for graphite market will expand at 5 percent compound annual growth rate over the next decade with key players coming from Japan, South Korea and Taiwan. Still, issues exist.

Thermal stresses between the TaC coat and graphite surface often lead to delamination of the coating from the substrate, reducing the useful lifetime of these graphite parts, an issue that Aixtron, for one, is currently trying to tackle. As detailed in UKRI's report about the AFTech project, parts from Aixtron's South Korea- and US-based suppliers have suffered from delamination, leading the reactor manufacturer to approach AFTech for a solution.

As Tolkien puts it: "We're not the first innovator here and our customer already has suppliers, but they want an additional supplier with expertise in CVD... so we're going to optimise the deposition process."

In the next four years, Tolkien and colleagues will work out how best to coat graphite parts with TaC to reduce thermal stresses, prevent delamination and extend lifetimes by up to 50 percent.

Right now, they are experimenting with the mass flow ratio of the reactive gases within their laboratory CVD set-up at AFTech. The general idea is to increase this ratio of reactive gases as layers are deposited onto the graphite to produce a TaC gradient across the coating. Initial carbon-rich layers will more closely match the thermal expansion coefficient of the graphite substrate, reducing the chance of delamination. Meanwhile, the outer metal carbide-rich layers will provide the all-important stability crucial for SiC epitaxy.

Tolkien also intends to scale up the TaC deposition process ready for commercialization. "Scaling is never linear and there will be plenty of experimental work to reach a high-yield point [at scale] – the innovation is going to be in our method and careful process control," she says. "If we can overcome the mismatch of thermal coefficients, we'll have cracked delamination and will be able to extend the lifetime of these parts."

Assuming project success, then the future for AFTech is set to be dazzlingly bright. A delamination-free TaC-coating graphite process will first see the Cambridge-based company manufacturing the necessary internal furniture for MOCVD reactors that will be sold by a world-leading supplier. And then the company will also hold a critical place in the rapidly expanding SiC semiconductor supply chain.

"Ultimately we hope that we can improve the efficiencies of epi-wafer growth for the SiC semiconductor market," says Tolkien. "We're a small company but want to contribute to this ramp up of SiC devices that is so important to energy efficiency and carbon net zero. As far as I see, efficiencies are being achieved through innovations along the supply chain and we're hopefully going to be a part of that."

III-V Epi: a need for speed

Recently launched UK foundry services provider, III-V Epi, intends to accelerate epitaxial structure manufacture for lasers, HEMTs and more. **REBECCA POOL TALKS TO CTO, RICHARD HOGG,** to find out how

IN JULY THIS YEAR, III-V Epi launched, aiming to bring new III-V devices to market as quickly as possible. Led by UK industry veterans that hail from Gas Sensing Solutions, quantum tech hub, Quantic and the University of Glasgow, the new company is already providing myriad wafer foundry services that rely on MBE and MOCVD to commercial firms and research organisations around the world.

III-V Epi's MBE and MOCVD epitaxial structures are being used in lasers, LEDs, photodetectors, HEMTs and more. And key customers to date include an Asia-based tech giant, the UK start-up Vector Photonics, laser equipment suppliers, defence organisations and several universities, with more of the same coming soon.

"Myself and colleagues have worked together in the past and it was a natural progression to launch the company – we believe there's a massive unmet need here for low-to-medium volume [wafer production]," asserts Richard Hogg, III-V Epi chief technical officer, head of The Electronic and Nanoscale Engineering Division at Glasgow University, and chair of the scientific advisory board at Vector Photonics.

"In the past, all of III-V Epi's partners have had problems getting epi-wafers fabricated as [foundries] have been busy making, say, hundreds of thousands of VCSELs for handsets, mice or datacoms applications," he says. "But as soon as you come away from an application that isn't in an iPhone or Samsung phone, your volumes are down and you may only need a dozen wafers – so we're focusing on low-to-medium volume and prototype III-V epitaxial structures for device applications."

Right now, III-V Epi is using two MBE systems and two MOCVD reactors, with each instrument handling 2-inch to 4-inch wafer sizes. Recently developed structures include 980 nm VCSELs, antimonide photodetectors on GaAs substrates, novel multi-colour LEDs and Vector Photonics' photonic crystal surface emitting lasers. The company routinely performs regrowth in InP and GaAs-based systems while its InP distributed feedback MOCVD re-growth processes have been qualified for 1310 nm DRB lasers.

On a different tack, Hall Effect measurements were recently carried out for a partner that had fabricated devices on a newly-commissioned reactor. And the company is also working with other UK-based universities on developing routes to generating and commercializing intellectual property.

For now, the company is firmly sticking to antimonide, arsenide and phosphide materials, but alternative materials systems may follow in the future. "We're busy enough with three atoms right now," quips Hogg. "But there's always a possibility we could expand to nitrides or more exotic materials."

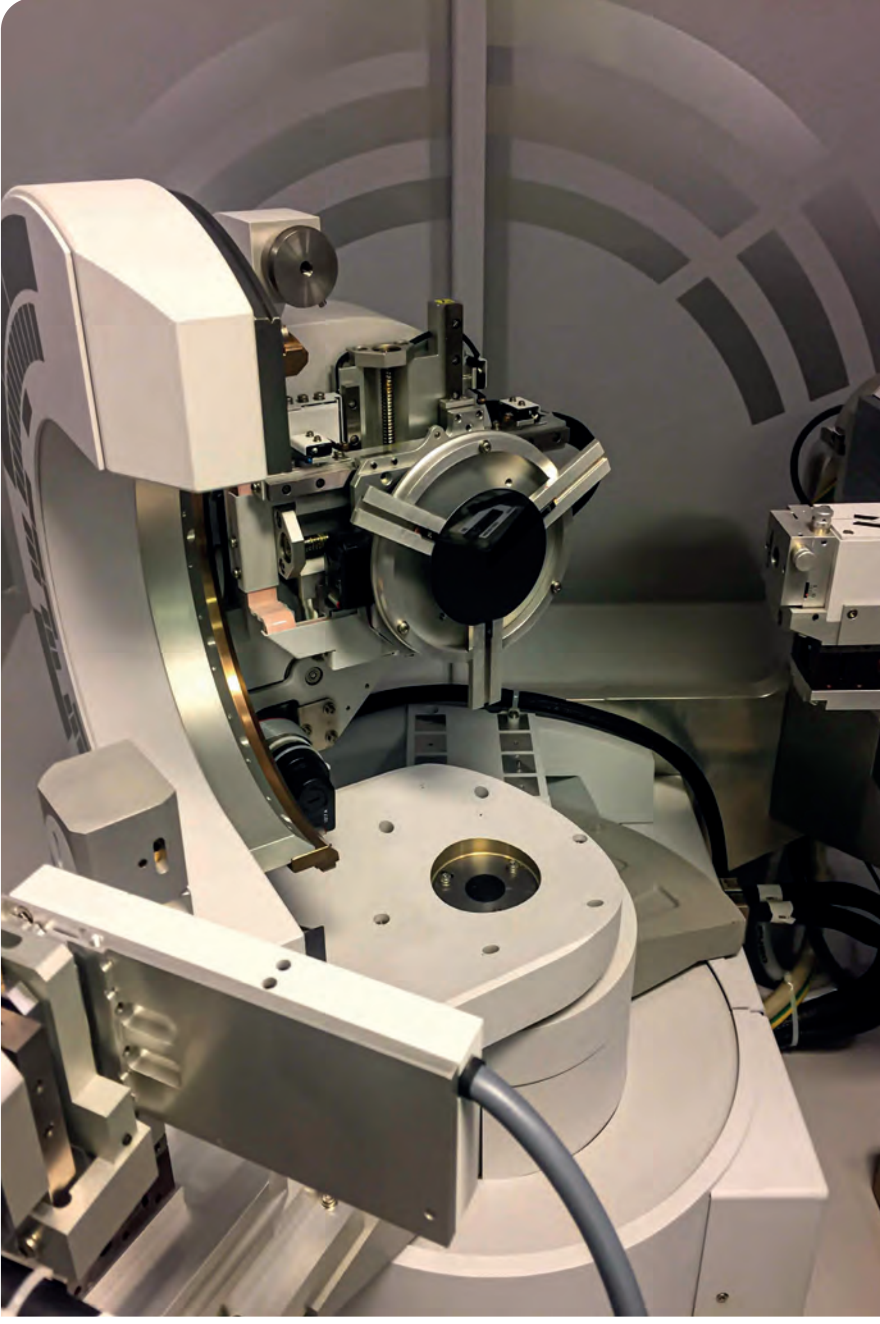
From concept to structures

In a typical scenario, III-V Epi will spend some time working with customers to define an exact device design. This could, for example, involve converting a software simulation to a realistic design with specified layers and tolerances.

"We might ask, do you really want that tolerance on layer 17? And the customer might say no, but it is critical to layer 22," explains Hogg. According to the CTO, this process can take time, but once the final design is decided, the company will typically fabricate the necessary structure in eight-to-ten weeks.

III-V Epi currently has two engineers running its MBE systems and four engineers running its MOCVD reactors across its three partner organisations, a set-up that Hogg reckons could be unique to the UK.

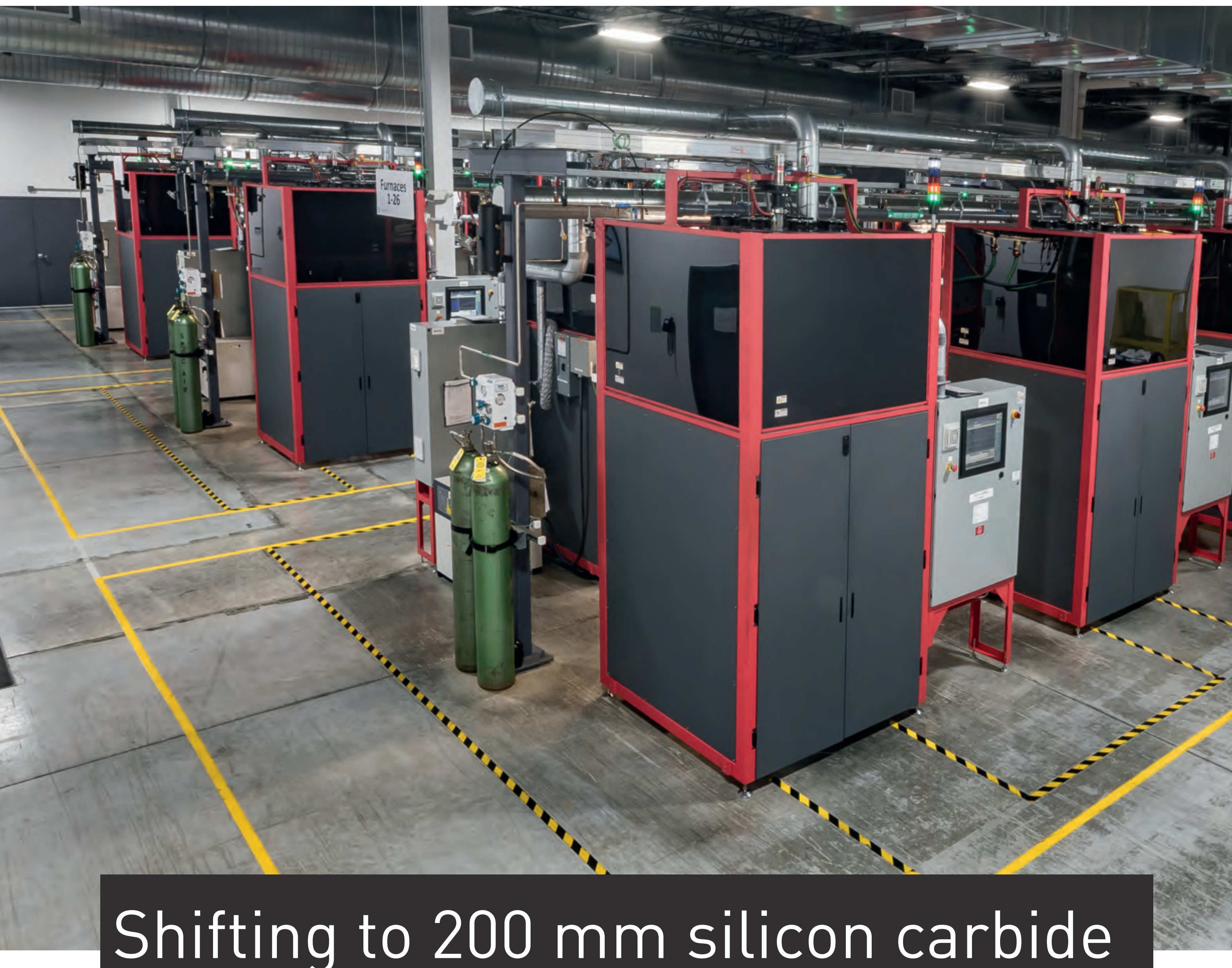
"We've got this mixed usage situation where we have both MBE and MOCVD capabilities, with neither within a university building," he says. "Many of the engineers working with III-V Epi's partners are from Glasgow University, and it has just made sense to collaborate – we've got so much knowledge about manufacturing and we can bring this together with our research and development."



In recent weeks, III-V Epi joined the European Photonics Industry Consortium (EPIC) and company growth is now expected. It's early days, but Hogg and colleagues anticipate strong demand for the materials systems they can manufacture, and at some point expect to recruit highly skilled tools operators and tool setters to ramp volumes.

"Our fast turnaround times are critical at the moment," says Hogg. "So much compound semiconductor capacity [is tied up] with a few big companies and getting spare capacity anywhere can be difficult."

"We're going to want to have the ability to ramp up volumes by using operators to run our tools overnight so we can manufacture 24/7," he adds.



Shifting to 200 mm silicon carbide

Introducing larger wafers will accelerate the production of power electronic devices in fully depreciated 200 mm fabs

BY SANTHANARAGHAVAN PARTHASARATHY FROM GT ADVANCED TECHNOLOGIES

The goal of achieving carbon neutrality has gained momentum worldwide. Many steps are being taken to transform our global energy system, including a dramatic reduction in reliance on fossil fuels. The adoption of wide-bandgap semiconductors made from materials like SiC will provide energy-efficient devices that have almost no losses, creating a sustainable path to achieving net zero carbon emission.

Today's power converters, including AC-DC rectifiers, AC-AC transformers, DC-DC converters and DC-AC inverters, tend to employ silicon-based power electronic devices – the IGBT, short for insulated gate bipolar transistor, is among the most commonly used. However, demands for faster switching frequencies, high power ratings, high conversion efficiencies and high-temperature operation are driving the adoption of devices made from SiC. This wide-bandgap semiconductor combines a bandgap that is three

times that of silicon with a thermal conductivity that's also three times higher and a breakdown field that is ten times greater, making devices made from SiC a perfect choice for these operations.

Shipments of SiC power devices, which are made on native single-crystal substrates, have climbed in recent years. This has enabled SiC to move out of the lab and establish itself as a mainstay for power electronic devices, especially when breakdown voltages greater than 900 V are required.

The foundation for commercialization of SiC power devices came in 1999, when 50 mm diameter wafers hit the market, selling for $495 a piece. While that seems an eye-watering price today, at the time this was considered a breakthrough. Now the majority of SiC power electronic devices, such as Schottky barrier diodes, MOSFETs, junction field-effect transistors and cascodes, are built on 150 mm wafers, with fabrication taking place in fully depreciated 150 mm and 200 mm fabs that have become available as wafer sizes in the silicon industry have transitioned to 300 mm.

To provide year-on-year productivity growth in the semiconductor industry, engineers tend to pull on five well-known levers: shrinking device dimensions, introducing a new device design, improving equipment productivity, increasing line yield, and migrating to a larger wafer size. Of these five, the latter offers considerable gains, which is why there is so much interest in the development of 200 mm SiC wafers.

The obvious benefit of increasing the surface area of the wafer is that it drives up the number of devices, or die, that it can yield. This increase diminishes fabrication cost per device, since the number of process steps remains the same (see Table 1).

Readily available fab capacity

Today silicon-based power devices, such as the IGBT, are mass-produced on 300 mm silicon wafers. That's because Tier 1 integrated device manufacturers (IDMs) have invested billions of dollars over the last few years on 300 mm fabs for making silicon power electronics.

Thanks to the migration of silicon power device manufacturing to 300 mm fabs, fully depreciated 150 mm and 200 mm fabs are now available for SiC production. Supporting this venture, IDMs have added toolsets for SiC device fabrication. These include : MOCVD reactors capable of growth up to 1600 °C; high-energy, high-temperature implanters; dopant-activation furnaces; metrology equipment; wafer-level testing; and die singulation tools. These fabs have enough excess capacity to handle several thousand wafer starts per week.

While Tier 1 IDMs have the benefit of fully depreciated and well-optimized day-to-day run yields aiding competitive manufacturing costs and device prices, it will not be so easy for newcomers with 200 mm fabs. These firms will encounter price pressure and lower yield numbers in the near term.

The introduction of 200 mm substrates is expected to bring down the overall device cost by 20-35 percent relative to production on a 150 mm platform. This can occur even if there is an increase in material costs at the wafer level. For the ease of achieving good wafer

	Wafer Diameter mm			
	76	100	150	200
Surface area(A=π. r^2) mm^2	4534	7850	17663	31400
Ratio increase over previous size		1.7	2.3	1.8
Die Size (mm)	4 x 4	4 x 4	4 x 4	4 x 4
No. of dies/wafer	172	338	858	1611
Increase in the number of dies%		97%	154%	88%
Ratio of increase in devices		2.0	2.5	1.9

Table 1. The number of die increase with wafer size.

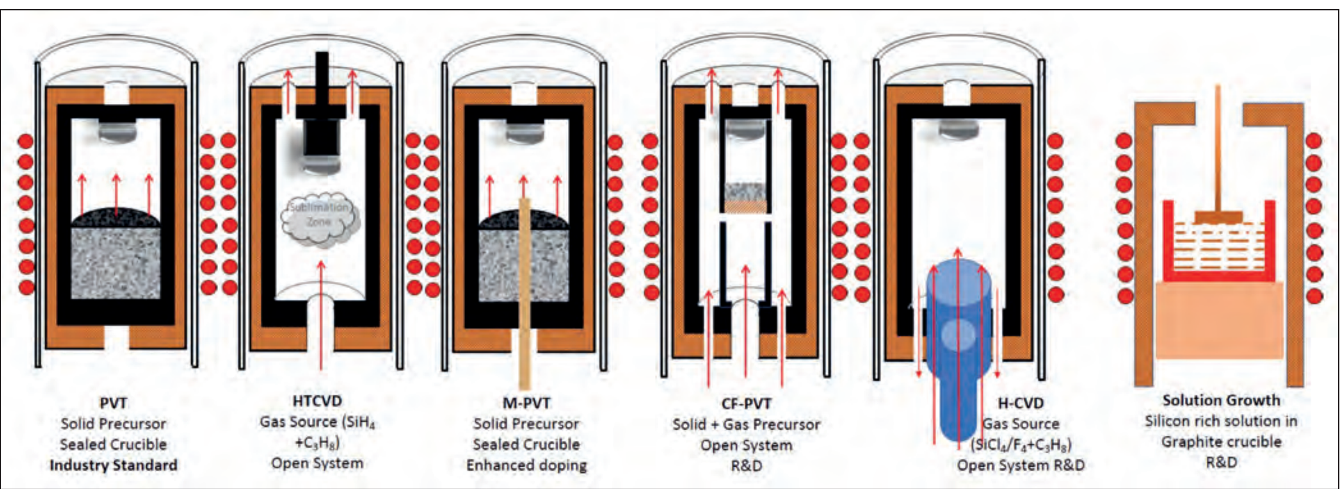


Figure 1. There are several different techniques for producing bulk SiC.

geometry, there is an increase in wafer thickness as the wafer diameter grows. 150 mm-diameter SiC wafers have a thickness of 350 μm, and the initial 200 mm SiC substrates introduced to the market will be 500 μm-thick. As increased thickness reduces the number of wafers made from each puck, there is a slight rise in wafer cost. However, the increased thickness helps to ensure a good wafer geometry, while minimizing bow and warp.

Even with today's fabrication tooling capabilities, it is possible to produce 350 μm-thick 200 mm wafers that would provide an additional reduction to substrate costs. However, that's not an essential step, as irrespective of wafer thickness, SiC wafers with a 200 mm diameter offer reduced device costs compared with their 150 mm siblings.

While moves to larger substrate sizes over the past two decades have helped to cut production costs for SiC devices, they are still about three times higher than those of silicon variants. That's not a showstopper, though, because when a circuit designer switches from silicon devices to those made from SiC, they get a 5-10 percent cost reduction at the system level. The introduction of 200 mm SiC wafers will amplify this benefit and lead to further falls in overall system-level cost over the next few years.

Scaling challenges

For elemental semiconductor materials such as silicon and germanium, as well as compound semiconductor materials such as GaAs and InP, crystalline material is grown from the melt. Crystal growers begin by taking a seed crystal, with a cross-section typically 10 mm by 10 mm, and use the thin neck created between the seed and the melt interface to increase the diameter of the crystal to the required level. Once this is established, the crystal is pulled out of the melt at a rate that depends on the material. This rate ranges from 1 mm/hour to 150 mm/hour.

One of the biggest downsides of SiC is that the material doesn't exist in a liquid phase, so crystals can't be grown from a melt. If SiC is held at a high temperature and low pressure, it dissociates into gaseous species without passing through the liquid phase. Due to this behaviour, SiC crystals are grown using a vapour phase technique called sublimation, or physical vapour transport (PVT). For growing material using

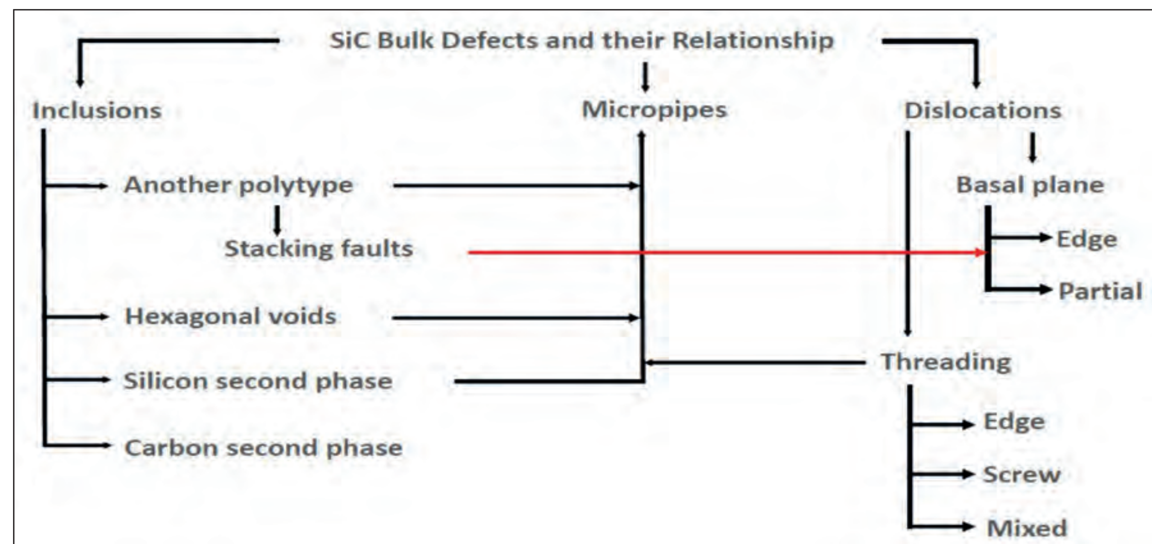


Figure 2. Various defects observed in bulk SiC and their relationship.

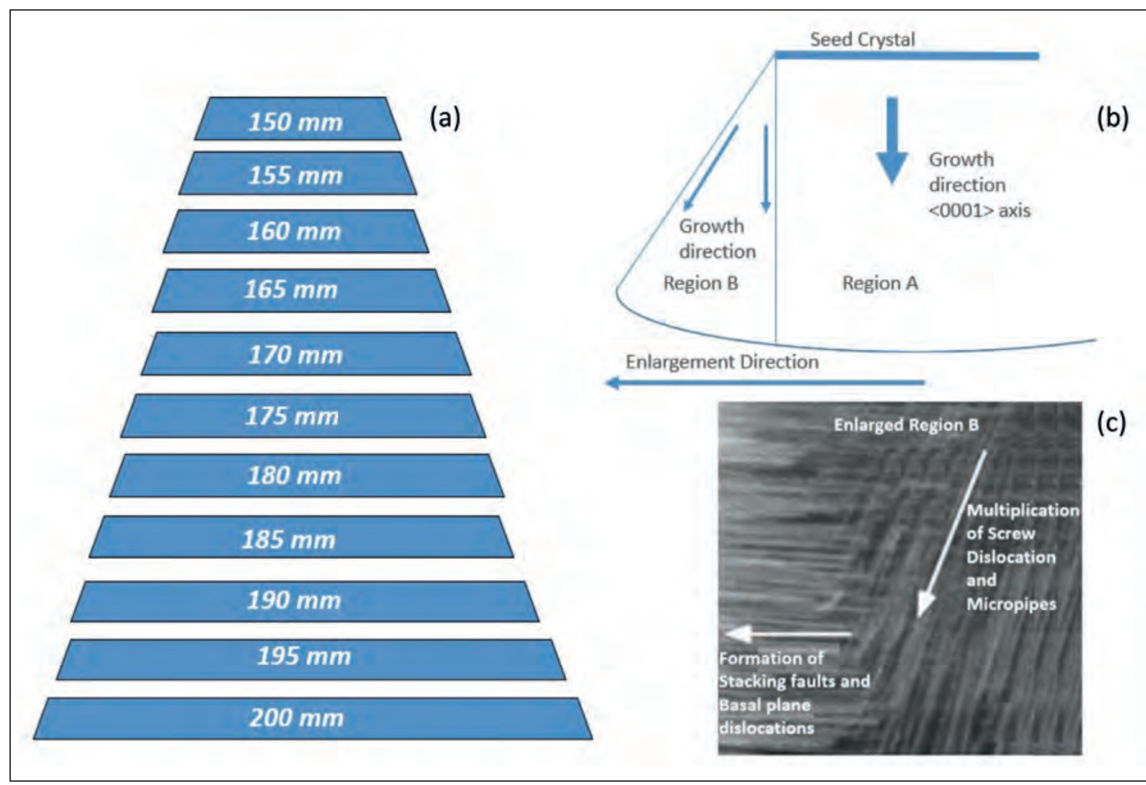


Figure 3. Seed enlargement lies at the heart of the introduction of larger wafer sizes. Shown here are illustrations of: (a) a seed expansion process from 150-200 mm, and (b), the defects that can develop during the seed expansion process. The newly expanded region is susceptible to the formation of more defects (c).

this method, an essential ingredient is a seed crystal with a diameter similar to that of the boule (read on to discover how the seeds are expanded). With PVT, growth rates are in the range of 0.1-0.5 mm/hour.

To take the quality of SiC to a new high, and to enable a more precise control of the growth of this material, researchers have realized additional advances to the PVT process, and explored other viable options (see Figure 1). One refinement, adopted by industry, is the use of gaseous cracking to supply the carbon and silicon, rather than a solid SiC powder. This technique is called high-temperature chemical vapour deposition (HT-CVD).

Another alternative is modified PVT (M-PVT), an approach that incorporates an additional feed tube into the growth zone for the dopant gas, which could be nitrogen or other materials. This modification enables the production of low-resistivity SiC with uniform resistivity profiles. Using conventional PVT, one downside is that the dopant gas is introduced outside the growth zone. This prevents the production of low-resistivity material with good uniformity, due to limited diffusion.

At the research level, other techniques are being explored for the growth of crystalline SiC. These methods, which are a long way off producing commercial-scale SiC wafers, include halide CVD, as well as a combination of HT-CVD and PVT that is known as continuous-feed PVT.

Recently, there has been interest in the growth of bulk SiC from solution, as this has the potential for producing large-sized, high-quality SiC wafers. But this technique, still being researched, is not yet capable of achieving commercialization. One of its drawbacks is that due to the lack of a stoichiometric SiC liquid phase at atmospheric pressure, it is impossible to employ congruent melt growth. Another downside is that the solubility of carbon in molten silicon is very limited at very high temperatures. It is possible to enhance the solubility of carbon by turning to solvents, such as Ti-Si, Al-Si, Cr-Si, Fe-Si, Si-Sc, Si-Co, Sn-Si and Si-Ge. However, these solvents threaten to be incorporated in the grown crystal matrix. Another issue is that the growth of larger crystals is not sustainable with these methods.

Due to the considerations surrounding the growth of SiC by a variety of methods, today almost all commercially grown SiC crystals are produced by PVT. With this approach, PVT furnaces are either inductively or resistively heated.

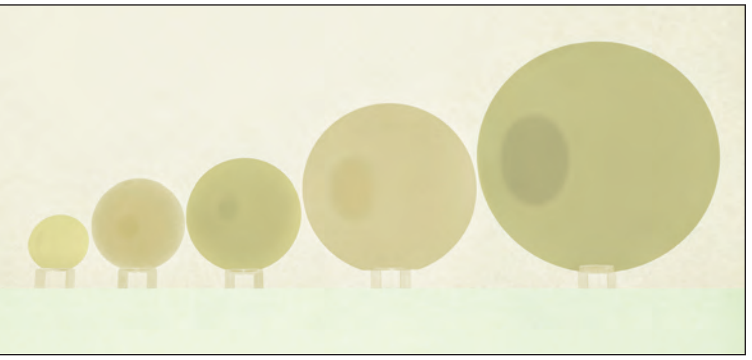
Crystal characteristics

SiC can be crystallized in three crystal structures: cubic (C), hexagonal (H) and rhombohedral (R). Variations of this material are far greater than these three, however, with SiC exhibiting more than 220 polytypes. These differ in how they occupy sites along the *c*-axis, with classification of the polytype depending on the number of Si-C layers in the unit cell. For power electronic applications, the best polytype is 4H SiC.

Difficulties inherent to vapour phase growth give rise to a variety of defects, including micropipes, screw dislocations, edge dislocations, stacking

faults, inclusions, and partial and mixed dislocations. Device performance is impaired by micropipes, screw dislocations and basal planar defects. However, the density of these imperfections can be reduced during crystal growth and subsequent epilayer deposition, which takes place prior to front-end processing. The relationship between the different defects in SiC is illustrated in Figure 2.

During the past twenty years, manufacturers of SiC have taken a step-by-step approach to expanding seed sizes. Progress is not easy, as this expansion is a time-consuming, iterative process, involving several cycles of learning and process optimization. The starting point for seed development dates back to the 1990s, with the formation of self-nucleated Lely platelets with a 4 mm by 4 mm cross-section. These days, efforts are directed towards expanding seeds from 150 mm to 200 mm, a challenging task given that the newly expanded region is susceptible to the formation of more defects (see Figure 3). Success in expanding seed dimensions demands a concurrent undertaking of several iterations of thermal and crystal growth computation, fluid dynamics and numerical modelling in a virtual platform, and hot zone design optimization for larger seed sizes. To preserve the quality of the crystal in the starting seed, there is a need to control the advancement of the solid-gas interface and maintain the shape of the growth interface via careful selection of axial and radial temperature gradients.



➤ Figure 4. GTAT's progress in crystal growth from 50 mm to 200 mm.

Evaluating economics

With the growth rate for 200 mm SiC crystals almost the same as that for their 150 mm siblings, there is no appreciable increase in the production cycle time, allowing equipment throughput to be maintained. Costs do rise slightly, however, due to an increase in the expense of hot-zone components, stemming from an increase in the size of this part in the growth chamber. Fortunately, there have been recent advances in graphite manufacturing, as well as a far better understanding of how to tune the growth process. Due to these gains, it is now viable to make cost-effective hot-zone components for 200 mm crystal growth, and if higher volumes are used, expenditure diminishes. Working in this manner, our team at GT Advanced Technologies (GTAT) has developed the SiClone 200 platform, which is capable of producing 150 mm and 200 mm diameter crystals without additional capex.

As well as crystal growth, seed/wafer fabrication involves outer diameter grinding, flat grinding, wafering, lapping and polishing – and each process needs to be optimized as the wafer diameter increases. There are already productivity increases at the wafering step, accomplished by reducing kerf loss during the slicing process. Traditionally, slicing SiC wafers involves multi-wire saws and diamond slurry, and leads to a kerf loss below 200 μm and a grinding loss of less than 100 μm, required for removal of sub-surface damage. Introducing laser-based slicing trims total material losses for wafer processing by one-third, to around 100 μm.

At the fab level, cost increases associated with migrating to 200 mm are minimal. Offsetting the relatively low add-on costs for 200 mm SiC crystal growth and wafer manufacturing is an increase in the number of dies per wafer. This makes the switch, which will deliver significant dividends in the power electronic industry, profitable and sustainable. Today's epi-ready 150 mm SiC wafers retail for $750-$900, and 200 mm wafers are expected to be priced at $1300-$1800. At GTAT, we have a roadmap to reduce costs even further.

Our company has a rich heritage as a manufacturer of crystal growth furnaces, with a global installed base of thousands of systems, and a strong track record in increasing wafer diameters (see Figure 4). Our know-how in equipment design, process scaling, facility planning, and the supply chain helps us to ramp SiC capacity faster, while competing successfully on price and quality. We are now in a position to push forward with 200 mm SiC, thanks to our continuous improvement, grounded in increased cycles of learning and optimization, along with R&D efforts. Our 200 mm product launch is slated for late 2021/early 2022.

If SiC continues to follow in the footsteps of the silicon industry, the next wafer size could be 300 mm. According to our initial thermal modelling, implementing unique hot-zone design components could minimize the applied shear stress, which is responsible for generating dislocations and micropipes, along with the von Mises stress that is to blame for boule cracking. If, further down the line, the industry seeks a 300 mm SiC wafer to reduce costs, we are confident in our ability to develop that next-generation crystal.

ACKNOWLEDGEMENTS

➤ The author profoundly thanks his colleagues and the world-class manufacturing team at GTAT. Special thanks and sincere appreciation to GTAT colleagues Chris Van Veen, Henry Chou and Jeff Gum, and Simon Price of Exawatt for useful discussions and critical review.

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UV Sterilisation

AGENDA 2021

DAY 1 AGENDA

Day 1 - Tuesday 9th November 2021

08:00 **Registration and welcome refreshments**

08:50 **Housekeeping by** *Chris Meadows, Conference Chair*

SATISFYING DEMAND FOR MORE DATA

09:00
Enabling wider mobile bandwidth no matter what frequency you choose.
*Presented by Ben Thomas - **Qorvo***

09:25
Presentation Title to be Confirmed

09:45
Millimetre-wave MMICs and integrated solutions enabling high-throughput 5G deployments
*Presented by Eric Leclerc - **United Monolithic Semiconductors***

10:05
The future of Germanium: Breakthrough Opportunities
*Presented by Pieter Arickx - **Umicore***

10:25
Improving yield for 5G market through defect inspection and metrology
*Presented by Varun Gupta - **KLA Corporation***

10:45
5G drives Compound Semi business expansion"
*Presented by Claire Troadec - **Yole Développement***

11:05 MORNING BREAK
Sponsored by Hewlett Packard Enterprise

SEEKING NEW OPPORTUNITIES FOR LEDs AND LASERS

11:35
Improving the architecture of the GaN VCSEL
*Presented by Tatsushi Hamaguchi - **Sony Corporation***

12:00
Can MicroLEDs and VCSELs revolutionize the Solid State Lighting Industry?
*Presented by Pars Mukish - **Yole Développement***

12:20
Refining microLED technology
*Presented by Wei Sin Tan - **Plessey Semiconductors***

12:40 LUNCH BREAK
Sponsored by Hewlett Packard Enterprise

13:55
Advanced technology of plasma dicing for GaAs VCSEL
*Presented by Shogo Okita - **Panasonic***

14:15
Optimizing 200mm Metal Lift-off for Smaller Dimensions
*Presented by Philip Greene - **Ferrotec***

14:35
Recent trends in LED and LASER diode device material characterization
*Presented by Yves Lacroix - **YSystems Ltd***

14:55 AFTERNOON BREAK
Sponsored by Hewlett Packard Enterprise

15:25
Highly uniform thin films and tool stability - key drivers for future LED display production
*Presented by Stefan Seifried - **Evatec***

15:45
Customer-specific VCSELs and VCSEL arrays technology development
*Presented by Marcin Gåbski - **VIGO System***

16:05
Seeking new opportunities for LEDs and lasers
*Presented by Samuel Sonderegger - **Attolight***

16:25
Leading-Edge MOCVD Technology Enabling Next-Generation Photonics Applications
*Presented by Mark McKee - **Veeco***

16:45
Compound Semiconductor Integration – Wafer Bonding towards new Di(e)mensions
*Presented by Thomas Uhrmann - **EV Group***

17:05
Presentation title to be confirmed

17:05 Closing Remarks

17:10 Networking Drinks Reception and Dinner

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DAY 2 AGENDA

Day 2 - Wednesday 10th November 2021

08:00 **Registration and welcome refreshments**

08:50 **Housekeeping by** *Chris Meadows, Conference Chair*

RAMPING VOLUMES IN THE POWER ELECTRONICS SECTOR

09:00
Presentation title to be confirmed
Speaker to be confirmed

09:25
The SiC & GaN Power Semiconductor Market: Forecasts and Drivers
Presented by Richard Eden - ***Omdia***

09:45
Driving the adoption of CoolGaN technology
Presented by Gerald Deboy - ***Infineon***

10:05
Solutions for high volume manufacturing of wide bandgap materials
Presented by Jens Voigt - ***AIXTRON***

10:25
Expanding opportunities for 650 V GaN FETs
Presented by Frédéric Dupont - ***Exagan***

10:45
Latest technologies for laser dicing, blade dicing of SiC and new ultra-thin grinding
Presented by Gerald Klug - ***DISCO HI-TEC Europe GmbH***

11:05
Reinforcement Factories
Presented by Julie Orlando - ***Nanotronics***

11:25 MORNING BREAK
Sponsored by Hewlett Packard Enterprise

11:55
Using high speed XRDI to improve and monitor SiC substrate quality
Presented by Paul Ryan - ***Bruker***

12:15
Advanced in-situ metrology for high-yield epitaxy of SiC/SiC, GaN/SiC and GaN/Si device structures
Presented by Iris Claussen - ***Laytec***

12:35
Presentation Title to be Confirmed - Revasum
Presented by Rob Rhoades - ***Revasum***

12:55
Unlocking The Full Potential of GaN Power: 650V, 1200V and Beyond Discreet Switches and Monolithic ICs on 200mm QST® Manufacturing Platform
Presented by Vlad Odnoblyudov - ***Qromis***

13:15
Advanced Plasma Processing solutions enabling the cost down per wafer and critical device performance required to accelerate the HVM of GaN and SiC Power devices.
Presented by Dr Mark Dineen - ***Oxford Instruments***

13:35
Hybrid monocrystalline silicon substrates for III-V heterostructures
Presented by Alexey Redkov - ***Alterphasic***

13:55 LUNCH BREAK
Sponsored by Hewlett Packard Enterprise

TAKING WIDE BANDGAP DEVICES TO THEIR ULTIMATE LIMITS

15:10
Ramping production of gallium oxide diodes and transistors
Presented by Kengo Takeuchi - ***FLOSFIA***

15:35
A New Technology of Commercialization for GaN on Diamond HEMTs
Presented by Won Sang Lee - ***RFHIC US Corporation***

15:55
Presentation title to be confirmed - Soitec
Presented by Marianne Germain - ***Soitec***

ENHANCING THE AUTOMOBILE

16:15
High-power blue VCSELs and VCSEL arrays
Presented by Masaru Kuramoto - ***Stanley Electric***

16:40
Compound semiconductor adoption by automotive market
Presented by Ezgi Dogmus - ***Yole Développement***

17:00
Electrochemical Deposition of Gold as Optimal Choice for Device Cost and Performance
Presented by John Ghekiere - ***ClassOne***

17:20
New CS Markets Challenge Traditional Reliability Testing Paradigms
Presented by Roland Shaw - ***Accel RF***

17:40
SiC: From Niche to Mass Production
Presented by Aly Mashaly - ***Rohm Semiconductor***

18:00
Speeding On-board Charging with Automotive-qualified GaN FETs
Presented by Philip Zuk - ***Transphorm***

18:20 **Closing Remarks**

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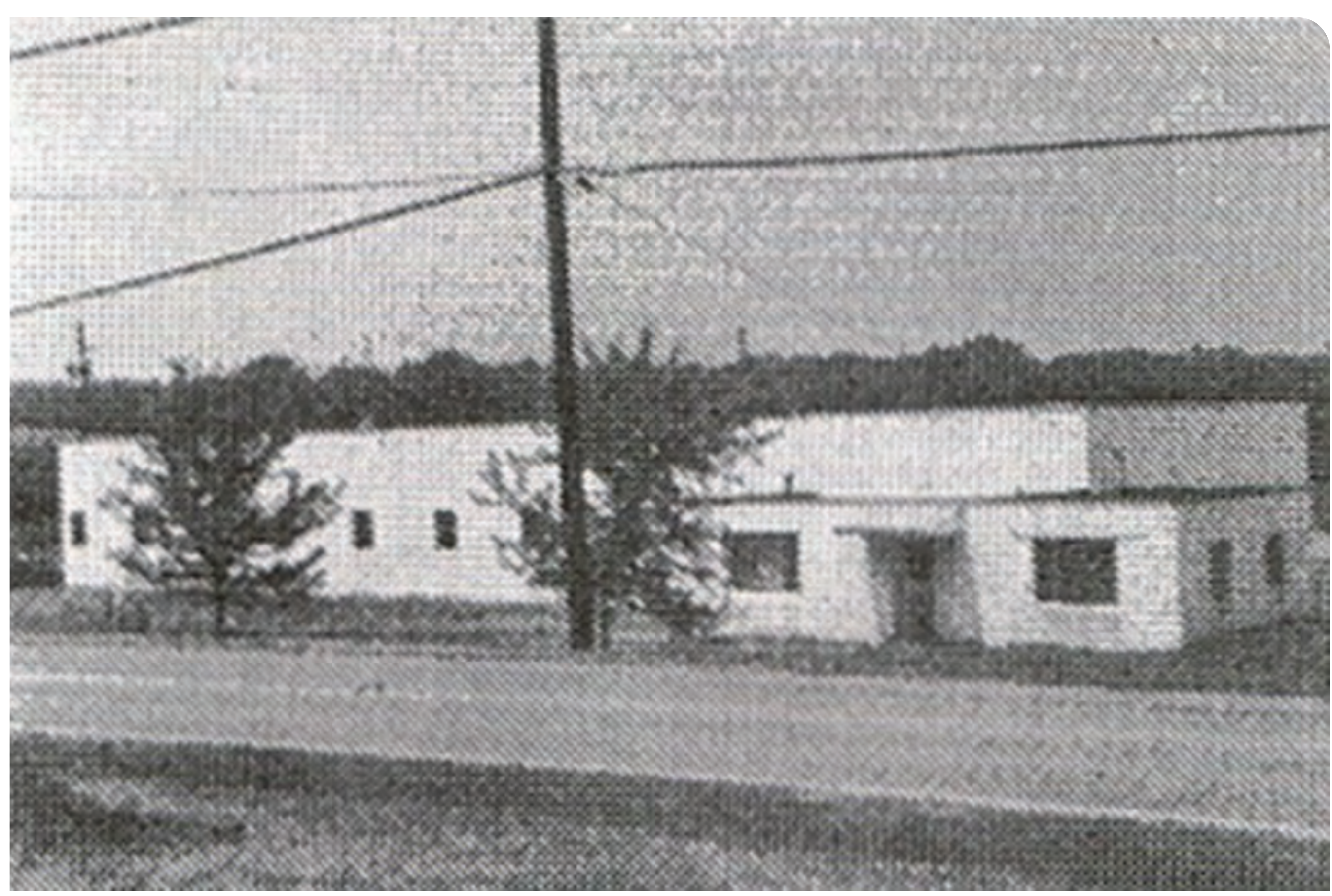


II-VI: Milestones of its first leader

In the first of a pair of features to mark the fiftieth anniversary of the compound semiconductor powerhouse II-VI, Richard Stevenson discusses the formative years with co-founder Carl Johnson

RS *Carl, how did you meet your co-founder, James Hawkey? And what provided the catalyst for getting the venture going?*

CJ I was looking for a high-quality crystal of cadmium telluride for use in my PhD thesis work at the University of Illinois. I was there from 1967 to 1969. I located a two-man crystal growth company near Pittsburgh, PA, where Hawkey was the crystal grower. They supplied the crystal that enabled and underpinned the measurements that I made at Illinois while investigating the electro-optic properties of cadmium telluride using far-infrared lasers and spectroscopy.

In 1971, after I had graduated and worked for a couple of years elsewhere, I contacted Jim Hawkey. We started talking and generated a mutual interest in founding a company to commercially manufacture CO_2 laser-grade, cadmium telluride optical parts. In the spring of 1971 we met one night for dinner and left with a name for the company, II-VI Incorporated. We also had recorded, on a restaurant paper napkin, a first-year, rough-cut budget – what we thought it would cost us to get up and get started.

RS *How did you fund this initiative?*

CJ I went out and raised $125,000 from family and friends, including former professors and business associates. The thirteenth share holder came in about a year later and topped off that $125,000. He was the landlord of our factory. He was curious, observed what we were doing, and decided to invest.

II-VI started out by renting a former metal-working and welding shop that provided 5,300 ft^2 of space. The company paid $2,500 in the first year, $5,000 in the second year and $7,500 in the third year to the landlord, who eventually became the thirteenth member of our founding shareholder group.

RS *What were II-VI's initial products, and what markets could they target?*

CJ The first product we envisioned was just the cadmium telluride material. We were going to make the material and sell it to optical shops, who would fabricate good optical parts for multi-hundred-watt CO_2 lasers. At that time the highest-power experimental lasers were around a kilowatt, but there were several versions in the 300 to 700 watt range.

Without exception, each of the thin-film coating vendors that we tried were unsuccessful in their attempts to make these optical parts. We had no choice but to tackle that and do it ourselves by vertically integrating. Once we had reasonably good optical coatings, we started supplying lenses, windows, mirrors, output couplers and the like to builders and users of CO_2 lasers.

After a year, we were in a position to supply single-crystal, cadmium telluride, electro-optic Pockels cells. Those would allow people to modulate or pulse-slice a CO_2 laser beam, shape the beam in time, and turn it on and off. You could modulate both in frequency and in amplitude with these Pockels cells.

We were the sole supplier of several optical parts to the CO_2 laser fusion programme at Los Alamos that started in the fall of 1972. They used a lot of these crystals during the 1970s, and they were our largest customer.

These modulators are still part of the offering that II-VI has today. II-VI sells into the supply chain for a number of high-power, high-performance CO_2 lasers. In the case of extreme-UV lithography, with wavelengths as short as 13.5 nanometres, the CO_2 laser is a key part of the process by which those wavelengths are emitted from a tin droplet. So this product idea has had a fifty-year life.

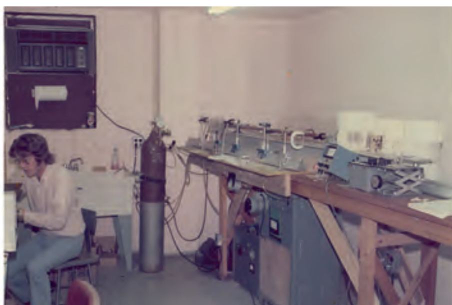
The first vertical Bridgeman furnace designed and built by II-VI, used to produce cadmium telluride material. Operating the furnace is co-founder James Hawkey.

When we started out, we'd turn on the lights with the polycrystalline cadmium telluride optics line, but the profits came from that electro-optic modulator. We could charge a fair price for that device. If we sold five of them in a month, it was a very good month.

RS *Did you and your co-founder have complementary skills?*

CJ Absolutely. Our skill sets were quite well matched, with Hawkey leading the crystal growth activities and equipment innovations. He was very hands-on, having a lot of experience with electronics, electrical, plumbing, welding, construction ... you name it. I would analyse and evaluate the crystals Jim was growing, study the results and suggest follow-on experiments in our joint collaboration to continuously improve the growth process and material.

When Jim had graduated from high school, he couldn't afford to go to college. He picked up all of his many skills along the way and through a lot of self-study. In the late 1960s, he got a chance to



During the fall of 1972, II-VI devoted much effort to learning how to cut, grind and polish cadmium telluride (left), undertake optical measurements on this material (middle), and apply optical thin-film coatings (right, with co-founder Carl Johnson pictured).

➤ The Saxonburg site of II-VI contains buildings previously owned by KDKA, the world's first commercially licensed radio broadcasting station, which took to the waves around 1928. The site was expanded by Carnegie Tech and the US Nuclear Regulatory Commission to become a world-class, 400 Mev Synchrocyclotron Research Facility by the late 1940s. II-VI acquired the property around 1978, and again expanded the site as shown in this aerial photo, taken about three years ago.

work with a professor at Carnegie Tech, growing bulk gallium arsenide crystals. That's where he learned to grow compound semiconductor crystals, and later branched off into the II-VI compounds by building on III-V experience.

Our combined knowledge, skills, experience and determination were a really good match to the unexpected challenge we faced when our survival as a company required that we quickly learn how to cut, grind, polish and apply thin-film coatings to our cadmium telluride materials. We accomplished that project in four to five months.

RS *The early years can be tricky for fledgling firms. Did II-VI have to go through any particularly precarious times?*

CJ I could probably list twenty or so such events that happened. You can have one or two problems at a time, but you can't have a lot of them, so we tried to resolve the encountered issues as quickly as possible.

In 1972, during our pre-revenue period, we missed several payrolls for Hawkey and myself, but we never missed a payroll for our two shop-floor employees. What happened was that our just-in-time successes at shaping, polishing and thin-film coating of cadmium telluride parts led to a late 1972 uptake in the sales of optics and Pockels cells. That saved the company.

In the early days, we did blow up a few vertical Bridgeman furnaces. No-one was ever hurt, but you can't disable your furnace every third run and survive. We eventually solved that problem by finding a different way to synthesize the material. Jim knew how to get around those things, and I got really good at rebuilding furnaces. I could have the damaged furnace ready to go again in 24 hours, about the time it took Jim to prepare the next load.

Our IPO in 1987 was launched five days before the October stock market crash. By that time, we had run up a half-a-million dollars or more of legal and accounting and investment-banking bills. If you don't have a successful IPO, you probably can't even pay those bills. That was another really close call.

RS *What roles did you and James Hawkey have?*

CJ From the outset I was leading the company. I raised the seed funding, organised a professional

Board of Directors, and led the sales and customer relations activities during the start-up period.

Jim Hawkey was a critical contributor in his role as the materials manufacturing and development leader. He continuously increased production capabilities in cadmium telluride, and eventually – and it's very significant – in zinc selenide. His accomplishments in the materials area allowed II-VI to become a uniquely positioned supplier in the high-power, mid- and long-wavelength infrared laser space.

Jim's legacy is embodied in today's company tag-line: Materials That Matter.

RS *In 1986 James Hawkey left the company to found, with his son, Keystone Crystal Corporation. What motivated him to leave II-VI and pursue this venture?*

CJ It was an unwanted departure on my part, at least. When you work shoulder-to-shoulder for 15 years, you are going to miss each other.

Here's the real story. We had gone about as far as we could by the educated-guess, cut-and-try empirical methods. Even the Air Force was encouraging us to apply more engineering and science to the materials problems they wanted us to solve. As we began bringing in materials-science thinking and talent to enable further company developments, Jim Hawkey became uncomfortable – he had a hands-on kind of approach and was as intuitive as you could hope anybody could be, but he was still a cut-and-try guy – so he chose to leave.

RS *What did the launch on the stock market allow II-VI to accomplish?*

CJ Two things. First, it was the only way we could get our shareholders a fair price. For some of them there was quite a bit of pressure to sell, as 16 years is a long time to hold that stock. We were able to get them 56 times their original investment.

The second is that we didn't have enough funding to go ahead and build additional expensive zinc-selenide chemical vapour deposition furnaces. We wanted to build three or four quickly. The IPO allowed us to move aggressively and smartly ahead with our zinc-selenide manufacturing capacity expansion.

RS *In the 1990s and early 2000s, II-VI started to grow through acquisitions. A year before the launch of the first ever SiC diode to market, you decided to buy Litton System's silicon carbide group. You have the touch of a visionary, don't you?*

Major milestones of the early years

II-VI's first leader, Carl Johnson, selects six key milestones from the 1970s and 1980s:

- Having, from day-one, a balanced, professional Board of Directors and a Board-approved budget. By 1984, five-year plans were underway.
- Setting a new benchmark for the quality of cadmium telluride, according to measurements made in 1972 by the Air Force Materials Lab at Wright-Patterson Air Force Base at Dayton, Ohio. Competition came from four teams involving the likes of Hughes Aircraft, Texas Instruments and MIT that all benefitted from million-dollar-plus contracts from the military.
- Achieving financial break-even by the nineteenth month of operation.
- Installing a performance-based all-employee incentive plan in 1973, the first profitable year.
- Growing export sales to more than 40 percent of total sales in the early 1980s. By then, a large portion of industrial CO_2 laser manufacturers and users were located in Japan or Germany, so II-VI had to become a global business in order to thrive. Efforts began by establishing overseas sales and marketing. Field service and engineering followed, and then manufacturing with the advent of II-VI/Singapore in 1988. By the mid-1990s, II-VI had firmly established itself as a global company.
- Realising, in 1985, self-sufficiency in the production of high-power, laser-grade zinc selenide. This had a huge impact on the company, enabling it to lay claim to being the world's best supplier of laser-grade zinc selenide.

CJ Litton System's silicon carbide group came out of the Westinghouse Science and Technology Center in Churchill, Pennsylvania, after the group's activity was shut down circa 1997. That put them only 35 miles from our home base. I went down there attempting to buy their equipment and hire some of those people – that's how I got interested in silicon carbide. But Westinghouse didn't feel comfortable selling and transferring people to a small company in Saxonburg, Pennsylvania. They choose to sell it to Litton. Litton put a wing on their Morristown, New Jersey, plant and moved as much of the group as possible over there.

Two years later, Litton had been acquired by Northrop Grumman. They too decided to shut that silicon carbide group down at a time when there was a lot of trouble in the electronic materials market. They tried to sell the gallium arsenide group and the silicon carbide group together, but II-VI wasn't interested in the gallium arsenide activity.

I tried to find someone to team with us; they would take the gallium arsenide and we would take the

In 2007, after 37 years in charge, Carl Johnson (right) stood down as leader of II-VI. He continued to serve the company as Chairman of the Board until 2014. Francis Kramer (left) held the CEO role from 2007 to 2016.

silicon carbide. There were no takers on the gallium arsenide side and Litton literally pulled the plug on that activity. I pursued silicon carbide and finally was able to buy it.

We already had a silicon carbide group operating in Saxonburg, where we had three growth furnaces running. Within a year or two we combined the two activities. We shut the furnaces down in Saxonburg and moved them all to Pine Brook, New Jersey, which is still where a lot of that group is located. This was ideal. We were able to combine what II-VI had learned with what Northrup Grumman was doing, and what they had learned. Thus the legacy of II-VI's present-day silicon carbide capabilities actually dates back to the early 1990s with respect and thanks going to Jim Choyke, Don Barret and their Westinghouse colleagues.

RS *What do you view as the other great acquisitions from your era?*

CJ There are two.

There are not too many times in the history of a company that you get to go out and acquire your largest and strongest competitor. We did, acquiring Laser Power Optics in 2000. During the prior ten years, we had met them everywhere in the world. In the late 1990s, they got in a bit of trouble and their board decided to sell the company. The acquisition had a huge impact on II-VI, making us much stronger than anyone else in IR optics. Fran Kramer, CEO of II-VI at the time, really supported this acquisition, and together we got it done. However, during the ensuing years, it was Fran Kramer who did a masterful job of leading the two-company integration and realizing the potential of every possible synergy.

Equally important to the development of II-VI was the acquisition of Photop in 2010, when I was Chairman of the Board. It was very appropriate that Chuck Mattera [current CEO] was deeply involved in this project, because of his photonics background. This acquisition gave us that starting point in the optical communications space that we were searching for.

RS *By the time you stepped down from the CEO role in 2007, you had grown the company from just two employees to more than 6000. In addition to that legacy, you gave the STEM community the II-VI Foundation. Tell me a little about the latter?*

CJ My wife and I had an interest in having a foundation that would go out and find kids that had this bent for science and technology and get them engaged early on. The first thing we did was to create a scholarship programme, to sponsor undergraduates who were going to go into science or engineering and had some industry experience. Previously, II-VI had created a Practicum Program, whereby we would go to selected high schools near our factories in the US, tell the science and math teachers that we would like to know who their best-performing students were, and ask whether or not these students would be interested in a summer job at II-VI after their junior year in high school. We had Practicum Programs operating in Pine Brook, New Jersey; Saxonburg, Pennsylvania; Dallas, Texas; and Temecula, California. These programmes served as an effective conduit for our fledging undergraduate scholarship programme. Eventually, the scholarship awardees didn't have to work at II-VI, but they did need to have 9-10 weeks of working in an industry setting every year. 54 undergraduate scholarships have been awarded for the 2021-2022 academic school year.

Then we said: What do we do if these kids come out of college and want to go ahead for a graduate degree – either a master's or a PhD? So we started up a 'Block-Gift Program' with the foundation. We sponsor a PhD programme with a professor at a university that attracts exceptionally good students and has a powerful group working in a technology area of interest to the company. We don't pay overheads at the university. We insist that all the funds go the professor's account to work on the technology. There have been, on average, about 12 awards per year.

In 2007, my wife and I donated shares of II-VI Incorporated to set up a $20 million endowment fund for the II-VI Foundation, a private foundation that has II-VI approval to utilize the II-VI name. Over the years, we've distributed $34 million of benefits, and the asset base is still around $20 million, thanks to the growth and performance of II-VI Incorporated.

In next month's issue, we'll track II-VI's meteoric rise as a producer of various forms of laser diode, in an interview with the current CEO, Chuck Mattera.

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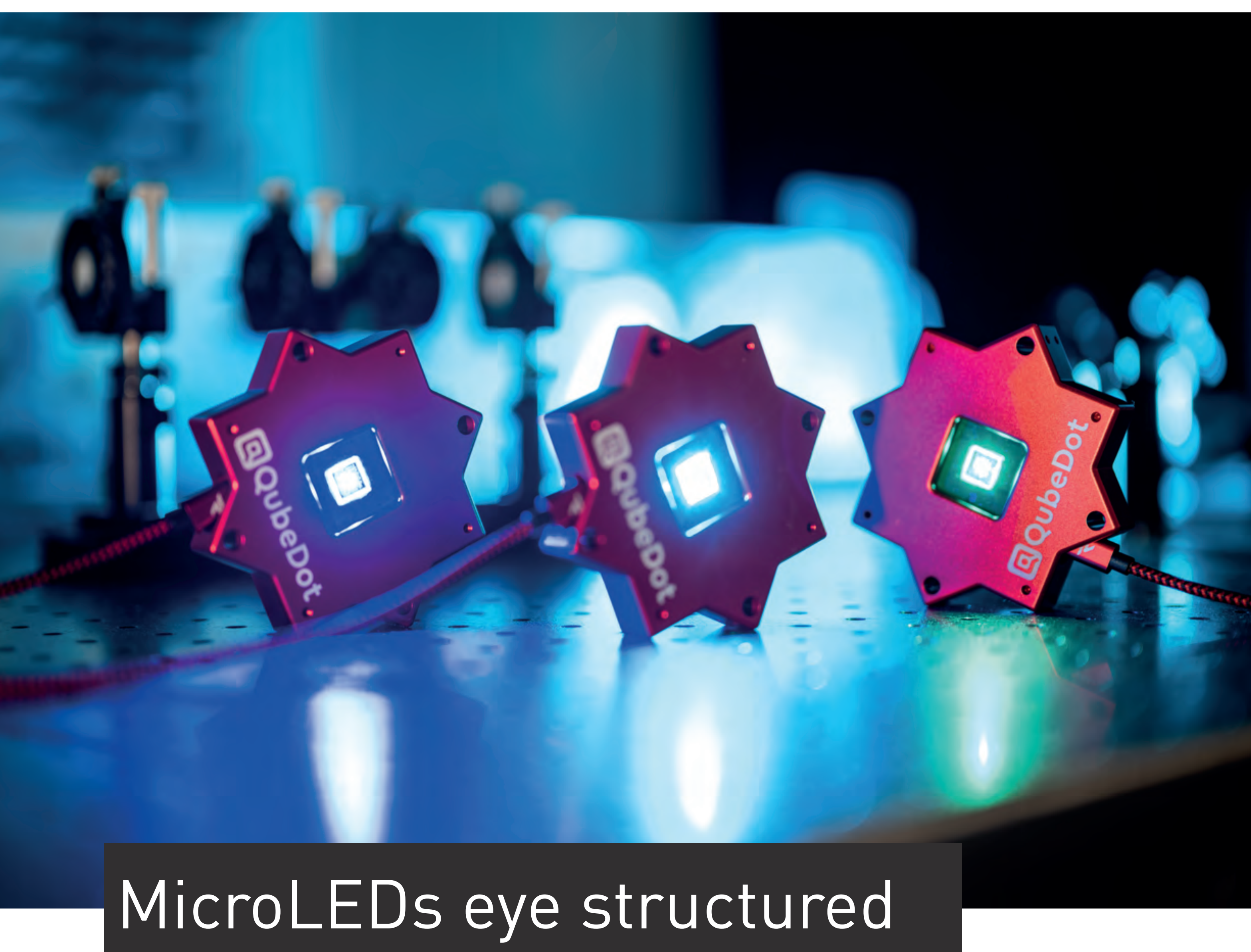

MicroLEDs eye structured illumination

Light engines formed from arrays of GaN microLEDs with a varying pitch, size and wavelength target numerous applications

BY JAN GÜLINK AND HEIKO BRÜNING FROM QUBEDOT AND UNIVERSITY OF TECHNOLOGY BRAUNSCHWEIG

PRODUCTION of GaN-based LEDs has reached phenomenal volumes, thanks to the widespread deployment of this device in general illumination. To date, this growing global market has drawn on large-area LEDs, with typical dimensions of 1 mm^2 and optical output powers in the Watt range.

Progress of the GaN LED has taken a markedly different path from that of silicon microelectronics. While the cornerstone of that industry is a continual shrinking of device dimensions towards the atomic scale, for LEDs for general lighting, there are no efforts to even move dimensions towards the micron range.

Today's LEDs used in general lighting serve in myriad applications. Examples of their numerous uses include

the illumination of optical display units, control panels and tachometers, and in a high-power form, providing the optical source for the automotive headlight. What all these applications have in common is that the LED is used to merely illuminate a target object – it could be the road ahead, or a display panel – rather than induce any change in its properties.

If there is a need to change material properties with light, the optical source that's employed tends to be a laser. Infrared lasers, and fibre lasers in particular, are renowned for their highly valued asset of a very good 'focusability'. Using optical powers that may be no more than 100 watts, this class of laser is capable of welding and cutting a range of metallic materials or plastics.

To optimise processing with a laser, engineers adjust the beam profile. For the welding of metals, the preference is a Gaussian intensity profile, because this ensures the highest possible intensity in the centre of the beam axis – a condition that leads to an energy-efficient, reproducible welding process involving the formation of a vapour capillary. In contrast, with laser-induced powder build-up welding, it is far better to employ a homogeneous intensity distribution, because this ensures uniform melting of the powder. Due to the importance of beam shaping, highlighted by these two examples, much effort within a large industrial sector has been directed at delivering good tools for that task that meet customer requirements. But just think how much simpler it would be if beam shaping could be done directly in the process.

When comparing LEDs and lasers, there is one essential difference that's so generally accepted that it is no longer highlighted: scalability. While it is very easy to drive LEDs and align their emission in parallel in frequencies in the kilohertz and megahertz range, this is far harder to accomplish with multiple laser beams. So when it comes to accelerating a light-induced process by parallelizing light sources, LEDs are a convincing candidate. One wonders how many fields of applications could be unlocked by changing the beam acoustics from a top-hat profile to that of a donut in a fraction of a millisecond?

More than 60 years ago – to be precise 29 December, 1959 – Richard Feynman delivered a widely acclaimed and ground-breaking lecture at the California Institute of Technology entitled *There is plenty of room at the bottom*. In Feynman's talk he described four applications that needed to be miniaturized, including the construction of miniaturized machines. Based on this line of thinking, what might be possible if we could build emitters that are in the order of magnitude or even smaller than the wavelength of the emitted light?

At QubeDot GmbH, a spin-off of the TU Braunschweig, we have asked ourselves these questions and, together with renowned research partners, have developed a platform technology as a solution. We call our technology SMILE – it's short for Structured Micro-Illumination Light Engines.

Creating these light sources that can serve in completely novel application fields requires three essential steps, plus a fourth that has much added value. The first of these mandatory steps is to adapt proven GaN processing technology so that it is also possible to manufacture micron-sized LEDs reproducibly. After this, we place a very large number of microLEDs on a single GaN chip, so that we can image multiple beam sources through one optic without having to apply much effort to any additional positioning. With this configuration, the relative positioning accuracy

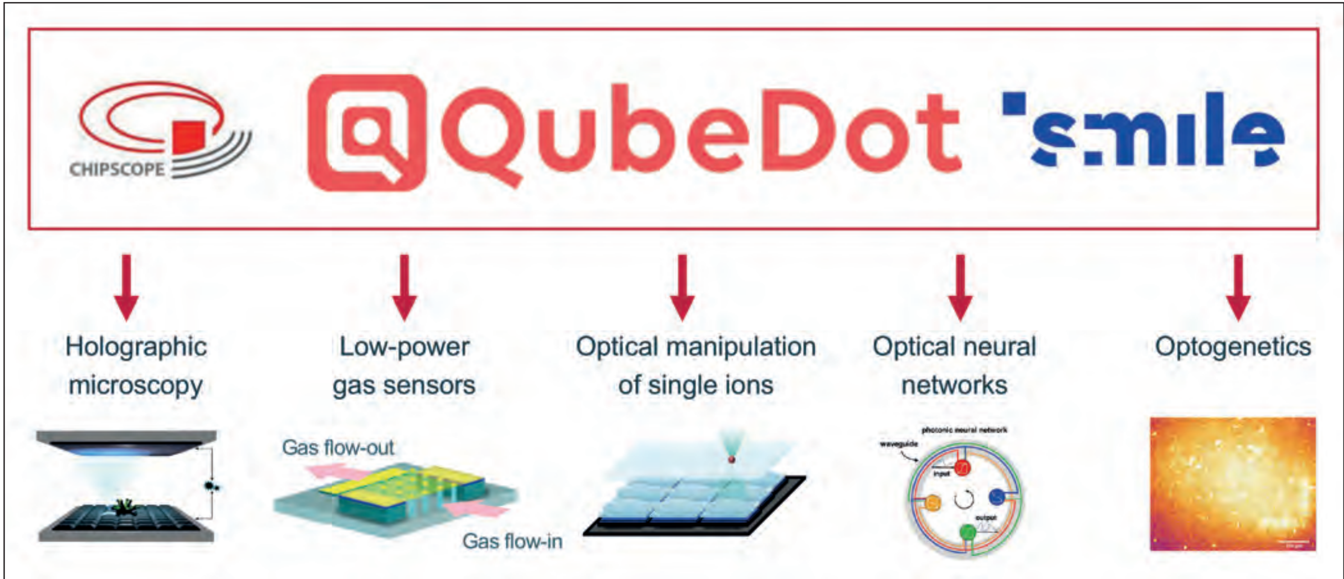

Figure 1. QubeDot and EU projects Chipscope and SMILE have led to versatile microLED platforms for different applications. More information is provided in the paper: H. S. Wasito *et al.* Beyond Solid State Lighting: Miniaturization, Hybrid Integration and Applications of GaN μLEDs, Applied Physics Reviews 2019

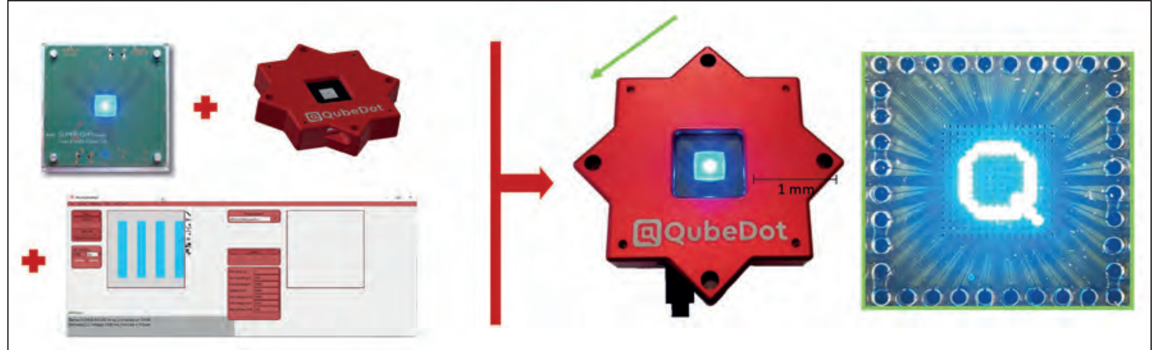

Figure 2. A SMILE platform consists of a microLED chip, electronics, housing and a Graphical User Interface (GUI).

of the light sources is a few nanometres – realised without any mechanical positioning effort! The third step is to introduce integrated circuitry, making it possible to control each microLED separately. This allows all microLEDs on the GaN chip to be controlled independently, in time and power.

With these three steps, the technology is mature. However, it would still take significant effort on the customers' side to use this to target applications. So, we help them by simplifying operability. It is easy to control the power of a laser with an analogue signal – but what if there are, for example, 256 light sources, all requiring a signal at the same time? To address this need we have written software that allows the user to immediately generate illumination patterns.

The development of our fully integrated platform has been supported by different projects. The first of these, Chipscope, targeted fabrication of pixel sizes that are as small as possible. This led to LEDs with an emitter edge size of only 200 nm, emitting at a wavelength of 450 nm. The follow-up project, SMILE, kicked off in December 2020, aims at showcasing the scalability and general possibilities of microLED arrays. Efforts have focused on optical power and modulation for different applications. Running in parallel with the progress we have made in science and engineering, those of us from QubeDot have focused, from day one, on ensuring that this novel technology will aid industry and the scientific community.

SMILE specifications

The current SMILE platforms are formed as chip-on-board (COB) on common PCBs. With these options, early adopters have no difficulty in bringing microLED technology into their products and labs. Today, we offer two different versions of the SMILE platform: 8 by 8 pixels, and 16 by 16 pixels. All SMILE platforms always consist of the LED chip, the electronics, the housing and the control software (see Figure 2).

Our software enables the user to construct lighting patterns in a very convenient manner. There is a graphical user interface that provides the possibility of calibrating the array and setting the voltage. In addition, this interface allows saving and loading of

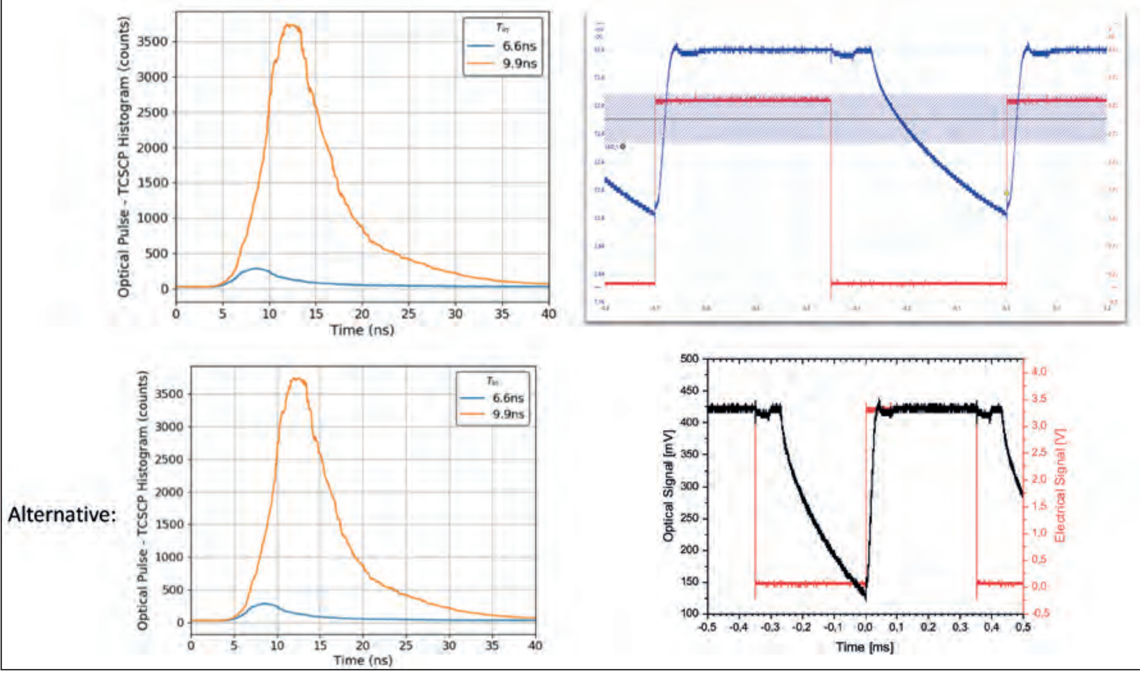

Figure 3. 100 MHz chip level modulation (left) and 3.330 MHz frame rate of a 16 by 16 SMILE platform (right) with the electrical stimulus in red and photodiode signal in blue.

sequences and animations; and offers imaging and measuring windows for different applications. With an application programming interface, control of the SMILE platform can be integrated in scripts and applications, such as Matlab, LabView and Python, by the end-users.

When considering modulation speed capabilities, it's important to distinguish between the chip level and the SMILE platform level. At the chip level we have evaluated modulation rates with time-correlated single-photon counting. This technique involves applying short electrical pulses to a microLED pixel and measuring its light output and its exact timing with a sensitive detector, such as a single-photon avalanche diode. Based on this approach, we have determined a modulation frequency for a 20 µm pixel in our 8 by 8 array of roughly 100 MHz, which corresponds to a pulse length of the order of 10 nanoseconds.

At the SMILE platform level, modulation is influenced by the surrounding electronics, and primarily its capacitances. For 16 by 16 SMILE platforms there are further limitations, associated with the synchronization of three microcontrollers. However, frame rates are still faster than those associated with the synchronization of multiple laser sources. For example, we have realised a rate of 3,333 frames per second, with the frame rate independent of image content (see Figure 3).

One of the questions we are asked most frequently at QubeDot is 'What is your output power?' The answer depends on the pixel's size, its emission wavelength and the drive current. State-of-the-art epitaxy and chip processing ensure that output powers are as high as possible. We do not roughen the backside of the chip to enhance the light extraction efficiency because although this would increase the light coupled from the chip, the pixels would no longer be clearly delineated from one another in their optical appearance. That would be a significant downside, as it would result in a blurring of the luminous pattern from the roughened chip surface.

Here we illustrate the capability of our SMILE technology by showing the characteristics of an 8 by 8 platform that has a 75 µm pixel size, a 150 µm pitch and a 450 nm emission wavelength. The single optical output powers from the 64 individual LED pixels of this array operated at a range of voltages are shown in Figure 4. When controlling individual pixels, average output powers are around 384 µW at 3.3 V and 830 µW at 4.0 V. At the higher operating voltage, the optical power density is 14.7 W/cm^2. So, if all 64 pixels are switched on, this 8 by 8 SMILE platform will emit 15.2 mW at 4.0 V (and 6.7 mW at 3.3 V).

When considering modulation speed capabilities, it's important to distinguish between the chip level and the SMILE platform level

With this 8 by 8 SMILE platform, the user can precisely control and distribute the desired optical power in the projected image plane. This is accomplished because the spatial distribution of the emitting LEDs can be controlled independently from their individual output powers. Note that an additional knob for controlling the optical output power distribution and its grid density is the selection of the SMILE platform.

Another question that we are often asked is how small can we make our pixels. Since the GaN technology for manufacturing SMILE platforms is understood and mastered, we can routinely produce pixel sizes in the range of 5 ... 100 ... 500 µm. Pixel sizes below 5 µm work reliably in the lab and will be introduced to the market soon. Typically, initial customer tests always take place with a pixel size of 75 µm, as this evaluation allows us to determine the pixel size that should be employed. The pixels do not necessarily have to be square in shape – there are also applications where several microLED lines are required. As one can imagine, there are countless combinations of size, pitch, wavelength, lighting pattern, LED output power control and modulation control for targeting a thousand-and-one different applications.

Another question that we are often asked is how small can we make our pixels

Optimising optogenetics

One group using our SMILE platform is led by Maria Leilani Torres and Alexander Heisterkamp from the Institute of Quantum Optics in Leibniz University Hannover, Germany. In the Optogenetics lab at NIFE, Hannover, their team employs fluorescence imaging, captured at a high frame rate, to visualize calcium fluctuations in cells, using a calcium-sensitive dye and a CMOS-camera. The calcium dye has been selected

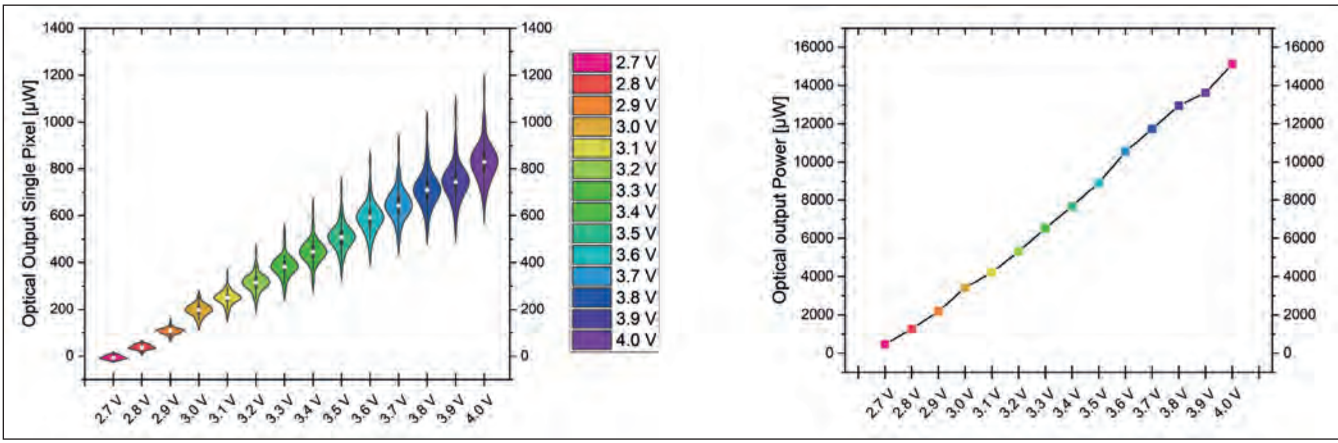

Figure 4. 75 µm pixel size 8 by 8 SMILE platform emitting at 450 nm. Violin graph of individual pixel output powers at different bias voltages (left) and overall output powers if all pixels are switched on (right). Measurements were conducted with a 10-inch integrating sphere.

in combination with an orange LED that emits at 590 nm, to ensure that excitation does not affect the activity of the rhodopsin channel. Using the SMILE platform, cell cultures are stimulated by different illumination patterns. A series of images, shown in Figure 5, illustrates how nine microLEDs can trigger a wave of electrical activity.

Conventionally, spatial light modulators are used to project a user-defined excitation pattern onto cell cultures. When carrying out this task, our SMILE technology offers several distinct advantages.

Substantial merits include dramatic reductions in both the complexity and the time taken to set up the system, which can be directly integrated into the existing cage system – there is no need to arrange and configure additional lasers. Another advantage is that the software is easy to use, thanks in part to a paint-like drawing mode that is easily accessible for every user. Custom illumination patterns are just exported and imported again. In addition to these strengths, costs come down, and it is possible to integrate several SMILE platforms, with different emission wavelengths, in one optical setup that's controlled by the main software.

Opportunities ahead

We have no doubt that our SMILE technology will find deployment in various applications. Its use in optogenetics, highlighted here, is just one of many possibilities. One of its great strengths is that it can be used directly 'out of the box' – the same cannot be said for systems based on lasers. The form of SMILE presented here, known as red star, is not suitable for all users. But given our mastery of microLEDs, and our expertise with the SMILE platform, we can easily tailor this technology for our customers. This solution is available now, and can start with small quantities, an unusual but welcome aspect for early adopters.

The SMILE project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 952135. More information can be found via qubedot.com and smile-technology.eu

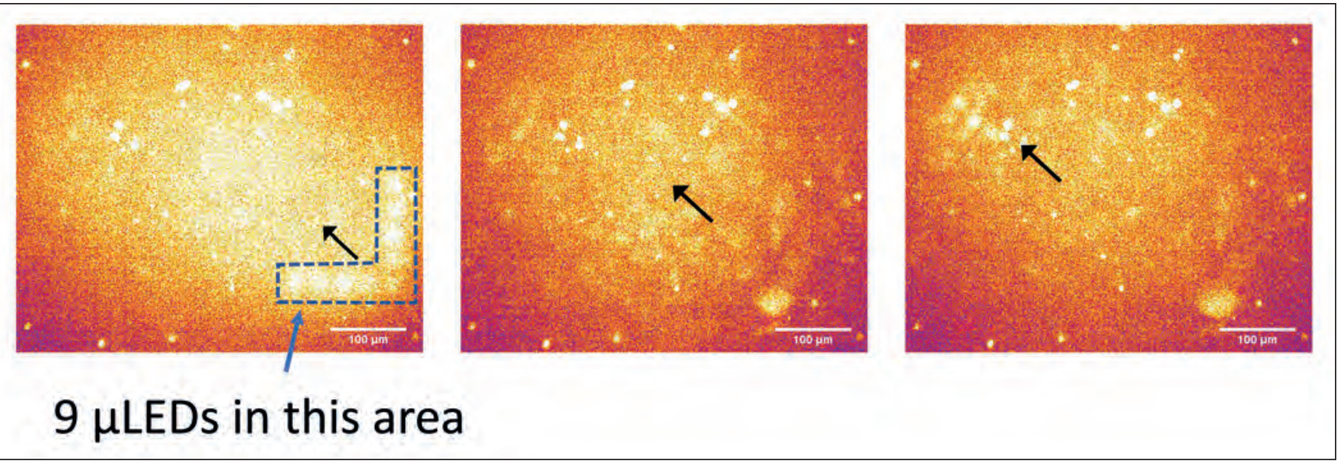

Figure 5. Nine microLEDs in the lower right trigger a wave of electrical activity from this lower right corner to the upper left corner. The arrows indicate the flow of calcium, visualized by the fluorescent calcium sensitive dye.

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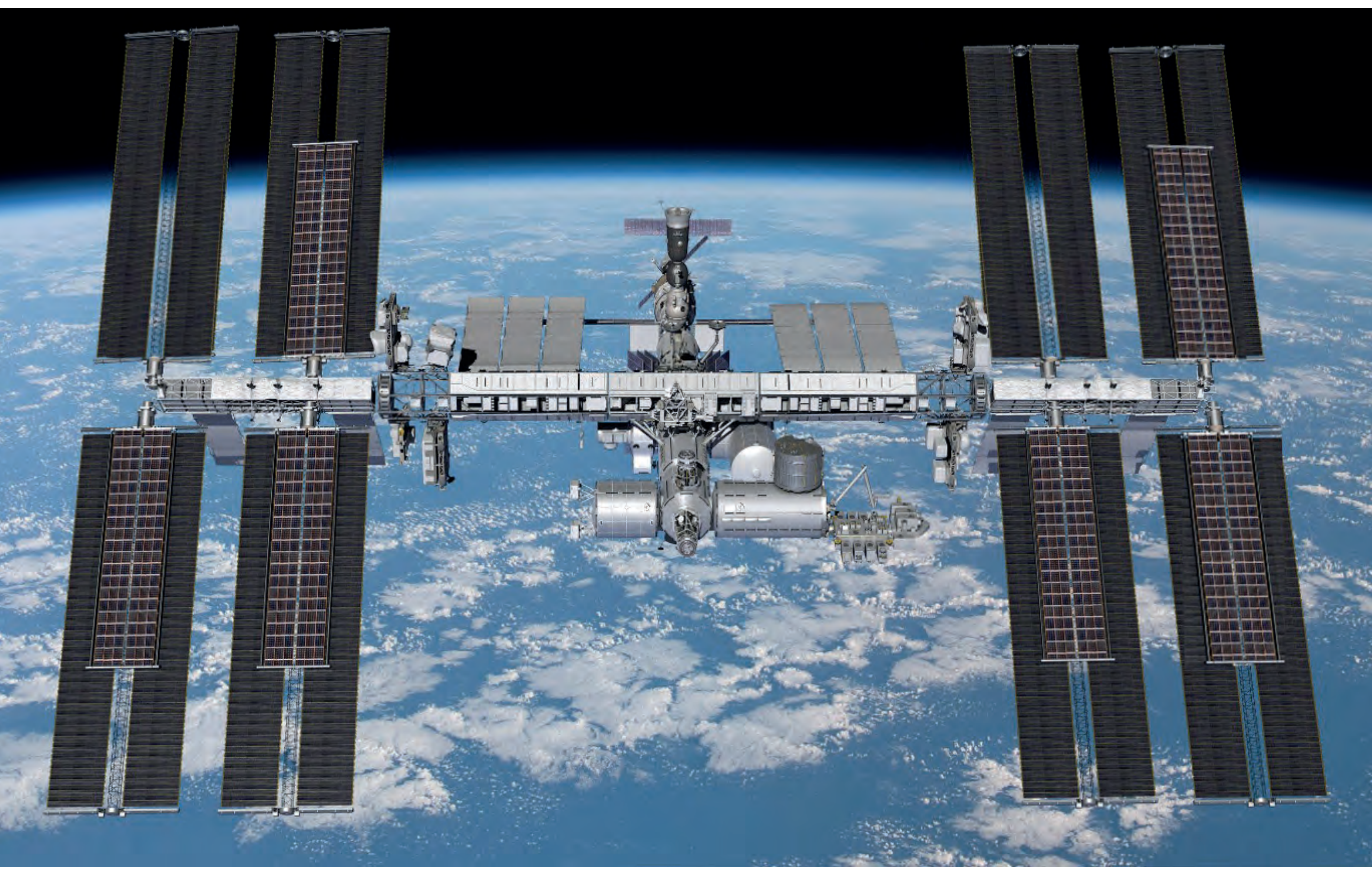

Refining the multi-junction solar cell

Multi-junction cells continue to improve by offering greater flexibility, a path towards streamlined manufacture and falling production costs

BY RICHARD STEVENSON

➤ Top: The *Roll Out Solar Array* has been used on the International Space Station. Credit: Boeing.

MANY DIFFERENT MATERIALS are competing in the solar market. For solar farms and rooftops, silicon dominates, providing rock-bottom prices for electrical generation. Cells made from a stack of compound semiconductor materials can't compete on this key metric, even when operating under very high levels of concentration and delivering far higher efficiencies.

Up in space and powering a satellite priorities are very different, playing into the hands of multi-junction cells featuring compound semiconductors. While cost still matters, it is only one of several important factors, and a premium is placed on efficiency. Excelling in this regard allows more power to be generated, and ultimately enables either the technologies on board to perform more tasks, or for actions to be undertaken that require more energy, such as electrical propulsion. Alternatively, gains in efficiency enable a reduction in cell area for the same power generation, leading to smaller satellites and lower launch costs.

Another attribute of the multi-junction cell is its superior radiation hardness. In space, cells are bombarded by high-energy protons and electrons,

causing severe damage to devices that reduces their output. All cells suffer, but III-Vs less so than silicon, the previous incumbent in this domain. This means that the fall in efficiency of these triple-junction cells over the duration of a mission is relatively small.

For more than two decades, power generation in space has been dominated by these high-efficiency cells, which typically combine a junction made from germanium with two or more based on GaAs and GaInP. Over that time much effort has been devoted to increasing the efficiency of the device, which has climbed steadily. But that's not the only improvement that's been made. As highlighted in talks delivered at this year's European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC), held on-line from 6-10 September, progress is being made in cutting manufacturing costs through the use of larger substrates and different foundations, and producing flexible cells that drive down launch costs.

Favouring flexibility

In Europe, flexible multi-junction cells, formed via substrate removal, are being developed through a multi-partner project entitled ALFAMA – that's short for Advanced Lightweight and Flexible Array with Mechanical Architecture. At EU PVSEC Jonas Schön from Fraunhofer ISE detailed some of the progress to date in this effort that is backed by €3 million of funding and involves many partners, including Airbus, Azur Space Solar Power and tf2 devices.

Schön began his presentation by championing the virtues of flexible, multi-junction solar cells. In addition to radiation hardness and the high efficiency, which are attributes that they share with their inflexible cousins, they excel in the key metric of Watts-per-gram, a valuable asset given that launch costs are up to around $10,000 per kilogram. What's more, thanks to the flexibility, satellites take up less space in the launch vehicles, potentially enabling more satellites to be deployed on each mission.

In the US, engineers have already started to use flexible cells, which are commercially available, to power their satellites. There is a NASA-led programme called ROSA, which is short for Roll Out Solar Array. Back in 2017, engineers carried out extra-terrestrial tests, supported by a robotic arm on the International Space Station. This venture provided valuable information on the responses of the cells to structural loads, aiding the launch this year of two new flexible panels, providing a total of 120 kW.

The ALFAMA project will help to drive flexible cells forward, with efforts directed at realising a power-to-mass ratio of greater than 1.3 Watts/gram. That's roughly a factor of two compared with a state-of-the-art conventional solar cell, according to Schön, who explained that another target of the project is to break new ground for the thinness of the cell. This will be trimmed below 40 μm. Progress on both these fronts will be made using low-cost manufacturing processes.

Before detailing the device adopted in the project, Schön reviewed several different forms of multi-junction cell that have been used in space. He explained that during the last two decades, efficiencies for devices with the relatively simple, conventional design that features a germanium bottom cell have

Flexible solar cells are needed on the ROSA (Roll Out Solar Array) held by the robotic arms at the International Space Station.

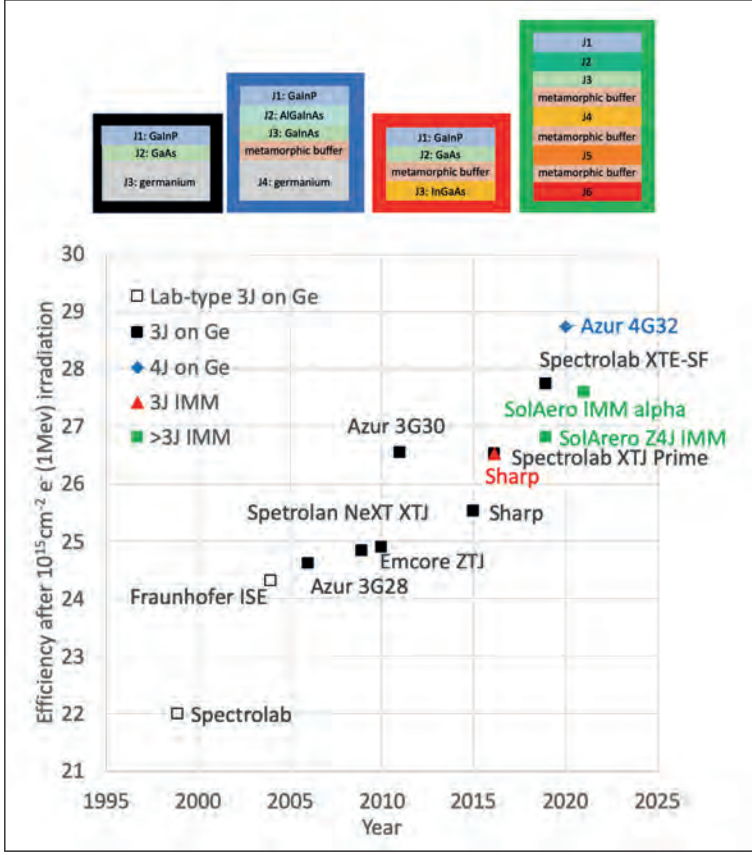

Figure 1. To evaluate the performance of multi-junction cells in space, it is appropriate to consider the efficiency after bombardment by radiation. It is common practice to use the condition of bombarded by 10^{15} electrons/cm^2 with an energy of 1 MeV. The use of an inverted metamorphic (IMM) structure allows the device to provide flexibility.

made steady progress. Over this timeframe, efficiencies have climbed from around 24 percent to almost 28 percent, according to measurements on cells that have been bombarded by 10^{15} electrons/cm^2 with an energy of 1 MeV to mimic the impact of radiation in space (see Figure 1). “The drawback [with this design], apart from the non-perfect efficiency, is the thickness due to the germanium substrates,” remarked Schön.

He pointed out that one option for reaching higher efficiencies is to add another junction, citing the 4G32 from Azur as an example. This product includes a metamorphic buffer to overcome lattice mismatch between the germanium sub-cell and the three III-V sub-cells. This design is able to reach an end-of-life efficiency of nearly 29 percent, but is still impaired by the thickness of the germanium substrate.

Overcoming this issue are the inverted metamorphic triple-junction cells, which employ GaAs, InGaP and InGaAs sub-cells. “These solar cells are potentially lightweight and flexible, but a little bit less radiation hard. Nevertheless, the solar cell from Sharp reaches an end-of-life efficiency comparable to other triple junction cells on germanium.” SolAero is also pursuing this approach, and has produced devices with up to six junctions that are just shy of an efficiency of 28 percent (see Figure 1).

A triple-junction version of the inverted metamorphic has been used in the ALFAMA project. Efforts involved taking a GaAs substrate and depositing a release layer, followed by a 1.9 eV GaInP sub-cell, a 1.4 eV GaAs sub-cell, a metamorphic buffer and a 1.0 eV GaInAs sub-cell. Engineers at tf2 devices removed the release layer by etching, before inverting the structure and adding: an anti-reflection coating and contact to the top of the device; and a metal to the bottom, which provides an electrical contact and aids structural integrity. In principal, the GaAs substrate can be re-used.

The team compared the performance of their device with a standard triple-junction cell. For this control, which has a cell size of 20 cm^2 and a total epitaxial thickness of around 10 μm, the areal density is 13.2 mg/cm^2 and the beginning of life efficiency 26 percent. Efficiency did not degrade during thermal cycling, undertaken to mimic conditions onboard a satellite.

Turning to simulations allowed the team to optimise their structure for different radiation doses. Insights provided by these calculations included the benefits of increasing doping in the contact layers, which improves efficiency through increases in the fill factor and the open-circuit voltage. Following irradiation, cells have produced an efficiency of 25.4 percent and an impressive power-to-mass ratio of 2.6 Watt/gram.

Schön and co-workers used electroluminescence to evaluate the performance of all three sub-cells. They found the material quality in the InGaP and InGaAs cells inferior to GaAs, due to the thermal load and the impact of the metamorphic buffer, respectively.

For the latest generation of cells, improvements were made to thin-film processing, current matching and the anti-reflection coating. Devices had a beginning-of-life efficiency of 30.2 percent.

The power-to weight ratio of the multi-junction cells produced by the project are similar to those of devices made by Sharp and Microlink, formed using a process involving separation of the device from the substrate. For the ALFAMA project, there is a particularly encouraging performance at the beginning of life. “For end-of-life we are optimistic that we will reach the efficiency of the Sharp cell in the near future.”

Scaling germanium

Within the semiconductor industry, a well-worn path to increasing productivity and trimming production costs is to increase the size of the wafer. Recently, Umicore has enabled the III-V solar industry to take another step on this road by offering 200 mm germanium. Investigating this opportunity is Azur Space Solar Power, which has been evaluating the growth of triple-junction cells on this platform through an EU-funded project entitled RadHard.

	I_{sc} (mA)	V_{oc} (V)	I_{mp} (mA)	V_{mp} (V)	P_{mp} (mW)	FF (%)	η (%)
mean	533	2.716	515	2.407	1239	85.6	30.0
medium	533	2.716	515	2.407	1240	85.8	30.1
minimum	530	2.687	508	2.375	1217	84.3	29.5
maximum	535	2.728	518	2.422	1250	86.1	30.3

➤ Table 1. Through the RadHard project, a team of engineers in Europe have made 60 cells with a size of 30.18 cm^2 from 19 wafers with a 200 mm diameter. A high shunt resistance and a scratch led to the discarding of two cells. Electrical performance is determined from current-light-voltage plots using an AM0 spectrum. I_{sc} is the short circuit current; V_{oc} the open-circuit voltage; I_{mp}, V_{mp} and P_{mp} the maximum values for current, voltage and power, respectively; FF is the fill factor; and η the cell efficiency.

Details of its findings were unveiled to delegates in a talk delivered by Tim Kubera from Azur. He explained that the company has established production of triple-junction devices with an efficiency of around 30 percent on 100 mm and 150 mm germanium substrates. MOCVD reactors can routinely accomodate twelve 100 mm wafers or eight 150 mm wafers. However, for the RadHard project the team is using an MOCVD reactor that houses five 200 mm wafers. "By increasing the format we can process more area per run, which should result in cost benefits," said Kubera.

During the RadHard project, efforts at Umicore have been directed at improving the quality of 200 mm germanium. Analysis of the surface, through measurements of the light point defect, indicate that its quality is now comparable to its 150 mm sibling.

A range of metrology techniques have been used to evaluate, across the wafer, the quality of multi-junction epitaxial stacks grown on 150 mm and 200 mm germanium. Growth rates have been determined by a combination of *in-situ* measurements and a profilometer; X-ray diffraction has provided an insight into material quality; and capacitance-voltage plots have tracked doping levels. Analysis of the GaInP top cell indicates that shifting to a larger wafer has little impact on the profiles associated with growth rate and composition. "The only real discrepancy we see is in the relative doping," revealed Kubera. "For the bigger wafers, the emitter doping of the top cell is shown to increase by up to 25 percent at the outer edge." Smaller variations have been observed in key characteristics of the InGaAs region, the Bragg materials and the InAlP window layer.

While this could be improved, it has not prevented the team from assessing the quality of devices produced from the larger foundation. As they are yet to have access to a 200 mm line, they have used a laser process to extract a pair of 100 mm wafers from the 200 mm wafer. This standard size allows the use of an established 4x8 cell design.

Adopting this approach, the team fabricated 60 cells, using nineteen 200 mm wafers from four epi-runs. Measurement on 58 cells showed very little variation between them (see Table 1). The other two cells, both with an efficiency below 29 percent, were discarded; one suffered from a shunt resistance and the other a big scratch.

Kubera concluded his presentation by saying that the development of an epitaxial process for producing triple-junction cells on 200 mm germanium wafers has been carried out quite successfully. "We can already show that the cell performance gets close to the state-of-the-art space cells that we make on 100 millimetre wafers."

Virtual value

An alternative option for scaling that promises large wafers, while realising low costs that might allow multi-junction cells to be used for terrestrial power

Progress on this front, along with that on larger substrates and an increasing number of flexible designs, will increase the prowess of the multi-junction cell. It shows no sign of loosening its vice-like grip on powering satellites, and if chip costs fall, that will improve its chances of generating terrestrial energy.

➤ Figure 2. Test structures suggest that an ultra-thin layer of germanium, deposited by RF plasma-enhanced CVD, could enable the production of multi-junction cells on silicon substrates.

generation, is to grow germanium and III-V layers on silicon substrates. It's an approach that has been pursued for several years by a team from The Technical University of Madrid, with recent efforts shifting to thinner germanium layers.

At this year's EU PVSEC a spokesman for this group, Iván García, provided an overview of the recent work, undertaken in collaboration with researchers at LPICM-CNRS in Palaiseau, France.

Placing the latest work in context, Garcia explained that the team had previously investigated the fabrication of triple-junction cells on silicon that had a germanium layer acting as a low energy sub-cell. The epiwafers were plagued with cracking, due to a difference in the thermal expansion coefficient, exacerbated by the 2-5 µm-thick germanium layer.

Garcia explained that to reduce cracking, they now stay below the critical thickness, having reduced the total thickness for the epistack from 10 µm to 5.5 µm. The first attempts with the new structure produced promising results, but uncovered some issues. On the plus side, the team found that the short-circuit current approached that for a conventional triple-junction cell grown on germanium. However, metastability still plagued the heterostructure, with the thinner structure failing to deliver an improvement in the open-circuit voltage, due to the use of templates with a high threading dislocation density.

To overcome that issue, the team is now using a low-temperature RF plasma-enhanced CVD process, developed by those of the group in France, to deposit ultra-thin germanium layers. "They have achieved high-quality epitaxial layers at temperatures as low as 175 degrees [Celcius]," explained Garcia. "We think this is an advantage, because the lower-temperature processes can be lower cost than higher temperature processes." Using this approach, involving germanium layers with a thickness in the range 20-140 nm, threading dislocation densities can be as low as 5×10^6 cm^{-2}.

One consequence of switching to ultra-thin germanium layers is that they can no longer be used for the low-energy sub-cell. So silicon is employed for the bottom junction. It is a compromise, offering simple low-cost fabrication steps, but the bandgap for the bottom cell is not ideal for terrestrial spectra. What's more, light is absorbed in the geranium layer, reducing the current produced by the silicon sub-cell.

Modelling by the team has determined, for a range of thicknesses for the germanium layer, how thick each of the top two junctions should be to maximise efficiency. "These thicknesses are way below the thicknesses for cracking, which is good," enthused Garcia, who explained that to maximise the performance from the silicon sub-cell, there needs to be back passivation and the introduction of light-trapping technologies.

An alternative approach to increasing efficiency is to increase the bandgap of the top two sub-cells by switching to AlInGaP and AlGaAs. According to modelling, the aluminium content can be below 10 percent, leading Garcia to believe that it should be possible to produce high-quality junctions.

Modelling a range of triple-junction cells with different bandgaps and threading dislocation densities suggests that for a germanium thickness below 60 nm, efficiencies of 30-34 percent under 1 sun are attainable.

"This potential efficiency is less than that obtainable by other techniques, such as wafer bonding, but we think that the simplicity of this method could be worth it," argued Garcia.

To start investigating whether this approach can fulfil its promise, the team produced a tandem cell featuring a germanium layer just 20 nm thick (see Figure 2). These efforts were compromised by: a lack of optimisation of the silicon surface prior to growth; a high threading dislocation density of the template; no back surface passivation in the silicon cell; and impurity in-diffusion, occurring during MOCVD growth of the upper layers. However, despite all this, for some incident wavelengths the device could still produce its target efficiency.

The team is now building on this promising start by using plasma etching to improve the surface of the silicon wafer, and developing techniques to trim the dislocation density, aided by analysis of the interface between silicon and germanium.

Progress on this front, along with that on larger substrates and an increasing number of flexible designs, will increase the prowess of the multi-junction cell. It shows no sign of loosening its vice-like grip on powering satellites, and if chip costs fall, that will improve its chances of generating terrestrial energy.

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Point defects: the ultimate blue LED efficiency killers

A previously unknown class of intrinsic light-quenching point defect is unveiled in InGaN quantum wells

BY THOMAS WEATHERLEY, CAMILLE HALLER, YAO CHEN, JEAN-FRANÇOIS CARLIN, RAPHAËL BUTTÉ AND NICOLAS GRANDJEAN FROM EPFL

TODAY'S InGaN-based LEDs are enjoying tremendous success in general and automotive solid-state lighting. However, this is by no means the limit of their reach – intense industrial and academic research is driving efforts to shrink the dimensions of this device below 10 μm, a feat that will enable the production of microLED displays for augmented/virtual reality, wearable devices, and smartphones.

Deployment of LEDs in all these applications is dependent on the remarkable conversion efficiency of injected electron-hole pairs into photons within the InGaN/GaN quantum wells that lie at the heart of these devices. This light-generating internal quantum efficiency can exceed 90 percent for blue LEDs,

even when the threading dislocation density in the epilayer is as high as 10^8 cm^{-2}. Yet there is a rarely-discussed feature of these LEDs which is crucial to this impressive performance: the 'underlayer'.

Commercial blue/near-UV LEDs are exclusively grown by MOCVD, and their structure always contains an underlayer – either a thick, low-indium-content InGaN layer, or an InGaN/GaN superlattice (see Figure 1 (a)). The motivation for including this underlayer, which sits beneath the quantum wells, is highlighted in device measurements that underscore the hike in efficiency it provides (see Figure 1 (b)).

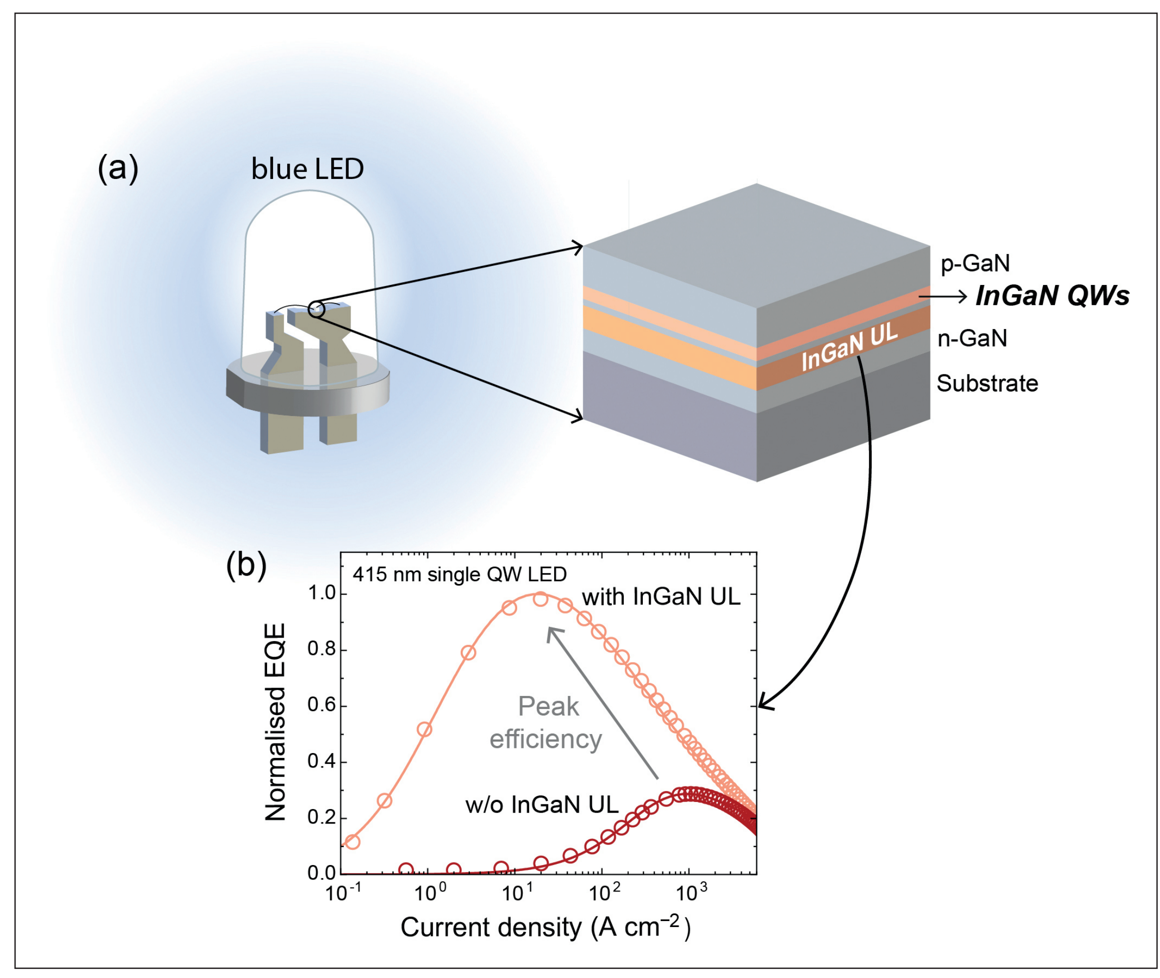
While there is no doubt of the benefit of this underlayer, its mechanism for increasing efficiency has been disputed for many years. Some have argued that the gains in performance come from increased efficiency of electron-hole pair injection into the quantum wells; others point to greater shielding of carriers from light-quenching dislocations; there are those that claim the underlayer aids device performance by mitigating lattice-mismatched strain in the wells; and some have postulated that the efficiency is improved by a reduction in the built-in electric field across the wells that quashes the quantum-confined Stark effect.

Working at EPFL, our team carefully considered all of these explanations, before ruling them out, one by one (see Further Reading). Through careful research, we can now uncover the real reason behind the benefit of the underlayer: it counteracts point defects which act as nonradiative recombination centres inside the InGaN wells.

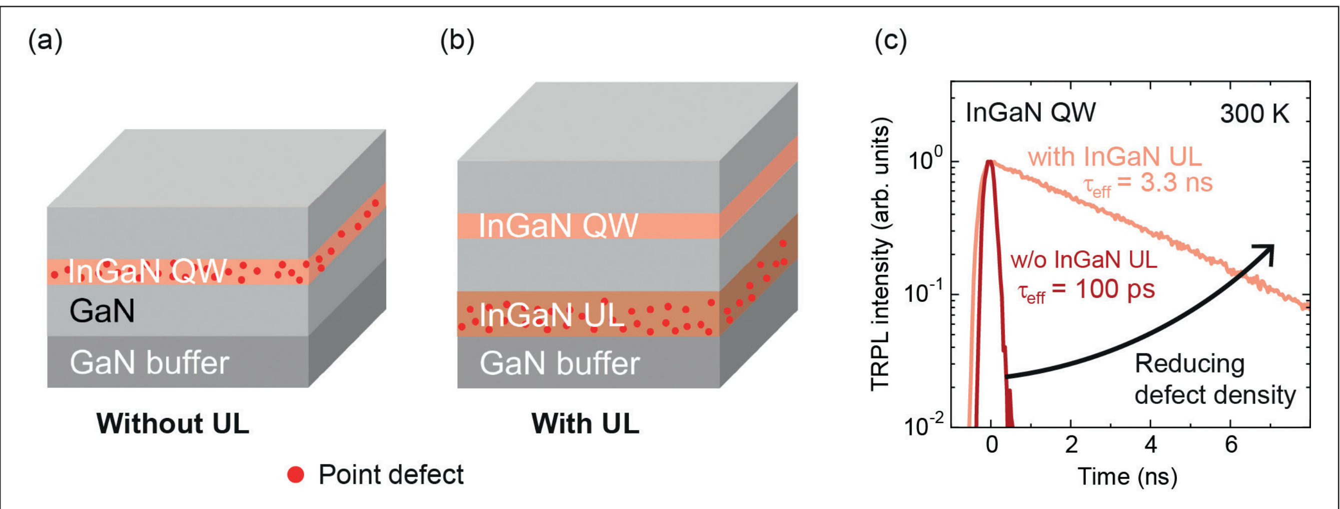
These previously unknown point defects have a strong interaction with indium, so the introduction of an InGaN underlayer provides a sink to trap them before they can reach the quantum well. Failure to use this underlayer allows the point defect density inside the wells to reach as high as 10^{16} cm^{-3}, killing the quantum efficiency of blue-emitting LEDs.

Elucidating the role of the underlayer

In our proposed mechanism, we hypothesise that when there is no underlayer, point defects are present in the InGaN quantum wells. Adding an underlayer



➤ Figure 1: (a) Blue LEDs have an active region containing InGaN/GaN quantum wells (QWs). All commercial structures also include a low indium content underlayer (UL, in brown). (b) External quantum efficiency (EQE) related to current density for two blue-emitting LED structures, with and without an underlayer. Using the underlayer brings a near four-fold increase in peak efficiency.



➤ Figure 2: (a) and (b) show proposed scenarios for growth without and with an underlayer (UL), respectively. Without an underlayer, there is a high concentration of point defects in the quantum well, whereas using an underlayer traps the point defects before the quantum well. (c) Examples of time-resolved photoluminescence (TRPL) decay curves obtained on samples with and without an underlayer; the increase in quantum well-effective carrier lifetime (related to the slope of the decay) with the addition of an underlayer clearly indicates a reduction in the point defect density in the quantum well.

traps these defects, leaving a high-efficiency quantum well (see Figure 2).

So far, it has not been possible to detect these point defects by common chemical analysis methods, such as secondary-ion mass spectrometry (SIMS). Instead, to track changes in point defect density, we need to analyse the degree of nonradiative recombination that occurs inside the quantum well. We accomplish this by using time-resolved photoluminescence to determine the room-temperature effective lifetime of carriers inside standard, 2.7 nm-thick $In_{0.12}Ga_{0.88}N$ single-quantum-well samples.

As all other parameters are unchanged between samples, any increase in the effective carrier lifetime is attributed to a decrease in the nonradiative recombination rate and hence a lower point defect density inside the well (see Further Reading for more details). Unsurprisingly, the underlayer provides a huge increase in the quantum-well effective carrier lifetime (see Figure 2 (c)), a trait indicative of a drastic decrease in the point defect density inside the well. This begs the question: what is the key ingredient in this underlayer that excels in trapping point defects?

To try and answer this, we grew a series of samples in an Aixtron 3 x 2-inch showerhead MOCVD reactor, making changes to underlayer materials and thicknesses. We used 2-inch Sumitomo Electric freestanding GaN substrates with a dislocation density of only about 10^6 cm^{-2} (see Figure 3 (a)).

Our efforts began by considering whether the low-temperature growth of a layer of GaN could deliver a decrease in the point defect density in the InGaN quantum well. Unfortunately, this is of limited benefit, providing only a very modest increase in effective carrier lifetime, even for a GaN underlayer over 200 nm-thick (see Figure 3 (b)).

Far better results are realised by introducing indium to the underlayer. The addition of an indium content of just 3 percent yields a dramatic improvement in the effective carrier lifetime, even for an underlayer thickness of just 50 nm. This benefit, stemming from a massive decrease in the point defect density in the well, underlines the importance of indium to the defect-trapping process.

To illustrate the role of indium, we grew another series of samples with underlayers of identical thickness but varying indium content (see Figure 3 (c)). Measurements on these samples show that increasing the indium content has the same effect in reducing point defects as increasing the underlayer thickness. This result demonstrates that it is the sheer quantity of incorporated indium atoms that governs the number of trapped point defects.

Notably, this indium-content sample series was grown using a different MOCVD reactor – an Aixtron horizontal 200/4 RF-S – and on sapphire substrates, confirming that the indium-related point defect trapping mechanism is independent of precise substrate or reactor conditions. More recent work has demonstrated that even for samples grown on silicon (111) substrates, which can have dislocation densities as high as 10^{10} cm^{-2}, trapping point defects using an underlayer is still crucial to attain high-efficiency InGaN quantum wells.

Since indium plays the critical role in this mechanism, there is no reason to be restricted to using InGaN underlayers. In its place could be an InAlN underlayer that's nearly lattice-matched to GaN, allowing

the same defect density reduction. We tested this hypothesis, finding that InAlN is an attractive alternative (see Figure 3). With InAlN, there is a larger indium content in the underlayer, typically 15 percent. Consequently, it is possible to realise the same point-defect-density reduction, and hence efficiency improvement, with a thinner underlayer.

Drawing on these results, we propose a specific chronology. Initially, there are surface defects present during GaN buffer growth. During subsequent GaN growth, these defects remain at the surface, until the growth of any indium-containing layer. When indium is introduced, these atoms interact with surface defects to form nonradiative point defects in the bulk material.

Using this concept, we developed a model that links the key properties of the underlayer, such as its indium content and its thickness, to the effective carrier lifetime in the InGaN quantum well. Fitting the data with this model, where crucially the term defining the interaction efficiency of the surface defects with the indium atoms is the same across all sample series (see Further Reading), confirms that indium alone plays the critical role in incorporating these surface defects to form point defects (see Figure 3).

Following on from this finding, we pinned down the origin of these surface defects. Since they seem to arise from the GaN buffer, we considered the impact of any difference in the growth conditions of this layer to that of the rest of the structure. For many III-nitride heterostructures, to ensure a flat surface morphology, it is common practice to grow the GaN buffer at very high temperatures (around 1000 °C): we wondered whether this higher temperature is behind the generation of surface defects.

To determine whether this is the case, we grew another portfolio of samples. No underlayer was included in this series; instead, we varied the growth temperature of the GaN buffer and monitored the effect on the quantum well (see Figure 4 (a)). We found that raising the growth-temperature of the buffer directly reduced the effective carrier lifetime in the quantum well (see Figure 4 (b)). Based on this observation, we can conclude that surface defects are generated by high-temperature GaN growth, with temperatures of around 850 °C or more threatening to drag down quantum-well efficiency.

These results also offer some hints into the nature of the surface defect. As the point-defect-trapping mechanism has been the same in samples produced with different MOCVD reactors, which will have different impurity environments, these surface defects must be intrinsic. We point our finger at the nitrogen vacancy, which has a low formation energy at high temperature and at the surface. This possibility is supported by both experimental and theoretical results (see Further Reading).

Our final view is that the formation of the efficiency-sapping point defects in the quantum wells begins with the generation of surface nitrogen vacancies, formed during high-temperature GaN growth. These vacancies remain at the surface during the growth of any low-temperature GaN layers that follow. When an indium-containing layer is grown – this could be the underlayer, or a quantum well – nitrogen vacancies interact with indium atoms to form point defects in the bulk that act as nonradiative recombination centres. At this stage it is critical to recognise that the nature of these final nonradiative recombination centres buried in InGaN is still unknown. They may take the form of group-III-nitrogen divacancies, or even a group-III vacancy associated with an impurity such as oxygen.

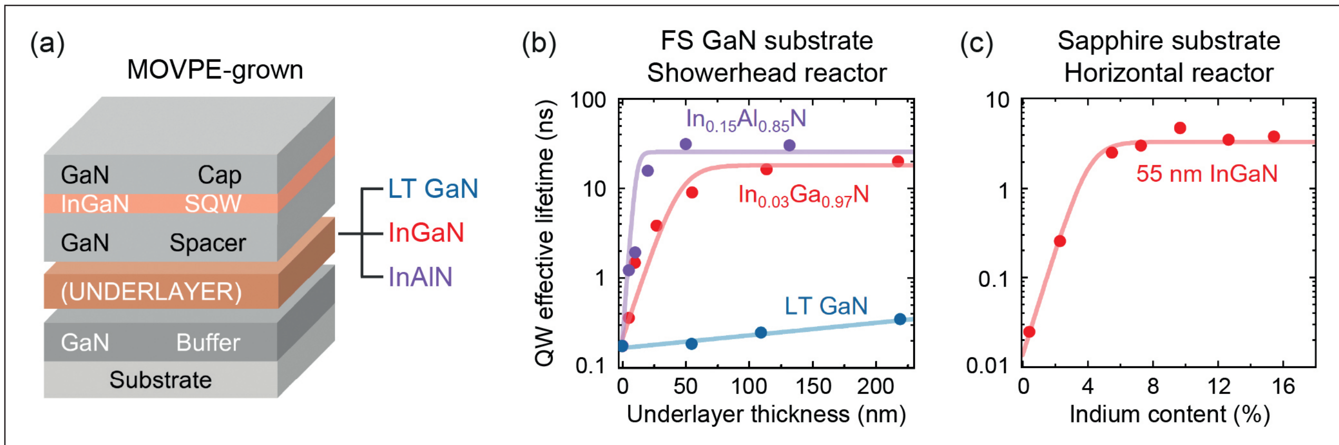
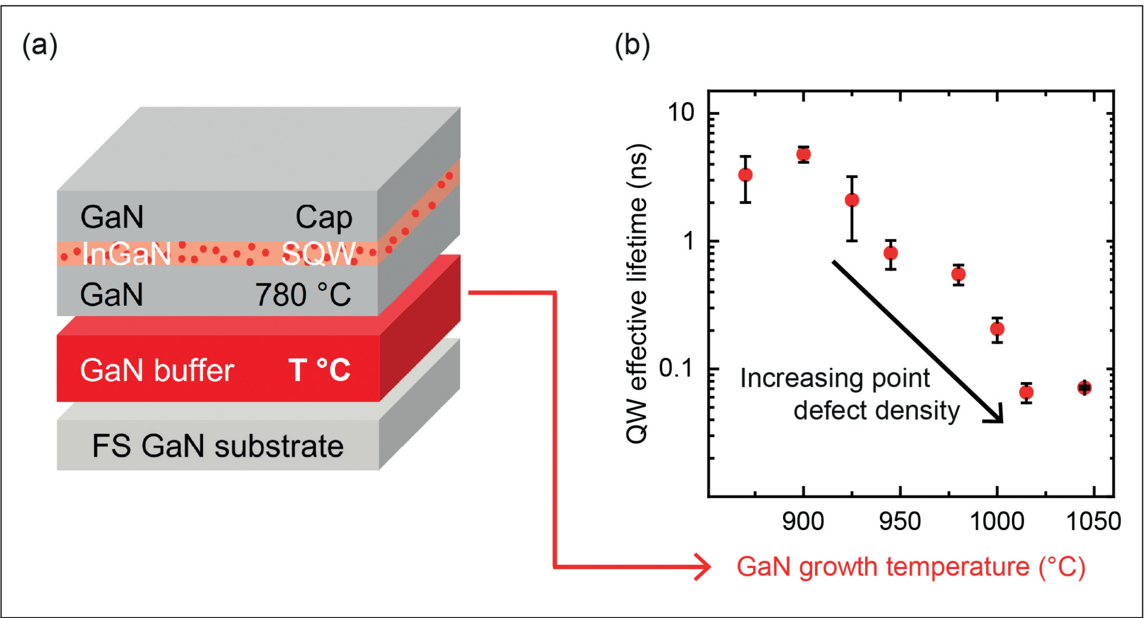


Figure 3: (a) The standard structure used by the researchers at EPFL is a 2.7 nm-thick $In_{0.12}Ga_{0.88}N$ single quantum well. The underlayer material is varied in this structure between GaN grown at low-temperature (LT), InGaN, and InAlN. (b) Quantum-well effective carrier lifetime against the underlayer thickness for these three materials for samples grown in a showerhead MOCVD reactor on freestanding (FS) GaN substrates. The more indium an underlayer contains, the more immediate the effective carrier lifetime improvement is, indicating a more rapid decline in the point defect density. Using just GaN results in barely any improvement. The critical role that indium plays in the underlayer is emphasised in (c), which demonstrates that a similar point defect density reduction can be obtained without changing the underlayer thickness, but by simply increasing the indium content in the InGaN alloy; this sample series was grown in a horizontal reactor on sapphire substrates. Lines indicate fits to the experimental data obtained using a surface defect burying model.



➤ Figure 4: (a) EPFL's new sample series structure, containing no underlayer. Instead, the growth temperature, T, of the GaN buffer beneath the $In_{0.12}Ga_{0.88}N$ single quantum well is varied to test whether surface defect creation is related to high-temperature growth. (b) The drastic decrease in quantum-well effective-carrier-lifetime on increasing the growth temperature for the GaN buffer demonstrates that high-temperature GaN growth is directly responsible for generating surface defects, which then interact with indium in the quantum well to form nonradiative recombination centres.

Imaging point defects

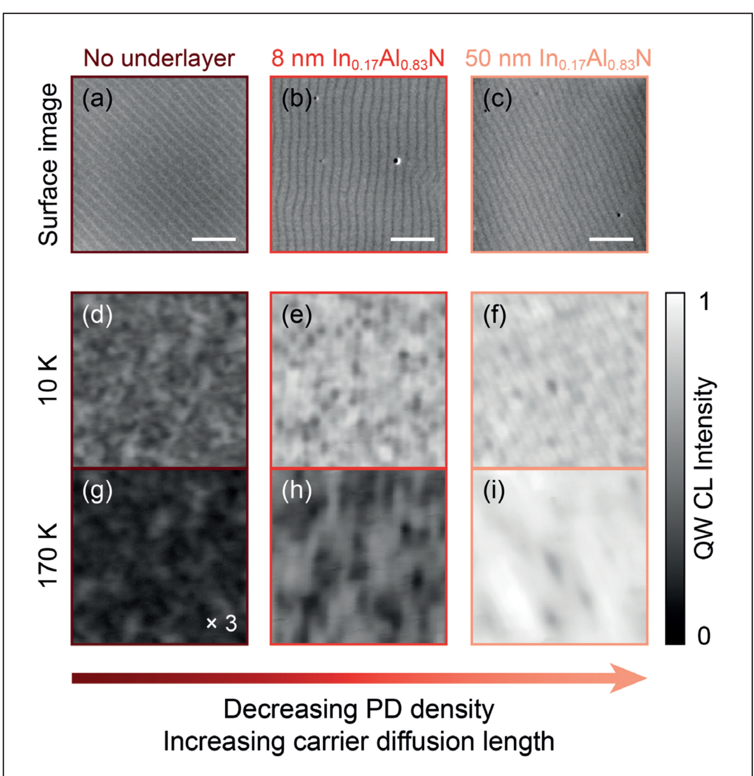
The work we have discussed so far has enabled us to fully elucidate the roles of both the underlayer and point defects on the quantum efficiency of InGaN/GaN quantum wells. To get this far, it was essential to exclude previous explanations that are non-defect related, a task we accomplished by producing many different carefully designed sample series. Such work requires much thought and consideration, partly because the effective carrier lifetime is an indirect metric for point defect density, and is sensitive to a variety of factors that include well structure, disorder, electric field, and strain. Clearly, our findings would be more compelling if we had a direct estimation of the actual point defect density in the well. To do this, we need a way to directly detect and even image the point defects that are buried inside the quantum well.

It is far from easy to spatially resolve individual atomic-scale nonradiative point defects buried inside a heterostructure, particularly if they are present at high densities. Structural microscopy techniques, such as transmission electron microscopy, are unsuitable because they are incapable of imaging single-atom-scale features hidden inside bulk material. Super-resolution imaging is also inadequate, because nonradiative defects do not exhibit localised light emission. Indeed, it might be that the difficulty of directly detecting intrinsic point defects in heterostructures is a contributing factor to why, only now, are they being seriously implicated in InGaN quantum-well efficiency, even though InGaN quantum-well devices, like LEDs and laser diodes, are well established products that have been produced for decades.

To overcome these issues, we turned to cathodoluminescence. Using this technique, we scanned an electron beam over the quantum well at scales below the diffraction-limit of light. By collecting luminescence intensity from the sample at each electron-beam excitation position, we built up a cathodoluminescence intensity map of the scanned area. Defects present in this area appear as dark regions in the image, due to local nonradiative recombination of excited carriers.

Success is not guaranteed with cathodoluminescence. To ensure the highest spatial resolution, it is critical to carefully design the experimental conditions and the sample structure. We turned down the electron beam energy to just 1.5 keV, to minimise the excitation volume; and we employed a very thin, single $In_{0.15}Ga_{0.85}N$ quantum well – it is just 0.8 nm-thick – to minimise carrier diffusion lengths (see Further Reading). Additional features of this portfolio of structures are an $In_{0.17}Al_{0.83}N$ underlayer to control the point defect density in this quantum well, accomplished by varying the thickness of the underlayer from sample to sample; and freestanding GaN substrates, to mitigate the impact of threading dislocations.

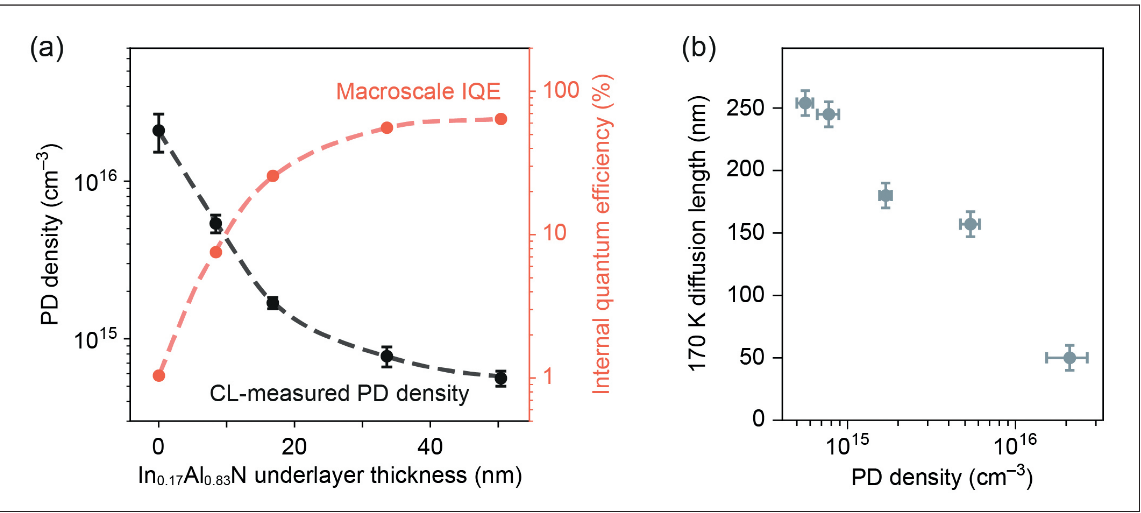
Cathodoluminescence images obtained from 2 µm by 2 µm scans of the quantum-well samples are shown in Figure 5. In images obtained at 10 K, dark spots that are unrelated to dislocations are immediately clear. Each of



➤ Figure 5: (a–c) Secondary electron images for three $In_{0.15}Ga_{0.85}N$/GaN single-quantum-well samples with different thickness $In_{0.17}Al_{0.83}N$ underlayers; these images show the surface morphology of the samples. Step-edges are clear as parallel lines and V-shaped pits marking the position of threading dislocations are visible as dark spots. All are 2 μm × 2 μm (500 nm scale bar). (d–f) show the quantum-well cathodoluminescence (CL) intensity images of the same 2 μm × 2 μm area for each sample at 10 K. Dark regions have no correlation with dislocation positions, and are instead a direct consequence of non-radiative recombination at single point defects. The decrease in density of the dark spots as the underlayer thickness is increased represents a decrease in point defect density. As the temperature is raised to 170 K, CL images on the same area again (g–i) clearly illustrate that nonradiative recombination is thermally activated. The loss of resolution in these 170 K images also indicates an increase in carrier diffusion length. Each image is plotted on an absolute intensity scale from 0 – 1. The 170 K intensity for the sample without an underlayer has been multiplied by three to make the image visible.

these spots corresponds to a single killer nonradiative point defect inside the well. From this experiment it is easy to directly see the impact of the underlayer: the number of dark spots drastically decreases as the underlayer thickness increases, because this drives down the point defect density in the quantum well.

Differences between the samples are more obvious when measurements are made at 170 K (see Figure 5 (g) to (i)). Due to the thermally-activated nature of defect-related nonradiative recombination, at this temperature each point defect has a much greater impact on the cathodoluminescence intensity. The increased thermal energy also leads to longer carrier diffusion lengths and hence a reduction in the spatial resolution, visible as a smoothening of the images compared with those obtained at 10 K. Note that the less-defective samples have much smoother



➤ Figure 6: (a) Point defect (PD) densities inside the InGaN/GaN quantum well as the InAlN underlayer thickness is varied, measured directly from similar cathodoluminescence (CL) images to those in Figure 5. These densities are compared to the macroscale internal quantum efficiency (IQE) measured for the same samples using time-resolved photoluminescence at room temperature. As expected, the drop in point defect density is directly reflected by a huge rise in IQE. Carrier diffusion lengths are also measured by CL at 170 K, and are compared to the PD densities in (b). Decreasing the PD density to less than 10^{15} cm^{-3} (thickest underlayer sample) leads to a significant increase in the carrier diffusion length. Dashed lines are guides to the eye.

cathodoluminescence images at 170 K (see Figure 5(i)) than the highly-defective samples (see Figure 5(g)); this directly indicates an increase in carrier diffusion length as the point defect density in the quantum well reduces.

Careful analysis of these cathodoluminescence images (see Further Reading) has enabled us to extract point defect densities and 170 K carrier diffusion lengths for five samples with different underlayer thicknesses (see Figure 6). Comparing these properties to the macroscale room-temperature internal quantum efficiencies measured by time-resolved photoluminescence provides a clear, unequivocal picture of the roles of the underlayer and of point defects: inserting an underlayer decreases the point defect density in the well from 10^{16} cm^{-3} to around 10^{14} cm^{-3}, enabling macroscale efficiency at room temperature to rise from only 1 percent to above 60 percent. Another insight is that adding a thick underlayer leads to a significant increase in the carrier diffusion length. Based on these findings, taking these killer point defects into account is crucial when designing microLEDs.

The road ahead

There is merit in revisiting previous design decisions, armed with this new knowledge of indium-interacting point defects and the underlayer mechanism in InGaN/GaN quantum well structures. For instance, we can now see that the low indium content cladding layers in InGaN-waveguide laser diodes are probably behaving as underlayers, improving device efficiency. But several questions remain: is one of the reasons behind the success of multiple-quantum-well structures that the lower quantum wells act as underlayers, ensuring high-quality upper quantum wells? How many previous results were skewed, due to unaccounted point defects inside the well? Is growing GaN at high temperatures, on balance, detrimental or beneficial? Could these point defects be related to the 'green gap', the phenomenon behind the low efficiency of high-indium-content InGaN quantum wells? The implications of our findings are widespread, and they require much further investigation.

There is merit in revisiting previous design decisions, armed with this new knowledge of indium-interacting point defects and the underlayer mechanism in InGaN/GaN quantum well structures

Note, though, that having unlocked direct imaging of nonradiative point defects inside heterostructures, we can now more easily detect intrinsic point defects. In addition to visible LEDs, these defects might be limiting the performance of other III-nitride devices, such as deep-UV LEDs. Our advances in imaging are also laying the foundation for new point defect studies, including time-resolved measurements at a single buried point defect.

FURTHER READING

- C. Haller *et al*. Burying non-radiative defects in InGaN underlayer to increase InGaN/GaN quantum well efficiency. Appl. Phys. Lett. **111** 262101 (2017)
- C. Haller *et al*. GaN surface as the source of non-radiative defects in InGaN/GaN quantum wells. Appl. Phys. Lett. **113** 111106 (2018)
- Y. Chen *et al*. GaN buffer growth temperature and efficiency of InGaN/GaN quantum wells : The critical role of nitrogen vacancies at the GaN surface. Appl. Phys. Lett. **118** 111102 (2021)
- T. F. K. Weatherley *et al*. Imaging nonradiative point defects buried in quantum wells using cathodoluminescence. Nano Lett. **21** 5217-5224 (2021)

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Targeting medium-voltage power electronics with vertical GaN devices

Vertical GaN *p-n* diodes combine excellent efficiencies with incredibly fast protection from unwanted electromagnetic pulses

BY ROBERT KAPLAR FROM SANDIA NATIONAL LABORATORIES, TRAVIS ANDERSON FROM THE NAVAL RESEARCH LABORATORY, SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY AND OZGUR AKTAS FROM EDYNX

WE ARE LIVING in an age of increased awareness of energy efficiency. This is partly caused by concerns over global warming, rammed home by alarming images of this year's floods and heat waves. However, it also comes from increasing use of battery power, particularly in transportation, and the need to make the most out of this stored energy.

For the electric grid and various microgrids, demand is on the rise for high-efficiency solid-state power conversion in the medium-voltage range, which roughly spans 1.2 kV to 20 kV. Power converters operating in this domain could serve in solid-state transformers operating at the grid distribution-level, such as those at 13.8 kV, as well as DC microgrids, including those proposed for all-electric aircraft at 10 kV.

Thanks primarily to a breakdown electric field that

is far higher than that of silicon, wide-bandgap semiconductors, such as SiC and GaN, offer outstanding opportunities for improving medium-voltage power electronics. As well as reducing on-resistance, they can increase conversion efficiency and slash system size, due to higher switching frequencies. Of the two successors, GaN may ultimately have the upper hand at voltages of 10 kV and more, due to its higher electron mobility (see Figure 1).

The results shown in Figure 1 compare the performance of a type of GaN vertical power transistor known as a CAVET – its full name is a Current-Aperture Vertical-Electron Transistor – with a SiC MOSFET. Note, however, that the trend is applicable to other types of vertical power device. The term 'vertical' is used for device architectures that contain a thick, low-doped drift region. This layer provides the blocking voltage and governs the on-resistance of the device.

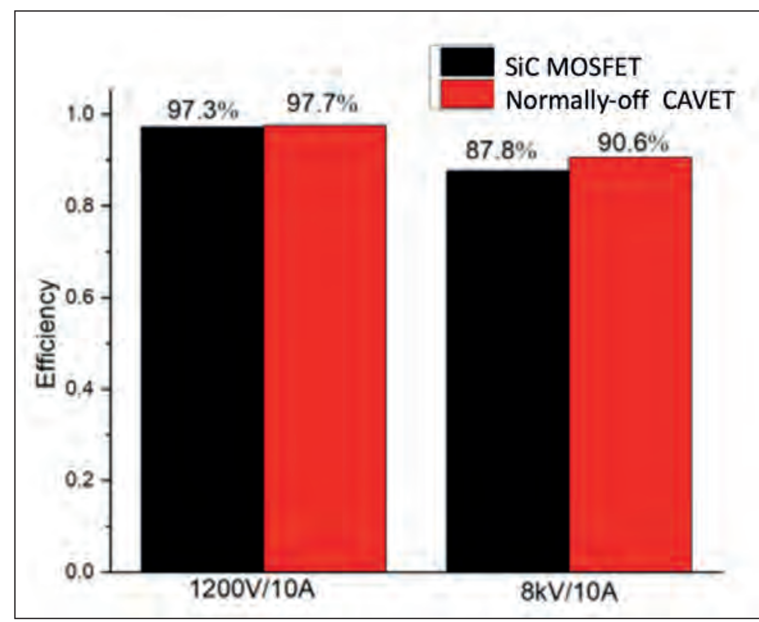
As the operating voltage increases, the efficiency of the GaN converter improves relative to that of SiC (this can be seen by comparing the performance of 1.2 kV and 8 kV devices). At first glance, the increase is trivial, but this overlooks the need to consider the difference from 100 percent efficiency. Evaluated in this manner, which hones in on the loss, the difference is substantial.

One major downside of vertical GaN devices is that they are not as mature as their SiC cousins, and in this regard, in a different league from those made from silicon. To fully evaluate the feasibility of vertical GaN there needs to be ongoing improvements in the epitaxial growth of GaN on its native substrate, as well as advances in device processing, such as those that enable effective edge-termination structures.

To this end, our US collaboration, led by researchers at Sandia National Labs and involving engineers at the Naval Research Laboratory, Stanford University, Edynx, and Sonrisa Research, has established a vertical GaN foundry that is targeting 1.2 kV, 3.3 kV, and 6.5 kV devices. This holistic effort combines epitaxial growth with wafer metrology, device design, processing and characterization – the latter includes investigation of yield, reliability testing, and failure analysis.

We are also undertaking a parallel effort that is focusing on higher-voltage structures, eventually up to 20 kV, and targeting specialized devices with a very fast breakdown that are capable of protecting the electric grid from electromagnetic pulses.

We have undertaken extensive mapping of bare GaN substrates and epiwafers with GaN *p-n* diode structures grown by MOCVD. Tools for this mapping include an optical profiling system, Raman spectroscopy, and typical mercury probe. The profiling system's capabilities are illustrated in Figure 2, which



➤ Figure 1. Simulated switching efficiency improvement for vertical GaN CAVETs (a type of vertical transistor) compared with SiC MOSFETs at 1.2 kV and 8 kV. Mobilities of 950 $cm^2 V^{-1} s^{-1}$ and 1200 $cm^2 V^{-1} s^{-1}$ are used for SiC and GaN, respectively (taken from D. Ji *et al.* Int. J. High-Speed Elec. Sys. **28(01n02)** 1940010 (2019)).

has maps of three 2-inch wafers featuring 8 μm, 10 μm and 12 μm-thick drift layers with a net doping density of 1.3×10^{16} cm^{-3}. For our foundry effort, we tend to use such structures for fabricating 1.2 kV devices.

Fabrication of our devices occurs at the 2-inch wafer scale, using a foundry environment at the US Naval Research Laboratory. Here, standard processing techniques for III-N devices realize contacts, isolation, and so on.

Evaluating edge termination

When producing these GaN diodes, the most critical process step is edge termination, which is realized by ion implantation. Although etch-based processes have been shown to achieve high performance, we employ implantation for the foundry, because this enables a planar process that is compatible with true foundry manufacturing. Using ion implantation, we have processed epitaxial wafers into devices with various combinations of junction termination extensions and guard rings (see Figure 3 for photos of typical GaN foundry wafers and associated forward current-voltage characteristics). Measurements on our diodes reveal excellent turn-on behaviour and electroluminescence typical of a GaN *p-n* junction.

For diodes with areas ranging from 0.1 mm^2 to 1.0 mm^2, forward current capability is more than 5 A, corresponding to current densities spanning 500 A cm^{-2} to 5000 A cm^{-2}. The related specific on-resistance is 0.3 mΩ-cm^2 to 1.2 mΩ-cm^2.
We have also assessed the breakdown voltage of our

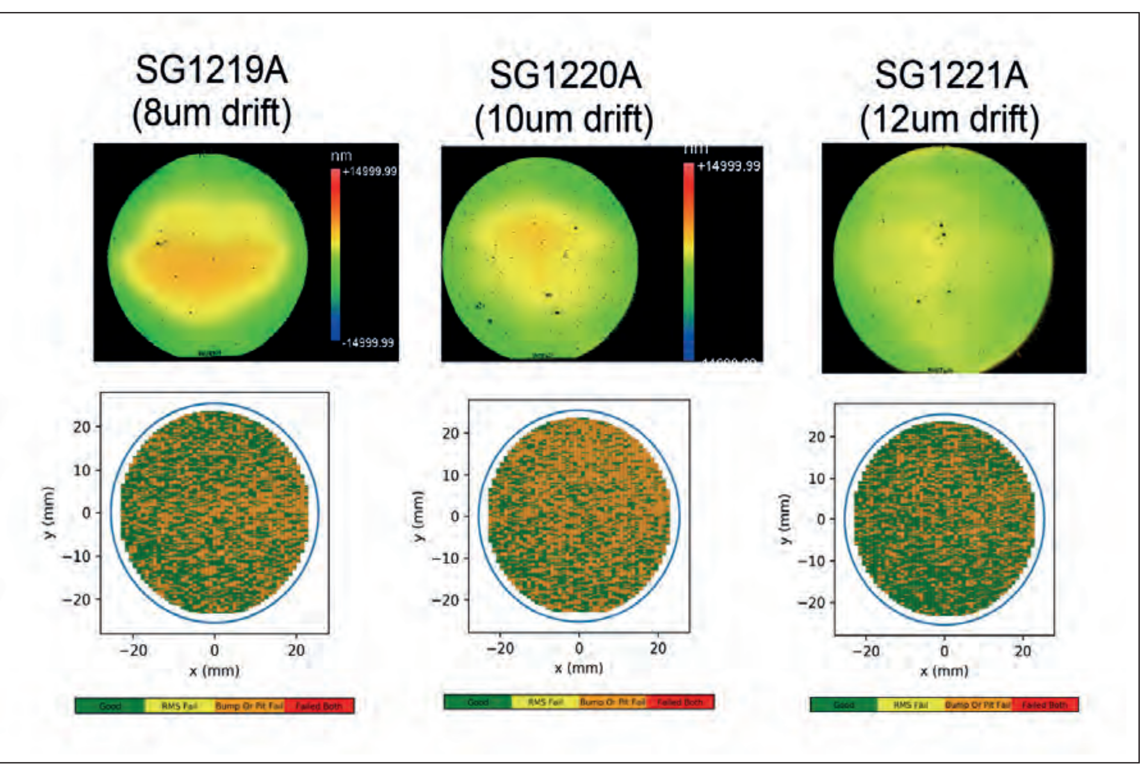


Figure 2. Optical profiles of 2-inch diameter GaN substrates with 8 μm, 10 μm, and 12 μm drift regions grown by MOCVD. The top portion of the figure shows the raw data, while the bottom portion shows yield maps: green indicates a good device; yellow a failure due to root-mean-square (RMS) roughness; orange a failure due to a bump or pit; and red a failure due to both modes.

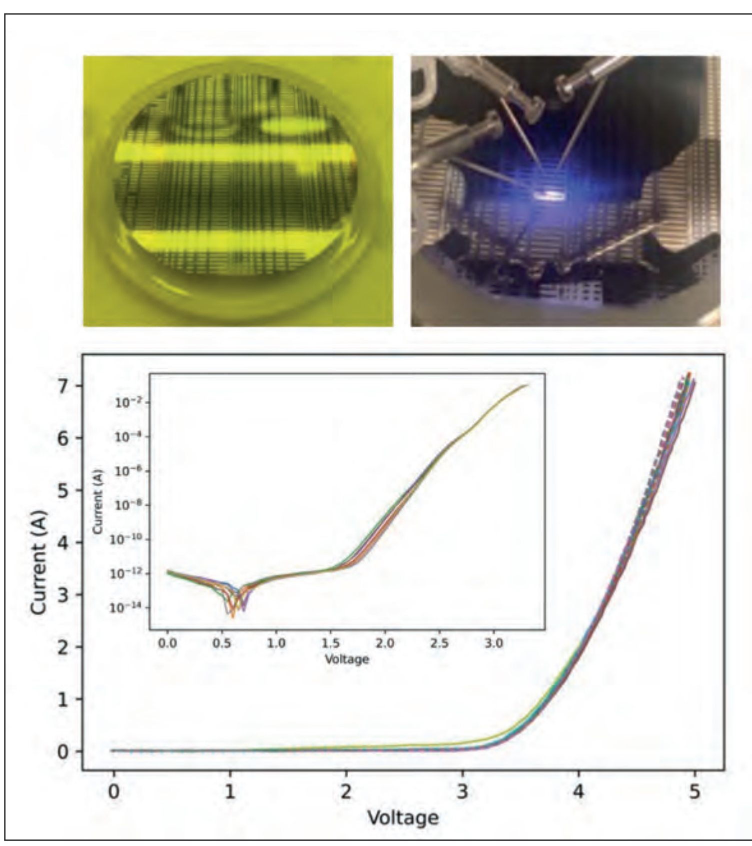


Figure 3. A photo of a typical GaN *p-n* diode foundry wafer (top left), and such a wafer under test (top right), with visible sub-bandgap light emission. The bottom portion of the figure shows representative forward current-voltage curves (main figure, linear scale; inset, log scale).

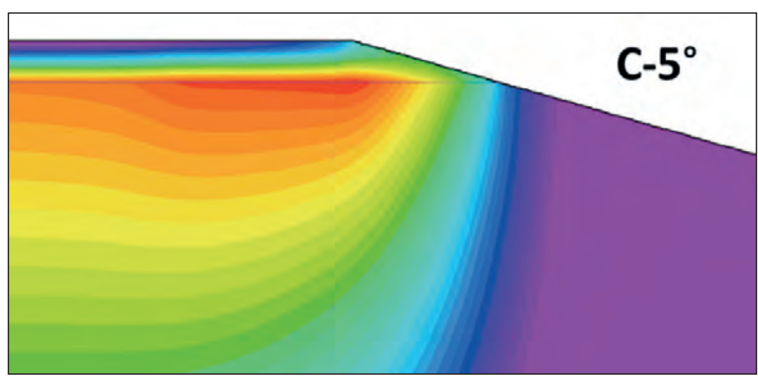
devices. Sampling twelve of them from a single wafer shows that the breakdown voltages exceeds 1.3 kV in all cases – this is approximately 90 percent of the theoretical parallel-plane limit. Note that the precise nature of the breakdown depends on the details of the edge termination. Devices receiving a shallower termination implant profile exhibit a breakdown indicative of avalanche behaviour and characterized by an abrupt increase in current.

We are also exploring other approaches to edge termination. They include a bevel design, which we have evaluated with extensive numerical simulations (one example is shown in Figure 4, with results for a 5° bevel). One key finding of this work is the need for very small bevel angles, employed to ensure that the electric field at the edge of the structure is maintained below the ideal parallel-plane maximum electric field (it is around 3.1 MV/cm for the case shown). We have drawn on the results of simulations to guide our fabrication of bevel-terminated diodes, using either a flowed photoresist for bevel angles of 5°, 15°, and 50°, or greyscale lithography for a bevel angle of 1°.

With vertical GaN power devices at an early stage of development, it is not surprising that reliability studies are relatively rare. Our team is adding to them, using high-temperature operating life tests to assess the diode forward-current stability, and evaluating reverse-current stability with high-temperature reverse-bias testing. In both cases, test conditions are carefully monitored to ensure that the device's temperature and its bias stay constant throughout this test.

One key finding of these investigations is that there is a significant increase in the forward current during high-temperature operating life testing. Another important observation is that when the diode is biased in the avalanche region, there is a change in the avalanche current during high-temperature reverse-bias testing. Thermal considerations limit the DC avalanche current, which exhibits a thermal transient during the first minute at elevated temperatures.

Our team has also conducted failure analysis on selected failed devices. This includes inspecting a diode that failed high-temperature reverse-bias testing with emission microscopy (see Figure 5). Using this technique, we observed that the emission is near the edge termination of the device, indicating that this portion of the diode is responsible for its failure.



➤ Figure 4. Electric field magnitude for a 5° bevel termination with an 8 μm-thick drift region with a net *n*-type doping of 1.3×10^{16} cm^{-3} and a 500 nm-thick anode layer with a magnesium concentration of 3×10^{17} cm^{-3} to achieve *p*-type doping.

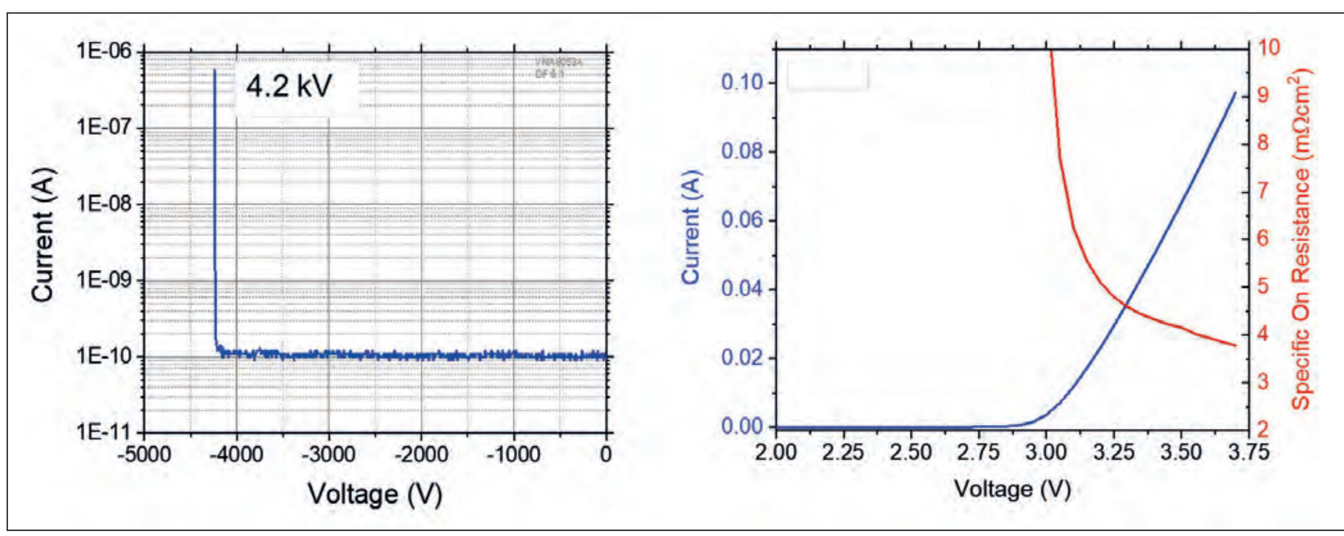
Protecting the grid

Electromagnetic pulses pose a significant threat to the electric grid, as they could potentially cause blackouts over an extremely large geographical area. For electromagnetic pulses with transients shorter than a microsecond, over-voltage conditions that ensue could cause damage to today's grid. One solution is to introduce fast breakdown GaN *p-n* diodes – they are capable of clamping the voltage across equipment on the grid when it is subjected to such pulses.

A target voltage for this specialized but critical application is 20 kV. This blocking voltage provides an adequate margin for protecting, with a single device, distribution-level equipment, when typically operating at up to 13 kV; and it provides a building-block for protecting sub-transmission equipment, as only a small number of stacked devices are needed to reach 69 kV, a typical requirement for this application.

We have started on the path to producing 20 kV devices, with efforts to date focusing on '5 kV class'

➤ Figure 5. Left image shows an emission microscopy image of a GaN *p-n* diode at 1 kV and 0.5 mA under 2.5x magnification. A single emission spot is visible at the corner of the device at the termination of the junction-termination extension. Right image shows expanded view of the emission spot.



➤ Figure 6. Current-voltage characteristics of GaN *p-n* diodes with 45 μm-thick drift regions intended for an electromagnetic pulse arrestor. Left panel shows low reverse-bias leakage current and breakdown around 4.2 kV; and right panel shows forward-bias current and differential specific on-resistance, which is approximately 3.8 mΩ cm^2 at 3.75 V.

While vertical GaN power devices hold promise for medium-voltage power electronics, challenges must still be overcome related to substrates, epitaxial materials growth, and device processing. Additionally, there is a need to characterise and understand yield and reliability, to enable the fabrication process to become commercially viable

GaN *p-n* diodes. These devices have an epitaxial structure that consists of a 45 μm-thick drift region with a net *n*-type doping in the 2-5×10^{15} cm^{-3} range. Like the foundry diodes, the structure has been grown by MOCVD. The anode design contains a two-layer *p*-region with a *p*-minus layer (magnesium level of around 1×10^{18} cm^{-3}) near the junction and a higher *p*-doped layer (magnesium level of around 3×10^{19} cm^{-3}) on top. After epitaxial growth, wafers are processed using a multi-step junction-termination flow, using sequential BCl_3/Cl_2 inductively coupled plasma etches.

Electrical measurements of a representative 150 μm-diameter diode reveal that it is extremely well-behaved under reverse bias, exhibiting a low leakage current until the onset of abrupt breakdown at around 4.2 kV (see Figure 6). When operated under forward bias at 3.75 V, the diode shows good turn-on and a differential specific on-resistance of 3.8 mΩ-cm^2, calculated when defining the area as that of the *p*-contact.

To assess the capability of these diodes for electromagnetic pulse protection, we measured response times with a transmission-line system. This approach, drawing on a setup previously used to measure the reverse-recovery time of GaN *p-n* diodes, provides an upper bound of 1.3 ns for the time to breakdown. This incredibly short time demonstrates that this diode can arrest the fast component of an electromagnetic pulse.

While vertical GaN power devices hold promise for medium-voltage power electronics, challenges must still be overcome related to substrates, epitaxial materials growth, and device processing. Additionally, there is a need to characterise and understand yield and reliability, to enable the fabrication process to become commercially viable. Our team is examining these issues as we establish a foundry for fabricating vertical GaN *p-n* diodes. Additionally, we are pursuing specialized applications, such as electromagnetic pulse protection, that utilize the diodes' fast breakdown response. Further research will determine the full extent of the capabilities of vertical GaN power devices.

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REFERENCES

- I. C. Kizilyalli *et al*. "Vertical Power PN Diodes Based on Bulk GaN," IEEE Trans. Elec. Dev. **62** 414 (2015)
- D. Ji *et al*. "On the Progress Made in GaN Vertical Device Technology – Special Issue on Wide Band Gap Semiconductor Electronics and Devices," Int. J. High-Speed Elec. Sys. **28(01n02)** 1940010 (2019)
- I. C. Kizilyalli *et al*. "Reliability Studies of Vertical GaN Devices Based on Bulk GaN Substrates," Microelec. Rel. **55** 1654 (2015)
- J. S. Foster Jr. *et al*., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," Defense Technical Information Center (2008)
- D. Mauch *et al*. "Ultrafast Reverse Recovery Time Measurement for Wide-Bandgap Diodes," IEEE Trans. Power Elec. **32** 9333 (2017)

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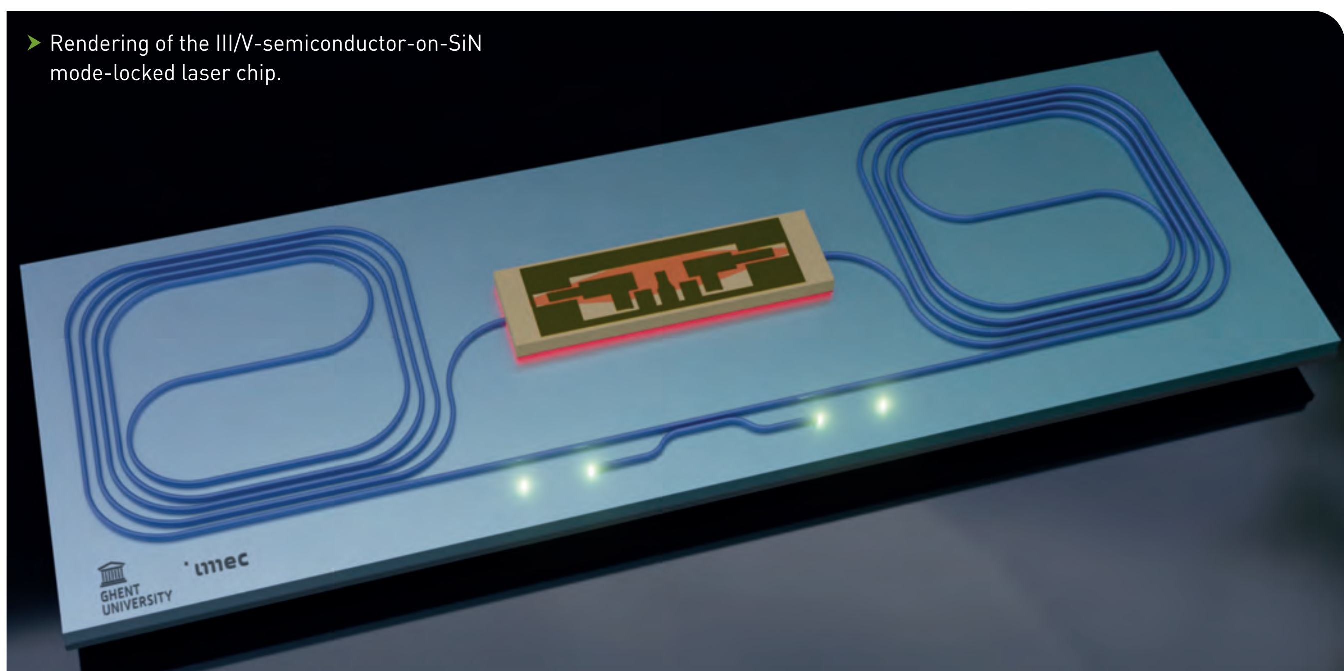

Rendering of the III/V-semiconductor-on-SiN mode-locked laser chip.

Mode-locked comb lasers for chip-scale spectroscopy

By integrating a semiconductor optical amplifier on a low-loss SiN photonic chip, an ultra-dense, low-noise laser comb is realized, delivering unprecedented precision for chip-scale spectroscopy

BY STIJN CUYVERS, BAHAWAL HAQ, GUNTHER ROELKENS, KASPER VAN GASSE AND BART KUYKEN FROM GHENT UNIVERSITY - IMEC

UNDERPINNING A REVOLUTION in precision frequency metrology and timekeeping is the optical frequency comb, an optical source that generates a large number of coherent equally spaced discrete laser lines. The impact of these combs has been widely recognized, most notably in 2005, when John Hall and Theodor Hänsch were awarded a Nobel prize in physics for their contributions to the development of laser-based precision spectroscopy, including the optical frequency comb technique.

Traditionally, comb spectra are generated using Ti:sapphire solid-state lasers and erbium- or ytterbium-doped fibre mode-locked lasers. As these laser sources are bulky, their use is restricted to experiments in a lab.

To unlock the full potential of comb spectra technologies, it is essential to develop a compact, mass-manufacturable device. In recent years, considerable effort has been directed towards this goal, with researchers focusing on the integration of optical comb generators on a photonic chip. Success on this front will extend the application range well beyond fundamental frequency metrology to areas such as laser ranging, telecommunications and on-chip spectroscopy.

There has been a great deal of interest in dual-comb spectroscopy, as it allows for a highly multiplexed interrogation of broadband absorption spectra using a single photodetector. This technique enables accurate characterization of rotational-vibrational transitions of numerous gases, liquids and solids. When using this spectroscopic tool, one comb is sent through the sample under study, while another, with a slightly different line spacing, acts as a 'local oscillator'. Interfering these two combs on a photodetector generates a frequency comb in the RF domain, composed of distinguishable beats between pairs of optical comb lines. With this approach, the sample's spectral information is hence readily available in the RF domain and accessible for electronic processing.

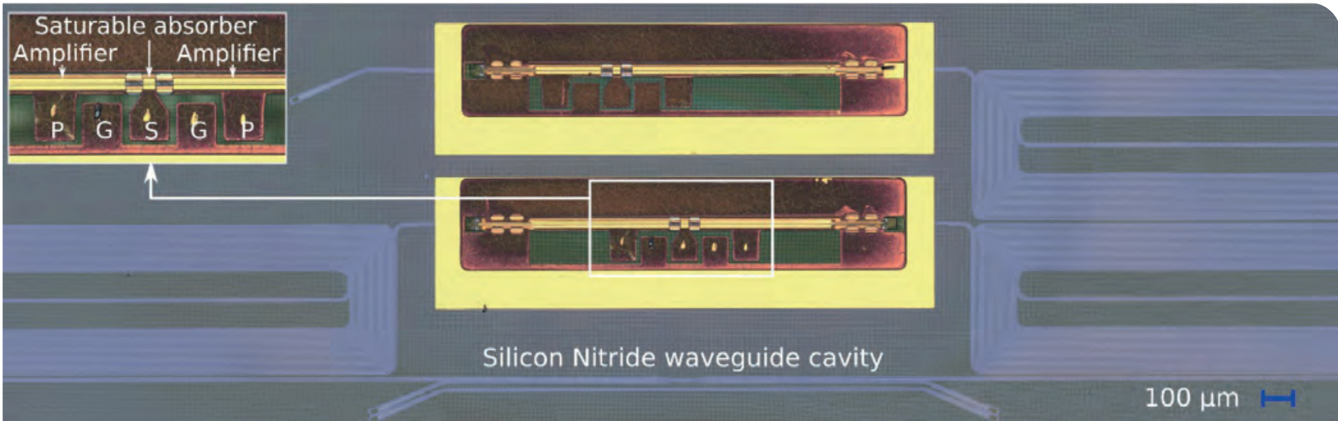

Figure 1. Microscope image of the III/V-semiconductor-on-SiN mode-locked laser chip, consisting of two 10 cm spirals and InP-based amplifiers and a saturable absorber.

One of the merits of this method is that as all spectral components are simultaneously measured. Systematic errors, such as temporal variations in the sample, are effectively equalized. Another strength is that the frequency combs can be calibrated with an atomic clock to provide unrivalled precision.

A key requirement for this spectroscopic technique is the ability to generate a dense low-noise optical comb on-chip. As the resolution of the spectral measurement is directly related to the spacing between adjacent comb lines, a denser comb enables identification of otherwise undetectable features in the sample's spectral response.

Efforts in developing the first chip-scale dual-comb spectrometers employed Kerr-effect combs, consisting of a high-quality optical ring resonator pumped with a continuous-wave laser. Due to the material's non-linearity, many new frequencies are generated in the resonator, leading to the creation of an optical comb with a line spacing determined by the size of the ring.

There have also been demonstrations involving quantum- and interband-cascade lasers, and so-called electro-optic frequency combs. The latter approach produces an optical comb by placing an electro-optic phase modulator in a resonator with a strong second-order nonlinearity, and pumping it with a continuous-wave laser. Modulation results in the growth of sidebands at the modulation frequency, which are subsequently modulated as well, resulting in a cascading effect.

Although these platforms have shown impressive results, their limited number of usable comb lines, integration challenges and their large comb line spacing (more than 10 GHz), inhibit their use in chip-scale high-resolution spectroscopic applications. In particular molecular spectroscopy in the gas-phase has proven challenging because gases typically have absorption features with linewidths on the order of 1 GHz. Optical combs with a narrow line spacing are crucial to accurately sample these spectra without the need for interleaving multiple spectra measured at different times.

Fortunately, there is a class of comb generators well-suited to the demands of on-chip gas-phase dual-comb spectroscopy. The breakthrough comes from translating the traditional optical frequency comb technique to a chip-scale device: the integrated mode-locked laser.

Mode-locked lasers on a photonic chip

Mode-locked lasers are a special class of lasers that generate ultra-short optical pulses by phase-locking a large number of longitudinal modes within a cavity. In accordance with the Fourier theorem, such a series of short optical pulses creates an optical comb in the frequency domain.

Engineers can fabricate these devices on a chip using the same manufacturing techniques employed for making continuous-wave laser diodes. The primary difference is the addition of a saturable absorber, which favours the formation of pulses over continuous-wave lasing. Saturable absorbers are typically realized by electrically isolating a part of the gain waveguide and reverse biasing it.

Numerous material platforms have been used to develop integrated mode-locked lasers. They range

Figure 2. Microscope image of the micro-transfer printed coupon on top of the two-stage taper coupling structure.

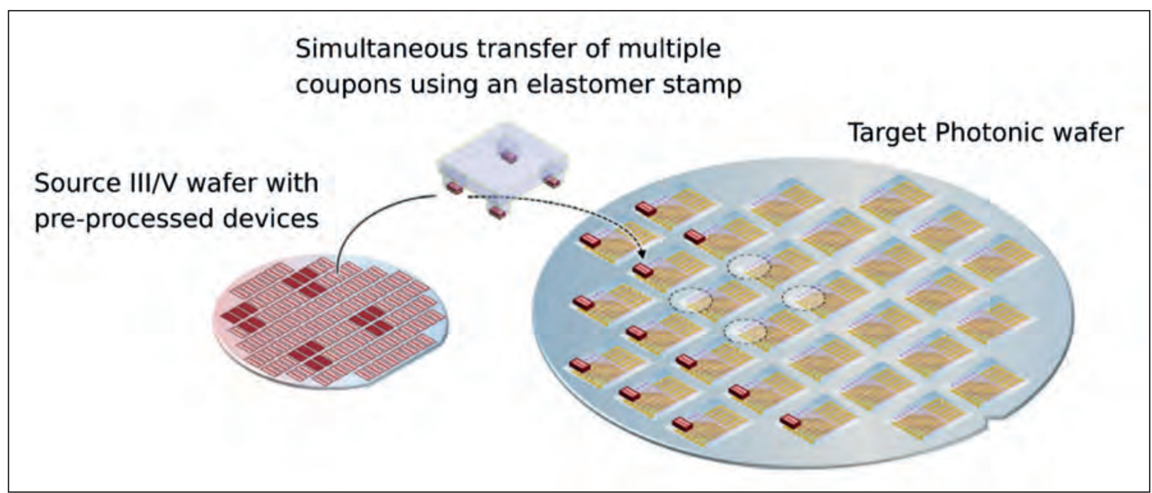

Figure 3. Concept of micro-transfer printing pre-processed III/V-semiconductor optical amplifiers on a target photonic integrated circuit using an elastomer stamp.

from InP/InGaAsP and InP/InAlGaAs quantum wells to InAs/InP, InAs/GaAs and InP/InAlGaAs quantum dots.

As the noise performance and comb line spacing are proportional to the cavity length, there is a large incentive to extend the laser cavity. This has driven the development of InP and III/V-on-silicon lasers with long passive waveguide cavities.

In 2017, a collaboration between researchers at Ghent University – imec and the University of Eindhoven realised a milestone in integrated mode-locked laser performance. Back then, they unveiled a III/V-semiconductor-on-silicon mode-locked laser with a repetition rate – that is, a comb line spacing – of just 1 GHz. Success came from transferring an InP/InGaAsP gain material, epitaxially grown on its native substrate, on top of a silicon-on-insulator (SOI) passive photonic circuit through a die-to-wafer bonding technique. Combining a long, low-loss silicon waveguide cavity with a high-quality quantum well gain waveguide enabled a narrow linewidth and a small comb line spacing.

SiN for ultra-low losses

A promising candidate for propelling performance to a new level is the use of a SiN platform for integrated laser sources. While typical silicon waveguides exhibit losses around 0.7 dB/cm, SiN waveguides can routinely realise losses that are far lower, close to 1 dB/m. Another advantage over their silicon cousins is that, thanks to the higher bandgap, they don't suffer from nonlinear two-photon and free-carrier absorption that fundamentally limit the attainable cavity size and lasing power.

Our team at the Photonics Research Group of Ghent University – imec has adopted this approach, developing the world's first on-chip mode-locked laser based on this novel III/V-semiconductor-on-SiN platform. By exploiting ultra-low losses of just 5 dB/m, we have realised the lowest noise reported for a chip-scale mode-locked laser to date and demonstrated a record comb line spacing of a mere 755 MHz, breaking the 1 GHz record.

Our laser has a ring cavity geometry, consisting of two 10 cm SiN spirals, deposited by means of low-pressure CVD on top of a patterned silicon-on-insulator wafer (see Figure 1 for a microscope image of this mode-locked laser). By defining the 330 nm-thick SiN waveguides using deep-UV lithography, we enabled low-cost, high-volume wafer-scale manufacturing.

To enable the heterogeneous integration of a III/V-semiconductor optical amplifier, we locally etch a trench in the 4.2 μm silicon oxide top cladding. This is accomplished with dry etching techniques, and results in a local exposure of the cavity waveguides. Furthermore, we employ a two-stage taper to efficiently couple the light from the SiN waveguide to the III/V gain waveguide. Light first couples from the SiN waveguide to a silicon waveguide underneath, and then into the III/V waveguide. This allows for an improved match in the refractive index and consequently an enhanced coupling efficiency (a microscope image of the coupling structure is shown in Figure 2).

Micro-transfer printing

We use micro-transfer printing for the heterogeneous integration of the III/V amplifier. This process relies on the kinetically controlled adhesion of an elastomeric stamp to pick devices from a source wafer and print them on a target wafer, in this case the SiN photonic integrated circuit (PIC). An overview of the integration process is shown in Figure 3.

An important advantage of micro-transfer printing is its ability to integrate the III/V amplifier in a deep recess, an attribute that is essential for compatibility with low-loss top-cladded passive photonic platforms. Additional strengths of micro-transfer printing technology, which leverages the advantages of flip-chip integration and wafer bonding techniques, are efficient use of expensive III/V material and massively parallel integration, because many devices can be picked up and printed simultaneously. It's also worth noting that III/V devices can be pre-processed on their native substrate prior to transfer printing, permitting

pretesting on the source wafer; and material stacks can be co-integrated on the same target wafer to implement diverse functionalities, offering unmatched versatility.

Fabrication of our devices begins by defining III/V semiconductor optical amplifiers, from here on denoted as 'coupons', on the native III/V InP-based substrate. The epilayer stack contains six InAlGaAs quantum wells and is grown on a 500 nm AlInAs release layer that can be selectively etched to release the active region from the substrate. After patterning the coupons, we deposit a photoresist encapsulation, before removing the AlInAs with a $FeCl_3$:H_2O solution. This leaves the coupons solely supported by the resist encapsulation and ready for micro-transfer printing.

To ensure a high printing yield, we deposit a 50 nm-thick adhesive divinylsiloxane-bis-benzocyclobutene (BCB) layer on the patterned SiN target sample. The source and target are then loaded into the micro-transfer printing tool and carefully aligned. An elastomer stamp picks up a coupon from the source wafer by laminating the stamp against the coupon and then rapidly moving upwards. During this movement, adhesion between the coupon and stamp increases, and encapsulation tethers break at predetermined locations. After this, the coupon-loaded stamp is pressed against the target sample, before it is slowly retracted to leave the coupon behind on the target.

Following the micro-transfer printing process, resist encapsulation is removed and the recess is planarized with BCB. The III/V amplifier is then post-processed, using a series of wet and dry etching steps to electrically isolate a saturable absorber, expose *n*-contacts and provide electrical contact pads for biasing.

Record comb density

To evaluate our device's performance, we have biased the amplifiers and saturable absorber with contact probes and collected the light output with a single-mode fibre. Capturing the optical output with a photodetector allows us to translate the comb spectrum to the RF domain (see Figure 5(a)). This indicates a comb line spacing of 755 MHz, which is, to the best of our knowledge, the lowest reported comb line spacing for an on-chip passively mode-locked

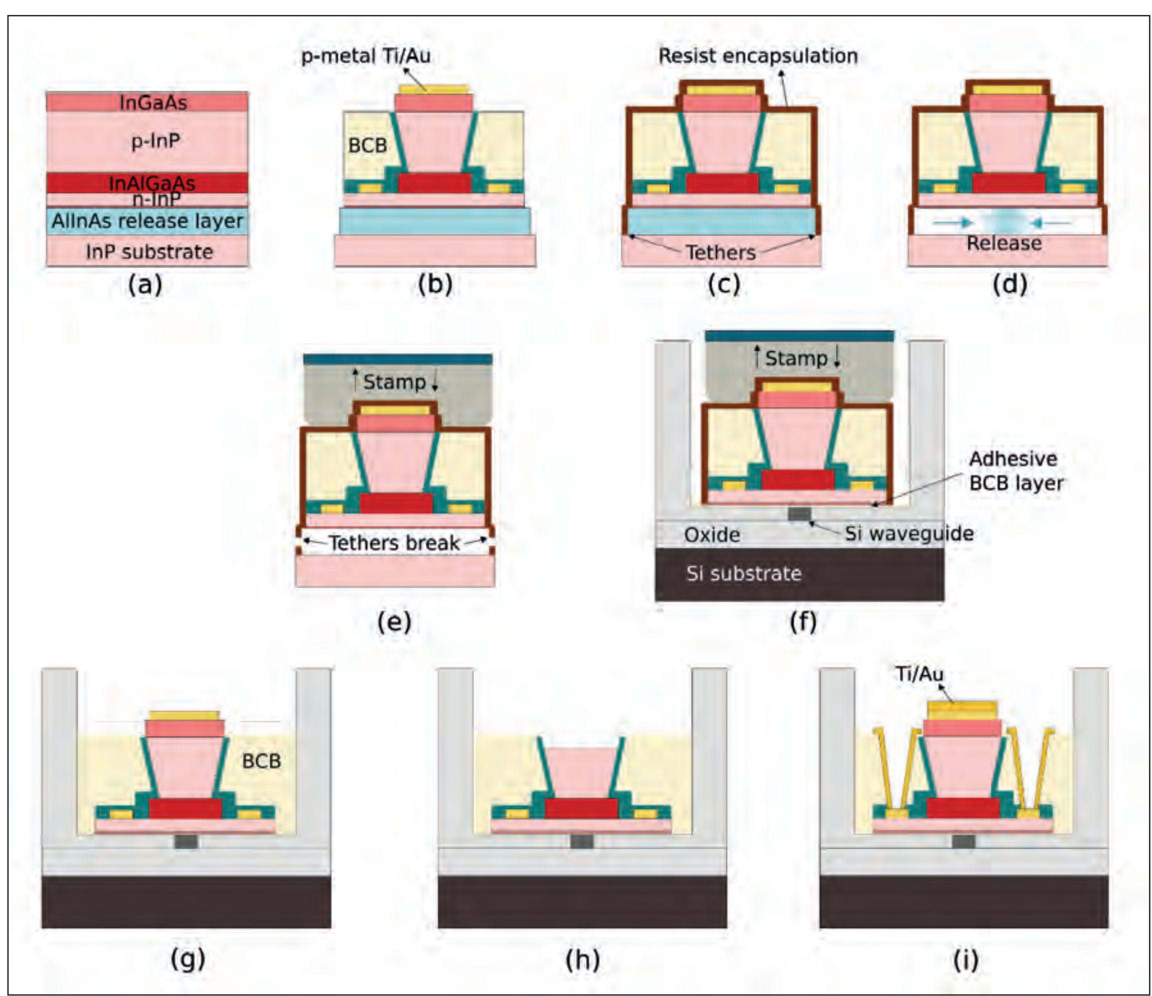

Figure 4. Fabrication process flow. (a)-(d) III/V-semiconductor optical amplifier fabrication, (e)-(f) micro-transfer printing process, (g)-(i) post-processing. (a) III/V-epilayer stack, (b) III/V coupon definition on the source substrate, (c) coupon encapsulation with photoresist, (d) release etch, (e) pick-up coupon from source, (f) print coupon on target in recess, (g) encapsulation removal and BCB planarization, (h) saturable absorber isolation, (i) final metallization.

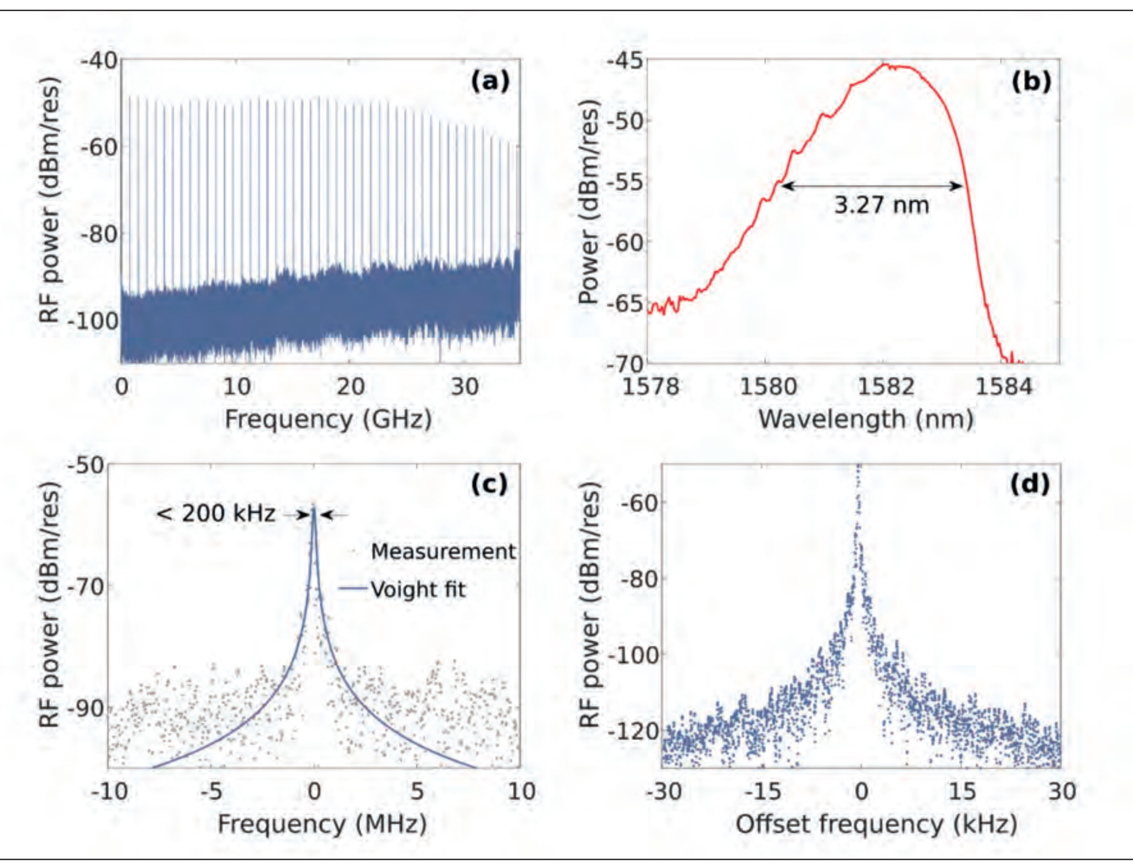

Figure 5. Experimental results. (a) RF spectrum of the generated pulse train with a comb line spacing of 755 MHz. (b) Optical spectrum with a 10-dB span of 3.27 nm, measured with a 30 pm resolution. (c) Optical linewidth, measured by heterodyning the mode-locked laser output with a tunable laser. (d) Repetition frequency signal at 755 MHz.

laser. Such a low spacing enables an unprecedented resolution for spectroscopic applications. Note that the comb roll-off at high frequencies is not related to the mode-locked laser, but rather a consequence of the 30 GHz bandwidth of the transimpedance amplifier of the photodetector. The optical comb spans over 3.27 nm (see Figure 5(b)), indicating that the laser generates over 500 densely and evenly spaced lines within a 10 dB bandwidth.

Characterisation of the noise properties has involved measuring the optical linewidth of the central lasing mode by heterodyning the output of the mode-locked laser with a tuneable continuous-wave laser on a photodetector (see Figure 5(c)). We fitted the heterodyne signal with a Voigt profile that has a full-width at half-maximum of just 146 kHz. To characterise the repetition frequency signal at 755 MHz, we measured the output of the mode-locked laser with a photodetector and an electrical spectrum analyser (see Figure 5 (d)). The narrow 300 Hz -10 dB RF linewidth indicates that all the optical modes are strongly phase-locked, and implies that the optical linewidth of the comb lines is similar to the linewidth of the central lasing mode. Single-sideband phase noise measurements reveal an amplified-spontaneous-emission-limited RF linewidth of 1 Hz, indicating that the RF linewidth is currently dominated by environmental and technical noise perturbations.

Our results showcase the potential of our on-chip mode-locked lasers for integrating high-resolution dual-comb spectrometers on a photonic chip. However, there are still a few challenges to overcome before commercial deployment follows. Firstly, it would be good to have an even larger number of usable comb lines, a goal that could be accomplished by further engineering of the laser cavity and spectral shaping of the gain. Secondly, there is a need to carefully package and stabilize these mode-locked lasers to minimize the impact of environmental perturbations. Another task is to explore other material platforms, such as GaSb, which could target spectral regions beyond 2 μm and enable us to uncover the full capabilities of on-chip spectroscopic sensing.

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FURTHER READING

- S. Cuyvers *et al*. European Conference on Optical Communications (2020)
- N. Picqué and T.W. Hänsch. Nature Photon **13** 146 (2019)
- K. Van Gasse *et al.* arXiv 2006.15113 (2020)
- K. Van Gasse *et al*. IEEE Photon. Technol. Lett. **31** 1870 (2019)
- Z. Wang *et al*. Light Sci. Appl. **6** e16260 (2017)
- B. Haq *et al*. Laser Photonics Rev. **14** 1900364 (2020)
- S. Cuyvers *et al*. Laser Photonics Rev. **15** 2000485 (2021)

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Lateral gallium oxide MESFETs power ahead

Record-breaking performance results from high-quality epitaxy and novel field plates

ENGINEERS in the US are claiming to have broken new ground for the all-round performance of lateral β-Ga_2O_3 MESFETs. Their devices are said to be the first to combine a high breakdown voltage with a high lateral figure-of-merit, which is aided by realising a low specific on-resistance.

Spokesman for the team, Fikadu Alema from Agnitron, believes that these MESFETs are promising contenders for providing highly efficient power switching at high voltages. This strength could drive deployment of this device in power supplies, power transmission, electric grid integration and electric vehicles.

Alema and co-workers, including a team led by Sriram Krishnamoorthy, who has recently moved from the University of Utah to UCSB, argue that the strong performance of their β-Ga_2O_3 MESFETs demonstrates that high-quality material can be produced with a conventional device process flow. Epilayers were grown by MOCVD at Agnitron Technology.

MESFETs have been produced with field plates electrically connected to the gate pad outside the mesa (not shown).

Devices based on β-Ga_2O_3 can employ vertical and lateral geometries. The team has pursued the latter, partly because it leads to: fewer processing steps; simplifies packaging and integration requirements; and allows the fabrication of devices with different dimensions on the same wafer, enabling the formation of a range of transistors that target different operating voltages and frequencies. In addition, lateral devices aid thermal management, thanks to the channel being closer to the surface, which enhances heat extraction.

REFERENCE

➤ A. Bhattacharyya *et al*. IEEE Electron. **42** 1272 Dev. Lett. (2021)

The team made their devices on 10 mm by 15 mm semi-insulating β-Ga_2O_3 substrates that are iron-doped, formed by edge-defined film-fed growth, and produced by Novel Crystal Technology. On this substrate, cleaned by HF, the engineers deposited a 230 nm-thick layer of β-Ga_2O_3 doped with silicon at a density of around 3.6×10^{17} cm^{-3}. According to Hall measurements, the charge in the channel and its mobility are 5.7×10^{12} cm^{-2} and 95 cm^2 V^{-1} s^{-1}, respectively.

To isolate the mesa and selectively grow source and drain ohmic contacts, the team turned to MOCVD regrowth, using a Ni/SiO_2 mask pattern. Dry etching with an inductively coupled plasma provided a contact recess etch, with this step removing about 10-20 nm of the β-Ga_2O_3 layer. For the regrown n^+ layer, silicon doping is around 2.6×10^{20} cm^{-3}. A combination of photolithographic pattering, lift-off, evaporation, and annealing formed ohmic source/drain contacts to the regrown layer. Electron-beam evaporation realized the Schottky gate.

Some MESFETs featured a gate-pad-connected field plate, formed by electrically connecting a gate field plate metal to the gate pad outside the device mesa. This architecture protects the channel region from dry-etching plasma damage, which occurs in the conventional gate field plate etch process flow.

The researchers have compared the performance of devices with and without a field plate. For MESFETs with a gate-to-source spacing of 1 μm, a gate length of 2.8 μm, and a gate-to-drain distance of 2.4 μm, on-resistance fell from 63.2 Ω mm to 55.8 Ω mm with the addition of the field plate. Transmission line measurements on structures produced with this approach to processing have a contact resistance of just 1.4 Ω mm, a figure ten times less than that associated with a previous generation of devices, thanks to the introduction of a low etch rate for dry etching of the contact recess.

Electrical measurement showed that adding a field plate cut on-resistance by 14 percent, increased on-current by 13 percent and boosted transconductance by 13 percent. For devices with 10 μm and 20 μm gate-to-drain lengths, breakdown voltages exceeded 2.4 kV and more than 3 kV. For the former device, the lateral figure of merit is 355 MΩ cm^{-2}.

Alema says that the goals for the future include increasing the breakdown voltage to beyond 10 kV, and developing devices for delivering high output currents while accommodating blocking voltages of more than 1 kV.

Diminishing droop with multi-junction LEDs

MOCVD-grown LEDs with multiple tunnel junctions push peak efficiency to higher drive currents

A COLLABORATION between researchers at The Ohio State University and Sandia National Labs is claiming to have produced the first triple-junction LEDs grown by MOCVD. According to the team, their work shows that with proper tunnel-junction design it is possible to increase wall-plug efficiency at high output powers by cascading several nitride-based LEDs.

This advance could improve the performance of high-power LEDs deployed in domestic, industrial and automotive lighting. While droop has been reduced in LEDs used for these applications, it is still an issue.

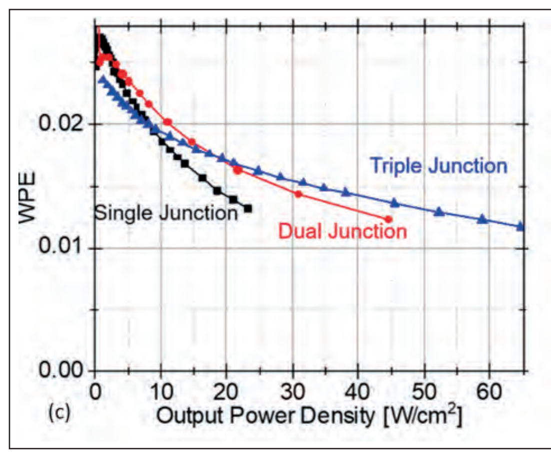
"We have been informed by those in the LED industry that fixing droop remains a significant challenge that they are actively pursuing, especially in longer wavelength LEDs," revealed team spokesman Zane Jamal-Eddine.

The recent success by the US collaboration is underpinned by a breakthrough in tunnel-junction design reported earlier this year. Simulations forming part of that previous work showed that the voltage penalty across MOCVD-grown tunnel-junction LEDs can be minimised by carefully controlling the doping profile. Optimising the magnesium profile in the heavily-doped *p*-type layer is particularly important. "Furthermore, it is key to utilize polarization charge to provide a favourable electric field profile to enhance the tunnelling probability," added Jamal-Eddine.

The team accomplished all these objectives by including a heavily doped, graded InGaN region with a peak composition of 6 percent indium in the tunnel-junction. The resulting three-dimensional polarization charge helps to compensate for doping issues associated with MOCVD grown tunnel-junctions, which tend to cause them to have a much higher forward voltage than equivalents grown by MBE.

Thanks to the introduction of the polarization charge, alongside optimisation of the doping profile, the forward voltage across the team's MOCVD-grown tunnel-junctions is similar to those grown by MBE. "This enabled the improvement in forward voltage, external quantum efficiency, and wall-plug efficiency scaling that we observed in our dual- and triple-junction cascaded LEDs," remarked Jamal-Eddine.

He and his co-workers produced their devices using a Taiyo Nippon Sanso SR4000HT reactor. Underpinning the device structure, formed on sapphire substrates, is: a 6 μm-thick layer of *n*-type GaN with a dislocation density of around 10^8 cm^{-2}; a 500 nm-thick *n*-type GaN layer doped with silicon to a level of 5 x 10^{18} cm^{-3}; and



The peak of wall-plug efficiency shifts to a higher current density with the addition of more tunnel junctions.

a 190 nm-thick $In_{0.04}Ga_{0.96}N$ underlayer, incorporated to prevent formation of V-type defects. On this platform the team produced LEDs with one, two and three junctions. Etching followed to create 100 μm by 100 μm mesas, before rapid thermal annealing activated the carriers in the buried *p*-type GaN layers.

Electrical measurements on devices with a ring-shaped top *n*-type contact showed that the turn-on voltage increased from 3.3 V for the single-junction device to 6.9 V and 10.8 V for double- and triple-junction variants. Electroluminescence measurements revealed that the peak of the external quantum efficiency scaled by 200 percent with the introduction a two-junction device, and 275 percent with a three-junction device (see Figure). These significant increases demonstrate that multi-active regions allow LEDs to offer a better performance at higher powers.

Moving to even more junctions promises to push peak efficiency to an even higher drive current, but there are concerns over degradation of underlying layers, associated with the thermal budget. Another issue in these structures is the propagation of extended defects, formed in the heavily-doped tunnel-junction layers. The team have hunted for these defects with a transmission electron microscope, but have found no evidence for them.

Jamal-Eddine says that the team are currently looking into possible thermal budget issues to see if they can push the device any further, or to a larger number of junctions.

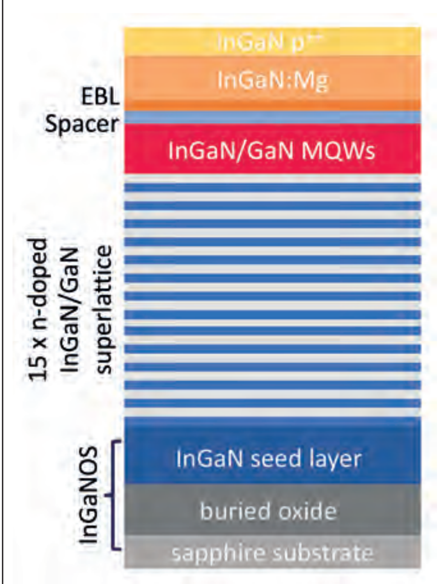
REFERENCE

➤ Z. Jamal-Eddine *et al*. Appl. Phys. Express **14** 092003 (2021)

Pseudo-substrates promise to produce better red microLEDs

By reducing strain with an InGaN layer on a buried oxide, red-emitting InGaN-based microLEDs are tipped to yield higher efficiencies

WHILE phosphide-based structures lead the way for making most red LEDs, their performance plummets as dimensions decrease. When shrunk below 10 μm, which is the size these microLEDs need to be for displays for virtual and augmented reality, losses are exacerbated by long carrier diffusion lengths and a high density of surface defects at sidewalls.



A 15 pair superlattice with n-type $In_{0.03}Ga_{0.97}N/GaN$ layers provided a foundation for the active region, containing five 2 nm-thick $In_{0.4}Ga_{0.6}N$ quantum wells, separated by 7.5 nm-thick $In_{0.03}Ga_{0.97}N$ barriers. The 15 nm-thick electron-blocking layer is made from $Al_{0.1}Ga_{0.9}N$.

Pioneering an alternative is a French partnership between the University of Grenoble-Alpes and Soitec. This team is developing red-emitting GaN-based LEDs that suffer from far less strain than equivalents grown on conventional substrates, thanks to deposition of epitaxial layers on an InGaN layer sitting on a buried oxide.

This foundation, formed using Soitec's proprietary Smart Cut process, enables thin InGaN quantum wells to span the entire visible spectrum, thanks to enhanced indium incorporation that results from an increase in the in-plane lattice parameter.

Another benefit of the InGaN platform is that it trims the internal electric field in the device's active region, opening the door to higher efficiencies.

Last year the French team reported the results of red-emitting microLEDs, made on InGaN Smart Cut substrates, that had device dimensions ranging from 300 μm by 300 μm to 50 μm by 50 μm. The latest results, realised with an improved process, are for devices with dimensions down to 10 μm.

Two variants have been used for this latest work: one substrate has a 120 nm-thick InGaN seed layer with an indium content of 8 percent; and the other, identical in thickness, has an 11 percent indium content. Both feature a step meandering substrate morphology and V-shaped defects with a density and size rising with indium content. Upping the indium content increases the density and size of the V-pits from 3 x 10^7 cm^{-2} and 100 nm to 2 x 10^8 cm^{-2} and 130 nm.

Device fabrication began by loading substrates into an MOCVD reactor and depositing an epitaxial stack that included a 15 period superlattice, a multi-quantum-well active region and an electron-blocking layer (see Figure for more details). Scrutinising this heterostructure with a high-resolution transmission electron microscope revealed additional dislocations in the active region and electron-blocking layer, attributed to local strain relaxation.

The team employed conventional LED chip fabrication processes to fabricate LEDs with mesa sizes ranging from 300 μm by 300 μm to 10 μm by 10 μm. The previous portfolio of devices were held back by V-shaped defects – when they go through the entire structure, they create an electrical path from anode to cathode. To eradicate this issue, the fabrication process for the latest generation of emitters includes the addition of a conformal layer, planarized with chemical mechanical polishing.

Photoluminescence measurements revealed that the increase in the indium content of the substrate shifted the microLED emission peak from 635 nm to 653 nm. The longer wavelength resulted from a higher a lattice parameter.

For a device with 10 μm-diameter, the maximum external quantum efficiency is 0.14 percent, realised at 8 A cm^{-2}. This value, inferior to that of 0.2 percent by a team from UCSB, is held back by a lower light extraction efficiency. For the device produced by the French team, light is collected from the backside, while the *p*-contact pad does not cover all of the top of the structure, and no metal prevents light from escaping the sidewalls. Extraction is also hampered by emission that goes through the backside of the device having to traverse the superlattice, buried oxide and sapphire substrate. The actual value for light extraction efficiency is difficult to estimate, but based on simulations, it is below 4 percent.

To improve performance, effort must be directed at increasing the extraction efficiency, trimming the operating voltage, and improving the crystalline quality of the LED.

REFERENCE

➤ A. Dussaigne *et al*. Appl. Phys. Express **14** 092011 (2021)

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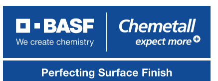

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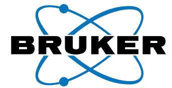

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