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INSIDE

News, Analysis, Features, Editorial View, Research Review and much more

QUASHING DROOP

Cubic GaN combats LED droop through elimination of internal electric fields and a reduction in effective hole mass

STRETCHING POWER DEVICES

GaN power rectifiers and transistors combine a breakdown voltage beyond 10 kV with a low on-resistance

GOING TO THE CUBIC PHASE

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VIEWPOINT

By Dr Richard Stevenson, Editor

Cubic champions

What do you do if efforts to improve your device through changes to its architecture fail to deliver the gains you need?

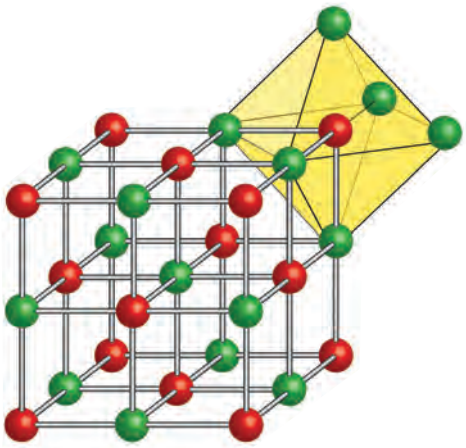
Given the opportunities that exist within the portfolio of compound semiconductors, one obvious choice is to see if replacing one material with another pay dividends. That's a pathway many pursue.

But there may be an even better solution, far closer to home. Rather than switching materials, how about sticking with them, but altering their atomic arrangement?

Within this issue we hear from two research teams that are adopting exactly that approach. Both are investigating what's possible when shunning an incumbent hexagonal form of the material in favour of a cubic alternative. In one case it's 3C-SiC, offering advantages for various electronic devices; and in the other it's cubic GaN, arguably a better bet for green LEDs.

Efforts at developing the 3C form of SiC are underway at Francesco La Via's group from the Institute of Microelectronics and Microsystems. Aided by collaboration in EU-funded projects, this team is trying to exploit the strengths of this polytype. Merits include the highest electron mobility and saturation velocity for any form of SiC and a great mechanical strength (see p.36).

MOSFETs that are made with the 3C form of SiC sport a channel mobility that's ten times higher than the 4H sibling. This asset, allied to a bandgap of just 2.3 eV, promise a lower on-state resistance and thus lower conduction loss.



Another alluring attribute of 3C-SiC is that it can be grown on silicon. Success is not easy, with differences in lattice parameters giving rise to various imperfections, such as micro-twins, anti-phase boundaries and stacking faults.But progress is being made, using silicon as the foundation for SiC seeds that underpin bulk growth of 3C-SiC. This has enabled the fabrication of 3C power devices delivering promising results.

Partnerships have also enabled the fabrication of 3C MEMS, exploiting the excellent mechanical characteristics of this material. They include a strain meter with such a high degree of sensitivity that it can detect the small deformations occurring in the hours leading up to earthquakes and volcanic eruptions.

For LEDs, switching from a hexagonal form of GaN to a cubic variant eliminates internal electric fields and reduces the effective mass of holes. Can Bayram's team at the University of Illinois at Urbana-Champaign have been considering these benefits from both a theoretical and an experimental standpoint (p.48). Simulations show that cubic GaN is great at combatting droop, while growth on nano-patterned silicon indicates that it may be possible to realise this polytype in a low-cost manner.

Although development of the cubic form of the two most common wide bandgap materials, GaN and SiC, is still in its infancy, there's certainly a lot to look forward to.

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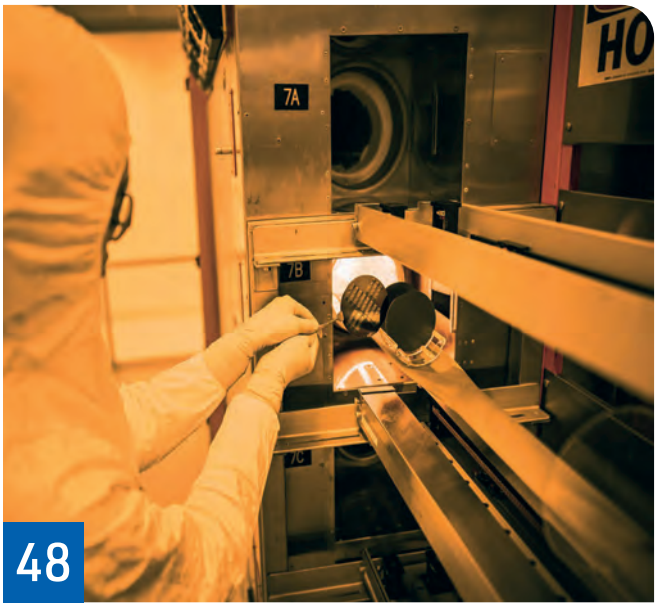

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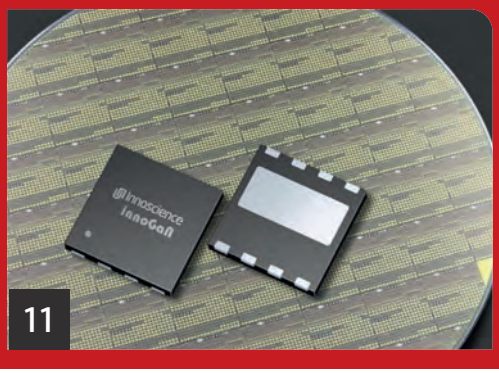

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Wolfspeed to build SiC materials manufacturing facility

Company expands partnership with NC A&T to foster next generation of SiC experts

WOLFSPEED is to build a new, state-of-the-art, multi-billion-dollar materials manufacturing facility in Chatham County, North Carolina. The investment is targeted to generate a more than ten fold increase from Wolfspeed's current SiC production capacity on its Durham campus, supporting the company's long-term growth strategy, accelerating the adoption of SiC across a wide array of end-markets and unlocking a new era of energy efficiency.

"Wolfspeed is the industry leader in supplying the materials required to meet the accelerating demand for next generation semiconductors and creating a more sustainable future for all," said Gregg Lowe, president and CEO of Wolfspeed.

Lowe added: "Demand for our products continues to grow at a rapid pace, and the industry continues to be supply constrained. Expanding our materials production will further our market leadership and allow us to better serve the growing needs of our customers,"We are particularly excited and proud to not only expand Wolfspeed's footprint in our home state of North Carolina, but also further our relationship with North Carolina Agricultural and Technical State University to nurture our best-in-class talent pool."

The facility will primarily produce 200 mm SiC wafers used to supply Wolfspeed's Mohawk Valley Fab, which opened earlier this year as the world's first, largest and only fully automated 200 mm SiC fabrication facility.

Phase one construction is anticipated to be completed in 2024 and cost approximately $1.3 billion. Between 2024 and the end of the decade, the company will add additional capacity as needed, eventually occupying

more than one million square feet on the 445-acre site. State and local funding, including a Job Development Investment Grant from the North Carolina Department of Commerce, will support the development of the facility's first phase and represents an approximately $1.0 billion incentive package from the State, County and local governments.

In addition, Wolfspeed hopes to apply for and obtain federal funding from the CHIPS and Science Act to accelerate the construction and build-out of the facility. Over the next eight years, the company intends to continue to invest, looking to create roughly 1,800 jobs.

"Wolfspeed's decision further validates North Carolina as the epicenter of clean energy," said North Carolina Governor Roy Cooper. "This is another milestone in our drive toward a clean energy economy, as it will boost electric vehicle manufacturing and offshore wind while fighting climate change and putting money in the pockets of every day North Carolinians with great paying jobs."

The company's talent development strategy is complemented by its continued partnership with North Carolina Agricultural and Technical State University (NC A&T). In 2020, Wolfspeed committed $4 million over five years to the historically black colleges and universities – at the time, the single largest donation in the university's history, to create the Wolfspeed Endowed Scholars Program. The two entities aim to establish comprehensive education and training curricula and cutting-edge research and innovation programs.

This partnership will open opportunities for undergraduate and graduate credentials in SiC semiconductor manufacturing, as well as training and career advancement programs for existing semiconductor manufacturing workers.

"North Carolina A&T is proud to partner with Wolfspeed to provide new opportunities to pursue the next generation of careers in the green economy, drive innovation and explore new possibilities," said N.C. A&T Chancellor Harold L. Martin, Sr. "Throughout our rich history as a doctoral, land-grant university and the largest historically Black university in the country, we have believed in the power of our students to change the world. Our expanded partnership with Wolfspeed will allow us to change the world together, and I am incredibly excited for what is to come."

Trumpf VCSELs to fly to space in quantum sensors

First satellite controlled by quantum technology is scheduled to be launched into space in 2027

Trumpf Photonic Components has developed a high-power, single-mode VCSEL to be implemented in an altitude gyroscope sensor suitable for use in space. In a few years, the satellite with the quantum-based gyroscope should fly into space to generate highly precise attitude determination.

The development is part of a €28 million subsidy project called QYRO, strongly supported by the Federal Ministry of Education and Research in Germany. There are a number of partners in the project including quantum technology start-up Q.ANT, Bosch, Trumpf and the German Aerospace Center (DLR). The aim is to use quantum technology-based sensors to achieve high-precision altitude control of miniaturised satellites. The sensors enable the satellites to be aligned with each other and thus enable a high-speed connection for data communication.

The newly developed single-mode VCSEL is a 795 nm device with 10 mW of output power. This is ten times higher than the laser power this technology was able to offer in the past, according to Trumpf. The company says the VCSEL technology delivers the required stability over a wide range of temperatures and offers a robustness demanded by this space application. The breakthrough in compactness and cost enabled by the VCSEL technology will also open up more applications in mass markets. Highly precise gyroscopes can be used in industry, logistics or even in autonomously driving cars, says Trumpf.

"It's great to be part of the subsidy project, and to combine various fields of expertise, push for innovations and strengthen Germany as photonics hub", says Berthold Schmidt, CEO at Trumpf Photonic Components. "We can't wait to see our VCSEL integrated into a mini satellite, to support worldwide high-quality data communication and to improve the availability of internet connections, especially in remote regions", Schmidt adds.

Trumpf Photonic Components is working closely with the Ferdinand Braun Institute, Leibniz Institute for High Frequency Technology, one of the world's most renowned research

institutes for laser diodes. Together with this institute, Trumpf is jointly developing the robust VCSELs with high spectral purity that also meet the demands of quantum technology and space.

Another Trumpf subsidiary based in Berlin will integrate the VCSEL component into a robust, miniaturised TO package with additional optics and temperature stabilisation. Trumpf brings to the table its innovative assembly and automation technology know-how. Overall, there are five project partners, each bringing their own specialisation. The first satellite controlled by quantum technology is scheduled to be launched into space in 2027.

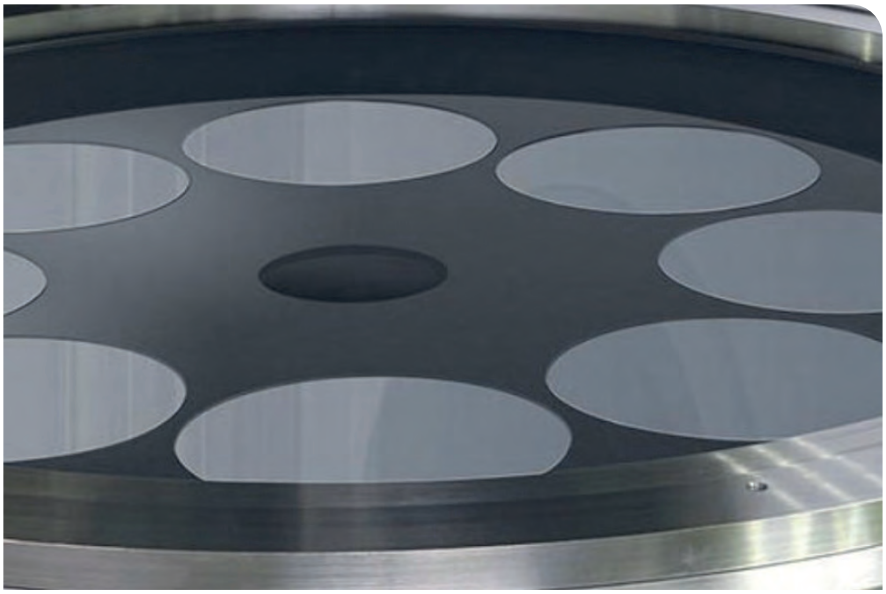
Aixtron launches next gen SiC epitaxy system

G10-SiC 200 mm system targets volume manufacturing of latest generation SiC power devices

AIXTRON SE has launched its new G10-SiC 200 mm system for high volume manufacturing of the latest generation SiC power devices on 150/200 mm SiC wafers.

This high temperature CVD system was announced at the International Conference on SiC and Related Materials (ICSCRM), which took place in Davos, Switzerland.

The new G10-SiC system is built on the established G5 WW C 150 mm platform and provides a flexible dual wafer size configuration of 9 x 150 mm and 6 x 200 mm. This feature is instrumental for the transition of the SiC industry from 150 mm to 200 mm wafer diameter.



The new platform is built around Aixtron's automated wafer cassette-to-cassette loading solution with high temperature wafer transfer. Combined with high growth rate process capabilities, the G10-SiC is said to provide best-in class wafer throughput and throughput per square meter to efficiently use the limited cleanroom space available in semiconductor fabs.

The Aixtron G10-SiC supports a large variety of device structures including single and double drift layer structures meeting stringent 150 mm uniformity requirements of sigma values less than 2 percent for doping and thickness. The automated wafer loading reduces the risk of particle defects to a minimum, "resulting in typical defect counts of less than 0.02/cm^2.

"This is a truly new generation high-performance system. The new dual wafer size configuration fully supports the transition from today's 150 mm wafer technology and safeguards the investments of our customer for the future. With the highest throughput available to date in this form factor, it maximises fabs productivity and capability to ramp even faster", says Frank Wischmeyer, VP SiC of Aixtron.

"At the same time, the newly developed *in-situ* top side wafer temperature control solution optimises the wafer-level process control within a batch as well as from batch-to-batch. This results in predictable high yields meeting tight production specifications at competitive cost levels", adds Wischmeyer.

The high throughput of the system paired with low consumption costs per processed wafers results in the lowest cost per wafer in the industry, according to the company.

"We are proud to deliver yet another solution to our partners around the globe, that combines industrial top-standard and immense climate effects. The positive feedback from our partners and customers after evaluation and production qualification of our new G10-SiC system has already generated additional customer interest", says Felix Grawert CEO & president of Aixtron SE.

"The G10-SiC is becoming an important building block for our customers' worldwide production expansion, and we are committed to support this scaling with our system manufacturing, service and process support excellence," added Grawert.

"This is a truly new generation high-performance system. The new dual wafer size configuration fully supports the transition from today's 150 mm wafer technology and safeguards the investments of our customer for the future."

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Ancora Semiconductor raises $14.6 million

Delta Electronics affiliate focusing on GaN announces first capital raising round

ANCORA SEMICONDUCTOR, a fabless Delta Electronics affiliate focusing on GaN technology, has announced the investments of its first capital, raising around $14.6 million. The strategic investors are Rohm, Sino-American Silicon, uPI Semiconductors, and Delta Electronics. The capital is expected to accelerate Ancora's GaN development endeavours.

"GaN is the future of power electronics with benefits of faster switching frequencies, higher efficiency, and lower energy consumption. The ecosystem of GaN technology is evolving rapidly as applications are continuously emerging. We are thrilled to have Rohm, SAS and uPI as our strategic partners and investors. We are also grateful for the commitment by our parent company Delta, a leader in power and thermal management technologies and a global provider of smart energy-saving solutions," said T.K. Shing, president of Ancora Semiconductors.

He added: "This powerful alliance will enable us to establish an ecosystem with strong partners in substrate materials, IC design, applications and system solutions, to expedite the adoption of GaN technology that promises unprecedented performance value".

Ancora semiconductor was cultivated under Delta Electonics and formally founded in 2022 as fabless design company focusing in GaN devices and its integration. The Ancora product line includes GaN discrete components, System in Package and System on Chip with quality, reliability and durability proven under Delta's stringent qualification system.

Delta says that its commitment to provide a wide range of smart energy-saving solutions in high-efficiency power electronics will provide additional momentum and fuel Ancora's long-term growth.

This alliance and capital raising is expected to enable Ancora to increase production capability to serve the growing demand for GaN devices in consumer electronics, telecom, and automotive applications. The ultimate goal is to maximise GaN performance to accelerate power technology innovation and contribute to sustainable development based on energy efficiency.

BluGlass joins UCSB GaN consortium

Australian semiconductor developer BluGlass Limited has joined the University of California, Santa Barbara's Solid-State Lighting & Energy Electronics Centre (SSLEEC) consortium; recognising the company's innovation in remote-plasma CVD epitaxy growth, novel laser architectures, and longer-wavelength GaN devices.

The SSLEEC is an invitation-only collaboration between industry leaders and the University of California, Santa Barbara's GaN researchers, including blue-LED inventor and Nobel Laureate, Shuji Nakamura, and industry Professor Steven DenBaars.

The consortium focuses on the development of new semiconductor technologies for energy-efficient lighting, disinfection, advanced mobile displays, augmented and virtual reality, communication, and power electronics.

Jim Haden, BluGlass president, said, "We are delighted to be invited to join the world's GaN industry and academic consortium, which is a testament to the cutting-edge development being conducted at BluGlass. Our membership enables us to leverage the expertise of industry pioneers Shuji Nakamura and Steven DenBaars; and to fast-track our advanced product roadmaps.."

Innoscience bi-directional GaN HEMTs used inside smartphones

Oppo announces world's first cell phones with inbuilt GaN charging protection

CHINESE GaN-on-silicon company Innoscience Technology has announced the Bi-GaN series of bi-directional GaN HEMT devices that save space and facilitate fast charging without suffering from the rises in temperature that can sometimes be seen in traditional silicon devices.

Innoscience has also revealed that mobile communications company, Oppo, is using the new BiGaN devices inside its phone handset to control the battery's charging and discharging currents. This is the first time that such protection, based on GaN technology, has been included in the phone itself – previously the circuitry had to be incorporated inside the charger.

The company says that one BiGaN HEMT can be used to replace back-to-back connected NMOS MOSFETs in a common-source configuration to achieve bi-directional switching of the battery's charging and discharging currents. This reduces on-state resistance by 50 percent, chip size by 70 percent, and temperature rise by 40 percent.
The first BiGaN device generally released by Innoscience is the INN040W0488, a 40V bi-directional GaN-on-silicon HEMT in the WLCSP package measuring 2.1 mm x 2.1 mm. The chip has on-state resistance as low as 4.8mΩ. BiGaN targets applications such as overvoltage protection circuits for smartphone charging, high-side load switching circuits, and switching circuits for multi-power systems. Innoscience is also working to extend the bidirectional family to lower on-state resistance as well as to higher voltages.

Oppo is using Innoscience's BiGaN HEMTs inside handsets, making it the world's first cell phone manufacturer using BiGaN as direct charging load switcher.

BiGaN products, said Oppo, not only save valuable space inside the phone but also reduce the temperature rise of the phone during charging.

This maintains a more comfortable temperature during fast charging, extends the possible duration of fast charging, and provides a better user experience. Oppo also announced that the BiGaN bi-directional technology will also be adopted in future volume production cell phone models.

Navitas acquires GeneSiC Semiconductor

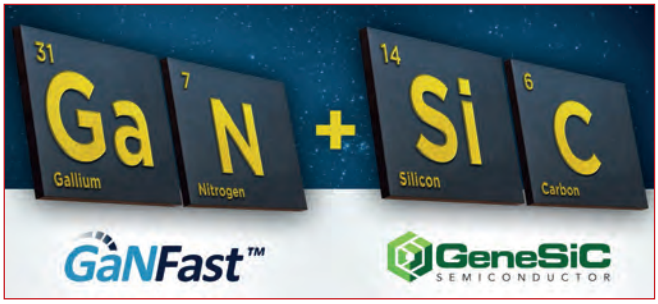
Positions Navitas as a pure-play GaN and SiC next-generation power semiconductor company

GaN COMPANY Navitas Semiconductor has announced the acquisition of GeneSiC Semiconductor, a SiC pioneer with deep expertise in SiC power device design and process.

"GeneSiC is an ideal partner for Navitas with its focus and success in developing industry-leading SiC technology," said Gene Sheridan, Navitas CEO and co-founder.

"Navitas has significant investments in global sales, operations and technical support teams, along with system design centres in EV and data centres. These capabilities are a perfect complement to GeneSiC and will further accelerate its growth in both synergistic and new customers and markets."

GeneSiC president Ranbir Singh added: "GeneSiC's patent-protected, advanced technology and innovative, experienced team are critical factors in the growth of our company. Our SiC MOSFETs offer the industry's highest performance, reliability, and ruggedness – parameters critical towards widespread adoption of electric vehicles and associated infrastructure," said "With almost 20 years of leading-edge R&D, proven platforms, over 500 diverse customers, and growing revenue and profitability, we can leverage Navitas' mass-production expertise and go-to-market strategy to accelerate SiC revenues."



Singh founded GeneSiC in 2004. Prior to that he conducted research on SiC power devices, first at Cree and then at the NIST, Gaithersburg, MD. He joins Navitas as executive VP for the GeneSiC business and Navitas expects to retain all members of the GeneSiC team.

GaN and SiC technologies address a broad range of applications from 20 W smartphone chargers to 20 kW EV chargers to 20 MW grid-infrastructure systems and everything in between. With over 500 customers, the GeneSiC acquisition adds new markets and customers, and accelerates Navitas' revenue in higher-power applications.

Navitas GaN ICs are optimised for 400 V EV systems, and GeneSiC technology is ideal for 800 V EV systems, with existing revenue and development customers including BYD, Land Rover, Mercedes AMG, Geely, Shinry, LG Magna, Saab, and Inovance.

Navitas GaN ICs serve residential solar, while GeneSiC has immediate revenue in higher power, commercial solar and energy storage customers, including APS, Advanced Energy, Chint, Sungrow, Growatt, CATL, Exide and many others.

GeneSiC high-voltage products bring immediate revenue in a wide range of additional industrial markets, including rail, UPS, wind, grid power, industrial motors, and medical imaging.

The acquisition should immediately add to Navitas' earnings per share. Total consideration consisted of approximately $100 million in cash, 24.9 million shares of Navitas stock and possible earn-out payments of up to $25 million, conditioned on the achievement of substantial revenue targets for the GeneSiC business over the four fiscal quarters ending September 30, 2023.

EPC opens Motor Drive centre in Italy

EPC has opened a new design application centre near Turin, Italy, to focus on growing motor drive applications based on GaN technology in the e-mobility, robotics, drones, and industrial automation markets. The specialist team will support customers in accelerating their design cycles and define future ICs for power management with state-of-the art equipment to test applications from 400 W to 10's of kW.

Strategically located, Turin has a historical tradition in electric motors and motor drives, enabling the company to draw on the wealth of local technical talent. EPC's engineers are helping customers reduce their design cycle times and adopt GaN for more efficient, smaller, lower-cost systems. Moreover, the centre is exploring ways to exploit the potential of EPC's GaN technology in motor drive applications to enable a substantial increase in the efficiency of the motor, leading to higher power density designs than what has been possible with historically MOSFET-based designs.

Turin also features the Power Electronics Innovation Centre, a cross-department entity in the Politecnico di Torino – one of the most important technical Universities in Europe – and EPC is collaborating closely with PEIC by investing in shared research and development.

The new facility is headed by Marco Palma, EPC's director of Motor Systems and Applications, who remarked: "Our new facility combines a comprehensive GaN product portfolio and design expertise offering customers a centre of excellence that is unrivalled for motor drive applications."

Onsemi celebrates expansion of US SiC facility

Hudson, New Hampshire facility will increase its SiC capacity by five times year-over-year

ONSEMI celebrated the inauguration of its SiC facility in Hudson, New Hampshire, with a ribbon cutting ceremony. The ceremony came days after President Biden signed the CHIPS and Science Act into law. The Act will strengthen US supply chain resiliency and help avoid disruptions for critical components.

Signifying the importance of this event and manufacturing of semiconductors in the US were the attendance of multiple guests of honour led by US Secretary of Commerce Gina Raimondo. Also present were US Senators Jeanne Shaheen and Maggie Hassan from New Hampshire, Representative Chris Pappas from the 1st congressional district of New Hampshire and Representative Annie Kuster from the 2nd congressional district of New Hampshire as well as other local governmental dignitaries.

The site will increase the company's SiC boule production capacity by five times year-over-year and almost quadruple the number of its employees in Hudson by the end of 2022. The expansion gives Onsemi full control of its SiC manufacturing supply chain, starting with the sourcing of SiC powder and graphite raw material to the delivery of fully packaged SiC devices.

Onsemi says this will allow it to provide customers with the assurance of supply required to meet rapidly growing demand for SiC-based solutions in applications such as electric vehicles (EVs), EV charging, and energy infrastructure. The SiC total addressable market is projected to grow from $2 billion in 2021 to $6.5 billion in 2026, at a compound annual growth rate of 33 percent.

"Our end-to-end vertically integrated solution in a supply-constrained environment is a compelling and differentiated competitive advantage," said Simon Keeton, executive vice president and general manager Power Solutions Group at Onsemi. "We have already expanded to a second building as we increased our substrate capacity and plan to continue ramping, allowing us to source our own cutting-edge SiC wafers for customer products."

Onsemi says it is the only large-scale supplier of both SiC and IGBT solutions with end-to-end supply capability. During its second quarter earnings call last week, the company announced $4 billion of committed SiC revenue for the next three years through long-term supply agreements with a broad base of customers. It will triple last year's SiC revenue in 2022 and exceed $1 billion in revenue in 2023.

II-VI closes $100 million SiC substrates contract

II-VI HAS CLOSED an over $100 million contract to supply Dongguan Tianyu Semiconductor Technology with SiC substrates to be delivered at the beginning of this quarter. Tianyu, one of China's first and largest SiC epitaxial wafer manufacturers, has signed a long-term supply contract, with upfront payments, to secure 150 mm SiC substrate capacity that will meet its demand through calendar year 2023.

"In November 2021, we were pleased to announce that Tianyu had selected II-VI as its primary strategic partner for the supply of 150 mm SiC substrates for power electronics," said Sohail Khan, executive VP, New Ventures & Wide-Bandgap Electronics Technologies Business Unit. "With the end-demand ramping up significantly, it became essential for Tianyu to secure its supply with this long-term, high-volume contract, which will be recurring and grow in value over time."

To meet market demand in Asia, II-VI established in 2021 a backend processing line for SiC substrates, in over 50,000 sq. ft. of new cleanroom space, at II-VI's Asia Regional Headquarters in Fuzhou, China. Tianyu will benefit from II-VI's 150 mm SiC global production capacity in both the US and China.

Tianyu and II-VI aim to provide a high-quality and reliable supply chain and future 200 mm capability that will be critical to support the rapidly growing demand for SiC power electronics in electric vehicles, renewable energy, smart grids, microgrids, and power supplies for data networks.

A GaN device for all markets

GaN power device maker, Navitas, believes its latest half-bridge power IC will deliver the high powers and efficiencies that mobile phone chargers, electric vehicles, photovoltaics and data centres need, reports REBECCA POOL

IN EARLY September this year, California-based GaN power device manufacturer, Navitas, released 'GaNSense', a half-bridge power IC that the company reckons provides a 'new level' of megahertz switching frequencies whilst slashing system cost and complexity compared with discrete half-bridge GaN ICs.

As Llew Vaughan-Edmunds, senior director of marketing at Navitas, points out: "The difference between Navitas and other gallium nitride companies is that we integrate the gate driver monolithically with the gallium nitride power and integrate real-time sensing and autonomous protection – that's the secret of our success and why we're number one in this field."

Following industry's relentless demand for more power and higher switching frequencies, Vaughan-Edmunds is certain that GaN ICs are going to be instrumental to the power devices of the future. Looking at mobile device chargers, right now Apple and Samsung wireless fast charge power adapters are currently rated to around 45W, but this is quickly changing. "These chargers are going to 65 W and 100 W now, and ultra-fast chargers have just been released at 200 W so you can charge your phone within 10 minutes," says Vaughan-Edmunds.

At the same time, data centres are striving for higher efficiencies to reduce electrical and cooling costs, as are electric vehicles to reduce battery recharge times. "[Industry] needs half-bridge topologies to meet these higher power, higher switching frequency and higher efficiency market demands, and this is why we've released our half-bridge IC now," he adds.

Navitas' half-bridge power IC integrates two GaN FETs with drive, control, sensing, autonomous protection and level-shift isolation in a single package. GaN is notorious for its sensitive gate structure, so from word go, Navitas has set out to deliver GaN power ICs with robust GaN gate protection. Given this, autonomous protection is a key feature of the latest chips. As Vaughan-Edmunds points out, gate driver and sensing protection is now imperative given the noise generated at higher frequencies and powers. At the same time, temperature protection and over-current protection

will autonomously shut down the chip to prevent device and system failure.

The Navitas director also points out how this set-up requires 61 percent fewer components and has a 64 percent smaller footprint than a typical discrete GaN half-bridge IC. "By eliminating all the [associated] circuitry, we're reducing circuit parasitics – this does give us nice, clean switching," he adds. "We are the first company to release a half-bridge power IC with this level of integration and rich feature set."

Market-driven

Importantly, these latest half-bridge power ICs are already in mass production in Europe. "Strategically, we wanted to be first to market in key growth segments," says Vaughan-Edmunds. This sentiment is clearly in line with past product launches.

Navitas power ICs have been in production since 2018, and just last year industry analyst TrendForce indicated that this west-coast chipmaker held the greatest market share amongst GaN power device suppliers.

According to Navitas, its technology is now in well over 150 different charging products from different companies – key partnerships include Lenovo, Xiaomi, Dell, Oppo, LG and Amazon. And, in a recent *Compound Semiconductor* interview, Navitas vice president Stephen Oliver estimated that the company was working with more than 90 percent of OEMs that are supplying phones, laptops and tablets.

Beyond mobile chargers, the company is gearing up for solar, datacentre and electric vehicle applications, and anticipates these markets to start bringing in revenue within the next 3 years. "The fast mobile charging market is our bread and butter right now, but beyond charging, our strategy includes looking at solar, electric vehicle and data centre markets," says Vaughan-Edmunds. "The electric vehicle and data centre markets take longer in design cycles and qualification, however these are key strategic markets for Navitas and where we are focusing.

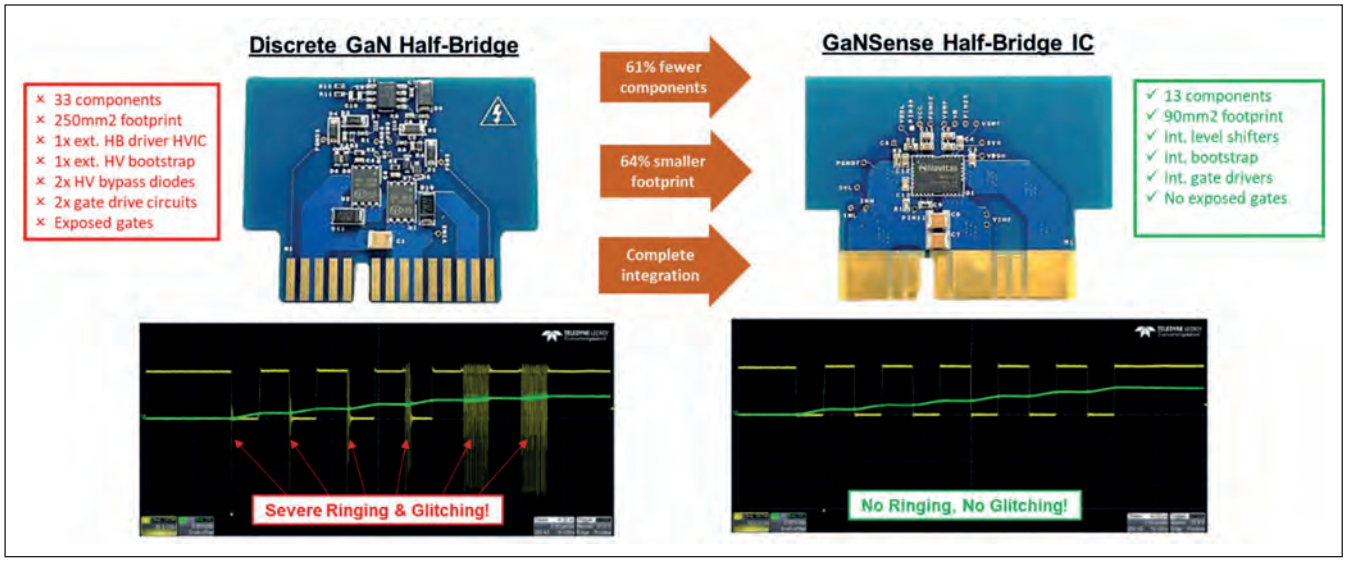
Navitas power ICs have been in production since 2018, and just last year industry analyst TrendForce indicated that this west-coast chipmaker held the greatest market share amongst GaN power device suppliers

"If we look at the mobile charging market alone – right now GaN only has a few percent of the total market so we've still got a lot of room to grow," he adds.

Bringing in SiC

Yet despite the company's clear advocacy towards GaN, it acquired SiC developer GeneSiC Semiconductor for $100 million in late August. At the time, Navitas chief executive, Gene Sheridan, said GeneSiC will help his company to accelerate growth in the high-power solar, datacentre and electric vehicle markets.

For his part, Vaughan-Edmunds highlights how rugged, vertical SiC devices are better suited to traction inverters, which provide enormous amounts of torque and acceleration in electric vehicles. "We're not a gallium nitride company trying to convince customers to use gallium nitride instead of silicon carbide. We realise that silicon carbide has its place in the market, and it's a big market that we want to go after," he says. "On gallium nitride alone, we've already shipped more than 50 million pieces, with zero field failures – and that's only just scratching the surface."



➤ Discrete GaN half-bridge IC versus Navitas' latest half-bridge IC.

Finwave: Getting GaN ready for 5G

Can a relatively unknown MIT spin-off deliver the fast, cheap GaN FinFETs that an entire industry needs? Finwave co-founders, Bin Lu and Tomas Palacios, have teamed up with industry veterans from International Rectifier, Peregrine Semiconductor and Soitec to do just this, reports **REBECCA POOL**

COME 2025, 5G networks are likely to cover one-third of the world population, accounting for some 1.2 billion connections, predicts the GSMA, UK's Global System for Mobile Communications. The impact on the mobile industry will be profound, a fact that hasn't been lost on many a semiconductor start-up vying to provide the tech the telecoms industry needs to chase ever-higher speeds and efficiencies.

One clear example is US-based Finwave Semiconductor, the MIT spin-off that started life as Cambridge Electronics and following a decade of quiet development, has emerged and rebranded to commercialise its high-efficiency, high-linearity GaN devices. Announcing its intention to 'revolutionise the future of 5G communications' in June this year, Finwave has also just won $12.2 million in Series A funding to expand its team, ramp up product development and get its FinFET-based GaN transistors swiftly to market.

As lead financier, Jennifer Uhrig, from Fine Structure Ventures, said at the time: "Finwave's technology unlocks the promise of 5G... The company combines best-in-class power amplification efficiency with high-volume manufacturing to overcome the

performance and cost limitations that have together stymied widespread adoption of millimetre-wave."

Firm foundation

The FinFET – with its multiple-gate architecture and nanometre-sized fin-shaped channels – isn't new. Thanks to superior gate control and reduced short-channel effects, silicon FinFETs have been widely used in digital and memory applications as CMOS technology nodes have shrunk over the last decade.

However, at the same time, researchers worldwide have also developed GaN FinFETs for high-voltage, high-frequency RF and power applications, with GaN-on-silicon FinFETs emerging more recently. And this is where, at least for 5G, the technology holds huge appeal.

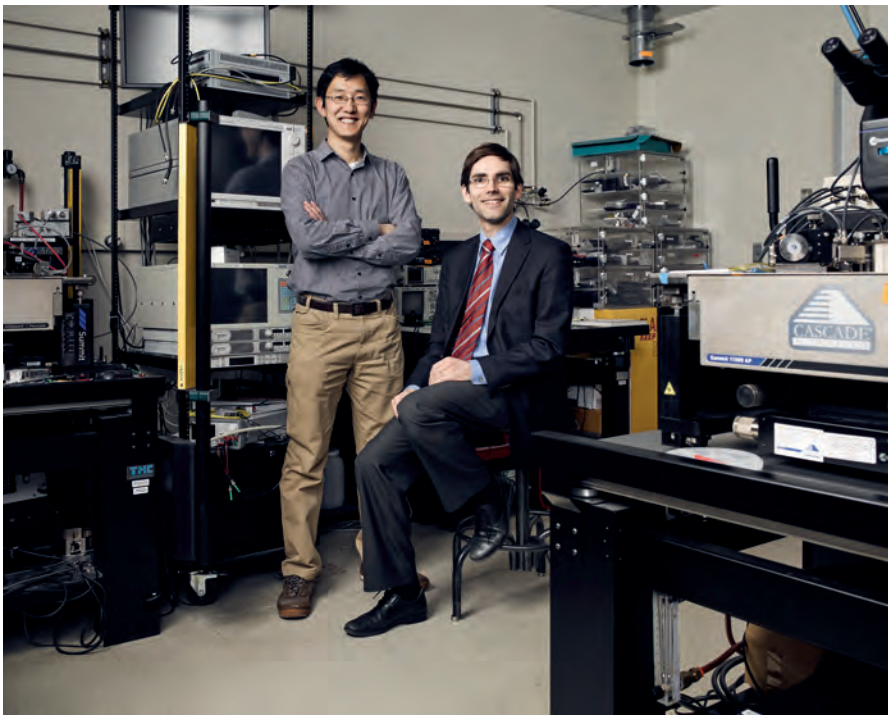
As Bin Lu, Finwave's chief executive and co-founder, points out, the 3D fin structure was exactly what GaN transistors needed to raise efficiency and linearity, to meet 5G requirements. "We started to work on GaN-on-silicon devices at MIT back in 2007, and then decided to borrow the silicon FinFET architecture and bring this to GaN so we could really shrink the gate length of the transistor," he says. "On doing this, we discovered some unique things about GaN FinFETs, including the reduced short channel effect and improvements in transistor linearity."

During this time, Lu and colleagues also devoted much time and effort to manufacturability, initially fabricating structures on 1 cm^2 coupons and pioneering their so-called etch-stop barrier structure to progressively scale up the technology. Along the way, as part of a $4 million ARPA-E program, they worked with industry's key epitaxial wafer vendors, foundries, chip and module manufacturers, and in an industry first, transferred their process to a US-based 8-inch silicon wafer manufacturing plant just last year. Lu won't be drawn on collaborator names, but as he says: "'We've been working with what I believe to be the three largest materials suppliers."

Industry experience

From word go, Lu has worked closely with fellow company co-founder Tomas Palacios, but in the last year or so, they have been joined by key industry veterans. Jim Cable, past chief executive of RF SOI pioneer, Peregrine Semiconductor, is chief strategy officer, while Ian Warbrick, also from Peregrine and International Rectifier, holds the position of chief operating officer. Thom Degnan, past Soitec president and chief operating officer as well as Intel, Infineon and Qualcomm vice president, is executive vice president of sales and marketing.

Excited to be a part of Finwave, each has a wealth of experience in manufacturing expansions and taking new products to market. As Cable puts it: "This journey is similar to past journeys – we're bringing a new material into high-volume markets." And according to Degnan: "We've taken a very organised, ready-aim-fire approach – we've established the value proposition, built the plan and executed that plan – this is a very good team."



➤ Finwave co-founders, Bin Lu (left) and Tomas Palacios (right).

Going forward, Cable believes the company's 8-inch and eventually 12-inch CMOS compatible processes – which don't require any special tooling – are going to be critical. Following their GaN FinFET on an 8-inch R&D process, they now expect to qualify 8-inch volume production by the middle of next year.

"The biggest cost reduction comes from using CMOS foundries.... and our thrust is to really get 8-inch GaN into high-volume production," highlights Cable. "Today, it is a challenge for epi-growers to do 12-inch GaN-on-silicon – but there are people that have done this."

All executives agree that the transition will only come once the market can support 12-inch volumes. Still, as Cable adds: "Soitec has invested in our Series A round of funding, and is the best materials company in the world. [Twelve-inch] is going to happen, there is no fundamental reason why it can't, and I think we could demonstrate it by the end of next year."

For his part, Lu believes that now is absolutely the right time to be taking GaN-on-silicon FinFET transistors to market. The latest devices can deliver more than 10 dB higher linearity compared with conventional technologies, such as silicon RF SOI MOSFETs, and he reckons cost parity is more than achievable.

"As we go to 5G, everyone is looking for technologies that can be more linear," says Lu. "GaN-on-silicon is coming, it's going to dominate RF devices at volume, and we've got the key technology to do this."

Advancing Ga_2O_3 doping

Nitrous oxide, ammonia, and several carbon-containing molecules are strong contenders for doping gallium oxide. But which one's the best?

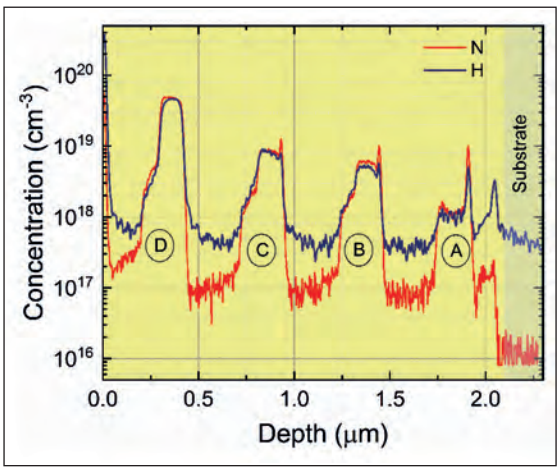
BY FIKADU ALEMA, AARON FINE, WILLIAM BRAND AND ANDREI OSINSKY FROM AGNITRON

THERE'S A LOT to like about Ga_2O_3. Thanks to a bandgap of around 4.8 eV, this semiconductor promises to provide more efficient switching than today's rising duo, SiC and GaN. What's more, crystals of Ga_2O_3 can be formed from the melt, indicating the potential for low-cost production of ultra-wide bandgap devices.

However, the picture is not all rosy. In addition to concerns over a limited thermal conductivity for Ga_2O_3, there are significant issues associated with doping [1].

Today it seems that the chances of effective *p*-type doping in Ga_2O_3 are rather bleak, due to the small energy dispersion of the valance band and the large effective masses in valance band states. These inherent weaknesses are limiting Ga_2O_3 device architectures to those that are unipolar. Although researchers have investigated whether impurities such as magnesium, iron, and nitrogen could unlock the door to *p*-type conductivity, all attempts resulted in deep acceptors.

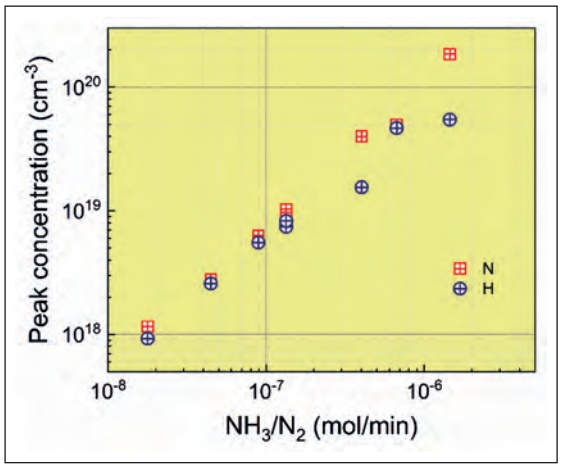
Such efforts are still valuable, though, because deep acceptors are beneficial for engineering Ga_2O_3 power devices. When Ga_2O_3 substrates are not intentionally doped, they still exhibit unintentional *n*-type conductivity, associated with significant levels of silicon, a background impurity. One can compensate for this by adding acceptor impurities, such as magnesium or iron, to the Ga_2O_3 melt – this enables the production of semi-insulating or highly resistive β-Ga_2O_3 substrates. The addition of deep acceptor impurities causes the equilibrium Fermi level to move away from the conduction band edge and closer to acceptor dopant states. This shift in the Fermi level allows a junction to form with adjacent *n*-type material, thus opening the door to the realization of potential barriers for voltage blocking. Ultimately, this could enable enhanced-mode Ga_2O_3 MOSFETs with an accepter-doped channel.



➤ Figure 1. SIMS depth profiles for nitrogen and hydrogen in a Ga_2O_3 SIMS stack of layers doped using NH_3/N_2 as a source for nitrogen doping. The A, B, C, and D labels show layers grown by introducing ammonia flow rates of 0.8, 4, 6, and 30 sccm. Increasing ammonia flow rate increases the nitrogen and hydrogen incorporation into the films.

Silicon does not just play a role within the layers of Ga_2O_3. In addition, as shown by secondary-ion mass spectrometry (SIMS), this element accumulates at the interface between the epitaxial film and substrate, regardless of growth method, process conditions, and the dopants in the substrate. The presence of silicon, thought to originate from silica-based polishing of the substrate, is a nuisance, degrading device performance. For example, in Ga_2O_3 FETs, silicon accumulating at the substrate-epilayer interface gives rise to a parasitic conductive channel that prevents the device from pinching off.

At Agnitron Technology, a provider of MOCVD tools for Ga_2O_3 growth based in Chanhassen, MN, we are fully aware of these issues and are playing our part in addressing them. We see ourselves as far more than simply an equipment supplier – we are heavily involved in developing Ga_2O_3 growth and processing technology, and through our collaborations with many leading research groups, we are helping to uncover solutions to many of the challenges associated with intentional doping of this oxide, as well as combating the impact of unwanted impurities. We shall offer a flavour of our success, and that of others, in the remainder of this feature.



➤ Figure 2. Linear dependence of the nitrogen and hydrogen incorporation on the molar flow rate of ammonia diluted in nitrogen (NH_3/N_2).

Excelling through etching

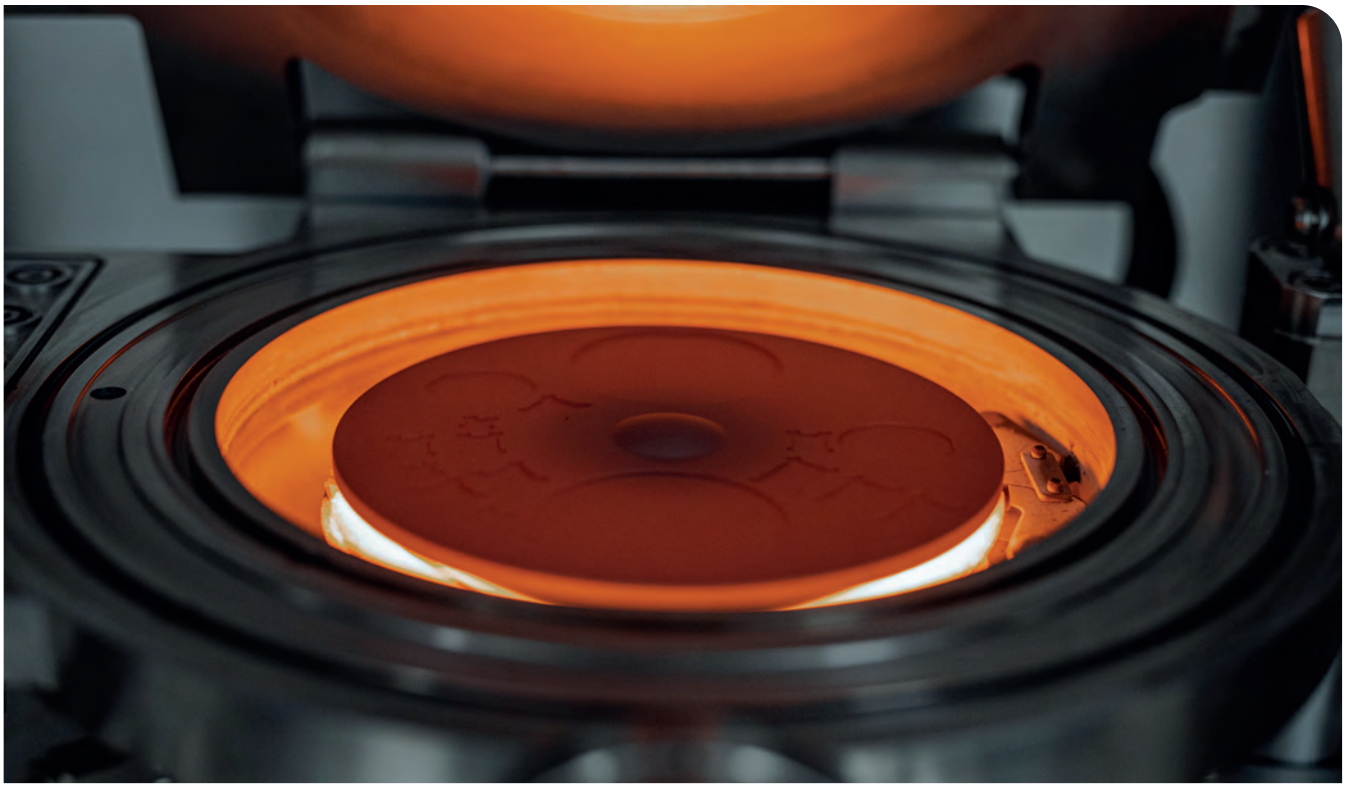
One common approach to trimming the concentration of silicon at the epilayer-substrate interface is to etch the Ga_2O_3 substrate in concentrated HF acid for around 30 minutes prior to growth. While this step does not eradicate silicon at the interface, its concentration falls. This leads to partial compensation by the acceptor impurity – either magnesium or iron – that defuses into the film/substrate interface from the semi-insulating substrates during epitaxial growth. Device results show that this methodology thwarts the threat of interfacial silicon reaching the active channel of the device. Working in partnership with Krishnamoorthy's group from the University of California, Santa Barbara (UCSB), last year, we reported high-performance, multi-kilovolt class Ga_2O_3 MESFETs with a record figure-of-merit for power of more than 350 MW/cm² [2].

As 30 minutes of etching fails to remove all interfacial silicon, it is tempting to increase the time for this process. But that's not a good idea: HF damages the substrate's surface, resulting in rough epitaxial films with surface pits that impair device performance. A far better approach is to compensate the interface with deep acceptor dopants, by either modifying the growth process or by ion implantation.

The merits of MOCVD

Of these two options, a growth-based approach delivers far better results. Implanting the likes of magnesium, nitrogen and iron requires an ion beam with such a substantial energy that it damages the crystal structure of Ga_2O_3 material and introduces unintended defects [3]. While thermal annealing can repair crystal quality, it causes impurities to defuse and redistribute inside and outside the implanted area. That's an impediment to realising a uniform, sharp doping profile.

Both MOCVD and MBE can provide uniform lateral and depth doping with no additional post-growth treatment. For MOCVD, researchers have demonstrated doping of Ga_2O_3 with magnesium, nitrogen and iron deep-acceptor dopants. Of the three, the two cation site acceptor species in



➤ Agilis 500 MOCVD from Agnitron that accommodates wafers with various shapes and sizes.

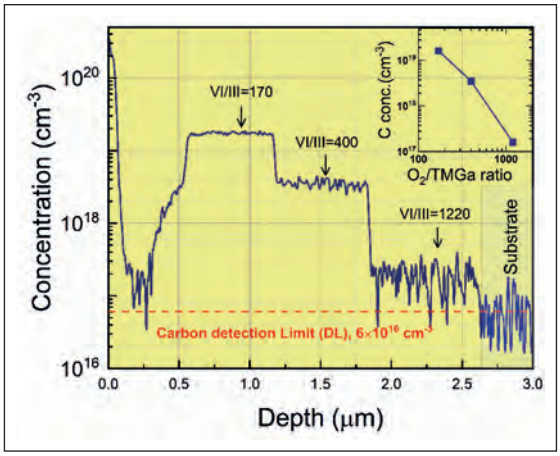
Ga_2O_3– that's iron and magnesium – have received more attention, partly because of their success in GaN. These dopants can be added using Cp_2Fe and Cp_2Mg, precursors that are solid at room temperature and have a low vapor pressure [4, 5]. Molar flow rates control doping concentrations.

For both these precursors, process engineers must deal with a surface riding issue. There's a threat that during the growth, doping extends into the layers not intended to be doped. This is exacerbated when a high substrate temperature is employed for the growth of the films [6, 7].

We have spearheaded efforts to develop doping by nitrogen, as this approach is less affected by thermal diffusion. Doping by nitrogen, which realizes deep acceptor conduction by substituting the oxygen site in Ga_2O_3 [8], can be realised with various nitrogen sources, including nitrous oxide (N_2O) and diluted ammonia. Note that molecular nitrogen (N_2) is unsuitable, due to its high level of stability that prevents the production of active nitrogen species for doping.

Nitrous oxide or ammonia?

The primary use of N_2O is as an alternative oxygen source for MOCVD of Ga_2O_3. Note that switching to this is not trivial, requiring an entirely different set of growth conditions to those typically used for growth with pure oxygen, including a higher growth pressure and temperature to ensure efficient decomposition of this oxide [7]. When used for both the growth of Ga_2O_3 and its nitrogen doping, the incorporation efficiency of nitrogen depends on process conditions, such as the N_2O/III ratio, substrate temperature, and chamber pressure. By varying these process conditions, β-Ga_2O_3 films with a nitrogen concentration ranging from an undetectable level up to around 2×10^{19} cm^{-3} have been realised, according to SIMS. Increasing the



➤ Figure 3. SIMS depth profiles for carbon in a Ga_2O_3 sample doped from TMGa by adjusting the O_2/TMGa ratio. The carbon concentrations increase with the decrease in the O_2/TMGa ratio, as seen from the inset.

Agnitron's MOCVD portfolio

THE EXPERIMENTAL RESULTS reported in this feature have been obtained using β-Ga_2O_3 MOCVD systems made by Agnitron. This original equipment manufacturer is proud to have had its MOCVD systems play a crucial role in the majority of scientific journals and conference presentations – more than 100 – associated with developing β-Ga_2O_3 materials and devices. Agnitron's contribution to all this success underscores its expertise in producing innovative and reliable β-Ga_2O_3 MOCVD systems.

At the heart of every Agnitron Ga_2O_3 MOCVD reactor is a proprietary, high speed Rotating Disc Reactor (RDR) vertical growth chamber with additional capabilities allowing for high speed operation – speeds over 1300 revolutions per minute. Through material science and design engineering, deposition throughout the chamber is less apt to find its way to the wafer surface. The unique feature of the high-speed RDR is its flow dynamics that repress particle recirculation, leaving areas above the wafer clean and free of deposition.

The remote injection gas delivery system has an unintentional gas phase reaction, resulting from the increase in the injection distance to the wafer, leaving undesirable particles on the growing surface of the films. This is due to the high oxidation rate during β-Ga_2O_3 growth, thus making it very difficult to utilize a remote injection gas delivery system, because the process generates particles that are hard to avoid. If particles reach the wafer surface, they can compromise device performance.

Agnitron addressed this concern by introducing high-speed rotation. With this refinement, particles are carefully managed on the surface and unwanted precipitation is eliminated. However, the excess gas phase reaction owing to the distance to the wafer remained a challenge.

Agnitron countered this threat by using a close-injection gas distribution system that combines the elimination of particles with excellent mixing of gases and precursors. High-speed RDR along with a close-injection gas delivery system reduces the formation of excess particles and prevents unwanted particles from reaching or sticking to the surface of the wafer.

Another merit of RDR high-speed rotation is its higher degree of control, ensuring superior thickness distribution uniformity.

Many of Agnitron's systems offer tremendous flexibility, allowing the operator to switch between a remote- and a close-injection gas distribution configuration in a matter of hours. Agnitron also offers the capability to add an upgraded close-injection gas distribution system, which ensures even oxygen injection across the entire wafer carrier, rather than just centrally.

Thanks to increasing interest in Agnitron's β-Ga_2O_3 reactors, all its systems are now capable of MOCVD growth on wafers up to 4-inch in diameter. For even larger single wafers, there is the Agilis 500/700.

growth temperature decreases the concentration of nitrogen, but its incorporation is accompanied by hydrogen, which follows a similar profile [5-7].

Films grown with an undetectable nitrogen concentration have also shown room-temperature mobility of more than 150 $cm^2 V^{-1} s^{-1}$, with a low free-carrier concentration of around 2×10^{14} cm^{-3}. Realising a low free-carrier concentration, alongside a mobility that's comparable to that for material grown using pure oxygen, is vital for high-voltage vertical power devices. Unfortunately, the purity of the N_2O-grown film is inferior to that grown using pure O_2, according to a low-temperature Hall measurement. This is thought to probably be associated with high compensation, related to nitrogen in the film, despite this element being undetectable by SIMS. At room temperature, the Hall mobility is not affected by nitrogen, because phonon scattering is the dominant mechanism.

The incorporation of hydrogen in the epilayers is far from ideal, because it acts as a shallow donor, compensating nitrogen [9]. This concern, alongside a high level of sensitivity of nitrogen incorporation to process conditions, makes it challenging to realise controllable doping. This led us to explore an alternative dopant, ammonia, which is widely used for the growth of GaN-based devices. Besides, ammonia decomposes at a relatively low substrate temperature of around 600 °C, making it a good candidate for use in nitrogen doping without altering typical growth conditions for Ga_2O_3 – that's not the case when using N_2O.

One of the key advantages of using ammonia, rather than N_2O, is that the flow rate can control the concentration of nitrogen incorporated in the film (see Figure 1). The relationship is ideal, with the nitrogen concentration linearly increasing with the molar flow rate of ammonia (see Figure 2). Unfortunately, when ammonia is employed as a precursor, the level of hydrogen tracks the nitrogen profile when films are formed at a typical growth temperature for Ga_2O_3. Moving to a higher growth temperature is beneficial: this increases the pyrolysis efficiency of ammonia, and when this gas is used to dope Ga_2O_3 films at these elevated temperatures, this reduces the hydrogen concentration, according to SIMS. Growing the film at a 100 °C higher than the typical growth temperature led to a reduction in hydrogen concentration by a factor of around 7. Annealing at elevated temperatures in a reduced-pressure environment may offer another approach to reducing the hydrogen concentration in these films, but its presence could still lead to compensative behaviour for nitrogen.

Our experiments back this up. We grew a number of nitrogen-doped single-layer Ga_2O_3 films with nitrogen concentrations of more than 2×10^{18} cm^{-3}. All samples were very resistive, with values for resistance more than three orders of magnitude higher than the control sample, an unintentionally doped Ga_2O_3 film produced under the same growth conditions. It is possible that hydrogenated gallium vacancies also lead to the electrical passivation of hydrogen [10].

Based on these findings, we feel that now is the time to explore an alternative precursor for the growth of nitrogen-doped, hydrogen-free Ga_2O_3 films. Our plan is to investigate nitric oxide (NO).

Carbon doping

In materials such as GaN, when carbon provides the dopant, it is known to act as a deep acceptor. However, how carbon behaves in Ga_2O_3 is far less clear. Some predict that it acts as a deep DX centre [11], while others argue that it behaves as a positively charged shallow donor [12].

There are several candidate materials for realising carbon doping during MOCVD. One option is to introduce simple hydrocarbons into the reactor, such as propane, but there is also the possibility of carbon doping with the precursor trimethylgallium (TMGa), which is used for film growth. A commonly cited challenge associated with the use of TMGa for the growth of Ga_2O_3 is a massive carbon incorporation into the growing layers, resulting from highly reactive methyl radicals forming during the pyrolysis process. However, the extent of this carbon incorporation is governed by process conditions – primarily the ratio of oxygen to TMGa. Adjusting this allows the growth of Ga_2O_3 films that are either doped or undoped with carbon.

We have used our family of Agilis MOCVD reactors to study the role that the ratio of oxygen to TMGa plays in carbon incorporation (see Figure 3). This involved growing a stack of layers at a constant pressure and substrate temperature, but varying the VI/III (oxygen to TMGa) ratio. According to

➤ Agilis 500 MOCVD reactor from Agnitron with an open showerhead and wafers with various shapes and sizes loaded onto the wafer carrier.

Samples	Carbon (cm^{-3})	Hall electron mobility results		
		n_{RT} (cm^{-3})	μ_{RT} (cm^2/Vs)	μ_{LT} (cm^2/Vs)
#1	No carbon (<6.0×10^{16}, DL)	1.1×10^{16}	106.0	12,600 @ 35K
#2	2.0×10^{17}	2.1×10^{16}	136.2	9,593 @ 35K
#3	2.0×10^{18}	3.2×10^{16}	89.0	227 @ 125K

➤ Table I: Electrical characteristics of carbon-doped films grown by varying the O_2/TMGa ratio.

SIMS, when we increased the VI/III ratio from 170 to 1220, this led to an almost linear fall in carbon incorporation by two orders of magnitude – it fell from around 2 x 10^{19} cm^{-3} to around 2 x 10^{17} cm^{-3}.

Working in partnership with researchers at the Air Force Research Laboratory, we have investigated films grown using oxygen-to-TMGa ratios beyond 2000. This created films that are essentially carbon-free – if there is carbon incorporated, it is beyond the SIMS detection limit of around 6 x 10^{16} cm^{-3} – with record high low-temperature mobility of more than 23,000 cm^2 $V^{-1}s^{-1}$ and an acceptor concentration of as low as 2 x 10^{13} cm^{-3} [13].

Our studies have shown that adjustments to the reactor pressure and the substrate temperature have no effect on carbon incorporation. This is evident from our growth of a number of layers at different pressures and temperatures, using a VI/III ratio in excess of 2000. Measurements of these test samples by SIMS show that the carbon content in the films remains below the instrument's detection limit. This has led us to conclude that the way to control the concentration of carbon in Ga_2O_3 films is to adjust the ratio between oxygen and TMGa.

Building on this investigation, we have explored the electrical properties of Ga_2O_3 films co-doped with carbon and silicon. Using O_2/TMGa ratios employed for the work presented in Figure 3, we have produced films and measured their room-temperature and low-temperature mobilities, using the Hall method. This investigation showed that for concentrations of carbon below 2 x 10^{17} cm^{-3}, the level of this dopant has no impact on mobility; but when this increases from this limit by an order of magnitude, mobility diminishes significantly (see Table 1). At higher carbon concentrations, there is more substitution on the gallium site, leading to crystal distortion and electrical compensation – both impact room-temperature and low-temperature mobilities.

While there is still much progress to be made, our efforts show that there are many different approaches to doping Ga_2O_3. Results depend on both the choice of dopant and the growth conditions.

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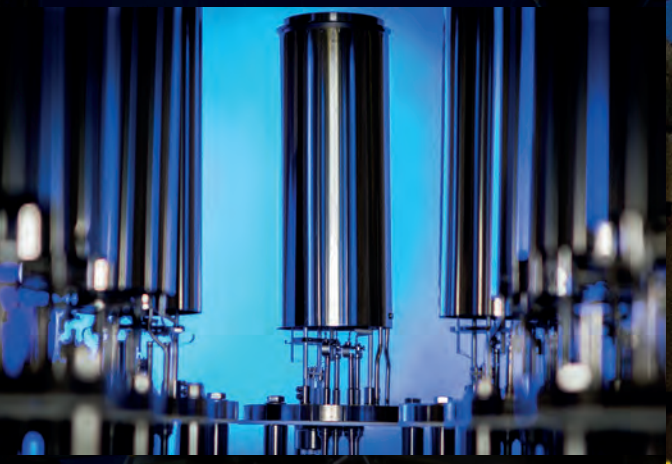

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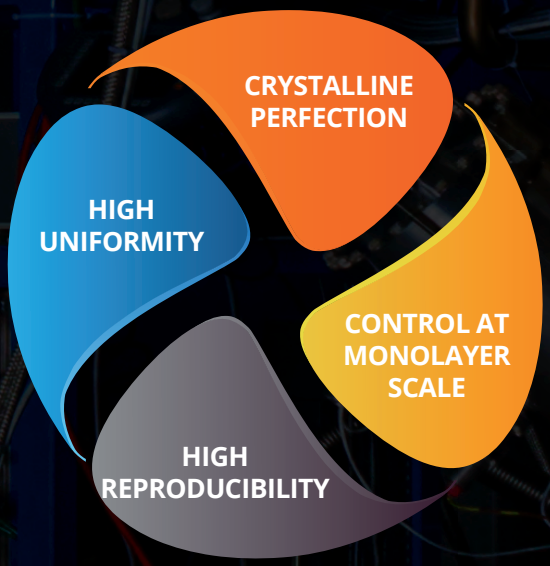

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Integrating microLEDs with advanced CMOS

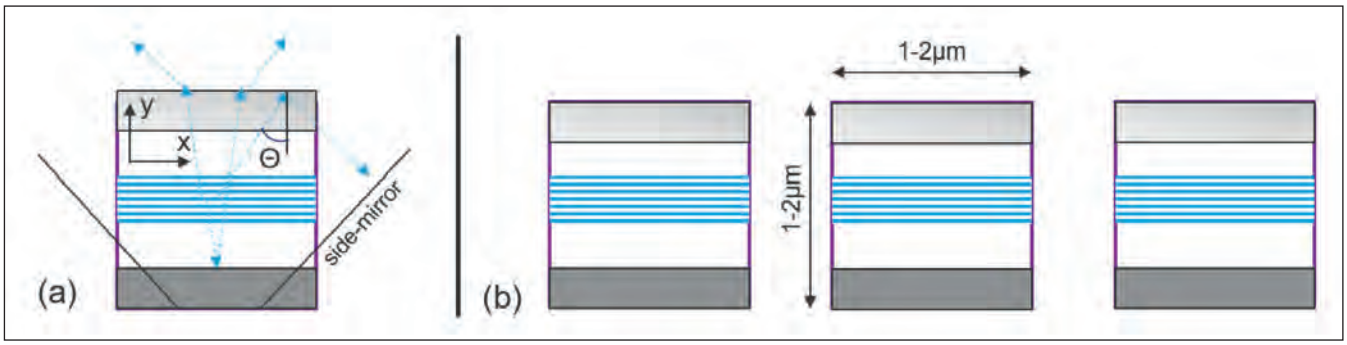
Bonding 300 mm GaN-on-silicon LED wafers to CMOS backplanes of the same size offers the best approach for producing displays that have a microLED pitch of just a few microns

BY SOEREN STEUDEL FROM MICLEDI MICRODISPLAYS

FOR THE LAST FIVE YEARS or so microLED manufacturing has been a very hot topic within the display industry. It's been high on the agenda at leading display events, such as *Display Week*, with the focus on flat panel manufacturing of various displays, ranging in size from smart watches to mobile phones and TVs. For this technology, efforts at scaling manufacture are thwarted by challenges associated with mass transfer of the microLED, as well as the repair of defective die.

A new set of issues are faced when considering microLEDs for microdisplay applications, like augmented-reality (AR) glasses. One approach to making a microLED-based display module for that type of application involves uniting microLEDs and CMOS backplane ASICs, which control and drive the microLEDs. This approach eliminates issues associated with mass transfer, but comes up against a different set of obstacles. Consider the primary application on the horizon for this technology, AR glasses: there's a need for a brightness exceeding 1 Mnits, pixel pitches below 3 μm, a resolution of up to 2K and beyond, ultra-low power consumption and acceptable cost, all in a light-weight module.

As of today, none of these specifications are being met by existing microdisplay manufacturing methods. But progress is underway. The chipmaker JBD of Shanghai, China, has introduced several impressive prototypes and is delivering modest volumes. However, high-volume manufacturing is elusive. Meanwhile, our company, MICLEDI Microdisplays of Leuven, Belgium, is making good strides on addressing issues that limit the brightness and resolution of microLED displays. To this end, we are developing an approach that's needed to deliver high-volume, low-cost manufacturing. Read on to discover the details of the challenges we face and our compelling solutions.



➤ Figure 1. Light-outcoupling in a planar microLED with (a) small pixel versus a (b) tight-pitched array.

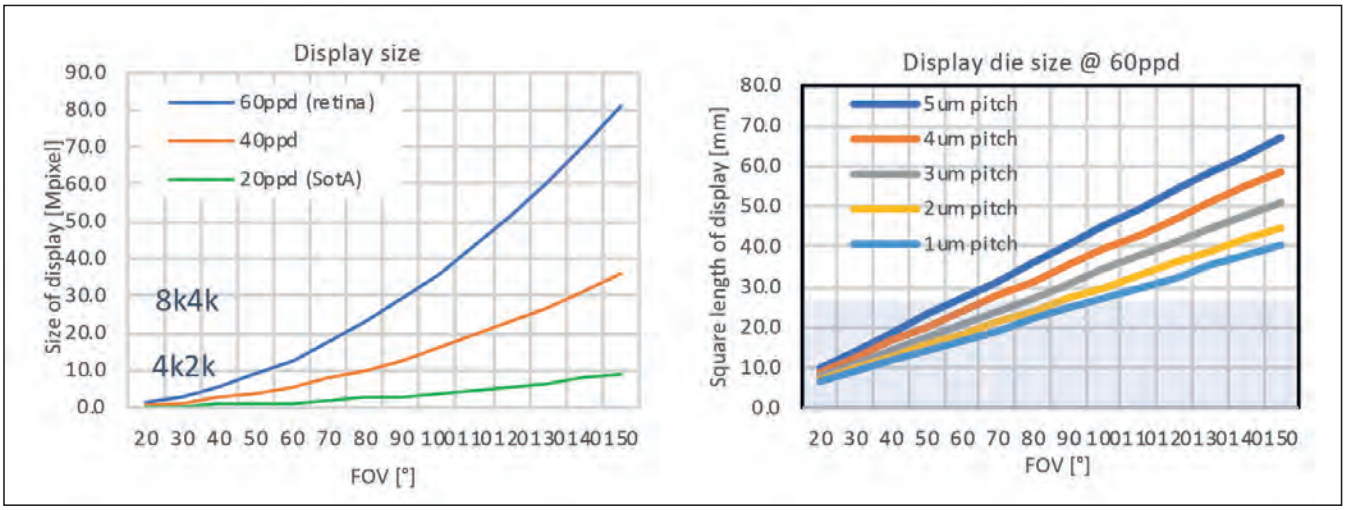
Brightness and efficiency

One weakness of AR glasses is their very substantial optical losses. The extent of this is governed by the implementation, but often less than just 1 percent of the photons emitted by the display arrive in the eye. Due to these staggering losses, displays have to generate up to 10 million nits of white light to support outdoor usage with high-transparency glasses.

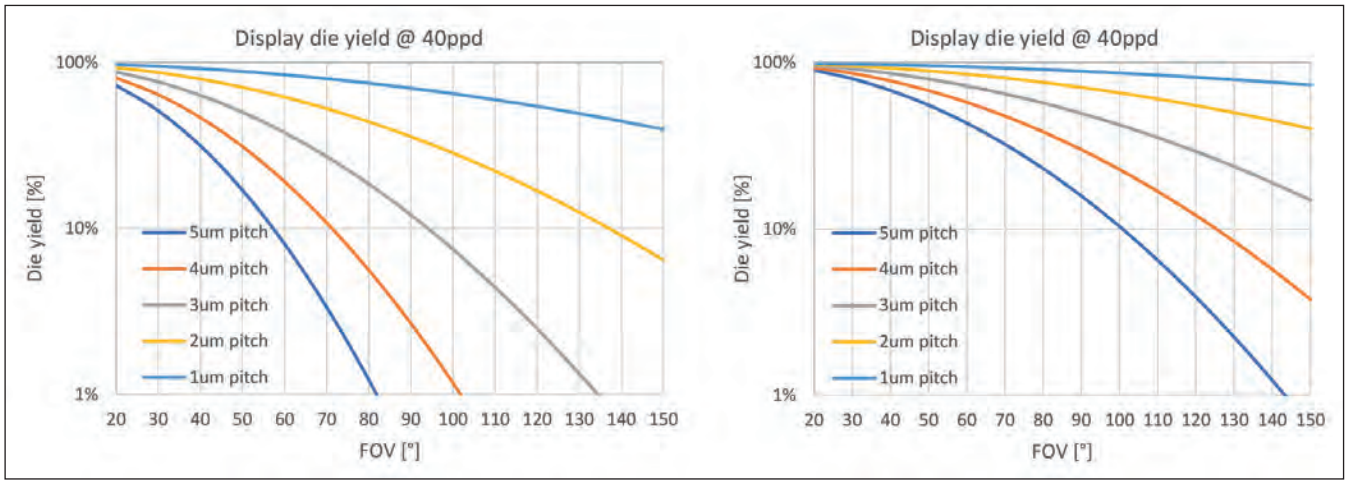
A comparable microOLED display, which is a rival technology to the microLED display, can achieve in the best case 20 knits for green, even though the efficiency number for OLED will be better than for microLED. A summary of the state-of-the-art by Yole Intelligence, the French market analyst, in 2019, showed efficiency numbers for OLED (RGB – 22 percent, 22 percent, 7 percent), versus the 5 µm microLED (RGB – 7 percent, 15 percent, 25 percent). Note that these figures are far below the values for the internal quantum efficiency of the GaN LED, which has a typical value of 85 percent in the blue, 60 percent in the green and less than 30 percent in the red.

Efficiency losses at scaled dimension are mostly due to optical outcoupling and, to a lesser extent, electrical losses due to defects at the mesa sidewalls, leading to a high amount of non-radiative recombination and an increased leakage current. The light-outcoupling in a planar LED is limited by the angle of internal reflection from the high index compound semiconductor material into air. This automatically means that for a GaN LED, less than 10 percent of the light can be extracted with a perfect backside mirror, neglecting interference effects. For larger LEDs with dimensions greater than 100 µm, surface texturing is applied with a very good backside mirror. This enables every photon to have multiple chances of escaping under different angles, leading to a theoretical light extraction efficiency of 75 percent. Surface texturing is not a solution for microLEDs with dimensions below 5 µm since there is no space for the photon to undergo multiple reflections.

It's also worth noting that the efficiencies provided by Yole are very optimistic, and only apply to individual LEDs spaced very far apart. This is illustrated in Figure 1, which considers different spacing scenarios. In microLEDs, the direct emission through the transparent front-side contact is very low, typically below 10 percent – but extraction



➤ Figure 2. ((left) Field-of-view (FOV) plotted as a function of pixel number for different angular resolutions (Mpixel refers to 1 pixel with a red-green-blue sub-pixel with a display ratio 1:1); (right) Die size for different sub-pixel pitches (assuming an advanced node CMOS (<45nm) with a framebuffer and a display ratio 16:9).



➤ Figure 3. Die yield versus field-of-view (FOV) for different sub-pixel pitches. (left) assumes RGB pixel-by-pixel; (right) assumes RGB die-by-die.

can be boosted by adding a sidewall mirror that extracts light beyond the angle of internal reflection. However, when packing microLEDs closer together to ensure a higher pitch, any type of sidewall mirror is less effective. Due to this impediment, the external quantum efficiency of microLEDs in very small displays is expected to be limited to no more than 8 percent, unless there is a shift to a directional emitter architecture.

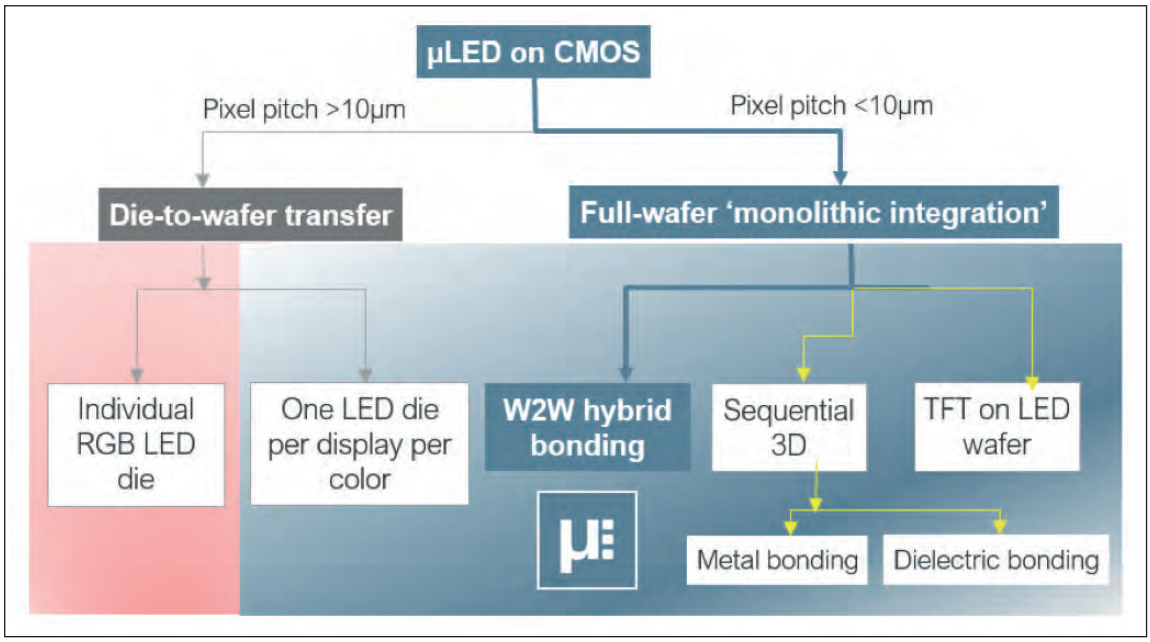
So, given these low values for microLED efficiency, these devices are still seen as a viable alternative to OLEDs, because they have a vastly superior current handling capability. By being able to sustain a current density that is more than a thousand times higher than an OLED can handle, these GaN-based devices can deliver the target brightness.

Display size and resolution

Two questions for any display based on the microLED are: What is its required size? And what resolution is appropriate? To answer them, it's imperative to consider the capabilities of the human eye. In both the green and blue spectral domain, the human eye has an angular resolution of 60 pixels per degree. We noted this figure when considering the targeted field-of-view for AR glasses. As one would expect, the number of pixels in a display must increase when increasing the field of view, or the angular resolution (see Figure 2, left). In some current commercial headsets, where the system supports a full high-definition display, there is a limited field-of-view of 50°. One benefit of moving from 5 μm to 1 μm microLEDs is that they can offer a larger field-of-view from the same display size (see Figure 2, right).

While this level of miniaturisation is appealing, it is far from easy to realise with routine success. Even the manufacture of a full high-definition display with 5 μm pitch approaches the limits of the reticule size of the exposure tool. Operating near this limit impacts manufacturability and yield.

We have calculated the impact of yield for different pitches. According to our manufacturing yield model (see Figure 3, left) – that assumes red, green and



➤ Figure 4. Overview of microLED-on-CMOS integration schemes.

blue microLEDs co-integrated side-by-side – even when the target resolution is reduced to only 40 pixels per degree, a pitch of less than 3 μm is needed to exceed a 50 percent yield.

It is possible to significantly relax these conditions by manufacturing three different colours of emitter independently, before bringing them together with an optical combiner (see Figure 3, right). This gets far closer to the yield model of an incumbent colour display technology, known as the sequential liquid-crystal-on-silicon display.

Manufacturability

Over the last ten years several groups have scaled the dimensions of the microLED below 1 μm. However, for these researchers, it is often only an afterthought to consider the integration of the LED pixel with the CMOS driver circuit, commonly known as the 'backplane' IC.

A number of approaches may be taken to realise this integration (options are summarised in Figure 4). One is die-to-wafer transfer, accomplished by either transferring and placing pixels one at a time to create an array of red, green and blue emitters, or by bonding the full array as an individual chiplet. Both these die-to-wafer transfers employ indium bumps, a technology that's been used in the mass production of infrared imagers for more than 20 years. Another strength of die-to-wafer transfer is that it allows the CMOS backplane to be made in a standard CMOS fab, and the front-plane diode array in a compound semiconductor fab – with each fab tailored to the particular wafer size and using dedicated tool sets. With this approach, production scales well to a pitch of 10 μm, before significant yield losses arise. There are also other die-to-wafer approaches with other types of micro-bumps, as well as hybrid bonding.

For military and space applications, ultraviolet and infrared imagers have been produced with pitches as low as 4 μm using die-to-wafer bonding. However, yield is very low – it's unacceptable for the display industry. So, for microLED displays, a full wafer-to-wafer approach is needed to go below a 10 μm pitch and combine the LED with the backplane. If wafer-to-wafer bonding is to be employed alongside a sequential 3D approach, the LED array wafer and the CMOS wafer must be the same size. That presents a problem: as microLEDs require more complex driving and compensation schemes compared with OLED displays, such as the inclusion of a framebuffer, the accompanying silicon circuitry must be made on 300 mm wafers, using advanced nodes that are well below 45 nm. As no 300 mm compound semiconductor epiwafers are produced in volume, efforts are currently directed at resizing (coring) larger CMOS wafers to 100 mm or 150 mm in diameter, resulting in costly wafer area loss. Progress with hybrid bonding is also hampered by the need for extreme surface planarity, as well as a very low wafer bow and generally low stress. All these requirements are challenging to fulfil with nearly every compound semiconductor stack deposited by heteroepitaxy.

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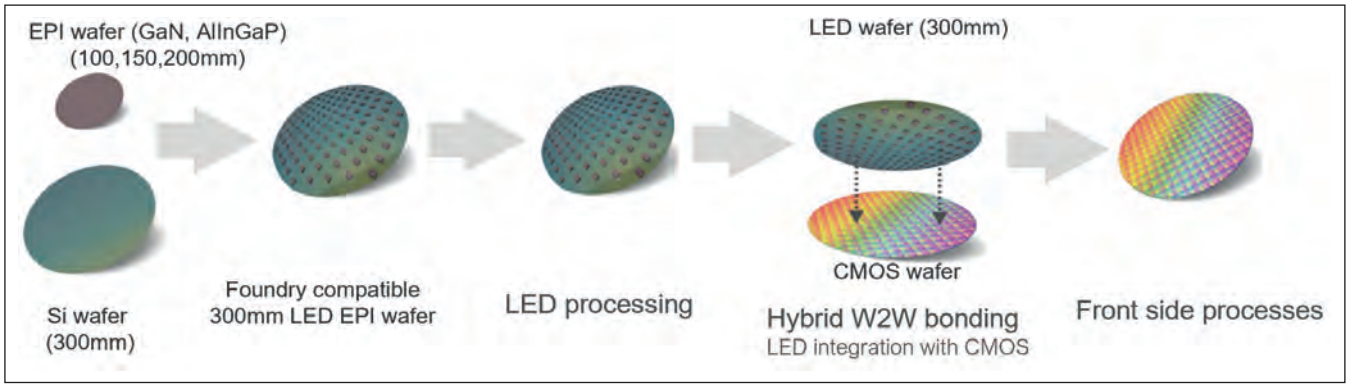
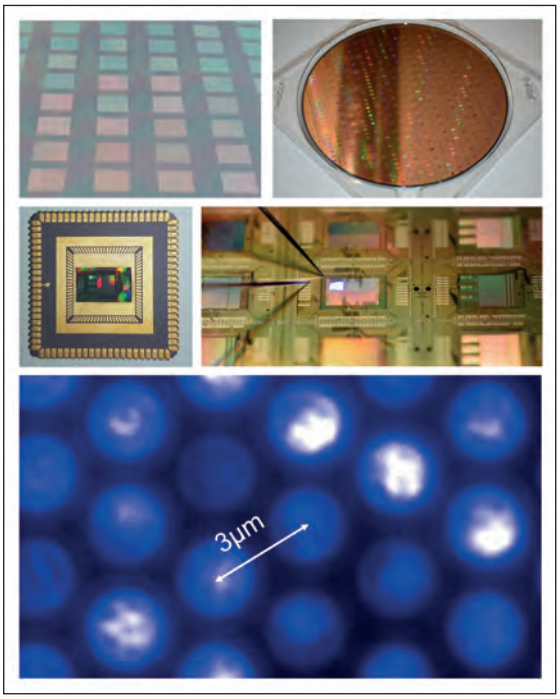
What's encouraging is that production processes to stack silicon wafers are already in use, combining sequential 3D structures with through-substrate vias and wafer-to-wafer hybrid bonding. The latter is commonly employed for producing backside-illuminated imagers with a pitch down to 3 μm, and is used in R&D departments to unite 300 mm wafers at a pitch down to 1 μm with overlays less than 200 nm.



➤ Figure 5. Manufacturing flow from 300 mm compound semiconductor reconstitution to hybrid bonding of a diode array with an advanced node CMOS.



➤ Figure 6. Images of a 300 mm LED wafer (a) after GaN reconstitution; (b) after a full wafer-to-wafer integration scheme. (c) packaged die. (d) a 480 x 320 passive array with 9150 ppi.

Display integration

Our company, a spin-out of imec that launched in 2019, is on a mission to solve the manufacturability and yield issues outlined above. While developing our display technology, the decisions that we have taken have adhered to the three following premises: our integration flow is developed on 300 mm production equipment, so that it can be transferred to a CMOS foundry; the materials we select are as compatible as possible with the contamination and waste management protocols of advanced CMOS fabs – so that means no silver, gold or GaAs; and that, as much as possible, established process steps and modules are adopted that have delivered high yields when manufacturing other products.

With these requirements at the forefront of our mind, we have developed an LED integration process that is very similar to that employed for making 3D backside-illuminated imagers. However, in our case we replace the silicon-photodiode wafers with that populated by GaN diodes (see Figure 5). We have overcome the limitations of the starting GaN material, such as its small size, significant stress and bow, and its high particle density, by sourcing best-in-class commercial epiwafers, screened from multiple vendors. Epi-dice are cut to the size of the final display, such as 4 mm by 6 mm for a full high-definition, prior to redistribution across a blank silicon wafer. Following removal and planarization of the epi-growth substrate and the buffer layer, we produce a stress-free 300 mm-diameter structure with known good epi-die pre-selected, so that only a 1.5 µm-thick GaN stack remains, featuring an active region sandwiched between doped layers (see Figure 6 (a)). From a wafer-handling perspective, this reconstituted wafer behaves like a silicon-wafer.

➤ Figure 7. Electroluminescence image of a red GaN-on-silicon linear array with a 7.5 µm mesa.

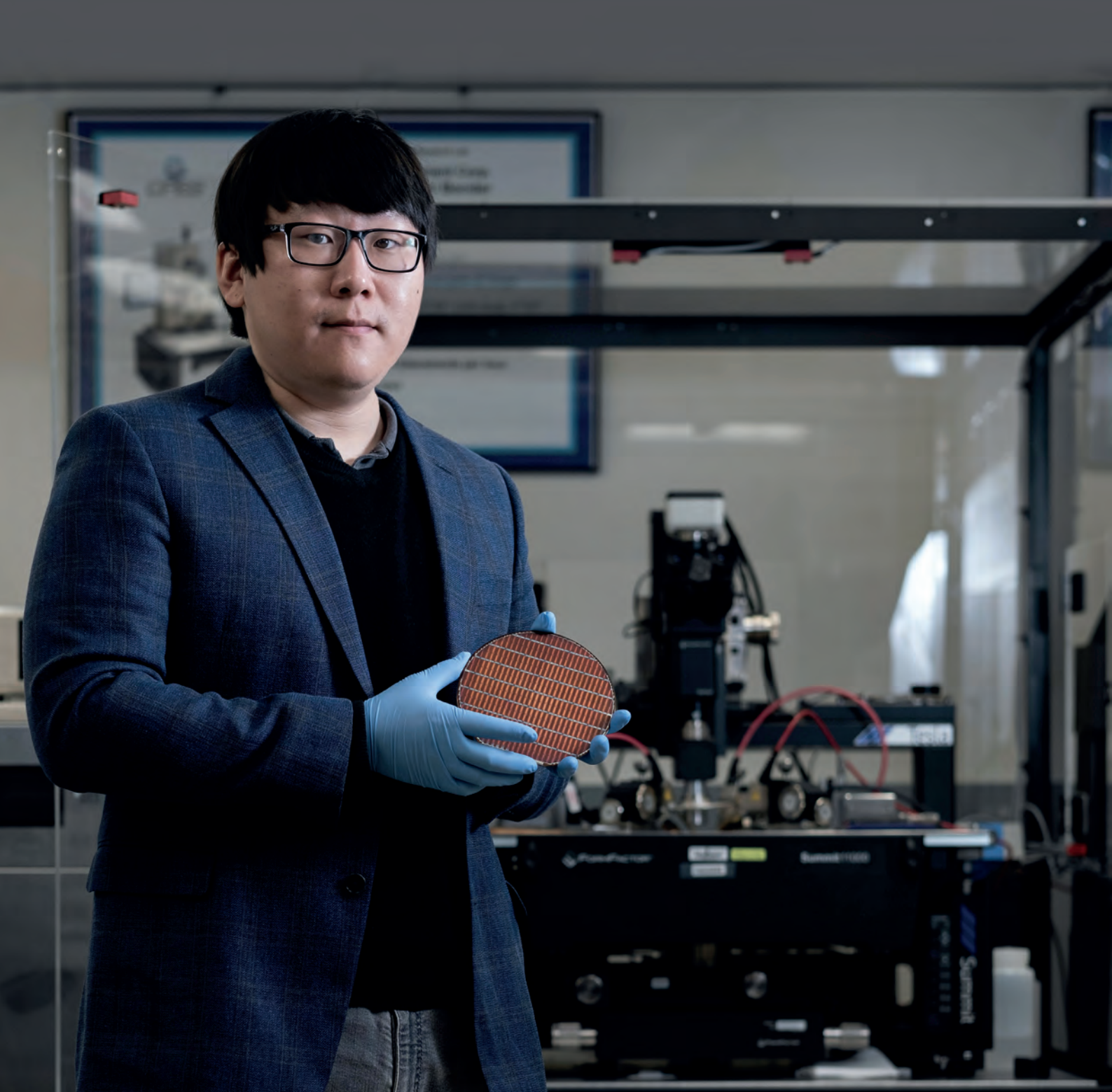
Processing creates LEDs with a 3 µm pitch on a 300 mm wafer. Subsequent wafer-to-wafer hybrid bonding unites this wafer to a 300 mm CMOS backplane ASIC wafer with an alignment accuracy tighter than 250 nm. For our initial process development, device characterization and sampling, we used a silicon wafer with just a few metal layers, limiting operation to passive control of the matrix arrays (see Figure 6 (d) for wafer-level testing of a passive array of 480 pixels by 320 pixels; Figure 6 (c) for an image of packaged die; and Figure 6 (e) for a microscopic image of the array with a 3 µm pitch and a 2 µm mesa). Our next step is to replace these passive arrays with an actual ASIC.

Using this integration scheme, we have realised a record aperture of up to 65 percent, with a mesa of 2.5 µm in a 3 µm hexagon-pitch configuration. This large aperture is a tremendous attribute, essential to achieving high brightness. The first blue-emitting wafers coming off the line have a brightness of 600,000 nits at 5 V. For these emitters, external quantum efficiency is more than 2 percent.

Our current approach is to draw together the output of red, green and blue die with an optical combiner. One implication of this methodology is that we have to use the same process flow for all three forms of die. As expected, it is the red LED that is providing the biggest challenge. Work is ongoing to improve the efficiency and the colour point. The first short-loop sample of a red source, formed from a 200 mm GaN-on-silicon epiwafer, can be seen in Figure 7.

Improving the wafer-level optics offers another avenue for raising performance. It should be possible to enhance brightness by a factor of two-to-four by enhancing light-outcoupling within the apex angle that is useful for waveguide integration – and suppressing light emission that is outside this angle. In a relatively short time we have demonstrated that for pitches of 5 µm and below, there is much merit in turning to a monolithic approach that involves bonding a 300 mm microLED wafer to a CMOS backplane wafer. Working with our partners at imec, we have addressed the challenges associated with the process, and we are now starting to transfer our technology to our foundry partner.

The authors would like to acknowledge the collaboration with the imec 300 mm pilot line and the imec 3D integration department.



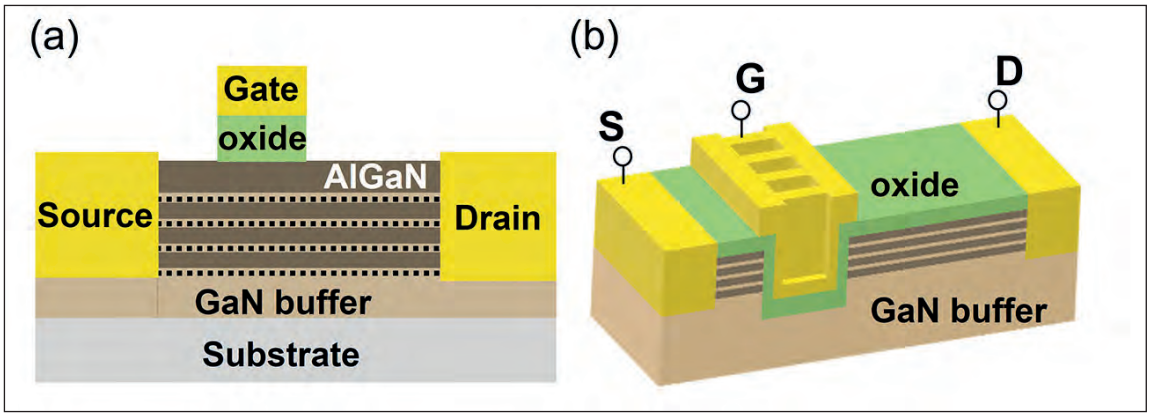
Stretching GaN power devices to 10 kV

GaN power rectifiers and transistors combine a breakdown voltage beyond 10 kV with a specific on-resistance that's below the SiC limit

BY YUHAO ZHANG FROM VIRGINIA TECH

➤ Yuhao Zhang holding a GaN power transistor wafer in front of the 10 kV probe station

ONE OF THE KEYS to getting carbon emissions to net zero is to increase the efficiency of electrical energy processing. This can be accomplished through the introduction of semiconductor-based power devices with a lower on-resistance, a faster switching speed and a high breakdown voltage. It is a roll-out that must include devices operating between 1 kV and 35 kV, a range that's often known as medium-voltage, but also referred to as high-voltage in many contexts. Devices operating in this range are ubiquitously used in electrical grids, renewable energy processing, industrial motor drives and electrified transportation. Driven by this widespread deployment, the market size for medium-voltage power devices has already topped $10 billion and is increasing at pace.



➤ Figure 1. The multi-channel AlGaN/GaN HEMT with a planar gate (a) and a trigate architecture (b).

Dominating today's medium-voltage power device market are a pair of silicon devices: the insulated-gate bipolar transistor; and the *p-n* diode, up to a voltage class of 6.5 kV. Both suffer from a slow switching speed, stemming from bipolar operation – as electrons and holes contribute to current conduction, both forms of carrier must be removed or supplied during device switching.

A superior performance can be realised by turning to the unipolar SiC MOSFET and the SiC junction barrier Schottky diode. These alternatives, which enable faster switching speeds, are covering an increasingly broad range of voltages. They have been commercialized up to 3.3 kV, and industrial R&D devices are available up to 10 kV.

But that's not the ultimate solution, as even better results are possible with SiC's wide bandgap rival, GaN. Providing a higher critical electric field and a higher electron mobility, GaN enables the fabrication of devices with a lateral or a vertical architecture. Lateral GaN HEMTs operating at up to 900 V are already on the market, and industrial vertical GaN transistors have been demonstrated at the 1.2 kV class. Progress has also been made at far higher voltages. Some groups are reporting GaN devices with blocking voltages close to 10 kV. However, specific on-resistances are much higher than those of SiC counterparts, leading many to conclude that GaN is only advantageous in the low-voltage range.

But those of us at Virginia Polytechnic Institute and State University – better known as Virginia Tech – beg to differ. Working in collaboration with engineers at the University of Southern California, the University of Cambridge, Enkris Semiconductor and Qorvo, we have developed a new generation of lateral medium-voltage devices that are based on a multi-channel GaN platform and outperform their silicon and SiC counterparts.

We produce our devices from multi-channel AlGaN/GaN wafers that consist of vertically-stacked heterostructures, which enable the fabrication of diodes and HEMTs that feature a high mobility two-dimensional electron gas (2DEG) channel. These devices offer a high-power handling capability, thanks to the stacked channels (see Figure 1(a)), and can leverage some of the benefits of vertical devices, such as a spatially distributed current. By drawing on a series of device innovations we have demonstrated 10 kV GaN Schottky barrier diodes and normally-off HEMTs that exceed the one-dimensional SiC unipolar limit, in terms of the trade-off between the specific on-resistance and the blocking voltage.

Challenges of multi-channel devices

It is easy to understand why the introduction of multiple channels reduces the on-resistance of a device. Using the 4-inch multi-channel GaN wafer grown by Enkris Semiconductor, the devices that we fabricate feature five channels, leading to a sheet resistance of just 120 Ω/sq – that's about a third-to-a-quarter of that of today's commercial GaN HEMTs formed from single-channel wafers. The upshot is that a switch to multiple channels enables a dramatic decrease in specific on-resistance.

Unfortunately, enjoying this benefit is far from trivial. There are two fundamental challenges associated with multi-channel devices.

The first arises because when the device is blocking voltage, there is a large volume of charge in the stacked channels that can lead to a fast drop in the electric field. This is a fundamental issue, expected from the simple Poisson equation. Due to this large

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volume of charge, there is a low average electric field across the device length, and increasing this dimension does not ensure an upscaling of the blocking voltage. Note that with these net charges, even if there is a good edge termination that enables a large peak electric field at the device edge region (see *Compound Semiconductor* 27 **3** 44), the blocking voltage of a multi-channel device tends to be much lower than that of a single-channel counterpart with the same length.

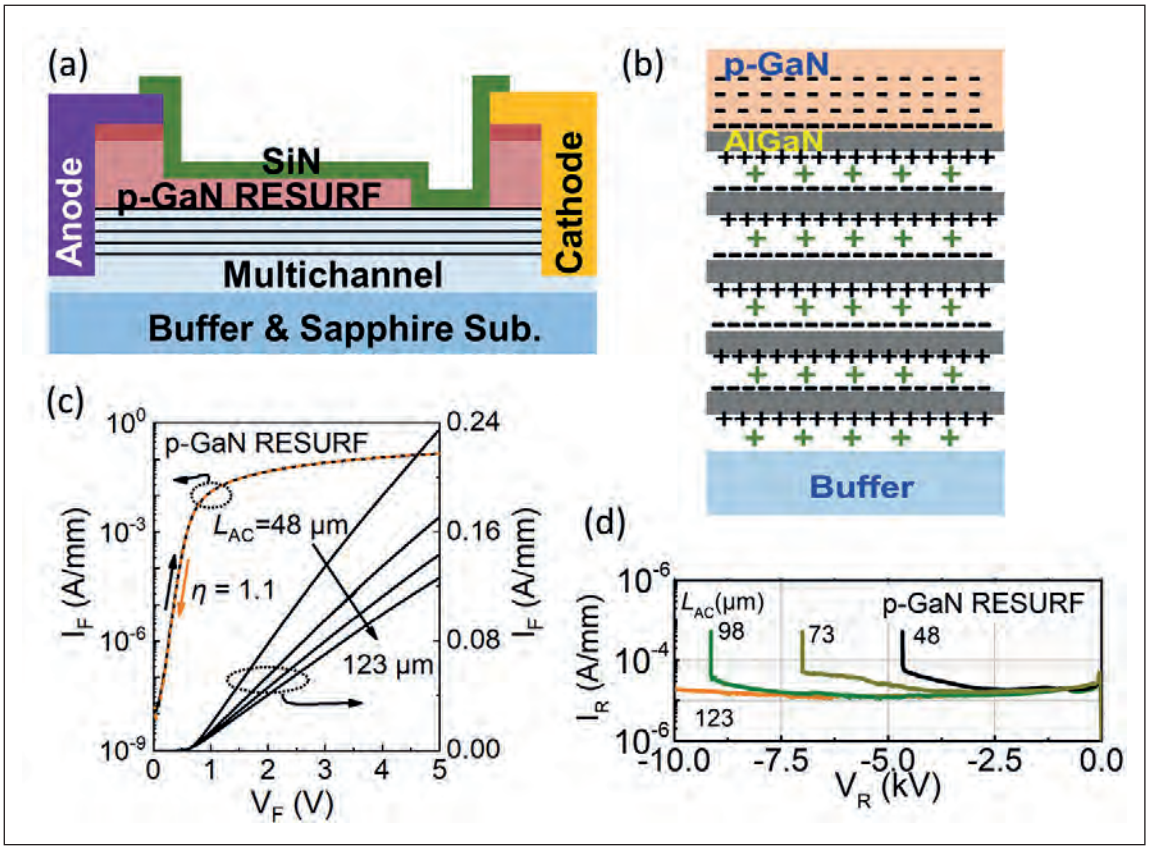
The second challenge faced with the multi-channel device is ensuring sufficient gate control. Within a conventional HEMT, a planar gate is often employed to modulate the 2DEG channel. That's not a good idea in a multi-channel device, because the top 2DEG channel will shield the gate electrostatics from reaching the buried channels. If this approach is taken, there is a very negative threshold voltage, even down to -100 V, and a very poor transconductance. In short, such a device is unsuitable for power electronics applications, which should have devices that are normally off.

A solution to this issue is to turn to either FinFET or trigate architectures, similar to those deployed in deeply-scaled silicon CMOS devices. Introducing a trigate design (see Figure 1 (b)) results in the wrapping of multi-channel fins around a gate stack. With this configuration, the sidewall gate controls the buried 2DEG channels. However, due to the high 2DEG density, the fins must be as narrow as around 10-15 nm to ensure normally-off operation in multi-channel HEMTs. Since today's power semiconductor industry mainly relies on processing at length scales of 180 nm or more, it is very difficult to manufacture trigate multi-channel HEMTs on an industrial scale.

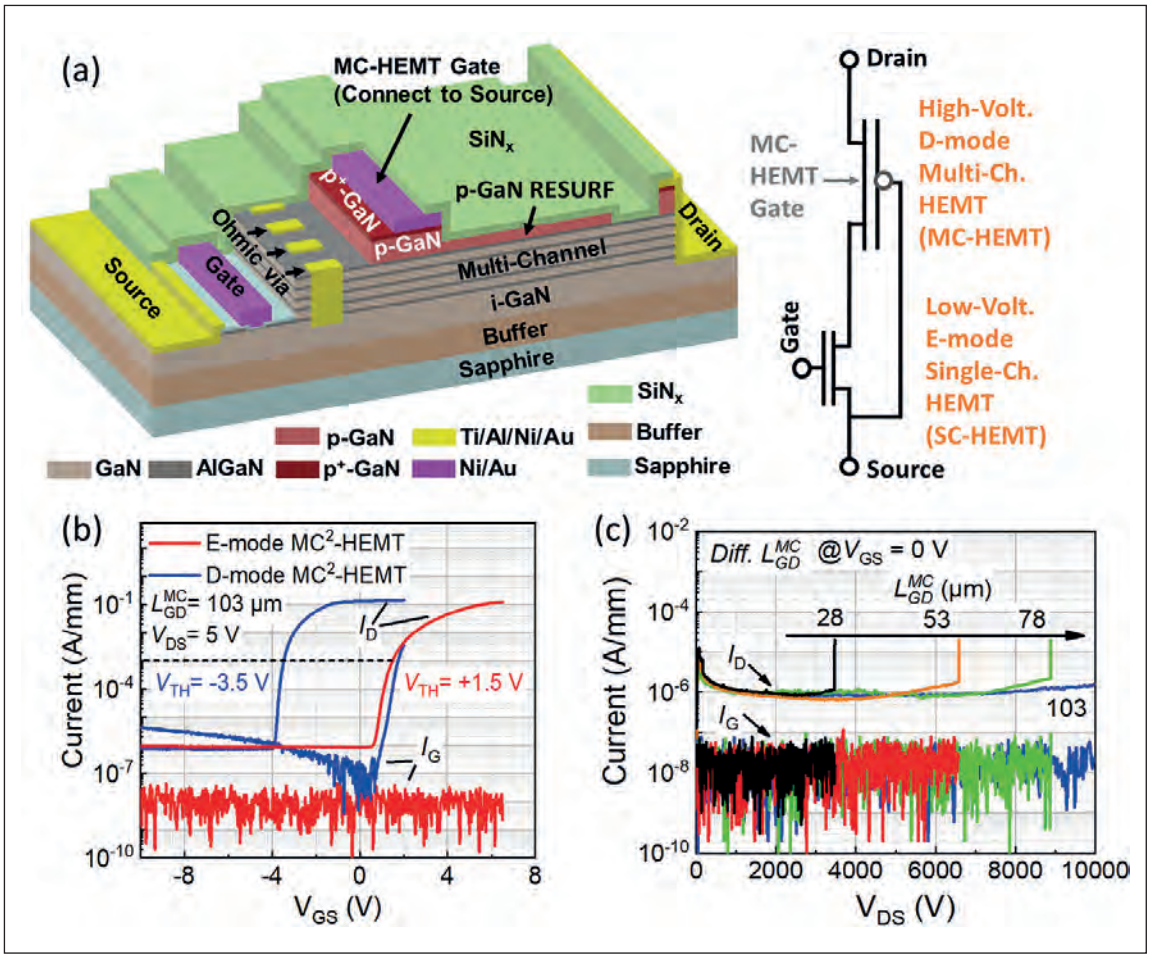
Reducing the surface field

Complicating the charge profile in a multi-channel architecture is the existence of multiple sources of polarization charge. Overall, a net donor tends to be present, which is in part the origin of the 2DEG in the multi-channel at zero bias. To balance this net donor at high blocking biases, we introduce a *p*-type GaN cap layer that provides a reduced surface field (RESURF) structure (see Figure 2 (a)). In a diode, this *p*-GaN RESURF layer extends to near the cathode, and its acceptor charges balance the net donor charges (see Figure 2 (b)). We are able to experimentally realise this charge balance by designing an appropriate *p*-type doping concentration, or by adapting the *p*-GaN thickness through a *p*-GaN etch that is monitored by a test structure.

It is worth noting that the addition of this *p*-GaN cap decreases the 2DEG density, particularly in the top channel. The wafer that we use, provided by Enkris, is produced by MOCVD, with the *p*-GaN layer grown continuously with the five-channel structure. This has a sheet resistance of 178 Ω/sq, which is still higher than the equivalent wafer without the *p*-GaN layer. However, compared to the single-channel wafer, the sheet resistance is smaller by more than a factor of two. The upshot is a slight increase in the on-resistance, but this is overshadowed by tremendous gains in blocking voltage, enabled by the RESURF layer.



➤ Figure 2. (a) The *p*-GaN reduced surface field (RESURF) architecture improves the performance of the Schottky barrier diode via charge balancing. (b) Illustration of charge balance at reverse bias. (c) Forward and (d) reverse current-voltage characteristics of devices with different anode-to-cathode distances (L_{AC}).



➤ Figure 3 (a) The multi-channel monolithic-cascode HEMT, known simply as the MC2-HEMT, combines an on-resistance and blocking voltage that comes from the multi-channel region with a gate control that is dominated by the single-channel region. The design of the MC2-HEMT is shown alongside its equivalent circuit. (b) Transfer characteristics of the MC2-HEMT with and without a gate recess in the low-voltage HEMT. (c) Off-state I-V characteristics of the MC2-HEMT with various lengths of the multi-channel region.

The introduction of RESURF technology has enabled us to fabricate a Schottky barrier diode with a turn-on voltage of just 0.6 V (see Figure 2(c)), which is lower than that of SiC junction barrier Schottky diodes. Through judicious choice of the anode-to-cathode distance, the blocking voltage of the *p*-GaN RESURF Schottky barrier diode can be about 1.5-fold higher than that of a Schottky barrier diode with merely a *p*-GaN termination (see Figure 2(d)).

For RESURF Schottky barrier diodes, the average lateral electric-field can be as high as around 1 MV/cm. This enables a Schottky barrier diode with a 123 µm anode-to-cathode distance to realise a blocking voltage of more than 10 kV and a specific on-resistance of just 39 mΩ cm^2 – that's 2.5-fold lower than the specific on-resistance of state-of-the-art 10 kV SiC junction barrier Schottky diodes.

Normally off 10 kV HEMTs

To realize normally-off operation without the need for sub-micron lithography, we are pursuing a new device concept: the multi-channel monolithic-cascode HEMT, which we refer to as the MC2-HEMT. Due to its cascode configuration, the normally off low-voltage transistor is connected to the normally on high-voltage transistor. The composite that results may be operated in a similar manner to the standalone, normally off, high-voltage transistor. Note that cascode configurations are well established, with commercial devices available in GaN and SiC, where a silicon MOSFET is co-packaged with a GaN HEMT or SiC JFET.

A key difference between these cascode devices and the MC2-HEMT is that the latter builds on a single chip. There is monolithic integration of a low-voltage, normally off HEMT that has a single 2DEG channel and a high-voltage, normally on HEMT that is based on a stacked 2DEG multi-channel (see Figure 3(a)).

Within this design there is a plurality of Ohmic vias, which function as the effective drain for the single-channel, low-voltage HEMT, as well as the source for the multi-channel high-voltage HEMT. Additional features of this architecture are the introduction of

a gate recess in the low-voltage HEMT to ensure normally off operation, and the use of a RESURF structure for the high-voltage HEMT to upscale the blocking voltage.

The MC2-HEMT delivers a strong performance on several fronts, combining an on-resistance and blocking voltage that comes from the multi-channel region with a gate control that is dominated by the single-channel region.

Thanks to these characteristics, our MC2-HEMT can exploit the low sheet resistance that stems from multiple channels while realizing a normally off gate control and enjoying complete shielding of the gate region from a high electric field. This design also obviates the need for sub-micron fin gates, significantly relaxing the lithography requirement.

Measurements of device transfer characteristics (see Figure 3(b)) shows that the introduction of a gate recess to the low-voltage HEMT enables a threshold voltage of over 1.5 V. Meanwhile, off-state current-voltage characteristics (see Figure 3(c)) validate our claim that the blocking voltage scales with the length of the multi-channel region up to more than 10 kV.

For the 10 kV MC2-HEMT, specific on-resistance is only 40 mΩ cm^2, which is 2.5-fold smaller than that of 10 kV SiC MOSFETs, and well below the one-dimensional SiC unipolar limit. Another great result for our MC2-HEMTs is that they have the highest Baliga's figure-or-merit for any power transistors operating at 6.5 kV or more.

Our progress helps to demonstrate that medium-voltage GaN power Schottky barrier diodes and HEMTs operating up to 10 kV will allow GaN power technologies to enter a new era. These devices are breaking ground on many fronts: as well as offering higher voltages, they are setting a new benchmark for the trade-off between on-resistance and breakdown voltage that goes beyond the one-dimensional SiC unipolar limit.

Such results call into question the commonly held belief that SiC is superior to GaN in medium- and high-voltage power electronics. While SiC is now displacing silicon in this power electronic sector, the future surely belongs to GaN.

FURTHER READING

- M. Xiao *et al*. "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV" 2021 IEEE International Electron Devices Meeting, 5.5.
- M. Xiao *et al*. "10 kV, 39 mΩ·cm^2 Multi-Channel AlGaN/GaN Schottky Barrier Diodes" IEEE Electron Device Lett. **42** 808 (2021)
- Y. Zhang *et al*. "GaN FinFETs and trigate devices for power and RF applications: review and perspective" Semicond. Sci. Technol. **36** 054001 (2021)

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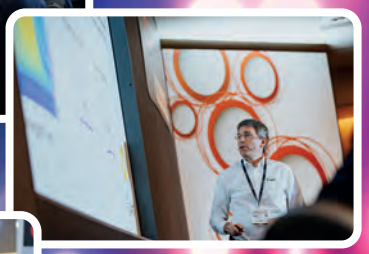


The allure of cubic SiC

The exceptional electronic and mechanical properties of the cubic form of SiC are enabling this polytype to take rapid strides towards serving in medical devices, MEMS and power electronic applications

BY FRANCESCO LA VIA FROM THE INSTITUTE FOR MICROELECTRONICS AND MICROSYSTEMS

SiC is blessed with many attractive mechanical and electrical properties. Due to these attributes, it is a compelling candidate for making electronic devices and sensors that can be deployed in many settings. Chips made from SiC are strong contenders for deployment in sustainable energy systems, hybrid vehicles, low-power-loss inverters, implantable medical devices, optical devices, and in MEMS operating with high efficiencies at high temperatures.

One of the key considerations facing designers of SiC devices is which form of SiC is best for their target application. This wide bandgap semiconductor exists in nature in a number of crystalline structures, called polytypes, that are differentiated by the stacking sequence of the tetrahedrally bonded Si-C bilayers. Through variations in this stacking sequence, SiC adopts different atomic arrangements and symmetries, from hexagonal to cubic and rhombohedral – each has a different set of physical properties.

Today, the 4H form of SiC grabs the headlines, due to ramping volumes of diodes and MOSFETs for the electric vehicle market. Yet, despite all this success, it is not the best polytype in many important regards. This accolade could go to the cubic form of SiC, which has the highest electron mobility and saturation velocity, thanks to reduced phonon scattering that results from a higher symmetry. Known as 3C-SiC, this cubic polytype has the lowest bandgap – it is just 2.3 eV – and great thermodynamic stability, enabling growth at lower temperatures, such as less than 1500 °C. Unfortunately, thermodynamic stability at lower temperatures is actually a double-edged sword.

Its downside is that it reduces the thermal budget required for growth, thus limiting development of a reliable 3C-SiC bulk growth technology for realization of the seed for subsequent homo-epitaxial growth of device-grade 3C-SiC epilayers. Due to the lack of such a substrate, device developers are forced to grow 3C-SiC hetero-epitaxially on different substrates. Much effort has focused on optimizing the hetero-epitaxial growth of 3C-SiC on the two common hexagonal polytypes, 6H- and 4H-, but manufacturing costs are prohibitively high.

With growth on a native substrate impractical, there is a strong desire from both a technological and a scientific perspective to be able to grow high-quality 3C-SiC epilayers on a substrate with as large an area as possible. Silicon is the obvious candidate: alongside its widespread availability, large sizes and high level of affordability, it can be grown by CVD, ensuring a very high purity of the resulting product.

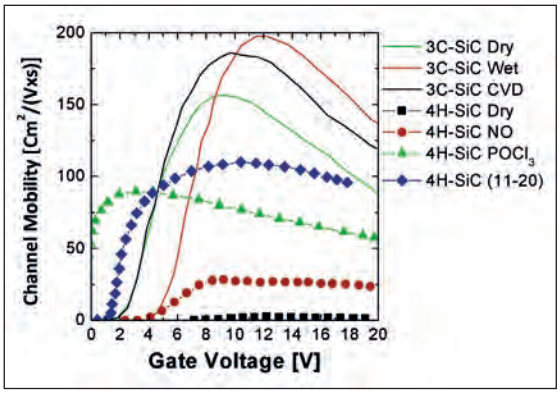
Power devices

The capability of 3C-SiC for making power devices is illustrated in Table 1, which compares the electrical properties of this polytype to those of 4H- and 6H-SiC. Silicon is also included, for the sake of comparison. The excellent characteristics of 3C-SiC have fuelled a persistent interest by the research community – and supported by the power device industry – to develop 3C-SiC devices with breakdown voltages ranging from 600 V to 1.2 kV.

Success would be most welcome. Growth on silicon would open the door to larger wafers and lower-cost production, while devices would benefit from high bulk electron mobilities, due to a higher symmetry within the crystal.

There are reports that channel mobility of 3C-SiC in structures produced with standard processing can reach ten times that of (0001) 4H-SiC (see Figure 1). Combined with the lower bandgap of 3C-SiC, the higher channel mobility should result in a lower value for on-state resistance, thereby reducing conduction losses in a forward-biased MOSFET. According to several device simulations, on-resistance should fall by about a factor of two, enabling a reduction in device area for the same on-resistance, and thus a lower-cost device.

Another attribute of 3C-SiC is its limited concentration of intrinsic carriers – they are about 11 orders of magnitude lower than that found in silicon.



➤ Figure 1. Comparison between the channel mobility in 3C-SiC and 4H-SiC.

This tiny concentration, correlated to the band-gap of 2.3 eV, contributes to a lowering of device leakage current under reverse bias, even in the low- and medium-power regimes.

In addition to these strengths, 3C-SiC has a high thermal conductivity and excellent mechanical properties. These characteristics ensure that sensors and devices based on this polytype are capable of working at temperatures above 250 °C. Operating under such conditions is required for devices that run at very high powers, or in extreme environments, such as those found in hybrid-vehicle engines and aerospace turbine engines.

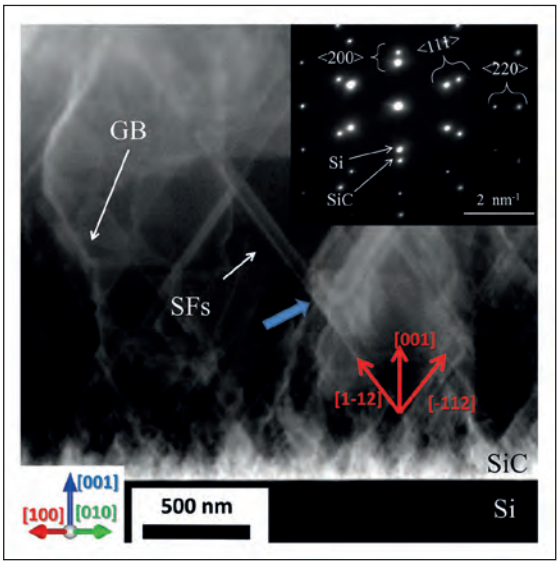
While there's no doubt that 3C-SiC has much to offer, enabling this material to fulfil its promise is far from easy, due to many challenges associated with the development of high-performance devices. To facilitate marketable production of electronic devices material quality must improve, costs must fall, and there must be a substantial increase in wafer size. The hetero-epitaxy of 3C-SiC on silicon offers an ideal solution to the last two necessities, but if this growth process is to make a real difference to the chances of cubic SiC, there needs to be a fall in the density of crystallographic defects in the epilayer.

These defects stem from the substantial difference in lattice parameters – they differ by 19 percent at room temperature – and the thermal expansion coefficients. For the latter, the difference between 3C-SiC and silicon is 23 percent at the deposition temperatures, and 8 percent at room temperature.

A variety of planar and volume defects originate at the interface between 3C-SiC and silicon. These defects include micro-twins, anti-phase boundaries

Property	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.12	2.35	3.08	3.28
Intrinsic carrier concentration at 300 K (cm^{-3})	0.3	1.5	2.2	2.3
Breakdown field ($MV\ cm^{-1}$)	1×10^{10}	1.5×10^{-1}	1.6×10^{-6}	5×10^{-9}
Electron mobility ($cm^2\ V^{-1}\ s^{-1}$)	1350	900	370	300
Hole mobility ($cm^2\ V^{-1}\ s^{-1}$)	480	40	80	120
Saturated electron velocity ($\times 10^7$ $cm\ s^{-1}$)	1	2	2	2
Thermal conductivity ($W\ cm^{-1}\ K^{-1}$)	1.5	3.2	4.9	3.7
Dielectric constant	11.7	9.7	9.6	9.6

➤ Table 1. The most relevant electrical properties of silicon, 3C-SiC, 6H-SiC and 4H-SiC.



➤ Figure 2. Transmission electron microscopy cross-section of the interface between silicon and 3C-SiC. Several extended defects can be observed.

and stacking faults in the epilayer, and voids in silicon beneath the hetero-interface (see Figure 2). These defects are device killers. However, their threat can be diminished by growing several tens of microns of 3C-SiC. This relatively thick film reduces their density, with some defects totally annihilated. Note that the defect density and the surface morphology strongly depend on the orientation of the silicon substrate.

Over the past three decades much effort has been devoted to developing a process for bulk growth of 3C-SiC. The motivation for this is that in very thick layers it's been observed that the defect density is low enough to enable the realization of power devices.

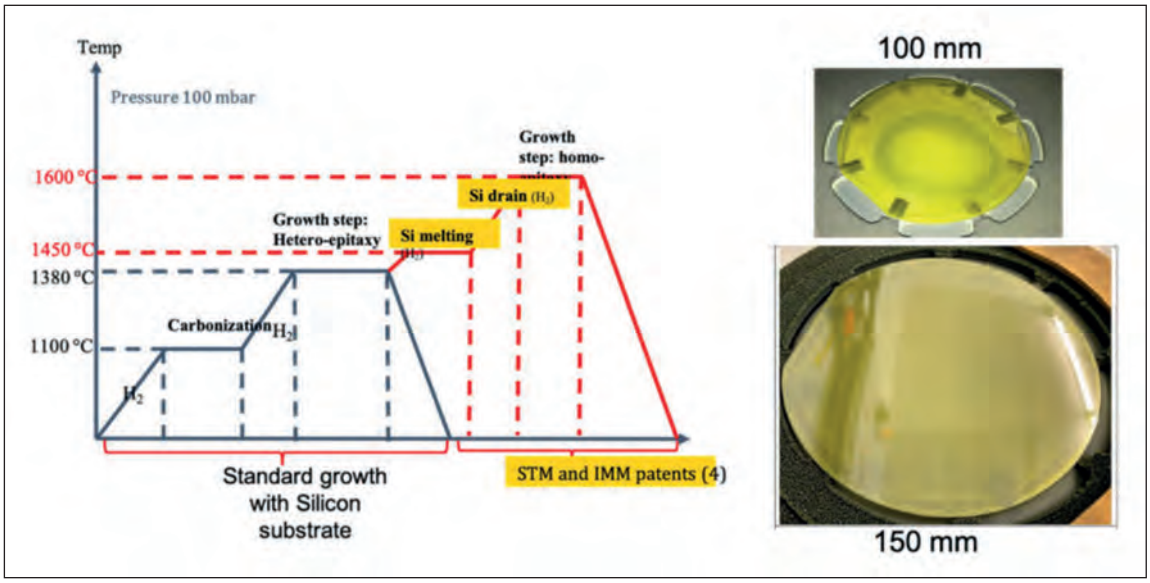
Working towards this goal is our team from the Institute of Microlectronics and Microsystems at Catania, Italy. We coordinated a four-year project entitled *Challenge*, which has driven the development of three different bulk processes that can produce a breakthrough in power technology. Through collaboration, those of us involved in this European project have developed a process for the bulk growth of 3C-SiC. Seeds of this polytype are formed on silicon (100) substrates that are loaded into a horizontal hot-wall CVD reactor, prior to the growth of epilayers with a thickness of 70 μm. A subsequent increase in temperature beyond the melting point of silicon (see Figure 3 for a temperature profile of the process) causes this substrate to fully melt inside the CVD reactor. The remaining freestanding SiC layer can then be employed as a seed layer for homoepitaxial growth, using a low-pressure regime and different temperatures (between 1600 °C and 1700 °C).

Our team increased substrate thickness with two hours of growth at a rate of 60 μm/h, with the last 10 μm low-doped for device realization. With this approach, using nitrogen and aluminium to form both *n*-type and *p*-type layers, our team produced 3C-SiC homoepitaxial samples with a thickness of about 200 μm, and wafers with diameters of 100 mm and 150 mm (see Figure 3).

Using this methodology, we have reduced the density of stacking faults with respect to thin layers by two orders of magnitude to typically just 10^2 cm^{-1}. Measurements of several *p-n* junctions formed by this approach show reasonable characteristics (see Figure 4). The leakage current of the diodes is still high, so efforts must be directed at a further decrease in the defect density, so that 3C power devices can deliver a competitive performance compared with their 4H cousins in the range of breakdown voltages between 600 V and 1200 V.

Making MEMS

The 3C form of SiC is blessed with very good mechanical properties (see Table 2). They include a high Young's modulus, a high fracture and flexural strength, and a low density. Thanks to the high ratio between Young's modulus and the density, devices made from 3C-SiC have exceptional promise for realizing very robust MEMS that can work at high



➤ Figure 3. Temperature schematics of the CVD process for the bulk growth of 3C-SiC. 100 mm and a 150 mm wafers are reported too.

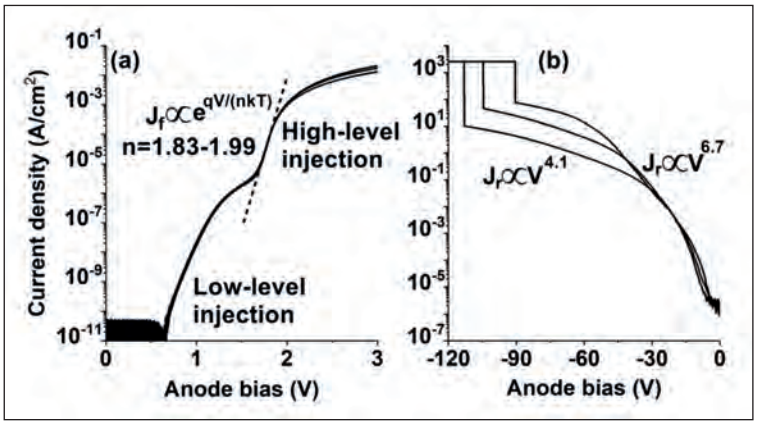
frequencies. What's more, these MEMS can operate at very high temperatures, such as 600 °C, because even in this regime there is not a large reduction in Young's modulus.

Efforts at developing micro- and nano-mechanical resonators have been motivated by the wide range of applications they can serve, both in industry and supporting fundamental science. These resonators can be used for precision sensing of mass, and to measure ultrasound, magnetic fields, inertia and strain. For many of these applications it is essential to realise a high resonator quality factor.

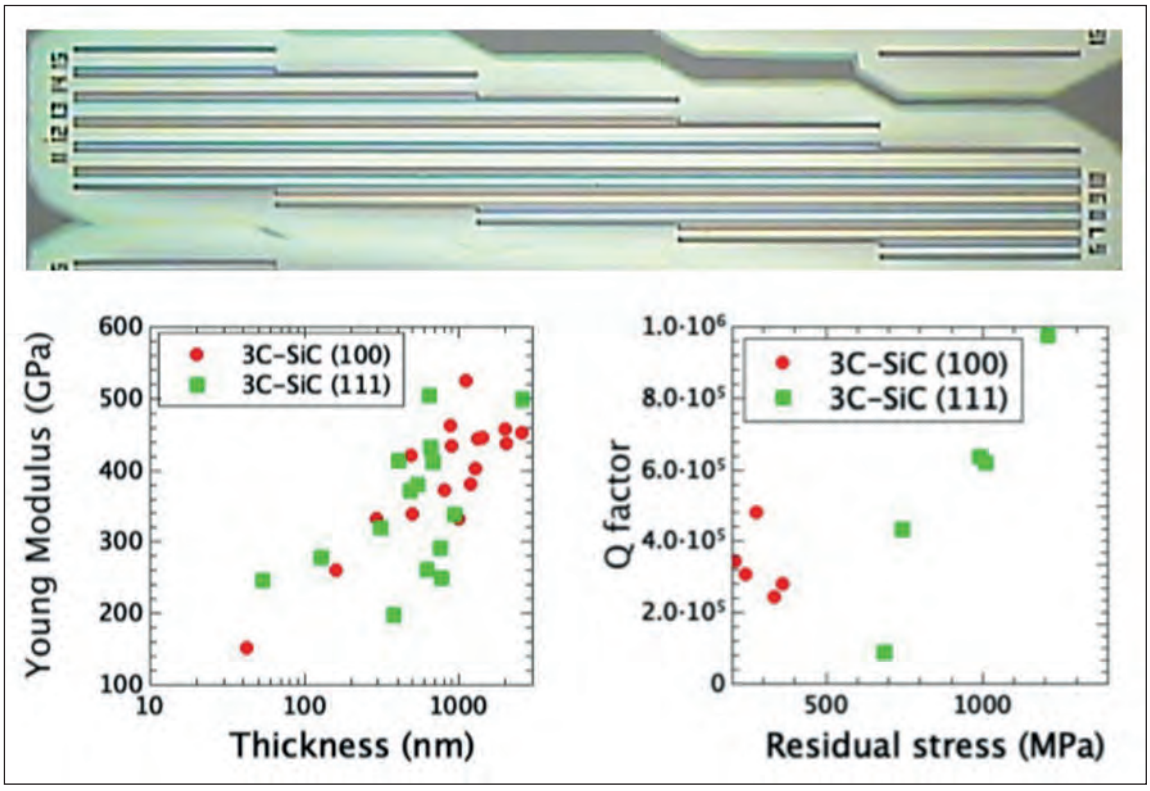
Recently, remarkable progress has been made in improving the quality factor of micro- and nano-mechanical resonators that are fabricated from highly stressed, thin amorphous films – most particularly amorphous SiN – formed on a silicon substrate. Further progress is possible by switching from these amorphous films to crystalline materials, which offer a range of advantages that could deliver a step-change in performance.

One of the merits of high-purity crystalline materials is their comparatively low defect density that allows significantly higher intrinsic quality factors. Values for this figure-of-merit of above 10^5 have been reported for highly pure diamond, CaF, and 3C-SiC – and when surface losses are eliminated, quality factors can exceed 10^6. This value far exceeds the quality factor of 25,000 for amorphous SiN and 1,000 for amorphous silicon. What's more, crystal-lattice mismatch is a benefit rather than a curse, as crystalline material with a high intrinsic stress is better suited to dissipation dilution.

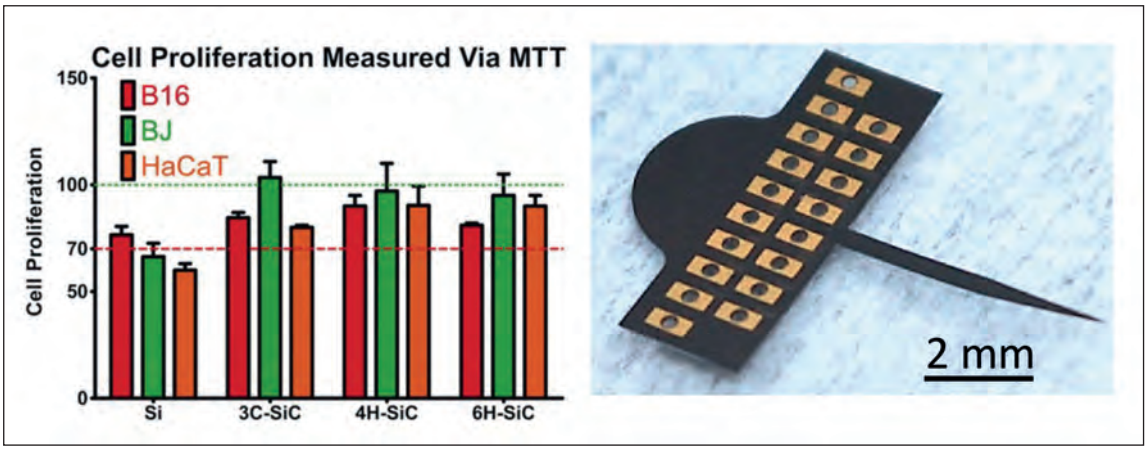
Yet despite these significant advantages, thin-film crystalline resonators are still to demonstrate the dramatic improvements in quality that have been shown in their amorphous counterparts. Progress is partly impaired by the increased complexity of fabrication, and – when grown on a silicon substrate – the dislocations and the high density of stacking faults near the interface. These imperfections degrade the mechanical quality factor and the Young's modulus.



➤ Figure 4. Forward (a) and reverse (b) characteristics of 3C-SiC p^+/n junctions on a bulk wafer grown by CVD. While the forward characteristics are almost ideal, the reverse show a high leakage current, due to the high defect density.



➤ Figure 5. (up) Double clamp beam array with different lengths and widths. (left) An increase in the Young's modulus with increasing thickness is observed in both (100) and (111) 3C-SiC. (right) The Q-factor increase at high residual stress is essentially in (111) 3C-SiC. In (100) 3C-SiC, the residual stress is lower, as is the Q-factor.



➤ Figure 6. (left) Cell proliferation for silicon and SiC. (right) A SiC neural probe.

In the last few years much progress has been made with 3C-SiC MEMS, due to developments in the growth process, in processing and in design. Several projects have reported success, including one we have coordinated called *SiC nano for picoGeo*. By addressing many of the potential pitfalls, this European effort has realised extremely good materials properties, even for films with a thickness close to 1 µm (see Figure 5, left).

Our measurements of the Q factor in structures with identical dimensions and design show that for the (111) form of 3C-SiC there is a clear linear dependence on residual stress, while this dependence is not clear for the (100) variant. Due to this characteristic, we are able to produce very efficient resonators, extremely sensitive strain meters and other high-performing MEMS devices with (111) 3C-SiC.

In the *SiC nano for picoGeo* project our team has produced a very sensitive strain meter, capable of detecting in the 10^{-12} -10^{-13} range. Such a high degree of sensitivity enables this sensor to detect very small deformations that occur a few hours before the eruption of a volcano or before an earthquake. These strain meters could also measure the deformation of a dam or a bridge.

It's worth noting that when 3C-SiC is used to make MEMS, only a thin layer of this material is needed, due to its good mechanical characteristics. Thanks to this, the fabrication process is quite easy, as it involves etching a thin layer of SiC, prior to a deeper etch of the silicon substrate, which can be accomplished using the standard process for silicon MEMS.

Implantable medical devices

Another important application where 3C-SiC can make a valuable contribution is in implantable medical devices. Silicon is highly toxic, leading researchers to pursue new classes of composite semiconductors, such as 3C-SiC, that offer a healthier solution. Experimental work by several groups suggests that SiC is extremely biocompatible, and is a good choice for this kind of device (see Figure 6, left).

Within the family of SiC poltypes, 3C-SiC appears to be a better option than its hexagonal siblings, because it enables the realization of thin implantable devices by etching the silicon substrate. This approach has enabled the fabrication of a neural probe (see Figure 6, right).

This work is in its infancy, and there are still issues to overcome. The biggest of these is the high leakage current from the junctions used to isolate the device from the substrate. Once this problem is overcome, 3C-SiC could be used to produce neural probes for the medical sector.

The cubic form of SiC clearly has much promise for power devices, MEMS and medical devices. Over the last few years much progress has been made in improving the structural quality of this material so that it can begin to fulfil its potential for delivering an outstanding performance. Thanks to these advances, it's not long before we could start to see the first commercial 3C-SiC devices on the market.

➤ Table 2. Physical properties of silicon, SiC and diamond.

Property	Si	SiC	Diamond
Lattice constant (A)	5.43	4.35	3.57
Cohesive energy (eV)	4.64	6.34	7.36
Young's modulus (GPa)	130	450	1200
Shear modulus (GPa)	80	149	577
Hardness (kg mm^{-2})	1000	3500	10000
Fracture strength (GPa)	1	5.2	5.3
Flexural strength (MPa)	127.6	670	2944
Friction coefficient	0.4-0.6	0.2-0.5	0.01-0.04
Relative wear life	1		10000

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- http://picogeo.eu/

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ANGEL EVENTS

Weighing up the options for gallium oxide crystal growth

What are the pros and cons of producing β-Ga_2O_3 by the two most common techniques, the Czochralski method and edge-defined film-fed growth?

BY JANI JESENOVEC AND JOHN MCCLOY FROM WASHINGTON STATE UNIVERSITY

There's much excitement surrounding ultra-wide bandgap materials, such as Ga_2O_3, AlN and diamond. They are renowned for a very high intrinsic voltage breakdown field, which makes them exceptional candidates for handling high powers.

Within this family of semiconductors, interest in Ga_2O_3 is on an exponential trajectory. As well as its great potential for making incredibly small and efficient power-switching devices that trim thermal losses, it is attracting attention for the fabrication of deep-UV detectors that are transparent to visible wavelengths.

Image Credit: Jeffrey Jensen

For developers of all forms of Ga_2O_3 devices, a key decision is the choice of polytype. There are many to decide among, but arguably the most important of all is β-Ga_2O_3, the room-temperature stable phase. One of its most promising features is that it can be alloyed with Al_2O_3 to increase the bandgap and push the transmission window deeper into the UV.

Efforts at understanding the nature of β-Ga_2O_3 rely on the growth of high-quality material. This can be in the form of a bulk single crystal, or a thin film that is grown by one of many methods. Today, high quality single crystal films of β-Ga_2O_3 may be deposited by MOCVD, HVPE and MBE.

One of the merits of bulk β-Ga_2O_3 is that, unlike the other ultra-wide bandgap materials, it can be formed from the melt, using techniques such as the Czochralski crystal growth technique, which has been employed for the manufacture of silicon wafers for many years. Crystals of this oxide can also be produced by edge-defined film-fed growth, a technique employed for commercial production of β-Ga_2O_3. In addition, research is underway into the growth of β-Ga_2O_3 by other methods, such as the vertical Bridgman and optical float zone techniques.

In the remainder of this feature we shall review the progress made with the more common methodologies and detail insights provided by characterisation. Within this survey, we include a brief account of the contribution to this field by our team from the Institute of Materials Research at Washington State University.

Of the techniques we have mentioned for crystal growth, the two primary approaches – the Czochralski method and edge-defined film-fed growth – have much in common. They both involve pulling solid single crystals out of molten Ga_2O_3, held at temperatures above 1800 °C and housed in iridium metal crucibles. Ga_2O_3 produced by

the Czochralski method tends to be cylindrical, while that formed by edge-defined film-fed growth involves the use of iridium capillaries, which can draw the material into the desired shape.

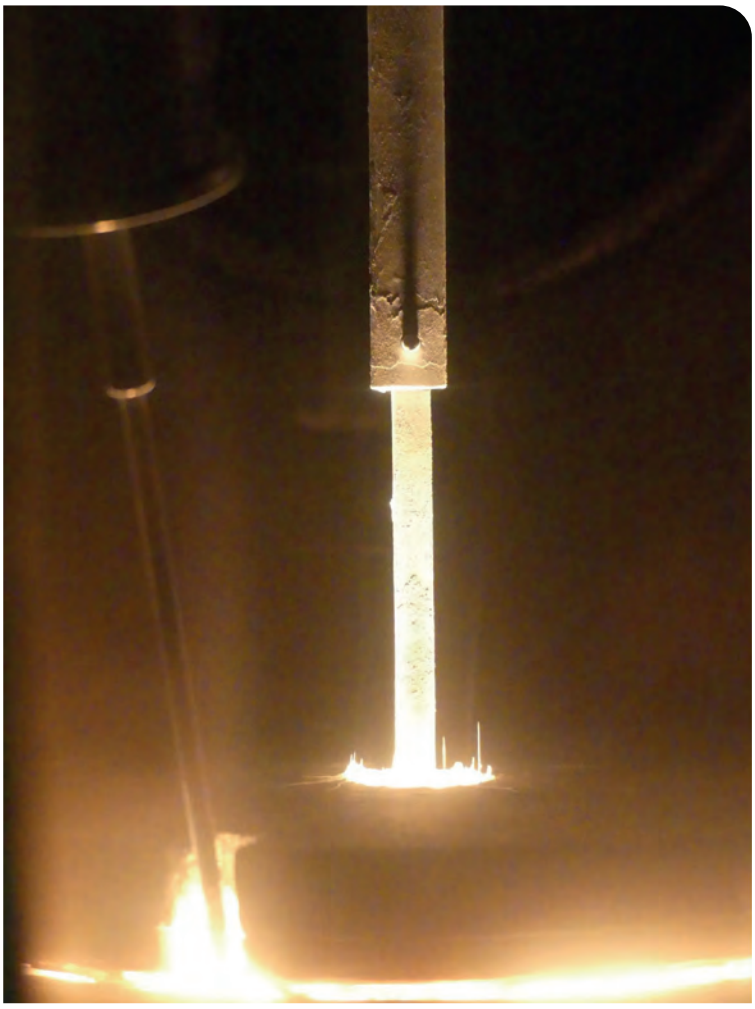
Pioneering β-Ga_2O_3 produced by the Czochralski method is a team at the Leibniz Institute for Crystal Growth, Germany. Commonly known as IKZ, this institute has demonstrated marked success, detailed in many publications and several patents.

Famous for producing β-Ga_2O_3 via edge-defined film-fed growth is Novel Crystal Technologies (NCT). This Japanese outfit, which manufactures and sells wafers of doped or un-doped β-Ga_2O_3, touts that crystals produced by this technique are superior to those made by the Czochralski method, due to the potential to produce very large wafers. However, edge-defined film-fed growth usually forms thin crystals, so the overall pulled volume is lower than that associated with the Czochralski method, which has the potential to scale and yield large cylindrical single crystals.

Delving into doping

For all semiconductors purity is critical. When small concentrations of other atoms are present, or defects added, this strongly affects the bulk properties. In the case of β-Ga_2O_3, there is the opportunity to intentionally replace the gallium that sits on its atomic site with other elements, via doping, to induce optical or electrical phenomena; and there is the threat that undoped β-Ga_2O_3 can be plagued with impurities. Common impurities in β-Ga_2O_3 produced by any method include silicon, iron, and chromium; iridium may also be introduced when crystals of this oxide are formed by the Czochralski method or edge-defined film-fed growth. Metallic impurities tend to originate from the precursor powders used in synthesis, or from the crucible that can contaminate the melt at high temperatures. Due to this, undoped β-Ga_2O_3 is referred to as 'unintentionally doped' material. Typically, this contains substantial background impurities, acting as dopants and enabling electrical conduction.

Intentional doping of β-Ga_2O_3, a topic undergoing much research, offers control over the electronic behaviour of this oxide. Material that is *n*-type, and thus dominated by electron conduction, may be formed by doping with silicon, germanium, tin, zirconium or hafnium. If electrically insulating behaviour is desired, appropriate dopants include iron, magnesium, zinc, nickel and copper. Realising *p*-type behaviour has proved far trickier. Some annealing experiments suggest marginal *p*-type behaviour may be realised due to hydrogen interaction, but this behaviour has not been observed in as-grown bulk crystals. Maybe this is not surprising, given that this difficulty has been observed in ZnO, another transparent semiconducting oxide. In the case of ZnO, this weakness has eventually limited the application of the material.



➤ Figure 1. Exterior view of insulation and the growth chamber as gallium oxide is pulled from the melt with the seed rod (centre), while temperature is monitored with a movable pyrometer (left).

A property that may pique the interest of many is photodarkening, which has been demonstrated in copper-doped β-Ga_2O_3 by the Institute of Materials Research at Washington State University. Uncommon in semiconductors, this novel effect is long-lived in copper-doped β-Ga_2O_3, with UV excitation causing a sample held at room-temperature to darken and remain in that state for weeks (see Figure 2). Note that heating accelerates the reversal of this darkening.

Growing pains

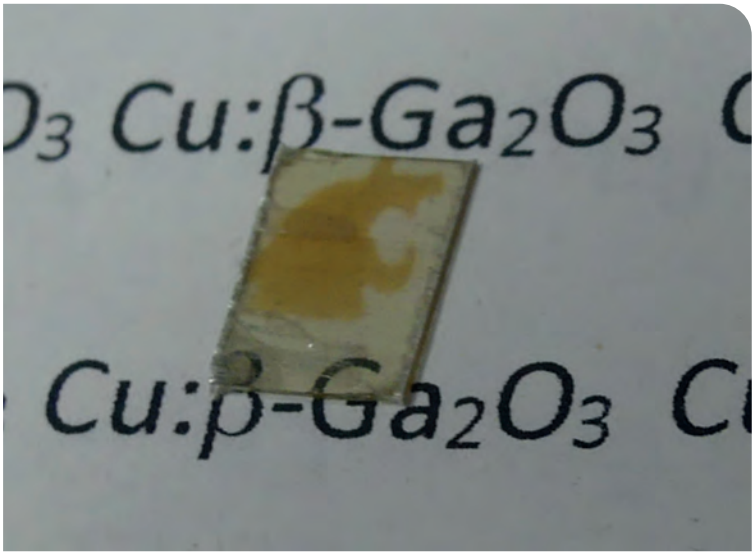
The progress that is been made with β-Ga_2O_3 crystal growth allows researchers to access substrates, deposit thin films on them, and investigate devices. But it does not follow that no further progress is required in crystal growth. Today, growth of β-Ga_2O_3 is very expensive, partly because iridium prices are very high, and the crucibles made from this metal weigh upwards of 0.5 kg.

Complicating matters is the decomposition of β-Ga_2O_3. As this oxide nears its melting temperature it tends to evaporate. To suppress this loss of material, there needs to be a partial oxygen environment in the growth chamber. However, that fix introduces other issues – iridium oxidizes and off-gases, or may become soluble in the melt in the

presence of oxygen at growth temperatures. Due to this, much costly iridium is lost in every growth simply through evaporation.

Progress may come through a switch to growth in other crucibles. With the vertical Bridgman technique it is possible to use a platinum-rhodium alloy. A popular choice for growing other semiconducting materials is molybdenum – but this is unlikely to yield much success, due to the rapid decomposition of β-Ga_2O_3, which oxidizes and destroys the crucible.

The team at IKZ continues to make advances with the Czochralski method, including the scaling of material to diameters of up to 5 cm and lengths of 6 – 8 cm. One of the issues that they face, along with anyone else that is trying to use this growth method, is a lack of stability that stems from the dopants. The addition of elements such as silicon, zirconium, hafnium and tin – added to induce conductivity – leads to absorption of radiation in the infrared, associated with excess electrons.



➤ Figure 2. A Washington State University cougar head logo photo-darkened through a mask onto a copper-doped sample with a 275 nm LED, where it remains for several weeks before returning gradually to the original homogenous colour.

Allied to the relatively low thermal conductivity of β-Ga_2O_3, this absorption is behind the retention of large amounts of heat during growth. That's far from ideal, as crystal growers rely on a highly tailored temperature gradient between the melting point of the material in the crucible in liquid form, and the temperature of the pulled crystal. Due to the near-IR absorption associated with free-carrier absorption, the melt-crystal interface can become unstable and form a corkscrew shape, rather than the typical cylinder. Corkscrews arise when the material dynamically forms geometries capable of dissipating heat. To prevent this from happening, the length of doped β-Ga_2O_3 crystals produced by the Czochralski method must be limited compared with their insulating or un-doped single-crystal siblings that do not have free-carrier absorption.

Several strategies have been employed to mitigate spiral growth of conductive β-Ga_2O_3. By turning to alloying with aluminium, we have improved crystal stability (see Figure 3).

Substrates obtained from crystals produced by the Czochralski method are typically (100) oriented. However, it's also possible to produce polished (010) and (001) samples. These crystallographic orientations are highly valued, due to the asymmetric repeating-lattice monoclinic structure of β-Ga_2O_3 that is behind electronic and optical properties, which are governed by the particular crystal orientation.

It is easier to grow conductive β-Ga_2O_3 by the edge-defined film-fed method. That's because the iridium capillaries force the single crystal to retain its shape when it is pulled. NCT applies this technique to its commercial production of tin-doped β-Ga_2O_3. The material that is produced by this method tends to have similar orientations to that of Czochralski crystals. However, the $(\bar{2}01)$ orientation is also available via edge-defined film-fed growth – this is much more difficult to obtain via the Czochralski method, due to the nature of this growth technique. The $(\bar{2}01)$ orientation has some technical challenges, with crystallographic twins forming in edge-defined film-fed growth. But these twins are not commonly seen in material made by the Czochralski method.

Options for characterisation

Within the scientific community, much effort has been devoted to characterising β-Ga_2O_3, with researchers undertaking electrical, optical, structural, and even magnetic measurements of this oxide. High-resolution rocking curve X-ray diffraction is widely used to analyse the structure of single-crystal β-Ga_2O_3, with the results supplied on commercial wafer specifications as a certificate of quality. These measurements often consider the (400) or (600) reflections of the crystal lattice, to determine whether there is any asymmetry in the material or knees to the curve. If these features appear in the curves, this reveals that the material is impaired with grain boundaries or twins, as well as a poor surface quality. For single-crystalline wafers and substrates, the full-width at half-maximum of the diffraction peaks ranges from 20 arcsec to 150 arcsec.

Other approaches are needed to uncover point defects, inclusions and inhomogeneity. A common tool for this is scanning or transmission electron microscopy, which may be used to study the atomic structure of samples, locate point defects and analyse inclusions and homogeneity.

Like many other semiconducting materials, the common approach for studying the surface roughness of bulk single crystals, prior to growing thin films upon them, is atomic force microscopy. This technique is incredibly insightful for assessing the impact on surface roughness resulting from polishing, chemical etching and annealing.

It is crucial to be able to determine material impurities in β-Ga_2O_3, because as well as leading to insulating or *n*-type conducting behaviour, these

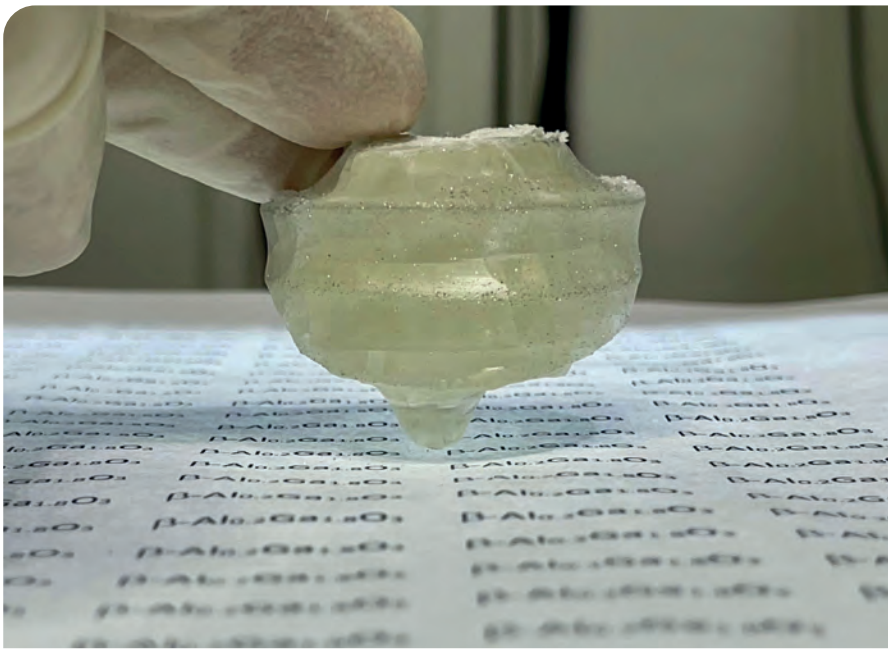
additions can lead to luminescence – that's the case for chromium and magnesium. Fortunately, many techniques can uncover impurities, including mass spectrometry and a number of optical emission spectroscopy techniques such as: glow discharge mass spectrometry; inductively coupled plasma mass spectrometry; secondary-ion mass spectrometry; and laser ablation, inductively coupled plasma mass spectrometry.

The latter of these has proven to be highly useful for studies of the spatial differences in β-Ga_2O_3 doping and inclusions. This optical technique involves focusing a laser on a sample's surface, using a beam width of typically around 10 μm. Due to the high intensity of the incident radiation, the laser beam ablates the surface or drills into it. The ablated material forms an extremely hot plasma, before ions are separated electromagnetically and counted, one by one, by a detector.

This laser-based technique has advantages over the common alternative, secondary-ion mass spectrometry, which requires expensive calibrated standards in the matrix being measured. The use of a laser enables rapid horizontal, vertical, and patterned measurements of substrates, can sample and identify inclusions, and is capable of detecting doping gradients. Another of its merits is that it can provide quantitative data, using simple geological standards to convert count rate into atoms per cm^3. And even if standards are not available, this technique offers a qualitative assessment of counts, which is still useful to determine the location of an inclusion and its composition.

Two complementary techniques for studying β-Ga_2O_3 are Raman microscopy and photoluminescence. Both offer insight into behaviour that's associated with doping and alloying, and facilitate forensic analysis of inhomogeneous materials. Additional information unveiled with Raman microscopy includes local vibrational analysis of inclusion phases, identification of lattice changes due to alloying, and help in ascertaining crystal orientation.

Light emission via photoluminescence can be obtained with some laser excitation Raman systems, or alternatively with a dedicated system. Detecting luminescence has much value, as it can be used to identify some impurities and dopants. Chromium, the active element in ruby laser crystals, acts as a very bright emitter in insulating β-Ga_2O_3 crystals; and the additional presence of magnesium can shift the chromium luminescence from red to orange.



➤ Figure 3. A gallium oxide Czochralski boule, alloyed with alumina to increase the bandgap.

Organic contaminants and certain other impurities, such as rare-earth elements, can also be identified by these techniques, which makes them excellent for comparing the surface of β-Ga_2O_3 crystals grown by a variety of approaches. For example, luminescence of chromium may be less intense in samples produced by the optical float zone process, because they don't use crucibles, which typically leach this element. If substrates produced by either the Czochralski method or edge-defined film-fed growth are to be used for any application, they must first be carefully analysed for inclusions.

When studying transparent materials, such as Ga_2O_3, optical characterization tends to employ transmission spectroscopy that utilizes light from the UV to the IR. This approach allows researchers to identify absorption from dopants and impurities, and to verify the presence of free-carrier absorption, indicative of *n*-type material.

For determining the electrical properties of β-Ga_2O_3 that is *n*-type or unintentionally doped, the use of the Hall effect is ideal, providing values of electron

One critical issue is *p*-type doping. The concern is that β-Ga_2O_3 will mirror ZnO, which lacked a bulk dopant to induce *p*-type behaviour. If that's the case, β-Ga_2O_3 may also be fundamentally incapable of high-mobility hole conduction.

volumetric concentration and mobility. Armed with this insight, one can assess the material's electrical conductivity. For insulating materials, a lack of carriers hampers the use of the Hall effect, so it may be better to use other methods to assess resistivity, such as impedance or current-voltage measurements.

To study impurities, defects, and their energetic location within the ultrawide bandgap, researchers can turn to electrical defect spectroscopy techniques, such as deep-level transient spectroscopy and thermoelectric effect spectroscopy. Complementing these are techniques such as thermoluminescence spectroscopy, allowing optical analysis of defects.

Meanwhile, when there's a need to determine how the concentration of defects varies with depth from the surface, one can turn to positron annihilation spectroscopy. This form of spectroscopy involves injecting positrons into the surface – they annihilate with electrons, with characteristics that depend on the open volume. Crucial information is revealed, especially associated with gallium vacancy formation in thin films or single-crystalline bulk samples.

Looking ahead

Over the last decade, much progress has been made in the growth of unintentionally doped and insulating β-Ga_2O_3 bulk substrates. Efforts at IKZ have led to significantly larger, higher-quality crystals using the Czochralski method, and progress has been realised by NCT using edge-defined film-fed growth. These technologies are now mature enough to provide production-quality substrates, which can provide a foundation for thin-film growth or serve in other applications.

However, all this success should not lead to complacency. Much more needs to be done, including advancing the growth of conductive β-Ga_2O_3 by the Czochralski method and addressing issues associated with the length of crystals produced by this technique. Efforts in academic laboratories are being directed at research into novel dopant and alloy behaviour, with many institutions and individuals pushing the material into new applications and discovering interesting phenomena.

One critical issue is *p*-type doping. The concern is that β-Ga_2O_3 will mirror ZnO, which lacked a bulk dopant to induce *p*-type behaviour. If that's the case, β-Ga_2O_3 may also be fundamentally incapable of high-mobility hole conduction. However, there's good reason for cautious optimism, given that some experiments have shown marginal success, with annealing inducing *p*-type behaviour. Given the great promise of β-Ga_2O_3, let's hope further success follows.

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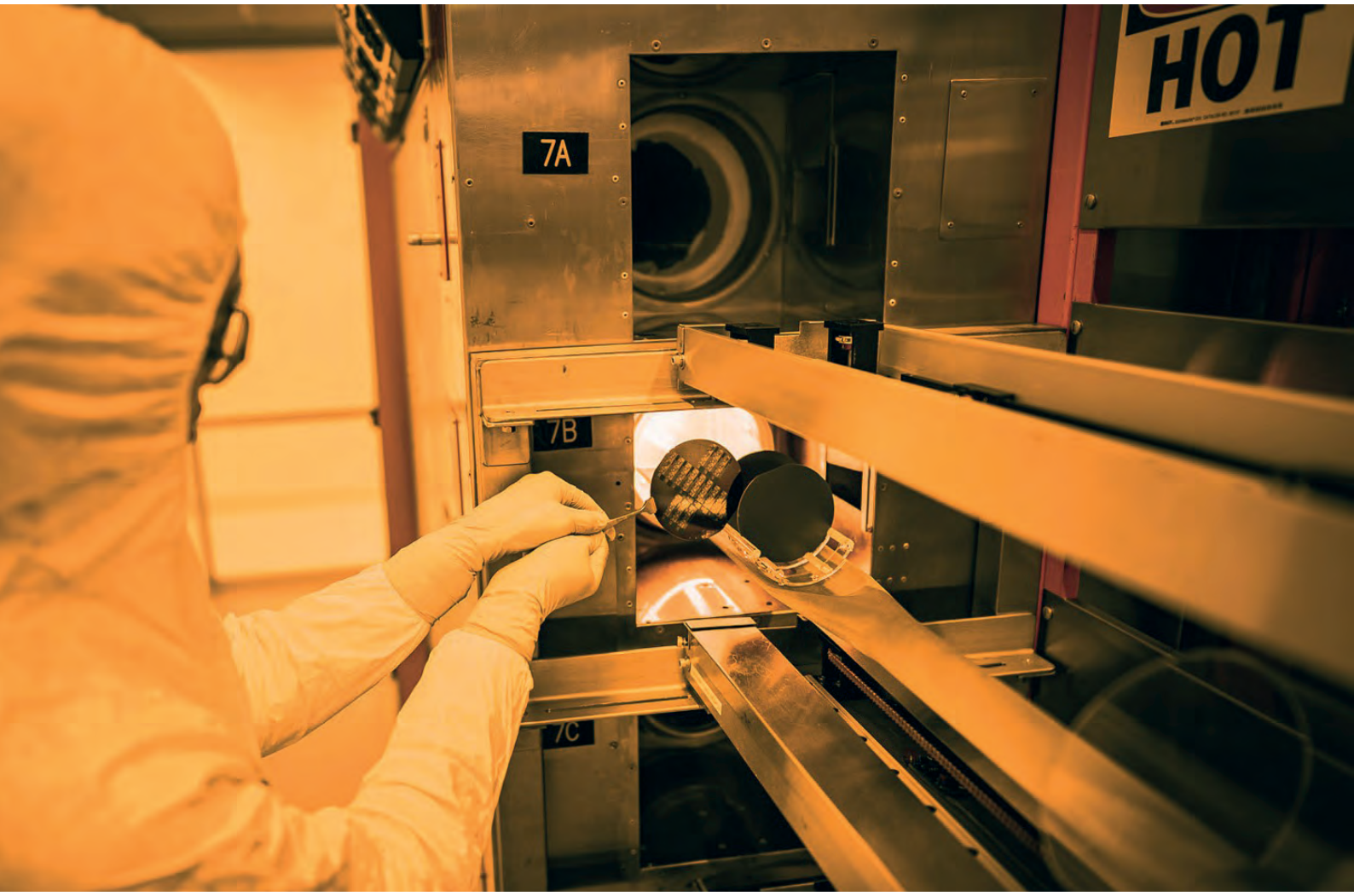


Quashing droop with cubic GaN

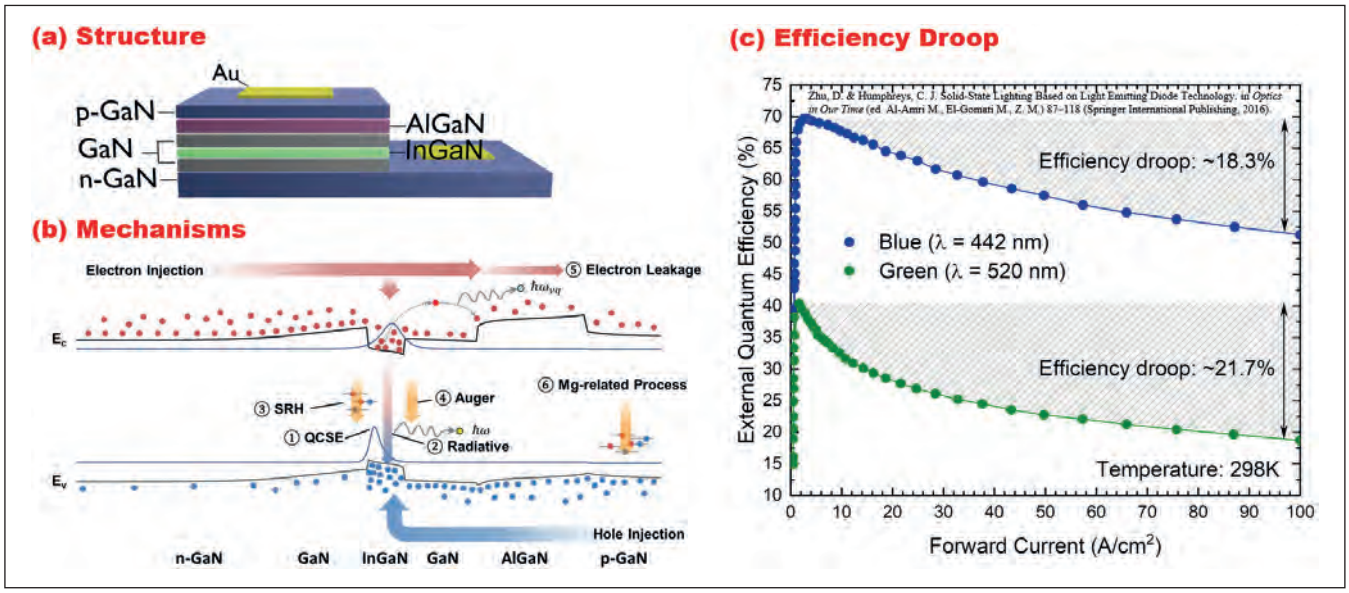
Cubic GaN combats droop through elimination of internal electric fields and a reduction in the effective hole mass

BY YI-CHIA TSAI, JEAN-PIERRE LEBURTON AND CAN BAYRAM FROM THE UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

1962 marked a significant milestone in LED development. That was the year that the late Nick Holonyak Jr. invented the world's first visible LED, emitting in the red, making the prediction that this class of device would go on to be the most efficient form of lighting ever created.

An important step towards this goal came three decades later, through the introduction of a practical blue-emitting source, based on InGaN. Since then it might feel that we are tantalisingly close to enjoying the ultimate form of solid-state lighting, involving colour mixing of efficient, direct-emitting red, green and blue sources. But this dream is yet to materialise, as a high-performance green LED is still elusive.

At first glance, this ultimate solution may not actually seem to be that important any more. After all, the world has now, by and large, ridden itself of the incandescent bulb, an inefficient, unreliable source that converted 90 percent of electricity into heat. But one should certainly not be complacent. According to the Global Lighting Challenge, lighting still accounts for 15 percent of the world's electricity consumption and 5 percent of all greenhouse gas emissions. And this situation is only expected to deteriorate, with research from Moira Zellner's group



at Northeastern University forecasting a tripling of the average household energy consumption for lighting over the next fifty years, due to population growth and an increase in housing size. Due to this, there is much urgency to transition to more-energy-efficient lighting, as this will play a key role in curbing carbon footprints.

At the heart of today's solid-state lightbulbs are a battalion of InGaN-based LEDs, each with an active region made of InGaN quantum wells (QWs), interlaced with GaN quantum barriers. This active region is sandwiched between *n*- and *p*-doped GaN layers. The other key ingredient in this heteroepitaxial stack is an AlGaN electron-blocking layer. Sitting between the active region and *p*-doped GaN, it is included to prevent electrons from spilling over into the *p*-type region (see Figure 1 for a diagram of the LED).

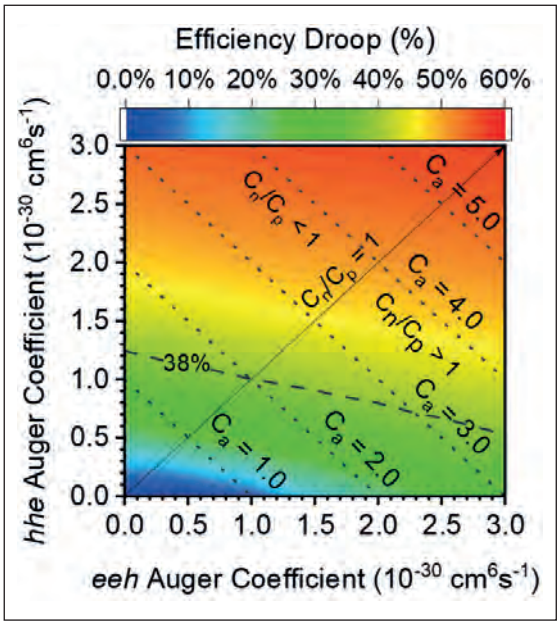
In this standard form of LED, which operates under forward bias, electrons and holes are driven towards the QW active region, where they recombine to emit light. However, this is a gross simplification of what is really taking place, with carrier transport actually governed by multiple processes, including the quantum-confined Stark effect (QCSE), radiative recombination, Shockley-Read-Hall recombination, Auger recombination, carrier leakage, and a number of magnesium-related processes (for an illustration of all these phenomena at play, see the bottom-left diagram of Figure 1).

The result of all these effects is efficiency droop, a malady behind the peaking of external quantum efficiency at low current densities (less than 35 A cm^{-2}) and its roll-off under high injection levels (see the right sub-figure of Figure 1). Droop is clearly highly undesirable, imposing a trade-off in traditional solid-state sources between the output power of the light source and its efficiency and cost.

LED droop: Inevitable or avoidable?

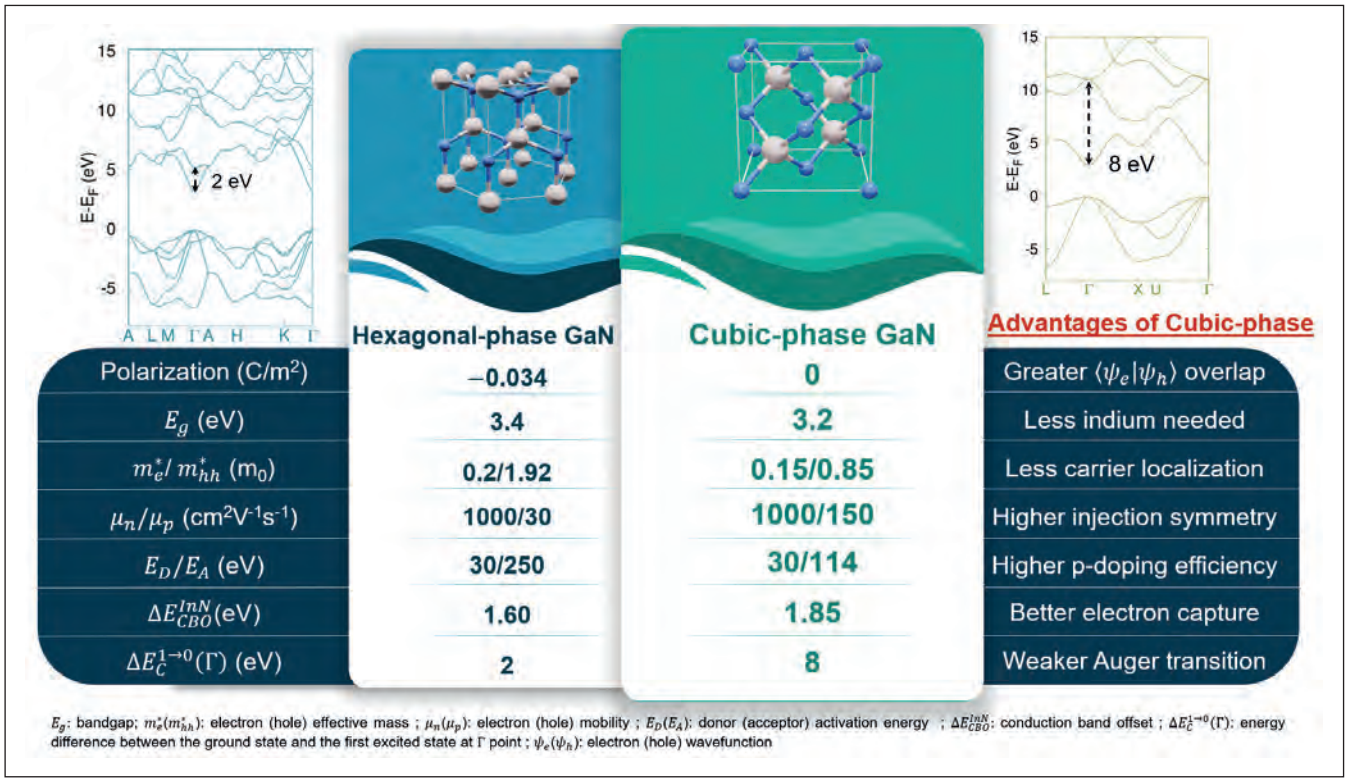
Much effort has been directed at uncovering the origin of efficiency droop in InGaN-based LEDs. Success is not easy, because it is challenging to isolate each non-radiative mechanism experimentally. Numerous culprits have been proposed – they include, but are not limited to, Auger recombination, carrier leakage, internal polarization and phase-space filling. However, none explains efficiency droop alone.

In some of the latest experimental works, hot-carrier emission from the active region of an InGaN-based LED strongly points to Auger recombination. But there are other experiments that have led researchers to attribute the mixture of mid-energy



➤ Figure 2. The efficiency droop as a function of *eeh* (C_n) and *hhe* (C_p) Auger coefficients under the current density of 200 A cm^{-2}. The ambipolar Auger coefficient (C_a), expressed in units of 2×10^{-30} cm^6s^{-1}, is shown as the dotted lines on the colour plot. Multiple solutions for (C_n, C_p) exist for an efficiency droop value.

➤ Figure 1. (a) An InGaN-based LED structure. (b) Competing mechanisms in an InGaN-based LED. (c) The efficiency droop in traditional blue and green LEDs.



➤ Figure 3. Tabulated hexagonal- and cubic-phase GaN parameters and the advantages of cubic-phase.

and high-energy peaks in the electron emission spectra to the coexistence of secondary Auger-electrons escaping the quantum wells and carrier leakage in InGaN-based LEDs.

Can theoretical studies clear up this matter? Well, not yet. Some simulations show that the Auger current outweighs the carrier-leakage current in InGaN-based LEDs, where phonon scattering, alloy scattering, and interface roughness scattering are proposed to explain a large Auger coefficient of 10^{-30} cm^6 s^{-1}. But this explanation is inconsistent with the low efficiency droop in GaAsP-based LEDs, which have similar Auger coefficients.

There are also simulations that point to carrier leakage. They show that efficiency droop and carrier leakage diminish when either: crystal growth is switched to non-/semi-polar substrates, there is an increase in barrier doping, or the electron-blocking layer is designed to have an internal polarization match to the substrate. Support for this view comes from remedies against efficiency droop that have been shown to trim carrier leakage. However, as effects on Auger recombination have not been investigated simultaneously, there is the possibility of misinterpretation of the inherent cause of droop. To try and get to the bottom of this matter, our team at the University of Illinois at Urbana-Champaign developed a new quantum-corrected drift-diffusion LED simulator called the Open Boundary Quantum LED Simulator, shortened to simply OBQ-LEDsim.

Our simulator has enabled us to demystify the interplay between Auger recombination, carrier leakage, and internal polarization, as well as their respective contributions to efficiency droop. It is important to note that, compared with conventional LED simulators, OBQ-LEDsim solves the Schrödinger equation by variational principles, where the ground-state wavefunction vanishes at infinity. While perfectly consistent with the conventional k·p method, our variational approach has the advantage of removing artificial boundaries between the quantum well and classical continuum. This provides high-accuracy modelling of both the inter-QW carrier interaction and QW carriers at arbitrary positions outside of the wells. Thanks to this capability, our OBQ-LEDsim model captures non-radiative processes outside the active region that potentially contribute to efficiency degradation.

A common, simple way to describe the internal quantum efficiency of an LED is the ABC model. That assumes carrier symmetry – i.e. the electron density is the same as the hole density. Under this assumption, the measured Auger coefficient, called the ambipolar Auger coefficient (C_a), has a value equal to the sum of the Auger coefficients for the electron-electron-hole (*eeh*) and the hole-hole-electron (*hhe*) channels ($C_a = C_n + C_p$).

Applying this ABC model to piezoelectric materials such as InGaN is questionable, because the carrier symmetry is plagued by internal polarization. Our investigations have revealed that the major culprit of the efficiency droop is the coexistence of a strong internal polarization and a large hole effective mass. The internal polarization leads to a separation of the electron-hole wavefunction, and in turn promotes carrier localization, which degrades radiative recombination but enhances the Auger process.

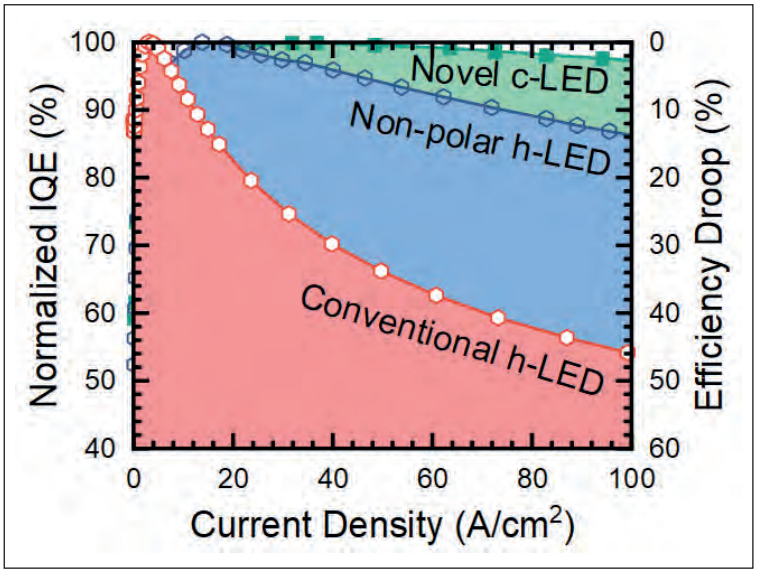
Compounding the influence of strong internal polarization, there is a large hole effective mass, further enhancing hole localization in the quantum wells. The upshot is that there is a higher hole density than electron density, and thus a larger *hhe* Auger current compared with the *eeh* Auger current. With these factors at play, the Auger electron-hole asymmetry value – that is, the ratio of *eeh* to *hhe* Auger coefficients (C_n/C_p) – plays a critical role in both the efficiency droop and in quantifying the ambipolar Auger coefficient. Unfortunately, there is a tendency to ignore Auger electron-hole asymmetry in experiments and simulations.

When the Auger electron-hole asymmetry increases, it quenches *hhe* Auger recombination and enhances *eeh* Auger recombination. Calculations by our team suggest that efficiency droop diminishes from 48 percent to 25 percent as the value for the Auger electron-hole asymmetry increases from 0 to infinity for a current density of 200 A cm^{-2} and an ambipolar Auger coefficient of 2×10^{-30} cm^6 s^{-1}. This decrease in droop indicates that the *hhe* Auger process is the dominant Auger recombination channel (see Figure 2).

We attribute this dominance to electrons being less localized than holes in the quantum wells. It is the internal polarization effects, leading to asymmetric carrier distributions that are behind the strong dependence of efficiency droop on the Auger electron-hole asymmetry. Since ambipolar Auger coefficients are commonly extracted via the ABC model that assumes carrier symmetry, the extracted ambipolar Auger coefficients are also subject to carrier asymmetry (i.e. Auger electron-hole asymmetry).

To highlight the influence of Auger electron-hole asymmetry on ambipolar Auger coefficients, we have included in Figure 2 a dashed line that indicates an efficiency droop of 38 percent. We selected this value as a reference, because it assumes Auger electron-hole symmetry and an ambipolar Auger coefficient of 2×10^{-30} cm^6 s^{-1}. From the plot, it is clear that there are multiple values of *eeh* and *hhe* Auger coefficients that correspond to the same efficiency droop. For instance, for Auger electron-hole asymmetry values that are less than unity, the ambipolar Auger coefficient is smaller than that obtained assuming Auger electron-hole symmetry. Meanwhile, when the Auger electron-hole asymmetry value is equal to zero, the smallest ambipolar Auger coefficient is 1.24×10^{-30} cm^6 s^{-1}; when the value for the Auger electron-hole asymmetry exceeds 1, the ambipolar Auger coefficient is larger than that obtained assuming Auger electron-hole symmetry; and when the Auger electron-hole asymmetry value is set to infinity, the largest ambipolar Auger coefficient is 5.20×10^{-30} cm^6 s^{-1}.

According to first-principles calculations, the actual value for the Auger electron–hole asymmetry is around 0.4. Using this figure, we found that the ambipolar Auger coefficient obtained when assuming Auger electron–hole symmetry – consistent with the common, but simple ABC model – is overestimated by as much as 62 percent.

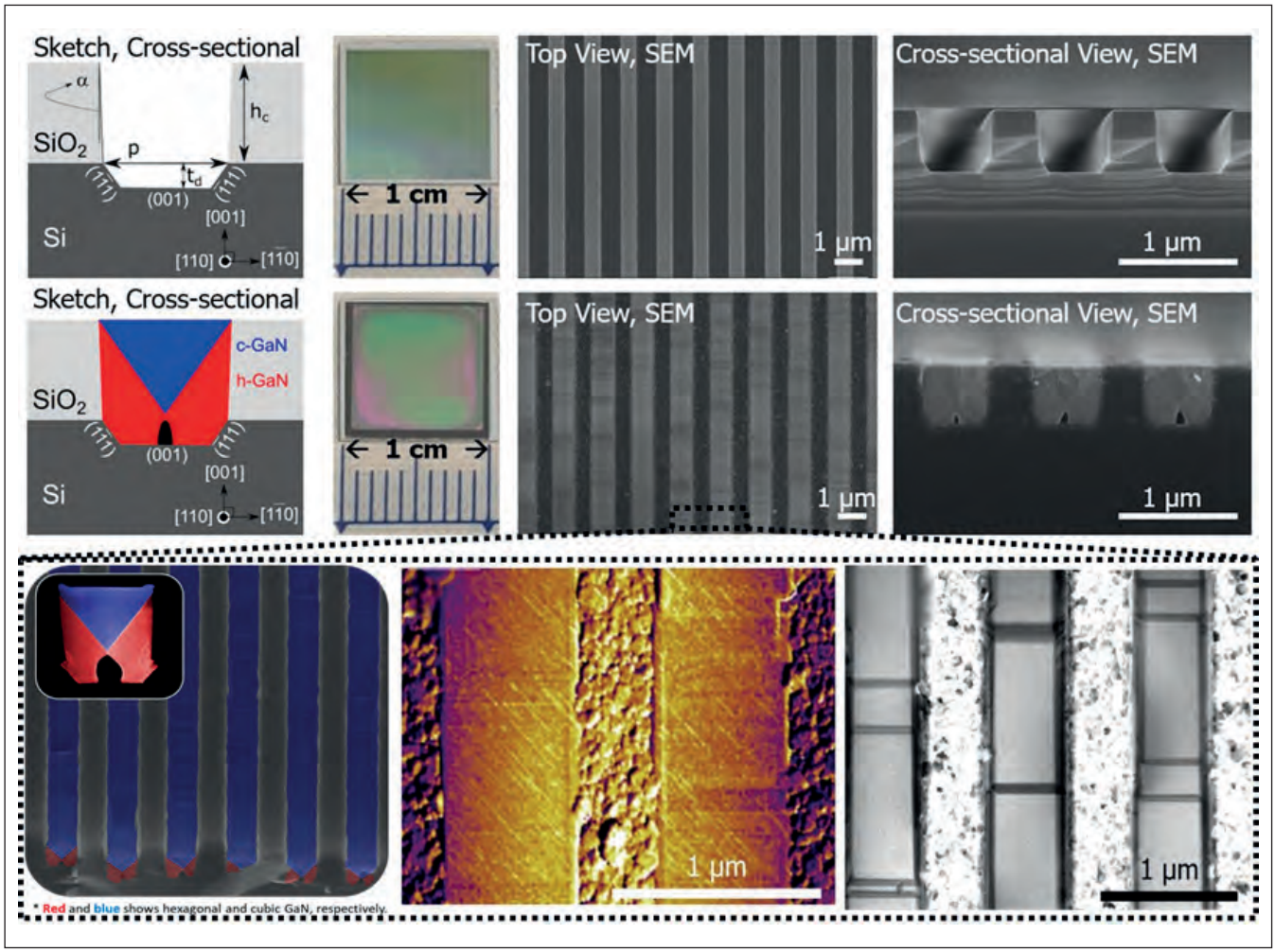


➤ Figure 4. Normalized internal quantum efficiency (IQE) (left y-axis) and efficiency droop (right y-axis) as a function of current density. Red open hexagons and blue hollow hexagons refer to the traditional and non-polar hexagonal-phase LEDs, whereas green solid squares represent the novel cubic-phase LED.

Next phase in LEDs

Our calculations suggest that the coexistence of internal polarization and a large hole effective mass offers an explanation as to why the Auger recombination in traditional hexagonal-phase InGaN-based LEDs is far, far larger than that in GaAsP-based LEDs, despite their similar Auger coefficients. Note that it is not possible to avert the coexistence of internal polarization and the large hole effective mass by modifying the device design or changing the crystal orientation in InGaN-based LEDs, so

One should be aware that as well as the LED-related promise of cubic-phase III-nitrides, they have much to offer in other distinguished applications. This class of nitride has great potential in polarization-free photonics, room-temperature ferromagnetism, high-temperature spintronics, and it could also serve in normally-off transistors and single-photon emitters



➤ Figure 5. Cubic GaN epitaxy on large-area (~1 cm^2) U-grooved silicon (100) dies is demonstrated. (Top row) U-grooved silicon (100) and (middle row) cubic GaN atop. (From left to right) cross-sectional sketches, top-view photographs, top-view scanning electron microscopy (SEM) images and cross-sectional view SEM images. (Bottom row) cubic GaN structural characterization. (From left to right) phase mapping, tapping-mode atomic-force microscopy and bright-field, top-view, scanning tunnelling electron microscopy (STEM) images. The plan-view STEM reveals no threading dislocations or other types of dislocations on the cubic GaN surface. Stacking faults with a density of 3.27 ± 0.18 x 10^4 cm^{-1} are observed.

these are limited levers to addressing efficiency droop. Our view is that there is more to be gained by switching to the cubic phase, which allows the design of InGaN-based LEDs that can combat droop, thanks to the absence of internal polarization and small hole effective masses (see Figure 3).

There are many other attributes associated with the cubic-phase of InGaN-based LEDs. Compared to hexagonal-phase GaN, this form of the LED triples hole mobility, halves the magnesium activation energy, offers a higher quantum barrier to the InGaN/GaN quantum wells, and is expected to have a smaller Auger coefficient. The cubic phase is also blessed with a very favourable band structure: there are relatively few energy states close to the conduction band minimum and the valence band maximum, and the energy difference between the first and second conduction bands at the Γ point is at least 8 eV (see Figure 3). The culmination of all these strengths should allow the cubic GaN-based LED to impede direct and indirect Auger transitions, leading to a smaller Auger coefficient compared with hexagonal cousins.

We have simulated three different forms of InGaN-based LED – conventional hexagonal, non-polar hexagonal, and cubic-phase – because that enables us to single out the effect of internal polarization from the influence of a large hole effective mass on the efficiency droop (see Figure 4). Our results show that in a traditional hexagonal-phase LED driven at 100 A cm^{-2}, droop is as high as 46 percent, due to the coexistence of a strong internal polarization and a large hole effective mass in the structure.

A significant improvement comes from switching to the non-polar hexagonal-phase, with the crystal orientation perpendicular to the [0001] internal polarization vector. LEDs with this geometry quench internal polarization and have a similar value for hole effective mass to a conventional InGaN-based LED.

These changes have led to a reduction in efficiency droop at 100 A cm^{-2} to 13 percent, due to enhanced overlap of the electron-hole wavefunction and carrier delocalization.

Even greater success comes from the move to the cubic phase. With this class of InGaN-based LED, droop is quashed to just 3 percent, with the reduction in the carrier effective masses delocalizing electrons and holes, and promoting band-to-band radiative recombination. We attribute the minimal droop to the suppression of the internal polarization and a lowering of the hole effective mass – we have assumed the Auger coefficients don't change. By drawing on our insights, we anticipate that the LED community will invest in cubic-phase InGaN-based LEDs, which will give the green light to a revolution in solid-state lighting.

Final thoughts

Our work follows the footsteps of researchers in the 1990s. Back then efforts focused on direct deposition on cubic substrates, such as GaAs, silicon (100), 3C-SiC and MgO. These foundations plagued cubic GaN with: incredibly high levels of defectivity, which were well beyond 10^{10} cm^{-2}; structural metastability, such as phase-mixing; and chemical metastability, which included a tendency toward spinodal decomposition. There were also issues arising for chemical incompatibility, such as that with GaAs. Given all these challenges, it's hardly surprising that cubic-phase InGaN-based LEDs have remained largely unexplored.

Recently, we broke new ground by inventing a novel method for cubic-phase GaN synthesis. Our success draws on the equivalence of the *h*-crystal <0001> direction and the *c*-crystal <111> direction. We discovered that if two *h*-phase growth fronts merge within a degree of around 110° – that is the angle between the two Ga-N bonds in hexagonal tetrahedral bonding – a *c*-phase will form. Building on this finding, we have just shown that it's possible to form areas of cubic GaN with a size of a square centimetre or so via growth on nano-patterned, CMOS-compatible silicon (100) substrates. This enables us to now explore the opportunity for cubic-phase LEDs to address droop and green gap problems in conventional and advanced forms of solid-state lighting.

One should be aware that as well as the LED-related promise of cubic-phase III-nitrides, they have much to offer in other distinguished applications. This class of nitride has great potential in polarization-free photonics, room-temperature ferromagnetism, high-temperature spintronics. It could also serve in normally off transistors and single-photon emitters. So, in years to come, we may look back on 2022 as the year that started a new, important phase in III-nitrides.

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HVPE offers a new route to high-quality AlGaN

AlGaN with a vast range of compositions can now be realised by HVPE

ENGINEERS from SCOICS, Japan, claim to have broken new ground by using HVPE to produce high-quality AlGaN layers that span almost all compositions.

By applying growth conditions that enhance etching and suppress parasitic reactions, this team avoids severe surface deterioration, which can arise through microstructural inclusions and the formation of hillocks.

➤ Optimised HVPE forms high-quality AlGaN on a GaN template.

The ability to rapidly grow thick layers of AlGaN promises to improve the production process for a number of devices. For example, the productivity of UV LEDs and lasers emitting in the UV, violet and blue could be enhanced by growing much of the device on GaN or AlN templates coated with thick layers of *n*-type AlGaN, added by HVPE.

What's more, SCIOCS technology could open the door to relaxed, *n*-type, free-standing AlGaN substrates. This could slash the substantial series resistance in UV LEDs and lasers, stemming from the use of *n*-type AlGaN cladding layers that are very thin, in order to avoid issues associated with the critical thickness. Ensuring a far lower series resistance would deliver a tremendous hike in the output power of UV LEDs and enable CW operation of UV lasers, thanks to suppressed self-heating.

Free-standing AlGaN substrates could also aid wide bandgap HEMTs. This foundation could quash unwanted impurities and address issues associated with device instability.

Note that it's not possible to reach the growth rates realized by HVPE by simply accelerating MOCVD. The latter technique, widely employed throughout the compound semiconductor industry for chip production, is limited to around 1 μm/hr. Higher growth rates would fail to suppress the vapour-phase reaction, even under low reactor pressures. The success by SCIOS has drawn on its previous breakthroughs, including the growth of highly pure, highly uniform GaN layers by HVPE. However, using HVPE to extend the growth from GaN to AlGaN is far from easy, according to team spokesman Hajime Fujikura, with efforts stymied by rather complicated chemical reactions. "One needs a huge number of growth trials to reach good results."

Another barrier to success is the lack of standardisation of HVPE systems. "HVPE systems are completely different from one another," remarked Fujikura, "so it is very difficult to reproduce HVPE growth results by reading papers from other groups."

Fujikura believes that the foundation behind the team's success is the HVPE machine and its accompanying growth technology for producing free-standing GaN, using extreme gas flow-control. "This excellent growth tool is also very helpful for developing good AlGaN growth conditions."

The engineers from SCIOCS developed their AlGaN technology by studying the growth of this ternary on three different templates: 4 μm-thick GaN on flat sapphire; 0.5 μm-thick AlN on flat sapphire; and 0.5 μm-thick AlN on patterned sapphire, which featured an array of 400 nm-high cones.

Using aluminium, gallium and HCl as starting materials, Fujikura and colleagues produced a range of samples with aluminium fractions spanning less than 10 percent to more than 90 percent, at growth rates typically varying from around 0.1 μm min^{-1} to 1 μm min^{-1}. During the study the team found that to ensure a high-quality surface, they had to use etching to supress parasitic reactions. These unwanted reactions might originate from parasitically crystallised AlGaN on the HVPE nozzle and the reactor wall, or from direct nucleation of irregular microcrystals on the epitaxial surface.

One of the highlights of the work by the team is a 10 μm-thick, fully-relaxed $Al_{0.17}Ga_{0.83}N$ layer with a mirror-like surface, grown on the GaN-on-sapphire template. Its crystal quality is not severely deteriorated by heteroepitaxy, according to X-ray diffraction. Another triumph is a smooth, high-quality layer of $Al_{0.67}Ga_{0.33}N$, grown on the AlN-on-patterned-sapphire template – this is a promising foundation for realizing UV LEDs with enhanced light extraction.

Fujikura says that the next target is a thick AlGaN layer, which could be used to make free-standing substrates.

REFERENCE
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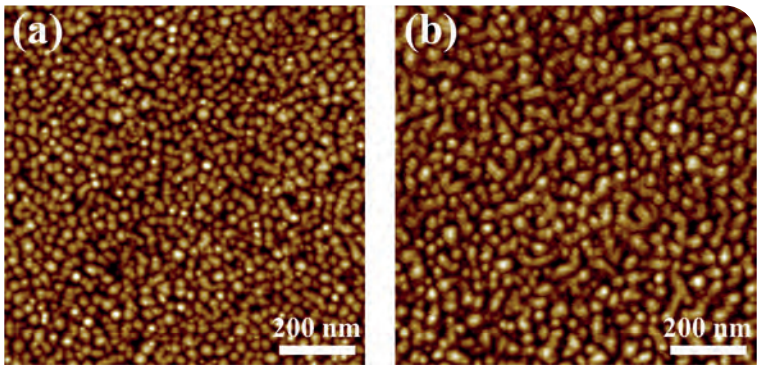
Optimising fabrication of the GaN-on-silicon HEMT

AlN layers with delayed coalescence provide a great foundation for realising GaN-on-silicon HEMTs with minimal RF loss

THE GaN-on-silicon HEMT has its pros and cons: it majors on the use of large, low-cost substrates, and the opportunity to process epiwafers into devices in existing CMOS foundries; but it can suffer from RF loss, stemming from residual metallic atoms diffusing into the substrate during MOCVD growth of the AlN seed layer, which is added to prevent gallium-silicon melt-back at high temperatures.

Fortunately, RF loss can now be addressed in an efficient manner, thanks to a team from China that has developed a CVD process for forming templates that feature an AlN layer with delayed coalescence.



➤ Atomic force microscopy reveals that lower RF powers during the growth of AlN lead to larger nuclei.

According to this team – a partnership between researchers at Peking University, Jimei University and the Collaborative Innovation Centre of Quantum Matter – their approach is more favourable than the more common one for ensuring that devices don't suffer from substantial RF loss, involving the cleaning and baking of an MOCVD reactor prior to GaN growth. The engineers argue that by introducing an AlN layer that's grown *ex situ* by PVD, it is possible to increase the productivity of GaN-on-silicon MOCVD growth.

The approach of using *ex situ* growth on sapphire is very mature, with sputtered and PVD growth of AlN on sapphire applied to the fabrication of LEDs. However, it is challenging to realise high-quality, crack-free layers of GaN on silicon substrates with a sputtered AlN interlayer. Compared to *in situ* growth of GaN on AlN, the defect densities in the GaN that's grown on *ex situ* sputtered AlN is an order-of-magnitude higher, and the surface morphology rough, due to the three-dimensional growth mode. To address the shortcomings of growth on silicon, the team from China turned to PVD, first depositing large AlN nuclei with a low density, before adding GaN via a three-dimensional growth mode that delayed coalescence, key to realising a crack-free epilayer.

Trials to establish a good process involved PVD of a 200 nm-thick AlN layer on 2-inch silicon (111), using an RF power of 200 W or 500 W at 1000 °C, followed by transfer of these samples to an Aixtron close-coupled-showerhead MOCVD reactor, employed for growing buffer-free GaN with a total thickness of 1.5 μm. Structures were formed using both three-dimensional and two-dimensional growth modes, realised using low and high V-III ratios, respectively.

The only crack-free sample, which also had the best crystal quality according to X-ray diffraction, came from the use of a low RF power in the growth of AlN by PVD, followed by the combination of three-dimensional and two-dimensional growth, with a coalescence thickness of 1200 nm.

Atomic force microscopy revealed that reducing the RF power from 500 W to 200 W increased the average size of the AlN nuclei from 20-30 nm to 30-50 nm, and halved their density.

The team argued that a high coalescence thickness is crucial for managing the stress in the GaN wafer, and preventing cracking. When there is fast coalescence, leading to a low coalescence thickness, there is insufficient compressive stress to compensate for the tensile strain comes that stems from the thermal mismatch between GaN and silicon during cooling.

Spokesman for the team, Xuelin Yang from Peking University, told *Compound Semiconductor* that further investigations are needed to uncover the optimal conditions for delayed coalescence growth, with efforts needing to consider a greater range of powers for the PVD process and alternative III-V ratios.

Yang thinks that increasing the coalescence thickness and/or the total thickness will improve the crystal quality of GaN. The team measured an RF loss of 0.2 dB mm^{-1} at 10 GHz, using transmission lines in a coplanar waveguide. This loss is said to be amongst the lowest values reported for GaN-on-silicon.

Targets for the team are to further investigate optimal growth conditions, so that they can realise thicker GaN films with better quality, and to grow AlGaN/GaN heterostructures for the fabrication of HEMT structures.

REFERENCE
➤ D. Liu *et al.* Appl. Phys. Express **15** 081001 (2022)

Co-doping promises ultra-efficient white Ga_2O_3 LEDs

Ga_2O_3 LEDs with rare-earth ions have a high colour rendering index while avoiding the losses associated with the Stokes shift

THE TREMENDOUS SUCCESS of today's white LEDs should not obscure their weaknesses. The common architecture, the pumping of a yellow phosphor with a blue-emitting chip, leads to several drawbacks, including a low colour-rendering index, a Stokes energy-converting loss and reduced thermal stability.

Switching from phosphors to rare-earth ions should eradicate these weaknesses, with recent success on this front reported by a team from Saga University. It is pioneering Ga_2O_3 LEDs that are co-doped with tantalum, europium and erbium ions.

Spokesman for the team, Qixin Guo, told *Compound Semiconductor* that the nature of the energy transfer mechanism in their co-doped, gallium oxide LEDs, which colour-mix emission from the red, green and blue, requires further investigation. "However, there are no losses due to the Stokes shift."

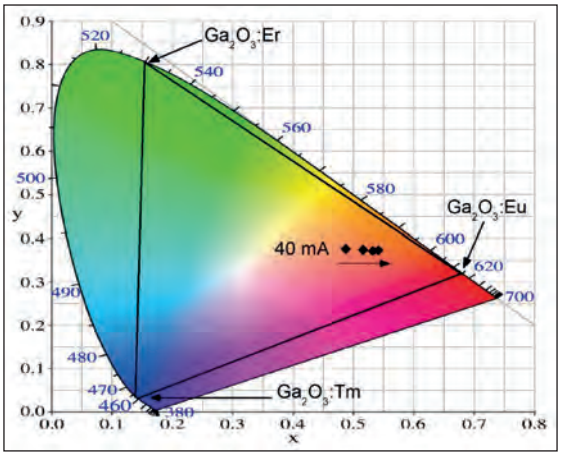
The team's latest emitters build on previous efforts at developing Ga_2O_3 LEDs with rare-earth ions. Back in 2021, Guo and co-workers reported a white-emitting LED containing a vertical stack of 150 periods, comprising films of Ga_2O_3 doped with either tantalum, europium or erbium.

As a complicated deposition process is required to produce an LED with so many layers, the team has moved on to investigate the feasibility of colour-tuneable LEDs based on co-doped tantalum, erbium and europium. Their device, formed by uniting co-doped Ga_2O_3 with a *p*-type GaAs heterostructure, has a threshold voltage of around 9 V and emits coloured electroluminescence.

To produce their devices, Guo and co-workers employed a pulsed laser deposition tool to grow a Ga_2O_3 film that is co-doped with tantalum, erbium or europium on *p*-type GaAs (111). For this process they used a substrate temperature of 500 °C, a growth pressure of 0.1 Pa, an oxygen atmosphere, a growth time of 3 hours, and a distance between the substrate and the target of 40 nm.

"Laser deposition is suitable for fundamental research," remarked Guo, but added that MOCVD offers the best method for mass production.

Scrutinising their LED structure with X-ray diffraction and Raman spectroscopy revealed that the co-doped Ga_2O_3 film is polycrystalline, and suitable for producing an LED.



➤ Tantalum, erbium and europium ions produce emission at around 460 nm, 530 nm and 610 nm, respectively. That makes this threesome a great combination for producing a white LED.

Measurements of the device, made by sputtering a 250 nm-thick film of ITO on the surface of Ga_2O_3 and adding a gold electrode to the backside of the wafer by electron-beam evaporation, showed that no emission is observed under reverse bias. Its absence indicates that device operation requires simultaneous injection of electrons and holes.

The combination of the tantalum, erbium and europium ions – said by Guo to be the optimal dopants for making a white LED – produces sharp emission peaks at around 460 nm, 530 nm and 610 nm, respectively. This led to bright, uniform pink light that gradually shifts in colour with drive current.

According to the team, white light can be realised with the existing combination of rare-earth ions by fine-tuning the doping concentrations of tantalum, erbium and europium.

One of the strengths of the co-doped Ga_2O_3 LED is that its emission wavelength does not change with the ambient temperature.

Guo and co-workers are still to investigate the efficiency and lifetime of their LEDs. Neither, though, are next on the agenda. Instead, efforts are now going to be directed at low-temperature photoluminescence measurements, to reveal the energy transfer mechanism with co-doped gallium oxide films.

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➤ Y. Huang *et al.* Appl. Phys. Express **15** 081005 (2022)

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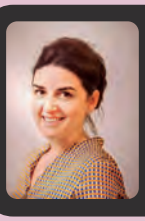

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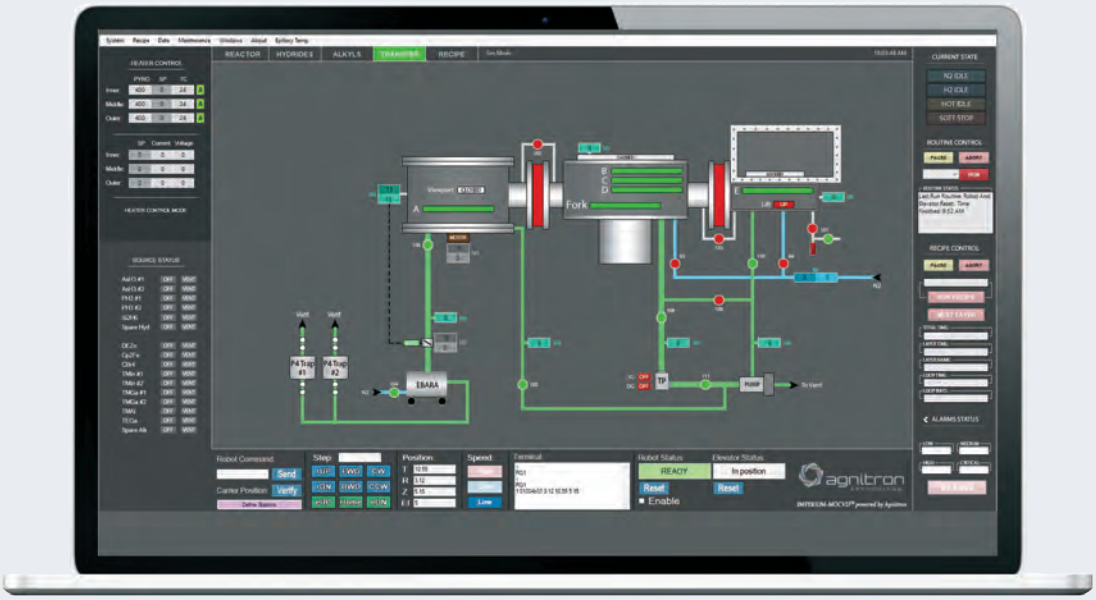

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