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News, Analysis, Features, Editorial View, Research Review and much more

Revolutionising microLED displays

Populating silicon wafers with blue-emitting nanowires and colour-converting quantum dots could transform displays

GaN transistors: Fighting for IP

While accusations fly of a lack of manufacturing know-how, what really matters in an IP war is the fine print in the patents

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VIEWPOINT

By Richard Stevenson, Editor

The devil is in the detail

There's no doubt that the temperature is rising in the GaN power electronics industry. And it's not just a result of companies going toe-to-toe with one another to win sales. Accusations are also flying around, with EPC suing Innoscience for theft of its IP.

Both of the sides in this dispute fired their first shots earlier this summer. As well as claiming that Innoscience is using stolen IP in its 100 V and 650 V products, EPC is accusing the Chinese chipmaker of poaching two of its employees. These hires, said to be appointed as CTO and Head of Sales and Marketing, are alleged to be behind the launch of copycat products.

Innoscience is not taking these charges lying down. Instead, it's fighting back, claiming that after conducting a thorough analysis, it found no grounds for infringement. When responding to the fabless Californian firm, Innoscience took the opportunity to boast about its internal production capacity, in what could be seen as a politically correct variant of the infamous insult 'real men have fabs'.

Whilst going on the offensive may make these two adversaries feel better about themselves, what really matters in this dispute are the claims and counterclaims made in court. There, the devil will be in the detail, with both sides arguing over what constitutes a significant difference in device architecture.

Anyone wanting to forecast what might lie ahead needs a good understanding of the intricacies of the design of GaN transistors, and the processes used to make them. They also need to try and make an assessment from a neutral standpoint, rather than taking sides.

Offering all this and more is David Radulescu, a leading patent litigator with a great deal of relevant expertise, acquired from working on many cases associated with GaN-based LEDs. As well as picking out the important details, Radulescu sees the big picture, understanding that a variety of factors come into play in these battles.

The court will consider just one form of normally-off transistor, featuring a *p*-doped (Al)GaN layer under the gate. Arguments will focus on the forming of the *p*-type doping in this layer, as well as the shape of the gate (details of possible differences are given on pages 14 and 15).

Which party wins will not just depend on the robustness of its patents. The quality of its legal team also matters, along with what budget they have and the strategy that's taken.

If you that have been in this industry for a while, you may feel a sense of déjà-vu. After all, plenty of court cases were fought over IP associated with the GaN LED. After paying out plenty on legal fees, many chipmakers went on to establish cross-licenses to navigate through the storm. Will history repeat itself? Who knows – but I wouldn't be surprised if it did.

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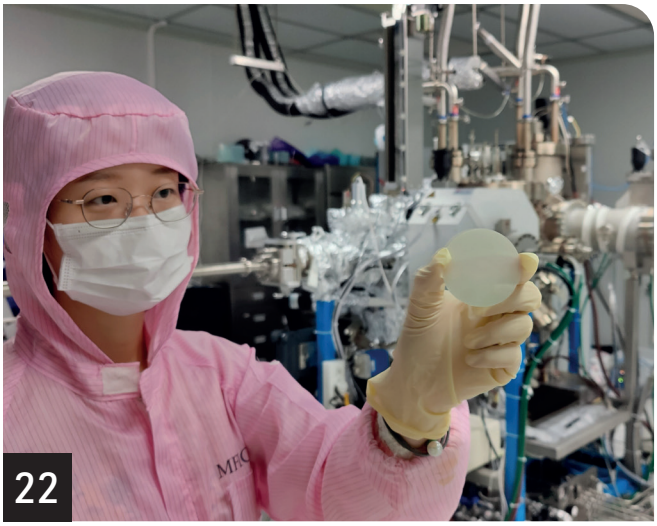

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Editor Richard Stevenson
richardstevenson@angelbc.com
+44 (0)1291 629640

News Editor Christine Evans-Pughe
christine.evans-pughe@angelbc.com

Design & Production Manager
Mitch Gaynor
mitch.gaynor@angelbc.com
+44 (0)1923 690214

Director of Logistics Sharon Cowley
sharon.cowley@angelbc.com
+44 (0)1923 690200

Senior Sales Executive
Jacob Caulfield
jacob.caulfield@angelbc.com
+44 (0)2476 718979

Marketing & Logistics Executive
Eve O'Sullivan
+44 (0)2476 823 123
eve.osullivan@angelbc.com

Circulation
Scott Adams
scott.adams@angelbc.com

Publisher Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

USA Representatives
Brun Media
Janice Jenkins
jjenkins@brunmedia.com
+1 724-929-3550

Tom Brun
tbrun@brunmedia.com
+1 724 539-2404

Chief Executive Officer
Sukhi Bhadal
sukhi.bhadal@angelbc.com
+44 (0)2476 718970

Chief Technical Officer
Scott Adams
scott.adams@angelbc.com
+44 (0)2476 718970

Directors
Jackie Cannon, Sharon Cowley

Published by
Angel Business Communications Ltd
6 Bow Court, Fletchworth Gate,
Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
E: info@angelbc.com

Indie Semiconductor buys Exalos AG

US-based autotech firm acquires Swiss photonics specialist

INDIE SEMICONDUCTOR, an automotive technology firm based in California, has acquired privately held Exalos AG, a 20 year old Swiss photonics company that specialises in the design of high-performance optical semiconductors including SLEDs for fibre optic gyroscopes and semiconductor optical amplifiers (SOAs).

"Exalos' differentiated solutions immediately expand Indie's ADAS and user experience product and technology offering to our global tier one and automotive OEM customer base," said Donald McClymont, Indie's co-founder and CEO.

"Specifically, Indie can now leverage Exalos' core superluminescent LED and SOA technologies to enable head-up display, high-brightness visible lighting and inertial-measurement-unit-based navigational applications and, importantly, to extend our frequency-modulated CW lidar portfolio. We are gaining a well-established team of 17 world class engineers, including the industry's leading expertise in bright light sources based on a proprietary GaN process. At a higher level, our acquisition of Exalos represents another step in our quest to build a broadline autotech powerhouse."

"We are excited to join forces with Indie at this key juncture of Exalos' evolution," said Christian Velez, CEO and founder of Exalos. "Given Indie's global sales channels and demonstrated scalability, I am confident that together we can take our business to the next level, capitalising on clear product synergies between us and extend our customer reach while preserving the Exalos innovation engine."

Subject to the terms and conditions of the definitive agreement, Indie paid approximately $45 million to Exalos equity holders comprised of 6.6 million Indie Class A common shares.

In addition, if certain revenue-based performance targets are exceeded over a 24-month post-closing period, there is an opportunity for Exalos equity holders to earn up to $20 million more in cash or Indie Class A common shares, at Indie's election.

IQE to collaborate with VisIC on GaN for EVs

IQE plc has announced a strategic collaboration with GaN company VisIC to develop high reliability GaN D-Mode (D-Mode GaN) power products for use in EV inverters.

200 mm D-Mode GaN power epiwafers will be developed at IQE's UK facilities, using IQE's well-established expertise in GaN technology.

Americo Lemos, CEO of IQE, commented: "We are pleased to announce this collaboration with VisIC Technologies to develop GaN power technologies for use in electric vehicles. Our combined expertise in the field makes this an ideal partnership. This is another sign of the progress we are making in our diversification strategy, as we look to capture the significant growth opportunities in the GaN automotive power market, which is vital in supporting the transition to electric vehicles."

Tamara Baksht, CEO and co-founder of VisIC Technologies, added: "We believe that teaming up with IQE is a pivotal step towards reshaping the EV industry. Their track record of delivery in the sector and technological leadership means they are ideally placed for us to collaborate with to develop next-generation technology to power the electric vehicle revolution."

Baksht added: "Our D-Mode D3GAN technology has the potential to transform electric vehicles, making them more efficient, reliable, and sustainable. Together, we are poised to create a brighter and greener future for transportation. The co-operation brings higher availability of ground-breaking technology for GaN-on-silicon and paves the way for a resilient supply chain to serve the automotive industry."

GlobiTech picks Aixtron tool for SiC expansion

G10-SiC enables foundry to ramp SiC epitaxy production into high volume

GLOBITECH INC, a subsidiary of GlobalWafers Co., Ltd, which makes SiC and silicon epiwafers for power and EVs, is using Aixtron SE's new G10-SiC system to expand its business into SiC epitaxy.

Since the G10-SiC was introduced a year ago, it has been rapidly adopted by 150 mm and 200 mm SiC device makers as well as foundries like GlobiTech, according to Aixtron.

"When one of the largest manufacturers and foundries like GlobiTech diversifies its business, it is a clear signal of a long-lasting trend in the semiconductor industry: conventional silicon is being replaced by SiC in an ever-increasing number of applications," said Felix Grawert, CEO and president of Aixtron SE.

GlobiTech, located in Sherman, Texas, is already in high-volume production using both G5WW C and G10-SiC Aixtron systems, with continued installation capacity available over the next years.

Modelled after the silicon business, GlobiTech supplies both SiC substrates and SiC epitaxy to the market.

"In Aixtron, we have found a strong partner supporting us in our vision and plans to expand our business into the SiC epitaxy market – an important step as SiC technology is one of the fastest-growing semiconductor sectors," said Mark England, president of GlobalWafers. "Aixtron tools allow us to get the most wafers out of our current fab. And Aixtron's team understands what it takes to compete against silicon to grow this market while offering great customer support and service"

The G10-SiC offers both 9 x 150 mm and 6 x 200 mm batch configurations, allowing rapid transition from 6-inch (150 mm) to 8-inch (200 mm) wafers. The new platform is built around Aixtron's automated wafer cassette-to-cassette loading solution with high-temperature wafer transfer. Aixtron expects this system will become its top-selling product this year.

Umicore and RENA announce collaboration

UMICORE ELECTRO-OPTIC MATERIALS has established a strategic collaboration with RENA Technologies, aimed at integrating RENA's ACE inception wafer processing tool into the ongoing development of germanium wafers for the space solar cell industry.

Umicore EOM makes epi-ready, dislocation-free germanium substrates designed for III-V multi-junction solar cells. RENA's wafer processing tool features flexible process performance and single side, full surface processing. The aim of the collaborative development programme is to ensure a seamless and efficient transition into mass production.

Jinyoun Cho, project manager at Umicore EOM, said: "The RENA advanced wafer processing solution plays a crucial role in our manufacturing process, and RENA's technology will be a key enabler for the performance of our germanium wafers."

MicroLED market to near $600 million by 2027

Mass production of large displays and wearable devices is propelling the microLED market, says TrendForce

TRENDFORCE predicts that the market value of microLED chips will reach $27 million in 2023, indicating a year-over-year growth of 92 percent. With the scaling of existing application shipments and the introduction of new applications, it projects that the market value of microLED chips will approach $580 million in 2027, representing a CAGR of approximately 136 percent from 2022 to 2027.

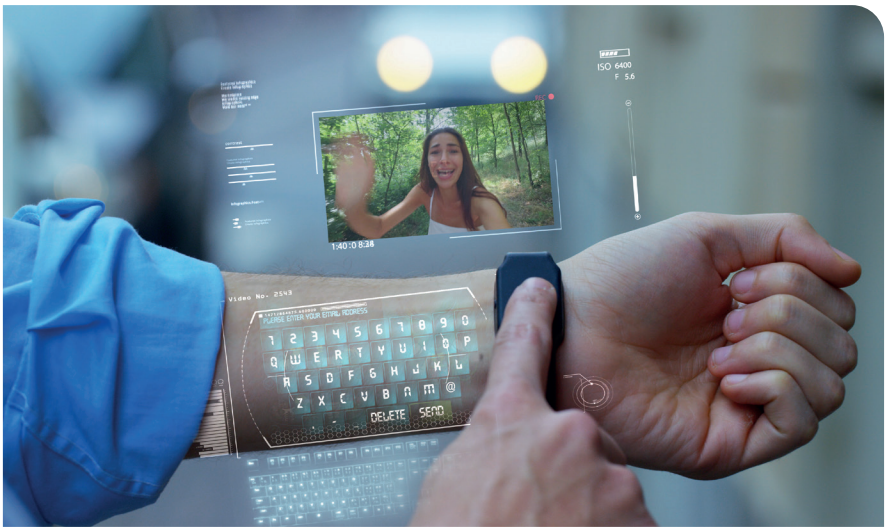
Alongside the consistent growth in chip values, ancillary industries – such as transfer and testing equipment, glass and CMOS backplanes, and both active and passive matrix drive ICs – are poised for synchronous expansion. This year, Samsung has unveiled an 89-inch 4K display and plans to further take advantage of microLED's seamless splicing by introducing 101-inch and 114-inch models.

LG Electronics, a South Korean brand, is set to commence mass production of its 136-inch 4K model, utilising a larger 22.3-inch backplane and cost-effective 16 µm by 27 µm chips, by the end of 2023.

Leading panel manufacturer BOE has charged a similar trajectory, with launches aimed at bolstering the overall industry's growth. The company has successfully launched its P0.9 active matrix display in 2Q23 and is planning to release the P0.51 active matrix display in the fourth quarter.

Additionally, BOE intends to introduce a turnkey solution in 2024. For brands interested in the microLED, this diversifies production acquisition channels and also contributes to the accelerated development of the overall industry.

Wearables are a key application for the microLED this year. AUO, pivoting from its traditional LCD operations, has successfully produced the world's



inaugural 1.39-inch microLED watch panel. In addition to initially providing it to European luxury watch manufacturer Tag Heuer, other major companies specialising in sports wearables and Japanese watch brands are all potential adopters of microLED wearable devices in the future.

Apple's rollout of a 2.12-inch microLED for the Apple Watch has been deferred from 2025 to 2026 due to supply chain adjustments. However, production operations for the microLED variant are already in motion, signifying possible integration into Apple's broader product range, including headsets, smartphones, and automotive applications.

Booming development in recent years has provided growth opportunities for innovative automotive displays like those based on the microLED. However, owing to the prolonged verification processes inherent to the auto sector, tangible mass production of microLED displays for vehicles might only materialise post-2026.

TrendForce believes that instrument displays with high demands for reliability and brightness, technologically advanced head-up displays (HUD), and transparent displays with numerous connections to autonomous driving technology are all primary avenues for microLED displays to enter the automotive sector. Automakers from Europe, the US, and Japan are demonstrating considerable enthusiasm toward adopting microLED tech.

The microLED continues to compete with technologies like LCOS, microOLED, and LBS when it comes to AR headsets. Industry leaders like Meta, Google, and MIT continue to assess and assist in the R&D of the microLED for micro-projection displays, attracted by its balanced performance, in terms of brightness, energy consumption, pixel density, and light engine size.

TrendForce hosted the "microLED Forum 2023" on Tuesday, September 5th at the NTUH International Convention Center. The forum invited TrendForce's senior research VP, Eric Chiou, alongside industry representatives from Mojo Vision, ITRI, Lumus, Unikorn Semiconductor, Porotech, Nitride Semiconductor, Tohoku University, Coherent, InZiv, AUO, and Tianma to share developments in microLED technology and its many applications.

Volvo Cars Tech Fund invests in start-up Leadrive

Shanghai-based SiC power module start-up benefits from Volvo's focus on vertical integration

VOLVO CARS TECH FUND has invested in Leadrive, a Shanghai-based company founded in 2017 to design and build SiC power modules.

"Leadrive's technology demonstrates a lot of potential for the development of more efficient electric drivetrains," said Alexander Petrofski, CEO of the Volvo Cars Tech Fund.

"That potential closely aligns with our own focus on electrification, so we're excited to invest in the company and help it to continue growing its business."

"Volvo Cars and Leadrive have been working very closely on the development of new generation SiC technologies, which has built a firm stairway towards the strategic collaboration," said Jie Shen, founder and CEO of Leadrive.

"This is a great milestone in Leadrive's global strategy and demonstrates the huge potential of our cooperation in advanced electrification technology."

Volvo's electrification roadmap is focused on vertical integration,

including bringing the development and manufacturing of e-motors and inverters in-house, and developing its own battery management software.

The company is also investing in the development and production of its own battery packs through Novo Energy, a joint venture together with Northvolt, optimising battery chemistry and integration in Volvo cars.

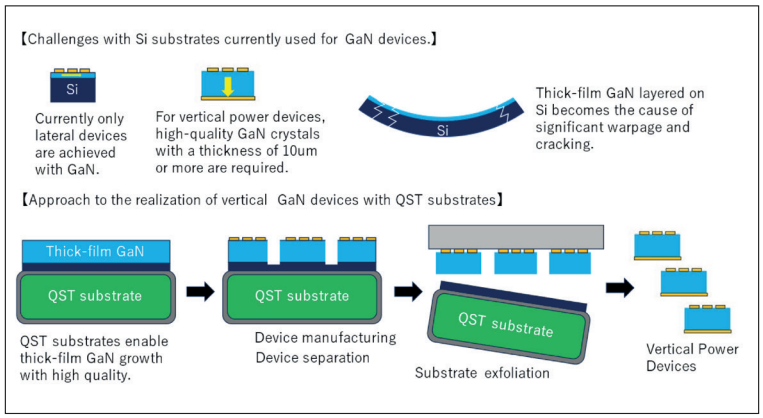
Volvo started the Volvo Cars Tech Fund in 2018 to invest in companies and technology for the automotive industry, such as artificial intelligence, electrification, autonomous driving, sustainability, and digital commerce.

This latest investment made by the Vovo Tech Fund is part of a new funding round by Leadrive, giving the Tech Fund a small minority stake in the company.

Shin-Etsu Chemical promotes QST substrate business

Substrate allows large-diameter, high-quality thick GaN epitaxial growth, making it suitable for power, RF and microLED devices

JAPANESE firm Shin-Etsu Chemical has announced the availability of QST (Qromis Substrate Technology) for GaN power devices. In addition, it will sell GaN grown QST substrates upon customer request. Currently, the company has a line-up of 6-inch and 8-inch diameter substrates, and is working on 12-inch substrates.



The substrate has the same coefficient of thermal expansion (CTE) as GaN, enabling suppression of warpage and cracking of the GaN epitaxial layer. This allows large-diameter, high-quality, thick GaN epitaxial growth, making it suitable for power devices and RF devices, as well as microLED growth for microLED displays, according to the company.

Customers in Japan and globally have been evaluating samples since 2021 for power devices, RF devices and LEDs. For power devices, continuous evaluation is underway for devices in the wide range of 650 V to 1800 V.

Shin-Etsu Chemical says it has been steadily improving the QST substrate technology. One example is the lowering of defects originating from the bonding process. In addition, for thicker GaN films, it has promoted the provision of template substrates with optimised buffer layers, to enable stable epitaxial growth of more than 10 µm thickness. The company has also achieved thick-film GaN growth exceeding 20 µm using QST substrates and a 1800 V breakdown voltage in power devices.

Shin-Etsu Chemical and Oki Electric have jointly developed a technology to exfoliate GaN from QST substrates and bond it to substrates made of different materials using Crystal Film Bonding (CFB) technology. Until now, most GaN power devices have been lateral devices, but CFB technology takes advantage of the characteristics of QST substrates to realise vertical power devices that can control large currents by exfoliating a thick layer of high-quality GaN from an insulating QST substrate (see figure).

For customers who manufacture GaN devices, Shin-Etsu Chemical will provide QST substrates or GaN-grown QST substrates and Oki Electric Industry will provide its CFB technology through partnering or licensing. In this way, the two companies hope to contribute to the advancement of vertical power devices.

Wolfspeed to sell RF business to Macom

WOLFSPEED will sell its radio frequency business to Macom Technology for approximately $75 million in cash, and 711,528 shares of Macom common stock, valued at $50 million based on the 30 trading day average for Macom's common stock through August 21, 2023. The company expects to close the transaction by the end of this year.

"Given the significant growth we've seen in automotive, industrial and renewable energy markets, we believe this is the right time to further focus on scaling our power device and materials businesses to meet this accelerated demand," said Wolfspeed president and CEO Gregg Lowe. "This transaction also represents a tremendous opportunity for our RF team to grow and operate at scale, leveraging Macom's diverse customer base, RF engineering leadership and operational efficiencies."

Wolfspeed RF's technology includes a strong GaN-on-SiC product portfolio optimised for next-generation telecoms infrastructure, military and other commercial applications. Macom will assume control of Wolfspeed's 100 mm GaN wafer fabrication facility in Research Triangle Park, North Carolina, approximately two years following the closing of the transaction to accommodate Wolfspeed's relocation of certain production equipment. Prior to such transfer, the shares of Macom's stock that Wolfspeed receives at closing will be subject to restrictions on transfer.

NSF and partners invest $45 million in future semiconductors

New US research and education awards will engage diverse talent in innovative semiconductor design and manufacturing

The US National Science Foundation has announced 24 research and education projects with a total investment of $45.6 million – including funding from the *CHIPS and Science Act of 2022* – to enable rapid progress in new semiconductor technologies and manufacturing as well as workforce development.

The projects are supported by the NSF Future of Semiconductors (FuSe) programme through a public-private partnership spanning NSF and four companies: Ericsson, IBM, Intel and Samsung.

Projects of potential interest for the compound semiconductor industry are within two categories: *Advanced Function and High Performance by Heterogeneous Integration* and *New Materials for Energy Efficient, Enhanced-Performance and Sustainable Semiconductor-Based Systems*.

"Faced with rising compute demands, semiconductor innovation will be required across materials, devices, heterogeneous integration, advanced packaging and compute architectures to enable an energy-efficient and sustainable full stack compute solution," said Vijay Narayanan, IBM Fellow and strategist, Physics of AI at IBM Research. "IBM is proud to support the FuSe programme's latest investment to accelerate semiconductor innovation to empower the next generation of innovators."

"Our investment will help train the next generation of talent necessary to fill key openings in the semiconductor industry and grow our economy from the middle out and bottom up," said NSF director Sethuraman Panchanathan.

"By supporting novel, transdisciplinary research, we will enable breakthroughs in semiconductors and microelectronics and address the national need for a reliable, secure supply of innovative semiconductor technologies, systems and professionals."

In addition to significant investment by NSF, including leveraging the $200 million appropriated by the *CHIPS and Science Act of 2022* for a CHIPS for America Workforce and Education Fund, these awards will be supported in part by Ericsson, IBM, Intel, and Samsung, which have committed to providing annual contributions through NSF.

Navitas launches GaNSafe

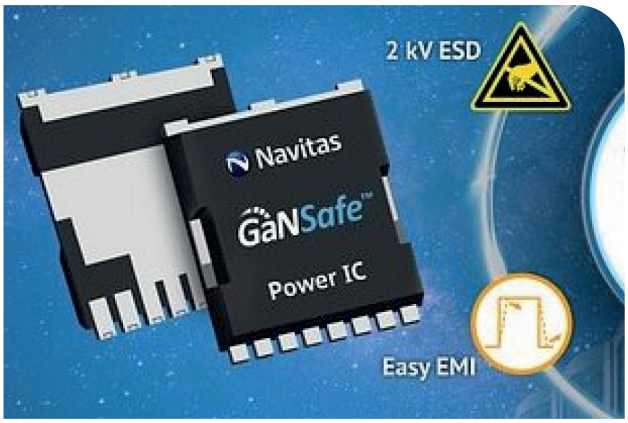
Next-gen power ICs feature new protection features and high-power packaging for gruelling high-temperature, long-duration conditions

NAVITAS SEMICONDUCTOR has launched GaNSafe, a new, high-performance wide bandgap power platform for applications in data centres, solar/energy storage and EV markets. The new chips are manufactured in Hsinchu by long-term Navitas partner TSMC.

Navitas' current generation of GaNFast power ICs integrate GaN power and drive with control, sensing and protection. Now, the new GaNSafe platform has been engineered with additional, application-specific protection features, functions and new, high-power packaging to deliver enabling performance under grueling high-temperature, long-duration conditions.

The initial, high-power 650/800 V GaNSafe portfolio covers a range of $R_{DS(ON)}$ from 35 mΩ to 98 mΩ in a novel, robust, and cool-running surface-mount TOLL package, to address applications from 1,000 W to 22,000 W.

"Our original GaNFast and GaNSense technologies have set the industry standard for mobile charging, establishing the first market with high-volume, mainstream GaN adoption to displace silicon," said Gene Sheridan, CEO and co-founder. "GaNSafe takes our technology to the next level, as the most protected, reliable and safe GaN devices in the industry, and now also targeting 1-22 kW power systems in AI-based data centres, EV, solar and energy storage systems. Customers can now achieve the full potential of GaN in these multi-billion dollar markets demanding the highest efficiency, density and reliability."



GaNSafe has a number of integrated features. These include protected, regulated, integrated gate-drive control, with zero gate-source loop inductance for reliable high-speed 2 MHz switching capability to maximise application power density. They also have high-speed short-circuit protection, with autonomous 'detect and protect' within 50 ns. Electrostatic discharge protection is 2 kV, compared to zero for discrete GaN transistors.

In addition, 650 V continuous, and 800 V transient voltage capability aid survival during extraordinary application conditions. Programmable turn-on and turn-off speeds (dV/dt) are said to simplify EMI regulatory requirements.

Navitas says that unlike discrete GaN transistor designs, with voltage spikes, undershoot and specification breaches, GaNSafe delivers an efficient, predictable, reliable system.

GaNSafe's robust 4-pin TOLL package has achieved the tough IPC-9701 mechanical reliability standard, and delivers simple, strong, dependable performance as compared to multi-chip modules which require three times as many connections and have poor cooling capability.

The GaNSafe portfolio is available immediately to qualified customers with mass production expected to begin in Q4 2023. 40 customer projects are already in progress with GaNSafe in data centre, solar, energy storage and EV applications.

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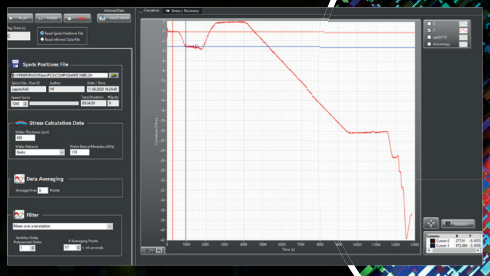

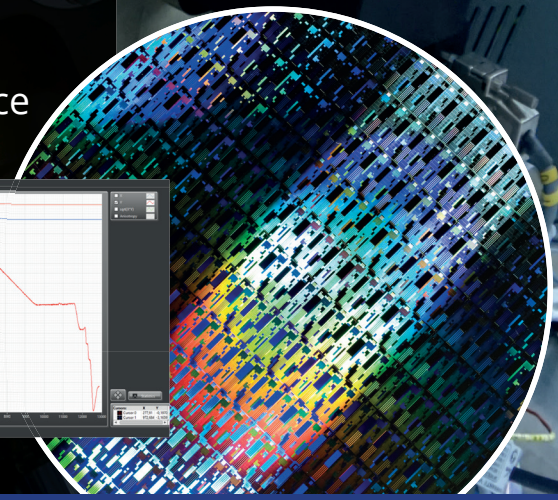

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Delving into the details of the GaN power electronics patents war

While accusations fly of disloyal employees and a lack of manufacturing know-how, what will really matter in an IP war is the fine print in the patents

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

THE COMMERCIALISATION of different classes of GaN devices seem to follow a similar trajectory. For the first major technology, the GaN-based high-brightness LED, the opportunity for lucrative sales spurred many companies from all over the world to launch products to market. Initially the efforts of these companies focused on improving product portfolios and revenue, but once sales had climbed, they started to wage war with one another, claiming infringement of key patents. Now it looks like history is starting to repeat itself, triggered by surging sales of GaN power devices.

The first significant shots in this sector were fired late this May, when the Californian fabless firm EPC issued a press release stating it had sued Chinese chipmaker Innoscience for infringing four of its US patents. EPC claims that Innoscience is drawing on this IP for the production of its 100 V and 650 V products.

As well as filing complaints in the federal court and with the US International Trade Commission, EPC has publicly accused Innoscience of poaching two employees that went on to be that chipmaker's CTO and Head of Sales and Marketing – hires that are said to be behind the launch of very similar products.

Innoscience did not take long to respond to EPC's accusations. The vertically integrated device manufacturer issued its own press release just two days later, saying that it had conducted a thorough analysis and found no infringement.

While throwing accusations around may help to strengthen a company's credibility, what will actually matter in this war is the fine print within the patents. They are not discussed in detail in the press releases from EPC and Innoscience, but have been examined by patent litigators Radulescu LLP; and in a recent webinar this firm's leader, David Radulescu, shared his thoughts. Radulescu is well-positioned to comment on such matters – he is neutral in this battle with a great deal of relevant expertise, having spent many years advising and representing GaN LED companies fighting disputes over claims of infringement of intellectual property.

The case between EPC and Innoscience considers just one of many classes of GaN transistor. Both parties produce devices that are normally off (E-mode), and feature a *p*-doped layer of (Al)GaN under the gate of the device.

EPC holds a total of 57 US patents, and its action against Innoscience involves four of them – two from 2013, and another two from 2017.

One of the patents from 2013, the US 8,350,294, concerns the design and fabrication of a compensated gate MISFET. A key issue here, according to Radulescu, is whether the phrase 'compensated GaN layer' describes the gate layer in Innoscience's devices, which are presumably formed by doping GaN with magnesium. Realising effective *p*-type doping is far from trivial. It was a key milestone in the development of the LED, with one of its pioneers, the Nobel Prize winner Shuji

Nakamura, discovering that annealing in a nitrogen environment breaks up magnesium complexes, drives hydrogen out of the material and ultimately improves conductivity.

Radulescu shared snippets of articles in the public domain that have been written by employees at Innoscience and discussed the use of a magnesium-doped *p*-type layer beneath the gate. In addition, he highlighted results of secondary ion mass spectrometry (SIMS) carried out by EPC, looking at levels of magnesium, oxygen, carbon, aluminium and hydrogen in the gate stack of an Innoscience device.

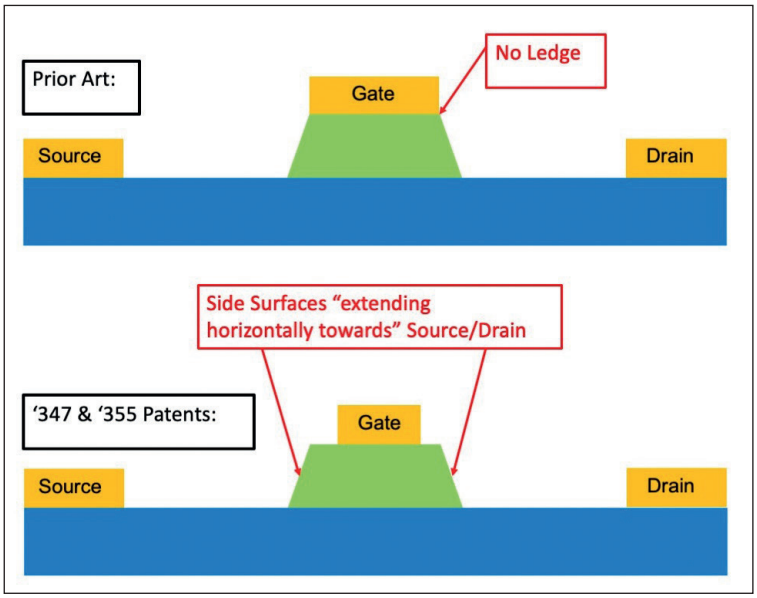
The expert in patent litigation explained that the court will have to mull over a number of questions. As well as considering whether Innoscience's devices use a 'compensated GaN layer', they will have to try and determine how the company makes its *p*-type GaN stack – is there a post-growth anneal in nitrogen, mirroring LED production – and what can be concluded from the SIMS data.

EPC's other patent from 2013 that is claimed to be infringed by the actions of Innoscience is that associated with a self-aligned gate E-mode HEMT (US 8,404,508). In this patent, EPC states that its self-aligned process leads to the bottom of the gate (contact) metal having the same dimension as the top of the 'gate compound'.

Radulescu pointed out that gates can have a variety of shapes, including a self-aligned geometry and a regular and inverted T-shape. Innoscience has a patent for its gate process (US 10,971,579). With this approach, the GaN beneath the gate is intentionally made wider than the gate (contact) metal.

According to Radulescu, a key question facing those that are trying to evaluate the validity of EPC's claim of infringement of the patent '508 patent is this: Does 'etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact,' describe Innoscience's process that results in a gate 'ledge'?

The remaining two of four asserted patents are from 2017 – US patents 9,748,347 and 10,312,335 – and cover a gate with self-aligned ledges for enhancement-mode GaN transistors. These patents describe an architecture for trimming the gate leakage current: a ledge beneath the metal gate that features side surfaces 'extending horizontally' towards the source and drain (see figure).



➤ EPC has two patents that detail how to cut the leakage current of E-mode GaN HEMTs with an architecture that uses gate ledges and side surfaces that extend horizontally.

Radulescu remarked that both patents require gate 'side surfaces' that 'extend horizontally' towards the source/drain. It is possible Innoscience will argue that its side surfaces are close to vertical, or it may question how one should define the required slope.

What is clear is that the legal process will take a great deal of time and money. A healthy budget for litigation is critical, the chances of success are far higher with a legal team experienced with GaN technology and devices, and it's crucial to avoid strategic mistakes during the process.

The hearing of evidence in this case is scheduled for next February, with a target date for a decision of 3 October, 2024. Should EPC win, Innoscience will be prevented from exporting products to the US.

Drawing on the history of the LED, one should expect that this patent battle will be the first of many associated with the GaN HEMT. And while there will be some winners and losers, many outcomes may not be so clear cut, with cross-licensing deals set up that have pros and cons for both parties.

What is clear is that the legal process will take a great deal of time and money. A healthy budget for litigation is critical, the chances of success are far higher with a legal team experienced with GaN technology and devices, and it's crucial to avoid strategic mistakes during the process

➤ David Radulescu has a PhD in compound semiconductors and devices (HEMTs) from Cornell University, so he is uniquely positioned to separate the wheat from the chaff from a legal and technical perspective simultaneously.

Nuburu: Seeking dividends with diversification

The pioneer of powerful blue lasers is expanding its portfolio and targeting new markets

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

AS COMPANIES GROW, they tend to diversify. That's certainly the case for Nuburu, the trailblazer of powerful blue lasers that began by producing systems for welding metals that are highly reflective in the IR, such as copper, aluminium and gold. Over the last year or so it has expanded its target markets with the addition of the 3D printing of metals, as well as launching more powerful lasers and transitioning from a private company to one that is traded on the stock market.

While the 3D printing of metals is not as well-known as that of plastics, it is a substantial and growing market. According to the analyst Grand View Research, the 3D metal printing market was worth over $6 billion in 2022, and is forecast to climb at a compound annual growth rate of almost 25 percent throughout this decade.

Printing of metals involves directing them, in their powder form, into a powerful laser beam. This is a very capable approach for printing high-density copper. It could be employed for the production of heat exchangers in rocket motors, and for making parts for electric vehicles, such as battery packs.

While infra-red lasers are the incumbent source for metal printing, blue lasers offer distinct advantages for a number of metals, just as they do for welding. The levels of optical absorption are 13 and 66 times higher in the blue than the infra-red, respectively, for copper and gold. This translates into a more efficient process that generates far fewer fumes.

➤ The BL-1000-F, which couples light into a fibre with a diameter of 200 μm, launched this summer and is the company's most powerful source to date.

Nuburu has demonstrated the superiority of its blue lasers over infra-red variants for 3D metal printing by evaluating the performance provided by both light sources in a commercial tool, the EOS M 100, using copper and stainless-steel powders.

According to Mark Zediker, the company's founder and CEO, the EOS M 100 could not print copper when fitted with a 200 W infra-red laser.

"We put a 150 watt blue laser into the machine and immediately got great results, printing copper with densities up to 97.5 percent," says Zediker. He anticipates even higher densities in the very near future, following an upgrade to the tool that involves a switch to a 250 W blue laser.

The team also obtained excellent results with stainless steel. "The 150 watt blue laser printed at a speed approximately three times faster than the 200 watt infra-red laser that came with the machine." This gain in speed, realised without compromising the density of the printed metal, is incredibly valued – within this industry, increases in speed of just 10-to-20 percent matter to those that use these tools.

In addition to copper and stainless steel, an EOS M 100 employing a Nuburu blue laser can print other metals. The full palette includes titanium and a copper alloy that's currently used for making rocket engines.

"In all cases, the blue laser was substantially faster, with better surface finish and porosity control," enthuses Zediker.

Nuburu is expanding the capabilities of 3D metal printing through a contract with the US Air Force. "Rather than just writing a single dot on the surface, we're imaging an image of a plane onto the surface and melting," says Zediker. By using a digital light engine from TI, the partnership can address around 4000 spots simultaneously. According to Zediker, all services within the US Department of Defense are looking at this 3D metal printing technology,

because it could allow them to print larger parts in their depots in a speedy, cost-effective manner.

While helping to develop this technology, Nuburu is enhancing its reputation with suppliers of parts for electric vehicles, including producers of batteries. "We're getting excellent results with them," remarks Zediker. "We think we will be able to move into larger scale welding of batteries and the electric contacts for batteries next year."

Responding to demands from this sector, which places a premium on systems with higher welding speeds, this June Nuburu launched its most power source to date, the BL-1000-F. This system couples light into a fibre with a diameter of 200 μm, which is double the width of that used in the 250 W laser.

Market moves

In addition to all the efforts at developing new products and processing technologies, Nuburu has been active on the financial front. Earlier this year, the company went through a reverse merger with a Special Purpose Acquisition Company and began trading on the NYSE American exchange.
This summer the company bolstered its balance sheet by raising additional funding of $9.2 million from existing and new investors.

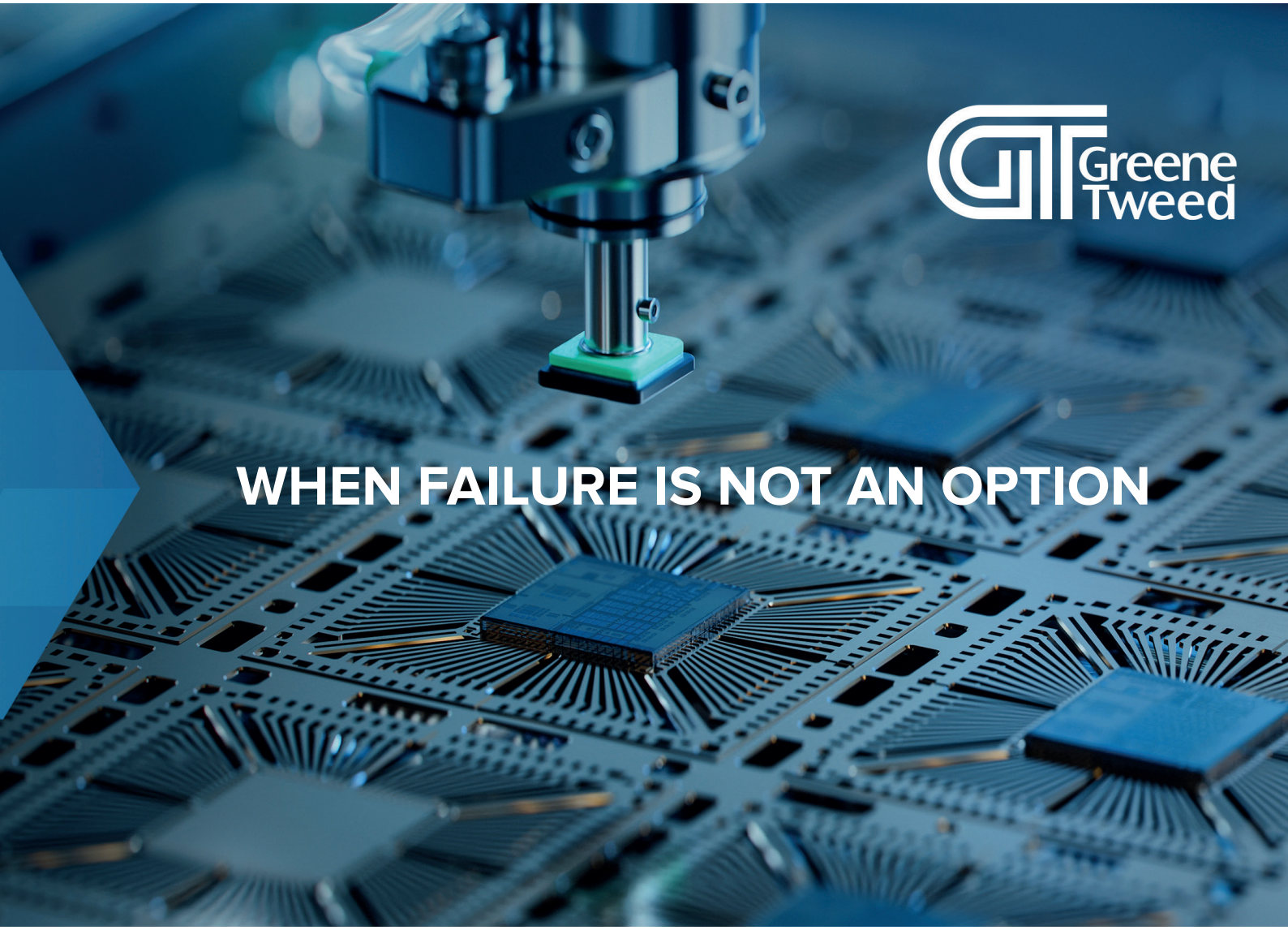
Following initial trading at just over $10, the value of these shares has plummeted to below one-tenth of that value.

"I think we put it down to the fact that nobody in the financial industry knows who we are," says Zediker.

"Many of the research analysts have adopted a wait-and-see attitude with us, and they want to see a couple of quarters of performance from the company before they'll start coverage."

One would expect the company's share price to recover, given that Nuburu has such promise on many fronts. It has impressive products, targeting growing markets, which is strong foundation for growing sales over the coming years.

➤ The BL-250 has an output power of 250 W.



WHEN FAILURE IS NOT AN OPTION

Greene Tweed engineers sealing solutions and structural components that outperform and outlast in the world's harshest semiconductor manufacturing applications

BY NICK MCNEAL, THYAG SADASIWAN AND PRAGATI VERMA FROM GREENE TWEED

ELECTRIC VEHICLES. Sensor-embedded Smart Devices. 5G and 6G connectivity. Quantum computing. What do they all have in common? They require chips made from compound semiconductors, handling the high voltages and powers that silicon can't.

As the demand for compound semiconductors soars, what do the manufacturers of these devices need besides more deposition and etch tools, and more substrates? It's a steady supply of some inconspicuous yet indispensable components that are critical for manufacturing new generations of compound semiconductor devices.

Chemraz Seals: Unsung Heroes

At Greene Tweed, we engineer sealing solutions that outperform and outlast in the world's harshest semiconductor manufacturing applications. They are a remarkable example of what we do, working behind the scenes to empower the intricate machinery of chipmaking. For 160 years, we've been equipping critical sectors with materials and engineered components that deliver certainty during crucial operations.

For instance, our perfluoroelastomer (FFKM) Chemraz o-rings and sealing solutions meet the critical demands of modern chip fabrication. They are renowned for preventing contamination, while withstanding aggressive chemicals and extremely high temperatures.

For decades, we have been at the forefront of the complex FFKM production process. These high-

performance materials need specific ingredients. Due to this, disruptions can occur when just a single ingredient is in short supply. During the last couple of years, an unexpected and tumultuous industry-wide supply crunch had gripped several FFKM ingredients. Exacerbating this situation, this supply shortage coincided with a global surge in the demand for chips. As a result, FFKM material was in short supply, just at the very moment when semiconductor manufacturers needed it to go into overdrive. This snared the FFKM industry in the epicentre of a perfect storm, where supply delays threatened to impede semiconductor availability and the resultant economic recovery.

If the recent silicon chip shortage has taught us anything, it's the need to fortify supply chains for the components that are powering the intricate machinery of semiconductor manufacturing. Chipmakers are now acutely aware of how dependent the semiconductor industry is on FFKM seals, especially as they turn to more demanding processes that rely on ultraclean processing.

Greene Tweed was the first company in the US to use cleanroom manufacturing to produce our sealing solutions. We pioneered this move, because we intimately understand the significance of ultraclean operations in the semiconductor industry. We know that our seals have to perform in the harshest environments of modern semiconductor fabrication processes, where they are critical to improve uptime, reduce contamination and boost wafer yield.

Where second best isn't good enough

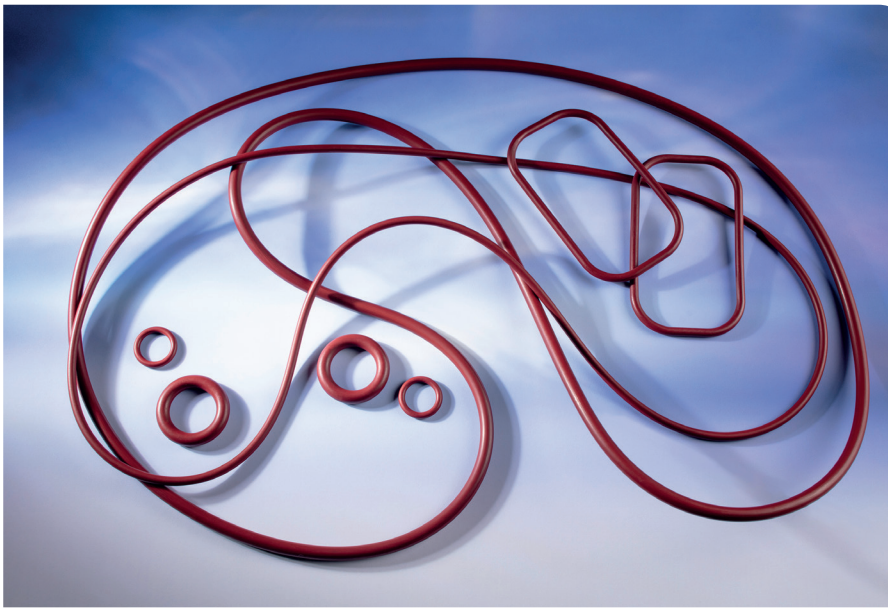
Over the last couple of years, the demand for materials used to make SiC and GaN power devices has been soaring. As a result, sales of compound semiconductor substrate materials are set to more than double by 2027, according to Yole Intelligence. This French market analyst forecasts that the compound substrate material market will grow from $945 million in 2021 to $2.3 billion in 2027, equating to a compound annual growth rate of 17 percent.

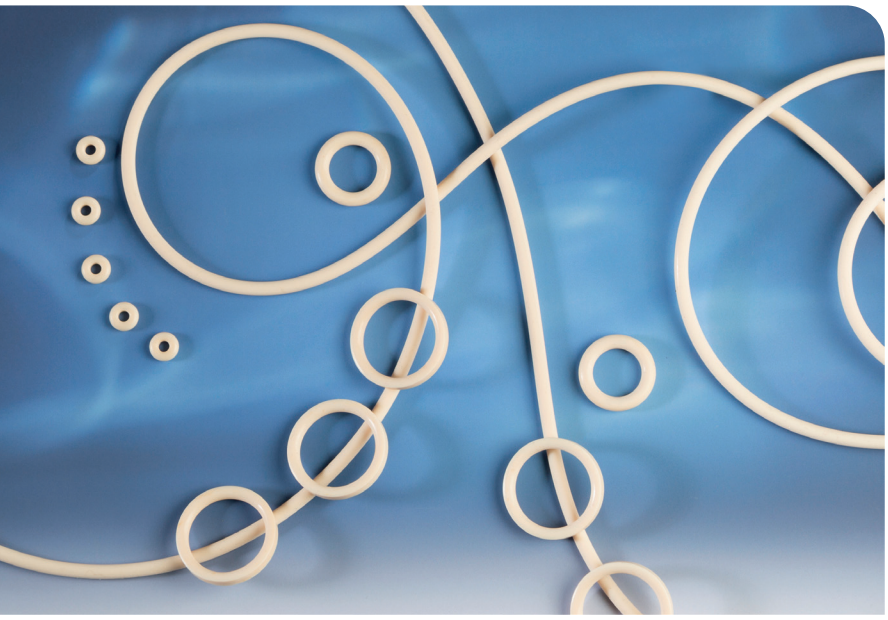
To meet the growing demand for compound semiconductors, chipmakers need to step up manufacturing capacity and strengthen their supply chains for components such as FFKM seals, which are critical to manufacturing these chips. As a global leader in seals based on FFKM elastomers, we know second-best seals aren't good enough in an industry as complex and challenging as semiconductor manufacturing. So, we have taken action to ensure a steady supply of our sealing solutions. This allows us to meet the burgeoning demand, while ensuring industry resilience and minimising the impact of any future disruptions on the supply of FFKM materials.

We realise that the dynamic and fast-growing landscape of the compound semiconductor industry demands strategic planning and foresight. To enable our customers to do this, we are proactively taking measures to create robust business continuity plans and ensure a steady and uninterrupted supply. Our efforts began by conducting comprehensive risk assessments, identifying vulnerabilities, and developing contingency plans to mitigate potential disruptions. Following this deep exploration, we have rolled out four major initiatives. They will help us navigate this turbulent terrain, circumvent future disruptions, and secure a regular supply – all critical initiatives for helping us to drive our semiconductor customers' continued growth and success.

Our first initiative has been the building of strategic stockpiles of critical raw materials to prepare for the anticipated upturn. While securing raw materials is essential, it's just one aspect of our multifaceted approach to ensuring supply. Our scientists are innovating, developing new products and reformulating existing ones to prepare for the ever-evolving regulations and shifting market dynamics. We are proactively identifying risks from ingredients that are supply-constrained and mitigating them with more readily available feedstock materials. At the same time, we are working with supply chain partners to determine the potential impact of government reviews and supply crunch on their materials, chemicals and production processes. Simultaneously, we are working with our customers to develop and validate alternative compounds with superior technologies and significant benefits.

The second initiative is that while we are reformulating and developing new products, we take proactive measures to diversify our supply chain and reduce the risk of overreliance on a single supplier or region. We realise that setting up multiple FFKM factories is too capital-intensive and might not be feasible for our suppliers. That's why we are leveraging multiple suppliers to build a resilient, adaptable supply chain that's better equipped to navigate the challenges of an ever-evolving semiconductor landscape.





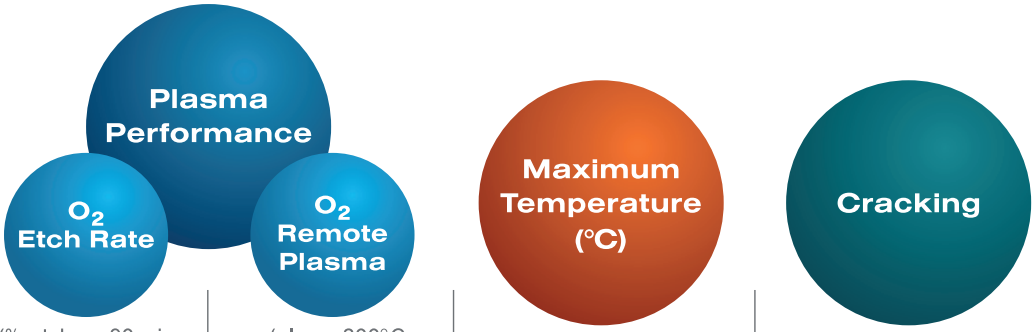
To do this, we are developing equivalent products that serve as alternatives to the original ones. We are carefully selecting compounds and sourcing raw materials for two equivalent products from different suppliers located in separate countries. For example, we are augmenting our supply chain by adding Chemraz G57. This is equivalent to Chemraz 657, and provides excellent plasma resistance in a variety of aggressive chemical environments.

Our third initiative is to spread our manufacturing footprint. We are strategically setting up factories in new locations all over the world, a move that helps us bring supply chain stability to our semiconductor customers. Our latest upcoming manufacturing facility is in Cheongju-si, Chungcheongbuk-do, Korea. Expected to be ready by the middle of next year, initially this facility will be dedicated to our highest-performing elastomer Chemraz product line, specifically formulated for semiconductor applications. By decentralising production and sourcing, we will be better equipped to manage supply crunches, overcome production bottlenecks, and maintain consistent deliveries to customers.

The last of our four key initiatives, which is being implemented in tandem with the expansion of manufacturing capacity, is a significant step-up in inventory optimisation. We are now building the right inventory, to meet future demand with industry-leading lead times. Coupled with our new facility, this initiative will help us to grow our capacity and capability, to better support the global demand for our products and bring enhanced supply chain stability to the semiconductor industry.

Back on track

The results of building our supply resiliency are already evident. We have been able to restore the standard pre-disruption level lead times that our customers enjoyed before geopolitical and regulatory events caused an unprecedented FFKM supply crunch. Getting supply times back on track is not only testament to our resilience, adaptability, and customer-centric approach – it's also critical



Chemraz	(% wt. loss, 90 min direct exposure)	(clean, 200°C % wt. loss)		
E38	1.003	0.100	260	Good
629	1.739	0.074	260	Good
657	0.417	0.053	280	Better
XPE	0.570	0.026	280	Best
G57	0.670	0.089	300	Better

All your semiconductor sealing questions, answered

DO YOU NEED an elastomer o-ring or sealing solution that's built to withstand aggressive liquids, gases, and plasma at the extreme temperatures found in the harshest semiconductor applications? Here are answers to the key sealing questions facing semiconductor manufacturers...

What kind of seals work best for semiconductor manufacturing processes?

Perfluoroelastomer (or FFKM) sealing material, known for its exceptional resistance to aggressive chemicals, extreme temperatures and plasma environments, is ideal for a manufacturing process as aggressive as semiconductor fabrication. Greene Tweed offers Chemraz sealing solutions, known for their exceptional resistance to extreme temperatures, chemicals and plasma environments.

What sets Greene Tweed's Chemraz sealing solutions apart?

At Greene Tweed, we take pride in our Chemraz sealing solutions that are engineered to outperform and outlast in the world's harshest environments. For 160 years, we've equipped critical sectors, including the semiconductor industry, with materials and engineered components that perform – no excuses, no exceptions. With the broadest temperature range and unmatched chemical resistance among all elastomeric materials, Chemraz is the prime choice for the most challenging semiconductor applications. Superior quality, precision engineering and customisability result in less downtime and higher wafer processing yields.

Can Greene Tweed customise seals to suit specific semiconductor applications?

Yes, at Greene Tweed we offer a range of sealing solutions that can be tailored to meet your specific requirements. Our engineering team works closely with semiconductor manufacturers to design custom seals that match equipment specifications and deliver optimised performance.

What kind of semiconductor manufacturing processes benefit from Greene Tweed's Chemraz sealing solutions?

Chemraz FFKM sealing solutions are ideal for a wide range of semiconductor equipment, such as:

- Conductor etch
- Dielectric etch
- PECVD
- ALD
- RTP
- Wet cleans
- Chamber seals
- Slit valve and BSVs
- Pendulum and gate valves
- Electrostatic chuck and pedestal barrier seals
- Chemical delivery

Can Greene Tweed's sealing solutions withstand aggressive cleaning and etching chemistries?

Absolutely! Chemraz exhibits exceptional chemical resistance, making it highly compatible with aggressive cleaning and etching chemistries used in semiconductor fabrication. It remains stable even when exposed to harsh plasma environments and reactive chemicals, ensuring optimal performance and longevity.

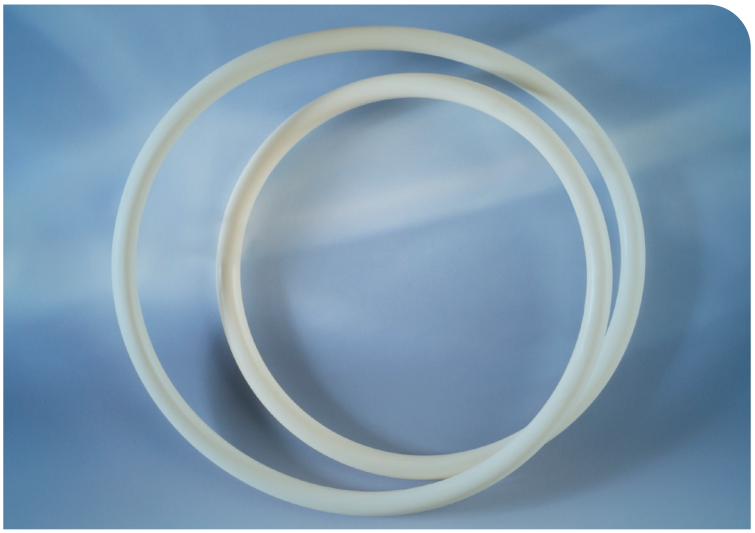
I want to implement Greene Tweed's latest sealing solutions in my semiconductor application. How can I start the process?

To explore the benefits of FFKM sealing solutions tailored to your semiconductor equipment, reach out to our expert team at Greene Tweed. Our engineers are ready to talk about your specifications and provide technical guidance. We'll keep working to iterate, improve and deliver high-quality sealing solutions to elevate your semiconductor manufacturing process.

for supporting robust demand from the makers of compound semiconductor devices.

As we continue to forge ahead on this transformative journey, we are committed to keeping customer satisfaction and supply chain stability at the core of everything we do. We understand that our high-performance Chemraz seals do what other seals can't do, and that the timely delivery of our products is essential for our customers' success and continued growth.

Together with our customers and partners, we will continue to shape a resilient future that thrives on innovation and a custom collaborative approach that delivers certainty for compound semiconductor manufacturers' fast-expanding crucial operations.



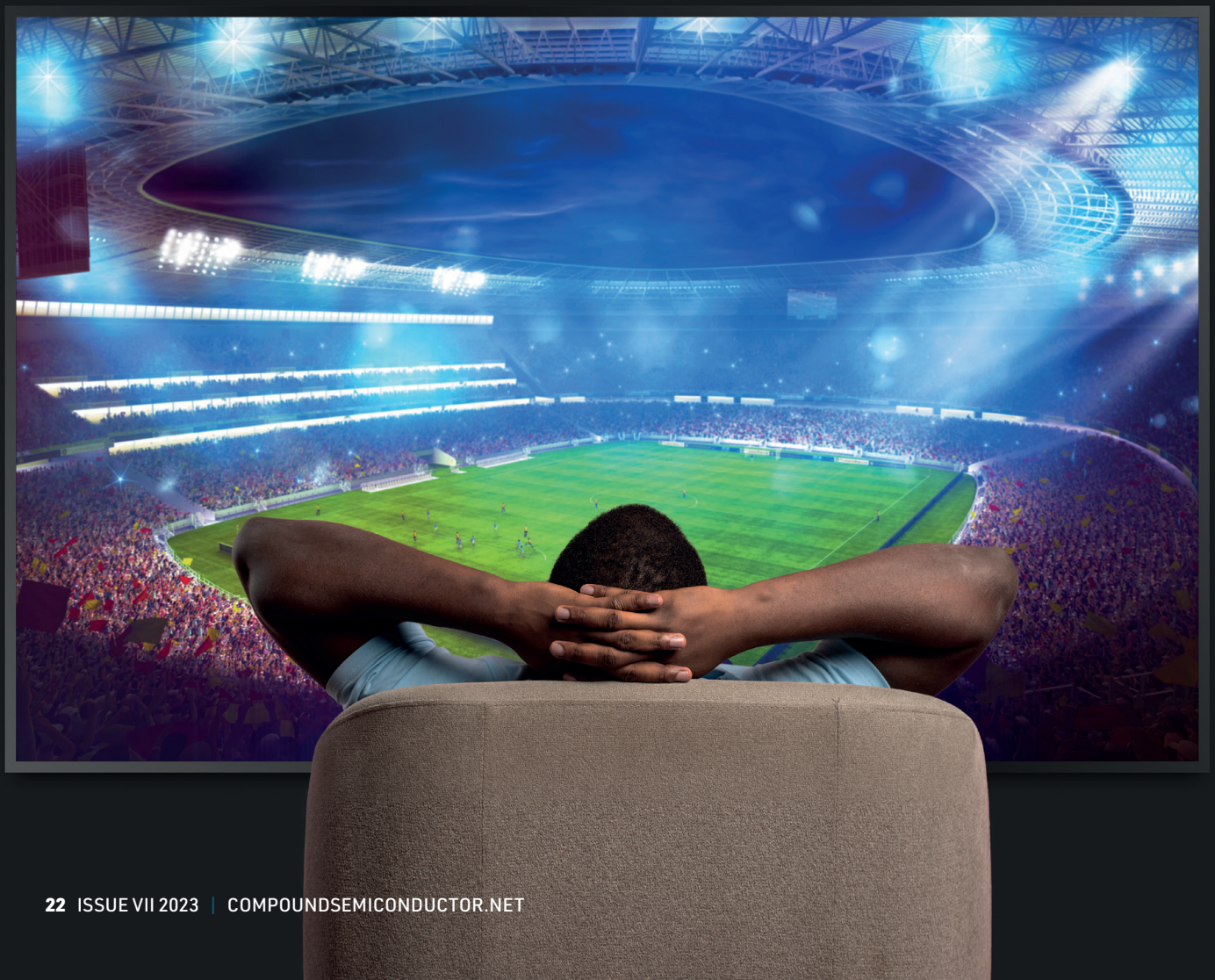
Revolutionising microLED displays with nanowires

Large silicon wafers populated with blue-emitting nanowires and colour-converting quantum dots offer a compelling approach to making microLEDs for many types of display

BY PIERRE TCHOULFIAN AND CO-WORKERS FROM ALEDIA

IT'S HARD TO IMAGINE a day that passes when we don't look at a screen. They are in our homes, incorporated into TVs, laptops and tablets; and when we go out to the shops we come across them in the form of videowall displays, and in consumer electronics stores promoting the next must-have tech, such as virtual/augmented reality displays. And even when we try and get away from it all, by heading to the beach or the hills, we're unlikely to forget our smartphones and smartwatches. The reality is that screens are everywhere, so it's not surprising that they are responsible for a substantial industry, netting around $120 billion every year.

One part of this industry facing significant challenges is the reasonably large-size display. To enable short-viewing-distance indoor applications, LED videowall displays and luxury TVs need to move to a smaller pitch. However, it's far from easy to integrate three different colours of pixel, plus driving circuitry, on a backplane. But success on this front is most welcome, as it could also breathe new



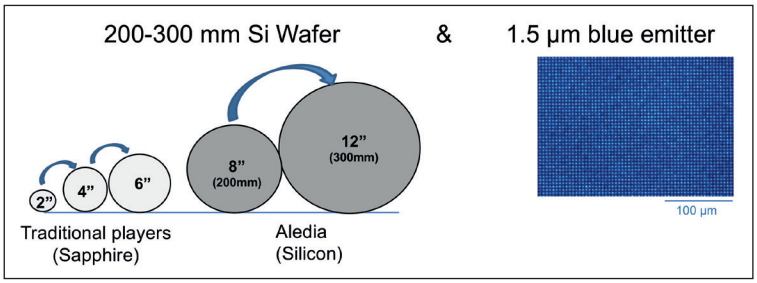
life into mid-size displays. Today's OLED and LCD technologies are limited in terms of their brightness, contrast and energy efficiency, and they struggle to scale beyond 90 inches.

The good news is that there is a unique, cost-effective technology that has been rapidly improving over the last years and could penetrate these and other segments of the display market: the GaN microLED. It is a descendant of the traditional GaN-based LED, now dominating the general lighting market, thanks to its high energy efficiency (75 percent in the blue), brightness and reliability.

An obvious difference between the conventional LED and the microLED is size. For general lighting, 0.35-1 mm chips are typically used, assembled individually in packages with a size of several millimetres. Meanwhile, to make displays from microLEDs, these devices have to have a high efficiency, a small size – typically less than 10 µm – and be relocated using an unpackaged chip assembly process, which moves millions of them with a collective high accuracy. In addition to this high-yield transfer technique, there needs to be a suitable electrical connection technology.

The most common form of GaN microLED is that with a 2D architecture. This design enjoys strong momentum, with many of its developers hoping it will deliver on its promise to provide a significant improvement in power consumption over LCD and OLED technologies. However, as the size of the 2D microLEDs falls, so does its efficiency. One option for overcoming this issue is to optimise the post-etching passivation of the GaN sidewalls. But our team at Aledia is convinced that there's an even better alternative: to switch to 3D microLEDs, employing GaN-based nanowires as light emitters (see Figure 1).

Since founding in 2012 as a spin-out of CEA-LETI, we have continued to develop our unique and radical GaN-on-silicon 3D microLED technology

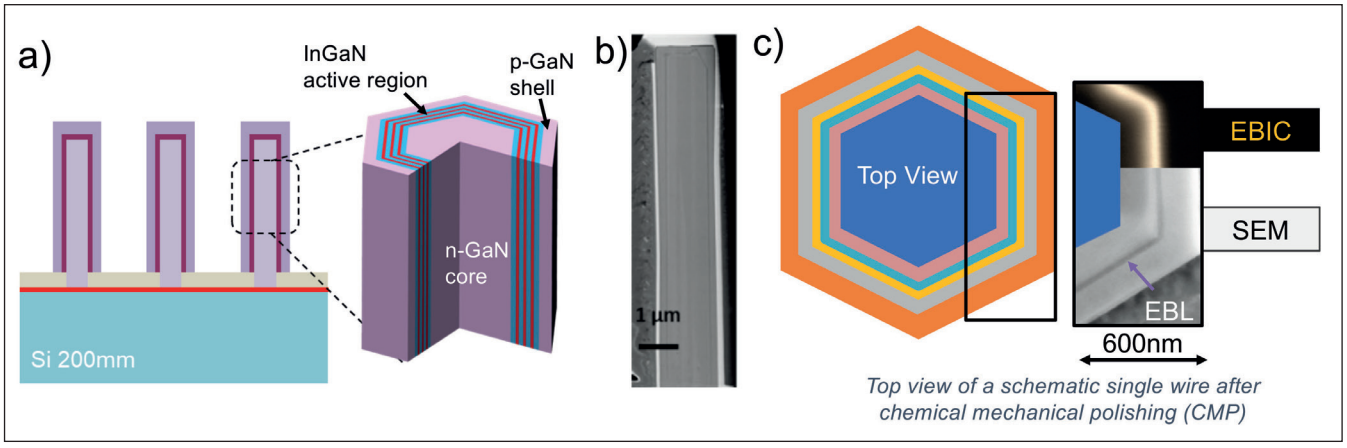


➤ Figure 1. Aledia's technology is based on using 200-300 mm silicon wafers, which provide the foundation for making 3D microLEDs with micron-range dimensions.

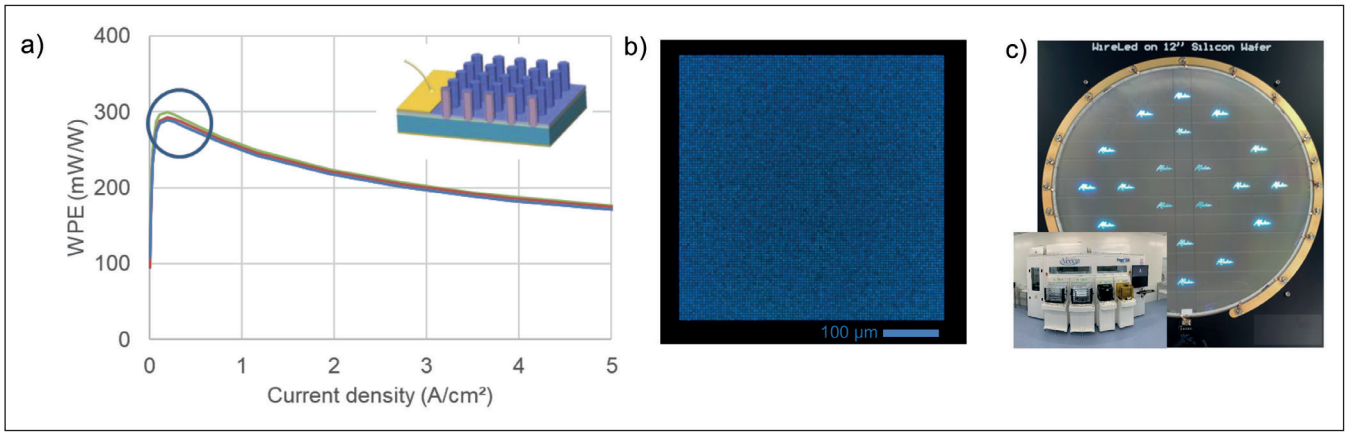
at our site in Grenoble, France, where our team has grown to 220 employees. Working together, we have developed a cost-effective technology that's compatible with 200 mm and 300 mm silicon wafers and has assets that include a high level of manufacturability and easy integration with electronics. Supporting our technology, which enables us to access completely new display formats based on microLEDs, are 250 patent families. While the technology is novel, the fabrication processes are not, with production able to leverage existing equipment and technologies from the display, semiconductor and LED industries.

The allure of nanowires

We begin production of our microLEDs with the growth of the blue emitting nanowires. They are transformed into devices using front-end chip processes that have been developed in standard 200 mm microelectronic foundries. To produce green and red emitters, we use advanced colour conversion, based on quantum dot patterning technology. Depending on our product's particular requirements, we produce chips populated with a couple to hundreds of nanowires. All these devices benefit from a built-in redundancy that's at the heart of our cutting-edge technology. Read on to discover more about the key aspects of our fascinating technology and its product opportunities.



➤ Figure 2. (a) Aledia's microLEDs are based on core-shell nanowires. (b) Transmission electron microscopy cross-sectional images show excellent crystalline quality. (c) Top-view scanning electron microscopy/electron-beam induced current signals highlighting the *p-n* junction position.



➤ Figure 3. (a) A wall-plug efficiency close to 300 mW/W at a low current density (0.2 A/cm^2), and (b) electroluminescence of an assembly of 10^4 wires, with all the wires lighting-up. (c) First blue electroluminescence on a 300 mm wafer.

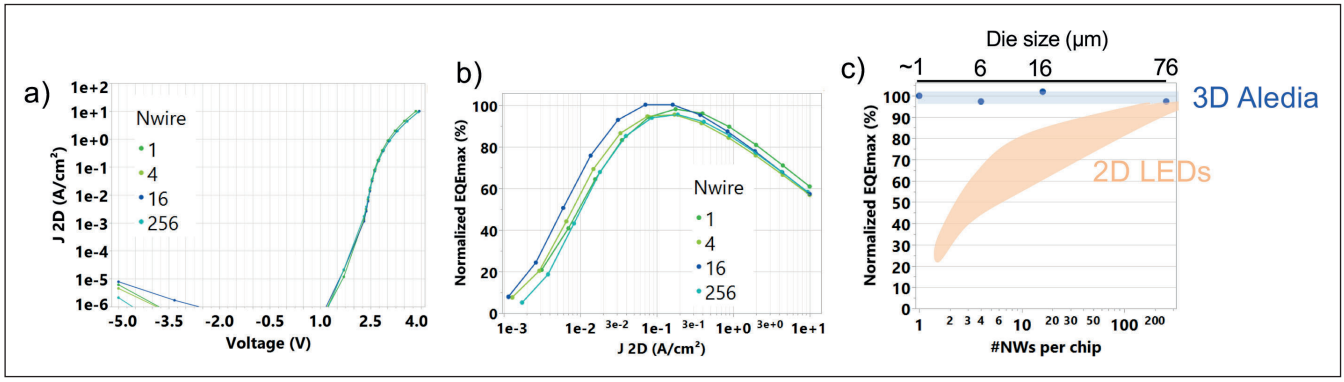
Over the last ten years, we have mastered the MOCVD of core shell nanowire LEDs, which we can grow on 200 mm and 300 mm SEMI-standard silicon substrates that are 725 µm and 775 µm thick, respectively. There's an LED epitaxial stack structure inside each nanowire (see Figure 2 (a)). This means that each nanowire is a microLED, with no need to etch through the quantum wells of the LED structure before forming contacts, an undesirable but essential requirement for 2D counterparts. Thus, there is no need to add a passivation layer to ensure good efficiency.

Scrutinising our nanowires with a transmission electron microscope reveals that they are free from defects, including threading dislocations (see Figure 2(b)). This is a great asset for our active regions. From this form of microscopy, we know that the dislocation density is below 1 x 10^6 cm^{-2}. The key point is that our microLEDs have a perfect active area. That's not the case for 2D microLEDs, which are held back by 'bulk defects', as well as surface local defects that arise when patterning the 2D epilayer.

Another advantage of our approach to producing microLEDs is the relatively short growth time. Epitaxy for our nanowires takes less than 3.5 hours, which is about half the time it takes to produce a typical planar LED heterostructure. This quick growth, which delivers cost savings, results from the absence of thick AlGaN-based buffers. In a typical planar LED, this thick buffer is needed to master the stress created during growth. Stress comes from a far higher coefficient of thermal expansion for GaN than silicon – this induces cracks in the GaN crystal as it cools down. Fortunately, that's not an issue for us. Thanks to a wire-based geometry, which is not continuous over the wafer surface, no stress is created in the GaN crystal. This ensures a perfect structure, regardless of wafer diameter and growth conditions.

Like any other developer of LEDs, over the years we have made continuous improvements to the internal quantum efficiency and the light extraction efficiency of our devices. Our approach to this has involved overcoming obstacles that developers of planar LEDs don't face, as we have had to apply different characterisation techniques, because methods such as secondary ion mass spectrometry are incompatible with our structures. To map the electric field inside the *p-n* junction of our devices, we use an electron-beam induced current approach, which has enabled us to determine the position of the junction and quantify the doping levels (see Figure 2 (c)).

Measurements of the efficiency of our devices demonstrate that our nanowire technology can address display applications (see Figure 3 (a)). When



➤ Figure 4. (a) Current density versus voltage (J-V) and (b) normalized external quantum efficiency versus current density (EQE-J) curves showing the superimposition of electro-optical behaviour whatever the device size. (c) EQE versus die size behaviour for 2D LEDs versus 3D LEDs.

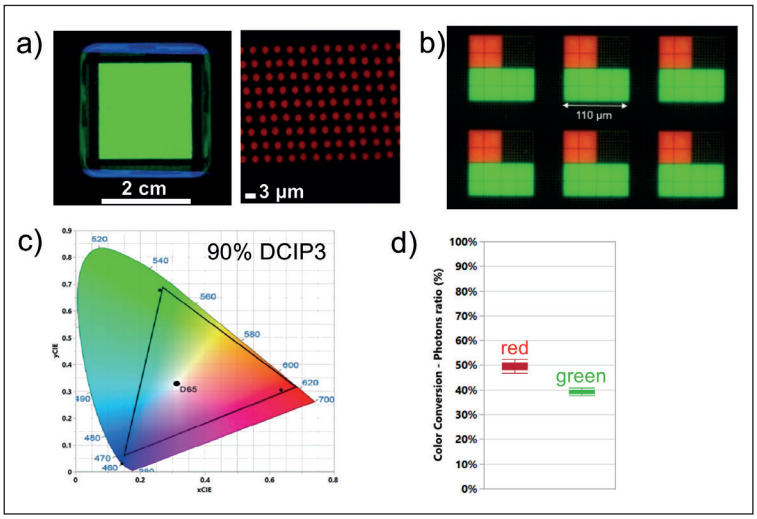
our nanowires are collectively driven in parallel, wall plug efficiency is close to 300 mW/W. Applying a voltage of just 3 V ensures that all the nanowires in an array of ten thousand light up (see Figure 3 (b)). The implication is that our nanowire light-up yield is above 99.99 percent, a valuable asset for the high demands of display manufacturing, where there is absolutely no tolerance to pixel defects.

One of our current goals is to transfer our epitaxial process to a standard 200 mm diameter high-volume manufacturing tool. We have every confidence we shall succeed in this endeavour, having already scaled our technology to large silicon wafers, leading to a world-first light-up on 300 mm silicon (see Figure 3 (c)). For this triumph, we grew our nanowires on (111) SEMI standard silicon wafers with a thickness of 775 μm. Our resulting epiwafer had a bow below 50 μm, ensuring full compatibility with post processing in a standard microelectronic foundry.

There are a number of compelling reasons why we have devoted such effort to transferring our technology to 300 mm wafers. There are several intrinsic advantages, including lower manufacturing costs, access to advanced CMOS electronics for LED direct bonding (nodes below 60 nm only exist in fabs with 300 mm lines), and significantly reduced costs for chip transfer.

We are encouraged by our measurements of current density versus voltage for microLEDs with 1, 4, 16, 64 and 256 nanowires (see Figure 4 (a)). Plots for all these devices, realised from the same location on a wafer, perfectly superimpose, showing that the size of the microLED has no impact on its performance. These devices also exhibit a low level of reverse leakage and good rectifying behaviour.

Plots of external quantum efficiency as a function of current density are also unaffected by device size (see Figure 4 (b)). Efficiency peaks at 0.2 A cm^{-2}, an ideal value for direct view displays, because microLEDs have to operate at low current density

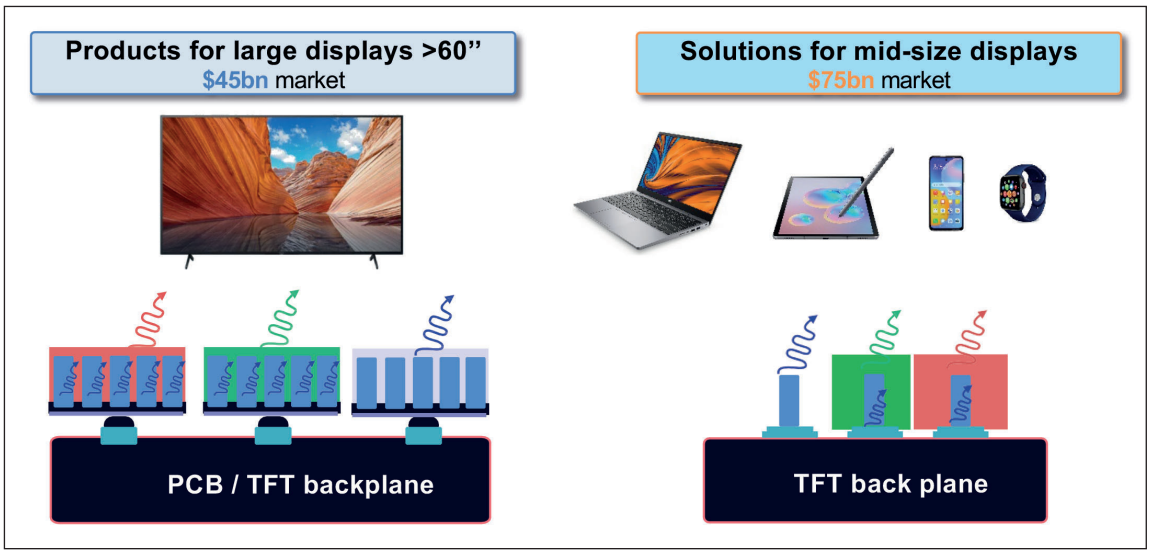


➤ Figure 5. (a) Colour conversion at different scales: cm to μm and (b) for a 110 μm pixel. (c) Colour coverage obtained using blue nanowires and green and red converted sub-pixels. (d) Photon conversion efficiency for green and red in the 110 μm pixel.

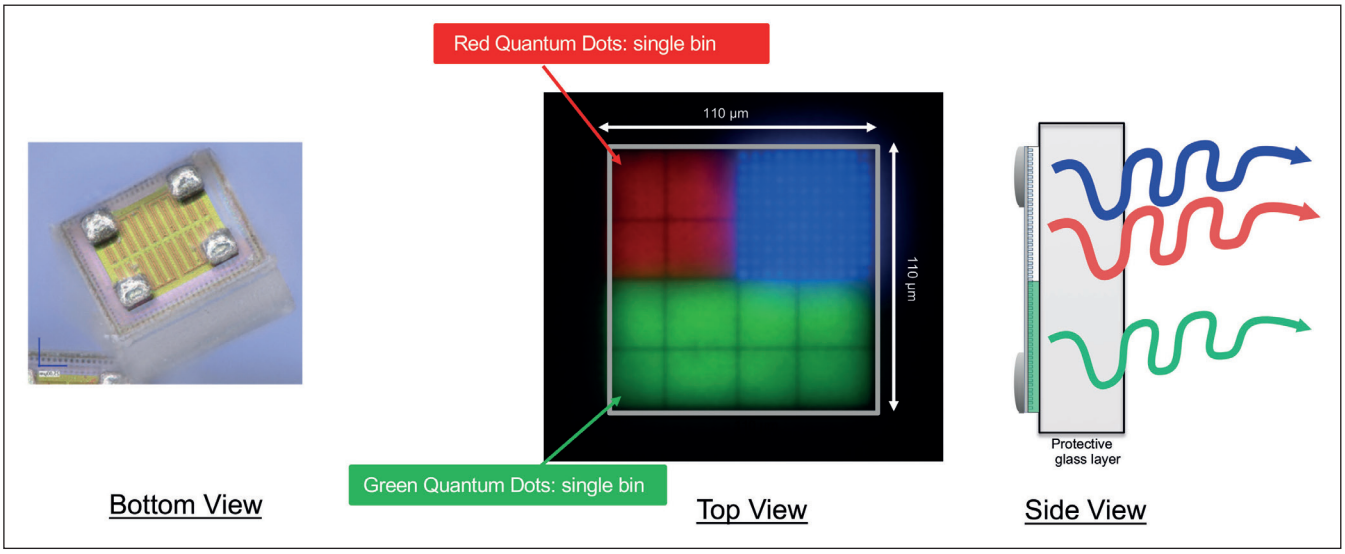
with a large grey scale range (bit depth). Note that size-independent efficiency is not found in 2D LEDs, with efficiency falling for blue microLEDs with dimensions below 30 μm (see Figure 4(c)).

Our device with a single nanowire can be considered to be the smallest microLED. This emitter, just 1.5 μm in diameter, has a state-of-the-art efficiency. Such characteristics inspire a re-thinking of microLED display economics.

For our technology to serve in displays, as well as blue light emitters, we need those that emit efficiently in the green and red. To produce high-performance, vibrant green and red sub-pixels, we use a patternable colour-conversion technology that's based on cadmium-free quantum dots. Processing takes place at the wafer-level, using standard microelectronic tools. By adopting this approach, we can pattern from the centimetre-



➤ Figure 6: Aledia 3D technology can address both large displays (greater than 60-inch) and mid-size displays.

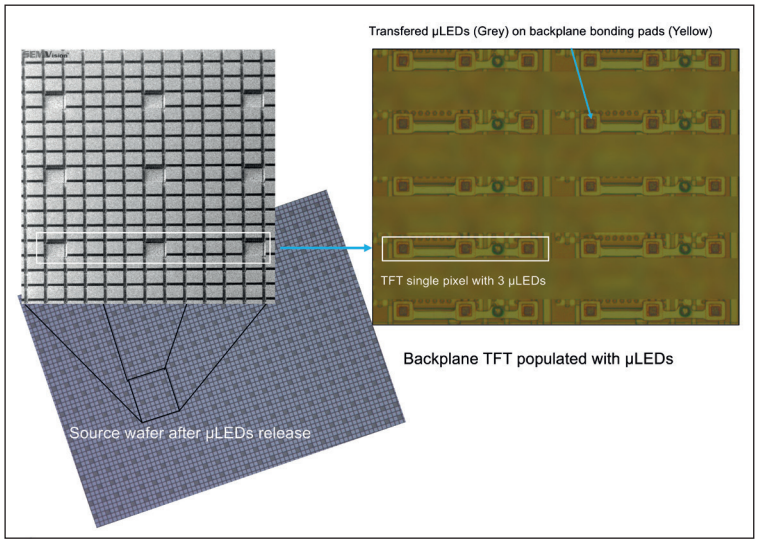


➤ Figure 7. (a) Four-contact RGB pixels (160 µm x 160 µm). Bottom view highlights the four bumps, top view demonstrates the working pixel under electroluminescence and the side view illustrates the pixel architecture with a protective glass layer.

scale down to just 3 µm (see Figure 5 (a)). Our sub-pixels are defined with a high spatial resolution (Figure 5b), and through the use of specific designs we realise appropriate inter- and intra-pixel contrast. Colour conversion provided by the dots is excellent, in terms of both wavelength stability and reproducibility. Illustrating this point, we have obtained a single-wavelength bin after conversion on a full 200 mm wafer, despite variations in the blue emission wavelength. The control over colour has enabled us to record a colour point with a DCIP3 overlap of more than 90 percent (see Figure 5 (c)). We expect further gains on this front in the short term, leading to 100 percent DCIP3 coverage. We can already access raw quantum dot material with a quantum yield of around 75 percent.

For our display technology, one important metric is the photon conversion efficiency, defined as the proportion of impinging blue photons converted into extracted green/red photons. This metric depends on the level of absorption of blue light from the quantum dot resist, the quantum yield, and the possible reabsorption of green/red light. We are continuing to make progress, and today we are realising green and red conversion efficiencies of more than 40 and 50 percent, respectively, for 55 µm by 55 µm subpixels (see Figure 5 (d)).

The performance we are realising with our nanowire microLEDs enables us to address the requirements of different display markets. In the remainder of this article we will focus on the demands for mid-size and large-size displays (see Figure 6).



➤ Figure 8. Direct mass-transfer, involving the transition of microLEDs from the source wafer to the TFT backplane.

Improving video walls

For large displays, like video walls, there's a need to realise a finer pitch, especially for 4K resolution in a 110-inch display – that requires a pitch of 0.625 mm. With this type of display space is limited, while the driving circuitry is becoming more and more complex to handle.

To support this type of display, we have introduced a 160 µm by 160 µm single-chip RGB LED called the LD0001 (see Figure 7). This device integrates blue-emitting nanowire technology, with more than a hundred nanowires in each pixel, with quantum dot conversion for realising green and red emission. The product also has four bumped pads to support electrical interconnections. Due to current flowing in GaN material for all three colours, they have consistent thermal and electrical behaviour. Just a single bin for both the green and the red emitters is possible, thanks to tremendous wavelength stability for the quantum dots.

Our RGB pixel can be transferred to a backplane – it could be a TFT or a PCB – that provides the driving circuitry. Thanks to the use of an integrated pixel,

➤ Aledia's volume production fab.

just a single transfer is needed from the wafer to the backplane. That's a big advantage over the standard pick-and-place approach for 2D LEDs that requires three transfers – one per colour. Due to the high number of nanowires in each subpixel, there is a built-in redundancy with our microLEDs, reducing pre-assembly sorting, lowering defectivity, reducing repair and ensuring very good reliability (there is no cataleptic failure).

Another strength of our technology is that it enables more efficient driving of the display. The voltage drop in the output stage of a TFT-based display typically exceeds 4 V, resulting in more than half the panel power being wasted. Due to this, it is advantageous to connect, in series, two or three groups of microLED per subpixel. In such a configuration each subpixel has an operating voltage that is higher by a factor of two or three. Therefore, to produce the same brightness, the driving current of the LED should be two or three times lower. In turn, this dramatically reduces joule losses in the lines, combats voltage drop, and slashes the power wasted in the TFT without sacrificing the footprint advantage.

There is much interest in what is referred to as the 'smart pixel', which can be realised during the co-integration of the light-emitting module with the driving module. We are developing such a technology, which involves monolithic stacking, at the wafer level, of the RGB LED and the CMOS controlling/driving circuit. Our first product incorporating smart pixels will be the SP1001. It will integrate three-colour drive electronics with an on-chip memory of 19 bits of data per colour. Other features will include pulse width modulation driving, an additional 7 bits for intensity trimming, and an idle current of just 12 nA. As only four interconnections are required, the SP1001 is able to employ an active-matrix architecture with a two-metal layer PCB and a pitch down to 0.3 mm.

Targeting mid-size displays

Our technology is also a compelling candidate for mid-size displays, such as laptops and smartphones. For these displays, we have a product built on 200 mm or 300 mm wafers, and employing vertical microLEDs with single nanowires and 3.5 μm by 3.5 μm chips. We are developing a direct mass-transfer method for moving these vertical microLEDs, at the right pitch for the TFT, directly from the wafer to the TFT backplane, without any manipulating (see Figure 8).

Using on-panel post-processing, we can add a top contact. Our technology ensures precise colour conversion and has additional strengths that include: excellent light extraction; contrast enhancement; and a redundancy strategy (two times or three times), thanks to the cost-effectiveness of our ultra-small microLED chips that results in a dramatic reduction in the required chip transfer yield.

To appreciate the benefits of this redundancy, let's consider a 4K display with 8.3 million pixels and 25 million sub-pixels. To meet the requirement for zero dead pixels, when using a three-times redundancy, our display manufacturing yield can hit 99 percent when there is only a 99.95 percent yield for chip transfer. With this approach we can avoid repair after transfer. While at first glance, a three times redundancy would suggest high expenditure, thanks to the extremely small size of the microLEDs, additional spend on them is lower than any repair cost.

There is much to like with our technology, including the use large silicon substrates, very high efficiencies for incredibly small microLEDs, and the capability of products that enable more efficient driving of the display. To bring the nanowire technology to high volume manufacturing, we have built a volume production fab on the outskirts of Grenoble, France. This year we started to install equipment in this fab, which will support a ramp in production in 2024.

FURTHER READING

➤ T. Lassiaz *et al.* "Nanoscale Dopant Profiling of Individual Semiconductor Wires by Capacitance–Voltage Measurement." Nano Letters **21** 3372 (2021)

Enabling coherent optical communication with InP PICs

Combining InP PICs with state-of-the-art silicon CMOS process nodes creates an incredibly efficient coherent technology with exceptional date rates

BY PAUL MOMTAHAN FROM INFINERA

EMERGING in the late 2000s, coherent optical technology has revolutionised optical transport over long-haul, submarine, data centre interconnect and metro networks. Prior to the introduction of this technology, optical communication had a more primitive format, involving simply on/off modulation. Commonly referred to as intensity-modulation direct detection, this previous standard involved transmitting one bit per symbol for each wavelength, initially at 2.5 Gbit/s and then 10 Gbit/s.

The migration to coherent modulation has underpinned tremendous increases in wavelength speed, spectral efficiency and fibre capacity. Wavelength speed shot up from 10 Gbit/s to 100 Gbit/s, then to 200 Gbit/s, 400 Gbit/s, 600 Gbit/s, and most recently 800 Gb/s. And that's certainly not the end of the line, with even higher-speed coherent engines poised to hit the market, including the 1.2 Tbit/s ICE7 from our company, Infinera.

Fibre capacity is benefitting from the increase in wavelength speed. For the extended C-band, having a bandwidth of 4.8 THz, fibre capacity has evolved from 960 Gbit/s (e.g., 96 x 10 Gbit/s) to 9.6 Tbit/s (e.g., 96 x 100 Gbit/s) and most recently to more than 40 Tbit/s (e.g., 53 x 800 Gbit/s).

There are also other advantages that come from the introduction of coherent technology. One is a simpler optical infrastructure, as there is no longer a need for a carefully planned dispersion compensation module placement. Another is that coherent technology can now provide data rates of 400 Gbit/s in compact pluggable form factors, such as QSFP-DD, that can be plugged directly into non-transport host devices, such as routers. What's more, power consumption is lower than ever – it fell from approximately 5 W/G with 10 Gbit/s to around 2 W/G with the first generation of 100 Gbit/s coherent, and is now around just 0.05 W/G with today's 400 Gbit/s pluggables. So how do these miraculous devices work, and what role does InP play in them?

Inside a coherent optical engine

To understand the role of InP, one must understand the building blocks and functions inside a coherent optical engine (see Figure 1). In these engines there are three basic, high-level building blocks: a digital ASIC/DSP, analogue electronics, and photonics. Often the analogue electronics and photonics are packaged together as a transmit-receive optical sub-assembly. Together with the RF interconnects and packaging, these three basic building blocks constitute a coherent optical engine. Note, though, that each of these blocks actually consists of multiple functions.

Leveraging state-of-the-art silicon CMOS process nodes – such as 7 nm, but evolving to 5 nm, then 3 nm and beyond – in the digital ASIC, often referred to as simply 'the DSP', there are digital signal processing (DSP) functions for the receive and transmit directions and the digital-to-analogue converter (DAC) and the analogue-to-digital converter (ADC). In addition, digital ASICs tend to incorporate other functions, such as forward-error correction, framing, multiplexing, encryption and performance monitoring.

In the transmit direction, drivers take the low voltages from the DAC and convert them to higher voltages required by the modulator. Meanwhile, in the receive direction, the transimpedance amplifiers take the currents from the photodetectors and convert them to the voltages required by the ADC.

The analogue electronics building block, typically packaged as a single ASIC, is made from a material other than the CMOS silicon used for the digital ASIC. For example, in Infinera's coherent engines, analogue ASICs are made from SiGe.

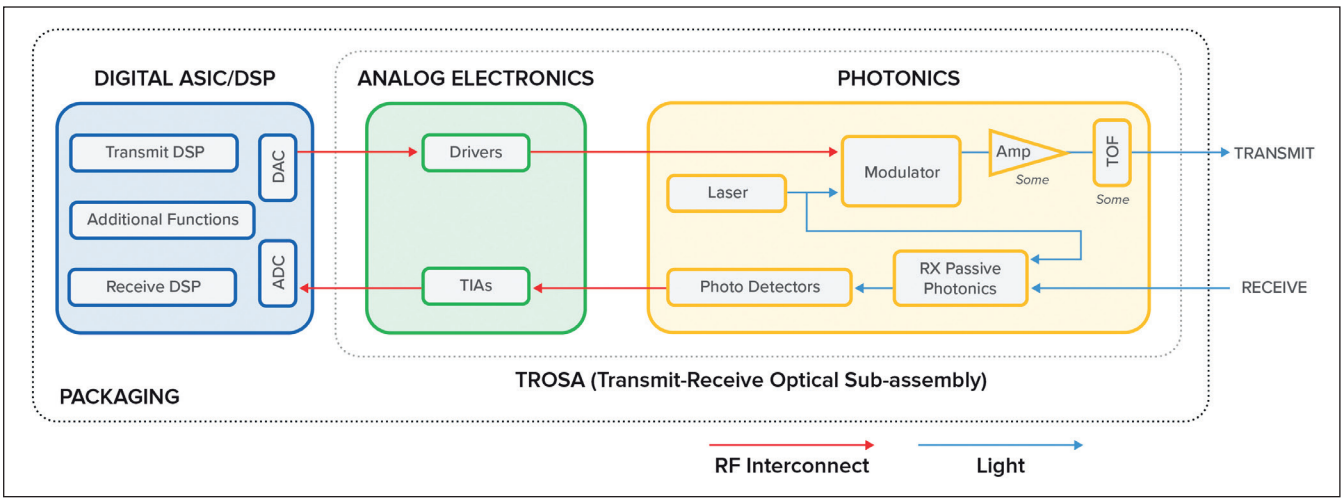
Inside the photonics

For the third building block, which provides photonics, the key transmit functions include the laser and the modulator. Generating light with the required frequency, the laser is always made from InP. Its emission is coupled into the modulator, which encodes data by changing the phase and amplitude of the light, using an electric field to alter the refractive index of the material the light passes through.

A coherent modulator leverages four Mach-Zehnder modulators. Each splits the light into two arms, with phase changes either taking place in one arm, or more typically both arms. When the light is subsequently combined, interference controls the resulting amplitude. As a pair of phase-shifted Mach-Zehnder modulators are needed to control amplitude and phase, four are required for coherent transmission, due to the two polarisations.

There are a number of other components inside a coherent modulator. They include splitters, combiners, phase shifters, a polarisation rotator and a polarisation beam combiner. In addition, some coherent engines include an amplifier in the transmit direction to boost the wavelength power. Depending on the type of amplifier, a tuneable optical filter might also be included, to minimise this amplifier's out-of-band noise.

The receive direction contains passive photonics and photodetectors. The passives include: a polarisation beam splitter, which separates the two polarisations of the coherent signal; and a pair of 90° hybrids, which extract the phase and amplitude from each polarisation, in the form of the in-phase and quadrature components. The role of



➤ Figure 1: Coherent optical engine high-level building blocks

the photodetectors is to detect light and convert it to electrical current. There is also a laser in this part of the photonics building block, employed to help extract phase information from the received modulated wavelength. In many devices, this laser is also used in the transmit section. However, in devices such as Infinera's ICE6, separate lasers are deployed for transmit and receive.

Photonic integrated circuits

When coherent optical engines were in their infancy, their photonics building blocks were constructed from hundreds of discrete components, connected with coupling optics. But this design is certainly not ideal. It led to bulky, expensive devices with a less than optimal mean time between failure. Pioneered by our company, originally for pre-coherent optical communication with the first 10 x 10 Gbit/s PICs in 2005, this issue can be addressed through photonic integration of hundreds of previously discrete photonic components into a single chip (see Figure 2).

Mirroring the factors at play with conventional electronics, the use of advanced fabrication and integration capabilities enables the manufacture of one PIC to be far more cost-effective than that associated with making many individual optical components, prior to the integration and packaging of them. PICs also have the upper hand on many other fronts, with strengths that include a far smaller footprint, enabling the miniaturisation of optical devices, and lower power consumption. Another asset is minimised optical coupling losses, reduced by replacing coupling optics with discrete components with waveguides that connect the optical functions inside the PIC. Using waveguides for coupling also ensures fewer equipment failures, because this eliminates coupling optics as a source of failure.

Benefits of InP

Manufacturers of communications components and equipment have two material options for their PICs: InP and silicon. Deciding between them requires a weighing up of various pros and cons. The only candidate for providing the laser and optical amplification functions at DWDM frequencies is InP, so some of this material will always be present in coherent optical engines. Silicon falls short in this regard, due to its indirect bandgap that causes excited electrons to generate heat rather than light. Consequently, silicon photonics tends to be used with external DWDM lasers and amplifiers.

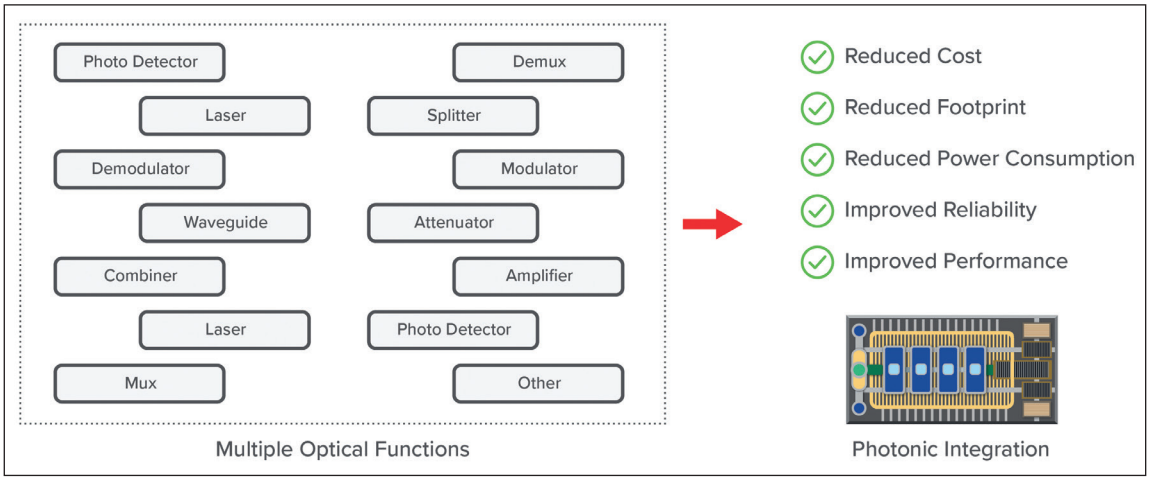
One promising approach to overcoming this drawback that has attracted substantial research and development is the heterogeneous integration of light-emitting materials, such as InP, into silicon PICs. However, this form of integration requires a specialised silicon foundry line. Due to this, heterogeneous integration is not currently supported as a standard offering by silicon foundries.

As well as its excellent light-generating characteristics, InP has an inherently superior modulation effect. This is a major asset for the highest-performance embedded segment of the coherent optical engine market. In addition, InP can detect DWDM light. That's not the case for silicon photonics, which leverages the integration of germanium for this function.

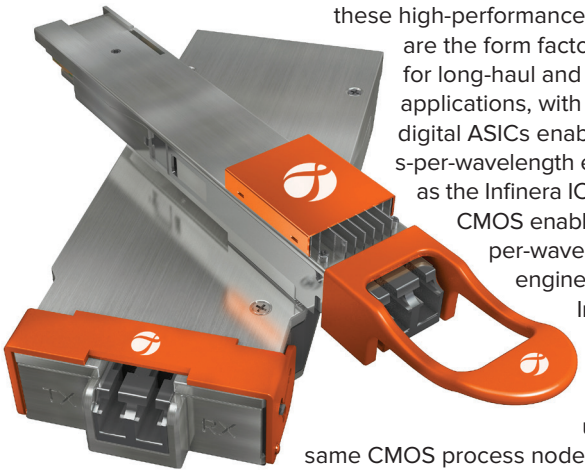
Today, several silicon foundries are enabling silicon photonics to be manufactured on legacy CMOS production lines, with the resulting chips using external light sources and amplifiers. This service lowers the barriers to entry for vendors that want to manufacture PICs but lack the necessary manufacturing expertise and facilities. For simpler applications, access to these foundries allows companies to produce products based on silicon photonics that have a cost advantage in very high volumes, such as millions of units per year.

Due to the evolution of CMOS process nodes and diversifying market requirements, the coherent optical engine market is bifurcating into two distinct segments: high-performance embedded optical engines and compact coherent pluggables.

High-performance engines draw on larger, more powerful and more power-hungry digital ASICs to deliver the highest possible baud rates and advanced features that maximise wavelength capacity-reach and spectral efficiency. Embedded in transponders,



➤ Figure 2: Photonic integration benefits



these high-performance engines are the form factor of choice for long-haul and submarine applications, with 7 nm CMOS digital ASICs enabling 800 Gbit/s-per-wavelength engines, such as the Infinera ICE6, and 5 nm CMOS enabling 1.2 Tbit/s-per-wavelength engines, such as the Infinera ICE7.

At the same time, using the same CMOS process node, coherent DSP designers have built ASICs that are more optimised for low power consumption and a small footprint. This focus has enabled 400 Gbit/s in QSFP-DD, OSFP, and CFP2 pluggable form factors. The 400 Gbit/s pluggables produced with 7 nm CMOS digital ASICs are available in a variety of flavours: 400ZR for point-to-point data centre interconnects up to 120 km; ZR+ as an umbrella term for 400 Gbit/s pluggables with enhanced performance; and XR optics, which also provides a transformative point-to-multi-point option.

As well as the generic advantages already discussed, InP PICs provide specific advantages for both types of optical engine. In the high-performance embedded segment, the electro-optic modulator effect in InP is inherently superior to silicon's plasma dispersion effect, enabling a phase change that's up to ten times higher for a given unit length and voltage. Thanks to this, InP enables more compact, power-efficient modulators that ensure lower loss, superior linearity, a larger modulation voltage for a higher transmitter signal-to-noise ratio, and thus a greater reach.

For compact pluggables, a key advantage of InP is associated with the integrated amplification required for a high transmit power. Coherent pluggables incorporating silicon photonics tend to have a low transmit power, typically around just -10 dBm, which is well short of that required by existing optical line systems – they need a transmit power of around 0 dBm. An imperfect solution is to integrate silicon photonics with an erbium-doped fibre amplifier, and add a tuneable optical filter to block out-of-band noise that's introduced with the additional amplification. But there's a price to pay, as the introduction of these additional components increases cost and power consumption. A far better option is InP-based pluggables. They include the Infinera ICE-X, which delivers a high transmit power by integrating a semiconductor optical amplifier into the PIC.

What's next?

In the high-performance embedded segment, evolution vectors include: higher baud rates; improved spectral efficiency and fibre capacity; advanced features related to nonlinear compensation, advanced modulation, forward-error correction, monitoring and automation; support for space-division multiplexing; and novel fibre types, such as multi-core fibres, multi-mode fibres and hollow-core fibres. However, as this sector starts encroaching spectral efficiency limits, there is much discussion over whether it makes sense to have one very high-speed interface (i.e., 3.2 Tbit/s) or multiple lower-speed interfaces (i.e., 2 x 1.6 Gbit /s). InP PICs have a strong role to play in both scenarios, with a proven path to 200+ Gbaud and the ability to integrate transmit and receive for multiple wavelengths into a single PIC. Demonstrating this capability are the latest coherent optical engines produced by Infinera, such as the ICE6 (2 x 800 Gbit/s) and the ICE4 (6 x 200 Gbit/s).

In the pluggable segment, likely introductions include low-power 100 Gbit/s for the metro edge, higher speeds (800 Gbit/s, 1.6 Tbit/s) for metro and data-centre interconnects, and longer reach enabling long-haul use cases. Undergoing debate is the role of coherent technologies inside the data centre, with some vendors targeting campus data centre interconnect applications with simplified 800 Gbit/s coherent engines, such as 800LR. Due to the need to reduce data-centre power consumption – a growing concern as artificial intelligence clusters and workloads are sure to scale – huge strain is being applied to data-centre power and cooling infrastructure. A strong contender to help to relieve this strain are InP modulators. Operating at low voltages and powers, these components are compelling candidates even in non-coherent intensity-modulated direct-detect transceivers that dominate today's data centres.

Beyond optical communications, InP PICs are a promising technology for a wide range of emerging and potential applications. These include defence, automotive lidar, 3D sensing for wearables and smartphones, solar cells, and medical sensing. This class of PICs could also have a role to play in quantum computing and in neuromorphic computing for AI and machine learning.

High-power lasers: wells or dots?

When it comes to satellite communication, is it better to use high-power lasers with quantum wells or variants that employ quantum dots?

BY YONGKUN SIN FROM THE AEROSPACE CORPORATION

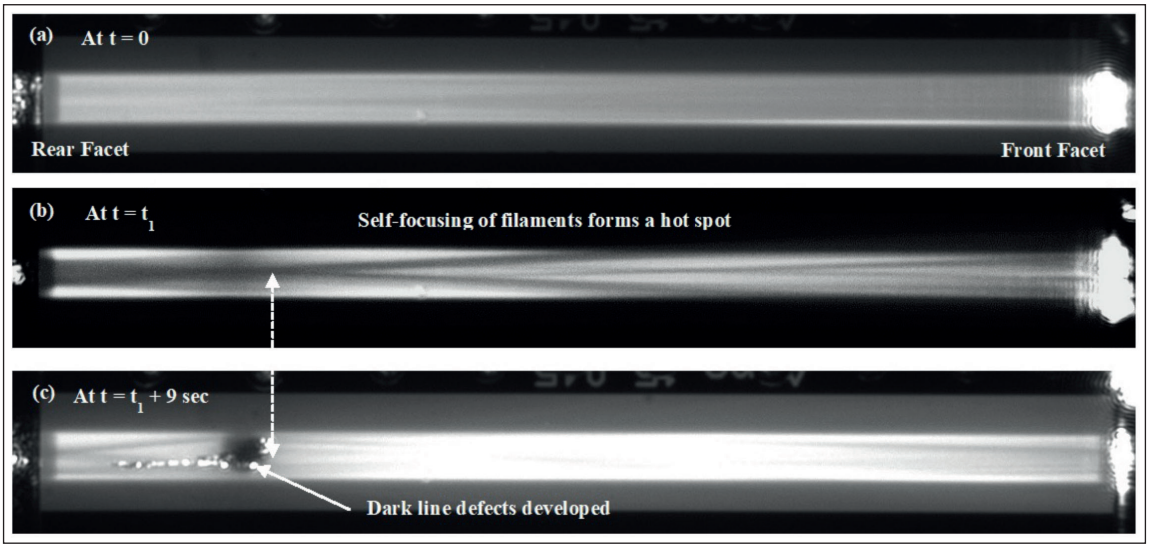
THIS DECADE will witness significant growth in the satellite communications market. That's good news for the makers of high-power broad-area lasers that emit between 915 nm and 980 nm, because these sources are a critical component in space satellite communications systems. For example, SpaceX, the company led by Elon Musk, uses Starlink satellites that are equipped with laser links to help to drive down latency on the internet network for satellite broadband. Note that plans for SpaceX include using lasers on future Starlink satellites for the transmission of information between them while in orbit.

At the heart of the broad-area lasers deployed in space are strained quantum well active regions made of an InGaAs-AlGaAs heterostructure. As well as a high level of efficiency, these broad-area lasers with a single InGaAs quantum well produce unprecedented high-power operation, thanks to efforts to understand and combat causes of device failure. Investigations have uncovered the origins of facet catastrophic optical damage or catastrophic optical mirror damage in GaAs-based lasers and led to the development of techniques such as facet passivation to significantly increase the threshold for the cause of facet failure. These advances have enabled broad-area lasers with a waveguide width of around 100 μm to produce CW output powers of over 20 W. However, while this progress is very encouraging, these lasers are still susceptible to catastrophic optical damage, which can cause catastrophic and sudden degradation. That's a major concern for space applications. So, to understand the origins of this failure, our group at The Aerospace Corporation has delved into this matter, finding that these broad-area lasers predominantly degrade by a new failure mode that's associated with catastrophic optical bulk damage.

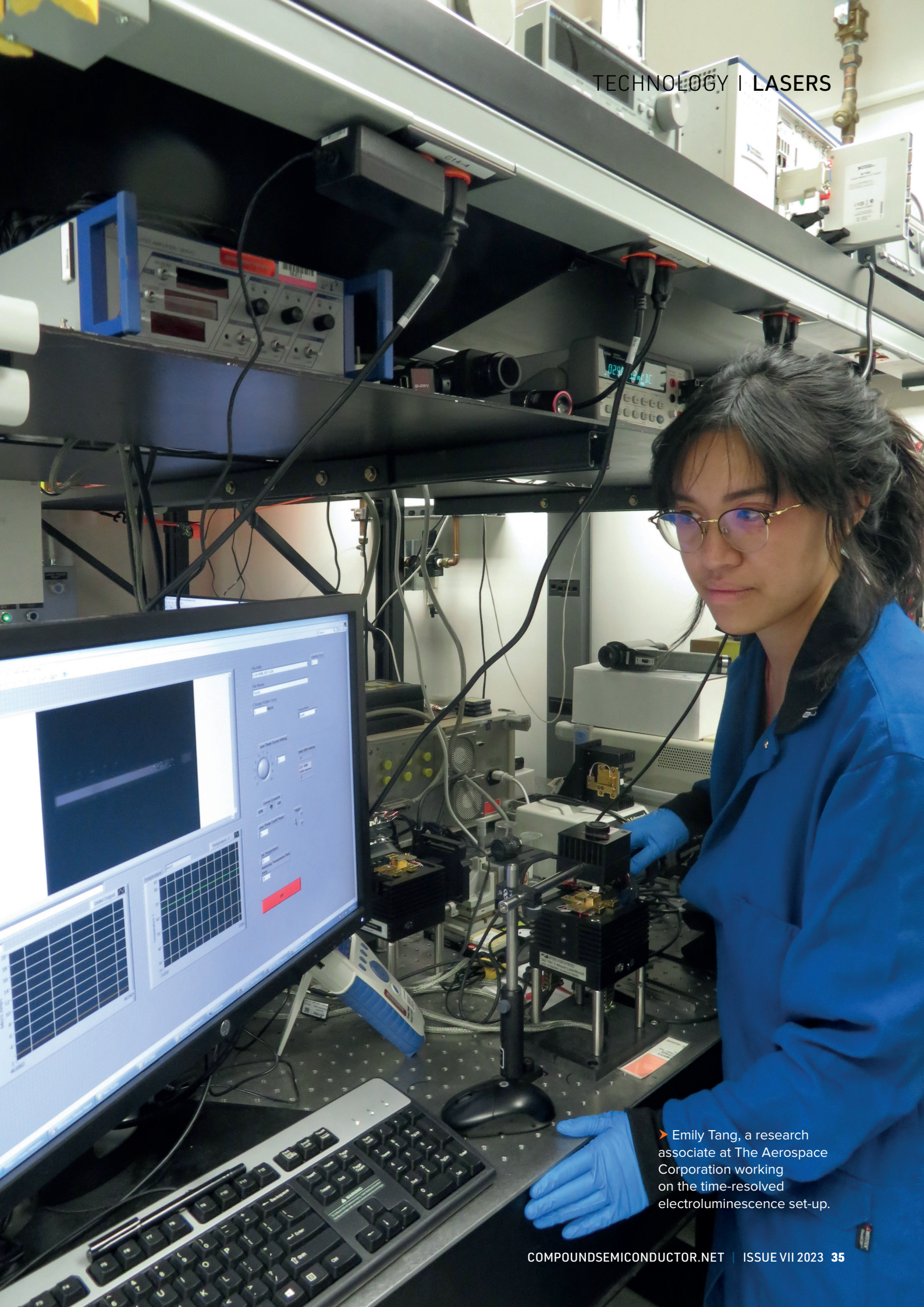
An alternative class of laser that could provide the source for satellite communication is the InAs-GaAs quantum dot laser. Recently, this emitter has attracted much attention as a potential successor to quantum well lasers in silicon photonics, with the three-dimensional confinement of carriers in the active region promising to suppress nonradiative recombination of carriers at growth and radiation-induced defect sites. This asset makes the quantum dot laser an attractive candidate for space applications. However, its failure modes and mechanisms are still not understood. To help address this lack of knowledge, we have compared the degradation processes in high-power broad-area lasers with quantum well and quantum dot active regions. Read on to discover our findings.

Device designs

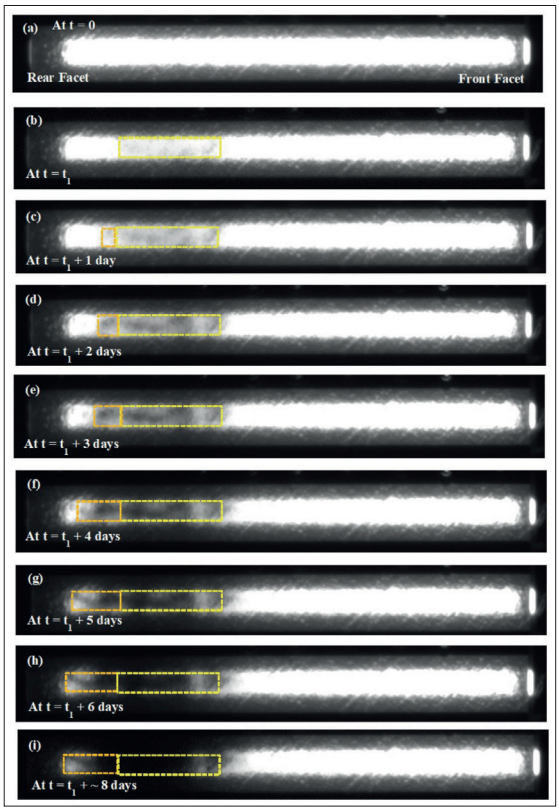
We have studied quantum well and quantum dot lasers that share the same geometry. Both have 2 mm-long cavities and waveguides 100 μm wide.



➤ Figure 1. Electroluminescence images of a quantum well laser showing self-focusing of filaments (b) and development of dark line defects (c).



Emily Tang, a research associate at The Aerospace Corporation working on the time-resolved electroluminescence set-up.



➤ Figure 2. Electroluminescence images of a quantum dot laser showing the development of dark area defects.

These lasers have been passivated and had anti-reflection and high-reflectivity coatings applied to their facets. In addition, windows have been introduced in the backside *n*-metals during the fabrication of these laser diodes, to allow us to directly observe spontaneous emission from the entire laser cavity.

Our strained quantum well lasers, emitting between 960 nm and 980 nm, are grown by MOCVD and contain an InGaAs graded-index separate-confinement heterostructure that is sandwiched between the AlGaAs cladding layers. In comparison, the InAs-GaAs quantum dot lasers, emitting at around 1 µm, are grown by MBE, with dots formed by the Stranski–Krastanov process. These lasers contain ten stacks of InAs quantum dots.

To evaluate both our quantum well and our quantum dot window lasers, we have attached them to C-mounts, using a *p*-side down configuration. As the lasing wavelength of both of these lasers is transparent to the GaAs substrate, it is easy for us to observe the optical intensity distribution within the active layer through the substrate.

Comparing quantum well lasers...

Our room-temperature measurements reveal that the quantum well laser has a threshold current of 280 mA, a slope efficiency of 0.9 W/A, a peak power conversion efficiency of 50 percent, and an external differential quantum efficiency of 0.71. In comparison, when the quantum dot laser is measured at room temperature it has a threshold current of 700 mA, a slope efficiency of 0.8 W/A, a differential resistance of 0.1 Ω, a threshold voltage of 1074 mV, and optical output power of 3.5 W at 6 A.

Near-field profiles for the two types of lasers are markedly different. The quantum-well laser has an array of filaments, with around 10 maxima and a typical filament spacing of 10 µm. In comparison, near-field profiles for the quantum dot lasers reveal significantly suppressed filamentation. The most probable cause of this difference is that the quantum dot lasers have a much smaller linewidth enhancement factor than their quantum-well cousins. We have undertaken accelerated life-tests, monitoring laser diode parameters, such as optical power, current and voltage, for a range of heatsink temperatures. This has allowed us to determine aging behaviour – be it rapid, gradual, or catastrophic/sudden – and failure times.

To gain insight into degradation processes in both types of lasers, we have also captured electroluminescence images from the window regions in real-time during the entire life-tests until device failure. With this technique, offering a nominal spatial resolution of 2 µm/pixel, we typically collect one electroluminescence image per second for the duration of the life-tests. These images allow us to observe quite a few critical events in real time, including self-focusing of filaments, formation of dark spot and dark line defects, and the propagation of dark line defects.

Snapshots of time-resolved electroluminescence images from our quantum well laser are shown in Figure 1. We drove this laser under continuous-wave operation at 6 A, using a heatsink temperature of 70 °C. Comparing images at times t = 0 and t = t_1, it is easy to spot the precursor signature of failure – self-focusing of filaments, indicated by the dotted white arrow.

This self-focusing, which causes the filaments to converge via thermal lensing, stems from local gain saturation and spatial hole burning. We find that the optically induced heating that results from self-focusing of filaments significantly increases the temperature within a localised area, thus forming a hot spot. Our electroluminescence images indicate that dark line defects develop at that location at t_1 + 9 s (the initiation point of these defects, shown in Figure 1 (c), is highlighted by the dotted white arrow). As the dark line defects develop, the power produced by the laser reduces significantly.

During device operation, pre-existing point defects in the active layer are transformed into defect complexes via a recombination-enhanced defect reaction process. During this process, the point defects migrate, react, and dissociate. This degradation comes from a defect reaction that is

enhanced by the non-radiative recombination of carriers. Note that the non-radiative recombination processes at the sites of non-radiative recombination centres generate thermal gradients during device operation.

One of the consequences of nonradiative recombination is that it leads to local heating, which subsequently increases optical absorption. Assuming an absorption coefficient of 200 cm^{-1} with no local heating in the quantum well lasers, the absorption coefficient increases to 8.7 x 10^4 cm^{-1} for local heating of 130 °C. Local heating of 130 °C is one of the three critical temperatures prior to quantum well laser degradation. We have found that when the local temperature reaches around 130 °C, the local area begins to strongly absorb lasing photons. In turn, filamentation and self-focusing of filaments resulting from local gain saturation and spatial hole burning start to play a critical role.

Another impact of local heating is that it creates a thermal lens, which also leads to local gain saturation. The thermal lens can cause a narrowing and self-focusing of the optical beam as it propagates, leading to a significant increase in the local optical power density (see the dotted white arrow in Figure 1 (b)). As thermal lensing can further enhance the self-focusing of filaments as they propagate along the longitudinal axis, it is likely that the optical intensities at local areas critically depend on thermal gradients.

When a local temperature rise exceeds 130 °C, the hot spot created by the optically induced heating can accelerate the recombination-enhanced defect reaction process and cause nonradiative recombination centres to develop into extended defects. Another event occurs when local heating increases beyond 300 °C, with the increase in the absorption coefficient reaching of 2.5 x 10^8 cm^{-1}, and a thermal runaway process commencing. This thermal runaway process may lead to local melting in the quantum well lasers when local heating reaches as high as 1200 °C. However, local melting is not a prerequisite for the generation of extensive dislocation networks.

...and quantum dot lasers

We have also carried out accelerated life-tests on quantum dot lasers, using automatic current control, with our time-resolved electroluminescence set up (see Figure 2 for images captured from one of the quantum dot lasers).

Driving this particular laser at 6.5 A and a heat-sink temperature of 75 °C, we have determined that the first sign of change is a weakly damaged area (indicated by the dotted yellow rectangle in Figure 2 (b), taken at $t = t_1$, and its absence in Figure 2(a), taken at t = 0). There is no evidence of any precursor signature of failure, such as self-focusing of the filaments. This clearly indicates that optical effects are less critical in quantum dot lasers than quantum well lasers, where they are to blame for forming dark line defects. However, electrical and thermal effects appear to be more critical for quantum dot lasers.

Driving quantum dot lasers for longer creates more regions of damage. Each of the electroluminescence images in Figure 2 (c) to 2 (i) has two dotted rectangles, coloured with yellow and orange to indicate original and newly damaged areas, respectively. We have three noteworthy observations from these electroluminescence images: newly damaged areas were mainly developed towards the rear facet; over 7 days the length of newly developed dark area defects increased from around 60 μm to 235 μm; and the patches of weakly damaged areas, or less dense dislocations, became significantly denser over 7 days.

To fully understand the nature of these dislocations, we would need to prepare transmission electron microscopy specimens from a series of quantum dot lasers at different stages of degradation. While that's our future work, we can still suggest a scenario for the degradation: there is a recombination-enhanced defect reaction process that generates dislocations (shown as the weakly damaged area in Figure 2 (b)) from nonradiative recombination centres and point defects in the quantum dot active region. These dislocations slowly propagate via a recombination-enhanced dislocation glide process, shown in Figure 2 (c) – (i). The propagation velocity for this process is much slower than that of dark line defects in quantum well lasers.

Wells versus dots

Our efforts have shown that broad-area lasers with quantum well and quantum dot active regions undergo very different degradation processes. In quantum well lasers, dark line defects form by precursory self-focusing of filaments, thus forming a hot spot; while in quantum dot lasers, dark area defects form with no precursor signature of failure. However, there is common ground, with quantum well and quantum dot lasers showing bulk failures – the former by fast catastrophic optical bulk damage and the latter by slow gradual degradation, possibly via a recombination-enhanced dislocation glide process. Further studies are necessary to fully understand degradation mechanisms in quantum dot lasers, but merits of quantum dot lasers articulated in this article may warrant these lasers in future space satellite systems.

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GaN RF transistors 2.0?

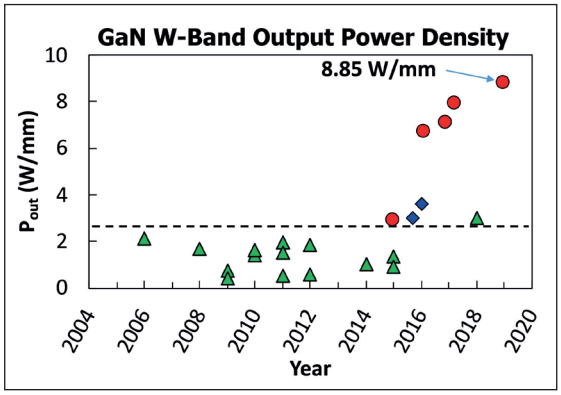
Switching to an N-polar architecture gives GaN transistors greater powers and efficiencies at high frequencies

BY STACIA KELLER AND UMESH MISHRA FROM THE UNIVERSITY OF CALIFORNIA, SANTA BARBARA

WE ARE LIVING in an era of evolving, diversifying wireless technology. As well as advances in existing technology, such as the introduction of additional standards for mobile communication, new opportunities are emerging, including imaging and autonomous driving. For all these applications, the W-band has great potential. Spanning 75 GHz to 110 GHz and earmarked for NR (new radio), this band is positioned at a local minimum of atmospheric attenuation, so it is well-suited for the propagation of electromagnetic waves.

Options for delivering amplification in the W-band include a number of compound semiconductor technologies. One of the candidates is GaN, which offers higher efficiencies and power densities than GaAs and InP.

In its conventional form, GaN delivers a superior performance to other compound semiconductor materials. However, even better results are possible by switching the polarity of this device. This move has enabled novel deep-recess N-polar HEMTs to outperform traditional Ga-polar technology by more than a factor of two in the W-band. Noteworthy results include a record power density of 8.8 W/mm and a power-added efficiency of up to 31.7 percent at 94 GHz. Another asset of these transistors is the constant high-output power density over a wide range of frequencies. Values are as high as 8 W/mm from 94 GHz down to 30 GHz and 10 GHz – this is a behaviour that's never been observed for other types of transistor.



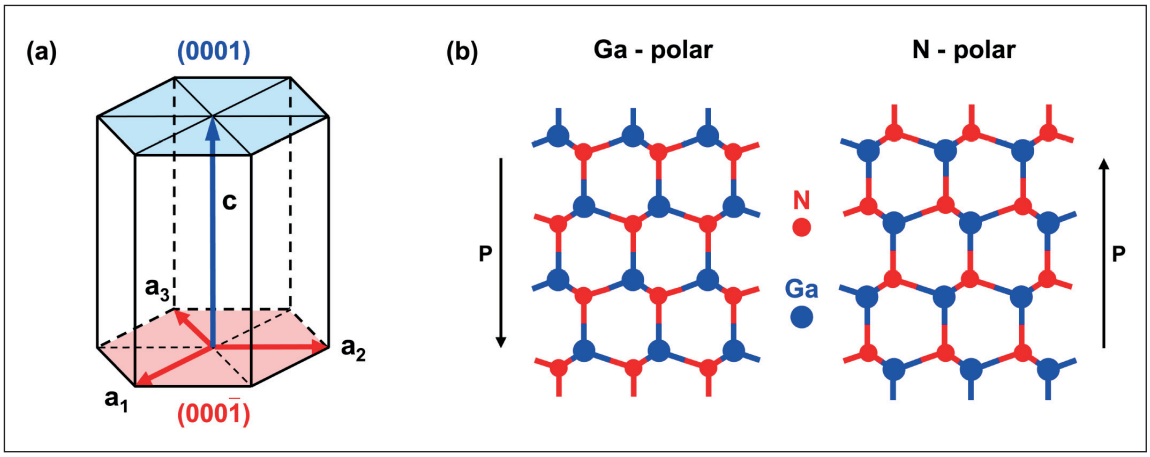
➤ Figure 1. N-polar GaN (circles) provides a breakthrough output-power density relative to traditional Ga-polar transistors (triangles and diamonds).

The team behind these results is our group at the University of California, Santa Barbara. We have been developing N-polar GaN technology for more than a decade, and over that time we have overcome a number of challenges that have led to performance improvements.

Conventional HEMTs

Conventional GaN-based transistors are well known for delivering high powers at high frequencies. This capability is enabled by the large GaN breakdown field, the high electron velocity and the high two-dimensional electron-gas density (2DEG) accessible in group-III nitride heterostructures. When AlGaN/GaN heterostructures for transistor fabrication are grown in the typical +*c*-direction, no doping is needed to form the 2DEG, in stark contrast to arsenide and phosphide semiconductors. This is a consequence of the higher ionicity of the Ga-N bond, compared with the Ga-As and Ga-P bond, that causes group-III nitrides to preferentially crystallise in the wurtzite structure, which is non-centrosymmetric in the *c*-direction. Strong polarisation-based internal electric fields in heterostructures result, giving rise to the formation of a 2DEG at the AlGaN/GaN interface. The Ga-polar (0001) or +*c*-direction of the GaN crystal is the standard growth direction for group-III nitrides, which is also employed for the production of current optoelectronic devices.

Using standard Ga-polar technology, many academic and industrial groups have produced and improved RF devices. At lower frequencies, such as 4 GHz (S band), Wolfspeed has demonstrated output power densities as high as 41.4 W/mm. Beyond our team at UCSB, an incomplete list of other US contributors to the development of these high-performance devices include HRL, Qorvo,



➤ Figure 2. (a) Hexagonal unit cell and (b) atomic structure of Ga-polar and N-polar GaN. Arrows represent the direction of the spontaneous polarization dipole, P, in the GaN crystal. Reprinted from S. Keller *et. al*. Semicond. Sci. Technol. **29** 113001 (2014), with permission from IOP Publishing, Ltd.

SEDI, Wolfspeed, Raytheon and NGC. Efforts by all have assisted the commercialisation of transistors operating in the S, X and K bands. Now commercially available for more than a decade, these devices are deployed in base stations, radar and satellite communication.

Future applications will involve higher operating frequencies, such as those in the V, E, W, and D bands. Here, the power performance of the standard transistors declines. For many years, power densities for transistors in the W-band have rarely exceeded 3 W/mm, and associated power-added efficiencies (PAEs) have been below 15 percent. To improve transistor performance at these high frequencies, there's a need to: scale the transistor gate length, enable high currents and good gate control, and ensure a very low access resistance. Departing from the standard Ga-polar transistor structure makes it easier to succeed on all these fronts.

... enter N-polar GaN

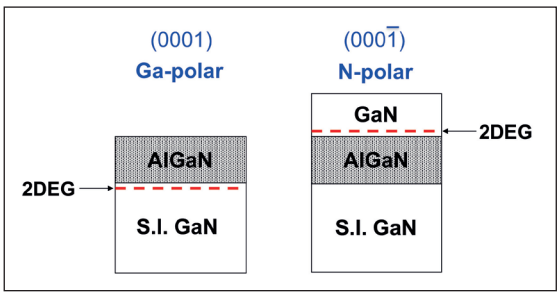
To understand the benefits that come from a switch in polarity, there's a need to take a closer look at the epitaxial layer structure. For the standard Ga-polar transistor structure, which is grown in the (0001) or +*c*-direction, the AlGaN barrier is positioned on top of the semi-insulating GaN base layer; and the 2DEG channel, which forms at the GaN/AlGaN interface, is located below the AlGaN barrier. In contrast, for transistors that employ the N-polar (000-1) or –*c* crystal direction, while the semi-insulating GaN base layer and the AlGaN barrier layer are just as they are for the standard Ga-polar structure, the GaN channel is now positioned on top of the AlGaN barrier.

There are several advantages that come from this difference in the order of the layers. One is that the 2DEG channel can be contacted via the lower bandgap GaN top layer, making it easier to form low-resistance ohmic contacts. Another advantage is that the 2DEG channel is now positioned on top of the AlGaN barrier, with the latter naturally serving as a backbarrier for carrier confinement, leading to improved gate control. The third significant benefit is that the channel charge can now be controlled independently from the channel thickness, enlarging the parameter space when scaling the transistor, where, in order to maintain good gate control, gate length and gate-channel distance must be scaled simultaneously. (A more detailed discussion of these advantages is provided in M. H. Wong *et al*. Semicond. Sci. Technol. **28** 074009 (2013). While not under consideration here, the N-polar orientation also possesses advantages for E-mode devices.)

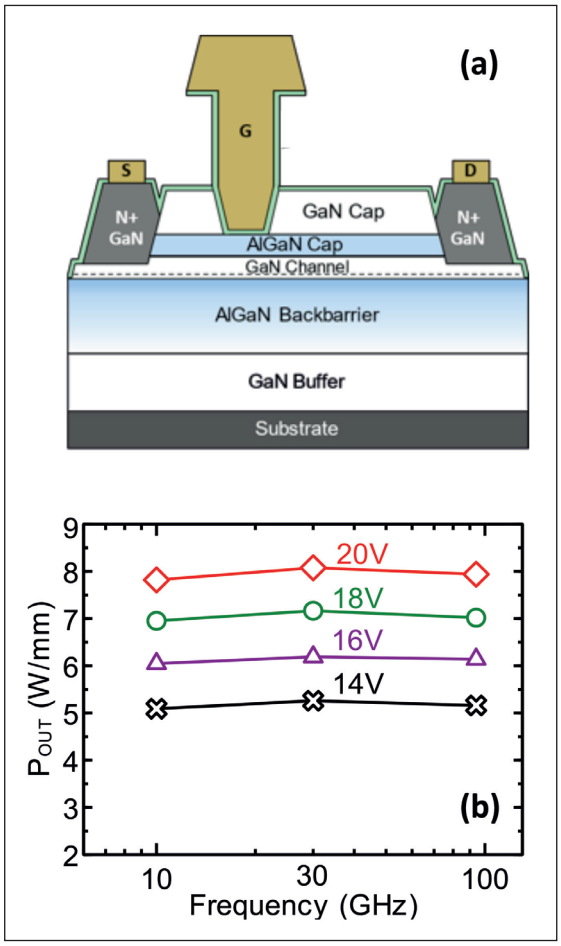
The origin of the difference between these two epitaxial structures is that the internal electric fields are in opposite directions. For N-polar heterostructures, the direction of the internal electric field is helpful for a number of device applications. However, drawing on this benefit is far from easy, due to difficulties in the epitaxy of high-quality N-polar III-nitrides.

Challenging epitaxy

One common approach to realising an N-polar GaN film begins by taking a *c*-plane sapphire substrate, which is a well-used platform for GaN epitaxy, and treating the surface with nitridation. This step, undertaken prior to epitaxy, involves exposure of sapphire to ammonia or atomic nitrogen at high temperatures. Unfortunately, no matter if grown on standard *c*-plane sapphire substrates or on *c*-plane GaN substrates, for a long time N-polar



➤ Figure 3. The layer structure of Ga-polar and N-polar HEMTs. In the N-polar structure the two-dimensional electron gas (2DEG) forms on top of the AlGaN barrier layer.



➤ Figure 4. (a) Schematic of deep-recess N-polar HEMT. (b) Output power density of N-polar deep-recess HEMTs at different operating frequencies and drain voltages. The observed independence of the output power on the operation frequency was never seen for transistors before.

GaN epitaxial films have been infamous for their hexagonal surface hillocks, thought to originate from inversion domains. In addition, these films contained high concentrations of unintentional carbon and oxygen impurities.

The initial breakthrough came in 2004 when a French team reported the first evidence of smooth N-polar GaN, using C-face SiC substrates and growth by MBE. Soon after this, our team could replicate this success and produce smooth N-polar GaN films by MBE, allowing us to start exploring N-polar GaN based heterostructures for device applications. In 2005 we published our first papers describing the properties of the MBE-grown AlGaN/GaN heterostructures, along with our initial transistor results; and in the succeeding years we have shared the details of our more advanced transistor designs.

We have also investigated the use of MOCVD for growing GaN on C-face SiC. Again, we initially observed unwanted hexagonal surface hillocks. However, we found that the shape and size of these hillocks strongly depends on the growth conditions. This suggested that surface processes influenced the crystal growth, which can be engineered by manipulating the step density on the growth surface via crystal misorientation. It is well known that the larger the misorientation angle from the ideal plane – that is, the perfectly flat crystal surface plane – the greater the number of steps that form on the crystal surface, and thus the shorter the terrace length between these steps. We found that when we grow N-polar GaN films on *c*-plane sapphire substrates with different surface misorientations, as the misorientation angle increases, the density of the hexagonal surface hillocks declines substantially. Under a wide range of growth conditions, we have produced hillock-free films using a misorientation angle of 4 degrees.

Note that increases in misorientation angle also improve the structural properties of the N-polar GaN films to the extent that they are then comparable with their Ga-polar counterparts. Another finding is that these smooth N-polar GaN films contain far fewer unintentional impurities. Following optimisation of the MOCVD growth conditions, our N-polar GaN films have residual carbon and oxygen impurity concentrations below 3×10^{16} cm^{-3}. We have also demonstrated N-polar GaN films with properties that are comparable with Ga-polar GaN on misoriented C-face SiC and (111) silicon.

Our development of transistors grown by MOCVD began by investigating device structures for transistors operating at 4 GHz. For this work we initially adopted the epitaxial architecture previously used for our MBE-grown transistors. However, we placed a thin AlGaN layer on top of the GaN channel to mitigate gate leakage. This led to a layer structure of semi-insulating GaN, followed by AlGaN, 25 nm-thick GaN and 2 nm-thick AlGaN.

The performance of these N-polar transistors fully matched their Ga-polar counterparts. We recorded output power densities of 12 W/mm and 20.7 W/mm on sapphire and C-face SiC substrates, respectively. Independent of polarity, the higher thermal conductivity of SiC enabled device operation at higher voltages, and thus higher output power densities. Our results demonstrated the high quality of N-polar GaN/AlGaN/GaN heterostructures grown by MOCVD, and assisted our development of scaled transistors operating at higher frequencies.

To realise transistor operation at 94 GHz, we reduced the GaN channel thickness to 12 nm and introduced a GaN cap layer on top of the epitaxial stack to enable the fabrication of a deep-recess transistor. The GaN top layer delivered two benefits: it moved the surface away from the 2DEG channel, mitigating DC-to-RF dispersion (a phenomenon where the RF performance of the transistor lags behind the one expected from DC testing); and lowered the access region resistance by reducing surface depletion.

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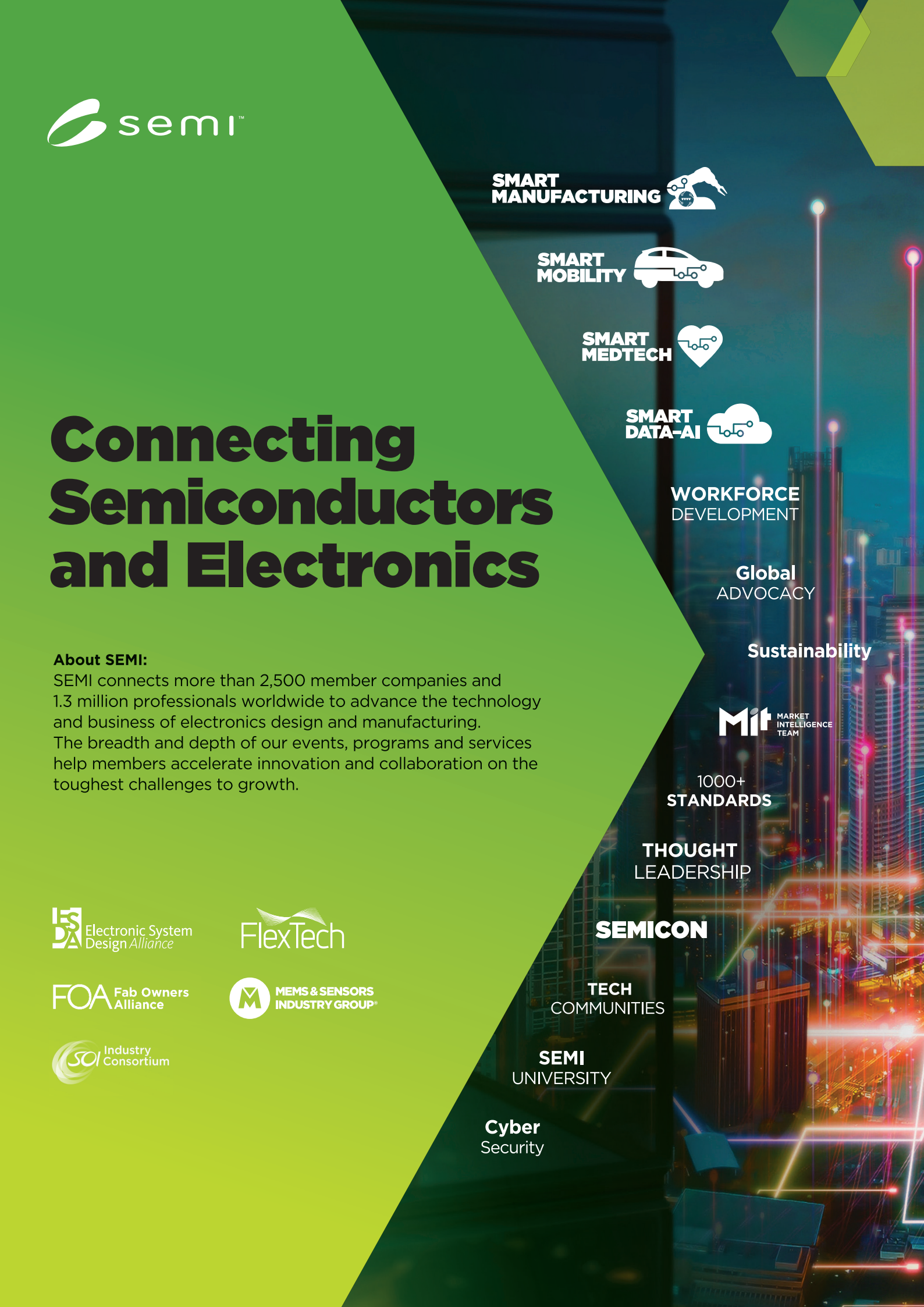
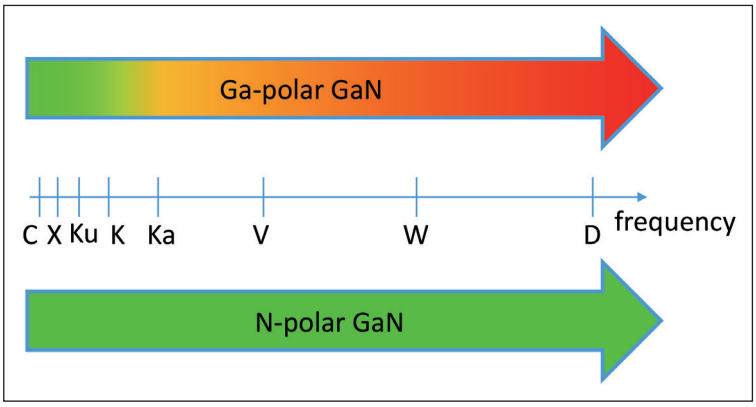


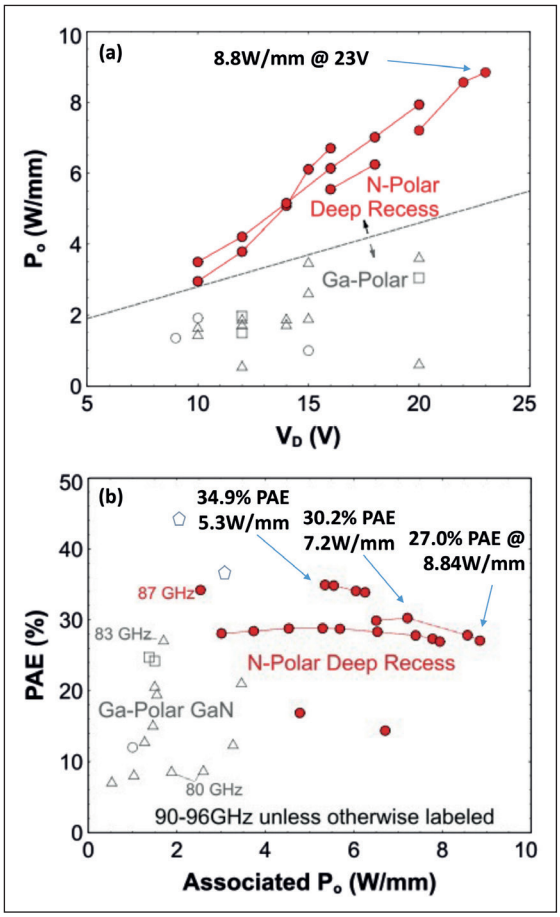


➤ Figure 5. N-polar GaN can serve the full electromagnetic spectrum of interest through D-band.

We reported the results of our first deep-recess N-polar HEMTs on sapphire in 2016, and in the following year the performance of variants on SiC. The latter exhibited a record output power density of 6.7 W/mm and a power-added efficiency of 14.4 percent at 94 GHz. After further optimisation of the device design, we were able to increase the output power density to 8 W/mm at 20 V, and the peak power-added efficiency to 28.8 percent at 16 V. As already mentioned in the introduction, these transistors produce this high output power density over a wide range of frequencies, from 94 GHz down to 30 GHz and 10 GHz, with peak power-added efficiencies of 56 percent and 58 percent at the latter frequencies, respectively.

More recently, we unveiled a power density of 8.84 W/mm (663 mW) with an associated power-added efficiency of 27 percent in 2020; and early this year we announced a single-cell W-band power record of 712 mW, alongside a power density of 7.1 W/mm and a power-added efficiency of 31.7 percent at 94 GHz. Our latest results, announced at the 81st Device Research Conference, are for a transistor with a 1 W output power.

Our body of work demonstrates that compared with standard Ga-polar technology, N-polar deep recess transistors can deliver a higher output power density at a given drain bias, and a higher power-added efficiency at a given output power density. This superiority stems from a high RF current, excellent dispersion control and high gain. The combined outstanding output powers and efficiencies realised with these N-polar deep-recess transistors makes them the leading technology for millimetre-wave applications today – after a nearly 20-year-long journey developing N-polar technology at UCSB.



➤ Figure 6. (a) Output power density, P_o, versus drain voltage, V_D, and (b) power added efficiency, PAE, versus associated output power density, of N-polar deep recess transistors at 90 – 96 GHz unless labelled otherwise. The N-polar HEMTs show a higher P_o at a given V_D indicating high RF current and excellent dispersion control. The latter together with the high gain of the N-polar transistors enable their higher PAE at a given P_o.

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The development of the N-polar HEMT technology at UCSB would have been impossible without the hard work of all the graduate students and post-doctoral researchers (too many to acknowledge but all deeply appreciated) who contributed to the project. This work would also have been impossible without the sustained support of the ONR under contracts supervised by Dr. Paul Maki, sharing the vision that N-polar GaN based transistors could overtake standard Ga-polar technology in performance. Additional support was provided by DARPA under the DREAM program (Drs. Y. K. Chen, Dan Green, and Tom Kazior).

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Yimeng Sang holding a 2-inch green LED wafer with a tunnel junction, regrown by MBE behind her.

Integrating microLEDs and MOSFETs

The monolithic integration of microLEDs and vertical MOSFETs offers a promising pathway for making microLED displays

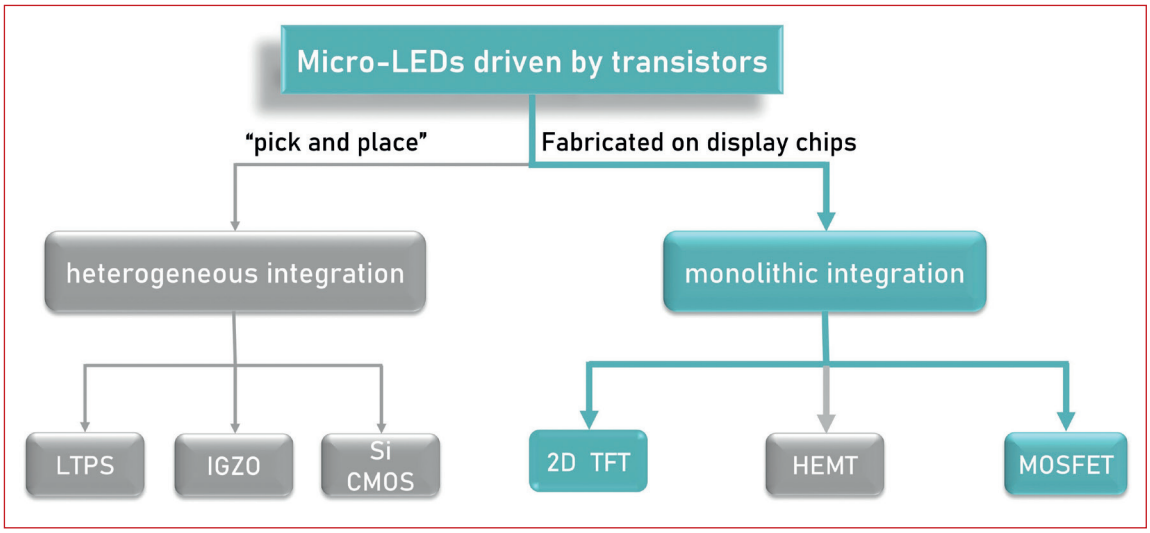
BY ZHE ZHUANG FROM NANJING UNIVERSITY

MANY REGARD the microLED as the most promising technology for next-generation displays. The primary attributes of this miniature emitter include high brightness, high reliability, a long lifetime and low power consumption. Compared with the organic LED, which is now widely used in smartphone displays and high-end TVs, the inorganic microLED based on III-nitrides is more than ten times brighter and consumes two-to-five times less power. Thanks to these strengths, microLEDs could be deployed in wearable electronic devices operating in very bright environments, such as head-up displays, augmented-reality glasses and cell phones. As some of these consumer products are powered by batteries, the lower power consumption of the microLED is valued, enabling a longer running time between charges. Due to all these advantages, the display industry is now investing in microLED technology, with the hope that it can soon replace OLEDs in many products.

As its name suggests, the microLED is much smaller than its forefather that's now widely adopted in general lighting. While there is no official definition for the boundary between the two, as a guide, microLEDs are no bigger than 75 μm.

When microLEDs are deployed in displays, their maximum size is governed by the working distance to the screen. The human eye has an angular resolution of 60 pixels per degree. Therefore, the closer the eye is to the display, the smaller the microLEDs must be to maintain the maximum distinguishable resolution. Unfortunately, the efficiency of microLEDs decrease as their size shrinks, an unwanted occurrence that's referred to as 'the size effect'. This issue is a major obstacle to the progress of displays based on microLEDs.

As well as microLEDs, switching control transistors are a key component in these displays. Their role



➤ Figure 1. Overview of the integration schemes for switching control transistors and microLEDs.

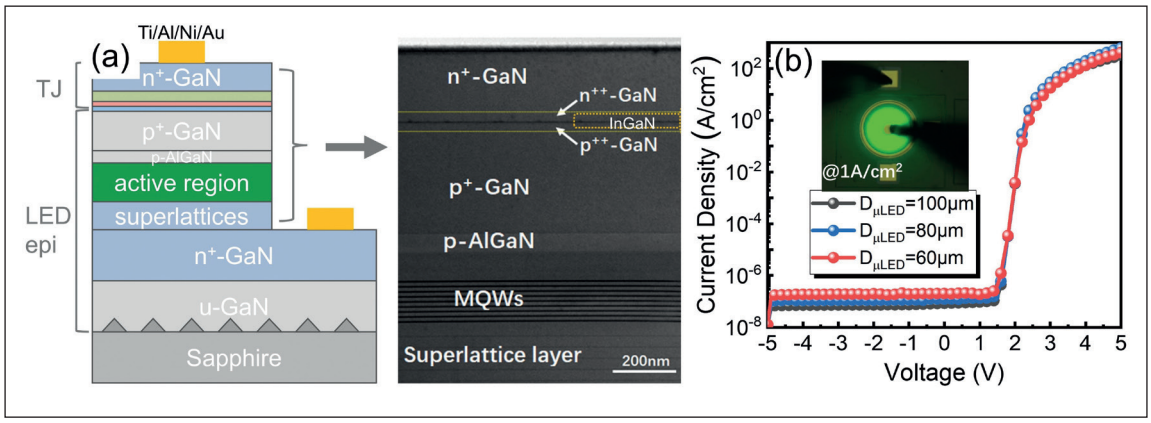
is to switch the corresponding microLEDs on and off and control their brightness. By performing these functions, displays can show images and play videos.

Unfortunately, the microLEDs and transistors that are used in displays tend to be made from different materials and produced using a separate manufacturing process. Blue and green microLEDs are made from GaN-based materials – and red are based on AlGaInP – while transistors are constructed from other classes of semiconductors. Options for the latter include thin-film transistors (TFTs) based on either low-temperature polycrystalline silicon or InGaZnO, or silicon CMOS ICs. The panel housing the TFTs or the CMOS IC is called a backplane, and it has to be integrated with microLEDs to make a display. Establishing an efficient, high-yield process for this integration is another critical challenge facing developers of microLED displays.

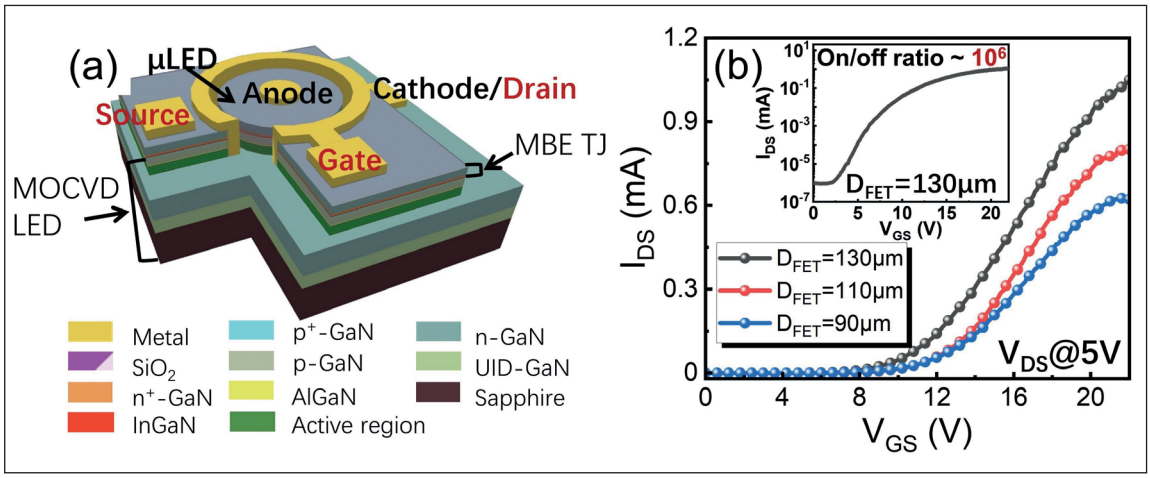
The majority of these developers are pursuing an integration technique known as 'mass transfer', with a 'pick and place' process that transfers millions of microLEDs to the specific positions on the backplane. Today the transfer yield is not high enough for production, and while microLED display prototypes are now in circulation, a significant gap remains towards commercial products.

An alternative approach that avoids this mass transfer process is the monolithic integration of microLEDs and transistors on the same wafer. It is worth noting that the benefits of this form of monolithic integration are not limited to leveraging conventional fabrication techniques, but include the simplification of the process via parallel processing. What's more, this monolithic approach eradicates the need for high transfer accuracy, and realises an extremely high resolution by conventional photolithography. All these strengths help to trim cost and boost yield, improvements that are highly valued by the display industry.

One team that has adopted the monolithic concept is ours at Nanjing University, China. We are pioneers of the lateral integration of pairs of microLEDs and MOSFETs, both based on the GaN platform. Our trailblazing technology involves the re-growth of a hybrid tunnel junction on a commercial GaN LED epiwafer. The tunnel junction allows us to fabricate



➤ Figure 2. (a) Cross-section schematic (left) and transmission electron microscopy (TEM) image (right) of tunnel-junction LED structure. (b) Current density-voltage plot of tunnel-junction microLEDs with different diameters. The inset is the emission image of a 100 μm tunnel-junction microLED at 1 A cm^{-2}.



➤ Figure 3. (a) Schematics of the monolithically integrated microLED/MOSFET device. (b) Transfer characteristics of the MOSFET with different diameters. The inset is the I_{DS}-V_{GS} curve.

microLEDs and MOSFETs with a vertical high-mobility electron channel from the same epiwafer. By drawing on a careful monolithic design, we have demonstrated pairs of microLEDs and normally-off MOSFETs in different sizes. This breakthrough is contributing to the advancing of GaN-based optoelectronic integrated chips, which have the potential to serve in transparent and flexible microLED displays.

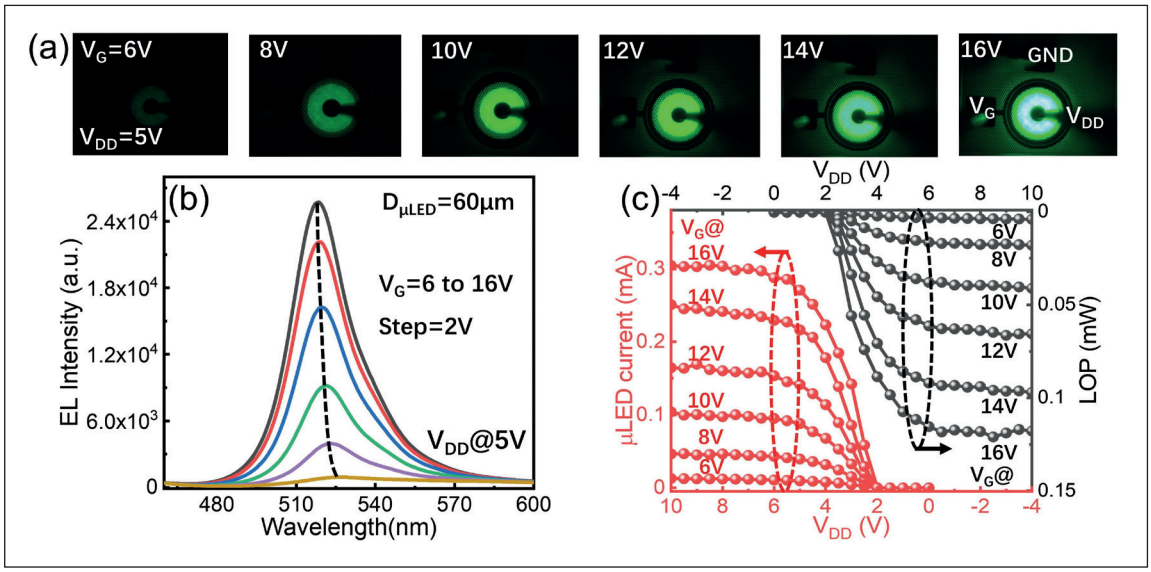
Monolithic options

One of the key decisions to make when pursuing monolithic integration is this: heterogeneous or homogeneous? Determining which one is the choice of material for the transistor. If the material for the transistor differs from that used to make the microLED, monolithic integration is heterogeneous; otherwise, it is homogeneous. For heterogeneous integration, fabrication tends to begin by integrating transistor materials on the LED wafer, before fabricating transistors on that wafer.

Initially, we pursued this approach to integration. In 2021, we reported a three-dimensional monolithic microLED display driven by a TFT matrix. For that work, our TFTs were made from the two-dimensional material MoS_2. Those TFTs have a mobility of 54 $cm^2 V^{-1} s^{-1}$, implying that they provide good drive capability for various display applications.

Thanks to the benefits of monolithic integration, we could skip over the precise mass transfer process, and realise a prototypical display with a resolution of 1270 pixels-per-inch. Our success enabled the first concept or demonstration of an inorganic microLED display driven by MoS_2 transistors. It is worth noting that the heterogeneous monolithic approach always requires an additional fabrication process to integrate different materials on a single wafer – and threatens to reduce yield and increase cost. In our case, we had to transfer MoS_2 materials onto the LED wafer.

More recently, we have advanced to a homogeneous monolithic approach, integrating microLEDs and transistors naturally on a single



➤ Figure 4. (a) Emission images and (b) electroluminescence (EL) spectra of the integrated MOSFET/microLED at different gate voltages when the V_{DD} is 5 V. (c) Drain bias modulated current-voltage (I-V) characteristics and light output power of the integrated device at different gate voltages.

As normally-off transistors are always preferred, due to their superiority for energy saving, GaN-based lateral and vertical MOSFETs are compelling alternatives to HEMTs for the pairing with a microLED

wafer. Due to the maturity of GaN transistors, both HEMTs and MOSFETs, the key challenge we faced when integrating microLEDs and transistors on a GaN platform was the design of a specific epitaxial structure.

The pairing of a microLED with a HEMT is the earliest and most common proposal for monolithic integration. It's crucial to position the microLED structure above that for the HEMT because the growth temperature for the microLED is lower than that for the HEMT. The fabrication to integrate the microLED and HEMT usually demands a selective etching process and a metal-based interconnect. To ensure normally-off operation for the HEMT, there's a need for precise control of the etching process when forming the recessed channel of this transistor.

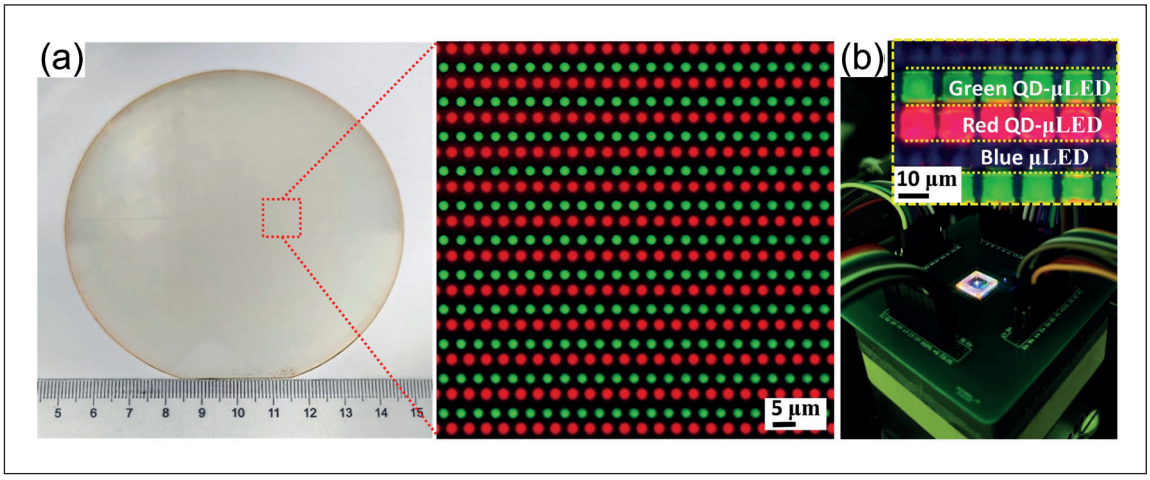
Another option for stacking a microLED and a HEMT is to use selective-area growth. This involves using a patterned dielectric layer, such as SiO_2 or SiN, to define an area for epitaxial growth. As normally-off transistors are always preferred, due to their superiority for energy saving, GaN-based lateral and vertical MOSFETs are compelling alternatives to HEMTs.

Introducing the tunnel junction

Over the last ten years the GaN community has devoted considerable effort to developing a GaN-based tunnel junction, and this is now an established feature within a cascaded LED. The conventional tunnel-junction consists of a heavily magnesium-doped *p*-type GaN layer and a heavily silicon-doped *n*-type GaN layer, and operation occurs under reversed bias. This kind of GaN-based tunnel-junction can be grown by MBE or MOCVD. Since the growth atmosphere in an MBE chamber excludes H_2 gas, which is used in an MOCVD chamber, the quality and performance of the MBE-grown tunnel-junction outperform that of a similar structure grown by MOCVD.

In 2021, we proposed the utilisation of an MBE-grown tunnel-junction structure on a commercial LED wafer to replace the indium tin oxide current-spreading layer in microLEDs. We inserted an ultra-thin InGaN layer to assist carrier tunnelling in the tunnel-junction (see Figure 2 (a)). The addition of the tunnel-junction reduced the operating voltage of the microLED and enhanced its performance. Through continuous optimisation of the growth conditions, we reduced the forward voltage to around 2.7 V at 10 A cm^{-2} (see Figure 2 (b)), a value that's comparable to that of conventional microLEDs.

Essentially, a microLED structure and a tunnel-junction structure are two forms of *p-n* junction. The difference between them is their operation condition: a microLED operates under a forward bias, while a tunnel-junction works at a reversed bias. Thus, when stacked together, the microLED and tunnel-junction form an *n-p-n* structure.



➤ Figure 5. (a) The green and red quantum dots pattern on a 4-inch wafer with sizes of 2 µm. (b) Display demonstration of a microLED array with green/red quantum dots. The insert is a magnified fluorescence microscope image.

Fortunately, this *n*-*p*-*n* structure is just right for use in a vertical MOSFET. We were so excited when we recognised this that we immediately designed new hybrid devices, formed from the monolithic integration of microLEDs and vertical MOSFETs.

We discovered that many of the fabrication steps for microLEDs and vertical MOSFETs could be performed in parallel. This applies to the etching process to form microLED mesas and MOSFET trenches, and to the sidewall treatment and passivation process to remove damage and protect both these devices. Drawing on this strength, we carefully designed fabrication procedures that enabled us to successfully make tunnel-junction microLEDs and MOSFETs on a single wafer. We connected each pair of devices with a conductive *n*-GaN layer (see Figure 3 (a)), which minimises parasitic issues caused by metal interconnects.

Our MOSFETs based on our hybrid tunnel-junction and LED structure are normally-off and exhibit an on/off ratio of around 10^6 (see inset of Figure 3 (b)). This ratio guarantees fine switching, on and off, of the corresponding tunnel-junction microLED. The typical threshold voltage is around 6 V, high enough to prevent false operation.

An important characteristic of our vertical MOSFETs is that they can scale in size with the microLED. The identical scaling rule ensures that our MOSFETs provide identical driving capability, regardless of the size of the microLEDs, a great asset for deploying our technology in different display applications.

We have examined the performance of our integrated tunnel-junction microLED/MOSFET pairs (see Figure 4). We have found that the current through our microLED can be well controlled by our vertical MOSFET's gate supply voltage (V_G) and anode supply voltage (V_{DD}). Our integrated 60 μm microLED exhibits a high output power of 0.12 mW (around 4.2 W cm^{-2}) at a current of 0.3 mA (around 10 A cm^{-2}) when modulating the MOSFET with a V_{DD} of 5 V and a V_G of 16 V. This driving capability in our novel structure is comparable to that of IGZO-based TFTs. That's sufficient to satisfy the requirements of the driving capabilities for most microLED displays.

Adding quantum dots

Ideally, microLED displays should be full colour, because they can then provide high-resolution, vivid images and videos that create a wonderful watching experience for the viewer. To realise a full-colour display, red, green, and blue microLEDs are integrated together on the backplane. If the red, green, and blue microLEDs are fabricated separately on different wafers, issues arise that are associated with the 'pick and place' mass transfer process.

To avoid this particular issue, we are pursuing a monolithic solution that utilises quantum dots as colour-conversion materials. We use blue microLEDs to provide blue emission and to also pump quantum dots, leading to green and red emission. Since the red, green, and blue microLEDs should be assembled together as a single pixel, the green and red quantum dots must cover blue microLEDs at specific locations.

This kind of quantum dot transfer is challenging. It demands high accuracy, large-area coverage, low cost and ease of operation. One promising option for high throughout involves developing quantum-dot-dissolved, UV-sensitive photoresists and patterning the photoresist with photolithography. This approach demands a very high solubility for the quantum dots in the photoresists. Unfortunately, products that combine quantum dots and conventional photoresists are yet to be widely available.

Due to this state of affairs, we have developed an advanced fabrication technique for patterning quantum dots on blue microLEDs that involves photolithography and dry etching. We have turned to double layers of resists, including a negative photoresist and spin-on-glass, to enhance the stability of the quantum-dot patterns during the fabrication process. With this approach we have fabricated green and red quantum dot patterns as small as 2 μm in size on a 4-inch wafer (see Figure 5 (a)). Note that the 2 μm size is the limitation of our contact aligner, but not our technique. We believe that the size of quantum-dot patterns can be continuously scaled down with advanced steppers.

By simply repeating the patterning process for green and red quantum dots, we have demonstrated a red-green-blue microLED array with each chip size less than 10 μm (see Figure 5 (b)). Through monolithic integration with GaN-based MOSFETs, as discussed above, we can go on to realise full-colour microLED displays with a GaN platform. Since our entire fabrication procedures are compatible with standard processes, our techniques are ready for transfer to mass production.

Our progress is an important contribution to the monolithic integration of GaN-based microLEDs with transistors. Such exciting results have established a new route towards achieving full-colour displays based on a GaN platform, which may go beyond the heterogeneous integration limit and spearhead the future for microLED displays.

FURTHER READING

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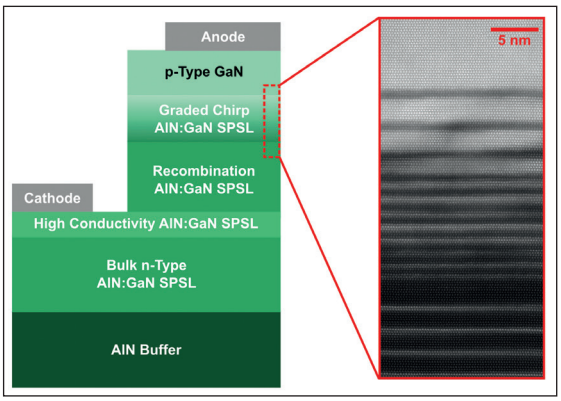
MBE for far-UV LEDs

150 mm sapphire substrates are a promising platform for high-volume production of far-UVC LEDs via MBE

WHILE MOCVD is the most common growth method for producing far-UV LEDs, MBE also enables high-volume, high-yield production of these devices, says Silanna UV.

This Australian outfit has made more than 10,000 functional devices from a 150 mm GaN-based epiwafer, produced on a sapphire substrate using a Veeco GEN200 MBE tool. Following packaging, these far-UV LEDs produce an output power of 1.7 mW at peak efficiency, and have a lifetime of several thousand hours.

Silanna's devices are compelling candidates for the optical source for disinfection and sterilisation. Emitting below 240 nm, radiation from these LEDs has minimal penetration beyond the outmost layers of skin, ensuring that exposure poses a reduced cancer risk. In addition, the company's far-UVC LEDs can be used in sensing and high-performance liquid chromatography.



➤ Silanna's far-UVC LEDs feature four superlattices.

These far-UVC LEDs are produced on commercial 150 mm sapphire substrates, which are outgassed prior to growth in the Veeco GEN200.

"The Veeco GEN200 platform is a dual-chamber system, so we are capable of meeting current demand," says Jordan Nichols, a senior device integration engineer at Silanna, who reveals that the company's epitaxy facility has been purpose built to expand production capacity as demand grows.

To form the LED's epistructure, Silanna's engineers deposit a 400 nm-thick AlN buffer, followed by four different superlattices and then a *p*-type GaN layer (see Figure). The superlattice for the recombination region is about 80 nm-thick and features 36 periods, with layer widths tuned to meet the target wavelength, which can vary from 229 nm to 240 nm.

"Devices at shorter wavelengths will have a lower output power," says Nichols. "We bin our LEDs to assist customers with selecting the appropriate output power and wavelength for their desired application."

One merit of using a short-period superlattice for the active region is a band structure that promotes transverse electric emission, leading to increased light extraction efficiency. This form of active region also reduces the dopant ionisation energy, thereby reducing resistivity, compared with a conventional quantum well region for a far-UVC LED.

To improve hole injection into the heart of the device, Silanna inserts a chirp superlattice between the *p*-type GaN layer and the active region. Also acting as an electron-blocking layer, this chirp superlattice prevents electrons from overshooting the recombination region.

Silanna produces LEDs from its epiwafers using standard photolithography and metallisation processes. After forming mesas by dry etching, Ti/Al contacts are deposited to form electrical contacts. Following the addition of a standard passivation layer, engineers at the company may undertake optoelectronic measurements at the wafer-level using an integration sphere.

Wafer-level maps of electroluminescence spectra were recorded for more than 10,000 individual LEDs driven at 20 mA. For these devices, emitting at around 233 nm, the standard deviation in peak wavelength for devices in the middle 100 mm of the wafer is just 0.16 nm, and the average optical power 0.2 W.

Nichols his co-workers have produced packaged LEDs by dicing 1 mm by 1 mm devices from epiwafers, thinning the substrate to 275 μm and polishing it, and then flip-chip bonding the die to an AlN ceramic package. These devices delivered a peak wall-plug efficiency of 0.55 percent at 50 mA. Cranking the current up to 1 A caused the output power to climb to 17.4 mW, which is claimed to be the highest radiant flux for a far-UV LED grown on sapphire.

Lifetime tests on 80 packaged devices driven at 20 mA indicate a lifetime of 2,800 hours, based on the time it takes for the radiant flux to decrease to 70 percent of its initial value.

Goals for the team include realising even higher output powers and longer wavelengths.

REFERENCE

➤ J. Nicholls *et al.* Appl. Phys Lett. **123** 051105 (2023)

TiO_2 enhances Ga_2O_3 diodes

Thanks to a high dielectric constant and a favourable band alignment, TiO_2 enables β-Ga_2O_3 diodes to realise a higher breakdown and a lower turn-on voltage

A KEY CHALLENGE facing designers of any power device is to ensure low losses under both forward and reverse bias. While success on these two fronts has proved particularly challenging with β-Ga_2O_3 diodes, progress may be realised by introducing a high-κ TiO_2 interlayer, according to a US team led by engineers at the Air Force Research Laboratory (AFRL). This partnership, which includes researchers at University of California, Santa Barbara, and APEX Microdevices, has recently reported that inserting a TiO_2 interlayer trims the turn-on voltage and leakage current of the Ga_2O_3 diode, and increases its breakdown voltage.

"Time will tell whether this is the most promising topology," says team spokesman Nolan Hendricks from ARFL. "But, at the very least, this topology with TiO_2 can be combined with other diode designs like junction-barrier-Schottky or trench-MOS Schottky diodes to unlock the full potential of Ga_2O_3."

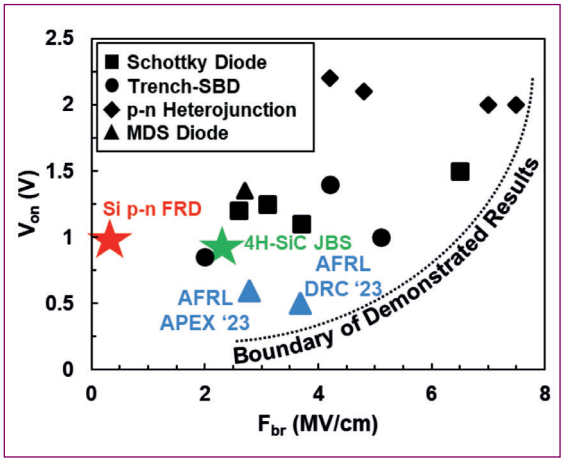
Hendricks and his co-workers are by no means the first team to investigate new device architectures for improving the performance of Ga_2O_3 power diodes.

A number of designs have already been reported that succeed in reducing the off-state current density. They include: trench-based structures, which are hampered by an increase in the specific on-resistance; devices with high Schottky barrier contacts, which cut leakage but increase the turn-on voltage; and diodes with *p-n* junctions that increase the barrier height, leading to higher on-state losses.

Offering more promise, argues Hendricks, is the metal/$BaTiO_3$/Ga_2O_3 structure pioneered by the team at Ohio State University, led by Zhanbo Xia and Siddharth Rajan.

"The metal/$BaTiO_3$/Ga_2O_3 structure gave a very large turn-on voltage due to a slightly positive conduction band offset, but the fundamental concept they conceived of was quite promising," says Hendricks. "When we saw that TiO_2 was also high κ but should theoretically have a negative band offset to Ga_2O_3, we got to work on implementing it in the metal-dielectric-semiconductor structure. The results have been great."

TiO_2 has a dielectric constant of 30-160 and a conduction band edge that is around 0.3 eV lower than β-Ga_2O_3. These characteristics promise a reduced leakage at reverse bias, due to improved blocking of tunnelling electrons, and no impairment to forward conduction, thanks to the band profile.



Results presented in the journal *Applied Physics Express* and at this year's Device Research Conference showcase the potential of Pt/TiO_2/Ga_2O_3 diodes

To determine whether TiO_2 could fulfil its promise, Hendricks and co-workers fabricated a conventional β-Ga_2O_3 Schottky barrier diode and a Pt/TiO_2/Ga_2O_3 diode in parallel. These devices were formed from adjacent die on a wafer containing a 13 μm-thick, silicon-doped β-Ga_2O_3 layer grown by HVPE on a tin-doped native substrate. Plasma-enhanced atomic layer deposition added a 4.3 nm layer of TiO_2.

Measurements on both types of diode, featuring edge passivation through the deposition of SiO_2, revealed that inserting TiO_2 lowered the turn-on voltage from 0.88 V to 0.59 V and increased the breakdown voltage from 548 V to 1380 V, corresponding to an increase in the breakdown field from 1.8 MV cm^{-1} to 2.8 MV cm^{-1}.

Hendricks regards these results as "very exciting", arguing that the breakdown field for the team's Pt/TiO_2/Ga_2O_3 diodes exceeds the limit of 4H-SiC in a planar topology, which also has a higher turn-on voltage.

Note that these results were realised without edge termination. This is now being introduced, with the team considering a range of field management structures that allow low resistive losses and a low turn-on loss. "We have already demonstrated an early advance in that area, pushing the breakdown field up to 3.7 MV/cm through *p*-NiO guard rings, which we shared at Device Research Conference 2023," says Hendricks, who is now hoping to make additional progress in increasing the breakdown field while realising a low forward voltage.

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N. Hendricks *et. al.* Appl. Phys Express **16** 071002 (2023)

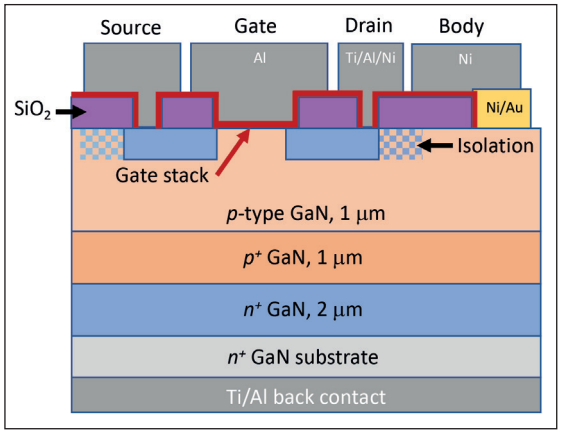
Trimming the on-resistance of GaN MOSFETs

Nitrogen radical treatment, followed by insertion of an AlN interlayer, increases channel mobility in GaN MOSFETs

A TEAM from Japan has reduced the on-resistance of its GaN MOSFETs by a factor of four through the introduction of a nitrided interface.

This advance by engineers from Toyoda Central Labs and the Institute of Materials Systems for Sustainability will help the development of devices that handle high voltages and currents at high efficiencies, a necessity for high-efficiency power conversion systems.

Potential candidates for such systems are a number of vertical device structures, including several forms of JFET. But these devices are held back by a limited gate overdrive, says team spokesman Kenji Ito, who points out that when the gate voltage exceeds 3 V the gate leakage current climbs, due to the forward current of the gate *p-n* diode. To suppress this leakage, there's a need to limit the applied gate voltage – and thus prohibit the use of gate overdrive.



➤ An AlN interlayer and nitrogen-radical pre-treatment increase the mobility of the GaN MOSFET

In stark contrast, MOSFETs have an extremely low gate-leakage current, thanks to the oxide/semiconductor junction that forms the gate structure.

One issue with GaN MOSFETs is that for a channel mobility of 100 $cm^2 V^{-1} s^{-1}$, channel resistance is 0.5 mΩ cm^2, a concern at 1 kV or more. Another weakness is insufficient reliability of the gate oxide.

Ito and co-workers are tackling both these issues. Back in 2020 they revealed that the introduction of an AlSiO gate oxide enabled a lifetime of 20 years under 5 MV cm^{-1} at 150 °C. However, the channel mobility was no better than 40 $cm^2 V^{-1} s^{-1}$. Now, thanks to nitridation, they have overcome that limitation, with mobility reaching 200 $cm^2 V^{-1} s^{-1}$.

Fabrication of these transistors began by loading *n*-type GaN substrates into an MOCVD chamber and depositing a stack of epilayers. Post-growth annealing at 850 °C activated the magnesium acceptors. Silicon-ion implantation and annealing created source and drain regions, before nitrogen-ion implantation provided isolation, suppressing leakage between source and drain electrodes. A HF solution then cleaned the GaN surface, removing GaO_x, before plasma-enhanced CVD added a 300 nm-thick layer of SiO_2. Removal of SiO_2 from above the channel followed, prior to plasma-enhanced ALD of a 40 nm-thick layer of AlSiO, acting as the gate oxide, and a 3 nm-thick SiO_2 cap.

In addition to this variant, formed by direct deposition of AlSiO on GaN, Ito and co-workers produced two variants: one with an AlN interlayer between AlSiO on GaN; and a second with that structure, but involving nitrogen-radical pre-treatment prior to deposition of the interlayer.

Devices were completed with 10 minutes of annealing at 950 °C under nitrogen gas and evaporation of metals to form body, source and drain electrodes.

Material profiles obtained with secondary ion mass spectrometry revealed that inserting the AlN interlayer supressed gallium diffusion. It's speculated that this suppression stems from the insertion of the interlayer, which prevents oxidation of the GaN surface during deposition and post-deposition annealing.

Measurements show that the interlayer also benefits effective mobility, which increases from 46 $cm^2 V^{-1} s^{-1}$ to 130 $cm^2 V^{-1} s^{-1}$. An additional hike to 229 $cm^2 V^{-1} s^{-1}$ results from nitrogen-radical pre-treatment.

While the team have used a native substrate for their work, this is not essential, says Ito, because the focus is the oxide-GaN interface. However, as the team is developing vertical GaN MOSFETs, they still have to consider the source-drain leakage through the *p-n* junction under bias stress. "Since the current GaN-on-silicon wafer involves high-density threading dislocations, reverse leakage is a critical problem," points out Ito, who argues that high-quality GaN substrates have an advantage in terms of reliability.

The team is now planning to investigate how to control the threshold voltage of their devices, without compromising mobility. One downside of the interface control technique is a negative shift in threshold voltage, which hampers fabrication of normally-off devices – they are required for fail-safe switching circuits.

REFERENCE

➤ K. Ito *et al*. Appl. Phys Express **16** 074002 (2023)

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