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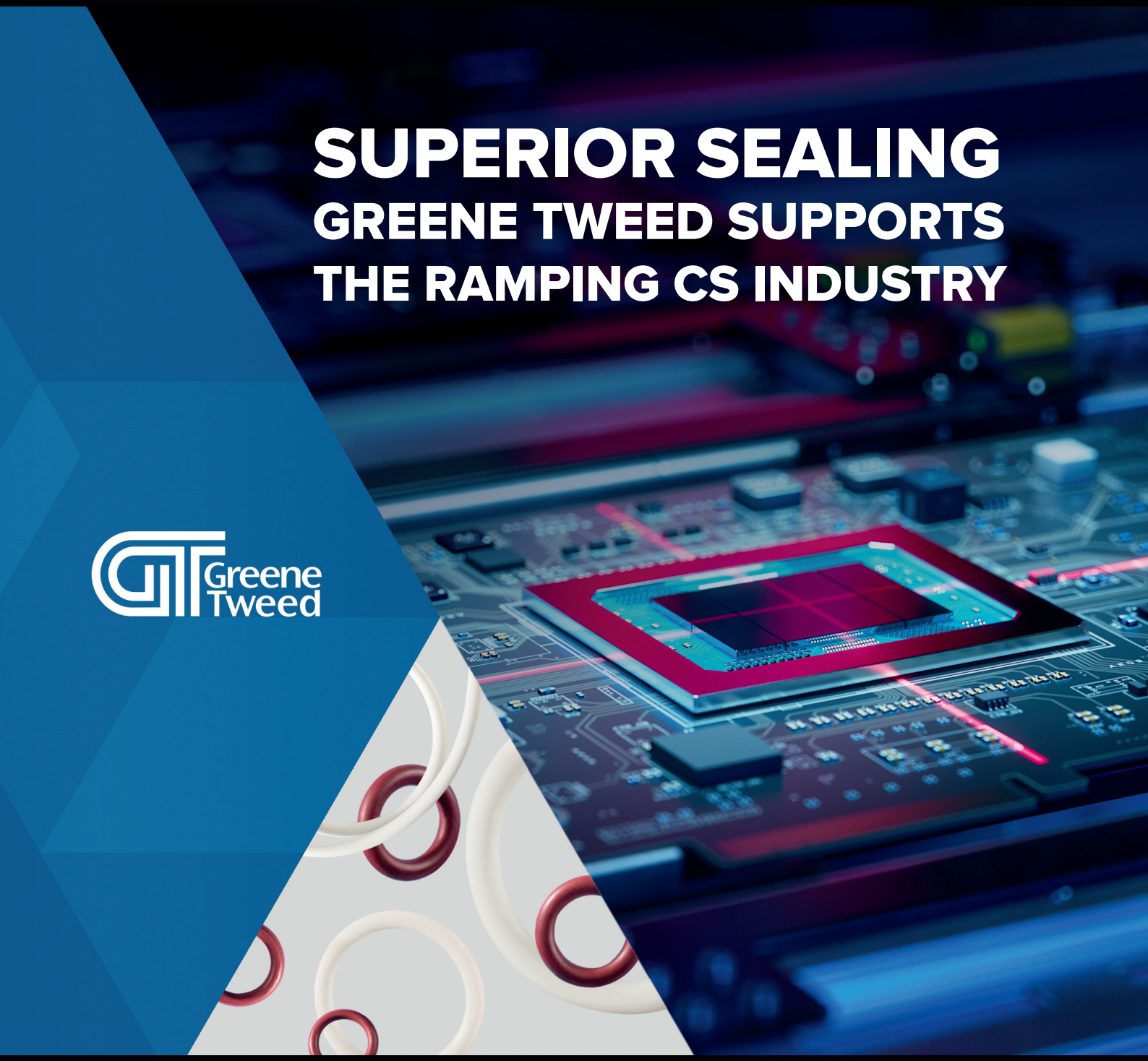

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INSIDE
News, Analysis, Features, Editorial View, Research Review and much more

Ready or not, AI is here to stay
AI and machine learning hold the key to improving the running of every compound semiconductor fab

Revolutionising RF oscillators
GaN IMPATT diodes enable compact and efficient solid-state oscillators that deliver high radio-frequency power

Monolithically integrated lasers
Low-strain quantum cascade lasers are closing the gap to realising reliable infra-red sources on silicon

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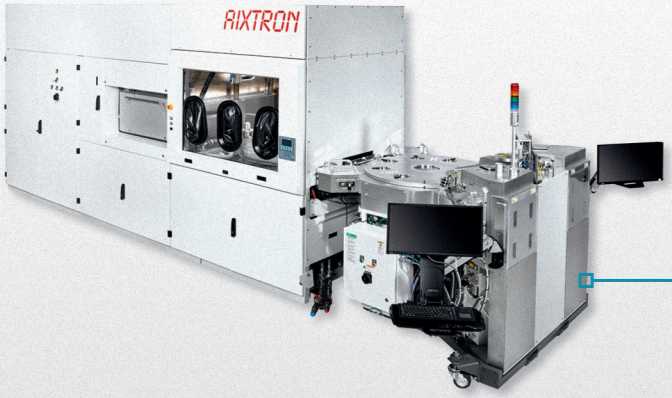

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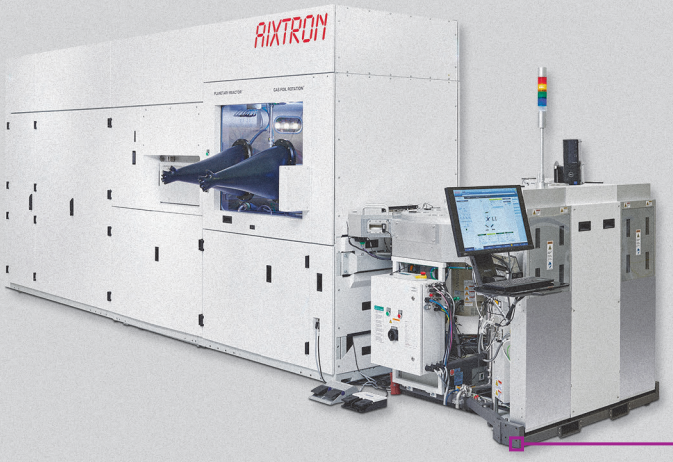

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VIEWPOINT

By Richard Stevenson, Editor

The long-term prospects for CPV

OVER THE COMING YEARS, the deployment of solar PV is forecast to rise substantially, before plateauing from 2037 at 3.4 TW per annum.

That figure for power generation is so big that's hard to put into perspective. It might help to know that all the PV installed to date stands at 1 TW. Or maybe it's easier to think that if 3.4 TW of power generation were provided by today's silicon panels, they would cover an area half the size of Belgium – or to put in another way, almost all of Hawaii or Shikoku.

As well as taking up a lot of land, 3.4 TW of silicon PV would consume a lot of the world's resources. Based on the make up of current panels, all the glass that's produced today would have to be given over to this application, which may well gobble up three times more silver than is on the market today.

These are scary numbers – and they encourage everyone in the PV industry to look at alternative forms of solar that are far less resource-intensive.

In this regard, concentrating photovoltaics (CPV) is a compelling candidate. Systems operating at several hundred suns or more use far, far less semiconductor material than those based on silicon, while the higher efficiency increases the power-generation density by around 30 percent, reducing the amount of land that's needed for power production.

One downside of CPV is that it's lacking a cohort of commercial pioneers. The technology appeared to be breaking through towards the end of the noughties, before the combination of a global credit crunch and plummeting prices of silicon PV thwarted success, causing its trailblazers to shut up shop.

But CPV may now be starting to see the very first steps of a revival. In Australia, RayGen is building novel plants

that combine many megawatts of electrical generation with substantial energy storage – and in Europe, efforts led by Fraunhofer ISE and tracker specialist Soltec have culminated in a refined form of CPV that employs five-junction cells from Azur Space Solar with an efficiency of around 40 percent (see p. 14 for details).

When you compare this latest design from the European team with those from the late noughties, you can see substantial improvements. They include the elimination of concrete structures to hold the trackers, a move to a higher level of concentration that trims costs –operation is now at 1000 suns – and the introduction of far smaller cells that allow for thinner modules and passive cooling.

CPV will not grab the solar market by storm overnight. But as concerns mount over the consumption of material, and how much power can be produced from plots in sunny climes, this technology is sure to make a compelling case for its deployment.

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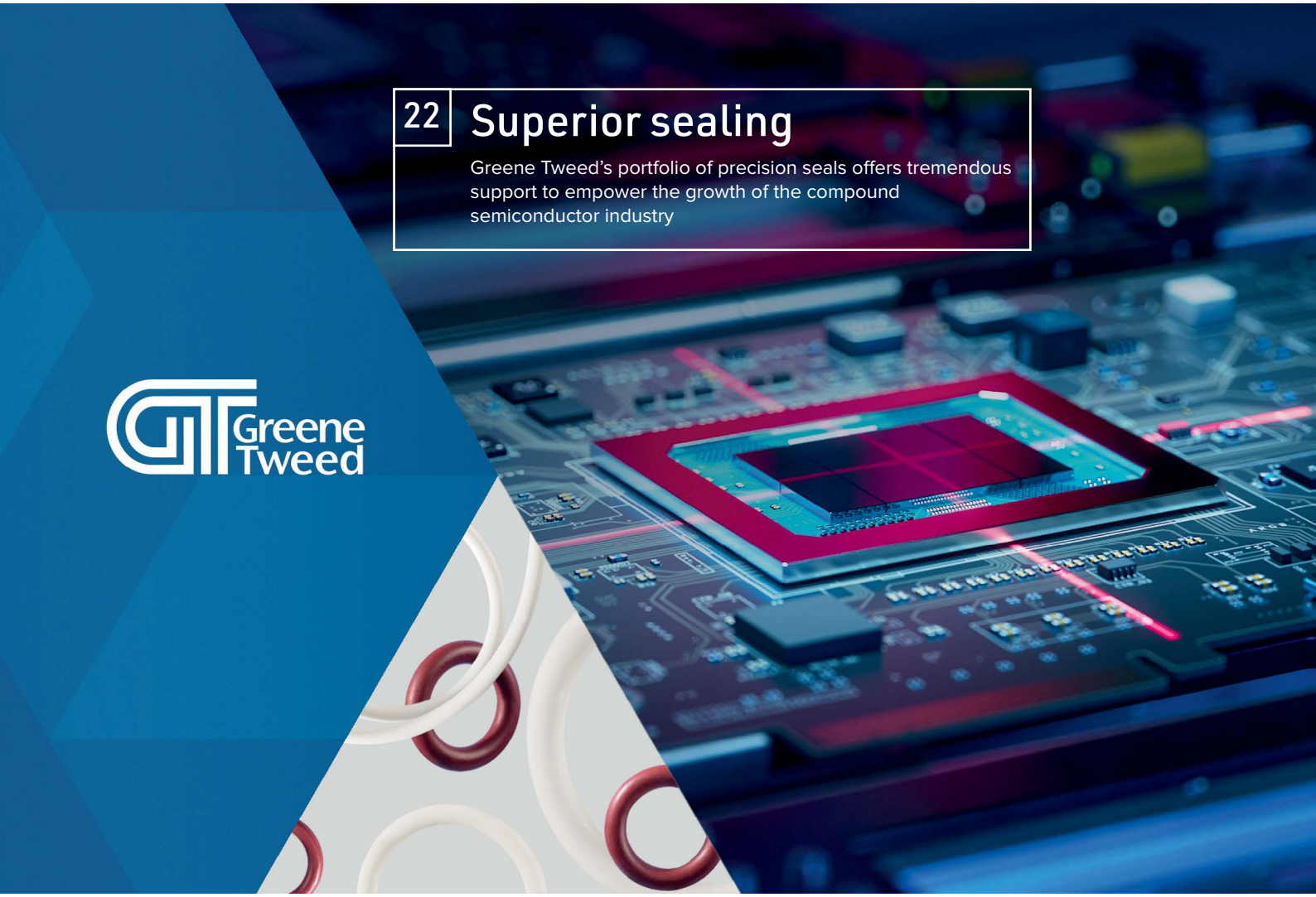

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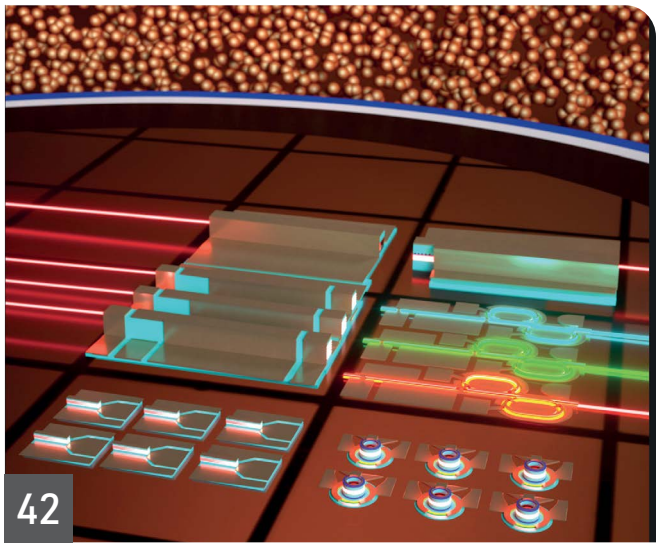

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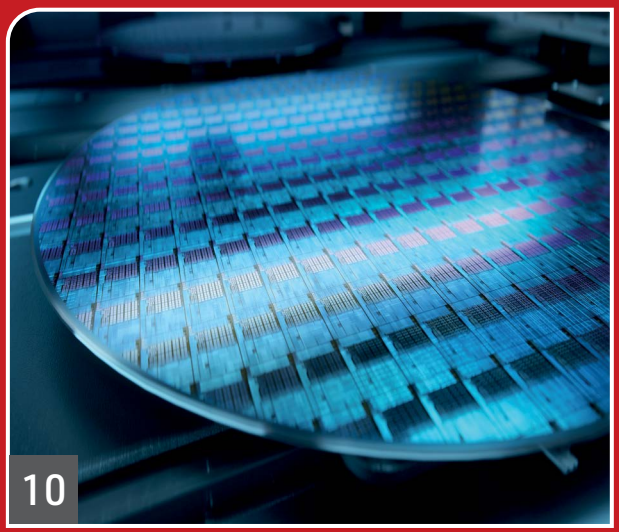

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Power electronics: facing rapid capacity expansion

A consolidation phase will follow the surge in manufacturing capacity, says Yole

ACCORDING TO Yole's *Status of the Power Electronic Industry, 2024* report, the power electronics market will reach $35.7 billion by 2029, growing at a CAGR of 7 percent from 2023, when it was $23.8 billion.

The power electronics supply chain has recently rapidly expanded its manufacturing capacity, particularly for SiC and silicon devices, as well as SiC wafers. However, this will consolidate, driving technology innovations, price reductions, and new strategies, says Yole.

The discrete market, valued at $15.5 billion in 2023, is projected to grow at a 3.9 percent CAGR to $19.5 billion by 2029, driven mainly by xEV, OBC, DC-DC converters, and charging infrastructure. Automotive and consumer are the biggest market segments. Power modules, pushed by battery energy storage, EV DC chargers, and xEVs, are set to reach $16.2 billion by 2029, with a 12.0 percent CAGR.

Milan Rosina, principal analyst for power electronics & battery at Yole Group, said: "The power device market is led by silicon, with SiC gaining ground in xEV and industrial applications, while GaN serves consumer power supplies and e-mobility. Gallium oxide could become a future contender."

Yole is projecting the SiC device market to reach nearly $10 billion by 2029, with a compound annual growth rate (CAGR) of 24 percent from 2023 to 2029.

Here the key players are focusing on the transition to 8-inch wafers and addressing the associated challenges.

As of 2024, 400 V BEVs, such as those from Tesla, are the largest consumers of SiC. The introduction of more 800 V BEVs by OEMs is further accelerating this demand.

Wafer demand is rising accross the board, including 12-inch silicon wafers, with GaN-on-silicon using 6- and 8-inch wafers. SiC wafer capacity is expanding, risking oversupply due to lower xEV demand.

Power electronics supply chain

The power electronics supply chain is evolving due to five main factors, according to Yole. These are: expansion in wafer and device manufacturing capacity, with a shift toward larger wafer diameters; an increase in new silicon and SiC wafer manufacturers from China; mergers and acquisitions across wafer, device, packaging, and system manufacturers; device manufacturers diversifying technology portfolios (silicon, SiC, GaN); and finally, system makers horizontally integrating into various applications including photovoltaics, wind, EV DC charging, and battery energy storage systems.

"Recent years have seen rapid growth in manufacturing capacity, particularly for SiC and silicon devices and wafers," says Rosina. "However, despite the demand drivers, the slowdown in xEV demand and the rush to increase capacity has led to overcapacity, especially in the SiC segment. This will likely lead to consolidation in the supply chain, fostering innovation, reducing prices, and creating new strategies. More partnerships, mergers, and acquisitions are expected in the coming years."

Chinese companies have a strong presence in end-systems like PV installations, wind energy, electric vehicles, and EV DC charging infrastructure and in power converter manufacturing. They also have extensive involvement in silicon and SiC wafer production and power device packaging.

The Chinese government and businesses are focused on addressing their reliance on foreign suppliers for bare dies, aiming to boost the market share of Chinese power device manufacturers in the near future.

Infineon develops first 300 mm power GaN wafer

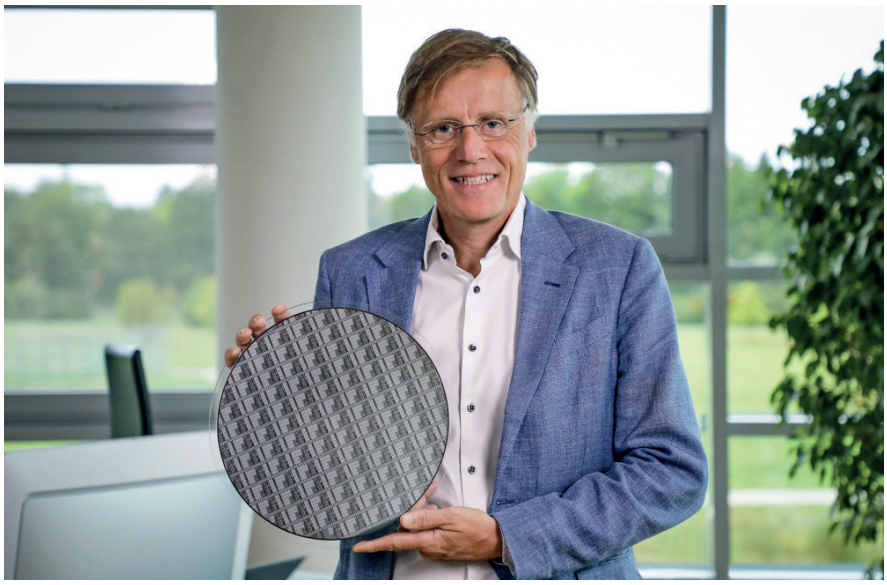
Company builds on existing large scale 300 mm silicon to more than double the number of GaN chips per wafer

INFINEON TECHNOLOGIES has succeeded in developing the world's first 300 mm power GaN wafer technology, claiming to be the first company in the world to master this groundbreaking technology in an existing and scalable high-volume manufacturing environment.

It believes the breakthrough will help drive the market for GaN-based power semiconductors. Production on 300 mm wafers, compared with 200 mm technology, offers 2.3 times more chips per wafer.

"This remarkable success is the result of our innovative strength and the dedicated work of our global team to demonstrate our position as the innovation leader in GaN and power systems," said Jochen Hanebeck (pictured above), CEO of Infineon Technologies AG.

"The technological breakthrough will be an industry game-changer and enable us to unlock the full potential of GaN. Nearly one year after the acquisition of GaN Systems, we are demonstrating again that we are determined to be a leader in the fast-growing GaN market. As a leader in power systems, Infineon is mastering all three relevant materials: silicon, silicon carbide and GaN."



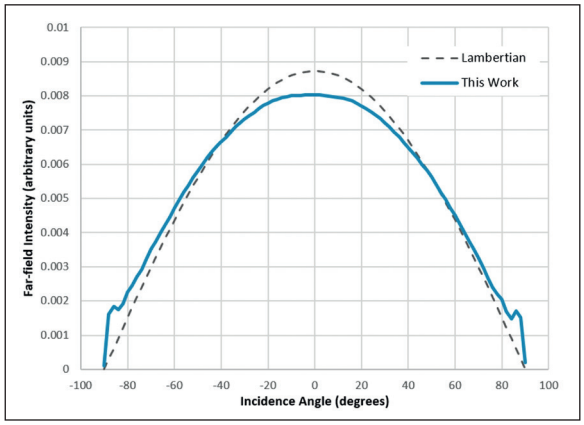
A significant advantage of 300 mm GaN technology is that it can utilise existing 300 mm silicon manufacturing equipment, since GaN and silicon are very similar in manufacturing processes.

Infineon has succeeded in manufacturing 300 mm GaN wafers on an integrated pilot line in existing 300 mm silicon production in its power fab in Villach, Austria. The company is building on well-established existing production of 300 mm silicon and 200 mm GaN.

Lumileds addresses microLED efficiency through EQE and directionality

Lumileds' R&D team realises Lambertian distribution from microLEDs

LUMILEDS has realised significant external quantum efficiency (EQE) performance for MicroLEDs in the past years. EQE, is the ratio between the energy contained in the light emitted from the LED and the energy in electrons injected into the semiconductor material.



However, for microLEDs, and display applications in particular, EQE on its own is not a sufficient measure of performance. To properly assess the efficiency of a microLED, one must also be able to measure the directionality of the light. The directionality of light is critical for microLED displays, and for this reason, displays are often characterised by radiant or luminous Intensity, as seen from an angle.

"Most LEDs emit the majority of light from their top surface. This is especially true for thin film LEDs. When we shrink the size of thin film LEDs to become microLEDs, the 'side-emitting' surfaces become a significantly greater portion of the overall light-emitting surfaces," explained Brendan Moran, Lumileds' Senior Director of MicroLED Development.

"The thickness of what we described as a thin film for a larger size LED now becomes substantial relative to the length and width of the microLED. This is a key reason why microLEDs emit a large portion of light from their sides, resulting in a wide viewing angle distribution and a reduction of intensity emitted from the top surface. For display applications, even high EQE microLEDs can have relatively low on-axis intensity," said Moran.

The Lumileds R&D team has now developed microLEDs with a highly desirable light distribution that approximates Lambertian distribution. The team's innovation results in brighter displays that consume less energy.

"Most LEDs emit the majority of light from their top surface. This is especially true for thin film LEDs. When we shrink the size of thin film LEDs to become microLEDs, the 'side-emitting' surfaces become a significantly greater portion of the overall light-emitting surfaces"

Coherent raises efficiency of InP CW lasers

LASER AND NETWORKING firm Coherent has launched a range of high-efficiency continuous wave (CW) distributed feedback (DFB) lasers.

Designed to operate in the O-band (1310 nm region), the InP lasers are claimed to redefine the capabilities of silicon photonics modulators used in 800G and 1.6T optical transceivers. Featuring a proprietary low series-resistance design, the lasers achieve approximately 15 percent greater power efficiency compared with the current industry standard. This breakthrough addresses the critical demand for reduced power consumption in silicon photonics transceivers, providing customers with a clear edge in operational efficiency.

"Our new family of CW lasers for silicon photonics is creating a wave of excitement among industry leaders," said Kou-Wei Wang, VP of InP Directly Modulated Lasers & Photodiodes. "By lowering power consumption, we're addressing one of the most pressing challenges faced by our customers today. And with our upcoming expansion to a state-of-the-art 6-inch InP fab in Sherman, Texas, by 2026, we expect production capacity to be five times our current production rate, a significant ramp given the complexity of this material. We are committed to leading the market with technology and supply chain capacity as our customers increase demand in the InP laser sector."

The first offering in this laser family is a 70 mW 1310 nm laser, designed for uncooled, non-hermetic operation up to an 85°C junction temperature. Commercial shipments of this laser begin in September 2024. Coherent will release a higher-power laser for cooled operations, along with lasers tailored for the CWDM grid, in 2025.

Sivers plans photonics spin-off

Merger expected to unlock value and create an independent US NASDAQ traded photonics company

SIVERS SEMICONDUCTORS AB has entered into a non-binding letter of intent to merge its Sivers Photonics Ltd subsidiary with byNordic Acquisition Corporation, a publicly-traded special purpose acquisition company.

The merger is expected to unlock significant value and create an independent US NASDAQ traded photonics company. (Sivers Photonics currently has approximately 80 percent of its net revenue in the US).

Once the merger is finalised, the company plans to establish headquarters in Silicon Valley, CA, with the manufacturing operations remaining in the UK.

Sivers today consists of two subsidiaries addressing two different markets: wireless and photonics. The Sivers' Photonics subsidiary has particular focus on InP technology, with which it develops customisable lasers aimed at high-growth AI infrastructure and sensing applications for data centres, consumer healthcare and automotive lidar. The company has three issued patents and 16 patents pending across the US, UK, Canada and the World Intellectual Property Organisation.

Additionally, Sivers Photonics has development contracts to develop unique lasers for several leading silicon photonics providers, such as Ayar Labs, and is in discussion with several leading AI companies, including hyperscalers.

Subsequent to the proposed spin-off and Sivers Photonics merger combination, Sivers' remaining wireless business will consist of a portfolio of products in millimetre-wave beamformer front-end integrated circuits, RF transceivers, repeaters, and software algorithms for millimetre-wave RF performance for satellite and 5G infrastructure. Wireless business

net revenue growth was 155 percent in 2023, reaching approximately $15 million. These markets are developing rapidly, and Sivers has secured a number of contracts and design wins that are projected to drive significant product revenue growth over the next 3-5 years.

"We believe the potential for AI Photonics is immense yet overshadowed by the equally exciting Sivers' Wireless business unit. With the attractive opportunity for silicon photonics in AI infrastructure and the emerging demand for photonic biometric sensors, we feel now is the right time to shine a light on this business unit as a standalone entity to gain access to the US capital markets and create an opportunity for our shareholders to participate in its potential future success," said Bami Bastani, Sivers Semiconductor chairman.

"At the same time, we also look to capitalise on the success of the Sivers' Wireless business unit and the demand for our leading-edge millimetre-wave beamformer solutions for satellite and 5G, which has gained substantial traction with customers in these developing markets over the last several years, enabling us to create a fully fabless and less capital-intensive company that will remain listed under Sivers Semiconductors AB."

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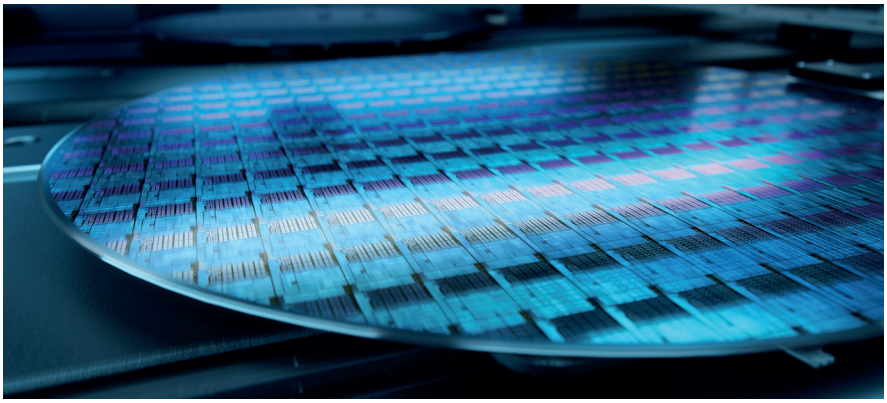
Finwave and GF partner on RF GaN-on-silicon

New agreement to accelerate development of Finwave's E-Mode MISHEMT technology

GaN COMPANY Finwave Semiconductor has announced a strategic technology development and licensing agreement with GlobalFoundries (GF). This partnership merges Finwave's RF GaN-on-silicon technology with GF's US-based high-volume manufacturing capabilities and legacy of RF innovation including RF SOI and silicon-germanium solutions.

The two companies believe they can offer a solution for high-efficiency power amplifiers in applications where traditional GaAs and silicon technologies fall short. This includes new higher frequency 5G FR2/FR3 bands, 6G and millimetre-wave amplifiers, and high-power Wi-Fi 7 systems, where superior range and efficiency are critical.

Finwave's GaN-on-silicon enhacement-mode MISHEMT technology is designed to deliver high gain and efficiency at sub-5 V voltages. The collaboration will focus on optimising and scaling the MISHEMT platform to volume production at GF's 200 mm semiconductor manufacturing facility in Burlington, Vermont, using GF's 90RFGaN process.



"This agreement marks a significant milestone for Finwave," said Finwave Semiconductor CEO Pierre-Yves Lesaicherre. "By leveraging GlobalFoundries' extensive manufacturing capabilities and bringing Finwave's E-mode MISHEMT technology breakthrough to volume production, we are unlocking large growth opportunities as we address the increasingly demanding wireless communication landscape.

This partnership opens the door to further innovation and integration of RF front-ends onto a single GaN-on-silicon device. This has never been done before, and has the potential to reduce cost and size, both of which are at a premium in cellphones."

"As next-generation wireless networks require devices that operate at higher frequencies, Finwave's low-voltage GaN-on-silicon technology combined with GF's 90RFGaN platform will become a vital part of power amplifiers in future mobile phones, ensuring both robust performance and high-power efficiency," said Shankaran Janardhanan, VP and general manager of GF's RF Business.

Finwave and GlobalFoundries aim to qualify this technology for mass production in the first half of 2026.

Geely EVs using Rohm SiC MOSFETs

ROHM has announced the adoption of power modules equipped with fourth generation SiC MOSFET bare chips for the traction inverters in three models of ZEEKR EV brand from Zhejiang Geely Holding Group, a Chinese car maker.

Since 2023, these power modules have been mass produced and shipped from HAIMOSIC Ltd. – a joint venture between Rohm and Zhenghai Group to Viridi E-Mobility Technology, a Tier 1 manufacturer under Geely.

Geely and Rohm have been collaborating since 2018, beginning with technical exchanges, then later forming a strategic partnership focused on SiC power devices in 2021. This led to the integration of Rohm's SiC MOSFETs into the traction inverters of three models: the ZEEKR X, 009, and 001. In each of these EVs, Rohm's power solutions centered on SiC MOSFETs play a key role in extending the cruising range and enhancing overall performance.

The ZEEKR X features a maximum output exceeding 300 kW and cruising range of more than 400 km. The 009 minivan features an intelligent cockpit and large 140 kWh battery, achieving a maximum cruising range of 822 km. The flagship model, 001, offers a maximum output of over 400 kW from dual motors with a range of over 580 km along with a four-wheel independent control system.

Element Six to lead DARPA UWBG programme

Diamond substrate expert to partner with Orbray, Raytheon, Hiqute Diamond, and the universities of Stanford and Princeton on next-generation semiconductors

ELEMENT SIX, part of the De Beers Group, will lead a US Defense Advanced Research Projects Agency (DARPA) programme to develop advanced UWBG (ultra-wide bandgap) semiconductors.

The goal is to develop UWBG substrates, device layers, and junctions, for next-generation electronics, including high-power RF switches, amplifiers for radar and communications, high-voltage power switches, high-temperature electronics for extreme environments, and deep-UV LEDs and lasers.

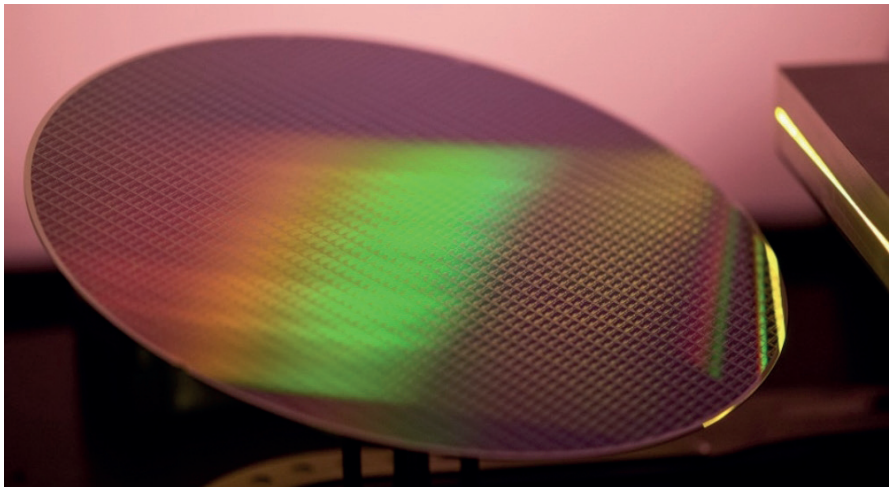
E6's contribution will harness the company's expertise in large area CVD polycrystalline diamond and high-quality single-crystal diamond synthesis, to realise 4-inch device-grade single-crystal diamond substrates.

E6 will be partnering with Orbray in Japan (with diamond heteroepitaxy expertise), Raytheon (leaders in GaN RF devices), Hiqute Diamond in France (with dislocation engineering expertise), and Stanford and Princeton Universities in the US (with materials bulk and surface processing characterisation expertise).

Daniel Twitchen, chief technologist at Element Six, said: "Industrial diamond has disrupted multiple markets since its first scale synthesis in the 1950s, and I am confident that technology breakthroughs in ultra-wide bandgap semiconductors will help unlock another 70 years of positive disruption in the semiconductor industry."

E6 polycrystalline diamond wafers over 4 inches in diameter are already enabling telecommunication infrastructures and defence applications, being used as either optical windows in EUV lithography for silicon chips, or in thermal management applications for high-power density silicon and GaN devices

E6 SC diamond was a crucial enabler in the CERN Large Hadron Collider's monitoring systems, helping lead to the discovery of the Higgs boson. In partnership with high-power semiconductor leader ABB, E6 realised the first high-voltage bulk diamond-based Schottky diodes. Furthermore, E6 recently completed build and commission of an advanced CVD facility using its core technology in Portland, OR, powered by renewable energy sources.



InP and TFLN: the way ahead for PICs?

IDTechEx report says addressing material challenges is crucial for advancing PIC technology

IDTechEx has published a new report, *Silicon Photonics and Photonic Integrated Circuits 2024-2034: Market, Technologies, and Forecasts* that explores emerging PIC materials including thin-film lithium niobate and barium titanite, along with new applications such as AI.

The report says that photonic transceivers for AI are poised to become the largest demand source for PICs, driven by increasing need for high-speed, efficient data processing in AI applications. Additionally emerging technologies such as programmable photonics, photonic quantum computers, and co-packaged optics will redefine the capabilities and applications of PICs, unlocking new potentials in computing, communication, and sensing technologies.

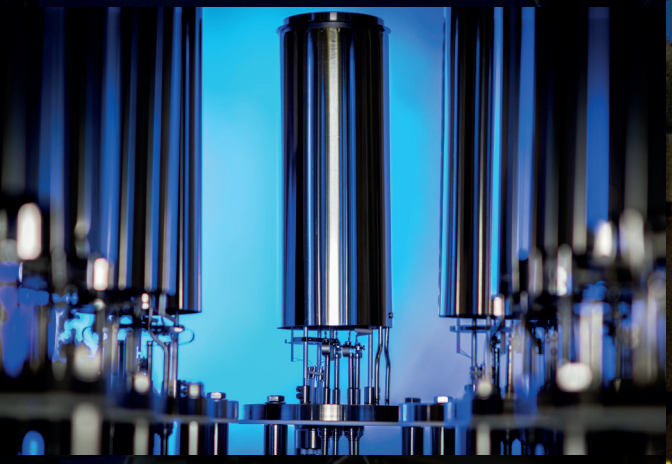
Despite these advantages, the PIC market faces several challenges. Material limitations complicate the development and performance of PICs.

While silicon and silica are common in current PICs, they are not the most efficient materials for light sources or photodetectors. This necessitates the combination of silicon with III-V materials; however, this brings another challenge to the table – integration complexity. Combining different materials and components into a single PIC requires intricate engineering and manufacturing processes, ensuring compatibility and consistent performance across the various materials.

While silicon remains dominant, several emerging materials are gaining traction. Thin-film lithium niobate (TFLN) offers moderate Pockels effect and low material loss, making it ideal for high-performance modulation applications, including quantum systems and future high-performance transceivers.

Monolithic InP continues to be significant due to its ability to detect and emit light, though it faces challenges related to high losses and costs. Barium titanite, known for its superior modulation performance, is anticipated to find applications in quantum photonic systems where modulation efficiency is paramount. SiN provides lower losses compared to other materials but comes with higher costs and larger device sizes due to its low refractive index, limiting its current widespread adoption.

RIBER's
MBE 6000



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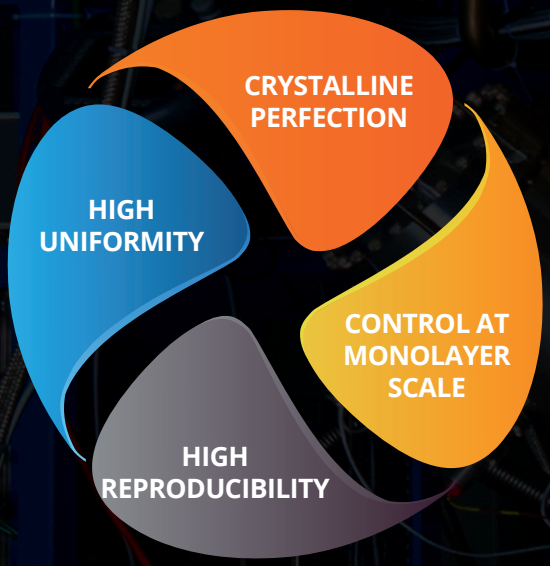
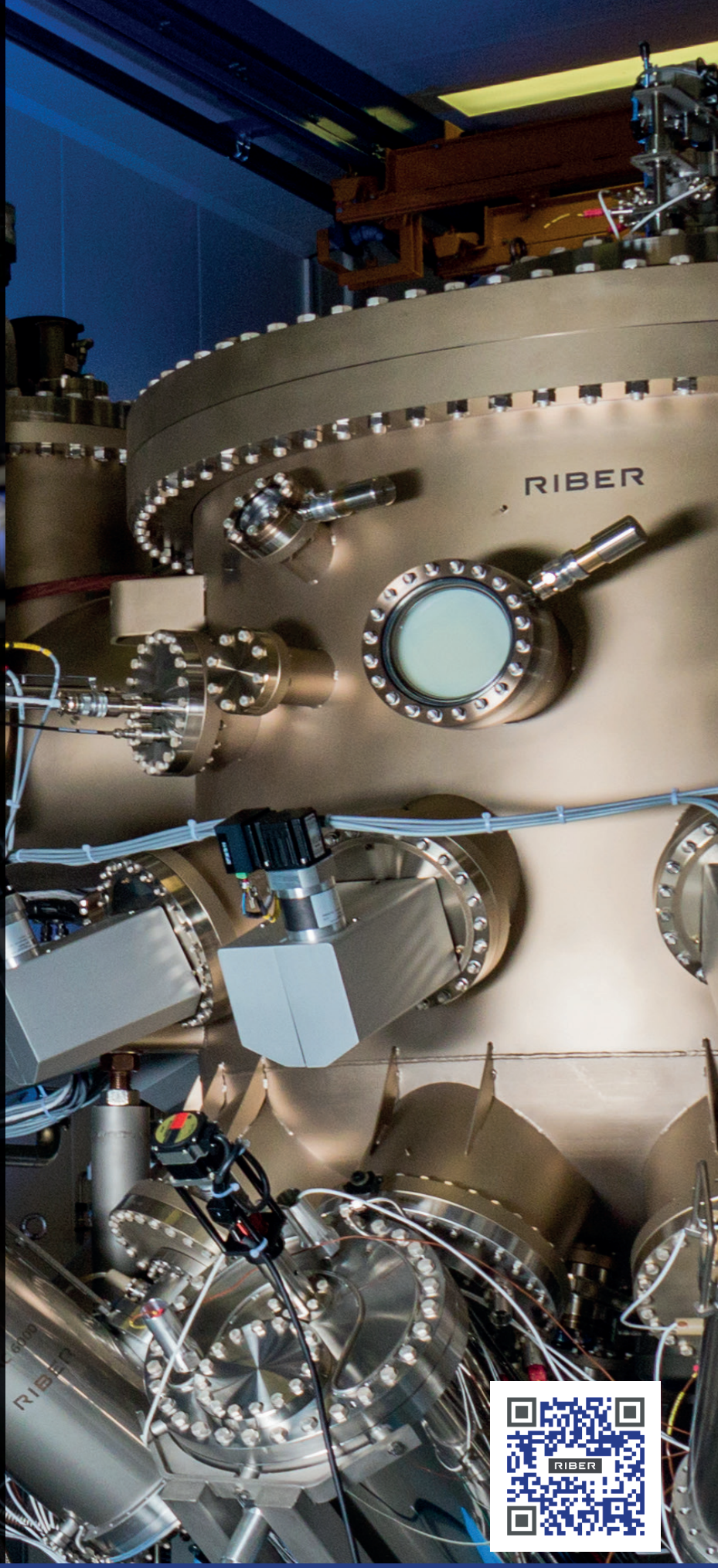
- LOW DEFECTS DENSITY





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CPV: Is a resurgence inevitable?

With record-breaking efficiencies and frugal materials usage, can concentrating photovoltaics (CPVs) succeed in tomorrow's solar sector?

SILICON IS THE entrenched technology for photovoltaics. Sales of panels made from this material are continuing to soar, supported by decades of high-volume production that cause prices to fall and ensure that this technology is ever more competitive. It's a direction of travel that leads many to assume that silicon will always hold a vice-like grip on the solar market.

But it's not a narrative everyone espouses. Calling it into question is Fraunhofer ISE academic Frank Dimroth, who is helping to commercialise a refined and superior design of CPV.

He argues that alternatives to silicon with superior efficiencies have good long-term prospects, based on the premise that investors in solar technology will always seek higher performances and a good return on the land they are using for power generation. Consequently, these investors want to select the solar technology that delivers the highest level of energy generation per unit area, a metric where silicon struggles.

The thought of shifting away from silicon will surprise many, given the vast amount of land that is unsuitable for the likes of farming and building dwellings.

➤ Dual-axis CPV systems developed by Fraunhofer ISE and Soltec, and incorporating five-junction cells from Azur Space Solar with an efficiency of around 44 percent, are designed to minimise both the bill of materials and production costs.

"But even in the deserts, [land is] not really always available, because there are constraints in terms of not having a huge impact on the environment," counters Dimroth, who points out that governments only permit a certain amount of land to be transformed into industrial renewable-energy fields. Conversations Dimroth has had reveal that in countries such as the United Arab Emirates, where the land that's available is quite limited, there is a strong desire to produce a lot of renewable energy, making high-efficiency PV very attractive.

Against this backdrop, today's silicon solar panels are already encroaching their efficiency potential. Due to this, there is motivation to switch to an alternative materials technology that will deliver a significant boost in the power generation density. While this transformation will not happen overnight, and the rise of any alternative will be far from easy, Dimroth believes that there is good reason to believe that silicon's dominance will diminish eventually.

The two leading candidates for delivering higher power densities are III-V multi-junction solar cells under high concentration (CPV) and tandem solar cells made of perovskite absorbers.

The latter already achieves high efficiencies in the laboratory, but there are concerns over its capability to maintain a high performance over many years.

According to Dimroth, the stability of perovskites used in high efficiency solar cells is a major challenge. "There is interaction with moisture, which is a fundamental problem," argues Dimroth, who points out that ion migration also takes place in this class of materials and has been found to accelerate degradation.

Due to this instability, it is not clear whether these cells will ever reach the 30-year lifetime that silicon has today.

"In terms of cost structure, you want to have a very reliable technology that keeps going over 30 years, because then you can depreciate your power plants over 25 or 30 years," explains Dimroth.

Modules that degrade before then fail to be commercially attractive, even if they offer gains in efficiency over silicon.

With CPV, cell efficiencies are ground-breaking – the current world record, held by Fraunhofer ISE, is 47.6 percent – and there are no concerns relating to the robustness and the reliability of this technology, which is quite similar to the solar cells used in space satellites for decades.

What's more, with CPV, volumes of materials required for power generation are relatively low. That's a big deal, argues Dimroth, given that solar deployments are forecast to climb substantially over the coming years, before plateauing at around 3.4 TW per annum in 2037. To put that figure in perspective, all the PV deployed until now stands at around just 1 TW.

If 3.4 TW were to be deployed using today's silicon PV, that would equate to 8.5 billion modules, covering an area of 15,600 km^2 – that's roughly half the size of Belgium. The resources consumed for this level of production are considerable, says Dimroth: "15,600 square kilometre would use all of the glass that is produced by the industry today, and, just as an example, three times more silver than is available on the market today."

While it is possible to increase production, using less material is more attractive, with CPV excelling in this regard.

A superior solution

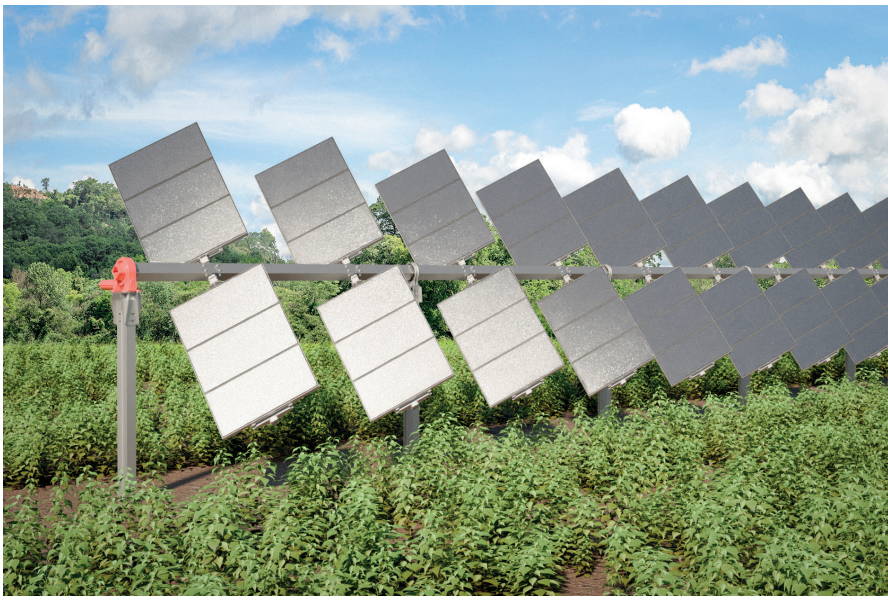
Working with partners of the German-government-funded project micro-CPV and the Spanish firm Soltec, which has tremendous expertise in tracker technology, Dimroth and his colleagues at Fraunhofer have developed a new generation of CPV that boasts a module efficiency of 36.5 percent.

At its heart is a five-junction cell in pilot production at Azur Space Solar. Sunlight at a concentration of 500 to 1000 suns is focused onto the cells, just 750 μm by 750 μm in size, using a combination of a Fresnel lens and a glass ball that's approximately 1 mm in diameter and sits on top of the photovoltaic cell.

One of the merits of this design is that by using such a small cell – leading to the phrase micro-CPV – active cooling is not required. Helping to aid the thermal management is a printed metal circuit with traces transferring the heat away from the cell.

Much effort has been directed at minimising the assembly cost of these micro-CPV modules, which are similar in size to silicon panels, and have all the components sandwiched between a pair of glass sheets.

Contributing to a trimming of the costs is the use of glass balls for secondary optics that are enabling concentration levels of 1,000 suns. These balls are already produced in high volumes, for example for reflectors in road networks.



➤ Operating at a concentration of 1000 suns, the CPV systems developed by Fraunhofer ISE and Soltec offer an increase in the energy yield from a given area of 30 percent compared with silicon.

As well as a minimised bill of materials, this micro-CPV design promise low assembly costs, realised by exploiting synergies with the emerging microLED display industry. To produce micro-CPV panels and microLED displays, myriad devices have to be transferred onto backplane, with a low cost for the panels key to commercial success. While Dimroth has not come up with all the solutions just yet, he's working on it, and looking to draw on what's been developed for the display industry.

Another lever for increasing the back-per-buck is a move to an even higher concentration. "I'm quite confident we can go to even 2,000 suns in the future," says Dimroth.

To help to refine, assess and validate their cutting-edge form of CPV, Dimroth and his co-workers are evaluating the tracker technology at the manufacturing site of Soltec, in Murcia, Spain.

"We want to demonstrate that this new tracking unit can fulfil the promises in terms of precision and economics," says Dimroth. There is hope that these efforts, involving dummy modules, will also attract investors keen to support the development of this micro-CPV technology and its tracking unit.

Looking further ahead, Dimroth hopes that in the next 18 months or so, the team will have a fully equipped prototype that fulfils expectation, in terms of power generation. This could provide the foundation for increasing manufacturing capacity for larger scale projects.

It's a sound plan that will hope to improve the prospects of CPV, which is the ultimate form of solar power generation, in terms of energy yield from a given area.

GaN: An escalating patents war

The battle over the intellectual property surrounding the GaN power transistor is intensifying, with EPC and Infineon attacking Innoscience over patent infringements that it vigorously denies

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WITHIN OUR INDUSTRY, last summer will be remembered as the start of a global war surrounding the intellectual property (IP) of the GaN power transistor. Back then, Efficient Power Corporation fired the first shots, accusing Innoscience of infringing four of its patents. In only a matter of days Innoscience shot back, denying any wrongdoing. More recently, another company has entered the fray, with Infineon claiming that Innoscience is also failing to respect its IP. And again, Innoscience is pleading innocence.

As claims and counterclaims are launched in courtrooms around the world, there is much value in hearing from those that combine expertise in this area with a neutral standpoint. Offering all this and more is David Radulescu, head of the patent litigation boutique firm Radulescu, who has been litigating semiconductor patents in courts throughout the US for three decades. More significantly, Radulescu also holds a PhD in compound semiconductor HEMTs and has previously devoted much effort to representing global companies fighting over IP associated with GaN-based LEDs.

In late July, Radulescu spoke for a second year in a row about the escalating IP war in a highly insightful webinar covering various patents that hold the key to deciding the outcome of the many court cases.

Before delving into details, Radulescu summarised the shots that had been fired to date: a pair of actions taken by both EPC and Innoscience in their battle, plus three fired by Infineon and another by Innoscience in their more recent skirmish.

This all kicked off last summer, when EPC announced it took legal action against Innoscience for infringing four of its patents. In the intervening months, EPC dropped two patents in its International Trade Commission (ITC) case, while initial rulings have been released on the other two this July. According to the administrative law judge (ALJ) in the ITC, both of EPC's patents are not invalid, but significantly, one of them is infringed.

What's also worth noting is that in the last couple of months action taken by Innoscience in China has also led to rulings that counterpart Chinese EPC patents were not invalid.

"We have Innoscience on its own turf losing in the Chinese Patent Office," remarked Radulescu, who added that the US Patent and Trademark Office (USPTO) is still considering the validity of the patent found to be infringed by the ALJ, although the claims and prior art at issue are identical.

Radulescu offered a closer look at the key patents after highlighting the recent stockpiling of US patents issued to Innoscience. In the past year-and-a-half, the Chinese chipmaker was issued 45 US patents, while EPC was issued only one, leading Innoscience to outpace EPC in the total number of US patents by 58 to 57.

Gate designs

Focusing on the shape of the gate structure is EPC's '508 patent, which the ALJ found to be not invalid but also not infringed. To put this patent in context, over the last few decades, a number of different gate structures have been used to produce GaN transistors, including: those that are self-aligned, with the gate and the insulator underneath having the same dimension (length); and those that have a T-shape or an inverted T-shape. The '508 patent describes a multi-step process involving the use of three different photoresist patterns to produce a self-aligned gate.

For the claims brought by EPC concerning this patent, the key issue, according to Radulescu, is whether "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact," describes the Innoscience process.

"When you visually look at the [Innoscience] device, you see a gate ledge that is not co-extensive with the gate contact layer," said Radulescu, who is not surprised that the ALJ viewed this transistor as being different from that of EPC, and thus concluding that there was no infringement.

The other important matter relating to the '508 patent is that Innoscience has asserted that it is invalid, an argument that was rejected by the ALJ.

Doping and compensation

Radulescu believes that those involved in ruling on the EPC-Innoscience battle will have a more difficult decision to make when it comes considering claims surrounding the '294 patent entitled 'Compensated Gate MISFET'. In his view, what's crucial is to understand what is meant by 'compensated', against the backdrop of the difficulties that have had to be overcome to realise *p*-type doping in GaN, key to producing LEDs with this material system.

The key claim by EPC is whether the phrase 'compensated GaN layer' describes the GaN layer in Innoscience's devices that is presumed to be *p*-type based on its own publications.

It's important to note, argued Radulescu, that EPC's patent does not say anything about the GaN layer's carrier type or its resistivity, characteristics that can be measured. Instead, it just uses the word 'compensated', a characteristic far harder to judge. This is because a picture or image of the device material is not determinative, but requires an understanding of semiconductor material science.

The other key point that Radulescu emphasised is that the '294 patent covers simply a transistor, and makes no reference to enhancement-mode or depletion-mode devices.

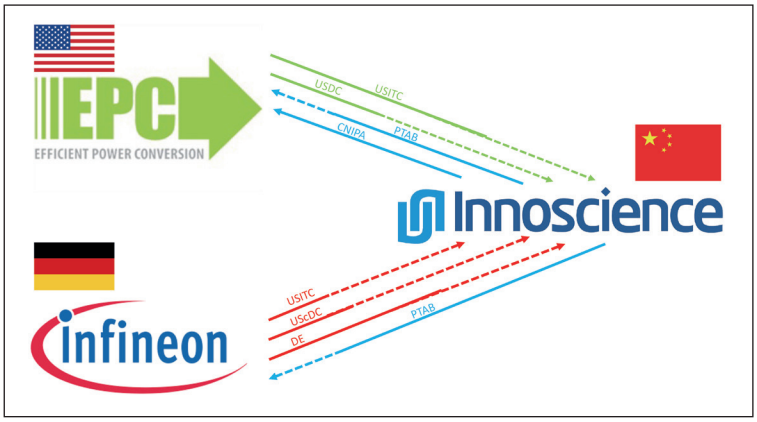
Many are assuming that the GaN employed by Innoscience is *p*-type. "They introduced magnesium, and I will be willing to bet that the hydrogen is intentionally removed after growth," remarked Radulescu, whom added that secondary ion mass spectrometry (SIMS) plots have been disclosed during the case. "Whether or not you can call it 'compensated' depends upon how you define what compensation is," added Radulescu.

Innoscience has argued that they do not employ a compensated GaN layer because they use a Schottky gate, as well as claiming that SIMS data reveals dopant activation, and testing confirms *p*-type conductivity. According to Radulescu, all these arguments were rejected by the ITC staff due to procedural errors of its counsel. For example, Innoscience offered evidence of the nature of the GaN through the testimony of an employee, an account viewed as problematic due to self-interest.

"Unfortunately for Innoscience, I don't think their best arguments were put forward," commented Radulescu, who explained that the full Commission will now review the ALJ's initial determination of infringement and issue a final decision on the investigation called a Final Determination, which is expected to issue in early November 2024.

Both Innoscience and EPC have tried to claim victory from the initial determination. Innoscience argues that it has won, because one of the patents was determined to not be infringed, while EPC is focusing on a finding of infringement.

The view of Radulescu is that while, in theory, EPC lost on three patents out of four, what really matters



is that it has a ruling of a violation of the ITC statute against unfair competition by importing products that infringe US patents. And he believes that given how Innoscience's lawyers argued their defences, it will be far from easy to get the ALJ's determination reversed or modified, although not impossible.

Looking ahead, in March 2025, the US Patent Office will rule on the validity of the four patents asserted by EPC against Innoscience (which are also still at issue in EPC's District Court case against Innoscience in California). If the '294 patent is determined to be invalid, this decision could be appealed, dragging the case on for a couple more years. Significantly, under this scenario, the ITC's final determination will likely not matter as any potential importation ban would be expected to be stayed pending appeal. On the other hand, if the '294 patent is determined to not be invalid, and at the same time the full Commission agrees with the ALJ on infringement of the '294 patent, Innoscience's products found to infringe would presumably be subject to some form of importation ban as that is a typical remedy available to patent owners in these type of ITC investigations.

Infineon versus Innoscience

Infineon's actions against EPC began in March this year, when they brought a suit in San Francisco for a patent associated with high-voltage packages featuring so-called 'source sensing'. Innoscience response to this has been to file a petition this June with the US Patent Office, arguing for invalidation of every single claim.

Meanwhile in Germany, Infineon has also filed several cases, as well as obtaining a preliminary injunction that prevented a small fraction of Innoscience's high-voltage GaN transistors from being promoted at PCIM.

Commenting on this, Radulescu remarked: "Infineon outmanoeuvred Innoscience's lawyers, because they got that injunction without Innoscience actually being heard on any of the issues. It was a surprise, but not unusual for parties to go to Germany to try to get these preliminary injunctions and mess up trade shows."

Within the last few weeks, Infineon has stepped up its action, adding three more patents to the San Francisco case, and filing its own complaint with the ITC. On the merits, the first of four Infineon patents that have been asserted involves an additional connection to the source of the power transistor, so that the parasitic elements associated with the packaging and connections have a reduced impact on overall system performance.

Infineon's accusations centre on Innoscience's use of a Kelvin source that it claims practices the patented source sensing functionality, as well as an identical pin layout. Like Infineon's products, those in question from Innoscience have 8 pins, including one that's a Kelvin source sensor.

Regarding the three other patents, one is concerned with the thickness of a titanium nitride capping layer in an electrode stack. The other two concern so-called 'merged cascode transistors', with one patent concerned with adding curvature to inter-digitated fingers to trim the electric field strength at the edge of the electrodes, and the other associated with combining a depletion-mode transistor with an enhancement-mode transistor to make a circuit. If the case is not settled beforehand, the ALJ's initial rulings on these patents are not expected until autumn 2025.

While it is impossible to predict the rulings of all the asserted claims to date in the GaN patent war, there is no doubt that substantial time and money will be spent over the next few years trying to defend IP and the products based on them. There are many different outcomes that could emerge, including licensing deals and import bans – but what is for sure is that interesting times lie ahead.

Ready or not, AI is here to stay

The combination of AI and machine learning, in conjunction with automation, optimisation, and exception management, holds the key to improving the running of every compound semiconductor fab

BY JON HERLOCKER FROM TIGNIS

IN TODAY'S WORLD, everywhere we look we see claims of how Artificial Intelligence (AI) will disrupt our world. If you take these assertions at face value, you might start thinking that AI is some kind of magic that will solve almost all of humanity's issues. However, that's not the case. To ensure the successful application of AI, appropriate inputs and a level of creativity are mandatory. The reality is that the successful implementation of AI in a manufacturing environment is a combination of mathematics, science, and innovation.

While previous waves of AI enthusiasm have failed to deliver broad market benefits, today's and tomorrow's AI is certain to play a critical role in compound semiconductor manufacturing. Companies that successfully adopt either AI, machine learning (ML), or both of them before their peers will benefit from significant competitive advantages. According to management consultant McKinsey, AL/ML currently contributes between $5 billion and $8 billion to annual earnings at semiconductor companies – and that figure is forecast to increase ten-fold over the next two-to-three years.

Leading-edge device makers manufacturing at 10 nm and below are already years into their journey of deploying AI. For these chipmakers, their revenue and market valuation are justifying investing billions of dollars into custom-built AI solutions for their state-of-the-art fabs.

Despite manufacturing at mature process nodes, compound semiconductor fabs have much to gain from AI and ML (see Figure 1). That's because successful AI/ML projects focus on business value metrics that matter.

One famous formulation of business value in a manufacturing facility is based on Goldratt's Rules of Flow, which postulates that the two most important metrics for any factory are throughput and cost. AI/ML can directly improve both. Impacts include enhancing throughput by increasing yield and uptime, and trimming operating costs by reducing scrap and increasing engineering productivity.

It is possible to significantly improve throughput and cost metrics via AI/ML without having to invest millions of dollars of capital on new hardware. And if you have a leadership role in a compound semiconductor fab, part of your job in the next decade will be deciding where and when to invest in ML.

In addition to the core business properties outlined already, there are two additional business considerations of note: agility and resiliency.

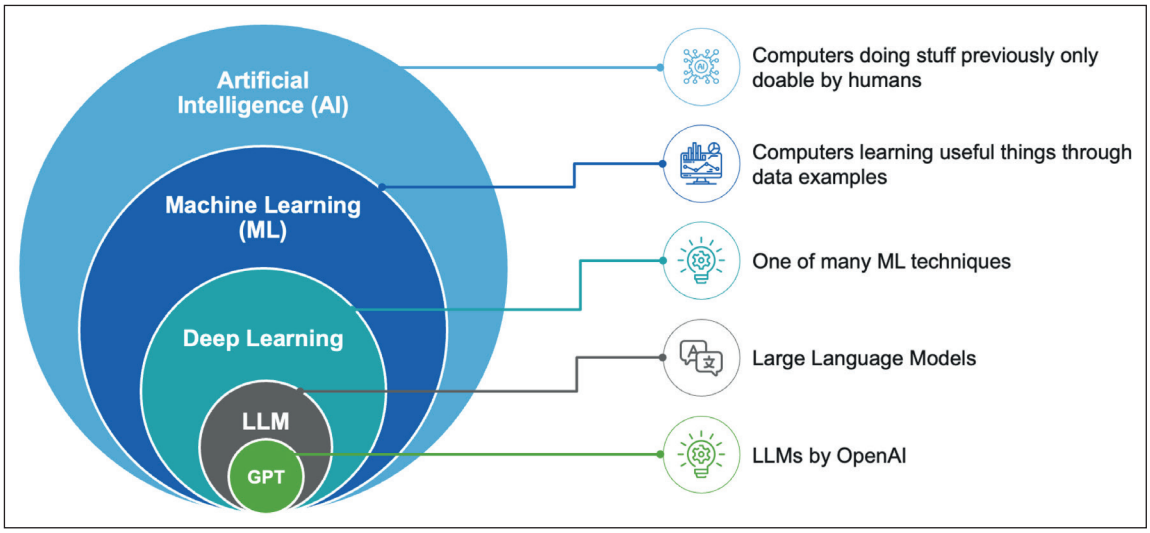
Agility is the ability of a business to adapt to changes more quickly. How fast can you respond to changes in raw materials due to obsolescence? Or a change in product mix due to a market shift? And what about a dramatic change in workforce availability? There could also be market changes – like we are seeing with the opportunity in electric vehicles for makers of SiC and GaN power electronics.

When it comes to resiliency, this reflects the ability of a business to survive or even thrive in the face of losses – those of key personnel, equipment, customers, and facilities.

To understand where you should be considering applying AI/ML to improve productivity, agility and resiliency, you need to think about automation, optimisation, and exception management.

The first of these three considerations, automation, is the reduction of human intervention in a process. Human intervention tends to take place when there is the need to make a decision, or there is a need for human dexterity. AI/ML is a great enabler of increased automation. Turn to automation when you have humans spending non-trivial time on repetitive tasks, from tweaking recipes all the way to updating spreadsheets.

Optimisation is about making the best possible decision from the available data. It becomes a true superpower when paired with automation, enabling the equipment in your fab to continuously adjust key



➤ Figure 1. Decoding AI/ML terminology. A Venn diagram of the most popular ML tools.

parameters, so that it remains in an optimal range of operation. You should think about the times where you need to make human decisions regularly, and revisit the results of past decisions – for example, the parameters of your process recipes, your scheduling logic, or your preventative maintenance schedules.

The third consideration, exception management, is a core foundation of more advanced fabs (operationally, not by process node). While automation and optimisation are about creating increasingly predictable processes, even in the best fab environments, disturbances and exceptions happen. Equipment fails, software suffers from bugs, operators do unexpected things, material sometimes fails to meet specifications. As you automate more of your fab, how do you even know when something is wrong, or is about to go wrong? You should look to AI/ML to reduce exceptions, to better detect exceptions before they cause damage, and to diagnose and resolve exceptions more efficiently.

When we consider these three factors when applying AI/ML, one can sum it up as saying that more automation means less human intervention – lower cost, faster cycles, and more agility/resiliency. Meanwhile, optimising throughput and costs have direct and measurable business value, and exception management ensures that manufacturing processes remain stable and available, minimising exception cost. Automation, optimisation, and exception management all deliver direct revenue or cost benefits.

While AI is not magic, don't dismiss it as a distraction. It will move the business needle. It will increase your wafer flow, it will reduce your operational costs, and it will also increase your fab's agility and resiliency. There's no doubt that AI and machine-learning will become a critical part of the compound semiconductor manufacturing world, with those successfully adopting AI early enjoying significant competitive advantages. For those that fail to appreciate AI, their oversight will be seen in inferior balance sheets.

Superior sealing

Greene Tweed's portfolio of precision seals offers tremendous support to empower the growth of the compound semiconductor industry

BY PRAGATI VERMA AND THYAG SADASIWAN FROM GREENE TWEED

FROM ULTRA-FAST communication and electric vehicles to energy applications and artificial intelligence, today's most innovative technologies rely on compound semiconductors. Excelling where silicon falls short, the unique properties of these chips support the innovation that's required for tomorrow's breakthroughs.

Given the growing demand for compound semiconductor technologies, it's of little surprise that this industry is generating substantial and growing sales. While well-established devices – such as LEDs that serve in general lighting and GaAs-based power amplifiers that are a key ingredient in mobile phones – no longer enjoy rapidly rising revenues, sales are growing fast in other sectors. The most notable of these is that of SiC power electronics, now deployed in automotive, industrial, energy, and rail applications. According to semiconductor market research analyst Yole Group, the SiC device market will increase in value to $10 billion over the next five years, with SiC substrate and epiwafer shipments growing to over 3 million units.

When it can't fail

Driven by opportunities to grow their revenues, many makers of compound semiconductor devices are pursuing capacity expansion plans. Their investments will take many forms, from tools for epitaxial growth and metrology to securing a steady supply of a number of inconspicuous yet indispensable components.

The latter includes products that play a critical role in the manufacture of compound semiconductors, such as the patented Chemraz sealing technology developed by our company, Greene Tweed.

Well known for having have a strong pedigree in this area, we are a global leader in perfluoroelastomer (FFKM) Chemraz sealing solutions. It's an enviable position that we are not taking for granted, as we continue to lead the way with multi-million-dollar investments in facilities, alongside the launch of several new products and manufacturing automation technologies.

Several prominent chipmakers depend on our Chemraz seals. Using them for the production of their most powerful chips, they view second-best seals as not good enough for challenging manufacturing environments.

Demand for our products is growing as chipmakers turn to our Chemraz O-rings and sealing solutions for more demanding processes, where they are able to prevent contamination while withstanding aggressive chemicals and extremely high temperatures. When operating in the world's harshest semiconductor manufacturing applications, our products combine a tremendous level of performance with exceptional reliability.

Another factor that makes our Chemraz seals indispensable relates to the increasing need for ultraclean processing in manufacturing applications. As the first sealing solutions company to use cleanroom manufacturing in the US, we fully understand the significance of ultraclean operations in the semiconductor industry. We have devoted much effort to ensure that our seals control particle excursions that threaten contamination, while they increase uptime and boost wafer yield.

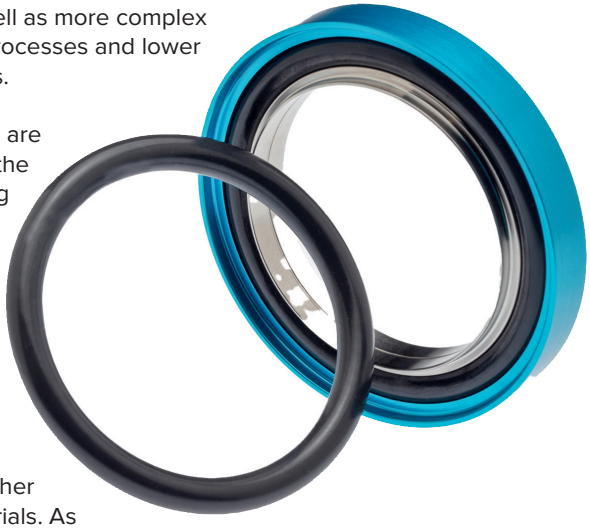
Balancing performance and costs

Greene Tweed understands that not every semiconductor application needs a Chemraz sealing solution. That's where our Fusion FKM (fluoroelastomer) products come in. They are field-tested in extreme temperatures, high pressures, corrosive chemicals, and volatile fluids.

The Fusion 707 has been specifically developed for flat panel display CVD and dry plasma etch equipment, where seal reliability and minimal contamination are essential. The 707 family of seals provides excellent chemical resistance and withstands various aggressive chemicals. Related to them is the Fusion 706 – it is ideal for a range of plasma equipment applications, from etch and plasma-enhanced CVD to plasma ashing applications, as well as those that must accommodate low sealing force materials, such as bonded slit valve gates.

Introduced earlier this year is the Fusion F07. This sealing solution is crafted to withstand common etch and CVD oxygen/fluorine-based gases in semiconductor processing sub-fab lines. The F07 handles continuous operating temperatures up to 180°C and has a minimum expected lifetime of six months. These figures are both better than those for standard FKM seals serving in the same applications. What's more, the F07 offers a lower cost of operations than premium FFKM materials.

That's not all. Greene Tweed's products help trim the costs of upgrading to larger wafers, such as a move from 150 mm to 200 mm. Note that the manufacture of compound semiconductor, such as SiC, is more expensive, due to the high cost of material, as well as more complex manufacturing processes and lower production yields.



Many companies are trying to reduce the costs of switching to larger wafers by acquiring older tools and modifying and retrofitting them with software upgrades, so that they can work with the likes of SiC, or other compound materials. As some of these tools come with older and obsolete components, we are offering upgrade seal kits to improve the capabilities of older refurbished tools, a more prudent alternative to making massive investments in entirely new equipment. By upgrading tools so that they can incorporate the latest high-performance sealing solutions required to prevent contamination and maintain a cleanroom environment, compound semiconductor manufacturers can increase throughput and yield, critical to meeting the surge in demand while optimising profitability.

Scaling up to provide chipmakers with the products that they will need during the anticipated boom is far from trivial. But the recent industry-wide supply crunch gripping the FFKM materials, which has coincided with a global surge in demand for chips, has given us valuable insights into how to meet the burgeoning demand while minimising the impact of possible disruptions.

Building on these insights, we are rolling out six major initiatives to ensure that we can promptly deliver high-performing sealing solutions, as customer needs evolve to meet the growing demand for semiconductors. These six initiatives, which we go on to discuss in detail, are: a new manufacturing facility in Korea; new innovations, designed for harsh conditions and expansion; the introduction of next-generation manufacturing to accelerate growth; the use of secured resources; fortification of supply chain resiliency; and ensuring that we are ready for the new tools that chipmakers will invest in.

A new facility in Korea

We are making significant investments to expand our global manufacturing capacity and capabilities within the semiconductor market. This initiative is exemplified by our construction of a new 6,500 m^2 facility in Ochang, Cheongju-si, Chungcheongbuk-do, South Korea. Our new factory is equipped with end-to-end manufacturing process capabilities – from initial extrusion of raw materials to warehousing finished products. We have already

started producing samples, and later this year we will transition to commercial production.

Featuring cleanroom space to maintain a pristine environment vital for components supporting chip fabrication, our new facility in South Korea will initially focus on our flagship Chemraz product line.

As well as increasing global capacity, this new facility for producing Chemraz products is underscoring our commitment to supporting customers based in South Korea and the surrounding region, including notable semiconductor leaders. This facility, which is creating a healthier global supply chain, will help us shorten lead times, build stronger co-development strategies with key customers, and enhance business continuity plans.

Aside from advanced manufacturing technology, our state-of-the-art plant in South Korea is equipped with solar panels and greywater recycling facilities to mitigate the environmental impact.

What's more, our new facility is designed with scalability in mind. It offers ample room for growth, enabling us to expand our production capabilities as demand increases. Over the next few years, we will be implementing a phased rollout of new production lines. This effort will begin by increasing capacity and adding automated equipment to enhance our production processes and reduce our lead times. Beyond that, we will be focusing on expansion, including an additional cleanroom, and integrating cutting-edge manufacturing technologies and processes.

Our long-term strategy is to ensure that we remain agile and responsive to our customers' evolving needs, while the demand for semiconductors grows over the remainder of this decade and beyond.

Outperforming in harsh conditions

As a global leader in FFKM seals, Greene Tweed knows that our Chemraz seals are critical for the most advanced semiconductor fabrication processes. To support our customers' growing needs, we have introduced two new high-performing, price-competitive products – the Chemraz G38 and G57.

This pair of products are designed to meet the evolving needs of various plasma applications, while being incredibly price competitive and delivered with world-class lead times. By expanding our line-up in this way, we are demonstrating our commitment to continuously innovating and responding to the demands of the market and ensuring that our customers have the best solutions at their disposal.

Custom-engineered to meet the demands of aggressive dry plasma systems, our Chemraz G57 technology provides improved plasma resistance and minimises contamination, resulting in less downtime and higher wafer processing yields in both static and dynamic oxide etch wafer-processing applications. This product has excellent chemical resistance and withstands temperatures up to 300°C, making it ideal for several applications, including endpoint windows, window seals, slit valve seals, bell jar seals, isolator valve seals, chamber seals, valve seals, lid seals, KF fitting seals, and gas inlet seals.

Meanwhile, the Chemraz G38 is targeting high-density plasma systems, where seal reliability and minimal contamination are essential. The G38 has excellent chemical compatibility and is capable of

Expanding our manufacturing capacity is just one of the prongs of our multi-faceted strategy that is laying the foundations for supporting a strong upturn in the market. To ensure world-class lead times, we have secured a reliable supply of raw materials from multiple suppliers. With these partners, we are well-positioned to cater for an anticipated ramp in chip production over the next two years

withstanding a variety of aggressive chemicals. Recommended for bonded gate seals and chamber seals, this product delivers exceptional value in a number of applications, including deposition, remote plasma cleans, oxidation, diffusion, ion implant, implant anneal, and rapid thermal processing.

Our development of new technologies continues at pace, and we have another Chemraz sealing solution ready to roll out in the next 6-12 months. Helping to encourage us in this endeavour is the adoption of our existing sealing solutions, including Chemraz and Fusion F07 FKM, in semiconductor fabs being built all around the world.

Next-gen manufacturing

We are committing significant resources to automating manufacturing processes, as this enables us to scale capacity and quickly meet the growing needs of our evolving semiconductor customers. By supplementing core manufacturing processes with robotics and digital solutions, we are supporting production floor employees to eliminate process bottlenecks and trim lead times.

Our largest investments are associated with high-impact process steps, such as compression moulding, inspection, and packaging. The reasoning behind this is that it maximises efficiency and productivity gains. For compression moulding, operators are currently responsible for moving and servicing moulds between every cycle. However, we are moving towards an automated approach, using a 6-axis robot to move moulds. This will allow the operator to focus only on value-added activities and service more moulding presses. Similarly, for current packaging operations, our operators are responsible for bagging and labelling parts individually – this is slow and tedious. Due to this, we are introducing an automated solution, involving multiple robots and an automatic bagging machine, as this will increase throughput and standardise bagging quality.

We are also building and utilising digital twins. It's a move that will allow us to proactively evaluate new innovative technologies and discover how to best introduce them into existing manufacturing facilities.

By turning to these technologies and dedicated technical resources, we are transforming our production lines. They are becoming more adaptable, and they are allowing us to scale up quickly to meet our customers' needs without compromising on excellence.

Secured resources

Expanding our manufacturing capacity is just one of the prongs of our multi-faceted strategy that is laying the foundations for supporting a strong upturn in the market. To ensure world-class lead times, we have secured a reliable supply of raw materials from multiple suppliers. With these partners, we are well-positioned to cater for an anticipated ramp in chip production over the next two years.

While running four factories with balanced workloads, we have significantly increased our workforce to stabilise the production process, in conjunction with bolstering our manufacturing capabilities by introducing new equipment in our plants in Korea, Taiwan and Selma. As well as keep pace with growth, these strategic moves

will enhance our production capabilities, minimise delays, and accelerate delivery times.

Fortified supply chain resiliency

As we work to secure a steady supply of raw materials, we are proactively reducing our reliance on a single vendor or market. Here's why: The industry-wide FFKM supply crunch, which occurred during the pandemic-led surge in demand for semiconductors, has taught us the importance of diversifying and strengthening our supply chain. That's why we have carefully selected multiple sources of raw materials, located in separate regions.

Proactively identifying and mitigating many potential risks, ranging from those that are geo-political to those associated with regulatory matters and climate change events, has enabled us to build comprehensive supply chain resiliency, as well as a business continuity plan that we share with customers

to ensure transparency. By securing raw materials and building supply chain resiliency, our customers benefit from reduced downtime, helping them to meet the incredibly tight production schedules they face during fast-increasing demand when markets are booming. This is critical in many sectors within the semiconductor industry, where missing a time-to-market window threatens to slash sales.

Preparing for new tools

Our innovation in sealing solutions supports the unique needs of the compound semiconductor market, as well as the latest technology inflections in the silicon industry.We work with OEMs across these markets as they upgrade their tools to serve their customer base. Whether it's the latest innovations in etch or in deposition, we are taking proactive steps to keep up with market demand and growth.

For example, our bonded slit valves, lip seals, seals for electroplating solutions, vacuum line solutions, cryogenic seals, and many other sealing solutions are continuing to be widely adopted by equipment makers, creating value and yield enhancement for both silicon and compound semiconductor fabs. Most recently, Xyfluor materials have been qualified for use in electrostatic chucks that can operate at temperatures as low as -40 °C.

Ready for growth

Building cutting-edge compound semiconductor chips is a challenging, cost-intensive process that hinges on small yet essential components, such as our sealing solutions. Working closely with our customers and partners, we are ready to address the burgeoning need for sealing solutions from chipmakers, thereby ensuring the scalability and sustainability of their operations for the rest of this decade and beyond.

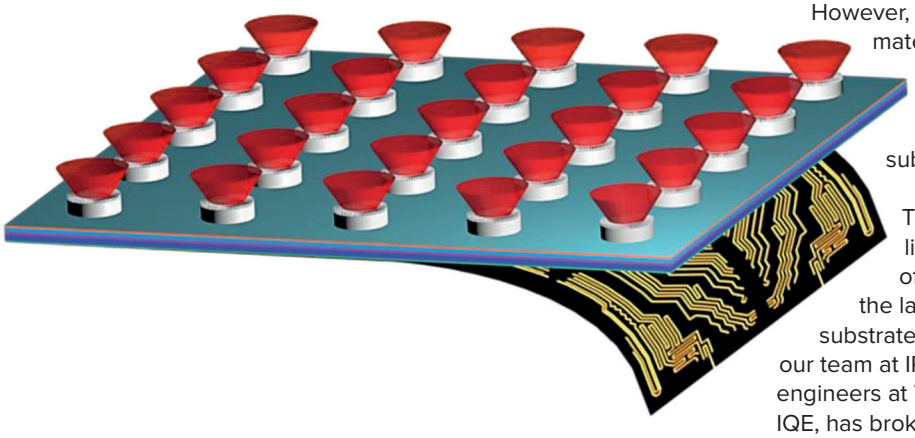
Monolithically integrated QCLs on silicon

Low-strain quantum cascade lasers with optimised metamorphic buffer layers are closing the gap to realising reliable, high-power, infrared sources on silicon

BY ENRIQUE SANCHEZ CRISTOBAL, AHMAD AZIM AND LUKE MILLBOCKER FROM IRGLARE, MATTHEW FETTERS, AMY LIU AND JOEL FASTENAU FROM IQE, AND ALEJANDRO VILLALOBOS MEZA AND ARKADIY LYAKH FROM THE UNIVERSITY OF CENTRAL FLORIDA

FOR DESIGNERS of semiconductor lasers, quantum wells are a fundamental building block for these nanoscale devices, as well as an incredible asset. Not only do these devices serve as effective generators of laser light through radiative recombination processes, but the use of quantum well engineering also allows for control of emission wavelengths through changes in material composition.

Common semiconductor lasers, such as laser diode and the VCSEL, emit at wavelengths determined by the difference between the lowest energy levels of the electrons in the conduction band and the highest energy of the holes in the valence band of the quantum well material. This is a limitation that can be overcome by another unique semiconductor structure, the quantum cascade laser (QCL), which achieves lasing through inter-sub-band transitions associated with different excited states of the conduction bands of two materials. (see Figure 1). At the heart of this semiconductor device is a superlattice composed of two alternating materials whose conduction bands work together to create a periodic quantum well structure, which emits infrared photons under an applied electrical bias. The material composition of the superlattice constituents can be varied to achieve emission in a broad infrared range, and the periodic nature of this structure enables a single electron to generate multiple photons as it cascades through the superlattice (see Figure 2).



While QCLs are not as well-known as diode lasers and VCSELs, they are produced commercially, and are used in a range of critical sectors, including defence, spectroscopy, and free-space communication. In these applications they serve as compact, high-powered infrared sources that span the mid- to long-wave infrared range, thanks to a highly tuneable quantum well superlattice structure. More recent designs can deliver a continuous-wave output power of several watts at room temperature, enabling them to play pivotal roles in applications such as defence, where their low atmospheric losses at critical spectral windows allow them to be used in direct infrared countermeasure systems. Another important application is in the field of imaging, where QCL-based infrared microscopy has been successfully deployed for the rapid, precise classification of different cancer tissues.

Up until now, QCLs have usually been produced with lattice-matched material systems, such as InP. However, while this is conducive to maximising material quality and device performance, it also significantly limits the opportunities for this device, due to the high cost and low scale of native substrates.

The solution to overcoming this limitation is to modify the fabrication of QCLs to be able to account for the lattice mismatch between non-native substrates and the active layers. In this regard, our team at IRGlare, working in partnership with engineers at The University of Central Florida and IQE, has broken much new ground. Our triumphs

include the first demonstration of monolithic integration of QCLs onto lattice mismatched substrates, and pioneering efforts related to the growth of these lasers on silicon. We are one of two groups to provide the first demonstration of integration of QCLs onto silicon – our team and another reported this success around the same time – and we trailblazed the integration of these lasers onto large-diameter silicon substrates. Another noteworthy claim of ours is that, until recently, our QCLs on silicon produced the highest performance on this foundation.

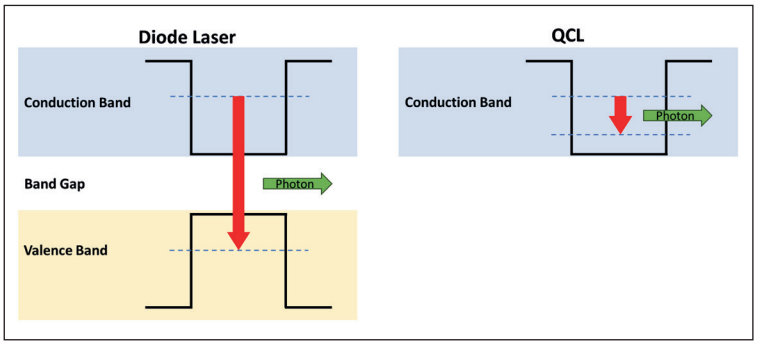
Silicon integration

In the remainder of this article, we detail our efforts at producing high-performance QCLs on silicon. These lasers employ an InP cladding, surrounded by an active region that's composed of alternating InGaAs and AlInAs layers that serve as quantum wells and barriers, respectively. By adjusting the composition of these materials, we either match the lattice-constant to the surrounding InP, or we target zero accumulated strain to maximise the quality of the epitaxial material – a crucial factor in ensuring laser performance.

One of the big attractions of growing QCLs on silicon is the opportunity to take advantage of the scalability and cost-efficiency of silicon technology. Thanks to the ubiquity of silicon in modern electronics, substrates made from this material are cheaper and far more accessible than the InP substrates that III-V-based QCLs traditionally rely on for good performance. Realising the direct epitaxial growth of QCLs on large-diameter silicon substrates offers the tantalising prospect of manufacturing compact infrared platforms that support both the electronic and photonic components on a single chip.

As well as the technical benefits of integrating complex components on a single compact chip, silicon substrates offer the benefit of massively upscaling the production and yield of standard QCLs, as silicon wafers with diameters that are larger than 200 mm are readily available. These large-diameter wafers, coupled with the exceptionally compact nature of standard QCLs, promise to enable the processing of significantly more QCLs on a single wafer, all while reducing the cost of production.

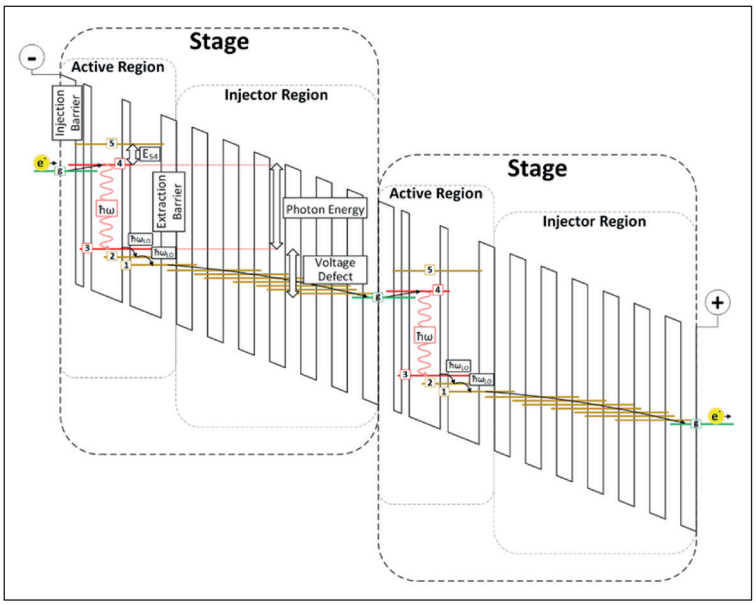
While success on this front would be a wonderful evolution for QCL technology, standing in the way is a significant hurdle. If this technology is to be viable, it is vital to reconcile the substantial lattice constant mismatch between InP and silicon. A threat that's faced when undertaking the epitaxial growth of InP QCLs on lattice-mismatched substrates is the creation of defects in the material that propagate through the epitaxial layers to reach the laser core, where they degrade device performance and reliability. However, despite this complication, researchers have produced QCLs on non-native substrates, with efforts currently focused on bridging the gap and delivering the performance that QCLs provide on native substrates.



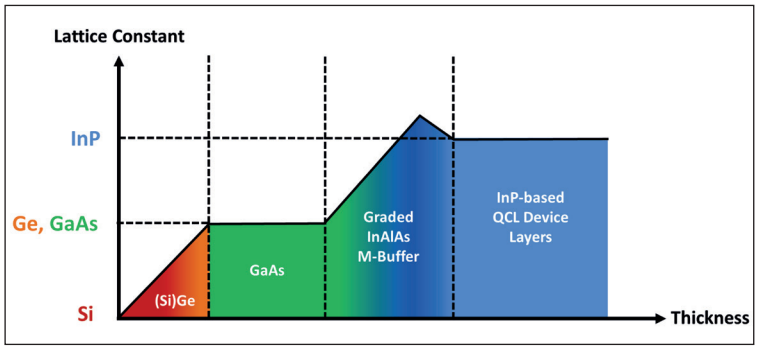
➤ Figure 1. Optical transitions in laser diodes (left) and QCLs (right). While transitions in laser diodes are limited by the tuneability of the material band gap, QCL optical transitions occur between excited conduction band states of two materials which make up a periodic quantum well structure. Engineering of these layers and their compositions allow QCLs to emit light in the range of 3-14.

One way to partially address the issue of lattice mismatch is to introduce metamorphic buffer layers, which gradually transition the lattice constants between adjacent layers of different materials during epitaxial growth. By slowly adjusting the lattice constant, it is possible to trim the density of defects that can hinder laser performance and reliability (see Figure 3).

Our initial efforts to integrate QCLs on lattice-mismatched substrates began with GaAs substrates,



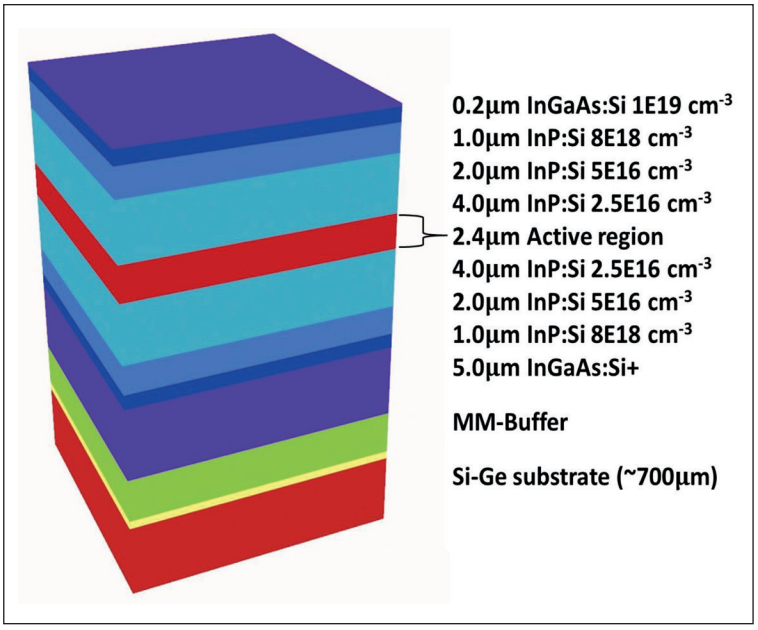
➤ Figure 2. Diagram of a stage, or period, of the periodic quantum well structure that is generated from the conduction bands of the two alternating superlattice constituents. Injected electrons experience optical transitions before undergoing several non-radiative transitions and reaching the end of the QCL stage. Electrons are then injected into the next stage, where they repeat the process and continue to generate infrared photons.



➤ Figure 3. The metamorphic buffer design for a medium-wave infrared QCL on silicon alleviates strain from lattice mismatch by gradually transitioning the lattice constant between adjacent materials along the growth direction.

which have a lattice mismatch of 4 percent with InP – half that of silicon. We produced a mid-wave infrared QCL with a highly strained laser core, incorporating a metamorphic buffer to drive down the defect density in the active region. These ridge-waveguide lasers operate at room temperature. Despite the lattice-mismatch, initial processing runs provided a good yield.

Building on this work, we monolithically integrated this design on a 150 mm germanium-coated silicon substrate template, utilising a graded InAlAs metamorphic buffer. These QCLs lase up to 170 K, but yield is low, and these devices consistently experience degradation after only 30 minutes. According to material characterisation of these preliminary designs, to ensure a good performance on silicon, strain in the material must be reduced. Options to realise this include introducing a low-strain laser core design and improving the metamorphic buffer designs.



➤ Figure 4. Waveguide design of a third generation long-wave infrared QCL structure, produced on a silicon substrate, employs an improved metamorphic buffer and a lower-strain active region.

Drawing on these initial attempts, more recently we produced a third-generation laser, this time emitting in the long-wave infrared range. This ridge-waveguide QCL design combines reduced strain in the laser core with an improved germanium-coated silicon substrate featuring a reduced defect density. Our design employs a modified metamorphic buffer, formed from interleaving GaAs and AlInAs layers, and an additional InGaAs layer beneath the InP cladding (see Figure 4). For this QCL, we use a 200 mm wafer, the largest in this analysis.

Our third-generation design delivers a dramatic improvement over the second-generation variant. Our successor boasts a good performance, delivering 3 W of pulsed power at room temperature, and according to M^2 parameter tests, provides a good gaussian beam quality (see Figure 5). In addition, our third-generation QCL provides excellent reliability, with no signs of degradation after 10 hours of operation at maximum power. Another encouraging observation is a good yield of functional devices. What's more, we can make many more laser chips from a single substrate, compared with what may be typically harvested from smaller InP substrates.

Based on all these merits, our QCL shows great promise for the future of this class of laser on silicon. Our findings illustrate the impact of improving material quality through low-strain laser core designs and improved metamorphic buffers.

Characterising material quality

The strengths of our third-generation design are evident in the materials characterisation of a range of structures. We have compared this third-generation silicon-QCL heterostructure to older generation mid-wave designs grown on InP, GaAs and silicon – the latter substrates have lattice-mismatches with InP of 4 percent and 8 percent, respectively.

As expected, X-ray diffraction reflection spectra of the lattice-matched sample show sharp superlattice satellite peaks, indicative of high crystal quality (see Figure 6). The positions of these peaks confirm that the superlattice period is within 1 percent of the expected value. For all the structures with lattice mismatch, there is a broadening of the diffraction peaks, preventing the gauging of the superlattice period. Despite this, the diffraction peaks of the lattice-mismatched samples reflect a successful transition of lattice constants from silicon to InP, as indicated by the distinct peaks of each alloy present in the spectra.

A major challenge facing every grower of QCL structures on mismatched substrates is maintaining a smooth surface required for device processing and operation. We have investigated surface morphology with atomic force microscopy, considering values of root-mean-square surface roughness for scans over a 20 µm by 20 µm area.

We find our QCLs lattice-matched to InP have the smallest surface roughness, never exceeding the thickness of a single monolayer (0.1-0.2 nm). Lattice-mismatching increases surface roughness, with values of 3.2 nm and 22.3 nm, respectively, for mid-wave emitting active regions grown on GaAs and silicon. However, refining the growth of the metamorphic buffer and the bottom cladding layers – these are the improvements introduced in our third-generation QCL – delivers a reduction in surface roughness to 4.9 nm (see Figure 7). This observation provides further evidence of the benefits of our latest design.

To understand the impact of the metamorphic buffer on defect suppression, we have scrutinised our samples with transmission electron microscopy, a technique that enables high-resolution imaging of defects in crystalline structures. This form of microscopy shows that the metamorphic buffer helps to reduce the defect density in the active region around structures grown on silicon. However, in the structure associated with our second-generation QCLs, large defects are present within the active region, as well as in the surrounding cladding material. In stark contrast, no defects are spotted in or around the active region of the QCL on native InP (see Figure 8). Such findings are consistent with the poor reliability of our second-generation QCLs.

Another insight provided by transmission electron microscopy is the level of effectiveness of the modified metamorphic buffer in reducing defect density. In our third-generation QCL, defects originating at the Si-Ge/GaAs interface are reflected back into the substrate. It is also worth noting that while defects persist in the cladding layers, the active region is devoid of large-scale defects that plague our second-generation QCLs (see Figure 9).

Quantifying defect density is ineffective when inspecting samples 'head-on' with transmission electron microscopy, because this leads to a limited view of the surrounding cladding. It is more informative to turn to plane-view imaging to determine defect density in specific regions. By taking this approach (see Table 1 for the results of our analysis), we have found that the defect density in our third-generation QCLs exceeds both the first- and second-generation variants, and is beaten in this regard only by QCLs on native InP substrates. We view this result as incredibly promising, demonstrating a substantial improvement in the realm of lattice-mismatched substrates that will inform future QCL designs.

Through our efforts we have solidified the connection between higher-quality material and more-reliable, high-performance QCLs on non-native substrates. The performance of our third-generation QCLs, produced on 200 mm wafers, provides proof of the innate scalability and cost-efficiency when transitioning to this foundation. By switching to a silicon substrate, we create high-quality devices on a wafer that is more cost-effective and has the potential to yield four times the number of functional devices that can be realised on 50 mm InP wafers.

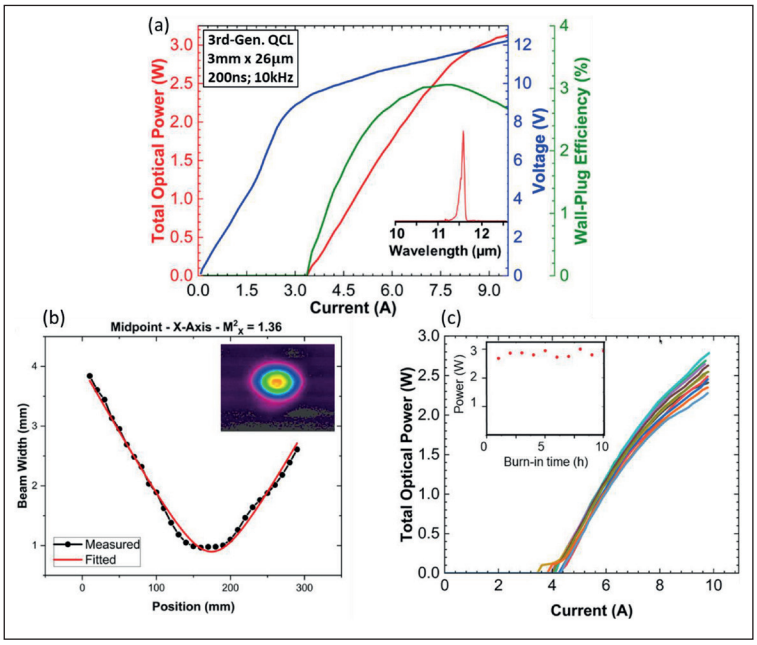


Figure 5. (a) Pulsed light-current-voltage (L-I-V) plots for a third-generation QCL. This device reached a maximum power of around 3 W. (b) M^2 measurements determine the deviation from a perfect gaussian beam, with M^2 =1 denoting a perfect gaussian beam. A high quality single-lobed beam was measured. (c) Pulsed light-current-voltage for multiple third-generation devices shows excellent short-term reliability.

While much progress has been made, we are not resting on our laurels. Instead, we are striving to improve the design and optimisation of metamorphic buffers, as well as the overall quality of silicon substrates. However, our results represent a clear step towards marrying the high performance and versatile spectral range of QCLs with the accessibility of silicon-based platforms. Our ultimate goal is to integrate QCLs on silicon without compromising their performance, so they are as good as they are on a native foundation.

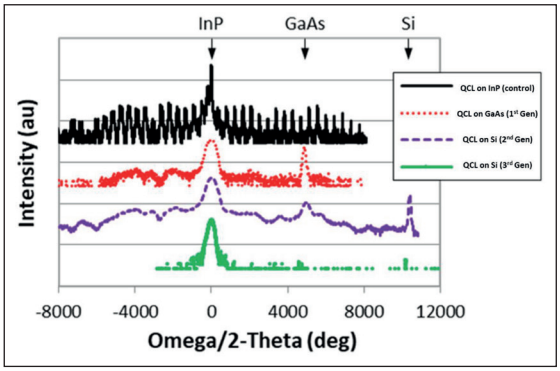
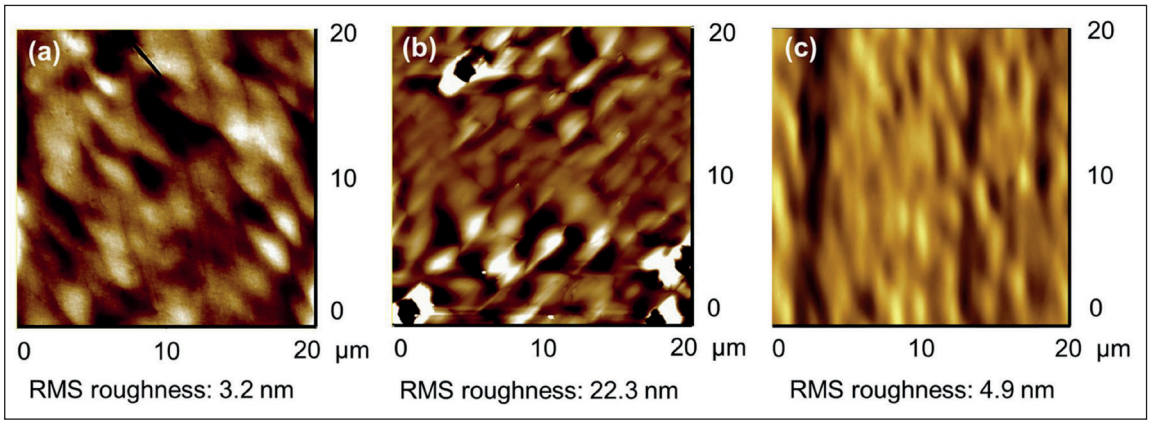


Figure 6. (004) Reflection high-resolution X-ray diffraction spectra for the four samples discussed in this work.



➤ Figure 7. Atomic force microscopy surface roughness images for a 20 µm by 20 µm area of (a) first-generation, (b) second-generation and (c) third-generation structures. Note that the first-generation structure is grown on a GaAs substrate, while second and third-generation structures are grown on silicon substrates.

Another aim, building on our success with QCLs-on-silicon in the long-wave infrared, is to replicate these results in the mid-wave infrared. To excel in this regard, we will have to employ design techniques such as lower-strain superlattices and reduced stage numbers, as well as placing greater emphasis on ensuring sufficient strain-reduction through strain-balancing the quantum wells and barriers. If we succeed, we will pave the way for game-changing infrared platforms, while further cementing QCLs as indispensable infrared solutions for myriad applications.

Conflict of Interest Statement: Arkadiy Lyakh owns stock in IRGLARE, LLC and as such may benefit financially as a result of outcomes of the research or work reported in this publication.

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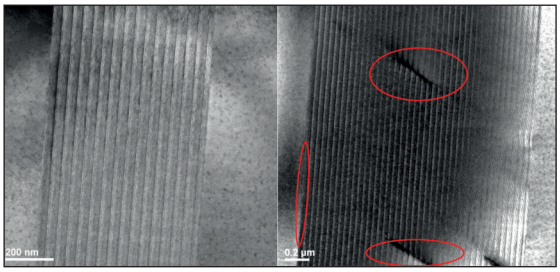
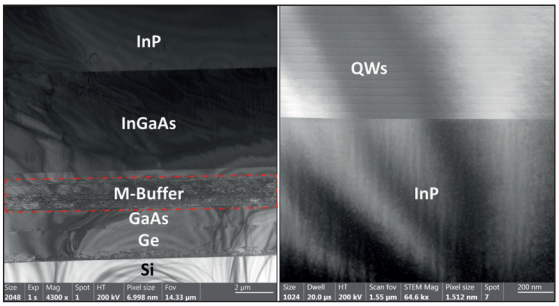


➤ Figure 8. Transmission electron microscopy images of an active region of a QCL grown on a native substrate (left) and the second-generation QCL, grown on silicon (right). The active region of the QCL grown on a native substrate (InP) appears entirely devoid of any defects, while the active region of the second-generation QCL has large linear defects, evident on the cladding and within the laser core (encircled).



➤ Figure 9. (Left) Transmission electron microscopy image of epitaxial layers of the third generation of QCL, grown on silicon. Inspecting the metamorphic buffer, circled in red, reveals that very few defects propagate past this buffer and into the mostly intact InGaAs layer. (Right) Transmission electron microscopy image of the active region and surrounding InP cladding of the third-generation QCL shows that it is devoid of the large-scale defects previously seen in the second-generation QCL, also grown on silicon.

Substrate	Defect density (cm^{-2})	Area (μm^2)
50 mm InP	1.6×10^7	100
150 mm GaAs	5.5×10^7	100
150 mm Si	7.1×10^7	100
200 mm Si	2.4×10^7	90

➤ Table 1. The defect density found in QCL structures produced on a range of substrates.

FURTHER READING / REFERENCE

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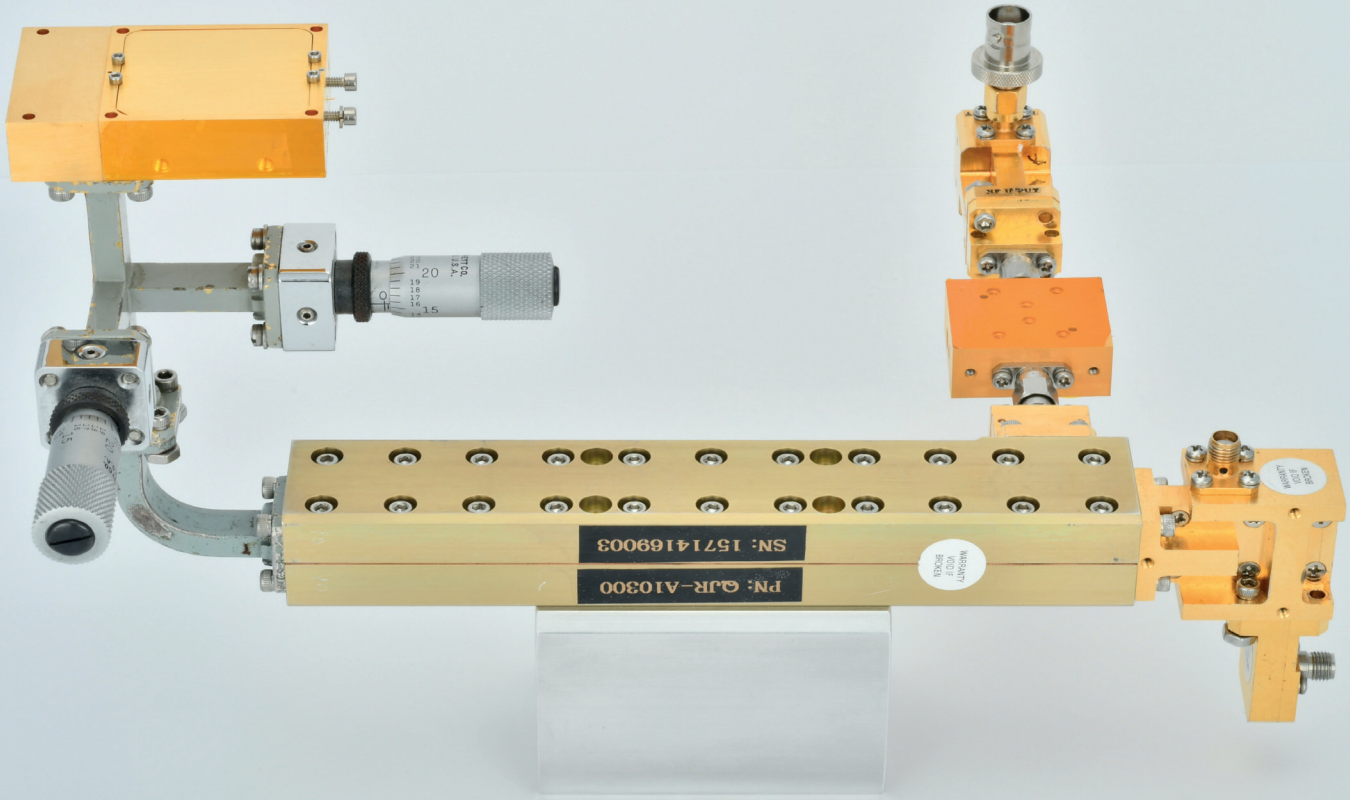


Revolutionising RF oscillators with GaN

GaN IMPATT diodes can enable compact and efficient solid-state oscillators that deliver higher powers in the millimetre-wave and beyond

BY ZHENGLIANG BIAN AND SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY

TO ADVANCE MODERN RF applications, much effort is directed at realising a higher RF power within a compact form factor. There are a number of solid-state devices that can do this, but the most compelling for efficient high-RF-power generation is the impact ionisation avalanche transit time (IMPATT) diode. This form of diode, which is capable of delivering an exceptionally high output power from a few gigahertz to hundreds of gigahertz, can replace elaborate multiplier and amplifier chains.

While you may not be that familiar with the IMPATT diode, it is certainly not a new device. Its inception dates back to 1958, when W.T. Read, working at Bell Laboratories, proposed a simple *p-n* structure that consists of a narrow avalanche carrier multiplication region followed by a drift region (see Figure 1). Read theorised that a 180° phase shift occurs with the applied voltage, due to the combination of the time delay associated with avalanche multiplication and the transit time of the injected carriers traveling through the drift region. This phase shift gives rise to a negative resistance that contributes to RF power generation.

In 1965 the first IMPATT oscillation was observed, in a device made from silicon. This triumph laid the groundwork for significant advances in IMPATT technology over the following decades, including the deployment of this device in satellite communications and radar systems. Today, a single commercial IMPATT diode, mostly realised with silicon technology, is capable of delivering 400 mW under continuous-wave mode and 20 W under pulsed-mode operation at 94 GHz.

Embracing GaN's benefit

Despite the success of the silicon IMPATT diode, the quest remains to develop higher-performance devices that draw on current RF technology. Throughout the evolution of the compound semiconductor industry, new materials have played a pivotal role in pushing the boundaries of device performance. It is a state-of-affairs that is

no different with the IMPATT diode, where GaN in particularly is reviving interest in this device.

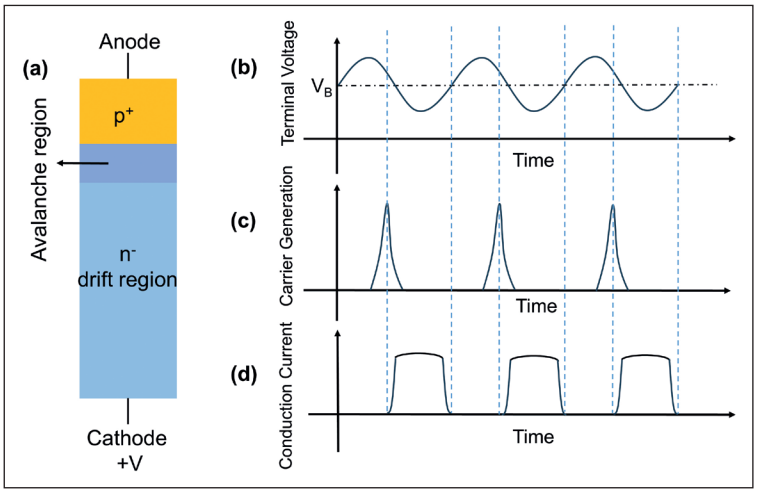
Due to its tendency to be deployed as an oscillator, the primary performance metric for the IMPATT diode is its power-frequency trade-off. Analysis reveals that both the output power and the oscillation frequency of an IMPATT diode are mainly determined by the critical field and the saturation velocity in the base material. The output power of the diode is proportional to both the square of the critical field and the square of the saturation velocity, and inversely proportional to the square of the frequency. Based on these relationships, GaN clearly has the upper hand over silicon (see Figure 2), thanks to a critical field that is 10 times higher, and twice the saturation velocity. Combining these attributes indicates that the GaN IMPATT diode has a 400 times higher power capability than its silicon counterpart at a given frequency.

Another promise of the GaN-based IMPATT diode is that it is projected to have a much higher cut-off frequency – it is in the terahertz range – due to its shorter avalanche response time. This makes the GaN IMPATT diode an attractive solid-state terahertz source that could enable various novel applications, such as high-resolution imaging through opaque materials for medical diagnosis and security screening, and extreme wideband wireless communications.

Current status

Unfortunately, engineers have struggled to convert the tremendous promise of the GaN IMPATT diode into a high-performance device. But the good news is that this situation is starting to change. Helping to facilitate this are improvements in producing low-defect-density bulk GaN substrates, high-quality epitaxy growth, and effective edge terminations – all these advances are crucial to routinely realising avalanche in GaN *p-n* diodes.

Initial efforts with GaN involved embedding a *p-n* diode in a series resonate circuit and observing an 800 MHz oscillation. This weak, low-frequency oscillation has been attributed to limitations



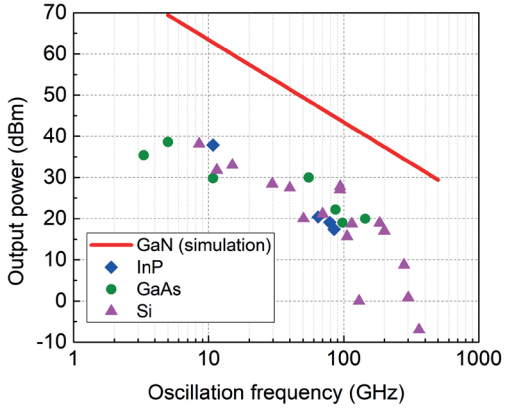
➤ Figure 1. (a) The design of the Read-type IMPATT diode. (b) Voltage transient at the cathode for an IMPATT under oscillation. (c) A carrier generation waveform in the avalanche region. (d) The induced terminal current for an IMPATT under oscillation.

associated with significant device self-heating and low-quality oscillation circuitry. Improvements were wrought by placing the diode on a copper heat sink and testing it under pulsed mode in a waveguide resonate cavity. This recent work, involving a GaN IMPATT diode, enabled a peak power of 30 dBm to be extracted up to 21 GHz.

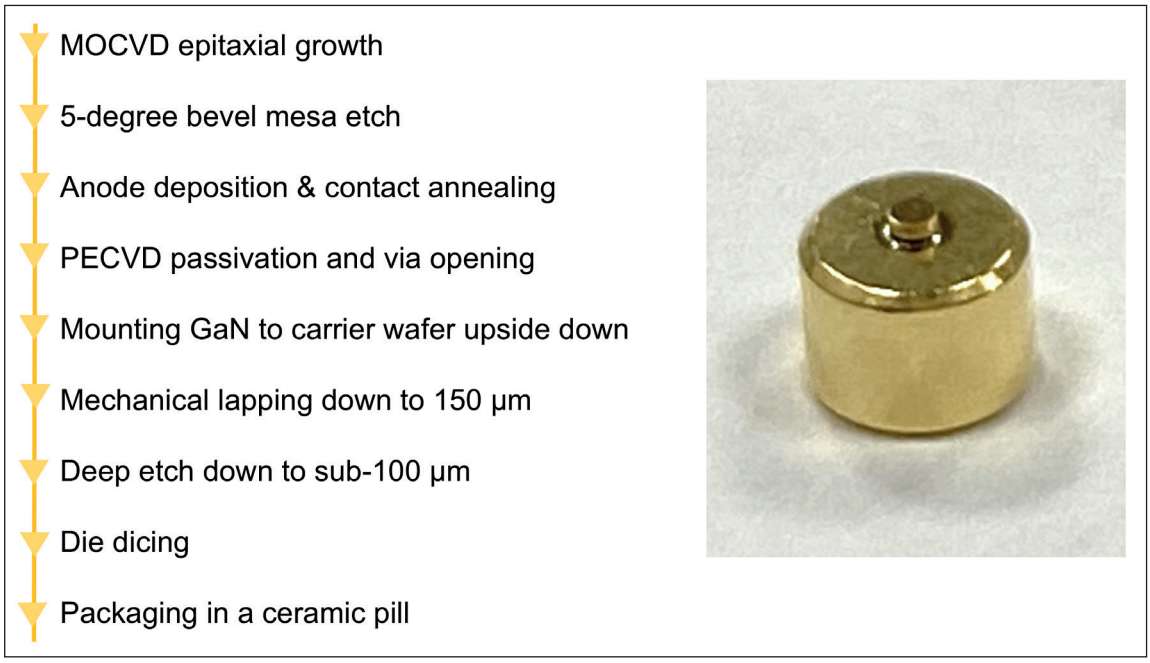
While these results are encouraging, as well as failing to unlock GaN's potential, they don't even exceed the performance of their silicon counterparts. Why is this? It's because GaN is held back by immature fabrication techniques. In sharp contrast, the performance of silicon IMPATT diodes draws on refinements in device fabrication and packaging procedures that result in a robust avalanche, minimised series resistance, and adequate heat removal – all are crucial.

With GaN, the fabrication processes for excelling on these fronts are still immature. To address these weaknesses, our team at Stanford University is pursuing the following pair of goals: the development of a substrate thinning process that results in 20 μm-thick wafers that do not lead

Material	Si	GaAs	InP	GaN
Bandgap (eV)	1.12	1.42	1.34	3.42
Critical field (MV/cm)	0.3	0.4	0.5	3.3
Electron saturation velocity ($\times 10^7$ cm/s)	1.0	1.2	0.7	2-2.5
Electron mobility ($cm^2/(V{\cdot}s)$)	1350	8500	5400	1000
Thermal conductivity (W/m/K)	130	55	68	200



➤ Figure 2. Material properties for various candidate materials for IMPATT oscillators, and a power-frequency benchmark plot.



➤ Figure 3. The process flow for fabricating our GaN IMPATT diodes, and a photo of a packaged diode.

to degradation of avalanche in the fabricated diodes; and flip-chip packaging to a type IIA single crystalline diamond heat sink, to ensure enhanced heat dissipation.

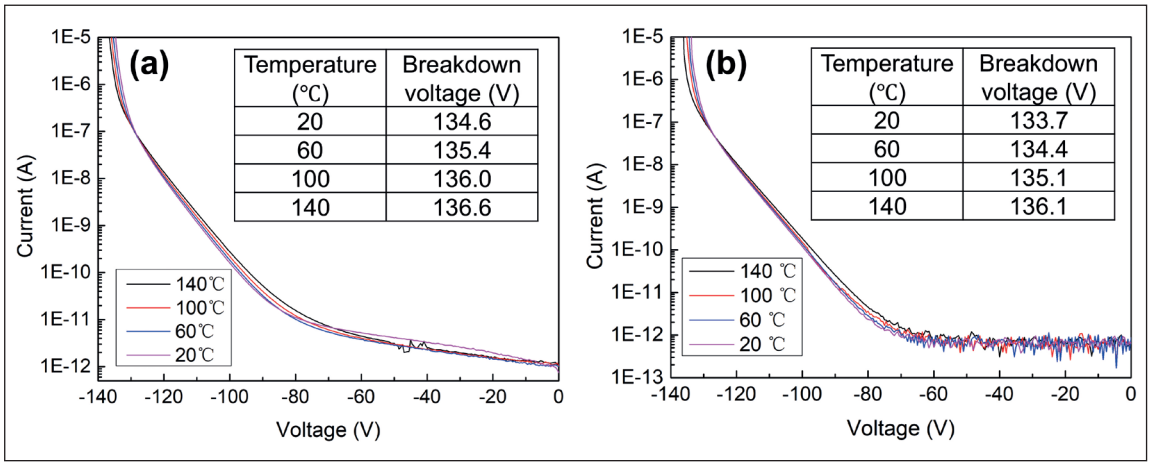
Innovative fabrication processes

Vital to our success is the introduction of a new process flow, involving diode fabrication, substrate thinning and packaging (this is illustrated in Figure 3). We begin by growing our desired epilayers by MOCVD on native bulk GaN substrates, and then incorporate a 5° bevelled mesa etch to mitigate field crowding around the mesa corner and enable avalanche. Here, our key technology is the introduction of a thinning and packaging process that does not compromise the avalanche in the diodes.

Note that a thinning process is critical to achieving high-frequency IMPATT diodes. For those made from silicon and operating in the W-band, a thickness of less than 10 µm is employed to minimise the series resistance coming from the substrate. A number of methods have been reported for realising a thin film of GaN, such as laser lift-off, nickel stressor spalling, and photoelectrochemical etching. However, none of these methods has been shown to enable avalanche compatibility.

We have overcome this obstacle with a two-step thinning process. This begins with mechanical lapping, to thin the GaN wafer down to around 150 µm, before we turn to a more gentle etching process for additional thinning. By adopting this hybrid approach, we avoid the threat of shattering the GaN wafer during the thinning process.

Validation of this process has come from examining the current-voltage characteristics of our diodes after thinning (see Figure 4). Plots reveal that the breakdown voltage does not change for our diodes on a thinned 20 µm-thick GaN wafer, and the leakage current remains minimal. The results also show a positive temperature coefficient in the breakdown voltage, confirming preservation of avalanche behaviour.



➤ Figure 4. Breakdown characteristics comparison between diodes on (a) an un-thinned 400 µm-thick wafer and (b) a 20 µm-thick wafer after thinning.

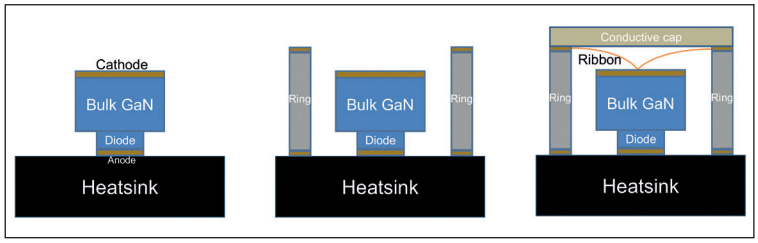
One of the benefits of thinning our substrates from 400 μm to 20 μm is a trimming of the total on-resistance by 43 percent, thanks to elimination of series resistance originating from the substrate. However, there is an increase in contact resistance, which indicates that the formation of the backside contact after the thinning process demands additional improvement to maximise the benefit of substrate thinning.

It is important to properly package our IMPATT diodes before they are embedded in an oscillation circuit. For this task we select a flip-chip-style ceramic pill package, as shown in Figure 5. In this configuration, a heat sink is directly bonded to the anode to quickly remove the heat that's generated around the *p-n* junction.

For this packaging process, we begin by bonding the GaN IMPATT diode to a diamond heat sink by thermal compression, and then solder quartz rings, which serve as a mechanical support and electrical isolators. Formation of the cathode follows, realised by connecting the backside of the diode to the top conductive seal with gold ribbons. We have optimised this packaging process for GaN to obtain an IMPATT diode that's free from any degradation in breakdown characteristics.

First Ka-band oscillation

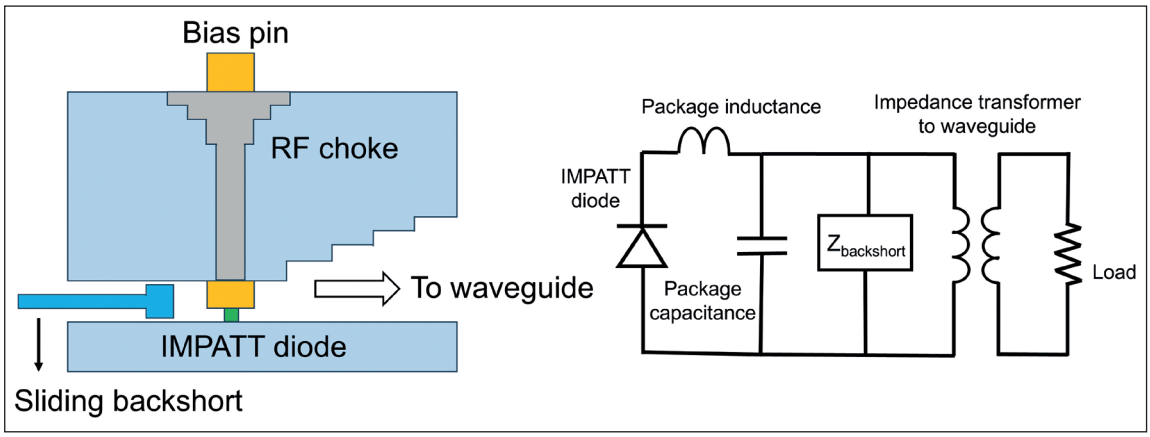
It's not been easy to observe and measure the IMPATT oscillation produced by our packaged devices. To do so requires extensive co-design of device characteristics and packaging, as well as circuitry optimisation. The equivalent circuit of an IMPATT oscillator, shown in Figure 6, highlights the need for a tuning network to provide sufficient impedance matching and obtain the desired oscillation characteristics.



➤ Figure 5. Flip-chip style packaging can improve the performance of GaN IMPATT diodes.

Initially, we embedded our packaged diodes in a waveguide resonate cavity. This is the most rigorous way to test IMPATT, as it replicates how commercial IMPATT diodes are used in real scenarios. With this approach, we recorded first Ka-band oscillations when biasing the diodes into the avalanche regime. However, these diodes could not survive for long enough for us to achieve optimal tuning. We suspect that breakdown occurred from air-arcing inside the package, due to the small spacing between the grounding plane and the GaN substrate in a flip-chip configuration.

While we focused on additional optimisation of our packaging to improve the reliability of our IMPATT diodes, our collaborators from QuinStar Inc. engineered a microstrip cavity (see Figure 7(a)) that enabled us to measure IMPATTs more systematically without complex packaging requirements. This is



➤ Figure 6. The waveguide resonate cavity and its simplified equivalent circuit under free-running oscillation.

a valuable adaptation, as short-loop feedback and device insight are very important when pursuing research and development.

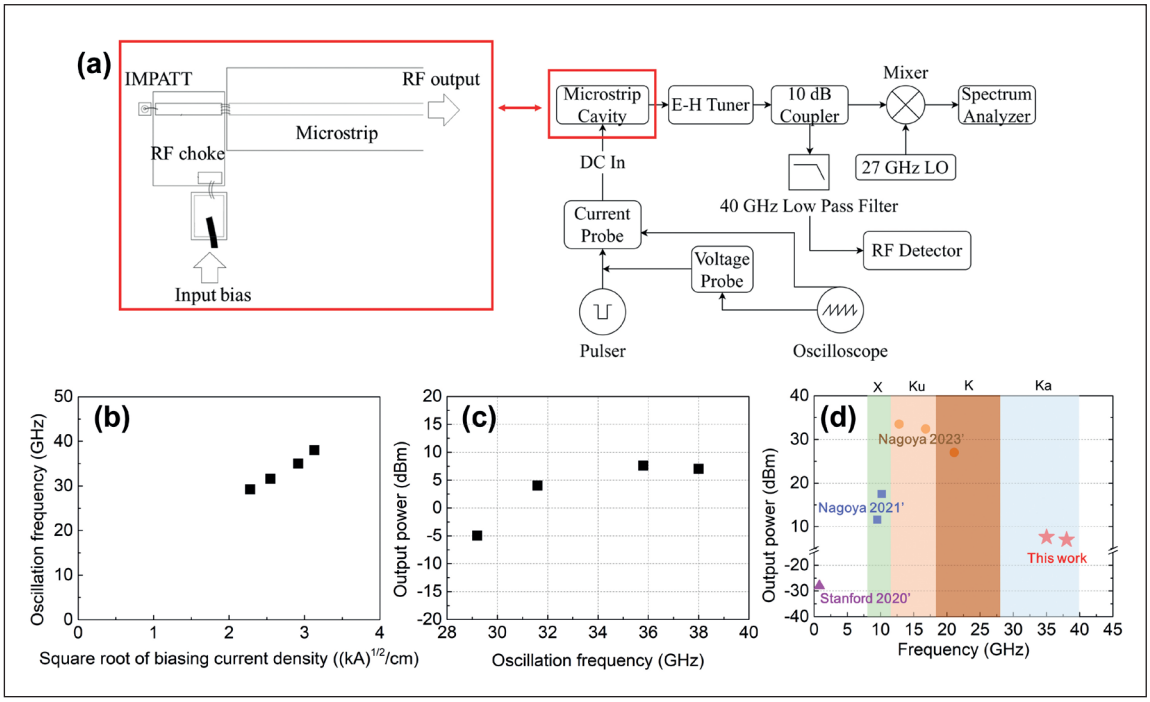
We have mounted our 100 μm-thick GaN IMPATT diode in our microstrip cavity circuit and carried out tests under pulsed mode to reduce the thermal stress in the device. We started to capture oscillation with our spectrum analyser when we increased our bias current beyond 4.9 kA cm^{-2}. By varying the biasing current density, we can tune the oscillation frequency from 28.8 GHz to 38.0 GHz. This tuning is a characteristic of IMPATT operation.

Benchmarking the power-frequency performance of our devices among experimentally reported GaN IMPATT oscillators produces encouraging results (see Figure 7(d)). We have recorded the highest oscillation at 38 GHz with an output power of 7 dBm. We attribute this success, involving entry to the Ka-band, to our thinning strategy that reduces series resistance and our tailored oscillation circuitry. It's important to note that our microstrip cavity measurement provides a lower limit for device performance. That's because compared with a waveguide resonate cavity, there is more parasitic loss in the circuit and reduced thermal dissipation in the diodes.

Next steps

During our measurement process, we noticed that when continuously increasing the biasing current density, our devices suffered from overheating and an irreversible breakdown. This poses a challenge, as our theoretical and simulation analysis projects that we need to apply a biasing current density of more than 80 kA cm^{-2} to reach W-band oscillation. Based on these observations, it is clear that we must overcome thermal limitations, in order to realise higher-frequency oscillations with higher output powers.

To take on this task, we are now trying to resolve the reliability issues associated with our flip-chip-style packages. Previously, it has been shown that by flip-chip bonding silicon IMPATT diodes to a diamond heat sink, they can be prevented from burning out under input power densities up to a few MW cm^{-2}. We expect that this state-of-the-art thermal solution



➤ Figure 7. (a) A microstrip cavity circuit and an RF measurement setup. (b) Oscillation frequency versus biasing current density. (c) Peak output power versus oscillation frequency. (d) A benchmark plot of experimentally achieved GaN IMPATT oscillators.

can also aid GaN IMPATT diodes, once they have been optimised.

However, we should keep in mind that our GaN IMPATT diodes will operate under a much higher input power density than those made from silicon at a given frequency. Due to this, cooling demands are far tougher to meet. To do so, we will need to evaluate all the available techniques in our toolbox, to ensure that our GaN IMPATT technology will not be prohibited by self-heating of the device.

It is possible that the development of diamond as a heat-spreading material, as well as the use of a thermally conductive substrate, could provide us with some inspiration. In addition to flip-chip packaging to a diamond heat sink, we will need to consider encapsulating the GaN IMPATT with a diamond heat spreader, and create diamond thermal vias to connect the hot spot to the heat sink. While there is still much work to do, we have already made much progress. Our key milestones include demonstrating the first Ka-band GaN-based IMPATT oscillator, a triumph that is supported by establishing a GaN substrate thinning process.

Our next steps, required to fully realise GaN's promising potential for this technology, will centre on electro-thermal co-design. Success will unlock the door to GaN IMPATT diodes that combine higher frequencies with higher powers.

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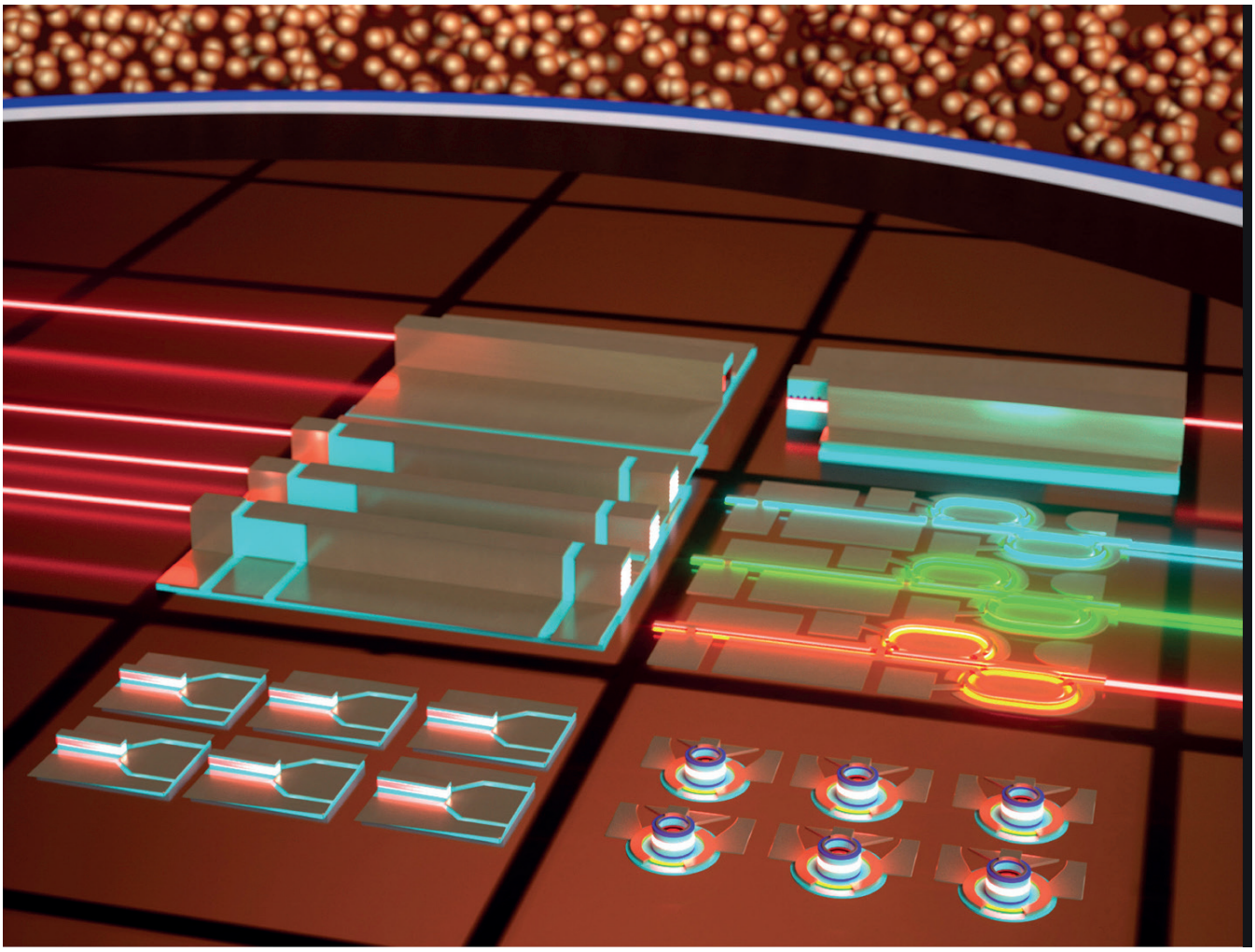


Quantum-dot lasers on silicon

Integrating quantum-dot lasers on silicon photonic chips promises to create high-speed devices for datacom and other applications

BY ARTEM PROKOSHIN AND YATING WAN FROM KING ABDULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

SINCE ITS INVENTION in 1962, the semiconductor laser has played a phenomenal role in changing our world. This source of monochromatic emission is now an essential component in CD and DVD players and recorders, laser printers, barcode readers, and most importantly, fibre-optic communication systems that connect our world through the internet.

Internet traffic continues to climb at an eye-watering pace, with analysts calculating a compound annual growth rate of 25 percent that, in 2022, propelled global traffic to 4.8 zettabytes – that's 4.8 trillion gigabytes. Given this tremendous rise in internet traffic, which shows no sign of abating, it is more important than ever to trim the power consumption of data transmitters and receivers. Efforts that are underway in that regard are not restricted to long-haul optical communications, and are also considering short-distance interconnects in datacentres, which now account for up to 2 percent of global electricity. The target is to drop below 1 picojoule per bit.

Fulfilling this goal will have far-reaching benefits. As well as helping to curb the carbon footprint in the datacom and telecom sectors, energy savings will help where there is a booming interest in the use of photonic chips in neural networks, known as photonic neural networks. With growing popularity of large language models, the cost of training and operating them is increasing. Photonic neural networks, driven by highly efficient semiconductor lasers, offer a promising solution to meeting this growing energy demand.

Helping to turn such dreams into reality by integrating quantum-dot lasers on silicon photonic chips is our team at the King Abdullah University of Science and Technology. By marrying these two technologies, we are uniting incredibly efficient sources with mature, high-volume semiconductor processing techniques.

Why silicon?

Silicon, by far the most widely used semiconductor material since the latter half of the last century, is the backbone of the microelectronics industry. When used to produce integrated photonics, silicon provides the most advanced material platform, developed over the last 20 years and relying heavily on CMOS technology. Merits of the silicon photonics platform include: a high refractive index contrast, leading to low-loss; high-confinement waveguides; and efficient grating couplers.

Drawing on silicon's doping technology, chipmakers can produce high-speed modulators based on *p*-*n* junctions, while this material's compatibility with germanium ensures fast and efficient silicon-germanium photodetectors. What's more, silicon photonics provides the highest manufacturing volume and the lowest cost, thanks to the opportunity to manufacture silicon chips on 300 mm wafers.

Unfortunately, despite all these strengths, silicon is not the perfect choice. Its biggest disadvantage for photonic applications is its indirect bandgap, preventing it from providing an efficient light source. While several silicon-germanium laser diodes have been demonstrated, they are unsuitable for real-world applications, due to their feeble output power and broad linewidth.

The lack of a silicon-based laser has led to the pursuit of two options for producing PICs with this material system. One involves combing silicon photonic chips, as purely passive devices, with an external light source. In this case, the downsides are high coupling losses, typically exceeding 3 dB, and increased packaging complexity. The second option is to integrate efficient lasers based on III-V semiconductors, such as GaAs or InP, directly onto silicon photonic chips. This approach reduces coupling loss to typically below 0.5 dB and simplifies packaging, but leads to constrained production volumes and increased costs.

Why quantum dots?

Since the introduction of the first semiconductor lasers, there have been a number of improvements to their design, along with the development of various different architectures. The first lasers were homojunction diodes, using the same material for the waveguide core material and its surroundings. To improve optical confinement, a breakthrough that ensured the first continuous-wave operation, engineers introduced a double heterostructure, sandwiching the active region between a pair of cladding layers with a wider bandgap and a lower refractive index. For example, this has been realised by surrounding a GaAs active region with AlGaAs. Another important advance followed, with a move to an active region employing a multiple quantum well structure that improves the efficiency of the radiative recombination process.

The next logical step, pursued by many in recent decades, is a move from a multi-quantum-well active region to one based on quantum dots. With this refinement, carrier confinement switches from one lateral direction to all three dimensions. Quantum dots, also referred to as 'zero-dimensional' structures, have dimensions on the order of tens of nanometres. They can be formed with a self-assembly process, involving epitaxial growth of InAs on a lattice-mismatched GaAs substrate.

The father of the quantum dot laser is Yasuhiko Arakawa from the University of Tokyo. In 1982 he proposed this device, claiming it had the potential to provide a lower threshold current and better temperature stability than its quantum-well-based cousins. Thanks to an atom-like structure and a discrete density of states, the quantum-dot laser provides an almost symmetric gain spectrum and a low linewidth enhancement factor, enabling narrow-linewidth and isolator-free operation. Additional opportunities for quantum dots are found in low-dark-current photodetectors and efficient Stark-effect amplitude modulators.

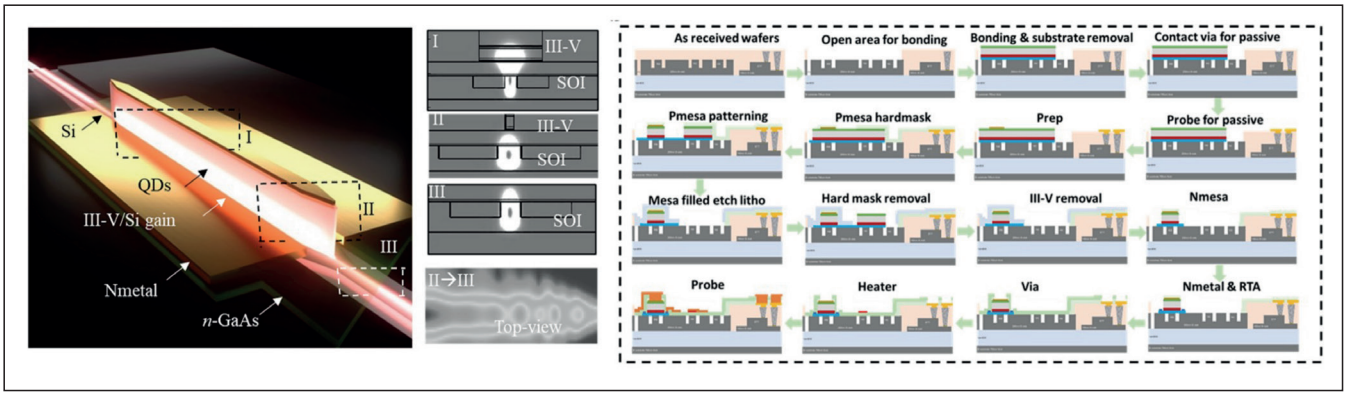
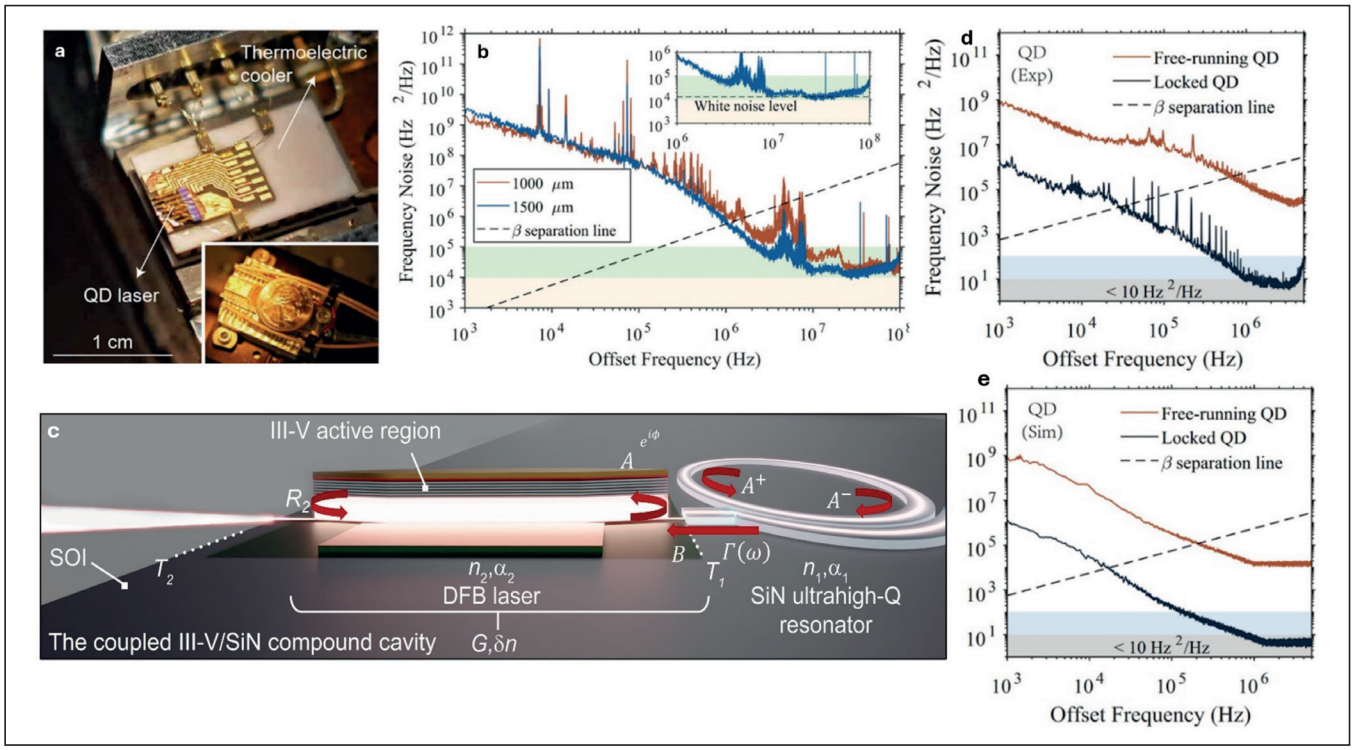


Figure 1. The fabrication process for quantum-dot lasers on silicon.



➤ Figure 2. (a) QD laser mounted in a butterfly package. (b) Frequency noise spectra of QD lasers with a 1 mm and 1.5 mm long cavity. The linewidth in the free-running regime is 41 kHz. (c) Illustration of the coupled compound cavity. (h) and (i) Measured and calculated frequency noise spectra, indicating a fundamental linewidth of 16 Hz.

In the context of integration with silicon, the main advantage of quantum dots is a reduced sensitivity to crystal defects. These nanostructures offer improved in-plane carrier confinement, with diffusion lengths on the order of several microns – that compares with tens of microns in quantum wells, and ensures that dots are highly tolerant to dislocation defects.

The great potential of quantum dots is realised in devices. Measurements of quantum-dot lasers demonstrate that they can operate with a long extrapolated-lifetime at high temperatures, thus relaxing the stringent requirements on temperature control of photonic chips. This class of laser also offers a threshold current of less than 1 mA, making it an ideal candidate for addressing the ever-increasing energy consumption in optical communication networks.

Combining the two

When quantum dot lasers are integrated with silicon photonics, rather than being manufactured on native substrates, both improvements and drawbacks result. Focusing on the positives, there is the integration of quantum-dot active regions with high-quality grating structures and ring resonators to realise single-mode lasing. In addition, there is a lower propagation loss for silicon waveguides compared with III-V materials – this leads to lower threshold currents and a narrower linewidth for integrated lasers with an extended cavity.

Recently, we have directed our efforts at the heterogeneous integration of quantum-dot lasers on silicon via wafer bonding. This has involved the use of silicon-on-insulator substrates with a 500 nm-thick layer of silicon, which provides higher mode overlaps between the silicon and quantum-dot regions compared with the standard, 220 nm-thick silicon photonics platform.

Production of our PICs began with patterning our SOI wafer with three different etching depths: a 500 nm etch for strip waveguides, a 231 nm etch for rib waveguides, and a 20 nm etch for grating structures. Following this patterning process, we bonded our GaAs wafer to the quantum-dot active region, prior to annealing at 100°C and removing the GaAs substrate. GaAs mesas were then patterned to form laser active regions, followed by the deposition of the contact metal layer (see Figure 1 for a step-by-step illustration of the entire fabrication process).

With this approach, light generated in the quantum-dot active region is directed into the silicon waveguides by evanescent coupling. This occurs when two waveguides are close to each other – typically less than the wavelength of the light – a situation that allows light to transfer from one waveguide to another (see Figure 2). To increase coupling efficiency and cut back-reflections, we employ a taper rather than an abrupt transition between the III-V and the silicon waveguide. By terminating the silicon waveguide at the end of the chip with a 7° angled taper, we reduce back-reflection at the facets.

Our lasers achieve single-mode operation with a side-mode suppression ratio of over 60 dB (see Figure 3 (a)) and a threshold current of just 4 mA. The latter corresponds to a threshold current density of 31 A cm^{-2}, which is an order of magnitude lower than that of standard quantum-well lasers.

These directly modulated quantum-dot lasers are attractive candidates for datacentre communications, as they do not require additional modulators based on silicon or lithium niobate. However, due to a finite intraband relaxation time and gain saturation effects, it's a challenge to realise a high modulation bandwidth with quantum-dot lasers, with the 3 dB modulation frequency typically limited to around 10 GHz for devices grown on native substrates. However, thanks to synergistic effects between the silicon cavity and the quantum-dot active region, our heterogeneous quantum-dot device produces a modulation frequency of 13 GHz at an injection current of 31 mA (see Figure 3 (c)) for the corresponding small-signal response).

Another important characteristic for lasers used in optical communications is their linewidth, which indicates the noise level and ultimately limits data transmission capacity. QD lasers have a low linewidth enhancement factor, leading to narrower linewidths than the quantum-well counterparts. Early collaborative efforts have also spotlighted the unique properties of QD lasers in chaos-free operation, achieving a remarkably low 16 Hz Lorentzian linewidth under external-cavity locking with a low-Q cavity – an improvement in frequency noise by an order of magnitude over conventional quantum-well lasers. Standalone, these QD lasers (see Figure 2 (a)) exhibit a 41 kHz linewidth (see Figure 2 (b)). Under external optical feedback, a 35 dB improvement in feedback insensitivity has been achieved, enhancing stability and enabling operation without coherence collapse even with -9.6 dB of feedback. This makes the QD lasers suitable for integration into compact, highly integrated photonic systems without the need for optical isolators.

Looking ahead, there is theoretical potential for an even more dramatic reduction in linewidth – to 1 Hz or less – by employing a high-Q SiN-based micro-ring resonator in conjunction with the self-injection locking technique, as shown in Figure 2 (d) and (e). This prospective development is particularly suited for microwave photonics applications, including microwave synthesisers where stability is paramount.

Outstanding challenges

It is beyond question that quantum-dot lasers on silicon are a promising solution to addressing the growing energy demand in datacentre optical communications. These sources are markedly superior to their quantum-well counterparts in key performance criteria, including threshold current, linewidth and temperature stability. Additional merits of these lasers are a high output power and an exceptional modulation frequency.

Still, there is considerable work to do to make this technology viable and affordable in high-volume production. Efforts must be directed at realising wafer-scale integration on 300 mm substrates to fully exploit the high-volume, low-cost production capabilities of silicon photonics. Other outstanding goals are to integrate quantum-dot lasers with high-speed silicon modulators and photodetectors, and to undertake a systematic study of reliability with high-power testing, to prove that quantum-dot lasers can deliver reliable operation at the elevated temperatures found in data centres. Once these tasks have been accomplished, the next step will be to demonstrate a platform that is best at leveraging the economies-of-scale of silicon while maintaining the highest yield at the lowest lifecycle cost.

The capability of our technology allows its opportunities to stretch beyond datacentres. The realisation of the dense integration of devices with on-chip lasers is an advance that will prove crucial in many of tomorrow's applications, including photonic neural networks, biochemical sensing and quantum computing. The addition of on-chip laser sources enables all-optical signals to be confined within an integrated circuit package, enhancing efficiency, stability, and scalability. This integration is poised to revolutionise many applications, while offering significant performance improvements, environmentally friendly solutions, and the potential for mass production.

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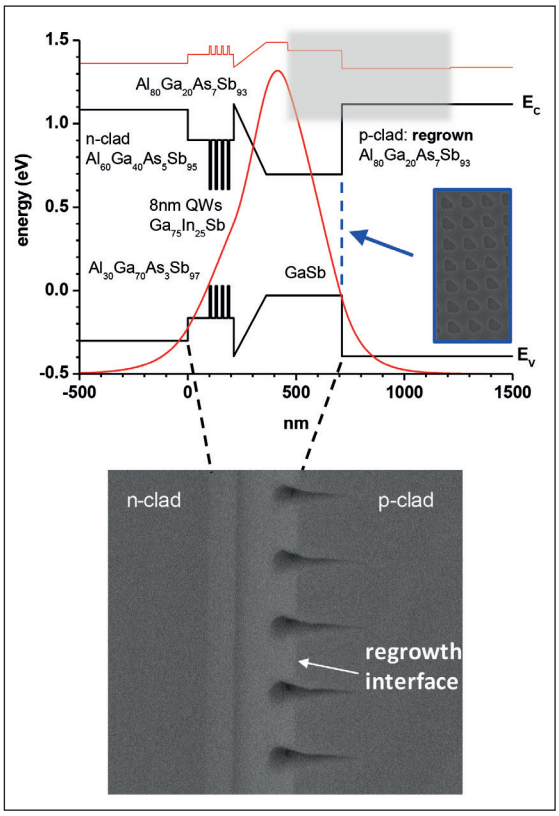
Propelling PCSEL emission to the mid-infrared

Turning to antimonides extends the emission of the PCSEL to the mid-infrared, enabling this source to provide a new class of cost-efficient active optical sensors

BY LEON SHTERENGAS FROM STONY BROOK UNIVERSITY

ONE OF THE KEY STRENGTHS of the photonic crystal surface-emitting laser (PCSEL) is its generation of a high-power beam with ultra-low divergence and a narrow spectral profile. As this goes hand-in-hand with potentially relaxed fabrication and packaging requirements, the PCSEL makes a compelling case for the ultimate format of semiconductor laser in many applications.



➤ Figure 1. Top of the image shows the band diagram under flat band condition and corresponding calculated refractive index profile and intensity distributions of the fundamental mode of the 2 μm PCSEL device. The bottom of the figure shows the cross-section SEM image of the buried high-index-contrast photonic crystal layer of the fully fabricated PCSEL.

The PCSEL's advantage originates from the incorporation of a layer that produces a periodic modulation of the dielectric function. Introducing this photonic crystal layer within the laser's heterostructure transforms its output from that of a multi-mode edge emitter to a single-mode surface emitter. When watt-class output power levels are not required, PCSEL postgrowth fabrication and packaging is virtually identical to that of inexpensive LEDs, opening the door to cost-efficient laser-based sensor systems.

Introducing antimonides

A critical technological step associated with PCSEL development is integration of the photonic crystal layer into the laser's heterostructure. The development of this new class of laser began with some of the more established material systems, such as those based on the arsenides. That's the material system employed by scientists at Kyoto University to pioneer their air-pocket-retaining epitaxial regrowth.

Turning to antimonide-based materials to realise PCSELs emitting in the mid-infrared is challenging, because epitaxial regrowth within the III-V-Sb material system is not that well developed. Breaking new ground on this front is our research group at Stony Brook University, with successes including the realisation of continuous-wave, room-temperature GaSb-based PCSELs emitting near 2 μm in 2023.

While GaSb-based interband semiconductor lasers are not as common as those based on either GaAs, InP or GaN, they are certainly not in their infancy, and can operate in the continuous-wave regime at room temperature over a wide spectral region that spans from below 2 μm to over 5 μm.

Here we discuss devices based on the so-called type-I quantum-well active region. GaSb-based edge emitting diode and cascade diode lasers with this

form of active region operate very well from about 1.9 μm to about 3.3 μm. Note that it is possible to transfer the air-hole retaining regrowth technology that we developed for this class of devices to type-II quantum well interband cascade lasers, which are capable of delivering a strong performance at even longer wavelengths.

We undertake the growth of antimonide-based PCSEL heterostructures using two epitaxial steps. The first, accomplished via MBE, is the growth of an incomplete laser heterostructure that is missing the top cladding layers. The heterostructure that's formed comprises AlGaAsSb *n*-cladding, an active region containing GaInAsSb quantum wells embedded into an AlGaAsSb waveguide core, and a thick GaSb top layer.

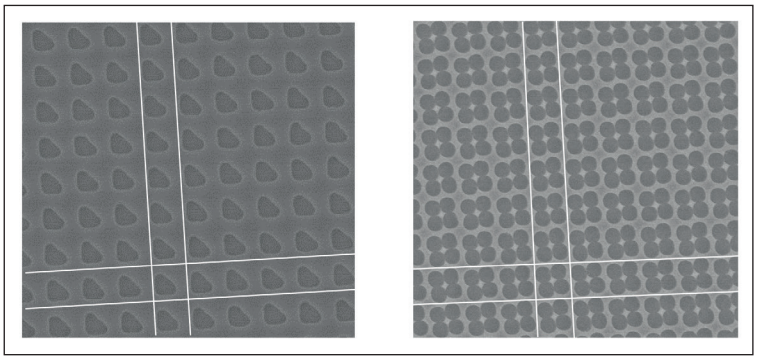
After removing this incomplete laser heterostructure from our MBE reactor, we use electron-beam lithography to form a hard mask for dry etching our photonic-crystal pattern. Inductively coupled plasma-reactive ion etching defines a square lattice of holes in the top GaSb layer.

Our next step begins by preparing the nano-patterned GaSb surface for regrowth. We apply an atomic-hydrogen-assisted surface-preparation process to clean the surface and remove a native oxide in high vacuum without degrading the crystalline quality of the active region. Regrowth of a nanopatterned incomplete laser heterostructure follows, using AlGaAsSb *p*-cladding and *p*-contact layers (see Figure 1 for the band diagram of the regrown diode laser heterostructure as well as calculated refractive index and modal intensity distributions).

Cross-sectional scanning electron microscopy of our regrown wafer containing a buried high-index-contrast photonic crystal layer reveals that a thin layer of AlGaAsSb material covers the etched GaSb surface, even inside the etched holes (see Figure 1). Buried voids are formed, due to self-shadowing of the etched holes from atomic fluxes incoming at the angle to surface normal. Due to this, we are able to integrate a high-index-contrast photonic-crystal layer within a diode laser heterostructure.

Challenges and outlook

So far, we have fabricated antimonide-based diode and cascade diode PCSELs operating at up to 2.8 μm. For the diode PCSELs operating near 2 μm, we have demonstrated devices with a continuous-wave output power of 30 mW. Far higher output powers will follow when we increase the outcoupling efficiency of our mid-infrared PCSELs. This is one of our objectives, along with improving the stability of our PCSEL cavities against excitation of the higher-order spatial modes. Our goal is to develop a mid-infrared PCSEL cavity design that delivers an optimal balance between the coupling of the laser modes to active quantum wells and to the buried photonic-crystal layer.

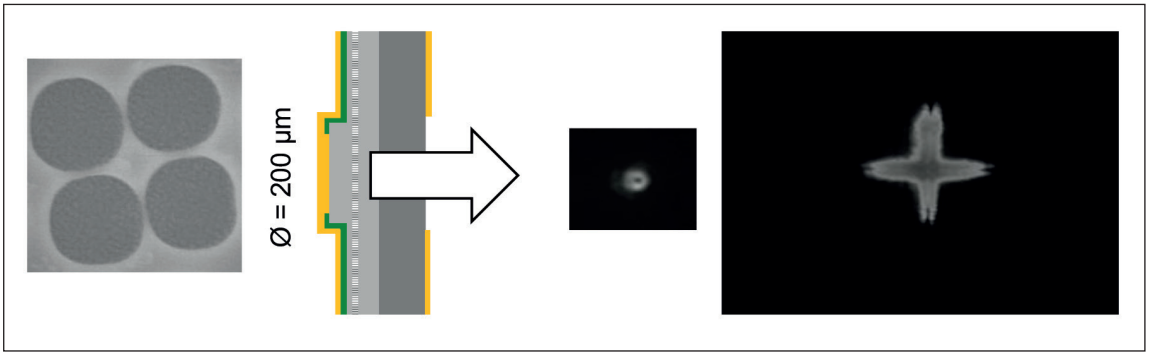


➤ Figure 2. Top views of the hard masks fabricated on SiN layer covering incomplete PCSEL heterostructure. On the left is the mask used to fabricate PCSELs with single void per unit cell, while on the right is the mask used to fabricate four-void per unit cell buried photonic crystal devices. The period of square lattice is 540 nm in both cases.

To increase the operating wavelength of a PCSEL, there needs to be a nearly proportional increase in the period of the buried photonic crystal. Realising this is not easy, as it is challenging to scale up the volume of buried voids, because they are not fully controlled by the lateral size of the etched holes – instead, they are strongly influenced by the regrowth step. If the relative size of the buried voids decreases with respect to period of the photonic crystal – a situation that reduces the void area fill-factor – this can result in an undesired reduction of the interaction strength between the laser mode and the buried photonic-crystal layer. The implications are problematic, such as weaker feedback and lower outcoupling efficiencies.

When increasing the period, turning to several voids per unit cell is an attractive option for ensuring an adequate area fill-factor of the void in the unit cell of the buried photonic crystal. This approach has already been adopted with arsenide-based PCSEL technology, where it has been used to fine-tune the buried photonic crystal spatial optical-mode selectivity and promote a high degree of coherence over large emitting apertures. We intend to explore this opportunity very soon. So far, we have studied designs with multiple voids per unit cell, solely to boost device outcoupling efficiency (see Figure 2).

We have fabricated antimonide-based PCSELs based on a four-hole unit cell that deliver significantly improved efficiencies and somewhat smaller threshold currents. In comparison with sources with a photonic crystal having one air-pocket per unit cell and emitting about 10 mW of power, those with four pockets produce 30 mW.



➤ Figure 3. Top view of the four-void unit cell, schematic of the side view of the PCSEL device and corresponding camera images of the far field patterns measured at 150 mA and 500 mA.

We have fabricated antimonide-based PCSELs with a four-hole unit cell that deliver significantly improved efficiencies and somewhat smaller threshold currents. In comparison with sources with a photonic crystal having one air-pocket per unit cell and emitting about 10 mW of power, those with four pockets produce 30 mW, which is already adequate for many laser sensor applications.

At a current just above the laser threshold, our four-hole PCSELs have a far field pattern that indicates a divergence angle of the order of a degree. This is a promising result, implying coherent operation over the whole 200 µm-diameter emitting aperture. Unfortunately, as the injection current increases, a cross-like shape appears in the far field pattern, as the beam broadens along orthogonal X-directions (see Figure 3). There is also some broadening of the laser emission spectrum, indicating excitation of higher-order lateral modes.

Our body of work highlights the benefits that can be realised with an air-pocket retaining regrowth methodology for antimonide-based PCSELs. We plan to build on this success by optimising the buried photonic crystal parameters of our devices, so that they can deliver stable single-spatial-mode operation and an increased external efficiency. Another objective is to extend the room-temperature continuous-wave operation of our GaSb-based PCSELs to 3 µm and beyond.

The work on III-V-Sb PCSELs at Stony Brook University is supported by US Army Research Office.

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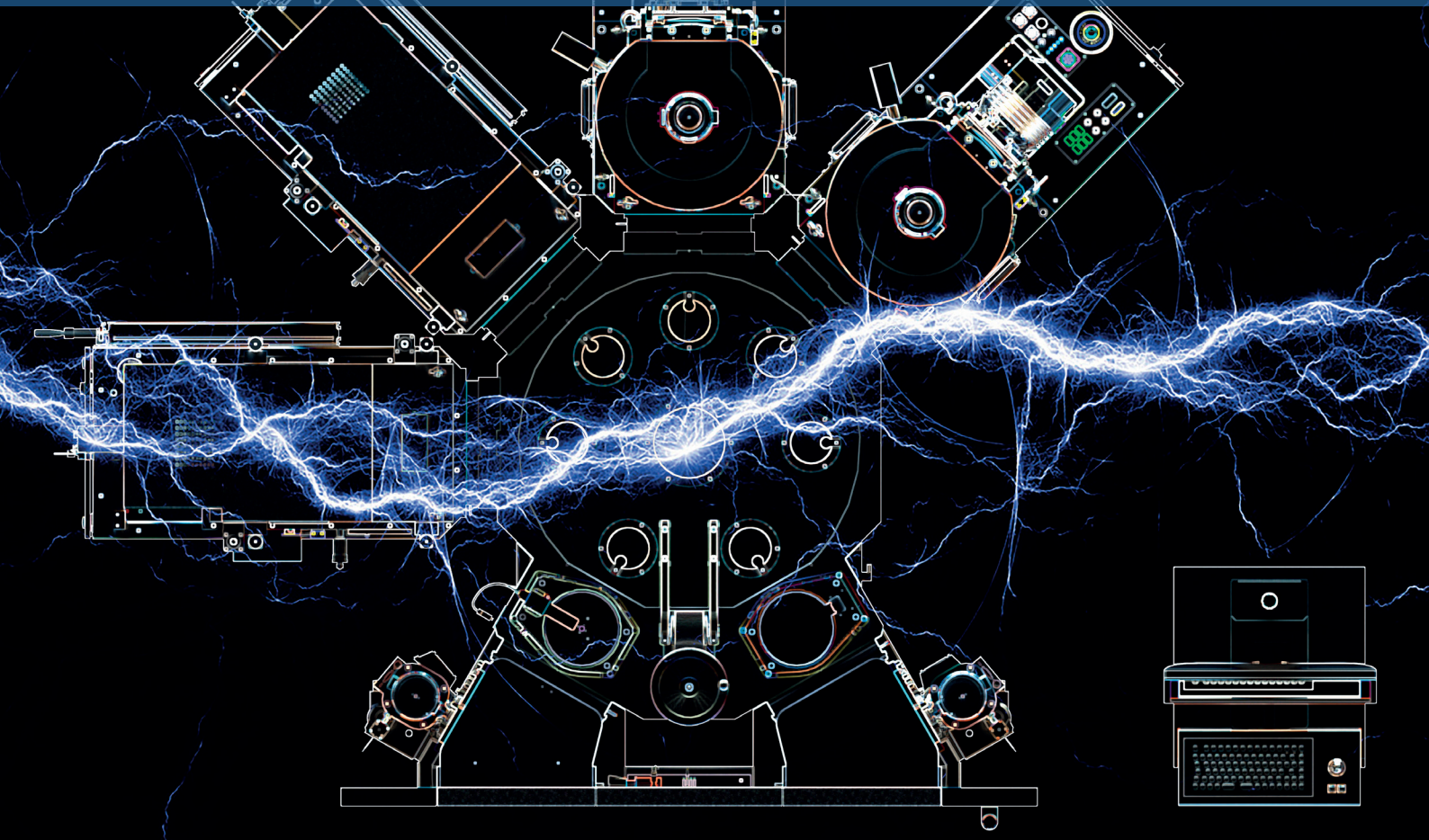

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➤ The iGaN Lab team from the University of Science and Technology of China, led by Haiding Sun and including his PhD student Huabin Yu and members who contributed to this work.

GaN nanowires on a silicon platform eye novel optoelectronics

Nitride nanowires with a large surface-to-volume-ratio offer intriguing optoelectronic properties that could advance integrated photonics

BY HUABIN YU, YUANMIN LUO, WEI CHEN AND HAIDING SUN FROM THE UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

ONE-DIMENSIONAL semiconductor nanostructures, such as single-crystalline nanowires, are the key ingredient in emerging nanoscale optoelectronic devices. These miniature marvels promise to play a variety of roles, including serving in the ultimate form of integrated photonics.

It is possible to produce nanowires with a range of materials. They include the group III-nitrides, which offer direct and tuneable bandgaps. Nanowires made from this material system offer single-crystalline quality, realised through MBE growth that allows for full strain relief during the epitaxial process. Additional merits of nanowires, when produced by MBE, are precise morphology and size control - and thanks to a large surface area, an exceptional light absorption efficiency and light extraction efficiency.

This wonderful set of attributes makes III-nitride nanowires a compelling candidate for a number of optoelectronic devices. These nanoscale structures could play a crucial role in LEDs, photodetectors, laser diodes, and even photoelectrochemical devices for chemical/biological photoelectronic sensors. Exploring all of these possibilities and more is our team from the iGaN Laboratory at the University of Science and Technology of China.

GaN nanowires for LEDs ....

GaN nanowires hold much promise for increasing the efficiency of the LED, thanks to properties that are superior to those of planar structures. One key merit of the GaN nanowire is that it can be grown directly on silicon or another foreign substrate, while offering an internal quantum efficiency that's enhanced through effective lateral stress relaxation during the epitaxial growth process. What's more, this class of nanowire increases *p*-type doping efficiency, due to a reduced activation energy of the magnesium dopant in nanowire structures. There are also the benefits of a large surface-to-volume ratio and multiple scattering effects, assets that facilitate a high light-extraction efficiency.

And on top of all of this, the large surface area of III-V nanowires opens the door to integration with various low-dimensional functional materials, including colloidal quantum dots. This leads to many tantalising prospects surrounding the future of multifunctional integrated photonic chips and optoelectronic systems.

In our iGaN Lab at the University of Science and Technology of China we have developed a broadband nanowire LED that produces emission that spans the UV to the red, via the integration of colloidal quantum dots (see Figure 1(a) for the photoluminescence spectra of bare nanowires, and Figure 1(b) for those coated with quantum dots).

We have investigated the morphology of our bare and coated nanowire arrays with scanning electron microscopy (see Figure 1(c) and (d)). Images indicate that the colloidal quantum dots uniformly reside towards the top of the nanowire array.

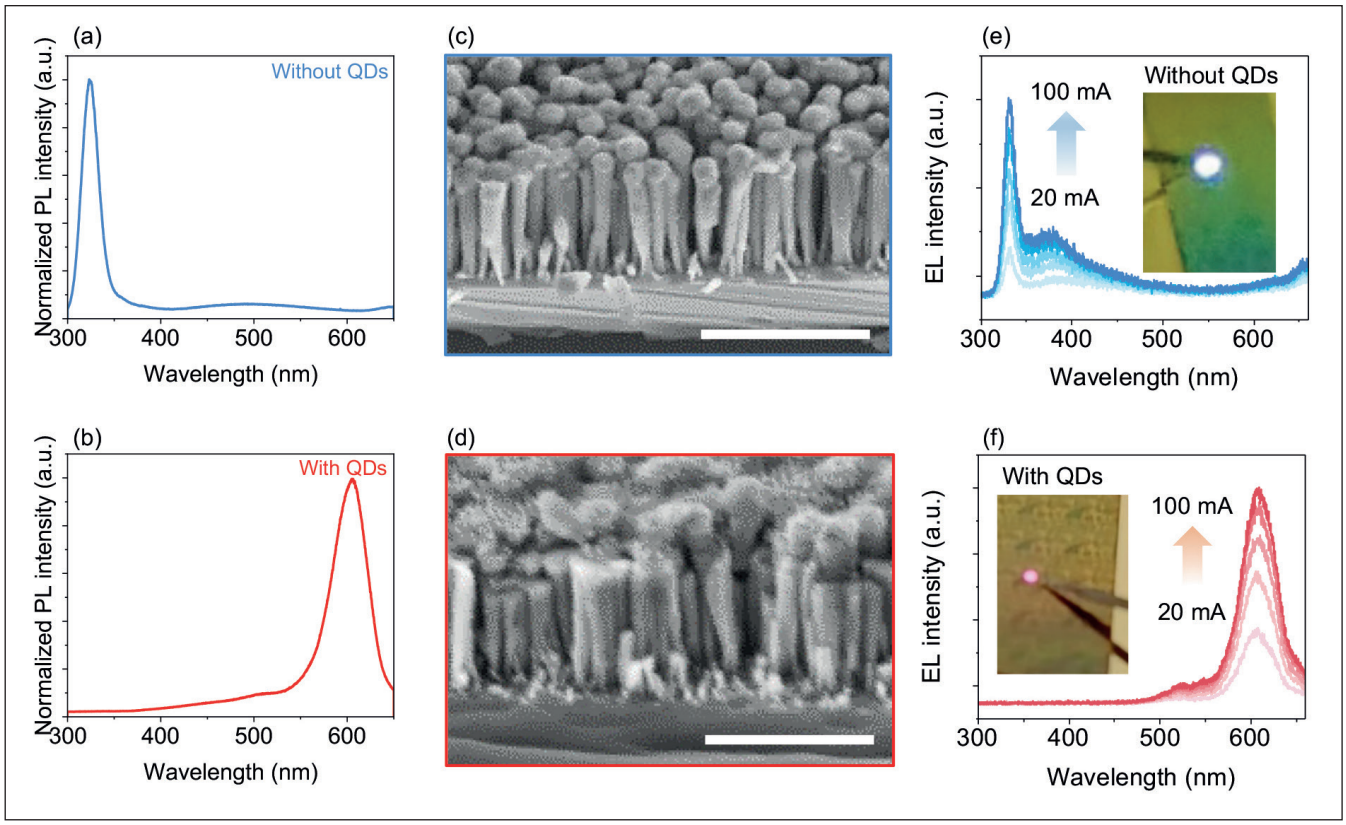
Our work has extended to evaluating our nanowire LEDs under electrical bias. These devices exhibit rectification behaviour and a sharp electroluminescence peak around 325 nm (see Figure 1(e)). The addition of colloidal quantum dots pushes the electroluminescence peak to 600 nm (see Figure 1(f)).

...photodetectors...

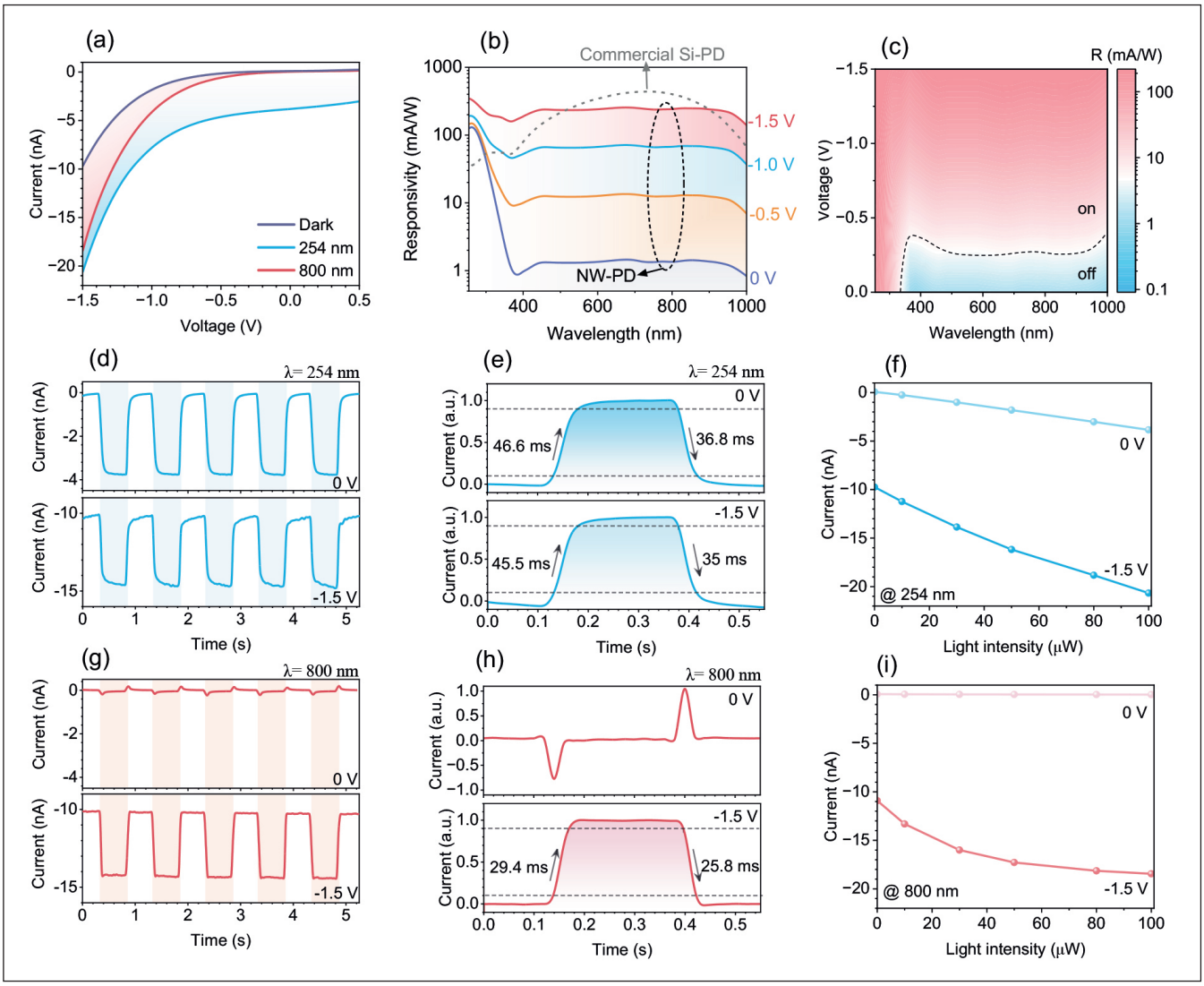
As stated already, GaN nanowires can be grown on various substrates with a near defect-free material quality, thanks to efficient strain relaxation that's associated with the one-dimensional geometry. It's an asset that enables our nanowires to be directly grown on a silicon substrate without a buffer layer, and ensures direct carrier transport between the GaN nanowires and silicon. Due to this, GaN nanowires on silicon sidestep the challenges faced when trying to realise the monolithic integration of III-V semiconductors with silicon photonic systems.

Drawing on this favourable situation, we have developed an integrated tuneable broadband light-detecting device that employs III-V nanowire/silicon heterostructures. Our design demonstrates a bias-controlled switchable operation mode, and enables extreme broadband photodetection as well as self-powered narrowband photodetection.

When we operate our device under zero or negative bias, our photodetector can realise a built-in electric field from the *n*-region to the *p*-region, or utilise an external electrical field from the bias. Photocarriers that are generated under optical excitation are driven by these electrical fields, causing electrons and holes to move in opposing directions. It is this



➤ Figure 1. The Photoluminescence spectra of (a) the pristine nanowires and (b) nanowires coated with quantum dots. The scanning electron microscopy image of GaN/AlGaN nanowires on a silicon substrate (c) without a coating of quantum dots and (d) with a coating of quantum dots. The scale bar is 1 μm. The electroluminescence spectra of the nanowire device (e) without quantum dots, (f) and with quantum dots under injection currents of 20 mA to 100 mA. Insets of (e) and (f) show optical images when the devices are emitting light.



➤ Figure 2. (a) The current-voltage (I-V) characteristics, (b) the responsivity as a function of wavelength, and (c) the colour contour plot of the spectral response matrix of broadband photodiodes. Incident light intensities of the deep-UV and near-IR light are 100 μW. Photocurrent responses of the photodiodes operating at (d) under 254 nm light, and (g) under 800 nm light. Representation of response time and decay time interval of the broadband photodiodes under (e) 254 nm and (h) 800 nm light. The incident light intensity is 100 μW. Photocurrent of the devices under (f) 254 nm light and (i) 800 nm light with various light intensities from 10 μW to 100 μW.

mechanism that enables the device to function in photo-detection mode (see Figure 2 (a)).

Note that our device demonstrates a broad response under reverse bias, transitioning to narrowband photodetection in the deep-UV under zero bias, where the off-rejection ratio ($R_{254\ nm}/R_{800\ nm}$) is very high, exceeding 10^6. We have also recorded bias-dependent spectral response curves (see Figure 2 (b)) and the matrix (Figure 2 (c)), results that further validate the ability of our photodetector to switch between broadband and narrowband operation.

We are encouraged by the competitive responsivity of our devices. This is evident in the UV region, where they are comparable to commercial broadband silicon photodiodes, such as the Thorlabs PDA10A2. According to square-wave photo-responses, our device demonstrates a rapid response under deep-UV/near-IR illumination (see Figures 2 (d) and 2 (g)). The response speed, evaluated in terms of the rise time, is 45.5 ms and 29.4 ms for illumination under deep-UV and near-IR light, respectively. The primary reason for the more rapid response at a longer wavelength is the narrower active region (intrinsic layer) between AlGaN and silicon, in comparison with the AlGaN multi-quantum-well region. However, there is a price to pay for this advantage, with the relatively thin active region of AlGaN/silicon leading to lower responsivity, and resulting in a saturated photocurrent under a high near-IR light intensity (see Figures 3 (f) and 3 (i)). Care is needed when considering this trade-off between the responsivity and the response speed, with the decision

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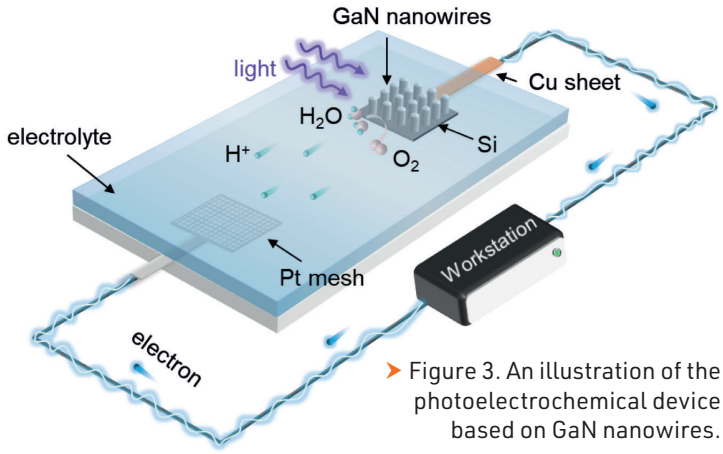

Figure 3. An illustration of the photoelectrochemical device based on GaN nanowires.

needing to take into account the total area for light absorption and response characteristics.

...and photoelectrochemical devices

As well as traditional optoelectronic devices, already described, we are able to produce novel, high-efficiency, photoelectrochemical devices (see Figure 3). One of the reasons that this opportunity arises is because we can tune the optical and electrical properties of our GaN nanowires, due to their physically confined structures and large exposed surfaces. What's also crucial is that these nanowires exhibit environmentally sensitive surface properties, enabling the operation of photoelectrodes in specific aqueous environments.

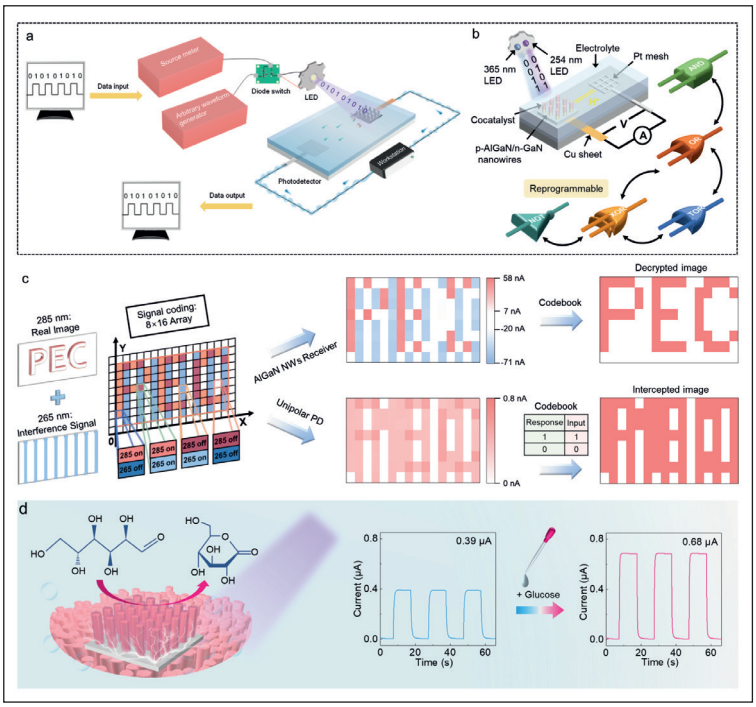

Figure 4. (a) A diagram of the photoelectrochemical photodetector optical communication system. (b) Demonstration of reprogrammable binary and ternary optoelectronic logic gates based on a photoelectrochemical photodetector. (c) Demonstration of an encrypted optical communication system. (d) The mechanism for a photoelectrochemical glucose sensor.

Our photoelectrochemical devices employ a GaN nanowire array as the working electrode, and a platinum mesh as the counter electrode. When operated in electrolytes and illuminated by deep-UV photons, electrons and holes are excited in the working electrode, the GaN nanowires. Driven by the downward band-bending at the interface between the GaN nanowires and the electrolyte, the photo-generated electrons drift to this interface, to undergo the following redox reactions in the electrolyte: $4H^+ + 4e^- = 2H_2$. Another consequence of the band bending is that it induces the directional transfer of holes in the opposite direction, towards the platinum counter electrode, through the external circuit. In this case, the reaction is $2H_2O + 4h^+ = O_2 + 4H^+$. The H^+ ions that are created diffuse through the electrolyte to reach the counter electrode and form the whole circuit. During operation, the device's photocurrent is read out by the electrochemical workstation.

The success that we have had is noteworthy, given that photoelectrochemical devices, which have unique working principles that combine semiconductor physics with a chemical reaction process, are attracting extensive interest by combining simple fabrication with low cost, self-powering and appealing electrolyte-assisted device properties. Thanks to their electrolyte-assisted operating characteristics, as well as following the conventional carrier-generation, separation, and migration processes in semiconductors, these photoelectrochemical devices have a procedure that involves a redox reaction at the semiconductor/electrolyte interface – this equips us with more freedom to regulate the photo-response behaviour.

Due to this promise, our iGaN Lab has unleashed the potential of GaN nanowire-based photoelectrochemical devices in a number of fields, including underwater optical communication, optoelectronic logic, artificial vision, automatic imaging, energy-conversion catalysis, and biosensors (this is illustrated in Figures 4 (a-d)).

Investigating opportunities

To explore the potential applications of our newly developed devices, we have integrated them in a diverse range of optoelectronic systems. We began by building an imaging system for broadband image recognition and classification (see Figure 5 (a)). This features a range of LEDs emitting at different wavelengths as the light source, and a mask displaying the seal character 'USTC' positioned between the light source and the broadband nanowire photodetector. In this system, the bottom broadband nanowire photodetector records light signals as the mask undergoes scanning in both horizontal directions.

By recording photocurrent data at different biases at each mapping position, we have generated a spatial response data cube for image recognition and classification. When we operate the device

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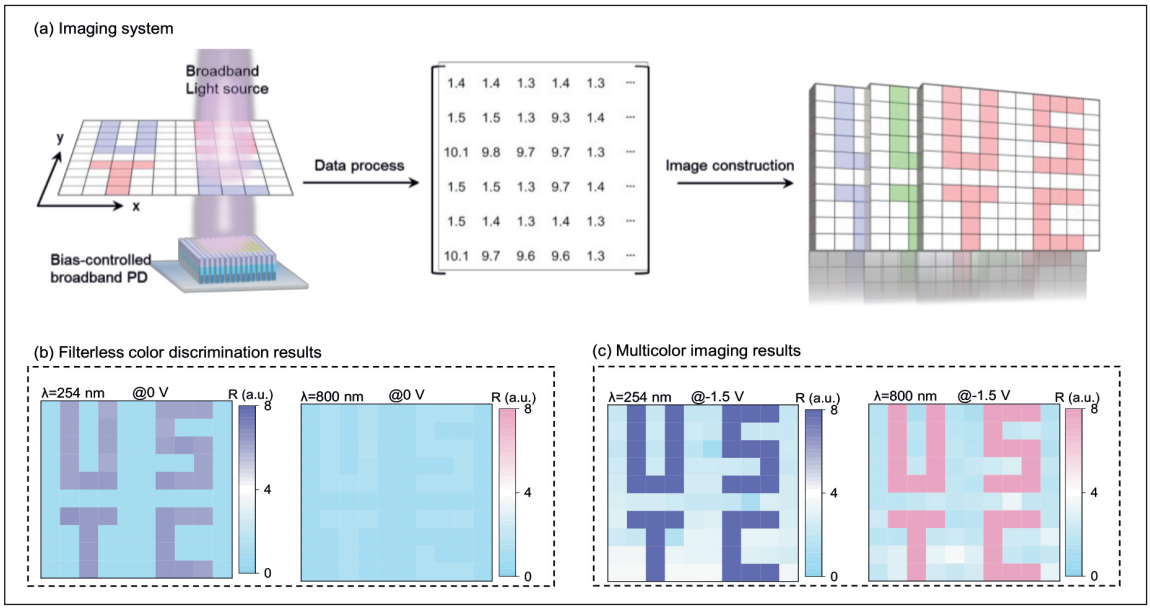


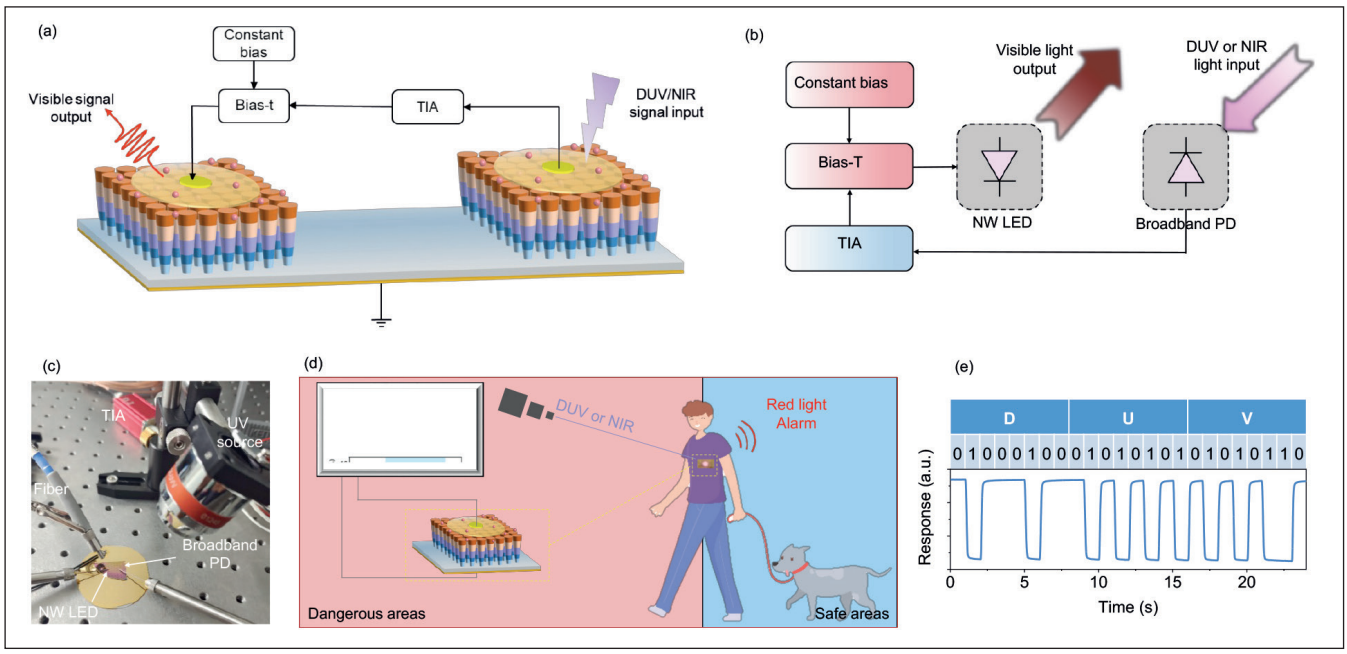
➤ Figure 5. (a) The imaging system setup. (b) A filterless colour discrimination system. (c) Broadband multi-colour system.

in a narrowband mode by applying a 0 V bias, we obtain a blurred pattern with 800 nm light. However, when we turn to 254 nm light, this ensures a distinguishable illuminated pattern (see Figure 5 (b)).

Switching to a broadband mode, realised by applying a negative bias, enables our system to deliver multi-colour imaging. Under this condition, there are discernible patterns of the 'USTC' seal character with deep-UV (254 nm) and near-IR (800 nm) light sources (see Figure 5 (c)), showcasing our device's capability for image recognition and classification across both the deep-UV and near-IR spectral domains.

Following on from the successful merger of two nanowire devices on a single silicon platform, we created a versatile deep-UV/near-IR visualisation system. Here one device acts as a broadband photodetector and the other as a visible emitter (see Figure 6 (a-c) for the system's schematics, circuit diagrams, and photographs, respectively).

To demonstrate the functionality of this system, we employ a visible-blind signal source by pairing a commercial LED with a UV lens. In this configuration, the light intensity of the LED serves as an analogue input signal. When the broadband nanowire device detects UV or near-IR light a corresponding photocurrent results. These signals are simultaneously converted and amplified with a



➤ Figure 6. (a) 3D schematic, (b) circuit diagrams, and (c) photograph of the setup for the on-chip deep-UV/near-IR visualisation systems. The photocurrent of the broadband photodetector (PD) is converted to voltage with a trans-impedance amplifier (TIA). (d) Demonstration of the deep-UV/near-IR visualisation systems for early warning systems. (e) The information of the encoded visible light signals when the system is operating to detect deep-UV signals.

trans-impedance amplifier, with the amplified voltage signals modulating a visible emitter with a consistent bias. The emitted visible light is collected and recorded by a spectrometer system, using a fibre.

The output that results from using UV light as the input signal (see Figure 6 (e)) demonstrates that this integrated system can function as an early warning system. For example, a red alarm light signal can highlight that someone has entered a dangerous area, while using an invisible light signal to prevent potential injury (see Figure 6 (d)). By successfully integrating nanowire devices in a UV/near-IR visualisation system, we are showcasing its potential for multifunctional applications in smart optoelectronic systems.

Our vertically integrated III-V nanowire architectures on the silicon platform holds great promise for future monolithic integrated multi-component photonic systems with simpler, cheaper hardware. So far, we have demonstrated a bias-controlled, multifunctional broadband emitting-detecting device that seamlessly integrates III-V *p-n* nanowires onto a silicon platform. This novel device offers remarkable functionalities, including tuneable detection and emission across a wide spectral range, spanning the deep-UV to the near-IR. This progress creates monolithically integrated multi-component photonic systems that feature reduced hardware complexity and cost.

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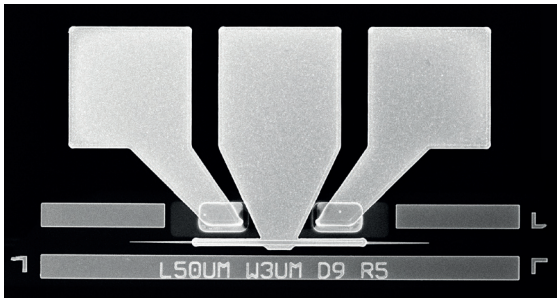
Printing high-speed modulators on SOI

Micro-transfer printing promises to provides a low-cost, high throughput process for uniting InP-based electro-absorption modulators with silicon-based photonic integrated circuits

A TEAM from the Tyndall National Institute, Ireland, is claiming to have provided the first demonstration of a micro-transfer printed electro-absorption modulator.

Their InP-based modulator, mounted to a silicon-on-insulator platform, is said to be suitable for applications in high-speed communication and sensing.

Both of the two leading forms of modulator – those based on a Mach-Zehnder interferometer and electro-absorption – combine a high bandwidth with a large extinction ratio, a low power consumption and a low operating voltage. However, the electro-absorption modulator has the key advantage of a very compact footprint.



➤ A top view of the electro-absorption modulator, micro-transfer printed to an SOI wafer.

For photonic integrated circuits, the predominant platform, in terms of materials, is silicon-on-insulator (SOI). Its merits include a high refractive-index-contrast that aids waveguiding, and the opportunity to employ mature, high-volume, high-yield, low-cost production processes. However, the indirect bandgap of SOI leads to a relative weak carrier-induced refractive index change, so it is better to produce modulators from III-Vs, such as InP.

Previous efforts by other teams have employed wafer bonding to unite InP-based modulators with SOI. However, the team from Tyndall claims that there are several advantages of replacing wafer bonding with pick-and-place techniques, such as micro-transfer printing, for uniting InP-based modulators and photonic integrated circuits based on SOI. Benefits include a potential increase in throughout, realising lower production costs through utilisation of all the devices on the source wafer, and opportunities to reuse the InP substrate and co-integrate materials through back-end-of-line processing.

The researchers have demonstrated the capability of their micro-transfer printing technology for optoelectronic circuits by transferring structures with an 80 μm by 500 μm footprint, featuring a waveguide ranging from 220 μm to 300 μm, to a 220 nm SOI waveguide circuit.

To enable the transfer of the modulator, they grow this structure, featuring a thin *n*-type cladding to ensure efficient coupling to the SOI waveguide, on top of InGaAs and AlInAs release layers.

Additional features of the epitaxial stack used for fabricating the electro-absorption modulator include: a small junction capacitance, to support high-speed operation; graded confinement on the *p*-side to enhance hole transport; and a thick confinement layer of AlInGaAs on the *n*-side to compensate for electron and hole transit times.

Evanescent coupling between the modulator and waveguides is realised by directly printing part-fabricated modulators on top of SOI waveguides. Tapers, increased up to 1 μm to ease the alignment placement tolerance, couple a fundamental mode from the SOI circuit to the modulator.

Production of the electro-absorption modulator from the printed coupon involves five lithographic levels, with the ridge waveguide defined using electron-beam lithography.

To assess the performance of the modulators, the team coupled light into the SOI circuit using cleaved single-mode fibres and a tuneable laser source. Measurements reveal an extinction ratio of 30 dB at 1550 nm, an electrical bandwidth of up to 40 GHz, and open-eye diagrams of up to 50 Gbit/s, using a back-to-back measurement.

“50 Gbit/s doesn’t beat any records for data transmission rates of optical modulators,” admits corresponding author Owen Moynihan. However, he argues that with the introduction of travelling-wave electrical contacts and a move to arrays of modulators, it is possible to realise far higher data rates. He points out that with this approach, there are already reports of 250 Gbit/s arrays.

Adopting this approach is one of the next goals for the team. “But more importantly, we will focus on the integration of multiple transfer printed devices, such as a laser, modulator and detector on the same chip,” says Moynihan.

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Boosting the performance of AlN-on-AlN Schottky barrier diodes

AlN Schottky barrier diodes with a lateral geometry combine a high blocking voltage with a low ideality factor

ENGINEERS AT Arizona State University are claiming to have delivered a significant breakthrough in the performance of AlN Schottky barrier diodes.

"Our work is the first demonstration that simultaneously achieves an ultra-low ideality factor and a high breakdown voltage for AlN diodes," remarks team spokesman Houqiang Fu.

One of these metrics, the ideality factor, is used to evaluate the quality of a diode, with better devices having lower values. For diodes made from many materials, ideality factors typically range from 1 to 2, but for those made from AlN much higher values have been reported, due to defect-induced current transport mechanisms in the AlN epilayers. Researchers have recorded values for AlN Schottky barrier diodes that range from 5 to 12.

"[Our] work presents an ultra-low ideality factor of 1.65, combined with a high breakdown voltage of 640 volt," says Fu, adding that while an even lower value of 1.5 has been reported by another group, that's for a device with a much lower breakdown voltage.

Fu says that realising AlN Schottky barrier diodes with ideality factors close to one is challenging, due to the relatively low maturity of AlN epilayer growth and subsequent fabrication processes, and the difficulty in forming good ohmic and Schottky contacts.

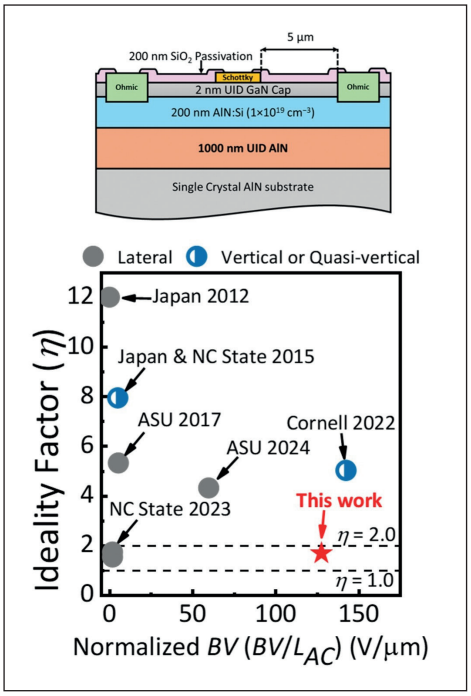
The team's success comes from addressing all these issues. "Growth of AlN epilayers on AlN substrates is crucial for developing high-quality layers with low defect and dislocation densities," argues Fu, who adds: "The device design, particularly the anode-to-cathode distance, is critical for optimising thermionic emission current."

Device fabrication began by loading AlN substrates with a dislocation density of around 10^3 cm^{-2} in an MOCVD reactor and depositing, at 1250°C, a 1 μm-thick AlN buffer, followed by a 200 nm-thick AlN layer that's heavily doped with silicon and an unintentionally doped 2 nm-thick caping layer.

According to atomic force microscopy and high-resolution X-ray diffraction measurements, the epiwafer has a smooth surface morphology, with a root-mean-square roughness of just 0.4 nm, and a full-width at half-maximum of just 17 arcseconds for the (0002) rocking curve.

Based on the latter result, the team claims that switching the substrate from sapphire to single-crystal AlN slashes the defect density in the epilayers by over three orders of magnitude.

Schottky barrier diodes were fabricated using conventional optical lithography and lift-off processes, with circular ohmic contacts with a 100 μm diameter formed from a Ti/Al/Ni/Au stack, and Schottky contacts of the same size produced by electron-beam evaporation of a Ni/Au stack. These diodes, with a cathode-to-anode distance of 5 μm, were passivated by plasma-enhanced CVD of a 200 nm-thick layer of SiO_2, and had contact vias opened by reactive ion etching.



➤ AlN Schottky barrier diodes fabricated at Arizona State University break new ground in terms of the combination of blocking voltage and ideality factor.

Electrical measurements on these diodes revealed that increasing their temperature from ambient to 573K produces a fall in ideality factor from 1.65 to 1.23, an increase in Schottky barrier height from 1.94 eV to 2.41 eV, and a hike in on-off ratio from 10^7 to 10^9.

Destructive breakdown of these diodes at 640 V is primarily caused by crowding of the electric field under the anode edge.

Fu reveals that the next step will be the development of AlN Schottky barrier diodes with near-unity ideality factors and multi-kilovolt breakdown voltages, realised through the introduction of field plates and effective passivation techniques.

REFERENCE
➤ D. H. Mudiyanselage *et al.* Appl. Phys. Express **17** 074001 (2024)

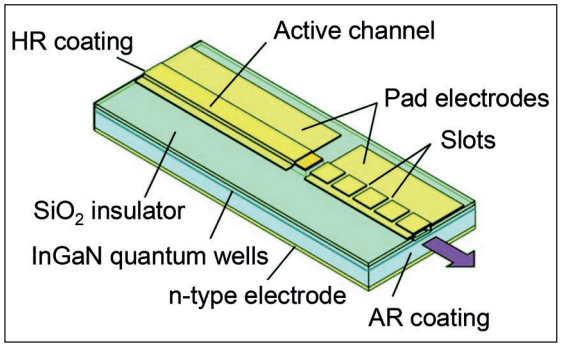
Realising tuneable InGaN laser diodes

Single-mode InGaN lasers with a periodically slotted structure provide a promising source for delivering far-UV light via second harmonic generation

RESEARCHERS from Osaka University are claiming to have produced tuneable in-plane single-mode lasers based on InGaN.

The team say that their devices could be a key component in far-UV sources that employ second-harmonic generation to deliver emission between 210 nm and 230 nm.

Recently, emission in this short-wavelength spectral domain has attracted much attention for providing viral activation and bacterial disinfection without the threat of harm to the human body. Realising compact sources in this region of the far-UV is currently impractical with LEDs and laser diodes, making wavelength conversion an attractive alternative. This can be realised by pumping a SrB_4O_7 nonlinear crystal with a laser that emits at around 405 nm and has a wavelength that can be precisely tuned to ensure optimal second harmonic generation.



➤ The slotted single-mode InGaN lasers produced by Osaka University having a tuning range of just over 0.5 nm.

The engineers from Osaka are fulfilling this requirement with a novel laser architecture that features a slotted design and can be produced using simple processes. Slotted single-mode lasers are not new, but previous variants have only produced emission in the near infra-red.

Tunable lasing at around 405 nm is realised with an InGaN device featuring a narrow-ridge active channel and a periodically slotted structure that acts as a very high-order surface distributed-Bragg-reflector grating.

With this design, injecting current into the slotted channel allows a tuning of the wavelength, resulting from a Bragg wavelength change associated with a rise in temperature. As the slotted channel behaves like a semiconductor optical amplifier, the laser output is obtained from the slotted channel side. A high-reflection coating is applied to the back facet to trim the threshold current and increase output power, and an anti-reflection coating is added to the front facet to prevent spurious lasing.

To produce their tuneable laser, the team employed a 30 kV electron-beam writing system to define 2 μm-wide stripe resist patterns for the 750 μm-long active channels and the 250 μm-long slotted channels in an epiwafer featuring InGaN multi-quantum wells. Ni/Au *p*-electrodes and SiO_2 masks with a thin chromium adhesive layer were added by an evaporation and lift-off process.

The next step involved the removal of the *p*-contact and upper cladding lasers outside the SiO_2 masks by inductively coupled plasma-reactive ion etching. Anisotropic wet etching followed, to obtain smooth and vertical *m*-plane sidewalls in the slots.

To complete the fabrication of the lasers, the team began by: adding a SiO_2 insulator layer by plasm-enhanced CVD; exposing a negative photoresist to remove only the resist on the *p*-electrodes, before etching away the SiO_2 insulator layer and remaining SiO_2 mask on the *p*-electrodes; annealing the chip; and adding *p*- and *n*-type electrodes.

Cleaving created both the end facets, with lengths for the active and slotted channels of 700 μm and 200 μm, respectively. The engineers coated the front facet with an Al_2O_3 anti-reflection coating and the back facet with a Al_2O_3/Ag/Au high-reflectivity coating, before mounting the lasers by conductive epoxy on copper heatsinks.

Evaluation of the continuous-wave performance at 15°C determined a threshold current density of 5.3 kA cm^{-2} and a maximum output power of 2.6 mW. When applying 75 mA to the active region and no current to the slot section, lasing occurred at 404.28 nm with a full-width at half maximum below 0.02 nm, the resolution of the optical spectrum analyser. Increasing the current in the slot to 40 mA red-shifted the emission, providing a tuning range of 0.55 nm.

Due to insufficient measurement resolution, the team were unable to provide a precise figure for their tuneable laser's side-mode suppression ratio. However, they say that their devices deliver single-mode operation with a side-mode suppression ratio of more than 10 dB over the entire tuning range.

REFERENCE
➤ T. Kusui *et al*. Appl. Phys. Express **17** 082003 (2024)

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