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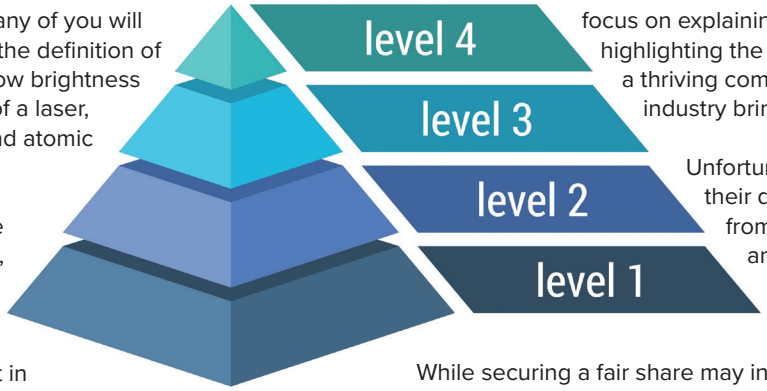
VIEWPOINT

BY RICHARD STEVENSON
EDITOR

The right level

ONE of my tasks as the editor of this publication is to ensure it's at the right level for its readership. I don't want to explains things to you that you already know, or go too far in the opposite direction, assuming content that is only well-known to those that are specialists in lasers, RF devices or power electronics. So, I assume you all will know what a substrate is, will have some familiarity with what MBE and MOCVD are, and don't need explanations for what LEDs and solar cells are – but on the other hand, I think that many of you will appreciate a reminder of the definition of Baliga's figure-of-merit, how brightness is defined in the context of a laser, and the mechanism behind atomic layer deposition.



While I grapple with these decisions on a daily basis, I'm sure this situation is not that unfamiliar to many of you, who will have devoted much effort in working out how to pitch your message at the level that's right level for your audience. If you are delivering a short presentation at an industrial conference, you'll want to avoid covering what's already familiar and focus on what's new, an objective that might be helped by having a speaking slot that goes after others that have already laid the foundations.

The dangers of working in an incredibly high-tech industry is that when you speak to those outside it, as well as possibly assuming too much knowledge on their part, you might also fall into the trap of trying to fill the gaps in their understanding. The reality is that there are those out there that are not fascinated by compound semiconductors, and you don't have to address this by explaining the need for lattice matching, why MOCVD has a higher throughput than MBE, and why bandgaps matter when it comes to power electronics.

Expounding on this topic in this issue is Howard Rupprecht, Managing Director of CSconnected (see p. 18). He explains that when discussing matters with non-industrial stakeholders, which could include a wide range of government officials, it's best to avoid technicalities. Instead, one should focus on explaining industry dynamics, and highlighting the economic benefits that a thriving compound semiconductor industry brings.

Unfortunately, dignitaries spend their days conversing with leaders from many different industries, and to avoid accusations of favouritism, they tend to favour spreading pots over many initiatives. While securing a fair share may initially appear a noble aim, funding that's spread thinly over many projects can fail to make an impact. And there's a strong case to be made that our industry should get a bigger slice of the pie.

In the south Wales cluster, they have a great case for receiving an above-average award. As well as a gross value-added contribution is three times the national average, since 2020 employment within the cluster has grown by 32 percent and total annual revenue has netted £500 million, with more than 90 percent involving purchases from overseas.

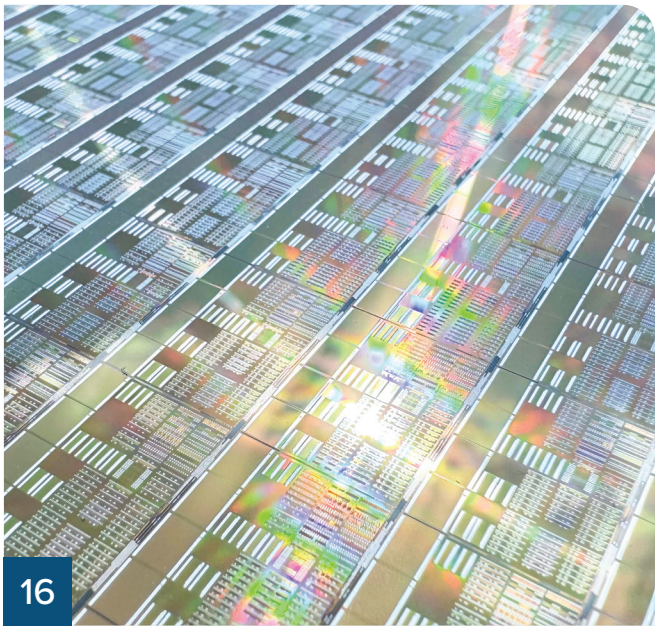
These are hard-hitting figures that are ideal to use when communicating in a clear and compelling manner with government officials and other stakeholders.

CS COMPOUND SEMICONDUCTOR

COVER STORY

Agnitron: Driving ultra-wide-bandgap breakthroughs

Advancing the capabilities of AlN, AlScN and aluminium-rich AlGaN is the Agnitron Agilis 100 MOCVD reactor



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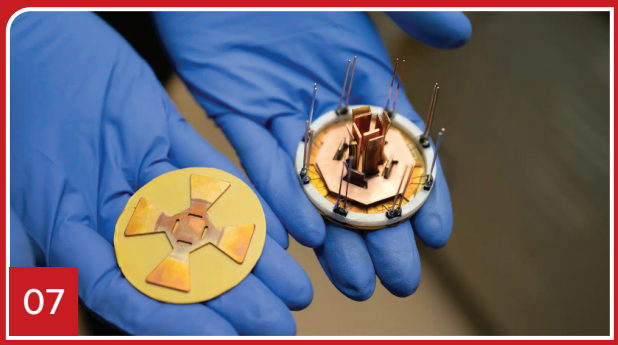

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Is Nvidia defining the future of power electronics?

Riding the AI boom, Nvidia is creating huge momentum for GaN in its 800 V data centre power infrastructure, says Yole Group

A RECENT article by Junko Yoshida for the Yole Group describes how Nvidia, a company that doesn't design or make power devices, is defining the features and functions of tomorrow's power electronics in moving to a 800 V high-voltage direct current (HVDC) data centre power infrastructure.

Yoshida's article describes the company as creating momentum behind GaN as like a 'Tesla moment for SiC'. And just as STMicroelectronics reaped the fruits of Tesla's early push for SiC, 'Infineon and Navitas are jockeying to profit from the emerging GaN moment driven by Nvidia'.

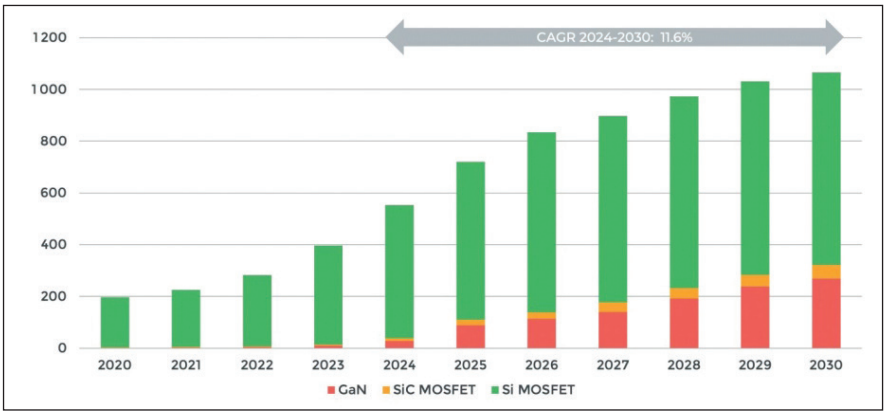
Many suppliers of wide wandgap semiconductors and silicon vendors are playing along, willing to invest in new technologies to deliver what Nvidia needs, writes Yoshida.

In the piece, Gerald Deboy, head of the System Innovation Group at Infineon Technologies, compared Nvidia to a maestro, orchestrating 'the entire world to architect a new way of building and operating data centres.'

Those enlisted by Nvidia include Infineon, MPS, Navitas, Rohm, STMicroelectronics, and Texas Instruments. Also in the mix are suppliers of power system components such as Delta, Flex Power, Lead Wealth, LiteOn, Megmee, and companies who build data centre systems, including Eaton, Schneider Electric and Vertiv.

A range of new power devices and semiconductors will be needed for the new HVDC data centre architecture.

According to Infineon's Deboy, for data centre power infrastructure that needs high-power, high-voltage solutions, SiC leads. But for conversion from 800 V to 50 V, space restraints dictate high-switching frequency. This makes it more of a GaN domain.



800 V AI data centres also demand new semiconductor-based relays, explained Deboy. In data centres today, AC is distributed in three phases, with a normal relay and a normal switch turning power on and off like a light switch. In contrast, in a new high-voltage DC AI data centre, Deboy said that safety requires 'new semiconductor components that control over currents and inrush currents in a very well-maintained behaviour.'

Taken all together, Poshun Chiu, principal technology and market analyst at Yole Group tabbed Infineon as 'by far the leader in power electronics.' When AI data centres ask for a hybrid power electronics solution, noted Chiu, Infineon's strength shines in all three fields, ranging from SiC to GaN and silicon semiconductors. Infineon, added Chiu, covers every phase of the power chain in AI data centres, striving to offer the best technology fit for each stage.

Infineon, however, isn't alone in racing to capture Nvidia-driven AI data centre opportunities. Gene Sheridan, CEO of Navitas Semiconductor notes in the article, 'As you get closer to the processor, Nvidia gets more hands on.' Starting at 48 V, Nvidia is driving design, component selection and supplier selection, he said.

Navitas is taking advantage of its strength in GaN to address power electronics solutions required by AI data centres. The acquisition of GeneSiC Semiconductor in 2022 has also helped Navitas bolster its wideband gap portfolio.

Beyond GaN or SiC, useful for traditional AC to DC converters, or 800 V DC-to-DC converters, Navitas also dabbles in '48 V down to power the processor,' which is closest to the processor.

Sheridan finds a new opportunity triggered by the industry's highest voltage SiC technology, which his company obtained via its GeneSiC acquisition. Ultra-high-voltage SiC technology will be essential in developing solid state transformers connected to the grid. Beyond data centres, Sheridan believes grids are getting upgraded to solid-state transformers everywhere, powering cities and homes, even connecting to renewable energy.

In the AI data centre market, Yole Group predicts that GaN will outgrow SiC. While SiC is focused on AC to DC, GaN used in DC to DC can also enter AC to DC. This is because GaN devices pose the potential for higher voltage.

"Although we see some upside market for SiC, about $100 million in three to five years, the opportunity seems much bigger for GaN," explained Chiu.

NREL team constructs record-beating SiC module

Ultra-Low Inductance Smart (ULIS) module can achieve five times greater energy density than predecessor designs

NREL has developed an Ultra-Low Inductance Smart (ULIS) SiC power module with a parasitic inductance seven-to-nine times lower than any current state-of-the-art SiC power module.

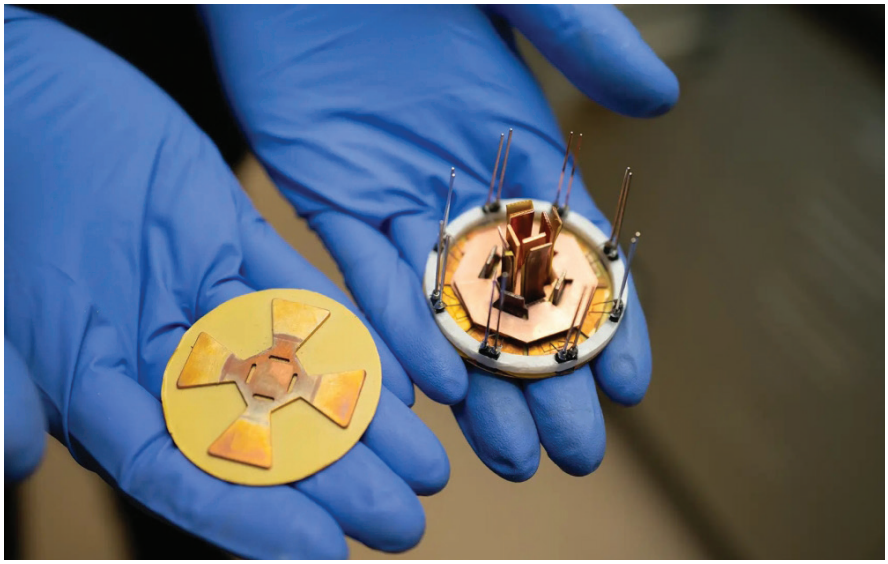
The 1200 V, 400 A module is capable of achieving five times greater energy density than predecessor designs in a smaller package, making it possible to build and power more efficient, compact, and lighter technologies for applications such as data centres, power grids, microreactors, and even heavy-duty vehicles, such as next-generation aircraft and military vehicles.

“We consider ULIS to be a true breakthrough,” said Faisal Khan, NREL’s chief power electronics researcher and the principal investigator for the project. “It’s a future-proofed, ultrafast power module that will make the next generation of power converters more affordable, efficient, and compact.”

Furthermore, Khan explained, ULIS is uniquely suited for high-intensity applications, like aviation and military operations, because the powerful, lightweight module also monitors its own state of health and can predict component failure before it occurs.

Unlike a typical brick-like power module, ULIS winds its circuits around a flat, octagonal design. The disk-like shape allows more devices to be housed in a smaller area, making the overall package smaller and lighter. At the same time, novel current routing allows for maximum magnetic flux cancellation, contributing to the power module’s clean, low-loss electrical output – in other words, its ultrahigh efficiency.

“Our biggest concern was that the device switches off and on very quickly, and we needed a layout that wouldn’t create a chokepoint within the design,” said Shuofeng Zhao, an NREL power electronics researcher who designed ULIS’ flux cancellation architecture.



One of the original layouts, Zhao said, looked like a flower with a semiconductor at the tip of each petal. Another idea was to create a hollow cylinder with components wired to the inside. Sarwar Islam, another NREL power electronics researcher on the ULIS team, came up with the 2D structure, which made it possible to build the module balancing complexity with cost and performance.

“We squished it flat, like a pancake,” Zhao said, “and suddenly we had a low-cost, high-performing design that was much easier to fabricate.”

Where conventional power modules rely on bulky and inflexible materials, also ULIS takes a new approach. Instead of dissipating excess heat by bonding copper sheets directly to a ceramic base, ULIS bonds copper to a flexible polymer, called Temprion, to create a thinner, lighter, more configurable design. Because the material bonds easily to copper using just pressure and heat, and because its parts can be machined using widely available equipment, ULIS can be fabricated quickly and inexpensively, according to the NREL team. Manufacturing costs total hundreds, rather than thousands, of dollars.

A further breakthrough allows ULIS to function wirelessly, as an isolated unit that can be controlled and monitored without external cables. A patent for this low-latency wireless communication protocol is pending.

ULIS can scale to accommodate advancements in semiconductor devices using SiC, GaN, and even gallium oxide.

> “We squished it flat, like a pancake, and suddenly we had a low-cost, high-performing design that was much easier to fabricate”

Navitas name Chris Allexandre as president and CEO

Semiconductor veteran succeeds founder Gene Sheridan

GaN and SiC specialist Navitas Semiconductor has appointed Chris Allexandre as president and CEO, from September 1, 2025. Allexandre, who also joins the company's board of directors, succeeds Gene Sheridan, a Navitas founder.

"We are excited to welcome Chris Allexandre as our new president and CEO," said Richard J. Hendrix, chairman of Navitas' board of directors. "Chris is joining Navitas at a pivotal moment in its evolution. We believe his track record of driving transformation and delivering sustainable and profitable growth, operational excellence and business leadership in power semiconductor markets makes him the right leader for the next chapter of Navitas."

He added: "On behalf of the board of directors, I'd like to thank Gene Sheridan for his vision in creating and leading Navitas over the last decade. Gene has established an exceptional company that stands ready to pursue the next phase of electrification in higher-power applications ideally suited for Navitas' portfolio of GaN and SiC solutions. We deeply appreciate Gene's leadership and impact, and his invaluable contributions to the board's succession planning and recruiting efforts, which have brought Navitas to this important transition point."

"I am incredibly proud of what we have accomplished at Navitas," said Sheridan, reflecting on his 11-year tenure at the company. "Building the industry's only next-gen, pure-play power semi company has been the privilege of a lifetime. As we look to the future, I'm confident that Chris Allexandre is the right choice to lead Navitas in its mission to electrify our world."

Allexandre brings more than 25 years of experience in the semiconductor industry. Most recently, he served in senior executive roles at Renesas Electronics, including SVP and general manager of its power division from October 2023. Allexandre oversaw Renesas' $2.5 billion power management business and led the pivot and execution of its power strategies toward the cloud infrastructure, automotive and industrial markets, including Renesas' acquisition and integration of Transphorm, a supplier of GaN solutions, in June 2024. Allexandre was previously Renesas' chief sales and marketing officer from 2019 to 2023.

"I am honoured and thrilled to join Navitas and look forward to working with this world-class team to accelerate our leadership in GaN and SiC technologies," said Allexandre. "With power demand growing in AI data centre and critically needed

energy infrastructure, I see promising opportunities to drive expansion in these important markets. I also want to thank Gene for his great support planning for this transition, and for everything he has done for Navitas."

Prior to his tenure at Renesas, Allexandre held executive roles at Integrated Device Technology (IDT) (acquired by Renesas in 2019) as SVP of sales and marketing; at NXP as SVP, worldwide sales for mass market; and at Fairchild Semiconductor as SVP of worldwide sales, marketing and business operations.

Allexandre began his career at Texas Instruments, beginning in its New College Graduate rotation programme, and over 16 years progressing through a series of business and sales roles based in Europe and China, becoming TI's VP of sales for EMEA and a member of TI's strategic leadership team in 2012.

IQE considers sale

Company expands scope of ongoing Strategic Review to incorporate the potential sale of the company

COMPOUND SEMICONDUCTOR wafer firm IQE plc has announced a trading update for the full year ending 31 December 2025, and that it's extending the scope of its ongoing Strategic Review to incorporate the potential sale of the company

IQE has previously said that trading in H1 2025 was impacted by macroeconomic uncertainty and as a result, some end customer demand was fulfilled with existing inventory.

The group says it has continued to experience weakness in wireless markets, largely as a result of softness in mobile handset sales, and this is expected to persist through 2025. In addition, delays to federal funding cycles in US military and defence sectors are resulting in the deferral of orders into 2026.

Revenue for FY 2025 is expected to be between £90.0 million to £100.0 million, resulting in an adjusted EBITDA position of between £(5.0) million to £2.0 million. H1 2025 revenue is expected to be at least £44.0 million. The group will report its interim results on 23 September 2025.

The board says there's significant market opportunity for IQE because of the group's leading position in providing

advanced compound semiconductors across several market verticals and to a base of global marque customers.

The board is now expanding the scope of the previously announced Strategic Review to also incorporate the potential sale of the company and is seeking buyers. While the Strategic Review process remains ongoing, IQE is progressing negotiations with multiple parties for the sale of the group's Taiwan operations.

Should the sale of Taiwan be concluded, it is expected that the proceeds from such sale will be used to fully repay the group's Revolving Credit Facility with HSBC Bank and Convertible Loan Notes issued in March 2025, as well as providing IQE with cash to invest in its core operations. The board continues to be advised by Lazard on the full scope of the Strategic Review.

Jutta Meier, CEO of IQE, commented: "We have updated our expectations for the full year to adjust for the deferral of certain contracts in our wireless and photonics segments.

This is a result of continued global and macro uncertainty which has impacted the unwinding of customer inventory levels pre-built in 2023 and 2024, the sale of new mobile handsets and the release of budgetary spending across the US military and defence sector.

"Looking ahead, while the Strategic Review remains ongoing I am encouraged by the progress we are making and remain confident in our ability to unlock value for all of our stakeholders."

SweGaN, Ericsson, Saab and Chalmers collaborate on 6G GaN PAs

Partnership will combine advanced modelling and fabrication to optimise PA performance across telecoms and defence

SWEGaN, a European semiconductor manufacturer specialising in GaN-on-SiC epitaxial wafers, announces the launch of a two year project funded by Vinnova (Sweden's innovation agency) with Ericsson, Saab, and Chalmers University of Technology, aiming to revolutionise GaN-based power amplifier technology for next-generation 6G networks.

The project targets the 7 - 15 GHz frequency range (X/Ku bands), a critical spectrum for future 6G applications. By leveraging SweGaN's proprietary QuanFINE epitaxial GaN-on-SiC solutions, the collaboration will deepen understanding of the material properties and the HEMT device characteristics and develop high-efficiency PA circuits that support energy-efficient, high-capacity wireless systems.

"This Vinnova-backed collaboration is a major milestone for SweGaN and our partners," said Jr-Tai Chen, CEO of SweGaN. "With this project, we're combining world-class expertise from telecom, defense, and academia to unlock the full potential of our QuanFINE materials for 6G." The project ensures vertical integration across materials, device processing, and system-level design, and it follows a dual-track approach.

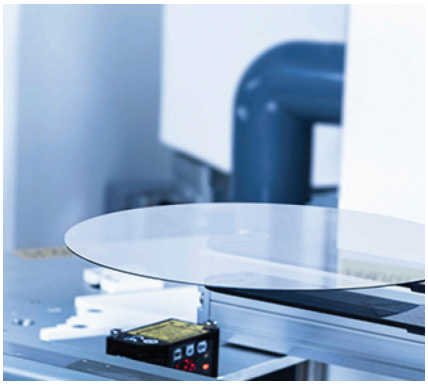
The academic track focuses on the influence and process variations on HEMT device-level performance by advanced modeling. The goal is to extract empirical models and define design boundaries for optimal PA efficiency.

The industrial track centres on PA design, fabrication, and benchmarking using state-of-the-art foundry processes. Industry partners will supply high-performance devices for modeling and validation, ensuring alignment with real-world system needs. The collaboration will deliver insights into how epitaxial design, processing, and circuit architecture impact device and system-level performance.

"This collaboration strengthens the bridge between civilian and defense technologies. By working closely with leading partners across the value chain, we accelerate the development of RF technologies that will have real-world impact in both defense and civilian domains," said Johan Carlert, head of microwave and antenna design at Saab.

"At Chalmers, we're thrilled to contribute our modeling and device expertise to a project with such high industrial relevance," said Christian Fager, professor at Chalmers University of Technology.

Toshiba and SICC sign SiC MoU



Companies announce intention to collaborate on improving SiC wafer quality

Toshiba and SICC have signed a memorandum of understanding (MoU) under which these two companies hope to work together to improve characteristics and quality of SiC power semiconductor wafers made by SICC, and enable expanded supply of stable, high-quality wafers from SICC to Toshiba.

According to Toshiba, it has an established track record in developing, manufacturing and selling SiC power semiconductors for railways, and is currently accelerating the development of SiC devices for applications including server power supplies and cars.

This work includes reducing power losses in SiC devices and improving their reliability and efficiency.

The proposed collaboration with SICC, a Chinese developer of SiC wafers, is expected to help drive forward improved solutions for various applications and to accelerate business expansion.

Since its founding in 2010, SICC has concentrated on producing single-crystal SiC wafers. Following its initial public offering in 2022, the first in China to focus on SiC, the company has expanded its market share.

In 2024, SICC introduced the market's first 12-inch SiC wafer, and in 2025 it announced 12-inch wafers for all products, including *n*-type, semi-insulating, and *p*-type.

In the proposed collaboration with Toshiba, SICC says it aims to link SiC power semiconductor manufacturers' requirements and expectations for SiC wafer element technology to improved wafer quality and reliability, and to contribute to the expansion of the SiC power semiconductor market.

Toshiba and SICC say they are still discussing specific collaboration details.

UW-Madison opens ultra wide bandgap lab

New US facility will focus on an emerging class of III-nitride semiconductors, such as AlGaN and AlN

The University of Wisconsin-Madison has opened an Ultra-Wide Bandgap Semiconductor MOCVD Laboratory, a facility that will focus on the emerging class of ultra wide bandgap III-nitride semiconductors such as AlGaN and AlN.

At the moment, fabricating and characterising ultra-wide bandgap semiconductors is challenging because they require expensive equipment and deep expertise in MOCVD or other advanced commercialisation-friendly deposition techniques.

Shubhra Pasayat (pictured above centre), who oversees the new facility as the lab's principal investigator, set up a commercial Aixtron MOCVD reactor for research when she first joined UW-Madison in 2021.

The new facility takes this to the next level with an Agnitron Agilis 100 system that can handle higher temperatures and lower pressures. This will allow Pasayat and her students to design

and precisely synthesise high-quality 2-inch diameter wafers of high-aluminium content ultra-wide bandgap materials.

The lab is described as being at the centre of UW-Madison's rising III-nitride ecosystem. The onsite faculty's broad expertise in chip design and architecture, materials characterisation, fabrication, advanced packaging, and systems integration means these ultra-wide bandgap semiconductors can go from the drawing board to the motherboard all on one campus – streamlining and improving the research process.

Wolfspeed launches 200 mm SiC materials portfolio

WOLFSPEED has announced the commercial launch of its 200 mm SiC materials products, marking a milestone in the company's mission to accelerate the industry's transition from silicon to SiC. It is also offering 200 mm SiC epitaxy for immediate qualification, which, when paired with the company's 200 mm bare wafers, will deliver breakthrough scalability and improved quality, enabling the next generation of high-performance power devices, according to the company.

"Wolfspeed's 200 mm SiC wafers are more than an expansion of wafer diameter – it represents a materials innovation that empowers our customers to accelerate their device roadmaps with confidence," said Cengiz Balkas, chief business officer.

The company says that the improved parametric specifications of the 200 mm SiC bare wafers at 350 μm thickness and enhanced doping and thickness uniformity of the 200 mm epitaxy enables device makers to improve MOSFET yields, accelerate time-to-market, and deliver more competitive solutions across automotive, renewable energy, industrial, and other high-growth applications. "This advancement reflects Wolfspeed's long-standing commitment to pushing the boundaries of SiC materials technology," said Balkas. "This launch demonstrates our ability to anticipate customer needs, scale with demand, and deliver the materials foundation that makes the future of more efficient power conversion possible."

CSA Catapult appoints Caroline O'Brien as CEO

THE UK's Compound Semiconductor Applications (CSA) Catapult has appointed Caroline O'Brien as its new CEO, who will join in late September.

A semiconductor industry specialist, O'Brien is currently CEO of Kubos Semiconductors and brings over 30 years of experience in the technology sector, where she has developed a broad knowledge of working with VC-backed businesses and blue-chip multinationals.

She has held senior commercial and executive positions in several companies, focusing on developing and commercialising new technologies and products.

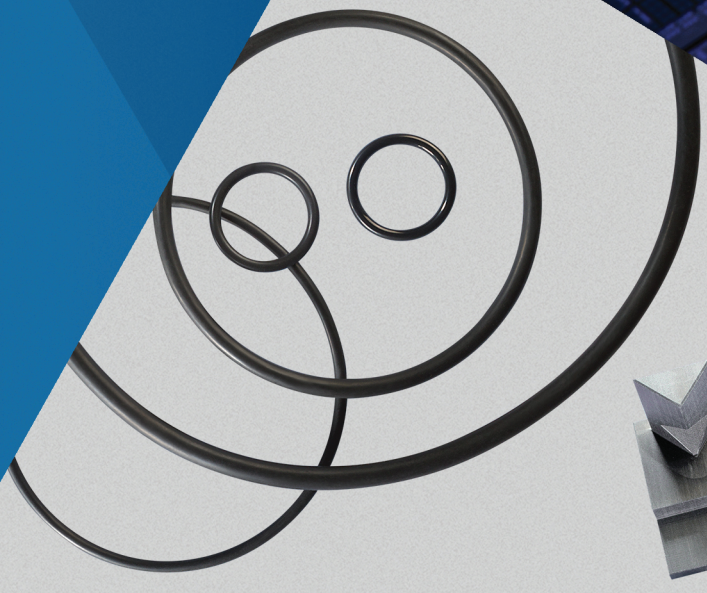
O'Brien holds a B.Eng in Electronics and Electrical Engineering and an MBA from the University of Bath.

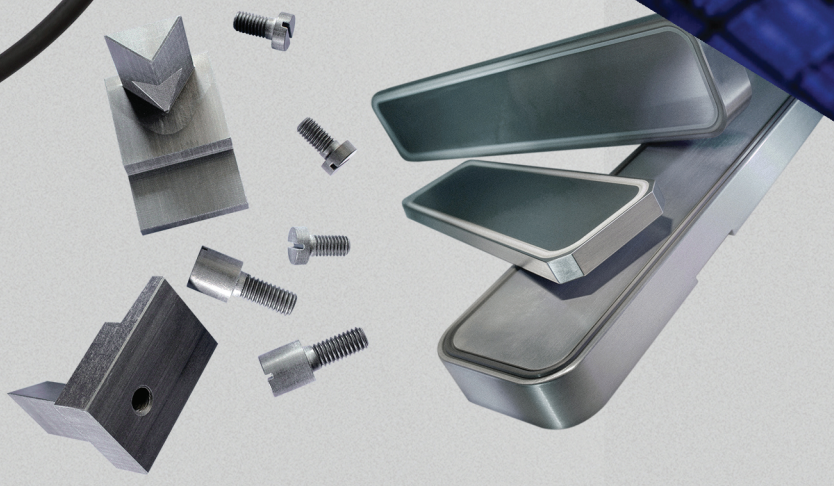
Martin McHugh stepped down as CEO of the Catapult in March 2025 and Raj Gawera, who joined the board in 2021, was appointed CEO on an interim basis from April 1 2025 and will return to his previous role as non-executive director.

WHEN IT CAN'T FAIL

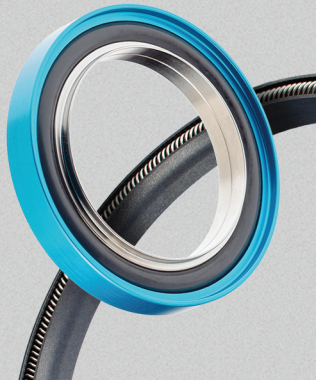
FROM ADVANCED MATERIALS TO PRECISION DESIGNS, OUR PRODUCTS ARE ENGINEERED FOR PERFORMANCE AND RELIABILITY

Greene Tweed





Discover our solutions for the semiconductor industry



Transforming transfer technology for microLEDs

Q-Pixel addresses the biggest bottleneck to manufacturing microLED displays with an out-of-the-box transfer technology that combines a critical hike in yield with superior throughput

BY RICHARD STEVENSON, EDITOR, CS MAGZINE

FOR around a decade or so, it feels like our industry has been on the cusp of a revolution in displays. But this breakthrough is yet to materialise. The only well-known display that's based on the microLED is the Samsung MS1A, a 110-inch TV that retails for an eye-watering $150,000 – it's so expensive that it's not going to win many sales, even to those with piles of cash and a strong interest in home entertainment.

Many would argue that the biggest barrier to the widespread manufacture of displays based on the microLED is the transfer technology employed to move vast numbers of these miniature marvels from processed epiwafers to a backplane.

While transferring microLEDs is not a pre-requisite for very small displays – they can be produced by bonding arrays of microLEDs formed on GaN-on-silicon epiwafers to a CMOS backplane that drives these emitters – a transfer process is non-negotiable for manufacturing displays for watches, smartphones, TVs and outdoor screens.

The big issue with conventional approaches to transferring microLEDs – such as the massively parallel techniques that involve picking-up vast numbers of these tiny emitters with an elastomeric stamp and placing them down on a backplane – is insufficient yield.

This view might raise a few eyebrows, as at first glance the yield figures realised with these traditional techniques look very impressive. But the reality is that they are not up to the task, argues J.C. Chen, CEO of Q-Pixel, a start-up with a yield-busting technology that's looking to license its microLED-related technologies to chipmakers and those wishing to produce displays.

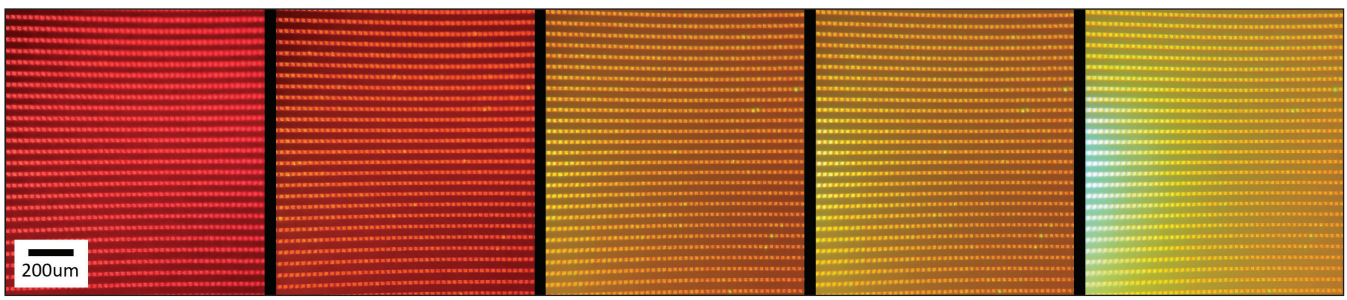
According to Chen, a commonly quoted yield figure for transfer technologies is 99.99 percent. "But in the microLED industry that's a no-no," claims Chen, pointing out that 24 million chips must be transferred to make an ultra-high-definition TV.

Expanding on this point, Chen explains that with a yield of 'four-nines', there are typically around 100 'dead' pixels for every million transferred.

"One hundred is very difficult to repair. But if you have 'five-nines' or 'six-nines', you have only one dead pixel."

Part of the reason why 'dead' pixels are unacceptable is that our benchmark is today's OLED and LCD screens, and they have an incredibly low level of defects.

"If you have 100 defects, you cannot really compete, no matter how good you are," says Chen, who explains that it's not possible to trade imperfections from dead pixels for the superior brightness and lower power



➤ Prototype panel demonstration of Q-Pixel's proprietary transfer process, using 10 µm tuneable polychromatic microLEDs to produce a display with a pixel density of over 500 pixels per inch. There are no missing pixels, and yield is more than 99.9995 percent.

consumption of displays based on microLEDs.

Breaking through this yield-related barrier is Q-Pixel's novel transfer technology, known as Q-Transfer, that is claimed to have a yield of more than 99.9995 percent.

Chen and his co-workers have demonstrated the production capability of Q-Transfer by using this technology to make prototype colour displays with 10 μm pixels, that are spaced close enough together to provide a density of more than 500 pixels-per-inch.

Q-Pixel stresses that as well as the phenomenal yield, this approach resulted in zero missing pixels.

For understandable reasons, Chen is tight-lipped when it comes to discussing the details of the Q-Transfer technology, which is credited to 'out-of-the-box' thinking. But he says that Q-Transfer is compatible with most transfer technologies, without much modification.

The origins of Q-Transfer can be traced back to Covid times, which hampered much company activity, but allowed the team to mull over challenging issues and come up with novel ideas.

Since then, they have been developing a new approach to microLED transfer. Efforts began with small displays, which gave encouraging results. However, bigger displays are needed to convince the display industry that Q-Transfer can be a game-changer. "We need at least a watch-size display. If you have just a 1 centimetre by 1 centimetre, it's probably too small," argues Chen.

Now Q-Pixel is demonstrating that its transfer technology is capable of producing displays for small watches.

"That means the technology has become available to industry," says Chen, who explains that this involves licensing Q-Transfer, and working with Q-Pixel on technology transfer.

Those interested in pursuing this will be keen to discuss throughput, as this plays a key role in determining the cost of manufacture. Those enquiring on this front will not be disappointed, according to Chen, as when Q-Transfer is applied to existing transfer approaches, the speed is similar, if not better.

Completing the puzzle

Chen views Q-Transfer as the last piece in the puzzle, when it comes to overcoming challenges to ensure an economically viable approach to producing microLED displays.

The company's other key technology is it's colour-tuneable GaN-based microLEDs. With this elegant device, emission wavelength is determined by driving conditions.

For all forms of GaN-based LED, there are concerns related to the efficiency in the red. Reaching this spectral domain demands an increase in the indium content in the quantum wells, a move that increases strain, leading to declines in crystal quality and emission efficiency.

Chen believes that for some applications, such as those that are indoors, the efficiency of Q-Pixel's colour-tuneable microLEDs is sufficient.

But for outdoor applications, it's not so clear, due to a lack of data. "Honestly, we are not up to that point yet."

What is beyond question is that microLEDs are incredibly compelling candidates for deployment in outdoor displays. Unlike those based of OLEDs and LCDs, they are not impaired by exposure to UV light, and they do not burn out.

Having demonstrated the key technologies to kick-start mass production of microLED displays, the next goal for Q-Pixel is to start working with companies that have invested in equipment to manufacture this class of display.

Such a partnership would be based on licensing technology from Q-Pixel. "We are basically an IP company. We're just doing the R&D and some demonstration," says Chen.

He believes that such ventures could allow the microLED industry to take off.

"The whole industry is not moving fast enough," laments Chen. "But I think that we can make it happen faster. That's our goal."

X-Fab: Normally-on, then normally-off

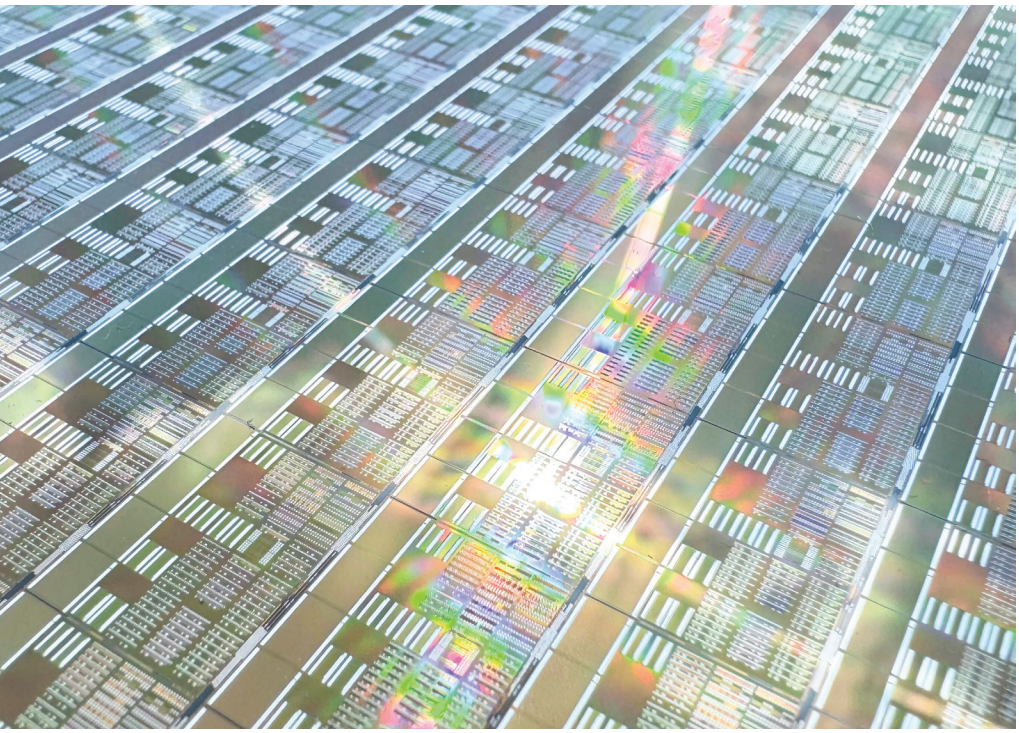
At X-Fab's Dresden foundry that's been churning out silicon devices for decades, production of normally-on GaN HEMTs is now underway, with normally-off variants soon to follow

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

EVEN if you don't know much about economics, you'll be familiar with the idea that supply rises and falls to meet demand. So, given that sales of GaN power devices are rising fast and will continue to climb, one should expect global GaN foundry capacity to increase over the coming years.

Against this backdrop, TSMC's recent decision to move away from offering a GaN foundry service will have raised a few eyebrows. It's a move that bucks the trend, as companies looking to outsource production of GaN HEMTs and Schottky barrier diodes are benefitting from an increasing choice of foundries, with this service now starting to be offered in Europe for the first time, thanks to efforts at X-Fab's Dresden facility.

At this fab, opened in 1961 and taken over by X-Fab about 15 years ago, chip production is dominated by silicon power devices for automotive applications, manufactured on a 200 mm line capable of producing 350 nm CMOS technologies. But X-Fab is now expanding the use of this facility, by offering customers the opportunity to design and make normally-on (D-mode) GaN HEMTs with blocking voltages from 100 V to 650 V. This is the first step in the formation of a commercial GaN portfolio, soon to be strengthened with the introduction of normally-off (E-mode) HEMTs and Schottky barrier diodes. All these devices are complementing those based on SiC, produced at the Lubbock Fab in Texas, and give X-Fab's customers a tremendous choice when it comes to the two leading wide bandgap technologies for power electronics.



➤ X-Fab has been developing GaN HEMT technology at its Dresden foundry since 2015.

X-Fab has been developing and refining GaN technology since 2015, with efforts originating from interest from a lead customer. This led to an initial process flow for D-mode devices.

"We didn't stop there," reveals the X-Fab's GaN Technical Marketing Manager, David Auffret, who says they also developed a Schottky barrier diode, viewed within X-Fab as a variation of the HEMT, thanks to the foundry's modular approach to device production.

A decade on from its first foray into GaN power technology, Auffret argues that now is the right time to offer this capability to customers.

According to Auffret, GaN has now reached a high level of acceptance within the power electronics industry. "If you go to conferences, you will see more and more talks about GaN." What's more, customer interest in GaN is high and increasing.

Within the GaN power electronics industry, much production occurs at IDMs, which produce some very impressive products. However, these off-the-shelf components, regardless of the performance they offer, may not meet everyone's needs.

Helping to address this limitation, X-Fab has been sampling D-mode technology. At its heart is a core platform that's open to all, rather than one that's customised for just one or two customers.

Interested parties are able to draw on X-Fab's process-design kits (PDKs), which are undergoing continuous improvement.

"The goal is to have something similar to our CMOS business," says Auffret. "The PDK will enable the customer to make first-time-right design, and have a faster time to market."

The 200 mm line at the Dresden Foundry has focused in producing devices using 350 nm CMOS technology, but will soon also provide the production of GaN-based D- and E-mode HEMTs and Schottky barrier diodes.

Another advantage of working with X-Fab is that customers wanting a unique product can customise process flow.

In the final quarter of this year, X-Fab will start running multi-projects wafers through its lines. "It's cutting the development cost, not only for the customer but also for us. It's really a win-win," says Auffret.

With multi-project wafers, customers can trim their time to market, while reducing proto-typing costs, by avoiding paying for mask sets. And rather than footing the bill for the manufacture of two or three wafers populated with thousands of die, they receive just 50 or so die, enough for evaluation purposes.

While X-Fab's D-mode technology is new to customers, it has a level of maturity that comes from production on a well-established 200 mm line featuring substantial monitoring. The engineers at Dresden have produced tests chips, with measurements revealing an on-resistance of less than 2 mΩ cm^2, at 650 V.

The decision to begin by offering normally-on HEMTs sets X-Fab apart from a number of rivals – many of them are focusing on the normally-off variant that provides much-valued fail-safe operation.

However, despite this weakness, normally-on HEMTs are in demand: they have a higher efficiency; they are better-suited to continuous sensing, making them attractive for medical applications; and with the addition of external circuity, fail-safe operation can be realised.

Interest in X-Fab's D-mode HEMTs is strongest for 650 V devices, and there is some demand up to 1200 V. In comparison, for the E-mode variants under development, which can be produced by processing modified epiwafers with just a couple of extra masks thanks to the foundry's modular approach, interest is at 650 V and below.

X-Fab does not have facilities for epi-growth, so sources material from partners. "Three of them are qualified or about to be qualified," says Auffret, who adds that customers can also provide their own epiwafers to the foundry.

For both approaches, epiwafers need to be produced on thick silicon substrates that are less prone to bow and warp that results from lattice and thermal mismatches between the GaN epilayers and its foundation.

At the Dresden foundry, processing stops at the wafer level. "We don't provide any packaging," says Auffret, who explain that X-Fab does work with some partners for dicing. What may come as a surprise is that as well as offering back-side grounding, there's micro-transfer capability at X-Fab, which has the potential to unite GaN power devices with silicon CMOS circuitry, by placing one technology on top of the other.

With interest in GaN on the rise, opportunities for production on 300 mm substrates are attracting debate. The view of Auffret is that now is too early, as this larger size would drive up chip costs, rather than delivering economies of scale. While X-Fab is involved in 'close' discussions with epiwafer and equipment suppliers regarding the larger format, the 200 mm platform is viewed as the sweet spot, not just for now, but also for the near future.

Looking ahead, another evolution that X-Fab will want to optimise, in order to maximise sales and profits, is the transition from CMOS to GaN at the Dresden fab. Today, CMOS is fully loading the fab, and funding its existence until GaN is ready to ramp.

Producing both classes of technology in the same foundry places X-Fab in an enviable position. While some within our industry are having to fight against silicon to ensure success, the Dresden fab can churn out chips, while reacting to any twists and turns within the power electronics industry.

Effective communication with government and other stakeholders

Discussions with government officials and leaders of other bodies should avoid detailing core technologies and focus on tangible benefits of a flourishing compound semiconductor industry

BY HOWARD RUPPRECHT FROM CSCONNECTED

SEMICONDUCTORS are ubiquitous and largely invisible. As the little black boxes attached to circuit boards, we are all utterly reliant on their functionality for virtually everything we do – yet we take their easy availability and low cost for granted.

During the pandemic, when semiconductor shortages thwarted car sales, the importance of these chips – and our dependence on them – finally started to resonate among policymakers. Geopolitics (particularly between China, the US and Taiwan) further escalated supply chain risks, prompting calls for 're-shoring', supported by huge subsidies.

But it's far from easy to construct sovereign supply chains. Semiconductor design and manufacturing is an exclusive club, only a few countries are members, and none of them enjoys full independence or capabilities to make the latest semiconductors.

Like many countries involved in our industry, to ensure that the UK maintains its membership, some level of governmental support is needed to continue to develop unique sovereign capabilities, which are traded with allies. But for those with leadership roles in semiconductor companies and associated bodies in the UK – and those holding similar positions in other countries – what's the key to successfully communicating our industry needs to national and regional policymakers, and justifying these investments to the nation at large, including the taxpayers?

It's fair to say that politicians and civil servants are unlikely to read *Compound Semiconductor* magazine, so it's essential to use different channels. In our case, at CSconnected, we are working with a wide range of non-industrial stakeholders, from local politicians that have semiconductor facilities within their constituencies, to national government departments whose role is to deploy funding for growth. From holding local events, to managing an All-Party-Parliamentary-Group, we strive to avoid explaining technicalities, focusing instead on increasing awareness and understanding industry dynamics, and the subsequent economic benefits that a thriving CS industry can deliver.

I don't need to tell you that semiconductors are not a commodity, and must be viewed markedly differently from the likes of oil and steel. Our sector produces highly differentiated individual components, with the market for them skewed by massive national and regional intervention, to support local industry. It is crucial to drive home the point that these are not 'subsidies for a failing industry', but are a price that's well worth paying to maintain a strategically important leadership position in a global industry. One should view support for the semiconductor industry as more akin to regularly watering an orchard. If it stops, trees will ultimately yield less fruit and eventually die. Sometimes nature supplies the necessary rain, and sometimes we need to irrigate to ensure long-term sustainability.

Publicly funded support tends to takes the form of R&D funding, generally leveraged by both public and private equity. In an industry spending around 16 percent of its revenue on R&D, it is essential to continually innovate, as this type of

work creates and sustains many highly paid knowledge-intensive positions. Equally, it's important to support the building of research and scale-up facilities with leading-edge equipment, to create an open access environment where deep-tech companies can develop the future. In south Wales, we are succeeding on this front with the Centre for Integrative Semiconductor Materials, at Swansea University. It's essential to explain to local stakeholders how these investments support long-term job creation, enable leverage for further investment, facilitate entrepreneurship and drive industrial scale-up.

In our locality, the compound semiconductor cluster works with the Welsh Economic Research Unit at Cardiff University to independently track the economic impact of local investment. Since 2020, employment has grown by 32 percent within the cluster, gross valued-added contribution is more than three times that of the national average, and we are proud to export over 90 percent of the collective £500 million in annual revenue from cluster companies. Ultimately, it's these numbers that resonate with our stakeholders and benefactors when justifying investment.

For us, the biggest challenge is associated with the public sector answering to a different group of stakeholders. Probably including some democratically elected decision makers, this group is made up of individuals that have their own vested interests, whether at a local constituency or ministerial portfolio level. As there are many competing sectoral and geographical investments on the table, this group will inherently struggle to focus, as doing so will threaten accusations of excluding worthwhile ventures. The result is that public money tends to be spread thinly across numerous causes, rather than being effectively focused.

Decision making can also be painfully slow, requiring independent evidence and adherence to onerous public procurement rules. This drawn-out process results in long cycles of investment and subsequent impact that often transcends political terms, bringing a risk of jeopardy from a changing strategy if the political incumbent changes. Against this backdrop, it's not uncommon for former policy makers to fail to see the results of their decisions until after their term in office.

Some of what I'm describing is common across western democracies. This is why we are unlikely to see the kind of focus evident in Tawain, South Korea or China, where there are closer industrial links to long-term policy and government support. This is unfortunately a disadvantage in such a fast-moving global market. Private companies are essentially autocratic and have the freedom to make fast, bold decisions on investment and strategy (within the bounds of applicable law) without having to seek approval beyond major shareholders.

Given the different perspectives that exist, what's needed to effectively work with government?

Our experience shows that working as a group has stronger impact and is more efficient for all parties. So, if a delegation is visiting our cluster, we collectively mobilize. A single voice representing a large group with common needs is more effective.

In addition, we devote much effort to building long-term relationships with the government and its officials. Like any relationship, we have good and bad times, but we all need to collaborate. We must accept that there will be a turnover of people, so a level of mutual re-education will be periodically required, and relationships must exist at many levels.

Finally, it's important to find common ground. Some things are easier for government to do than others. For instance, an investment in skills development has a wide impact on the community, while still supporting the development of essential resources needed for cluster growth. Equally, there may be a preference for interventions that leverage large amounts of private equity.

What's clear is that the future success of the UK's semiconductor industry will depend in part on successful collaboration between industry and public stakeholders – and we will endeavour to keep these relationships active and constructive.

Agnitron: Driving ultra-wide-bandgap breakthroughs

Advancing the capabilities of AlN, AlScN and aluminium-rich AlGaN is the Agnitron Agilis 100 MOCVD reactor

BY FIKADU ALEMA, WILLIAM BRAND, BENJAMIN BRAND, AARON FINE, VITALI SOUKHOVEEV AND ANDREI OSINSKY FROM AGNITRON TECHNOLOGIES

WITHIN the family of known semiconductors, AlN possesses a number of tremendous attributes. They include a remarkably wide bandgap of 6.2 eV, a Schottky barrier height of more than 2 eV, an outstanding thermal conductivity, and a critical breakdown field exceeding 15 MV cm^{-1}. Thanks to these great characteristics, the Baliga Figure of Merit for AlN is far higher than that for GaN, SiC, and even other ultra-wide bandgap materials, like Ga_2O_3, making AlN a leading contender for future high-power and high-temperature electronic applications.

Also offering much promise is a relatively novel ternary alloy that's closely related to AlN: AlScN. For scandium concentrations of more than 20 percent or so, AlScN combines ferroelectric switching behaviour with excellent thermal stability and CMOS compatibility, making it highly suitable for non-volatile memory and pyroelectric sensors operating above 600°C. Due to its robustness in ferroelectric applications, devices made from AlScN promise to provide reliable performance in extreme environments, while pyroelectric capabilities enhance sensitivity and durability in thermal detection and surveillance applications. Additional assets include: exceptional piezoelectric properties, supporting applications such as filters, resonators, energy-harvesting transducers, and MEMS sensors in harsh and high-temperature conditions; and an ultra-wide-bandgap, enabling use in high-temperature RF electronics exceeding 500°C. What's more, AlScN holds significant promise for optoelectronic applications, including spatial light modulators, further extending its applicability across a broad temperature range.

Critical to leveraging the vast potential of both AlN and AlScN is the growth of high-quality epitaxial material with characteristics suitable for making high-performance devices. Assisting in this endeavour is our team from Agnitron Technology, offering MOCVD reactors that are tailored to producing AlN-based epiwafers with ground-breaking levels of free electron concentration, and AlScN-based epiwafers with exceptional material quality.

AlN challenges

Despite their immense potential, AlN-based power devices are still in their early stages of development, with several key challenges to overcome. Obstacles include: a lack of cost-effective, large-area native substrates; difficulties in achieving high-efficiency doping; and the need for reliable, low-resistance ohmic and Schottky contacts. Fortunately, these difficulties are steadily being addressed through continued progress in AlN epitaxy, doping, and contact engineering, with advances unlocking pathways to a new generation of power devices that surpass the limitations of today's wide bandgap technologies.

One of the main challenges hindering deployment of AlN power electronics is achieving sufficiently high and stable *n*-type carrier concentrations and mobilities in device layers needed in diodes and transistors. Dopants typically come from group IV elements, and include silicon and germanium, with the former the most extensively studied. However, when silicon dopants are used in AlN, they fail to form the shallow hydrogenic donors they do in GaN. Instead, when adding a small amount of silicon to AlN, the result is a deep-level defect known as a DX centre. This deep-level defect, an electron trap near the conduction band edge with an activation energy ranging from 78 meV to 345 meV [1], leads to poor carrier activation at room temperature.

Increasing silicon doping initially improves the free-electron concentration, but only up to a point. Beyond a critical doping level, there's a fall in free-carrier concentration – a phenomenon known as the compensation knee. This detrimental decline in free-carrier concentration comes from compensation mechanisms, including the formation of DX centres, cation vacancies, silicon-vacancy complexes, and other point or extended defects. All these mechanisms fundamentally limit the effectiveness of heavy doping in AlN, and are a critical barrier to achieving technologically relevant *n*-type conductivity.

Point defect control in AlN

To enhance the electrical properties of AlN, and ultimately realise stable and efficient *n*-type doping, it's essential to control the formation of point defects. In this regard, one must consider the formation energy of a point defect. This energy, strongly influenced by the crystal's chemical potential and the position of its Fermi level, determines the equilibrium concentration. By tuning the crystal's chemical potential and the position of its Fermi level, it's possible to cut the density of compensating defects, and thereby enhance the activation efficiency of intentional dopants.

The chemical potential depends on growth conditions and can be controlled by process optimisation. For AlN, epitaxial films can be formed with a number of techniques, including MOCVD, MBE, HVPE, and sputtering. Amongst them, MOCVD stands out as the most mature and widely adopted method for forming high-quality, device-grade films. This growth technology provides excellent crystalline quality, low dislocation densities, wafer-scale uniformity, and precise doping control, making it suitable for scalable production.

With MOCVD, the chemical potential can be controlled by adjusting growth parameters, such as temperature, reactor pressure, and the V/III precursor ratio. In parallel, it's possible to dynamically manipulate the position of the Fermi level with UV-assisted epitaxy. The mechanism behind this is the injection of minority carriers into the crystal, which occurs when light with a wavelength above the bandgap is absorbed. It's a process that's referred to as defect quasi-Fermi level control. Adjusting the growth parameters to control the chemical potential and using UV light to manipulate the Fermi level dynamically increases

the formation energy of compensating defects, such as carbon substituting nitrogen (C_N), nitrogen vacancies, and impurity complexes, making their formation less favorable [2].

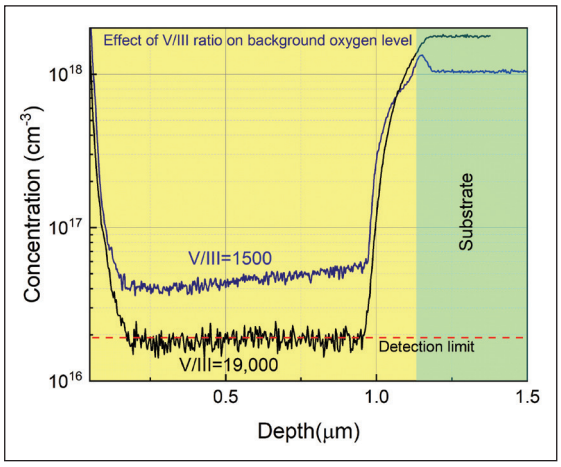
Agilis 100 reactors for AlN growth

Through a DARPA-funded project, we have been actively developing an MOCVD process for growing thin films of high-quality AlN. This effort employs our Agilis 100 MOCVD platforms, equipped with two different showerhead geometries: a remote-injection showerhead (RIS) and a close-injection showerhead (CIS). These studies have involved growth on *c*-plane AlN substrates obtained from domestic suppliers.

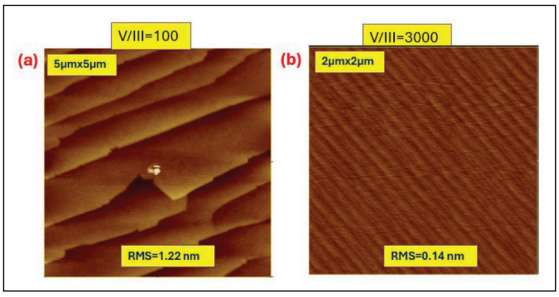
For both configurations, reactor design and process conditions have delivered a significant impact on the resulting film quality, particularly with respect to improvements in surface roughness, background carbon and oxygen incorporation, and structural and electrical properties of the AlN films. The CIS configuration, featuring a short distance between the showerhead and substrate, allows the use of a wide range of ammonia flow rates (V/III ratios) without negatively impacting the growth rate. This flexibility is particularly valuable, as the V/III ratio plays a critical role in controlling impurity levels in the grown films, such as the carbon and oxygen concentrations.

According to secondary ion mass spectrometry (SIMS) measurements, our AlN films grown in the CIS reactor at a high V/III ratio of 19,000 have oxygen concentrations near the detection limit, which is around 2×10^{16} cm^{-3}. In contrast, films grown at a lower V/III ratio of 1,500 have an oxygen concentration approximately 2.3 times the detection limit (see Figure 1). We have observed similar trends for films grown in our RIS reactor, underscoring the importance of high ammonia flow in suppressing oxygen incorporation across different reactor designs.

As well as offering the opportunity to control impurities, the V/III ratio impacts surface morphology. Assessments with atomic force microscopy highlight the benefits of a higher V/III ratio when growing AlN films that are around 1 µm-thick in the RIS reactor, using trimethylaluminum (TMAl) as the source of aluminium. When increasing the V/III ratio from 100 to 3,000, under otherwise identical conditions, atomically smooth, step-flow surfaces without any visible pits are maintained. However, the higher V/III ratio produces a significantly smoother surface, with values for root-mean-square (RMS) roughness comparable to those of the starting substrate. We can conclude that the benefits of increasing the V/III ratio are reduced impurity incorporation and improved surface smoothness – both are critical attributes for device-quality AlN layers.



➤ Figure 1. Secondary ion mass spectrometry depth profiles of oxygen (O) concentration in AlN layers grown in the CIS reactor at two different V/III ratios: around 19,000 (black trace) and around 1,500 (blue trace).



➤ Figure 2. Atomic force microscopy images of undoped AlN films that are around 1 µm-thick and grown on AlN substrates using RIS MOCVD. TMAl provides the aluminium source, and V/III ratios are (a) 100 and (b) 3000.

We have also investigated the influence of substrate temperature and silane flow on film morphology. This work determined that unintentionally doped AlN films grown between 1200°C and 1300°C consistently produce smooth surfaces with RMS roughness values around 0.18 nm. We did not observe any surface pits in these epilayers, indicating high-quality growth that's independent of temperature within this range.

However, the intentional introduction of silane, to provide silicon doping, causes surface morphology to become more sensitive to process conditions. In this case, one must carefully optimise growth parameters to suppress pit formation and maintain a high film quality.

To evaluate the crystalline quality of our AlN films grown using RIS and CIS reactors, we have turned to high-resolution X-ray diffraction. This investigation considered films formed with TMAl as the aluminium source, using different V/III ratios, and with and without intentional doping. For AlN layers grown in the RIS reactor, (0002) rocking curves have a full width at half-maximum (FWHM) ranging from just 15 to 110 arcseconds (see Figure 3). To put those figures in perspective, the typical FWHM specification for a bulk AlN substrate is below 100 arcseconds. Therefore, we can conclude that our MOCVD-grown AlN films – regardless of doping – exhibit excellent crystalline quality that's comparable to or exceeds that of the substrates.

Another encouraging finding is that a range of AlN layers grown in our CIS reactor have FWHM values

below 20 arcseconds. This confirms that both configurations of the Agilis 100 can produce high-quality AlN epitaxial layers.

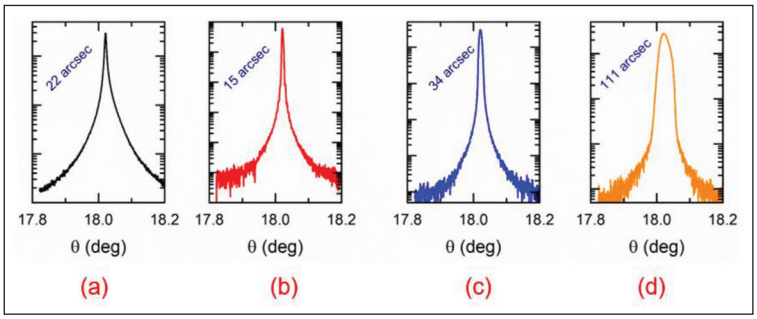
Encouraging electrical results

Amongst the various process parameters that influence the quality of AlN films, it is well established that the growth pressure plays a significant role in the activation energy of silicon dopants in AlN. To investigate this effect, we have grown a series of silicon-doped AlN layers in the RIS MOCVD reactor by systematically varying the growth pressures.

Our study revealed a clear trend: at standard pressures, often around 20 Torr as typically used by other researchers, AlN films exhibit relatively low free carrier concentrations in the 10^{15} cm^{-3} range, while Hall mobilities can exceed 30 cm^2 V^{-1} s^{-1}. In sharp contrast, films grown under lower pressures show significantly enhanced carrier concentrations, ranging from 1.3 × 10^{16} cm^{-3} to 4.4 × 10^{16} cm^{-3} – more than an order of magnitude higher than values usually reported for silicon-doped AlN [3].

According to SIMS measurements, the silicon doping concentrations in these low-pressure films remain in the low 10^{18} cm^{-3} range. Comparison of these doping levels with the corresponding free-carrier concentrations reveals activation efficiencies exceeding 1.5 percent under the lowest growth pressure conditions, representing a substantial improvement over films grown at standard pressures.

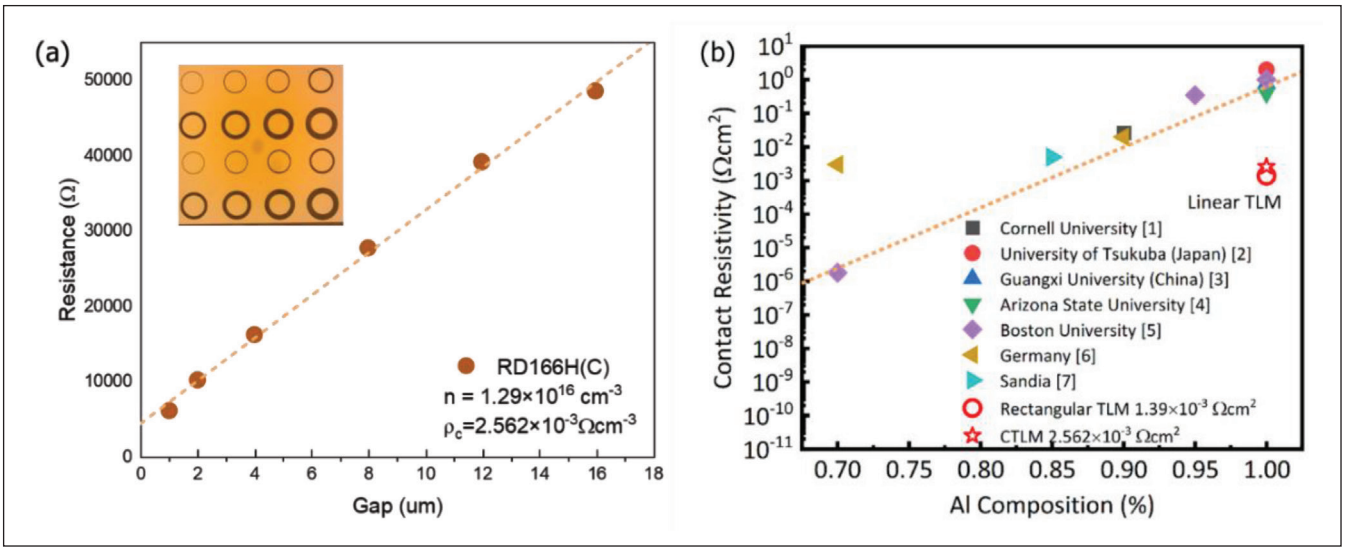
The exact mechanism behind enhanced activation is unclear. One plausible explanation is that low-pressure growth drives the system away from thermodynamic equilibrium, thereby suppressing the formation of silicon-related DX centres and enhancing dopant activation. Under these non-equilibrium conditions, the chemical potential of the film can be altered, influencing the formation energies and concentrations of compensating point defects.



➤ Figure 3. High-resolution X-ray diffraction rocking curves for the (0002) reflection of AlN films grown on native substrates using the RIS reactor. The layers were grown under varying growth conditions: (a) unintentionally doped AlN layer grown using a V/III ratio of 100, (b) a doped AlN layer grown using a V/III ratio of 100, (c) a doped AlN layer grown using a V/III ratio of 3000, and (d) a doped AlN layer grown using a V/III ratio of 1500.

To evaluate the electrical contact quality of our AlN layer grown at low pressures, we have collaborated with Houqiang Fu's team at Arizona State University. Fu and his colleagues have fabricated circular transfer-length measurement structures and determined a contact resistivity of 2.56 × 10^{-3} Ω cm^2 (see Figure 4). This is an impressive figure, as typical AlN contact resistivities range from 0.1 to 100 Ω cm^2 [4-6].

Further evidence of the merit of low-pressure growth for good electrical contacts comes from rectangular transfer-length measurement structures, processed



➤ Figure 4. (a) Extracted resistance versus gap spacing from circular transfer-length measurements with data corrected for pad geometry. (b) Benchmark comparison of contact resistivity, with the red star and circle representing results from AlN samples grown at Agnitron Technology. References: [1] Appl. Phys. Express **15** 061007 (2022); [2] Appl. Phys. Express **16** 064005 (2023); [3] Cryst. Growth Des. **24** 3960 (2024); [4] Appl. Phys. Express **17** 074001 (2024); [5] Appl. Phys. Lett. **90** 062115 (2007); [6] Photon. Res. **8** 1381 (2020); [7] Phys. Status Solidi **A 214** 1600842 (2017).

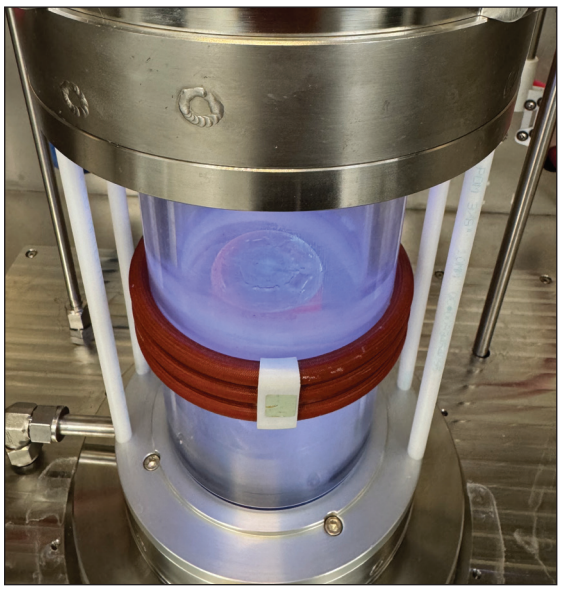
AlGaN: Si layers	n (cm^{-3})	μ(cm2/Vs)	ρ (mΩ.cm)	Reactor type used
$Al_{0.75}Ga_{0.25}N$	1.1×10^{19}	33.0	17.6	RIS
$Al_{0.77}Ga_{0.23}N$	4.5×10^{18}	72.3	19.1	RIS
$Al_{0.77}Ga_{0.23}N$	1.2×10^{18}	96.8	18.6	CIS
$Al_{0.75}Ga_{0.25}N$	9.8×10^{18}	24.0	27.0	C. E. Quiñones et al[3]
$Al_{0.86}Ga_{0.14}N$	2.8×10^{18}	23.3	94.8	RIS

➤ Table 1. Electrical properties of silicon-doped AlGaN layers with a high aluminium content (around 75–84 percent), grown using RIS and CIS MOCVD reactors. The table summarises the free-carrier concentration (n), electron mobility (μ), and resistivity (ρ) of each sample. For comparison, representative best values reported in the literature are included.

without mesa isolation. In this case, contact resistivity is even lower: 1.39×10^{-3} Ω cm^2. Taken together, these results highlight the promise of low-pressure MOCVD growth for realising high-activation-efficiency, low-resistivity silicon-doped AlN layers [7].

As is the case for AlN, with its related alloy AlGaN, it is hard to realise a high conductivity when the aluminium content is high, due to dopant compensation. But success is possible, and through careful optimisation of the growth process in our Agilis 100 MOCVD reactor with CIS and RIS showerheads, we have demonstrated highly conductive silicon-doped AlGaN films with aluminium compositions exceeding 75 percent. For films with an aluminium mole fraction of 75-80 percent, we consistently realise resistivities below 25 mΩ cm (see Table I) – that's significantly lower than literature values [3]. The corresponding carrier concentrations are up to 1.1×10^{19} cm^{-3}, and mobilities can be as high as 97 cm^2 V^{-1} s^{-1}.

Drawing on our optimised growth conditions for high-aluminium-content AlGaN, in combination with our low-pressure AlN growth that yields a free-carrier concentration of 1.3×10^{16} cm^{-3}, we have partnered with the team at Arizona State University to produce a Schottky barrier diode structure. To ensure smooth band alignment between AlN and AlGaN layers, this heterostructure incorporates a graded AlGaN transition layer, effectively minimising the conduction band discontinuity at the interface.



➤ Figure 5. An RIS reactor with UV exposure capability.

Our diodes deliver excellent electrical performance. Plots of current-voltage reveal a current density exceeding 4 kA cm^{-2} at 20 V. Using this data, we have calculated that the specific on-resistance is below 20 mΩ cm^2 at +15 V [7]. These results are particularly remarkable, given the wide bandgap nature of AlN. They underscore the viability of our epitaxial processes for high-performance vertical diode applications.

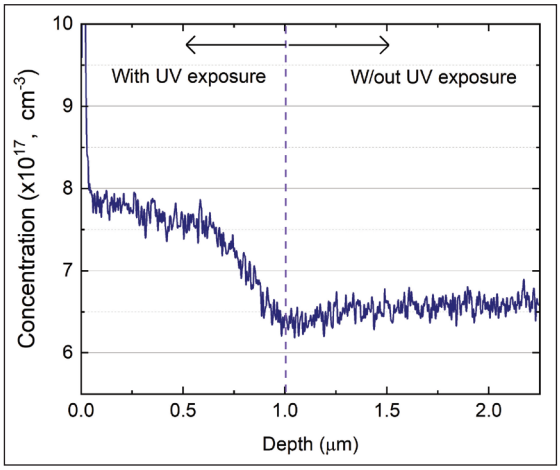
UV-assisted growth of AlN

We have also investigated the benefits of applying UV light during growth, an addition that suppresses compensating point defects in AlN. For this effort, we developed a new-generation RIS for the Agilis 100 reactor (see Figure 5). Designed from the ground up, this new showerhead incorporates UV light from either deuterium or Hg-Xe lamps. Switching between these sources is easy, with selection based on employing the most suitable spectral range for optimal defect control.

Constructed using US Patents 12,011,764 B1 and 12,337,388 B2, along with other proprietary technologies, our showerhead features a port for a fibre optic cord. With this approach, UV light is delivered through a single ultra-precise UV viewport, ensuring minimal distortion and losses, without the need for a light pipe. UV light entering the growth chamber is uniformly distributed across a 2.3-inch OD wafer carrier via a carefully engineered funnel, developed to ensure perfect coverage while minimising space within the showerhead and preserving gas dynamics and precursor delivery. Fully interchangeable with legacy Agilis 100 and Agilis Mini systems, our innovative design allows existing users to upgrade seamlessly, maintaining our commitment to scalable, high-performance MOCVD hardware for advancing ultra-wide bandgap materials, such as AlN.

To evaluate the effect of UV illumination on silicon incorporation in AlN, we have grown a 2 μm-thick silicon-doped film of this nitride on an AlN substrate. For this investigation we grew the layer in two segments in the same MOCVD run: the first 1 μm without UV exposure, and the second 1 μm with UV exposure.

According to SIMS, UV exposures increase the silicon concentration. In this AlN sample, UV exposure causes the silicon concentration to rise by almost 20 percent from 6.5×10^{17} cm^{-3} to 7.7×10^{17} cm^{-3}.



➤ Figure 6. SIMS depth profiles showing silicon concentration in AlN layers grown using the RIS reactor with and without UV exposure. UV illumination during growth resulted in approximately a 19 percent increase in silicon incorporation compared to the non-UV-exposed region.

To assess the electrical impact of our UV-assisted growth, we have grown additional single-layer silicon-doped AlN films, both with and without UV exposure, and characterised them with Hall-effect measurements. We found that UV exposure increases the carrier concentration from around 8.0×10^{14} cm^{-3} to 1.3×10^{15} cm^{-3}, produces a slight reduction in electron mobility from around 107 cm^2 V^{-1} s^{-1} to 90 cm^2 V^{-1} s^{-1}, and ultimately trims resistivity from around 65 Ω cm to 55 Ω cm. The upshot is enhanced conductivity, driven by a higher free-electron concentration. Separately, a silicon-doped AlN layer grown without UV achieved a mobility of more than 120 cm^2 V^{-1} s^{-1} mobility with an electron concentration of around 4.3×10^{14} cm^{-3}.

These results show that UV-assisted MOCVD growth effectively enhances silicon incorporation in AlN films, and improves electrical conductivity. This significant benefit comes with a slight reduction in mobility, probably due to either modified defect dynamics or increased scattering, associated with the altered growth environment.

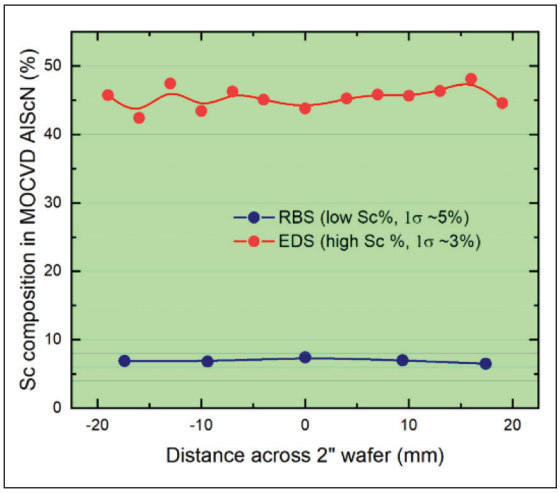
Ferroelectric AlScN films

Over the last few years, we have extensively utilised our R&D MOCVD reactor for the growth of high-quality thin films of AlScN. At first our primary goal was to explore the growth of AlScN using Cp_3Sc, which was the most widely used precursor at the time. But this state-of-affairs has recently changed, and now we are evaluating the growth of AlScN using ASGARD, an alternative scandium precursor offering many advantages compared with Cp_3Sc. Unlike Cp_3Sc, which stays solid up to 240°C, ASGARD is liquid at room temperature and thus provides the higher vapour pressure needed for efficient scandium delivery to the reactor. This allows for faster growth rates and improved consistency.

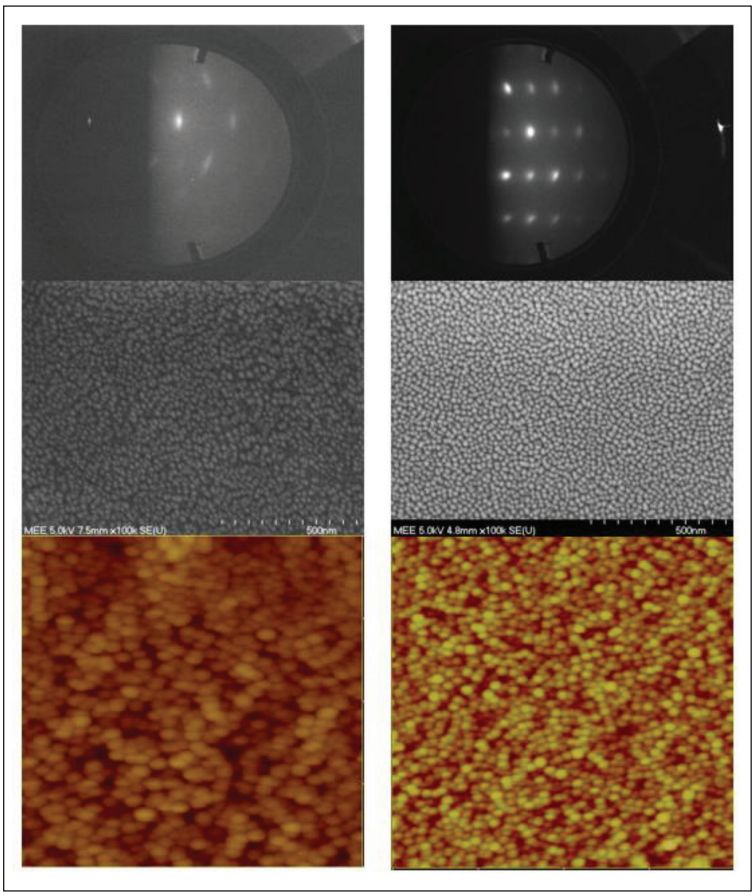
To address the notoriously low vapour pressure of scandium precursors, we have developed a fully integrated high-temperature delivery module for our Agilis platforms. This module couples a dedicated, heat-traced gas panel – it's capable of maintaining precursor lines, mass-flow controllers, and valves at up to 150 °C – with our third-generation CIS, which features coolant channels and a flange rated for sustained operation above 130 °C. Strengths of this combination include the elimination of cold spots, preventing precursor condensation, and the delivery of a stable, perfectly metered scandium flux directly into the growth zone.

During development of this AlScN platform, we utilised extensive engineering prototyping to optimise the CIS showerhead for high-temperature operation all while optimising the placement of custom heater assemblies that are fully insulated and that allow the process piping to be temperature zone controlled, which helps to enhance tight temperature uniformity of the process's gas along all lengths from bubbler to wafer carrier, all without altering the reactor's original gas-flow behaviour. As the CIS head is retro-fit compatible with legacy Agilis 100 and Agilis Mini tools, customers that have purchased those reactors are able to upgrade to high-temperature scandium delivery with no changes to existing recipes or hardware footprints – maintaining Agnitron's hallmark of seamless, future-proof MOCVD engineering.

Since October 2024, we have been playing a key role in a project focused on the MOCVD growth of ferroelectric AlScN films that's funded by the

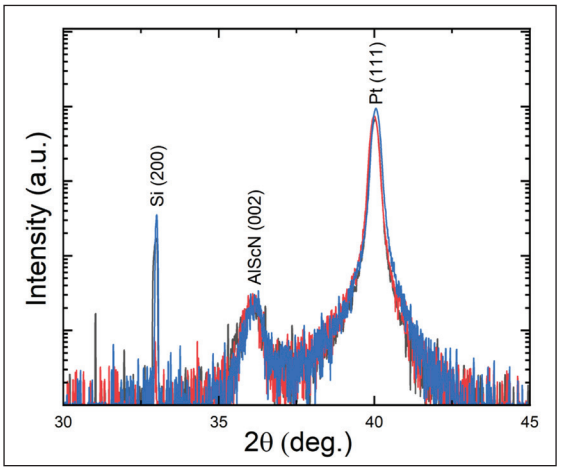


➤ Figure 7. Scandium composition in MOCVD-grown AlScN. Two representative samples are shown: one with a low scandium content of around 7 percent, measured with Rutherford backscattering spectrometry; and another with a high scandium content of around 45 percent, measured by energy dispersive X-ray spectroscopy. Both samples have a scandium composition variability of less than 5 percent over the diameter of the wafer, demonstrating effective control over scandium incorporation during growth.

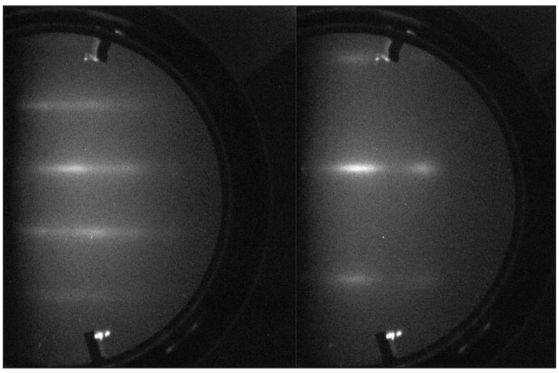


➤ Figure 8. A reflection high-energy electron diffraction pattern (top), scanning electron microscopy (middle), and atomic force microscopy (bottom) images of AlScN films grown on platinum/TiOx/silicon (left) and conductive silicon (right) substrates.

AFRL Regional Network-Midwest Hub. This effort includes the growth and characterisation of AlScN films on both platinum/silicon and silicon substrates. The resulting material systems are candidates for metal-ferroelectric-metal and metal-ferroelectric-semiconductor capacitor structures. As part of this project, test structures are being evaluated for their ferroelectric properties to gauge their potential for use in emerging high-temperature electronic and non-volatile memory applications.



➤ Figure 9. X-ray diffraction scan (2θ-ω) of AlScN/Pt/Si. Phase pure wurtzite structure is observed for all three samples.

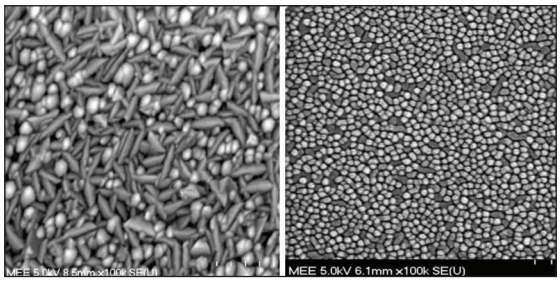


➤ Figure 10. Reflection high-energy electron diffraction pattens taken in two orientations from the 2D AlScN film with 29 percent scandium.

Using Dockweiler Chemical's ASGARD scandium precursor, we have utilised our Agilis 100 reactor to achieve reproducible and stable deposition of monocrystalline, textured, and polycrystalline AlScN films with scandium contents of up to 38 percent, while maintaining the wurtzite structure.

We have been able to achieve scandium incorporations up to 47 percent, but this is for amorphous films with crystalline inclusions (see Figure 7). Our films of AlScN have been grown on silicon, platinum, and GaN-on-sapphire templates, enabling compatibility with capacitor and CMOS device architectures.

We have used a variety of techniques to characterise our AlScN films. The thickness variation is less than 1 percent over a 2-inch wafer, according to reflectivity measurements, and scandium composition variation is less than 5 percent, based on Rutherford backscattering spectrometry and energy dispersive X-ray spectroscopy (see Figure 7). For these films, the RMS surface roughness is below 2 nm, according to atomic force microscopy scans (see Figure 8). To confirm that our AlScN films with a scandium content ranging from 18 percent to around 38 percent are phase-pure wurtzite, we have investigated them with X-ray diffraction (see Figure 9) and reflection high-energy electron diffraction (see Figures 8 and 10). Our films have a uniform, fine-grained morphology, with no nodules or pinholes,



➤ Figure 11. High-resolution scanning electron microscopy images of AlScN on Pt/Si, displaying growth of a blend of oriented and misoriented grains (a) and fully oriented grains (b).

Testimonial from Dinusha Herath Mudiyanselage, Assistant Professor of Electrical Engineering at Texas State University

OVER the past five years I have worked extensively with Agnitron's Agilis 100 and Agilis Mini MOCVD systems in research and development settings. These tools offer state-of-the-art capabilities for growing oxide and nitride materials, and consistently delivering best-in-class performance and reliability.

At Iowa State University, I used the Agilis 100 system to grow high-quality Ga_2O_3 and AlGaO epitaxial layers with excellent morphological and electrical characteristics. More recently, at Arizona State University, we acquired both the Agilis 100 (oxide) and Agilis Mini (nitride) systems. I was closely involved in their installation, setup, and operation.

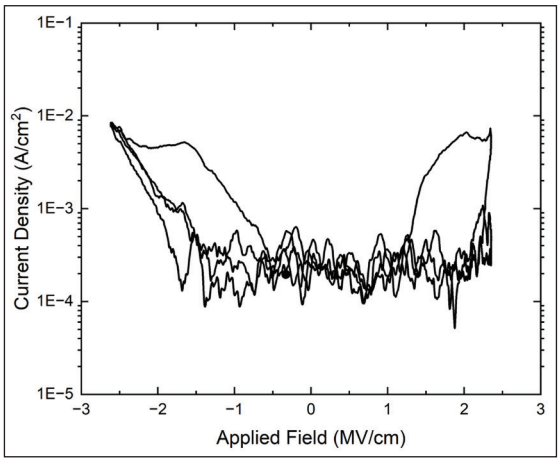
My work with Agnitron Technologies has spanned a wide range of materials – including Ga_2O_3, AlGaO, AlGaN, AlBN, AlScN, and AlN – grown using their systems. These epitaxial layers consistently exhibit high crystal quality (verified via X-ray diffraction and atomic force microscopy) and strong electrical performance. From these materials, I fabricated high-performance devices, such as Schottky barrier diodes, ferroelectric capacitors, and metal-semiconductor-metal structures.

Based on my experience, Agnitron's platforms continue to evolve and set a high bar for custom MOCVD technology. These systems are among the most advanced tools available in the US and globally for oxide and nitride semiconductor research.

Now, as I begin building my lab at Texas State University, I have selected the Agilis Mini system to support my group's work on wide and ultrawide bandgap semiconductors. This tool will be central to efforts to develop next-generation high-power and high-temperature electronic devices.

reducing the leakage risk in ferroelectric devices, according to high-resolution scanning electron microscopy images (see Figure 11). And according to reflection high-energy electron diffraction, by optimising the growth of AlScN, its growth mode is shifted from 3D to 2D (see Figures 8 and 10).

Undertaking this systematic study of key process variables – including growth temperature, nucleation strategies, ammonia and carrier gas flows, growth rates, and aluminium precursor selection – has allowed us to uncover strong correlations with surface morphology, crystalline quality, and roughness. The process conditions that are employed have a significant influence on grain size, density, and orientation, with variations clearly visible in scanning electron microscopy and atomic force microscopy measurements.



➤ Figure 12. Current density versus applied electric field for a 75 μm-diameter capacitor of AlScN/Pt/Si. Ferroelectric looping is observed at each end of the curve.

Testimonial from Chirag Gupta, Assistant Professor, Electrical and Computer Engineering, University of Wisconsin-Madison

OUR Ultra-Wide Bandgap MOCVD Laboratory, equipped with Agnitron's Agilis platform, serves as a unique testbed for our work on III-N-based ultra-wide bandgap semiconductors. This lab, led by Prof. Shubhra Pasayat, focuses on III-N research (both wide bandgap GaN, and ultra-wide bandgap AlGaN/AlN) and can also be utilised for Ga_2O_3 research. This offers a major advantage in a university setting where adaptability is key.

The system is stable at high temperatures and precise in gas handling. Students are already running it independently and producing high-quality materials for next-generation devices. Our researchers had previously collaborated with the Agnitron team on BN/AlGaN growth for an SBIR project that advanced into device fabrication. We look forward to continuing to evolve our system with the latest capabilities for defect management as we pursue new research directions.

We are thrilled to have recently celebrated the grand opening of this UW-Madison research facility, which provides a strong foundation for advanced semiconductor materials research.

To support the electrical evaluation of our AlScN films, we acquired a Radiant Technologies Precision Premier II-FE ferroelectric tester that's integrated with a probe station. Initial test structures, such as AlScN-on- Pt/Si films that are around 113 nm-thick, have demonstrated clear ferroelectric switching, with electric fields exceeding 2.6 MV cm^{-1} and low leakage in 75 μm-diameter capacitors (see Figure 12). These preliminary measurements indicate remnant polarisations of

about 10 μC cm^{-2}. We are now testing other devices, fabricated from films with various morphologies on platinum and heavily-doped *n*-type silicon substrates.

Our work with AlScN, aluminium-rich AlGaN and AlN is helping to advance the quality and capability of these materials. Thanks to our growth tools, the tremendous promise of this subset of nitrides is now a significant closer to fulfilling its potential.

The AlN/AlGaN work discussed is supported by the Defense Advanced Research Projects Agency (DARPA) under Contract No.140D0424C0048. The AlScN work discussed was funded by the Air Force Regional Network - Midwest hub, Contract number FA8750-22-2-0501, under the direction of Dr. Ahmad Islam of the Air Force Research Laboratory AFRL, Sensors Directorate. Agnitron also acknowledges Capt. Guillermo Salcedo from the Air Force Institute of Technology for his collaboration and assistance, as well as Prof. Travis Anderson of the University of Florida, for measuring and confirming our data through Hall measurements.. The views, opinions, and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

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Swansea's superpower: The Centre for Integrative Semiconductor Materials

Buoyed by the emergence of Vishay Intertechnology within the South Wales compound semiconductor cluster, Swansea University's recently constructed Centre for Integrative Semiconductor Materials (CISM) is focusing on power electronics while encompassing a broader portfolio of activities that includes CdTe solar cells and molecular electronics

RICHARD STEVENSON INTERVIEWS CISM'S OWEN GUY, MIKE JENNINGS AND DAN LAMB

RS: In 2023, you opened the Centre for Integrative Semiconductor Materials. What does this choice of name reflect? And in particular, what's meant by integrative?

OG: The concept of CSIM is to explore and develop multiple materials and technology sets. In particular, we are looking at silicon carbide, gallium oxide, gallium nitride and some of the newer thin-film technologies, which might be known as organic semiconductors.

The integrative aspect is to potentially integrate or hybridise some of those technologies.

I think the integrative name also applies to the integrative nature of what we do here in the cluster, very much supporting each other, including our industry partners. That's in terms of technologies, research and development of processes, and also in terms of the education and skills landscape.

RS: Where did the idea for this marvellous purpose-built fab come from? And who are the trailblazers?

OG: It really stemmed from Paul Meredith coming back to Wales. He was out in Australia for many years, but he came back to Swansea, and then the initiative for CISM really started in earnest. There'd

been a lot of activity in semiconductors previously, but Paul galvanised that.

This activity coincided with Wyn Meredith, Paul's brother, coming back to Wales from Scotland. They had the vision of forming this centre at Swansea.

SPTS, now KLA, and Microchip, and the Newport Wafer Fab that's now Vishay, had historically collaborated very closely with Swansea on various projects. CISM takes that to the next level.

RS: Prior to the launch of CISM, what were the semiconductor-related efforts that took place at Swansea University?

OG: They go back many, many years. Ken Board, who our boardroom is named after and includes his portrait, is historically a big name in the field; and Mike Jennings and I were involved in work on silicon carbide 20 years ago as part of Phil Mawby's group, Phil is now at Warwick. There's also surface science activity at Swansea, and work on metal semiconductor contacts stemming back to Robin Williams and Steve Wilks.

More recently I've worked with SPTS, now KLA, for over 20 years, and I've worked with the Newport Wafer Fab in some capacity for about 20 years. We've had very close relationships with IQE over a similar period. In fact, all those three companies were involved in a Department of Trade and Industry (now Innovate UK) project together 20 years ago.

RS: Since the launch of this centre, who are the leaders you've attracted and retained?

OG: Mike Jennings, who has moved from Warwick University, has had a massive influence in leading power device technology. We also brought in Dave Richie from Cambridge University. We brought in young talent like Emyrs Evans, who came from Richard Friend's Group in Cambridge.

We've been quite lucky also in bringing key industry people. I'm thinking of the likes of Simon Conway, who was previously one of the key guys at Pure Wafer, which sadly closed after the fire there. Simon has been one of the key instrumental people in getting the fab running here. And Gordon Horsburgh, formerly IQE, is playing a similar role. He's been extremely influential.

MJ: We've also appointed honorary academics from industry, mainly from within the cluster, such as Honorary Associate Professor, Dr Craig Fisher. We did a lot of work together on early silicon carbide rectifiers. You will frequently find him in Swansea's CISM, giving lectures and lending us his expertise. Vishay have also kindly sponsored a number PhD students here. And Dr. Huma Ashraf in a similar capacity with KLA.

RS: Space Forge has just taken residence at CSIM. What is its thinking behind this move? And what are you offering Space Forge, and how will you benefit from this development?

OG: They get the benefit of being in the same building as experts. We get the benefit of having a thriving company in the building, and the promotion, branding and all the publicity around that, which is brilliant. I know they're extremely supportive of CISM, and we're extremely supportive of what they're trying to do.

RS: Research in power electronics is a strong feature of CSIM. How much effort is being devoted to silicon carbide? And within that, what avenues are you exploring?

MJ: We've got the 'Driving the electric revolution, eight-inch Silicon Carbide pilot line'. We are the open-access facility for Silicon Carbide power device development in the UK. This is wrapped into a Royal Academy of Engineering fellowship sponsored by Vishay for the purpose of using

➤ The boardroom at CSIM includes a portrait of Ken Board, an emeritus professor at Swansea University in the department of electrical and electronic engineering. After graduating at Swansea in 1964, Board held a research post with Philips Research labs in Redhill, before taking an academic position at Swansea University as a lecturer, researching semiconductor devices and their technologies. As well as Ken Board and his family, those pictured in the boardroom include Swansea academic's Mike Jennings, Owen Guy, Paul Meredith, and Mohammed Darwish from Vishay.

Owen Guy

As well as being a member of CSIM, Owen Guy is Head of Chemistry at Swansea and Director of the Centre for Nanohealth in the College of Engineering at Swansea University. Guy's research background in SiC led to him developing the world's first epitaxial graphene biosensors in 2010 for detection of a cancer risk marker. He is pioneering the integration of biosensor chips, based on active nanostructure transducers, with microfluidics, and has developed silicon microneedle and microfluidics technology, collaborating closely with industry partner SPTS Technologies, now part of KLA.

that facility to aid industry in getting their power MOSFETs into production.

We're processing commercial wafers in this fab, right now. Much of it is simple, cleaning etc.., but there are also more advanced structures being investigated through other compatible processing, such as etching, metallisation and process module design. There's a lead time on equipment, so we are filling as many gaps as possible for our commercial partners.

It's also characterisation. The MOS interface in silicon carbide is problematic. Detailed characterisation requires a lot of data processing, physics equations and numerical methods. Our commercial partners send that activity to us. We'll characterise and send the results back, etc.

We are also supporting commercial activity on another form of silicon carbide – cubic silicon carbide to be exact. I've got history in cubic silicon carbide, due to an €8 million EU project, which started in 2017, led by STM.

We've also got process development, which we've been doing in collaboration with KLA and also Vishay, particularly on rounded trenches, corners, and silicon carbide dicing. And the other side of KLA, on metrology and defect characterisation, because there are still lots of defects in silicon carbide, and progress to be made on that front.

➤ There is substantial cleanroom space within CSIM, with suite of tools that can process epiwafers into devices, as well as extensive characterisation equipment.

I think the most exciting work we're doing is on plasma dicing with KLA. This won best poster at ICSCRM, 2024. We've got a lot of interest in that for obvious reasons, improving yield and die strength. It's not perfect yet. There's more work to do, but that's got real mileage.

We have a dedicated power lab for the characterisation and long-term reliability testing of packaged silicon carbide parts. We work with numerous commercial partners on the testing side. Large commercial entities obviously have their own bespoke instrumentation for this purpose, but what you find is that the large IDMs use all of their instrumentation for product. They are not set up for R&D. They don't have the capacity, and they don't have the flexibility either, so they come to the likes of us.

If you buy a reliability tester, it's off the shelf. It'll do 80 percent of the rated voltage for a thousand hours with humidity and that's it. It'll just tell you when its failed. But with our kit, we can programme our own voltage-ramping recipe, be very flexible with the temperature, voltage and humidity control. If requested, we can go above the rated breakdown voltage. We can do whatever test they want, within reason, and monitor the current and the failure mechanism.

RS: There is a lot of interest in GaN for power electronics. Do you have programmes in that area?

MJ: We work very closely with processing experts at Vishay Intertechnology on GaN. Being a power electronics guy, I want to see if GaN is limited to a maximum of three kilowatts. The main market is laptop charges, but can you get a GaN device to work at higher voltages, higher currents, higher temperatures, higher power?

We're looking at vertical gallium nitride. When it's lateral, when you go up in voltage, you have to make the die larger. Therefore, you have problems with yield, and it becomes commercially unviable beyond about 650 volts. We're looking to scale up vertically, like you would a classic silicon carbide power MOSFET, and use a MOS interface. You lose some good properties, but you may be able to increase the power level.

We're looking at HEMT technology as well. We've got interesting ideas on how to keep the die the same size, but increase the voltage rating.

RS: You have also commissioned a reaction for gallium oxide. Tell me about the gallium oxide efforts at CSIM.

DL: Yes, we were very fortunate to win EPSRC Strategic Equipment funding that enabled us to procure a state-of-the-art Aixtron close-coupled showerhead research reactor. The reactor can deposit a range of different semiconductor thin films, including gallium oxide and cadmium telluride. The reactor was delivered straight into a purpose designed laboratory, within CISM, and has been successfully depositing gallium oxide material since January this year. We have been providing lots of high-quality 2-inch and 4-inch gallium oxide thin films into Swansea-based research projects and the wider UK gallium oxide community.

MJ: There are a lot of challenges for gallium oxide, no question. Even with heterogeneous integration, if that's the correct term, growing diamond or nickel oxide above gallium oxide, the *p-n* junction voltage is still very high. With very-high-voltage devices, like silicon thyristors, you can get over one kiloamp conduction through a device with a one-volt drop across it. You can't even turn gallium oxide on, even with heterogeneous integration, until about three, four volts. So, how is that going to work? Our challenge is to overcome these problems, including the poor thermal properties. I was sceptical about silicon carbide as well, because I thought that its MOS channel is so poor. Turns out that one worked so who is to say that an answer will not be found for gallium oxide.

RS: You're also involved in a project associated with cadmium telluride solar cells for powering satellites. Can you explain the role you're playing here?

DL: 80 percent of the radiation-hard glass that protects space solar cells is made in North Wales by a company called Qioptiq Space Technology.

It's ultrathin glass, not much thicker than a human hair, laminated on top of most space solar cells. Here at Swansea University, we had the novel idea of making cadmium telluride film solar cells directly onto the space glass. That means huge weight savings – critical for space – and even the potential for flexible solar cells that pack more efficiently. CISM has an EPSRC-funded project that is using our Aixtron close-coupled showerhead metal organic chemical vapour deposition system to make each of the semiconductor layers directly onto the ultrathin glass.

Our team is aiming for a step-change reduction in the cost of space solar cells, opening the door to emerging space power applications that require low-cost, volume manufacturing and high-radiation stability.

RS: You're in the CS cluster. Do you think this centre would have been built were not for the cluster and the investment its generated?

OG: Definitely not. The cluster have been hugely financially supportive – and this centre was built to support the cluster. So it's been a mutual process throughout the whole timeline.

There was co-investment from SPTS KLA, from the Newport Wafer fab, and from IQE – £15 million each over 10 years, plus additional co-investment from other industry partners. That was instrumental in helping us obtain the grant funding for this building. They've been extremely supportive in the technologies that we›re developing or co-developing.

RS: And how valuable is it to have a power electronics chip manufacturer within the cluster?

MJ: Having a big chip maker like Vishay on the doorstep is very, very valuable for our research. And more than that, really, our mission is to see

➤ Recently CSIM installed an MOCVD reactor capable of the growth of gallium oxide epilayers on 4-inch substrates.

Mike Jennings

Mike Jennings gained his PhD from the University of Warwick where he spent 13 years working on power semiconductor technology. In 2019 he moved to Swansea University, recognising the scale and technology development opportunity provided by the South Wales Compound Semiconductor Cluster. He is Professor and Head of Energy and Power Engineering at Swansea University. Jennings holds a Royal Academy of Engineering Chair in 'Advanced Semiconductors for Electric Vehicle Drives', sponsored by Vishay Intertechnologies Ltd. His current projects include the design, processing and characterisation of silicon carbide, gallium nitride and gallium oxide power devices and the manufacturability of advanced silicon MOSFETs and IGBTs. Most recently, Jennings spends much of his time performing collaborative research internationally as well as across the South Wales Compound Semiconductor Cluster with a focus on growing the sector for future generations.

Dan Lamb

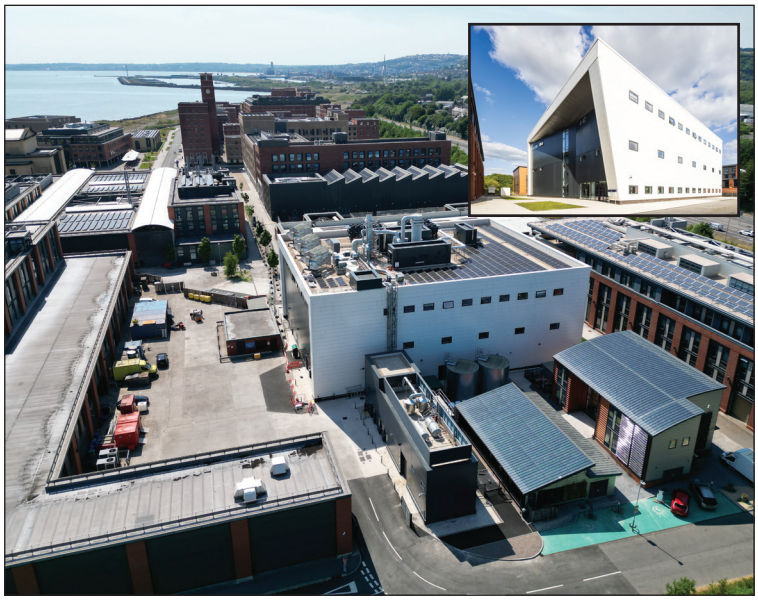
Dan Lamb leads a Swansea University research group specialising in MOCVD of oxide and chalcogenide thin films, with expertise in gallium oxide and cadmium telluride. Based in the CISM, the group operates an EPSRC-funded Aixtron CCS MOCVD system for 2-inch and 4-inch wafers. Lamb's research advances power electronics, deep-UV photodetectors, transparent conductive oxides, and CdTe photovoltaics for space applications. His team captured the first in-orbit performance data for CdTe solar cells via the AlSat-Nano mission, and actively collaborates with academic and industrial partners.

the cluster grow and, to some extent, move on from silicon. If you've got a fab now, if you're only doing silicon power chips, which is what they do in Newport, it's going to be very, very difficult to be competitive longer term, particularly at 8-inch. So it's great to see that they are diversifying their product portfolio, because you need to be able to turn your hand to silicon carbide, to gallium nitride.

RS: And the other partners in the cluster, like Microchip and IQE. What are the mutual benefits you're getting there?

OG: IQE we've worked historically with for over 20 years. They supply materials to projects, which is hugely valuable. We've worked with them on solar technologies in the past.

MJ: IQE through their subsidiary company, Compound Semiconductor Centre Ltd, are developers of GaN epiwafers. It is mutually beneficial for us to prove out their material via our GaN device processes here at CISM. As you can imagine, this relationship has formed the basis of many UKRI funded projects together.



➤ The CSIM facility is part of the Swansea Bay campus, which is home to Engineering, the School of Management and the Computational Foundry, as well as student accommodation with direct access to the beach. Inset: The £50 million CISM facility on Swansea University's Bay Campus officially opened in 2023.

Microchip's activity within our region is power-electronics packaging. Obviously, they're a device manufacturer within their own rights, but their device-manufacturing activities are in the United States. We don't have a strong packaging activity at Swansea University. We mainly focus on device fabrication technologies, and test at the die level and package level. Having a partner like Microchip is very, very important, because sometimes you do need to package chips effectively for advanced testing strategies.

RS: All clusters have strengths and weaknesses. You could argue that optoelectronics is, in relative terms, a weakness within the cluster, as there isn't the equivalent of a Vishay to provide volume production. Do you think that in time, this would be a good thing to address?

MJ: I'm not so sure, but I'm definitely going to be biassed. The site in Newport, now Vishay, and Microchip to some extent, have worked in power management for the majority of their existence. The cluster is geared up for power technology, in my view. Furthermore, compound semiconductor power technology is an excellent entry-level activity in order to grow a commercial semiconductor cluster in the first instance. Why? It is high volume, provides plenty of jobs, has a high figure for gross value added, and only requires a 0.18 micron fab capability, unlike a quantum, memory, GPU or VLSI facility, and is therefore cheaper. Old silicon fabs and tooling can be used with little additional investment. Innovation and novelty originate from processing new wide bandgap materials at relatively lower costs compared to a 3-nanometre node at the likes of TSMC. Of course, power technologies are self-perpetuating, feeding into more-efficient power supplies and industrial drives, such as data centres and future fabs, through higher energy efficiency, helping the quest for net zero. Wide bandgap power electronic device development as a commercial activity is a no brainer, isn't it?

I think we should focus on our strength, I think we should focus on power, as simple as that. Sensors can be integrated into the power domain, but for me, the flagship activity is wide bandgap power electronic devices.

OG: Mike's right, the flagship activity should be power. But there is room for some other activities at a lower priority level. Within the cluster, we've worked on a collaborative project with IQE, CSC, and Cardiff University, developing VCSEL technology, but the majority of that project was done at Cardiff.

RS: Over the remainder of this decade, how are you expecting CISM to evolve?

OG: We're very closely aligned with our industrial partners, and there are huge expansion plans with Vishay and KLA in particular. There will undoubtedly be a big focus on silicon carbide technology, on gallium nitride technology. A lot of that will be going into automotive, but I think expanding into other applications, such as offshore wind, and the supply chain related to that.

There's also Paul Meredith's activity on molecular semiconductors and films, and our work on molecular deposition technologies. These are exciting materials technologies, which can be applied to displays, thin-film solar, and probably applications we might not even have thought of.

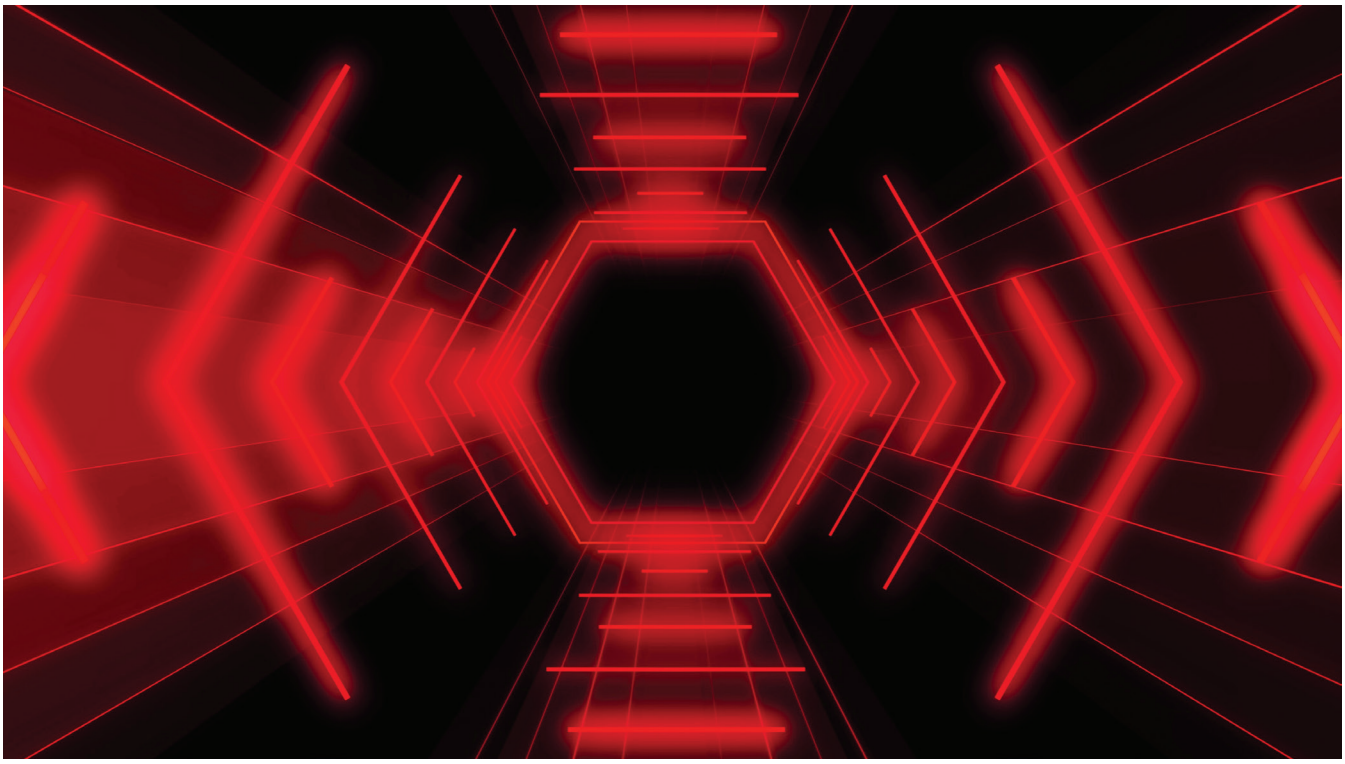
Another area is artificial intelligence, and the integration of computer science into some of the stuff we're doing, as a tool. That's quite exciting.

Advanced packaging, 3D packaging, is another interesting technique for us. We might see that evolve and translate into medical sensing technologies. We are working on utilising some technologies for biosensing applications.

MJ: Having Cadence come into the region, we'll focus on IC design. They are interested in IC design on compounds. That will help us with this more integration approach.

We run campaigns, GaN campaigns, silicon carbide campaigns. It's not only about demonstrating the devices – this is a fab of the future. What's a fab going to look like in the future, in order to be able to run all of these in one facility? They face these issues in fabs all over the world. If you're a commercial fab that's thinking about wide bandgap materials longer term, how are you going to do all this in the same fab? Imagine having to process lots of different materials, processes with one material process, potentially harming another material. It's a whole philosophy of how you run a facility, which is really interesting.

One of the key milestones on the horizon is ICSCRM 2027, which we'll be hosting here in the UK for the very first time, in Newport. That's a major international conference for silicon carbide and related materials, and a real opportunity to showcase what's happening not just at CISM but across the cluster and the wider UK. We were proud to present award-winning work at ICSCRM 2024 and bringing the global SiC and wide bandgap community here really puts South Wales on the map.



The race to revolutionise silicon photonics with seamless III-V integration

Growing III-V nano-ridge lasers directly on silicon sidesteps the complexities of existing integration methods and paves the way for scalable, cost-efficient photonic integrated circuit production

BY BERNARDETTE KUNERT AND JORIS VAN CAMPENHOUT FROM IMEC

IN TODAY'S data-driven world, the demand for faster and more efficient data computation and transmission is growing at an unprecedented pace. On top of the everyday expectation of instant access to high-resolution images, seamless video streaming, and immersive augmented reality experiences, the rapid expansion of AI and machine learning introduces even greater challenges. These technologies rely on massive volumes of machine-to-machine data exchange, further amplifying the need for high-speed, low-latency communication.

To keep up with these demands, optical data transmission must extend beyond traditional long-haul networks, moving closer to the chip level. This has implications for fibre-to-the-x deployments and chip-to-chip optical interconnects, in which ultra-fast, low-power data transfer is becoming increasingly critical. As data volumes continue to surge, innovative solutions to optimise transmission efficiency are paramount. A particular focus is reducing power consumption per transmitted bit to ensure computing infrastructure is both scalable and sustainable.

One key technology in this transformation is silicon photonics, which leverages the well-established CMOS fabrication process to enable large-scale production of optical systems.

However, a longstanding barrier to the full-scale deployment of silicon photonic integrated circuits (PICs) is that they lack one critical element: the light source. Due to its inherent material limitations, silicon cannot efficiently emit light. The industry has so far filled this gap by using III-V compound semiconductors – materials prized for their exceptional optoelectronic properties. But integrating these crystalline materials into silicon photonics has proven to be a formidable engineering challenge.

For this reason, most datacom products currently rely on III-V light sources that are separately processed on native III-V substrates and later attached to silicon photonic chips using micro-mounted laser packages or high-precision flip-chip assembly techniques. While these hybrid integration approaches are effective, they are also costly and tricky to scale, making PIC devices an expensive, low-volume solution.

To address this, the industry is exploring alternative integration methods. For example, micro-transfer printing, a back-end-of-line technique, involves the parallel transfer of prefabricated III-V components onto silicon photonic wafers, significantly improving throughput. Another heterogeneous integration approach employs die-to-wafer bonding of unprocessed III-V device chips onto silicon photonic wafers, followed by III-V device patterning and CMOS-based back-end-of-line metal interconnect formation.

The latter method has gained commercial traction and is now available in at least two commercial manufacturing lines. Yet its dependence on complex bonding techniques and expensive III-V substrates remains a bottleneck. Additionally, the substrates are discarded as waste during the manufacturing process, raising concerns about health, safety, and environmental sustainability.

The ultimate goal is the direct monolithic growth of III-V materials on silicon wafers, which would eliminate the need for external III-V substrates and intricate assembly processes. However, silicon and III-V materials have significant differences in their lattice structures, leading to strain in the III-V layers during this monolithic growth. When this strain releases, it leads to defects such as misfit and threading dislocations forming in the III-V film during deposition. These crystal defects do not just appear at the interface with silicon, but also penetrate the entire device stack, degrading its performance and rendering it commercially unusable.

Nano-ridge engineering

For decades, researchers have worked to control the inevitable strain release and block the propagation of dislocation defects through the device stack to the active layers. Some of the techniques explored include growing very thick transition buffers between the silicon and III-V, employing annealing treatments to fix some of the defects, and adding strained superlattice layers to control and isolate defects, accommodating them while limiting their wider propagation. However, these approaches have met with limited success.

A game-changing development emerged with the successful demonstration of InAs quantum dot lasers monolithically grown on silicon. These zero-dimensional nanostructures confine charge carriers, the electrons and holes, more tightly than the more common quantum wells, in which carriers can move in two dimensions. Electrons and holes in quantum dots are therefore less likely to encounter defects, meaning that quantum-dot structures exhibit greater defect tolerance than traditional lasers based on multi-quantum well gain regions. Thanks to these properties, quantum-dot lasers have achieved reliability levels that make them a promising technology for future PIC applications.

One fabrication method that has driven recent advancements in monolithic growth and in integrated photonics more broadly, is selective-area growth (SAG). This technique allows the deposition of III-V material exclusively within predefined silicon oxide patterns, minimising the need for extensive material removal during fabrication, and making the process more efficient than conventional two-dimensional growth. SAG can also leverage aspect ratio trapping (ART), which involves creating deep features that can trap relaxation defects and suppress their propagation through the device. Since only selected regions of the silicon substrate are overgrown, rather than the whole surface, this approach also reduces strain and mitigates common challenges, including crack formation and silicon wafer warpage.

Yet, despite these advantages, SAG based on ART has a drawback; the narrow deposition patterns that are critical for effective defect reduction also limit the amount of III-V material that can be integrated. This constraint restricts the range of devices that can be realised.

Enter nano-ridge engineering (NRE), a cutting-edge integration approach

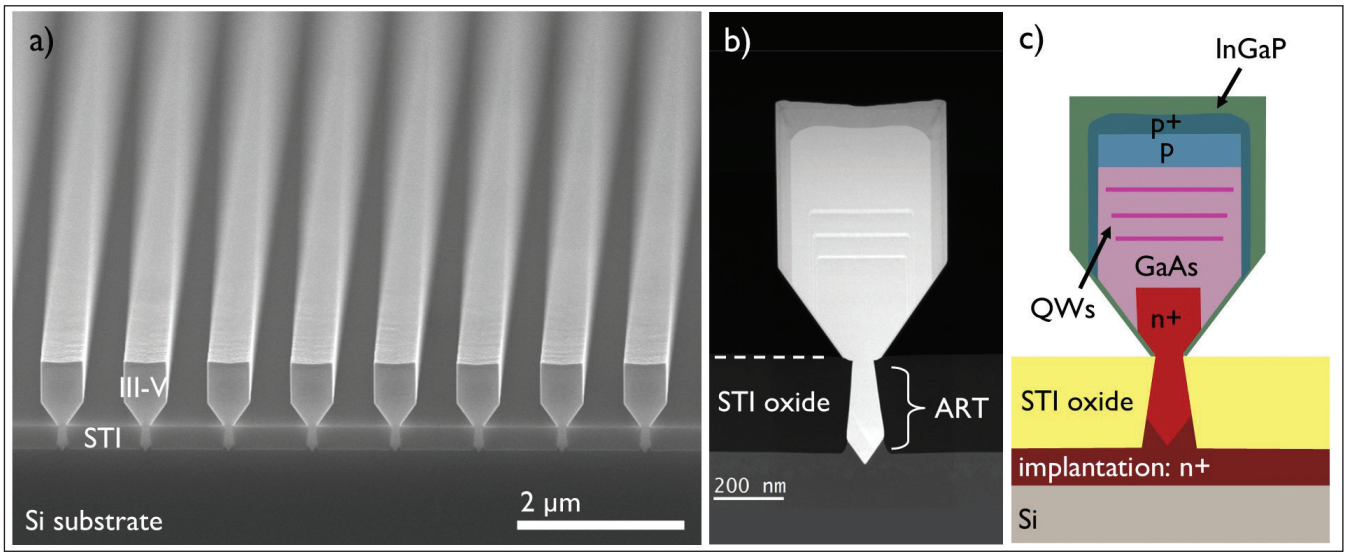


Figure 1. (a) Scanning electron microscope image of a III-V nano-ridge array grown by MOCVD on a 300 mm patterned silicon dioxide/silicon wafer. The oxide pattern was fabricated by applying a shallow trench isolation (STI) process. (b) High-angle annular dark-field scanning transmission electron microscope image of a III-V nano-ridge laser in cross-section highlighting the different III-V material systems. (c) Schematic of the nano-ridge device stack (QW: quantum well; n^+: highly *n*-doped region; p: *p*-doped region; p^+: highly *p*-doped region).

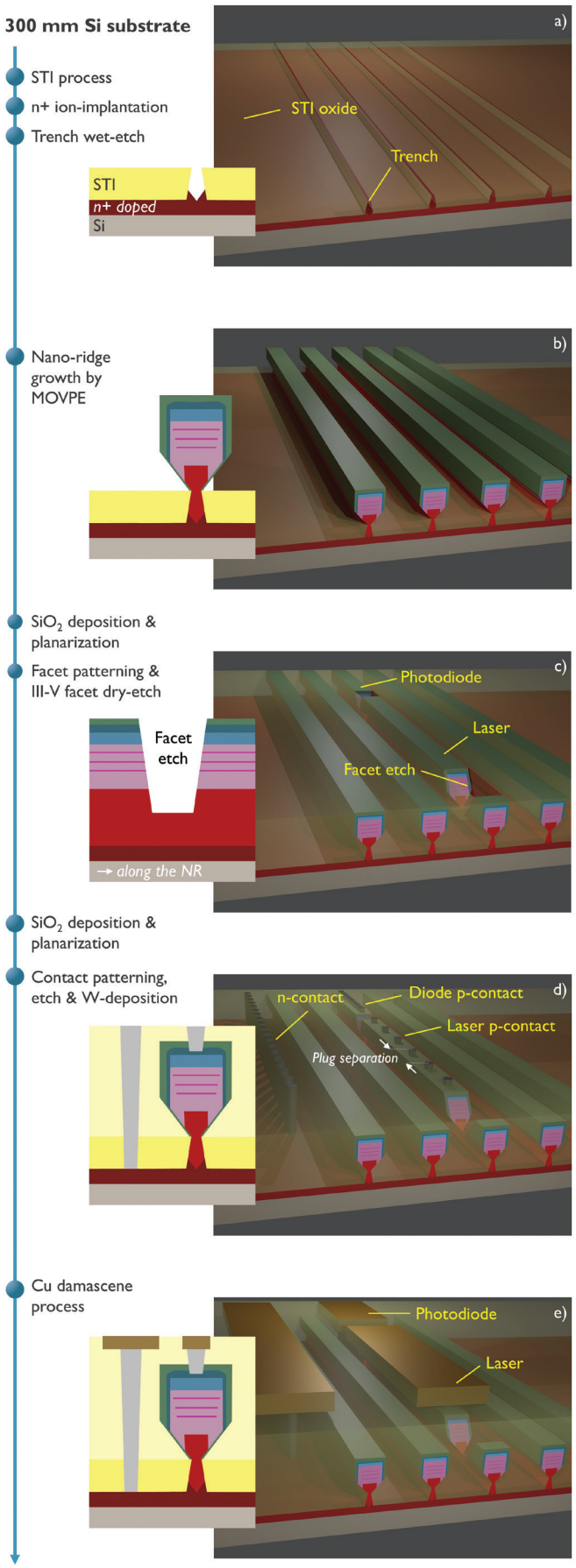
pioneered by imec. By refining SAG with MOCVD – the preferred deposition technique to achieve selectivity – and enhancing ART through the use of very narrow, elongated trenches, NRE enables efficient defect suppression while significantly increasing the volume of usable III-V material. This is achieved through continuous growth beyond the trench pattern and carefully controlled nano-ridge shape engineering.

This breakthrough not only expands the design possibilities for III-V-based devices, but also redefines their functionality. The nano-ridge itself can serve as a waveguide in optoelectronic components, such as light-emitting diodes, lasers, modulators, and photodetectors. Additionally, when multiple nano-ridges are contacted in parallel, they can provide sufficient current to power a heterojunction bipolar transistor – a type of transistor that is often used as a power amplifier in RF communications.

Imec's recent milestone – the demonstration of nano-ridge lasers fully processed on 300 mm silicon in a CMOS prototyping line – marks a major step toward scalable, cost-efficient, and environmentally sustainable integration of high-quality III-V devices on silicon.

Fabrication challenges

To make this vision a reality, imec's researchers had to overcome three major hurdles. The first challenge was ensuring defect-free nano-ridge growth on 300 mm silicon substrates. ART has been proven effective in reducing misfit defects across various material systems, particularly for GaAs inside narrow trenches. However, for this approach to work, complete strain relaxation must occur within these trenches before uniform nano-ridge growth can extend beyond them. To achieve this, the imec team optimised the MOCVD conditions to facilitate efficient strain release at the III-V/silicon interface and gliding of the threading dislocation inside the trench.



III-V nano-ridge laser diode + read-out photodiode

➤ Figure 2. Simplified schematic of the 300 mm process flow executed in imec's CMOS prototyping line (W: tungsten; Cu: copper). For more details see Y. D. Konick et al. Nature **637** 63 (2025)

Once a uniform *n*-doped GaAs base-ridge was established, we grew an InGaAs/GaAs multi-quantum well stack to serve as the laser's optical gain medium, followed by a *p*-doped GaAs contact layer. We then capped the final nano-ridge waveguide with an InGaP layer to enhance carrier confinement and to reduce carrier losses at the III-V surface (see Figure 1).

Measurements of the unprocessed nano-ridges (using cathodoluminescence techniques) confirmed an impressively low density of misfit defects – fewer than 6 x 10^4 per cm^2 – in the nano-ridge waveguide. This is a remarkable achievement for such a thin III-V stack.

The second challenge was designing a low-loss contact approach. It was relatively straightforward to perform electron injection via a silicon layer implanted with n^+ ions and the *n*-doped GaAs inside the trench. However, establishing a robust *p*-contact on top of the nano-ridge proved more difficult. Using a continuous metal stripe on top of the nano-ridge would have led to excessive optical losses. Instead, we distributed isolated *p*-plugs along the nano-ridge.

To enable efficient hole injection, these metal plugs were selectively punched through the InGaP layer to reach the *p*-doped GaAs. This periodic *p*-contact design introduced a unique beating-mode formation, supporting discrete waveguide modes with minimised overlap with the metal plug array – a phenomenon that also supported single-mode laser operation. To create the Fabry-Pérot laser cavity, we etched facets into the nano-ridge using a dry-etch process.

Finally, integrating and processing III-V materials within a CMOS prototyping line presented an additional set of challenges. Most semiconductor manufacturing tools are not designed to handle III-V materials, or even tolerate the risk of contamination from III-V traces on 300 mm silicon wafers. Furthermore, we had to develop many of the necessary fabrication processes from scratch. To do this, we leveraged imec's extensive expertise in III-V material processing, establishing a controlled manufacturing environment tailored to accommodate these non-standard CMOS materials.

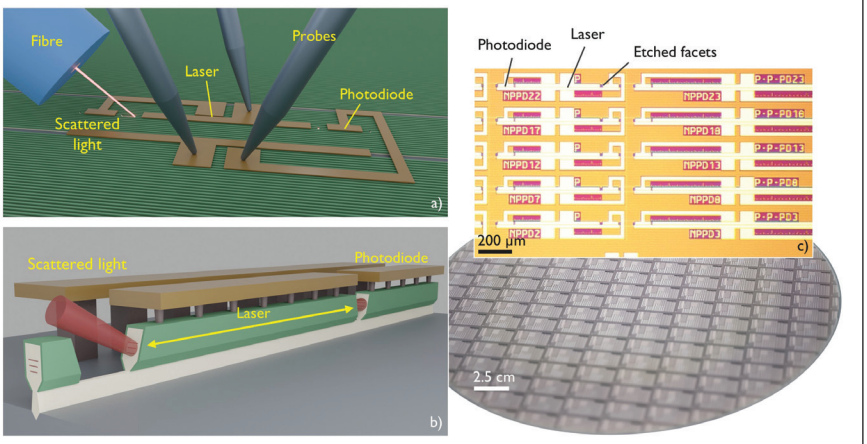


Figure 3. (a) Schematic of the wafer-scale readout test setup: light scattered upwards from the left facet can be collected by a multimode fibre. The three electrical probes drive the nano-ridge laser and photodiode. (b) Schematic (ignoring the oxide) of the nano-ridge cavity formed by two etched facets with an inline photodiode collecting light emitted from the right laser facet, while the light from the left facet is scattered. (c) An optical top-view image of processed devices. A photo of a completely processed 300 mm wafer is shown in the background.

In light of the inherent uncertainties associated with novel sequential process steps and device operability, we devised a mask layout that incorporated a diverse set of physical device parameters. This included variations in laser cavity lengths, pattern trench widths, and *p*-plug separations to systematically assess their impact on device functionality and increase the probability of a successful demonstration.

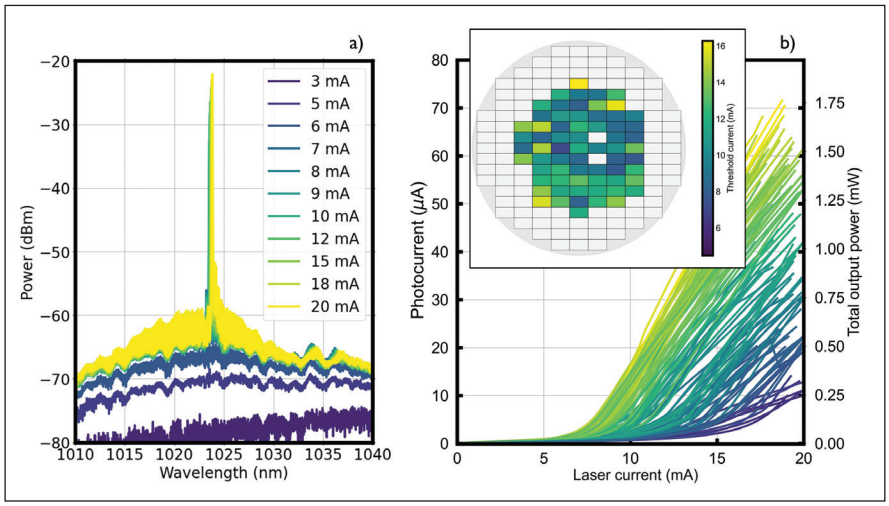
To enable rapid, wafer-scale characterisation of these nano-ridge laser devices, we introduced an innovative approach: integrating a nano-ridge photodetector in line with the laser. This coupled device layout provides an elegant and efficient method for obtaining wafer-scale performance statistics, ensuring a comprehensive evaluation of device operation across the wafer. Further details on the 300 mm process flow and measurement configuration are provided in Figures 2 and 3.

Nano-ridge lasers

Leveraging the wafer-scale fabrication, we put thousands of GaAs nano-ridge devices – including lasers, photodetectors, and test structures – to readout test, as shown in Figure 3. The results were highly promising: over 300 functional nano-ridge lasers exhibited emission at approximately 1025 nm at room temperature, as evidenced by a clear threshold behaviour in the photodiode current (see Figure 4).

This milestone is particularly noteworthy considering the challenges of pioneering a completely new 300 mm process flow. Risks such as short circuits, imperfect facet quality, and high contact resistivity could easily have hindered performance. Instead, these findings mark a major step forward, proving that nano-ridge lasers can be reliably fabricated at scale, and bringing III-V integration on silicon closer to real-world applications.

To validate these findings, we conducted additional measurements, including wafer-scale measurements detecting radiated laser light from the top of the wafer, as well as die-level analysis, for example of the emission spectra from cleaved facets of diced wafers. These tests confirmed the laser operation, revealing a threshold current as low as 5 mA, a slope efficiency of up to 0.5 W A^{-1}, and a maximum total output power of 1.75 mW. These are encouraging values, given the nano-ridge's sub-micrometre cross-section. Furthermore, the periodic grating structure formed by the *p*-contact plugs played a crucial role in stabilising single-mode operation in the Fabry-Pérot resonator, achieving a side-mode suppression ratio exceeding 30 dB.



➤ Figure 4. (a) Optical output spectra collected at a cleaved facet of a 1.4 mm-long laser cavity with an optical fibre for different drive currents. (b) Photodiode current (left) and related total output power (right) versus the laser drive current of a 2 mm-long device. The inset shows a wafer map of the die distribution containing the operational 2 mm-long laser devices. The colour code indicates the corresponding threshold current.

A particularly notable observation is that lasing occurred only in devices where the *p*-plug separation exceeded 3 μm, highlighting that, if the plug density is too high, the absorption losses in the top metal contacts have a significant impact on the laser threshold.

However, increasing the *p*-plug separation introduced a device performance trade-off as it also led to higher current densities at each contact point. While initial reliability tests showed continuous-wave lasing for over 500 hours, further investigation revealed that the high current density at the *p*-plugs induced localised defects, ultimately leading to device failure.

A more promising observation was that, aside from the region surrounding the *p*-plugs, the rest of the nano-ridge waveguide retained high crystalline quality, with no additional misfit defects forming. This finding suggests that further optimisation of the contact design could significantly enhance the long-term reliability of these nano-ridge lasers, paving the way for silicon photonics applications.

Future focus

To the best of our knowledge, this demonstration marks the first successful realisation of a fully processed III-V nano-ridge laser on a 300 mm silicon wafer. By enabling monolithic III-V deposition directly onto silicon, this approach eliminates the dependence on III-V substrates and complex bonding techniques, leveraging the advanced fabrication capabilities of a CMOS pilot line. This breakthrough is pivotal in facilitating high-volume scalability, improved yield, and reduced production costs – key factors for the widespread adoption of silicon photonics. However, while this achievement represents a major milestone, the nano-ridge engineering technology remains in its early development phase.

This work is part of a broader pathfinding mission at imec to advance III-V integration processes towards higher technological maturity. In the near term, the focus remains on hybrid approaches, such as flip-chip assembly and transfer printing. In the mid-term, we expect heterogeneous methods based on die-bonding techniques to further enhance integration efficiency. Ultimately, the long-term goal is to achieve direct epitaxial growth of III-V materials on silicon – a concept that this work demonstrates is possible.

Current R&D efforts in our NRE technology focus on refining the contact approach to mitigate localised high-current injection spots, thereby extending device lifetime. Additionally, we are investigating alternative GaAs-based optical gain media to red-shift the laser emission wavelength, expanding the potential range of applications.

Another promising avenue involves leveraging the waveguide nature of III-V nano-ridges to enable efficient coupling into silicon photonic waveguides. This would open up the possibility of developing external cavity lasers, further enhancing the versatility of this platform.

Beyond device-level innovations, significant work remains to optimise fabrication processes and improve throughput. Achieving full-scale commercialisation will require close collaboration with semiconductor tool suppliers to improve processing techniques and ensure compatibility with existing CMOS manufacturing infrastructure. Encouragingly, ongoing global efforts in heterogeneous integration, combined with the growing importance of III-V process technologies in CMOS environments, are set to drive continuous improvements in tool capabilities and manufacturing efficiency.

By addressing these challenges, imec aims to accelerate the development of III-V-on-silicon lasers, bringing them closer to large-scale deployment in future-generation silicon photonics applications.

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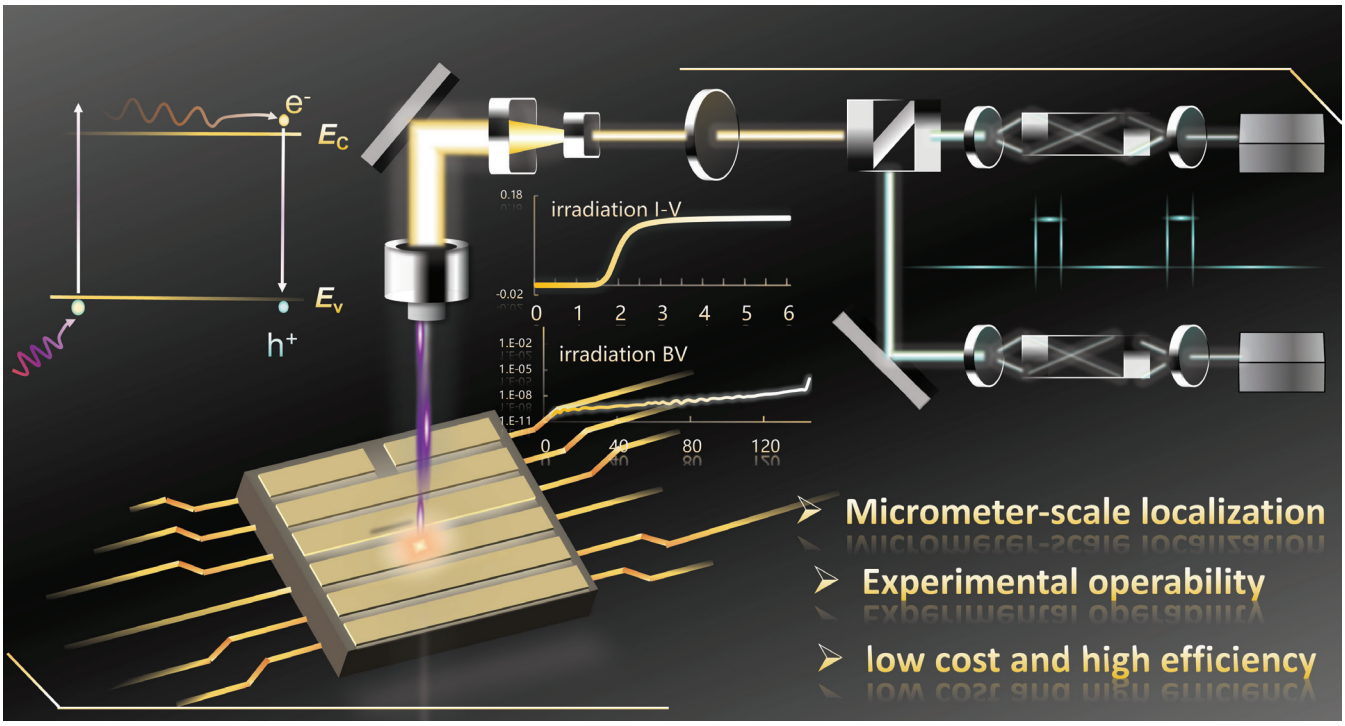


Evaluating radiation hardness with UV laser pulses

By delivering radiation-induced damage with a high spatial resolution, UV pulsed laser irradiation technology is providing a powerful approach for assessing GaN power electronics in space applications.

BY FENG ZHOU, MAI ZHANG, CAN ZOU AND HAI LU FROM NANJING UNIVERSITY

WITHIN the palette of compound semiconductors, GaN has emerged as a promising candidate for next-generation aerospace electronics, due to its superior material properties. Of those, arguably the most important is the high displacement threshold energy, which effectively suppresses irradiation displacement damage.

However, GaN-based power devices do have their weaknesses, suffering from pronounced susceptibility to single-event effects, induced by high-energy heavy ions that are prevalent in space. When these ions bombard semiconductor devices, high linear-energy transfer occurs, leading to single-event burnout that's triggered by ionisation effects and charge accumulation. This chain of events is a major issue, threatening to result in severe performance degradation and even catastrophic device failure.

Due to these severe concerns, it is critical to enhance the irradiation hardness of GaN power devices to single-event burnout. Unfortunately, that's not a straightforward task, as irradiation experiments primarily rely on heavy-ion accelerators, which suffer from prolonged experimental cycles, exorbitant costs, and inherent limitations in achieving precisely localised irradiation and dynamic *in-situ* testing. Consequently, it is imperative to develop a cost-effective test system with a high spatial resolution that's capable of supporting both static and dynamic irradiation experiments.

The good news is that pulsed laser irradiation produces similar conditions to heavy-ion irradiation. The latter induces single-event effects via particle-scattering-generated electron-hole pairs, while pulsed laser irradiation generates electron-hole pairs through the photoelectric effect. Note that pulsed laser irradiation offers a number of distinct advantages over heavy-ion irradiation, including precise spatial control of the incident position, extended operational duration, superior experimental reproducibility, and cost-effectiveness. Thanks to these merits, pulsed laser irradiation is a viable method for simulating single-event effects induced by heavy ions, and enables the establishment of correlations between heavy ions and the pulsed source. With pulsed laser irradiation, the two main physical mechanisms used to simulate

Institution	Laser Wavelength	Laser Spot Diameter	SPA/TPA/3PA
CNRS	1030 nm	1 µm	3PA
University of Bordeaux	481nm	1µm	2PA
NRL	293nm	0.32µm	SPA
	630nm	1µm	2PA
NSSC	620nm	1µm	2PA
Nanjing University	266 nm	<1µm	SPA

➤ Table 1: Summary of pulse laser irradiation experimental system. SPA, TPA and 3PA are short for single-photon, two-photon and three-photon absorption, respectively.

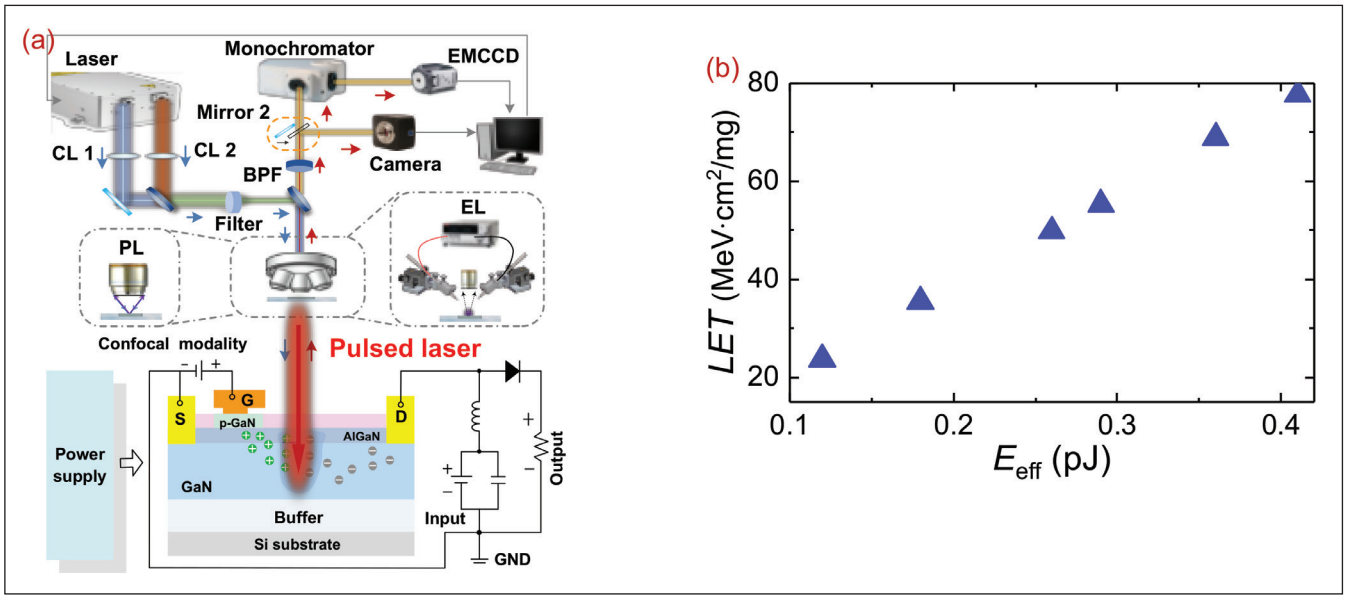
single-event effects are single-photon absorption and two-photon absorption.

One photon or two?

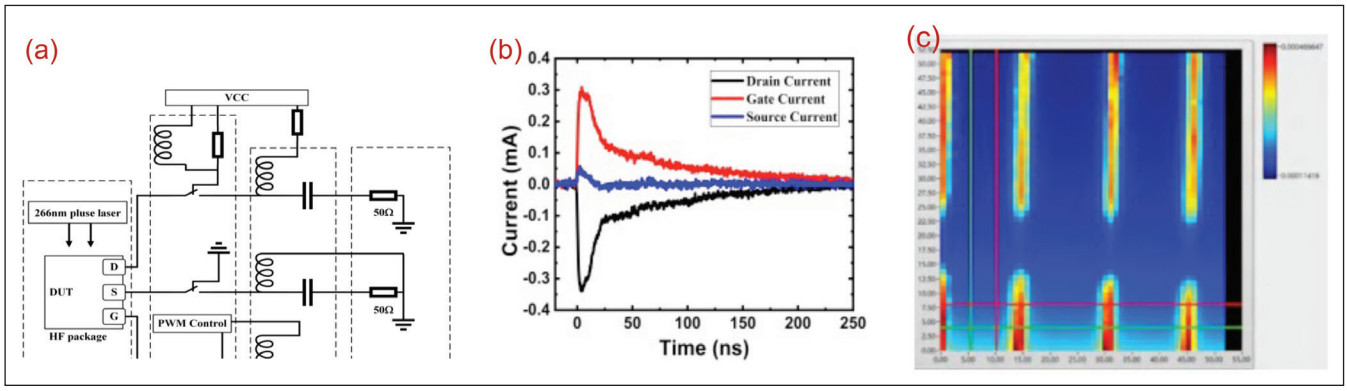
For irradiation investigations using single-photon absorption, one must employ a laser with an energy higher than the bandgap of the device. As each absorbed photon generates an electron-hole pair, the pulsed laser source can induce carrier generation in a micron-scale area of the device under test. Thanks to these conditions, researchers can realise a high accuracy and a high test-efficiency, enabling high matching with heavy ion irradiation.

A key difference with two-photon absorption is that as the laser energy is beneath the material bandgap, almost no carriers are generated at low light intensity. Switching to a high light intensity addresses this issue, so long as the light is strongly focused, enabling two-photon absorption in the material that leads to the generation of electron-hole pairs (the principle of three-photon absorption or four-photon absorption is similar to two-photon absorption). Note that efforts based on the absorption of multiple photons are better suited to devices covered with thick metals, or those requiring the optical source to be directed to the backside.

Today, experiments involving the pulsed laser irradiation of GaN power devices are concentrated in institutions such as the French National Center for Scientific Research, the University of Bordeaux,



➤ Figure 1. The UV pulsed laser simulated irradiation testing system comprises the following integrated modules: (1), a UV pulsed laser source module with a repetition rate of around 10 kHz that generates 266 nm UV pulses that are shorter than a nanosecond and a maximum single-pulse energy at the surface of the device under test (DUT) of more than 15 nJ; (2), an optical coupling module that efficiently couples and delivers the laser output to the surface of the DUT; (3), a two-dimensional scanning displacement platform, providing a scanning range of 3 cm by 3 cm with sub-micron resolved irradiation for localised sensitivity mapping of devices; (4), a variable-temperature-control module, offering precise temperature regulation across 80-420 K with a stability of ±0.1 °C, facilitating temperature-dependent irradiation effect studies; and (5), a real-time electrical characterisation module, enabling *in-situ* electrical measurements during irradiation, to capture dynamic responses of the DUT. (b) Equivalence between pulsed laser and heavy ion (linear energy transfer, *LET*, as a function of the effective laser energy, E_{eff}). This plot has been obtained using: an experimental impact ionisation energy for GaN of 8.9 eV; a density for GaN of 6.1 g cm^{-3}; a lasing wavelength of 266 nm; and a single-photon absorption coefficient at that wavelength of 1×10^5 cm^{-1}. As the lasing energy is 4.66 eV, well above the GaN bandgap of 3.39 eV, single-photon absorption occurs in the active region and the two-photon absorption coefficient can be considered as zero.



➤ Figure 2. (a) SET test circuit (model: PSPL5580, bandwidth: 15 GHz) and (b) corresponding waveforms. (c) Irradiation-induced photocurrent mapping image.

the US Naval Research Laboratory and the National Space Science Center of China (NSSC) (see Table 1 for a summary of the relevant laser system parameters). Among these efforts, only the NRL has reported studies on UV pulsed laser irradiation targeting wide-bandgap GaN based on single-photon absorption. Furthermore, no studies have been published on dynamic electrical characterisation under pulsed laser irradiation.

Addressing this omission is our research team from Nanjing University. We have independently developed an advanced UV pulsed laser simulated irradiation testing system (for details, see Figure 1 (a)).

Using this pulsed laser system, we have investigated a number of matters. They include: the equivalence between a pulsed laser and heavy ions; single-event transient, and single-event burnout; irradiation-sensitive area mapping; dynamic double-pulse switching; un-clamped inductive switching robustness; and power-conversion efficiency. All these studies promote the application of pulsed laser experimental technology in GaN power devices.

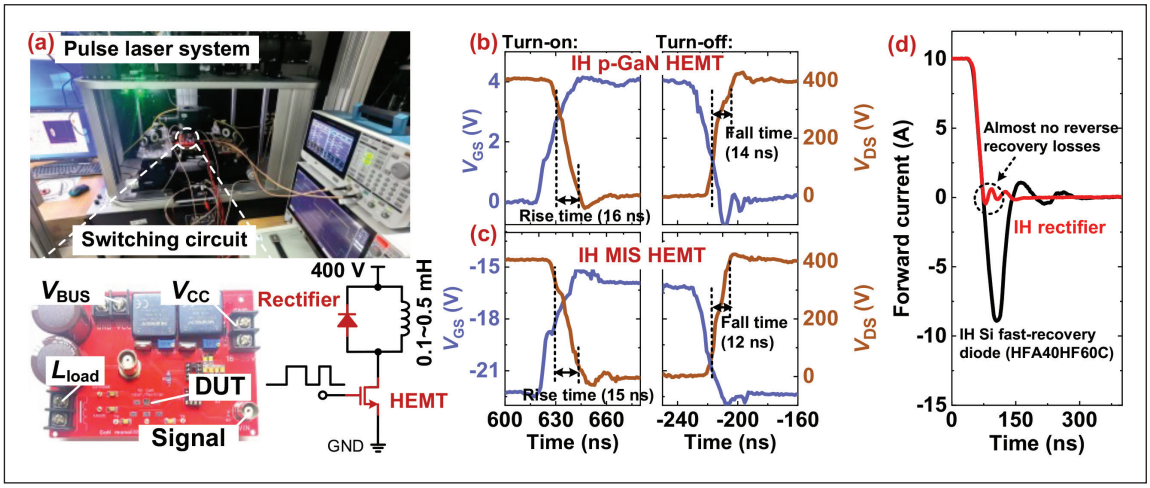
Before determining pulsed laser experimental conditions and optimising functionality, we considered the equivalence between pulsed lasers and heavy ions. The absorption of a 266 nm pulsed laser in GaN can be calculated from the laser intensity in the semiconductor, the free-carrier absorption cross section, the free-carrier density, and single-photon and two-photon absorption coefficients. We have also calculated the effective laser energy, using values of 0.144 for the passivation layer reflectivity, 0.22 for the reflectivity of the interface between the passivation layer and the barrier layer, and 0.212 for the reflectivity of the interface between the barrier layer and the buffer layer. Combining these equations with others that consider how the effective laser energy varies with distance, and the change in electric field intensity with distance, provides us with an equation for determining the equivalent linear energy transfer value for a pulsed laser (see Figure 1 (b)).

Under pulsed laser irradiation, single-event transients resulting from single-photon absorption can lead to disturbances in the current signal that influence the device's high-frequency operation and its stability. We are able to investigate this with our single-event transient test circuit (see Figure 2 (a)), featuring three high-frequency bias tees.

The gate, source and drain terminals of the device under test are connected to the common ports of the three bias tees. Subsequently, the AC ports of the bias tees are interfaced with three channels of an oscilloscope to capture single-event transient waveforms. To ensure precise focusing on the sample surface and laser incident positioning, we use a CCD camera. An adjustable power supply provides power to the laser system. Once the laser is turned on, we use an optical attenuator to adjust the effective incident energy of the pulsed laser.

Extracted single-event transient waveforms are shown in Figure 2 (b). They show that gate and drain currents of the GaN HEMT increase, indicating that there is a dissipation passage between the gate and drain for the irradiation-induced carriers. We are able to investigate this in more detail with our pulsed laser experimental techniques, which offer an advantage over approaches based on heavy ion irradiation – for that case, it's challenging to observe single-event transients, due to the randomness of particle incidence and large-area irradiation.

To determine the single-event burnout for devices, we apply a bias voltage to the device under test through a high-voltage source under pulsed laser irradiation. This experimental arrangement is simpler than that for single-event transients, which use a similar setup to that involving heavy ion irradiation. During the test, the single-event burnout depends on the bias voltage, as well as the pulsed laser equivalent of heavy ions. It is worth noting that since the pulsed laser provides micro-area localised irradiation, the device's susceptibility to irradiation may be weaker than that of heavy ions, and a higher bias voltage is desired to obtain critical single-event burnout.



➤ Figure 3. (a) Pulse laser irradiation system and dynamic switching circuit. Double-pulse switching waveforms for (b) p-GaN and (c) MIS HEMTs, and reverse recovery waveforms for GaN diodes.

Irradiation-sensitive area mapping

Within our pulsed laser irradiation system is a fluorescence spectroscopy module, which can perform mapping scans according to different bias voltages during irradiation. Drawing on this feature, we are able to observe the local current size on the device and thus identify its sensitive areas.

To gain this insight, we use the 2612B source meter (programmable by software) to provide the bias voltage. We apply an output voltage of up to 400 V and have a pulse current capacity of 10 A.

One strength of our system is that it has a measurement accuracy at the picoamp level. However, to optimise this accuracy, it is critical to select a suitable measurement range, based on the photocurrent size of the device. After scanning, our system automatically performs data storage and graph drawing.

Illustrating the capability of our instrumentation is Figure 2 (c). This photocurrent map reveals that the sensitive areas of the GaN HEMT (highlighted in the red stripe area) have a wider distribution than adjacent areas under pulsed laser irradiation, confirming that they are susceptible to local charge deposition and are irradiation-sensitive areas.

Integrating a double-pulse switching circuit into our pulsed laser irradiation system allows us to evaluate the dynamic characteristics of GaN power devices. Based on equivalence evaluation, we have used an effective laser energy of 0.432 pJ to emulate a linear energy transfer value that's equivalent to 82.7 MeV cm^2 mg^{-1} in heavy-ion experiments (see Figure 3 (a)).

We have obtained plots of dynamic switching waveforms (400 V/10 A) of *p*-GaN HEMT and GaN MIS-HEMT devices, along with reverse recovery waveforms of the GaN rectifier (see Figures 3 (b) - (d)). Data shows that devices exhibit nanosecond-scale fast switching performance under UV pulsed laser irradiation.

Assessing robustness

Robustness of non-avalanche *p*-GaN gate HEMTs against dynamic overvoltage and transient surge-energy shocks is critical for device applications, especially for extreme irradiation switching applications. While un-clamped inductive switching characteristics of *p*-GaN HEMTs are partially understood in terrestrial application scenarios, their behaviour under extreme irradiation conditions remains unexplored.

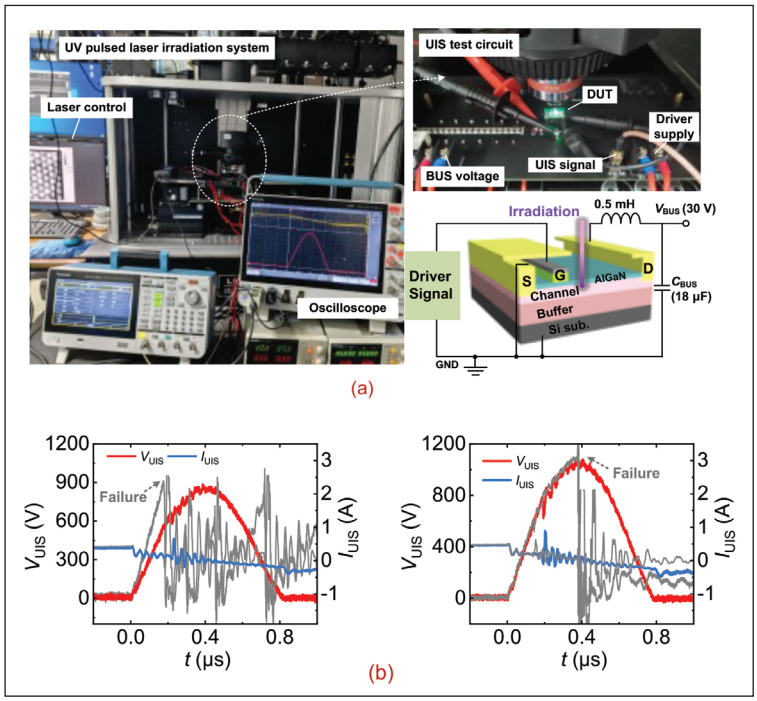
We are lifting the veil on this with a UV pulsed laser irradiation system that's integrated with an un-clamped inductive switching module (see Figure 4 (a) for an illustration of this system, and that of the 650 V *p*-type GaN HEMT under test).

With this experiment, during irradiation the device is initially turned on to charge the load inductor. Then the HEMT is turned off, forcing the energy stored in the inductor to surge toward the device under test. During this process, we use an oscilloscope to record real-time waveforms for the un-clamped inductive switching voltage and current. Laser irradiation is realised by using wire bonding to mount the HEMTs onto a custom-printed circuit daughterboard.

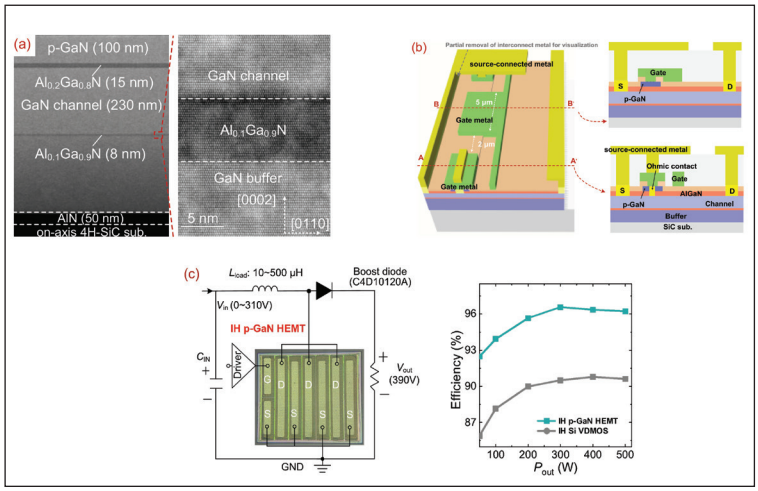
Under irradiation, we find that the critical dynamic overvoltage of the device is approximately 897 V, beyond which catastrophic failure occurs (see Figure 4 (b)). In contrast, without irradiation this metric reaches 1109 V. Based on these two values, we have determined that the dynamic overvoltage capability of the irradiated device deteriorates, with a degradation rate of 19 percent.

To determine energy loss, we integrate power over time during the charging and discharging phases associated with un-clamped inductive switching. This reveals that the irradiated device exhibits a consistently lower energy loss than its unirradiated counterpart across the entire range of surge currents.

These experiments uncover a concurrent reduction



➤ Figure 4. (a) Un-clamped inductive switching circuit setup in a UV pulse laser irradiation experimental system. (b) Critical un-clamped inductive switching and failure waveforms.



➤ Figure 5. (a) Cross-sectional scanning tunnelling electron microscopy image of an irradiation-hardened epitaxial structure. (b) 3D schematic of an irradiation-hardened GaN-on-SiC HEMT. (c) Power factor correction circuit, and system efficiency versus output power for an irradiation-hardened *p*-GaN HEMT and a 400-V irradiation-hardened silicon VDMOS (JHCS6N40NJR).

in dynamic overvoltage and energy loss. The fall in dynamic overvoltage signifies a decline in device endurance, while the diminished energy loss implies a decreased sensitivity to charge imbalance, governed by un-clamped inductive switching. We attribute these characteristics to the pre-filling of acceptor traps within the GaN buffer layer, with electron charges generated by single-event irradiation. To further enhance dynamic overvoltage hardness, it is crucial to alleviate the drain-side strong electric-field caused by irradiation. These findings and hardening guidelines offer critical insights to improving the robustness of *p*-GaN HEMTs in irradiation applications.

Power conversion efficiencies

We have also employed our pulsed laser technology to scrutinise the power-conversion efficiency of irradiation-hardened devices. They feature additional epitaxial material and a device structure that forms hole accumulation and dissipation passages. The robust design includes an additional 8-nm thick $Al_{0.1}Ga_{0.9}N$ layer to effectively confine the charges in a narrow heterojunction interlayer region (see Figure 5 (a)), and a source-connected partitioned gate structure design to quickly discharge the radiation-induced charges to the outside of the device (see Figure 5 (b)).

Measurements of these irradiation-hardened *p*-GaN HEMTs operating at 500 W at 300K under a linear energy transfer of 82.7 in a continuous-conduction power factor correction circuit have a power-conversion efficiency of 96 percent. That's far higher than a power-conversion efficiency of 400 V for irradiation-hardened silicon VDMOS – it's just 91 percent.

Our wide range of investigations using pulses of UV for irradiation showcase the strength and breadth of this technique, which will help to assess, enhance and demonstrate the capabilities of GaN HEMTs for deployment in space.

FURTHER READING

- F. Zhou *et al*. "800-V Irradiation-Hardened Device Technology on GaN-on-SiC Power Integration Platform" IEEE Int. Electron Devices Meeting (2024)
- T.Y. Zhou *et al*. "Normally-Off Schottky-Gate *p*-GaN HEMTs with Enhanced Irradiation Hardness" IEEE Int. Symp. Power Semiconductor Devices IC's (2024)
- F. Zhou *et al*. "Ultrathin-Body GaN-on-Sapphire HEMT with Megahertz Switching Capability Under Prompt Irradiation Dose Rate Exceeding 1010 rad(Si)/s" IEEE Electron Device Lett. **45** 1433 (2024)

Giving GaN a superjunction

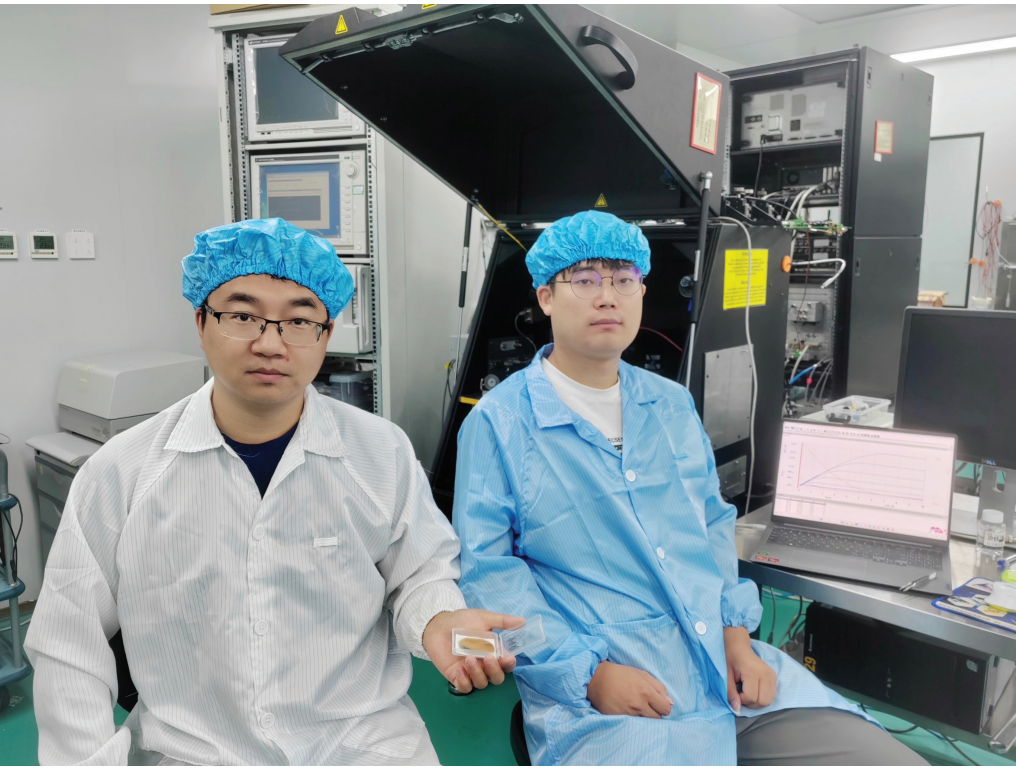
Equipping enhancement-mode GaN transistors with a superjunction boosts the blocking voltage beyond 10 kV

BY JIN WEI AND BO SHEN FROM PEKING UNIVERSITY

TODAY'S GaN power devices are well-established, generating significant sales in consumer electronics. They are widely deployed to block several hundred volts, with the 650 V enhancement-mode HEMT enjoying wide utilisation.

However, at higher voltages, SiC is seen as the main contender to incumbent silicon power technologies. There are only limited reports of GaN power HEMTs operating at kilovolts, a requirement for serving in high-voltage power grids, rail transportation, and industrial applications. However, GaN has much promise, offering superior theoretical characteristics to its established rivals.

There are two major challenges to address when developing GaN devices for kilovolt applications. One is that the key figure of merit – it's equal to the square of the blocking voltage, divided by the specific on-resistance – falls far short of what theory suggests. Closing this gap is crucial, as it will allow a GaN power device to attain an equivalent breakdown voltage at smaller device dimensions, and ultimately slash chip costs through substantial miniaturisation. The second issue to address is to tackle the severe degradation in dynamic on-resistance under high-voltage stress that arises from notorious trapping effects – they are particularly prevalent in the kilovolt-range.



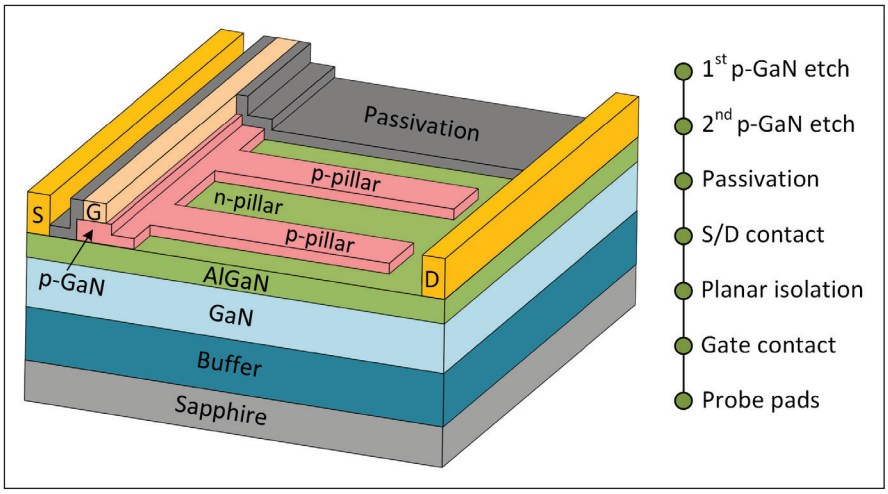
A viable approach for enhancing the figure of merit for ultra-high-voltage GaN transistors is to increase the blocking voltage while retaining the gate-to-drain distance, by introducing sophisticated field plates, gate termination extension, surface treatment, or the addition of a GaN cap layer. However, all these solutions suffer from trade-offs associated with processing complexity, reliability, and performance. Due to this, their adoption must be carefully evaluated for target applications.

A promising alternative is the superjunction, an architecture successfully implemented in silicon power devices, where it provides an effective boost to the figure of merit. The superjunction is viewed as a promising candidate for electric-field management and increasing the blocking voltage of GaN power devices. However, it is difficult to implement in enhancement-mode GaN lateral devices.

GaN superjunction technology

Recently, our team at Peking University has proposed a novel superjunction concept that's based on a standard enhancement-mode *p*-GaN gate HEMT platform (see Figure 1).

We fabricate this device using a standard *p*-GaN gate HEMT epiwafer, resulting in enhancement-mode operation. The superjunction structure is constructed by alternative *p*-/*n*-pillars along the direction perpendicular to current flow. The *p*-pillar is a thinned *p*-GaN stripe, and the *n*-pillar is the two-dimensional electron gas (2DEG) stripe between two adjacent *p*-pillars. The width of *p*-pillar is fixed to 4 μm, and



➤ Figure 1. The structure and process flow of the proposed superjunction *p*-GaN gate HEMT (SJ-HEMT).

charge balance is achieved by tuning the lateral width of the 2DEG stripes using photolithography. This approach gives the freedom to study device performance as a function of charge balance.

Devices are produced on a 2-inch GaN-on-sapphire wafer that features a 90 nm-thick *p*-GaN layer, a 15 nm-thick $Al_{0.2}Ga_{0.8}N$ barrier layer, a 200 nm-thick undoped GaN layer and a buffer layer. Fabrication commences with a partial etch of the *p*-GaN layer outside of the gate region, and a second etch defines the *p*-pillars. We then deposit a SiO_2 layer by plasma-enhanced CVD at 300°C, before adding source and drain ohmic contacts, formed from a Ti/Al/Ni/Au stack annealed under nitrogen gas at 810°C for 30 s. After this, fabrication turns to fluorine ion implantation for planar isolation and the deposition of a Ni/Au stack for the gate, followed by annealing in oxygen gas to form an ohmic contact to *p*-GaN. Finally, probing pads are added.

It's worth noting that the process for fabricating our superjunction HEMT is compatible with that employed for standard *p*-GaN gate HEMT technology. The superjunction structure can be realised with an additional *p*-GaN etching process. Thanks to the high degree of compatibility with the process used to make conventional devices, it would be straightforward to produce the proposed superjunction HEMT in existing foundries.

Charge balancing

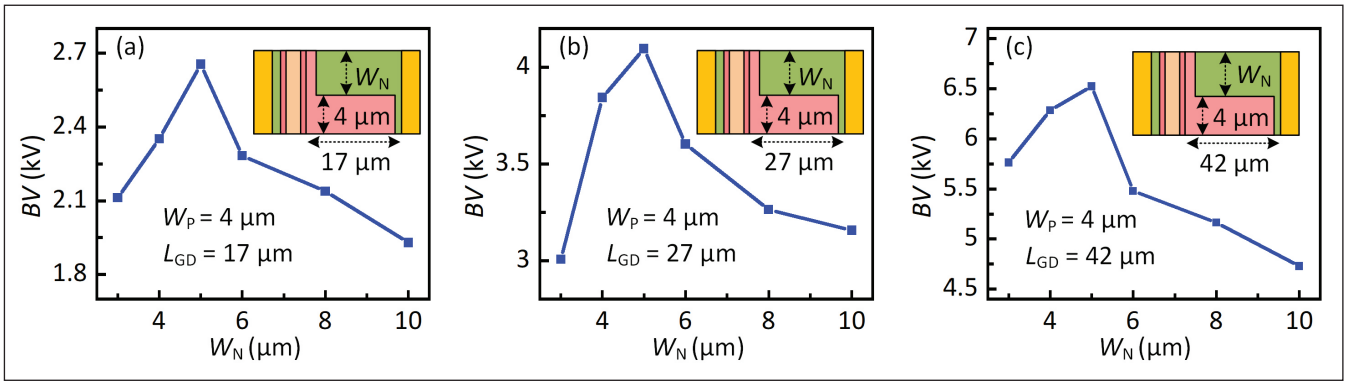
Charge balance is the core feature for all superjunction devices. For our proposed superjunction HEMT, during operation at a low drain stress, *p*-pillars and *n*-pillars are mutually depleted and the depletion region expands with drain stress. Meanwhile, at a high drain stress, the *p*-pillars and *n*-pillars are fully depleted, inducing a fast expansion of the depletion region. Due to this behaviour, our superjunction HEMT realises a more uniform electric field and a higher breakdown voltage. However, enjoying these benefits is not easy – compared with their silicon siblings, lateral GaN power devices are more involved, with complex charge distributions that can arise through polarisation charges, incomplete ionisation, and internal trapping.

Due to these complexities, the test devices have been developed that are similar to JFETs to characterise the charge balance effect. These transistors uncover the depletion behaviour of *n*-pillars and *p*-pillars under reverse bias.

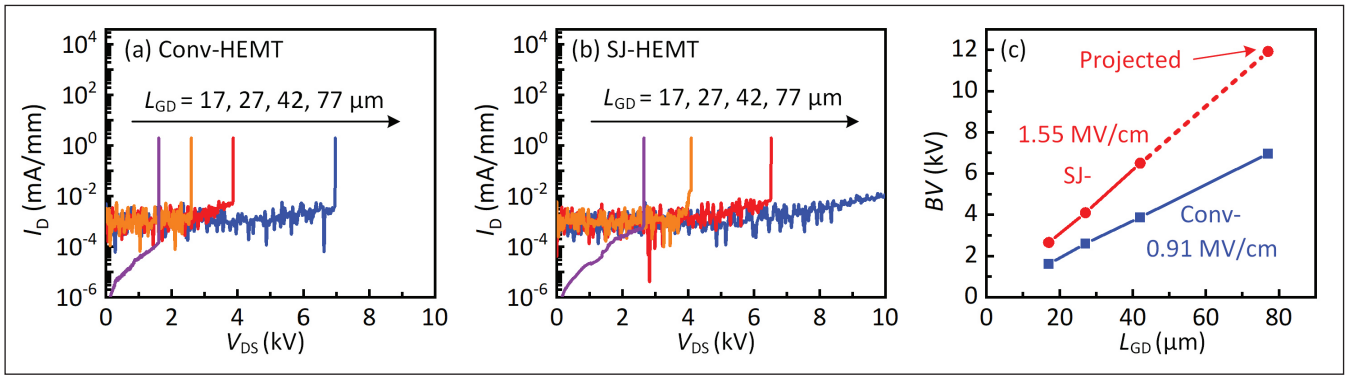
During tests, testing currents through the *n*-pillar and also the *p*-pillar are measured. When a negative bias is applied to the *p*-pillar, a depletion region is formed in both the *n*-pillar and *p*-pillar, mimicking the depletion behaviour of the superjunction HEMT. Eventually, the current is cut off as the bias increases, marking the conditions for depletion of the whole *n*-pillar.

When *n*-pillars and *p*-pillars are simultaneously depleted at the same bias, charge balance is realised. This allows specially designed testing devices to provide clear guidance for the charge balance design in GaN power devices. According to measurements, charge balance is realised for a *n*-pillar width of 5 μm and a *p*-pillar width of 4 μm. This is a milestone: the first experimental proof for charge balance in GaN devices in the scientific literature.

The charge balance condition has been



➤ Figure 2. The measured relationship for the blocking voltage (*BV*) and *n*-pillar width (W_N) of superjunction HEMTs with different source-to-drain lengths (L_{GD}) when the *p*-pillar width is fixed at 4 μm. For all source-to-drain lengths, the highest blocking voltage is obtained at W_N/W_P = 5/4 μm, which is the charge balance point.



➤ Figure 3. Off-state current-voltage curves of (a) conventional *p*-GaN gate HEMT and (b) superjunction-HEMT with widths of the *n*- and *p*-pillars (W_N/W_P) of 5 µm and 4 µm, respectively. (c) The relationship between blocking voltage (*BV*) and gate-to-drain distance (L_{GD}). For the superjunction HEMT with a gate-to-drain distance of 77 µm, the blocking voltage exceeds 10 kV (the measurement limit), and is projected to be 11,935 V by linear extrapolation.

additionally verified with breakdown voltage measurements (see figure 2). This involved fixing the width of the *p*-pillar to 4 µm, and investigating the relationship between the blocking voltage and the width of the *n*-pillar for superjunction HEMTs with various gate-to-drain distances. This study determined that the highest blocking voltages occurs at charge balance, with an *n*-pillar width of 5 µm, indicating that the charge-balanced point arises at an *n*-pillar width of 5 µm and a *p*-pillar width of 4 µm.

Another area of this work involves investigating the breakdown voltages of conventional *p*-GaN gate HEMTs, as well as our proposed superjunction HEMTs with gate-to-drain distances from 17 µm to 77 µm. For this study, we used charge-balanced superjunction HEMTs with an *n*-pillar width of 5 µm and a *p*-pillar width of 4 µm.

This investigation determined that conventional *p*-GaN gate HEMTs have an average breakdown field – defined by the blocking voltage, divided by the gate-to-drain distance (BV/L_{GD}) – of just 0.91 MV cm^{-1}. The corresponding maximum breakdown voltage is 6,965 V.

In comparison, the performance of the charge-balanced superjunction HEMTs are far more impressive. They have an ultra-high average breakdown field of 1.55 MV cm^{-1}, a figure derived from a breakdown voltage of 6525 V, recorded for a device with a gate-to-drain distance of 42 µm. More significantly, the breakdown voltage of the superjunction HEMT with a gate-to-drain distance of 77 µm is beyond 10 kV – based on linear extrapolation, it is projected to be 11,935 V. As far as we know, this is the first experimental demonstration of an enhancement-mode *p*-GaN gate HEMT with a breakdown voltage beyond 10 kV, marking a technological milestone for lateral GaN power devices in high-voltage applications.

This substantial enhancement in breakdown voltage opens the door to a significant reduction in gate-to-drain spacing for kilovolt-rated devices, which can simultaneously offer a lower specific on-resistance and a reduction in active area by 20-40 percent compared with conventional designs.

More critically, the charge-balanced superjunction HEMT provides electric-field-profile optimisation, demonstrating a lower peak electric field intensity at equivalent blocking voltages, according to numerical simulations. Thanks to this refinement, reliabilities at high-voltage are expected to be enhanced with the superjunction HEMT, which promises to offer greater robustness to the likes of hot-electron effects, high-temperature reverse-bias stress and current collapse.

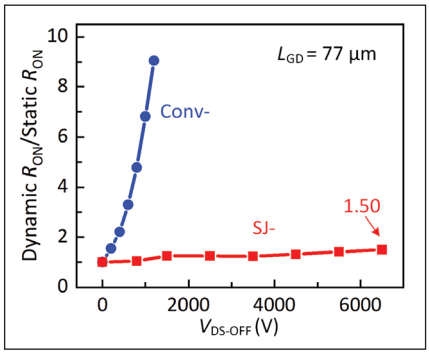
Improved performance

The proposed superjunction HEMT has one unique advantage, thanks to having a 2DEG under both the *n*-pillar and *p*-pillar contributing to conduction. That's not the case with the conventional silicon superjunction MOSFET, which has just the *n*-pillar contributing to conduction.

When in the on-state, the 2DEG under the *p*-pillar can be generated by field effect, when the *p*-pillar is directly connected to *p*-GaN gate. According to transfer length measurements, sheet resistances under the *n*-pillar and *p*-pillar are 416 Ω/sq and 411 Ω/sq, respectively. Therefore, there is no degradation to the on-resistance of superjunction HEMTs. The fabricated superjunction HEMT with a gate-to-drain distance of 77 µm has a threshold voltage of 0.9 V, defined at a drain current density of 10 µA mm^{-1}, meeting the requirement of enhancement-mode operation for power systems. The corresponding on-resistance is 36.4 Ω mm – defined at a drain-source voltage of 1 V and a gate-source voltage of 3.5 V – corresponding to a specific on-resistance of 32.03 mΩ cm^2.

For conventional GaN HEMTs, one of their weaknesses is a degradation in dynamic on-resistance that stems from the intrinsic trapping-induced negative charge storage. This is to blame for unexpected power loss.

Note that this is not an issue in



➤ Figure 4. An ultra-low dynamic on-resistance/static on-resistance ratio of 1.5 is obtained in superjunction HEMT after a 6.5 kV drain stress.

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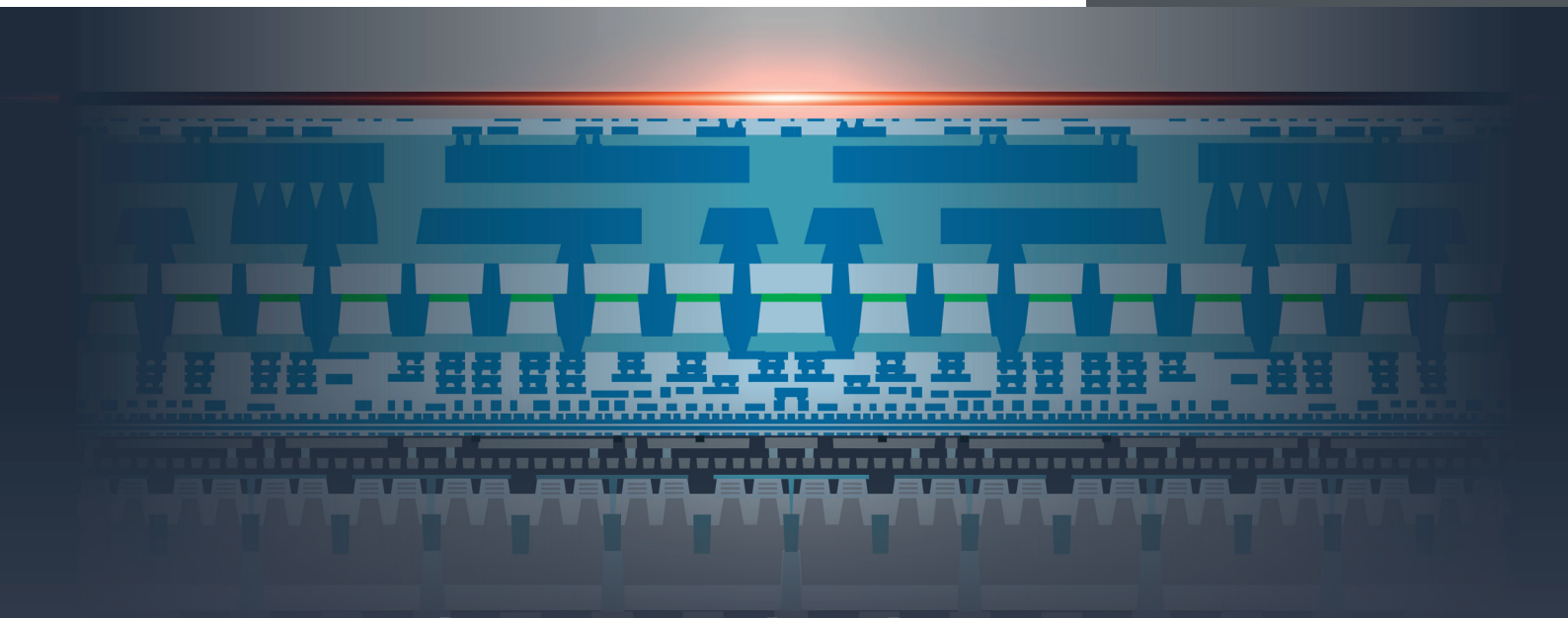

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superjunction HEMTs, which benefit from a combination of: surface traps above the *p*-pillar being effectively screened by holes in the *p*-pillar; and the recovery of traps, effectively accelerated by hole injection/light emission. Due to these benefits, the superjunction HEMT with a gate-to-drain distance of 77 μm exhibits an ultra-low ratio of dynamic on-resistance to static on-resistance – it's just 1.50, after off-state stress up to 6500 V.

Based on these results, one can conclude that the proposed superjunction HEMT, which is capable of enhanced stability and reliability, offers great potential for serving in kilovolt applications. As far as we know, this study provides the first report of dynamic on-resistance of GaN power HEMTs with a drain stress of up to 6.5 kilovolts. This demonstration paves the way to ultra-high voltage applications using GaN transistors, with results confirming that the proposed superjunction HEMT technology overcomes the critical reliability barrier for practical kilovolt-level GaN devices.

Compared with state-of-the-art high-voltage GaN power HEMTs, the superjunction HEMT provides best-in-class performances, with a figure of merit of 3.81 GW cm^{-2} at a gate-to-drain distance of 42 μm. For the variant with a gate-to-drain distance of 77 μm, blocking voltage exceeds 10 kV, realised while maintaining a specific on-resistance of 32.03 mΩ cm^2. The associated, projected figure-of-merit is 4.45 GW cm^2 – a landmark achievement that redefines the potential performance of single-channel GaN HEMTs.

More significantly, the superjunction HEMTs offer a high degree of fabrication compatibility with conventional devices, and feature a natural single-channel planar structure, facilitating the development of a high-voltage integration platform. These advances are a critical step towards bridging the gap between theoretical material potential and practical device performance in ultra-high-voltage GaN technology.

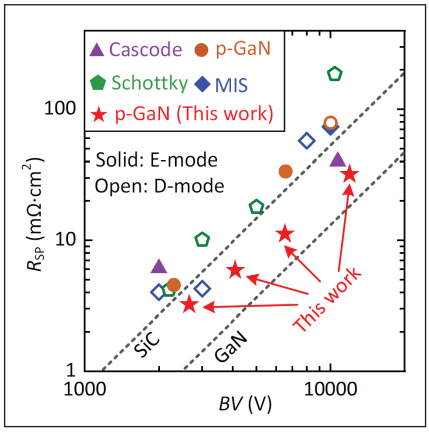

Figure 5. Benchmark for the specific on-resistance as a function of breakdown voltage for superjunction HEMTs and state-of-the-art high-voltage (more than 2 kV) GaN power transistors.

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Ammonia MBE targets HEMTs that feature ScAlN

Enhancing GaN-based HEMTs with ScAlN, via growth by ammonia MBE, promises to improve the performance of high-frequency power devices

BY YVON CORDIER FROM UNIVERSITÉ CÔTE D'AZUR, CNRS-CRHEA

WITHIN our community, much effort is devoted to developing new material systems with the potential to produce higher-performing devices. Often this work involves much breaking of new ground, but sometimes it's possible to get a helping hand by considering materials that have already enjoyed success in related fields.

For many years, one of our significant revenue streams has been the GaAs-based PA, which plays a key role in the RF front-end of billions of handsets. Sitting close to the PA is another crucial component in this part of the mobile, the acoustic-wave filter. It faces demands that have become far more strenuous over the years, and since 2009 there has been much interest in meeting these more stringent requirements by turning to the alloy scandium aluminium nitride (ScAlN). This relatively novel material is an attractive alternative to the incumbent, AlN, offering a larger response, realised when adding scandium with a mole fraction of about 20 percent to 40 percent to the original AlN.

Recently, due to its wide bandgap characteristic, ScAlN has started to gain attention as an attractive candidate for fabricating electron devices, with this ternary promising to play a key role in GaN-based heterostructures. This interest tends to focus on the HEMT, a very popular high-frequency electron device that can be based on the nitride family of materials.

Compared with a compound semiconductor like GaAs, GaN presents several advantages when fabricating a HEMT. As well as a critical electric field that is ten times larger – and provides a commensurate increase in breakdown voltage – GaN features a wurtzite crystal lattice that spawns internal electrical polarisation, leading to electrical charge, either at the surface, or at the interface between this material and other compounds. Thanks to this doping-free charge, free electron densities as high as 1×10^{13} cm^{-2} are realised at the interface of alloys like GaN and AlGaN – that's more than five times that found in a typical AlGaAs/InGaAs pseudomorphic HEMT.

Another strength of the established nitrides is that when AlN is grown on GaN, this leads to the generation of up to 5×10^{13} electrons per cm^2. However, there is a downside of this pairing: a difference in the natural distance between aluminium and nitrogen atoms, compared with that for gallium and nitrogen. This mismatch induces considerable mechanical stress inside the crystal lattice, hampering the fabrication of stable materials and devices.

Due to this issue, there is much interest in alternative alloys, such as InAlN and ScAlN. For both these ternaries, there is almost no stress when they are grown on GaN, when the aluminium mole fraction is around 85 percent.

While much effort has been devoted to InAlN, ScAlN is the more promising of the two. In terms of electron density, ScAlN can reach a value of around 4×10^{13} cm^{-2} in the GaN channel, about twice that of InAlN. A high value is cherished, as this helps maintain a carrier density of more than 10^{13} electrons per cm^2, even for film thicknesses between 5 nm and 10 nm. This strength is analogous to that of oxide thinning in a silicon MOSFET, an approach employed to limit the short channel effect – this is the undesirable weakening of drain-current modulation with gate bias, occurring when shrinking the gate to 100 nm or less to cut the carrier transit time and reach operating frequencies of several gigahertz or more.

Note that unlike InAlN, ScAlN can be ferroelectric. This asset offers opportunities associated with memory, and also for programming the threshold voltage of transistors.

The need for epitaxy

For the fabrication of filters operating at a few gigahertz, sputtering can deposit ScAlN with sufficient chemical and structural quality. But this form of film growth is not capable of producing a stack of semiconductors with sufficient crystal quality and purity for making HEMTs with high performance. For this reason, heterostructures are epitaxially grown on monocrystalline substrates, such as sapphire, silicon or SiC (see Figure 1).


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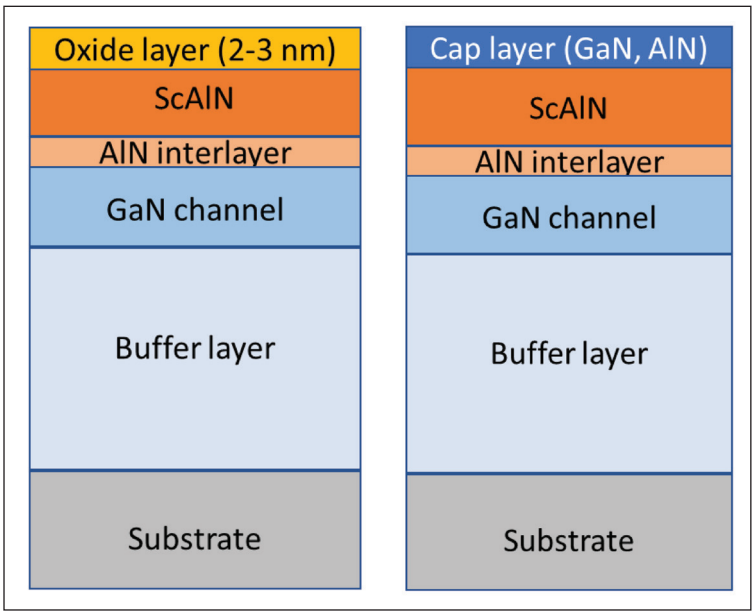
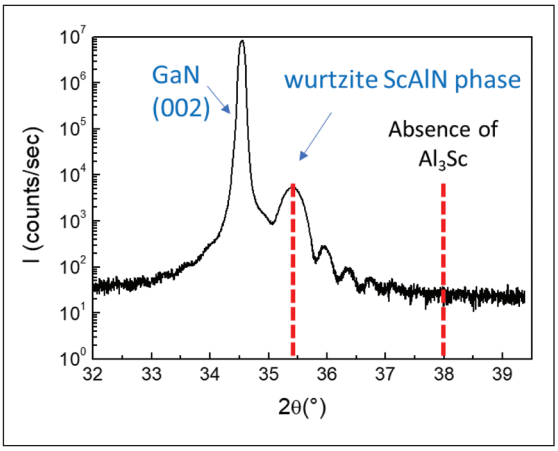


➤ Figure 1. Schematic cross-section of the first (left) and second (right) generation HEMTs studied at CRHEA.

Within the family of epitaxial growth techniques, plasma-assisted MBE produced the first ScAlN epilayers. This form of epitaxy involves the evaporation of pure metal atoms under high vacuum. As nitrogen molecules are very stable, this gas is introduced in the growth chamber through an RF cavity, employed to generate radicals that combine with metals to form III-nitride compounds. The constituents come together on the surface of a substrate, radiatively heated by a resistive filament positioned close to the back face.

Like all epitaxial techniques, certain conditions are essential for high-quality material growth. They include the growth temperature, which has an operating range that is governed by the conditions for generating nitrogen radicals and their reaction rate with metals. Optimum conditions for growth of GaN rely on a subtle equilibrium between the metal reaction with nitrogen, and metal re-evaporation at a temperature around 700°C, resulting in the accumulation of a gallium layer floating on the surface. It's not easy to realise this state of affairs,



➤ Figure 2: High resolution X-ray diffraction performed on a ScAlN film grown by ammonia MBE on a GaN.

as a slightly lower temperature leads to the accumulation of metal droplets at the surface, and a higher one generates defects due to a lack of metal. It's even more challenging to grow high-quality layers of ternary materials, because different metals react with nitrogen radicals at different rates, and re-evaporate at different rates. But despite these complications, plasma-assisted MBE is the most common epitaxial technique for growing ScAlN-based heterostructures.

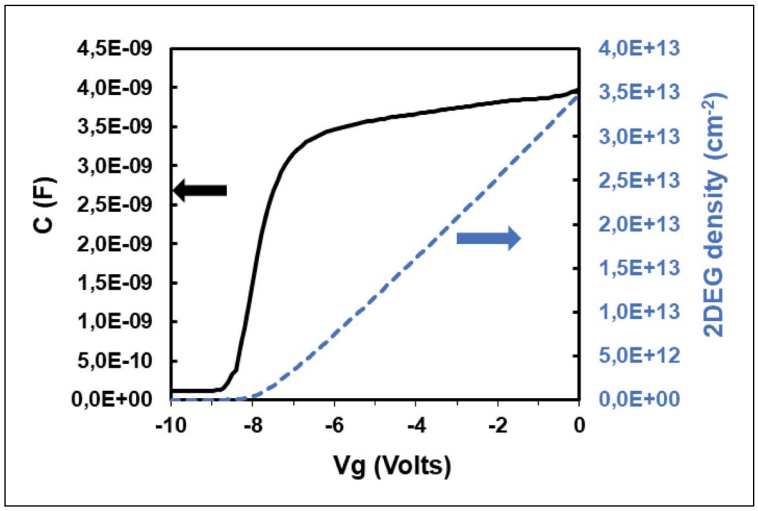
For nitrides in general, MOCVD is the most widely adopted approach to growth. But it's held back by a lack of scandium-containing organometallic precursors with sufficient partial pressure. While new precursors are looking to address this issue, even if there is success on this front, there's still the challenge of fabricating heterostructures with sharp interfaces at the high temperatures necessary for good crystal quality and high-purity material. In this context, ammonia-source MBE has much promise, allowing GaN growth at temperatures around 800°C under an excess of nitrogen, a condition that guarantees easy control of growth rate and material quality.

Using this epitaxial technology, our team at CRHEA, France, has been developing and refining ammonia MBE since the 1990s. With this approach we draw a parallel to MOCVD, thermally cracking ammonia at the surface of the heated substrate. In our case the temperature is sufficiently low to limit diffusion in the crystal, but high enough to ensure growth of smooth films with a relatively high purity. Additional assets are that: ammonia consumption is far lower than it is with MOCVD; the undoped GaN that's produced by this technique is sufficiently resistive to enable the fabrication of functional transistors on HEMT heterostructures; and the control of the growth of alloys, such as AlGaN, is facilitated by the fact that all the gallium and aluminium atoms reaching the surface can be incorporated into the crystal.

Since the beginning of this century, our laboratory has been using ammonia MBE to produce AlGaN/GaN HEMTs on silicon substrates for RF power applications. By working with partners that include IEMN, ETH Zürich, Daimler Chrysler, Thales, and the III-V Lab, we have realised CW power densities of 6.6 W mm^{-1} at 2 GHz and 3.2 W mm^{-1} at 40 GHz with our material.

We started investigating the growth of ScAlN in 2021. Back then, in terms of scandium-containing alloys, only ScGaN had been grown by ammonia MBE. We began by focusing on the effect of the growth temperature, supported by funding from the French 'Investments in the future' programme named GaNeX and the European ECSEL JU project Gallium Nitride for Advanced Power Applications (GaN4AP).

This study determined an optimal growth temperature window of around 670°C, and

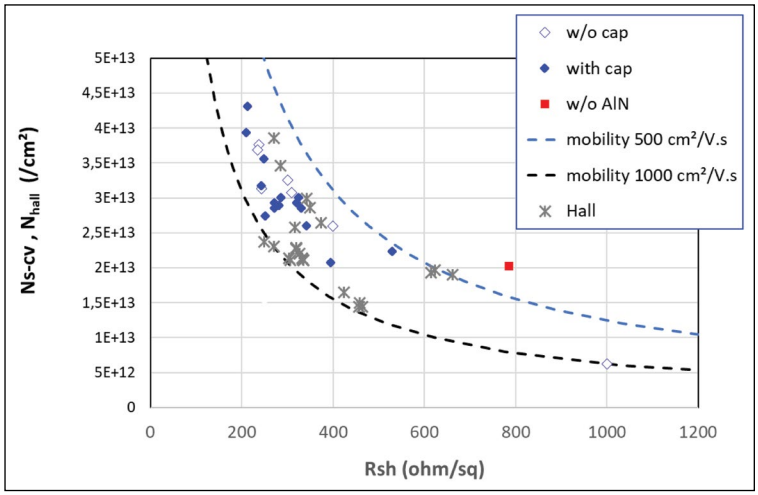


➤ Figure 3. Capacitance-voltage and corresponding charge density in the 2DEG of a ScAlN/GaN HEMT grown by ammonia MBE.

demonstrated that it's possible to grow films on GaN with low strain that have a scandium molar fraction of around 14 percent. For this work, our collaborators studied film quality at the GREMAN laboratory in Tours, GPM in Rouen, France, and CNR-IMM in Catania, Italy – and we benefited from fruitful discussions with Fraunhofer IAF in Freiburg, Germany. Characterisation rapidly revealed the advantages of ammonia MBE for ScAlN alloy growth, determining that there is no change in scandium content throughout a widely explored 180°C growth temperature range, and it's possible to grow uniform random alloys free from metallic precipitates, like Al_3Sc, which can plague plasma-assisted MBE.

We confirmed the high crystal quality of the ScAlN films grown on GaN-on-sapphire with X-ray diffraction (see Figure 2). Interference fringes in the diffraction spectrum highlight low roughness for both the surface of the ScAlN film and its interface with GaN.

To rapidly assess the number of charges that are present in our HEMT's two-dimensional electron gas (2DEG) that's formed in the GaN channel and at the interface with ScAlN, we have used the mercury probe capacitance-voltage technique. This has determined high carrier concentrations, in the range 3-4 x 10^{13} cm^{-2} in HEMT heterostructures with an ScAlN barrier that's around just 10 nm thick. That's a very encouraging result for high-frequency applications.



➤ Figure 4. Transport properties of the 2DEG in a ScAlN-based HEMT grown by ammonia MBE.

As our HEMTs are grown on a highly resistive buffer and substrate, we are able to determine their transport properties with a contactless technique involving Eddy currents (see Figure 4). In the plots of these results, the dashed lines represent calculations corresponding to different values for electron mobility. In addition, there's data from Hall-effect measurements, obtained using Van der Paw cloverleaf patterns fabricated on some of these samples. Note that almost all the data is bounded by two lines, corresponding to electron mobilities of 500 cm^2 $V^{-1}s^{-1}$ and 1000 cm^2 $V^{-1}s^{-1}$.

The single result sitting outside this domain is for a HEMT grown without an AlN interlayer that exhibits a higher sheet resistance, due to a reduced electron mobility. This observation underlines the critical role of the thin AlN (1-2 nm) layer in obtaining sharp interfaces with an energy barrier that confines the 2DEG in the high-electron-mobility region provided by the GaN channel, while not suffering from scattering associated with ScAlN.

Critical capping layers

Using this first-generation material, we have fabricated transistors with a low gate leakage, and with a drain current capability of 2-3 A mm^{-1}. However, we have found a lack of stability during device processing. We attribute this to the susceptibility of scandium to oxidation, which is a significant downside of working with ScAlN. We find that when the surface of this alloy is exposed to air, a 2-3 nm thick oxide layer spontaneously forms. What's more, when immersed into a photoresist developer etching occurs, progressively reducing film thickness at each lithographic step of device processing.

To tackle this issue, we are introducing capping, using thin layers of AlN and GaN, grown immediately after ScAlN. According to data shown in Figure 4, capping layers don't impede 2DEG transport properties. In a HEMT that has a total thickness for the barrier and the cap layer of less than 10 nm, the sheet resistance is as low as 210 ohm/sq. Thanks to these advances, more stable device processing has been undertaken by our colleagues at IEMN in Lille, France, enabling short-gate transistors with a maximum oscillation frequency over 100 GHz, based on a ScAlN/GaN HEMT on a silicon substrate.

Characterisation of these HEMTs, featuring a 75 nm gate, reveals a 2DEG carrier density of 1.6 x 10^{13} cm^{-2} and a mobility of 621 cm^2 $V^{-1}s^{-1}$. Evaluations of DC performance have revealed a drain current density of 1.35 A mm^{-1} and a transconductance of

284 mS mm^{-1}, and an assessment of RF performance has determined a cut-off frequency of 82 GHz, and a maximum power gain frequency of 112 GHz, indicating that these devices are promising candidates for serving in the Ka band.

Next steps

Our efforts have provided the first demonstration of using ammonia MBE for fabricating high-frequency HEMTs. Building on this foundation, ScAlN/GaN heterostructures could be used for power-switching transistors, which could benefit from a low 2DEG sheet resistance, so long as we realise efficient surface passivation and preserve low leakage currents. Working towards this goal, we are investigating passivation with *in-situ* SiN, drawing on a process we previously developed for AlGaN/GaN-based heterostructures.

Another avenue for further work is the use of epitaxy for growing our material systems on other semiconductor films or substrates. This approach could allow us to more fully explore various functionalities provided by the piezoelectric and ferroelectric properties of ScAlN, and more generally ScAlGaN compounds. As part of such efforts, in the national project TWINS, we are developing a monolithic, voltage-controlled oscillator operating in the 1-10 GHz range, based on joint use of SAW devices and transistors. We are also involved in another national project, named BE-SAFE, that's dedicated to the study of ferroelectric properties.

As we pursue the targets of these projects, this may generate numerous questions concerning the relationship between properties, reliability, crystal quality, and the purity of different co-integrated materials. What is for sure is that we have some exciting years ahead of us, exploring a field that's new and wide.

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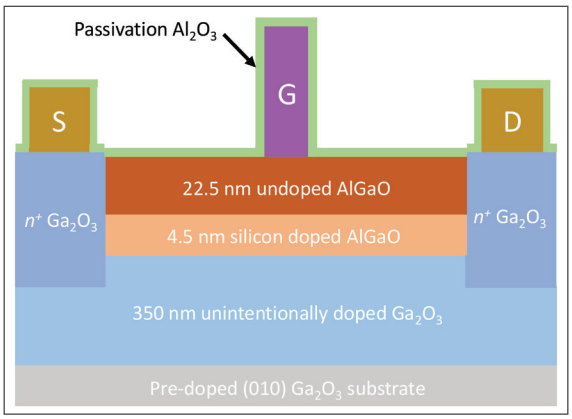
Passivating β-Ga_2O_3 devices

The combination of gentle etching, annealing and the addition of a thick passivation layer of Al_2O_3 is taking the performance of β-Ga_2O_3 RF devices to a new level

ENGINEERS from the University of Buffalo are claiming to have realised the first successful trap passivation of β-Ga_2O_3 RF devices. This is accomplished by using a relatively thick layer of Al_2O_3, which prevents current collapse that's detrimental to the performance of RF devices.

The team's FETs have been formed by 'meticulously designed' fabrication steps that address imperfections in their predecessors.



➤ A relatively thick layer of Al_2O_3 passivates the traps in β-Ga_2O_3 RF devices

The recent improvements will help to advance the capabilities of β-Ga_2O_3 RF devices, which have a high critical electric field and a good saturation velocity. Thanks to these strengths, the Johnson figure-of-merit, which provides a good yardstick for evaluating the RF potential of various materials, is higher for β-Ga_2O_3 than SiC and GaN.

Fabrication of the University of Buffalo's heterostructure FETs involves the etching of the Al_2O_3 layer and the unintentionally doped Ga_2O_3 layer, prior to regrowth of heavily doped Ga_2O_3. Previous devices produced by the team involved a high-power reactive-ion etch before re-growth. This etch led to a high interface resistance between this layer and the two-dimensional electron gas, limiting transconductance and RF performance.

Other groups have shown that MBE annealing under vacuum can recover some of the damage caused by plasma etching, and that dialling down the power of this etch leads to very little damage, and a very low contact resistance.

The team from the University of Buffalo have adopted both of these strategies in their latest transistors, produced by processing an epiwafer from Novel Crystal Technology, consisting of a 350 nm-thick unintentionally doped layer of MBE-grown β-Ga_2O_3 on a iron-doped insulating substrate.

On this platform the team added a 4.5 nm-thick layer of β-$(Al_{0.21}Ga_{0.79})_2O_3$ with a silicon doping concentration of 1.5×10^{19} cm^{-3}, followed by an un-doped barrier of 22.5 nm-thick β-$(Al_{0.21}Ga_{0.79})_2O_3$.

Subsequent steps in the fabrication process included a selective low-power reactive-ion etch that ensured slow removal of the AlGaO layer and stopped on the unintentionally doped Ga_2O_3 layer without imparting any damage. The engineers cleaned this sample with deionised water, before loading it into an MBE chamber and annealing it at 600°C for 1 hour under a vacuum of 10^{-10} Torr. To complete device fabrication, they grew a 100 nm-thick heavily-doped *n*-type layer of Ga_2O_3, removed the growth mask, added contacts, and passivated the devices by using atomic layer deposition to form a 100 nm-thick layer of Al_2O_3.

Plots of drain current as a function of drain-source voltage did not uncover any non-linearity at lower voltages, an issue present in the team's previous FETs. The team attributes the absence of this unwanted behaviour to process optimisation, including the low-power etch, the dip in hydrochloric acid prior to regrowth, and MBE annealing. Another benefit attributed to these steps is an increase in peak drain current, which hits 500 mA mm^{-1} at a gate-source voltage of 3 V.

Measurements also determined no significant shift in threshold voltage and no collapse in either the peak drain current or the peak transconductance after passivation, highlighting the benefit of the relatively thick layer of Al_2O_3.

Note that the team's previous devices suffered from a shift in threshold voltage, which may have been caused by high-temperature deposition or plasma damage.

The team have also conducted pulsed current-voltage measurements, which revealed that Al_2O_3 passivates the traps and eliminates dispersion. Work by a collaboration between KBR, the Air Force Research Laboratory, Teledyne Scientific and Cornell University, have employed a similar approach and obtained moderate dispersion, but they employed an Al_2O_3 layer just 20 nm-thick.

RF measurements show that prior to passivation, the FETs fail to deliver any gain and suffer from huge DC-RF dispersion or current collapse.

Devices with passivation and a gate length of 191 nm have a value for the cut-off frequency (f_T) of 32 GHz, at a gate-source voltage of -3 V and a drain-source voltage of 7 V. The maximum oscillation frequency (f_{MAX}) is 55 GHz, for a gate-source voltage of -3 V and a drain-source voltage of 15 V.

Benchmarking these results, the team says that its values for f_T and f_{MAX} are amongst the highest reported for β-Ga_2O_3 FETs.

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Hot-wall MOCVD helps GaN-on-AlN HEMTs

An Aixtron hot-wall reactor enables record mobilities for GaN-on-AlN HEMTs

A COLLABORATION led by Linköping University is raising the bar for the performance of GaN HEMTs grown on AlN substrates. Devices featuring a thin channel and grown by hot-wall MOCVD are claimed to combine a high carrier density with a record mobility for the two-dimensional electron gas (2DEG).

Commenting on this success, Vanya Darakchieva, who is affiliated to both Linköping University and Lund University, remarks: "Achieving this requires growing thin GaN layers on AlN with low impurity and defect densities and excellent structural quality, which is very challenging."

Key to the team's success is its MOCVD reactor. "Our Aixtron reactor is unique worldwide, featuring a hot-wall MOCVD process that minimises vertical and lateral temperature gradients while enabling precise control over gas-phase chemistry," says Darakchieva.

Developing GaN HEMTs on AlN substrates may raise a few eyebrows, given that this foundation has a reputation for its high cost, small size and limited availability. But Darakchieva says that there is the potential to significantly lower costs, thanks to alternative substrate fabrication methods and a growing ecosystem that's driven by deep-UV LEDs and emerging power and RF applications. She highlights the Swedish deep-tech spin-off Xtal.works, which is developing innovative PVT and CVD growth methods for wide and ultra-wide bandgap semiconductors.

One of the challenges that Darakchieva and her co-workers have faced stems from the 2.4 percent lattice mismatch between AlN and GaN. Once the critical thickness is exceeded when growing GaN on AlN, strain relaxation kicks-in through elastic mechanisms, such as a transition from the two-dimensional to the three-dimensional growth mode, or plastic deformation via dislocation generation.

Efforts are also hampered by the relatively high surface energy of the AlN substrate that leads to a higher gallium adatom binding energy, shorter diffusion lengths, and a tendency for GaN to nucleate as islands.

Despite all these issues, high-quality growth of a GaN epilayer on an AlN substrate is possible by hot-wall MOCVD, which offers stable high-temperature growth conditions.

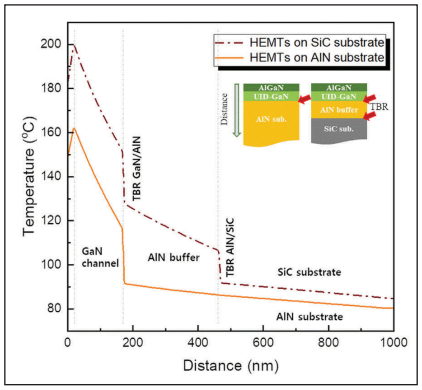
The Swedish-based team have demonstrated this by using their Aixtron VP508GR reactor to produce a portfolio of GaN-on-AlN heterostructures on small AlN and 4H-SiC substrates.

Following chemical cleaning with a standard process, both substrates were loaded into the hot-wall reactor, annealed and etched under hydrogen at 1340°C. Formation of the heterostructures began by growing a 300 nm-thick AlN layer at 1250°C, and then a GaN layer at 1080°C, using a range of pressures, V-III ratios, and flow rates for the gallium precursor.

Scrutinising samples with scanning electron microscopy revealed that the team's standard conditions, which provide a smooth surface morphology and excellent electrical properties for a 1 μm-thick GaN layer, lead to incomplete coverage and individual sparse islands when attempting to form a thin channel layer.

Employing a higher flow rate for the gallium precursor enhanced island coalescence and increased layer coverage. Further gains resulted from reducing the growth pressure to 50 mbar – this helped to form fully merged GaN channel layers under optimised conditions.

The team found that despite GaN nucleation on the AlN surface, this foundation led to greater GaN coverage than that realised with a SiC substrate. Darakchieva and co-workers attribute this advantage to the higher out-of-plane thermal conductivity, which led to higher surface temperatures, and in turn increased adatom mobility and faster clustering and coalescence.



➤ Compared with a SiC substrate, that made from AlN leads to a significant reduction in device temperature.

HEMTs have been produced using more promising growth conditions and an AlGaN barrier layer, as well as an AlN interlayer between the GaN channel and barrier layer.

Record mobilities for a GaN channel without an AlGaN buffer of 1910 $cm^2 V^{-1} s^{-1}$ and 1805 $cm^2 V^{-1} s^{-1}$ were obtained on SiC and AlN substrates, respectively, using 150 nm-thick GaN channels, produced with a two-step process.

Using measurements of the thermal conductivity of the entire device stack and its individual layers, the team determined the thermal boundary resistance and, through TCAD simulations, estimated the hotspot temperature in the channel.

"Comparing identical device stacks grown simultaneously on AlN and SiC substrates revealed that the device on AlN is approximately 20 percent cooler," remarks Darakchieva.

Recently, the team have processed devices on SiC and AlN substrates, and they are now evaluating their performance and thermometry.

REFERENCE
➤ M. Kim *et al*. Appl. Phys. Lett. **127** 032104 (2025)

Mastering the manufacture of HEMTs with an AlN buffer

The performance of RF networks could benefit from a 150 mm GaN foundry process for producing AlN/GaN HEMTs with an AlN buffer

A US collaboration is making tremendous strides towards the commercialisation of AlN/GaN HEMTs with an AlN buffer, grown on SiC substrates.

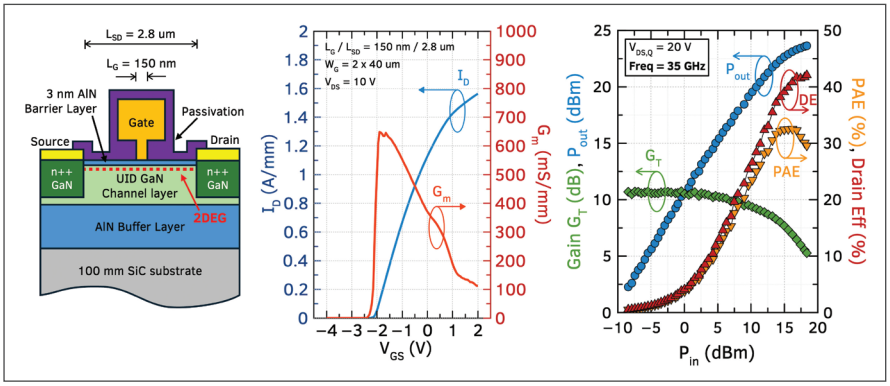
According to the team from Soctera and Qorvo, this class of HEMT has the capability to produce higher output powers at high frequencies than its conventional counterpart that's based on the GaN-buffer, making it an attractive candidate for providing faster communication at gigahertz frequencies. However, up until now, demonstrations of AlN/GaN HEMTs grown on SiC substrates and featuring an AlN buffer have tended to be provided by academic research laboratories, and involve small pieces of substrate.

Addressing this limitation, engineers from Soctera and Qorvo have produced AlN/GaN HEMTs with an AlN buffer and an ultra-thin barrier on SiC substrates using a 150 mm GaN foundry process. These transistors, which have several impressive characteristics, promise to provide the foundation for Soctera to start sampling bare die HEMTs by the end of this year.

According to spokesman for the team, Soctera co-founder and CTO Reet Chaudhuri, his company's contributions have included epitaxial layer design and the epitaxy of the HEMT structure on SiC wafers.

"Qorvo performed the fabrication of the devices using Soctera's epitaxial wafers, utilising their expertise from their 150 nm RF GaN technology," remarked Chaudhuri. "This highlights a strong collaborative effort in advancing the technological readiness of the AlN/GaN/AlN HEMTs."

Fabrication of the collaboration's metal-polar heterostructures began by loading 100 mm SiC substrates into an MOCVD reactor and growing an AlN buffer layer, a GaN channel layer that's less than 200 nm-thick, and a 3 nm-thick AlN barrier layer. None of these layers featured any intentional doping. It's argued that the heterostructure is unlikely to be pseudomorphic, due to a partially relaxed GaN channel layer.



➤ The Soctera-Qorvo collaboration has evaluated drain currents, transconductance, gain, output power and drain and power-added efficiency of AlN/GaN HEMTs.

Electrical measurements of the epiwafers determined that the two-dimensional electron gas (2DEG) has a density of 1.26 x 10^{13} cm^{-2}, a mobility of 1248 cm^2 V^{-1} s^{-1}, and a sheet resistance of 442 Ω sq^{-1}. Across the epiwafer, variation in sheet resistance is just 1.5 percent, indicating a high level of uniformity that enables this material to provide a good foundation for electronic device fabrication.

The team processed their epiwafers into HEMTs with a 150 nm gate length that included re-grown GaN contacts for the source and drain and a Schottky gate electrode defined by electron-beam lithography (see figure for more details).

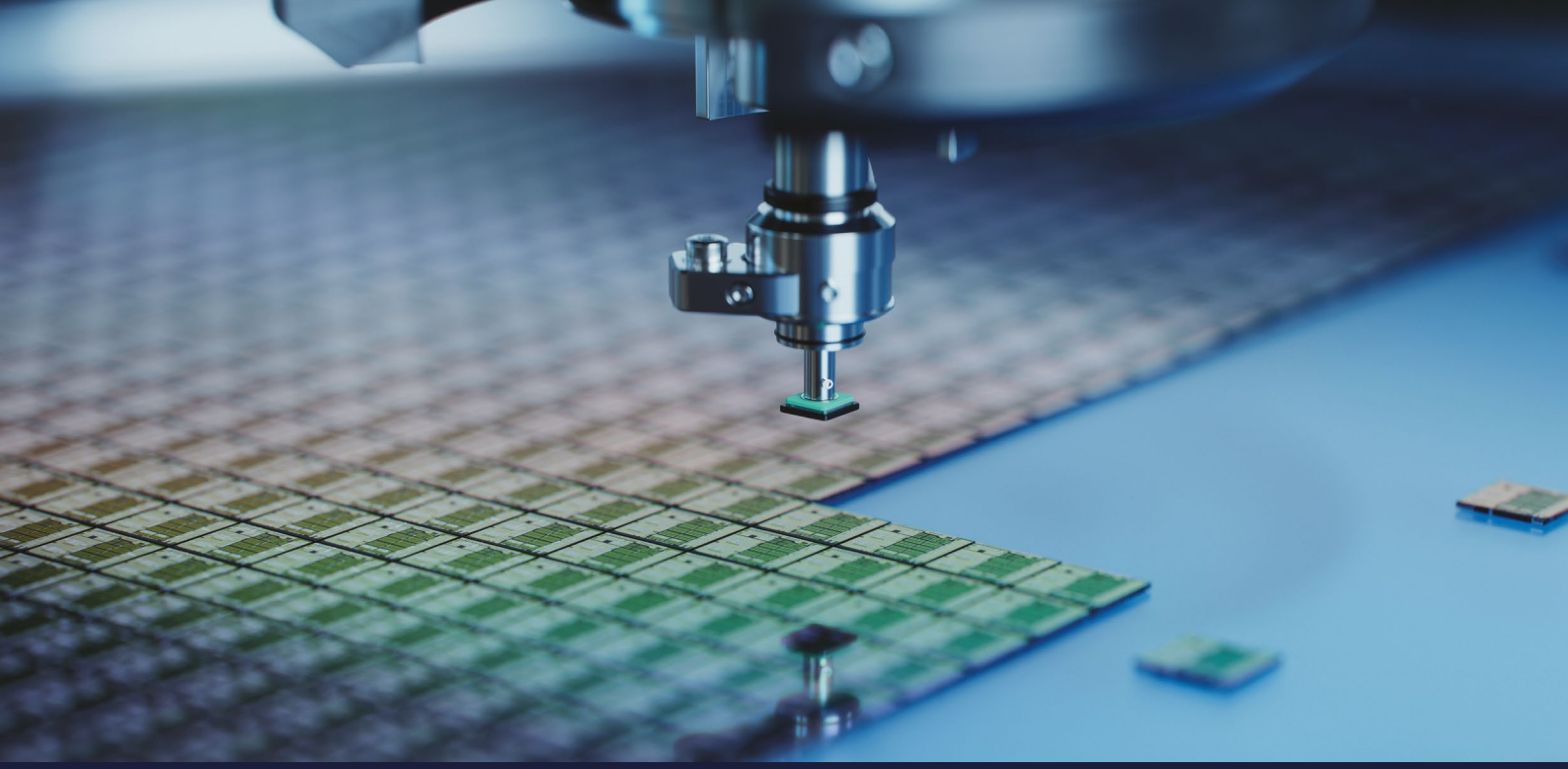
Charcaterisation of the HEMTs determined: an ohmic contact resistance of 0.09 Ω mm; an on-off ratio for the drain current of around 10^6; a peak transconductance of 643 mS mm^{-1}; and normally-on behaviour, with a pinch-off voltage of about -2 V, defined as the gate voltage at a drain current of 1 mA mm^{-1}. Stressing the device for 1 hour at a drain-source voltage of 20 V produced a 10 percent permanent degradation in drain current. Evaluation of large signal amplification determined a power-added efficiency of 32 percent and an output power density of 2.68 W mm^{-1}.

Reet argued that the ultra-low contact resistance and extremely high transconductance of these HEMTs provides a fantastic foundation for building millimetre-wave power amplifiers.

"To translate these metrics to higher output power at Ka-band, reduction of current collapse will be key, which will involve optimisation of the passivation technique for this specific epitaxial structure."

According to Chaudhuri, Soctera will continue to devote efforts towards developing GaN power amplifiers that outperform today's products, in terms of delivering higher powers at cooler operating temperatures. "Our first product devices are going through the production foundry right now, and we anticipate providing samples to interested customers by the end of 2025."

REFERENCE
➤ R. Chaudhuri *et al*. Appl. Phys. Express **18** 076501 (2025)



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