

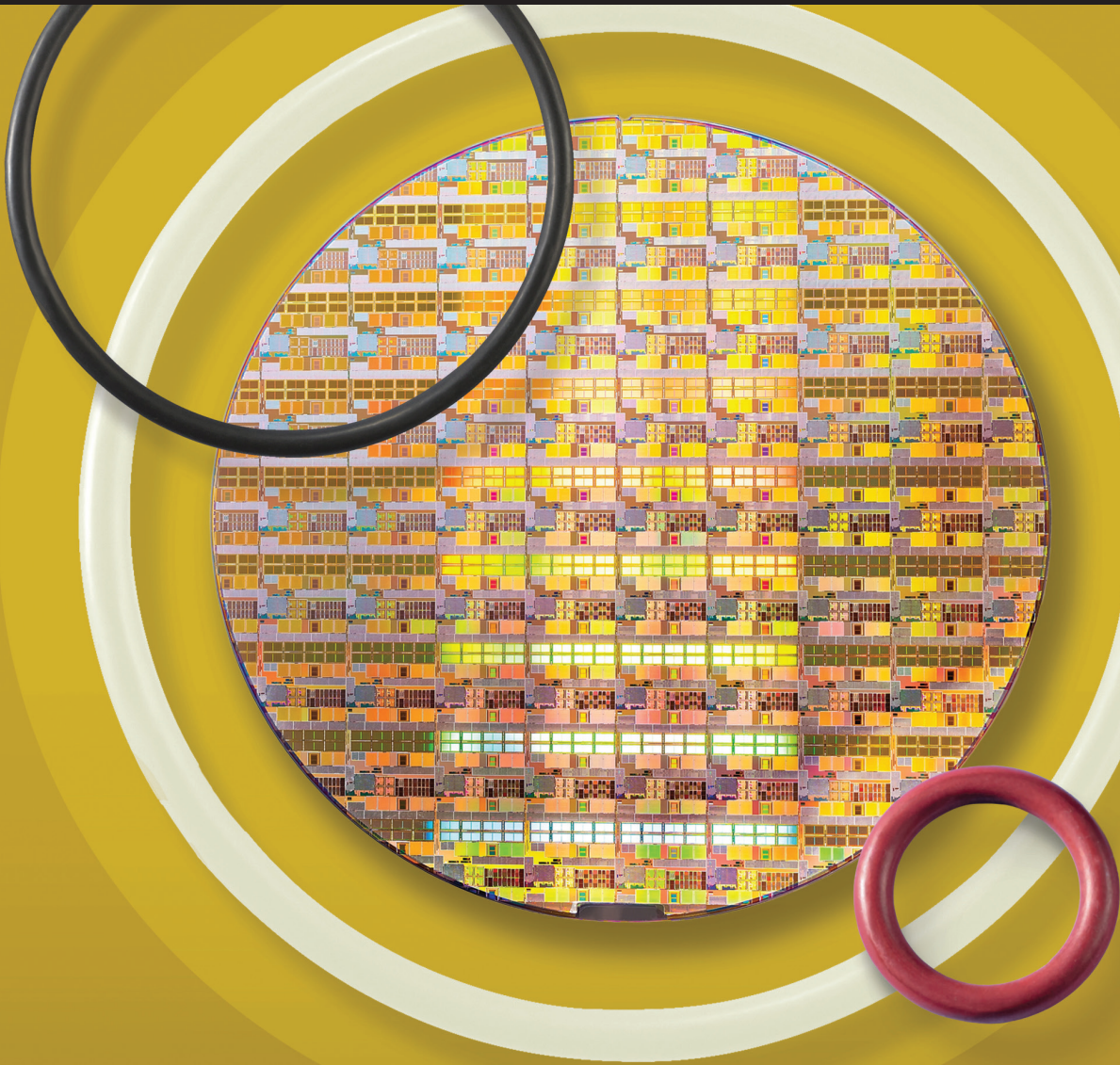


COMPOUND SEMICONDUCTOR

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Growing pains for SiC

Initially, new devices tend to fail to make good profits. Sales will start out low as customers evaluate the new chip, with small volumes hampering economies of scale. And margins are compromised until engineers gain a deep knowledge of the manufacture of the new device, and ultimately maximise yield and throughput.

For SiC power electronics, though, those days are long gone. It's now well over a decade since the first MOSFETs hit the market, and since then strong supply chains have emerged, leading to volume deployment of devices in established applications. So, now is the time when chipmakers should be reaping the rewards for their efforts, and ideally making good returns.

However, it's not all rosy in the SiC industry. While this market is still growing significantly – according to market analyst Yole, it will enjoy a compound annual growth rate of 20 percent through to 2031, by which time global revenue will total \$11 billion – there is significant competition, and margins are not where many wish them to be.

The woes of one of the pioneers of SiC devices, Wolfspeed, are well-documented, and could be summed up by saying it went too hard, too fast. Recently, much effort has been devoted to trying to secure a firmer financial footing, through negotiations surrounding debt, a culling of the workforce, and a new leadership team. So, is Wolfspeed now on the right track? Well, judging by the latest quarterly results, it still has some way to go. Gross margin is well below zero – it's underwater by 20-25 percent, depending on which metric you apply – and there's no expectation of a substantial improvement anytime soon.

For further evidence of tough times within the SiC industry, consider the closing of SK Siltron's Michigan fab, and the resulting loss of 140 staff. For this Korean chipmaker, that's a



significant change in outlook from late 2024, when it secured a \$544 million loan from the US Department of Energy to expand US manufacture of SiC wafers.

But it's not all doom and gloom in the SiC industry. This summer Element 3-5 secured a grant from the European Commission to build a facility for its 'SiCnature' epiwafers, said to feature a very thin, high-quality top layer; and Bosch received funding worth up to \$225 million from the CHIPS Act to produce its SiC trench MOSFETs at a fab in Roseville, CA, that previously produced a range of silicon-based devices (for more details, see p. 14).

As Bosch already has a fab in Reutlingen, Germany, for production of its SiC trench MOSFETs, the new site will provide a second source, reducing risk for this chipmaker.

So, with the likes of Bosch expanding, while others pull back, it's an interesting time for the SiC industry. There's plenty of opportunity for SiC revenue, with demand from the AI industry adding to that from the EV sector. But which firms are going to secure those sales, accompany this with a healthy profit, and avoid the growing pains within this sector?

COVER STORY

Advancing sustainable chipmaking

Drawing on decades of sealing expertise, Greene Tweed is helping fabs to reduce their environmental impact without having to compromise performance, reliability, or yield



18

24 Driving commercialisation of gallium oxide

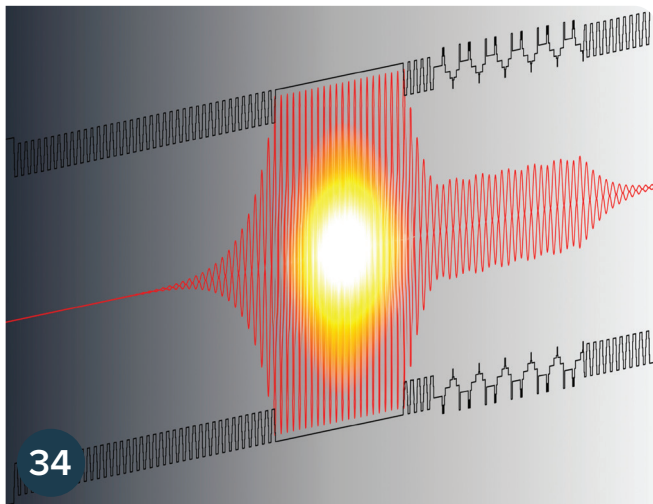
A European supplier of gallium oxide epiwafers is playing a pivotal role in the birth of an ultra-wide bandgap power electronics industry

28 The triumvirate for tomorrow's wireless

Next-generation wireless communication systems will benefit from heterogenous monolithic integration of InGaAs HEMT and GaN HEMT on silicon CMOS chips

34 Transforming lidar with anti-reflective VCSELs

Progressing anti-reflective VCSELs from laboratory prototypes to high-volume production is facilitating cost-effective long-range sensing for automotive lidar



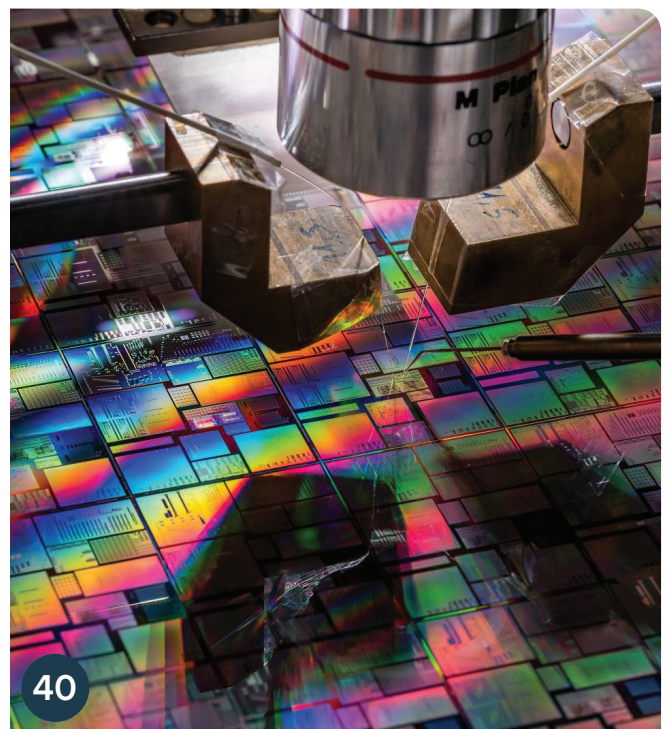
34

40 SiC: A solution for photonics?

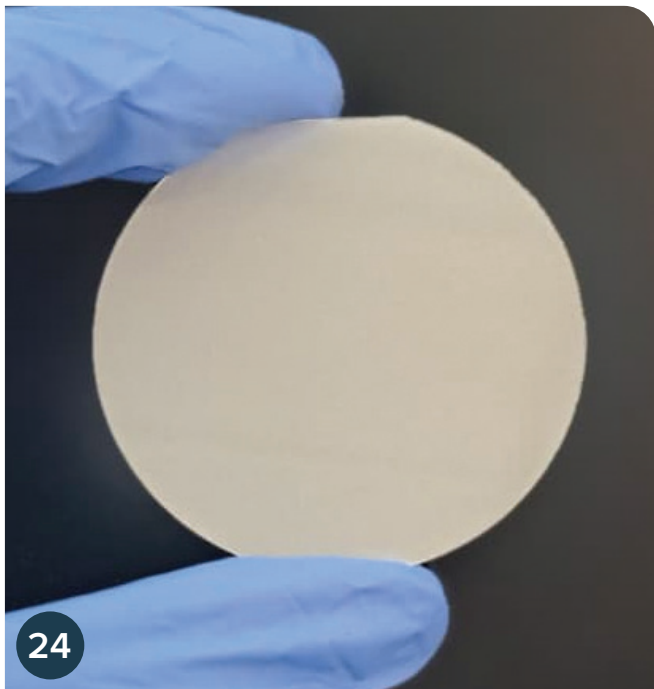
By combining controlled thickness with low defect density and industrial compatibility, Smart-Cut technology is creating high-quality SiC-on-insulator substrates that are opening the door to practical photonic integrated circuits

46 Double duty diamond

Equipping a GaN HEMT with a topside diamond film allows it runs cooler and more reliably, thanks to superior heat spreading and effective passivation



40



NEWS ANALYSIS

14 Bosch boosts SiC capacity

Supported by up to \$225 million from the US CHIPS Act, Bosch is expanding the production capacity of its SiC trench MOSFETs, with devices from its second site in Roseville now out for sampling

RESEARCH REVIEW

51 Revolutionising short-circuit reliability

52 V-defects boost green LEDs efficiency

53 Superior *p*-GaN ohmic contacts

NEWS

06 RF GaN IP competition intensifies

07 NoMIS demos 6.5 kV SiC MOSFET

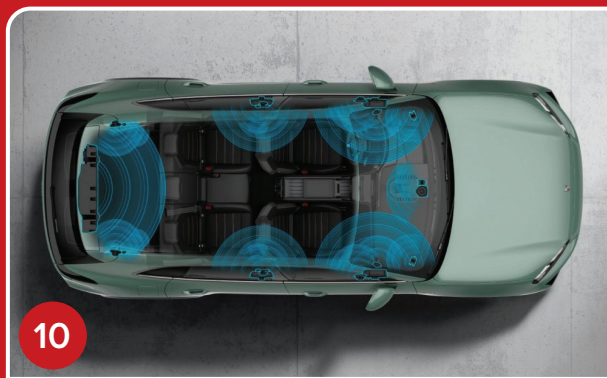
08 Onsemi introduces 'Embedded Power Platform'

09 Sivers invests \$30 million to expand Scottish InP fab

10 Porsche introduces GaN for high end audio

11 IQE announces epitaxy agreement with Quintessent

12 Besxar completes first space flight



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RF GaN IP competition intensifies

Patenting activity is slowing while competition is intensifying in selected technology segments and regions, says KnowMade

RF GaN technology is entering a new phase of growth and strategic competition, according to KnowMade in its latest report, *RF GaN Technology Patent Landscape Analysis 2026*, based on analysis of 5,300 patent families.

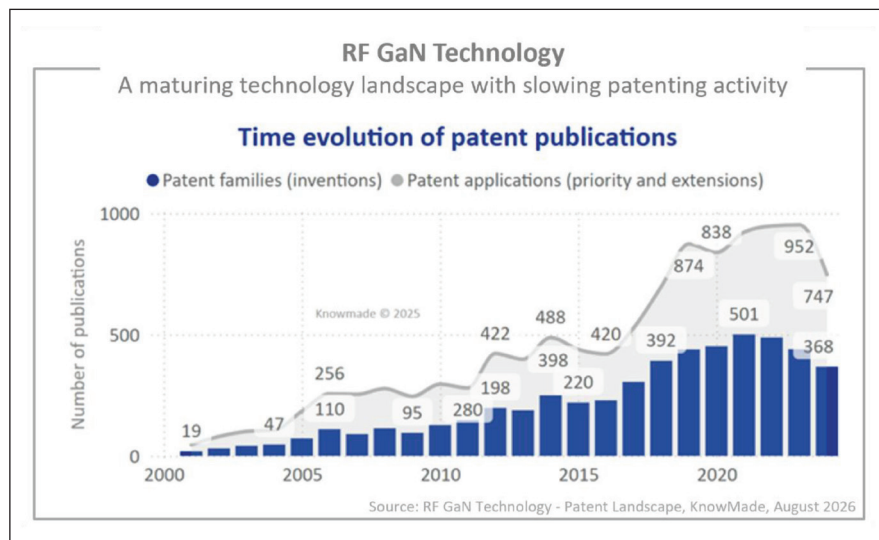
While telecommunications infrastructure remains an important market, demand is increasingly supported by defence, electronic warfare, counter-drone systems and satellite communications.

At the same time, the industrial landscape is being reshaped by consolidation, technology licensing, patent transfers, manufacturing-sovereignty initiatives and restrictions affecting access to critical materials and process know-how.

KnowMade's analysis reveals a dual trend. Overall RF GaN patenting activity is slowing as the technology matures, yet competition is intensifying in selected technology segments and geographic regions. Portfolio breadth, international patent coverage and control of critical process technologies are becoming increasingly important dimensions of IP leadership.

GaN-on-SiC remains the reference platform for high-power telecommunications, radar and electronic-warfare applications. However, substrate availability, manufacturing know-how, long qualification cycles and the transition toward larger wafer diameters maintain high barriers to entry.

In parallel, GaN-on-silicon is progressing from an emerging platform toward early industrialisation, supported by 8-inch manufacturing. Its development could create opportunities in lower-power radio architectures and, over the longer term, in FR3 and 6G applications above 10 GHz. Nevertheless, cost competitiveness, thermal management, reliability, process maturity and scalability remain important technical challenges.



Innovation is also extending toward longer-term platforms such as GaN-on-diamond and GaN-on-AIN, which aim to overcome current thermal and performance limitations. Although their industrial adoption remains constrained by cost, manufacturing complexity and qualification requirements, patent activity can help identify the organisations already building positions in these emerging fields.

Japanese companies continue to hold strong patent positions in RF GaN wafers and epiwafers. Sumitomo Electric and NGK Insulators rank among the established leaders, while Shin-Etsu has emerged as a significant challenger. These portfolios reflect the strategic importance of substrates and epitaxy for device performance, manufacturing control and supply-chain security.

US players retain a particularly strong IP position in devices and downstream technologies. Following the transfer of Wolfspeed's RF business and related patent assets, Macom stands out for the breadth of its IP position across RF GaN devices, packaging and circuits. Its patent portfolio gives the company one of the most comprehensive positions across the value chain and illustrates

how acquisitions and patent transfers can rapidly reshape the competitive landscape.

China's leading RF GaN patent positions remain largely driven by state-backed organisations and academic institutions. CETC and Xidian University are particularly prominent, with Xidian University emerging as the leading domestic patent applicant in RF GaN devices. At the same time, industrial companies, including Huawei, Enkris and Hanhua Semiconductor, are becoming more visible, indicating a gradual diversification of China's innovation base beyond institutional applicants.

Patent protection strategies are also becoming more international.

US companies are increasingly extending their filings into Europe and China, while Japanese players have expanded their patent protection in the United States and China since 2022. Europe is consequently gaining importance as a strategic patent jurisdiction, as companies seek to protect technologies in the regions where RF GaN supply chains, markets and industrial capabilities are developing.

NoMIS demos 6.5 kV SiC MOSFET

Company on track with high-voltage roadmap to 10 kV and 20 kV SiC IGBTs

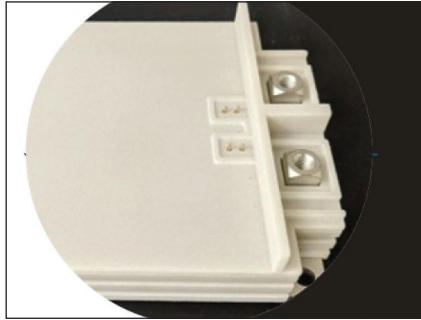
US-BASED NoMIS Power Corporation, a maker of SiC power semis, has announced the successful demonstration of its first 6.5 kV large-die SiC MOSFET.

The device was measured at over 8 kV blocking, 90 mΩ on-resistance, and 55 A drain current. NoMIS says the result carries its planar SiC device technology from its established 3.3 kV devices into the high-voltage class, and establishes a clear, demonstrated path toward the company's forthcoming 10 kV MOSFETs and 20 kV SiC IGBTs.

Currently, NoMIS Power's high-voltage SiC roadmap spans three stages: 3.3 kV in production, 6.5 kV sampling, with 10 kV in development.

The complete 3.3 kV SiC MOSFET family is in production, spanning 80 mΩ (34 A), 50 mΩ (55 A), and 25 mΩ (105 A) devices in TO-247-4L-HC and bare die, complemented by 50-160 mΩ SiC bi-directional switches and a 500 A half-bridge power module.

6.5 kV is sampling now to US-based customers. The demonstrated large-die SiC MOSFET is sampling now for evaluation and anchors an expanding 6.5 kV line, adding on-resistance variants, small-die devices, hybrid



junction-barrier Schottky FET (JBSFET) devices, and standalone diodes. JBSFET construction prevents body diode degradation issues, making it very robust for critical applications.

Target applications include high-voltage direct current (HVDC), solid-state transformers, pulsed power, rail traction, and MW-scale EV charging.

Standard production 6.5 kV parts are scheduled for Q4 2026 and will be available to commercial customers.

10 kV and above is in development, sampling in Q4 2026. The pipeline includes MOSFETs, diodes, hybrid (JBSFET) devices, and SiC insulated-gate bipolar transistors (IGBTs) targeting grid-scale HVDC, next-generation traction, and advanced pulsed power, extending the roadmap toward 20 kV.

"Demonstrating 6.5 kV blocking to over 8 kV proves our planar SiC platform scales cleanly from the 3.3 kV devices shipping today into the high-voltage class," said Adam Morgan, co-founder and CEO of NoMIS Power.

"High-voltage SiC is becoming foundational to data-centre, grid, aerospace, and defence power systems, and it should be built at home – we're building the domestic source the industry can qualify against, from 3.3 kV and 6.5 kV today to 10 kV MOSFETs and 20 kV SiC IGBTs on our roadmap."

The 6.5 kV large-die SiC MOSFET is sampling now to US-based customers for evaluation, with standard production parts scheduled for Q4 2026.

NoMIS Power is engaging system developers on design-in, custom current ratings, and packaging. Teams evaluating high-voltage SiC for HVDC, solid-state transformers, pulsed power, traction, high-power charging, or aerospace and defence platforms can contact NoMIS Power to align to the 6.5 kV, 10 kV, and 20 kV roadmap.

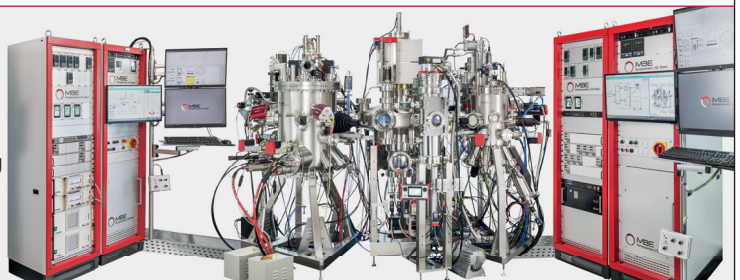
NoMIS Power designs SiC devices, packaging, and power modules at its facility within the Albany Nanotech Complex in Albany, New York.



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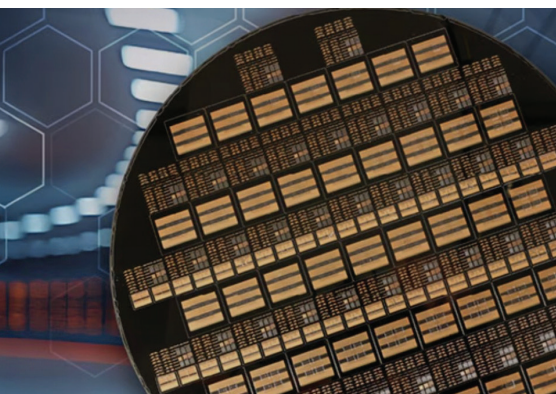
Onsemi introduces 'Embedded Power Platform'

New architecture uses silicon wafer as the package for combining electrical, mechanical and thermal design

ONSEMI has unveiled the Embedded Power Platform (EPP), a new architecture that uses the silicon wafer itself as the package to enable a more integrated approach to power system design.

Designed to be scalable, EPP brings electrical, mechanical and thermal design together from the outset to help customers achieve higher power density, improve system performance and accelerate development in AI, electrification and autonomous applications.

"For decades, the semiconductor and the package have been treated as separate technologies. EPP changes that by making the silicon itself part of the system architecture," said Hassane El-Khoury, president and CEO of Onsemi.



"EPP brings together advanced semiconductor technologies, manufacturing and system-level optimisation into a common architecture that can evolve alongside future innovations. This approach will redefine how power systems are built and create a new foundation for AI infrastructure, electrification and automation."

Onsemi describes EPP as 'reimagining' the package from passive housing into an active contributor to system performance. By using the silicon

wafer itself as the package, EPP enables the seamless integration and interconnection of silicon, SiC and GaN technologies within a highly integrated wafer-level architecture.

Multiple devices, including FETs, drivers and controllers, can be embedded together in a single package and co-optimised for electrical, thermal and mechanical performance. This enables complete power-system co-design, allowing electrical, thermal and mechanical characteristics to be evaluated and optimised together from day one. The result is higher power density, improved system performance, reduced development complexity and faster time-to-market.

EPP uses Onsemi's standard 12-inch silicon wafer manufacturing capabilities, that apply mature semiconductor design tools, wafer-level manufacturing and advanced simulation capabilities to power-system integration, helping improve performance while accelerating innovation.

Subaru Corporation is one of the first early engagement partners for EPP, working with Onsemi to evaluate how the platform could support future electrified vehicle architectures.

Through the collaboration, Subaru will gain early access to engineering samples, simulation models and technical expertise as the companies explore opportunities to improve vehicle performance, streamline development and accelerate innovation.

Onsemi says that EPP replaces that sequential model with a common platform that can be co-designed, co-simulated and co-optimised.

This approach is designed to help customers achieve three-to-five times higher power density, depending on the application. Other benefits include

development cycles as little as four months; better thermal performance and heat dissipation; reduced electrical losses through lower parasitic inductance; and the ability to scale a common architecture across power levels, device types and applications semiconductor technologies

As an example, an early EPP-based solid-state circuit-breaker design for AI was approximately 50 percent smaller and 20 percent cooler than existing designs, according to Onsemi. By reducing packaging overhead and using the full EPP footprint to conduct heat, EPP can support more compact power systems, improve thermal management and enable greater power density in AI infrastructure.

Electric vehicle traction inverters are often constrained by efficiency losses, thermal limitations, development complexity and system size. Onsemi says EPP addresses these challenges with up to four times higher power density and 15 percent lower power losses compared with conventional approaches, enabling smaller, lighter and more efficient inverter designs.

In addition, its scalable architecture supports a single inverter platform spanning low-end to high-end vehicle applications, allowing automakers to reuse a common design across multiple vehicle models and power classes. This approach can reduce R&D and manufacturing costs, accelerate qualification and development cycles, improve vehicle range or lower system costs, and help bring new vehicle programs to market faster.

EPP is expected to begin sampling in 2026 with strategic customers and ecosystem participants across automotive and AI applications.

Sivers invests \$30 million to expand Scottish InP fab

Company to increase facility's output to more than 100 million CW DFB lasers a year

SWEDISH company Sivers Semiconductors has announced a \$30 million investment to significantly expand its InP manufacturing facility in Glasgow, Scotland, as the company prepares for anticipated customer production ramps driven by AI data centre and optical networking demand.

On completion, the expanded facility is expected to support annual production of more than 100 million CW DFB lasers, while adding new process capabilities, increased automation and greater manufacturing flexibility. The expansion program will begin in the second half of 2026 and is expected to become operational in Q4 2027.

Sivers says the investment marks an important step in its transition from a Fab-Lite manufacturing model to a Hybrid Manufacturing strategy, combining expanded in-house manufacturing capabilities with strategic foundry, packaging and manufacturing partners.

"The scale of today's AI infrastructure build-out is creating unprecedented demand across the optical supply chain," said Vickram Vathulya, president and CEO of Sivers Semiconductors.

"Our customers need significantly more laser production capacity and, just as importantly, the confidence that supply will be there when their programs ramp. This investment positions us, along with our foundry partners, to meet that demand."

As hyperscale operators build larger AI clusters and move toward higher-speed networking architectures, demand for advanced optical interconnect technologies is accelerating. Sivers believes InP-based lasers and semiconductor optical amplifiers will play an increasingly important role in enabling the high-performance, energy-efficient optical connectivity required by these systems.

"Scaling photonics for AI infrastructure requires more than increasing capacity.



It requires a manufacturing strategy built for flexibility, quality and long-term customer demand," said Neeraj Chopra, COO of Sivers Semiconductors.

The Glasgow expansion will complement Sivers' broader manufacturing ecosystem, including foundry, packaging and manufacturing partners in Asia.

This Hybrid Manufacturing approach is designed to provide greater production scalability, geographic flexibility and supply-chain resilience while maintaining strategic in-house manufacturing capabilities for Sivers' core photonics technologies.









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Porsche introduces GaN for high end audio

Announces world's first production-ready high-end automotive audio system featuring GaN technology

PORSCHE has adapted GaN technology for its first automotive application in the Burmester 3D High-End Surround Sound System.

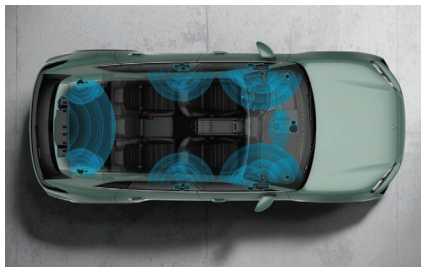
The GaN-based chip handles the voltage conversion required to power the 400-watt subwoofer amplifier. The technology is scheduled to make its production debut in a future Porsche vehicle in 2027.

In Spring 2024, a team from Porsche began work with the Institute for Robust Power Semiconductor Systems at the University of Stuttgart to develop the first prototype of the GaN-based subwoofer amplifier.

"We focused on the fundamental technical challenges of efficient voltage conversion. In a sports car, efficiency and weight are crucial factors," says Lars Heuken, who is responsible for strategic semiconductor management at Porsche. Working closely with an international chip manufacturer and an audio development partner, the team succeeded in creating a production-ready subwoofer amplifier.

To protect the innovations developed as part of the project, Porsche says it has already filed several patent applications.

"The potential is huge – and this is just the beginning. GaN is ideal wherever power is converted," says Heuken. "Many fields of application



are conceivable in Porsche sports cars and we are investigating them in more detail. For example, the semiconductor can be used for power conversion in high-voltage systems."

Heuken says that this makes GaN particularly interesting for the high-voltage systems of electric sports cars, for instance. "Quality and tangible customer benefits are at the heart of all our considerations."

Steffen Buros, who is responsible for audio system innovations at Porsche's Weissach Development Centre commented: "A powerful bass foundation is part of the emotive experience our customers expect from a Porsche. The power reserves of our systems enable confident and dynamic sound reproduction, which is perfectly in keeping with the character of our sports cars."

He added: "We see further opportunities particularly in the field of automotive audio and are already defining the next areas of application."

We focused on the fundamental technical challenges of efficient voltage conversion. In a sports car, efficiency and weight are crucial factors

Belgium holds researcher over GaN espionage case

A 52-year-old man of Belgian and Chinese nationality is in pre-trial detention accused of transferring GaN IP from the company BelGaN to China.

A statement issued by Belgium's Federal Prosecutor's Office has revealed that a 52-year-old man, born in Beijing, and holding Belgian and Chinese nationality, is under investigation for suspected theft of IP and trade secrets relating to GaN chip production from the Belgian chipmaker BelGaN.

The person, who is accused of transferring the IP to China, is in pre-trial detention at Oudenaarde prison. He was arrested at Zaventem National Airport on the 11th May 2026, just before his return flight to Beijing.

The arrest took place as part of an investigation being conducted by the East Flanders Federal Judicial Police into, amongst other things, espionage, participation in a criminal organisation, misuse of company assets and the unlawful disclosure of company secrets.

The investigation forms part of the insolvency case relating to BelGaN, formerly based in Oudenaarde, and declared bankrupt on 31 July 2024.

The press statement says they are indications that the person concerned, who held a senior research position within BelGaN, was simultaneously acting as a director of a Chinese company engaged in a similar manufacturing activity, which had been established a few months after he joined the company and was financed by a Chinese investment fund.

IQE announces epitaxy agreement with Quintessent

IQE to supply 6-inch GaAs epiwafers through foundry-ready service as QD Laser tech moves to customer sampling

COMPOUND SEMICONDUCTOR wafer firm IQE has announced a purchase agreement with Santa Barbara-based Quintessent for the supply of Quantum Dot Laser (QDL) epitaxy.

Following an initial announcement and purchase order in January 2025, the extension of the companies' long-term relationship will see IQE supply 6-inch GaAs epiwafers through its foundry-ready service. This will support Quintessent's customer sampling as its technology progresses towards commercial deployment and new production introductions.

Compared to traditional laser technology, Quintessent's QDL architecture is designed to enable lower power optical interconnects, simpler manufacturing and improved reliability for next-generation AI data centres.

IQE and Quintessent have been working together for over a decade to transition the technology from research to large-scale production and previously announced a partnership to establish the world's first large-scale QDL epitaxial wafer supply chain.



Jutta Meier, CEO of IQE, commented: "After a period of successful development, we are pleased to be enabling customer sampling with our partner Quintessent as its Quantum Dot Laser technology moves towards broader market adoption and commercialisation. IQE's proven expertise in advanced epitaxy and high volume manufacturing means we are ideally positioned to support the scaling of multiple complementary optical interconnect technologies that are enabling the AI revolution."

Alan Liu, CEO and co-founder of Quintessent, commented: "We are proud of our long-standing partnership with IQE. The next phase of the AI infrastructure buildout will require deep technology and supply chain partnerships to address the scale required in the AI ecosystem."

Liu added: "IQE has been a wonderful production partner, helping Quintessent enable our Laser and SOA technology. We look forward to continued collaboration with IQE."

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HESTIA

Besxar completes first space flight

Washington DC start-up takes first steps to semiconductor manufacturing in Space

BESXAR, a Washington DC-based start-up with aims to make semiconductor materials in Space, has reported the results of its inaugural flight: Besxar Flight-1 'Mission Asimov.'

On July 5, 2026, two Besxar-built 'Clipper-class' canisters flew aboard a SpaceX Falcon 9 first stage booster and were recovered intact after the booster returned to land.

It was the first flight carrying custom wafer cartridges, power, avionics, and printed-circuit hardware that Besxar designed and built in-house, all of which qualified on the first attempt.

The mission carried GaN-on-sapphire, undoped silicon, and bare sapphire wafer samples from Besxar, in addition to GaAs and AlInAsSb wafers from academic research partners at the University of Virginia (UVA) and the University of Texas at Austin (UT Austin).

Besxar's primary test objective for Flight-1 was the viability and performance of the canister design in admitting vacuum – in short, does it work as a cleanroom? The canister needed to: maintain structural integrity through all phases of flight, re-entry, and recovery; allow vacuum into the canister during flight to expose test materials; and prevent contaminants from entering the canister. Post flight testing indicates that Besxar's canisters performed as expected.

Besxar also tested the canister design's ability to carry wafers safely through the entire flight profile. The canisters flew multiple wafer samples of varying compound semiconductor materials, and initial analysis indicates that none sustained damage. Besxar engineers examined the wafers and canister interiors against pre-flight markers and found no cracking, no warping, and no visible damage. Substrates flown for UVA and UT Austin are currently undergoing independent analysis at the



material level that may yield additional data on the effects of vacuum exposure on compound semiconductor materials and their manufacturability.

Besxar's ultimate in-space manufacturing process will be fully autonomous, which requires significant real-time data and testing infrastructure. The company built the initial foundation of that data collection system for Flight-1 and says it will expand it across subsequent flights and, eventually, operations. The company says that the data system performed well. Besxar was able to collect pressure, acceleration, thermal, vibration and shock data for the entire mission. One canister performed as expected. The

second had an anomaly when recording flight data. Besxar says it is completing its anomaly review ahead of the next flight.

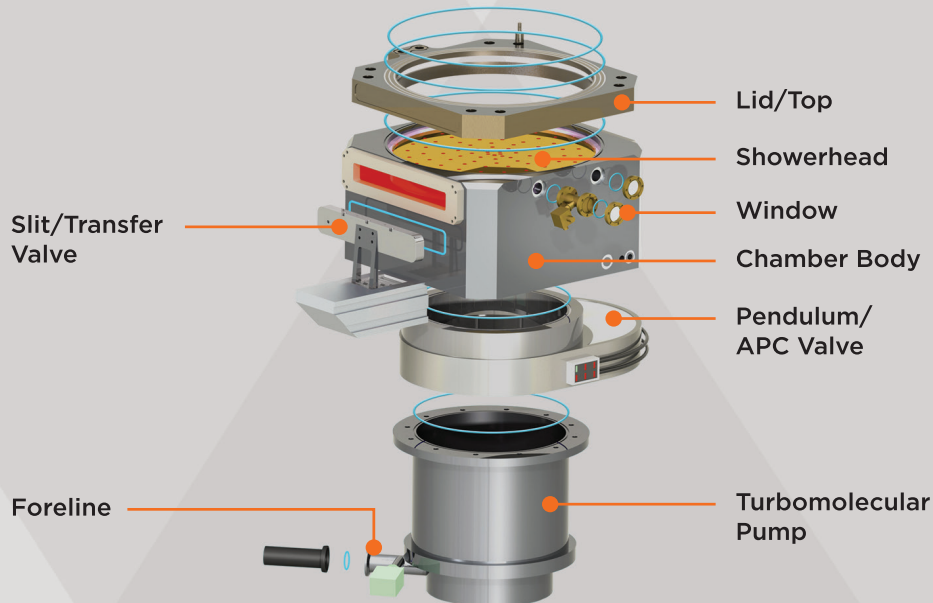
"This is an achievement we're incredibly proud of. In just nine months, we've been able to design and test initial key capabilities for our in-space compound semiconductor wafer manufacturing technology," said Ashley Pilipiszyn, founder and CEO of Besxar. "We proved that the hardware is viable and that our systems can survive the extreme swings of spaceflight. Now we have real data and, more importantly, a team with payload integration, spaceflight, and recovery heritage that will only accelerate our work as we take on the next set of technical milestones on our roadmap."

"This mission and future flights are financed by Besxar's early investors. Ahead of the mission, the company raised a \$10.3 million seed round led by Dauntless Ventures alongside Overture VC, Keymaker VC, 645 Ventures, Singh Capital Partners, Koru Capital, Plum Alley Ventures, Mana Ventures and Earthrise VC, bringing total funding to \$14.7 million.

Besxar's primary test objective for Flight-1 was the viability and performance of the canister design in admitting vacuum



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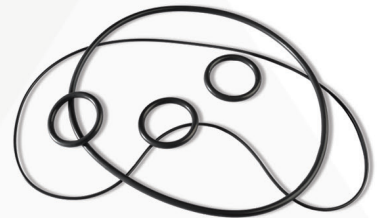
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Bosch boosts SiC capacity

Supported by up to \$225 million from the US CHIPS Act, Bosch is expanding the production capacity of its SiC trench MOSFETs, with devices from its second site in Roseville now out for sampling

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

WHEN CHIPMAKERS want to increase their capacity, they have a number of options at their disposal. They can invest in tools with higher throughput, possibly in conjunction with expanding the footprint of a fab. Or they can build a new fab, or even buy an existing facility.

Going with the latter is power electronics manufacturer Bosch. This European chipmaker recently bought silicon fab in Roseville, CA, and is now investing \$2 billion in this facility, where it will ramp production of its SiC trench MOSFETs. These devices, with a smaller footprint than their planar cousins, are produced using the Bosch process, which involves a high-aspect-ratio etch. To accelerate the production ramp of these devices, engineers at the site are drawing on processes already employed for SiC MOSFET production at Bosch's established fab for SiC chip production in Reutlingen, Germany.

The Roseville facility has a rich history in semiconductor chip production. Built by NEC in 1984, ownership initially transferred to Renesas, before Telefunken bought the facility in 2011. The latter used the fab for chip production on a 200 mm line that primarily manufactured high-voltage and low-voltage devices based on silicon-on-insulator structures. In addition, the fab produced silicon IGBTs and MOSFETs, and SiGe-based devices, all typically at the 0.25 µm node.

Acquiring this site to expand Bosch's production of SiC trench MOSFETs has merit on a number of fronts, according to seasoned engineer Dan Marrujo, who has intimate knowledge of this facility, recently held the role of chief strategist at Sacramento's Defense Microelectronics Activity, and had been working with investors to ensure that the Roseville facility can be

accredited under the US Department of War's Trust Accreditation Programme.

Marrujo points out that as well as increasing capacity for chip production, having a second site for making SiC trench MOSFETs reduces the risk associated with catastrophic unknown events. For example, if a delay hampered the installation of a new tool in Reutlingen, devices could be produced in Roseville.

Another advantage of acquiring the Roseville site is that it gives Bosch an existing engineering ecosystem. "It's not a greenfield facility, where people are having to learn how things are or are not going to work."

Having the facility already equipped with 200 mm tools is a huge benefit in the current climate, according to Marrujo, given the long lead times associated with tool purchases, which are impacted by high demand and tariffs.

While it's not possible to replicate Reutlinger's line exactly, the team at Roseville can 'copy smart', using existing and established recipes, fine-tuning them for their set of tools.

As well as production tools, the Roseville facility is equipped with what Marrujo describes as a world-class set of testing capabilities. "They have everything from wafer-level testing to select package-level testing."

Thanks to this capability, which allows engineers to assess environmental and thermal stresses on components, the fab can quickly ramp to full-rate production.

According to Marrujo, yet another advantage of Roseville acquisition is that it comes with 'once-in-a-generation' timing.

"You have a heavily invested site from the Japanese, prior to the ownership of Telefunken TSI, and the CHIPS Initiative working with the Department of Commerce to ensure that there were grants to help with the cost of that facility."

Marrujo understands that support from the Department of Commerce, worth up to \$225 million, is more competitive than any bank can provide. Thanks to funding on very attractive terms, Bosch has a wonderful opportunity to expand its customer base and develop new products.

Further support for Bosch's Roseville acquisition has come from the Greater Sacramento Economic Council (GSEC).

"GSEC made this a priority within the region. It has allowed Bosch to not only hit the ground running, but see the opportunity space grow, as they want to grow the site," says Marrujo.

Bosch will initially invest up to \$2 billion at the Roseville site, and is already sampling SiC MOSFETs produced at this facility.

Marrujo expects that as this chipmaker

progresses from 'short-loops' to full-rate production, it will draw on baseline data from the German fab, and allow customers to evaluate SiC devices with a range of fidelities.

Final capacity at Roseville is unclear. Bosch's investment of up to \$2 billion could be the first of many, with customer demand ultimately determining this facility's final footprint.

"There's so much land that's available there," says Marrujo, who adds that the expansion could be aided by a central utility plant that's oversized.

Prime location

For any chipmaker, high-quality device production is not just dependent on great tools and processes – skilled and dedicated staff are needed to run them.

Fortunately, Sacramento is home to many manufacturers of memory chips, including Micron, Samsung, Western Digital and Solidigm – in fact, it has more fabs than Silicon Valley. The addition of Bosch to this list will help to strengthen the local semiconductor ecosystem, and allow engineers and technicians to advance their careers without having to leave California.

In this regard, success breeds success, encouraging other companies operating in the semiconductor supply chain to set up satellite offices in Sacramento, and even headquarters. The result is an

ever-expanding semiconductor cluster.

The chipmakers in and around Roseville are already working together, supported by the regional government.

Helping such efforts are local academic institutions, responding to the launch of Bosch's second site for SiC trench MOSFETs. This includes: Sierra College, which is adding mechatronics courses to support students who wish to develop skills that are needed at the Roseville site; and Sacramento State, which is considering overhauling its electrical engineering department, with an increased focus on ruggedized technologies through a programme called WARPTEN. Further afield, but still within a 100-mile radius of Roseville, is Berkley University – Bosch is drawing on its expertise.

Local beneficiaries

As production of SiC MOSFETs ramps at the Roseville fab, this facility will take on more staff, providing employment for hundreds of local people.

While it is not possible to know where every chip will go, it's likely that a significant proportion will be deployed domestically, within the US electric vehicle sector. And that's surely good news for those overseeing the implementation of the CHIPS Act, as it strengthens native production of an increasingly important device, the SiC MOSFET.



➤ The Roseville site that Bosch has acquired is equipped with a central utility plant that is oversized in many aspects.

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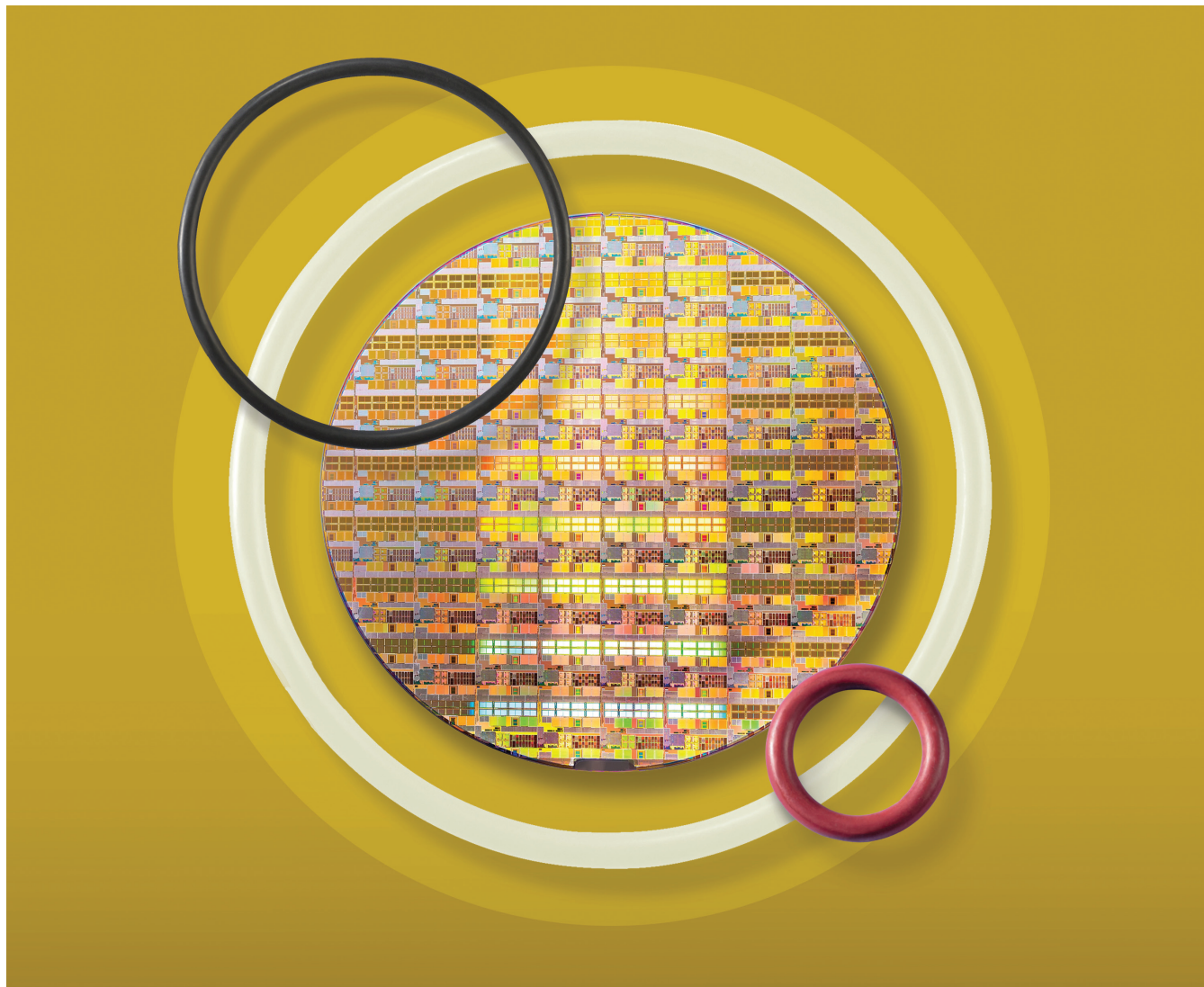


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Advancing sustainable chipmaking

Drawing on decades of sealing expertise, Greene Tweed is helping fabs to reduce their environmental impact without having to compromise performance, reliability, or yield

**BY THYAG SADASIWAN, HENRY MA, AND
ALAN MAHER FROM GREENE TWEED**

THE COMPOUND SEMICONDUCTOR industry is helping to transform our world. Thanks to the uptake of GaN and SiC high-efficiency power electronics, we have more efficient electric vehicles and renewable energy systems, while the deployment of InP and GaAs lasers and RF transistors is underpinning high-speed communications infrastructure, connecting our increasingly digital world.

Yet the fabs that make these chips, and the suppliers that support them, remain resource-intensive, and are having a significant impact on the environment. Chipmakers are using a number of process gases that threaten to harm the climate. They consume a great deal of water and energy, and they generate emissions throughout their operations and supply chains.

With governments, customers, and investors placing greater scrutiny

on environmental performance, manufacturers of all forms of semiconductor device are under increasing pressure to trim their emissions, minimise waste and improve resource efficiency – and in conjunction, demonstrate progress toward sustainability targets.

Unfortunately, it's not possible to fulfil these goals with a single breakthrough. What's needed is a series of improvements, spanning equipment design, materials selection, process optimisation, and supply chain collaboration.

Playing a critical role in addressing this overarching objective are suppliers of equipment, including their consumables. Inside a fab, every component contributes to this facility's total environmental footprint, whether through energy consumption, maintenance requirements, material usage, equipment uptime, or process reliability. That includes sealing solutions, which have a significant influence on emissions containment, contamination control, equipment longevity, and waste reduction.

Component-level sustainability

For decades, our company, Greene Tweed, has worked with semiconductor and semiconductor equipment manufacturers to solve some of the industry's most demanding sealing challenges. Today, that expertise helps our customers to build more sustainable fabs that are not compromising

performance, reliability, or yield. As a prominent supplier of industry-leading Chemraz sealing solutions that outperform and outlast in the world's harshest semiconductor manufacturing applications, we help fabs comply with a Scope 3 emissions profile (this metric offers a complete breakdown of all indirect greenhouse gas emissions that occur across a company's entire value chain).

High-performance sealing solutions, such as our Chemraz FFKM and Fusion FKM, are engineered to withstand aggressive chemistries, extreme temperatures, and demanding process environments. Our solutions can contribute to both operational efficiency and environmental performance by helping contain process gases, extend maintenance intervals, reduce unplanned downtime, and support longer equipment life. As our engineering decisions have a direct and measurable impact on our customers' sustainability performance, we take that responsibility seriously.

Our approach extends beyond product durability. We are also advancing material solutions that are Non-Fluorosurfactant (NFS)-compliant; exploring circularity initiatives, such as FFKM recycling; and developing technologies that empower our customers to monitor their equipment performance and optimise maintenance practices. Collectively, these initiatives are enabling a reduction in the environmental impact of semiconductor manufacturers, while maintaining the

process control and reliability that advanced device production demands.

Real sustainability gains come from thousands of small engineering decisions made throughout the fab. While material selection, sealing performance, equipment reliability, and lifecycle management are rarely the most visible aspects of a sustainability strategy, all have a substantial impact. Through continued innovation in materials science, sealing technology, and responsible manufacturing, we are supporting semiconductor manufacturers to transition to a more sustainable future.

Enabling greener fabs

For semiconductor manufacturers, there are few sustainability topics generating more discussion than those surrounding per- and polyfluoroalkyl substances (PFAS). Concerns surrounding these classes of material are related to evaluations throughout the world by regulatory agencies, which are considering restrictions on various PFAS substances. This scrutiny creates uncertainty for an industry that's, for many years, been relying on fluoropolymer materials for some of its most demanding applications. Addressing these challenges requires both urgency and precision. PFAS is a broad class of chemicals with diverse properties and applications. Note, though, that fluoropolymers, such as those used to make our Chemraz and Fusion portfolios, are considered polymers of low concern.





The uncertainty surrounding the future of PFAS is weighing heavily on fabs. They are striving to strike a perfect balance between preparing for changing rules, while avoiding a hit to process stability, contamination control, uptime, or yield. To help them navigate through these choppy waters, we are pursuing a multi-pronged proactive strategy that's focused on material innovation, supply chain collaboration, and customer qualification support. Keys to our approach are an absence of polymerising fluoropolymers and the removal of fluorosurfactants from our manufacturing processes. We are working closely with suppliers to transition toward NFS across our material portfolio.

In conjunction with this strategy, our materials scientists are developing next-generation alternative materials and solutions capable of meeting the demanding requirements of semiconductor applications. Recent efforts have been directed at PFAS-free elastomers, designed to operate at temperatures up to 180°C; and high-performance thermoplastic composites, engineered for maintaining strong chemical and wear resistance while operating at temperatures exceeding 300°C.

As well as material development, we are contributing to qualification, a critical part of the transition process. Working directly with our customers, OEMs, and fluoropolymer manufacturers, we are evaluating new materials under real-world operating conditions. We are already supplying

NFS-based materials for testing and qualification programmes – this is helping fabs to assess performance and accelerate adoption where feasible.

One of our goals is to transition most of our FKM and FFKM compounds to NFS formulations by 2030, or sooner where technically feasible. We are also aligned with broader industry initiatives, including the Semiconductor PFAS Consortium, which is advancing science-based approaches to PFAS management throughout the semiconductor value chain.

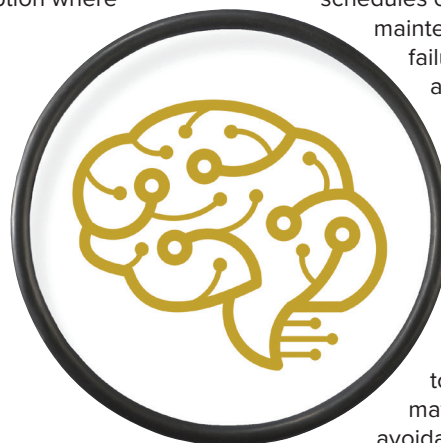
For manufacturers of compound semiconductor devices, the ultimate goal is not simply compliance. We know that chipmakers want to reduce risk while preserving the key metrics to fab performance: reliability, process control, and yield.

Predictive smart seals

Those running fabs increasingly see sustainability as going hand-in-hand with operational efficiency. When equipment performs reliably for longer periods, fabs consume fewer replacement components, generate less waste, reduce maintenance interventions, and maximise the value of resources already invested in production.

A significant weakness of traditional seal maintenance practices is that they often rely on fixed replacement schedules or reactive

maintenance following failure. While this approach reduces some operational risk, the downside is that perfectly functional components are removed long before the end of their useful life. This leads to unnecessary material consumption, avoidable waste, and costly downtime.



Semiconductor manufacturers are looking to avoid these pitfalls as they pursue smarter, lower cost, more sustainable operations. To support their endeavours, we have developed an intrinsically sensing seal material that's capable of providing real-time insight into seal health. As these novel seals experience compression, wear, aging, and process exposure, an electrical signal is generated, which changes predictably. By monitoring this response, equipment operators gain a better understanding of the actual condition of a seal, without having to open a process chamber or rely solely on an elapsed service time.

For makers of compound semiconductor materials and devices running high-value process tools, these insights extend well beyond

sustainability. Superior visibility into seal performance helps reduce unexpected failures, increase uptime, protect yield, and cut the total cost of ownership. In an industry where disruptions, however brief, have significant operational consequences, greater predictability creates substantial value.

Our informative seal technology has valuable long-term potential. As fabs continue to invest in automation, as well as Industry 4.0 initiatives and digital transformation, the seal health data provided by our technology can form a key part of a broader ecosystem of connected equipment intelligence. When integrated with AI-driven analytics, smart seals promise to support predictive maintenance strategies, process optimisation, and even digital twin environments that are capable of simulating equipment behaviour before failures occur.

For semiconductor manufacturers, initiatives such as our seal technology deliver a powerful combination of environmental and operational benefits. They allow components to be used more efficiently, maintenance to become more targeted, and equipment performance to become more predictable. In an industry where reliability, yield, and sustainability are increasingly interconnected, smart sealing offers a glimpse into the future of intelligent fab operations.

Recycling and circularity

Due to the exceptional chemical and thermal resistance of FFKM seals, they are extremely difficult to recycle. That's a concern, as fabs are pursuing circularity initiatives, and are placing a premium on recovering value from these high-performance materials.

One of the reasons why it is so challenging to recycle FFKM is that the material properties that make these polymers valuable inside semiconductor equipment also hamper efforts to reclaim and



reprocess. Successfully recovering and reusing these materials demands deep expertise in both fluoropolymer chemistry and semiconductor process requirements.

Working with a leading semiconductor manufacturer, we have demonstrated the technical feasibility of recycling FFKM O-rings into renewed high-quality sealing materials that are suitable for both demanding semiconductor and general industrial applications. These efforts address one of industry's most challenging materials recovery problems. At the same time, they are offering a potential pathway toward greater circularity within semiconductor manufacturing.

Our roles in this initiative have included evaluating recycling technologies, developing manufacturable compounds that contain recycled FFKM content, and validating performance characteristics against demanding requirements expected of critical sealing applications.

For fabs, this programme is creating a tangible opportunity to enhance

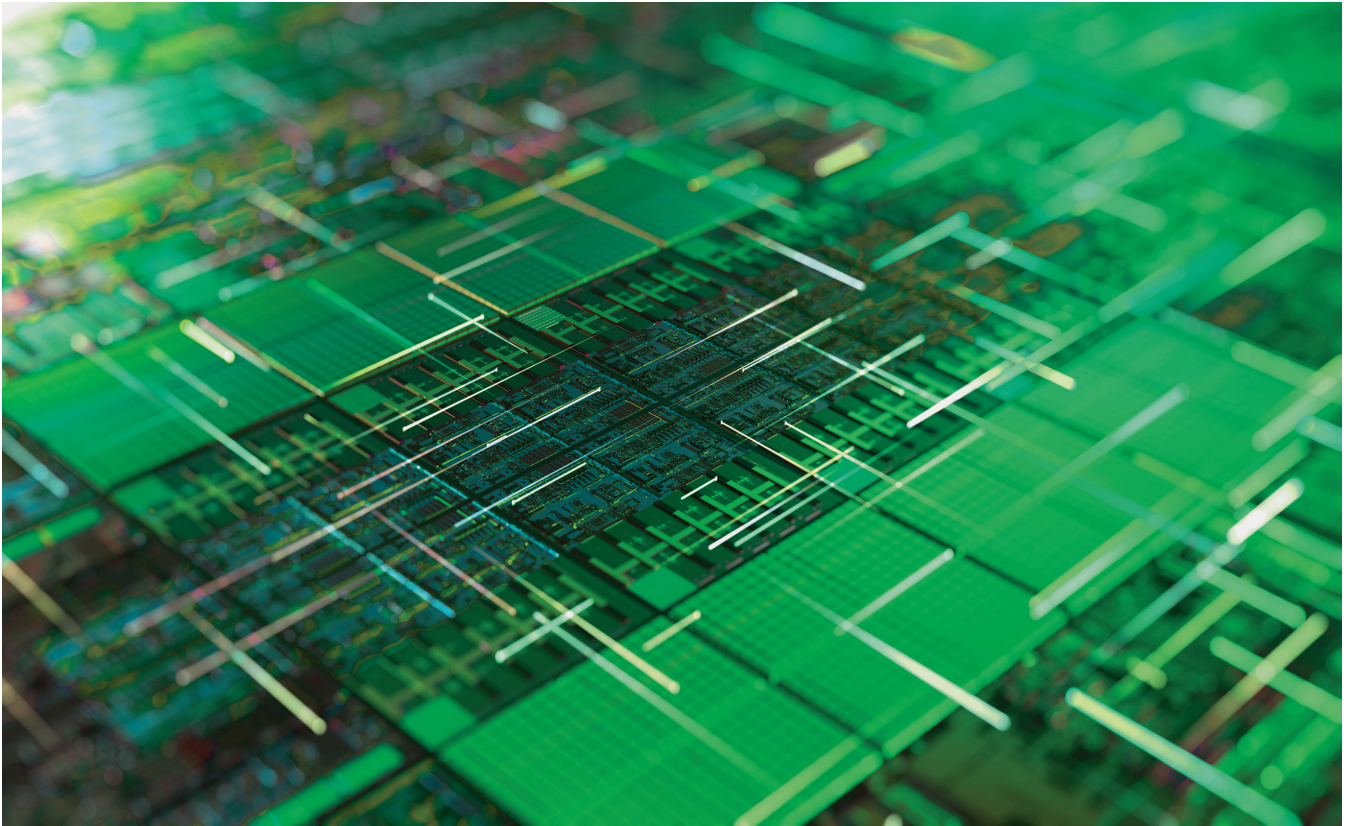
sustainability through verified material circularity, while maintaining seal performance without compromise, and potentially reducing total cost of ownership.

Beyond materials and sourcing, we are working closely with customers to identify sustainability improvements across the broader semiconductor supply chain. In partnership with a leading OEM, we are helping develop and implement a returnable packaging programme that's aiming to replace single-use shipping materials with reusable packaging solutions. Following multiple rounds of testing and deployment across a number of locations, this initiative is helping to reduce packaging waste, support customer sustainability objectives, and advance more circular logistics practices without compromising product quality or operational efficiency.

Sustainability beyond our products

Efforts to improve sustainability should not begin and end with the products used inside the fab. Semiconductor manufacturers are increasingly

For makers of compound semiconductor materials and devices running high-value process tools, these insights extend well beyond sustainability. Superior visibility into seal performance helps reduce unexpected failures, increase uptime, protect yield, and cut the total cost of ownership



concurring with this view, and as part of their own sustainability commitments, they are evaluating the environmental performance of their suppliers and broader value chains.

We hold these values high, and are integrating sustainability across our operations, facilities, supply chain, and logistics network. These efforts are helping us reduce our environmental impact, while supporting our customers that are seeking to improve the sustainability performance of their supply chains, and address Scope 3 reporting requirements.

One example of this mindset is our global manufacturing network. By strategically locating our production closer to customer demand centres, we are reducing transportation requirements, while shortening lead times and trimming our emissions associated with the shipping of products around the world.

We are also rolling out programmes that reduce waste in packaging and logistics operations. In partnership with a leading OEM, we are helping develop and implement a returnable packaging solution designed to replace single-use shipping materials with reusable transport containers. The initiative has

successfully completed multiple testing and implementation phases across customer sites, demonstrating how supply chain innovation can cut waste while maintaining product protection and operational efficiency.

Within our own facilities, we are continuing to pursue projects that increase resource efficiency and reduce our environmental impact. For example, at our Korean facility, we have introduced greywater recycling. This initiative is helping drive down freshwater consumption and support more responsible water management. This effort reflects a broader focus on identifying practical opportunities to reduce resource use while maintaining operational excellence.

Recently, we have been awarded an EcoVadis Committed. This reflects our progress related to sustainability. In this regard, we are already building on a strong foundation, while making continuous improvements across environment, labour and human rights, ethics, and sustainable supply chain practices.

Taken together, these efforts demonstrate that sustainability extends well beyond the fab floor. Through

responsible operations, supply chain collaboration, resource efficiency initiatives, and long-term product design, we are working to reduce our own environmental footprint while helping customers advance theirs.

Bring us your challenges

We view sustainability as a shared responsibility. We have to play our part, alongside our customers, partners, and the broader semiconductor ecosystem.

As the compound semiconductor industry scales to support electrification, renewable energy, communications, and clean energy technologies, the fabs making the devices to support these applications must employ practical solutions that improve environmental performance without compromising reliability, yield, or process control. The goal of sustainability is an evolving, complex target.

We have several projects and customer co-innovation programmes to help fabs achieve their sustainability goals. Together, we are leveraging resources, from R&D through to operations, in our joint commitment to sustainability.

Bring us your challenges.

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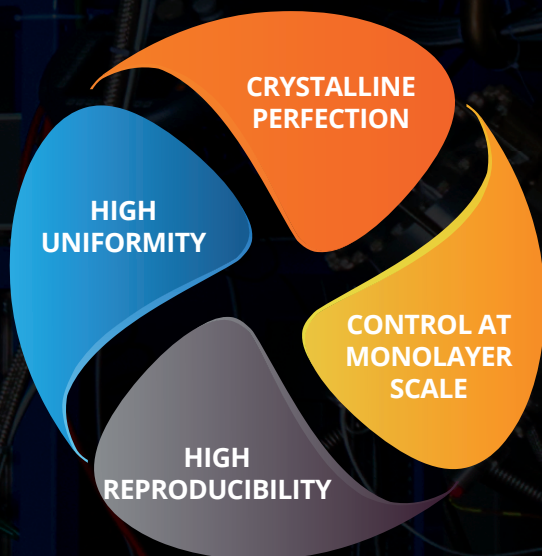
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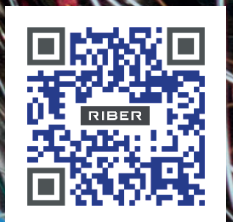
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Driving commercialisation of gallium oxide

A European supplier of gallium oxide epiwafers is playing a pivotal role in the birth of an ultra-wide bandgap power electronics industry

TWO CO-FOUNDERS OF NEXTGO EPI TALK TO EDITOR OF CS MAGAZINE, RICHARD STEVENSON

RS: *Andreas Fiedler, as a co-founder of NextGO Epi, and someone who has been working on this material for a decade, you have been championing the promise of gallium oxide in power electronics for many years. Where do you expect this oxide to make the biggest impact?*

AF: Right now, in solid-state transformers. The more renewable energies in our grid, the more we have to deal with smart grids and routing our grids, because of fluctuations from renewable energies. So far, this has been covered by big wheels in steam-based power plants, but since we want to get rid of those, because they

typically produce steam by burning something we don't want to have in our atmosphere, we need solid-state transformers to handle our grid. You need a semiconductor that can help you manage above 10 kV at a high-power level. Gallium oxide has the potential to fulfil that need.

There's not enough material on the market yet. The research community was basically supplying material for itself, to get research done. Now big players want to jump in. Someone has to fulfil the need, and we can do this. We have to build a gallium oxide sub-supply chain, just for Europe, to be resilient for whatever will come.

RS: *Ta-Shun Chou, as CEO of NextGO Epi, you have your finger on the pulse of the gallium oxide industry. How would you describe the current state-of-play?*

T-S. C: From 2022, multiple suppliers started supplying at least 4-inch gallium oxide. Now more start-ups and companies are showing interest, from China, Japan, Taiwan and the USA. This year we see 6-inch and even 8-inch gallium oxide demonstrated. We believe that we are now in the transition phase. Industrial players are prototyping, showing that gallium oxide can be a competitor to silicon carbide and gallium nitride, rather than a cool material in published papers. Most likely, in the next 2 or 3 years, you will see the first gallium oxide product come out.

RS: *Why is now the right time to have the emergence of NextGO Epi, a gallium oxide epiwafer supplier in Europe?*

T-S. C: First, for semiconductor material, size matters. Now we see more 4-inch and 6-inch substrates available, and the price is coming down.

Our customers and partners are saying, 'I want to try gallium oxide. May I have some epiwafers?' This indicates that there's a bottleneck in getting high-quality, large-diameter epiwafers.

Our partner, Aixtron, has a gallium oxide MOCVD tool on the market.

All three factors encouraged us to push the NextGO Epi further.



➤ The Aixtron CCS system with which NextGO Epi produces its Ga₂O₃ epiwafers.

For epitaxial businesses, this business usually only exists at the beginning of a new material generation. If you come too late, there's no place for you. So, that's why we decided to join right now.

RS: *You claim that NextGO Epi is the only European supplier of gallium oxide epitaxial wafers in Europe. Are there other epitaxial suppliers in the US and Asia?*

T-S. C: There are several other epiwafer suppliers. They are in China, Japan, and the United States.

There are mainly three technologies for gallium oxide epitaxy: HVPE, MBE, and MOCVD. Our partners in the USA and Japan are more famous for MBE and HVPE. Some suppliers in China are also exploring MOCVD and MBE.

We believe that MOCVD, in general, is much better for large-scale, high-homogeneity epiwafer production. We have more than 10 years in MOCVD process development. We have a unique position in this whole ecosystem.

A.F: At this early stage of the transition of the material into the power electronics market, it's good to have multiple suppliers. Most R&D departments don't want a monopoly on materials. They say we wouldn't invest in this if you were the only firm. If something happens to you, we need someone else to provide the material; otherwise, we will lose all the money we spent on development.

T-S. C. We have signed strategic co-operation agreements with six substrate suppliers. They are in China, Japan, and the United States. In general, gallium oxide is still too young to mention competition. Everyone wants to make the cake bigger. We are also happy to have multiple suppliers, with good quality and lower cost. All substrate suppliers want to send their substrates to us. If they provide a good substrate, it's good for their reputation.

RS: *Recently, restrictions in international trade have held back the compound semiconductor industry. How is this impacting the nascent gallium oxide industry?*

T-S. C. We foresee that getting the cost down for gallium oxide may not be as



➤ The Hall measurement system to evaluate the electron mobility in the epilayer, a criteria for its high quality.

fast as we expected.

The second point is that NextGO Epi is a Germany-based company. We are in a very neutral position compared with companies in, say, the United States or Japan. We are not restricted or limited by strict export controls.

RS: *NextGO Epi has now been operating for over a year. But the history of the team goes back much further. How did the co-founders get together, and what provided the spark to transform three researchers into co-founding entrepreneurs?*

A.F: We met during our studies at the Leibniz Institute for Crystal Growth (IKZ), where we developed the whole technology. I started in 2015, doing my PhD on this material system, overcoming issues to obtain high-quality material.

Andreas Popp joined in 2017, first as a postdoc. He did so well that in 2019 he became group leader for epitaxial growth.

His first hire was Ta-Shun, as a PhD student, in 2020. Ta-Shun finished his PhD in record time. He published the most papers, so far, for any PhD student, and wrote the most patents. I'm very happy to work with him because he's not just smart – he's also working hard.

We saw the clear potential of the material. In 2019, we talked to industries about gallium oxide. They were like: 'We

just invested in silicon carbide. What is gallium oxide? Why are you bothering us?' Five years later, in 2024, industry came to us. 'Hey, you were mentioning this gallium oxide. Do you have some samples for us that we can test?'

With this momentum switch, we can push our research into a real application. This is also the main motivation for the entrepreneurship. We did great research, and those papers are well received. But when I talk to people outside the research bubble, they never understand what I was doing. When I can say, one day, this application, what you hold in your hand, comes from my research, this is a very strong motivation to go in this direction.

RS: *What challenges have you overcome to raise capital?*

T-S. C. Usually, you cannot expect the investor to invest in you so you can buy hardware equipment. Although you are a startup, they expect you to have all the equipment to run the business. Luckily, we are able to solve this problem. We are linked very deeply with our host institute, so we are able to lease equipment, including MOCVD, from our host institute.

A second challenge is that, in general, a semiconductor business model is not very common in Europe, including the UK. So, it's very unlikely you can find an investor with a background in evaluating semiconductors.

We are very lucky that we found

an investor. They don't know our technology, but they are willing to sit down with us, listen to us, and try to understand how good our technology is.

We also have very good support from the previous COO of Aixtron, Dr. Jochen Linck. He happened to be a Limited Partner of one of the VCs. He knows our technology because Aixtron is the vendor of our MOCVD tool. He does not just provide business understanding. He guides us and teaches us what an epi-company should look like, based on his experience. He's the mentor of business for the founding team.

RS: *NextGO Epi produces gallium oxide epiwafers using MOCVD. It's also possible to grow gallium oxide by MBE, HVPE, and mist CVD. What do you see as the pros and cons of all these techniques?*

A.F: MOCVD is the most mass-production-compatible technique. MBE, HVPE, and mist CVD suffer from either low throughput or single-wafer growth runs.

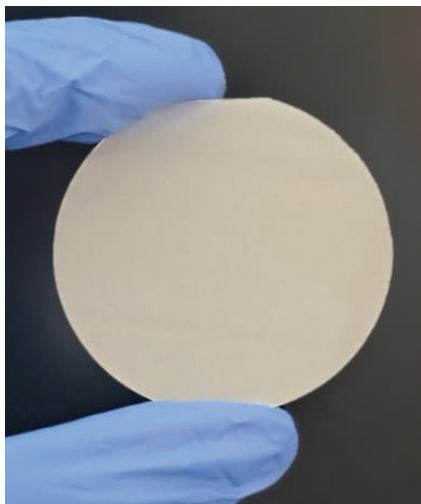
MBE is not just a single-wafer tool, and you have unmatched precision and purity in an ultra-high-vacuum chamber. But growth rates are very, very low for gallium oxide.

With HVPE, growth rates are very, very high, but samples are very rough, inhomogeneous, and have issues with structural defects.

Mist epitaxy is for the alpha phase. There are scientific reasons why most people focus on the thermodynamically stable beta phase. As soon as you process devices and want to ion implant or anneal your contacts, your alpha phase may form the beta phase, because that's the thermodynamically stable one.

With the beta phase of gallium oxide, the first devices were made with gallium nitride processing recipes. They work like a charm. They need just a little bit more optimisation.

The transition into the fabs will probably be very, very fast. What's needed is constant homogeneous electrical properties, which we can provide with MOCVD.



➤ A 2-inch Ga_2O_3 wafer with an epitaxial layer from NextGO Epi on top.

RS: *You have spun out of IKZ, an institute with expertise in crystal growth. So why don't you produce your own substrates?*

A.F: First of all, as a founding team, our main expertise is epitaxy. None of us has ever worked on bulk growth.

There are IKZ experts producing the best and highest-quality material. However, in Germany, energy costs are not as low as in other countries, and it's a high-energy process. You grow at $1,800^\circ\text{C}$, and you have to keep that temperature for at least a week or two to grow one crystal.

The technique developed at IKZ is not the cheapest. You have a very bulky iridium crucible. With the iridium price fluctuating, when we put everything in the business model, we didn't see that we would be compatible with other companies on the global market. So, we decided to stick to epitaxy.

RS: *IP matters in our industry. NextGO Epi has two international patents. What do they cover?*

T-S. C. One is a very unique technology to monitor the epitaxial growth of gallium oxide. The second is a process and technology patent for growing very thick and high-quality gallium oxide films, which are critical to power electronics applications.

RS: *How do you characterise your material prior to shipment?*

A.F: In the semiconductor world, reproducibility, reliability, and the specs are the keys to success. We have strict quality standards before we ship any product. We look at X-ray diffraction measurements, then perform Hall measurements to gauge the charge-carrier concentration, as well as the mobility of the material, because those two are, for most devices, the most important parameters.

Charge-carrier concentration gives you insight into how well you match the doping concentration to what the customer wants, and how clean your material is.

Mobility gives you direct feedback about the quality of the material. The higher the charge carrier mobility, the fewer defects and scattering centres are in the material.

We do some general screening, with AFM and microscopy, to see that the whole surface is clean and fine.

RS: *Are all your customers capable of processing your material into devices? Or do some work with foundries? And do you think fabless firms could prosper in a gallium oxide power electronics industry?*

A.F: Back in 2016, when we gave the first samples to make devices, they just used their gallium nitride recipes. The first device directly broke the critical breakdown field record of silicon carbide and gallium nitride. So, this material directly exceeded 3 megawatts-per-centimetre. That shows you how compatible it is with the gallium nitride technology. Therefore, I think fabless foundries will have an easy way to get into the market, because they can go directly to any foundry that can process gallium nitride and is willing to take gallium oxide.

RS: *Gallium oxide has weaknesses, particularly p-type doping. Why do you think that this is not a show-stopper?*

A.F: Most materials still use an *n*-type channel, because electrons have a higher mobility than holes. But *p*-type is really important for field management.

At least two solutions are very promising and have shown 8 megawatts-per-centimetre critical electrical breakdown fields in the

device. Actually, the periphery of the device broke down, not the gallium oxide, so people still think they can push even further.

One solution is an ultra-high- κ dielectric. There, you have polarisation charge that helps you with field management. This is, of course, only possible for low-frequency devices. But when we think about high-voltage devices that run at 200 kHz, this is possible to implement.

The other one is integrating hetero-epitaxy or deposition. For example, *p*-type nickel oxide or copper oxide, using sputtering, which is a very normal process in any cleanroom. That worked like a charm.

RS: *The thermal conductivity of gallium oxide is around just a tenth of that for silicon carbide. Is that an issue for this industry?*

A.F.: This topic has been part of research from early on. When the value is so low, people directly noticed and said: 'We have to do something about it, otherwise this material will never succeed'.

The research community came up with promising solutions. Any device has to extract all the heat from the top, because heat will never make it to the bottom of the substrate of the device.

The most promising solution, lately developed by Martin Kuball at Bristol University, is another CVD process. You deposit polycrystalline diamond within your gate stack and your dielectric stack. Polycrystalline diamond has such good thermal conductivity that it extracts basically all the heat out of the structure.

You can get certain advances in packaging. We had, early on, collaborations with ZF in Germany. They showed it's possible to package in a way that you can get the heat out.

RS: *You are already shipping material to customers in various countries. How much of this business is associated with device development in academia? And how much is industrial development?*

T-S. C. Most customers are from the R&D departments of their companies, or academia.



➤ The NextGO Epi Founder team, from left to right: Andreas Fiedler, Ta-Shun Chou, and Andreas Popp

RS: *You have just raised €2 million in seed investment. Tell me about your investors. Why are they backing you?*

T-S. C. Our lead investors are Vireo Ventures, Ultratech Capital Partners and IBB Ventures, alongside angel investor Boris Habets. They are backing us because they believe in our next-generation semiconductor material for power electronics.

RS: *What will that investment be used for?*

T-S. C. For a startup, it's all about growing, growing, growing. Our team now is three co-founders, all experts in gallium oxide. In the next couple months, we are having a new colleague join us, an engineer, to expand our production capacity and to allow us to attract more customers to gallium oxide. Also, we will have an operations manager join us to support us in the

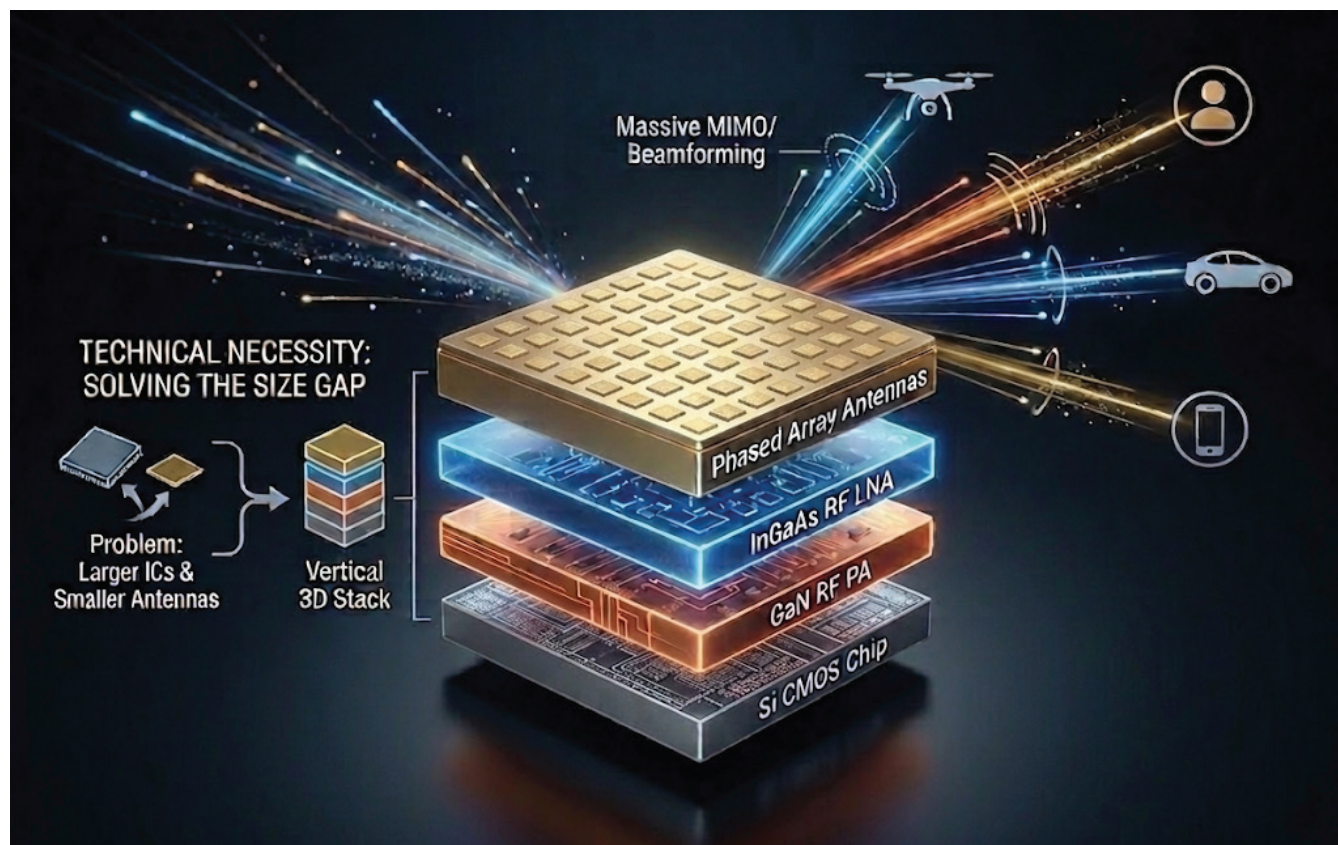
daily administrative stuff. We already have many student workers on site. In the future, when we attract more customers, we'll definitely expand our team.

RS: *What are your plans for the next 18 months?*

T-S. C. We should establish our brand as the leading gallium oxide epiwafer provider. But more than that, we want to push gallium oxide technology further, providing high-quality epiwafers to companies around the world, to accelerate gallium oxide technology.

We need to see a gallium oxide product. The gallium oxide epiwafer is not a product. A module for the EV car, or the AI data centre, that is a real gallium oxide product. And we want to help everyone in the community make it happen.

MOCVD is the most mass-production-compatible technique. MBE, HVPE, and mist CVD suffer from either low throughput or single-wafer growth runs. MBE is not just a single-wafer tool, and you have unmatched precision and purity in an ultra-high-vacuum chamber. But growth rates are very, very low



The triumvirate for tomorrow's wireless

Next-generation wireless communication systems will benefit from heterogeneous monolithic integration of InGaAs HEMTs and GaN HEMTs on silicon CMOS chips

BY JAEYONG JEONG, CHAN JIK LEE, YOON-JE SUH, NAHYUN RHEEM, BONG HO KIM, JOON PYO KIM, JUHYUK PARK AND SANGHYEON KIM FROM KAIST

WIRELESS communication systems are the neural network of modern infrastructure, supporting a vast array of interconnected services. It's vital that they provide reliable connectivity to support the rapid expansion in autonomous transportation and advanced AI platforms. Both these sophisticated technologies generate and process immense volumes of data in real time, and require unprecedented transmission speeds to function effectively.

To address these demanding requirements, researchers must explore opportunities to expand physical channel capacity through fundamental hardware innovation. At the Korea Advanced Institute of Science & Technology (KAIST), our team is taking on this challenge, through the integration of III-V and III-N transistors onto silicon substrates.

This triumvirate is pushing the boundaries of high-performance, RF blocks.

Our efforts at expanding channel capacity are drawing on two primary physical pillars: the widening of the available bandwidth, and an increase in the signal-to-noise ratio. A wider bandwidth necessitates a transition to a higher frequency spectrum, where more spectral resources are currently underutilised. This move must go hand-in-hand with maintaining a high signal-to-noise ratio at these frequencies – and that requires exceptional performance from both the transmitter and the receiver ends of the system. Power amplifiers must deliver high output at the source, while low-noise amplifiers must preserve signal integrity at the destination. To excel on these two fronts, both components must be seamlessly coupled with high-

gain antennas, to ensure the efficient radiation and reception of signals across the environment.

Breaking limits

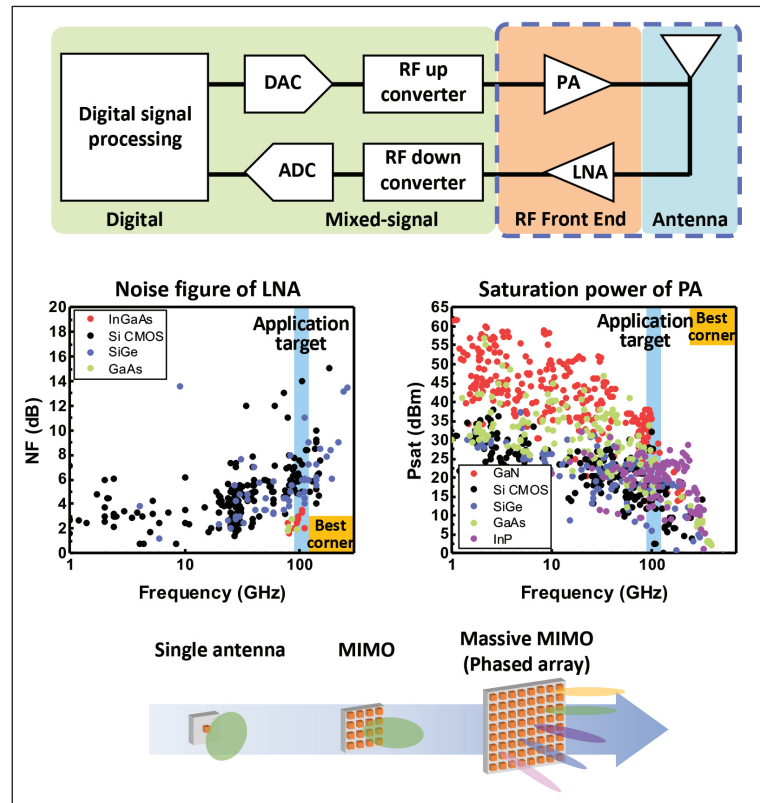
It is the physical properties of semiconductor materials that dictate the ultimate performance limits of high-frequency communication systems. Within the portfolio of compound semiconductor materials, InGaAs and GaN are the premier candidates for low-noise and high-power applications, respectively. InGaAs devices are renowned for their remarkable low-noise characteristics in the 100 GHz range, making them ideal for sensitive receivers; and GaN transistors offer exceptionally high-power saturation levels within the same frequency bands for transmission. We utilised these two materials during our development of a robust RF front-end that leverages a wide bandwidth while maintaining a superior signal-to-noise ratio.

Our technology draws on significant breakthroughs in antenna design and spatial multiplexing.

Early wireless systems relied on basic single-input, single-output structures, which tended to limit capacity, and were often hampered by interference. They have been superseded by multiple-input, multiple-output (MIMO) configurations that increase data throughput in crowded environments. However, as operating frequencies increase and move towards the millimetre-wave and sub-terahertz regimes, traditional architectures face severe physical constraints.

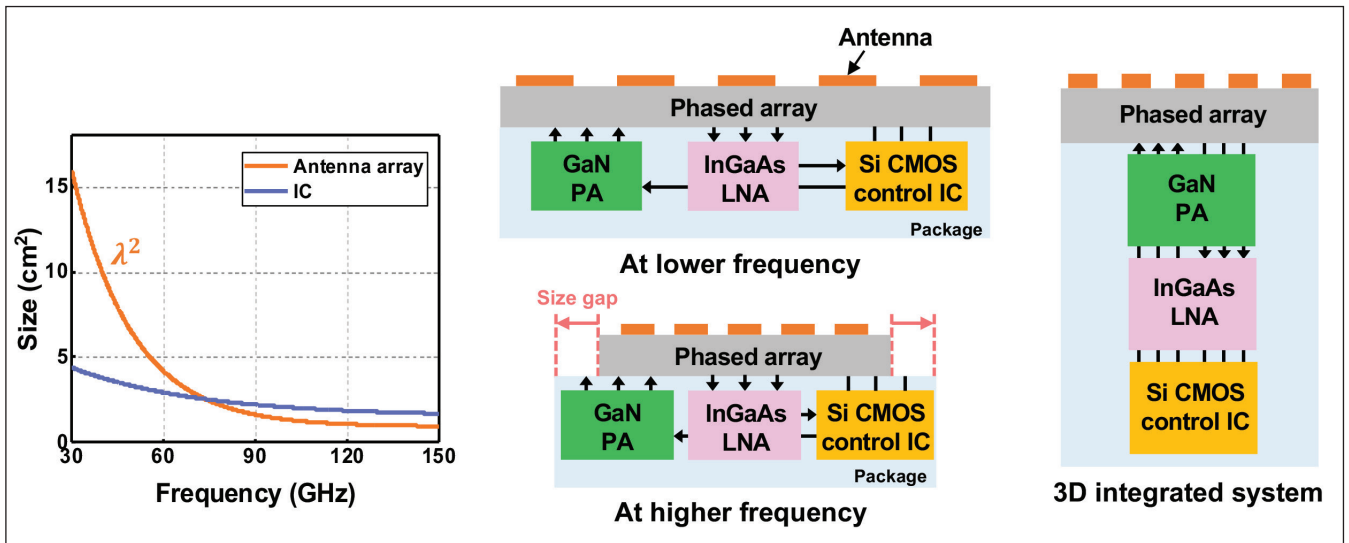
Due to this, phased-array antenna technology, based on massive MIMO systems, is emerging as the leading solution for next-generation wireless hardware. Utilising advanced beamforming, these systems concentrate electromagnetic energy into precise spatial directions for targeted communication. Spatial focusing is a game changer, dramatically increasing the communication range and its capacity by cutting energy waste and minimising interference with other users. Implementing these arrays requires the dense integration of many individual antenna elements with respective control circuits.

Unfortunately, dense integration is far from trivial. One major issue is that conventional 2D packaging technologies fail to fulfil the tight integration requirements demanded by modern phased-array antenna systems. Using a side-by-side layout, it is physically difficult to integrate an InGaAs Low Noise Amplifier (LNA), a GaN Power Amplifier (PA), and silicon-based control chips. This challenge arises because as the operating frequency increases, the physical size of the antenna elements tracks those changes in signal wavelength – while the supporting control electronics and RF components scale far more slowly. This mismatch in component sizes leads to long interconnects, which introduce parasitic losses and degrade signal performance at high frequencies.



➤ Figure 1. An illustration of the essential components of a next-generation radio frequency communication system. KAIST selects InGaAs and GaN for the front end, due to their superior noise and power performance at 100 GHz. Antenna technology has evolved, from simple structures to massive multiple-input multiple-output (MIMO) phased arrays to meet high-capacity demands. This integrated strategy is critical for supporting the extreme data rates of future wireless standards.

For the bonding stages, we made several critical engineering choices to ensure the thermal and mechanical stability of the final device. To facilitate efficient heat dissipation away from the GaN PA, we implemented a metal bonding interface. This high-power device generates significant heat during operation, so thermal management is critical to prevent thermal degradation of the surrounding circuits.



➤ Figure 2. The scaling mismatch between antenna elements and supporting integrated circuits creates a significant architectural challenge as operating frequencies increase. While antenna size shrinks rapidly according to wavelength, the circuitry footprint remains relatively large, leading to a physical size gap. Vertical 3D integration resolves this bottleneck by stacking functional layers directly beneath the antenna array. This approach ensures a compact, efficient footprint for high-frequency phased-array systems.

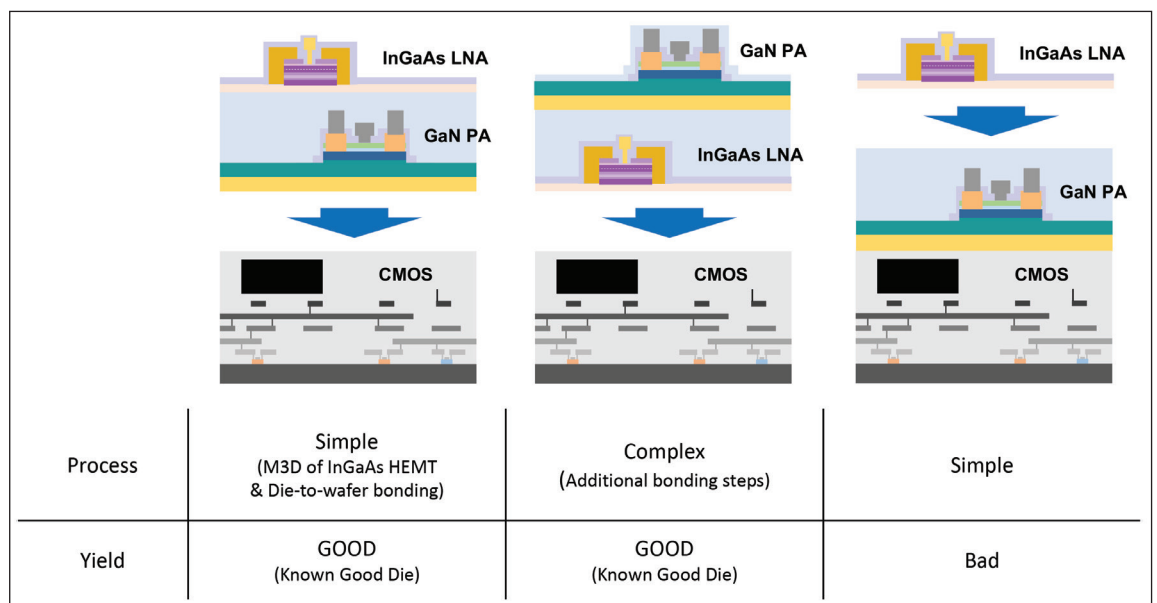
Offering a powerful, compelling alternative is vertical 3D integration technology. By allowing the stacking of different semiconductor layers directly on top of each other, this form of integration maximises spatial efficiency and shortens the signal paths between active devices and antenna.

Vertical integration: Pros and cons

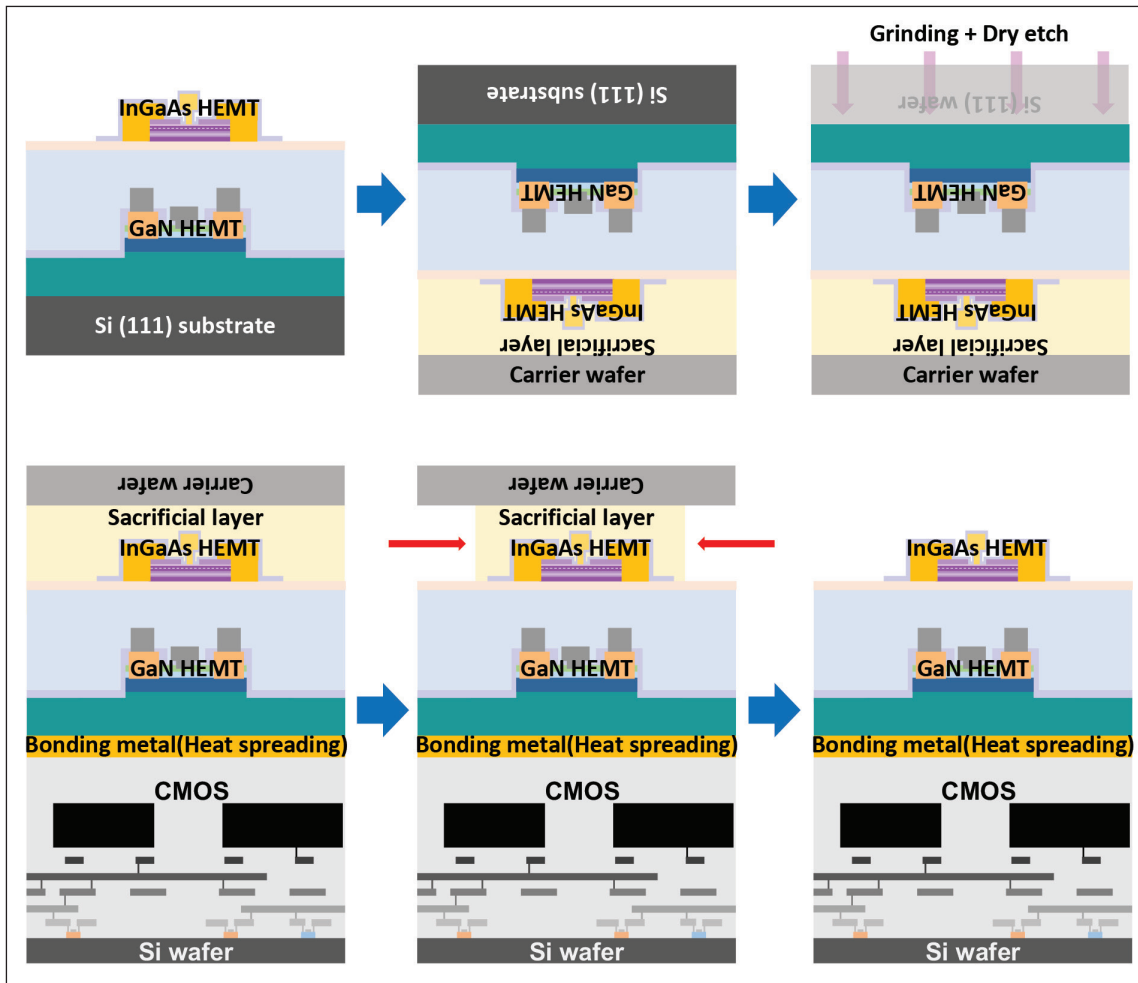
One great strength of vertical stacking is that it allows the creation of heterogeneous systems

where each material is utilised for its specific strengths. This is realised without compromising the overall footprint.

Using this approach, we handle control logic and complex signal processing with cost-effective silicon CMOS processes. Meanwhile, high-performance RF functions are delegated to specialised compound semiconductor layers, bonded directly to the silicon base.



➤ Figure 3. A comparison of 3D integration pathways highlights the optimal balance between process complexity and manufacturing yield. Utilising monolithic integration to build a pre-verified RF block before bonding ensures a high yield through the known good die approach. Other sequential methods are less effective, due to increased bonding steps or significant yield loss. A modular manufacturing flow provides the most advantageous strategy for ensuring overall system reliability.



➤ Figure 4. 3D integration process for an RF block on a silicon CMOS chip.

Adopting this strategy allows us to use expensive compound materials only where they are strictly necessary for electrical performance. This platform opens the door to fully integrated antenna modules that house all necessary components in a single compact package.

Motivated by these architectural advantages, we overcome formidable technical hurdles to combining diverse compound semiconductors on a silicon platform. It is extremely difficult to grow compound semiconductor layers directly on silicon, due to the significant mismatch in crystal lattice constants. There are also differences in the coefficients of thermal expansion of these materials, leading to mechanical stress and structural defects during fabrication.

Yet another obstacle is the high temperatures that are required for manufacturing GaN devices, which threaten to damage pre-existing structures on the chip. To address all these concerns, we introduced an innovative fabrication flow that stabilises these disparate materials without sacrificing their individual device characteristics.

With our fabrication flow, we realise a heterogeneous 3D stacking architecture that combines GaN HEMTs with InGaAs HEMTs on a

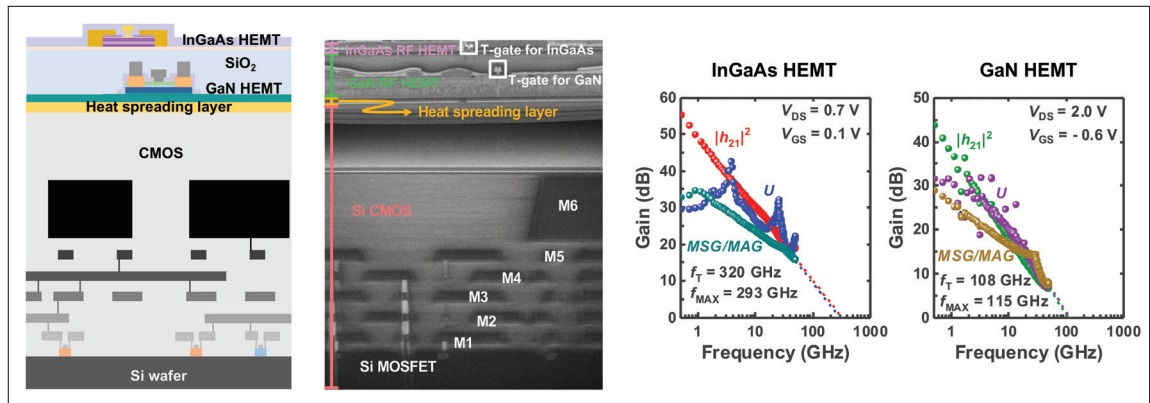
silicon CMOS chip. This process begins with the fabrication of GaN HEMTs, and is followed by the integration of InGaAs layers, which provide low-noise functionality. We combine these two RF blocks into a single chip unit, which is transferred to the silicon control circuitry.

To combine different material technologies, we utilise a sophisticated die-to-wafer bonding technique that ensures a stable mechanical and electrical connection between the layers. With this methodology, we minimise the number of interlayer vias required, and significantly improve the overall integrity of high-frequency signals.

When forming our heterogeneous structures, we begin by producing an RF block. This involves the integration of InGaAs devices onto GaN devices via monolithic 3D integration. We then integrate this completed RF block onto the silicon CMOS chip using a secondary vertical process.

Our approach avoids integrating individual components sequentially onto the silicon chip. If we adopted that approach, it would be impossible to verify the operation of the RF block before bonding. By avoiding this limitation regarding known good die, we do not suffer from an inevitable reduction in the overall manufacturing yield. Additionally, we

➤ Figure 5. KAIST's successful vertical integration of the RF block onto a silicon CMOS chip. A 3D integrated InGaAs LNA and GaN HEMT maintain superior RF performance.



reject stacking GaN devices onto InGaAs devices, as this would involve a redundant and costly bonding step.

Process design strategy

The fabrication sequence that we have devised, involving three primary stages, starts with the standard manufacture of GaN HEMTs. Their production includes conventional high-temperature annealing to form source and drain ohmic contacts. For the subsequent monolithic integration of the InGaAs layer, we employ an inverted transistor structure. Our specific design choice ensures superior alignment. The resulting composite block provides a high-performance engine for the transmit and receive paths of the communication system.

We use a two-stage bonding process to transfer our dual material RF block onto our silicon CMOS chip. We begin by bonding the block to a temporary carrier wafer in an inverted orientation, to allow removal of the silicon substrate of the GaN HEMT. After removing this substrate, the RF block is permanently attached to the top of the silicon control chip.

For the bonding stages, we made several critical engineering choices to ensure the thermal and mechanical stability of the final device. To facilitate efficient heat dissipation away from the GaN PA, we implemented a metal bonding interface. This high-power device generates significant heat during

operation, so thermal management is critical to prevent thermal degradation of the surrounding circuits.

The entire bonding sequence proceeds below 150°C to protect the integrity of the pre-fabricated transistors. This low-temperature budget maintains delicate doping profiles, as well as the metal interfaces of the underlying silicon and compound semiconductor devices.

With our delicate and considered approach, the structural integrity and electrical characteristics of our InGaAs and GaN transistors remain stable throughout the integration process. According to post-integration testing, our HEMTs maintain their high-frequency capabilities without significant performance loss. The 3D integrated InGaAs HEMTs have a cut-off frequency of 320 GHz and a maximum oscillation frequency of 293 GHz, and the corresponding figures for GaN HEMTs are 108 GHz and 115 GHz, respectively. These results confirm that our vertical integration approach is compatible with the most demanding requirements of the sub-terahertz frequency spectrum.

Future communication vistas

Our research establishes a viable pathway for vertical integration of high-performance compound semiconductors. By maximising the strengths of different material systems, we have created a platform that combines high-power and low-noise capabilities in a compact form factor.

In addition to this asset, there's a drastic reduction in the physical footprint of the RF front end – that's a major milestone for the development of future antenna systems.

It's possible that other teams will build on our foundation, which provides the essential hardware foundation for implementing the massive MIMO-based phased arrays antenna, which are required by next-generation wireless standards.

We expect our 3D stacking platform to be a transformative technology for the future landscape of global connectivity.

FURTHER READING

- N. Collaert *et al.* "From 5G to 6G: will compound semiconductors make the difference?" ICSICT 2020 (2020)
- J. Jeong *et al.* "Heterogeneous and Monolithic 3D Integration of III-V-Based Radio Frequency Devices on Si CMOS Circuits" ACS Nano. **16** 9031 (2022)
- G. Xiaoxiong *et al.* "W-Band Scalable Phased Arrays for Imaging and Communications", IEEE Communications Magazine. **53** 196 (2015)



Thin film technologies reducing energy consumption in a power-hungry world

From more efficient powertrain management to reduced energy consumption for vehicle displays and lighting, Evatec thin film tools and production process know-how help automobile manufacturers reduce energy consumption extending battery life and range for the latest generation of electric vehicles. Evatec expertise in the manufacture of Wide Band Gap Power Devices reduces losses, while its mini- and micro-LED capabilities enable bright, efficient lighting and display technologies that drive down energy consumption in a power-hungry world.



Find out how Evatec thin film technology solutions are helping to shape a sustainable future.

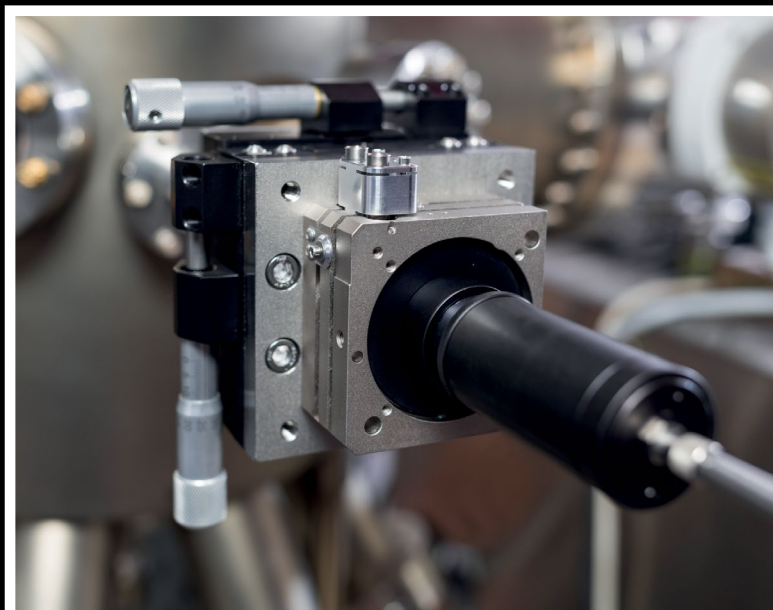
kSA ACE for Atomic Flux Control

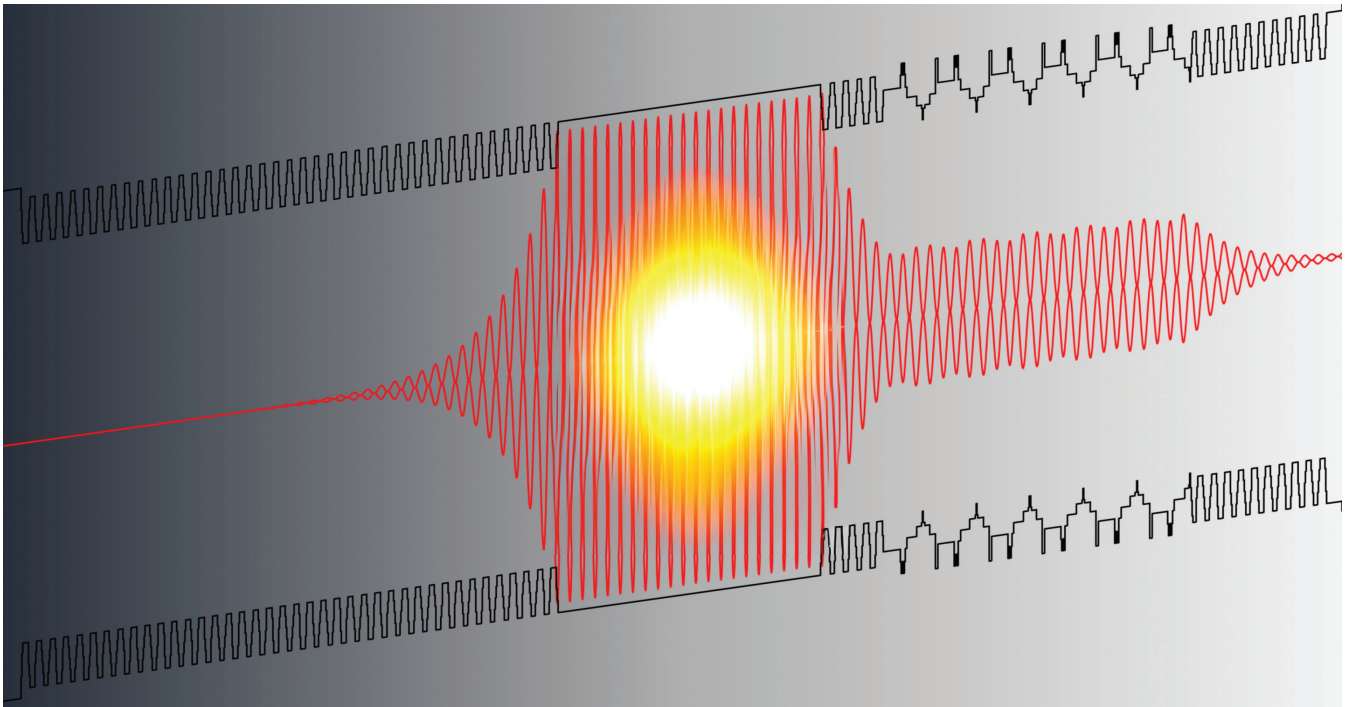
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Transforming lidar with anti-reflective VCSELs

Progressing anti-reflective VCSELs from laboratory prototypes to high-volume production is facilitating cost-effective long-range sensing for automotive lidar

BY DONG LIANG, CHENG ZHANG, ZHITONG LUO, SHOUZHU NIU, PENGFEI ZHANG, SONG LIU, HUIJIE LI, RYAN Z. RAO, LI ZHAO, XIAOCHI CHEN, HANXUAN LI AND YIJIE HUO FROM VERTILITE

FOR well over 100 years cars have been rolling off production lines. Over this time, there have been many substantial changes, including the introduction of more efficient engines, seat belts for all, and breaking assistance. But the most profound changes are happening now – a switch from engines burning petrol and diesel to power provided by a battery, and the introduction of self-driving cars.

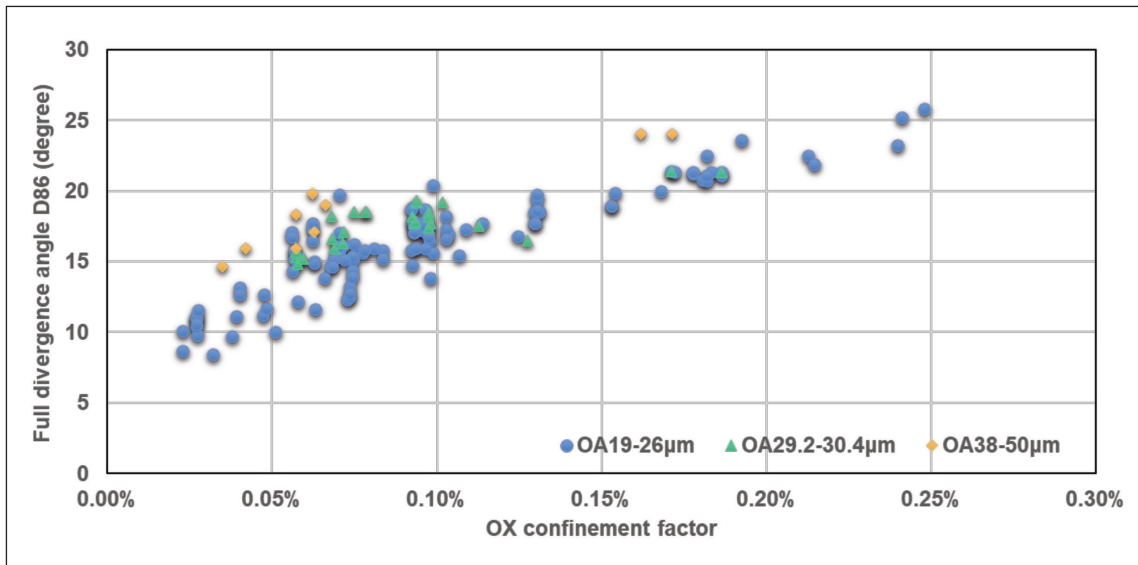
The latter revolution in the automotive industry draws on compound semiconductor lasers for the light source for lidar. These chips fulfil the demands of design engineers, who prioritise power, efficiency, and scalability.

For long-range lidar, high brightness – that's a measure of the concentration of optical power within a minimal area and a narrow angular spread – is the critical performance metric. To maximise the detection range, sensors need emitters that combine a high output power with an extremely low beam divergence.

One candidate for the light source is the VCSEL. It's a class of laser that's produced in very high volumes, and is already widely deployed in short-range consumer applications, such as facial recognition. But if it is to be used in lidar, it must provide a significantly higher brightness.

Helping to meet that goal is the introduction of multi-junction structures, which enable higher power densities. However, that's only a partial solution to the problem. Higher powers must be combined with efforts to address the excessive divergence of the traditional VCSEL architecture. That's a weakness that restricts the VCSEL in long-distance perception.

To meet stringent brightness and divergence requirements, our company, Vertilite, has developed and then ramped production of the anti-reflective VCSEL (AR VCSEL). A key feature of our novel laser is the AR layer, integrated between the active region and the extended cavity of a traditional extended VCSEL structure.



➤ Figure 1. Divergence angle dependence on the oxide confinement factor for aperture sizes ranging from about 20 μm to about 50 μm .

Critical to realising a low divergence is limiting the number of lateral modes to just a few. In a VCSEL, the number of supported lateral modes is governed by the effective refractive index contrast between the core and the cladding – these two regions correspond to areas inside and outside the light-emitting aperture. As the oxide layers in a VCSEL provide the dominant contribution to the lateral index difference, this contrast is nearly proportional to what is referred to as the oxide confinement factor.

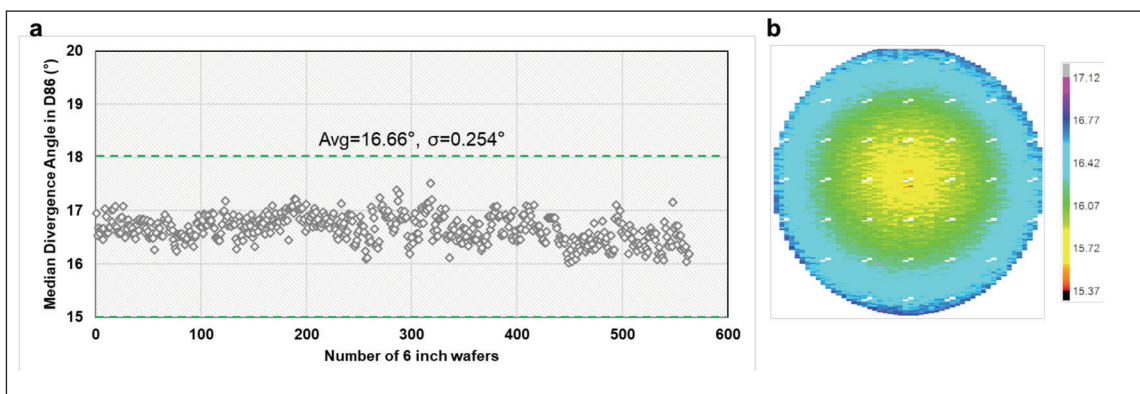
When the AR layer is integrated between the active region, where current-confining oxide apertures sit, and the extended ‘light reservoir’ region, there’s a significant enhancement to the standing-wave electric field intensity within the extended region. This physical modification leads to a dramatic reduction in the oxide confinement factor. In turn, there’s a fall in the number of lateral modes that are allowed, and ultimately a smaller divergence angle.

Precise control over the oxide confinement factor, and thus the beam’s divergence, is realised by adjusting the property and design of the

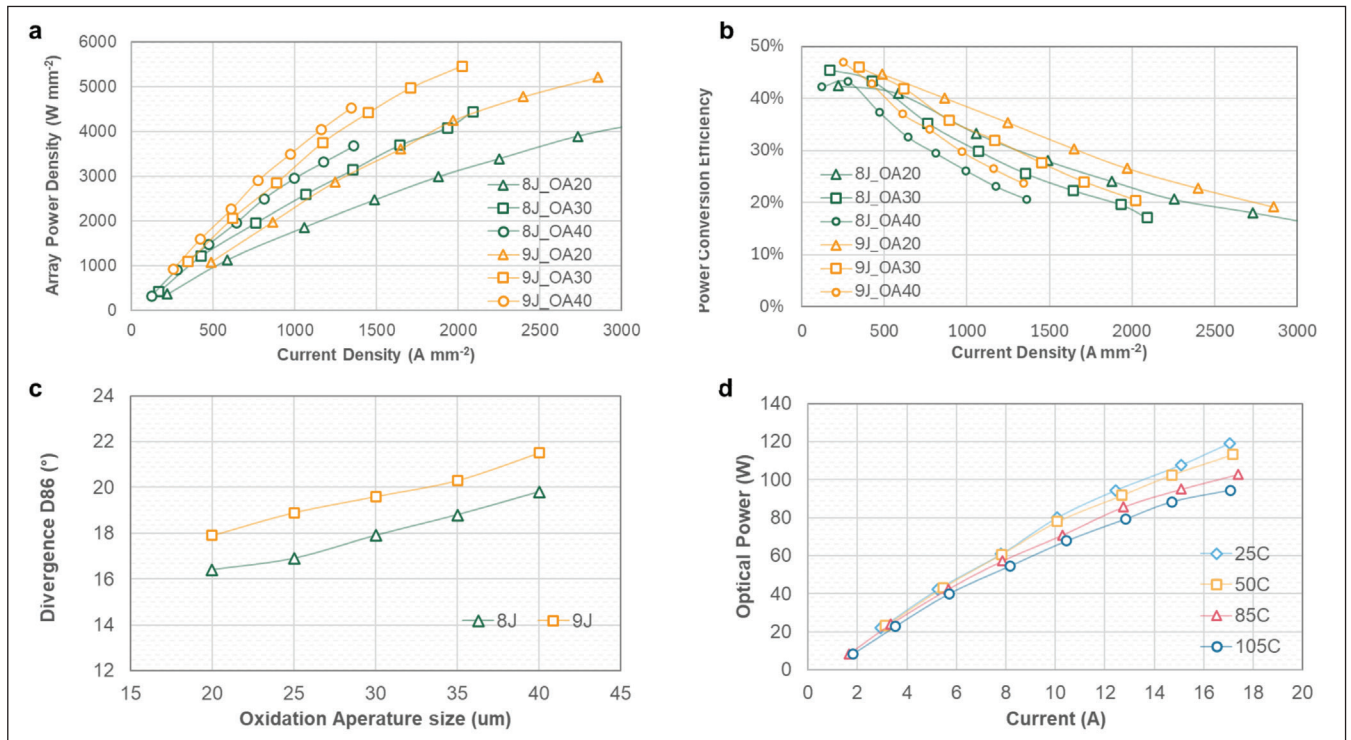
anti-reflection layer. With appropriate choices, we design VCSELs with narrow angles necessary for long-range detection.

To demonstrate our capabilities in this regard, we have demonstrated a clear positive correlation between the beam divergence and the longitudinal confinement factor (see Figure 1). For this work, we consider a metric known as the D86 divergence angle – it’s the diameter of a circle that encircles exactly 86.5 percent of the laser’s total beam power (compared with the full-width at half-maximum, that’s a more stringent metric for evaluating small divergence). We have shown that we have precise control over the D86 divergence angle – spanning from 8° to 26° – across devices featuring 5 to 14 junctions.

One of our key findings is that while the overall pattern of the laser array does not fundamentally alter the dependence of divergence on the confinement factor, the size of individual oxide apertures matters. This has led us to categorise our devices into small, medium, and large aperture groups. We note that divergence typically



➤ Figure 2. Performance consistency across 500 wafers and typical intra-wafer divergence distribution. (a) D86 divergence angle of an AR-VCSEL product, evaluating of over 500, 6-inch wafers in production. (b) A typical D86 divergence angle distribution of the AR-VCSEL product in (a) within a 6-inch wafer.



► Figure 3. Performance metrics for 8-junction and 9-junction arrays, including power density and efficiency. (a) Normalised light-current (L-I) curves for arrays with oxidation apertures (OA) ranging from 20 to 40 μm ; current density is normalised to the total OA area, and array power density is normalised to the total array area (the minimal area to enclose all emitters). (b) Power conversion efficiency (PCE) as a function of current density. (c) Far-field divergence angle for 8-junction and 9-junction arrays across various OA sizes. (d) Temperature-dependent L-I characteristics for a 9-junction, 12-emitter array (30 μm OA) measured from 25 $^{\circ}\text{C}$ to 105 $^{\circ}\text{C}$.

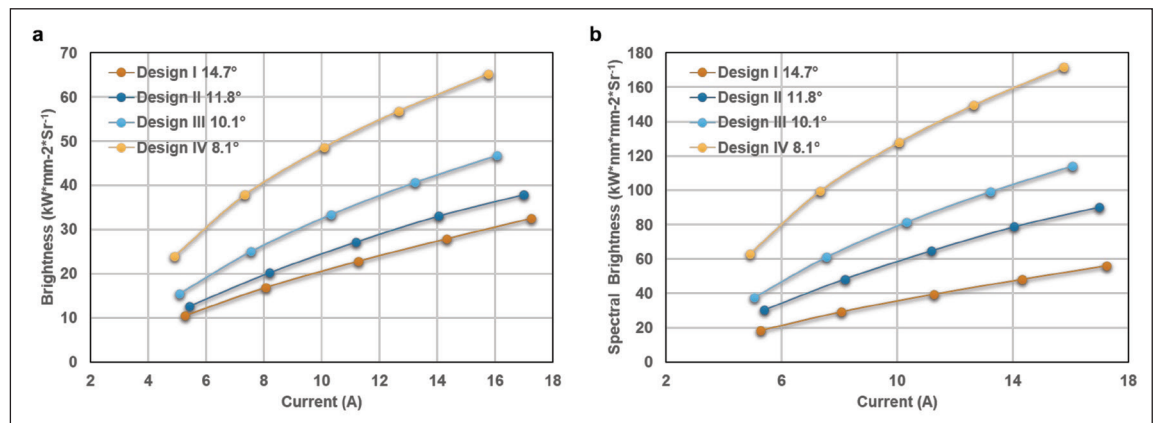
increases by 1° for every 5 μm increase in aperture size. Using this technology, we have realised a record-low full divergence angle of 8° and record-high brightness of approximately 140 $\text{kW mm}^{-2} \text{sr}^{-1}$ in our multi-junction AR VCSELs. These performance figures meet the range and precision requirements for primary lidar.

Mass production success

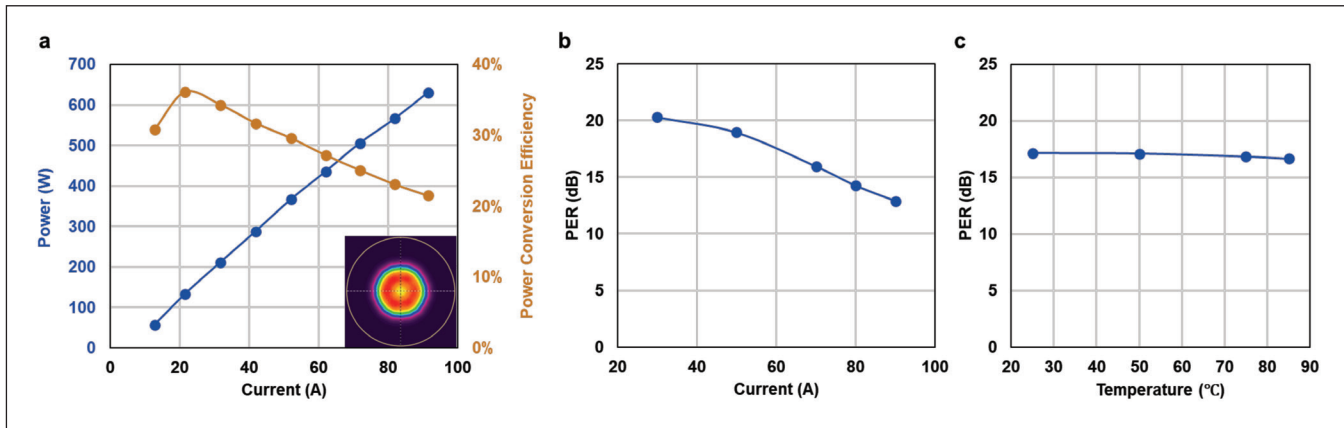
For any device developer, one of the biggest challenges when moving a technology from a laboratory to mass production is ensuring extreme

consistency. We have made much progress on this front, with our 6-junction AR VCSELs now produced in high volume.

According to performance data from more than 500 6-inch wafers, our manufacturing process has exceptional stability (see Figure 2(a)). The average wafer-median divergence angle across this massive sample size is 16.66°, and the standard deviation a mere 0.254°. This level of uniformity is essential for automotive manufacturers, as they require predictable performance across thousands of units.



► Figure 4. Comparison of brightness (a) and spectral brightness (b) across four different epitaxial designs for 8-junction AR-VCSEL arrays with 42-emitters (OA 24 μm and emission area 225 μm by 218 μm).



➤ Figure 5. Characteristics of a polarisation-controlled array (0.3 mm × 1.0 mm emission area, about 24 µm oxidation aperture) showing power and extinction ratio stability. (a) Pulsed light-current characteristics (20 kHz, 6 ns) at 50°C; the inset displays the far-field profile at about 70 A with a D86 divergence of approximately 19°. (b) Polarisation extinction ratio (PER) versus driving current under 50°C pulsed operation. (c) Temperature sensitivity of the PER measured at about 70 A from 25°C to 85°C.

Intra-wafer distribution is also impressive, with a yield of nearly 100 percent against strict divergence specifications (see Figure 2 (b)).

Based on all these results, we conclude that our AR VCSEL architecture is high-performing and highly manufacturable. We are transitioning this manufacturing excellence to AR VCSELs with 8 junctions that offer an even higher power density, while maintaining the same rigorous divergence standards.

Power scaling

An attractive option for increasing the power of the VCSEL is to add more junctions within the same vertical stack. With this approach, there's a linear relationship between power and the number of epitaxial junctions.

Our AR VCSEL trajectory includes a rapid increase in junction count. Typically, we add a couple junctions every couple of years. Back in late 2021, 5-junction and 6-junction designs were industry standard, providing enough power for early hybrid scanning lidar systems. By 2024, 8-junction designs had emerged, providing a significant boost to brightness and enabling the first wave of long-range solid-state sensors. This year, architectures with 9 or more junctions are entering mass production.

We have successfully navigated the complexities of mass-producing 6-junction, 8-junction, and 9-junction AR VCSELs. With the introduction of every additional junction, we increase optical power and efficiency at a given current level. Our 9-junction arrays, featuring 30 µm apertures, are delivering an array power density of 5450 W mm⁻² that's limited only by the maximum driving current of the driver (see Figure 3 (a)). Power-conversion efficiency of these VCSELs outperforms their 8-junction counterparts with various oxide aperture designs, especially under high driving currents.

However, careful engineering trade-offs must be made when scaling to higher power levels. Introducing more junctions increases the operating voltage, which must remain within the limits of automotive electronic drivers. While considering this matter, another ponderable is that larger aperture arrays generally offer higher fill factors by trimming the dead space between the emitters – but this tends to be realised alongside a slightly higher divergence (see Figure 3 (c)).

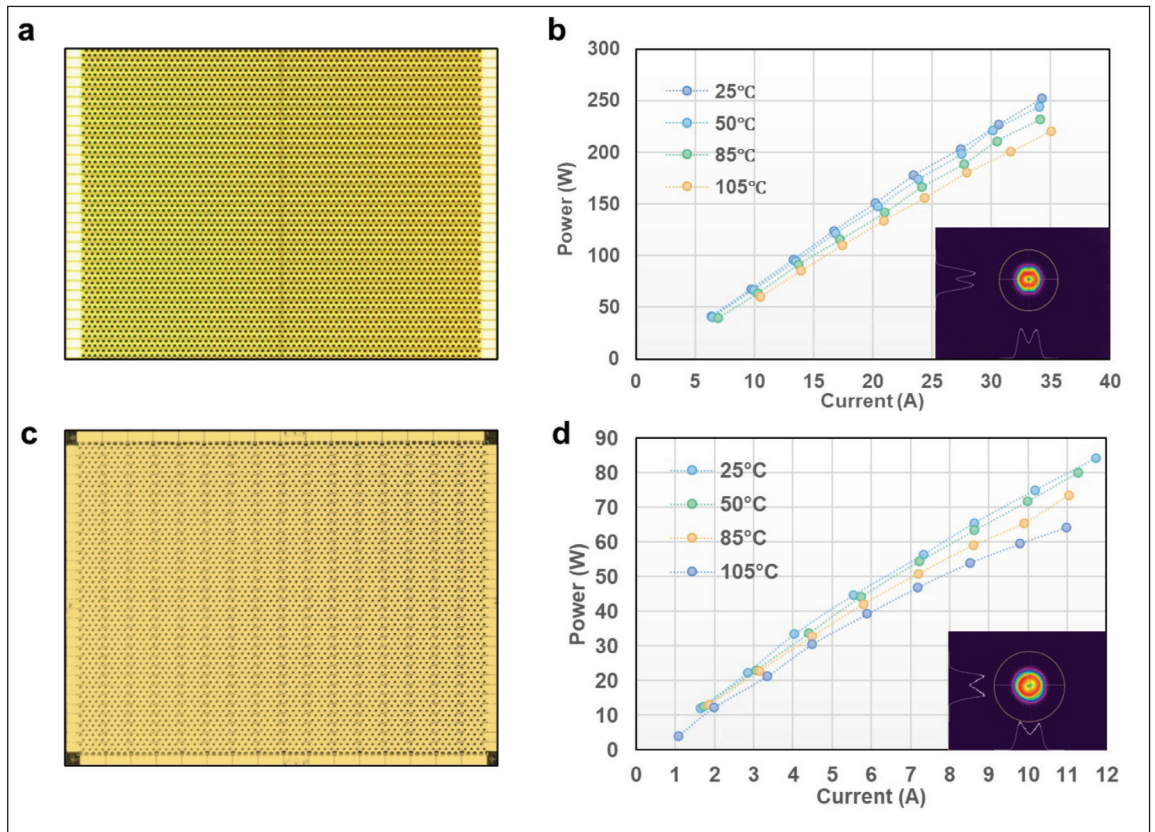
When balancing these various pros and cons, we often find that 30 µm devices represent the 'sweet spot' in design, outperforming 20 µm and 40 µm variants when trading power density against beam quality. In practical automotive applications, we tend to recommend maintaining current densities below 1000 A mm⁻² to ensure a sufficient lifetime margin.

Robustness, brightness and polarisation

Amongst the various applications involving deployment of semiconductor lasers, automotive environments are one of the most demanding. One issue is that ambient temperatures can fluctuate wildly.

We are encouraged by the results from testing of our-junction AR-VCSEL arrays at temperatures up to 105°C. At this extreme, our emitters retain 80 percent of their room-temperature power (see Figure 3 (d)). Special designs could enable even more impressive high-temperature performance.

A multi-pronged engineering approach is behind the enhanced performance at over 100°C. Success comes from focusing on minimising the thermal resistance of the package and the chip itself, while simultaneously optimising the gain spectrum of the quantum wells. We carefully engineer the degree of offset between the gain peak and the cavity resonance to ensure the laser remains in its most efficient operating regime, even as the temperature



► Figure 6. Addressable AR-VCSEL array configurations and performance. (a) Optical micrograph of a 1D addressable array comprising 64 individual sections. (b) Temperature-dependent light-current curves (25–105°C) for a single section from the 1D array; the inset illustrates the far-field emission pattern during operation. (c) Optical micrograph of a 2D addressable array organized into 32 × 16 zones. (d) Light-current (L-I) characteristics across varying temperatures (25–105°C) for an individual zone within the 2D array, with an inset showing the corresponding far-field profile.

risers. By placing a premium on thermal robustness, we ensure lidar systems incorporating our VCSELs maintain a consistent detection range, regardless of the environmental conditions. That's a prerequisite for Level 3 and Level 4 autonomous systems.

We have also undertaken a series of controlled experiments to evaluate how variations in the anti-reflective region alter the confinement factor. We produced a family of devices with an 8-junction base epitaxial design. These AR VCSELs have divergence angles of 14.7°, 11.8°, 10.1°, and 8.1°. Compared with the design with a 14.7° angle, that with a value of 8.1° delivers a two-fold increase in brightness and a threefold increase in spectral brightness. As we transition these optimisations to our 9-junction platforms, we expect to push brightness levels higher.

Driven by the increasing sophistication of lidar systems, the focus for the optical source is shifting beyond raw power and towards signal quality. As part of this trend, polarisation control is emerging as a pivotal tool for increasing the signal-to-noise ratio in complex driving environments. When system designers utilise a light source with a fixed, stable polarisation, they can place a linear polariser at the receiver to filter out unpolarised ambient sunlight

and glare from other vehicles. With this simple step, the signal-to-noise ratio can increase by approximately 3dB, effectively doubling sensitivity under certain conditions.

Beyond noise suppression, polarisation signatures offer a new dimension of data for material classification. Different road surfaces and objects – such as water, asphalt, vegetation, metal, or human clothing – depolarise light in unique ways. By analysing these changes, it's possible for the autonomous vehicle to have a better understanding of its surroundings.

Based on this opportunity, we have developed polarised AR VCSELs with integrated gratings that produce a record-high polarised output of 630 W with a polarisation extinction ratio exceeding 12 dB. These polarised AR VCSELs deliver this level of performance across diverse operating conditions and temperatures (see Figure 5). While the integration of these gratings often results in a small power loss of 10 to 20 percent, our high-precision fabrication techniques minimise these effects, enabling a high-power density and stable polarisation across a wide range of operating currents and temperatures.

Shifting to all-solid-state lidar

For the automotive sensor, the ‘holy grail’ is an all-solid-state lidar. Such systems are highly desirable, combining compactness with affordability and the absence of mechanical moving parts, which are prone to wear and calibration issues.

To support this transition, we are developing and producing addressable AR-VCSEL arrays in both one-dimensional and two-dimensional formats. Two 8-junction addressable arrays are showcased in Figure 6: a 1D version (2 x 32 sections) with a 21° divergence ((a)-(b)), and a 2D version (16 x 32 sections) with a 24° divergence ((c)-(d)). Both chips maintain a footprint of approximately 5.0 mm x 3.8 mm.

While many of today’s addressable arrays are utilised for supplemental sensors, such as blind-spot monitors or short-range pedestrian detection, the future of primary long-range lidar lies in all-solid-state configurations. These systems will demand divergence angles significantly below 18° to maintain a high resolution over hundreds of meters. To meet this requirement, the AR VCSEL architecture is not just advantageous – it is an indispensable component. This form of emitter has a unique ability to provide low-divergence, high-power light in an addressable format, a set of strengths providing a technological foundation for the next decade of automotive sensing.

The road ahead

Thanks to high brightness AR-VCSELs, it’s possible to significantly extend the detection range and precision of VCSEL-based commercial lidar. This breakthrough may be widely adopted, as

AR VCSELs provide a universal light source for all ranges of commercial lidar.

The introduction of AR VCSELs are not just elevating performance to a new level. This technological breakthrough will have a profound impact on the economics of lidar, as well as the electric vehicle market. By providing a high-performance light source, manufactured by leveraging existing high-volume semiconductor processes, AR VCSELs are helping to drive down the cost of primary lidar units towards the critical \$100 mark. This is a tipping point, representing the threshold for mass adoption in mainstream passenger vehicles.

Results of greater affordability are already visible. Last year, lidar market penetration in the Chinese automotive sector exceeded 10 percent, with nearly all major manufacturers integrating these sensors into flagship and mid-range models. Over time, deployment will expand into basic models, with the overall penetration rate expected to reach 20-30 percent this year. And as AR-VCSEL technology continues to mature and scale, we forecast this trend to accelerate globally.

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SiC: A solution for photonics?

By combining controlled thickness with low defect density and industrial compatibility, Smart-Cut technology is creating high-quality SiC-on-insulator substrates that are opening the door to practical photonic integrated circuits

BY STÉPHANIE HUET FROM CEA-LETI

While SiC is best known as a material for power electronics, that's not its only application. This wide bandgap material is rapidly emerging as a compelling platform for next-generation photonic technologies, with applications ranging from non-linear optics to quantum systems. SiC provides a broad transparency window, strong optical non-linearities, and remarkable thermal robustness – that's a unique combination of properties that few materials match.

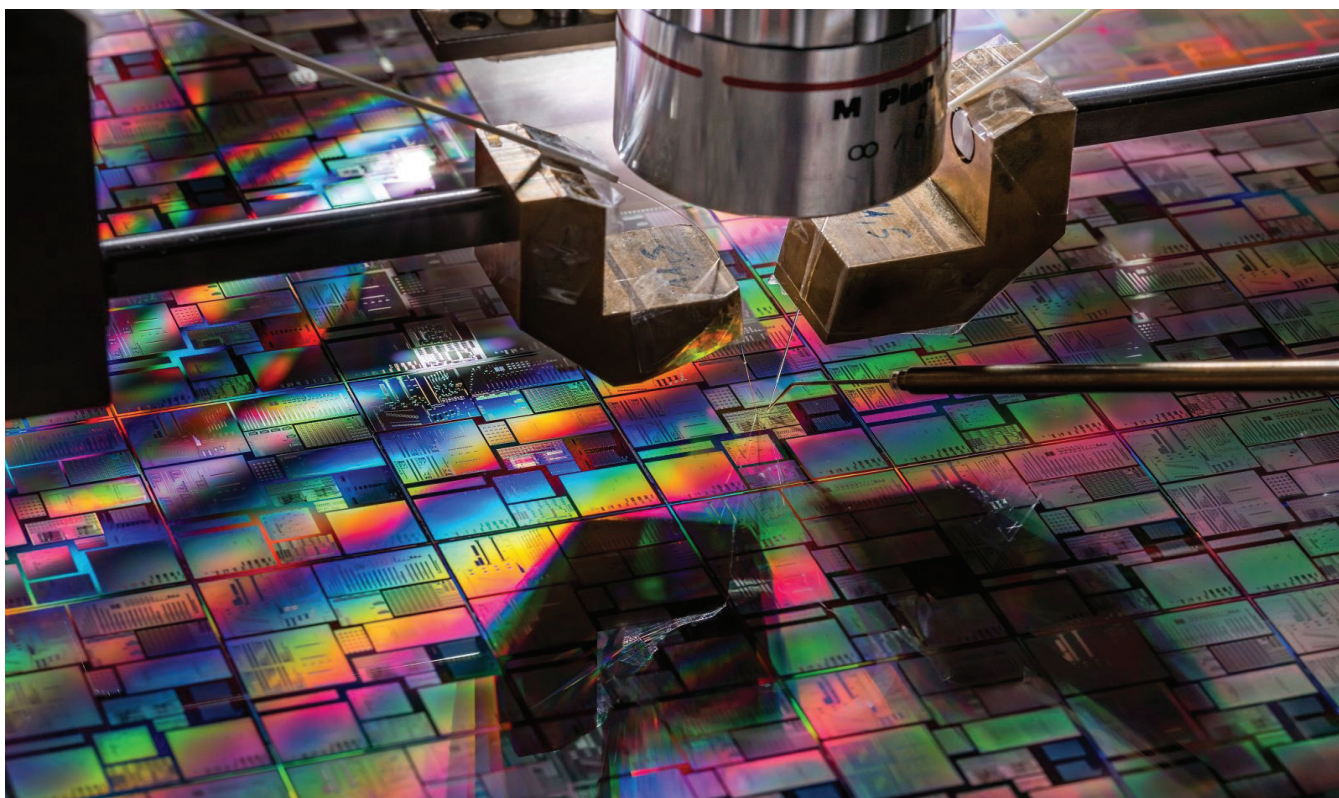
Yet despite these advantages, SiC photonics has failed to make the leap from lab to fab. That's not due to a lack of performance, but the absence of suitable substrates. It is challenging to produce high-quality SiC-on-insulator wafers, essential for guiding light efficiently, at scale and reasonable cost.

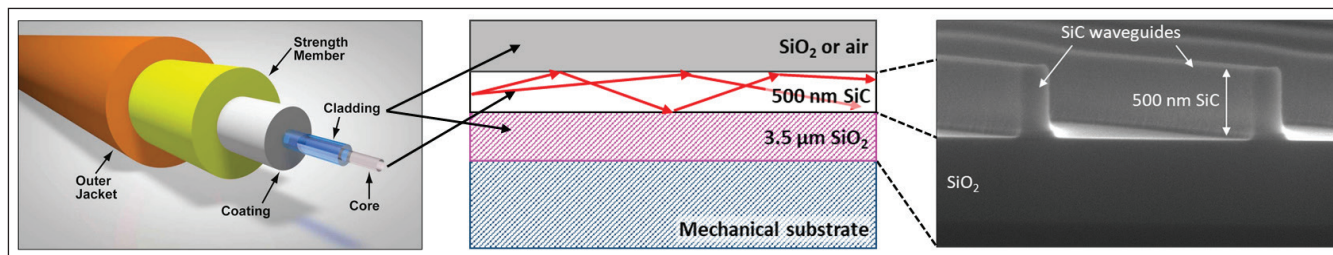
Overcoming this limitation is a critical challenge. Without a viable substrate platform, it's impossible to transition even the most promising device concepts into real-world technologies.

Rising platform

The appeal of SiC lies in its unique and wonderful set of attributes. Thanks to a bandgap that ranges from about 2.4 eV to 3.2 eV, this material supports operation from the visible to the mid-infrared. At the same time, it exhibits both second- and third-order optical non-linearities, enabling functions such as frequency conversion and high-speed modulation.

In practical terms, this means that SiC can support applications that are difficult to implement with silicon or SiN. There are opportunities in high-power





➤ From fibre to chip: light confinement in an optical fibre (left) and in a SiC-on-insulator waveguide (centre), where a 500 nm SiC layer on a 3.5 μm oxide enables strong confinement at 1550 nm; scanning electron microscopy cross section image (right) shows the fabricated structure.

photonic circuits, non-linear optical devices, and quantum systems based on optically active defects.

Key to exploiting these properties is tight optical confinement. In many ways, this mirrors the challenge encountered in optical fibres, where light is guided within a high-refractive-index core that's surrounded by lower-index materials. A comparable principle applies to SiC photonic devices.

However, instead of a cylindrical fibre, the structure is formed as a planar waveguide on a chip. In this case, a very thin layer of SiC acts as the region carrying light, with the surrounding materials ensuring confinement.

Many of the devices made from SiC are designed to operate at 1550 nm – that's the standard wavelength for optical communications. At this wavelength, the SiC layer must be thin, typically around 500 nm. Below this layer is a buried silicon dioxide layer, typically about 3.5 μm -thick, that's either exposed to air or covered by another dielectric material. The resulting stack provides a strong refractive-index contrast, ensuring that light is tightly confined within the SiC layer as it propagates through the device. Unlike optical fibres, which are flexible and guide light over kilometres, these waveguides are rigid structures fabricated on a chip, with light manipulated over much shorter distances.

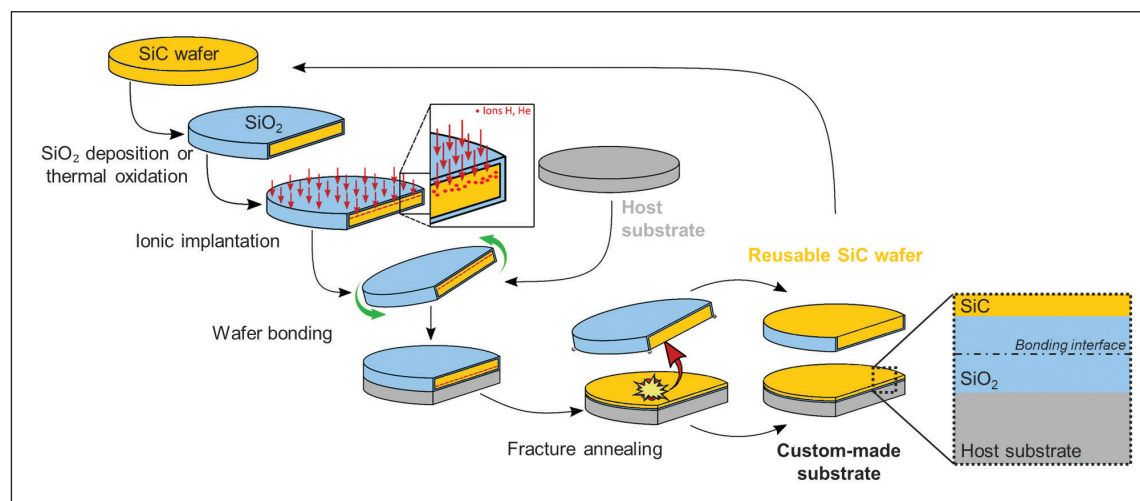
With these optical SiC-based chips, a high level of control is critical. Even small variations in thickness or interface quality increase optical losses and degrade performance.

Critical bottleneck

Developing SiC-on-insulator substrates has been far more challenging than initially anticipated. Unlike silicon photonics, which benefits from decades of industrial infrastructure built around silicon-on-insulator wafers, SiC photonics lacks a mature, widely available substrate technology.

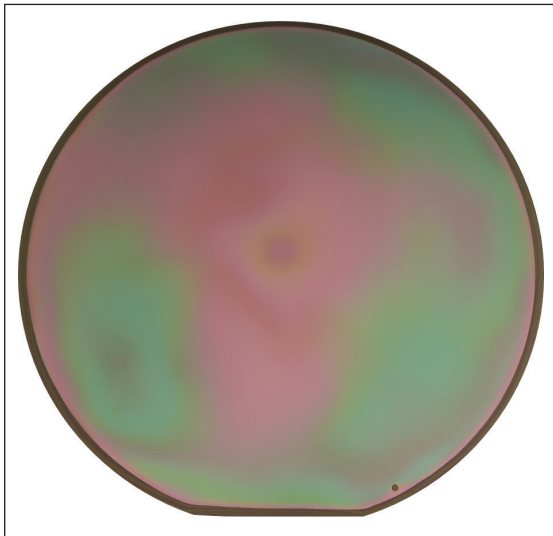
Early demonstrations employed bespoke substrates, fabricated using bonding and thinning techniques. While excellent material quality is possible, there are significant downsides, including poor thickness control, with variations reaching the micrometre scale, and an inherently wasteful process – much of the original material is removed. Turning to amorphous deposition improves scalability, but at the expense of optical performance. The absence of crystalline order limits non-linear effects and increases propagation losses, making these substrates less suitable for demanding photonic applications.

Due to these issues, developers of SiC photonic technologies are caught between high-performance, impractical solutions, and scalable, lower-quality alternatives. Bridging this gap is essential for industrialisation of SiC photonics.



➤ Smart Cut process for SiC-on-insulator substrates, enabling the transfer of a thin SiC layer and its optimisation through annealing and polishing for photonic applications.

Top view of a 150 mm SiC-on-insulator wafer demonstrating scalable fabrication of the platform.



Smart Cut edge

One promising route for overcoming these limitations involves turning to ion-cutting techniques, and in particular the Smart Cut process. Originally developed for fabricating silicon-on-insulator wafers, this technology is now producing thin, uniform layers with high reproducibility on an industrial scale.

When Smart Cut technology is applied to SiC, a thin crystalline layer of this wide bandgap material is transferred from a donor wafer onto a handle substrate, with a SiO₂ layer in between. This oxide layer provides the refractive-index contrast needed to confine light within the SiC layer, while the transfer process preserves the crystalline properties required for photonic devices.

A key strength of this method is its efficiency. Unlike bonding and thinning, the donor wafer can be reused, slashing material consumption and cost. And it's possible to control the thickness of the transferred layer with high precision, enabling the fabrication of waveguides with optimised optical properties.

The big challenge is to adapt Smart Cut to SiC – and that's not straightforward. The issue is that the quality of the transferred layer can be degraded during ion implantation, bonding, and

high-temperature annealing. Preventing this from happening is crucial when attempting to produce a viable photonic platform.

Process control

To address these challenges, our team at CEA-Leti has developed an optimised fabrication process for SiC-on-insulator substrates that's based on Smart Cut technology. Our approach focuses on three key matters: ion implantation conditions, thermal budget, and surface finishing.

Our process begins with the preparation of donor and handle wafers. Both are coated with a silicon dioxide layer. A fracture plane is then defined within the donor substrate with hydrogen ion implantation. As this step may introduce defects that diminish optical performance, we carefully optimised implantation conditions to minimise crystal damage while preserving efficient layer transfer. After bonding the two wafers through their oxide layers, we use thermal annealing to induce the transfer of a thin SiC layer onto the handle substrate.

A critical parameter for our process is the thermal budget. Annealing temperatures between 1200°C and 1400°C play a central role in restoring the crystalline quality of the transferred layer. Annealing at 1200°C leads to a significant recovery of the crystal structure, and when we increase the temperature towards 1400°C, material quality improves, coming close to that of bulk substrates.

It should be noted that we realise high material quality at temperatures compatible with silicon-based substrates. This opens the possibility to integrate SiC photonics with conventional microelectronics platforms.

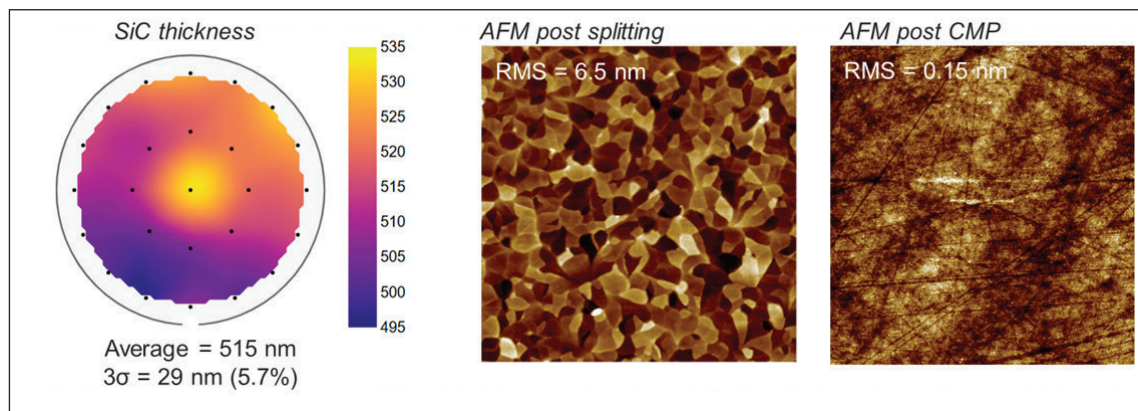
Crystal quality

The effectiveness of our optimised process is reflected in the structural and morphological properties of the resulting substrates. Across 150 mm wafers, we transfer a SiC layer with a thickness close to 500 nm, chosen as it corresponds to the optimal value for a waveguide operating at telecom wavelengths.

For SiC photonic applications, surface quality is equally critical. Immediately after layer transfer, surface roughness can be a concern, as it's on the order of several nanometres. But this is reduced dramatically after chemical-mechanical polishing, to around just 0.15-0.2 nm. These ultra-smooth surfaces are essential for minimising optical scattering losses in waveguides.

At the crystalline level, advanced characterisation techniques reveal a clear improvement in material quality after annealing. According to X-ray diffraction measurements, there's a reduction in peak broadening, indicating a decrease in lattice disorder. Raman spectroscopy reveals a similar story, with annealing enhancing crystalline coherence.

The most straightforward applications are low-loss waveguides, ring resonators and interferometers, as these devices are the building blocks of photonic integrated circuits. These devices are used to route, filter and manipulate light, in much the same way that transistors control electrical signals in conventional electronics



➤ Thickness uniformity map of the transferred SiC layer across the wafer (left), showing a 3σ non-uniformity of 5.7 percent. Atomic force microscopy scans (right) compare surface roughness before and after chemical-mechanical polishing, demonstrating significant surface improvement.

A more direct view of our material is provided with transmission electron microscopy. Images reveal that the transferred layer features well-defined lattice structures and clean interfaces. There are no detectable defects at the SiC/oxide boundaries.

Based on these findings, we can conclude that the combination of implantation, annealing, and polishing produces a high-quality crystalline film that's suitable for photonic applications.

Defect reduction

As well as ensuring sufficient structural quality, the control of defects within a material enables low optical losses. Even when the crystal lattice appears largely recovered, it's possible that residual defects interact with light and degrade device performance.

Helping determine if that is the case are photoluminescence measurements, which are highly sensitive to the presence of defect-related states. Using this optical technique, we uncovered broad defect-related emission bands associated with implantation-induced damage and defect complexes within the transferred layer.

When we optimise our implantation process, there's a clear reduction in these unwanted signatures, which were more prevalent in our previous generation of substrates. We find that as the material recovers, defect-related luminescence decreases, indicating a lower density of optically active defects. Cathodoluminescence measurements support this observation, showing a significant reduction in deep-level defect emissions.

Drawing on these insights, we have established that improving crystalline quality is only part of the solution. It's equally important to reduce residual defect populations, as they ultimately determine the optical quality of the material and its suitability for low-loss photonic devices.

Fortunately, we have demonstrated that through careful control of implantation and annealing conditions, we can significantly improve the optical quality of SiC-on-insulator substrates.

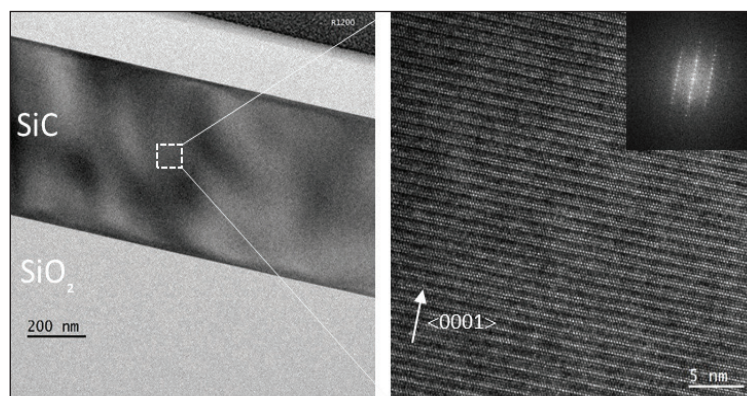
Device impact

While material characterisation provides important insight, the ultimate test for any photonic platform is device performance. In this context, our improvements have direct implications for the fabrication of waveguides and other integrated components.

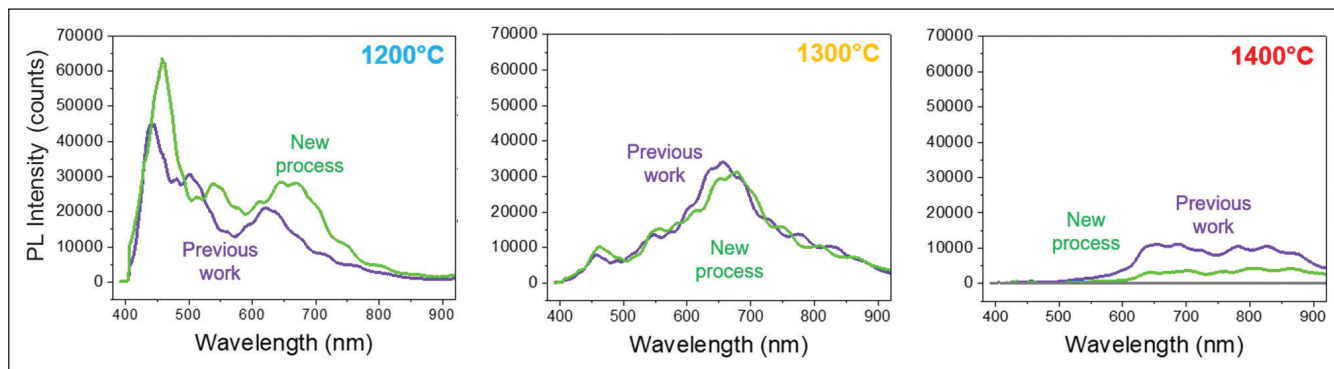
It is expected that the combination of precise thickness control, low surface roughness, and high crystalline quality trims propagation losses and enhances device efficiency. Smoother interfaces and fewer defects should reduce scattering and absorption, both of which are critical for high-performance photonic circuits.

Moreover, by producing uniform substrates at the wafer scale, we are opening the door to more complex and densely integrated devices. This could be a game-changer for applications such as quantum photonics, where numerous components must operate coherently on a single chip.

Although our detailed device measurements are ongoing, and we cannot disclose any details at this stage, our material properties are providing a strong foundation for the development of competitive SiC photonic technologies.



➤ Cross-sectional transmission electron microscopy (TEM) image of the optimised SiC-on-insulator structure after 1200 °C annealing (left). High-resolution TEM images and corresponding selected-area electron diffraction patterns (right) reveal a high crystalline quality within the transferred SiC layer.



► Photoluminescence spectra obtained at 405 nm excitation for SiCOI substrates post-annealed at (a) 1200°C, (b) 1300°C and (c) 1400°C fabricated with previous process and new process.

Future devices

Producing high-quality SiC-on-insulator substrates is not an objective in itself. The value of these structures lies in the photonic devices that can be built on top of them.

The most straightforward applications are low-loss waveguides, ring resonators and interferometers, as these devices are the building blocks of photonic integrated circuits. These devices are used to route, filter and manipulate light, in much the same way that transistors control electrical signals in conventional electronics.

When we look beyond passive devices, we have opportunities with SiC that are difficult to accomplish with silicon alone. The electro-optic and non-linear optical properties of SiC can be exploited to realise functions such as high-speed modulation, wavelength conversion and frequency comb generation – all are attracting growing interest for telecommunications and optical sensing.

Another promising area is quantum photonics. SiC can host optically active colour centres that emit single photons and act as quantum bits. Combining these quantum functionalities with wafer-scale photonic integration could enable compact chips for quantum communication and quantum sensing.

Due to this combination of functions, SiC-on-insulator is a promising platform for a wide range of integrated photonic devices.

Future scale

Beyond immediate performance gains, the broader significance of our work lies in its industrial potential. By leveraging a mature, scalable process such as Smart Cut, SiC photonics can be aligned with existing semiconductor manufacturing infrastructures.

A highlight of our work is that it shows that Smart Cut technology is compatible with different handle substrates. While the use of SiC handles enables high-temperature processing and optimal material matching, transferring the SiC layer onto silicon substrates offers additional advantages. In particular, this transfer facilitates integration with conventional microelectronics, and reduces overall system cost.

Our possible plans for further development include using polycrystalline SiC substrates to create fully SiC-based structures. In parallel, we may scale the process to larger wafer sizes, such as 200 mm, as this will be essential for realising the economies of scale for commercial deployment.

More broadly, our approach offers a way to reconcile three key, often conflicting requirements: high material quality, process scalability, and cost efficiency. Some success on all three fronts is critical for moving SiC photonics from the laboratory to real-world applications.

In short, rather than simply improving a fabrication process, our work opens the door to the industrialisation of SiC photonics. By combining Smart Cut technology with optimised implantation and annealing, we have provided a pathway to realising high material quality while maintaining scalability and cost efficiency.

As SiC photonics progresses towards practical applications, the availability of targeted, high-quality substrates will play a decisive role. Thanks to our advances, SiC is no longer just a promising material – it is now on the cusp of becoming a realistic platform for next-generation photonic integrated circuits.

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Double duty diamond

Equipping a GaN HEMT with a topside diamond film allows it runs cooler and more reliably, thanks to superior heat spreading and effective passivation

BY JEONG-KYU KIM AND SRABANTI CHOWDHURY FROM STANFORD UNIVERSITY

AT THE HEART of many RF and microwave power systems are GaN HEMTs. These devices offer a rare combination of high output power, strong efficiency, and operation at very high frequency. It's a set of attributes that ensures that this class of transistor is essential for a number of applications, ranging from radar and satellite communications to advanced defence systems and next-generation wireless infrastructure. Yet even these high-performance HEMTs face a stubborn internal limit. As operating power increases, self-heating inside the channel rises rapidly to become a critical factor that restricts the maximum achievable output power, as well as long-term device reliability and operational stability.

An increasing channel temperature introduces several penalties, all appearing at once. They

include a degradation in carrier transport as mobility drops, as well as an increasing on-resistance and a falling in efficiency. Due to this, performance that looks promising on paper maybe much harder to sustain in real operating conditions. At the same time, elevated temperature accelerates heat-driven degradation processes in contacts, barrier layers, and gate regions, causing devices to wear out faster and shorten their usable lifetime. The upshot is that designers of practical RF power amplifiers are often forced to step back from the theoretical performance limit, simply to maintain the junction temperature within a safe operating window. This means that thermal constraints frequently end up defining the real ceiling on output power, rather than the intrinsic electrical potential of GaN.

A second limitation appears at the device surface. Here trap states may introduce charge lag and distort local electric fields during high-frequency, large-signal operation. This quashes the maximum available drive current and makes the transistor behave less predictably. Often described as DC-RF dispersion, this phenomenon holds back the usable RF output and complicates device optimisation.

Unfortunately, thermal and trapping effects are closely coupled. Higher temperatures intensify trapping behaviour, and trapping can reshape local electric fields, while altering where power is dissipated. Working in menacing unison, these effects create an electro-thermal reliability challenge that's more severe with increases in power density and operating frequency.

Engineers have traditionally treated this issue as two separate problems. They addressed thermal limits with superior substrates, better packaging, and external heat spreaders, and improved electrical stability at the device-unit level through the introduction of dielectric passivation layers. But that disparate methodology, shaping GaN design for many years, prevents these devices from delivering their full potential. It would be more effective to address heat and surface effects together, close to where they originate.

At Stanford University, we pursue this unified approach, leveraging diamond, a material that combines exceptionally high thermal conductivity with strong electrical insulation. By integrating a low-temperature-grown polycrystalline diamond film directly on top of fully fabricated AlGaIn/GaN HEMTs, we are placing the world's most conductive material incredibly close to the channel hot-spot region, where heat is generated most intensely. In this topside position, diamond spreads heat efficiently away from the active region without creating an electrical conduction path, while serving as a surface passivation layer. This dual role improves thermal and electrical performance.

Heat bottleneck

To suppress surface trapping and mitigate DC-RF dispersion, Ga-polar GaN HEMTs feature surface passivation. The most widely adopted solution is deposition of a SiN_x layer – providing effective electrical passivation, this is now standard practice across industry. However, there's a critical limitation: SiN_x has a relatively poor thermal conductivity, so it is typically used at a thickness sufficient to ensure reliable trapping suppression.

Due to this weakness, it's problematic to pair SiN_x with a topside diamond heat spreader. As the SiN_x layer sits directly above the active region, it's a thermal barrier to heat flow from the channel hotspot to the diamond layer. It's possible to thin the SiN_x layer and improve thermal coupling, but that comes at the cost of weaker surface control and the return of DC-RF dispersion. Due to this, designers

seek the optimum trade-off when considering electrical stability and thermal performance.

But could compromise be avoided by employing a topside diamond layer, integrated close to the channel hotspot? Would this provide passivation-like surface stabilisation, while retaining excellent thermal spreading capability, and reducing or even removing the need for a thick SiN_x layer? If all this is possible, diamond would no longer function as just a heat spreader. Instead, it would act as a new kind of dual-function passivation layer – one that simultaneously improves heat extraction and suppresses dispersion. It's a combination that's especially attractive for high-power GaN transistors.

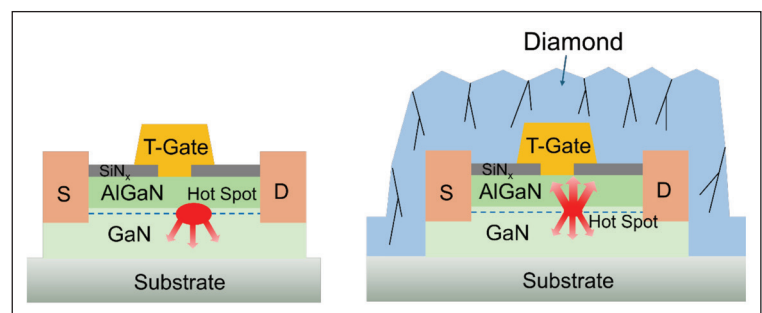
Close coupling

To put theory to the test, we have produced diamond-coated GaN HEMTs (see Figure 1), adding diamond with a microwave plasma CVD growth process that operates below 500°C. As this growth temperature remains within a device-compatible range, we deposit diamond after full transistor fabrication, including gate formation and metallisation. This enables a device-first, diamond-last integration sequence, and avoids exposure of sensitive features to harsh thermal cycles that threaten to degrade performance.

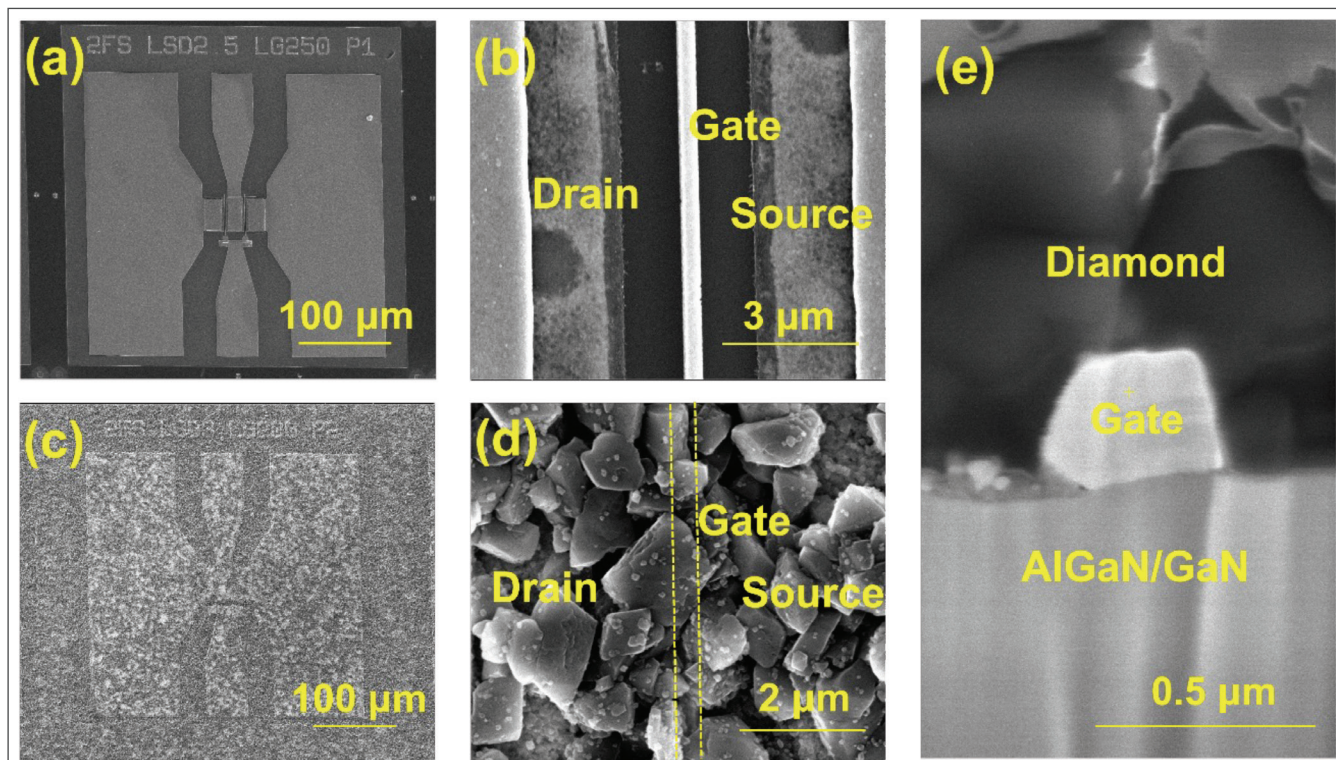
Our polycrystalline diamond layer, approximately 1-1.5 μm thick, is grown on top of an ultrathin SiN_x layer. With a thickness of roughly 10 nm, it's much thinner than would normally be used for passivation alone. According to electron microscopy and cross-sectional analysis (see Figure 2), we realise uniform, void-free diamond coverage across the device surface, including the narrow gate region. Our grain structure supports effective lateral heat spreading, and our geometry ensures that the thermal pathway is extremely close to our channel. In this configuration, an ultrathin dielectric separates the diamond layer from the active region. This architecture provides strong thermal coupling, while modifying the trapping environment at the surface.

Cooler channel

To quantify the thermal benefit of our technology, we turned to gate resistance thermometry. After



➤ Figure 1. Cross-sectional schematics of the device (left) before and (right) after topside polycrystalline diamond integration. Diamond integration enhances thermal dissipation from the hotspot, enabling more efficient heat flow in both upward and downward directions.



► Figure 2. Top-view scanning electron microscope (SEM) images of the fabricated AlGaIn/GaN HEMT used in this work: (a) before polycrystalline diamond passivation, (b) zoomed-in view of the gate finger region showing the adjacent source and drain contact, (c) after polycrystalline diamond passivation, and (d) zoomed-in view of the gate finger region covered with polycrystalline diamond grains. Figures (c) and (d) confirm uniform polycrystalline diamond coverage across the entire device, including the gate finger region. (e) Focused ion beam (FIB) SEM cross-sectional image of the gate metal region, showing the top-side polycrystalline diamond layer uniformly encapsulating the gate metal without voids.

calibrating the temperature dependence of the gate resistance, we monitored resistance while the device dissipated power, and converted this signal into average channel temperature. This provides a direct electrical method for tracking internal heating under realistic high-power operating conditions.

Our measurements revealed a substantial reduction in device temperature (see Figure 3). When the HEMTs delivered a DC power density near

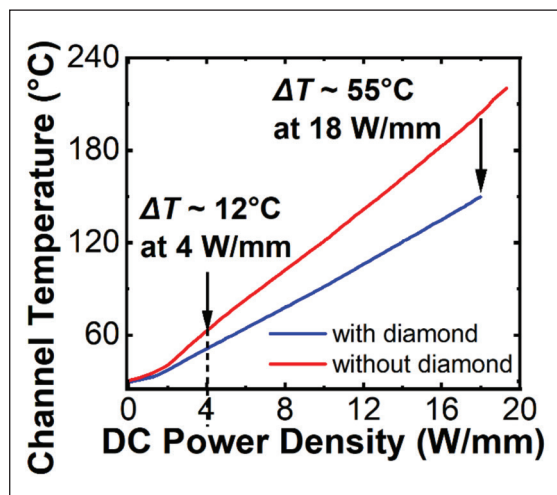
18 W mm^{-2} , the average channel temperature dropped by roughly 55°C after diamond integration. At lower power densities that difference reduce, but it's still 12°C at a power density near 4 W mm^{-2} . These results confirmed that the addition of a top-side diamond layer introduces an efficient thermal pathway and significantly lowers the effective thermal resistance.

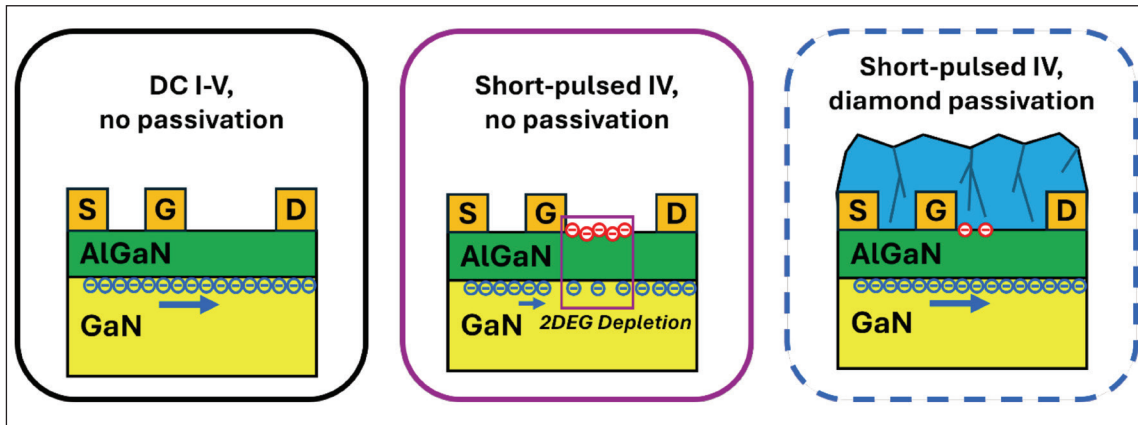
As well as lowering the operating temperature, heat flows in different directions. With the introduction of our technology, as well as a downward flow through the GaN epilayer and into the substrate, heat spreads upward into the diamond layer. As the diamond, which sits very close to the hotspot, has high in-plane thermal conductivity, heat is redistributed laterally across the device surface. This spreading is particularly beneficial in multi-finger RF transistors, as it combats localised heating that can create strong temperature gradients and limit uniform current operation.

Trap control

Electrical measurements show that our diamond layer improves surface stability. We determined this by examining surface trapping under high-frequency operation – this is accomplished by comparing DC current-voltage characteristics with short-pulsed current-voltage characteristics, using electrically stressed quiescent bias conditions. When trapping

► Figure 3. Gate resistance thermometry results indicating strong channel temperature reduction after top-side diamond integration.





➤ Figure 4. Conceptual illustration of DC-RF dispersion and the effect of diamond passivation in AlGaIn/GaN HEMTs. Without passivation, surface traps have little impact under DC conditions, but under short-pulsed operation they capture charge, leading to channel depletion and current collapse. With diamond passivation, surface trapping is suppressed, preserving channel charge and maintaining stable current under dynamic operation.

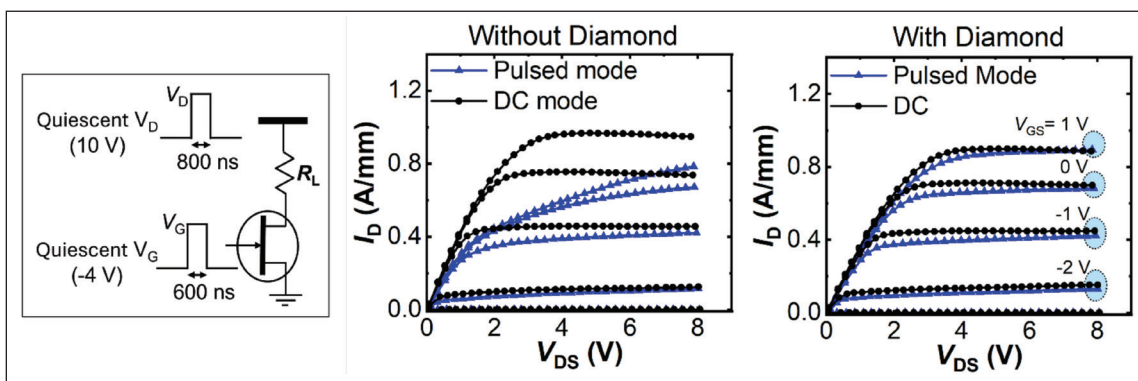
is significant, there's a reduction in pulsed current and a clear discrepancy from DC behaviour (see Figure 4). This undesirable phenomenon, known as current collapse, is a well-known signature of charge trapping at the device surface. Following diamond deposition, dispersion is dramatically reduced. On-current mismatch nearly disappears, and knee-voltage movement is minimal, even under more demanding bias conditions.

An investigation of multiple devices determined that diamond integration reduced dispersion values from around 30-40 percent to roughly 5-8 percent (see Figure 5). That's a level of suppression comparable to that realised with conventional SiN_x passivation. This shows that the diamond overlayer, together with the ultrathin dielectric underneath, is sufficient to control trapping, and indicates that diamond actively contributes to stabilising the surface. In other words, as well as increasing heat flow, the diamond layer improves electrical behaviour.

Our polycrystalline diamond layer, approximately 1–1.5 μm thick, is grown on top of an ultrathin SiN_x layer. With a thickness of roughly 10 nm, it's much thinner than would normally be used for passivation alone

Scaling ahead

Our study provides an early example of how a low-temperature CVD-grown diamond layer improves a conventional GaN HEMT on two fronts: reducing surface trapping and enhancing heat removal. In higher-voltage GaN HEMTs, featuring advanced field-plate designs, self-heating becomes much more severe as power density increases. This makes thermal resistance a key factor limiting



➤ Figure 5. Measured DC and short-pulsed I-V characteristics of GaN HEMTs without (left) and with (right) diamond passivation. Without diamond, a clear reduction in pulsed drain current compared with DC behavior indicates strong DC-RF dispersion due to surface trapping. With diamond passivation, the discrepancy between DC and pulsed currents is significantly reduced, demonstrating effective suppression of current collapse and improved dynamic performance.

performance. As our technology positions the diamond layer very close to the channel hotspot, with no thick SiN_x dielectric layer in between, cooling should become even more pronounced as bias voltage and output power increase during amplifier operation.

We expect applying our dual-function diamond layer to high-voltage GaN transistors will enable higher

output powers, improved efficiency, and longer device lifetimes. Our initial results are just a baseline demonstration, and even larger gains are likely in more aggressively scaled, higher-power RF GaN devices.

Beyond GaN

Our work points to a broader shift in how thermal materials may be applied to compound semiconductor devices. Rather than serving as only external heat spreaders, materials such as diamond can become functional parts of the device. When integrated late in the fabrication process at low temperature, diamond is not just influencing heat flow – it is also smoothing peaks in surface electric fields and combatting trapping behaviour.

A topside diamond layer that performs a dual role – spreading heat and passivating the surface – provides a practical path toward the production of compound semiconductor transistors that run cooler, behave more predictably under large-signal operation, and scale more effectively to higher power densities. As integration techniques continue to advance, we anticipate dual-function layers, such as diamond, will become broadly useful across a wide range of next-generation compound semiconductor technologies.

FURTHER READING

- J.-K. Kim *et al.* “Demonstration of the dual role of topside diamond as a passivation layer and heat spreader in AlGaIn/GaN HEMTs” IEDM (2025)
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- M. Malakoutian *et al.* “Low Thermal Budget Growth of Near-Isotropic Diamond Grains for Heat Spreading in Semiconductor Devices” Adv. Funct. Mater. **32** 2208997 (2022)
- R. Soman *et al.* “Novel all-around diamond integration with GaN HEMTs demonstrating highly efficient device cooling” IEDM (2022)

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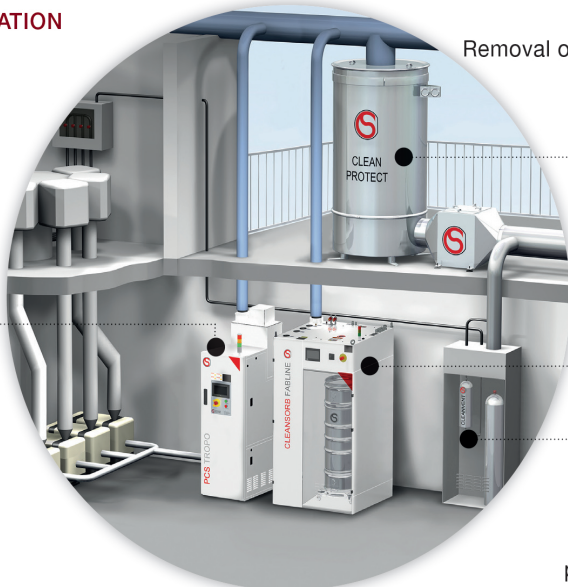
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Revolutionising short-circuit reliability

Equipped with a thin AlGaIn barrier, the GaN HEMT gives a short-circuit performance superior to that of SiC MOSFETs and silicon power devices

ENGINEERS from China have demonstrated that the introduction of a thin AlGaIn barrier can deliver a substantial hike in the short-circuit reliability of the GaN HEMT. The III-N transistors produced by the team – a partnership between researchers at the University of Electronic Science and Technology of China, Sichuan Ai-Link Technology Company, and Shenzhen Pinghu Laboratory – withstand up to 12,000 repetitive short-circuit cycles at a bus voltage of 450 V. In comparison, commercial GaN HEMTs running under those conditions fail at the third cycle.

According to team spokesman Qi Zhou, an affiliate of the University of Electronic Science and Technology of China, Shenzhen Institute of Advanced Study and UESTC, their devices' robustness will help efforts to drive the, broader adoption of GaN power devices in high-reliability power-conversion applications. Devices produced by Zhou and co-workers are strong on a number of fronts – they combine the exceptional switching performance and power density that GaN is renowned for with a level of fault robustness that's comparable with established silicon and SiC technologies.

These assets will be welcomed by designers of motor drives, industrial inverters, UPS systems, renewable-energy converters, and electric-vehicle powertrains. In all these applications, short-circuit faults may occur during abnormal operating conditions, and power devices must withstand the resulting irregularities until system-level protection detects the fault and safely shuts down the device. So crucial is the need for short-circuit capability that it's part of standardised testing, says Zhou.

The team's devices, fabricated from 150 mm GaN-on-silicon epiwafers, feature a 2 μm -thick GaN buffer, a 2.85 μm -thick AlGaIn/GaN superlattice, a GaN channel, and an AlGaIn barrier with a thickness of 11 nm. Processing produced HEMTs with a *p*-GaN length of 1.42 μm , a single gate field plate of 3.32 μm , and a source field plate length of 2.4 μm .

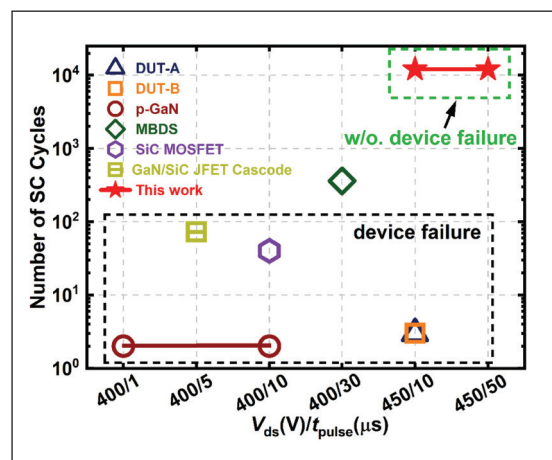
Zhou admits that this design may not appear that radical, since it relies on just reducing the thickness of the AlGaIn barrier. "However, the underlying design is not simply a matter of making the AlGaIn barrier thinner, because the barrier is closely coupled with the *p*-GaN gate and the overall device structure."

Note that if the barrier is too thin, it could shift the threshold voltage, leading to a reduction in the available gate-control margin, as well as increases in gate-drive requirements and associated turn-

on losses. "This is particularly important for enhancement-mode devices, where the threshold voltage must remain sufficiently positive to ensure robust normally-off operation," says Zhou.

Another concern that can arise if the barrier is too thin is an overwhelming increase in the electric field across the gate stack. A stronger field may facilitate gate-current injection, potentially increasing static gate leakage and electrical stress on the gate structure.

Zhou and co-workers avoid all these issues, while still benefitting from a reduced barrier thickness that substantially enhances the transient gate current during a short-circuit event. "This distinction is central to our design: the objective is not to increase gate current indiscriminately, but to maintain low static gate leakage while obtaining a strong transient gate-current response during a short-circuit fault to provide



➤ The short-circuit capability of GaN HEMTs with a thin AlGaIn barrier compare favourably with other forms of power device.

the adaptive short-circuit protection to the device."

Benchmarking of the team's devices shows that they outperform 1.2 kV SiC MOSFETs and 650 V silicon power transistors (see Figure).

One of the next goals for the team is to further optimise its AlGaIn barrier and *p*-GaN gate structure, together with the relevant epitaxial and device parameters.

In parallel, efforts will be directed at systematically investigating the effects of gate resistance and gate-drive conditions on transient gate-current response and short-circuit behaviour.

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➤ N. Yang *et al.* Appl. Phys. Lett. 129 063306 (2026)

V-defects boost green LEDs efficiency

When the arms of half-loop threading dislocations are opened into V-defects, green LEDs deliver higher efficiencies

RESEARCHERS from the University of California, Santa Barbara (UCSB), have shown that V-defects and an optimised AlGaIn cap enhance the efficiency of green III-N LEDs. When the emitters produced by the West-coast team also feature distributed Bragg reflectors (DBRs) to increase light extraction, external quantum efficiency peaks at 44 percent, and wall plug efficiency hits 37 percent.

Producing green III-N LEDs with a high efficiency is a well-known challenge, due to the poor material quality that results from a low temperature required for the growth of indium-rich InGaIn quantum wells, as well as polarisation-related effects. When stretching to longer emission wavelengths, increases in the quantum-confined Stark effect drag down radiative recombination rates and enhance polarisation-induced barriers, which hamper carrier injection and lead to a higher forward voltage.

Helping address the low efficiency in green LEDs are V-defects. These hexagonal pyramid-shaped depressions, containing six semipolar sidewalls that typically form at the apex of threading dislocations during kinetically limited low-temperature growth, provide an avenue for efficient carrier injection into the quantum wells.

According to the team, it is possible to ‘properly engineer’ the V-defect density on a patterned sapphire substrate through the generation of pure-edge dislocation half-loops – they are realised by growing a preparation layer with a high silane or disilane flow at low temperature. When a low-temperature GaIn layer is deposited afterwards, this opens the half-loop threading dislocation arms into V-defects.

Fabrication of team’s LEDs began by loading a patterned GaIn-on-sapphire template into an MOCVD chamber and depositing a 600 nm-thick *n*-GaIn buffer at 1220°C, followed by a 60 nm-thick half-loop formation layer at 800°C, grown using a disilane flow of 9.9 sccm. It is said that heavy silicon-doping is needed to form the edge-dislocation half-loops that will be opened into V-defects.

During growth at the relatively low temperature of 800°C, existing threading dislocations open into V-defects. To ensure a uniform V-defect size, the team grew a 60 nm-thick *n*-GaIn layer at 1000 °C to planarize over the open V-defects, before adding another 60 nm-thick *n*-GaIn layer at 800 °C to

open these defects. The addition of a 25 period superlattice, formed from alternating layers of 3.5 nm-thick $\text{In}_{0.05}\text{Ga}_{0.95}\text{N}$ and 3.5 nm-thick GaIn, enlarged the V-defects. On this V-defect template the team added an active region, grown under nitrogen to promote V-defect propagation, that contains 8 periods with a: 0.5 nm-thick GaIn pre-layer, designed to recover surfaced morphology; followed by a 3.3 nm-thick $\text{In}_{0.15}\text{Ga}_{0.85}\text{N}$ quantum well and a 2.3 nm-thick AlGaIn cap, both grown at 810°C; and a quantum barrier, with 6 nm-thick GaIn grown at 850°C, and then 3 nm-thick GaIn grown at 900°C.

Growth of the green LEDs concluded with the addition of magnesium-doped GaIn at 960°C. A 60 nm-thick *p*-GaIn layer planarized the open V-defects, before the addition of a 12 nm-thick contact layer. Samples were then annealed in air at 630°C for 15 minutes.

Device measurements revealed that optimising the growth of the 2.3 nm-thick AlGaIn cap – realised by increasing the flow rate for the gallium precursor and reducing that for ammonia – increases the peak external quantum efficiency and wall plug efficiency from 29 percent and 35 percent, to 34 percent and 41 percent, respectively. Even higher values of 37 percent and 44 percent, respectively, come from combining the optimised AlGaIn cap with the DBR.

Inspecting the active region with cross-sectional transmission electron microscopy revealed that as well as V-defects, there are trench defects in the active region, originating at the interface between the quantum wells and the caps. These trench defects consist of a basal-plane stacking fault, terminated by a stacking mis-match boundary that acts as a non-radiative centre.

When evaluating their device, the team points out that the quality of the capping layer plays a role in efficiency enhancement. It is noted that last year a team from China reported peak values of 65 percent external quantum efficiency, and 60 percent wall plug efficiency, for LEDs produced with an aluminium treatment step immediately after quantum well growth.

For the UCSB devices, there is a sizeable difference between values for external quantum efficiency and wall plug efficiency. Motivated by this observation, the team is planning to investigate the impact of AlGaIn caps on lateral injection through V-defects. The researchers hope that by using the growth conditions they have developed, they will improve the quality of their low-temperature capping layers, and ultimately increase the efficiency of their long-wavelength LEDs.

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► A. Quevedo *et al.* Appl. Phys. Lett **129** 053301 (2026)

Superior *p*-GaN ohmic contacts

Depositing a very thin magnesium film on a *p*-GaN surface, followed by soft annealing and chemical cleaning, creates an ohmic contact with minimal contact resistance

A COLLABORATION led by Hiroshi Amano's group at Nagoya University is pioneering a process for producing very thin *p*-GaN layers with an ultra-low contact resistance. According to the team – a partnership between Nagoya University, Cornell University, the University of Illinois Urbana-Champaign, MIT, City University of Hong Kong, and Suzhou Institute of Nano-Tech and Nano-Bionics – their simple low-thermal-budget post-growth approach, involving magnesium deposition, annealing, and chemical cleaning, creates high-quality ohmic contacts on thin *p*-GaN layers.

A wide range of devices should benefit from the team's process that realises a specific contact resistance of just $1\text{--}3 \times 10^{-4} \Omega \text{ cm}^2$. This ultra-low resistance reduces operating voltage, boosts efficiency, and trims power consumption.

Note that there are additional benefits for devices that require a very thin *p*-GaN layer, or are vulnerable to process-induced damage.

That means that HBTs will benefit, because the *p*-GaN base is very thin – during device fabrication the exposed base surface can suffer significant damage from dry etching, which is difficult to repair.

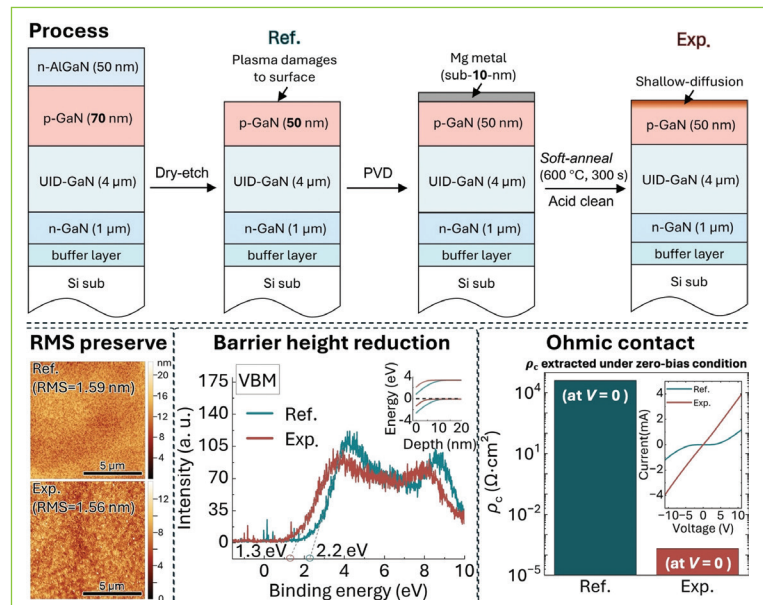
"In contrast, our magnesium-annealing approach can be applied directly after processing, and provides a relatively simple way to recover the electrical performance of the exposed *p*-GaN surface and improve the overall device characteristics," remarks team spokesman, Haitao Wang.

The researcher from Nagoya University points out that UV LEDs and lasers could also be improved with the team's process, as it enables the *p*-GaN to be very thin, aiding light extraction and optical efficiency.

"Our technique is attractive in this situation, because it can improve the contact properties of very thin *p*-GaN without introducing severe surface roughening. This provides an important combination of electrical and optical advantages."

The team's process for producing ohmic contacts is markedly different from conventional approaches, which involve epitaxial growth of an extremely thin, heavily doped *p*⁺-GaN contact layer.

According to Wang, traditional approaches place stringent requirements on epitaxial growth and doping control, and leave the *p*-GaN surface susceptible to damage from a dry-etching plasma process, required before metal-electrode formation.



Since 2021, Amano's team has been investigating the formation of low-resistance ohmic contacts through the deposition of magnesium films on GaN surfaces. Initially, researchers produced magnesium films with a thickness of several tens of nanometres, using relatively high annealing temperatures, but this led to substantial roughening of the GaN surface after annealing. Now they have refined the process, depositing a sub-10-nm-thick metallic magnesium film on *p*-GaN, before undertaking a 5 minute 'soft anneal' at 600°C, followed by a HCl clean.

X-ray photoelectron spectroscopy measurements have revealed that the energy separation between the valence-band maximum and the Fermi level has decreased from 2.2 eV to 1.3 eV. This suggests that soft annealing reduces the effective hole-injection barrier at the metal/*p*-GaN interface while narrowing the depletion region and enhancing hole tunnelling.

Using their process, the team produced quasi-vertical *p-i-n* diodes with a flat *p*-GaN surface, favourable hole-transport characteristics, a high breakdown voltage, and a low leakage current.

According to Wang, the team's next goals are to demonstrate the universality of their technique on more GaN devices, understand the underlying physics in much greater detail, and establish a systematic and standardised magnesium-annealing process platform.

➤ Superior *p*-GaN contacts result from physical vapour deposition of a thin layer of magnesium, followed by a 'soft' anneal and an acid clean.

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➤ H. Wang *et al.* Appl. Phys. Lett. **129** 063306 (2026)

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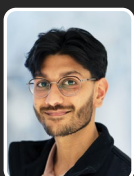
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