

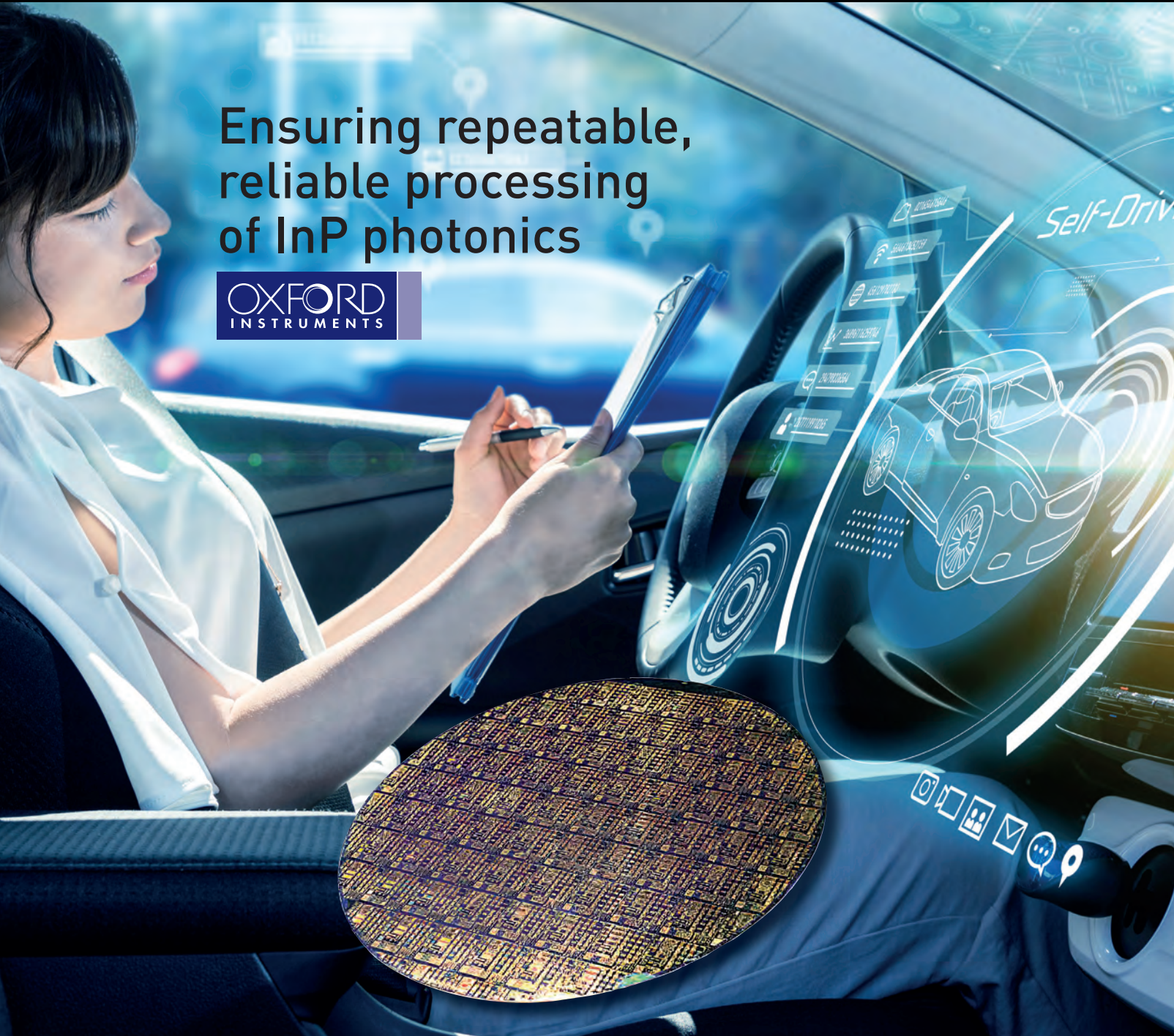


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VIEWPOINT

BY DR RICHARD STEVENSON, EDITOR

How green?

▶ THERE'S A LOT to like about working in our industry. It involves an eclectic mix of materials science, statistics, engineering and physics – sometimes including some quantum mechanics. And there's also the chance to do our bit for the planet by developing and producing devices sporting increased energy efficiency.

For many years, those working within our power electronic sector have been promoting the superior efficiency of wide bandgap devices, and how this can reduce the energy consumed by power supplies and motors and boost the yield from PV systems. However, there is a tendency to overlook the additional energy required to make SiC and GaN devices, rather than those based on silicon.

When a more rigorous analysis is applied, do wide bandgap devices stand up to that scrutiny? After all, it takes incredibly high temperatures to produce SiC, and a lot of energy to make and ship all the tools needed to produce devices.

Fortunately, if you go through the maths, wide bandgap materials retain their green credentials. According to work presented by John Palmour at this year's European Conference on SiC and Related Materials, although it can take four times as much energy to produce a SiC MOSFET as a silicon IGBT, the payback is huge. When deployed in an automobile, there is a seven-fold benefit for the SiC MOSFET, and in an inverter for PV, this factor can be well over 50 (see p. 34 for more details).

Our industry is also having a positive impact in communication infrastructure. Given humanity's insatiable demand for data in, there is a need to keep cutting the energy-per-bit just to keep a



lid on the energy consumption from this sector. Developers and producers of InP transmitters are certainly playing their part in this endeavour by increasing the extent of wavelength-division multiplexing and using novel ridge waveguides to trim optical losses (see p. 46 for a report on this topic, based on presentations delivered at this year's International Semiconductor Laser Conference).

You may be wondering what is the size of the carbon footprint associated with my reporting on both these conferences. Well, not that much, as I attended on-line. However, while this is convenient, this digital form fails to provide anywhere near the same level of interaction with fellow attendees as an in-person event. That much is clear from this year's CS International, which is covered on pages 22 to 26. At this meeting everyone I met revelled in the chance to cement established relationships and forge new ones.



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Navitas tops GaN power device shipments

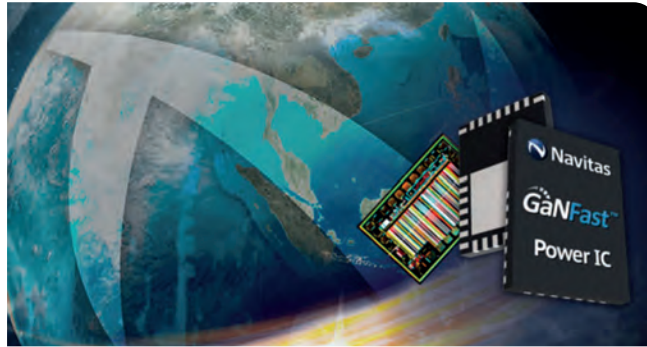
DEMAND for fast chargers used for various consumer electronics has been quickly rising. For instance, smartphone brands such as Xiaomi, OPPO and Vivo led the industry by releasing fast chargers in 2018, subsequently gaining consumer acceptance via their fast chargers' competitive advantages in cooling efficiency and compact physical dimensions.

At the moment, notebook computer manufacturers are also expressing a willingness to adopt fast charging technology. Hence, the GaN power devices segment became the fastest-growing category in the third-generation semiconductor industry. TrendForce expects annual GaN power devices revenue for 2021 to reach \$83 million, an impressive 73 percent year-over-year increase.

Navitas is projected to obtain a 29 percent market share (measured by total shipment) and overtake Power Integration for the top position this year. Thanks to Navitas' proprietary GaNFast power IC design and great relationships with its partners in the semiconductor supply chain, it has become the largest supplier of GaN power IC chips in the consumer electronics markets.

The company is currently partnering with leading smartphone and PC OEMs, including Dell, Lenovo, LG, Xiaomi and OPPO. Given the rising demand for Navitas' fast charge ICs from clients this year, the company is expected to transition its chip orders in 2H21 from TSMC's Fab 2, which is a 6-inch wafer fab, to other 8-inch fabs instead, in order to resolve the issue of insufficient production capacity. At the same time, Navitas is also targeting SAIC (Xiamen Sanan) as a potential supplier of foundry services. With regards to other markets for GaN applications, Navitas will likely target the data centre market first by releasing related products in 2022.

Proven power management IC supplier PI (Power Integrations) was the longtime undisputed leader in the GaN power



devices market. For this year, PI has released the latest InnoSwitchTM4-CZ series of chips, based on its proprietary PowiGaN technology. Featured in products such as Anker's 65 W fast chargers, the InnoSwitch4-CZ chips have received universal acclaim from the fast charge market. In addition, PI's recently released integrated AC-DC controller and USB PD controller ICs are expected to be major drivers of PI's revenue growth this year. With an estimated 24 percent market share, PI will likely take the runner-up spot in the ranking of GaN power devices suppliers for 2021.

China-based Innoscience is expected to possess the third-highest market share in 2021, due to increased support from the Chinese government.

The market share of China-based Innoscience is projected to rise to 20 percent this year, the third highest among GaN suppliers. Innoscience's performance can primarily be attributed to the massive spike in its shipment of high-voltage and low-voltage GaN products. In particular, Innoscience's GaN power ICs, used for fast chargers, are now entering the supply chains of tier-one notebook manufacturers for the first time ever. At the same time, while the company's Suzhou-based 8-inch wafer fab has already kicked-off mass production, Innoscience will gradually expand the competitive advantage derived from its IDM business model in the fast-evolving GaN industry.

Not only is the company currently actively cultivating its presence in applications including Lidar, on-board chargers for EVs, and LED power supplies, but it will

also look to increase its market share even further next year via its diverse product mix.

The Chinese government has been increasing its support of the domestic third-generation semiconductor industry, while the ongoing China-US trade war has also forced Huawei and other companies in the downstream supply chain to reassess potential

supply chain risks. Taken together, these factors have now created the perfect opportunity for China's third-generation semiconductor material and component suppliers in both qualification/validation and production of domestic substitutes, thereby further propelling the growth of the third-generation semiconductor industry in China.

According to TrendForce's investigations, China invested in about 25 projects aimed at expanding the domestic production capacity of third-generation semiconductors in 2020 (excluding GaN-based optoelectronics materials and devices). These projects totalled more than RMB¥70 billion, a 180 percent year-over-year increase.

Commercial products manufactured using SiC substrates, which are the most crucial materials in the third-generation semiconductor industry chain, are primarily based on 4-inch wafers in China, but the country is currently migrating to 6-inch wafers.

Although the technological gap between China and its global competitors is fast narrowing, China is still noticeably inferior in terms of monocrystalline quality, resulting in a relatively low self-sufficiency rate of high-performance SiC substrates. TrendForce's data indicate that, as of 1H21, about seven production lines have been installed in China for GaN-on-silicon wafers, while at least four production lines for GaN power devices are currently under construction, also in China. On the other hand, China possesses at least 14 production lines (including those allocated to pilot runs) for 6-inch SiC wafers.

GM and Wolfspeed forge SiC agreement

GENERAL MOTORS and Wolfspeed have announced a strategic supplier agreement to develop and provide SiC power device solutions for GM's future electric vehicle programmes. Wolfspeed's SiC devices will enable GM to install more-efficient EV propulsion systems that will extend the range of its rapidly expanding EV portfolio.

The SiC will specifically be used in the integrated power electronics contained within GM's Ultium Drive units in its next-generation EVs. As a part of the agreement, GM will participate in the *Wolfspeed Assurance of Supply Program*, which is intended to secure domestic, sustainable and scalable materials for EV production.

"Our agreement with Wolfspeed represents another step forward in our transition to an all-electric future," said Shilpan Amin, GM vice president, Global Purchasing and Supply Chain. "Customers of EVs are looking for greater range, and we see SiC as an essential material in the design of our power electronics to meet customer demand. Working with Wolfspeed will help ensure we can deliver on our vision of an all-electric future."

"Our agreement with GM further

demonstrates the automotive industry's commitment to delivering innovative EV solutions to the market and using the latest advances in power management to improve overall vehicle performance," said Gregg Lowe, CEO of Wolfspeed.

"This agreement ensures long-term supply of SiC to GM to help them deliver on their promise of an all-electric future."

The SiC power device solutions will be produced at Wolfspeed's 200 mm-capable Mohawk Valley Fab in Marcy, New York, which is the world's largest SiC fabrication facility. Launching in early 2022, this state-of-the-art facility will dramatically expand capacity for the company's SiC technologies, which are in increasing demand for EV production and other advanced technology sectors around the world.

The widespread adoption of SiC as an industry standard semiconductor for transportation supports the automotive industry's rapid transition to clean energy vehicles. SiC enables greater system efficiencies that result in longer EV range while lowering weight and conserving space. Wolfspeed's technology is fueling electric propulsion systems across the entire voltage spectrum – from 400 V to 800 V – and beyond.



II-VI expands UK plant

II-VI has announced a major expansion of its compound semiconductor fab in Newton Aycliffe, County Durham, UK. This will lead to the creation of a large number of jobs in the North East, UK.

The company, which has its headquarters in Pennsylvania, is investing in its III-V compound semiconductor technology platform in the UK to sustain its market leadership and long-term growth.

As a result, it is expanding its team on Aycliffe Business Park by recruiting materials scientists, process engineers, device engineers, manufacturing technicians and operators. The 310,000 square feet fabrication plant at Aycliffe features advanced manufacturing and development facilities.

Jason McMonagle, senior director of operations at II-VI, said: "This expansion significantly increases our manufacturing capacity and represents a real vote of confidence in the Aycliffe site. All as we look to advance the state-of-the-art, next-generation radio frequency and optoelectronic device technology."

II-VI has research and development, manufacturing, sales, service and distribution facilities worldwide and the team at Aycliffe has a wealth of experience in compound semiconductor technology, design and manufacture.

II-VI's existing County Durham site (previously Kaiaam) was acquired in 2017 as part of the company's long-term strategy to scale up its compound semiconductor technology platforms and global manufacturing operations to serve rapidly growing markets created by the convergence of communications, computing and sensing.

Rohm and Zhenghai Group to establish joint SiC module business

THE ZHENGHAI GROUP has signed a joint-venture agreement to establish a new company in the power module business. The new company, Haimosic, is scheduled to be established in China in December 2021, and will be owned 80 percent by Shanghai Zhenghai Semiconductor and 20 percent by Rohm.



The new company will engage in the joint-venture business of development, design, manufacturing and sales of power modules using SiC power devices, with the aim of developing a power module business that is ideal for traction inverters and other applications in new energy vehicles.

The agreement will help to develop highly efficient power modules by combining the inverter technology of the Zhenghai Group companies, the module technology of both companies, and Rohm's cutting-edge SiC chips.

The module products to be developed through the new company are already scheduled to be used in electric vehicles, and mass production will begin from 2022.

The Zhenghai Group and Rohm will work closely with this new company to contribute to further technological

innovation through the development and widespread use of SiC power modules.

Bi Bohai, chairman of Zhenghai Group, said: "Rohm is a respected global leader in silicon carbide devices. The establishment of a joint venture between Rohm and the Zhenghai Group to develop the silicon carbide power module business will surely bring new changes to the power module market."

Through more than 30 years of development, Zhenghai Group has accumulated rich industrialization experience in many industries such as rare earth permanent magnets, regenerative medicine, automobile interiors, and electronic information.

The Zhenghai Group has determined to make the power module business a strategic business for the Group, giving it the greatest support in terms of capital and human resources.

"Combining Rohm's advanced power device technology with Zhenghai's industrialization capabilities, we believe that the joint venture will contribute to the development of China's power module industry," added Bohai.

Isao Matsumoto, president and CEO of Rohm, added: "We are very pleased to establish a joint venture with the Zhenghai Group, which has a wide range of businesses in China."

"As a leading company in silicon carbide power devices, Rohm has been developing the world's most advanced devices and providing power solutions together with peripheral components."

The development of power modules in the new company will encourage the use of SiC power devices in new energy vehicles, which are gaining momentum in China, as well as play an important role in other application research.

IQE announces GaN partnership with GlobalFoundries

IQE PLC, the compound semiconductor wafer company, has started a long-term strategic collaboration with GlobalFoundries to develop vital GaN-on-silicon technologies for mobile and wireless infrastructure applications.

The result of this collaboration will be a GaN-on-silicon offering at GF's Fab 9 facility in Burlington, Vermont, using wafers supplied by IQE.

Working together, GF and IQE will pool their expertise and facilitate the development of crucial building blocks for current and future communications systems.

"IQE's collaboration with GlobalFoundries marks a step change for us. It recognises the quality of our market-leading GaN products and demonstrates how IQE's ever-closer customer relationships can bring more innovative products to market, at scale," said Wayne Johnson executive VP of Wireless & Emerging Products at IQE. "This is a unique opportunity to leverage the performance of GaN with the cost structure of high-volume silicon manufacturing. We look forward to working closely with GlobalFoundries over the coming years."

Bami Bastani, SVP and general manager, of Mobile and Wireless Infrastructure at GlobalFoundries said: "GlobalFoundries continues to lead with innovative and feature-rich solutions for 5G. Our collaboration with IQE will enable us to deliver differentiated gallium-nitride-on-silicon solutions that enable next-generation connectivity and user experiences that will help enable our customers' innovations."

US Army grant will help build Arkansas SiC facility

MORE THAN \$5 million in total funding from the US Army Research Office and the Army Research Laboratory will go toward a unique SiC fabrication facility at the University of Arkansas.

The grants – \$4.5 million from the Army Research Office and \$900,000 from the Army Research Laboratory – come on the heels of an \$18 million grant from the National Science Foundation to fund construction and operation of the unique national fabrication facility.

Alan Mantooh, distinguished professor of electrical engineering, is principal investigator for both grants.

The Army Research Office grant will be used for equipment, and the Army Research Laboratory grant for student and staff compensation, tuition and materials for supporting collaborative research activities with the Army Research Lab.

Combining cutting-edge equipment and infrastructure with a core of research experts focused on SiC semiconductor devices, sensors and integrated circuits, the fabrication facility will develop new electronics to address areas of national defence.

The facility will also train the next generation of semiconductor researchers and engineers who can work in both the silicon and SiC semiconductor industries. Students at all degree levels will be given research opportunities and be exposed to a high-need area of science and technology. The research will engage under-represented students in this new and burgeoning area of electronics.

With now decades of experience working with SiC, Mantooh will lead a team that will acquire, install and integrate cutting-edge equipment for the purpose of building a low-volume prototyping facility to produce SiC integrated circuits.

In addition to Mantooh (pictured far right), researchers on this project include

(left to right) Zhong Chen, associate professor of electrical engineering; Greg Salamo, distinguished professor of physics; and Shannon Davis, business and operations manager in the Department of Electrical Engineering.



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Feel-good factor flowed through Compound Semiconductor International 2021

THE MANY DELEGATES attending this year's Compound Semiconductor (CS) International, held at the Sheraton Hotel at Brussels Airport on the 9th and 10th on November 2021, delighted in the in-person format.

Attendee numbers were incredibly healthy – despite Covid-19 hampering travel from China, Japan and South Korea – with many enjoying face-to-face meetings within the compound semiconductor community for the first time since the start of the pandemic.

Those at the conference were able to hear 30 talks, divided into five key themes: satisfying demand for more data; seeking new opportunities for LEDs and lasers; taking wide bandgap devices to their ultimate limits; ramping volumes in the power electronic sector; and enhancing the automobile.



Delegates could also drop in on presentations at Photonic Integrated Circuits (PIC) International and Sensors Solutions International (SSI), and talk to company representatives at an exhibition housing over 70 exhibitors.

As well as the feel-good factor that came from attending this vibrant event, delegates at CS International were buoyed by the positive outlook for this industry. According to a handful of presentations provided by analysts from Yole Développement, all the key sectors within this industry are set to enjoy growth over the coming years.

Helping to fuel this are many opportunities for sales of GaAs-based and GaN-based transistors for

communication infrastructure, argued Claire Troadec, Power & Wireless Division Director at Yole. Troadec pointed out that GaAs devices are viable contenders for the switch, the low-noise amplifier and the gain block (PA). She added that in the final-stage PA, the battle is raging between LDMOS and GaN, but GaN will emerge as the winner in the longer-term. Looking ahead, she expects GaAs to prevail in backhaul, while GaN will enjoy success in sub-6 GHz 5G. This will help to swell annual sales for GaN RF devices, which are tipped to climb from almost \$1 billion today to nearly \$2.5 billion by 2026.

Troadec also offered some insight into the smartphone market, where GaAs dominates amplification. She described the RF front-end as the biggest opportunity for RF components, with the wide bandwidth for amplification requiring the use of several PAs. The introduction of 5G has increased GaAs content in the phone, with the latest communication standard leading to more than 4 mm² of GaAs in an entry level phone, and more than 6 mm² in a luxury variant.

Within the power electronics sector silicon still dominates, but wide-bandgap devices are tipped for a rapid growth in sales over the coming years. SiC devices are forecast to generate the greatest revenue, spurred on in part by the expansion in production capacity at the likes of Wolfspeed and STMicroelectronics. However, sales for GaN should also grow at a healthy rate, as this class of device expands from serving in fast chargers for smartphones to deployment in other applications, including automobiles.

Championing the capabilities of GaN, Philip Zuk, Senior Vice-President of Technical Marketing and Business Development at Transphorm, made a strong case for the use of this device at various voltages, including some considered to be the domain of SiC.

During Zuk's talk, he compared the performance of a SiC FET, SiC MOSFET and Transphorm's SuperGaN. When

evaluating these three in turn, in a 12 kW application, the SuperGaN is found to run more efficient and cooler than both forms of SiC. Adopting an upper limit on the device temperature of 165 °C, the maximum power when using the SiC FET and SiC MOSFET is restricted to 9.2 kW and 11 kW, respectively. With the GaN FET, the junction temperature is just 139 °C at maximum power, leading to a power loss of only 102 W. In comparison, the use of SiC FETs and SiC MOSFET incurred losses of 164 W and 130 W, respectively.

Another exciting opportunity for compound semiconductor devices is in the display industry, where microLEDs could be used to provide direct emission, leading to higher efficiencies and contrast ratios. Samsung showcased the first commercial luxury microLED TV earlier this year, but prices must tumble if this technology is to be used for mass deployment.

Yole's Business Unit Manager for Solid-State Lighting and Display, Pars Mukish, offered some options for doing this, telling delegates that the biggest opportunity for slashing costs is to shrink the size of the LED. Mukish estimated cost reductions ranging from a factor of 4 to 70 by diminishing die size. According to him, a very significant impact could also come from improving yield and repair, and from streamlining transfer and assembly: these two options could lead to cost reductions of up to 50 times and 120 times, respectively. Further gains could come from an increase in manufacturing efficiency, which could halve costs.

If fabs are to make tiny microLEDs in high volumes with a high yield, they will need to invest in new equipment. Fortunately, many companies are offering tools that will help in this endeavour.

Given the strong demand for face-to-face interaction, delegates will be pleased to note that they will not have to wait a whole year for the next CS International. The next instalment, which will be the 11th CS International, will be held in June 2022 at the Sheraton Hotel, Brussels Airport.

GaN Systems raises \$150 million

GaN SYSTEMS, based in Canada, has announced a \$150 million growth capital funding round to accelerate innovation and adoption of GaN technology across its automotive, consumer, industrial, and enterprise markets. Fidelity, celebrating 75 years since its founding with US \$4.2 trillion in assets under administration, led the fundraising round.

Fidelity is joined by investors including Vitesco Technologies, an international developer and manufacturer of state-of-the-art powertrain technologies for sustainable mobility. Existing investor BMW i Ventures joins Fidelity, Vitesco Technologies, and existing investors in the financing.

GaN Systems will use the investment to fuel the rapid market penetration of GaN as global power electronics companies shift from legacy silicon devices to unlock the value of small, low-cost, efficient power systems.

Dell, Samsung, Harman, Siemens, Signify, and Philips are amongst the companies using GaN Systems' transistors.

Vitesco Technologies is the lead strategic partner in the round and has announced a broad strategic partnership with GaN Systems to enable GaN solutions across the EV platform.



The strategic partnership comes on the heels of GaN Systems' recent announcement of a capacity agreement with BMW.

"We share a successful track record in power electronics. By combining our automotive know-how with our partner's GaN expertise, we will be able to reap the benefits of comprehensive wide-bandgap technology in the car," said Thomas Stierle, member of the executive board and head of Vitesco Technologies' Electrification Technology business unit. "We are enthusiastic about our strategic partnership with GaN Systems to accelerate GaN adoption across our electrification solutions."

Jim Witham, CEO of GaN Systems, said: "This transaction is a game-changer and comes at a perfect time. The demand for higher performing, more efficient power electronics is growing exponentially, and traditional silicon solutions cannot keep up. Gallium nitride takes the baton from legacy silicon to enable smaller platforms to run cooler and use fewer materials. We stand apart from the competition as the only GaN power transistor company currently shipping to automotive, consumer, industrial, and data center customers. Our relationships with industry leaders and our \$8 billion pipeline tell us that the gallium nitride inflection is here, and the time is now to accelerate investment in the business."

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Navitas and Anker partner on next-gen mobile fast chargers

GaN CHIP MAKER Navitas Semiconductor and fast-charging firm Anker Innovations have signed a new strategic partnership. The agreement dedicates engineering teams from both companies to be co-located at Anker offices to develop and launch leading-edge GaNFast chargers to accelerate time-to-market.

The initial focus will be on next-generation mobile chargers but will expand into the high-growth energy-storage markets. The deal also provides a longer planning horizon for co-operative marketing across all media platforms and in-person events, such as the Consumer Electronics Show (CES), in Las Vegas.

Anker and Navitas have an established relationship, starting in 2017 when Anker was one of the first companies to create next-generation, fast-charger prototypes and then qualify the breakthrough new GaN technology. The 2019 Anker PowerCore Fusion PD combination charger and portable power bank was a game-changing shift in mobile power, using Navitas GaNFast power ICs to reach new levels of efficiency and power density.

Steven Yang, CEO of Anker Innovations said: "I believe that having engineering



teams from Anker and Navitas sitting side by side on a daily basis will greatly improve the efficiency of the product development process, translating into faster and better chargers for our customers."

"As both a long-term customer and investor in Navitas, Anker has demonstrated a passion for innovation and vision for the future of charging," said Gene Sheridan, co-founder and CEO of Navitas. "Mobile charging is a \$2 billion target market for GaN power ICs, and working with Anker on energy-storage is aligned with our renewable / solar energy expansion strategy."

The first two fast chargers released under the new partnership are the 30 W

USB-C and 65 W 2C+A chargers in Anker's collaboration with the "League of Legends" multi-player online battle arena video game, played on phones, tablets and laptops. With fast action and intensive, detailed graphics, the game has a high draw on battery power, and fast charging – with portability – is crucial for any League of Legends gamer.

Measuring 28 x 29 x 32 mm, the 30 W USB-C 'Jinx' is a similar size to the original 5 W so-called 'sugar-cube' phone charger and 70 percent smaller than the standard silicon-based 30 W. The 65 W 2C1A 'Yasuo' charger, has 2x USB-C and 1x USB-A port to charge three devices simultaneously such as a phone, headphones and a laptop – with enough power for high-performance gaming laptops.

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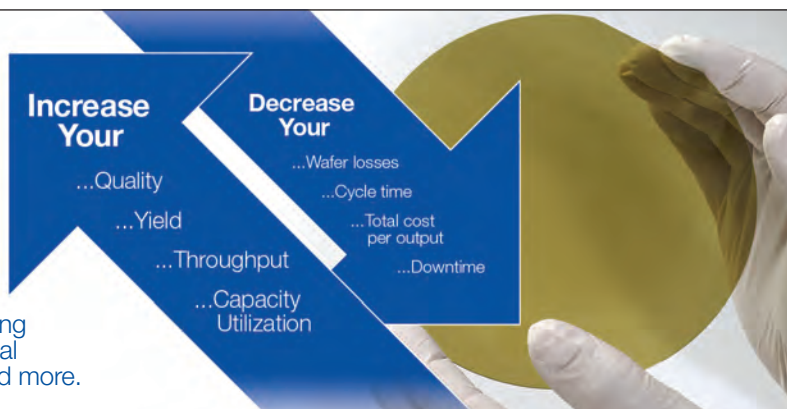
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Korean GaN epiwafer startup raises \$17.4 million Series C funding

IVWORKS in South Korea, a GaN epitaxial wafer startup, has announced that it has successfully raised \$17.4 million Series C round funding.

This investment was subsequent to the \$6.7 million raised in the Series B round in December 2019. YG Investment, Korea Investment & Securities, Wonik Investment Partners, Log Investment Wooshin Venture Investment, Deslaube PEF and Hyundai Venture Investment, have invested a total of \$17.4 million in new and existing shares.

IVWorks has used the self-developed technology of a highly efficient and eco-friendly epitaxy system as well as AI-based production platform to produce 6-8 inch GaN-on-silicon epitaxial wafer products used in power devices and 4-6 inch GaN-SiC epitaxial wafer products used in RF devices. The funds were secured through new investments and are planned for use in the production

capacity expansion and AI-based production platform advancement. In particular, recent market circumstances (application of GaN fast charger in IT products of Apple, Samsung, Huawei, and the expansion of GaN power devices used in electric vehicle onboard chargers and power converters) have been reflected in this funding round, which demonstrates the company's interest in maintaining differentiated technological competencies and focusing on scaled growth in response to market demand.

Furthermore, to proceed with the KOSDAQ listing, IVWorks has entered into a contract with the Korea Investment & Securities listing underwriter. The company announced that it has commenced operation of a full-fledged initial public offering.

CEO Young-Kyun Noh of IVWorks said: "Raising investments concluded favourably owing to recognition of

the company's capacity and epitaxy technology, and expectations towards the GaN power device market has entered the growth phase amid global technological trends such as digital transformation and energy paradigm shift". He added that additional collaborations with global semiconductor companies and strategic investments are in progress.



Sino-American Silicon Products invests in Transphorm

TRANSPHORM, a supplier of high-reliability GaN power products, and Sino-American Silicon Products, a Taiwanese green energy provider (and parent company to silicon wafer company GlobalWafers), are starting a strategic partnership to expand the companies' supply chain in the fast-growing GaN market. SAS and GWC have a combined market capitalisation of more than \$16 billion.

In addition, SAS has made a \$15 million equity investment into Transphorm, which includes its initial \$5 million investment in Transphorm in August. The investment was through a private placement of Transphorm's common stock at \$5.00 per share.

Through the new strategic partnership, Transphorm plans to significantly enhance the supply chain for GaN epiwafers. The deal includes GWC becoming Transphorm's manufacturing partner and supplier, captive for Transphorm's GaN epiwafers, a move

that will augment Transphorm's internal capacity. Additionally, SAS will become a distributor for select Transphorm epiwafer products as well as power products, that will boost the growth of Transphorm's GaN product sales.

Commenting on the announcement, Doris Hsu, Chairwoman and CEO, SAS/GWC said: "We are excited to become shareholders of Transphorm as we begin our new GaN strategic partnership. Transphorm is a proven GaN power and epi products leader with vertically integrated manufacturing and one of the strongest GaN power IP portfolios in the world. Our strategic partnership will enable Transphorm to scale at a faster pace."

"The GaN power and RF markets represent a multi-billion-dollar opportunity with fast growing segments including fast chargers and adapters, server-storage-networking power, renewable energy and industrial power, electric vehicles as well

as RF GaN electronic devices for 5G and a variety of communication/infrastructure applications."

Primit Parikh, co-founder and president of Transphorm, commented: "Transphorm is thrilled to partner with SAS/GWC, a recognized global leader in green energy and wafer manufacturing. This partnership will allow for our rapid expansion in the GaN market, with a multi-year growth plan to scale GaN epi-wafer manufacturing for Transphorm, while protecting our intellectual property.

"It will provide Transphorm's customers – from compact high-speed fast chargers to efficient higher power electric vehicles – the security of supply, multiple locations (including our core US manufacturing), and rapid expansion capability. SAS' investment in Transphorm is a testament to our leading position in the fast-growing GaN market and brings the total of new equity capital raised recently by Transphorm to \$33 million."



The bright future of laser diodes

The last few decades have seen the laser diode market grow from a multi-million dollar to a multi-billion dollar market, but Yole Développement reckons there's much more potential for growth, reports **REBECCA POOL**

➤ Above: This year, OSRAM unveiled a chip design for edge-emitting lasers that improves the wavelength stability at operating temperatures of up to 125 °C, typical for automotive applications, including LiDAR technology. [ams Osram]

THE MARKET FOR LASER DIODES is set to more than double and surpass \$9 billion by 2026, forecasts Yole Développement in its recent webcast, *From legacy technology to innovation, the laser diode market is exploding*. As part of the impressive growth, Martin Vallo, technology and market analyst for lighting at the France-based analysis firm, highlights how optical communications and 3D sensing applications will dominate market growth for many years to come.

Since the datacom and telecom boom of the 1990s, more and more devices have been used in materials processing applications. And in the last ten years, laser diode revenues have been largely driven by sensing applications. However, thanks to the burgeoning optical communications and 3D sensing markets, as well as near-term growth from medical laser systems, the overall laser diode market is

expected to grow from \$4.1 billion to \$9.2 billion at a CAGR of 14.4 percent from 2020 to 2026.

Laser diodes are based on one of two semiconductor technologies, the edge-emitting laser or VCSEL, and the market for each is buoyant. According to Vallo, from 2020 to 2026, revenues for edge-emitting lasers will rise from \$2.9 billion to \$6.6 billion at a CAGR of 15 percent. At the same time, VCSEL revenues will increase from \$1.2 billion to \$2.6 billion, a CAGR of 14 percent.

Technology choice

When it comes to the choice of device technology, VCSELs tend to be cheaper than edge-emitting lasers, but are not suitable for all applications. For example, edge-emitting lasers will be used in higher-power applications where high density VCSEL arrays cannot be used for the same power output.

Each type of device will be fabricated on either GaAs or InP wafers. Both near-IR 850 nm VCSELs, as used in datacom applications, and 940 nm VCSELs, for 3D sensing, are fabricated on 6-inch GaAs wafers. Meanwhile short-wave IR 1500 nm VCSELs are typically based on 2- to 3-inch InP wafers. Similarly, edge-emitting lasers will be manufactured on GaAs wafers for lower-wavelength applications, but at 1300 nm and higher wavelengths, will be based on InP. Without a doubt, optical communications is still fuelling edge-emitting laser market revenues, with revenues from this market sector alone expected to rise from \$1.7 billion to \$4.7 billion from 2020 to 2026, a CAGR of 18 percent. Along the way, sensing and medical applications will also contribute to significant market growth.

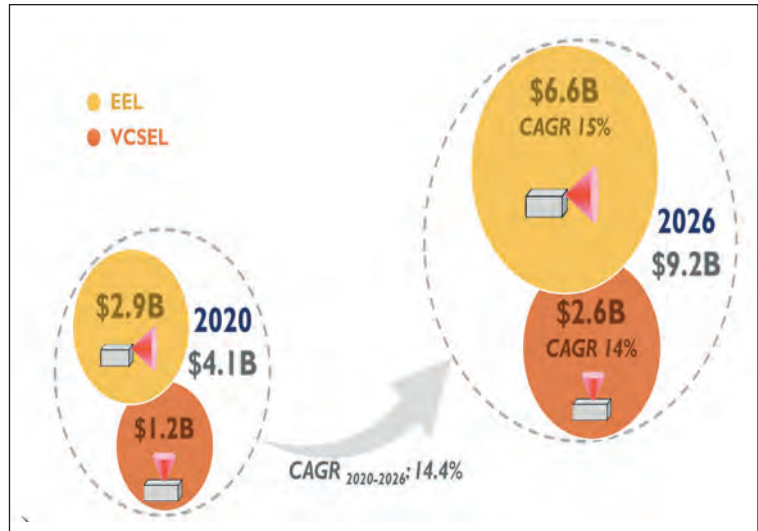
Meanwhile, for VCSELs, 3D sensing in mobile phones and other consumer devices will dominate growth with this market expanding from \$797 million to \$1.9 billion from 2020 to 2026, delivering a 16.9 percent CAGR. However, VCSELs are also making in-roads to automotive 3D sensor applications, such as LiDAR and in-cabin monitoring systems, with this small market set to grow by a massive 121.9 percent CAGR from \$1.1 million in 2020 to \$57 million come 2026. And along the way, the telecom and infrastructure market will remain important for VCSELs, with Yole predicting 5.6 percent CAGR growth from \$430 million to \$566 million.

Growth drivers

But what is responsible for the laser diode's rosy future? As Vallo points out, optical communications growth is being driven by data-centric applications such as Cloud services from the likes of Apple and Facebook, higher definition 4k and 8k video streaming from companies such as Netflix, Disney+, as well as rising industrial automation traffic.

As cloud operators race to connect more and more data centres to keep pace with the huge increase in global IP traffic, the migration to higher-speed optical communications, from 400 G and beyond, continues. This is seeing manufacturing volumes of both edge-emitting lasers and VCSELs, now on a steady ramp up, spelling good news for both II-VI and Lumentum from the US, which dominate the laser diode market. Optical communications aside, 3D sensing offers huge promise for VCSELs, and also edge-emitting lasers. As Vallo highlights: "Smartphones and tablets dominate in the 3D sensing market today... with the mobile market being by far the main market for VCSELs."

"While VCSEL-based proximity sensors are now widely used by OEMs, Apple is almost the only player that is implementing 3D sensing modules in its smartphones in 2021," he adds. "Apple is expected to continue using such modules and push for new applications using augmented reality... if consumers accept this use-case, we expect other players may implement such modules in the future."



Beyond consumer and mobile applications, automotive manufacturers are incorporating more and more sensors to vehicles. Vallo points out how BMW has been using VCSELs in its gesture recognition systems, and now expects that future driver monitoring systems, which require high-precision sensing, will be based on VCSELs.

However, the analyst also anticipates automotive LiDAR to be a key market for laser diodes, particularly VCSELs. Both edge-emitting lasers and VCSELs have already been integrated to long- and mid-range LiDAR modules for safety and automated-driving systems. And VCSELs have also been used in short-range LiDAR for automated driving.

Come 2025 to 2026, Vallo forecasts that automotive LiDAR applications will take a big leap forward as the use of multiple-junction VCSELs – that provide a high output power in a compact footprint – rises. Indeed, both Lumentum and II-VI recently released multi-junction devices.

As Vallo emphasises: "This type of VCSEL architecture will be key for [LiDAR] applications in the automotive industry."

► Sales of edge-emitting lasers (EELs) and VCSELs are forecast to grow at similar rates, according to Yole.

► iPhone 13: the TrueDepth camera system in Apple smartphones uses VCSELs for 3D sensing face ID. [Apple]





Enkris: Breaking 300 mm barriers

Enkris has demonstrated 300 mm GaN-on-silicon epiwafers for HEMTs – here’s how the China epi-foundry super-sized its epitaxy processes, reports **REBECCA POOL**

IN SEPTEMBER THIS YEAR, Enkris Semiconductor claimed a breakthrough when it demonstrated high-quality 300 mm GaN-on-silicon HEMT epiwafers for 200 V, 650 V and 1200 V power applications. In response to industry demand, the China-based pure epi-foundry transferred its 200 mm AlGaIn/GaN HEMT epitaxy process to 300 mm silicon substrates, a feat that company chief executive, Kai Cheng, says was a collective effort of both hardware modification and process control.

Enkris had developed its 200 mm process back in 2014. But as Cheng points out: “We decided to move to 300 millimetre following market requests. Thanks to continuous research and development over the years, we transferred our technology to the larger wafer size after we had optimized parts of the process, such as deposition and metrology tools.”

At the heart of Enkris’ structures lies a high-crystalline-quality AlN-based nucleation layer onto which aluminium-containing buffer layers are grown to

relieve the lattice and thermal expansion mismatches between the silicon substrate and active GaN layers. Thanks to the AlN nucleation layer, Enkris managed to fabricate 300 mm GaN-on-silicon HEMTs with relatively thin buffer layers that meet leakage current requirements whilst keeping overall device costs down.

According to Enkris, the buffer layers in its latest epiwafers are only 2-6 μm -thick, have uniform composition across the entire wafer and deliver consistent electrical properties. Company figures indicate wafer bow remains within an acceptable 50 μm while leakage current comes in at 1 $\mu\text{A mm}^{-2}$ at room temperature.

As Cheng points out: “Thanks to our aluminium nitride nucleation layer, we have a pretty large process window to manage the stress in thick buffer layers and keep the wafer bow acceptable for the 300 millimetre fab. In addition, the high-quality aluminium nitride also means that defects, such as V-pits and melt-back



► Kai Cheng,
Enkris CEO

etching defects at the nitride/silicon interface, are minimized,” he adds. “Thus, the leakage current in the vertical direction can be significantly reduced and meet the requirements for high-voltage applications on large-size silicon substrates up to 300 millimetre.”

Cheng emphasizes that despite the industry-wide challenges associated with epitaxy, strain management and defect control when moving to 300 mm wafer size, his company has achieved excellent structural quality and electrical properties in its AlGaIn/GaN HEMT structures. “This will certainly encourage the development of high-power integrated circuits... [and] reduce the cost of gallium nitride power devices,” he says.

But what about yield figures? It’s no secret that poor yields have held back many industry players, keen to work with larger wafers sizes and reap the cost benefits this transition brings.

Cheng is optimistic about yields at 300 mm wafer sizes, but says: “It’s still too early to talk about the yields of our twelve-inch wafers in terms of substrates and epitaxy at this moment.”

Still, as he adds: “We haven’t seen any real difficult hurdles of physics yet, but the final yield improvement is dependent on the whole industry’s efforts, including metrology tool vendors, processing tool vendors, growers and device makers.”

Back in 2014, Enkris also worked closely with Aixtron on its high-voltage GaN HEMT structures on 200 mm

silicon, using a high-throughput Crius II Close Coupled Showerhead Reactor. This time around, such system details are not disclosed, but Cheng is certain that devices fabricated from Enkris’ 300 mm GaN-on-silicon epiwafers will be cost-competitive. “The gallium nitride-on-silicon wafer costs are generally higher than silicon materials, but gallium nitride materials have very unique properties,” he says. “And if we look at silicon power devices, more than three times more gallium nitride devices can be produced from the same wafer size, making the gallium nitride device costs comparable or even lower than its silicon competitors.”

So where next for Enkris Semiconductor? Right now, the pure-play epi-foundry is shipping its large size GaN-on-silicon HEMT epiwafers around the world – Cheng says his company is seeing interest from China, the rest of Asia, the US and Europe.

He also points out how vertical breakdown measurements indicate the structures can operate at 200 V, 650 V and 1200 V voltage ranges for a wide range of power applications, such as consumer electronics and data-centre applications.

And while Enkris also develops GaN-on-SiC, GaN-on-sapphire and GaN-on-GaN epiwafers, GaN-on-silicon wafers are currently in the greatest demand, being required for RF, power and microLED display applications. “We are growing various interesting structures, but we do pay close attention to customer needs,” he says. “As a commercial company, we are creating world-class products for industry.”

Driving tomorrow’s technologies

Compound semiconductors provide the key enabling technologies behind many new and emerging applications. CSconnected represents the world’s first compound semiconductor community based in and around South Wales in the UK

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Ensuring repeatable, reliable processing of InP photonics

Advances in the processing of InP lasers and detectors will aid the growth of a third wave of connected devices, following in the footsteps of the computer and smartphone revolutions

BY GRANT BALDWIN AND MARK DINEEN
FROM OXFORD INSTRUMENTS PLASMA
TECHNOLOGY

JUST BEFORE the dawn of the 21st century, when many feared a digital Armageddon from the Millennium Bug, a new expression entered our vocabulary: the smartphone. Back then, owners of mobile phones were benefitting from incremental advances in capability that started in the 1980s, giving them a device that no longer performed a narrow function, but provided voice and text communication – and possibly some very basic gaming. However, at that time few, if any, would have anticipated the revolutionary advances in the smartphone over the next two decades, propelling it to the generation-defining connected device that changed forever how we exist and interact.

The latest generations of smartphones make it easier for us to perform known functions, while offering limitless and inconceivable functionality. Now we can

pay, play, consume, create, share, locate, navigate, communicate and monitor our internal and external environment – at one stage all these functions were unimagined and unimaginable.

For good reason, some believe that the dawn is breaking for another consumer device to deliver a similar explosion in capability and bring an equally epochal change. Up until now automobiles have only really got better and more efficient at performing a narrow, but important function of transporting us from A to B. We are now on the cusp of a profound change, with the automobiles of the not-too-distant future providing a data centre and infotainment hub on wheels that takes you to places. With the inexorable progression toward vehicles that drive themselves and entertain us along the way, due to this additional functionality, the hourly data generated by the automobile is projected to grow exponentially.

According to Statista, today a moving 'connected' car produces 25 GB of data per hour. Storage system developer Tuxera forecast that this will mushroom to between 1 TB and 19 TB per hour for self-driving vehicles. 5G and the 'cloud' will be critical to processing and storing this deluge of data, says market analyst Gartner.

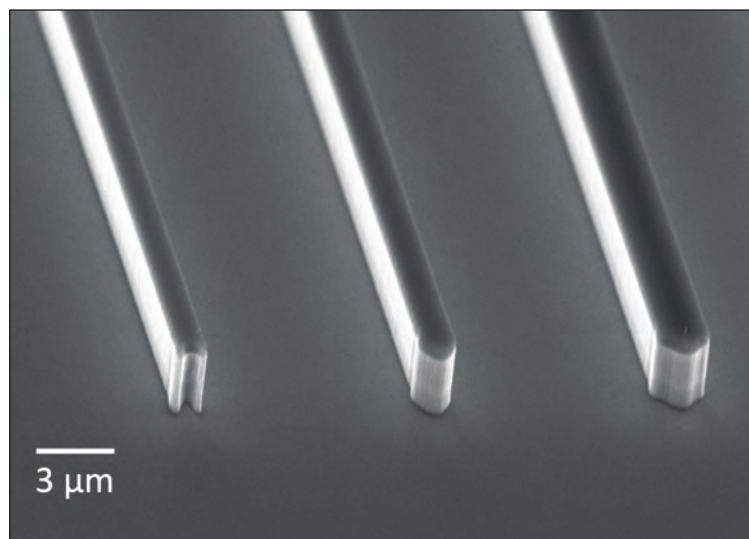
But what is the critical enabling technology for 5G and the cloud? Fortunately, fibre-optic networks based on high-performance InP devices are on hand to enable this next wave of connected consumer device. However, given the drastic rise in data being produced, there is a need for considerable investment in infrastructure to move, process and store this new data.

Increasing network capacity is not trivial. For example, there are several challenges associated with reliable, repeatable high-volume production of the high performance InP devices, that play a critical role in the network.

At Oxford Instruments Plasma Technology we are helping engineers to take on these challenges by sharing our extensive process knowledge, while providing cutting-edge systems to chipmakers. These solutions are playing a crucial role in enabling InP to be the catalyst for change.

InP and optical, a perfect match?

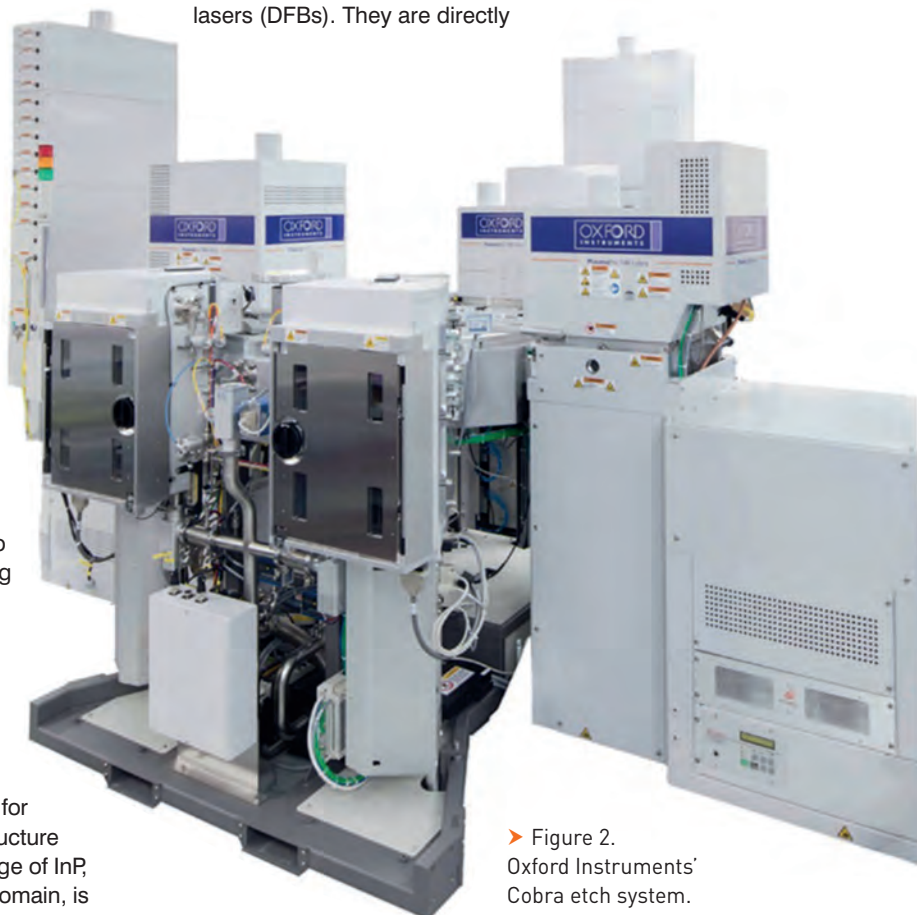
The InP-based photonic-integrated circuits deployed in big data centre transceivers and 5G networks are ideal for supporting the required network infrastructure transformation. The natural spectral range of InP, which spans the 1300 nm to 1650 nm domain, is a perfect match for the low-absorption windows of



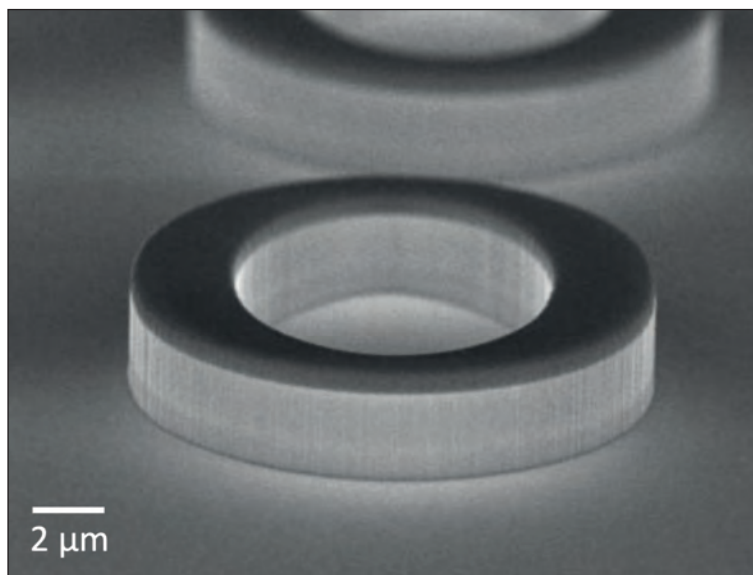
➤ Figure 1. InP structures.

fibre-optic communication. However, to ensure more cost-effective, higher-yield, higher-performance devices, chipmakers must employ robust, innovative InP plasma-processing solutions. Taking this approach will support a scaling-up of manufacturing and help to deliver the desired network transformation.

At the heart of every optical network are a number of transceivers, formed from InP lasers and diodes. The majority of these high-volume optical devices incorporate InP distributed-feedback lasers (DFBs). They are directly



➤ Figure 2. Oxford Instruments' Cobra etch system.



► Figure 3. Ultra-clean structure processed on Cobra etch system.

modulated, and provide a narrow line width and a high spectral purity. However, due to growing demand for 400 Gbit/s big data centre transceivers, and 25 Gbit/s fronthaul 5G transceivers, industry is rapidly shifting towards external modulation of the laser as this increases transmission bit rates while ensuring much lower chirp. These advances are happening through an increase in the deployment of 1300 nm sources that pair a DFB laser with an electro-absorption modulator, alongside far higher shipments of 1550 nm components that combine a tuneable laser with a Mach-Zehnder modulator.

To ensure the desired electronic performance, these devices are manufactured using complex multi-step epitaxial deposition, masking and plasma-etch processes. Plasma etch is also employed to create the physical geometric structures – that is, the gratings and waveguides – that modulate and control laser emission. To help engineers master these steps, we offer a market-leading range of InP process solutions, from slow etch for fine features, such as gratings, to solutions for etching ultra-smooth structures (see Figure 1).

Perfecting the processing

Gratings are created by patterning the InP epiwafer with either a photoresist or a silicon dioxide/nitride

To minimise losses due to broken wafers, we provide a robotic wafer-handling system that is supremely capable of processing high-value InP substrates. This system is adept at transferring the delicate substrates from cassette to chamber and back, and provides some of the lowest loss rates in industry.

‘hard’ mask, prior to plasma etching. The depth and geometry of the finished structures dictates performance characteristics, such as the coupling coefficient, side-mode suppression ratio and the threshold current.

We recommend our Cobra etch system for forming the high-precision gratings in InP. Using a mixture of CH_4 and H_2 , etch rates of 10-40 nm/min are achievable, to form high-quality structures with depths up to 100 nm. With this approach, the two-dimensional mask pattern is accurately transferred through to the InP substrate. Etching creates three-dimensional structures, because the process demonstrates high preference toward removing unmasked InP material while retaining the mask – this is a condition known as high selectivity. With the etch complete, the mask is plasma-stripped to reveal the finished high-precision gratings. In contrast to hot InP plasma etching, we recommend ambient process temperatures, to prevent the photoresist mask from being rapidly consumed mid-process. If this were to happen, it would change the shape of the finished structures and ultimately compromise device performance.

When producing devices that deliver maximum power-to-light conversion relative to light scattering, absorption and noise, there is a need to not only optimise the depth and geometry, but to also realise straight (sloped or vertical), clean and smooth sidewalls. When seeking to achieve higher performance and a deeper etch, there are limits to what can be accomplished with the CH_4/H_2 chemistry used in the lower-cost ambient temperature process. Essentially, forming structures in the process chamber involves removing exposed InP material with an etch, while simultaneously protecting the newly formed sidewall under the mask by means of passivation. A CH_4/H_2 etch/passivation chemistry creates a polymer-type sidewall passivation, and while this option has many benefits, it is not the optimum choice for ultra-clean smooth sidewalls.

To overcome this issue, we have developed advanced hot InP plasma processing capability. This technique requires the use of a ‘hard’ mask, because it withstands process temperatures in excess of 150 °C, a regime where photoresist masks will not survive. By using silicon dioxide/nitride hard masks, we open up the process window and allow the introduction of alternative etch chemistries, such as chlorine/argon.

There is great benefit in using chlorine as the etch component. It reacts readily with InP, because chlorine plasma reacts with InP to create InCl_x . As InCl_x has a low volatility at ambient temperature, deposition occurs rather than etching, which is undesirable. However, if the process is too hot and the volatility too high, the etch will undercut the mask and compromise the accuracy of the structure.

The key to running at higher temperatures with hard masks is to tune the process temperature to the sweet

spot where InCl_x has sufficient volatility. Once this is achieved, chlorine provides an excellent option as the etch gas. By adopting a non-polymer chlorine/argon process, this approach creates ultra-clean structures (see Figure 3), and highly repeatable results. What's more, by eradicating polymers from the chamber, there is an increase in the mean-time between cleans and a dramatic reduction to machine downtime.

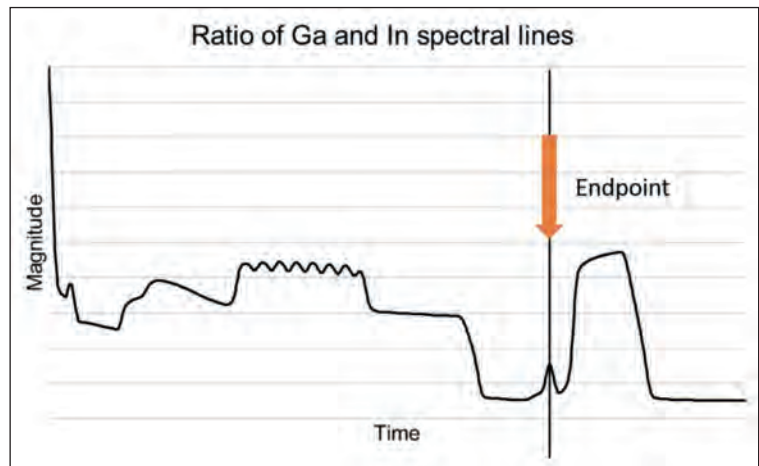
Controlling the outcomes

To optimise feature sidewall angle and smoothness, process engineers must carefully balance several process parameters, including the gas ratio, run pressure and plasma power. The equipment must also deliver excellent wafer-stage temperature uniformity, as this is critical to maintaining an even cross-wafer volatility threshold. Process engineering is not the dominant driver for controlling sidewall angle and smoothness, because the final outcome is influenced significantly by the mask angle and quality. Consequently, it is critical to use a highly accurate mask opening process.

For patterning of hard mask onto InP, engineers tend to use a similar process to that described already, to create structures in InP. However, a noteworthy distinction is that for this particular task, the oxide or nitride is etched, to then expose the underlying InP for chlorine/argon etching. To fully optimise this process flow for volume production, our etch systems are clustered around a single robotic handler. By combining several tools, we equip process engineers with the capability to perform a smooth-profile high accuracy 60-90° mask opening process, before undertaking a hot InP process that creates ultra-clean smooth structures. Crucially, all these tasks take place under the same vacuum, which limits issues such as contamination and therefore increases repeatability.

As well as controlling dimensions and characteristics of the finished structure, there are two more factors that device manufacturers must consider: wafer-to-wafer repeatability and substrate transfer reliability. With our processing systems these requirements are met. According to reports provided by our sizable customer base – we have systems installed in seven of the top ten optoelectronics device manufacturers – once the process is dialled in, wafer-to-wafer repeatability is excellent; and if the incoming mask remains regular and defect-free, finished InP structures are highly accurate and repeatable. While InP is resilient to high temperatures, low pressures and high plasma powers, anyone who has ever handled these wafers will know that they are incredibly brittle. To minimise losses due to broken wafers, we provide a robotic wafer-handling system that is supremely capable of processing high-value InP substrates. This system is adept at transferring the delicate substrates from cassette to chamber and back, and provides some of the lowest loss rates in industry.

A final consideration when using a plasma etch to create structures in InP is when to stop the process.



With depth being so critical to device performance, getting this just right is paramount. To ensure this is the case, our Cobra etcher can be fully integrated with endpoint detection and automated process stop capability. Using optical emission spectroscopy, this system can capture and analyse the wavelengths of light emitted by the volatile compounds released during etching. With this insight, it is possible to evaluate structure-depth part way through the process and accurately stop on layers as thin as 10 nm. Post-etch metrology on a 3-inch InP wafer reveals cross-wafer depth uniformity of just ± 3 percent (see Figure 4, which shows the endpoint at which the process was automatically stopped).

► Figure 4. Oxford Instruments OES automatic process stop capability.

Compound interest?

The breath-taking revolution in handsets over the last few decades has set a compelling precedent for vehicle integrated technology. Automobiles are blessed with fewer limitations associated with form factor and power management, so the functionality potential is astonishing. Fast-forward a few years and drivers could enjoy the likes of: gesture recognition, thanks to GaAs VCSELs; electric-vehicle fast-charge and power management provided by GaN power transistors; and, of course, data transmission, underpinned by InP-based transceivers. These are just a few examples of a connected vehicle ecosystem packed with compound semiconductor technology.

At Oxford Instruments Plasma Technology, we have been at the forefront of compound research and production for decades, and are already offering a full range of volume and niche solutions that are critical to enabling the vehicle integrated-technology revolution.

FURTHER READING

- Chart: Big Data on Wheels | Statista
- Autonomous cars generate more than 300 TB of data per year (tuxera.com)
- Connected cars: How 5G and IoT will affect the auto industry | ZDNet

Laying the foundations for manufacturing microLED displays

Makers of deposition and metrology tools are well prepared to support the launch of high-volume microLED manufacture

BY RICHARD STEVENSON

THE GaN LED is our biggest success story. Launched to market in the 1990s, to date it has enjoyed three 'killer' applications: it rose to fame backlighting the keypads and screens of early handsets; it had another rapid increase in revenue from backlighting TVs, tablets and laptops; and it now nets yet more billions by illuminating our homes, our streets and our offices.

Unfortunately, all of these triumphs have come at a cost. The growth of the market has drawn in many new players, driving down margins and commoditising the device. Now there is little interest left in the traditional LED and companies in this sector are looking for new, more profitable opportunities.

Amongst them, the microLED offers tremendous promise. It can raise the bar for the performance of the display, combining an exceptional contrast ratio with far higher levels of efficiency. Such virtues are valued by the makers of smartwatches, augmented-reality

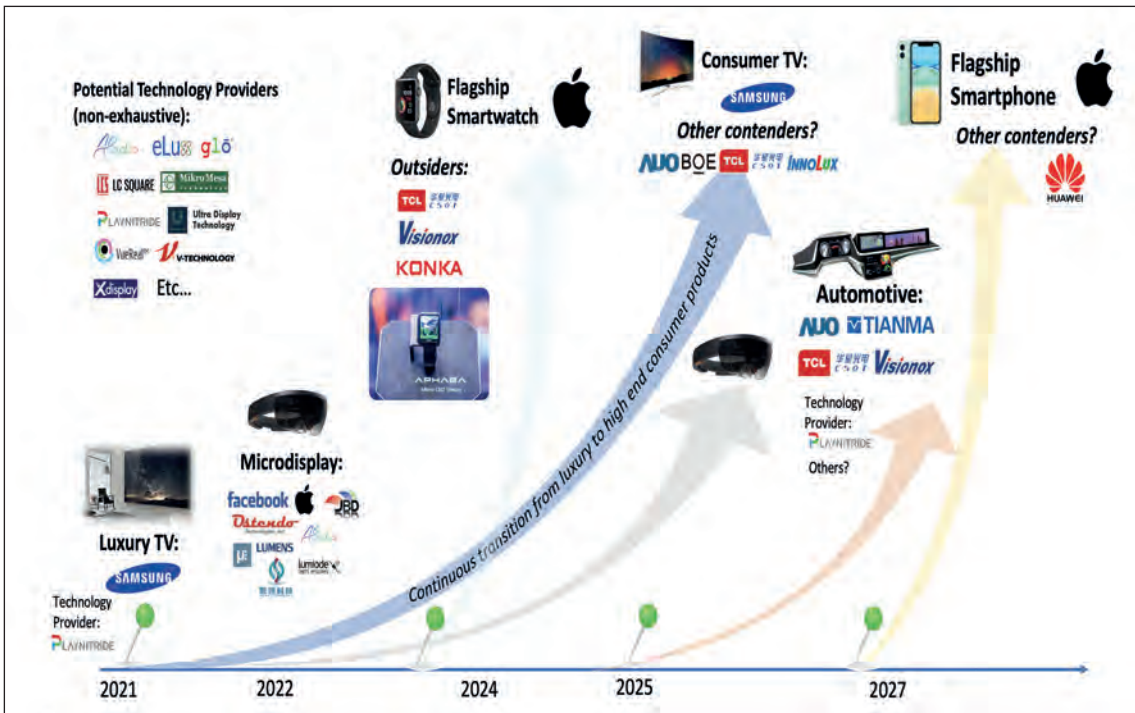
and virtual reality-headsets, TVs and outdoor displays. But what is needed to unlock this opportunity? Are there tools in place to support such a move? And are we now on the cusp of a revolution in displays?

Offering answers to all of these questions were a handful of speakers at this year's CS International, held on the 9th and 10th of November at the Sheraton Hotel, Brussels Airport. At this meeting Pars Mukish, Business Unit Manager for Solid-State Lighting and Display at Yole Développement, provided great insight into the state of play of the microLED industry and how it may unfold; and a number of makers of production equipment and metrology tools detailed how they are able to support this nascent industry.

If you don't have deep enough pockets to shell out \$150,000 and pre-order a 110-inch Samsung luxury TV you will argue that the commercialisation of microLEDs is still to take place. But in this very young, dynamic industry it will surely come, given the flurry of patent activity that kick-started in 2014 with the acquisition of LuxVue by Apple. Patent publishing has been climbing at breakneck speed – between 2016 and 2020, this occurred at a compound annual growth rate of 86 percent, according to Mukish. He revealed that display makers are leading the filings, followed by start-ups, with China dominating and South Korea ramping activity in 2020.

Realising cost-effective, high-volume manufacturing of microLED displays will not be easy. Much has been made of the difficulties associated with the mass transfer of millions and millions of red, green and blue LEDs to form the pixels of the displays. But that is by no means the only challenge. There is also the need to make progress on: the cost and the efficiency of the LED; light extraction and beam shaping; generating colours; increasing yield; managing and repairing defects; driver technologies; and establishing a strong supply chain.





► Yole Développement is forecasting that the growth in the microLED market will begin with luxury LEDs, before extending to smartwatches, followed consumer TVs, automotive displays and smartphones. Park Mukish presented this figure in his talk: *Can microLEDs and laser diodes revolutionise the solid-state lighting industry?* Copyright: Yole Développement.

The good news, according to Mukish, is that many potential solutions are being offered for each of these challenges. For example, techniques based on lasers for self-assembly could speed the transfer and assembly of microLEDs to a backplane; and the use of die-shaping techniques, quantum-dot patterning and photonic crystals may be promising pathways for improving the emission from the device.

A substantial reduction in costs is essential to make the microLED a contender for displays. For Samsung’s 146-inch screen that is known as ‘The Wall’ and showcased at CES 2018, the cost associated with the use of 125 µm by 225 µm miniLEDs equated to more than \$50,000 per square-metre. To take on a large OLED TV, this figure must plummet by a factor of more than 20, to below \$2,000 per square-metre.

By far the biggest opportunity for slashing costs by this magnitude is shrinking the size of the LED. Mukish estimated a cost reduction ranging from a factor of 4 to 70 by diminishing die size. He pointed out that a very significant impact could also come from improving yield and repair, and streamlining transfer and assembly: these two options could trim costs by up to 50 times and 120 times, respectively. Further gains could come from an increase in manufacturing efficiency, which could halve costs.

Mukish offered a route for progress in cutting the cost and size of the LED. There has already been a reduction in the size of miniLEDs on PCB used

in Samsung displays showcased at CES, with dimensions down to 35 µm by 60 µm. Alongside this scaling, Samsung introduced a shift in technology to a TFT backplane. This may be used for additional miniaturisation – Mukish speculated its use for 15 µm by 30 µm microLEDs – but to target consumer applications, he sees the need to migrate to die with a vertical architecture, having dimensions of initially 10 µm by 10 µm, followed by smaller sizes.

Upgrading traditional fabs will allow the microLED industry to get off the ground. This will enable the manufacture of microLEDs with dimensions of 10-20 µm that will be deployed in smartwatches, automotive displays and luxury TVs. But for consumer 4K and 8K TVs, which require microLEDs with dimensions no bigger than 10 µm and 5 µm, respectively, new manufacturing approaches could be needed to ensure device efficiency, sufficient yield and device transfer. And further refinements may have to follow for smartphones and augmented reality, requiring devices with dimensions below 3 µm and 2 µm, respectively.

To make displays with microLEDs on such length scales will require dedicated fabs, possibly featuring class 100 air quality, i-line steppers, and tools for ALD, lift-off and wafer-bonding. What’s more, there may be a need for a shift to a semiconductor fab mindset. This would include fab-wide defect and yield management, an increase in in-line metrology and the close monitoring of tools and process excursion.

➤ As the price of the microLED plummets through its miniaturisation, the cost of high-end TVs based on this technology will start to fall.



Mukish warned that progress could be hampered by a lack of standardization. It is risky for equipment makers to develop tools when the task they will be used for has not been defined. And without tools for mass production, it is difficult to set up a supply chain.

Despite this catch-22 scenario, Mukish is forecasting a bright future for displays based on the microLED. By the middle of this decade he expects to see flagship smartwatches on the market that have adopted this technology, and as 2030 approaches, luxury TVs based on microLEDs will fall in price, with this device also starting to appear in automobiles and top-of-the-range smartphones.

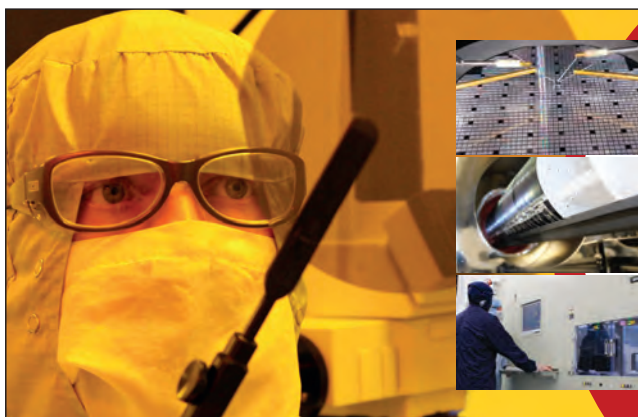
Better epi

Echoing the need for a reduction in the size of the microLED, Mark McKee, Director of Product Marketing at Veeco, argued that this must go hand-in-hand with a high yield and the use of large epiwafers – both are critical to reducing cost.

For the making of microLEDs, yield hinges on defect density and wavelength uniformity. For 150 mm and

200 mm substrates, McKee claimed that the defect density must be below 0.1 cm⁻². This equates to less than one defect from a transfer field – this is an area of around 15 mm by 15 mm that provides all the microLEDs of a particular colour for one display. According to McKee, for wavelength uniformity the spread across the transfer field must be below 1 nm, and less than 3 nm across the wafer. To meet such specifications, he advocates multi-wafer tools for the growth of arsenide-phosphide LEDs, and single-wafer tools for GaN growth.

Veeco's leading tool for the growth of arsenide-phosphide LEDs is the Lumina system, which can accommodate seven wafers with a 150 mm diameter. Results on wafers with a peak in photoluminescence at 630 nm show that within the transfer field there is a uniformity yield of around 95 percent. Another encouraging result is finding just three defects on a 150 mm GaAs-based microLED wafer. Results on Veeco's Propel tool for the high-volume growth of blue-emitting LEDs show that the variation in the photoluminescence peak across a 200 mm wafer is just 1.55 nm.



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Hunting for defects

When producing conventional LEDs for demanding applications, fabs can employ end-of-line electroluminescence probing for all devices. With microLEDs this is not an option, so an alternative approach is desired, given the need for minimising imperfections, due to the eye's sensitivity to any imperfection within a display.

At CS International, Matthew Davies, Head of Industry Applications at Attolight, championed the use of cathodoluminescence for exposing defects in epilayers. This technique, which involves scanning a sample with an electron beam and collecting and recording the emitted light, does not depend on optical absorption and can routinely realise a spot size below 10 nm.

Davies presented the results of a study on epiwafers analysed with the Attolight Sântis 300 platform. This tool is said to provide fully automated quantitative front-end cathodoluminescence metrology and a user-defined recipe interface. In addition, it offers automated data analysis and is capable of cassette-to-cassette handling.

In the study presented, Davies and co-workers carried out automated probing of wafers on three length scales. Efforts commenced with fast wafer screening, which detected local variations at the wafer level. A chip-level review followed, uncovering variations between individual chips, before ultra-high resolution imaging exposed intra-chip variations.

To ensure that screening of the whole wafer offers a fast, insightful review, scanning occurs over multiple channels. By applying differential analysis to this data, engineers can identify shifts in peak wavelength, alongside variations in the intensity and width of the signals. This can uncover local 'hotspots' on variable length scales, exposed by extremes in the data.

Davies presented results of fast screening on a 100 mm wafer. This provided an easy discrimination of surface and buried particles by comparing the cathodoluminescence image with the scanning electron microscopy image, also provided by the Sântis 300 platform. According to Davies, extremes in data in good regions with a length scale of hundreds of microns are equivalent to extremes of data in regions covering several millimetres, implying that there is no need to probe all of a wafer to obtain reliable data.

The fast scan results allowed Davies and colleagues to select the best, the worse and the median 'performers' from a region. Using cathodoluminescence to image these chips with a high resolution unveiled the local threading dislocation density, while the corresponding scanning electron microscopy image offered insights into chip shape, etch deposits and mask transfer uniformity. By comparing the performance of the best, worse and median chips from different regions of the wafer, regional viability maps were constructed.

Davies claimed that the identification of low viability regions reduces the feedback time on critical process steps; lowers the total probing costs, by optimising the time spent during a subsequent metrology step; and speeds time to market, by accelerating the time taken to understand which process changes have the biggest impact on viability.

Ultra-high resolution mapping, which Davies sees as an optional extra, employs a pixel size below 100 nm. Imaging at this length scale provides an insight into the local threading dislocation density and allows evaluation of the emission wavelength homogeneity, the intensity homogeneity at the chip level, and the shape and uniformity of the mesa edge.

Tools for vertical LEDs

One of the implications of shrinking the size of the microLED, and the resulting shift from the flip-chip to the vertical architecture, is the need to introduce new tools and processes to some LED fabs. Two of the key features of a vertical LED are an ITO layer that provides a transparent, current spreading layer and a distributed Bragg reflector (DBR) for boosting light extraction – examples of equipment that can add these features formed the focus of a presentation given by Stefan Seifried, Head of the Optoelectronics Business Unit at Evatec.

Seifried explained that Evatec offers tools for single-wafer and batch deposition of ITO, both accomplished with a low-damage process. For a batch process, Evatec offers the CLN 200 BPM, which can handle substrates up to 200 mm in diameter and vary the ITO deposition temperature from below 80 °C to as high as 350 °C. Using this tool, on 150 mm substrates ITO thickness uniformities across the wafer, between wafers and between runs are below 1 percent for 15 nm-thick and 100 nm-thick layers. Switching to 200 nm substrates degrades the uniformity of the ITO thickness, with the greatest level of non-uniformity found within-wafer on 15 nm-thick films – in this case, non-uniformity is 3 percent.

➤ The Smartwatch is tipped to be one of the first applications where the microLED will make an impact.

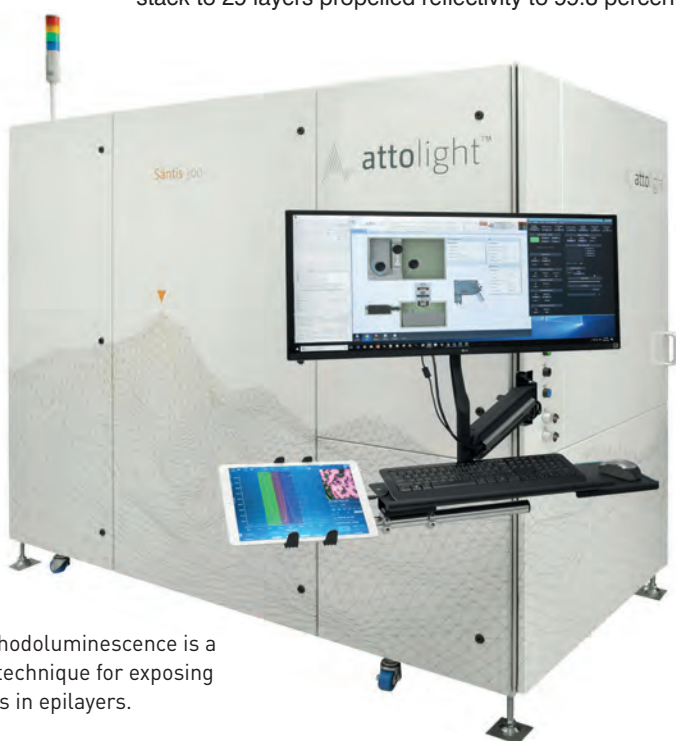


► Augmented reality is an attractive application for the microLED, but device dimensions need to be below 2 μm .



When ITO is deposited on the epilayers, it forms grains with dimensions that vary with process condition. Increasing the temperature and the throw distance leads to increases in grain size.

The CLN 200 BPM can also be employed to deposit a stack of oxide films that form a DBR. Seifried shared results for a 10-layer stack assembled from alternating SiO_2 and TiO_2 layers. The mirror had a reflection band centred around 570 nm with a reflectivity of 98.4 percent. Uniformities across 150 mm-diameter wafers, between them and between runs are no more than 0.5 percent, when evaluated by considering values for 90 percent reflectivity. Increasing the DBR stack to 29 layers propelled reflectivity to 99.8 percent.



► Cathodoluminescence is a great technique for exposing defects in epilayers.

ALD advantages

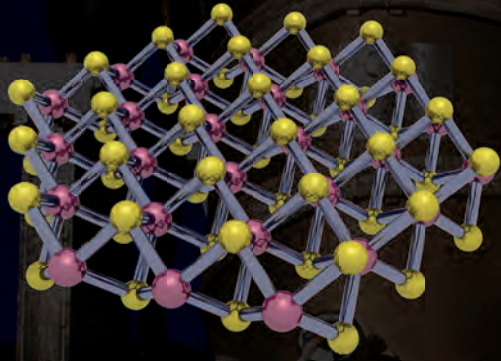
Another option for depositing thin films, promoted at CS International by Beneq's Head of Worldwide Sales, Mikko Söderlund, is atomic layer deposition (ALD). Söderlund argued that the attributes of ALD include: its gentle, sequential gas-phase process; the formation of dense, pinhole-free coatings with unrivalled conformality; a process window spanning 70 °C to 400 °C that is well-suited to back-end-of-line processing; easy process control and repeatability; the opportunity to scale by batch processing; and a good selection of materials with tuneable properties.

According to Söderlund, ALD can be used to improve the performance of the microLED. Using this technique to passivate sidewalls, possibly with a film of Al_2O_3 , increases external quantum efficiency while lengthening lifetime, lowering leakage current and minimising wavelength shifts. ALD can also be used to produce DBRs with a thickness precision that is sub-nanometre, and a nanometre thickness uniformity. There is also the possibility to produce coatings with an incredible level of resistance to moisture.

To carry out all these processes, Beneq offers the Transform portfolio. This suite, combining thermal and plasma-enhanced ALD processing modules, enables single-wafer and batch processing. These tools can accommodate wafers up to 200 mm in diameter – 300 mm is on the roadmap – and provide deposition of a wide variety of thin films, including Al_2O_3 , SiO_2 , HfO_2 , Ta_2O_5 , TiN, AlN, SiN and ZnO.

These ALD tools, plus those providing other deposition techniques and metrology, are sure to play a key role in the emergence of the microLED industry. Progress over the coming months will be reported at the next CS International, held on 28-29 June 2022, so save the date now so you can follow the latest developments in this very promising sector.

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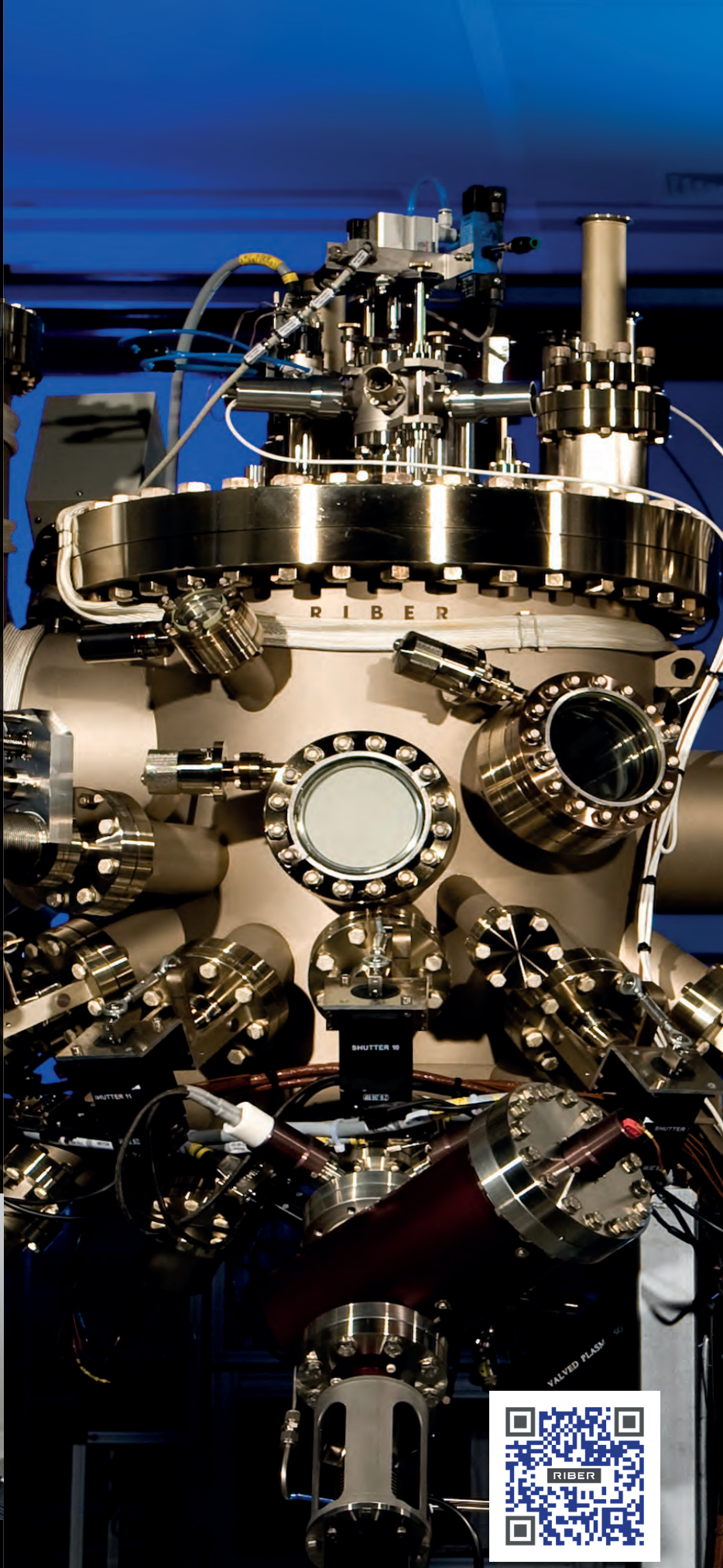
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The flaws in Haitz's law

A successor to Haitz's law is needed, now that the focus has shifted from the brightness of the LED and its retail price to its efficacy and its colour quality

BY MICHAEL WEINOLD FROM **ETH ZÜRICH / UNIVERSITY OF CAMBRIDGE**

THERE'S A LOT to like about the LED bulb. It draws very little power, it comes on in an instant, it lasts for tens of thousands of hours and thanks to falling prices, it is now very inexpensive. Thanks to all these merits, sales of this source of illumination continue to climb. In the European Union and the United States, the LED's share of the general illumination market has recently topped 50 percent, and in 2020 estimated annual electrical energy savings from the adoption of LED-based lamps in these geographies amounted to 131 TWh/year and 442 TWh/year, respectively.

The biggest drivers behind the solid-state lighting revolution have been the dramatic reductions in the cost of this emitter and the hike in its efficiency. Within just 25 years of the introduction of the first commercial white LED, the electrical efficiency of this device has rocketed by three orders of magnitude, while

manufacturing costs for LED chips have fallen by two orders of magnitude. Today, bulbs based on LEDs are delivering efficacies of 200 lm/W or more, and thanks to substantial retail price reductions, purchase prices can be as low as \$1 per 1000 lumen.

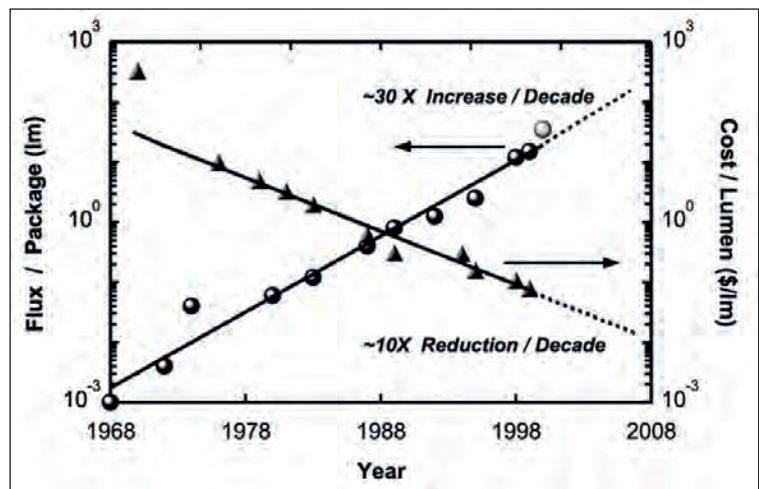
In scientific and technical literature, progress in LED technology tends to be illustrated with a pair of plots: those of the total luminous flux per packaged LED, and the associated up-front purchase cost-per-lumen. Both are based on logarithmic axes over time. The first prominently featured version of such a plot appeared in a report, published in 2000, that was commissioned by the United States Department of Energy and written by Roland Haitz, working at Hewlett-Packard, and co-authored by colleagues at both HP and Sandia National Labs. The striking visual and contextual similarity of both these plots to that of Moore's law

ensured its popularity in subsequent publications, while giving rise to the designation of the historical progress in these metrics as 'Haitz's law' (Figure 1).

Outdated metrics

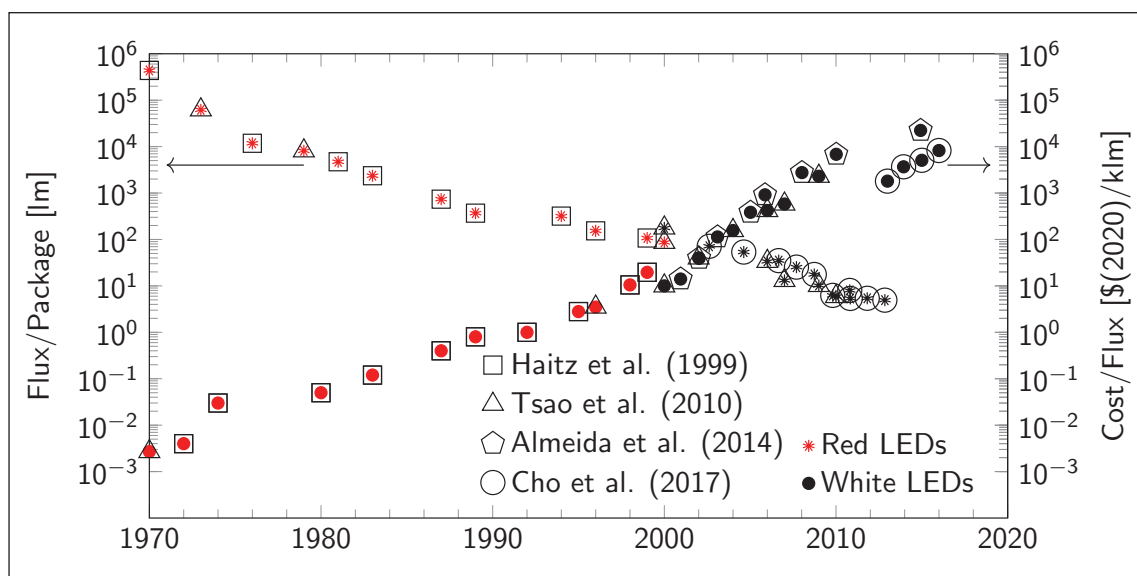
Since the turn of the millennium, Haitz's law has been widely used as a measure of progress in LED technology and industry. However, despite its continuing popularity, the metrics used in Haitz's Law are no longer providing meaningful representation of technological progress in this field. That's because there are two significant flaws in Haitz's law. One is that in recent years, the total brightness per package has become a less relevant metric for assessing industrial progress. The other significant flaw is that recent updates to Haitz's law are failing to normalize the brightness-per-total-chip area.

Regarding the latter issue, recent updates to Haitz's law figures (see Figure 2 for a summary) do not take into account the different levels of device integration found in LED products on the market today. When Haitz and co-workers published their initial figure, retail products were primarily single-chip packages. That's not the case today, with most commercial products now containing multiple chips in a single package. Plotting the total flux of multi-chip packages together with historical single-chip packages distorts the real trend of increasing flux in high performing LED chips (see Figure 3). Correcting this skew is not easy, because even when single-chip packages are explicitly labelled, the task of normalization-per-surface area is hampered by datasheets that only detail package dimensions – and they can be considerably larger than the area of the chip they enclose.



➤ Figure 1. The original figure prepared by Roland Haitz et al. in *The case for a national research program on semiconductor lighting*, published in 2000. The figure presented 'Historical and projected evolution of the performance (lm/package) and cost (\$[2000]/lm) for commercially available red LEDs'. Cost was defined as 'the price charged by the LED supplier to OEM manufacturers'.

As for the former issue, the use of diode brightness as a metric of progress implies that brightness has remained the primary focus of research, development and manufacturing efforts in the past decades. But while that's true of the past, it holds no longer. While low brightness has historically been a major limitation on potential applications of LEDs, this was no longer the case at the time the first commercial LED light bulbs came to the mass market around 2010.



➤ Figure 2. Summary of recent representations of Haitz's law in scientific literature. Historical increases in luminous flux and decreases in purchase price are plotted for LED packages. Note the units on the right on the vertical axis are kilolumens (klm) as opposed to lumens (lm) in the original 2000 figure by Haitz et al. Data points for red LEDs include devices based on various materials, with original data points from Haitz et al. (2000) marked by squares. Data points for white LEDs are for GaN based, phosphor-converted cool-white LEDs. Compiled from publications: Haitz et al. 2000; Haitz et al. 2010 (10.1002/pssa.201026349), De Almeida et al. 2014 (10.1016/j.rser.2014.02.029), Cho et al. 2007 (10.1002/lpor.201600147)



► Battle of the bulbs: cool-white LEDs are slowly replacing warm-white halogens in this residential high-rise. Decreases in retail price and improvements in electrical efficiency have underpinned this switch.

New yardsticks

For the last decade and more, in the eyes of both industry and policy makers, the primary metric for LED-based lighting has been efficacy. Unfortunately, there is a trade-off between higher brightness and higher efficacy (see Figure 4). This occurs because brightness is a function of diode current, and electrical losses in the device increase with diode current.

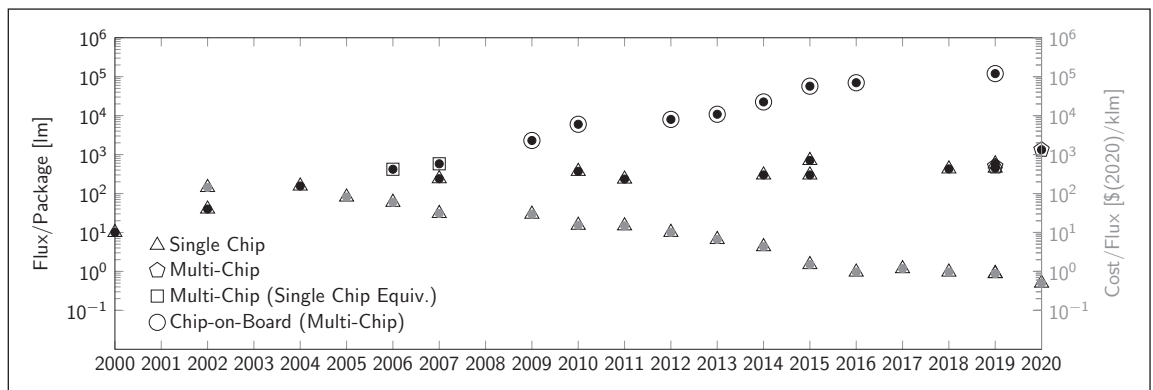
In the last few years, western lighting manufacturers have given far more consideration to human-centric lighting to increase sales. This shift in emphasis had led to improvements in LED technology that are not focussed primarily on total brightness, but rather on other properties of this light source that matter more to consumers, such as colour-rendering performance, colour temperature ranges and minimal flicker.

Lighting design considerations limit the brightness of devices. Designers of luminaires do not want to work

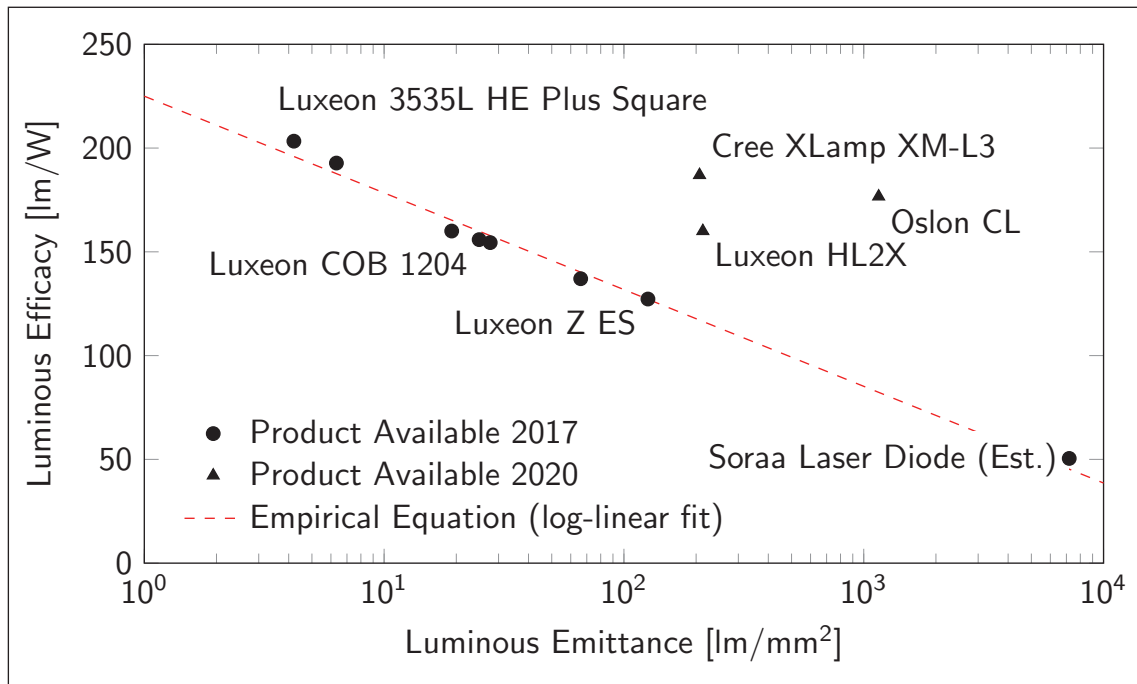
with small light sources of high brightness, because they have a level of glare that leads to unpleasant viewing experiences.

In addition to the two problems detailed above, associated with brightness and the number of chips per package, there are potential pitfalls associated with interpreting the cost metric of Haitz's law. Plots tend to use up-front retail prices of LED-based luminaires, rather than actual LED manufacturing costs. While the former is certainly a metric that matters to consumers, it is not a good proxy for diode manufacturing costs. Taking a more rigorous approach is not easy, however, as it requires information on company margins, so that manufacturing costs can be deduced from price data, which is proprietary by nature.

Another weakness of the cost metric of Haitz's law is that it obscures the real progress in LED chip



► Figure 3. Historical increase in luminous flux and decrease in purchase price for GaN-based, phosphor-converted cool-white LED chips and packages since 2000. Shown are datapoints for the best commercial performers from press releases, datasheets and industry periodicals. Different package types, containing one or more chips, are marked for reference. Note the units on the right on the vertical axis are kilolumens (klm) as opposed to lumens (lm) in the original 2000 figure by Haitz *et al.* Note that the overall increase in flux per single chip over time is significantly smaller than in the flux for multi-chip packages.



► Figure 4. The trade-off between brightness and efficacy in commercial white LEDs. The plot includes LED lighting products available in 2017 and 2020, ranging from low-power to high-power devices. The dashed line shows a log-linear fit of the empirical data for 2017. Data adapted and updated from the *2019 Lighting R&D Opportunities* report published by the US Department of Energy.

manufacturing costs, as by necessity it also includes the cost of LED packaging and the luminaire. For instance, chip manufacturing costs are reduced significantly by going to larger wafer sizes, while the cost of packaging steps, particularly at the luminaire level, remains relatively stable and thus becomes the single biggest contributor to the total cost.

Understanding the shortcomings of Haitz's law provides a foundation to proposing more meaningful metrics for tracking recent technological progress in solid-state lighting.

First, one valuable contribution would be to introduce a new yardstick for measuring improvements in performance. Today, the flux per package and the flux per chip are poor primary metrics for describing recent improvements in LED technology. Efforts in research and development have mostly focused on increasing luminous efficacy, and on improving metrics related to human-centric lighting. Considering this, it would be better to monitor performance improvements in LEDs using diode efficacy for a given colour rendering index and colour temperature.

The adoption of this methodology would not be difficult, because historical data for LED efficacy is available from product datasheets, and also from the solid-state lighting reports of the US Department of Energy (see Further Reading). There are also scientific publications and technical reports that provide data on the underlying device sub-efficiencies, describing different physical loss channels within devices. An excellent

example of this is a paper from Sandia National Labs, by Jeffrey Tsao and co-workers and published in 2010. Using this metric, our team from ETH Zurich and the University of Cambridge has quantified the impact, over the last 25 years, of technological breakthroughs and performance improvements on LED manufacturing. We first presented our findings at this year's *Photonics West* conference.

Second, as already pointed out, the retail price of LED luminaires per flux is of limited use as a proxy metric for LED manufacturing cost, because it includes unknown manufacturer margins, as well as the costs of LED packaging and producing the luminaires. We recommend focusing directly on LED manufacturing costs for evaluating LED technology cost reductions over time.

This might appear a challenging approach, given that LED manufacturing cost is often proprietary. However, major western manufacturers voluntarily report selected data to the US Department of Energy (DoE) as part of the SSL Industry Roundtables. This data, provided in regular reports on progress in lighting (see Further Reading), provides a deeper level of insight into decreasing manufacturing cost than the retail price of lamps (see Figure 5).

Note that even when specific data is not available this approach can still be adopted, as one can turn to a bottom-up manufacturing cost model. This methodology can draw on a comprehensive template provided by the LEDCOM cost model, first developed

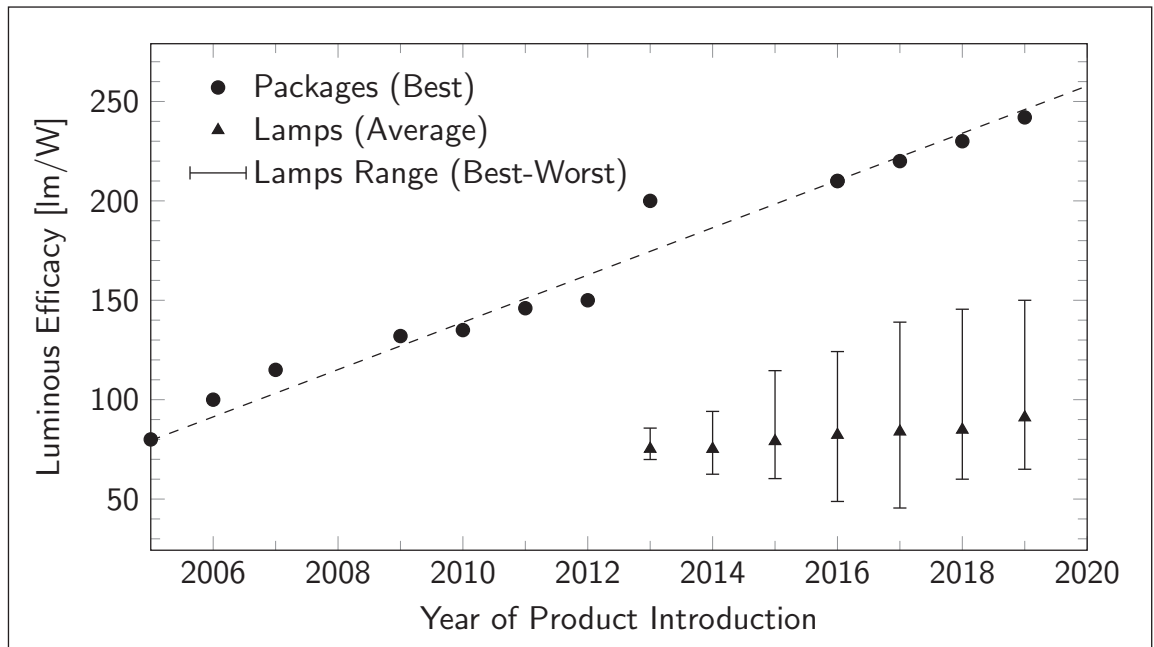


Figure 5. A proposed alternative to Haitz’s law: the historical trend of luminous efficacy in GaN-based phosphor-converted cool-white LED packages and lamps with a colour rendering index (CRI) below 90. The dashed line gives a linear fit of data for best performers, indicating an annual efficacy increase of 13 percent. Lamps have lower efficacy due to additional loss channels from the electrical ballast and additional optical elements. Data for lamps taken from the Energy Star LED Bulb database (https://www.energystar.gov/products/light_bulbs), data for best performers from scientific publications, datasheets and industry periodicals.

for the DoE in 2012 (see Further Reading). Making reasonable assumptions about the progress of technology allows this type of model to predict how manufacturing costs will evolve.

Two decades after the introduction of Haitz’s law, now is the time to accommodate changes in LED technology and industry. There are fundamental flaws in displaying data on contemporary multi-chip LED designs alongside historical single-chip designs – this distorts the real picture of technological progress in this field. Another pitfall is to use retail prices. While they provide valuable information to consumers, they fail to offer sufficient insight into industrial developments.

We are encouraging research, policy and industry communities to move on from Haitz’s law, which is a historically valuable but no longer relevant indicator of progress in the LED industry and technology. We propose instead to replace it with metrics that are better at representing LED technology improvements in areas that matter the most right now, rather than those that did 20 years ago.

○ *The author would like to thank Prof Laura Diaz Anadon and Dr Sergey Kolesnikov for valuable discussions and input. This research is funded by the Alfred P. Sloan Foundation, grant number 253128. Michael Weinold further gratefully acknowledges support from the Swiss Study Foundation of Zurich, Switzerland.*

FURTHER READING

- Research Project of the authors: <https://www.ceeng.landecon.cam.ac.uk/research/climate-change-and-energy-policy/what-factors-drive-innovation-in-energy-technologies-the-role-of-technology-spillovers-and-government-investment>
- Weinold *et al.* “Quantifying the impact of performance improvements and cost reductions from 20 years of light-emitting diode manufacturing”, SPIE OPTO, 2021 <https://doi.org/10.1117/12.2577591>
- Haitz *et al.* “The case for a national research program on semiconductor lighting”, Sandia Report, 2000

https://old-www.sandia.gov/~jytsao/hpsnl_sand_report_2000.pdf

- Tsao *et al.* “Solid-State Lighting: An Integrated Human Factors, Technology, and Economic Perspective”, Proceedings of the IEEE (Volume: 98, Issue: 7, July 2010) <https://doi.org/10.1109/JPROC.2009.2031669>
- United States Department of Energy Solid-State Lighting Research Publications: <https://www.energy.gov/eere/ssl/information-resources>



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SiC flexes its green credentials

With ramping levels of chip production and proven green credentials, SiC is well-positioned to play a major role in preventing excessive global warming

BY **RICHARD STEVENSON**

THE DRIVE to net zero cuts both ways. It promises to spur sales of products that cut carbon footprints; but it also heightens the scrutiny that is subjected to anything claimed to curb the rise in the temperature of our planet.

For many years the makers of SiC diodes and transistors have championed the capability of these

devices to green our world by deploying them in place of silicon incumbents in electric vehicles, various forms of power supply, solar inverters and power drives for motors. In all these applications making the transition to wide bandgap power electronics trims efficiency losses and paves the way to higher switching frequencies, which in turn allows substantial reductions to the size and weight of electrical units.

However, producing SiC devices requires a great deal of energy, in part due to the need for incredibly high temperatures for processing this material. So does SiC really have green credentials? And if it does, is it possible to produce diodes and transistors in volumes that are high enough to actually make a difference?

Providing an emphatic ‘yes’ to both those questions were some of the biggest names in the SiC industry, speaking at this year’s European Conference on SiC and Related Materials (ECSCRM), held from 24-28 October in Tours, France. At that hybrid event John Palmour, CTO of Wolfspeed, delivered compelling evidence for the carbon-cutting capability of SiC power devices, alongside plans to ramp their manufacture; Mario Giuseppe Saggio, SiC Power Devices Design Director at STMicroelectronics, championed the benefits that these devices deliver to electric vehicles, as well as outlining the company’s roadmap for increasing its SiC power portfolio; and Victor Veliadis, Deputy Executive Director and CTO of PowerAmerica, presented an option for cutting the cost of SiC device manufacture.

Gloriously green

Speaking in person at the conference, Palmour presented the results of incredibly rigorous calculations for evaluating the environmental impact of SiC devices. This work, considering the energy of SiC device production from the “cradle to the factory gate”, included factors such as the energy to build and ship production tools and make substrates.



When comparing a 400 V silicon IGBT with a SiC MOSFET – these are rivals for deployment in a typical electric vehicle – researchers found that the wide bandgap rival takes about four times as much energy to produce. For this class of MOSFET, requiring 4.75 GJ to make, more than three-quarters of the energy expenditure is associated with the electricity consumed during its production. However, the savings that come from SiC easily outweigh the additional energy required for its production. For a sedan in EV form, assuming that it covers 200,000 miles over its lifetime – that’s a reasonable figure, given that the relatively few moving parts should ensure high reliability – the superiority of SiC over silicon is, in energy terms, a factor of 7:1. And if the EV can operate at 800 V rather than 400 V, this factor climbs to 13:1. Such high returns matter a great deal to the automotive industry, emphasized Palmour, because they allow this sector to get closer to its carbon-neutral target.

Even higher returns on energy expenditure are possible in the solar sector. That’s not surprising when considering that cars tend to spend most of their time not being driven, while PV inverters operate for many hours every day. Palmour stated that for a 50 kW system in Albany, the payback would be 55:1, while in the sunnier climes of Phoenix, that figure should hit 77:1.

Further insights into the benefits of using SiC in electric vehicles were provided by Mario Giuseppe Saggio from STMicroelectronics. He pointed out that a typical internal combustion engine has a mass of between 100-250 kg, runs at 250 °C, has an efficiency ranging from 30 percent to 45 percent, and for every kilometre driven, it emits more than 100 g of CO₂.

“That’s a very large number,” pointed out Saggio. In comparison, electrical motors are considerably lighter, operate at 65 °C with an efficiency of more than 90 percent, while emitting no CO₂.

Sales of electric vehicles are tipped to climb at a phenomenal rate. Saggio pointed out that one market analyst recently revised its forecast upwards, upping the figure for the compound annual growth rate for the next few years from an already impressive 27 percent to a whopping of 42 percent. Such an astonishing growth rate will help to meet goals for market shares of EVs: in the US and Europe, political leaders have set targets of 50 percent and 37.5 percent by 2030, respectively; while China is aiming for 30 percent by 2025.

Moving to far greater electrification of transportation will deliver a tremendous hike in sales of semiconductor devices to automakers. According to analysis quoted by Saggio, the car market was worth \$35 billion in 2020, and will soar to more than \$70 billion by 2025. Cars with internal combustion engines have a semiconductor content that typically totals \$400, while for EVs, this figure tends to top \$1000.

Saggio claimed that the motivation for using SiC devices, rather than those made from silicon, is not limited to a higher efficiency. The wide bandgap device also offers a smaller form factor and diminished demand for cooling – SiC has an excellent thermal conductivity, and can handle very high temperatures. For automotive applications, these merits have led to SiC being considered for traction inverters, high-voltage DC-to-DC converters and on-board chargers. While the cost of SiC is higher, with Saggio saying it can be \$300 more, analysis by Goldman Sachs suggests that thanks to a higher efficiency, switching from silicon to wide bandgap devices delivers efficiency savings worth around \$2000.

When accelerating hard, the power consumed by an EV is very different from when it is coasting along. These variations in load lead to differences in values for efficiency. Saggio compared values for efficiency at different loads, showing that for typical driving conditions, the benefits of SiC over silicon are even greater than at high loads.

For many considering whether to buy an EV, a potential deal-breaker is the long charge time. But, in future, it may take no longer to charge a car than fill a tank, suggested Saggio. He spoke of the possibility of a 350 kW fast charger, capable of injecting enough energy into a battery in 5 minutes to increase the vehicle’s driving range by 250 km. In his view, 800 V devices would suit this application, and could speed adoption of SiC MOSFETs rated at this value or slightly higher.

Incredible expansions

Many of the manufacturers of SiC devices have plans for a massive increase in their production capacity. The roadmap for Wolfspeed is well-publicised, with the building of a large fab in the Mohawk Valley in New York state attracting a lot of publicity.

During Palmour’s presentation, he offered an update on the construction of this 484,000 ft² fab that will swell the company’s production capacity by a factor of 30 compared with 2017. Despite the pandemic, the build is on track, with opening slated for 2022. Initially, Wolfspeed planned to start device production in its new fab on 150 mm substrates, before shifting to 200 mm variants in 2024. But this has changed, with the manufacturer now to use the larger size from the outset. Although there are downsides – currently, the cost-per-unit-area on 200 mm SiC is higher, due in part to an increase in the thickness of the substrate from 350 mm to 500 mm – there are considerable advantages in avoiding having to re-tool two years down the line.

Palmour provided some insights into the progress of Wolfspeed’s 200 mm SiC substrates and epiwafers. He shared cross-polarised images of 200 mm SiC substrates, saying that they indicate a very high a structural quality. Dislocation maps reveal basal plane and threading-screw densities of 684 cm⁻² and 289 cm⁻², respectively. Following chemical mechanical

► The additional energy required to produce SiC devices over those made from silicon is outweighed by the savings that stem from reductions in electrical losses of a PV inverter.



polishing, surface quality has been shown to improve, with a Lasertech surface scan revealing no scratches and just 66 defects. Another encouraging result is that trials of epilayer growth in three reactors show that it is possible to realise variations in thickness and doping uniformity that are just over 1 percent.

STMicroelectronics is also expanding its SiC production capacity. It is setting up a sister fab in Singapore, with qualification taking place in the final quarter of 2021. For producing its SiC diodes and MOSFETs, this multi-national draws on a combination of its internal production of 150 mm substrates, thanks to the acquisition of Norstel in 2019, and a supply agreement with Wolfspeed for material of that size. STMicroelectronics has interest in 200 mm SiC, and announced this summer that it had demonstrated the fabrication of SiC diodes on this platform.

Production of SiC MOSFETs is well-established at STMicroelectronics, with third-generation products automotive-qualified in late 2020, and a fourth generation underway. Saggio explained that in all these iterations a planar architecture has been favoured over a trench design, because it ensures a simple, very high yield process that is scalable. What's more, this geometry results in a higher channel mobility.

With the introduction of each new generation of MOSFET, customers gain access to better devices. Resistance has fallen from 52 mW to 21 mW and then on to 15 mW with the shift from the second to the third and then the fourth generation of SiC MOSFETs, a move that allows designers to exploit more current for the same die size, or a smaller chip for the same on-resistance. According to Saggio, one of the benefits of replacing a second-generation device with a third-generation equivalent is a trimming of losses by 65 percent.

Saggio also took the opportunity during his presentation to warn delegates of a false myth that is perpetuating and threatening to provide a headwind to the phenomenal growth in SiC sales. Rumours are circulating that SiC MOSFETs suffer from reliability issues that are linked to bias threshold instability. However, Saggio said that he has seen no evidence for this.

Additional motivation to migrate SiC device production to the 200 mm platform came from Victor Veliadis from PowerAmerica. He claimed that a shift from 150 mm to 200 mm SiC substrates could cut costs by 20 percent. However, to succeed, engineers making this move must increase thickness and doping uniformity.

Veliadis championed the use of silicon fabs for manufacturing SiC devices. He accepts that some new tools are needed that are specific to SiC production. They include equipment used for: dry etching; substrate thinning; ion-implantation doping; and for providing new processes for metallisation, and for the formation of ohmic contacts and a gate oxide with a high-quality interface. According to Veliadis, the total cost for all this equipment is in the range \$12-15 million. He believes such an investment is worthwhile, allowing silicon fabs that are "20 years obsolete" to process SiC.

With SiC's green credentials beyond doubt, and COP 26 highlighting that the need to tackle climate change is more pressing than ever, it is good to know that there are plans in place to deliver a tremendous ramp in the production of SiC devices. After all, this rapidly growing multi-billion dollar global industry is going to play a key role in securing the future of our planet.

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II-VI: The laser years

In the second of a pair of features to mark the fiftieth anniversary of II-VI, Chuck Mattera, the current CEO, looks back at the diversification of the company's offerings through the introduction and expansion of its laser portfolio

INTERVIEW WITH RICHARD STEVENSON

RS: *Your involvement with II-VI started long before you took over as CEO in 2016. Back in 2000, when working at Lucent Technologies Bell Laboratories, you started a two-year stint on the II-VI board, offering your expertise surrounding a variety of InP and GaAs laser diode technologies. At that time, how much progress had been made on the laser side of the business?*

II-VI: When I came into the company as a board member, I was coming from a perspective of a company making semiconductor laser components and fibre amplifier subsystems for communication

networks. Whether they were 1480-nanometre pumps or 980-nanometre pumps, or both, they were ending up inside an amplifier for a long-haul network. I was aware that IPG was figuring out ways to combine these pumps to cut steel. The workhorse of II-VI at that time was CO₂ laser optics, used by the Industry 3.0 infrastructure for cutting up to 25-millimetre-thick steel.

We had to ask ourselves the questions, 'Is the one-micron laser an opportunity, is it a threat, or is it both? How should we think about it, from a strategic point of view?'

Well before I got here, on the heels of the invention of the YAG laser, which operates at 1064 nanometres, II-VI realised that one-micron solid-state lasers were also going to be important. So II-VI acquired two small materials companies: Virgo Optics, in 1995, and Lightning Optical Corporation, in 1996. Those acquisitions of Virgo and Lightning created the well-known II-VI VLOC. VLOC became a division, and Fran [Kramer, who went on to be the company's second CEO] had a lot to do with that. I think it was the beginning of the company starting to cut its teeth on acquisitions: how to stage them, how to execute them, and how to integrate them.

RS: *In 2004, you joined II-VI as Vice President, with a charter to establish a compound semiconductors capability. You have been with the company ever since. What did you work on to begin with?*

II-VI: Fran and Carl [Johnson, co-founder and CEO at that time] encouraged me to think long-term about one-micron solid-state lasers and fibre lasers. We had this strategic challenge, and the future was unclear, but we acted on what our board also believed was an opportunity to transform the company. They encouraged us to take the long-term view, including



The acquisition of Anadigics in 2016 enabled II-VI to increase its production of VCSELs.

ten years and beyond, and come back with the management team and help lay out a number of scenarios that could play out and drive exceptional long-term shareholder value.

We laid out, over about a five-year period, a roadmap to enter the one-micron laser market. It was clear that IPG had already gotten started a few years before. It probably wasn't going to pay off to try and compete head-on without the basic competency, which was the semiconductor laser. So, we laid out a roadmap to take a view further up the food chain, for a component that was agnostic as to whether it used a YAG laser, a fibre laser, or a direct diode laser. Knowing that we would need time to either acquire or develop the competencies of the laser, we decided – and Fran guided us – to get two or three levels up in the stack as a high ground from which to learn the market and develop new competencies.

We identified a beam delivery system for cutting steel as a place where we could get organised and establish a beachhead and, from there, understand the market. So, in 2007, we acquired HIGHYAG. We acquired 75 percent of the company in 2007, and the remaining 25 percent in 2013. [With that acquisition] we could address people who were in the system business for establishing competencies for cutting steel, and at the same time collaborate with people who had a YAG laser, a fibre laser, or a direct diode laser. No matter where you looked, every place our optics were employed, a laser was being either focused, reflected, or refracted. A company that had this footprint could further accelerate its penetration into a growing market if they had access to the semiconductor laser. So, after Giovanni Barbarossa joined us in 2012 as our first CTO, we made a strategic decision to acquire a semiconductor lasers platform.

RS: *How did you progress toward that goal?*

II-VI: Along the way, in 2012, we acquired the Santa Rosa optics coating facility of Oclaro, which had been Cierra Photonics, a thin-film filter company acquired by Bookham; Oclaro got it through the acquisition of Bookham.

When we acquired the thin-film filter business, Fran established a rapport with Alain Couder, CEO of Oclaro. On the heels of a successful transaction in thin-film filters, and that CEO-to-CEO relationship, we expressed our interest in acquiring the Oclaro semiconductor laser capability in Zurich. That platform focused on the industrial market and was not in line with the core of Oclaro, which is communications. Fran saw that as a nice opportunity.

I had been to [Oclaro in] Zurich for the first time in 1988, when it was IBM, and I had been there a few times before 2013, when we started due diligence. I had a real good idea about what a compound semiconductor fab and team looked like, because



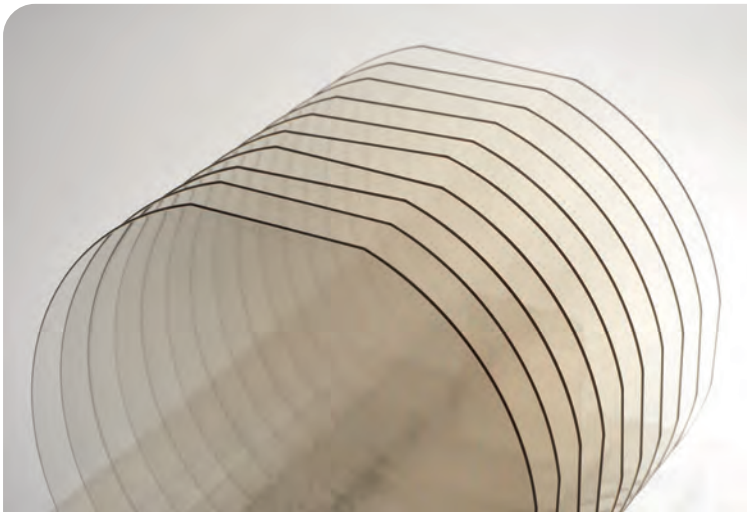
I had said goodbye, in my humble opinion, to the world's best when I retired in January 2003. Maybe I spent a week or two there. I was so impressed by what they had accomplished, and I fell in love with the team, as I have with all the other acquisitions we have done since I've been at II-VI.

I really liked the gallium arsenide laser. What I liked about it, besides the team, was the technology endowment, the accumulated knowledge, and the experience they had developed, all the way back to the investment by IBM for getting high-power LEDs and lasers to keep pace with the high-speed printing infrastructure, including for 200-megabit optically linked mainframe computing.

What we got [from the acquisition] included Avalon Photonics, a VCSEL innovator. They were selling VCSELs into the mouse market and the Blackberry market for finger navigation.

In 1988, I was part of the Bell Labs development team for VCSELs. There were maybe 35 to 50 of us. So I had a perspective about VCSELs when I got to Zurich, and I was excited about that. It wasn't too long after that we learned about other opportunities for the VCSEL, including those for the 3D sensing market.

The acquisition of HIGHYAG in 2007 opened up new opportunities for II-VI, by allowing the company to collaborate with makers of YAG lasers, fibre lasers and direct-diode lasers.



II-VI has a strong pedigree in SiC. In 2015 it produced the world's first 200 mm SiC substrate, and recent acquisitions of Ascatron, INNOVION and the IP of GE have strengthened this part of the business.

Given our long-term roadmap for the industrial fibre laser market, and the benefits of vertical integration of our components capabilities, we thought that the best thing we could do was acquire the amplifier business from Oclaro at the same time. So, our management team recommended that we do that. Fran understood the value proposition, and he could easily see that this long-term vision that he and Carl asked me to take early on with regard to the one-micron laser market was beginning and was complementary to Photop Technologies, the one-micron optics platform we acquired in 2010. So, by this time, we had established the beachhead, and now we were working to backward-integrate all the way to the laser component, which I believe was a great decision and a turning point for II-VI.

RS: *What else did you need to complete the line-up?*

II-VI: There was one step in between: the subsystem, as it relates to communications in the future. We acquired the core elements of the laser, the subsystem, and the beam delivery system. Those three things were ultimately essential parts of the industrial food chain that would also branch out to serve an aerospace and defence market.

[At the time] we had built the foundations and the roof but in a sense were missing some floors. We had to go a bit out of order; sometimes you can't time these things perfectly, and you've got to have a long-term vision. Carl always ingrained in us the value of not getting full of ourselves with big ideas about revolutionising things, preferring to maintain a posture that the long game is won by evolution, rather than revolution.

RS: *In 2016, just three years after buying the Zurich facility, II-VI bought Anadigics. How did that come about?*

II-VI: When explaining laser technology to the II-VI board, we got to introduce the concept of the VCSEL. It became the centrepiece of a lot of our conversations when the opportunity for 3D sensing became more than just obvious; and when it became more than just obvious, it was that the scale that was going to be required was beyond that which Zurich had been sized for, so we needed an alternative.

At the time, Anadigics was still a public company. It had, by some measures, its exciting years behind it. To transform itself, it started offering a foundry service for making VCSELS for 3D sensing in 2014.

I went there as a prospective customer who might want to use their 6-inch technology to scale the design we were developing in Zurich. I visited their Warren, New Jersey, fab on a Sunday. On the way back, I called Fran and said I think we should acquire the company, as it would be the best way to scale our VCSEL capability and meet the market window.

Fran encouraged us to work further on the strategy, so we prepared a presentation to our board. As part of the strategy, we needed to be sure that we had enough VCSEL epitaxy capacity to serve the Warren fab should we be successful at acquiring Anadigics, so we identified EpiWorks of Champaign, Illinois, as the strategic target. We knew a lot of the functionality and value of the device was going to be added into the VCSEL by proprietary device designs and the epitaxy itself.

RS: *You became the company's third CEO in 2016, the year II-VI acquired Anadigics and EpiWorks. Three years on II-VI bought Finisar. How important was that?*

II-VI: In August 2016, I presented to the board a number of strategic opportunities in compound semiconductors and innovations in photonics, which underpin mega-growth markets. We had begun developing a footprint, both geographically and from a market perspective, in a number of growing markets. We had established a number of technology platforms, but some were missing. There were half-a-dozen or so opportunities that would allow us to increase the scale of the company and build out other parts of our infrastructure that would enable us to drive long-term value.

The single biggest opportunity at that time was the

We had begun developing a footprint, both geographically and from a market perspective, in a number of growing markets. We had established a number of technology platforms, but some were missing.

indium phosphide platform that Finisar had invested in for a long time. We like acquiring companies that have made long-term investments in innovation and R&D. With those investments and endowments, we begin to think about ways in which we can stitch together those platforms with either the business we have, or ones that we could have, don't have yet, but could target.

We liked that complementarity. In addition to the indium phosphide platform, a fabless design capability for electronics – for TIAs, for clock and data recovery circuits, and for laser drivers – and the experience Finisar had in not only designing but also making and scaling production lines for indium phosphide lasers, Finisar had also done a world-class job of integrating them with optics and electronics in a transceiver.

RS: *How will the buying of Coherent strengthen your offerings?*

II-VI: Coherent is the market leader in laser technologies and is a great complement to II-VI. Together we will make for a great opportunity to innovate at scale and drive long-term value in our respective markets, while we aim to drive growth in new ones as well.

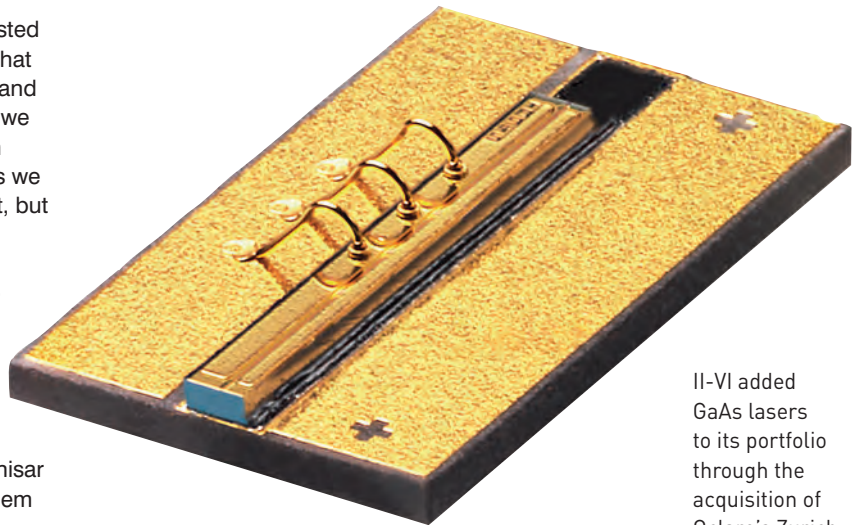
The acquisition goes with having the roof and foundation, and now putting in the floors. And as only one example, that relates to our earlier investments that we discussed: we believe it will enable us to competitively address the industrial fibre laser market. We have the amplifier, the laser, and the laser processing [head]; now comes Coherent's fibre laser.

RS: *Recent acquisitions have positioned II-VI as a major player in the compound semiconductor industry. In some of the sectors of this industry you are offering materials, and in other cases, it is devices. Do you have any plans to try and develop any vertical integration? And is this important within the compound semiconductors industry?*

II-VI: As it relates to compound semiconductors, vertical integration is an important element of our strategy, and I believe it will continue to be.

In silicon carbide, we started with more than two decades of investment in the substrate itself. We have realised that there is both an opportunity and an unfulfilled need, long-term, for high-performance modules based on high-performance devices, which in turn are based on high-performance silicon carbide substrates, epitaxial wafers, and ion-implanted devices.

To accelerate the development and the offering of those products, knowledge is gained between multiple levels of substrate and epitaxy, epitaxy and device processing and design, and reliability assurance and incorporation into a module. Overall



II-VI added GaAs lasers to its portfolio through the acquisition of Oclaro's Zurich facility.

integration of all that proprietary knowledge and innovation is most efficiently done when focusing on multiple layers of integration.

You can't do everything at one time, so it's not about revolution, but evolution. We have that underway with silicon carbide. To accelerate our developments, we acquired Ascatron in Sweden, which has capabilities for silicon carbide epitaxial growth; and before that we acquired INNOVION, that's an ion-implantation service provider that has IP and capabilities for high-temperature ion implants into compound semiconductors, including silicon carbide; and we acquired IP from GE, based on their long-standing investment in this technology. With these investments, we have a multi-year plan in place to be able to vertically integrate forward from the strong foundation we have in the substrate.

Finally, I wish to acknowledge the pioneering work of so many extraordinary companies and people who have invested for nearly fifty years to create an entire technology ecosystem that is vital to the world.



Since its founding in 1971, II-VI has had just three CEOs. To mark the fiftieth anniversary of the company, they got together this summer in New York. The current CEO, Chuck Mattera (centre), has led the company since 2016. Co-founder of the company, Carl Johnson, is on the right, and Fran Kramer, CEO from 2007 to 2016, is on the left.

► MicroLEDs are promising candidates for use in next-generation displays. The red, green and blue microLEDs shown here have dimensions from 20 μm by 20 μm to 100 μm by 100 μm



Enabling high-efficiency microLEDs

Sidewall treatments empower microLEDs with size-independent efficiency

BY MATTHEW WONG, JAMES SPECK, SHUJI NAKAMURA AND STEVEN DENBAARS FROM **THE UNIVERSITY OF CALIFORNIA, SANTA BARBARA**

THE COMMERCIALIZATION of smartphones and portable electronics has piqued academic and industrial interest in developing better display technologies. It's a sector that is moving fast, progressing from cathode-ray tubes to liquid crystal displays (LCDs) and more recently organic LEDs (OLEDs), with latter already employed extensively in wearables. However, emerging display applications – namely near-eye displays for virtual-reality, augmented-reality and head-up displays – are demanding even better display performances, such as a superior colour gamut and a greater resolution. Efforts at fulfilling these requirements are driving the rapid development of new display technologies.

Among the various candidates for next-generation displays, microLEDs are the most promising, offering a variety of benefits that include a high brightness,

a long operating lifetime, excellent stability and outstanding efficiency characteristics. While there is no official cut-off for the device dimensions of the microLED, with some use the term 'miniLEDs' to refer to bigger microLED, it is reasonable to assume that the dimensions of this device are less than 100 μm . The actual value matters a great deal, as it determines the display resolution and the manufacturing cost.

To produce a full-colour display, designers tend to employ red, green, and blue colours that match mankind's visual receptors. So when making a display, designers want to employ microLEDs with these three emission wavelengths. The emitting chips are made from either the InGaN or AlGaInP families of materials. Although InGaN-based LEDs are capable of spanning the entire visible spectrum, red InGaN LEDs are currently limited to the active research stage

and not commercially available. Hence, one option for realizing a full-colour microLED display is to employ InGaN microLEDs for the blue and green and AlGaInP variants for the red.

One of key advantages of the microLED display is that it draws on the exceptional performance of microLEDs. In this form of display, every red, green and blue subpixel is modulated independently. This equips the display with a simple architecture that is capable of futuristic applications. These are out of reach of conventional displays based on liquid crystals and OLEDs – they are held back by issues related to bulkiness and stability, respectively.

Scaling issues

As the performance of the microLED display is governed by device performance, these emitters must retain the remarkable optical brightness and efficiency of their larger siblings. For standard-size InGaN-based blue and AlGaInP-based red LEDs, engineers have demonstrated efficiencies greater than 80 percent and 50 percent, respectively.

These values give microLED displays the potential to operate with a much higher efficiency than today's LCDs and OLED displays, and deliver a leap in energy efficiency for display technologies. However, for this to happen, the efficiency of the LED must remain high when its dimensions are reduced. And that's far from a given: early reports show that the maximum efficiency of the microLED plummets when device dimensions are shrunk below 100 μm .

The dramatic fall in efficiency is attributed to two factors: sidewall damage and surface recombination. Both are inevitable in conventional device fabrication. Surface recombination results from surface states and dangling bonds of the semiconductor surface, and sidewall damage comes from a plasma process that's employed to define the light-emitting area. Both these issues, which are present in microLEDs and standard LEDs,

create undesired Shockley-Read-Hall non-radiative recombination sites. However, the key difference with standard LEDs is that they have a huge light-emitting area compared with the sidewall perimeter, so sidewall damage and surface recombination have minor influences on device performance.

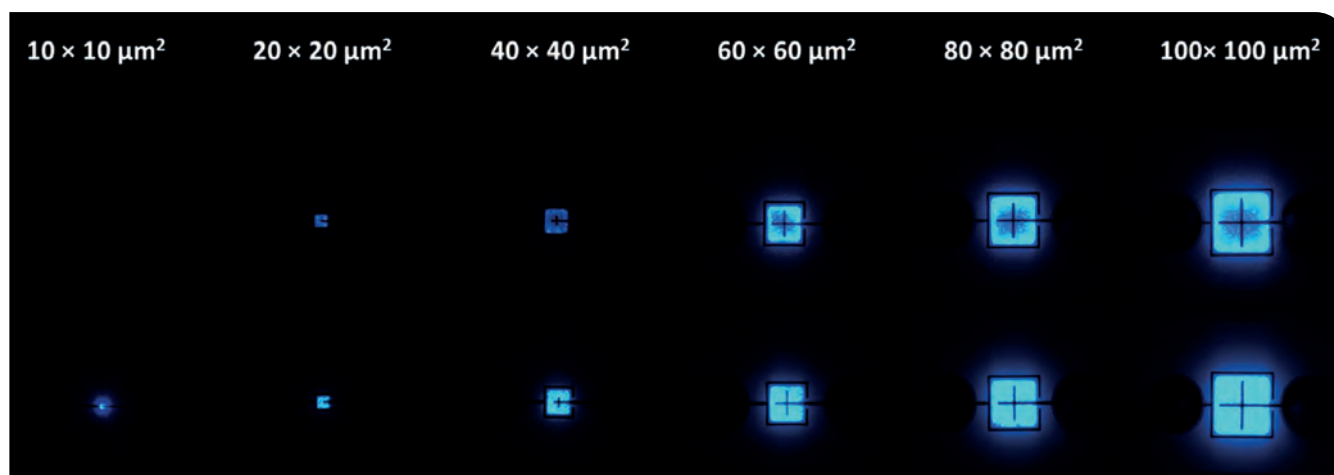
For these devices, other factors have a greater impact on efficiency characteristics, such as device design and material quality. In stark contrast, in small microLEDs sidewall damage and surface recombination can wreak havoc, due to a far higher sidewall perimeter-to-emitting-area ratio.

It is important to note that both these issues are more of a concern in LEDs made from the AlGaInP material system. As this alloy has a longer minority-carrier diffusion length and a higher surface-recombination velocity than the III-nitride material system, the fall in efficiency with scaling is more severe in AlGaInP red microLEDs than it is in the blue and green cousins made from InGaN.

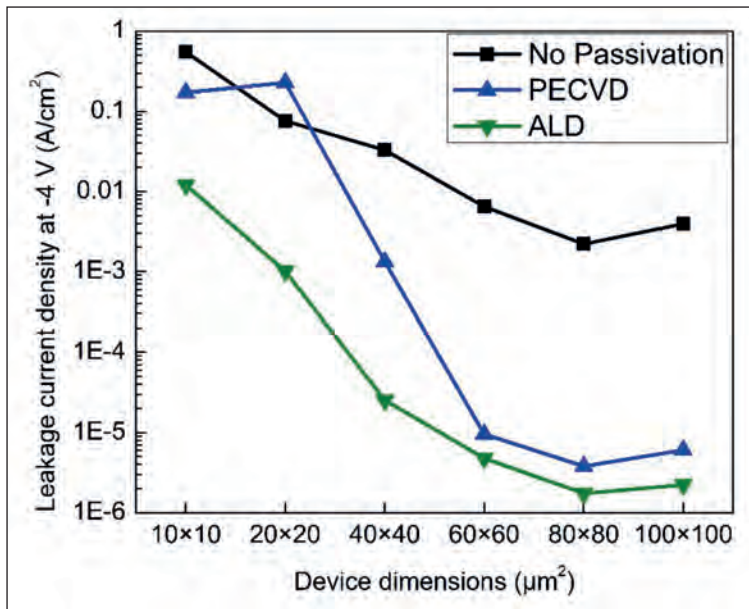
The impacts of sidewall damage and surface recombination are easily illustrated by measurements of optical performance, thanks to the strong coupling of efficiency and light output power characteristics (see Figure 1). Electroluminescence images of microLEDs with dimensions from 100 μm by 100 μm to 10 μm by 10 μm show that despite inhomogeneous light emission appearing in devices larger than 40 μm by 40 μm , the bigger devices are brighter. This indicates that non-radiative recombination has dominating influences in smaller devices.

Building better devices

At the University of California, Santa Barbara, our team is addressing these scaling issues associated with microLEDs by developing post-etch fabrication techniques that either lessen or eliminate the effects of sidewall damage and surface recombination. An insight into the pitfalls of scaling, and how to



► Figure 1. Electroluminescence images show that as microLEDs get smaller, their maximum efficiency decreases. This trend is a major issue, because ultra-small devices with high efficiency are needed to produce efficient microLED displays. Note that the crosses are the p-contact of the devices.



➤ Figure 2. Researchers at UCSB have shown that atomic layer deposition (ALD) and plasma-enhanced CVD cut the leakage current in microLEDs. These results are for InGaN microLEDs.

overcome them, is provided by measurements of the leakage current of microLEDs (see Figure 2). For devices without sidewall passivation, the leakage current is high for devices of all dimensions. However, the leakage increases as the device gets smaller, due to a rise in the perimeter-to-area ratio.

One well-known and common approach to reducing leakage, which stems from sidewall damage and surface recombination, is to passivate the sidewalls using plasma-enhanced CVD. This technique, also known as physical vapor deposition, is effective in larger devices. However, as the results in Figure 2 show, it fails to suppress leakage current as the device size shrinks.

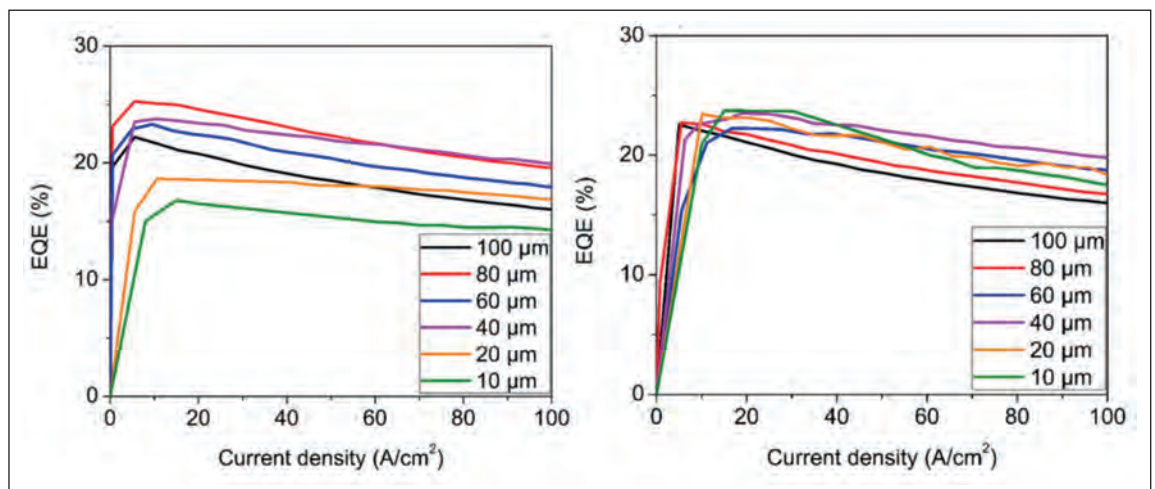
We are pioneering a superior alternative for microLEDs, using atomic layer deposition (ALD) to passivate sidewalls. Our results, presented in Figure 2, show that this technique is far better at suppressing

the leakage current than plasma-enhanced CVD. The success stems from the excellent dielectric material quality and the uniformity of thickness control provided by ALD, as well as this technique's more effective deposition mechanism that eliminates surface states.

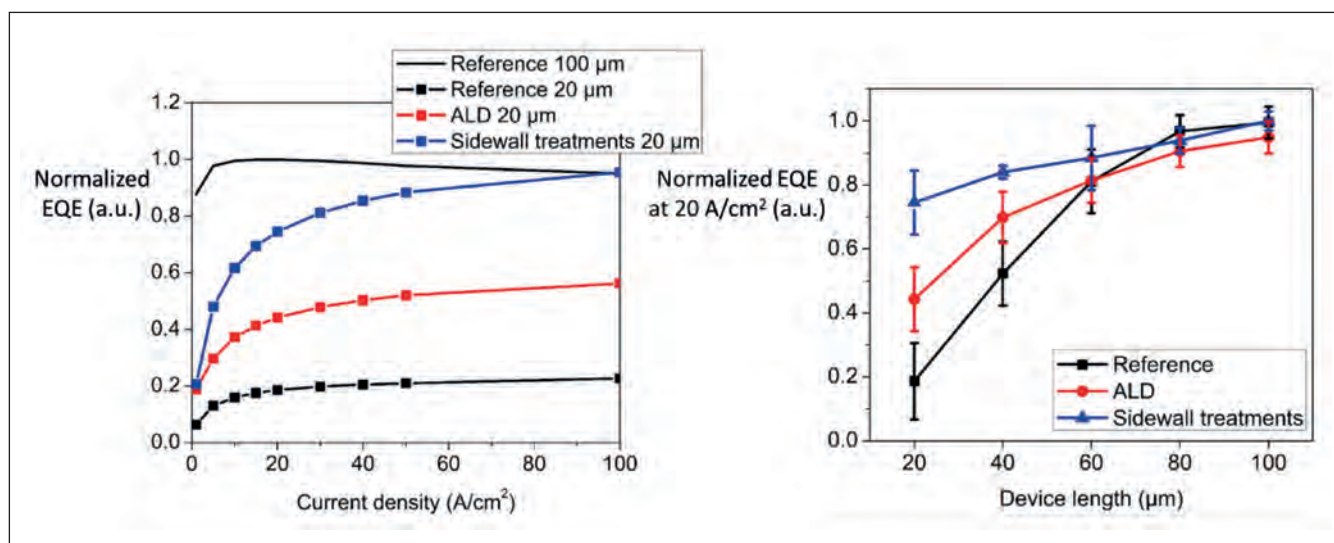
As expected, the benefits of ALD make the biggest difference in AlGaInP microLEDs. However, they still deliver significant gains in those made from InGaN. In both cases, devices with sidewalls passivated by ALD have better forward current-voltage characteristics, a lower leakage current and a lower ideality factor. Optical performance is also better, with ALD sidewall passivation ensuring a uniform light emission homogeneity (see Figure 1), and a significant increase in the light output power. For 20 µm by 20 µm microLEDs driven at 20 A cm⁻², this ALD treatment increases the light output power for blue-emitting InGaN devices by 40 percent, and for the red-emitting AlGaInP siblings by 150 percent. We attribute these gains to suppression of sidewall damage and surface recombination, and the resulting reduction in Shockley-Read-Hall non-radiative recombination.

The passivation of sidewalls by ALD is certainly a step in the right direction, delivering a remarkable improvement in the optical and electrical performance of InGaN and AlGaInP microLEDs. However, on its own it is insufficient to prevent efficiency from holding up when shrinking device dimensions. Additional sidewall treatment techniques are needed to realise miniature microLEDs with a high efficiency.

We have pursued this, combining chemical treatment with ALD sidewall passivation to demonstrate, for the first time, size-independent efficiency performance in InGaN and AlGaInP microLEDs. Our technique has much promise, providing a straightforward, versatile way to enhance the optoelectrical characteristics of the microLED.



➤ Figure 3. External quantum efficiency measurements show that treating InGaN microLEDs with potassium hydroxide chemical treatment and ALD sidewall passivation (results for conventional devices are on the left, and treated ones on the right) leads to leakage current and efficiency characteristics that are independent of device size.



► Figure 4. Combining sidewall treatments with etching in potassium hydroxide delivers a substantial improvement in AlGaInP microLED performance.

The downside of dielectric sidewall passivation is that it merely lessens the influences of sidewall damage and surface recombination. With this form of passivation, sidewall defects still drags down device performance. To eradicate these imperfections, chemicals can be applied that either alter the chemical composition or etch away surface defects, so that pristine material results at the sidewalls.

For InGaN microLEDs, we have combined sidewall passivation with a potassium hydroxide chemical treatment. This is an attractive approach, because we can draw on a wealth of reports that describe the reaction mechanism between potassium hydroxide and the III-nitride material system, and detail how this chemical treatment can be applied to standard LEDs.

Combining potassium hydroxide chemical treatment with ALD sidewall passivation has enabled us to realise size-independent leakage current and efficiency characteristics in InGaN microLEDs with dimensions from 100 µm by 100 µm to 10 µm by 10 µm (see Figure 3 for details of efficiency performance). These results reveal that with our approach we can eliminate or greatly diminish the influences of sidewall damage and surface recombination.

We have applied similar principles to AlGaInP devices. This has enabled 20 µm by 20 µm AlGaInP microLEDs to deliver a size-independent efficiency performance at a high current density (see Figure 4). This suggests that we are now on the brink of realising a size-independent efficiency for AlGaInP microLEDs, a goal that could be reached via optimizations that improve performance at low current densities. While we are still to demonstrate a size-independent efficiency at low current densities for the AlGaInP devices, we take heart from the significant reduction in the drop in efficiency at 20 A cm⁻², thanks to the

combination of chemical treatment and ALD sidewall passivation. With unoptimized sidewall treatments, the efficiency reduction in 20 µm by 20 µm AlGaInP microLEDs is just 20 percent at a current density of 20 A cm⁻²; in comparison, for devices without sidewall treatments and with just ALD sidewall passivation, reductions at the same current density are 80 percent and 50 percent, respectively.

Our work offers much hope for realising high-performance displays based on miniature microLEDs. We have substantially cut the reduction in performance with the scaling of red-emitting AlGaInP microLEDs, and a size-independent performance is now tantalisingly close.

◉ *The authors would like to acknowledge the Solid State Lighting and Energy Electronics Center (SSLEEC) for funding the research.*

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Advancing hybrid PICs

Innovations in InP laser design are destined to keep the energy consumed by the internet in check

BY **RICHARD STEVENSON**

JUDGED IN TERMS of its impact on our climate, the internet is both a friend and a foe. It has enabled teleworking and the remote attendance of international conferences, leading to a reduction in the number of journeys taken by car and plane; but it is having an impact on the climate that is roughly equivalent to the aviation industry, accounting for around 2 percent of the world's CO₂ emissions, according to the Boston Consulting Group.

With humanity's insatiable desire for data, there is the threat that the internet's contribution to the global

carbon footprint will rocket. Fortunately, though, gains in the efficiency of infrastructure are offsetting exponential rises in the transmission and consumption of data.

To ensure that this equilibrium continues, much effort is being devoted to developing components that set a new benchmark for the energy required per bit. If they are to have a commercial impact, competitively pricing is also essential.

Addressing both of these key requirements is the hybrid photonic integrated circuit (PIC), combining the low cost, large wafer size and high level of maturity of silicon technology with the InP laser, the only realistic choice for a high-performance light source operating in the spectral domains employed for data transfer.

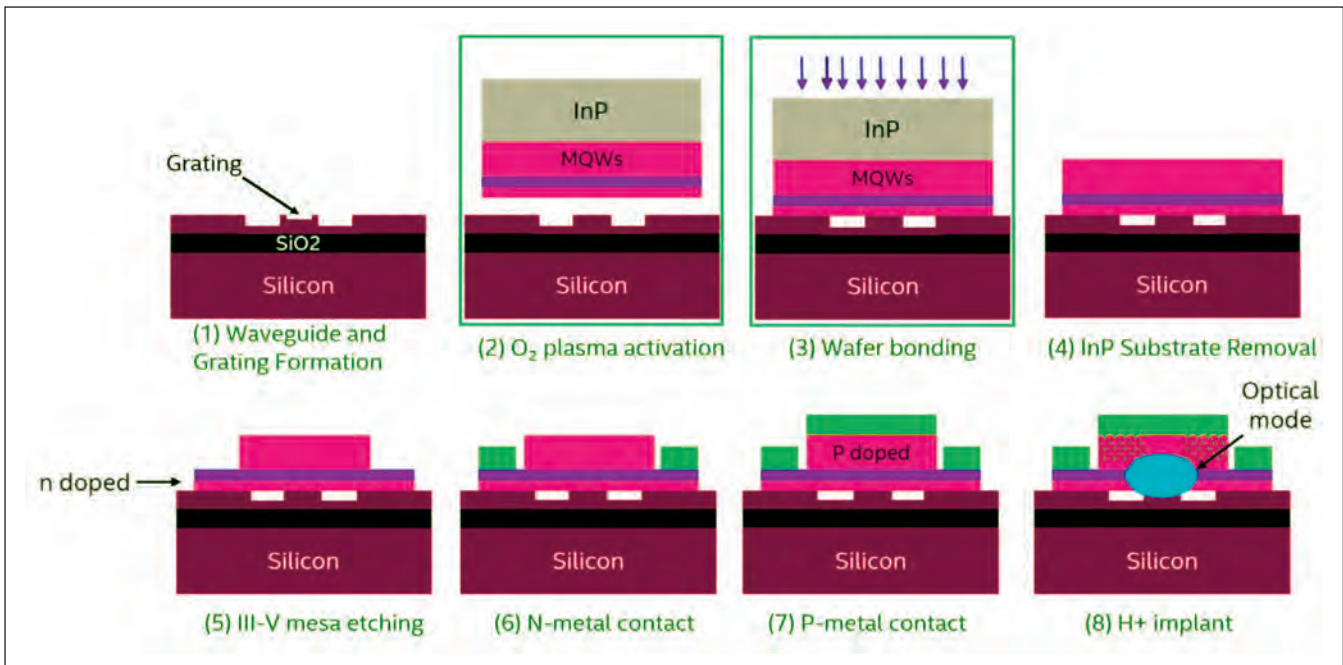
At the 27th International Semiconductor Laser Conference (ISLC), held in Postdam, Germany, from 10-14 October and organised by FBH Berlin, engineers showcased a variety of technologies for forming InP-based lasers on silicon substrates. Triumphs announced at that meeting included an 8-channel transmitter by Intel, featuring distributed feedback (DFB) lasers; a laser with a wide tuning range and a two-storied ridge structure, pioneered by a team led by Sumitomo Electric Industries; and a GaInAsP laser within a buried-ridge waveguide structure, trailblazed by researchers at Tokyo Institute of Technology.

Turbo-charging optical engines

Intel is well-known for its development of optical transceivers for data centres. These products, which first hit the market in 2016, are produced with a 300 mm hybrid silicon photonics platform that features advanced lithography.

At ISLC, Intel's Duanni Huang outlined to delegates attending in-person and on-line how the deployment of these transceivers will evolve over time. Huang





► Figure 1. Intel’s hybrid III-V/silicon laser process begins by taking a silicon wafer with a silicon-dioxide layer and defining a waveguide and a grating using deep-UV lithography. Oxygen plasma activation of the wafer follows, along with the bonding of InP chiplets to silicon. The bulk InP is removed to leave behind just the active region, before a III-V mesa is etched and the laser contacts added. The final step involves passivating regions of the mesa with hydrogen-ion implantation to leave a current channel in the centre that overlaps with the optical mode.

explained that the company’s 100 Gbit/s to 400 Gbit/s transceivers are now being produced in high volume for ethernet-compliant products. These transceivers are based on front-plate pluggable optics and operate at an energy efficiency of 30 pJ/bit. “In these products, the optics is still very far away from the central Ethernet switch,” remarked Huang.

“In 2020, we had a demonstration of so-called co-packaged optics, in which a photonic engine capable of 1.6 terabits-per second is co-packaged with the switch core,” remarked Huang.

This is said to bring the optics much closer to the photonics. With this architecture, optical engines could run at a total data rate of up to 3.2 Tbit/s, while drawing less than 15 pJ/bit.

Looking further ahead, Intel anticipates a time when photonics will be united with the package where the processor sits, using an optimised optical interface. This architecture will operate at a total data rate that could be as high as 16 Tbit/s, and have an energy efficiency well below 5 pJ/bit.

“In order to reach the bandwidth density and energy efficiency needed to make this happen, we utilise wavelength-division multiplexing,” revealed Huang. This approach, similar to that employed in long-haul links, exploits the resonance of silicon micro-ring modulators to select specific wavelengths. At the receiver, a similar approach can be employed to separate the various wavelengths transmitted down the fibre and extract encoded data.

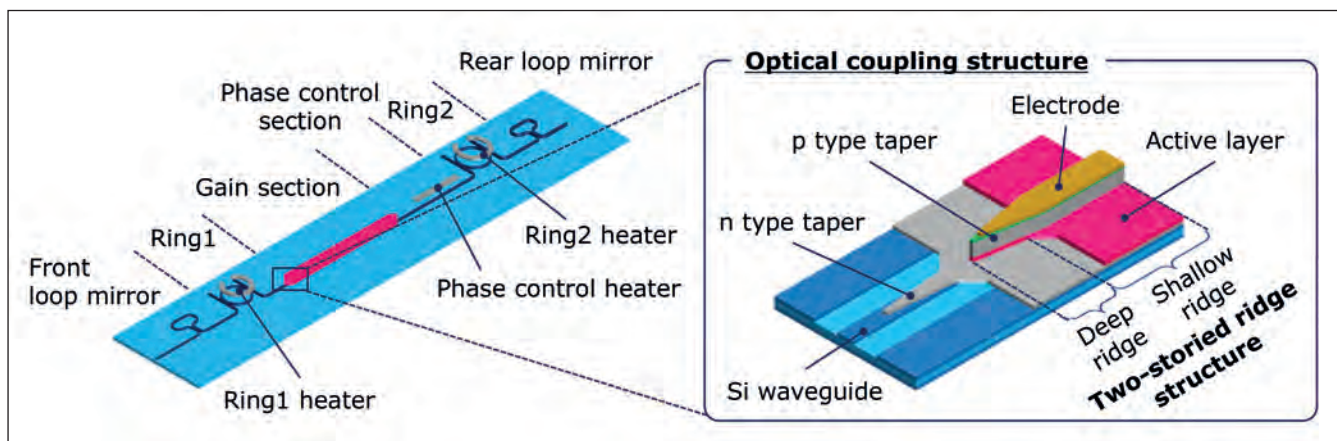
Intel produces its laser by forming a waveguide and a grating on a 300 mm silicon wafer with a silicon-dioxide layer, and then adding an InP chiplet that is subsequently processed (see Figure 1 for details).

To define the laser’s emission wavelength, Intel adjusts the dimensions of the grating. For the 8 channels deployed in the latest generation of technology, there is a 200 GHz spacing, equating to a difference in the grating period between adjacent laser channels of just 0.2 nm. “This is difficult, but something that is achievable with our deep UV-lithography,” remarked Huang.

He and his co-workers have provided a proof-of-concept transmitter. “Only a single indium-phosphide chiplet is used to fabricate all eight lasers, and each laser can be controlled individually,” explained Huang.

An 8-channel transmitter is formed by combining the output from the eight lasers with three stages of multimode interferometer, formed in silicon. This is a relatively easy way to combine eight channels into four, then two, and finally just one. However, it does incur a power penalty of around 3 dB at each stage.

With this approach, the team have fabricated a transmitter with 8 wavelengths spaced apart by $200\text{ GHz} \pm 13\text{ GHz}$, centred at around 1305 nm. Driving each laser sequentially with 80 mA produces lasing peaks with a side-mode suppression ratio (SMSR) of 54 dB and an output power of around 1 mW. “When we turn on all eight laser together, we see a number of side peaks on either side of the eight main



► Figure 2. Sumitomo Electric Industries has developed a laser structure with a two-storied active region and *n*- and *p*-type tapers, introduced to minimise coupling losses. The laser’s emission wavelength is tuned by heating the ring resonators. Reproduced from the paper MP2.1, 27th ISLC. © IEEE.

laser peaks,” explained Huang. This is attributed to four-wave mixing in the silicon waveguide, which quashes the SMSR to 38 dB.

It is worth noting that changes in temperature do not have a devastating impact on the DFB lasers. While there is a red-shift with temperature, all channels move together, according to measurements at temperatures ranging from 22 °C to 62 °C.

Another encouraging result is that the power and channel uniformity are well within those defined in the CW-WDM-MSA standard. This standard stipulates values of ± 50 GHz and ± 1 dB power imbalance.

Enhanced coupling

One of the downsides of hybrid PICs is that there are coupling losses when light transfers from one material system to another. To minimise these losses, a team led by Sumitomo Electric Industries, and including engineers from Tokyo Institute of Technology, has recently developed a novel hybrid-laser architecture. It features a two-storied ridge structure, employing *n*-type and *p*-type tapers to connect a III-V gain section to the silicon waveguide (see Figure 2).

Details relating to the fabrication of this laser, along with measurements demonstrating its wide tuning range, were provided in a presentation by Takuo Hiratani from Sumitomo Electric Industries. He and his co-workers are advocating the use of hybrid integration in data-centre optical interconnects, because they can combine the merits of InP-based lasers, photodetectors and modulators with silicon’s strengths, which include passive waveguides with tight bends and the opportunity for large-scale integration.

The team from Sumitomo unite InP and silicon using wafer-bonding. “High density integration and high alignment tolerances are strong advantages,” argued

Hiratani, who compared this approach to butt-coupling and micro-transfer printing.

Sumitomo’s latest lasers, emitting at around 1.55 μm , are based on an architecture that realises gain within an InP-based section that is positioned in an external cavity laser featuring two silicon ring resonators, a phase-control section and rear-loop mirrors. With this design, controlling the heating of the rings, which have differing dimensions, allows a tuning of the lasing wavelength over 60 nm.

“In this [latest] work we introduced a new optical coupling structure, including a two-storied ridge structure,” explained Hiratani. “This structure enables constriction of the current, plus, by a shallow-ridge-type gain section, a low optical coupling loss, with zero wavelength dependence.” According to simulations, coupling loss at the interfaces is just 0.4 dB across the entire C-band.

To produce their novel laser, Hiratani and co-workers employ electron-beam lithography to prepare silicon waveguides on the silicon-on-insulator wafer. An InP epiwafer, containing the GaInAsP quantum wells, is directly bonded to this patterned surface, before the InP substrate is removed by chemical wet etching. Stepper lithography and dry etching form a shallow ridge structure and the two-step taper structures. To complete fabrication, cladding layers are deposited, electrodes formed by evaporation, and microheaters and anti-reflection coatings added.

By comparing the performance of Fabry-Pérot lasers with and without an optical coupling structure, the team estimated a loss per interface of less than 1 dB. “This low coupling loss is thanks to the two-storied ridge structure,” remarked Huang.

Measurements on the team’s novel laser, which has a 1.1 mm-long III-V gain section and a total device length of 2.5 mm, reveal a threshold current of 32 mA and a

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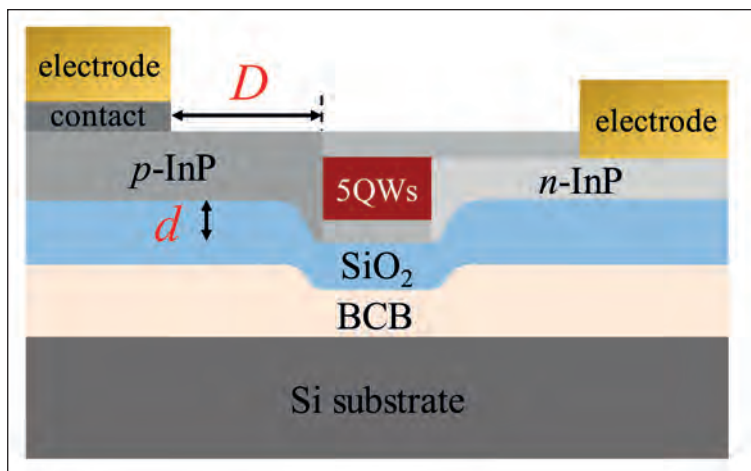
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► Figure 3. The performance of the GaInAsP membrane laser produced by the University of Tokyo is improved by introducing a ridge height, d , and reducing the distance D , which is the separation between the p -type electrode and the active region. Reproduced from the paper MP2.3, 27th ISLC. © IEEE.

maximum output power of 1.3 mW. Kinks appear in the light-output power plot with increases in current, due to mode-hopping associated with phase changes in the gain section. By exploiting the Vernier effect and applying up to 60 mW to the two rings, the laser's wavelength can be tuned over 56.2 nm. Over this range, the SMSR is at least 41 dB. "These results show that the III-V-silicon hybrid tuneable laser is very promising for next-generation PICs," concluded Hiratani.

Masterful membranes

The massive microprocessor chips that are produced today suffer from Joule heating and a delay associated with wiring. A promising solution is to switch from electrical wiring to on-chip optical interconnects. But if this is to succeed, the associated light source must draw incredibly little power, be easily integrated with passive devices using an in-plane platform, and produce enough light for a corresponding detector.

"In order to meet these requirements, we propose a membrane laser light source," explained Naoki Takahashi from Tokyo Institute of Technology, during his talk to delegates at ISLC. He championed this novel form of laser, promoting its strong optical confinement and a high modal gain, realised by essentially replacing an InP cladding with SiO₂ or air. "This leads to a reduction in the threshold current, as well as a higher modulation efficiency."

To place the team's latest success in context, Takahashi began by sharing the results of previous work. In earlier development, he and his co-workers realised a membrane laser with a threshold current of 0.21 mA, a high differential quantum efficiency – it hit 32 percent – and a high differential resistance of 880 Ω. "This makes an energy cost of 93 femtojoules-per-bit when operating at 20 gigabits-per-second. However, it is estimated that an energy cost of

10 femtojoules-per-bit or less is required to realise on-chip optical wiring."

Recently, efforts have been directed at reducing the energy-per-bit by increasing optical lateral confinement through modifications to p -type and n -type structures that surround the active region (see Figure 3). Calculations suggest that changes to the ridge height, d , in this buried-ridge waveguide architecture can lead to a substantial enhancement in lateral optical confinement.

Another approach to improving this key metric, which also trims differential resistance, is to move the p -type electrode closer to the active region. In a conventional structure, such a move would threaten to interfere with the optical mode; but by optimising the ridge height, this is avoided.

Calculations by the team have determined that a judicious choice for their laser's ridge height is 50 nm. This can lead to a 40 percent fall in device resistance. To produce their devices, Takahashi and co-workers begin by growing the p -type cladding, active region and an InP cap on an InP wafer. Using a SiO₂ mask, photolithography and etching they define a ridge-shaped active region, before re-growing p -type and then n -type layers. A SiO₂ layer is grown on top, before this wafer is bonded to a silicon substrate coated with the polymer BCB, and the InP substrate removed and electrodes added.

The benefits of the buried waveguide architecture have been quantified by comparing this device with another that is identical, apart from having a flat structure. Measurements on these devices, which have a 560 μm-long cavity and a 1.8 μm ridge width, reveal that the introduction of the buried ridge reduces the threshold current from 12.5 mA to 9.8 mA and increases the output power. Investigations have also shown that reducing the distance between the electrode and active region from 1.3 μm to 0.8 μm drives down differential resistance by 20 percent.

Takahashi and colleagues have also fabricated a distributed-reflector laser with a buried waveguide that has a width of 1.3 μm. This 1558 nm laser has a threshold current of 0.24 mA and a differential resistance of 430 Ω. "The threshold current was almost the same as the previous work, and the differential resistance was reduced by about half from the previous work," enthused Takahashi, adding that the SMSR is 33 dB. "These results indicate that the introduction of the buried waveguide structure can effectively reduce the power consumption of membrane lasers."

With progress being made by academic and industrial developers on using InP lasers to reach higher data rates without paying a power penalty, there is hope that the internet will not become a major contributor to global warming. And that's clearly good news, given our increasing dependence on what is the virtual world.

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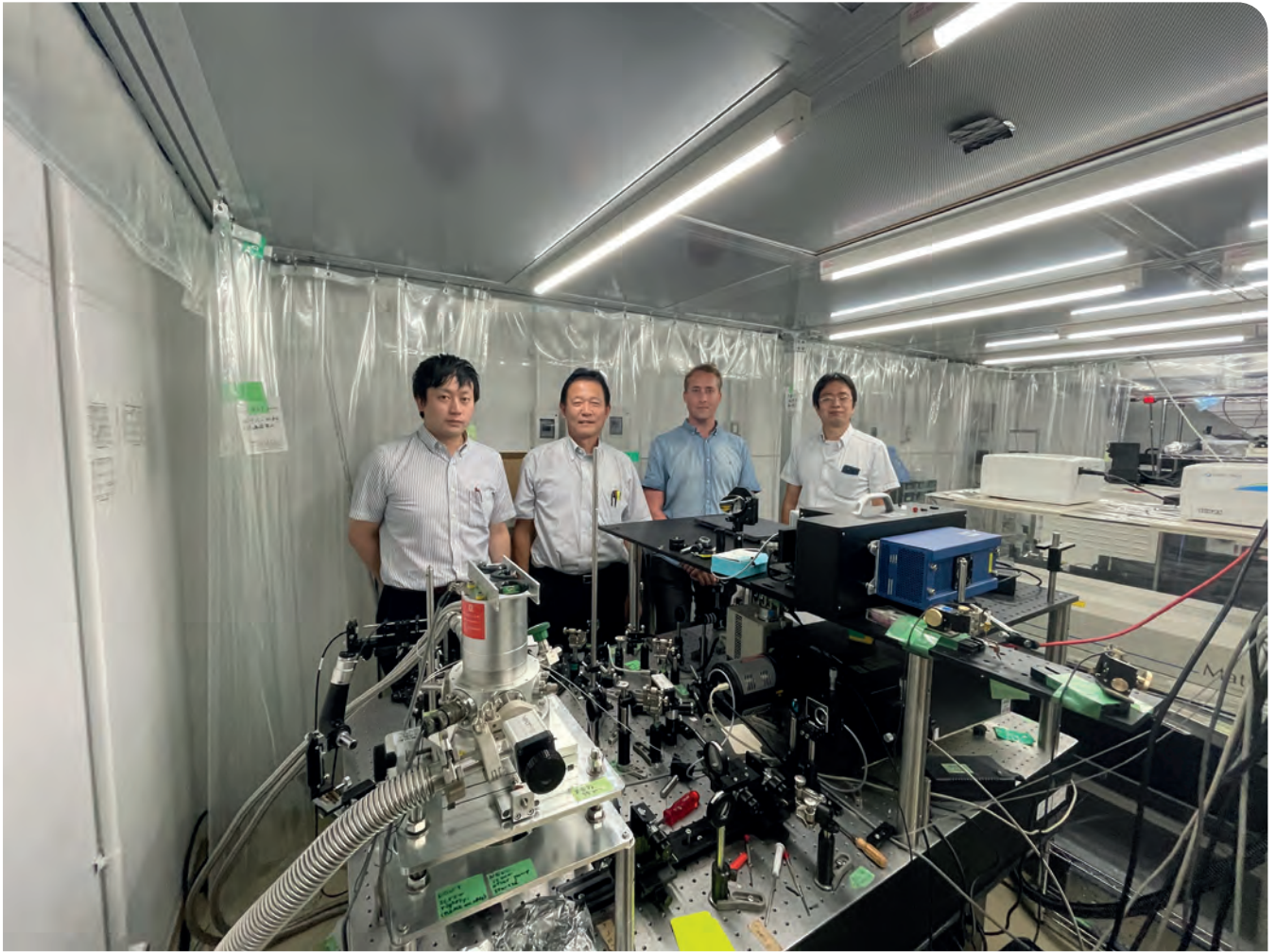


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Realising red GaN-based microLEDs with europium-doping

The novel red luminescence provided by doping GaN with europium ions enables the monolithic integration of nitride-based full-colour LEDs for ultrahigh-resolution microLED displays

**BY SHUHEI ICHIKAWA, DOLF
TIMMERMAN, JUN TATEBAYASHI AND
YASUFUMI FUJIWARA FROM
OSAKA UNIVERSITY**

WE ARE ON THE CUSP of a new era, known as 'Smart society', that will see cyber space and the physical space interactively fused. Critical to this is the introduction of a small-size, high-resolution display, which is an essential ingredient in virtual-reality, augmented-reality and mixed-reality glasses.

One candidate for producing these tiny high-resolution displays is the microLED. Screens formed from a vast array of these miniature LEDs have many virtues, including a high efficiency, high contrast and high stability. Fabrication of this class of display draws together devices emitting each of the three primary colours. A very common combination is the use of InGaN/GaN-based LEDs for the blue and green and AlInGaP/GaAs-based LEDs for the red. These devices are brought together to form pixels using a pick-and-place technique. However, there is a problem: when the dimensions of the LEDs are reduced, the efficiency of the red variant plummets, due to an increase in

surface recombination associated with the hike in the surface-to-volume ratio.

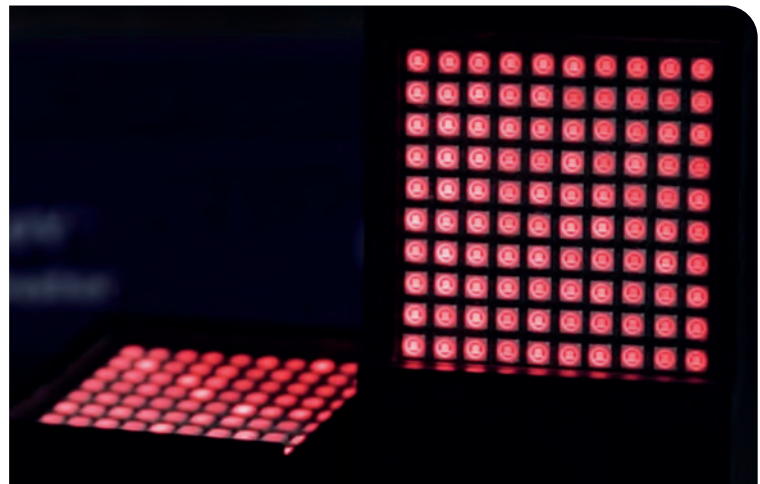
Several solutions are being explored for reducing the dimensions of the red LED while maintaining its efficiency. One option, receiving much attention, is to use GaN-based LEDs emitting in the blue or ultraviolet to pump red-emitting quantum dots or phosphors. However, while this approach also offers monolithic integration, it suffers from insufficient stability and an inadequate colour-conversion efficiency. What's more, with this particular technology, there is a need to increase the pixel contrast ratio and enhance the colour purity by suppressing crosstalk between various light emitters. Unfortunately, when black light-blocking partitions are applied between all the subpixels to accomplish this, the effective area of the pixels diminishes, impairing the number of pixels-per-inch (PPI).

Switching to InGaN nanocolumns avoids this issue. It's an architecture that effectively relaxes material strain, even for the high-indium contents that are necessary for red light emission. But it is challenging to produce nanocolumn structures with a high colour purity – they are held back by large variations in emission wavelength, due to the ensemble nature of these structures and the sensitivity of individual nanocolumns to size fluctuations. Another drawback is the need for electron-beam lithography, prior to epitaxial growth, to precisely control the nanocolumn size and ultimately ensure the desired emission wavelength. Note that for this type of microLED, and also for that based on quantum dots, fabrication requires a lateral integration method.

There is much merit in taking a very different approach, based on the vertical-stacking integration of tri-colour LEDs. Realising this with a single epitaxial sequence eradicates several steps in the microLED production process, such as the mask-patterning prior to growth and the addition of black partitions. What's more, with this technique the areal density of the microLEDs is only limited by lithography and flip-chip accuracy, so it is possible to integrate these emitters with a PPI beyond 5,000.

A pioneer of this approach is the group led by the Nobel-prize winning physicist Hiroshi Amano. Recently his team demonstrated the monolithic integration of tri-colour microLEDs using InGaN quantum wells. These devices, with a 100 μm by 100 μm active area, are composed of independent subpixels, which emit in the blue, green and yellow–orange range and have a colour saturation of over 90 percent. However, there are drawbacks: one concern is that the longer wavelength emission is much broader; and another is that its peak position shifts to shorter wavelengths as

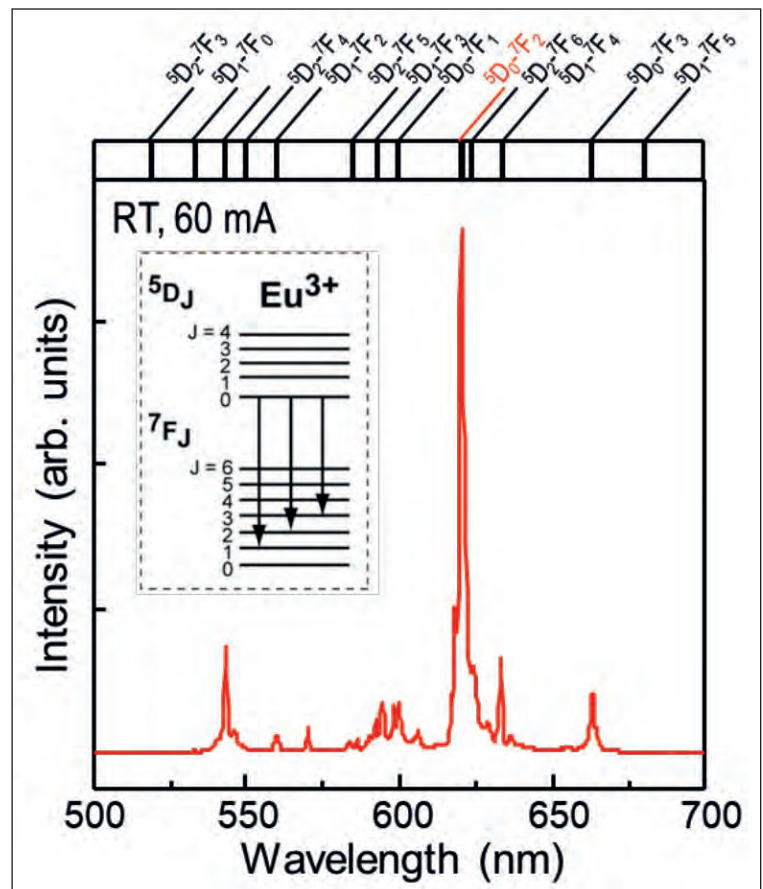
► Figure 2. Eu³⁺ ions doped in GaN under current injection deliver a very sharp emission peak, crucial for a high colour purity.

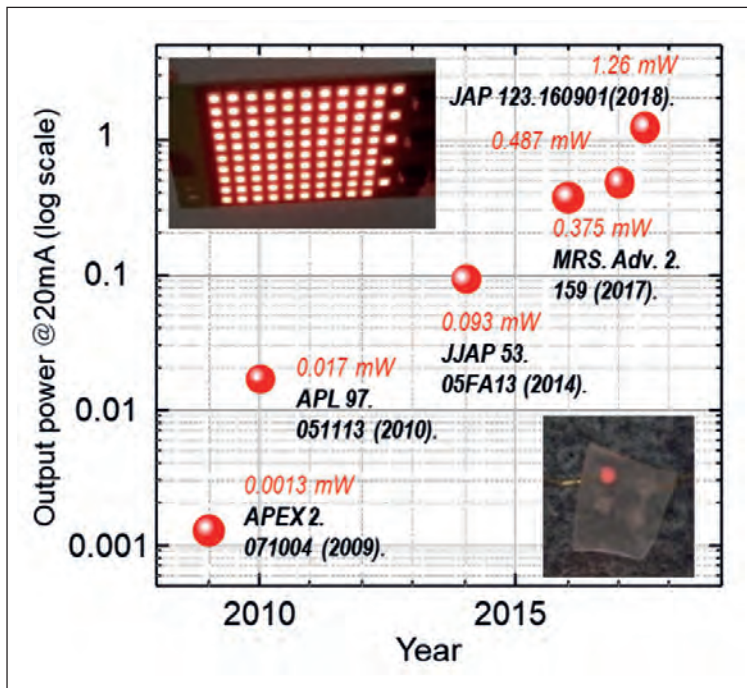


the injected current increases, due to a reduction in the quantum-confined Stark effect.

Our team offers a way to overcome this issue, drawing on our previous success from more than a decade ago. Back in 2009 we invented a novel red LED, formed by adopting europium-doped GaN. In the intervening years we have continued to refine this device, enabling its output power to steadily increase to the milliwatt level. In the remainder of this feature we will detail this triumph, and how we have used vertically-stacked integration to combine it with conventional blue/green LEDs to create a

► Figure 1. Europium-doped GaN LED arrays exhibit bright red luminescence.





► Figure 3. Recent progress of the output power of europium-doped GaN-based LEDs produced at Osaka University.

key technology for the next-generation of microLED displays.

Europium doping

Our approach fulfils the requirement for the vertical-stacking of tri-colour LEDs, which is the monolithic integration of all three colours. We needed to develop an alternative to the more obvious approach of just using InGaN quantum wells, because although blue and green LEDs based on this have been successfully commercialized, a red cousin is lacking. The route to producing red emission with this type of LED is to either increase the indium-content or the thickness of the InGaN quantum well, or to use a combination of the two. But this strategy is precarious: it leads to an increase in piezo-electric polarization fields, and the low miscibility of indium in GaN hampers efforts

to realise a sufficient indium content in the well while maintaining sufficient crystal quality. We are able to sidestep these issues by manipulating the emission through the doping of GaN with an intrinsic red emitter, the rare-earth element europium Eu^{3+} .

The Eu^{3+} ion is no stranger to display applications, having been widely deployed as a luminescent centre in red-emitting phosphors in cathode ray tubes and plasma display panels. In general, rare-earth ions, including Eu^{3+} , are characterized by partially filled 4f shells, which are localized inside completely filled 5s and 5p shells. This localization shields the electrons in the 4f shell from the surrounding environment, allowing rare-earth ions to maintain their atom-like properties and exhibit sharp luminescence bands associated with radiative transitions within the 4f manifold. These transitions are virtually insensitive to changes in current injection and temperature. When Eu^{3+} ions are incorporated into GaN, they take the place of the Ga^{3+} metallic cations and occupy sites with reduced symmetry.

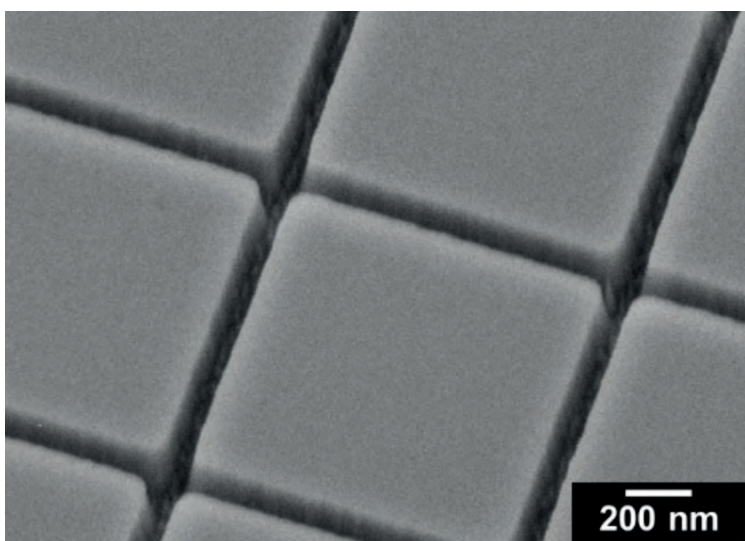
Adding Eu^{3+} ions alters the light-emitting mechanism. Conventional band-to-band transitions are replaced by the transfer of energy from injected carriers in the GaN host material to Eu^{3+} ions, which are promoted to an excited state that leads to the emission of red light. This energy transfer is strongly dependent on the material properties, and can be enhanced by changing the material fabrication processes, or by intentionally introducing other dopants, which can act as energy hubs.

Eu^{3+} ions exhibit a sharp luminescence around 620 nm, due to intra-4f shell transitions from the 5D_0 to 7F_2 states (see Figure 2). This attribute is most welcome, helping to create red-emitting devices with a high colour purity and robust emission wavelength stability. Over the last decade and more, we have developed expertise to epitaxially grow high-quality GaN materials that are doped with Eu^{3+} ions and are optimised to deliver excellent performance in LED structures. The output power of these devices has exponentially increased over time, and has recently exceeded 1 mW at 20 mA, a respectable figure for mass production (see Figure 3).

Maintaining efficiency

To enable immersive experiences in entertainment, education and communication, microdisplays need to come as close as possible to matching the human visual system. For a typical virtual-reality headset, this requirement implies that the spatial resolution needs to be as high as 4600 PPI to match the eye's central field-of-view capabilities. This specification translates to a pixel size of approximately 5 μm , and thus even smaller feature sizes for individual sub-pixels.

When the dimensions of a microLED are reduced to below around 100 μm , the influence of their sidewalls increases, leading to the introduction of non-radiative recombination associated with imperfections induced



► Figure 4. A scanning electron microscopy image of 1 μm -sized mesa.

by the fabrication process. The upshot is a lowering of the internal conversion efficiency. To address this, engineers are turning to new LED structures, modified chip architectures and better processes to diminish the impact of sidewall defects. With these refinements, blue-emitting microLEDs based on InGaN quantum wells can maintain their efficiency when scaled down to a size of just 5 μm .

With red microLEDs, which are typically based on phosphides, it's a different story. The issues associated with scaling are not addressed with the approaches that work for their GaN-based siblings, and their efficiency drops quickly when the pixel size shrinks. These devices are hampered by a combination of long carrier diffusion lengths that allow carriers to reach sidewalls from a larger distance, and the high surface-recombination coefficient.

When switching from red LEDs made from phosphides to those employing europium-doped GaN, the carrier diffusion length plummets to a value even shorter than that found in conventional nitrides. That's because the Eu^{3+} ions are extremely efficient at trapping injected carriers. Diffusion lengths are typically around 100 nm, a distance so small that carriers are prevented from reaching the sidewalls.

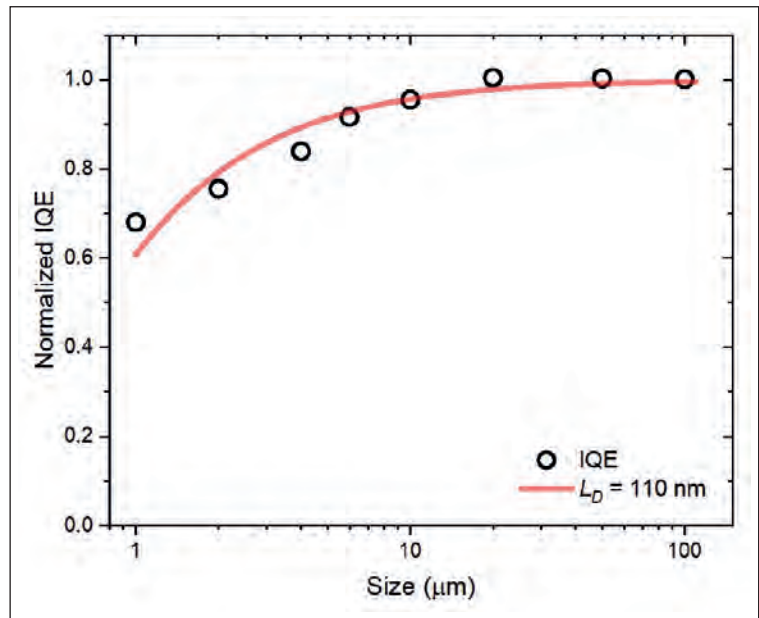
This virtue is at play in our set of square europium-doped structures, with sizes ranging from 1 μm to 100 μm (see Figure 5). We have found that the internal quantum efficiency remains constant down to sizes of 10 μm , and only shows modest decreases at even smaller sizes. For our smallest structure of 1 μm , the internal quantum efficiency is 70 percent of the maximum value. This impressive result is realised without any post-treatment of the sidewalls, so it could be further improved by employing the process optimizations developed for the blue GaN-based LEDs.

Our results underscore the inherent potential of europium-doped GaN as an optically active material, and they provide much encouragement for using this material in microLEDs. The work has provided us with a platform to investigate the performance of microLED structures based on this material. We hope that we can realise high efficiencies in devices as small as 1 μm .

Monolithic integration

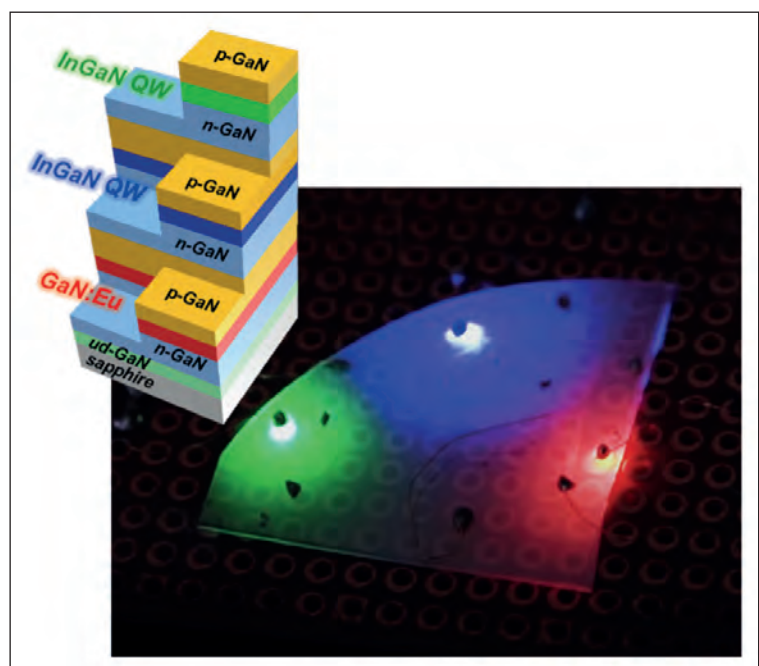
Compared with displays based on conventional liquid crystals and organic LEDs, those employing microLEDs offer an increased pixel density, a higher efficiency and a hike in brightness. However, commercialising this technology in its highest fidelity is not easy, due to complexity in the fabrication of high-resolution full-colour displays that provide a wide colour gamut.

To realize a pixel density beyond 1000 PPI, it is indispensable to employ a growth technique that allows the monolithic integration of the three primary-colour LEDs from the same material system, because

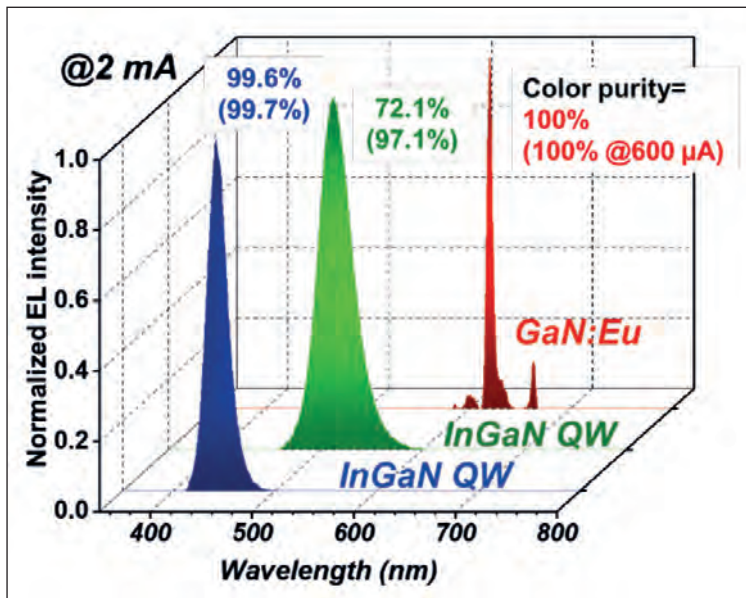


► Figure 5. Normalized internal quantum efficiency as a function of mesa size for europium-doped GaN-based LEDs. The red line indicates the modelled internal quantum efficiency for a 110 nm carrier diffusion length.

this eliminates complications arising from pick-and-place techniques used to transfer ultra-small-sized LED chips. For ultra-high resolutions beyond 4600 PPI, it is also advantageous to adopt a vertical stacking approach for bringing together red, green and blue LEDs, because this minimises gaps between pixels and sub-pixels. Another consideration is to realise a luminance of at least 3,000 cd m^{-2} , as this



► Figure 6. Vertical stacking of red, green and blue LEDs enables a very high pixel density (left). Electroluminescence from monolithically integrated LEDs on the same sapphire substrate under simultaneous operating conditions (right).



► Figure 7. Individual electroluminescence spectra of red, green and blue LEDs obtained at room temperature under 2 mA current injection.

allows displays to be read outdoors, assuming a typical ambient illuminance of 50,000 lux.

Accounting for all these considerations, we have used monolithic integration to produce vertically stacked full-colour LEDs that feature europium-doped GaN and the emission from InGaN quantum wells (see Figure 6). These integrated LEDs were grown by MOCVD on a single sapphire substrate and did not require any additional preparation. It is possible to select all three primary colours from anywhere in the wafer by controlling the etching-depth and position.

The optimal growth temperature for the europium-doped GaN layer is 960 °C – this is higher than that used for the InGaN quantum wells, which are grown at temperatures between 650 °C and 800 °C.

The europium-doped layer is thermally stable at the temperature employed for its growth, and is better suited for stacked-type integration of red, green and blue devices than InGaN-based red LEDs, which suffer from indium desorption. This desorption is accelerated by temperatures used for the growth of the InGaN layers used in subsequent LEDs.

Room-temperature electroluminescence spectra of our individual devices show a high colour purity. This

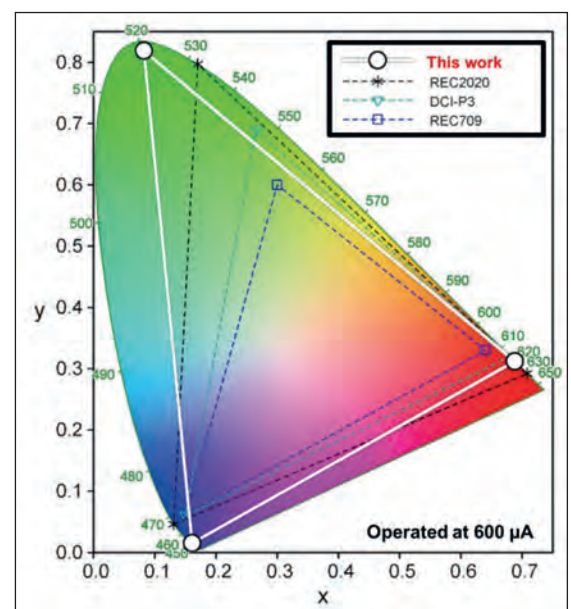
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is valued, as it improves the capability for displays to generate reproducible colours. Driven with a 600 μA injection current, the maximum colour purity for the red, green, and blue emission are 100 percent, 97.1 percent, and 99.7 percent, respectively (these figures are 100 percent, 72.1 percent, and 99.6 percent, respectively, at 2 mA operation). These results demonstrate the extremely high colour purity of europium-doped GaN LEDs under any current injection, due to the stable intra-4f shell transitions in the Eu³⁺ ions.

The most common approach to evaluating the reproducibility of colours of displays is to consider the space on the *International Commission on Illumination* (CIE) chromaticity diagram (see Figure 8). Using this metric – and the colour purity efficiencies for our red, green and blue LEDs – indicates that this combination of emitters provides an exceptionally large coverage. According to the Rec.2020 standard, our devices provide 105.5 percent of the area with 91.2 percent coverage; and for the DCI-P3 standard, the corresponding values are 147.0 percent and 96.5 percent, respectively. Crucially, these figures show that our devices fulfil the colour gamut requirement for the *Ultra HD Premium TV* standard. What’s more, they produce a maximum luminance of around 3100 cd m⁻², so they satisfy the minimum requirement for outdoor applications.

These results show that our technology has a great deal of promise. By adding europium doping to the microLED to aid monolithic integration, we are paving the way for displays with a very high PPI and great colour quality that can serve in virtual-reality, augmented-reality and mixed-reality glasses.

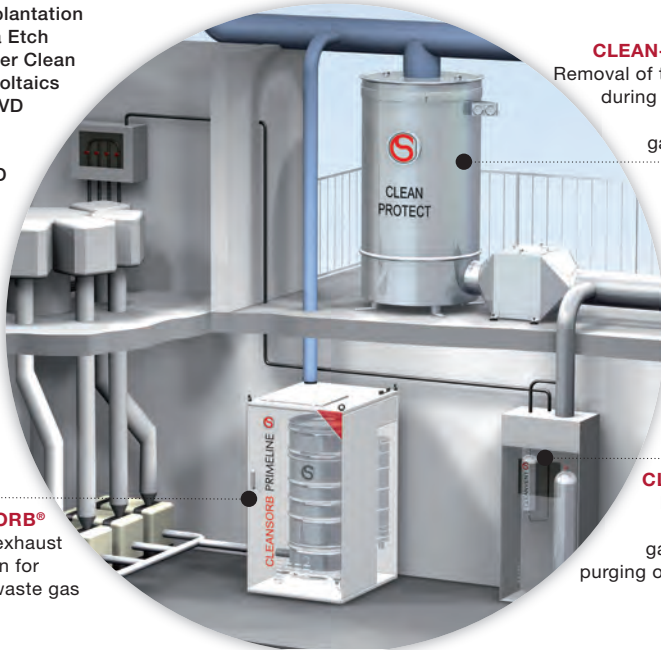


► Figure 8. The emission colour gamut of red, green and blue LEDs on the CIE chromaticity diagram under 600 μA current injection.



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Cranking up the growth temperature of red InGaN LEDs

Intentional decomposition of an InGaN layer provides a foundation for high-temperature growth of red-emitting quantum wells

RESEARCHERS at the University of California, Santa Barbara (UCSB), claim to have broken new ground by increasing the temperature employed for the growth of red-emitting InGaN LEDs. This breakthrough comes from introducing a relaxed InGaN buffer.

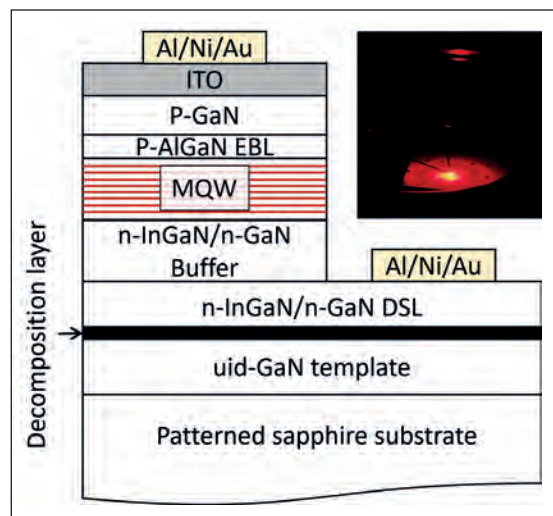
The approach by the West-coast team differs from the norm, which is to grow re-emitting InGaN-based LEDs at a considerably lower temperatures than their green and blue siblings. While growth at a lower temperature enables the higher indium content in the quantum wells required for emission in this spectral domain, it has a major downside: it applies the brakes to adatom mobility, and ultimately drags down efficiency, due to a hike in the defect density and degradation of surface morphology.

The promise of a higher efficiency that stems from a higher growth temperature will be welcomed by developers of displays based on microLEDs. Although AlInGaP LEDs delivers a very high level of efficiency when they have dimensions that are hundreds of microns or more, performance nosedives when scaling, due to the long minority carrier diffusion length. Fortunately, this is not an issue for nitride-based LEDs, due to their reduced surface recombination velocity.

One of the difficulties associated with the fabrication of red-emitting nitride LEDs is the large lattice mismatch between InGaN and GaN. As well as inducing misfit dislocations, the strain that stems from this mismatch reduces indium incorporation through a mechanism known as compositional pulling.

To combat this pulling effect, relaxed InGaN buffers can be introduced that reduce strain and enable higher growth temperatures. Previous work at UCSB has formed such a buffer via an electrochemical etch that porosifies a GaN underlayer. However, according to Philip Chan, spokesman for the latest work, that approach has several weaknesses: it requires complicated processing, it only ensures partial relaxation of the buffer, and it leads to a substantial reduction in the usable area of the substrate.

Chan and co-workers have developed an alternative approach to realising a relaxed buffer, involving intentional thermal decomposition of an InGaN layer.



► The decomposition stop layer provides a relaxed template for growing a red-emitting LEDs at high temperatures. The inset shows a device operating at 100 A cm².

The team's device fabrication began by growing a 3 nm-thick InGaN decomposition layer at 720 °C. Growth of a 4 nm-thick GaN layer at that temperature followed, before cranking the chamber up to 930 °C and adding a decomposition stop layer, comprising five periods of 18 nm-thick *n*-type InGaN and 2 nm-thick *n*-type GaN. During this high-temperature growth the high-indium-content decomposition layer decomposed to form voids, allowing the decomposition stop layer to relax and form a template for the LED. On this relaxed platform the team added an InGaN buffer that relaxed, thanks to the compliant decomposition layer, followed by the device (see figure).

On-wafer testing revealed a shift in the peak wavelength of the LED from 770 nm to 660 nm when increasing current density from 5 A cm⁻² to 50 A cm⁻². Chan described the magnitude of this shift as "pretty standard", attributing it to mainly polarization field screening of the carriers. "Careful control of the doping profile can help to screen this field. But, in general, the commercial viability of red InGaN microLEDs remains to be seen."

Another concern is the width of the spectral peak. It has a full-width at half-maximum of 69 nm, a value that is not viable for a display, according to Chan. Poor current spreading on the *n*-side is partly to blame, and should be easy to fix in future devices.

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Two-photon spectroscopy exposes defects in multi-junction cells

Imaging by two-photon excitation provides a non-destructive method for identifying threading dislocations within inverted metamorphic solar cells

A JAPANESE collaboration has shown that two-photon excitation spectroscopy is a powerful technique for exposing threading dislocations in the graded buffer layers of inverted metamorphic solar cells.

In inverted metamorphic solar cells, including the record-breaking six-junction cell produced by NREL that has an efficiency of 47.1 percent, threading dislocations form during the strain relaxation of heteroepitaxially grown layers, potentially degrading the device's electrical characteristics.

Options for minimising the creation of these damaging dislocations are to use of a slightly mis-cut substrate and to introduce an InGaP superlattice – both control misfit dislocation glide-planes in the buffer layers. However, controlling these glide planes is not easy, leading to variations in the efficiency of solar cells produced from a single wafer.

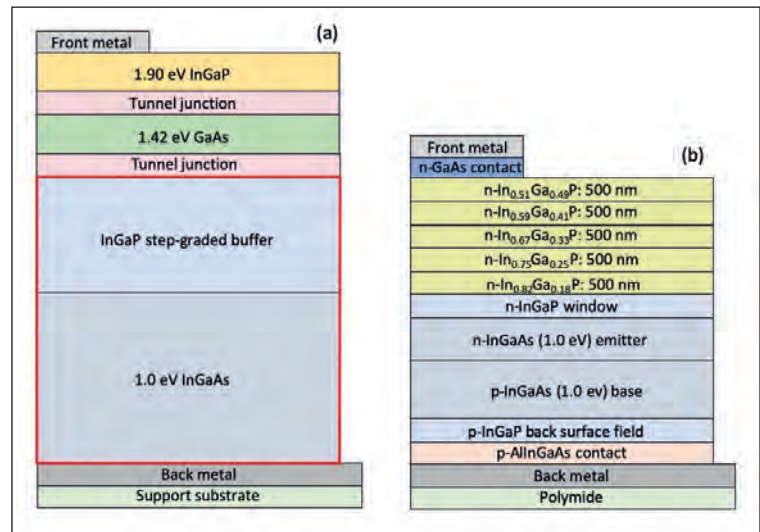
Reducing the threading dislocation density across these epiwafers would increase efficiencies. According to a study reported back in 1985, there is a practical upper limit for the threading dislocation density in this material system of 10^5 cm^{-2} .

Two established techniques for evaluating the threading dislocation density in graded buffers are electron-beam-induced current and cathodoluminescence measurements. However, both lead to simultaneous excitation of several buffer layers, hampering efforts to pinpoint the location of the threading dislocations.

Addressing this weakness is the two-photon excitation spectroscopy approach employed by the Japanese team, which is a partnership between researchers at the Japan Aerospace Exploration Agency, Osaka University, Sharp Corporation, and the National Institute of Advanced Industrial Science and Technology.

The optical technique they employ has previously been used by another team to expose threading dislocations in bulk GaN. In that work, researchers constructed a three-dimensional map of the dislocations by scanning the focus of the excitation light through the sample.

It is challenging to apply this approach to inverted metamorphic multi-junction solar cells, because the high refractive indices of the materials elongates the focal spot in the depth direction. However, by selecting an appropriate detection wavelength, corresponding to the bandgap of the layer under investigation, it is possible to image thin layers.



The Japanese collaboration has used a Nikon A1MP two-photon excitation microscopy system to investigate three samples: a triple-junction inverted metamorphic cell based on InGaP, GaAs and InGaAs; and a pair of single-junction InGaAs cells with different open-circuit voltages (see figure for details).

Imaging the surface, using detection below 650 nm, revealed an absence of threading dislocations in the top InGaP layer of the triple-junction cell. Meanwhile, imaging 7 μm -deep into this sample uncovered many dark spots and lines, corresponding to threading and misfit dislocations that act as non-radiative recombination centres.

Employing detection above 750 nm enabled determination of the density of nonradiative recombination centres in the buffer layer next to the active layer of the single-junction cells. The team recorded a density of dark spots of $7 \times 10^6 \text{ cm}^{-2}$ in the sample with the lower open-circuit voltage, compared with $3.3 \times 10^6 \text{ cm}^{-2}$ in the better-performing device.

Turning to X-ray diffraction, the researchers found that the distribution of preferential glide planes has a higher degree of homogeneity in the sample with a higher open-circuit voltage. This result highlights the strength that comes from combining two-photon excitation microscopy with X-ray diffraction.

➤ Two-photon excitation spectroscopy can identify threading dislocations in the graded buffer layers of inverted triple-junction (a) and single-junction (b) metamorphic solar cells. The combination of the step-graded buffer and InGaAs junction in the single-junction cell is similar to the structure surrounded by the red rectangle.

REFERENCE

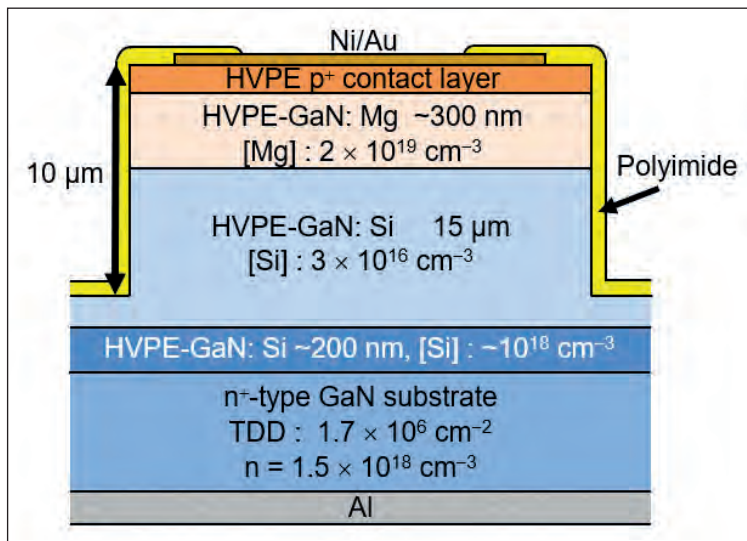
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HVPE yields vertical GaN *p-n* diodes

A new approach for magnesium-doping enables the continuous growth of vertical GaN *p-n* diodes by HVPE

ENGINEERS at Nagoya University, Japan, are claiming to have produced the first GaN *p-n* diodes by HVPE, a technique that combines very high-growth rates with carbon-free sources.

Spokesman for the team, Kazuki Ohnishi, says that this work could cut production costs for vertical GaN power devices, due to the switch from MOCVD to HVPE. "According to our estimates, manufacturing 400 million 6-inch epiwafers will cost \$530 billion with MOCVD, but can be reduced to \$76 billion with HVPE."



► The use of HVPE improved the performance of the *p-n* vertical GaN diode by eliminating the silicon accumulation layer at the interface that occurs with a hybrid growth method. A polyimide layer provides passivation.

At present, companies ordering HVPE reactors are offered bespoke tools, primarily for research. However, if demand rises, due to greater interest in this growth technique, it could drive the development of reactors for high-volume production.

It is also possible to produce GaN *p-n* diodes by growing the *n*-type region by HVPE, followed by the *p*-type layers by MOCVD. However, the downside of that hybrid approach is that it tends to create silicon impurities at the interface – and they result in poor electrical properties for the diode. By employing continuous HVPE growth, Ohnishi and co-workers avoid creating silicon-accumulating layers at the *p⁺-n* interface.

The team from Nagoya produced its devices on a free-standing, HVPE-grown GaN substrate with a threading dislocation density of $1.7 \times 10^6 \text{ cm}^{-2}$ and a carrier

concentration of $1.5 \times 10^{18} \text{ cm}^{-3}$. On this foundation they first deposited, by HVPE, a pair of silicon-doped *n*-type layers – initially a 200 nm-thick *n⁺* layer, and then a 15 μm-thick *n*-type layer, grown at 30 μm/hour, with a silicon concentration of $3 \times 10^{16} \text{ cm}^{-3}$. For the *p*-side they added a 300 nm-thick GaN layer with a magnesium doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$, and a 20 nm-thick GaN contact layer, heavily doped with magnesium.

Crucial to the team's pioneering of HVPE growth of vertical GaN *p-n* diodes has been the development of a new approach to magnesium doping. As far back as the 1970s, researchers had realised *p*-doping in HVPE-grown films using magnesium. However, the high equilibrium vapour pressure of the metal source hampered control of the doping level.

Ohnishi and colleagues have addressed this weakness by switching the magnesium source to MgO, which has a very low equilibrium vapour pressure and a melting point of 2800 °C. The new process involves supplying HCl gas to heated MgO. A reaction results in MgCl_2 , a precursor for the growth process. One concern with this approach is that MgO could introduce oxygen impurities. However, this does not appear to be an issue, according to Ohnishi: "Fortunately, the oxygen concentration is suppressed, even if magnesium oxide is used. This mechanism is under investigation, but we consider that *c*-plane growth is effective for oxygen suppression."

He and his co-workers formed diodes from the epiwafers by: using reactive-ion etching to define 340 μm-diameter mesas that are 10 μm high; activating magnesium acceptors, by annealing samples in nitrogen at 700 °C for 5 minutes; and adding a Ni/Au anode and an aluminium cathode to the *p⁺* contact layer and the back of the substrate, respectively.

Secondary-ion mass spectrometry revealed a sharp increase in the concentration of magnesium from $5 \times 10^{15} \text{ cm}^{-3}$ in the *n*-type GaN drift layer to $1.9 \times 10^{19} \text{ cm}^{-3}$ in the *p*-type layer beside the *p-n* interface. This indicates that HVPE is capable of producing a steep *p⁺-n* interface.

Current-voltage plots for the device revealed an ideality factor of 1.6, which is lower than that for *p-n* diodes formed by a combination of MOCVD and HVPE, due to the suppression of silicon at the interface.

Ohnishi and colleagues are now planning to use HVPE to fabricate other vertical devices, such as MOSFETs. "In addition, we are interested in the HEMT."

REFERENCE

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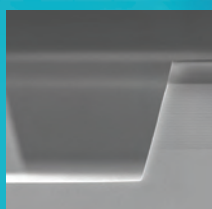
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