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Field-emission transistors

III-Nitride field-emission vacuum transistors unlock the door to compact circuits delivering high powers at high frequencies

Chiral light from topological LEDs

Strong magnetic fields during crystal growth enable LEDs to transfer chirality from electrons to photons

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Makers of SiC power devices produce better transistors when they adopt infrared spectroscopy and picosecond ultrasonics

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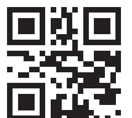

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VIEWPOINT

By Richard Stevenson, Editor

GaN's next killer application

MANY compound semiconductors can barely boast of one killer application. GaN, though, already counts four, and more will surely follow.

For this particular material, the first three killer apps were associated with the LED. Backlighting the keypads and screens of mobiles spawned the first of the multi-billion-dollar markets, with similar levels of success following from the backlighting of a variety of screens, and then the dominance of the light bulb. In all these markets, manufacturers that pushed the performance boundaries got their first, and were rewarded with high margins. But as time went on and more chipmakers fulfilled the specifications, competition squeezed prices, ultimately leading to commoditisation.

It's a similar story for GaN transistors in fast chargers, the first killer app for this material in power electronics. As well as generating revenue, success in this market has provided a great opportunity for promoting the strengths of this GaN power transistor far beyond its pioneers. However, competition is now fierce, with little profit to be made. Illustrating just how entrenched this form of transistor is in fast charging, it's now even deployed in hybrid toys and chargers, such as those launched this summer by GravaStar to coincide with a world-wide release of the movie *Transformers: Rise of the Beasts*.

So where will the next killer applications for GaN come from? It's hard to predict, but there are a few leading contenders. On the optoelectronics side are displays based on the microLED, which are sure to feature GaN emitters; and in the power arena, GaN is tipped to win substantial business in the growing market for electric vehicles, and possibly in inverters supporting the distribution of energy from renewables.

Interest in microLEDs has been strong for quite a few years, but commercialisation, at least on a large scale, is still some way off. What's needed is the development of simpler manufacturing processes that don't compromise

yield. Offering promise on that front is the three-in-one microLED that's being pioneered by engineers at Toyoda Gosei. Development of this device has involved the growth of a GaN-based epitaxial stack on sapphire that features quantum wells emitting in the red, green and blue (see p. 52). Through a combination of etching and localisation of carriers, that team has realised red, green and blue emission, and ultimately a wide colour gamut. However, the efficiency of the red and blue emission is a concern – increasing this in the blue should be possible by improving the etching process, but the pathway for a higher efficiency in the red is far from clear.

For the makers of GaN power devices, the upcoming opportunities involve more strenuous operating conditions than those required for fast chargers, such as higher powers and more varied operating temperatures. To fulfil these requirements, Navitas has launched a new range of GaN ICs, known as GaNSafe, discussed in an interview starting on page 14. Will it spawn another killer app for GaN? Who knows, so stay tuned to find out about its future, along with that of the microLED.

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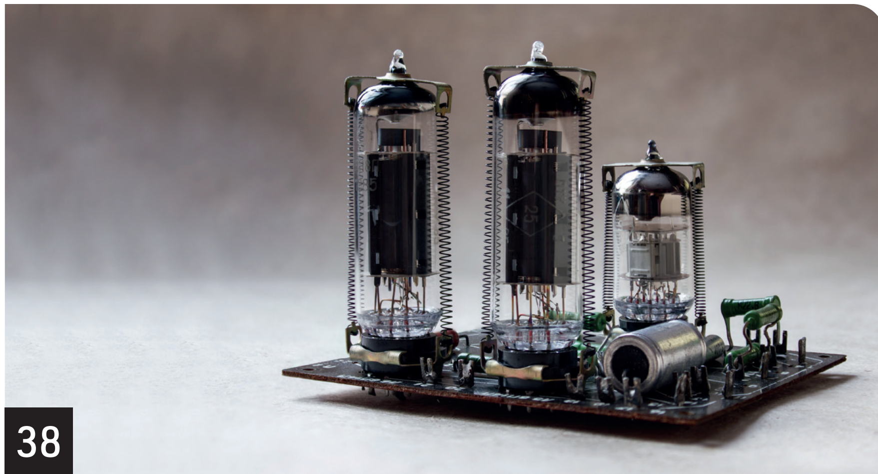

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Steady growth for power electronics

Total power electronics market expected to grow to $33.3 billion by 2028, according to Yole

RENEWABLES, increased efficiency, and government regulations for different segments will driving steady growth of around 8 percent for power electronics over the next five years, according to Yole Intelligence's annual power electronics report, Status of the Power Electronics Industry 2023.

In 2022, the total power electronics market was worth $20.9 billion, including discretes and modules. Yole expects it to grow to $33.3 billion by 2028.

Worth $14.3 billion in 2022, the discrete market is expected to reach $18.5 billion by 2028. The main applications driving this growth are xEV , DC charging infrastructure, and automotive. Consumer remains the largest market for discrete devices even if it is in decline.

In parallel, the module market is pushed by xEV and renewables applications. It includes both photovoltaic and wind. According to Yole Intelligence, this market should reach $14.8 billion by 2028.

The top three companies remain the same as the previous year: Infineon Technologies, Onsemi, and STMicroelectronics, who show significant SiC revenue boosts.

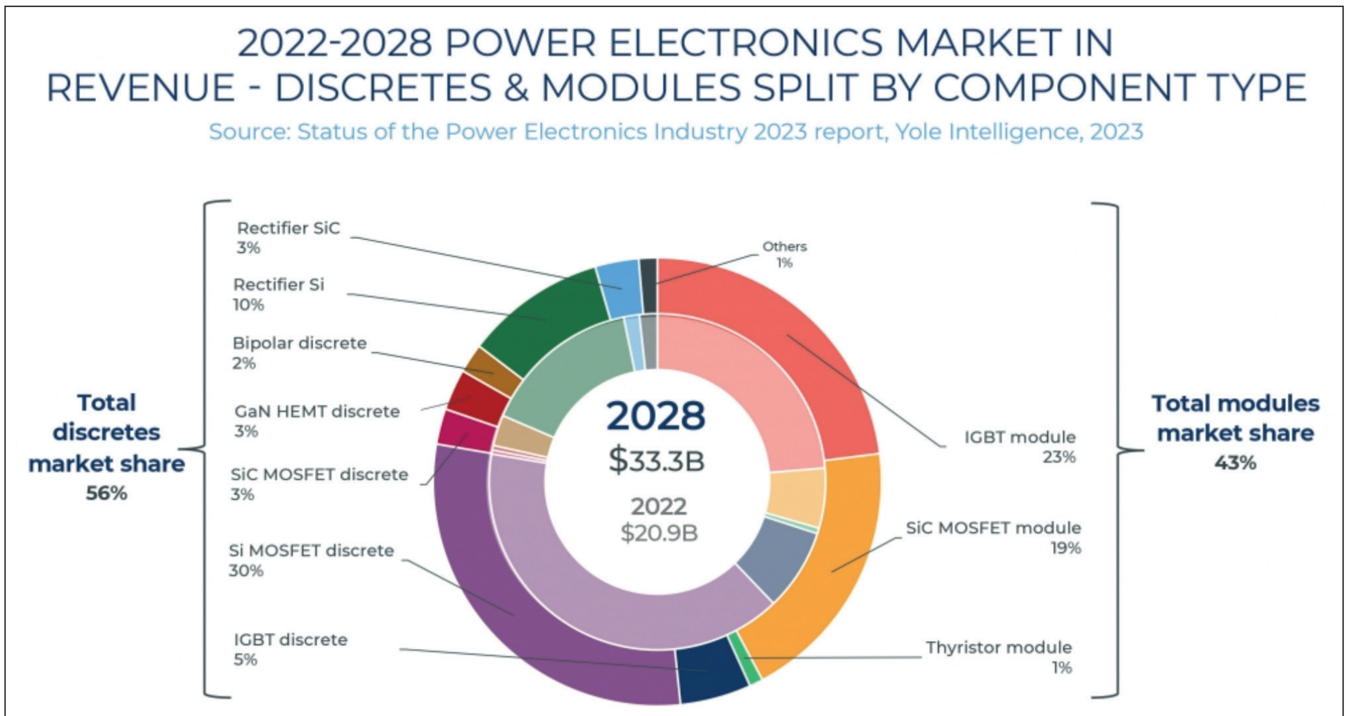
Ana Villamor, team lead analyst, power electronics at Yole Intelligence said: "The power device market is split into three different materials: silicon, SiC, and GaN. Without doubt, silicon is the major part of this market, though SiC is gaining momentum. At Yole Intelligence, we see the growing demand for modules for xEV. In parallel, GaN's main application will continue to be consumer power supplies."

In the long term, total wafer production is increasing alongside the growing power electronic device demand from renewables, automotive and industrial applications. To meet this demand, silicon wafers for power applications will grow to about 47 million 8-inch equivalent wafers per year. Meanwhile, wafer players are focusing on 12-inch. SiC's transition to 8-inch is taking place, and in the coming years, this will take a greater share of the market.

Today, China is the largest buyer of power components, followed by Asia/Pacific and Europe. New growth areas, previously less active in semiconductor manufacturing, are found where major companies are investing to supply Asia, other than China, such as Malaysia, Vietnam, and Singapore.

At the device level, the top manufacturers are pushing the three different device technologies: silicon, GaN, and SiC. "We have noticed that a few players pushing GaN have stepped back on R&D to wait for a market increase before investing further, such as Onsemi and Alpha and Omega," adds Villamor .

From the manufacturing side, China remains the leader in investments for manufacturing expansion in 300 mm, as well as in 200 mm and 150 mm.



£300k award for Quinas ULTRARAM

Lancaster University spinout gets funding to commercialise compound semiconductor memory

LANCASTER UNIVERSITY spinout company Quinas Technology has been awarded £300,000 from Innovate UK to commercialise the universal compound semiconductor-based computer memory ULTRARAM.

ULTRARAM is described as combining the best properties of DRAM and flash into a single device. It is fast, non-volatile, has high endurance and is orders of magnitude more energy efficient than other memory technologies. It achieves these properties by harnessing a quantum mechanical process called resonant tunnelling.

In a paper ULTRARAM: *A low-energy, high-endurance, compound semiconductor memory on silicon*, published in *Advanced Electronic Materials* (2022), the team described implementing ULTRARAM on a silicon substrate; a vital step toward cost-effective mass production.

The ULTRARAM outlined in this paper uses InAs quantum wells and AlSb barriers to create a triple-barrier resonant-tunnelling structure. The 2.1 eV conduction band offset of AlSb with respect to the InAs that forms the floating gate and channel provides a barrier to the passage of electrons that is comparable to the SiO_2 dielectric used in flash memory. However, inclusion of two InAs quantum wells (of different thicknesses) ensures transparency to electrons when a low voltage (around 2.5 V) is applied, due to resonant tunnelling.

By using the triple-barrier resonant-tunnelling heterostructure as the barrier between floating gate and channel, rather than the usual monolithic material, the paper authors say that a charge-based memory with extraordinary properties can be achieved. The memories showed clear 0/1 logic-state contrast after around no more than 10 ms duration program/erase pulses of about 2.5 V.

Furthermore, the Quinas team found that the combination of low voltage and small device capacitance per unit area resulted in a switching energy orders of magnitude lower than DRAM and flash, for a given cell size.

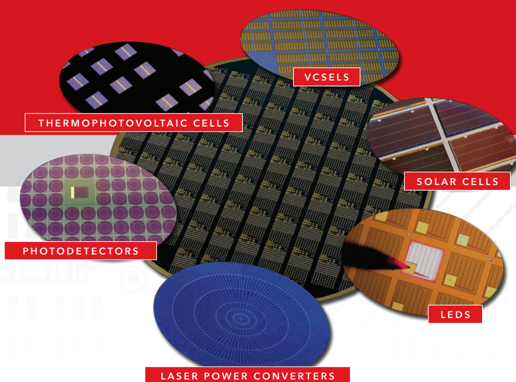
Extended testing of the devices revealed retention in excess of 1000 years and degradation-free endurance of over 10^7 program/erase cycles, surpassing recent results for similar devices on GaAs substrates.

The inventor of ULTRARAM is Manus Hayne, professor of the Physics Department at Lancaster University and chief scientific officer at Quinas.

He said: “This is a significant first step for a newly formed company and has fired the starting gun in the race to commercialise ULTRARAM, but it will be a marathon, not a sprint. We look forward to tackling the challenges that lie ahead.”

The award from the UK’s national innovation agency follows the completion of the intensive and highly competitive ICURe programme, which is designed to validate the commercial viability of leading-edge science and aid spinout formation.

Quinas’ CTO, Peter Hodgson, who led the ICURe submission, said: “The funding will allow us to demonstrate the performance of the memory devices at near-state-of-the-art feature sizes and help secure the significant investment required to bring a new technology to market.”



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Denso and Mitsubishi invest $1 billion in Coherent's SiC business

Coherent to operate the business as an independent subsidiary

COHERENT has announced that Denso and Mitsubishi Electric have agreed to invest an aggregate $1 billion ($500 million each) in its SiC business.

The investment will be in exchange for a 12.5 percent non-controlling ownership interest, with Coherent owning the remaining 75 percent. Prior to the completion of the transaction, Coherent will separate and contribute the business to a subsidiary, which will continue to be led by Sohail Khan, Coherent's executive VP, Wide-Bandgap Electronics Technologies.

This SiC subsidiary will enter into long-term supply arrangements with Denso and Mitsubishi Electric that support their demand for 150 mm and 200 mm SiC substrates and epitaxial wafers.

"We are excited to expand our strategic relationships with Denso and Mitsubishi Electric to capitalise on the significant demand for SiC," said Vincent Mattera, Jr., Chair and CEO, Coherent.

Mattera added, "After a thorough review of strategic alternatives for our SiC business, we determined that the creation of a separate subsidiary and the strategic investments from Denso and Mitsubishi Electric, two leaders in SiC power devices and modules, is the best path forward to maximise shareholder value and position the business for long-term growth."

According to Mattera, the investments from the strategic partners will be used to accelerate Coherent's capacity expansion plans and help sustain its leadership position, while ensuring the development of a robust and scalable supply for the rapidly growing market for SiC-based power electronics, largely driven by the explosive growth of the global electric vehicle market.

"We are very pleased to establish a strategic relationship with Coherent, which has a world-class track record in SiC wafer manufacturing. Through this investment, we will secure a stable procurement of SiC wafers, which are critical for BEVs, and contribute to the realisation of a carbon-neutral society by promoting the widespread adoption of BEVs," said Shinnosuke Hayashi, president and COO of Denso.

Masayoshi Takemi, executive officer, group president, Semiconductor & Device of Mitsubishi Electric, said: "Demand for SiC power semiconductors is expected to grow exponentially as the global market for electric vehicles increases in line with the transition to a decarbonised world. To capitalise on this trend, we have decided to expand our SiC power semiconductor production capacity, including by constructing a 200 mm wafer plant in the Shisui area of Kumamoto Prefecture."

"We are delighted to strengthen our partnership with Coherent by investing in this new SiC company, which will provide us with a stable supply of high-quality SiC substrates essential for our increased supply capacity," added Takemi.

Indian team makes home-grown GaN power switch

RESEARCHERS at the Indian Institute of Science (IISc) have developed a home-grown GaN power switch that can have potential applications in systems like power converters for electric vehicles and laptops, as well as in wireless communications. The entire process of building the switch – from material growth to device fabrication to packaging – was developed in-house at the Centre for Nano Science and Engineering (CeNSE), IISc.

"It is a very promising and disruptive technology," says Digbijoy Nath, associate professor at CeNSE and corresponding author of the study published in *Microelectronic Engineering*. "But the material and devices are heavily import-restricted. We don't have GaN wafer production capability at commercial scale in India yet." The know-how of manufacturing these devices is also a heavily-guarded secret with few studies published on the details of the processes involved, he adds.

To design the GaN power switch, the IISc team used a MOCVD technique developed and optimised over a decade by researchers in the lab of Srinivasan Raghavan, professor and chair, CeNSE.

GaN transistors typically operate in depletion mode – they are on all the time unless a negative voltage is applied to turn them off. But power switches used in chargers and adapters need to work the other way around.

To achieve this operation, the team combined the GaN transistor with a commercially available silicon transistor to keep the device normally off.

"The packaging of the device was also indigenously developed," explains Rijo Baby, PhD student at CeNSE and first author of the study. After packaging and testing, the team found the device performance to be comparable to state-of-the-art switches available commercially, with a switching time of about 50 nanoseconds between on and off operations.

Going forward, the researchers plan on scaling up the device dimensions so that it can operate at high currents. They also plan to design a power converter that can step up or step down voltages.

Yuanjie Semiconductor to supply lasers to POET

Collaboration will enable POET's joint venture, Super Photonics Xiamen, to ramp optical engines to high-volume

Canadian PIC company POET Technologies has announced that it is collaborating with Yuanjie Semiconductor Technology (YST), a Chinese supplier of lasers.

The partnership will enable POET's joint venture, Super Photonics Xiamen (SPX), to ramp optical engines to high-volume production using YST's lasers.

POET, SPX and YST will initially collaborate on 100G CWDM4, POET ONE, 100G LR4 and 200G FR4 transmitter products. All the design verifications and reliability testing of the optical engines is complete and all will be released to production this month.

Current module customers for these products include ADVA, Beijing FeiYunYi and Fibertop, along with others whose names have not yet been disclosed.

"As we start ramping production of our optical engines, securing an additional reliable laser source that is well established in the industry with known good quality is of utmost importance to our business," said Suresh Venkatesan, chairman and CEO of POET.

He added: "Our partnership with YST has enabled POET and SPX to deliver reliable, high-performance optical engines to customers. SPX will start production of 100G CWDM4, POET ONE (a 100G single chip TxRx engine), 100G LR4 and 200G FR4 optical engines using YST's directly modulated lasers this month and we expect to extend the collaboration to other products in the future."

Peter Zhang, CEO and chairman of the board at YST said. "Our superior quality lasers and reputation for reliability will complement POET's Optical Interposer technology, which offers a unique and highly adaptable platform to module makers." Zhang added: "We will continue to collaborate with POET on high-speed optical engines while supporting SPX to ramp current products to high volume production."

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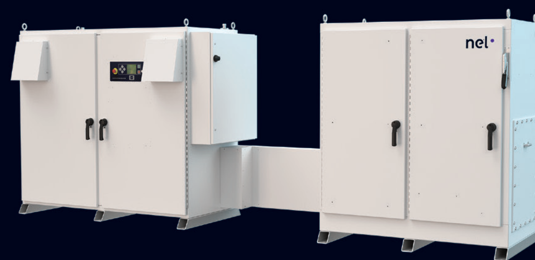

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Germany commits to Ams Osram funding

Intention to provide IPCEI funding to drive next-generation optoelectronic semiconductor technologies

AMS OSRAM will get substantial public funding from the German federal government and the Free State of Bavaria to boost the further development of semiconductor technology. The envisaged IPCEI funding (Important Project of Common European Interest) will support Ams Osram in making its own investments in the research and development of optoelectronic components at its Regensburg location.

The subsidy is thought to be more than €300 million, which will be mainly invested in activities for the research and development of optoelectronic semiconductors and their manufacturing processes, creating 400 new high-tech jobs. In addition, Ams Osram will invest in new clean room and laboratory facilities for research, development and pilot production for working on applications such as UV-C LEDs for disinfection and near-infrared emitters for lidar for autonomous driving. Another special focus will be microLEDs.

Automation and AI generally play a major role in Regensburg, enabling Ams Osram to break new ground at its production facilities. The construction of the first pilot assembly line for 8 inch wafer production is currently underway in order to launch the cost-efficient large-scale production of highly innovative microLEDs in the very near future.

"By expanding our development activities in the field of optoelectronic semiconductors, we can create room for innovation and accelerate the time to market for our products", emphasises Aldo Kamper, CEO of Ams Osram.

Hubert Aiwanger, Bavarian Minister of Economic Affairs, stresses: "Ams Osram stands for high tech made

in Regensburg. As the Bavarian state government, we deliberately participate in the financing of this IPCEI project. This is fully in line with our intention to further expand Bavaria as a top international location for the semiconductor industry. Every euro is well invested and will create new jobs in a highly innovative environment."

Ams Osram has been developing semiconductors in Regensburg for 50 years. 2,700 employees currently work at the location.

Nexperia partners with Kyocera AVX on 650 V SiC rectifier module

NEXPERIA, has announced it has entered into partnership with Kyocera AVX Components (Salzburg) GmbH, an international supplier of advanced electronic components, to jointly produce a new 650 V, 20 A SiC rectifier module for high-frequency power applications ranging from 3 kW to 11 kW power stack designs, aimed at application like industrial power supplies, EV charging stations, and on-board chargers.

This release will represent a further deepening of the existing, long-lasting partnership between the two companies.

Space-saving and weight reduction are the key requirements for manufacturers of the next generation power applications. The compact footprint of this new SiC rectifier module will help to maximise power density, thereby reducing the amount of required board space and lowering the overall system cost.

Thermal performance is optimised using a combination of top-side cooling and an integrated negative temperature coefficient sensor, which monitors the device temperature and provides real time feedback for device or system level prognosis and diagnosis.

This rectifier module has a low inductance package to enable high-frequency operation and it has been qualified to operate with a junction temperature of up to 175 °C.

"This collaboration between Nexperia and Kyocera AVX combines cutting-edge silicon carbide semiconductors with state-of-the-art module packaging

and will allow Nexperia to better serve the market demand for power electronic products which offer exceptionally high levels of power density," according to Katrin Feurle, Senior Director of the Product Group SiC at Nexperia.

She adds: "The release of this rectifier module will represent the first step in what is envisaged as a long-term SiC partnership between Nexperia and Kyocera AVX".

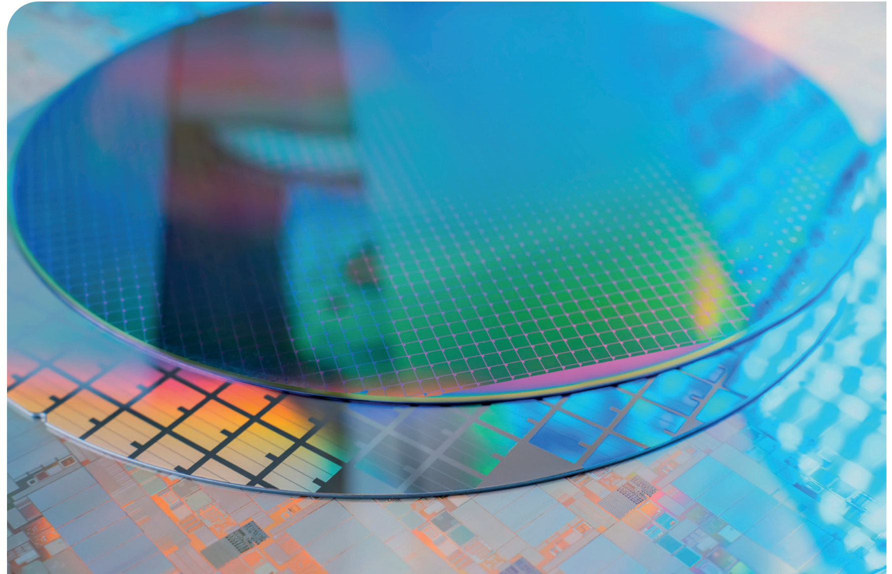
GF awarded $35 million to accelerate GaN plans

US funding brings Vermont fab closer to large-scale production of next-generation GaN chips

GLOBALFOUNDRIES has been awarded $35 million in federal funding from the US government to accelerate the manufacturing of GaN-on-silicon chips at its facility in Essex Junction, Vermont.

With the new funding, awarded by the Department of Defense's Trusted Access Program Office (TAPO), GF plans to purchase additional tools to expand development and prototyping capabilities, moving closer to at-scale 200 mm GaN-on-silicon production.

GF says it also plans to implement new capabilities for reducing the exposure of GF and its customers to supply chain constraints of gallium, while improving the speed of development, assurance of supply and competitiveness of US-made GaN chips. The funding builds on previous collaboration with the US government – including $40 million in support from 2020-2022.



GF's facility in Essex Junction, Vermont, near Burlington, was among the first major semiconductor manufacturing sites in the United States. Today around 1,800 GF employees work at the site.

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J2 to build Hong Kong's first 8-inch SiC fab

Company plans to start volume production in the next couple of years

THE Hong Kong Science and Technology Parks Corporation (HKSTP) has signed an agreement with mainland China-based J2 Semiconductor to set up an R&D Centre at the Hong Kong Science Park, and Hong Kong's first SiC 8-inch wafer fab.

J2 Semiconductor will invest an estimated $900 million (HK$6.9 billion) into the project, with plans to start volume production in the next couple of years. It expects to reach annual production capacity of 240,000 SiC wafers in 2028, and create more than 700 job positions in Hong Kong.

Sunny Chai, chairman of HKSTP said, "The plan of establishing J2 Semiconductor's R&D Centre in the Science Park will promote

Hong Kong's R&D and advanced manufacturing capabilities of third-generation semiconductor devices. J2 Semiconductor brings the core technology and expertise to Hong Kong in advanced chip design, fabrication process and semiconductor product development."

J2 Semiconductor mainly provides SiC devices with a focus on automotive, power conversion and communications.

GaN Systems co-founder joins QPT

GEOFF HAYNES, co-founder of GaN Systems and one of the pioneers of GaN technology. is joining UK start-up QPT as an advisor.

QPT's qGaN module solution enables GaN transistors to be run at up to 20 MHz with nanosecond switching to deliver better operational precision. The technology in a variable frequency drive, for example, enables motors to be driven at up to 99.7 percent efficiency at peak load with hardly any decrease in efficiency at lower loads. This overcomes a challenge for conventional designs today, where efficiency can drop off rapidly at lower loads.

Haynes said: "I have been following the progress of QPT's technology with considerable interest. It solves the thermal and RF problems that GaN is now facing that currently form an insurmountable major barrier for the widespread use of GaN in high power, high voltage, hard switching applications."

He added: "I visited the company's laboratory and was so impressed with its solutions that I am joining the company as an advisor to help them rapidly deploy this technology to the market. With it, GaN can now operate at the high frequencies needed to deliver significant power savings and open up applications worth billions as it provides a far superior performance and efficiency than SiC."

Rob Gwynne, founder and CEO of QPT, added, "We are delighted that Geoff Haynes is coming onboard. He is a world authority on GaN and knows the challenges that it currently faces that limit its use. He immediately understood how our solutions and patents unlock the next phase in the evolution of GaN to become the enabling technology of choice for power electronics."

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GaN: Going beyond fast charging

Navitas has introduced a range of GaNSafe ICs to expand its sales into electric vehicle, solar and data-centre markets

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IN THE FAST CHARGING of mobile devices GaN found its first killer application. But as is often the case with mass market adoption, phenomenal success has led to lower margins and ultimately commoditisation. So, for the makers of this class of device, efforts must now be directed at developing new products for new applications.

That's the latest strategy of the US-based wide bandgap specialist Navitas Semiconductors, which unveiled its GaNSafe portfolio this September.

Strictly speaking, this fabless firm has also had success in a handful of other consumer applications, with its established range of GaN devices deployed to drive motors in washing machines, hairdryers and vacuum cleaners. "But there has been a glass ceiling into data centre, into solar and into electric vehicles," says Stephen Oliver, Navitas' VP of Corporate Marketing & Investor Relations. He told *Compound Semiconductor* that while the company's previous products excel in efficiency, reliability and quality, they don't meet all the needs for lengthy operation at high powers. "The GaNsafe range breaks through, smashes that glass ceiling, and can now be taken seriously by customers in the high-power areas."

There is a rich heritage behind the GaNSafe portfolio, which today has four parts, each designed to operate at 650 V and handle up to 800 V. Together spanning the delivery of electrical power between 1 kW and 22 kW, these packaged ICs that are based on Navitas' fourth generation of GaN benefit from three rounds of about one-fifth die shrink compared with the debut range that came out in 2018. Over the intervening years the company has equipped the GaN IC with more features, such as lossless current sensing and 2 kV electrostatic discharge protection. The launch of GaNSafe includes the addition of short-circuit protection and a higher operating temperature.

To enable higher power operation, GaNsafe features refinements to both the IC and its packaging. The three key advances at the chip level are: the introduction of a Miller clamp; a more intelligent approach to handling short-circuits, as well as ensuring overcurrent protection; and an absence of overshoot and undershoot during switching. Note that even a well-designed device, operating in an efficient manner, can run into problems by generating electromagnetic interference (EMI). But with GaNSafe it is possible to reduce any spikes in EMI via external programming.

"That means that the design team doesn't have to do another spin and cross their fingers and hope they found the thing that's making the spike," enthuses Oliver. "You can tune it in in real time."

Perfecting the package

Innovation is also seen in the 10 mm by 10 mm package, referred to as TOLL – Transistor Outline Lead-Less. Despite the tremendous functionality of the GaNSafe IC, just four external connections are used, allowing leads to be fused together. This creates what is essentially a solid lump of copper, aiding thermal performance, a particular valuable asset in solar systems that undergo wide variations

in temperature every day.

Navitas has also ‘keyed’ some of the pins in its GaNSafe design, creating a ridge metal surrounded by plastic. It’s a design that ensures a tough joint, aiding the mechanical integrity of the product. Another strength of GaNSafe is that it is better at handling humidity and preventing liquid ingress. “It’s a longer path for any humidity to get into the package and destroy it,” explains Oliver.

Since the start of this year, about 40 of Navitas’ customers have been working with products from the GaNSafe portfolio. These firms include: Enphase, a producer of power inverters for the Solar Industry; and Geely, a maker of power systems for the electric vehicle (EV) market that supplies its products to Volvo’s EV off-shoot Polestar, as well as Proton and Lotus.

To help succeed in new markets, Navitas has set up design centres for a data centre power team and an electric vehicle team. Both are staffed with a mix of talent, including experts in devices and those with real-world system knowledge, gained in previous roles outside Navitas. These design teams offer tremendous support to customers, including details for the full bill of materials, circuit diagrams, a PCB layout, and results of tests of EMI, thermal characteristics and efficiency.

One reason why these design teams are needed is that some of the companies that they work with are only just starting to move away from silicon power devices.

“With GaN, we are asking people to go from 50 kilohertz switching for the system to 500 kilohertz-to-a-megahertz, which means that they can’t use the same control chip from their favourite provider that they’ve used for the last 20 years,” says Oliver. Navitas can help in this instance, by advising customers about suitable replacement components.

Minimising manufacturing costs

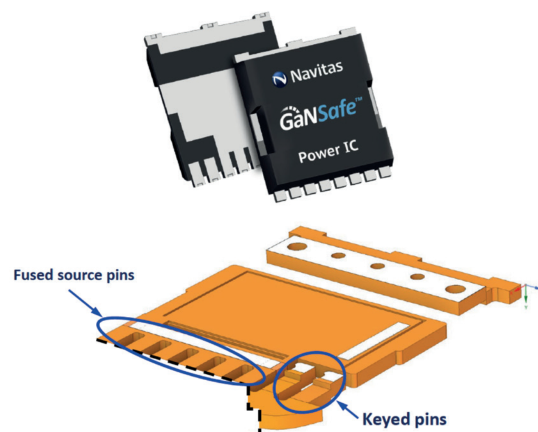
To produce its GaN devices, Navitas partners with an undisclosed packaging partner and the world’s biggest foundry, TSMC. Some may question this approach, claiming that it’s hard to develop breakthrough technologies with external fabs, while warning that it is risky to depend on partners when there’s a need to ramp volume. But Oliver questions both these views, seeing the situation very differently.

“Circuit development has nothing to do with the fab,” counters Oliver “It’s all about good engineers sitting around the table, having good ideas and making it happen.”

And while he agrees that it’s vital to have capacity, he argues that the crucial question is whether it is economical to have that capacity. He sees no sense in spending billions on new fabs – as Wolfspeed and Infineon are doing – and points out that there is no need to buy new equipment to make state-of-the-art GaN devices. At TSMC, Navitas’ latest ICs are produced on 500 nm equipment around 30 years old.

Fabs with this level of capability are very common, with plenty in the US running silicon products on 6-inch and 8-inch lines at low margins. Retrofitted with a handful of tools, they can produce GaN ICs within a year, a move that is welcome, thanks to the higher margins.

With access to capacity clearly not an issue, and GaN ICs gaining traction in new markets, Navitas looks assured of a successful future.



➤ Through sourcing and ‘keying’, GaNSafe ICs deliver a superior thermal performance to their predecessors.

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PowerAmerica powers on

Five years of additional funding will swell domestic production of SiC and GaN power devices

LATE THIS SUMMER, the US renewed its commitment to accelerating the development and deployment of more efficient power electronics by funding five more years of PowerAmerica, the Department of Energy's first Clean Energy Manufacturing Innovation Institute.

In the first year of this second phase of funding, which will see a shift in a focus from SiC to roughly equal backing of both this class of device and that based on GaN, PowerAmerica is contributing another $8 million. A call for proposals will soon follow, with projects maintaining the existing formula for funding – that's private funding supporting federal funding, with both contributing 50 percent of costs.

The latest $8 million builds on $70 million of initial federal funding in the first phase, alongside combined contributions of $81 million from member partners, which total 90 and include those from industry, academia and national labs.

Drawing on that total investment of $151 million, the 196 projects supported by PowerAmerica have been a great success. The 73 projects led by industry, along with 112 led by academia and another 11 fronted by National Energy Labs, have spawned more than ten wide bandgap technologies.

Chris Saldaña, director of the US Department of Energy Advanced Materials and Manufacturing Technologies Office, which is responsible for renewing funding for PowerAmerica, argues that another impressive aspect of PowerAmerica is the relatively high proportion of projects that have reached commercial status. Note that these projects aren't necessarily directly linked to product commercialisation:

"They are pre-competitive in nature, so commercialisation isn't the immediate goal. You have a group of companies, universities, government organisations that come together to work on problems of importance for us, the clean energy sector."

Highlights of successes so far from PowerAmerica include the creation of a SiC chip pilot line in the US, owned by X-FAB.

"The purchase and process development for that line was done through Power America, and has had a major impact in terms of meeting growing demand for those devices," says Saldaña.

PowerAmerica also supported Wolfspeed's development of 3.3 kV, 6.5 kV and 10 kV MOSFETs. "The 3.3 kilovolt MOSFETs are in production," enthuses Saldaña.

While the first phase focused on SiC, GaN was not neglected. Funding supported the growth of Navitas, which has mushroomed from a start-up to a billion-dollar company listed on the NASDAQ exchange. Growth has come from rocketing sales of GaN ICs for laptop and cell phone power supplies.

Funding from PowerAmerica is also driving the uptake of SiC in heavy vehicles. John Deere has developed a 200 kW, 1050 V DC bus inverter based

on SiC that enables 25 percent fuel savings. Cynics might argue that all of these initiatives could have happened without the support of PowerAmerica. But that misses the point.

“The goal of the Manufacturing USA institutes is to supercharge innovation in these technology spaces that we invest in,” says Saldaña. And he points out that while individual advances at companies are to be celebrated, it is important to not overlook the collective impact, which is more than the sum of its parts. “We’re trying to move the whole sector forward, not necessarily individual companies, individual commercial products.”

Growth in domestic production of wide bandgap power electronics is also helping to trim US greenhouse gas emissions. As well as supporting the proliferation of electric vehicles, increased production of SiC power electronics is underpinning the rejuvenation of an electric grid, making it more reliable, more responsive and better at working with renewable energy technologies.

Upskilling the workforce

Another major contribution by PowerAmerica is the creation of a highly skilled workforce for producing and deploying wide bandgap power electronics. Efforts have already included STEM programmes for 9,000 students in their last year of school, and the training of more than 400 masters and PhD students.

Having tracked the destinations of these graduates, it is clear that training is providing a great return on investment, with the majority entering and remaining within the wide bandgap power electronics industry.

“When you create this critical mass of activity in an area, they’re going to be part of the same community moving forward, and will help to push the mission that they were trained under through the Institute,” says Saldaña. Motivated by this success, PowerAmerica is developing training materials, training programmes and certification to support those wanting to further their careers within this sector.

Efforts are also being directed at attracting everyone to this industry. “There’s a strong emphasis on diversity, equity, inclusion and accessibility through the Institute,” says Saldaña.

Another appeal of working in the US semiconductor industry is its long-term support. That extends beyond PowerAmerica, which will certainly run for the next five years and quite possibly more, to an initiative called Energy Efficiency Scaling for Two Decades. It’s a national programme that aims to double the energy efficiency of microelectronics every two years. Success will drive disruptive innovation, giving yet more impetus to America’s burgeoning semiconductor industry.

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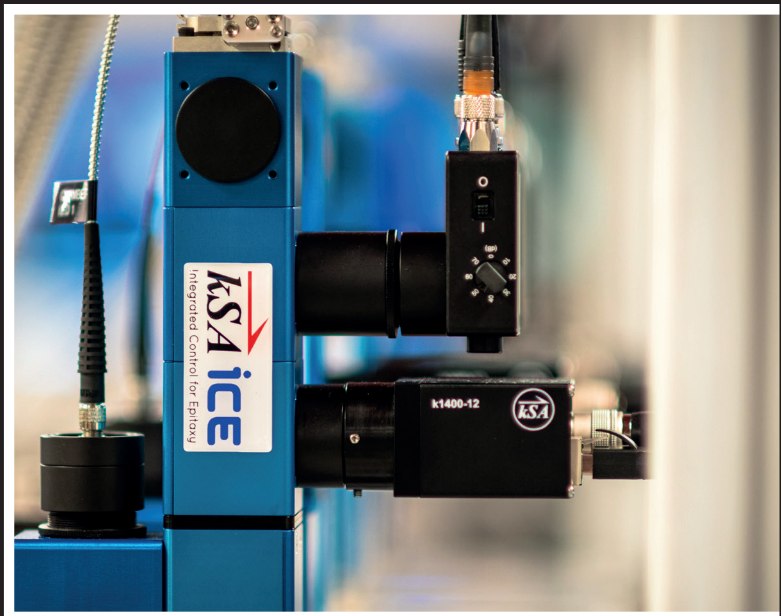


Empowering electric vehicles with superior SiC

SmartSiC substrates hold the key to ramping volumes of better SiC devices for automotive and industrial applications

BY EMMANUEL SABONNADIÈRE, CHRISTOPHE MALEVILLE AND CYRIL MENON FROM SOITEC

IN SEPTEMBER 2021, SmartSiC made its debut in *Compound Semiconductor* magazine. Pioneered by our company, Soitec, this novel material technology is a game-changer within the SiC industry: it is enabling a new generation of engineered substrates that consist of a thin layer of single-crystal SiC, bonded on a polycrystalline SiC wafer. Now two years on from this unveiling, SmartSiC is starting to fulfil its potential, delivering impressive results.

The impact of SmartSiC will be colossal. It has fundamentally changed perspectives for SiC, especially for 200 mm acceleration, and it is starting to reshape the SiC industry with a much greener technology. The great strengths of SmartSiC, compared with incumbent single-crystal SiC wafer, include an unparalleled ten-times hike in re-use capability and an eight-fold enhancement in electrical conductivity. Due to these massive improvements in key metrics, SmartSiC is opening new frontiers for high-performance SiC devices and their applications.

As well as these exceptional capabilities at the wafer level, SmartSiC is demonstrating its capability to produce a foundation that ensures better diodes and transistors. Measurements reveal a reduction in the drain-source on-resistance of 1200 V MOSFETs of between 10 percent and 15 percent, and around a 15 percent decrease in forward-voltage at a rated current in 650 V SiC diodes. These noteworthy improvements in device-level performance translate into a significant advantage in the fabs, with the opportunity for around a 25 percent increase in the number of high-quality die that can be produced from every 200 mm wafer for 25 mm^2 dies.

Leading the way, STMicroelectronics is the initial adopter of SmartSiC technology. Its collaboration with us has been dedicated to the rigorous automotive qualification of SmartSiC. The ultimate goal for our partnership is to qualify SmartSiC on ST SiC MOSFET technology in mid-2024, with products based on SmartSiC available from Q3 2024 onwards. Meeting this target will position both of us at the forefront of innovation in the EV sector.

Our SmartSiC technology continues to evolve and improve. Recently, we increased the crystal quality of our SmartSiC wafers with a specific epitaxy preparation, realised before the layer transfer of single-crystal SiC. Thanks to this advance, we have

drastically reduced the basal plane dislocation density in our material. In turn, this will lead to better device performance.

This year, SmartSiC became a 'must-have' technology for key leaders in the SiC industry. With over a thousand prototypes under assessment and more than thirty prospects and clients, SmartSiC is now being adopted. High-volume production will take place at our new plant, Bernin4, which opened this September, following the installation of initial industrialisation lines over the summer months. When fully up and running, this fab will have a capacity of 500,000 wafers per year. Note that the production process used in this fab is flexible, starting with 150 mm wafers and adding 200 mm wafers in the first half of 2024. Once the ten-fold re-use goal is attained, another significant advantage will emerge: a secured production process, thanks to reserves of refreshed wafers that we will hold.

To put it succinctly, given all the strengths of SmartSiC, this technology is an obvious choice for any SiC device maker wanting to process 200 mm wafers – and that's before considering current global scarcity of this material.

High-volume manufacturing

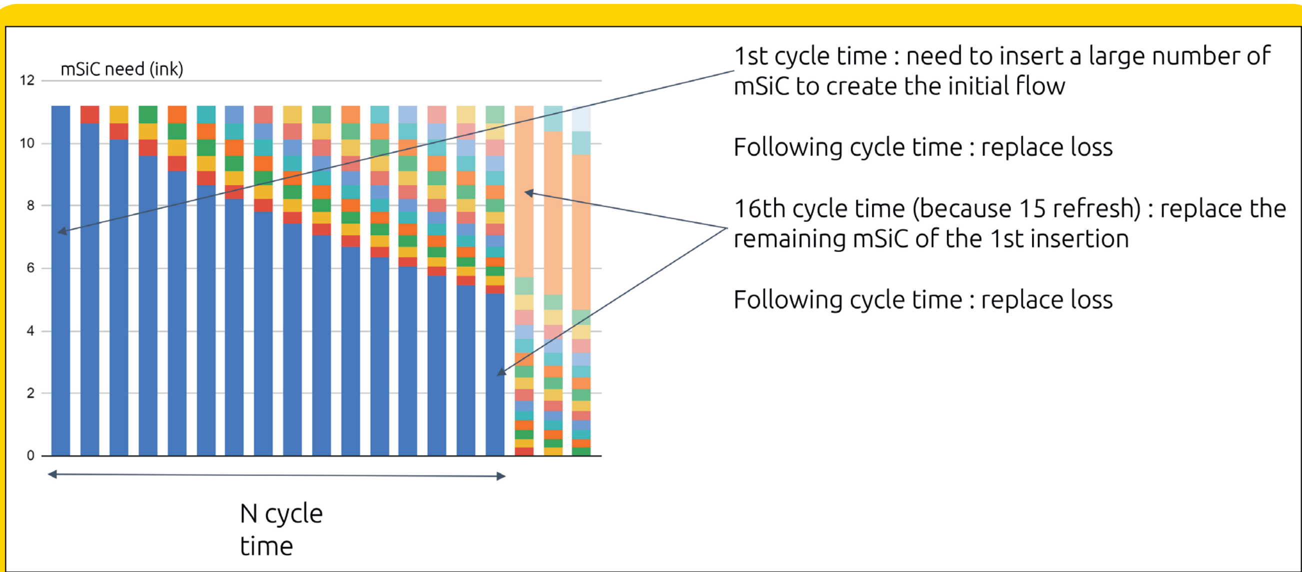
The unparalleled performance of SmartSiC is not just attracting the attention of makers of SiC power devices. Our technology is also garnering significant attention further along the supply chain, from Tier 1 and OEM companies within the automotive industry. What pleases them is that it will not be long before we attain IATF and ISO9001 certification at Bernin4, aligning with the standards of our other manufacturing plants in Bernin and Pasir-Ris. Note that our company, and our SmartSiC portfolio, are deeply committed to an impressive environmental, social and governance agenda.

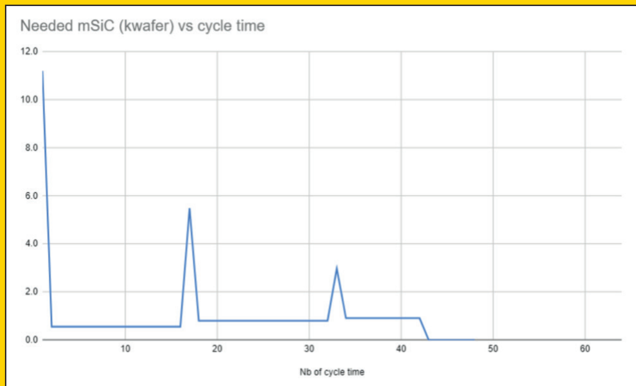
High on our agenda when developing our production process is energy efficiency, with much effort directed at reducing energy consumption. Perfectly aligning with this objective, SmartSiC is starting to play a pivotal role in realising substantial reductions in carbon footprint when compared with traditional bulk SiC materials. Such a synergy is vital in supporting the ongoing EV revolution, which is making a crucial contribution to combating climate change. Our company, and SmartSiC, are actively aiding this cause at various levels, from wafer production to power device development and system integration.

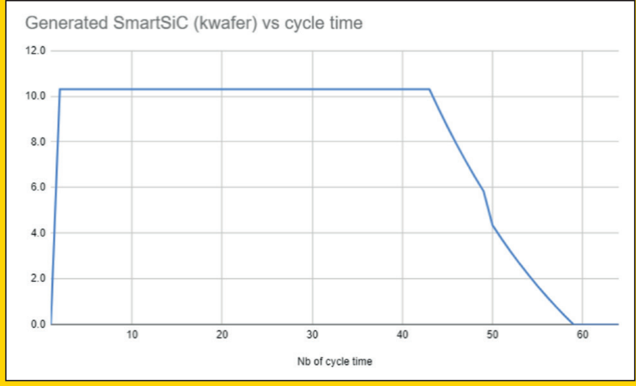
Building Bernin4 has not been easy. As well as a supply crisis in construction materials, there's been a flurry of industrial construction projects in the Grenoble region. Yet despite these issues, we have completed the 2000 m^2 clean room for SmartSiC on time, with just 18 months elapsing from breaking ground to the construction of the first prototypes.

Our state-of-the-art clean room is seamlessly integrated into our pre-existing infrastructure. Due to this, we have established crucial links with Bernin 2 (300 mm silicon-on-insulator wafers), raw materials storage and the finished products warehouse. This strategic connectivity enhances operational efficiency by ensuring optimised flow and maximising flexibility for the facility.

To provide a high-skilled workforce for Bernin 4, we are gradually transferring over operators, technicians and engineers trained on the SmartSiC pilot line at CEA/LETI in Grenoble. These staff are being integrated into the Bernin 4 organisation to manufacture the first industrial prototypes. Bernin 4 benefits from the same digital resources supporting the other plants on the site: a semiconductor manufacturing execution system, a process control system, and manufacturing equipment that's monitored using statistical process control, fault detection and classification, and computerised maintenance management systems. The production line is scheduled to receive ISO 9001 certification by October 2023, and plans are in place to obtain IATF certification in 2024.







➤ Targeting a 10,000 SmartSiC production per cycle time with a steep ramp up (permanent regime since the 2nd cycle time), around 11,000 single-crystal SiC substrates are injected for the first cycle time to initially load the line. To compensate for losses linked to yield, for of each following cycles, roughly 600 single-crystal SiC substrates are added per cycle time. Considering a maximum number of refresh of 15x, the first injection of SmartSiC has to be replaced at the 16th cycle time, equating to around 5,000 single-crystal SiC substrates in this example. Losses linked to yield are compensated for in each of the following cycles (roughly 800 single-crystal SiC substrates per cycle time). The graphs show the number of monoSiC substrates injected in the line every cycle time (left) and the number of SmartSiC wafers produced versus cycle time (right). Based on a realistic industrial scenario, we can see that the manufacturing kinetics are such that the number of SmartSiC wafers generated exceeds rapidly the number of single-crystal SiC substrates inserted to reach a factor of 10x across *N* cycle time.

A quick, efficient ramp up

One of the great strengths of our SmartSiC industrial line is that we are able to manufacture more than 10 SmartSiC substrates from a single-crystal SiC substrate.

By adjusting the single-crystal SiC supply volumes, we can deliver a very steep ramp up in the production of SmartSiC substrates. This is accomplished by injecting a larger quantity of single-crystal SiC from the start of production, to load the line, a point illustrated in Figure 1. Starting with just over 11,000 SiC wafers, we can yield around 10,000 during the first cycle (Figure 1 shows the number of single-crystal SiC wafers present in the line as a function of the cycle time, with the colour indicating the origin of the wafers – in blue, 1st injection; in red, 2nd injection; in orange, 3rd injection; and so on).

During our industrialisation of SmartSiC, we control ramp up, and then we retain a steady state by adjusting the level of injection of single-crystal SiC substrates in the line. By using single-crystal SiC substrates over *N* cycle times – an approach that provides a degree of inertia – we ensure a level of resilience, in terms of the number of SmartSiC wafers that we produce, by catering for the possibility of irregularity in the number of single-crystal SiC wafers injected in each cycle time.

As well as pioneering SmartSiC, we are playing a key role in driving the development of the polycrystalline SiC supply ecosystem. This effort includes a joint-development agreement with Mersen, a renowned French-based company with broad materials expertise. Together we are crafting

the most efficient polycrystalline SiC wafers. Our joint strategy is to qualify suppliers across different regions. We have already established long-term contracts with two suppliers and we are actively engaging with a third. Notably, Bernin 4 can accommodate a high degree of flexibility from our suppliers, as this facility allows for a seamless transition between 150 mm and 200 mm wafers.

Automotive and industrial markets

Our SmartSiC is targeting markets that are tipped for phenomenal growth. For the Light Vehicles market, worldwide production is forecast to increase at a low-to-mid single digit compound annual growth rate (CAGR) through to 2030. Within this, battery EVs are the dominant driving force, predicted to climb at a CAGR of above 20 percent. Thanks to this rapid growth, the CAGR for SiC modules is 32 percent. In addition, there is a profound shift towards electrification in industrial applications, providing additional opportunities for SmartSiC.

We will quickly penetrate these markets by ramping our production by a factor of ten in just 18 months at our Bernin facility. Our expectation is that by 2030, the SmartSiC share of the SiC market will be higher than 30 percent. The SmartSiC wafer manufacturing process also reduces CO_2 emissions by 70 percent compared with current monocrystalline SiC substrates.

Our progress aligns with one of our key values, which is contributing to a reduction in climate change. We are deeply committed to environmental, social and governance performance, with considerable effort directed at reducing water and energy consumption, as well as minimising waste. Moreover, our strategic SiC programme that led to the development of SmartSiC involved a strong commitment to greener values, while delivering superior results compared with bulk SiC.

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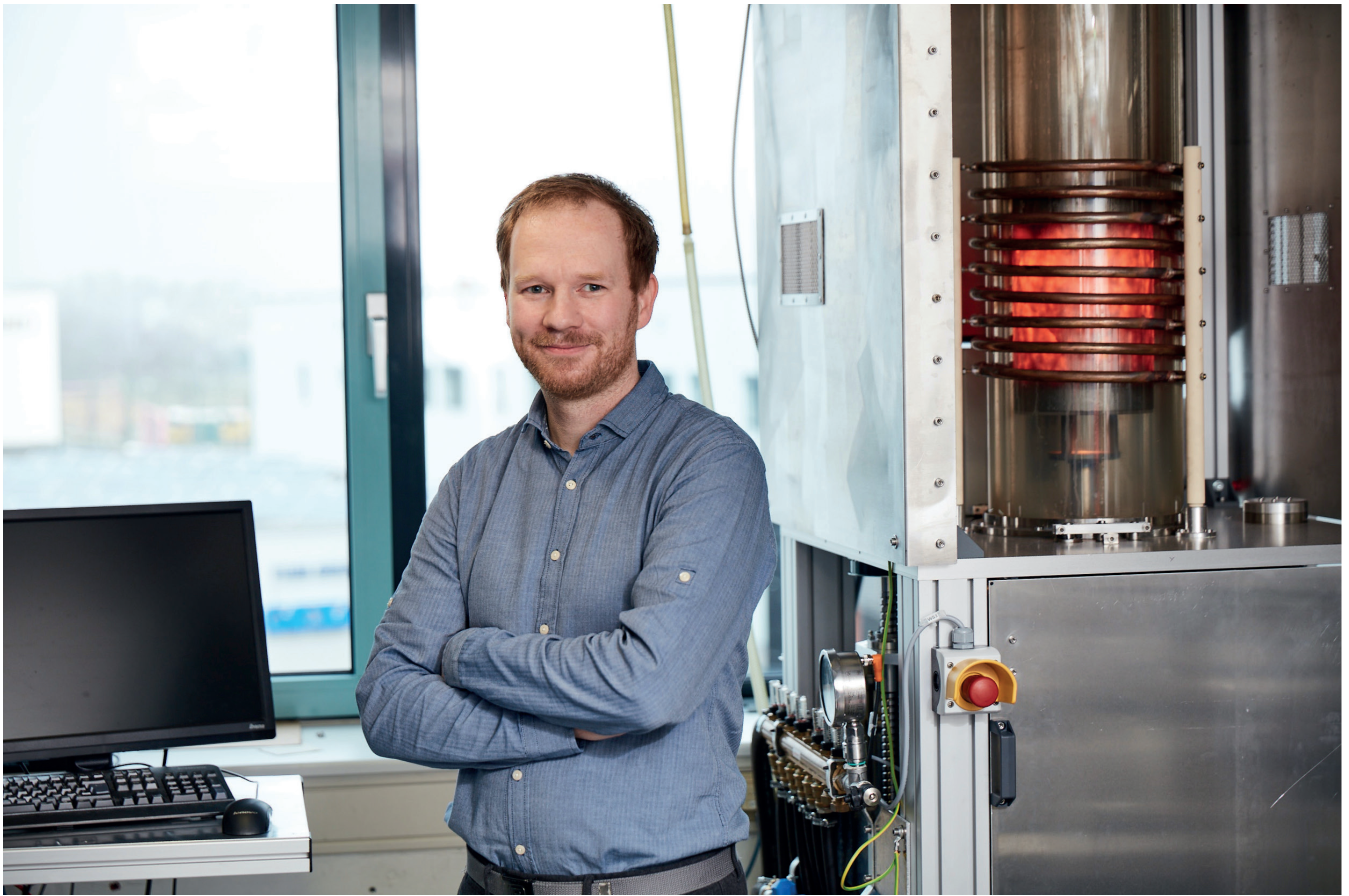

Efficient enlargement of bulk AlN

Introducing expansion angles in excess of 45 degrees can slash the time it takes to realise bulk AlN grown by physical vapour transport with industrially relevant crystal diameters

BY CARSTEN HARTMANN AND THOMAS STRAUBINGER FROM THE LEIBNIZ INSTITUTE FOR CRYSTAL GROWTH

THE ULTRA-WIDE band gap semiconductor AlN, as well as its ternary cousin AlGaN, has a number of attributes that make this material system a promising one for electronic and optoelectronic devices. This class of nitrides can withstand harsh conditions and high temperatures, and thanks to the very wide bandgap, can be used to make LEDs that emit in the deep and far UVC. The largest markets for such devices, which span 220 nm to 280 nm, are the disinfection of drinking water and waste water treatment. However, emission in this spectral range can also be deployed for surface sterilisation and bio-chemical sensing. As well as these opportunities in deep-UV photonics, AlN-based devices are compelling candidates for next-generation high-frequency power-conversion. Already, AlN-based high-power transistors are outperforming those made from the two most common wide bandgap semiconductors, SiC and GaN.

Due to a lack of native substrates, researchers exploring the capability of AlN and its alloys began by using sapphire substrates for the development of epitaxial layers. However, even when they turned to complex processing steps, the threading dislocation densities in the AlGaN layers remained high – typically in excess of 1×10^{8} cm^{-2}. The high density of these threading dislocations is one of the primary reasons why the potential of the AlN material system is yet to be fully exploited.

The power of PVT

Offering a promising way forward is the growth of AlN crystals by Physical Vapour Transport (PVT). In recent years, this approach to the growth of AlN with a high degree of crystallinity has advanced significantly, laying the foundation for substantial improvements in device performance. Successes include the fabrication of electrically injected

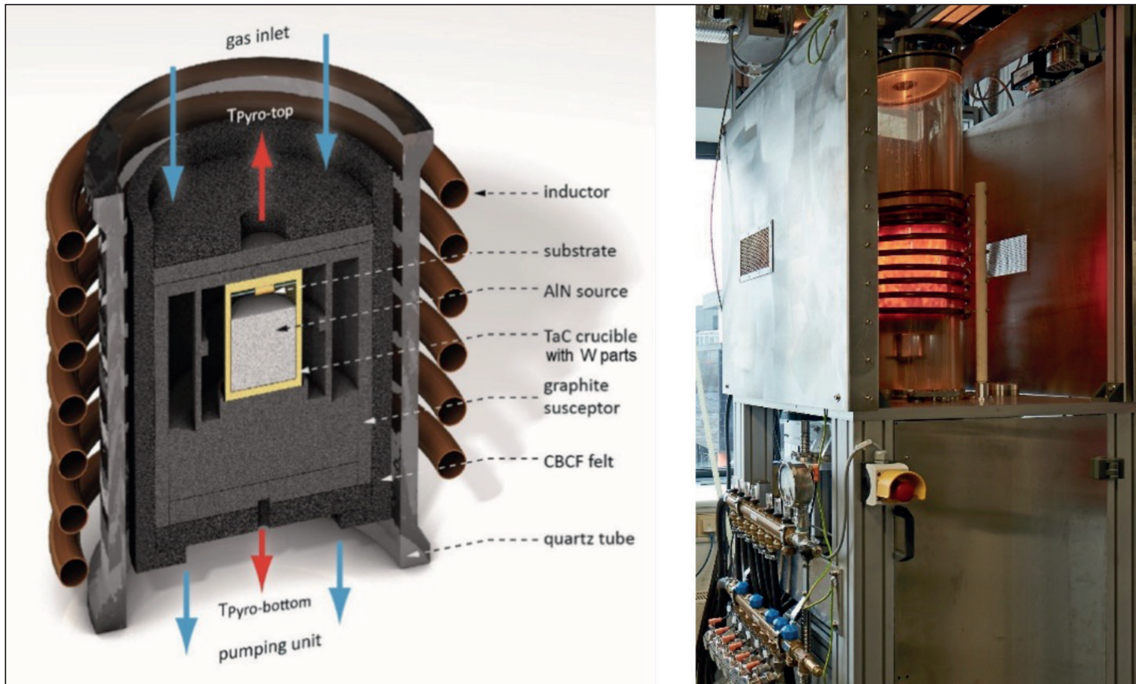

Figure 1. (a) A sketch of the setup, with four identical PVT reactors built at IKZ. (b) one shown here with opened housing for a better view of the heated setup. For more details see C. Hartmann *et al*. Cryst. Eng. Comm. **18** 3488 (2016).

deep-UV laser diodes and LEDs with high output power over long lifetimes.

Pioneers of AlN substrates produced by PVT include Hexatech Inc., which has introduced AlN substrates with diameters of up to 2 inches and threading dislocation densities below 1×10^4 cm^{-2}. Hexatech is offering this material to selected scientific partners.

Another provider is Crystal IS, which demonstrated 4-inch AlN substrates with an 80 percent useable area earlier this year, and makes 3-inch AlN substrates for internal use.

For both these trailblazers, progress has been slow and hard won. To increase the diameter of the AlN crystals to the size they are today, engineers at these companies have devoted more than a decade to producing generation after generation of crystals, each with a larger diameter. Increases in size have come from dynamic growth of unfaceted regions. This enlargement, occurring at the beginning of crystal growth (cone-shaped), is restricted to small expansion angles.

Our team at IKZ – that's the common shorthand for the Leibniz Institute for Crystal Growth in Berlin, Germany – has developed an approach that overcomes this restriction. PVT is also used to grow our bulk AlN crystals, produced with an inductively heated graphite setup (see Figure 1).

A foundation for our latest success is our expertise acquired through the growth of SiC boules by PVT. When moving from SiC to AlN growth we retained the reactor, the thermal insulation felt (carbon-bonded carbon fibre), and large parts of the graphite components. The growth temperature for both materials is around 2200 °C.

One key difference between the growth of AlN and SiC is the ambient atmosphere. For SiC, an argon atmosphere below 50 mbar is employed, while for AlN its N_2 at a pressure of more than 400 mbar. Crucibles also differ, with graphite used for the growth of SiC, and tungsten or TaC used for AlN. Note that these two options are the only refractory materials capable of withstanding the reactive aluminium vapour under growth conditions.

To produce a high-purity AlN source – it contains less than 150 ppm wt oxygen – we start with a commercially available AlN powder and apply multiple sublimation–recrystallisation steps. During crystal growth, this source, located in the lower part of the crucible, decomposes gradually into aluminium

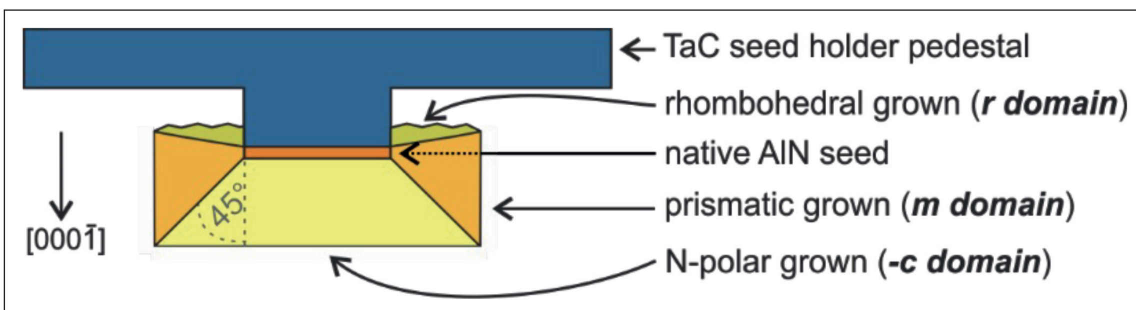

Figure 2. Simplified sketch of the seed holder design: TaC pedestal and fully faceted grown crystal with an expansion angle of 45°. For more details see C. Hartmann et al. Appl. Phys. Express **16** 075502 (2023).

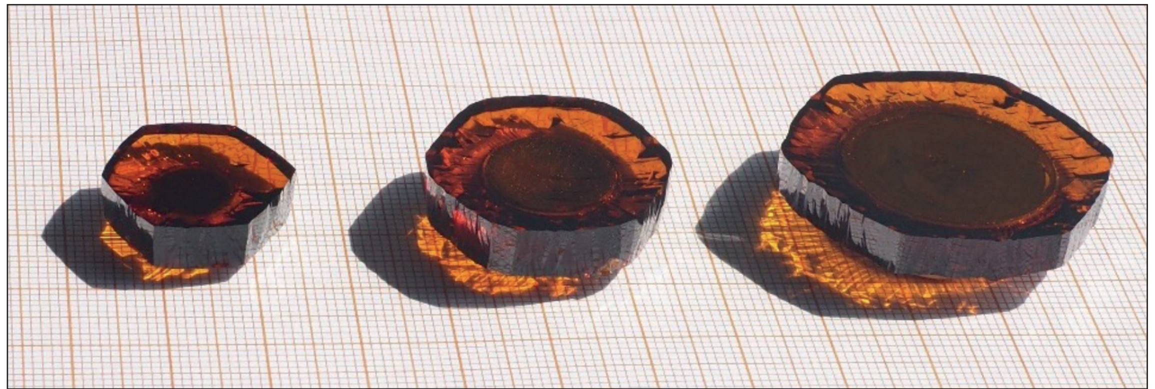

Figure 3. Three AlN crystals of subsequent crystal generations (17 mm, 27 mm, and 37 mm in diameter).

and N_2 vapor species. The aluminium vapour pressure in the crucible depends on the temperature, and typically ranges from 50 mbar to 150 mbar – one may imagine an aluminium 'fog' inside the N_2 ambient. During growth, gaseous aluminium species diffuses along the concentration and temperature gradient through the nitrogen ambient in the growth space, before re-condensing on the AlN seed.

Seeding the growth

Recently, we have developed a seed holder design that positions the seed on a TaC pedestal. With this arrangement, crystals grow freely without contact to parasitic grains (see Figure 2). This design allows high radial thermal gradients – the driving force for diameter expansion.

With this new configuration we have realised far higher lateral growth rates. At a seed temperature of 2230 °C growth rates are as fast as around 200 µm/h in both the N-polar and the prismatic *m* directions, resulting in huge expansion angles of around 45° along the entire crystal length. The crystal habit consists of the (000$\bar{1}$) N-polar top facet, the (10$\bar{1}$0) prismatic *m* facets, and (101*x*) rhombohedral *r* facets. The full diameter spans the entire crystal length, ensuring that all cut *c*-plane wafers have the same (final crystal) diameter.

AlN seeds with a diameter of 8 mm and a threading dislocation density below 1 x 10^3 cm^{-2} provided the starting point for this work. These first-generation seeds were prepared from spontaneous nucleated AlN crystals. Using our seeded process, growth on them produced crystals with a length of 5-7 mm and a diameter between 18-24 mm. With just two to three steps, we magnified dimensions, producing AlN crystals with diameters of more than 30 mm, which are very suitable for preparing 1-inch substrates (see Figure 3). Based on our current findings, we can't foresee any obstacles to a fast scale-up to industrially relevant diameters of up to 4 inches or more.

If AlN substrates are to make a significant impact, a substantial increase in production speed and availability must go hand-in-hand with maintaining high material quality – note that the latter is possible, according to our characterisation. Measurements of symmetric 0002 and asymmetric 10$\bar{1}$3 rocking curves on the -*c* facet of the crystals with an open detector aperture reveal typically a single sharp peak with a full-width at half-maximum of 11 arcsec (see Figure 4). Such a sharp peak is indicative of a high structural quality, including a low dislocation density and an absence of small-angle grain boundaries.

Often rocking curves are used to determine the dislocation density in wide bandgap materials and epilayers. However, this approach only provides meaningful results for dislocation densities down to 5 x 10^4 cm^{-2}, as at lower dislocation densities there is no peak broadening compared with perfect, dislocation-free AlN. Another issue is that bulk crystals often show inhomogeneously distributed dislocation densities, having wide areas with very

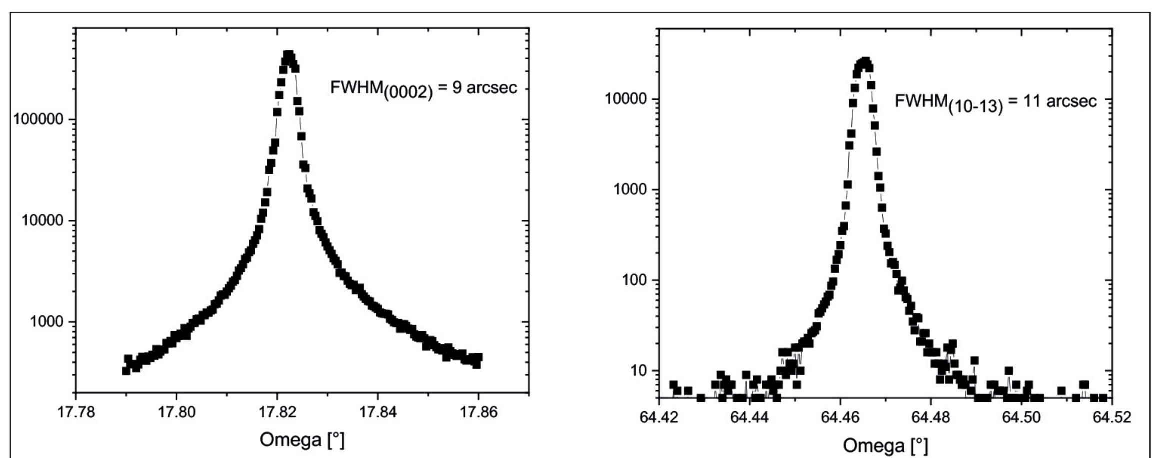

Figure 4. Double crystal rocking curves (semi logarithmic scale) measured with open detector aperture in the 0002 (a) and 10$\bar{1}$3 reflection (b).

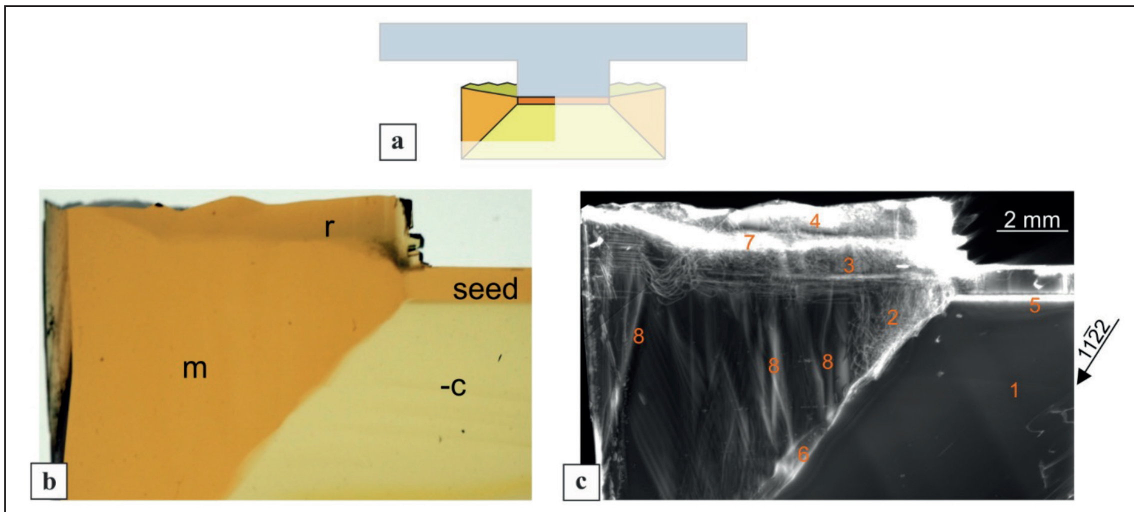

Figure 5. (a) A sketch with a highlighted area of an m-plane sample prepared from a seeded crystal with diameter of 20 mm; (b) Transmission photograph of a 1 mm-thick cross-section m plane sample. The several growth domains (-c, m, and r) are distinguishable by the different colours. (c) White-Beam X-Ray Topography (WB-XRT) stitched images ($11\bar{2}2$ reflection) of the cross-section sample. No dislocations are visible in the -c grown domain (1). Dislocations exist only in the m domain near the -c/m boundary (2). Further dislocations exist in the upper part of the m domain (3) and in the r domain (4). The lower half of the sample is dislocation free. Strain contrasts are visible at the domain boundaries (5,6,7) and within the m-domain (8). For more details see C. Hartmann et al. Appl. Phys. Express **16** 075502 (2023). The WB-XRT image was recorded by Merve Pinar Kabukcuoglu, Elias Hamann, and Daniel Hänschke from the Institute for Photon Science and Synchrotron Radiation, Karlsruhe Institute of Technology. We thank the Institute for Beam Physics and Technology for the operation of the storage ring, the Karlsruhe Research Accelerator.

few dislocations and local dislocation clusters. It's not possible to uncover the details of these variations with rocking curves, which only offer an average over the recorded area. To identify the lateral dislocation distribution, one can turn to X-ray topography or defect-selective etching.

We have scrutinised an *m*-plane sample cut from a seeded crystal with a 20 mm diameter using white-beam X-ray topography. This involved the selection of the $11\bar{2}2$ reflection, which is sensitive to all possible types of dislocations (*a*, *c*, and *a*+*c* type).

From this form of X-ray topography, we have established that the entire -*c* grown domain of this sample is dislocation free. The only dislocations that exist are in the *m* domain near the -*c*/*m* boundary and in the *r* domain. We find that dislocations start at the seed rim and stay in the *m* area without crossing the -*c*/*m* domain boundary. So far, we are yet to determine the origin of these dislocations. Possible explanations include: insufficient polishing quality at the seed rim; unfavourable initial growth conditions, such as gradients that are too large, at the seed rim; and contact between the *r* domain and the seed holder. We have also observed additional contrast features at several domain boundaries and within the *m* domain, caused by strain that stems from different impurity concentrations.

To obtain defect information over the entire diameter, we prepared a wafer from a crystal 34 mm in diameter. We characterised the wafer with defect-selective etching (see Figure 6). With this technique we determined that the medium etch-pit density, using a standardised 21-point measurement, is 5×10^3 cm^{-2} inside the 25 mm target diameter. We also uncovered a linear arrangement of dislocations, occurring at the domain boundary between the -*c* and *m* grown domains. The origin of the associated etch pits can be traced back to dislocations formed at the seed rim, which continued along the -*c*/*m*

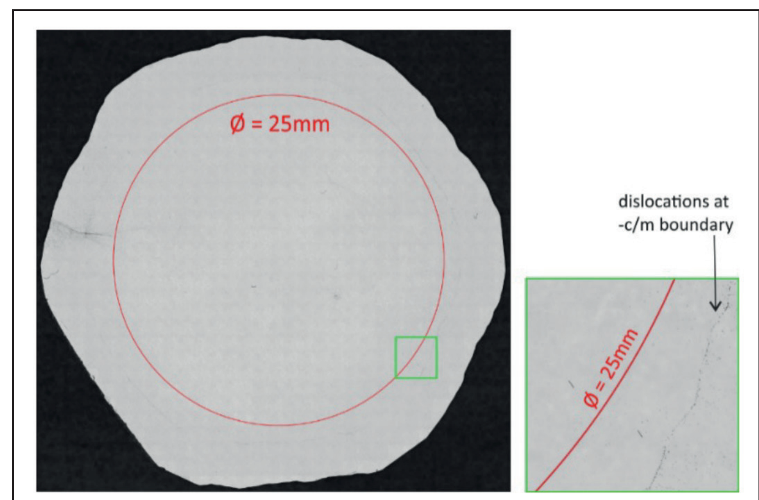

Figure 6. Defect selective etched AlN wafer with a diameter of 34 mm an average etch pitch density of 5×10^3 cm^{-2} inside the 25 mm target diameter. The -*c*/*m* domain boundary with an increased etch-pit density is outside of the 25 mm target diameter (green square). For more details see C. Hartmann *et al*. Appl. Phys. Express **16** 075502 (2023).

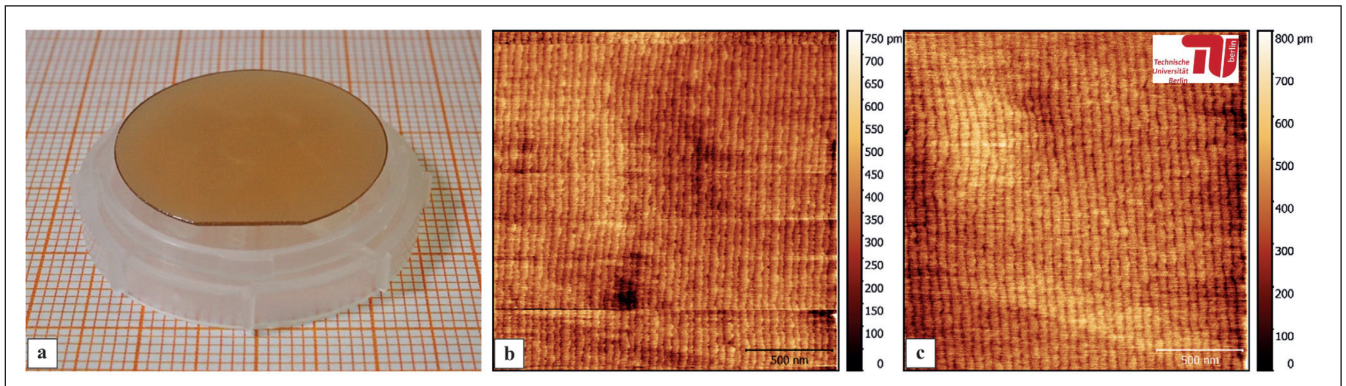

Figure 7. (a) 25 mm epi ready Al-polar AlN substrate; (b) atomic force microscopy (AFM) image of Al-polar epi-ready surface after chemo-mechanical polishing (off-cut of 0.4°); (c) AFM image of a 5 µm-thick Al-polar AlN epi layer (off-cut of 0.4°) grown by MOCVD. We thank Marcel Schilling, Tim Wernicke, and Michael Kneissl from the TU Berlin (section 'Experimental Nanophysics and Photonics') for the homoepitaxial growth of the AlN epi layers and the recording of the AFM images.

boundary in the *m* domain (compare with Figure 5 (c)). Recently, we have been pursuing further diameter enlargement of our AlN crystals. Our efforts have involved selecting the *c*-plane wafer close to the top of the crystal, where the -*c*/*m* boundary is close to the crystal edge, and using a seed diameter that gets as close as possible, but below, the -*c*/*m* boundary. This approach promises to provide a shortcut to the development of commercial substrates with a diameter of 100 mm or more.

One of the highlights of our work on AlN is the fabrication of an epi-ready 25 mm substrate with an *m* flat (see Figure 7 (a)). The entire substrate area is grown on the -*c* facet, clearly identified by homogeneous yellowish colouring. To produce this substrate, our team in our preparation lab developed a complete AlN preparation line, beginning with the sawing of *c*-plane wafers and including lapping, mechanical polishing and chemo-mechanical polishing. The latter form of polishing using silica under basic conditions ensures a root-mean-square surface roughness below 0.3 nm (see Figure 7 (b)). Encouragingly, when MOCVD is used to grow pseudomorphically homoepitaxial layers on this substrate, the epilayer matches the quality of its foundation (see Figure 7 (c)). We can adjust the substrate off-cut – this mainly determines the step widths/macro step formation – precisely between 0.05 and 0.5 degrees.

Our institution is now selling epi-ready single crystalline wafers with a diameter of 10 mm. These substrates are divided into a range of grades, with some better suited to research purposes and others more aligned to technology development.

By the end of next year, we hope to offer 1-inch prototype substrates and 2-inch demonstrators. We are also keen to investigate the performance of devices that are built on our substrates, and are open to project ideas for AlN-based opto-electronic or high-power devices. In such a collaboration we will be able to provide AlN substrates with diameters presently up to 1-inch that feature tailored optical, electrical and structural properties.

FURTHER READING

- C. Hartmann *et al.* "Efficient diameter enlargement of bulk AlN single crystals with high structural quality" Appl. Phys. Express **16** 075502 (2023)
- C. Hartmann *et al.* "Favourable growth conditions for the preparation of bulk AlN single crystals by PVT" Cryst. Eng. Comm. 22 1762 (2020)
- R. Dalmau *et al.* X-Ray "Topography Characterization of Large Diameter AlN Single Crystal Substrates" Mater. Sci. Forum **1004** 63 (2020)
- R. T. Bondokov *et al.* (Invited) "Development of 3-inch AlN Single Crystal Substrates" ECS Trans. **109** 13 (2022)
- H. Amano *et al.* "The 2020 UV emitter roadmap" J. Phys. D: Appl. Phys. **53** 503001 (2020)
- J. Kotani *et al.* "24.4 W/mm X-Band GaN HEMTs on AlN Substrates With the LPCVD-Grown High-Breakdown-Field SiNx Layer" IEEE J. Electron Devices Soc. **11** 101 (2023)

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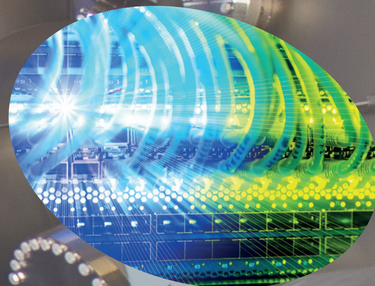

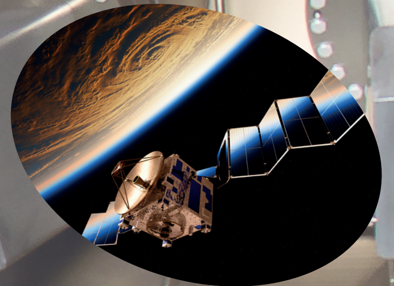

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The road to SiC process control

Manufacturers of SiC power devices produce better transistors when they turn to metrology techniques involving Fourier transform infrared spectroscopy, optical critical dimension and picosecond ultrasonics

BY NICK KELLER FROM ONTO INNOVATION

EFFORTS at curbing carbon dioxide emissions are stepping up, with more electric vehicles on our roads and the installation of renewable energy sources on the rise. Alongside these advances, the makers of these green technologies are increasing the electrical efficiency of their offerings, with silicon-based power devices being ditched in favour of superior alternatives based on the likes of SiC.

Supporting this move are the superior physical properties of these compounds. Compared with silicon, semiconductors such as SiC have wider-bandgaps, a higher electron saturation velocity, a higher critical electric field and a larger thermal conductivity. Drawing on all these strengths, power transistors offer higher operating frequencies, higher power ratings, elevated operating temperatures, better cooling capability and lower energy loss – just the traits that the market wants.

Today's manufacturers of SiC power devices are tending to focus on trench-based devices, a design that reduces on-resistance and increases carrier mobility. But there is a trade-off, with these strengths coming at the expense of increased fabrication complexity.

To address this issue, high-volume manufacturers of SiC power devices must adopt inline process control at several key steps, including optical metrology methods like Fourier transform infrared (FTIR) spectroscopy, optical critical dimension (OCD) and picosecond ultrasonics. When armed with these techniques, chipmakers are far better informed when undertaking critical processing steps, including epilayer growth, trench etch, gate poly-silicon etch back, and frontside/backside contact metallisation.

All of these three process control techniques that have just been mentioned can play a major role in streamlining SiC production. When FTIR is adopted alongside advanced algorithms, SiC manufacturers can extract epilayer thickness and carrier concentrations for two- and three-layer stacks. What's more, FTIR can non-destructively characterise the depth and the dopants in the implant layer directly on SiC substrates before and after the anneal process step. That's a significant benefit, as it removes the need for monitoring silicon wafers and secondary ion mass spectrometry when undertaking implant characterisation. Meanwhile, the introduction of a multi-channel OCD

METROLOGY SOLUTIONS FOR SiC TRENCH MOSFET PROCESS

LAYER	Drift Layer Epi	P Base Implant	N+ Implant	P+ Implant	Carbon Layer Dep & Anneal	Hard Mask Etch
KEY PARAMETER(S)	Thickness Dopant Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Thickness Carrier Conc. + Depth	HM Height HM CD
DEVICE IMPACT	R_{on} Breakdown Voltage	Channel Mobility(μ_{FE}) V_T	Contact Resistance	I_{DSAT} C_{GD}	Surface Roughness Si Desorption Block	R_{on} Gate SWA (Mobility)
TECHNOLOGY	FTIR	FTIR	FTIR	FTIR	OCD and FTIR	OCD

LAYER	Gate Trench Etch	Gate Oxide Growth	Poly Si Etch Back	Passivation Oxide Etch	Source Metal Dep	Drain Metal Dep
KEY PARAMETER(S)	Depth and TCD/ BCD/SWA/Rounding	Sidewall Thickness Bottom Thickness	Recess Depth	Height CD	Thickness (Ti/Al) Roughness	Thickness (Ti/Al) Roughness
DEVICE IMPACT	R_{on} & I_{DSAT} Parasitic JFET R	Channel Mobility(μ_{FE}) V_T & Q_{GD}	V_{GS}	Leakage Current C_{GS}	S/D Contact Resistance	S/D Contact Resistance
TECHNOLOGY	OCD	OCD	OCD	OCD	PULSE	PULSE

Figure 1. SiC trench MOSFET process flow.

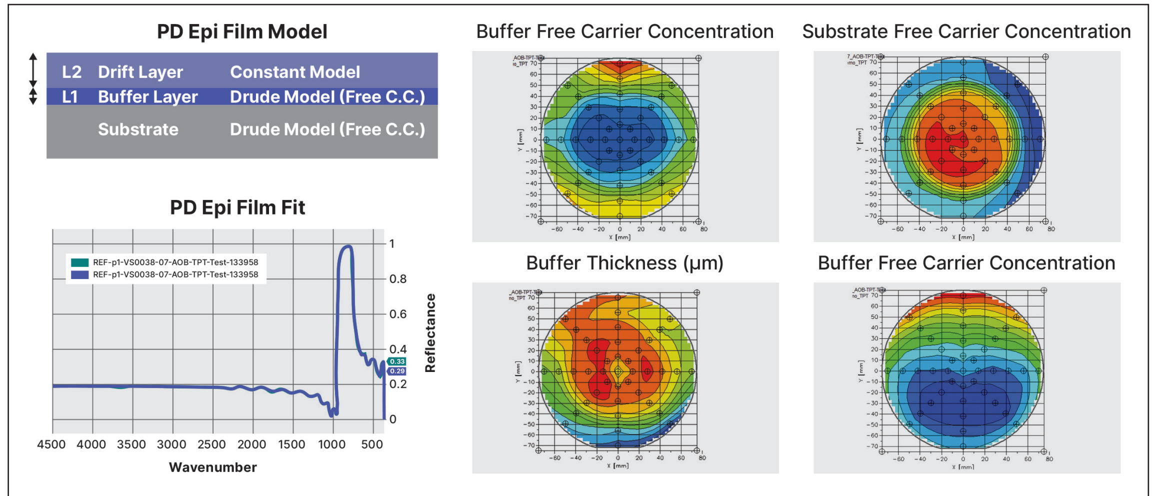
tool in a SiC fab can accurately and non-destructively determine trench depth, bottom and top widths, and bottom rounding at the trench etch step, when this technique draws on electromagnetic solvers that utilise advanced rigorous coupled wave analysis. Note that bottom rounding of the trench is critical to preventing a high electric field density, and ultimately premature device failure. Lastly, picosecond ultrasonics can improve efficiency in a SiC fab by measuring frontside and backside metal contact thickness. Together, these non-destructive, in-line process control methods empower chipmakers to solve many of the challenges posed by the increased fabrication complexity of SiC power devices.

Soon we will take a closer look at all three techniques. But before we do, let's take a minute to review the process steps for making a simplified SiC trench MOSFET and a SiC trench insulated-gate bipolar transistor (IGBT). This is outlined in Figure 1, which illustrates the process flow for the SiC trench MOSFET, and shows the key process steps, key parameters, device performance impact and the proposed process control solution. This figure also illustrates the process flow for a SiC trench IGBT device. While the steps are very similar, there are differences. The most significant is that a SiC trench IGBT has a p^+ substrate and a n^+ buffer layer before the drift layer.

Scrutinising layers with FTIR

Incorporating a Michaelson interferometer, a broadband light source and a fast Fourier transform (FFT) algorithm, FTIR spectrometers are well suited to studying the layers of SiC devices. This technique, requiring acquisition of infrared spectra extending from the near-IR to the far-IR, is quick, non-destructive and highly sensitive to molecular and free-carrier absorption. By measuring both transmission and reflectance spectra, a single tool can measure the elemental composition of epilayers and their thickness. A well-designed system is capable of obtaining the characteristics of five epitaxial layers from a single scan.

Spectroscopy in the IR offers much insight, including values for the carrier concentration of doped semiconductors. This is possible due to free carrier absorption, a process described by the Drude model, which accounts for the frequency-dependent conductivity of metals. The Drude model can be used to calculate the plasma frequency, which depends on the concentration of free carriers and their effective mass. For wavelengths above the plasma frequency, the electric field of the incident light oscillates so fast that the material acts like a dielectric. That's not the case for wavelengths below the plasma frequency, which absorb light. Note that



➤ Figure 2. PD Epi model fitted to the experimental spectra from the FTIR system and the wafer maps for all parameters of interest.

the absorption coefficient is directly proportional to the free carrier concentration.

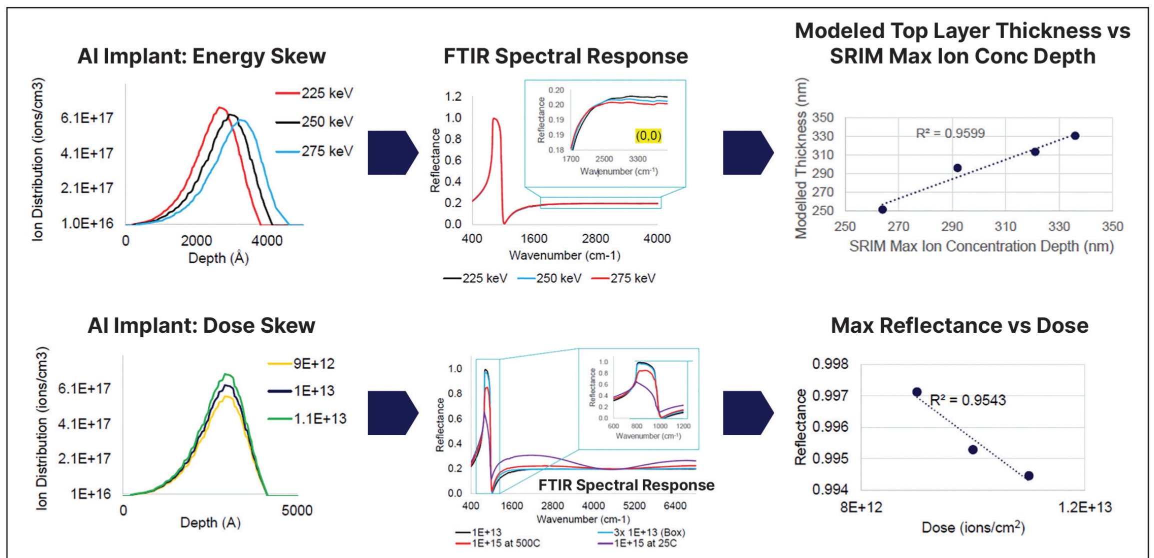
The information garnered by FTIR spectroscopy is incredibly valuable to makers of SiC trench MOSFETs and IGBTs. For the SiC MOSFETs, the thickness and the carrier concentration of the drift layer directly determines the breakdown voltage of the transistor. Meanwhile, for the IGBT, the buffer layer thickness and the free carrier concentration determine a number of key characteristics, including switching speed and conduction losses.

FTIR spectroscopy also offers great insight into the ion implantation process. Measuring the depth and free-carrier concentration of the *p*, p^+ and n^+ regions is critical, because all these features influence the channel mobility, contact resistance, threshold voltage and saturation current.

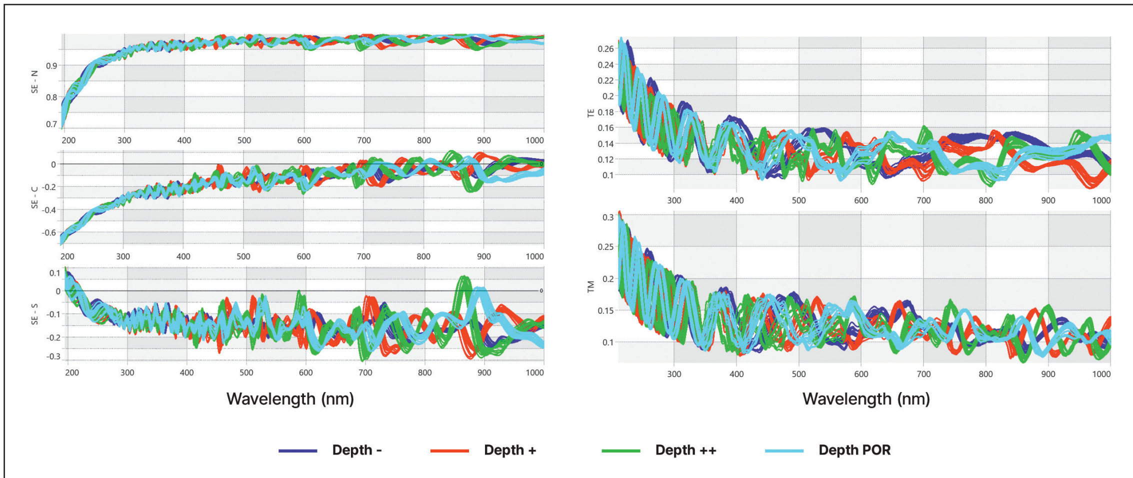
At Onto Innovation we are supporting this task, having developed a new analysis engine called PD Epi, which enables the modelling of complex epitaxial film stacks in compound semiconductors. Our analysis engine provides direct modelling of carrier concentrations and film thicknesses of multiple layers, including the substrate. Utilising Drude oscillator models and gradient layers, our engines determine the carrier concentration profile through the structure during the diffusion and implantation process.

To illustrate the power of our PD Epi model, we have used it to characterise an IGBT epiwafer. Using our model we have determined the buffer and drift layer thickness, and the carrier concentration for the buffer layer and the substrate. This study involved a Design Of Experiment (DOE) methodology, with the drift layer thickness varied from 5 μm to 30 μm. while all other parameters of interest were kept constant.

An example of results on these IGBT epiwafers, obtained with our PD Epi model and fitted to the experimental spectra from the FTIR, is shown in Figure 2, which has wafer maps for all parameters of interest. We have correlated the measured drift layer thickness to the expected thickness. This gave a coefficient of determination (R^2) exceeding 0.99, demonstrating that the predictive capabilities



➤ Figure 3. SRIM simulations for energy and dose skews, then raw FTIR spectral response to those skews and finally correlation of FTIR measurements to SRIM.



➤ Figure 4. The spectral variation of the spectroscopic ellipsometry and normal incidence reflectometry OCD channels.

of the PD Epi model are accurate. The measured precision levels – that is, the standard deviation of repeat measurements – averaged 0.2 percent for the drift layer thickness, and 8.5 percent and 2.5 percent for the buffer free-carrier concentration and substrate free-carrier concentration, respectively.

Additional capabilities of FTIR spectroscopy are measuring the implant depth of aluminium ions, and detecting dose variations of this species after the ion implantation process and prior to annealing. Normally, dopants must be activated, so that FTIR can detect the effects. However, with our PD Epi model, manufacturers can conduct their measurements prior to dopant activation.

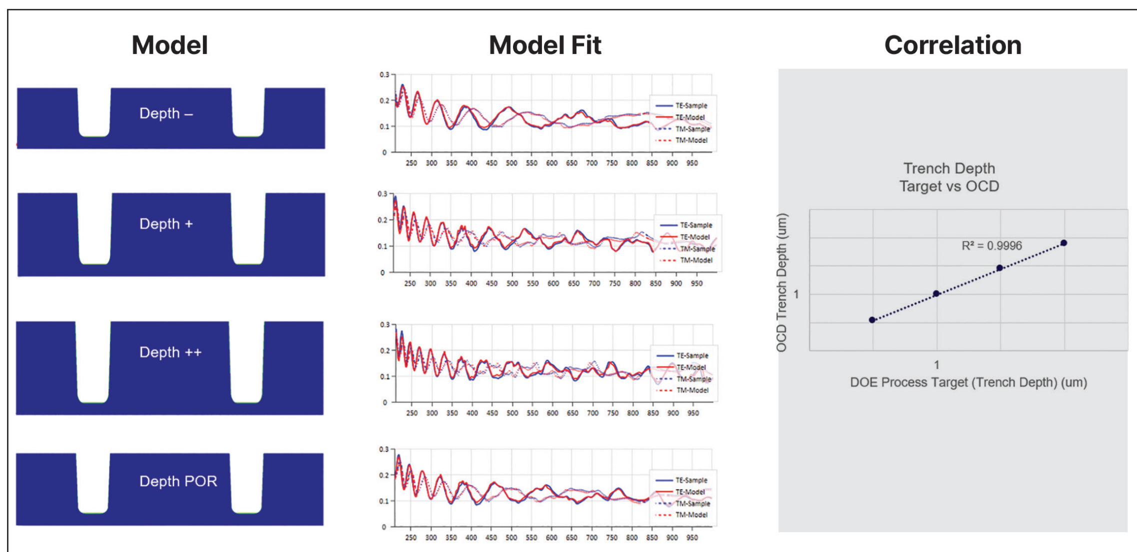
To demonstrate this, we have used FTIR spectroscopy to measure dose and energy skews. This involved simulating the stopping range of ions in matter – allowing us to then model implant depth and carrier concentrations. Using this model as a reference for our FTIR measurements, we then simulated the energy and dose skews (see Figure 3, which also shows the FTIR measurement response to the skews, and the correlation of the measurements to the SRIM simulations).

As part of this particular effort, we used a simple Drude oscillator model to determine the free-carrier concentration, while floating the thickness. The thickness results coming from this model were used to correlate peak implant depth; that correlation is roughly 0.96. Following this, we used the maximum reflectance to correlate to the dose. Again, we obtained excellent correlation.

Determining dimensions with OCD

OCD has been used in semiconductor manufacturing for over 20 years. During that time its application has shifted from top-down approaches, like critical dimension scanning electron microscopy (CD-SEM) and image-based microscopy, to OCD for dimensional metrology. Driving this move has been the need to measure re-entrant and vertically recessed structures, which are invisible to top-down metrologies. Today, OCD metrology is an indispensable part of the process control loop in high-volume manufacturing.

In contemporary thin-film and OCD systems designed for the specialty market, spectroscopic



➤ Figure 5. The physical model and the model fit to the experimental structure on the four DOE wafers.

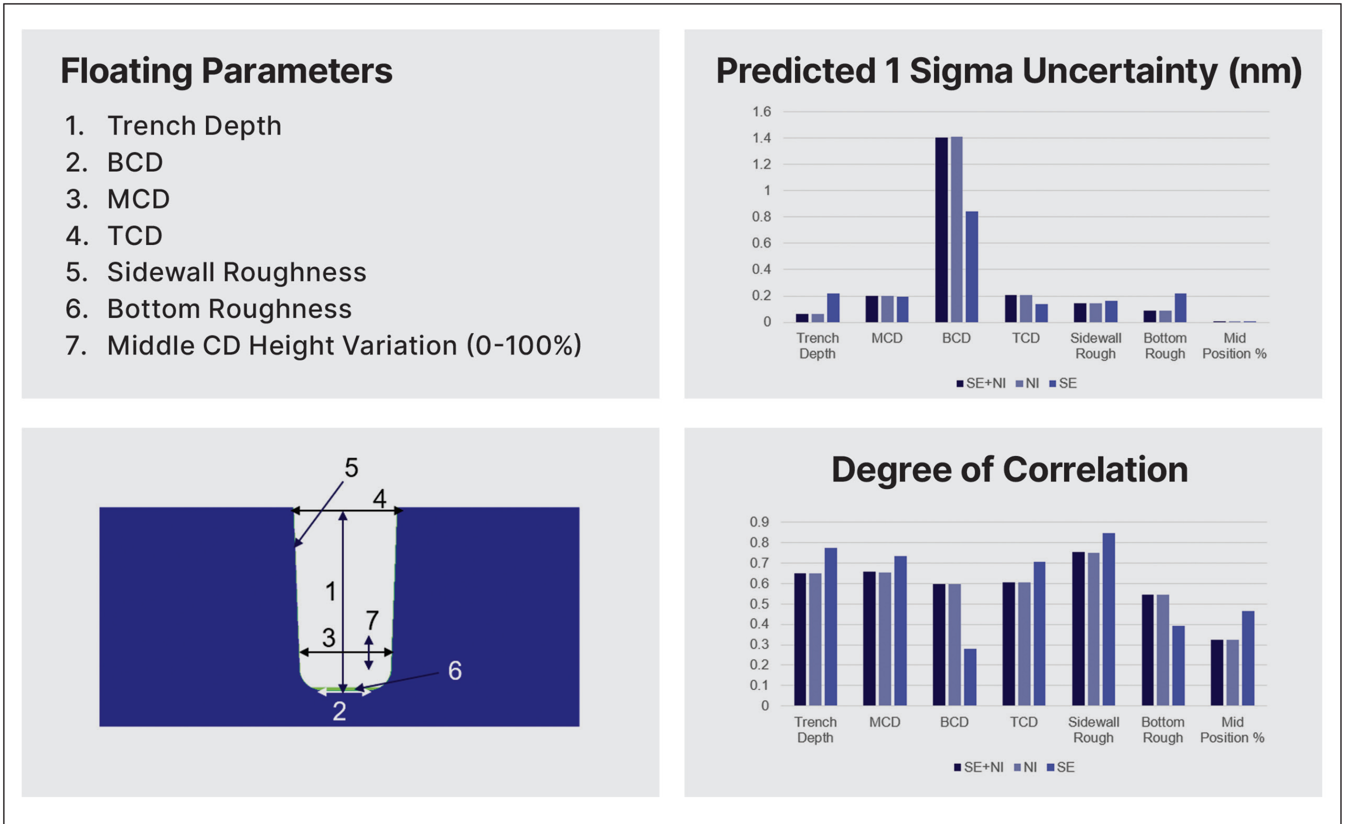


Figure 6. A comparison of simulations using spectral ellipsometry (SE), normal incidence (NI), and combined SE and NI.

ellipsometry provides the gold standard for thin-film measurements. This is employed alongside polarised spectroscopic reflectometry, which collects specular scattering spanning the deep ultraviolet to the near-infrared from periodic structures, both 2D and 3D, at oblique and normal incidence, respectively. Analysing this data with our proprietary Ai Diffract software, which is an electromagnetic solver based on advanced rigorous coupled wave analysis, allows us to extract detailed structural information. Process engineers can draw on this when running advanced process control. There are several advantages of OCD over other approaches, such as atomic force microscopy,

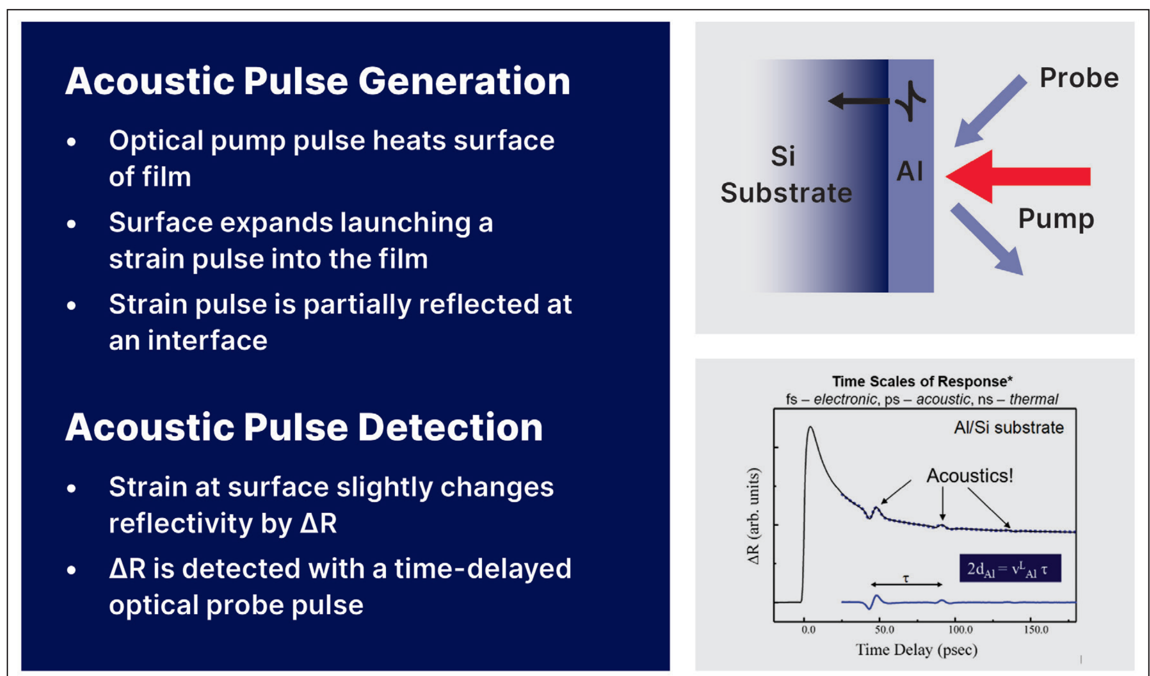


Figure7. Picoseco nd ultrasonics measurement principles. The decaying thermal component is subtracted from the signal to get the blue curve.

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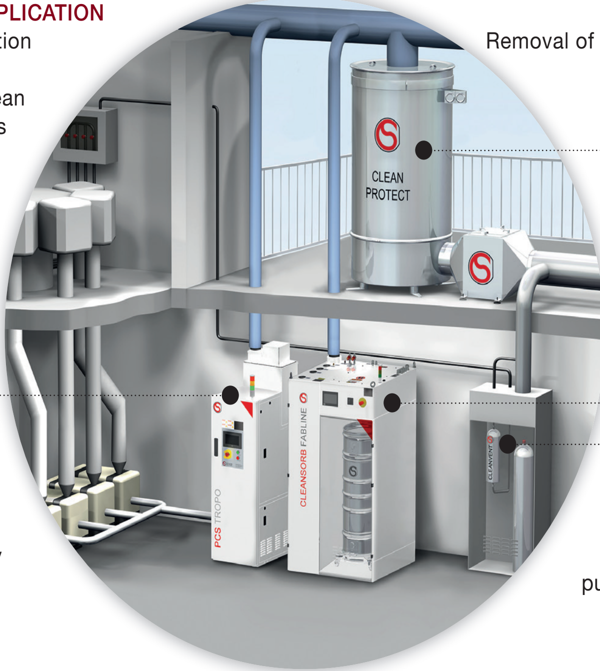

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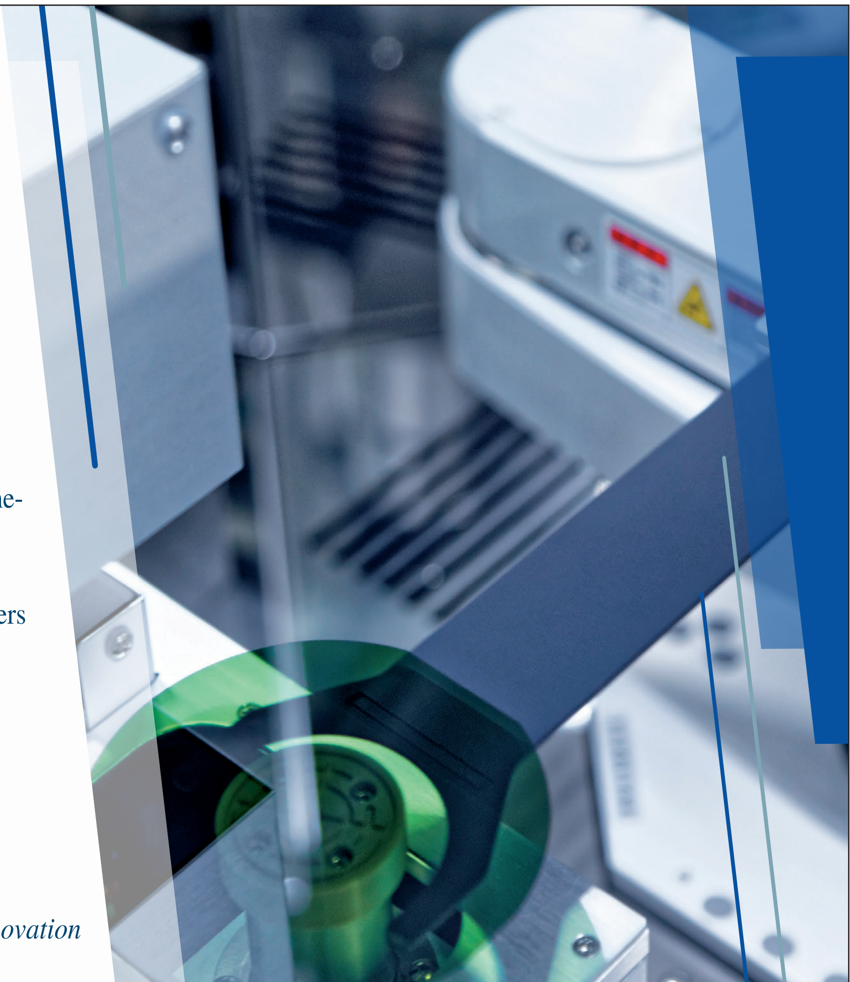


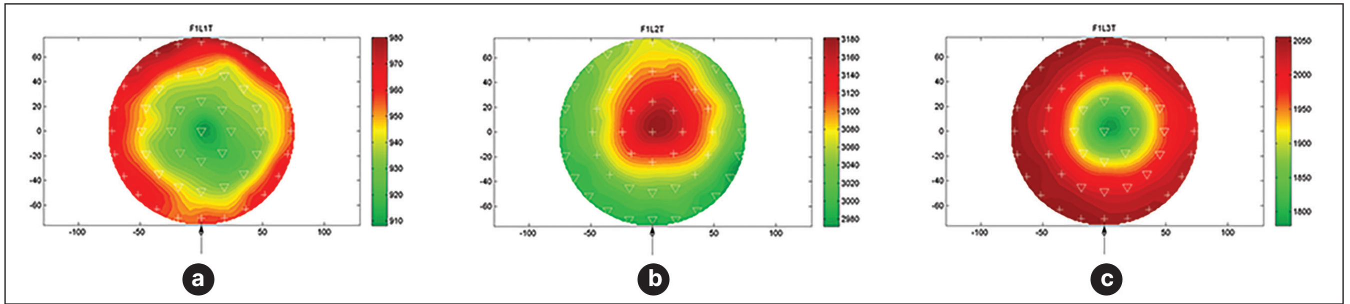


Figure 8. Forty-nine point maps of (a) Ti 1000 Å, (b) NiV 3000 Å, and (c) Ag 1500 Å.

CD-SEM, and transmission electron microscopy. Merits of OCD are that it's: non-destructive; measurements may take less than a second; it is highly precise, offering angstrom level repeatability; and it is data rich, with the capability to measure tens of parameters simultaneously in complex 3D structures. However, OCD also has a significant disadvantage: being an indirect method, it requires a model to interpret complex spectroscopic data. Due to this, OCD metrology is seen by some as inaccurate and subject to long setup times. But both these drawbacks can be avoided with a model-guided machine learning algorithm that synergizes physical modelling with machine learning.

During production of SiC trench MOSFETs, OCD can be used at the key process steps shown in Figure 1. Of particular interest are the post-trench etch measurements. The trench etch is a key step because trench parameters, like bottom width, bottom rounding, sidewall angle, depth and roughness, contribute to key performance attributes, such as breakdown voltage, on-resistance, channel mobility, and time-dependent gate oxide breakdown. Evaluating the quality of the etch is paramount, because this step is challenging, due to SiC being extremely hard, chemically stable, and having a low selectivity to SiO_2 hard masks.

To demonstrate the benefits that analysis with our Ai Diffract software brings to OCD of SiC MOSFETs, we have undertaken a DOE, processing the trench etch step on four wafers. We began by varying the etch time to skew the trench depth, and then carrying out spectroscopic ellipsometry and normal incidence reflectometry measurements (see Figure 4). Using a physical model, we fitted the data, finding an excellent correlation between the average trench depth measured with the Ai Diffract model, and the expected depth based on DOE conditions (see Figure 5).

Building on this investigation, we considered other key parameters in the model, such as the trench bottom width. It's possible to also measure these parameters. However, how do we know whether OCD has sufficient sensitivity and discrimination? To answer this, we used uncertainty and sensitivity analysis to predict specific parameter measurements (see "Uncertainty and sensitivity analysis" for details).

Following that, we used a model with Process Of Record (POR) conditions and defined seven floating parameters: trench depth, trench bottom width, trench middle width (at variable depth), trench top width, sidewall roughness, bottom roughness, and a parameter to vary the depth location of the middle width. We simulated individual OCD channels, spectral ellipsometry and spectral reflectometry measurements, and both channels together (see Figure 6). Based on results of these simulations, we concluded that combining both channels together gives the benefits that normal-incidence channel has for trench depth and that the spectral ellipsometry channel has in sensitivity to bottom CD and top

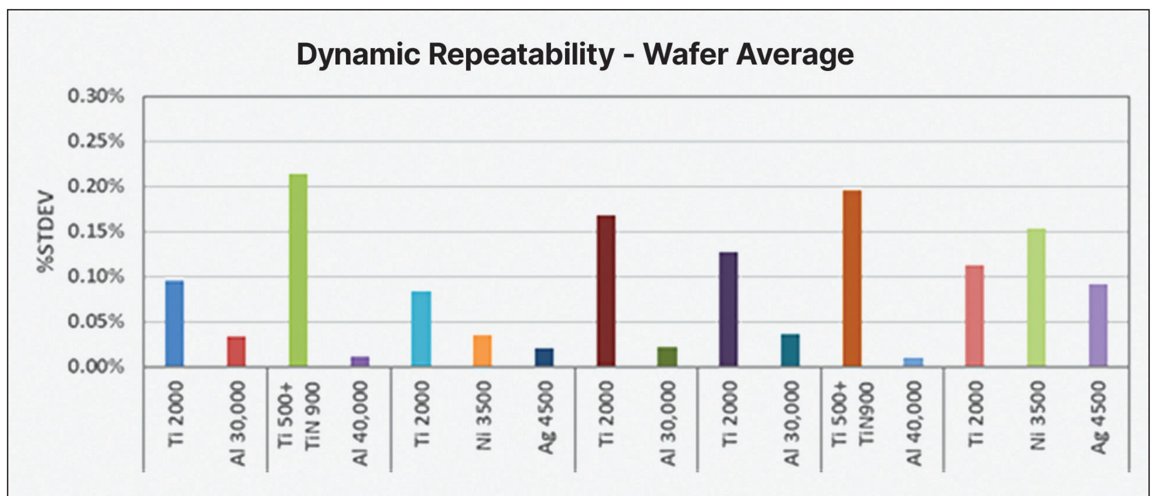


Figure 9. Repeatability performance.

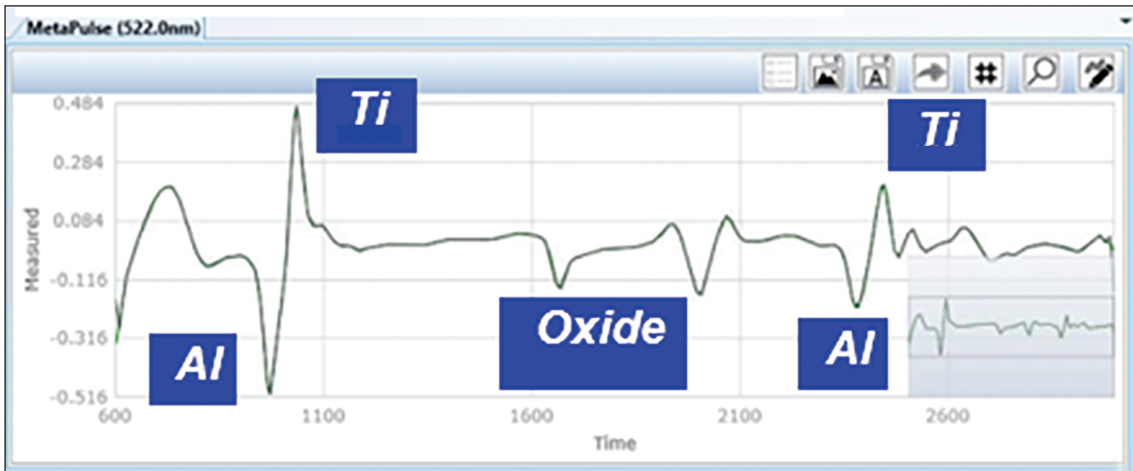


Figure 10. Multi-layer metallization stack measurement.

CD. It is clear that one can measure all the key parameters impacting device yield and performance at the trench etch step using OCD metrology, due to the low predicted parameter of uncertainty and the degree of correlation.

Pursuing picosecond ultrasonics

The third of the three process control techniques that we are recommending for producers of SiC power electronic devices is picosecond ultrasonics, a pump-probe technique using ultrafast laser pulses, typically with a duration of 200 fs. This is a very well understood and documented technique that involves focusing a pump pulse to a tight spot on the device surface, leading to the generation of a sharp acoustic wave. The resulting traveling acoustic wave reflects off various interfaces, and when it returns to the surface it changes surface reflectivity, which is measured by the time-delayed probe (see Figure 7, which provides a plot of surface reflectivity as a function of the optical probe-pulse time delay).

Picosecond ultrasonics reveals a lot of information about the material, with raw data including contributions from electronic, thermal and acoustic components. The thickness of the material may be extracted from this acoustic signature using the arrival time of the echo, and the longitudinal speed of sound in the material. Other properties such as roughness, density and elastic modulus can be characterised, depending on the application.

To provide a more thorough materials characterisation, the set-up can be used for time-domain thermos-reflectance measurements. Thanks to recent improvements in hardware, the thickness and the thermomechanical properties of a material can be characterised with a single configuration. With this non-destructive technique, chipmakers can measure multi-layer metal films simultaneously, and discriminate individual layers of repeating metal. As mechanical and thermal properties can be obtained quickly on micrometre-scale regions, spatially mapping is possible.

Showcasing the power of this technique for SiC power device manufacturers, we have used it to obtain the ohmic contact and conduction metal layer thicknesses of source and drain contacts of a SiC trench MOSFET. These measurements are highly valued, because they have a direct impact on contact resistance. In addition, the metal thickness uniformity impacts device reliability, and the metal roughness contributes to its contact resistance, due to the presence of crystallographic defects, such as micropipes, stacking faults and basal plane dislocations, as well as damage from etching and polishing steps.

Thanks to the advantages of picosecond ultrasonics, it is rapidly replacing more traditional methods such as four-point probe methodology, a destructive technique that only offers indirect thickness information and cannot detect missing layers or misprocessed wafers. Using picosecond ultrasonics, makers of SiC power devices can have far greater metallisation process control, with monitoring that includes the contact barrier (Ti/TiN), trench metallisation (W-based contacts), and both frontside and backside metallisation (Ti/NiV/Ag) stacks.

To illustrate such capability, we have produced wafer uniformity maps of a multi-layer metal stack (Ti/NiV/Ag), shown in Figure 8. Using a spot size

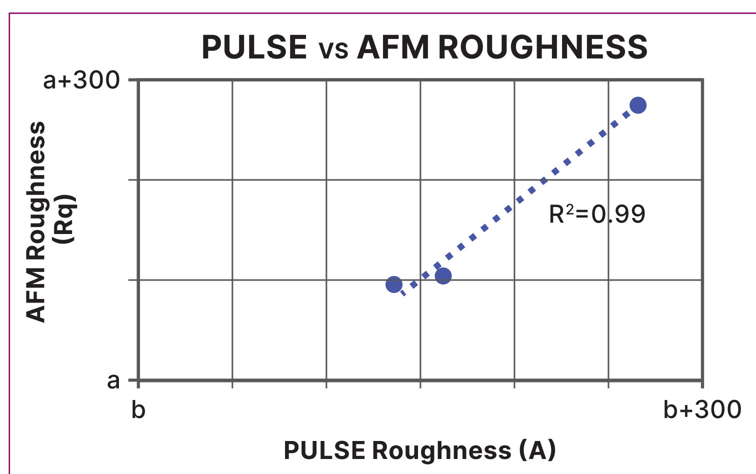


Figure 11. The correlation of PULSE measurement to transmission electron microscopy (TEM) and atomic force microscopy (AFM).

There is no doubt that power devices based on wide bandgap materials, such as SiC, are the future of the power electronics industry. Thanks to their superior properties, enabling performance enhancements over silicon-based devices, sales are climbing fast

of just 8 µm by 10 µm and a rapid measurement time – it is less than 4 s per site – it is possible to characterise full wafer uniformity. Selected metal layer stacks are highlighted in Figure 9.

We also offer an example of measurements of repeating metals in a multi-layer stack, in this case Ti/Al/Ox/Ti/Al (see Figure 10). The raw data shows an excellent signal-to-noise ratio, with echoes from every layer clearly resolved. Note that competing techniques, such as X-ray metrology, cannot provide details of individual layers in such a stack, while measurements on blanket films are not representative of product performance. To assist those running SiC fabs, recipes can be set up to flag missing layers or detect misprocessing.

As mentioned previously, in addition to thickness, picosecond ultrasonics can monitor roughness, especially for thick films (hundreds of nanometres to the micron range). Roughness provides a qualitative indicator for monitoring a well-established process. Illustrating this capability are measurements from an aluminium film (see Figure 11).

The road ahead

There is no doubt that power devices based on wide bandgap materials, such as SiC, are the future of the power electronics industry. Thanks to their superior properties, enabling performance enhancements over silicon-based devices, sales are climbing fast. According to Yole Group, global revenue will reach $6 billion by 2027. Much of that will come from the automotive industry, with Yole forecasting SiC will represent approximate 80 percent of that market.

High yield, high-volume production of SiC power devices is far from trivial. There are challenges associated with process control, which is needed in many of the key steps in the fabrication process. Offering tremendous assistance are FTIR, OCD and picosecond ultrasonics metrology – all provide SiC power device manufacturers with options to address these obstacles. And once these obstacles are removed, the highway is largely clear for high-volume manufacturing of SiC power devices.

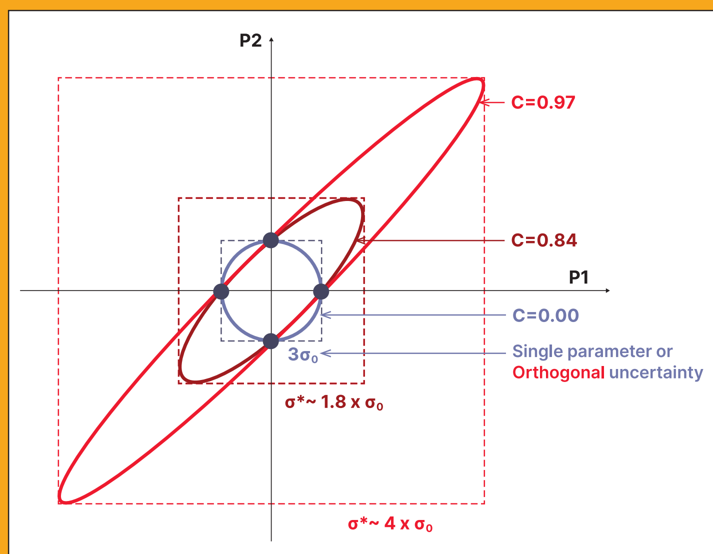
The author of this feature would like to thank the following members of the Onto Innovation team for their contributions to this article: Priya Mukundhan, Aseem Srivastava, Zhuan Liu, Andy Antonelli, and Robert Fiordalice.

Uncertainty and sensitivity analysis

IF OCD is to be employed for process control, it is critical to apply uncertainty and sensitivity analysis. This is the primary method for model optimisation and feasibility simulations, and is based on Bayesian analysis.

One input is spectral noise, which is derived from real measurements and is representative of all sources of system noise, including light source variability, detector shot noise and positional uncertainty. Another input is spectral parameter sensitivity. This is given by the partial derivative, or Jacobian, of each spectrum, with respect to each floating parameter and any weighting used in the fitting function. The output of the analysis comes in the form of a probability density function of the parameter uncertainty, given as a standard deviation.

In addition, the analysis provides an orthogonal uncertainty, or O-sigma, which is essentially parameter uncertainty from noise alone, and a degree of correlation. The latter is defined as the coefficient of multiple correlation, where the correlation between the given parameter and all other floating parameters are considered for each parameter. The figure below illustrates the impact of parameter correlation on parameter uncertainty. This plot reveals the change in the probability density function of two parameters as correlation is increased.



The impact of parameter correlation on parameter uncertainty.

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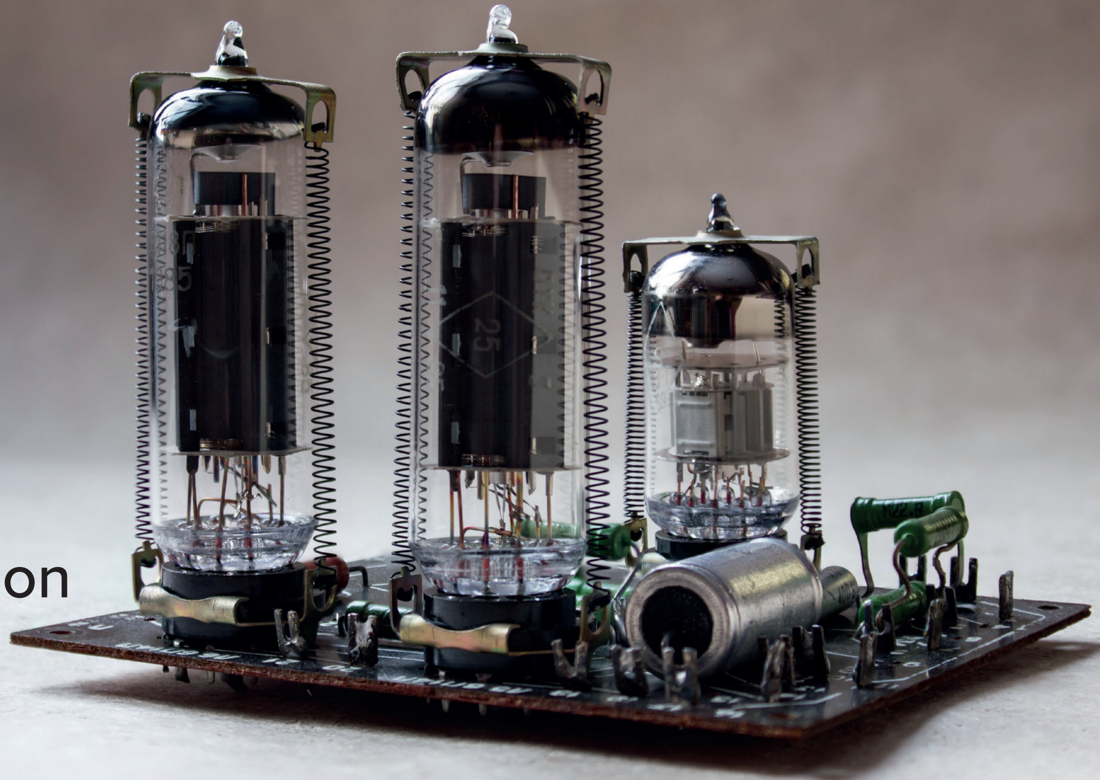


III-Nitride field-emission vacuum transistors

Field-emission transistors featuring III-Nitrides unlock the door to robust, compact vacuum-electronics-based circuits that deliver high powers at high frequencies

BY PAO-CHUAN SHIH AND TOMÁS PALACIOS FROM MIT

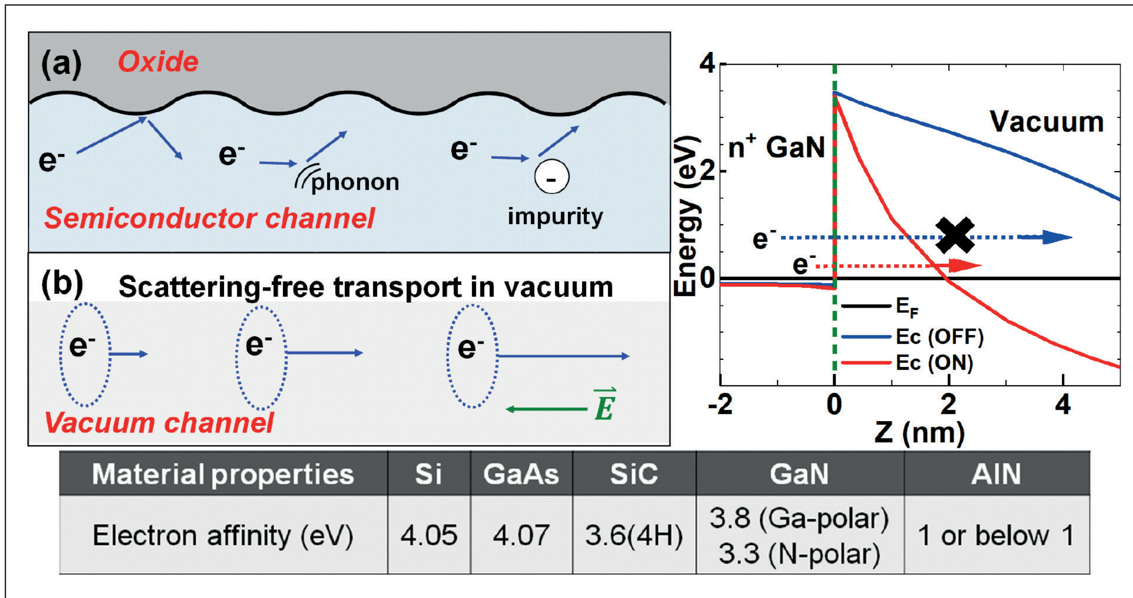
VACUUM-BASED electronics have an incredibly rich and successful history. At the beginning of the twentieth century they enabled the first electric switch, based on a vacuum triode. Vacuum tubes also lay at the heart of the first programmable general-purpose electronic computer, known as ENIAC, which was built in the 1940s. Its construction revolutionised calculation speed, being about a thousand times faster than the electro-mechanical machines of the day. However, this trailblazing computer had a substantial footprint and lacked green credentials, being 2 m by 1 m by 30 m in size, occupying 170 m^2, and consuming 150 kW of electricity.

Since the invention of solid-state transistors in 1947, semiconductor devices have gradually replaced vacuum electronics, due to lower production costs and ease of scaling. Due to this, vacuum electronics are now only used in few niche applications. Where they are still having an impact is in travelling wave tubes and klystrons, which produce intense high-frequency signals at 10-100 GHz and above 100 GHz, respectively, thanks to scattering-free electron transportation and a high breakdown field in the channel (see Figure 1). Additional merits of vacuum electronics are robustness at high temperatures and a capability to withstand radiation environments that degrade solid-state devices.

Key to leveraging the excellent potential of the vacuum channel is the injection of electrons into vacuum. A conventional approach for realising one form of electron emission, known as thermionic emission, is to heat the cathodes so that they give the electrons enough energy to overcome the work function barrier between the solid and vacuum. However, this requires high temperatures, hampering the construction of compact devices. Additional factors limiting the deployment of thermionic cathodes in large-scale circuits and systems are high power consumption, a need for cooling, and a relatively low switch speed.

Finding favour with field emission

Fortunately, all these issues can be addressed by turning to field emission. With this approach, electric fields control the tunnelling distance for the emission of electrons into vacuum. A number of semiconductors and metals have already been



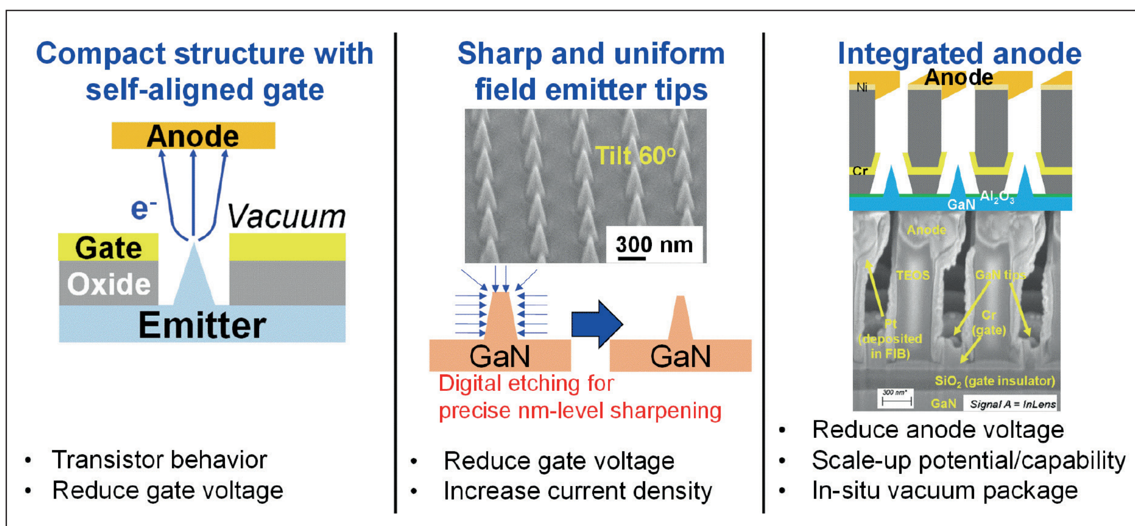
Material properties	Si	GaAs	SiC	GaN	AlN
Electron affinity (eV)	4.05	4.07	3.6(4H)	3.8 (Ga-polar) 3.3 (N-polar)	1 or below 1

➤ Figure 1. Electron transport in (a) semiconductor and (b) vacuum channels. Scattering-free transportation and a high breakdown field in vacuum make vacuum channels excellent candidates for high-power and high-frequency electronics. Theoretically, degenerately *n*-doped III-Nitrides, such as AlGaN alloys, can have a low electron emission barrier thanks to their low electron affinities, making them excellent vacuum emitters.

investigated as field emitters, but issues have often arisen, such as a limited gate control efficiency, less-than-ideal current densities, and device instability.

One class of material that promises to avoid these pitfalls is the III-Nitrides, such as GaN, AlGaN, and AlN. Recently, these compounds have been attracting attention due to their engineerable electron affinities (see Figure 1). Electron affinities reduce when the aluminium composition of the AlGaN alloy increases, and when the surface polarisation is changed from metal polar to N polar. According to theory, degenerately *n*-doped semiconductors with low electron affinities should have very low work functions, leading to a high emission current density and a low operating voltage.

Despite the great potential that III-Nitrides have for field-emission applications, research efforts have focused on ‘bottom-up’ approaches, growing these materials as nanostructures. Reports are often limited to two-terminal geometries with operating voltages usually larger than a few hundred volts.



➤ Figure 2. There are three key building blocks for compact field-emission-based vacuum transistors: a self-aligned gate, which enables transistor-like behaviour and a low operating voltage for electron emission; sharp, uniform emission tips that are critical for uniform electron emission for reduced operating voltage and high current density; and an integrated anode with an *in-situ* vacuum cavity package, which is necessary for circuit-level scale-up capability.

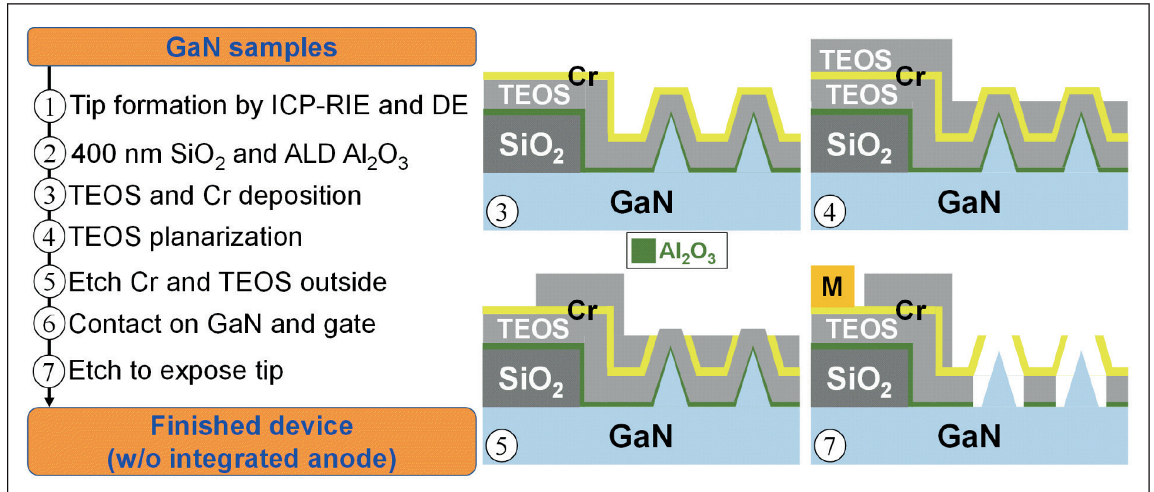


Figure 3. The process flow of the GaN field-emission-based vacuum transistors and the cross-section device diagrams after key steps. The anode electrode is not yet integrated in these devices.

The lack of a third control terminal is a significant drawback, limiting their use in applications such as power amplifiers, high-voltage switches, and computation circuits for harsh environments.

Over the last five years, our team at MIT has been developing and improving III-Nitride field-emission-based vacuum transistors. Our efforts have involved identifying three key challenges and developing new technologies to address them: (1), a compact self-aligned gate; (2), sharp and uniform field-emitter tips; and (3), an integrated anode (see Figure 2).

To tackle the lack of gate terminals, which has traditionally limited the applications of III-Nitride field emission devices, we have developed self-aligned gate structures for this class of material. For this development, we have drawn on work by other groups that developed silicon and metal field-emitter tips. Our team adopted a 'top down'

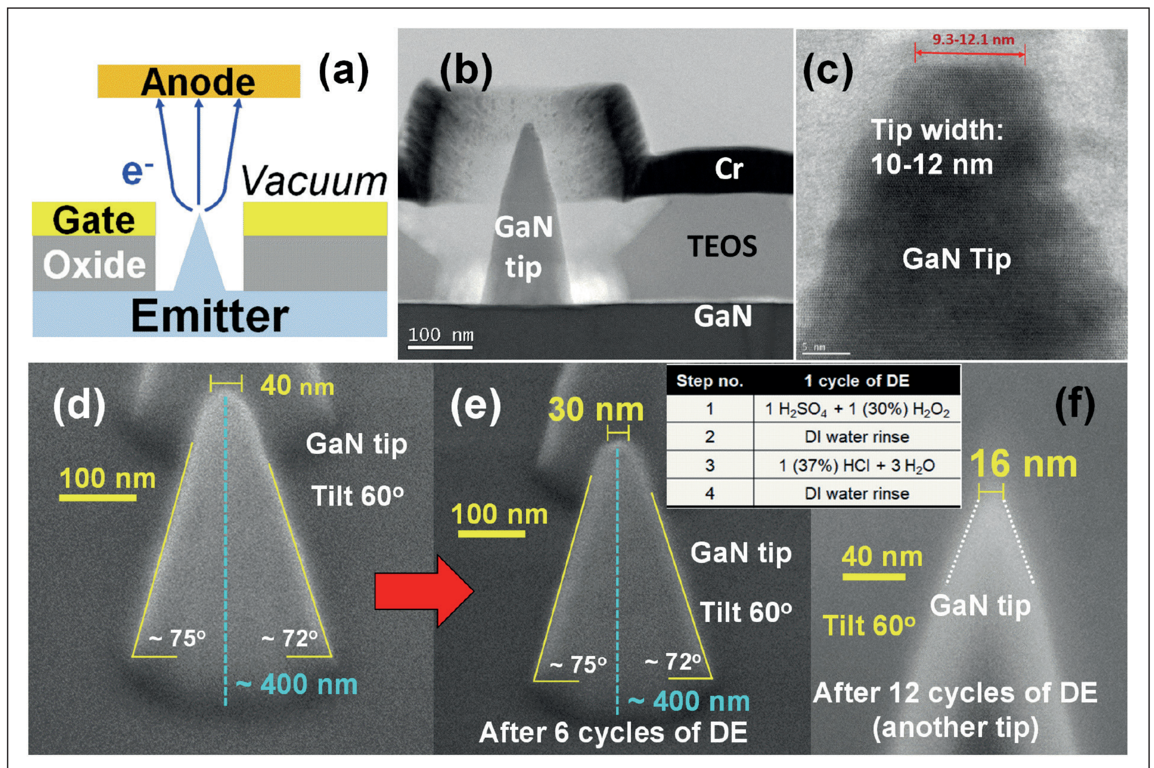
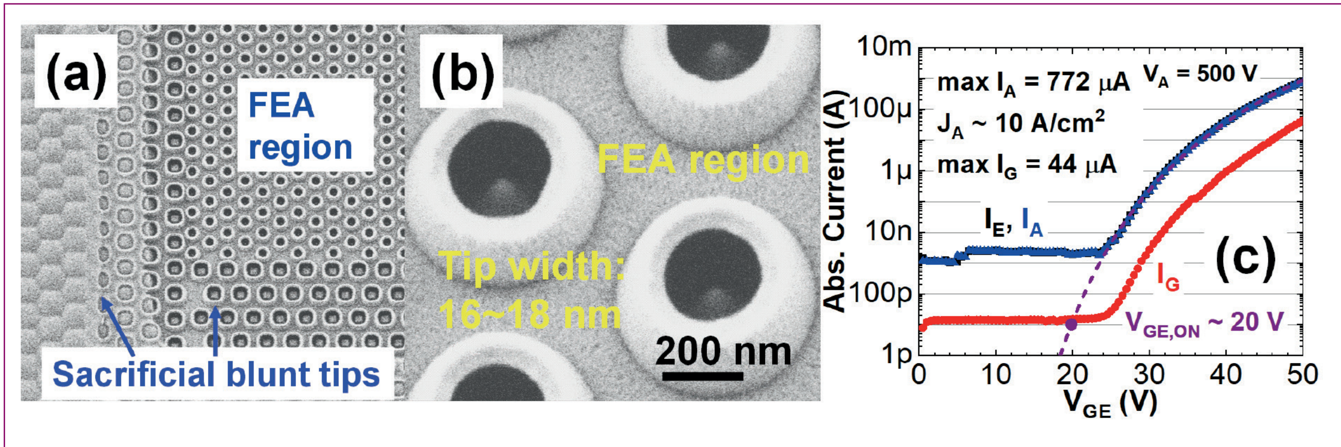


Figure 4. (a) A simplified device diagram representing measurement setup and (b) a cross-sectional scanning electron microscopy (SEM) image of the fabricated GaN emitter tip with a self-aligned gate. (c) Transmission electron microscopy (TEM) image of the GaN tip confirms the tip width of 10-12 nm. SEM images of the GaN emitter tip (d) before and (e) (f) after the digital etching (DE) confirm the effective tip sharpening of this DE technology. One cycle of DE consists of $H_2SO_4 + H_2O_2$ for oxidisation and dilute HCl for oxide removal. This process enables the fabrication of sharp and uniform tips in field emission arrays. (b) Cross-sectional SEM and (c) TEM images provided by Prof. Bruce Gnade's group at Southern Methodist University.



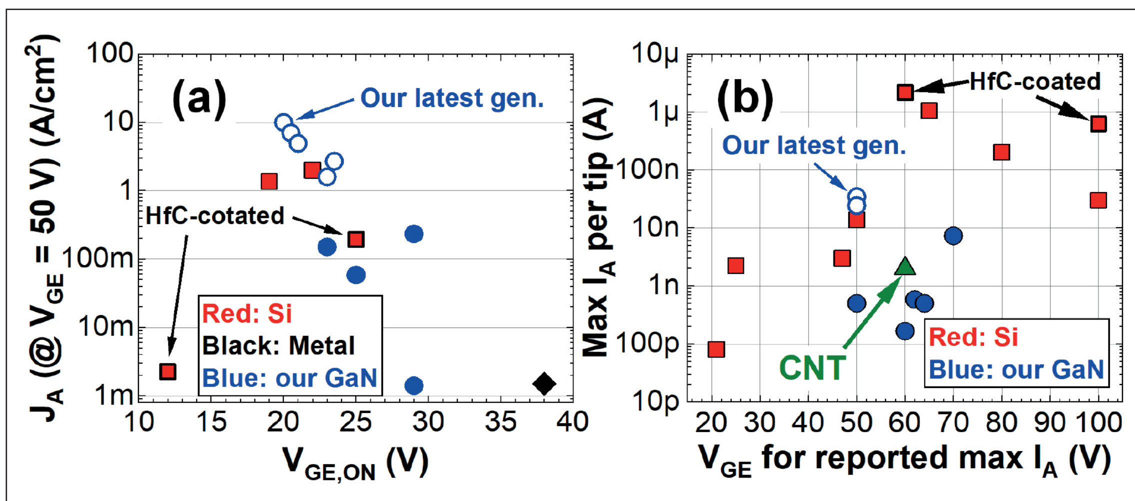
➤ Figure 5. (a) (b) Scanning electron microscopy images and (c) transfer characteristics of the state-of-the-art GaN field emitter array with a self-aligned gate. The device has good gate control of the emission current (I_E) and anode current (I_A) with an above 10^5 on-off ratio and low gate leakage (I_G), which is less than 10 percent of I_A at on state (V_{GE} = 50 V).
The fitting (purple dashed line) of the anode current confirms that the current conduction is dominated by field emission.

approach, using dry etching to produce well-organised GaN field-emitter arrays. We deposited and defined a self-aligned gate structure on these field-emitter arrays, enabling them to deliver excellent gate-control capability and a transistor-like behaviour at operating gate voltages below 100 V.

In addition to introducing a self-aligned gate, improvements to the uniformity and sharpness of field emitter tips are essential for increasing the performance of field-emission-based vacuum transistors. To ensure field emission, there's a need for high electric fields, which reduce the electron tunnelling barrier from the Fermi level to the vacuum level. This quantum tunnelling mechanism has an exponential dependence on the electric fields on the surface – the stronger the field, the higher the electron emission. It is also possible to locally enhance the electric field by altering the shape of emitter tips. Due to this, uniform and sharp tips are critical to realising uniform electron emission in field-emitter arrays, and thus ensuring an increased current density.

Our third initiative – following development of the gate structure and the GaN emitter tips – has involved the integration of the anode electrode in our state-of-the-art field emitters. By taking this step, we have been able to form three-terminal fully-integrated vacuum transistors, which are necessary for scale-up applications, such as vacuum-electronic-based integrated circuits.

Efforts on this front have enabled us to reliably produce an integrated anode with a sub-1 μm channel length. Note that we are able to alter the



➤ Figure 6. Benchmarking plots of (a) current density (J_A) versus turn-on voltage ($V_{GE,ON}$) and (b) maximum anode current per tip versus gate-emitter voltage (V_{GE}) for maximum anode current reported. These devices have the highest current density (10 A/cm²) and comparable current per tip (35 nA /tip) at V_{GE} = 50 V. The maximum current per tip of reported silicon field emission arrays at V_{GE} = 50 V is about 100 – 500 nA/tip.

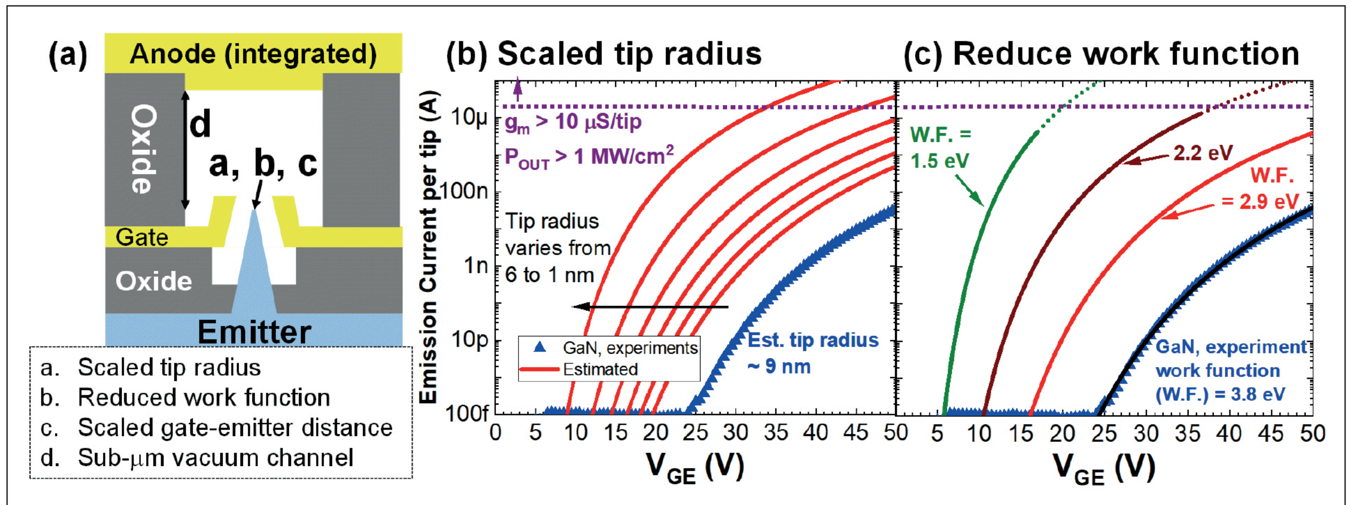


Figure 7. (a) Proposed fully-integrated field-emission-based vacuum transistors with advanced modifications for performance improvement, and the estimated emission current per tip with a (b) scaled emitter tip radius and (c) reduced work function in the emitter tip. The dashed lines in (c) indicate the region where the assumption of estimation is invalid due to high electric fields corresponding to the emitter work function. The gated emitter is assumed to have a (300 nm)2 device area and the breakdown voltage in the vacuum channel is assumed to be more than 200 V to estimate the possible output power density.

channel length by adjusting multiple parameters during device fabrication. Our approach also provides us with the potential to seal the vacuum cavity, which relaxes restrictions on vacuum packaging and circuit-level integration. We will soon publish the details of our anode-integration technology and describe its impact on device performance.

Engineering the emitter

Etching and cleaning steps have been used to fabricate our III-Nitride field-emitter transistors (see Figure 3 for an overview of the main steps). We begin with GaN-on-silicon coupons, which are cut from a 6-inch wafer. Using plasma dry etching with nickel hard mask that's defined by an e-beam lithography and lift-off process, we form GaN field emitter arrays on these coupons. The tips of the GaN emitters are sharpened by wet-based digital etching (see Figure 4, as well as Step 1 in Figure 3).

During one cycle of digital etching, the sample is initially treated with a mixture of H_2SO4 and H_2O_2 to oxidise the GaN surface (step 1). After this, deionised water removes the residual chemicals (step 2), before the surface oxide layer is etched away with dilute HCl (step 3), and the sample rinsed once more by deionised water (step 4). Following a few cycles of digital etching, it's imperative to renew the chemicals, because H_2O_2 decomposes and the temperature of the mixture of H_2SO_4 and H_2O_2 decrease over time. We have found that three cycles of this wet-based digital etch sharpen Ga-polar GaN pyramid tips by 5 nm, enabling reliable fabrication of uniform GaN emitter tips with a sub-20-nm tip width in field-emitter arrays.

After forming GaN field-emitter arrays with sub-20-nm emitter tips, we deposit SiO_2 and Al_2O_3 by PECVD and ALD, respectively (step 2 in Figure 3). Adding a SiO_2 layer improves device stability under the gate pad region, while coating with Al_2O_3 protects the sharpened GaN emitter tips from subsequent fabrication steps, key to ensuring a high fabrication yield and good device performance.

These subsequent fabrication steps begin with the addition of a SiO_2 layer by PECVD, using a tetraethyl orthosilicate (TEOS) precursor. The growth of a conformal chromium layer by sputtering follows (step 3 in Figure 3). It is the SiO_2 and chromium layers that form the gate stack of the GaN field-emission vacuum transistors.

Finally, we deposit a thick SiO_2 layer with the TEOS precursor by PECVD. We then planarize the device surface through carefully timed dry etching on this TEOS SiO_2 layer (step 4 in Figure 3). We then dry etch the chromium gate metal on top of the emitter tips, with the TEOS SiO_2 layer acting as a hard mask (step 5 in Figure 3). After forming metal contacts on both GaN and the gate metal, chromium, GaN emitter tips are exposed by a carefully timed dry etch. A short wet etch using a buffered oxide etchant then removes the remaining SiO_2 layer and the protective Al_2O_3 layer (step 7 in Figure 3). Using this process, we have reproducibly fabricated three different generations of GaN field-emitter arrays with self-aligned gates and sub-20-nm tip widths.

Promising potential

We have characterised our field emitter arrays in an ultra-high vacuum chamber with a base pressure below 2 x 10^{-9} Torr. When determining transfer characteristics, we applied a gate-emitter bias voltage (V_{GE}) to extract electrons out from the emitter tips, and used a high voltage on the suspended anode terminal – between 500 V and 1000 V – to

collect the emitted electrons (as shown in Figure 4 (a)). While we could adjust the anode-emitter distance by moving the sample stage up and down, for all our measurements we fixed this distance to 1-2 mm.

Our latest generation of GaN field-emitter arrays feature self-aligned gates with uniform sharp tips in the array, surrounded by sacrificial blunt tips that help manage the peak electric field in dielectric layers, leading to improved device stability (see Figure 5 (a) and (b)). Our best field-emitter arrays have a good on-off ratio in anode current, a low gate leakage (it is less than 10 percent of the anode current in the on state), and a current density of 10 A cm^{-2} at a gate-emitter voltage of 50 V – to our knowledge, that's the highest current density among all the field-emitter arrays reported in the literature (see Figure 6 (a)). Note that the relatively high noise levels in the emitter and anode currents are a measurement artefact related to the high-voltage source measure units. The current-voltage curves can be well fitted by field emission equations, such as the Murphy-Good model.

Thanks to the combination of a compact self-aligned gate structure and uniform and sharp GaN emitter tips, our field-emitter arrays are state-of-the-art for III-Nitride field emission devices, and deliver the highest field-emitted current density in the literature at a gate-emitter voltage of 50 V (see Figure 6 (a)). For these structures, the current density is based on the total device area for the field-emitter array with its self-aligned gate.

In addition to the current density, a key metric for these field-emitter arrays is the emission current per tip. Ideally arrays have a high average emission current per tip under low bias conditions, because this enables these devices to deliver a high level of efficiency when serving in integrated circuits and power applications. Our best GaN field-emitter arrays have a maximum average-emission-current-per-tip of 35 nA, while those based on HfC-coated silicon field-emitter tips have demonstrated 100-500 nA per tip, also for a gate-emitter voltage of 50 V. Based on these results, it is clear that there is still room for improvement in the current density in III-Nitride devices.

We have identified significant opportunities for making additional gains in device performance. These pathways include: reducing the gate-emitter distance, now about 150 nm, to enable an increase in gate control over electron emission from the emitter tips (see Figure 7 (a)); sharpening the tip width to below 10 nm, to enhance the local electric field (see Figure 7 (b)); and leveraging low-electron-affinity III-Nitride semiconductors or low-work-function materials (see Figure 7 (c)).

Initial efforts on these fronts have included the fabrication of silicon field-emitter arrays with a gate-emitter distance below 50 nm and a sub-5-nm tip radius in prior work. Encouragingly, the turn-on voltage – that is, the gate-emitter voltage to turn the device on – is around just 10 V. However, these devices suffer from performance variations, associated with tip-size variability and the narrow device geometry.

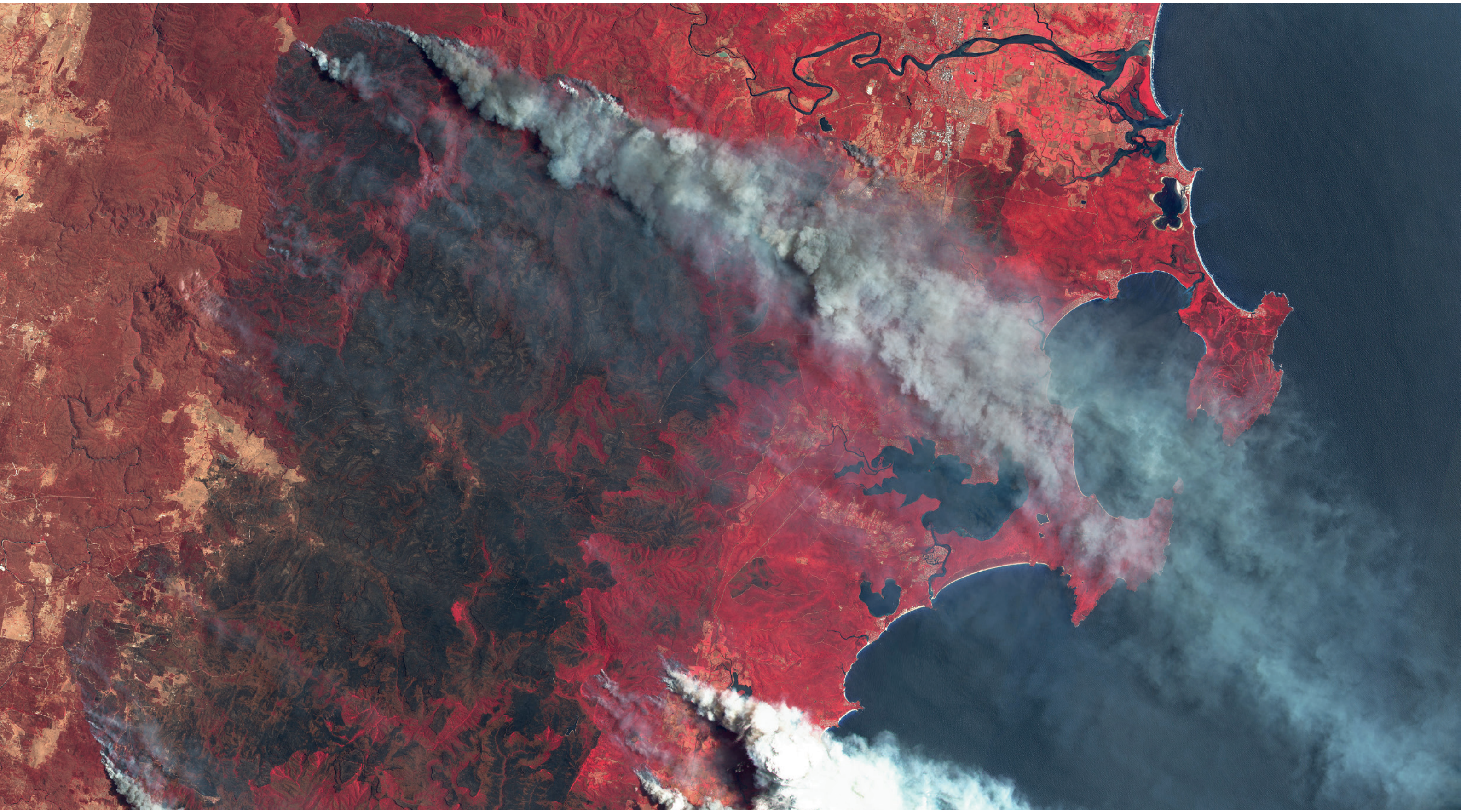
Thanks to the combination of a compact self-aligned gate structure and uniform and sharp GaN emitter tips, our field-emitter arrays are state-of-the-art for III-Nitride field emission devices, and deliver the highest field-emitted current density in the literature at a gate-emitter voltage of 50 V

We hope that by leveraging the low-electron-affinity of III-Nitride materials and the polarisation engineering of the surface dipole, we will be able to produce field emitters with an even lower work function and a reduced energy barrier for electron emission (see Figure 7 (c)). Nevertheless, our preliminary experiments on both n^+ aluminium-rich AlGaN and n^+ N-polar GaN are yet to offer a clear improvement in device performance. To address this particular shortcoming, we plan to undertake a material-dependent optimisation of the etching processes for emitter tip formation.

While there is still more work to do, we have a strong foundation to build on. Our GaN field-emitter arrays with a self-aligned gate and uniform, sharp emitter tips have enabled us to demonstrate state-of-the-art field-emission-based vacuum transistors with the highest current density at a gate-emitter voltage of 50 V. Once we have made further improvements in performance by integrating anode structures and applying advanced materials engineering we are confident that our III-Nitride field-emission-based vacuum transistors will be able to play an important role in tomorrow's high-frequency, high-power, and harsh-environment electronics.

FURTHER READING / REFERENCE

- Pao-Chuan Shih *et al.* "Self-Align-Gated GaN Field Emitter Arrays Sharpened by A Digital Etching Process," IEEE Electron Dev. Lett. **43** 422 (2021)
- Pao-Chuan Shih *et al.* "Wet-based digital etching on GaN and AlGaN," Appl. Phys. Lett. **120** 022101 (2022)
- Pao-Chuan Shih *et al.*. "GaN Field Emitter Arrays with J_A of 10 A/cm^2 at V_{GE} = 50 V for Power Applications," 68th International Electron Devices Meeting (IEDM), December 2022
- Pao-Chuan Shih, "Vacuum Transistors Based on III-Nitrides Field Emitter Arrays with Self-Aligned Gate," PhD Dissertation, Massachusetts Institute of Technology, 2023.



Antimonides enhance avalanche photodiodes

Turning to antimonides for the fabrication of avalanche photodiodes delivers high gain in the infrared, while quashing excess noise

BY SANJAY KRISHNA FROM THE OHIO STATE UNIVERSITY

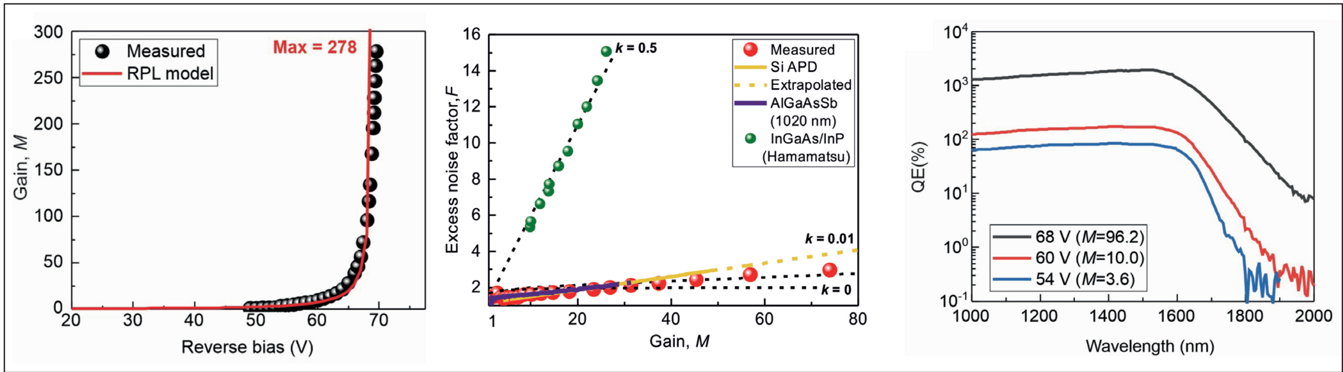
IN DAYS GONE BY, we had the weather after the news. But now the weather is the news – well, to be fair, not all of it, but certainly more than ever before. Take this year, for example. During the summer the various social media platforms focused coverage on exceptional heat waves in the US, central Europe and China that sparked substantial wildfires. More recently, it's pictures of floods that fill our screens, with torrential rain causing bursting of dams in Libya.

A contributing factor behind all these extreme weather events is global warming, fuelled by ever higher greenhouse gas emissions. In order to tackle climate change, it is crucial to monitor these emissions as we implement emissions reduction efforts.

One option for observing the emission of gases that contribute to global warming is the deployment of instruments on the ground. But this is incredibly time-consuming, expensive, and provides only limited coverage. Far better is to equip satellites with suitable remote sensing instruments, which gather timely and continuous data as they orbit the globe.

A suitable technology for observing the Earth's greenhouse gas emissions from space is lidar. Lidar, which stands for light detection and ranging, is similar to radar but uses lasers and optics instead of microwave radiation. Lidar instruments can be fitted onboard satellites, including the International Space Station, allowing measurements at an altitude of 400 km.

Lidar is now a reasonably mature technology, in part due to its recent proliferation in self-driving cars and autonomous airborne drones. Regardless of application, lidar systems consist of a laser, transmission optics, receive optics, an infrared detector and backend electronic circuits, and an optional display for the user interface. However, the range and range resolution of the lidar system on a self-driving car is very different from that required on a satellite.



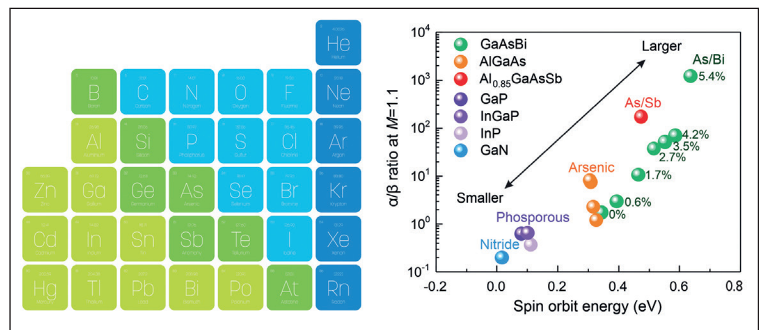
➤ Figure 1. Room temperature measurement of high gain, low excess noise and large spectral quantum efficiency in the short-wave infrared (SWIR) using a GaAsSb/AlGaAsSb heterostructure design on an InP substrate (Lee et al, Optica, 2023).

Designs for lidar

The detector is just one of key components in any active sensing and imaging system. In such systems, including lidar, there are five key components. The first of these is a transmitter, usually either a laser or an LED, that provides an incident beam. The light source is either focused at a particular target, flood illuminated or flashed across a field of view, or scanned across a scene in one or two dimensions to generate a cloud point image. The second component is the optics, which can be divided into front-end transmission and back-end collection. Depending on system design, the optics may use a single aperture (mono-static) or two separate apertures (bi-static) for illumination and collection. The third component is the back-end receiver, based on a photodetector that converts collected photons into electrons to create a photocurrent; and the fourth element is a back-end electronic circuit, which converts the photocurrent into a photovoltage, using an analogue-to-digital converter to generate digitized bits of information. The fifth component is the software and an optional graphical user interface (GUI) for applications in which there is a human-in-the-loop for decision making. The software provides the timing for the front-end transmission and the back-end information processing. The GUI serves as the interface for the user to customise the system to extract the relevant information pertinent to their application. To meet customer performance targets and price points, system-level integration of these five components demands a careful architectural design.

One key consideration facing the designers of lidar systems is the operating wavelength. Today's systems are limited to near-infrared wavelengths of around 1 µm or less, primarily because the photoresponse of mature, inexpensive silicon-based detectors and arrays falls off dramatically at longer wavelengths. Similarly shorter wavelength lasers are cheaper and more mature than their longer wavelength counterparts. However, there is much merit in extending lidar systems to longer wavelengths, such as 1.55 µm. Systems operating around that wavelength are inherently eye-safe, since any reflected or scattered light that enters the eye is absorbed by anterior portions, mainly the cornea, so never reach the retina. Infrared wavelengths also undergo far less absorption in the atmosphere, thereby extending the range of the lidar system, an asset for gathering data from space. Moreover, the infrared wavelength is sensitive to vibration of the hydrocarbon atoms, ensuring sensitivity to greenhouse gases such as methane and carbone dioxide. Key to extending the capabilities of lidar to longer wavelengths is to replace silicon, which is held back by the intrinsic physical limitation of its bandgap, with compound semiconductor materials with a narrower bandgap.

Lidar system engineers must ask themselves several key questions, which form a 'decision tree' determining the selection of various key components, but especially the detector. One crucial decision is whether the application is for sensing/imaging, or for ranging. Photon budget calculations are also required, determining whether the detector should be an avalanche photodiode (APD), which has a higher sensitivity, or a *p-i-n* diode. Here we discuss the later, a linear-mode APD. Our focus is on our advances in the figures of merit of this critical component by our team at The Ohio State University.



➤ Figure 2. Variation of the impact ionisation ratio of electrons and hole (α/β) versus spin-orbit energy for various compound semiconductor materials from nitrides, phosphides, arsenides and antimonides to bismides. This trend seems to suggest that there is an interesting correlation between the size of the atom in the periodic table and the spin-orbit/impact ionisation mechanisms.

Members of the Krishna Infrared Detector (KIND) laboratory at Ohio State University.

APDs provide internal gain using impact ionisation and this increases the sensitivity of the receiver. When increasing the reverse bias of a photodiode close to its breakdown voltage, impact ionisation may be realised by optimising the doping, bandgap and thickness of the semiconductor heterostructure stack. Note that impact ionisation occurs when a primary electron, or hole, gains enough energy under a high electric field – the energy must be far more than the bandgap of the material – to knock off secondary electrons or holes. When this occurs, a multiplication process results that provides internal gain, increasing the photocurrent (and unfortunately the dark current too).

APD architectures

APDs fall into two categories: those that operate in linear mode, and those that are referred to as Geiger mode.

For linear-mode APDs, as the name suggests, the multiplied photocurrent is proportional to the primary photocurrent, with the proportionality constant a figure of merit called multiplication gain. Unfortunately, due to the stochastic nature of the impact ionisation process, there is an excess noise that also arises – and it is dependent on the gain. In other words, excess noise increases as the gain is increased.

Geiger-mode APDs operate in a markedly different manner, delivering a large burst of current when detecting incident photons. For this class of APD, output is not proportional to the number of incident photons, and a quenching circuit tends to be incorporated to limit the current in the circuit. In Geiger mode configuration, it's possible to produce single-photon APDs, offering ultimate sensitivity. However, Geiger mode devices requires more complex circuitry, and they are susceptible to damage from stray light.

For the linear-mode and Geiger-mode APDs, the key figures of merit are very different, as well as the semiconductor heterostructure architecture and design. The focus of our team has been on short-wave infrared linear-mode APDs, formed by growing antimonide-based heterostructures on InP substrates.

To optimise the performance of linear-mode APDs, one should maximise the quantum efficiency and gain, while minimising bulk dark current, surface dark current and excess noise. While optimising these five parameters, there's a need to adhere to constraints placed by the system designer and the application engineer, such as those relating to size, weight, power, cost, operating temperature, allowed bias voltage, radiation hardness and environmental stability. For a given linear-mode APD technology, the device designer must also understand the component that is limiting the signal-to-noise ratio and optimise the device architecture and material stack accordingly.

Our research group takes all of these considerations into account when developing antimonide-based APDs on InP substrates that incorporate a separate absorption charge and multiplication design. Note that this foundation makes a lot of sense for our devices, given that InP substrates are available in large diameters, and there is significant development of silicon-based photonic devices using InP substrates. With our design we have realised the highest reported gain and the lowest excess noise factor at room temperature in the short-wave infrared region (see Figure 1).

While our antimonide-based APDs demonstrate promising performance, we still need to address several challenges in semiconductor design, epitaxial growth, surface passivation and radiometric testing.

Geiger-mode APDs operate in a markedly different manner, delivering a large burst of current when detecting incident photons

There are two directions of research with these material systems. One is toward the understanding of the underlying physics of the multiplier portion. We are now reaching the point where we need to go beyond the McIntyre model, which provides a well-known analytical formula for the excess noise factor associated with avalanche photodiodes, to models offering a true deterministic gain. Taking this step would allow us to pinpoint the location of the impact ionisation event and the value of the impact ionisation coefficient. Our initial experiments and modelling with antimony-containing compounds suggest that they have increased spin-orbit coupling, leading to alloy scattering as the dominant scattering mechanism. This has important consequences, such as low excess noise factors and a low breakdown voltage coefficient – both require further investigation.

Our second direction of research is the pursuit of higher sensitivity and speed. Applications such as lidar, remote sensing, and 3D imaging are going to push the limits of the performance of the APD, so choices must be made related to device optimisation parameters. The use of antimonide materials in Geiger-mode APDs could also be interesting. However, this will require careful understanding of the defect states in these materials, as well as the carrier dynamics that limit after-pulsing and dead time. Finally, if true photon resolving detectors are developed, this could unleash new frontiers for APDs and create new applications in areas like quantum information sciences and long-range remote sensing.

For the latter, progress can't come fast enough. While it's a step too far to suggest that humanity depends on better detectors, having them will improve the monitoring of greenhouse gases, a crucial first step to curbing global warming, undoubtedly the biggest issue facing us all in the twenty-first century.

We would like to acknowledge our group members and our collaboration with Prof. Joe Campbell, Prof. John David and Prof. Grein's research groups. We acknowledge the support of Directed Energy–Joint Technology Office (DE-JTO) and NASA's Earth Science Technology Office (ESTO).

FURTHER READING

- Krishna *et al*. "Linear Mode Avalanche Photodiodes With Antimonide Multipliers on InP Substrates." IEEE Journal of Quantum Electronics **58** 1 (2022)
- S. Lee *et al*. "High gain, low noise 1550nm GaAsSb/AlGaAsSb avalanche photodiodes" Optica **10** 147 (2023)

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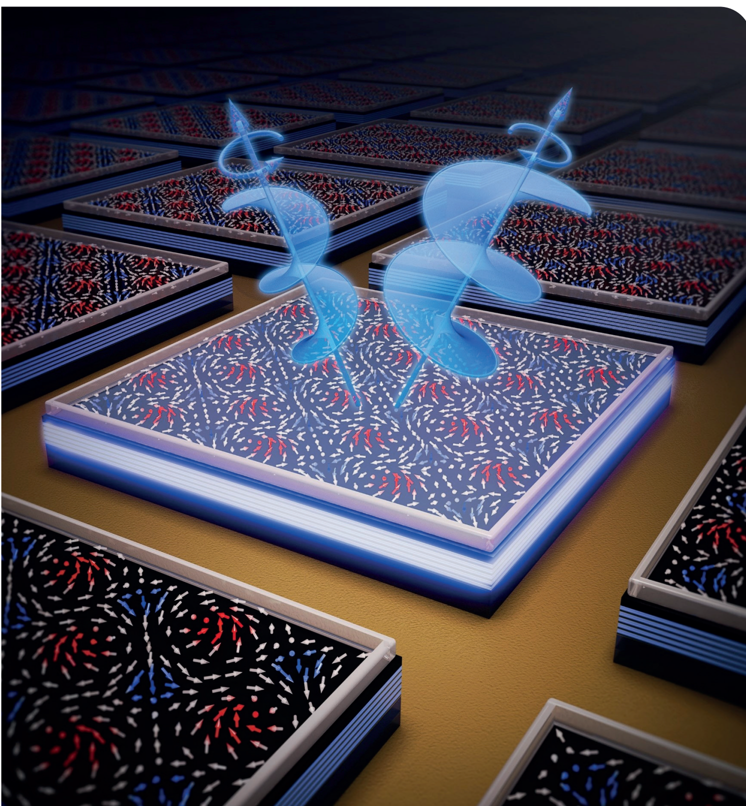
Realising chiral emission with topological LEDs

Applying strong magnetic fields during crystal growth enables the fabrication of LEDs that transfer chirality from electrons to photons

BY JUNYONG KANG FROM XIAMEN UNIVERSITY

THE REVOLUTION in the sharing of information is underpinned by the highly efficient processing, storage and transmission of data. For the latter, information is sent and received over optical networks, with data encoded through effective modulation of the amplitude or phase of the transmitted light. However, despite the ubiquity of this approach, it is not without weakness. One major drawback is that external perturbations and attenuations compromise the quality of this form of optical communication. So significant is this issue that the technology of today will fail to meet the challenges associated with tomorrow's wide-band, high-speed data transmission.

Offering a solution to this important problem is chirality, an intrinsic feature of the photon. By encoding photons with different chirality, namely either the left-handed or the right-handed form, networks will be able to efficiently transfer binary information while offering a much stronger resistance to background noise. That's not the only merit, however: encoding light with phase and chirality will also enable highly stable quantum key distribution, crucial to secret communication.



The chirality of a photon is closely related to the spin of an electron. To ensure simplicity and elegance, rather than using polarised optical elements to realise chirality, existing chiral photon sources employ spin-polarised materials. Such structures enable the transfer of electron spin to photon chirality via spin injection. However, chiral selectivity is far from ideal, due to constraints in spin polarisation and spin injection efficiency. Additional impediments to producing high-performance, practical systems are the need to use external magnetic fields or low temperatures to suppress electromagnetic or thermal perturbations. Substantial strides have to be made in stability and polarisation, in order to develop high-performance chiral photon s ources.

Turning to topology

A very promising way forward involves the use of a relatively new class of materials. For this particular family, characteristics depend not only on what the material is made from, but how it is arranged. Due to this rather striking behaviour, such materials are known as topological structures, named after a branch of mathematics known as topology.

Researchers discovered the first topological structures, which were insulators, as far back as 2007. In such materials, electrons zip along edges or surfaces in a manner that does not change under deformation of the material. Over the intervening years, the range of topological materials has expended to include photonic topological insulators – structures with photons zipping around the edges and surfaces – and topological superconductors and semimetals.

Within this growing family are those that involve the spin of the electron. Within this subset are skyrmions and merons – they feature vortex-like spin textures in magnetic thin films that exist out-of-plane and in-plane, respectively. Due to their unique topological protection features, skyrmions and merons have a higher stability than conventional electronic materials.

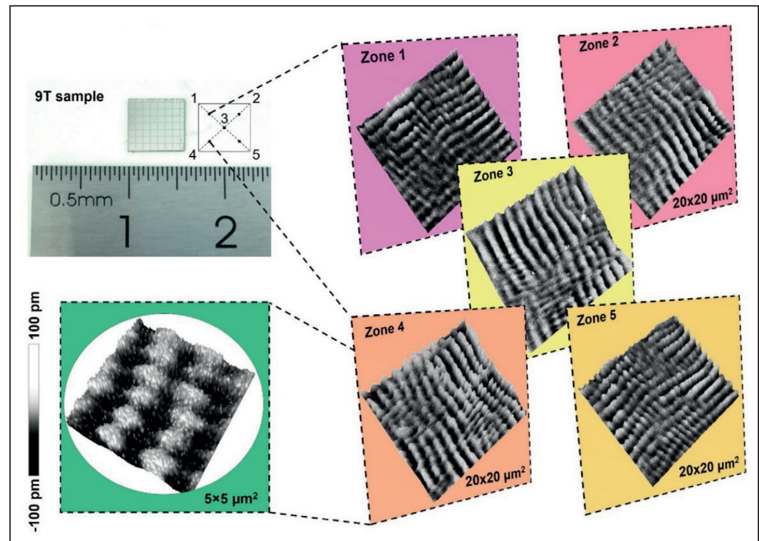
Our team at Xiamen University is trying to seize on this asset, which promises to address the stability bottleneck in polarised materials. Breaking new ground, we are pioneering the introduction of topological spin structures for chiral photon sources.

We are not the first to produce a topological spin structure. There are already a handful of reports of experimental success by other groups. However, device applications are hindered by a limited lattice scale, as well as strict temperature or magnetic field requirements. What's needed to realise the practical application of topological spin structures in chiral photon sources is the fabrication of large-scale ordered topological lattices that exist at room temperature and without a magnetic field – with the latter of these requirements needing to be solved first.

Success on this front needs the nucleation of topological order in magnetic systems. This can be accomplished with a strong Dzyaloshinsky Moriya interaction (DMI), which is an asymmetric exchange interaction originating from strong spin-orbit coupling. The DMI is associated with the orientation of *d*-orbitals in typical metallic magnets. Unfortunately, manipulating the orbital orientation is challenging, with no solution forthcoming for many years.

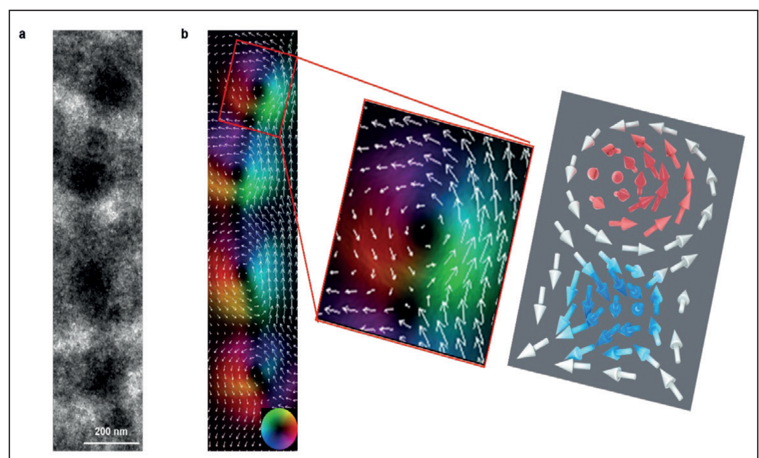
Offering a breakthrough is our latest work, which draws on our experience in growing magnetic crystals under high magnetic fields. Our progress has led us to propose a new principle: orbital-regulated topological protection. Based on theoretical simulations, we have established that a strong magnetic field during crystal growth can enhance and freeze orbital coupling, thereby improving crystalline and spin ordering and ultimately inducing a strong DMI. This finding promises to provide the foundation for the nucleation of large-scale topological lattices that are stable at room temperature and under zero external field – essential conditions for practical devices.

Motivated by this tantalising possibility, we have developed high-magnetic field-assisted MBE equipment, which has been subsequently patented in China and the United States. Following systematic selection of materials, we have settled on a Pd/Fe/MgO trilayer structure, which offers broken spatial inversion symmetry when grown on a GaN substrate. During the deposition of iron, we apply an *in-situ* magnetic field of up to 9 T. According to our comprehensive structural and magnetic characterisation, samples grown under a 9 T magnetic field exhibit superior crystallinity and a higher magnetisation. Measurements reveal a strongly DMI (–0.4266 mJ m^{-2}) and a dominant in-plane magnetic anisotropy, which are enhanced compared to those grown without any magnetic field.



➤ Figure 1. Large-scale meron lattices produced by high magnetic field MBE and observed by magnetic force microscopy.

We have been intrigued by finding paired circular magnetic domains with opposite polarities. They were uncovered by magnetic force microscopy (see Figure 1) and Lorentz transmission electron microscopy (see Figure 2). They provide confirmation that we constructed topological meron-antimeron pairs, and also reveal a Bloch-type spin texture with left-handed spin chirality in meron



➤ Figure 2. (a) Overfocused Lorentz transmission electron microscopy images of meron pairs with alternated dark and white contrast, measured under zero magnetic field and at 300 K. Scale bar, 200 nm. (b) Schematic of the meron pairs where in-plane spin component distributions were deduced from the selected domain region at 300 K using the transport-of-intensity equation. The inset shows the colour wheel for the direction of in-plane magnetisation.

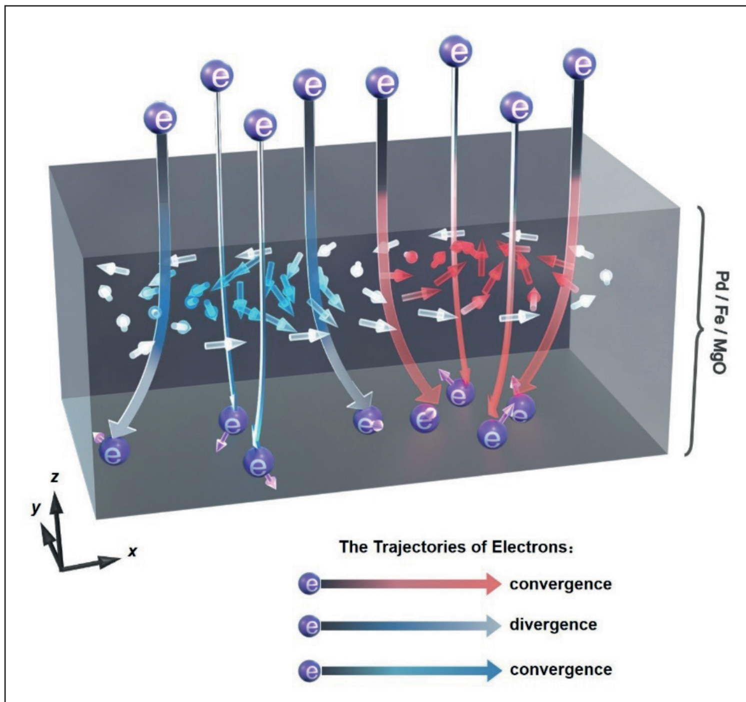


Figure 3. Trajectory of electrons injecting through a meron pair. The purple balls with the letter 'e' are electrons. Purple arrows illustrate the directions of electron spin after injection.

lattices, consistent with the negative value for the DMI strength. These meron-antimeron pairs exhibit long-range ordering over the 6 mm by 6 mm wafer, forming large-scale meron lattices.

It is worth noting that were observed these meron lattices at room temperature and without a magnetic field. Even after 530 days, our meron lattices exist stably. These findings demonstrate that topological protection can be introduced into the magnetic thin films through orbital-regulated growth.

Transferring chirality

One obvious, crucial question is whether the chirality in meron lattices can be transferred to light, to form a chiral photon source. Often this is not considered, because topological spin structures tend to be viewed as information carriers for future information devices, and their opportunities in optoelectronics are overlooked. Current research is focused on manipulating topological spin structures using light or spin current – there are, for example, efforts directed at the likes of race-track memories and skyrmion logic gates – while the manipulation of electrons and photons by topological spin structures is not on the agenda.

Helping to reset the balance, we have analysed the trajectories of electrons vertically injected into the meron lattice (see Figure 3). We have found that the chiral spins in the meron lattices act on the incident electrons as vortex magnetic fields. Consequently, when electrons pass through these vortices, they are deflected by an additional Lorentz force without an external magnetic field. Due to the particularly small core size of the merons, this force is strong enough to dispatch electrons to regions with different spin polarisations.

It is possible to calculate the degree of spin polarisation produced by a meron-antimeron. In the meron area, the force converges the electrons into the core region, causing them to be polarised along the core spin. Meanwhile, in the antimeron area, the force ensures divergence, driving half of the injected electrons to the adjacent meron area. Due to both of these activities, the number of output electrons in these two areas differs, inducing a spin polarisation of up to 50 percent in the output current – and revealing the potential for chirality modulation for electrons.

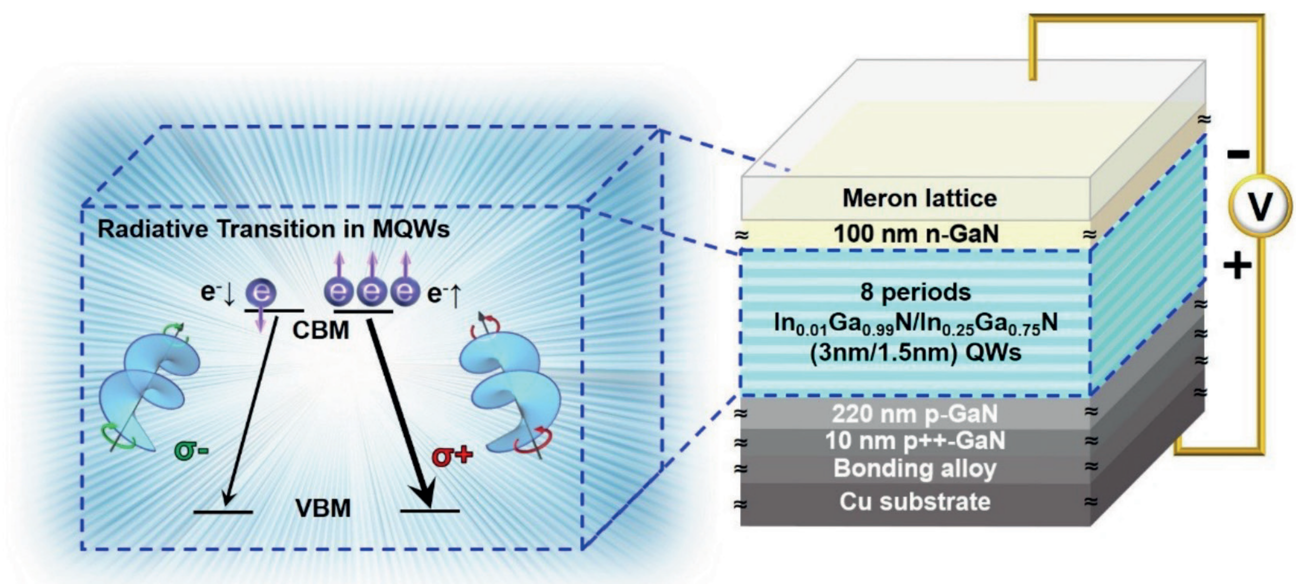


Figure 4. The topology-induced spin LED structure and the principle of chirality transfer from injected electrons to emitted photons in the electroluminescence measurements.

Following identification of the modulation effect in electron spin, we have integrated meron lattices in nitride-based LEDs, using a Pd/Fe/MgO trilayer as the spin injector. With this novel structure, the injection of spin-up and spin-down electrons produces electroluminescence with right (σ+)-circular and left (σ−)-circular polarisation, respectively – as expected from the selection rules for electronic transitions (see Figure 4).

The degree of chirality of the emission is governed by the strength of the magnetic field during MBE growth. For the 0 T sample, circular polarisation is just 0.9 percent, so essentially neglectable, while the 9T variant produces a record-high circular polarisation of 22.5 percent (see Figure 5).

We attribute the tremendous hike in polarisation to the modulation of electron spin from the topological meron lattices that form under the high growth-magnetic-field. Due to this, we describe our device as a topology-induced spin LED. Its high degree of polarisation is direct evidence of effective chirality transfer from topological spin structures to electrons and then photons. Note that this behaviour occurs under practical working conditions for the LED – that's room-temperature operation under zero magnetic field with an applied current of 1 mA. Thus, our topology-induced spin LED breaks through the constraints of poor stability and low polarisation, weaknesses impairing existing chiral photon sources.

Key to our breakthrough is our high-magnetic-field MBE growth technology, which manipulates interactions within strong-correlated materials through orbital control. Note that this is a versatile approach that could be employed for controllable growth of other crystals and topological lattices, such as skyrmions and vortices.

As the large-scale topological meron lattices created in our work have room-temperature and zero-field stability, they provide an ideal platform for the frontiers of photonics research. That's because our on-chip chiral photon source is capable of transferring chirality from topologically protected quasiparticles to fermions with mass and further to massless bosons. It's a breakthrough that as well as having scientific significance in its own right is a significant step towards the practical applications of topological spin structures.

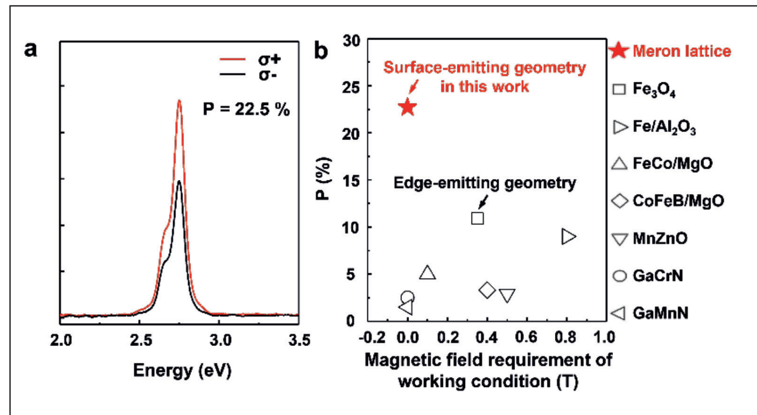


Figure 5. (a) Circularly polarised electroluminescence spectra of the topology-induced spin LED (T-LED) grown under 9 T magnetic fields. (b) Comparison between the T-LED and nitride-based spin LEDs, using results reported in the literature. The T-LED has a surface-emitting geometry. This ensures a substantially higher luminous efficiency than that for an edge-emitting geometry, due to an anisotropic carrier transition.

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FURTHER READING

- X Wu *et al*. "Topology-induced chiral photon emission from a large-scale meron lattice" Nat. Electronics **6** 516 (2023)
- X. Wu *et al*. "Semiconductor applications of large-scale meron lattices" Nat. Electronics **6** 477 (2023)

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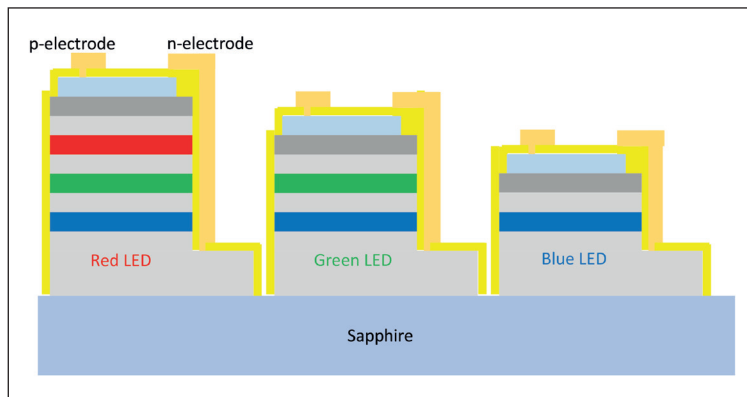
The three-in-one microLED

Selective removal of active layers creates a monolithic full-colour LED

ENGINEERS from Toyoda Gosei are claiming to have made significant strides in improving the simplicity of making microLEDs for full-colour displays. Using the selective removal of active layers, they have created a monolithic InGaN LED that emits in the red, green and blue.

"We believe that this simplicity makes it possible to produce micro-displays with fine pixels at low cost," claims team spokesman Koichi Goshonoo.

He points out that another attribute of their architecture is the common cathode, which negates complexity in the driving circuit.



➤ The monolithic full-colour LED has emitting regions separated by a 50 nm-thick layer of undoped InGaN and a 20 nm-thick layer of *n*-type InGaN.

Toyoda Gosei's technology is not the only approach that realises multi-colour monolithic microLEDs. Other options include: combining blue LEDs with quantum dots that emit in the red and green; using a cascaded or stacked structure of LEDs; turning to nanowires; and adjusting the facet plane to increase indium uptake. However, according to Goshonoo and co-workers, all these alternatives are plagued by cost and yield issues, stemming from the complexity of the structure and the process.

In the team's design, the blue LED has just a blue emitting quantum well, while the green LED has green-emitting wells on top of blue variants, and the red LED has all three forms of wells (see Figure). However, in each case, emission from just one region dominates.

An explanation for the spectral purity of the emission is provided by simulations of the band diagram and carrier profiles. Such efforts have been undertaken with a LASTIP package produced by Crosslight.

Simulations show that for the red LED, there is preferential electroluminescence in the red-emitting layer. That's partly because this layer has the smallest bandgap, but it is also a consequence of the low mobility of the holes – those injected from the *p*-type layer don't travel that far, staying near the red-emitting wells. Another factor at play is that the *n*-type intermediate layers between the radiative regions ensure the transportation of electrons from the blue-emitting region to that emitting in the red. Similarly, the transport of holes to the green and blue light-emitting layers is inhibited, aiding pure red emission.

The same mechanisms are at play in the green LED, ensuring that it produces predominantly green emission, while in the blue LED there are just blue-emitting wells, as is the case in a conventional LED.

Goshonoo and colleagues produced their full-colour LED by loading a sapphire substrate into an MOCVD reactor and growing a GaN-based epistructure that contained three 3.5 nm-thick blue-emitting InGaN quantum wells, two 3.5 nm-thick green-emitting InGaN quantum wells and a single 3.5 nm-thick red-emitting InGaN quantum well. The team decreased the number of wells at longer wavelengths to try and limit the deterioration in quantum-well quality that occurs when increasing indium content.

Patterning and dry etching with chlorine gas enabled selective removal of regions emitting in the green and red, prior to the growth of a *p*-type region with an electron-blocking layer, the formation of a mesa, and the addition of a protective film and electrodes.

The emitting area, determined by the dimensions of an ITO layer, is 250 μm by 400 μm. However, smaller values are possible. "The target size of each color sub-pixel is less than 1 μm," says Goshonoo, who adds that 10 μm has been verified.

Luminescence characterisation revealed a wide colour gamut, with a National Television Standards Committee coverage of 95.4 percent. However, wall-plug efficiencies are a concern, with values at 20 mA of 0.17 percent in the red, 5.9 percent in the green and 0.65 percent in the blue.

Lower efficiency in the blue is blamed on the formation of non-radiative recombination centres during removal of regions developed for emission in the red and green. Optimising the process could address this issue.

Increasing the efficiency of the red LED is more challenging. "Many research institutions, including ours, are working on this issue, and we hope that it will be overcome someday," says Goshonoo, who added that another of the team's goals is to prototype a microLED.

REFERENCE

➤ K. Goshonoo *et. al.* Appl. Phys. Express **16** 082004 (2023)

Mist epitaxy of β-Ga_2O_3 devices

β-Ga_2O_3 MESFETs produced by mist epitaxy validate the promise of this low-cost growth technique

IDEALLY, compound semiconductor devices are produced with relatively simple tools on native substrates, because this offers the opportunity to make low-cost, high-performance chips.

Unfortunately, for most classes of compound semiconductor device, it's not possible to meet both these two requirements. But they can be met with power transistors made from β-Ga_2O_3, according to a Japanese collaboration between Kyoto University, Nagoya University and Panasonic.

This partnership claims that it has broken new ground by producing β-Ga_2O_3 MESFETs on native substrates using mist CVD, a low-cost growth technique that is far simpler than MBE and MOCVD, and has already been employed by the Japanese company Flosfia to make α-Ga_2O_3 power devices on sapphire substrates.

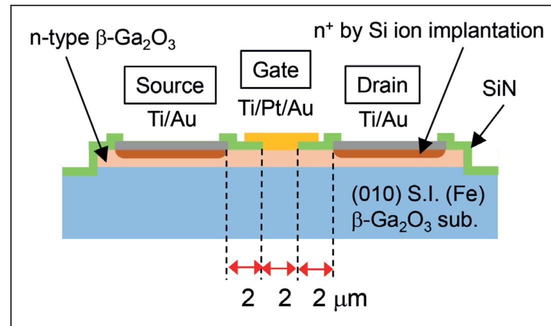
Spokesman for the collaboration, Shizou Fujita from Kyoto University, told *Compound Semiconductor* that the team were able to draw on previous experience involving the use of mist CVD to grow transparent conducting oxides, such as ZnO.

"One of the challenges was to apply this simple and cost-effective technology to the growth of semiconductor crystals, which require extremely low impurity incorporation and flat surfaces," remarks Fujita.

He adds that no longer having oxygen as an impurity, as is the case with GaAs, InP, SiC, and GaN, is a benefit. However, there are still obstacles to address, such as impurity doping, and designing a mist CVD reactor that introduces mist particles smoothly into the reaction tube without condensation.

Fujita and co-workers produced by their MESFETs by loading semi-insulating β-Ga_2O_3 (010) substrates into a homemade hot-wall-type mist CVD system and depositing *n*-type Ga_2O_3 layers. Precursors for gallium and silicon, which provides the *n*-type dopant, were (acetylacetonato)gallium and chloro-(3-cyanopropyl)-dimethylsilane. Using oxygen carrier and dilution gases, the team supplied the precursor mist to the horizontal reactor, heated to between 700 °C and 800 °C.

Higher temperatures slowed the growth rate. This led the team to select a growth temperature of 750 °C, which provided a growth rate of just 750 nm/hr – well below the value of 3.2 μm/hr reported by another group that had used a precursor with a higher gallium concentration to produce Ga_2O_3 films by mist CVD.



➤ β-Ga_2O_3 MOSFETs deliver competitive values for trans-conductance and drain current, but there are concerns related to pinch-off and the breakdown voltage.

Following the growth of a 200 nm-thick layer of β-Ga_2O_3, Fujita and co-workers produced a mesa structure by conventional lithography and inductively coupled plasma-reactive ion etching, before using silicon implantation to form source and drain regions. After adding a Ti/Au metal stack to both these regions, the team deposited a 60 nm-thick SiN passivation layer, subsequently etched off by inductively coupled plasma-reactive ion etching in the gate region, to allow the addition of a Ti/Pt/Au stack. Finally, this form of etching removed the SiN passivation layer above the gate and drain regions.

Electrical measurements using the Van der Pauw method determined a mobility of 80 $cm^2 V^{-1} s^{-1}$, said to be comparable or only slightly lower than that for β-Ga_2O_3 films grown by MBE and MOCVD. Maximum transconductance hit 46 mS mm^{-1} and drain current peaked at 240 mA mm^{-1}, values Fujita describes as high, and almost reflecting the properties of Ga_2O_3.

However, several devices did not exhibit pinch-off, indicating insufficient suppression of the leakage path at the interface between *n*-Ga_2O_3 and the substrate. Additional weaknesses were a breakdown voltage of just 195 V and an on-resistance of 30 Ω mm, issues that can be addressed by optimising the device structure and the growth conditions.

Another issue is the difficulty in obtaining a carrier concentration below 10^{17} cm^{-3}, which is necessary for normally-off transistors and devices offering a high breakdown voltage.

"In mist CVD, the unintentional doping from the source chemicals or quartz tube is a problem to be solved in the next stage," says Fujita.

REFERENCE

➤ H. Takane *et. al.* Appl. Phys. Express **16** 081004 (2023)

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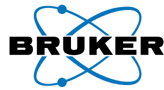

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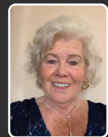

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