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INSIDE

A symphony of semiconductors

Industry-facing academics champion the capabilities of devices based on SiC, GaN and Ga_2O_3 at WiPDA Europe

LEDs: Realising a red revolution

Machine learning and quantum-mechanical modelling and can accelerate the design of polychromatic LEDs

Ubiquitous communication

Visible communication based on GaN lasers will empower wireless and optical networks in space, on land and under the sea

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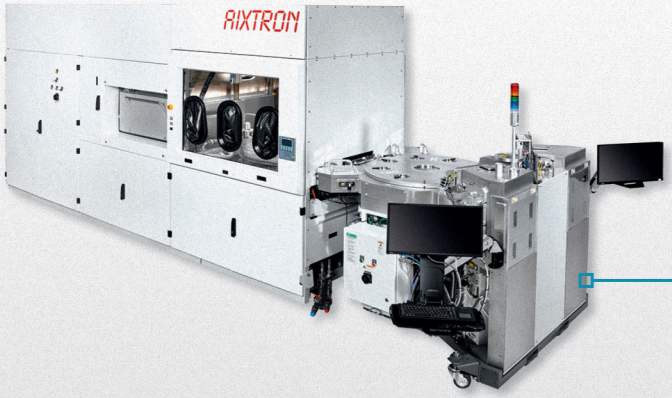

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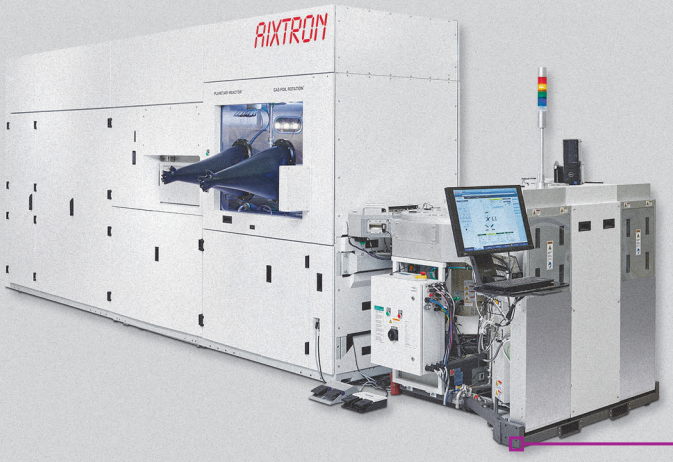

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VIEWPOINT

By Richard Stevenson, Editor

Catching up with silicon

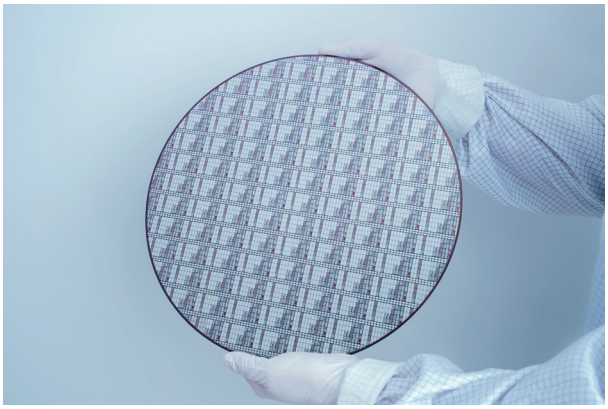
LIKE IT OR NOT, we are often compared to the silicon industry. This could paint us in a positive light, should there be a focus on efficient light emission and detection, power handling capabilities, or maximum RF power densities. But unfortunately, many prefer to apply other merits, such as global revenue, where silicon wins hands down, or the size of the wafers.

For the latter, the gap is closing all the time. In part that's due to silicon's stagnation. From the 1960s to the 1990s, the most common wafer size for chip production climbed steadily from 1 inch to 6 inch. By the turn of the millennium, production had started to shift to 200 mm, with 300 mm becoming common in the 2010s, and remains so today.

While the silicon industry stalls, we are catching up. Notable recent progress on this front includes Coherent's move to manufacturing on 6-inch InP at its fabs in the US and Sweden, and a shift by many of the leading SiC chipmakers to production on 200 mm wafers.

And when we grow GaN on silicon, the gap has now vanished, with Aledia leading the way. Back in 2000, it announced that it had produced it first microLED chips on 300 mm silicon substrates. And GaN power devices have just caught up, thanks to the efforts of Infineon (for more details, see p. 16).

It's interesting to see how the arguments within our industry have changed as production has shifted from the 200 mm to the 300 mm format. Back in 2011, when Bridgelux believed that by pioneering growth of LEDs



on 200 mm silicon it could enable a $5 LED light bulb, this California-based chipmaker argued that epiwafer processing could be outsourced to under-utilised 200 mm fabs around the world. While that was the case then, it's not now, with such fabs in high demand.

Today Infineon is promoting the benefits of processing 300 mm epiwafers. As well as more die per wafer, yield is up and the metrology is better, due to more advanced tools. And as the on-resistance for GaN power devices is less than that for silicon equivalents, comparable performance is realised with smaller die, making cost parity a tantalising prospect.

Such success would be a major triumph. While we may always be in the shadow of silicon, the more we have to cheer, the better.

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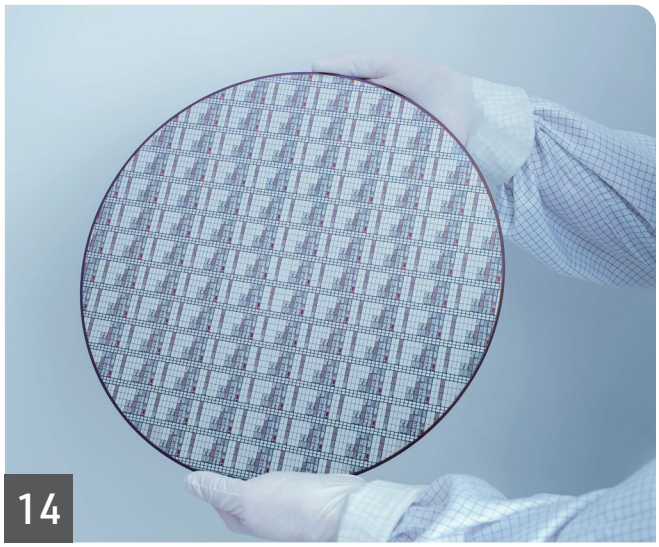

NEWS ANALYSIS

RESEARCH REVIEW

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Wolfspeed announces $750M in CHIPS Act funding

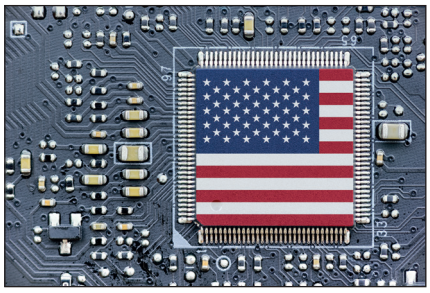
Government funding to be supplemented by an additional $750 million of new financing by investment funds

THE US Department of Commerce and Wolfspeed have signed a non-binding preliminary memorandum of terms for up to $750 million in proposed direct funding under the CHIPS and Science Act. In addition, a consortium of investment funds led by Apollo, The Baupost Group, Fidelity Management & Research Company and Capital Group have agreed to provide Wolfspeed an additional $750 million of new financing.

Together these investments support Wolfspeed's long-term growth plans and bolster domestic production of SiC to power clean energy systems underpinning electric vehicles (EVs), artificial intelligence (AI) data centres, battery storage and more. In addition, Wolfspeed expects to receive $1 billion of cash tax refunds from the advanced manufacturing tax credit under the CHIPS and Science Act (section 48D), giving the company, in total, access to up to $2.5 billion of expected capital to support the expansion of SiC manufacturing in the United States.

The importance of bolstering the domestic production of SiC has been recognised across multiple federal agencies; the Department of Energy denoted it as one of 17 'critical materials' with a high risk of supply disruption that are integral to clean energy technologies, while the Department of Commerce recognises SiC semiconductors as important to national security.

Wolfspeed CEO, Gregg Lowe, said: "To reach this milestone under the US CHIPS and Science Act is an incredible achievement in Wolfspeed's long-term growth strategy, and we believe today's announcement is a testament to the market-leading quality of Wolfspeed products and significance of Wolfspeed to broader US economic and national security interests. This support galvanizes our ability to expand



domestic manufacturing, accelerate innovation in next-generation semiconductor technology, and meet the increasing global demand for SiC. As a key player in the semiconductor industry, this proposed investment will enable us to solidify our leadership position with a first-of-its-kind 200 mm SiC manufacturing footprint in upstate New York and central North Carolina, while contributing to the resilience and competitiveness of the US supply chain. It's not just about growth for Wolfspeed – it's about driving technological advancement that powers the future."

Lowe added: "SiC is already enabling superior energy efficiency across mission-critical industries of the future like electric vehicles, e-mobility, solar and wind energy, industrial power applications, and AI data centres. While EVs have been the driver of SiC adoption thus far, we believe the use cases for our technology are expansive and will only continue to grow as more and more industries find themselves needing to solve for the same power loss, system size, and system cost challenges as automakers."

"Artificial intelligence, electric vehicles, and clean energy are all technologies that will define the 21st century, and thanks to proposed investments in companies like Wolfspeed, the Biden-Harris Administration is taking a meaningful step towards reigniting US manufacturing of the chips that underpin these important technologies," said US Secretary of Commerce Gina Raimondo. "Because of the Biden-Harris Administration's CHIPS and Science Act, the United States is building and fortifying our semiconductor manufacturing capabilities to serve our economic and national security interests while creating jobs and economic opportunities for communities across the country."

"We are pleased to expand our investment in Wolfspeed by providing additional capital in support of the company's build out of its leading SiC capabilities," said Apollo partner Joseph Jackson. "We believe Wolfspeed is at the forefront of a critical transformation in sustainable transportation and ensuring that the company has durable capital access to complete its expansion plans will help solidify its leadership in this space. Along with our lending consortium, which includes multiple funds that also own substantial equity stakes in the company, we believe this strategic investment will drive significant long-term value while advancing key tenets of the CHIPS and Science Act."

These proposed funds, which are expected to be received upon milestone achievements in the coming years, would enable Wolfspeed to complete its multi-billion-dollar greenfield US capacity expansion plan, which consists of the largest and most advanced 200 mm SiC footprint in the world. In addition to the proposed direct funding, Wolfspeed intends to benefit from the US Treasury Department Investment Tax Credit of up to 25 percent of the qualified capital expenditures primarily related to its construction and installation of equipment at The John Palmour Manufacturing centre for SiC in Siler City, NC, and completion of the Mohawk Valley Fab M-Line West Expansion in Utica, NY.

Meta reveals LED-based AR glasses prototype

‘Orion’ glasses are based on silicon-based microLEDs and weigh just 98 grams

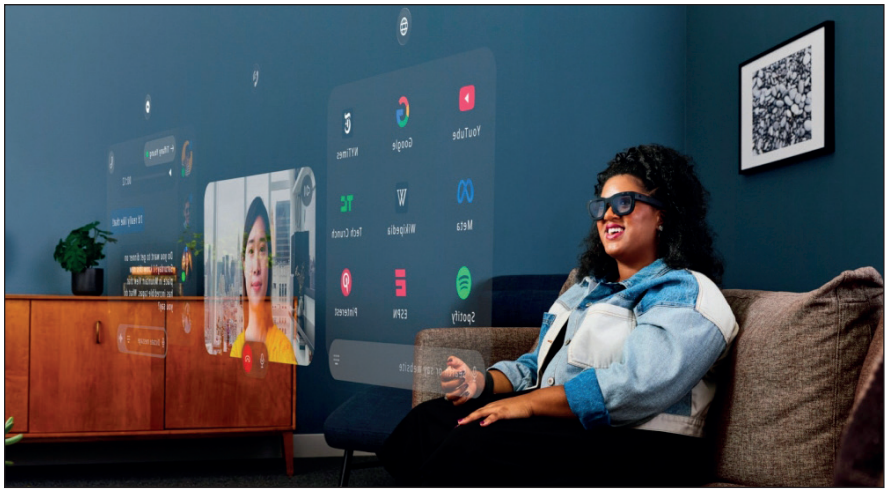
META HAS JUST unveiled its first-ever full-colour AR glasses, Orion, at Meta Connect 2024. The glasses are based on LEDoS (silicon-based microLED) technology and weigh just 98 grams.

According to TrendForce’s recent analysis, 2024 is set to be a crucial year for leading brands venturing into the near-eye display market within the metaverse. Nevertheless, Meta’s AR glasses are still struggling to achieve an optimal balance between field of view (FOV) and resolution, as well as developing a more robust application ecosystem. It’s predicted that these devices may not be commercially available until after 2027.

The Orion AR glasses, unveiled at Meta Connect 2024, come equipped with an array of sensors. TrendForce’s findings reveal that the optical design incorporates a diffraction-type waveguide made from SiC, combined with JBD’s three-panel full-colour LEDoS technology to achieve a 70° FOV.

While Meta’s Orion is positioned as their first consumer-facing AR product, the prototype is primarily intended for developers and testers, with no plans for mass production yet. TrendForce says several hurdles need to be overcome before large-scale production can commence.

Key challenges include the steep costs associated with LEDoS micro-display panels and resolution constraints linked to SiC waveguides. This material, often utilised in military radars and sensors, is also subject to export limitations, which will further escalate production costs, pushing the price of each unit to nearly $10,000. Additionally, the device’s battery life is capped at just two hours, indicating a need for improvements.



TrendForce emphasises that AR devices, thanks to their lightweight and compact nature, are viewed as perfect candidates for AI integration. LEDoS technology aligns well with the requirements of AR – offering high brightness, miniaturisation, and low power consumption – and makes it a pivotal technology for the future of AR. If advancements in full-colour LEDoS solutions can be achieved through vertical stacking or colour conversion, it could emerge as the leading technology for AR glasses.

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The shipments of Apple’s Vision Pro VR/MR headset in early 2024 failed to meet market expectations, primarily due to its steep price point. Meanwhile, Meta’s Orion AR glasses are currently aimed solely at developers. For Meta to effectively enter the consumer market, it must find a better equilibrium between FOV and resolution while also boosting its application ecosystem.

TrendForce predicts that Meta’s consumer-oriented AR glasses may not debut until after 2027. Nevertheless, with increasing backing from major brands and a faster pace of application development, the production of more advanced and affordable devices is expected to commence between 2026 and 2027 – potentially paving the way for a major advancement in head-mounted displays.

TrendForce’s 2024 report on near-eye displays forecasts that the AR device market will hit 25.5 million units by 2030, with LEDoS technology projected to capture 44 percent of the market as it establishes itself as the leading solution.

HexaTech wins DARPA AlN substrate contract

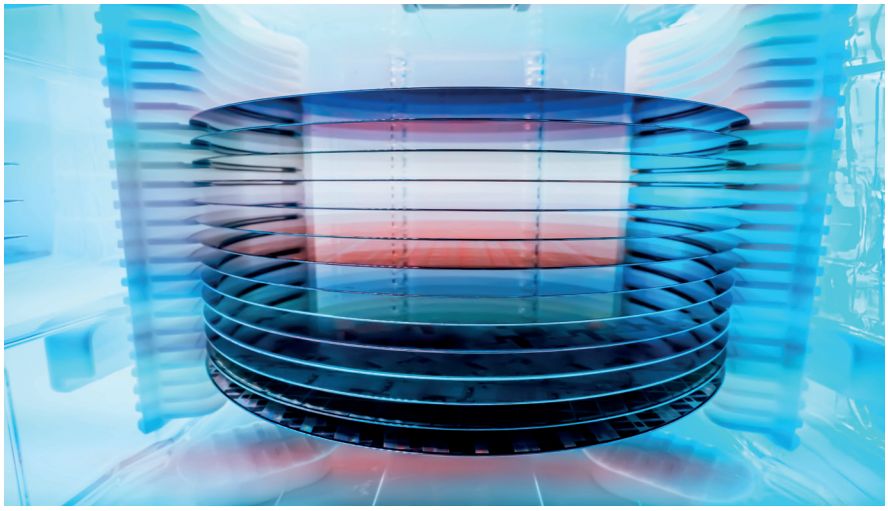
Potential three year $10.2 million programme for 100 mm diameter substrates

HEXATECH, a subsidiary of Japanese firm Stanley Electric, has signed a multi-year contract with the US Defense Advanced Research Projects Agency (DARPA) as part of the agency's new Ultra-Wide Bandgap Semiconductors (UWBGS) programme.

The UWBGS programme aims to develop high-quality materials for realising practical UWBG electronics and applications. HexaTech's role will be to focus on the development of 100 mm diameter, low-defect-density AlN substrates.

HexaTech CEO, John Goehrke said: "We are extremely appreciative for this collaboration with DARPA and the support they are providing, as we continue to drive our AlN substrate technology forward."

The potential three year contract is valued at $10.2 million, and builds on top of HexaTech's previously announced 100 mm development effort, accelerating the timeline and building on the scale of HexaTech's production process from crystal growth through substrate finishing.



Rafael Dalmau, the programme's principal investigator at HexaTech noted: "To fully support the technical potential of AlN substrates in both existing and new device technologies, expansion to 100 mm in diameter, coupled with superior bulk quality characteristics, will be critical for several reasons, including device fabrication line capabilities, device performance, and reliability."

"HexaTech will be a supplier to all DARPA awardees tied into AlN, as well of course to others worldwide as we are now, which will significantly contribute to our business in both the near and longer term, " Gregory Mills VP, business development told *Compound Semiconductor.*

Mills says the result of the programme will be the direct translation of 100 mm AlN substrates into volume production, enabling industry adoption by both commercial and defence foundries.

Atomera/Sandia tackles GaN challenges

Collaboration aims to create first GaN transistors from wafers using Atomera's Mears Silicon Technology

ATOMERA, a US semiconductor materials and technology licensing company, has announced a project at Sandia National Laboratories to address the challenges of growing GaN films on silicon.

The project, which is a collaboration with the Centre for Integrated Nanotechnologies (CINT) at Sandia, aims to create the world's first GaN transistors and test data from wafers employing Atomera's Mears Silicon Technology (MST). The effort will build upon improvements already observed at the materials level in GaN/MST on silicon wafers.

MST consists of layers of a non-semiconductor, such as oxygen, inserted into a semiconductor material, such as silicon, so that epitaxial growth is preserved. These layers can be used to modify or enhance the basic semiconductor properties and device attributes in a number of ways, including: diffusion blocking, variability, mobility, gate leakage, and reliability, among others.

"Atomera's MST represents a tremendous opportunity to improve GaN-on-silicon manufacturing and provide speed, efficiency and cost-saving benefits to a wide range of industries including electronics, RF/microwave electronics and even microLEDs. This user project will test the effectiveness of the MST solution quickly using CINT's highly specialised tools and technology and give Atomera access to our team of scientists and researchers," said Jeffrey Nelson, director of CINT.

"Over the past approximately 25 years, GaN has transformed multiple industries, including lighting, RF/microwave and power electronics, but manufacturing limitations have hindered the widespread adoption of GaN for modern power electronics," said Shawn Thomas, vice president of Marketing & Business Development at Atomera.

"This user project with Sandia Labs will allow Atomera to fabricate devices and collect data to validate the mechanical and electrical benefits of MST-enhanced GaN-on-silicon."

Managing stress is the most important aspect of growing thick GaN on silicon. Commercial GaN-on-silicon power devices are rated up to 650 V, a limitation that Atomera hopes to address.

NREL to design SiC inverter for US combat vehicles

SiC-based propulsion system will deliver four times the power at a quarter of predecessors' size

THE US National Renewable Energy Laboratory (NREL) will be redesigning the traction inverter used in US ground combat vehicles, with a SiC-based propulsion system that will double vehicle range in a footprint four times smaller than its predecessors.

The new inverter, called PICHOT, is expected to save 53 percent of fuel compared to existing technologies, meaning vehicles will be able to stay in the field for nearly twice as long before needing to refuel.

To create PICHOT, NREL says it is reimagining nearly every aspect of conventional power inverters.

Because traction inverters are typically installed next to other heat-generating elements in a combat vehicle, they need to be able to withstand high operating as well as ambient temperatures. This usually requires them to be packed with bulky cooling technologies, like cold plates or coolant reservoirs.

PICHOT will require none of these heavy cooling solutions, according to NREL. Instead, it will link to the existing engine coolant system, eliminating the need for additional coolant loops. In turn, unlike conventional silicon-based inverter systems – which become essentially powerless when exposed to operating environments over 70°C – PICHOT will be able to function at full power in environments of 105°C.

Because traction inverters are typically installed next to other heat-generating elements in a combat vehicle, they need to be able to withstand high operating as well as ambient temperatures

PICHOT will be capable of the same 200-kilowatt output as its predecessor, Zeus, but at a fourth of the size – small enough to fit in a shoebox. And to reduce electrical wiring , PICHOT's main communication will be a tailored wireless system featuring remote control and monitoring. It will even come equipped with a 'smart' feature that allows it to monitor its own state of health: in other words, to predict component failure before it occurs.

Combined with silent performance thanks to the hybrid-electric engine and electromagnetic interference shielding, Army ground combat vehicles are poised to become safer, longer-range, and higher-performing than ever before, says NREL.

NREL predicts that PICHOT will take three years to design, fabricate, and evaluate. In the first year, NREL researchers will build a computer-generated model of the inverter and simulate its operations in the real world, ensuring that it will operate as planned. Then, they will build it using the laboratory's end-to-end prototype fabrication pipeline and demonstrate its effectiveness versus other combatants' standard vehicles.

Finally, the blueprints will become available to manufacturers at a forthcoming industry day. The final design will be manufactured at scale, with potential to be leveraged in multiple kinds of US Army ground combat vehicles.

The three-year, $6 million project has been funded by the Operational Energy Capability Improvement Fund (OECIF), which guides energy innovations for the United States Department of Defense. It will be led by the United States Army Combat Capabilities Development Command, known as DEVCOM, with researchers from both NREL and the Army Research Laboratory (ARL) providing technical expertise.

Toray accelerates III-V chip mounting technology

Demonstrates industry-first laser transfer and bonding technology to reduce data centre power loads

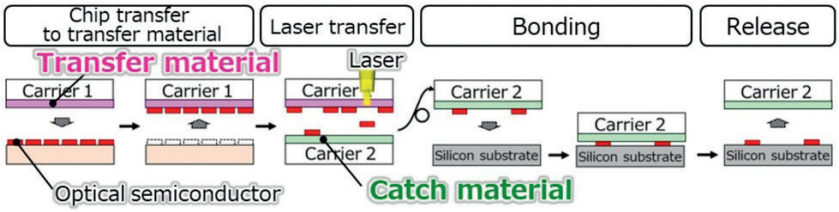
AI-DRIVEN DEMAND for high-speed communications is fuelling the construction of more data centres, raising concerns about their heavy power demands. This has accelerated the development of both long-distance and short-range optical communications within data centres.

Along with the increasing use of silicon photonics has come the challenge of mounting optical semiconductors made from InP and other III-V compounds onto silicon. Mass transfer technology is essential to do this swiftly and in large quantities.

Toray, with subsidiary company Tory Engineering, has now developed a material for fast laser transfers of InP and other optical semiconductors. They have also worked on a material to 'catch' transferred chips and bond them directly to silicon substrates and a related mounting process technology.

These efforts are said to have boosted optical semiconductor bonding speed to 6,000 units per minute, compared with around four units per minute with conventional flip chip bonders.

Toray previously developed transfer materials for microLEDs. In this case, the InP-based optical semiconductors are 640 μm long and 90 μm wide and less than 3 μm thick. While longer and wider than general microLEDs, the chips are also extremely thin. Toray developed a new material that enables transfer with a single laser irradiation without damaging chips, which should improve yields and throughput.



Toray's high-speed mounting process for optical semiconductors

'Catch' material must not only capture fast-flying chips but also withstand the subsequent direct bonding of these chips to the silicon substrate after chemical cleaning and activating the bonding surface with plasma, pressurising under high temperatures of more than 200°C. Release must thereafter be easy. Toray says it employed years of expertise in designing heat-resistant polymers and controlling adhesive properties to develop a new catch material that makes this possible.

Toray has used these materials to collaborate with Toray Engineering in developing and demonstrating the entire process, from laser transfer to direct bonding on a silicon substrate. The company has confirmed a post-bonding positional accuracy of ±2 μm and a rotational deviation of ±1°.

Toray says its next step is to verify chip operations and use actual devices to establish its technology. It will endeavor to enhance positional accuracy and broaden technology applications to include mass transfers of chips made from other different materials and millimeter-order semiconductor chips.

Toray developed part of this technology with a grant for the JPNP 20017 project of the New Energy and Industrial Technology Development Organization.

This R&D initiative project aims to solidify the foundations of post-5G information and communications systems.

Battle for 8-inch SiC heats up

8-inch SiC product market share to grow to around 15 percent by 2026, says TrendForce

ALTHOUGH 6-inch wafers currently dominate the SiC market, transitioning to 8-inch is an inevitable trend expected from 2026 to 2027, according TrendForce.

Today, the market share of 8-inch SiC products is currently less than 2 percent, but TrendForce forecasts it will to grow to around 15 percent by 2026.

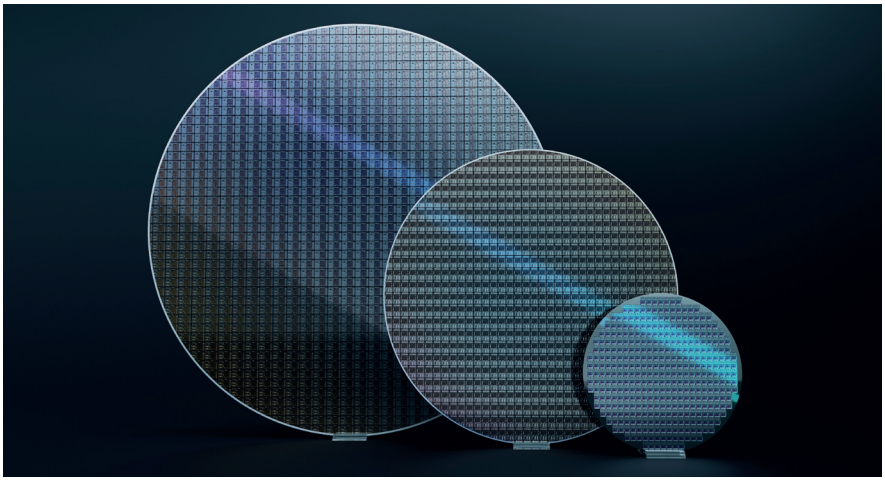
And the 8 inch wafer battle is already heating up.

On September 17, Japan's NGK Insulators (NGK) announced on its official website that it had successfully produced 8-inch SiC wafers. The company plans showcased these wafers, along with related research results, at ICSCRM 2024.

Reportedly, Resonac has achieved 8-inch SiC epitaxial wafers of the same quality as its 6-inch products. Currently, the company is working to reduce costs by improving production efficiency, and sample evaluations have reached the final stages of commercialiation.

Once the cost advantage surpasses that of the 6-inch products, Resonac is expected to transition to producing 8-inch products. Besides mass production of 8-inch SiC epitaxial wafers, Resonac plans to start mass production of 8-inch SiC substrates in 2025.

Additionally, Onsemi is set to accelerate the production of 8-inch SiC wafers, with capacity adjustments based on market demand expected to start in 2025. The company plans to launch its 8-inch SiC wafers later this year and begin production in 2025. Onsemi's president and CEO, Hassane El-Khoury, stated that the company is proceeding as planned and will complete the certification of 8-inch wafers this year, covering the entire process from substrate to wafer fab.



On September 9, Wolfspeed launched a 2300 V bottomless SiC power module for 1500 V DC bus applications, using its most advanced 8-inch SiC wafer technology. This product aims to drive development in renewable energy, energy storage, and high-power fast charging by improving efficiency, durability, reliability, and scalability.

In China, Sanan Optoelectronics' Chongqing Sanan project (an 8-inch SiC substrate support factory) has successfully lit up its production line. The substrate plant built by Sanan Optoelectronics using its own SiC substrate technology is operated by its wholly-owned subsidiary Chongqing Sanan Semiconductor. The plant plans to produce 480,000 8-inch SiC substrates annually.

SICC's 8-inch conductive SiC wafers have recently achieved mass production, and products are being continuously delivered. Additionally, in July, SICC announced a plan to raise investment in its 8-inch automotive-grade SiC substrate technology improvement project.

Looking ahead, TrendForce notes that, SiC as a crucial development in future power electronics is rapidly penetrating markets such as automotive and renewable energy, where power density and efficiency are paramount. Over the next few years, overall market demand is expected to maintain growth, with predictions that the global SiC power device market could reach $9.17 billion by 2028.

According to Tankeblue data, upgrading from 4-inch to 6-inch can reduce unit costs by 50 percent, and moving from 6-inch to 8-inch could further cut costs by 35 percent.

Market reports suggest that the price of mainstream 6-inch SiC substrates in China has dropped by nearly 30 percent, now referencing international prices of $750-$800 per wafer.

TrendForce has pointed out that with the entry of Chinese companies into the SiC market, the price drop for SiC substrates has accelerated.

SICC chairman commented that SiC substrate prices will fall due to technological advancements and economies of scale, leading to lower costs. Additionally, the high price of SiC substrates compared to silicon substrates has hindered wider adoption, and price reductions will help expand downstream applications, pushing SiC into broader use.

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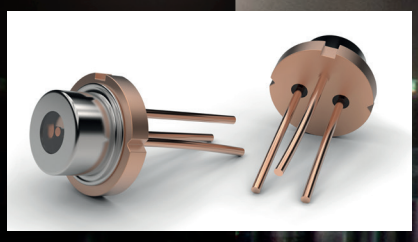

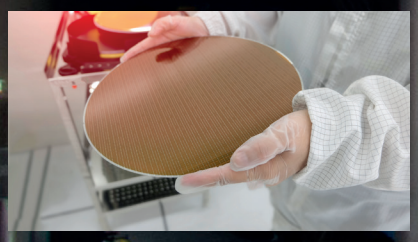

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Nexperia: Expanding GaN and SiC operations

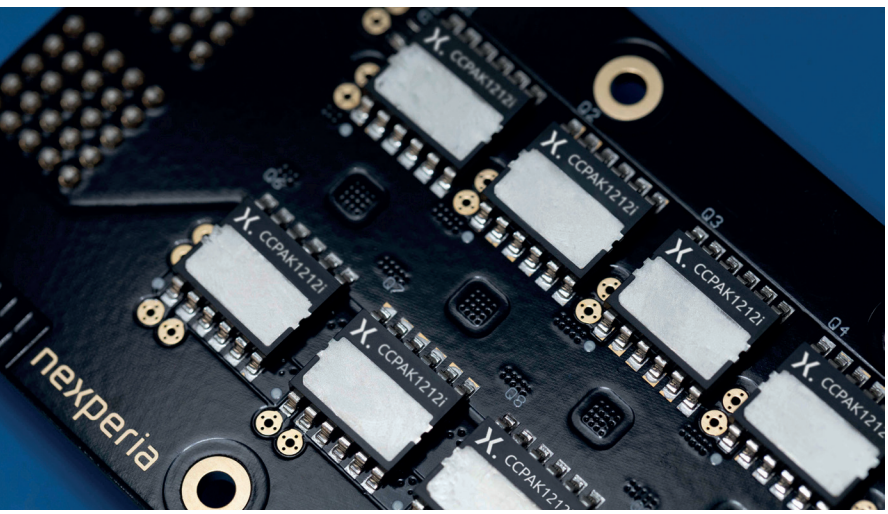
Re-fitting its Hamburg fab lays the foundations for Nexperia to hike its production of GaN and SiC transistors and diodes on 200 mm lines

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

INVESTING PHENOMENAL SUMS in infrastructure that enables the production of SiC and GaN devices is the new norm. In this regard the likes of Infineon, Wolfspeed and Innoscience are making the biggest splashes, by building fabs of breath-taking proportions that are propelling their capacity for high-volume production of wide bandgap power devices.

But as well as constructing new fabs, chipmakers are spending a lot of money on repurposing the space within them for the manufacture of SiC and GaN diodes and transistors. And in this regard, Nexperia is not holding back – it's investing $200 million in new tools and equipment to strengthen the development and production of its wide bandgap portfolio at its fab in Hamburg, Germany.

Nexperia has a tremendous pedigree in electronics, with a history going back 100 years, and second-generation parent companies that include the household name Philips. Production of vacuum tubes in Hamburg provided the first source of revenue in the 1920s, and in the decades that followed efforts extended to the research, development and production of semiconductor devices. Further milestones came in the 1980s and 1990s, including the first MOSFET and the first 150 mm line, respectively. And in this century, two of the biggest moves have been carving out NXP from Philips in 2006, and in 2017, spinning out NXP's standard product division under the name Nexperia.



➤ Nexperia's proprietary CCPAK packages

Today Nexperia is renowned as a major supplier of silicon power devices to automotive markets – this accounts for around half of its annual production of 100 billion discrete parts. However, over the last few years the power electronics producer has broadened its portfolio with the introduction of SiC and GaN devices.

Since 2019, GaN FETs have been part of this chipmakers' line-up. SiC products came in 2023, and now include SiC diodes and SiC MOSFETs, the latter in collaboration with Mitsubishi Electric.

An additional advance came this June, with the introduction of the production lines for high-voltage GaN D-Mode transistors and SiC diodes at the Hamburg site. And according to Nexperia, the next milestone will be modern and cost-efficient 200 mm production lines for SiC MOSFETs and GaN HEMTs.

These new lines will be established over the next two-to-three years at the Hamburg facility that is undergoing substantial change, as all activities unrelated to either lab or fab are relocated to another office in the city. It's a move that's enabling an increase in the capacity of the silicon side of the business, as well as the expansion of SiC and GaN capability.

Nexperia's Senior Director Product Management for SiC, Katrin Feurle, told *Compound Semiconductor* that most of the $200 million investment will be spent on new equipment and a remodelling of the fab to fit to the new machinery. Money is also allocated to increase the automation of existing infrastructure.

To scale epitaxial capabilities, Nexperia has placed orders with Aixtron. This German maker of MOCVD tools is a trusted partner that fulfils Nexperia's needs, according to Carlos Castro, Vice President and General Manager for GaN.

As well as purchasing a range of processing tools to turn epiwafers into devices, Nexperia is making substantial investments in metrology.

Castro claims that Nexperia has a strong reputation for really high standards in production and performance, adding: "Metrology is key, because it gives you a very precise characterisation and control of materials, structures, and the process." In turn, this ensures performance, reliability, quality, and a competitive cost.

In addition to the equipment, Nexperia has recruited accompanying personal. "We have some people already on board there, experts in metrology," says Castro.

This increase in headcount is part of a pattern of long-term growth in staff at the Hamburg site. In 2017 the facility had 950 employees, a figure that now stands at 1,600, with more than 50 added in the last three years for roles solely associated with wide bandgap devices.

Growth in GaN...

Since launching its first wide bandgap power device in 2019, the GaN FET, Nexperia has made much progress with this class of transistor. Each new generation features a 20 percent cut in specific on-resistance.

One of the strengths of Nexperia is that it supplies both E-mode and D-mode devices.

"We are the only supplier giving the option to customers to go for D-mode technology, which we believe is more suitable for high-voltage and high-power applications, as well for E-Mode devices, which are very successful right now in the market for low-voltage or low-power applications, like, for example, fast chargers for mobile phones or notebooks," says Castro.

Another attribute of Nexperia's GaN portfolio is that it draws on the company's 20 years of expertise in copper clip technology. As well as ensuring a superior thermal performance, this packaging technology leads to better electrical performance, with a trimming of parasitics and stray inductance resulting in an increase in reliability. And that's not all – the copper clip technology enables a much more compact design that ensures a higher efficiency, as well as the opportunity to turn to higher frequencies, a strength well suited to high-power applications, such as power supplies and electric vehicles.

While GaN power devices have much appeal, they are currently attracting bad press for patent battles fought between Innoscience and EPC and Infineon.

Castro is not expecting Nexperia to be on the wrong side of such skirmishes, since it has its own IP. Back in 2017 and 2018 the company worked with a collaborator in the US, an activity that involved some licensing, and since then it has been internally and significantly growing its IP portfolio.

➤ Lithography at Nexperia's Hamburg Wafer-Fab

... and SiC power portfolios

In the last year or so Nexperia has expanded its SiC portfolio, to include 650 V diodes with a current rating from 6 A to 20 A, in a range of formats that incorporate both surface mount and through-hole configurations. Additional advances are the launch of the first automotive-grade product, announced at this year's PCIM conference, and first design wins, especially in power supply applications.

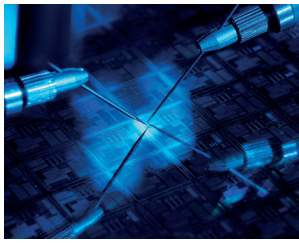
Feurle describes the relationship with Mitsubishi Electric, which is key to the production of discrete SiC MOSFETs, as a strategic collaboration that's mutually beneficial for both sides. She says: "It's supporting the mission of Nexperia, but also Mitsubishi, to meet the rapidly growing demand for silicon carbide." By combining complementary expertise, both partners are reducing requirements for in-house development, and enabling them to go faster to market.

Obstructing Nexperia's plans has been its forced sale of its fab in Newport, Wales, a move dictated by the UK government. While this has caused serious disruption, it has not impacted Nexperia's compound semiconductor activities, as there were no plans to reintroduce them at the Newport site.

At the Hamburg fab, conversion of office space to clean rooms is underway, and over the next few years lines will be established for SiC and GaN production, with full production slated for 2027. "Selected key customers, of course, will receive samples in advance, to be able to qualify dedicated target applications," remarks Feurle.

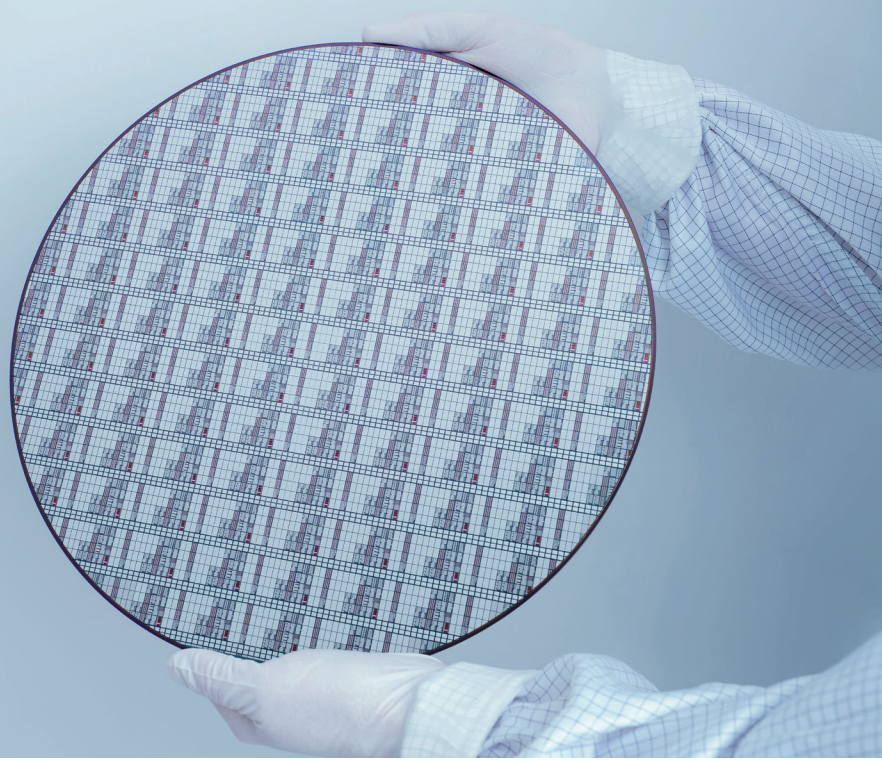
The balance between the production of SiC and GaN devices will be determined by the market. Today SiC dominates, but the gap is expected to narrow, with Castro expecting that by 2028, the SiC market will be around four times that of GaN.

Based on this forecast, and Nexperia's substantial investment, this chipmaker is sure to be a significant supplier of a broad range of wide bandgap devices by the end of this decade.



➤ Electrical Testing in Nexperia's R&D Labs

Power GaN: The 300 mm milestone



Migrating the manufacture of GaN power devices to 300 mm lines will boost yield, improve metrology and trim costs

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

➤ It has taken Infineon just 18 months to develop its 300 mm process, building on its 200 mm GaN-on-silicon technology.

A COMMON METRIC for measuring performance of any device is the bang per buck.

When it comes to GaN, there are many ways to measure that 'bang'. They include the on-resistance, the breakdown voltage, and the mobility of the two-dimensional electron gas.

But what about the 'buck'? That's a little harder to fathom, as chipmakers rarely reveal their yield, or the cost of producing their devices. But there are occasions when they will champion their efforts to trim their manufacturing costs, such as a move to larger wafers.

Claiming significant success on this front is the well-known European producer of power electronics, Infineon. It grabbed the headlines this autumn, when announcing the fabrication of the first GaN power devices on 300 mm wafers.

With manufacturers of GaN-on-silicon HEMTs currently carrying out production on substrates with a diameter of 200 mm, and sometimes less than that, Infineon's milestone is more than doubling the number of devices produced per wafer.

Note, though, that this gain is not the only one that will help to trim the cost of production. According to Johannes Schoiswohl, Infineon's Business Line Head for GaN, migration to larger wafers will also lead to improvements to the manufacturing process, such as a higher yield and access to superior metrology. Engineers at Infineon enjoyed these when progressing from 150 mm to 200 mm wafers, and they are seeing them again in the move to the 300 mm platform.

"We can get really great results – better than expected – because the 300-millimetre tools, from a performance perspective, from a monitoring perspective and a process control perspective, are better than the 8-inch tools," remarks Schoiswohl.

Due to these benefits, Infineon took just 18 months to develop its 300 mm process, building on its 200 mm GaN-on-silicon technology.

According to the company's projections, its GaN power devices could reach cost parity with their silicon equivalents. Helping to reach this goal will be: economies-of-scale; improvements in the technology itself, particularly the epitaxial stack; and the lower on-resistance of GaN, enabling smaller die to deliver the same performance as comparable products made from silicon.

To develop its trailblazing technology, Infineon's engineers have had to grapple with the lattice mismatch between GaN and silicon, as well as differences in thermal expansion coefficients.

"The bigger the wafer diameter, the harder it gets," admits Schoiswohl. "The wafers start to bow because of the lattice mismatch, and at a certain epi-thickness, they simply crack."

By developing and refining its epitaxial technology, Infineon releases strain during the growth.

Schoiswohl says that the particular epitaxial processes employed by providers of GaN power transistors are a key differentiator. According to him, the quality of the epitaxy determines the degree of early lifetime failures and often defines the device's failure mechanisms.

With Infineon's GaN power devices, a thicker epitaxial stack is needed to realise a higher blocking voltage. According to Schoiswohl, the company's engineers can see a path to progressing from 100 V to 650 V devices, but going beyond that will be more challenging. He says that one solution could be a switch to thicker wafers: "These are all details we have to figure out."

Infineon already offers wide bandgap power devices operating at a kilovolt or more, based on SiC. But that will not stop the company investigating what might be possible with GaN, which offers the tantalising possibility of a better performance at a lower cost.

Following the production of GaN-on-silicon epiwafers on dedicated MOCVD tools, processing of this material is undertaken on standard silicon lines – that's a significant merit from a CapEx perspective.

Infineon's pioneering work has been carried out at its facility in Villach, with attention paid to ensuring that processing of its GaN-on-silicon wafer in a 300 mm line did not introduce any contamination. As volume ramps, there will come a time when a 300 mm line can be devoted solely to the production of GaN devices. Infineon also has 300 mm equipment in Dresden that could be used for the production of GaN devices, and opportunities to potentially outsource due to established foundries.

At the upcoming trade show Electronica, to be held in Munich from 12-15 November, Infineon will release its next-generation G5 HV technology. The plan is to take this process and apply it to 300 mm wafers, with engineering samples reaching customers by the end of next year, and production ramping in 2026.

A technical engineer in the cleanroom at Infineon Technologies in Villach, Austria, holds a 300 mm GaN-on-silicon wafer.

Today the biggest market for GaN power devices is consumer chargers. "We can see that this is now reaching points where some customers say 100 percent of their volume will move there," remarks Schoiswohl.

Additional opportunities are found in power supplies for AI, motor controls and inverters, as well as the automotive industry. While all these markets are important, Schoiswohl sees the automotive sector as an important one, due to the opportunity for higher volumes, with GaN a compelling candidate for the on-board charger.

Success will hinge on the bang-per-buck, helped by a move to 300 mm GaN-on-silicon.

A happy coexistence: silicon IGBTs and SiC MOSFETs

Opportunities in electric vehicles, automation, data centres and renewables will underpin the growth of the SiC MOSFET, as well as its lower performance, but cheaper alternative, the silicon IGBT

BY CALLUM MIDDLETON AND PAUL PICKERING FROM OMDIA

THOSE OF YOU owning vehicles powered by a battery will know that, in many ways, the driving experience is no different from that provided by a car consuming petrol or diesel. But there are some notable differences.

One of the first of these you'll encounter is that rather than having a traditional fuel gauge, you'll get a figure for the estimated range. And unfortunately, it will not take you long to discover that what this figure lacks in accuracy, it makes up for in optimism.

Driving range often tops the list of considerations of those looking to purchase an electric vehicle in an ever more competitive marketplace. Helping to maximise this range is the SiC MOSFET, which draws on its superior efficiency over the silicon IGBT. Having the upper hand on this front is the primary justification for OEMs to opt for the SiC solution.

While the efficiency of the SiC MOSFET is a major selling point, that's not the only benefit it offers over the silicon IGBT. Additional merits are a doubling of thermal conductivity and a far higher switching frequency, which allows the use of smaller passives and cheaper systems. It's also worth noting that many of the advantages of SiC are greater at higher voltages, allowing the wider bandgap transistor to shine in higher-voltage systems, such as 800 V electric vehicles and 1500 V photovoltaic inverters. The only significant downside of the SiC MOSFET is that it's pricey, but that concern is diminishing, as wafer sizes expand and material prices fall. So, is there much of a future for the silicon IGBT?

Well, one should not dismiss the importance of its lower price. The best engineering solution is not always the best solution, and there is no reason to expect the SiC MOSFET to ever reach price parity with the silicon IGBT, due to its higher inherent costs that are associated with the manufacturing process. While turning to SiC can drive down system costs, offsetting some of the difference in die cost, this can be a challenging proposition to make, and it is likely that users will always face a choice between performance and cost.

In the traction inverter market, after weighing up the pros and cons, many automotive OEMs and tier ones are deciding to deploy SiC. Tesla introduced SiC to this sector to distinguish its vehicles from its competitors, and in the process became the leading BEV manufacturer in the world. Now many automotive

companies are following suit in an attempt to close the gap. This is driving a ramp in SiC device sales, which climbed by 75 percent in 2023. However, today's BEVs are primarily in the 'luxury' and 'mid-range' categories, where consumers are willing to pay a little more for improved performance. As the BEV market expands, makers of these vehicles will have to penetrate the economy end of the market, where price matters much more. For customers who tend to use their vehicles for short journeys in urban settings, cars fitted with IGBTs will appeal.

It's quite feasible that even the more expensive vehicles will not solely use SiC. The Tesla model that pioneered SiC featured 48 MOSFETs. But in March 2023, that trailblazer of the BEV surprised many when it announced it would be trimming usage of these wide bandgap chips by 75 percent. Arguably, this decision should not have raised that many eyebrows, as one should expect that innovations in device design and inverter design would lead to a reduction from 48 MOSFETs, alongside a possible move to a blend of SiC MOSFETs and silicon IGBTs.

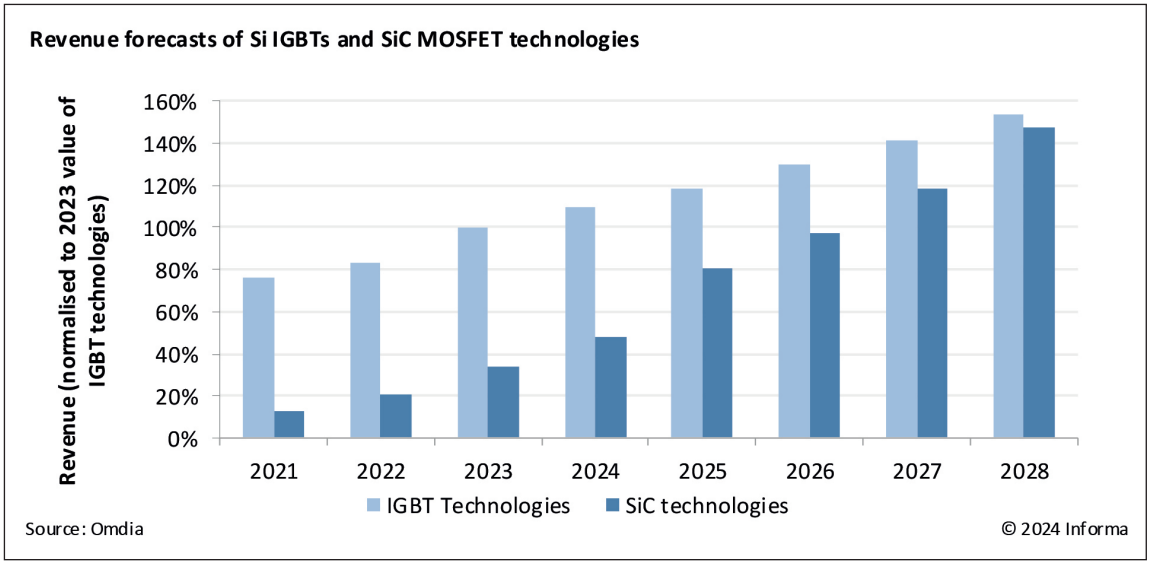
As already mentioned, BEVs are renowned for their optimistic range. This is partly due to difficulties in estimating this critical distance, which is influenced by numerous factors, including driving style and ambient temperature. The mission profile of the traction inverter within a BEV can vary greatly depending on where it is located, who the owner is, and even the day of the week. Due to these considerations, what's needed is a varied internal solution that allows the system to operate in the most efficient manner, irrespective of what is asked of it, without over-engineering. It remains to be seen whether this blended solution comes from vehicle designers deploying multiple inverters within a vehicle, or the use of power modules containing both SiC MOSFETs and silicon IGBTs.

When considering these factors, it is clear that the rise of the electric vehicle provides a great opportunity for both SiC MOSFETs and silicon IGBTs.

At Omdia, we are forecasting a compound annual growth rate of 32.6 percent for SiC device revenue between 2023 and 2028, and over that time frame an equivalent figure of 10.8 percent for power modules based on the silicon IGBT. Our forecast growth in SiC is eye-catching, justifying the level of investment in this technology, while the growth in the silicon IGBT offers a compelling reason to continue investing in device research and development to help companies claim more of this growing pie.

Outside the automotive sector, many of the same trade-offs apply. However, the absence of a key performance metric, such as range, makes it harder to justify a transition to SiC. We are living in a time of high energy costs and increased automation, factors that encourage investment in motor drives and grid infrastructure – and present opportunities for both SiC MOSFETs and silicon IGBTs. As SiC capacity expands, this should trim costs, but capacity is closely tied to the automotive sector. This tie-in may encourage equipment manufacturers in other sectors to stick with silicon until there's greater maturity in the SiC industry. Whilst improved efficiency is a big benefit at a time of increased energy costs, it still may not be enough to offset the extra chip cost. Therefore, it is most likely that the greatest penetration will come in applications where space savings are highly desirable, such as microinverters for photovoltaic systems, or power supplies for data centres.

There's no question that SiC growth is a huge opportunity for the power semiconductor industry, but it's not easy to see MOSFETs getting to the price of silicon IGBTs. Instead, they offer another option for the power electronics engineer, who has the opportunity to use the SiC MOSFET and the silicon IGBT concurrently. Thanks to overarching growth trends of electrification, electric vehicles, and renewable energy, there is the potential for a significant growth in sales of both device types; and industry should continue to develop IGBT technologies to aid the green transition.



➤ The historical and forecast revenue for the silicon IGBT and the SiC MOSFET. Data has been normalised to the 2023 revenue of IGBT technologies.

Clas-SiC expands technology in its stride

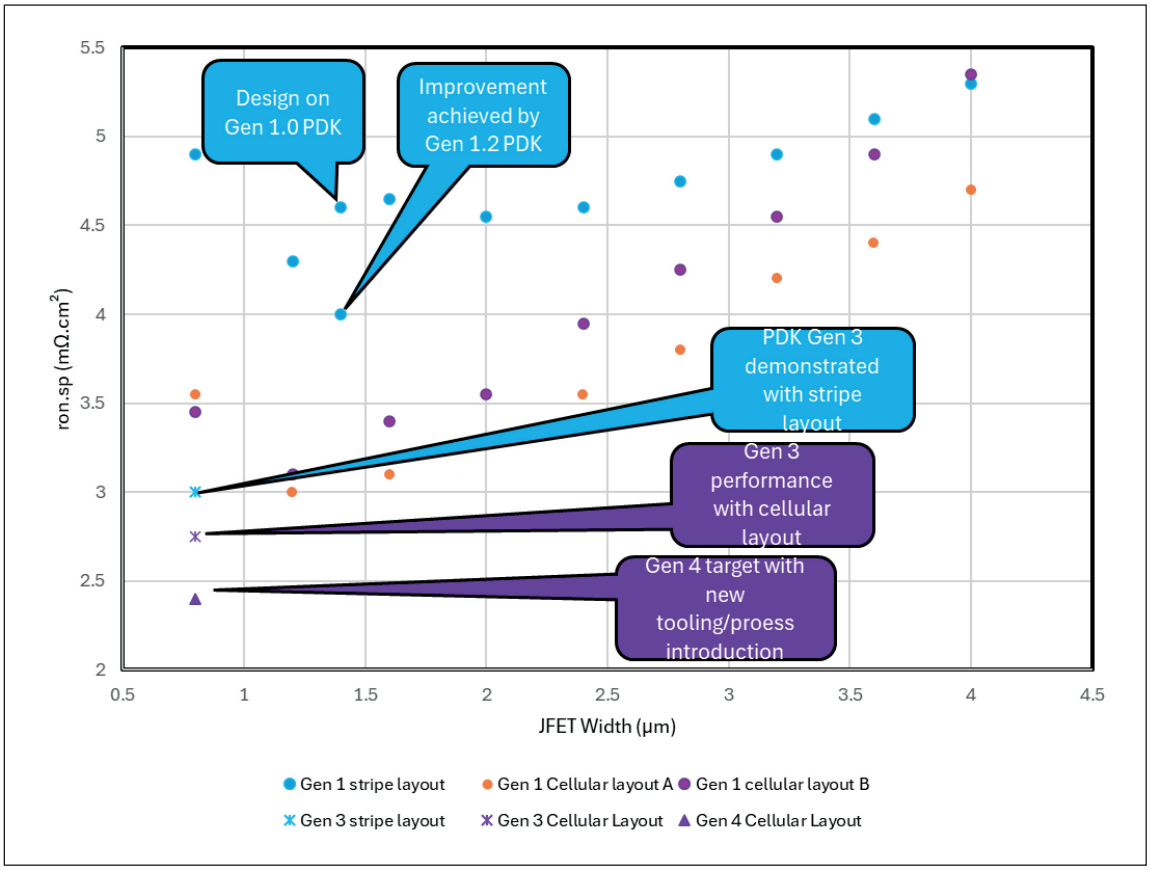
Not content with opening the world's first SiC foundry that partners with power device designers, Clas-SiC Wafer Fab is evolving and adapting to grow its success

BY JEN WALLS AND DAVID CLARK FROM CLAS-SIC

FOUNDED IN 2017, Clas-SiC Wafer Fab is the world's first open foundry dedicated to SiC. At our facility, located in Lochgelly on the outskirts of Scotland's capital city, Edinburgh, we have adopted a pure-play approach, which means that we'll never be in competition with our device customers. Instead, they draw on our standard process flows and flexible Process Design Kits (PDKs) to simply and quickly design highly customised SiC devices. By using PDK models to minimise non-recurring engineering and trim the cost and cycle time, our customers can work with us to produce a range of competitively priced SiC transistors and diodes operating at 650 V, 1.2 kV, 1.7 kV and 3.3 kV on both conventional and engineered SiC substrates.

Our mission is to provide a low barrier to entry for all of our customers seeking to develop new products. We support them at every step, from proof-of-concept to market seeding, low-volume production, right through to high-volume production. This sets us apart, as we are the only foundry in the SiC industry that takes customers through all stages of product lifecycle. Most of our business comes from the manufacture of enhancement-mode MOSFETs, but we also produce depletion mode MOSFETs and two forms of diode – the merged *p-i-n* Schottky diode, and the junction barrier Schottky diode. We use PDKs to support a high level of integration, during successful customer designs for highly customised unique devices, even to the extent of including integrated sensors as part of the device design. Our customers can have confidence in these PDKs – as well as having reliability proven on our reference devices, they have been used by customers that conduct reliability trials on their own specific devices, with efforts on this front demonstrating that our foundry produces devices that satisfy AEC-Q101 using JEDEC 22 conditions.

Since releasing our initial generation of PDKs in 2022, we have been working on developing Generation 3 PDKs. These successors deliver significant improvements in the performance of 1.2 kV planar MOSFETs, realised by shrinking transistor dimensions (see Figure 1). With favourable wafer-level results, Generation 3 devices are currently undergoing reliability trials, ahead of a scheduled release at the end of 2024. In parallel we are qualifying devices fabricated on engineered substrates to add to our PDK offerings.



➤ Figure 1. Reducing the width of the JFET is leading to a reduction in specific on-resistance.

We are now starting to turn our focus to Generation 4 MOSFETs. They feature a shrinking of the transistor interconnect, a refinement that enables a further reduction in cell pitch and thus a corresponding reduction in specific on-resistance. To produce these transistors, we are investing in upgrading and expanding our tooling.

Right now, we are on the cusp of this exciting new phase, with the new tooling being identified, procured and installed ahead of interconnect technology development. Our timescales are governed by tool delivery times, and we are forecasting the introduction of our Generation 4 PDK in 2026. We plan to begin our Generation 3 and 4 technologies on 1.2 kV MOSFETs, before subsequently extending this technology to 1.7 kV and then 3.3 kV variants.

While we are currently focusing on planar MOSFET technology, this has not stopped us from conducting trench processing work for specific customer projects. As part of this effort, we are investing in process tooling to expand our trench processing capabilities, and support the possibility of developing our own trench MOSFET PDKs in the future.

We have drawn on our standard process modules that underpin our PDKs to fabricate novel trench and planar SiC MOSFETs, using heavily customised process flows. In addition, we have adopted this approach to produce *p-n* diodes, JFETs, and other customised devices, including both lateral and vertical device architectures.

As well as producing a wide range of SiC devices, we are active in UK innovation-based funding calls. They include APC (Advanced Propulsion Centre), DER (Driving the Electric Revolution), as well as the EU Horizon scheme. Projects in progress include an automotive BEV/FCEV project, a Solid-State Transformer project, and a project for Condition & Health Monitoring in Power Electronics. To keep close to technology advances, we are maintaining close academic links with research teams in the UK, at the University of Glasgow and Warwick, as well as overseas, such as at Purdue University.

Our innovation surrounding process development extends beyond 'normal' process advancements. We are closely involved in wafer fabrication tool development, partnering with major industrial players that advance semiconductor equipment design. This extends through to our work with substrate and epitaxy providers, to help them validate their materials for the market. Through this work we are advancing the world of SiC device processing.

As well as technology development, which is the R&D part of our business and where we tend to begin our engagement with customers, we have another two business streams. They are Low-Rate Production (LRP), and Licensing, Royalty and Consulting (LR&C) (see Figure 2 for a summary of our business streams).

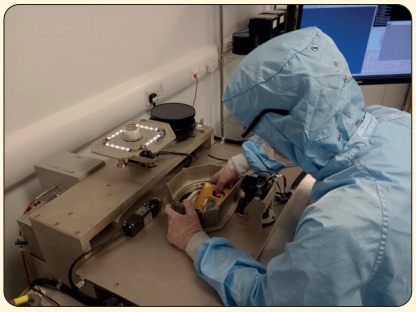
Views from Clas-SiC apprentices

Clas-SiC has a strong, well-established apprenticeship programme. Below, told in their own words, are the stories of three of those involved: Dani Johnston, a Modern Apprentice Manufacturing Equipment engineer (top left); and Duncan Colston (bottom left) and Kieran Healy (bottom right), both Graduate Apprentice engineers.

I AM IN MY final year as a Modern Apprentice at Clas-SiC Wafer Fab. My journey with this unique company started in 2020. I began as an operator, before I was given the opportunity to progress my career as an apprentice equipment engineer.

Starting off as an operator allowed me to gain a lot of understanding and knowledge of not only each tools' capabilities, but also an insight into the various processes applied to semiconductors. This has benefited my ability to fulfil my role within the apprenticeship programme.

While progressing towards my HNC qualification I have gained a wide variety of experience by working alongside very knowledgeable process, equipment and facility engineers, who have guided and mentored me. My responsibilities as a equipment engineer include carrying out tasks such as preventative maintenance, fault diagnosis, and testing mechanical and electrical equipment.



I AM REALLY enjoying the second year of my apprenticeship experience with Clas-SiC. It is a challenging but rewarding environment, where I have been surrounded by knowledgeable people to help me get the most out of my apprenticeship, both on the work side and with university.

At university I am working through my degree, which is a BEng design and manufacture (electrical) at Heriot Watt University in Edinburgh. I attend once a week and complete work-based learning tasks, and write reports on those tasks to consolidate my knowledge and complete the modules, along with gaining hands-on skills through working in the cleanroom.

I have gained a lot of relevant knowledge in the past year working in the test department, and spending some time working in the photolithography department. There has always been someone to help me when I'm stuck or confused. I started with learning the basics of operation, for example, how to run the tools and process batches. Now I am being introduced to more of the process aspects in semiconductors. I've also enjoyed the exposure I've had so far with the layout of the devices with the software we use, as I had an interest in CAD drawing at high school.

THE GRADUATE apprenticeship programme inside Clas-SiC has given me the opportunity to gain valuable industry skills whilst still having the possibility to be recognised with an educational degree (BEng – Engineering design and manufacture; electronic) that will be important for my future. Being local to me, Clas-SiC provides an easy stepping stone into the semiconductor industry, in which I have been able to gain an appreciation for the industry and its significance in the world.

My experience at Clas-SiC has been positive, and I am now in the third year of my studies. I have been able to work alongside experienced engineers who are happy to share their knowledge with me. This has accelerated my development in both semiconductor knowledge and process engineering skills, learning different ways to carry out tasks such as data collection/presenting.

My time has been spent on a mix of day-to-day activities (monitoring SPCs, keeping batches moving etc.) and being involved in larger projects (process optimisation, development of new products), with a larger focus on the etching processes, dry and wet.

I have had support, where needed, from the Clas-SiC team. This has helped me in my university learning, where I have been able to lean on expertise to aid my understanding of topics, as well as with aspects such as time management. During my apprenticeship I have been given various opportunities to represent the company, attending schools to talk about Clas-SiC and the opportunities available, as well as events such as awards evenings.

I am looking forward to continuing my learning with Clas-SiC on their journey in SiC and hoping I can be a part of their growth.

Our LR&C business stream enables customers with ambitious expansion plans to ramp up to high-volume/low-cost manufacture. This initiative provides support for independent foundries in low-cost manufacturing locations, such as those in Asia, to set up replicas of Clas-SiC processes. Our capacity in Scotland is limited to low-rate production, so this model allows us to access much higher volumes without Capex investment, keeping prices down for our customers.

For those that work with us under LR&C contracts, the norm is that a defined portion of their capacity is reserved for Clas-SiC customers. When our customers outgrow the capacity of Clas-SiC foundry, we outsource production to one of these associated but independent fabs. Throughout this evolution our customers maintains their partnership with us, utilising our advancing PDKs for their next-generation devices as they start another R&D cycle.

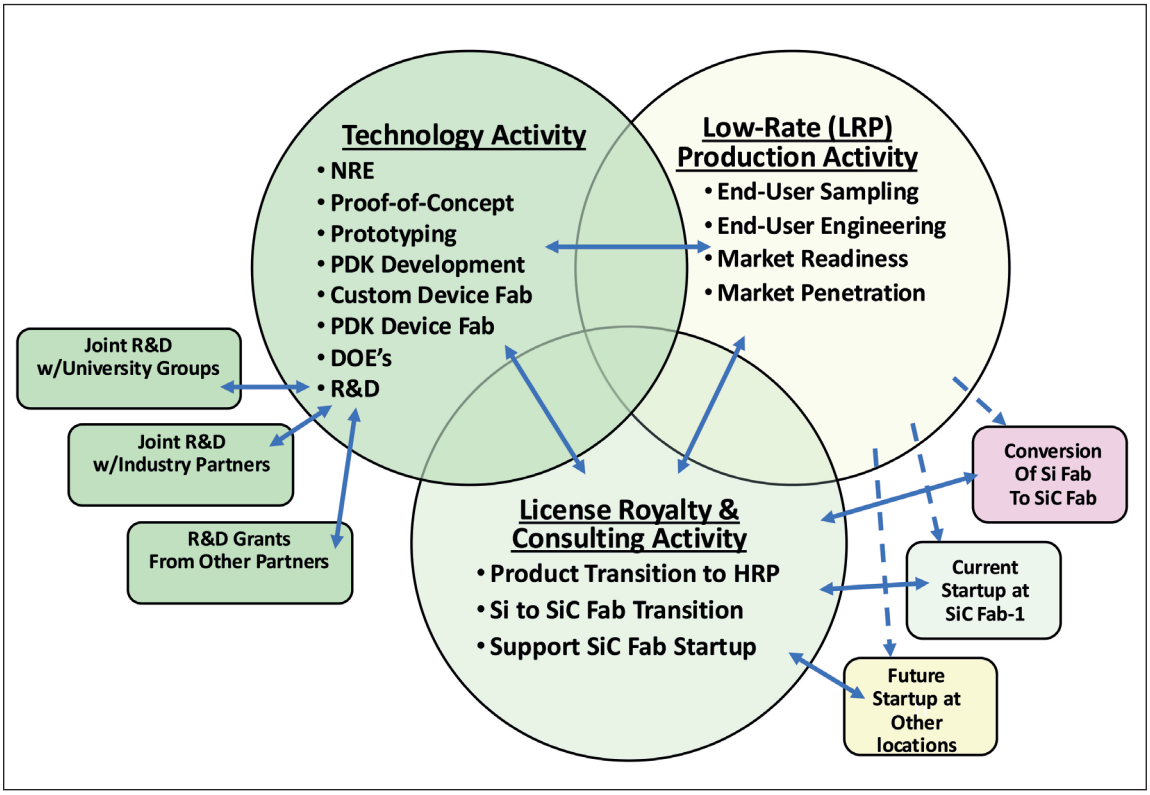
The first wafer fab utilising this model is now well advanced. Supported by our team, this fab has been constructed, facilities and tooling are installed, processes have been set up, and production will soon begin. We also have a number of other potential LR&C projects at the stage of advanced discussion.

Key to our success is our continual re-investment, not only in capital equipment, but also in our people. Our staff, with their advanced skill sets and out-of-the-box thinking, are our greatest asset. We now have more than 320 man-years of experience in SiC device processing, putting us in an unrivalled position for taking on the challenges of our customers. We pride ourselves in the continual development of our workforce, from our production operators through to our senior management team.

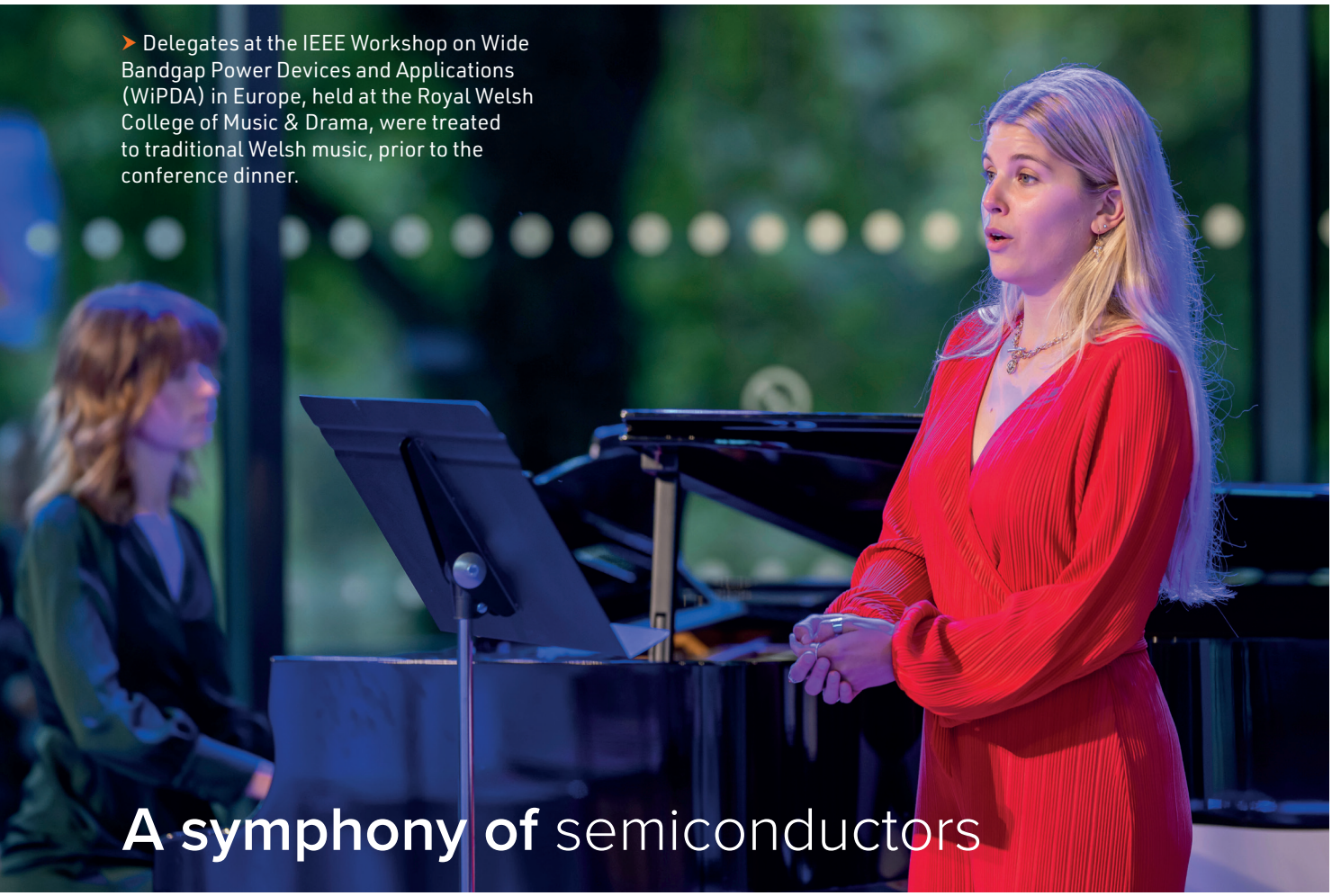
Training has been crucial to our advancing over the last year, as we have undergone exceptional growth and transitioned to a 24/7 operation for device production. More than 80 percent of our direct labour has received advanced training to fully utilise and build their skillsets, a move that has led to a more flexible and satisfied workforce. Our investment in new entrants, in the form of modern apprentices and graduate apprentices, is also well advanced. As well as ensuring that we keep the talent pipeline in a healthy state, this introduction of 'young blood' maintains a well-balanced age demographic within our workforce.

Despite the tough investment environment throughout the world, we have managed to secure equity investment from Archean Chemical Industries Ltd. We are excited to have them on our team and looking forward to the exciting times ahead. This funding will help to grow our business, supporting the launch of Gen 4.0 technology in 2026, as well as strengthening our Board of Directors.

We have been privileged to have both the financial support and the wisdom of knowledgeable investors since our foundation. One of our founding members, Carl Johnson, launched a CdTe crystal growth company just over fifty years ago that has blossomed into Coherent. By drawing on this expertise, we are well supported in our efforts that will see us take Clas-SiC to the next level and beyond.



➤ Figure 2.The business stratergy of Clas-SiC Wafer Fab



➤ Delegates at the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA) in Europe, held at the Royal Welsh College of Music & Drama, were treated to traditional Welsh music, prior to the conference dinner.

A symphony of semiconductors

Industry-facing academics championed the capabilities of devices based on SiC, GaN and Ga_2O_3 at the recent European workshop on wide bandgap power devices and applications

BY RICHARD STEVENSON, EDITOR, CS MAGAZINE

IT'S WONDERFUL to listen to a beautiful voice singing *a cappella*, or a guitar in the hands of a maestro. But for many, this is eclipsed by great singer fronting a talented band or a professional orchestra playing a wonderful symphony. Why do we feel that way? It's probably a reflection of the harmony, the interplay and the rich variety that comes from hearing different instruments playing different parts.

Parallels can be drawn between these musical experiences and the state of play in today's power electronics industry. Once dominated by just silicon, this is now complemented by a growing portfolio of wider bandgap semiconductor, each with a particular set of attributes that come together to offer the designer a tremendous palette for constructing circuits. There's GaN, delivering great efficiency and incredibly fast switching without a significant increase in cost while operating at several hundred volts; SiC, a more mature technology that's well-suited to handling higher voltages; and Ga_2O_3, with the potential to outperform this duo, thanks to an even higher bandgap, along with the promise of lower costs that stem from melt-growth of crystal boules.

Promotion of this symphony of semiconductors came from many of the speakers at the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA) in Europe, held on 16-18 September, at the Royal Welsh College of Music & Drama, part of Cardiff University. At this venue, where delegates were treated to traditional Welsh music in the run up to the conference banquet, a number of keynote speakers emphasised the need to improve the efficiency in electrical systems, through refinement to circuit design and the introduction of better devices, as well as outlining the pros and cons of the many diodes and transistors within the wide bandgap portfolio.

The big picture

It's easy to feel overwhelmed and powerless when thinking about climate change. This makes it tempting to bury of one's head in the sand. But that's never ideal, given that action is required – and particularly so for us, given that our industry has a very important role to play in decarbonisation.

A good reminder of the alarming consequences of global warming, along with the opportunities for power electronics to combat this, despite the implications on global resources resulting from a ramp in their production, came from the opening keynote address from Johann Kolar from ETH Zurich.

Kolar began his presentation by pointing out the need for a clean energy transition, which demands an all-electric society. He explained that today CO_2 emissions stand at 40 gigatonnes, and questioned whether humanity is going to succeed in meeting the goal of net zero by 2050, suggesting it may take 50 years from now to reach this target.

If we are not going to reach net zero, it's prudent to prepare for climate change, argued Kolar, who outlined efforts to accommodate a rise in sea level.

He explained that there are engineers in The Netherlands that are thinking about building really huge dams to enclose the North Sea and prevent roughly 25 million people from having to deal with increasing sea levels. By the end of this century, many people other parts of the world could also be having to deal with a rise in sea levels, including those in parts of east Asia, Brazil and the east coast of the US. "Time is running out," warned Kolar.

The ETH academic went on to consider the energy requirements of humanity, which currently stand at around 2.5 kW per person. By 2050 this figure will have increased a little, while the global population will have climbed to 10 billion, leading to a total power demand of around 27 TW.

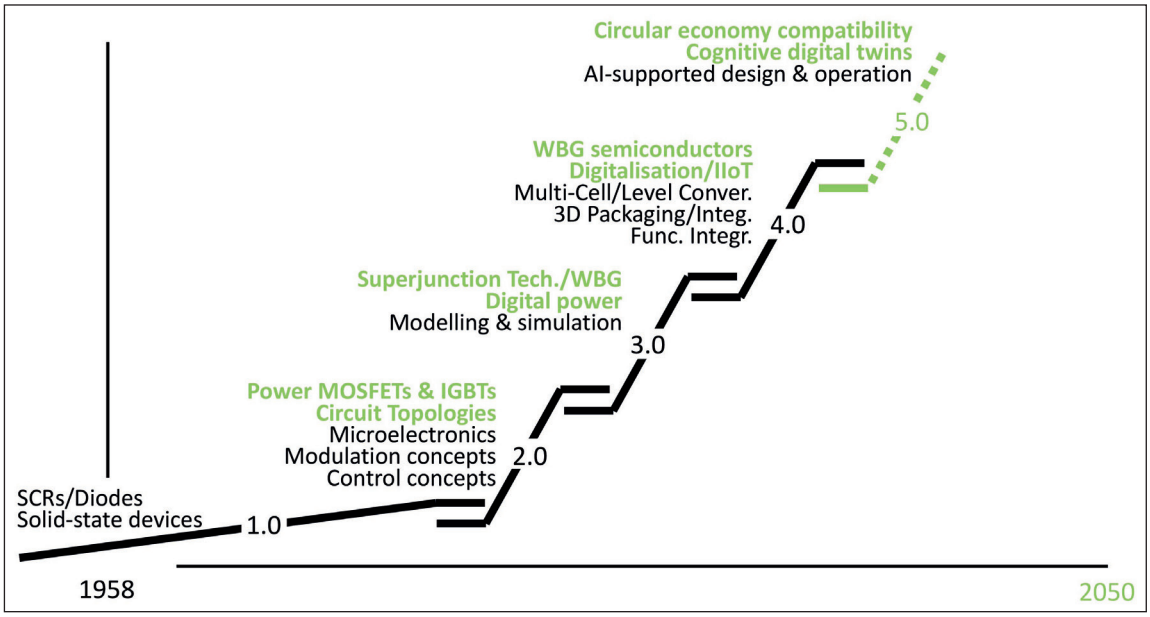
The good news is that this figure is dwarfed by the power from the sun. If we consider just the sunlight falling over land, its power is still roughly a thousand times higher than that required by humanity.

Helping us to tap into this power is the rising deployment of renewable energy. According to forecasts shared by Kolar, deployment of photovoltaics and off-shore wind power are set to increase at compound annual growth rates of 9 percent and 7 percent, respectively, until 2050. By then sunlight will provide 8.5 TW of power generation, and off-shore wind another 5 TW.

For these renewable deployments, power electronics has a fundamental role to play, argued Kolar, who pointed out that it is needed to convert the electricity generated by these sources into a form that can be fed into the grid. However, he believes that improvements are needed to these critical components, such as reductions in cost, failure rate, weight and losses, as well as an acceleration in the time-to-market.

During his presentation, Kolar provided a whistle-stop tour of the evolution of the modern power electronics industry. He sees the starting point as 1958, the commercial introduction of the thyristor. This device dominated through to the 1970s, before the introduction of the first MOSFETs, the first bipolar transistors and then IGBTs, along with new circuit topologies and some microelectronics. The next big breakthrough came in 1995, with the introduction of superjunction technology. By the turn of the millennium digital power had also attracted much attention.

Over the last decade and more, SiC has been an increasingly significant player in the power



➤ Johan Kolar from ETH Zurich suggested that the power electronics industry is in its fourth era, and championed a move to a circular economy that involves recycling of materials when moving to the fifth era.

electronics sector, added Kolar: "In industry, from 2015 you could see more and more applications of silicon carbide components. This, for sure, is one of the X technologies. What is an X technology? It is aiming for a factor of ten improvement."

SiC and GaN both offer this, with substantial reductions in on-resistance over silicon. However, more thought needs to be given to making the most of this with appropriate circuit design. While engineers have been designing circuits for many years, Kolar emphasised that there is still much room for improvement in their architectures, and offered a number of examples where his team have made significant advances.

Moving towards an all-electric society will help with decarbonisation, but there is a price to pay, a significant consumption of resources. Due to this, Kolar is championing the need for far greater re-use of electronic materials. He argued that if we move to 25 TW of installed electrical energy generation, due to four steps associated with conversion from source to load, total global installation would equate to 100 TW. He went on to point out that 20 years of lifetime means that there would be 5 TW of electronic waste per year. This means that we need to not just think of the technology and the design. Kolar is urging a shift from a linear economy, which is already generating close to 50 million tonnes of waste per year, to a circular one that involves the re-use of critical materials, and zero end-of-life waste.

Device comparisons

A more detailed look at the family of power devices came from Florin Udrea, a Cambridge University academic and the founder and Chief Technology Officer of Cambridge GaN Devices.

Udrea pointed out that all the wide bandgap materials outperform silicon in one key characteristic: the breakdown field strength. "Silicon carbide is ten times better, GaN even more, and arguably diamond and gallium oxide are the star contributors there – they are classified as ultra-wide-bandgap semiconductors."

While the breakdown field is the most important metric for power semiconductors, there are others that are also important, according to Udrea, such as thermal conductivity. Judge on this front, silicon is reasonable, but SiC and diamond are much better. "This is where gallium oxide has a problem, because it has very low thermal conductivity. It behaves more like an oxide than a silicon carbide," remarked Udrea.

Another metric that matters is carrier mobility. "Gallium nitride is incredibly interesting, because it's the only material that beats silicon not only in terms of the critical electric field being higher, but also in terms of the mobility," remarked Udrea. He pointed out that the carrier mobility in Ga_2O_3 is relatively low, and while silicon has a high intrinsic mobility, it collapses after doping and falls at elevated temperatures.

Udrea summarised the properties of all the key materials in a table (see Table 1). He championed those with a wider bandgap, reasoning that this leads to a higher critical electric field that in turn enables the fabrication of scaled-down devices that feature a smaller drift region with a higher doping concentration, key to ensuring a higher efficiency.

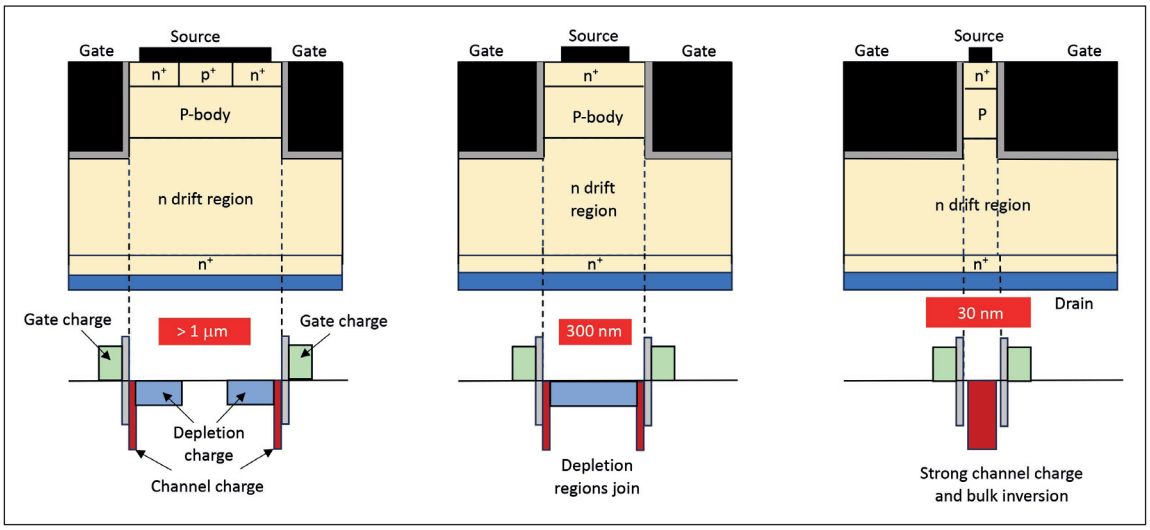
Of the leading alternatives to silicon, while those with the ultra-wide bandgaps may have the biggest promise, Udrea is sceptical about their prospects. Although he believes that diamond and Ga_2O_3 are interesting from a materials science perspective, he is concerned by the low thermal conductivity and an absence of *p*-type doping in Ga_2O_3, and the absence of *n*-type doping in diamond.

Although the coming years will see a substantial rise in the sales of wide bandgap devices – led by SiC MOSFETs, SiC Schottky barrier diodes, and GaN HEMTs – Udrea is adamant that silicon will still have a significant role to play. That's partly due to its strengths, in terms of its reliability, ease of manufacturing, infrastructure, cost, as well as its diversity, attributes that provide a significant advantage, according to Udera.

What's more, silicon is not as far behind its wider bandgap rivals as one might expect, in terms of performance. With a critical field that's lower by a factor of around ten, and an on-resistance proportional to the cube of this, one might expect silicon devices to be completely outclassed by the

System and technology key aspects	Silicon	4H-SiC	GaN	Diamond	Ga_2O_3
Efficiency/performance					
Size/form factor					
Reliability					
Ease of manufacturing					
Infrastructure					
Cost					
Diversity					

➤ Table 1. The strengths and weaknesses of the key materials in power electronics, according to Florin Udrea. Green denotes strength, yellow a satisfactory performance, and red highlights weakness.



➤ Figure 1. One option for lowering the on-resistance of SiC transistors is to switch from a MOSFET to a finFET.

likes of GaN and SiC. But that's not the case, with silicon overcoming its limit described by Baliga's figure of merit, due to a number of sophisticated device designs, such as the superjunction and the power MOSFET.

Udrea highlighted the revolutionary performance of the silicon superjunction transistor: "It's not 10 percent or 20 percent better than the MOSFET. It's orders of magnitude better." This is realised by increasing the doping in the drift region by a factor of around 100.

Another important silicon device is the IGBT. This has evolved over several decades, with the latest design, known as a trench field stop IGBT with an electron injector, combining strengths of punch-through and non-punch-through structures by incorporating a very thin drift region and an electron-injection mechanism.

The superior material properties of SiC and GaN allow for far better performance when replicating designs based on silicon. Udrea illustrated this, comparing the silicon power MOSFET with that made from SiC. Thanks to a ten-fold hike in the critical electric field, it's possible to shrink the thickness of the doping region by this factor – and by also increasing the doping concentration in this region by around 100 times, there's the potential for a 1000-fold hike in conductivity. In practice, such gains are not possible, due to a relatively high channel resistance and a low mobility, but despite this, the gains are substantial.

"But remember, we are not competing against this now," warned Udrea, who explained that when up against superjunction devices, SiC is only better by a factor of seven or eight – and when it comes to the IBGT, it's even less.

Opportunities for SiC and GaN

However, there are other advantages with SiC, such as its capability to switch at higher frequencies. To make the most of these strengths, one needs to fully understanding the properties of this material, argued Udrea. He cited a study by Kimoto Tsunenobu's group from Kyoto University that uncovered that compared to the A-face of SiC, the C-face has a higher mobility and a higher critical field strength.

The SiC devices on the market today are predominantly offering blocking voltages between around 600 V and a few kilovolts. However, there's a peak in performance at around 1 kV, according to Udrea.

He shared data showing contributions to the specific on-resistance from the channel, the drift region, the substrate and other factors, for SiC MOSFETs operating at 600 V, 1.2 kV and 3.3 kV. At the highest voltage, drift resistance dominates, and at the lowest resistance the channel resistance is the most significant factor. At the 1.2 kV sweet spot, where there are substantial sales for the traction inverter, both the channel and the drift are important. Looking to the future, Udrea wants to see SiC superjunction devices for high voltages, finFETs for lower voltages, and finFET superjunctions for devices handling around 1 kV.

In silicon the finFET is well established, with Udrea describing this class of transistor as the most advanced digital structure of today. He championed the development of SiC devices based on this architecture, using the SiC MOSFET as a starting point. For this device, with a *p*-body width of more than 1 µm, the pair of depletion charges and channel charges are balanced by the gate charge (see Figure 1). Shrinking the width of the *p*-body causes depletion charges to merge and then disappear, and re-position all the gate charge in the channel. When the *p*-body is reduced to 30 nm or so, quantum effects also aid performance, which benefits from total inversion in the bulk rather than on the surface.

According to Udrea, SiC finFETs with these dimensions benefit from an increased electron charge, along with bulk inversion and elimination of the transverse electric field, two factors that reduce

➤ Florin Udrea, an academic at the University of Cambridge and the CTO of Cambridge GaN Devices, championed advances in SiC and GaN devices, such as superjunctions, fins and multiple channels.

the likelihood of Coulombic scattering. All these gains help to trim the on-resistance.

Working with partners at Mirise Technology Corporation, an R&D institution supported by Denso and Toyota, Udrea and colleagues at Cambridge University have produced a range of finFETs with different fin widths. With fins just 35 nm wide, mobility increases to more than 200 $cm^2 V^{-1} s^{-1}$, a substantial increase over the standard mobility in SiC transistors.

Udrea also outlined progress in superjunction devices made from SiC, which unlike some other wide and ultra-wide bandgap semiconductors, can be doped *n*-type and *p*-type, a requirement for this device architecture. He predicts that this device will be commercially available within a few years, and based on modelling, explained that performance can be maximised by optimising both the width and doping of the pillars, and moving from a 2D to a 3D superjunction.

...and GaN

Udrea went on to champion GaN, comparing the silicon laterally-diffused MOSFET to the GaN HEMT. Thanks to internal piezolelectric fields in the latter, no doping is needed to produce a channel that provides a carrier mobility of around 2000 $cm^2 V^{-1} s^{-1}$. Additional strengths are: a high critical electric field strength, enabling a ten-fold reduction in device size; and an opportunity for isolation on the chip, enabling the construction of power IC blocks.

According to Urea, makers of GaN devices fall into two camps. There are those that make discrete enhancement-mode HEMTs, including Cambridge GaN Devices, Innoscience, and Infineon; and there are those that employ a cascode structure and use a depletion-mode HEMT, an option pursued by Transphorm and Nexperia. Udrea pointed out that the latter approach has the benefit of addressing the poor gate reliability of the GaN HEMT, but with two devices in series, there are reverse recovery losses.

Another key differentiator in the market is the level of integration. While the discrete is the norm, some companies have gone further. One example is Navitas, which has integrated the driver. “This solution has worked, and it’s in the market, and has done very well in the low power [regime],” remarked Urea, but he feels that at higher powers there are concerns related to heat generation and efficiency.

At Cambridge GaN Devices they have adopted a different approach, referred to as sensing and protection. “We chose to integrate what is necessary, but we left the driver outside,” explained Udrea. Merits of this design include a high degree of robustness, and the opportunity for the engineer to access the driver. This allows the use of very intelligent, multi-channel drivers, a level of functionality that is much easier to realise in silicon than GaN.

Like SiC, which is advancing with superjunctions and finFETs, the architectures for GaN are advancing. Udrea highlighted the multi-channel E-mode HEMT that his team has helped to pioneer, an innovation led by Yuhao Zhang’s group at Virginia Polytechnic Institute and State University. This device, operating in a cascode configuration, is said to benefit from extremely good conduction, thanks to the introduction of five layers of two-dimensional electron gas. And in terms of the combination of breakdown voltage and on-resistance, it is breaking new ground, according to Udrea.

Enhancing production processes

Supporting the UK’s capabilities in producing compound semiconductor devices is the recently constructed Centre for Integrative Semiconductors at the University of Swansea. Its strengths were described by Mike Jennings, Head of Energy and Power Engineering at Swansea University, who explained: “Our interest is working with industry, to take prototype devices and scale them with our manufacturing process. We are working across all materials.”

Drawing on investment from the UK government from 2019 to 2024, and supported by industrial partners, the Centre for Integrative Semiconductors has around 1,000 m^2 of cleanroom, equipped with more than 60 tools that can process 150 mm and 200 mm wafers. Within this facility, focused on power electronics, is an industrial process line for the design, fabrication, testing and pilot production of SiC, and a tool for the growth of Ga_2O_3. The centre is also home to advanced dielectric and dry etch specialities. “Dry etch is probably our forte,” claimed Jennings. “We can etch pretty much any material to any depth, through our close relationship with KLA.”

Jennings discussed a range of materials and devices, including opportunities related to the 3C form of SiC. While this has a lower bandgap than GaN and the 4H polytype of SiC, and thus a lower critical electric field strength and breakdown voltage, it is a very attractive candidate for making robust devices. “If you want a really reliable MOS interface

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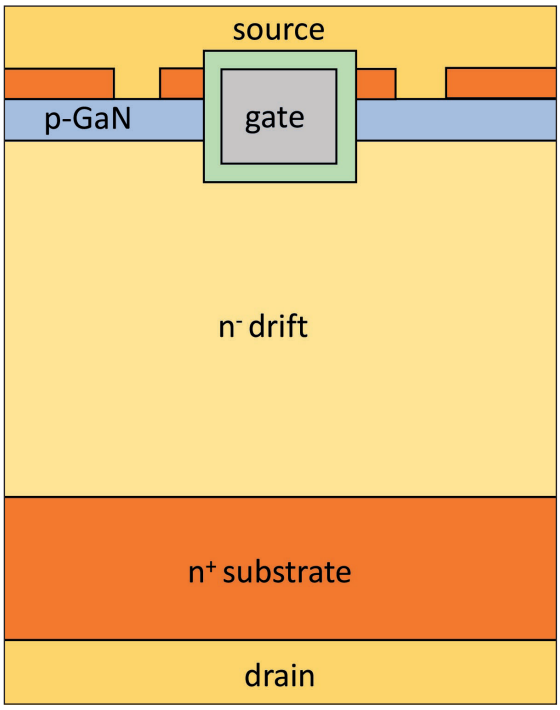


➤ Figure 2. Strengths of the vertical trench GaN MOSFET include a blocking voltage that is governed by vertical dimensions and the possibility for avalanche capability.

gate oxides, then cubic silicon carbide is the dream," enthused Jennings, who explained that 3C-SiC has a bigger band offset with SiO_2 than silicon. Due to this, Fowler-Nordheim tunnelling across the oxide-semiconductor barrier, the main failure mechanism, is 1.5 times less in 3C-SiC than silicon, and around 2.25 times less than it is for 4H-SiC. In addition, there is the promise of a far lower density of interface states in 3C-SiC than 4H-SiC.

Experimental work by Jennings and colleagues is underscoring the potential of 3C-SiC. Capacitance-voltage measurements on the interface between the semiconductor and the dielectric formed with a range of treatments has revealed a density of interface states below that of silicon, and far, far lower than that for 4H-SiC.

Jennings said that the most exciting work that he's currently engaged with is that of the vertical GaN transistor. He compared this device with the lateral GaN HEMT, which benefits from a high mobility in the two-dimensional electron gas that gives some great characteristics, such as the absence of reverse recovery losses and extremely fast switching. "But the blocking voltage depends on the distance between the drain and the gate, which is problematic when commercialising technologies above 650 volts, such as a large-area die," remarked Jennings, who also pointed out the lack of avalanche capability.

➤ Mike Jennings, Head of Energy and Power Engineering at Swansea University, is helping to lead efforts at the recently established Centre for Integrative Semiconductors.

A vertical trench GaN MOSFET (see Figure 2) addresses both these issues, and features a standard MOS gate that is easy to drive. However, there are concerns associated with the mobility in the channel and the need for *p*-type doping.

"The question is: Can this be competitive? Can we get that channel mobility good enough that it will be commercially viable?" remarked Jennings, who also pointed out the need to extract the heat from this high-current device. To help to answer these questions, Jennings and colleagues fabricated quasi-vertical GaN-on-SiC MOSFETs with a 2.5 µm-thick drift layer that are designed to handle up to 200 V. Initial results are encouraging, with a very low series resistance of 8.5 mΩ cm^2, and a breakdown voltage of 220 V.

Opportunities with Ga_2O_3

A keynote presentation from Martin Kuball from the University of Bristol detailed the promise of Ga_2O_3, alongside approaches to accommodate its weaknesses, by pairing this oxide with other materials.

In terms of substrate size, it's already possible to buy 4-inch material, and there are research demonstrations up to 6-inch, according to Kuball: "You could think about commercialisation at that moment in time, because the substrate size of gallium oxide is already at the level where you could do manufacturing."

Kuball pointed out that devices made from Ga_2O_3 have the potential to withstand very high electric fields while exhibiting an incredibly low on-resistance. However, there's a need for thermal management, to compensate for the low thermal conductivity of this oxide, and to introduce new materials to provide *p*-doping within the device, if it's required.

Among a number of devices that Kuball and his colleagues are developing, arguably the most exciting is that incorporating a superjunction, based on the pairing of *n*-type Ga_2O_3 and *p*-type diamond, which is used to fill trenches. Back in 2021 the team simulated such structures, using realistic properties for diamond that account for a lower thermal conductivity due to the grain structure, and found that this still led to a dramatic improvement in thermal management. This work also showed that by optimising charge balancing and adjusting

Martin Kuball, Director of the UKRI Innovation and Research Centre REWIRE at the University of Bristol, is driving development of Ga_2O_3 devices featuring hetero-integration.

the field distribution, it's possible to boost the breakdown voltage quite significantly.

Working with Stanford, Kuball and coworkers have started working towards the fabrication of superjunction devices, looking at sidewall properties. Initial structures have a breakdown voltage of 900 V, limited by the peak electric field not sitting at the interface between the two materials. Addressing this could increase the breakdown to 5 kV or more.

"Just to point out, it's not good diamond. It's nanocrystalline diamond, so there's still need for optimisation," revealed Kuball, who views these early results as quite promising.

He clearly has many plans for the future, as do all of those working on the development of wide bandgap devices and the design of the circuits that incorporate them. There is much to look forward to, due to these harmonious efforts.

Turn to page 52 to discover more about the development of Ga_2O_3 devices by Martin Kuball and his co-workers and collaborators in "Enhancing β-Ga_2O_3 with hetero-integration".

Around 130 delegates attended the IEEE Workshop on Wide Bandgap Power Devices and Applications in Europe, held in mid-September at Cardiff University.

Progress opens the door to viable quantum markets

Recent successes in the scale-up of quantum photonic components is giving the green light to system-level product manufacturers looking to capitalise on Quantum 2.0 effects

BY DENISE POWELL AND WYN MEREDITH FROM THE COMPOUND SEMICONDUCTOR CENTRE

WHILE INTEREST in quantum technologies is eclipsed by that in AI, it is still grabbing a great deal of attention. And that's not surprising, given that this sector is forecast for tens and even hundreds of billions of dollars per annum over the coming years.

Such figures are attracting individuals and companies with an entrepreneurial spirit to consider pursuing opportunities in quantum markets. That includes system integrators, looking to leapfrog from successful demonstrators to commercial quantum products.

Unfortunately, it's not easy for system integrators to succeed in this endeavour. As well as having to overcome the significant technical difficulty of realising robust quantum systems, their progress has been held back by two critical obstacles. The first of these is having access to a wide pool of end-users willing to commit time and resources to evaluating systems and creating use cases. And the second, more fundamental obstacle to the viability of quantum markets, is that unless quantum laser sources and detectors are readily available at sufficient yields – and thus acceptable price-points – quantum technologies will always be limited to high-margin and low-volume mission-critical applications.

Here we will focus on the latter issue. When tackling this, it's important to note that the specifications governing quantum photonic components (QPCs) are so tough to fulfil that unviable processes will prevent component prices from falling to acceptable levels, thereby creating a barrier for volume markets to emerge. Quantum markets are not immune to the basic principles of supply and demand, and end-users must evaluate where the quantum advantage delivers a justifiable benefit within their product offerings.

While this outlook is not what many wish to hear, it is not merely pessimism, but reflects manufacturing process controls. In a well-controlled environment that is adhering to a 6σ methodology, control limits encompass the process distribution, while the specifications relating to the product are wider, to ensure zero defects.

During the manufacture of many forms of compound semiconductor devices, it's not unusual for them

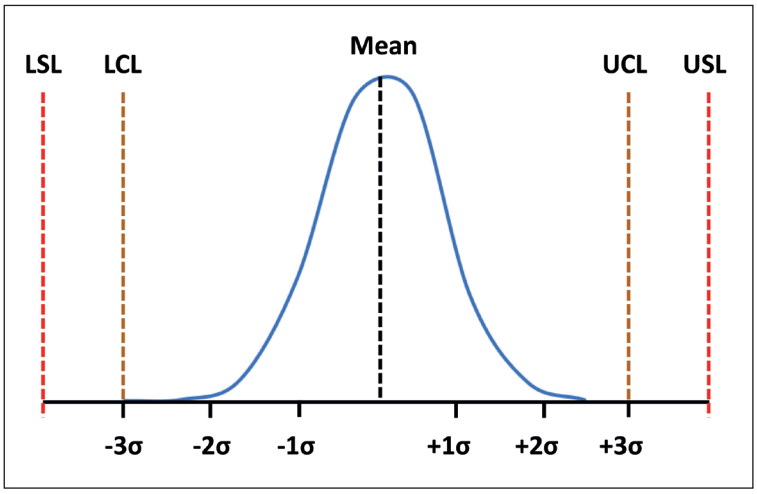
to fall outside the 6σ standard. However, when that happens, product specifications governing industrial processes tend to generate budget yields that are still sufficiently viable for market adoption. For QPCs, however, the situation is starkly different, with product specifications only encompassing a small proportion of standard manufacturing process capabilities.

So what does this mean? Let's consider the VCSEL, a class of laser that's employed to pump and probe transition lines of atomic species when it is serving in quantum applications. The typical uniformity of epiwafers used for high-volume VCSEL products, such as for sensing applications, is too non-uniform for quantum applications. An epiwafer controlled to the same uniformity distribution would only provide a narrow ring that is suitable for QPC device fabrication, if we assume that the wafer's uniformity has a radial profile. Making matters even more challenging, there's a need to meet tight specifications at the device level on parameters such as power and single-mode operation. Given all this, we can expect that commercially viable yields for QPCs will be extremely low. While it is possible to produce thousands of die on a single 100 mm wafer, an incredibly small proportion of these lasers are going to be single-mode, polarisation-stable VCSELs that combine the right output power with acceptable values for threshold current, temperature and current-tuning coefficients, and also fall inside the stringent operating temperature window while emitting a near-perfect beam profile.

Is it unreasonable to pick the VCSEL in this discussion of QPCs? Certainly not, given that VCSEL fabrication is a relatively mature process. Difficulties arise because it is challenging to scale device production for quantum applications, due to the stringent specifications required, as well as the need for single-mode performance.

To help address this challenge, since September 2020 our team at the Compound Semiconductor Centre has led a project involving twelve partners across the UK aimed at improving the manufacturability of QPCs. However, the ultimate goal of this £5.8 million three-year programme, which is known as QFoundry and is part-funded by the UK Quantum Technologies Challenge, under UK Research & Innovation, is the establishment of robust and resilient supply chains that are committed for the long-run.

The QFoundry project has focused on the viability of QPCs that are urgently needed for the commercialisation of demonstrator systems in atomic clocks, quantum magnetometers, gyroscopes, lidar and quantum key distribution. These applications are viewed as relatively mature at the systems-level compared to quantum computing, suggesting market adoption will be earlier. This expectation is in-line with a number of publicly available roadmaps, including the *Optica*

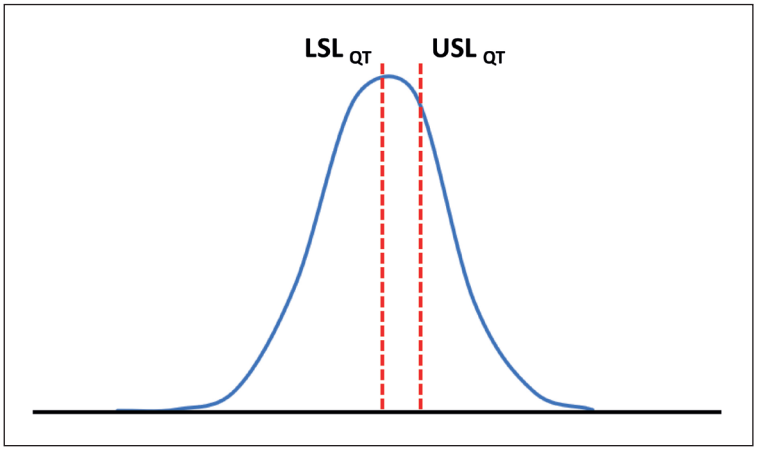


➤ Illustration of an ideal, under-control 6σ process that operates within the product specification limits.

Quantum Photonics Roadmap: Every Photon Counts, released in 2020. Supporting this prediction are reports arguing that quantum computing business models are more likely to be based on high-value/low-volume, shared-access hardware, while sensing and quantum key distribution applications will drive relatively higher volumes at the QPC-level – making the latter a more attractive business proposition for compound semiconductor supply chains.

Status quo for semiconductors

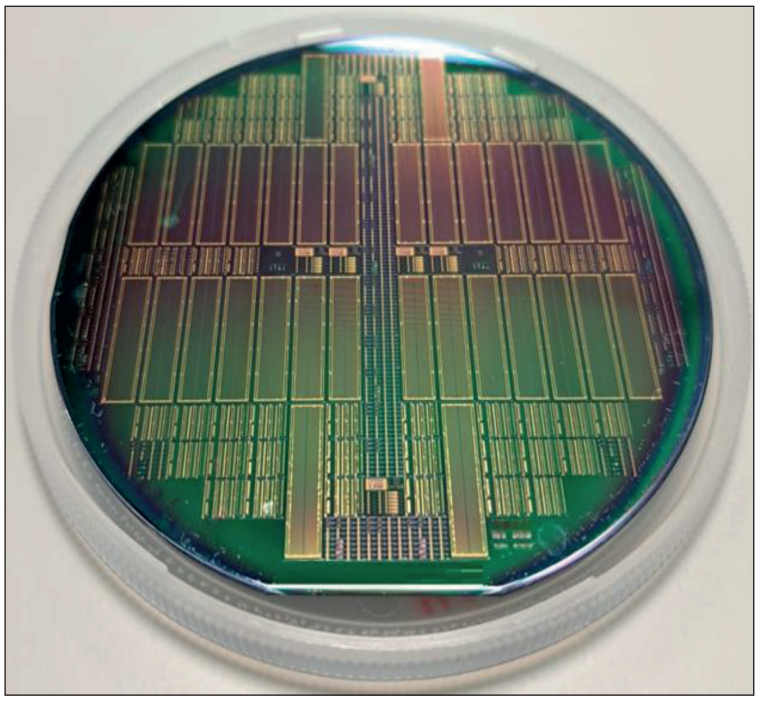
Scale-up is, undoubtedly, the latest buzz phrase to hit the quantum scene. For industrial semiconductor supply chains, however, this task is their bread and butter; each new technology platform has to undergo extensive scale-up activity to understand and address critical process interactions, establish control limits and ensure inherent manufacturing repeatability, reproducibility and reliability. These principles have underpinned the QFoundry approach to deliver notable progress across VCSELs, quantum dots and single-photon avalanche diodes (SPADs).



➤ Illustration of typical relationship between the overall manufacturing process distribution to the lower and upper product specification limits (LSLQT and USLQT) for quantum applications.

➤ Automated die bonding at Bay Photonics of customised TO-can packages for atomic clock applications.

Following three years of activity, the UK supply chain is now offering the world's broadest portfolio of single-mode VCSELs tailored to quantum applications, with lasers spanning 760 nm to 940 nm. Encouragingly, these VCSELs are manufactured with a threefold improvement in yield at the device level as a result of efforts to drive semiconductor material uniformity at CSC, and major advances in device design, chip fabrication and characterisation by the team at Integrated Compound Semiconductors.



➤ Successful scale-up of SPAD fabrication from 50 mm to 75 mm substrates at the University of Cambridge.

What is particularly pleasing is a reduction of almost 60 percent in the R&D effort and cost required to develop a new device against custom specifications, thanks to improvements to the models that are designed to closely match manufacturing processes. These models have been refined through iterative development, enabled by QFoundry. Another triumph is that these devices have realised more than 10 years of operation at 70 °C under accelerated ageing conditions, demonstrating that they can serve in atomic clocks deployed in low earth orbit applications. To increase their capability for these missions, we plan to carry out additional device reliability testing.

QFoundry has derived much benefit from its technology validation partners, such as Toshiba and the National Physical Laboratory (NPL). These collaborators have expertise in validating QPCs in custom, application-relevant testbeds.

Our efforts have re-enforced our view that quantum technology development desperately needs supply chain partners that translate application requirements through to appropriate component specifications. Progress on this front has been a big factor in the success of QFoundry.

One example, highlighting this point, is the identification of system-level noise caused by standard TO-can packaging. The team at NPL are leading experts on atomic clocks and were able to identify the problem and work closely with Bay Photonics on re-designs and custom package development. Following successful demonstration, those at Bay have invested in the automation of VCSEL packaging, and are now ready to support the quantum community with volume ramp.

For quantum dots and SPADs, the challenges are starkly different to those faced for the VCSEL, despite also using iterative development for material and process improvements. This discrepancy is due to decades of industrial research in the epitaxial structures and fabrication of the VCSEL, which has propelled this device to a technology readiness level that is well ahead of that for quantum dots and SPADs. Much effort has been devoted to materials development, to address the background emission of quantum dots and the dark currents of SPADs. Progress has also required a lot of manpower to ensure that the fabrication processes lead to robust device operation.

Despite these challenges, the QFoundry quantum dot and SPAD partners have made significant progress. Milestones for quantum-dot development include the development of reproducible droplet epitaxy on an industrial MOCVD reactor, as well as: forming structures that produce a low-background emission from different growth methods, the realisation of functional fabrication processes, and recording long coherence times at telecom wavelengths.

Many may question whether the gruelling efforts across the QFoundry partners make sense, given that quantum markets are yet to be established. But there are times when supply chains must take the long-term view and co-invest in technologies, even though entry into mainstream markets is a question of when, rather than if

Our SPAD development has benefited from previous prototyping. Drawing on this expertise, partners in the QFoundry partners have scaled-up epitaxial growth from 50 mm to 75 mm wafers with processes that allows the detector's temperature to be managed with thermo-electric cooling, thanks to extensive custom butterfly package development at Bay Photonics.

The advances that we have made, in terms of the technology readiness level, are giving confidence to quantum system communities. While challenges remain, we are seeing a viable pathway to robust supply of quantum photonic components. The next step is for the quantum community to work hand-in-hand with the compound semiconductor supply chain to ensure that system-level development does not run away with specifications that further constrain the viability of quantum technologies.

Is it really worth it?

Many may question whether the gruelling efforts across the QFoundry partners make sense, given that quantum markets are yet to be established. But there are times when supply chains must take the long-term view and co-invest in technologies, even though entry into mainstream markets is a question of when, rather than if. The quantum industry is in a situation that can be likened to a Mexican standoff, where someone has to pull the trigger first. It is only when supply chains are robust and validated that system integrators can commit to offering quantum systems. In this case, QFoundry partners have dived headfirst, but they are reaping rewards that are far greater than ever anticipated.

Quantum is perhaps one of the few mystifying areas of research, where the sum of the parts is definitely bigger than the whole, as well as the whole being bigger than sum of the parts. Developments across each step of the supply chain have yielded incredible insights and capabilities that would have never come during more typical laser and detector development. We have uncovered subtle, yet critical interdependencies and process interactions that govern QPCs that sit deeply within the relatively slack tolerances associated with standard, non-quantum applications.

Those of you that have had the pleasure of visiting high-tech research facilities, such as the UK's Harwell Campus, will appreciate the enormity of the capability that must be developed in order to address unknown unknowns that arise. What can initially appear as a distraction often leads to insights and know-how that can be rewarding beyond the original scope and goals of a technical challenge.

Ultimately, a significant amount of expertise and intellectual property has been developed across the QFoundry partner base, with the project establishing robust supply chains that do not shy away from hard-to-hit specifications. On the other hand, semiconductor foundries serve markets best when specifications converge, which is equally relevant to quantum systems.

One of the legacies of QFoundry is that it has set the scene for an industrial approach to addressing the viability of quantum markets. Timing is everything and having established baseline process windows, all the partners in QFoundry are ready to work with the quantum community in developing custom QPCs across different verticals. The work is never complete in the semiconductor industry; product launches are followed by intensive continuous improvement, and quantum technologies are at the very beginning of their journeys. But one thing is certain: there is no world of quantum without compound semiconductors.

➤ The 12 partners in the QFoundry project.





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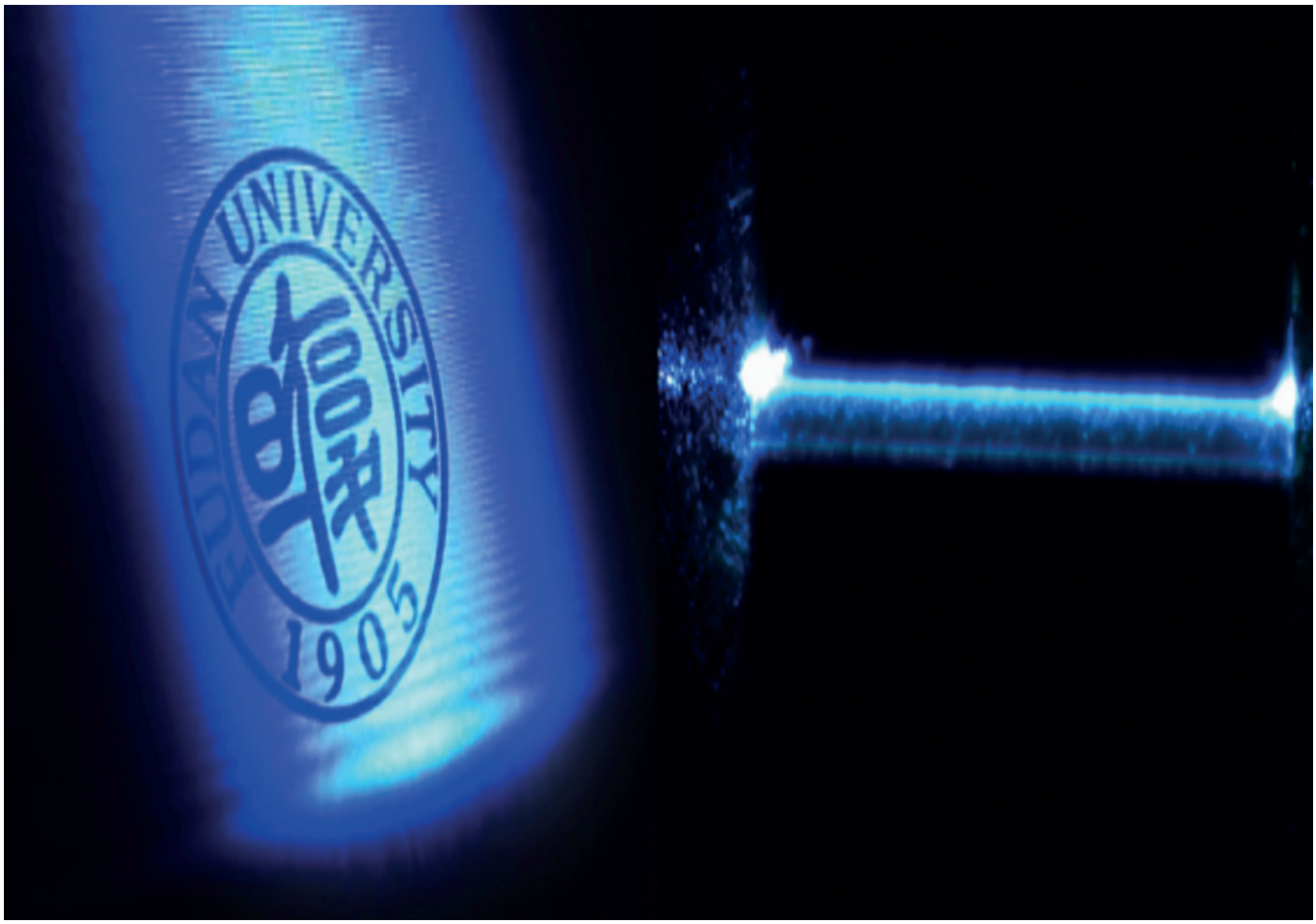


Targeting ubiquitous communication with GaN lasers

Visible communication based on GaN lasers will empower wireless and optical networks

BY CHAOWEN GUAN, NAN CHI AND CHAO SHEN FROM FUDAN UNIVERSITY

WHILE SCIENCE FICTION often falls short of depicting the current capabilities of technology, it still offers a glimpse into potential future advancements. A prime example is Marvel Comics' hero Iron Man, whose body armour has evolved since its debut in 1962. In recent iterations, Tony Stark's suit features nanoscale devices that communicate with one another. For science fiction to become science fact, such body armour would require formidable capabilities in high-speed data transmission.

Although we are unlikely to try and exactly mimic Iron Man, there are moves to more wearables, along with the rapid development of technology for 6G wireless data links. Within this infrastructure, visible light communication (VLC) is poised to play a crucial role. VLC is expected to provide wide-coverage communication across space-air-ground-underwater domains at ultra-high speeds and low latency. In the future, light could even be used to power the Internet of X-things.

What is VLC?

The term 'visible light communication' is relatively self-explanatory. It refers to a wireless optical transmission technology that utilises visible light for data communication within the spectral range 380 nm to 790 nm.

In stark contrast to traditional wireless communication, which grapples with a scarcity of spectral resources, visible light communication enjoys an abundance, boasting a bandwidth of

around 400 THz. This vast expanse of untapped potential beckons human exploration and innovation. Additional strengths provided by VLC are an immunity to radio interference, an absence of electromagnetic radiation, and high confidentiality. However, the biggest advantage of VLC is its high speed. Today's lab record for data transmission stands at over 20 Gbit/s, a rate so high a wireless download of a movie in the Ultra HD format takes just a few seconds.

A typical VLC system comprises three main parts: a visible light transmitter, a channel for transmission, and a receiver. Information transfer begins with encoding, modulating, and pre-balancing the signal in the optical transmitter. Transmission then occurs through free space to reach a receiver, where either a *p-i-n* photodiode or an avalanche photodiode converts the optical signal into an electrical one. This is followed by equalisation, demodulation, and decoding to restore the original transmission signal.

Today there are two significant limitations with VLC systems. One is associated with the transmitter, such as a high-speed blue laser, in intensity-modulation direct-detection systems. This soure is held back by a relatively small bandwidth, as well as a level of maturity that falls far short of its counterparts operating at around 1550 nm. The second limitation is the slow development of key components, such as external modulators, amplifiers and balanced photodetectors in coherent modulation systems.

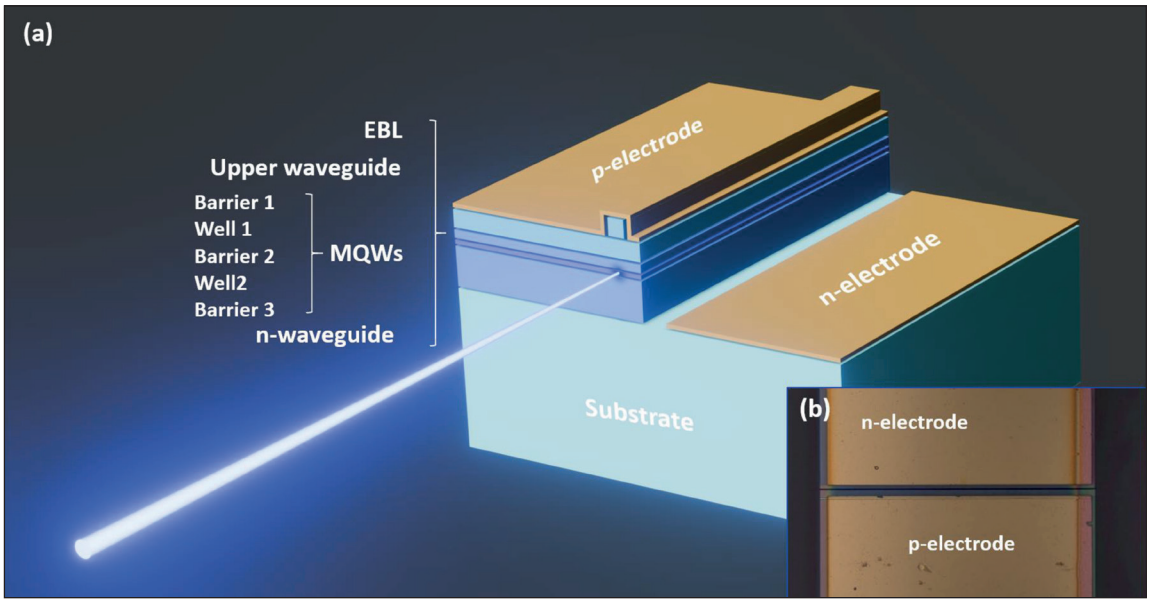
At Fudan University we are striving to address these all limitations, initially by developing a novel GaN laser that offers a higher modulation rate.

High-speed sources

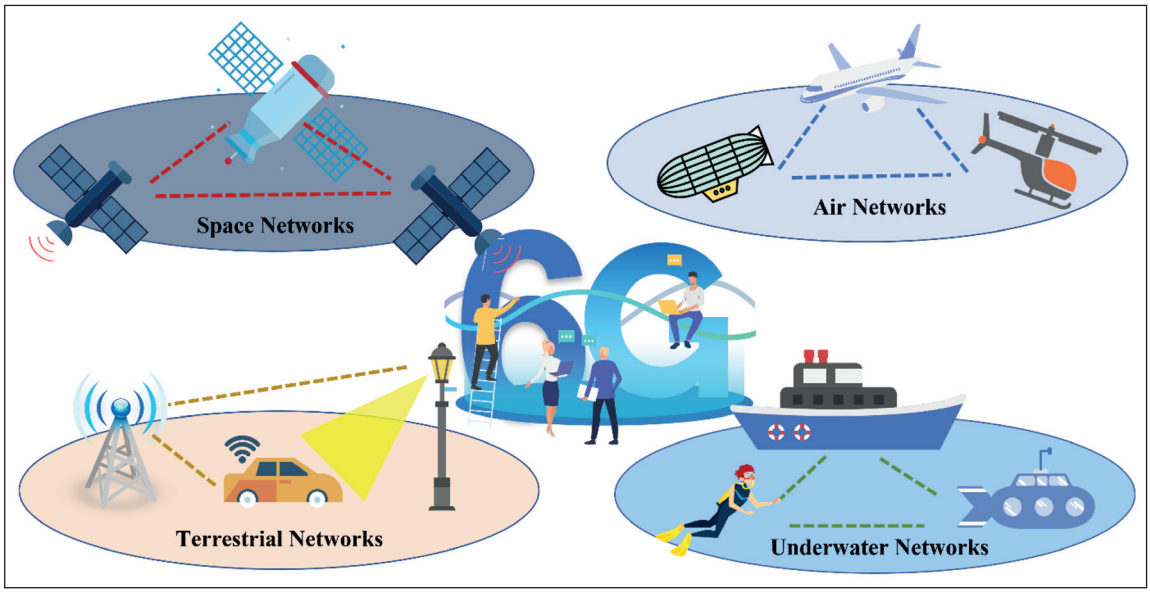
As the ancient Chinese saying goes: *A craftsman who wishes to do his work well must first sharpen his tools*. We have taken this advice to heart in developing a GaN-based laser, a fundamental component for white light and a promising source for underwater wireless optical communication. At present, GaN-based lasers emitting in the purple, blue, and green are primarily deployed for the likes of optical storage, lighting, displays, and material processing, with a focus on DC characteristics, such as output power and slope efficiency. Since there is a strong built-in electric field presented in blue lasers fabricated on *c*-plane GaN substrates, owing to polarisation effects, researchers are utilising semi-polar and non-polar GaN substrates to eliminating such polarisation fields. This enables to a better efficiency and a higher modulation bandwidth. However, the supply of GaN substrates with suitable orientations is limited.

Our efforts at developing high-speed GaN-based lasers have considered both the design of the epitaxial structure, including the active region and the electron-blocking layer, and the device architecture, such as the ridge waveguide. Through simulation of various epi-structures we have uncovered design rules that have led us to an improved frequency response in InGaN/GaN quantum well lasers, with findings subsequently verified by experimental work.

Measurement and characterisation of our high-speed lasers has involved the detailed analysis of light-current-voltage characteristics, emission spectra, junction temperature, relative intensity noise, frequency response, and data transmission performance. We have obtained the threshold current and slope efficiency of our lasers by determining light-current-voltage characteristics. The intrinsic parameters of our lasers have been further extracted. The -3dB modulation bandwidth can be derived through small-signal frequency response testing. During this work we gained much insight into the influence of design on performance – for example, the influence of different waveguide layer structures, with thicker ones found to lead to a more divergent light field that increases its overall volume. The optimal thicknesses for the



(a) Laser epitaxial structure. (b) Microscopic photographs of the high-speed blue laser diode chip.



VLC application scenario.

p- and *n*- waveguide layers are 50 nm and 150 nm, respectively.

As is the case for the LED, shrinking the dimensions of the laser diode offers a promising route to improving its high-speed operation. We have found that a shorter cavity enhances the modulation performance, thanks to a smaller optical field volume. However, this comes at a cost, with increased mirror loss and a suppression of the damping effect. Despite these drawbacks, we have demonstrated a high-speed blue laser-based VLC system achieving a transmission rate as high as 20.06 Gbit/s, and a variant with green lasers reaching 17.73 Gbit/s.

Building on the rapid development of laser-based VLC technology, we are refining this technology for a world with better connectivity. Our vision for VLC includes indoor systems that combine lighting and communication, as well as long-distance and underwater wireless optical communication. To turn these ideas into reality, our lab is pursuing innovative designs and practices.

VLC for mobile...

When laser diodes are deployed in VLC systems, they promise a high modulation bandwidth and output power, attributes that can lead to high-speed, long-distance communication. However, as laser diodes produce a narrow beam, pointing and alignment are required in laser-based optical wireless links, which limits the mobility of communication systems. VLC with a wide coverage transmitter and enhanced mobility offers a fundamental advantage for wireless services by providing users with flexibility and convenience, while enabling connections while on the move. Therefore, we go beyond a point-to-point VLC link and are trying to figure out a way to address mobile-communication-related challenges.

Progress has come from leveraging a laser-based light transmitter with wide spatial coverage, enabling a VLC system with a mobile receiving end. Using on-off keying (OOK), which is the simplest modulation technology, a data rate beyond 500 Mbit/s has been achieved in laser-based white light VLC link. Transmission is stable at distances of both 1 m and 2 m, and the system is capable of supporting a transmission rate of 500 Mbit/s when it's moving at 0.48 m/s. Although distance and mobility impact the system's performance, it is able to maintain a considerable degree of reliability and efficiency.

... indoor illumination...

One key advantage of VLC is that it can combine illumination and communication. To ensure that this is realised with a low carbon footprint and reduced operating costs due to compatibility with lighting systems, VLC may not come from increasing the number of light sources. Instead, it is a good idea to expand the field-of-view of a single light source.

A white light source is designed by combing a blue laser array, a diffuser, a plano-convex lens, and a ceramic phosphor plate. The laser-based white-light source exhibits excellent stability, with an irradiation range extending to a half-angle of 20°. To ensure high spectrum-utilisation efficiency, we employ discrete multi-tone bit-loading modulation. With this approach, we divide the laser's bandwidth into 256 sub-carriers, each matching the modulation order based on its bit error rate. Using this transmitter in a VLC system, a peak data transmission rate of 3.24 Gbit/s has been achieved, spanning 1 m to 5 m. The results are promising for demonstrating a long-distance, wide coverage, high-speed VLC link for mobile network applications, as well as the feasibility of utilising a white-light emitter based on a laser for solid-state lighting.

... and satellite interconnects

Up in space, one important trend is the building of satellite constellation. This has implications for

real-time data links between multiple satellites that require communication methods with high capacity, low latency, and high reliability. Laser communication is often used between satellites. Currently, infrared band is chosen for inter-satellite and satellite-to-ground communication, due to the matured devices and systems. Moving forward, given the radiation hardness of GaN and its associated alloys, the blue laser might be a useful source for inter-satellite optical wireless communications, such as those involving low-earth orbit satellites to provide internet access.

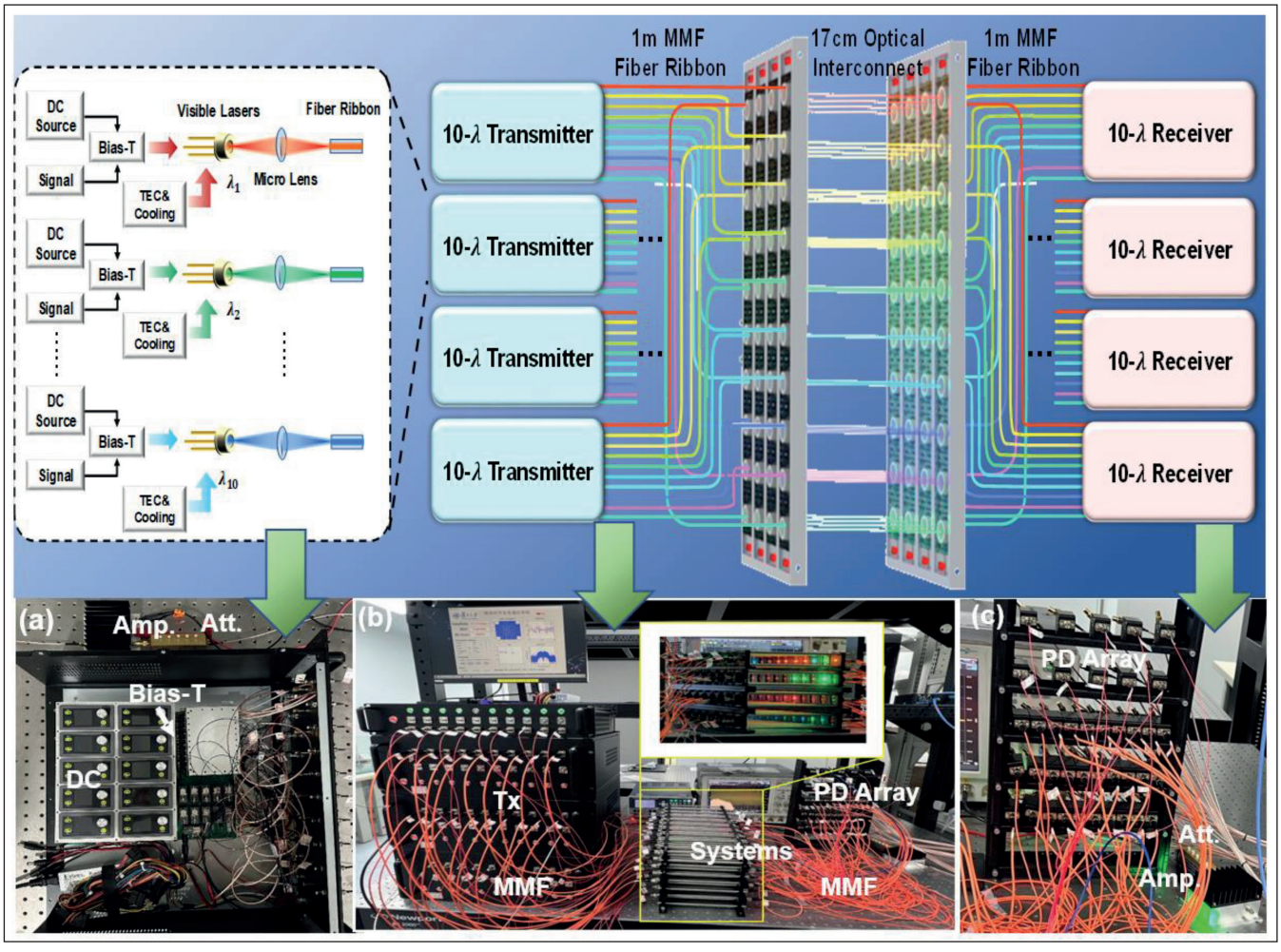
To advance inter-satellite communication via VLC, we have focused on increasing communication capacity and distance. For the former objective, we have been investigating the capability by using wavelength-division multiplexing (WDM) technology. Using a 40-channel WDM VLC system, we have achieved a total transmission rate of 418.3 Gbit/s, employing discrete multi-tone bit power loading and a Levin Campello algorithm. In terms of increasing the communication distance, we applied bidirectional reservoir computing to a VLC waveform for symbol-level equalisation, an approach that enabled us to record transmission at 11.2 Gbit/s over a free-space distance of 100 m.

Video streaming underwater

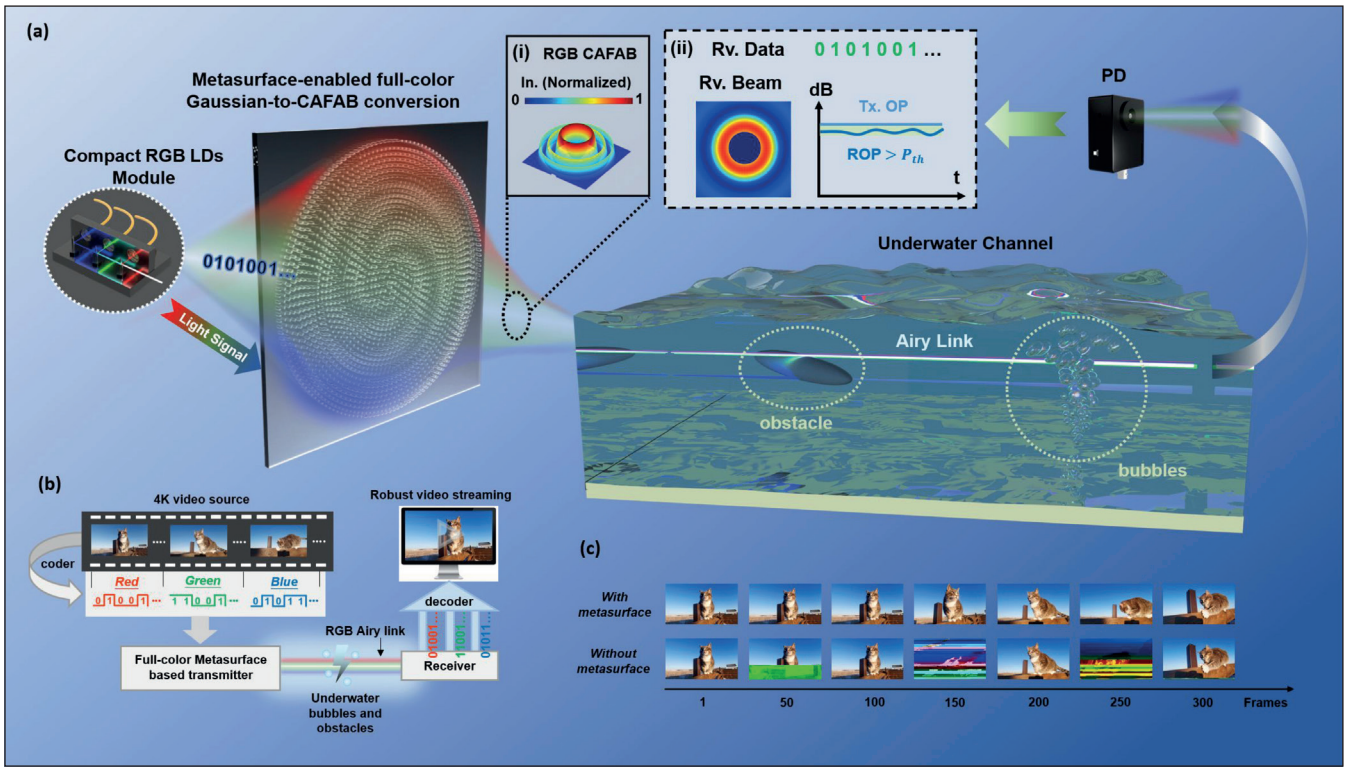
Another important application of VLC is underwater wireless optical communication (UWOC). Due to the presence of a blue-green transmission window in seawater, lasers emitting in this spectral domain are attractive candidates for enabling an underwater wireless data link.

At present, the main challenge facing UWOC is the prevalent time-varying and complex channel characteristics. A typical laser-based UWOC link is based on Gaussian beams. When disturbances such as bubbles, turbulence or obstacles are present, the quality of the beam reaching the receiver end degrades. Typical issues include a decrease in light intensity and a violent drift motion of the beam centroid. As a result, delivering stable, high-speed data transmission over long distances is challenging.

Our team is addressing this challenge by introducing a high-efficiency visible ultra-broadband auto-focusing Airy beam meta-surface. In the self-focusing area, the obstruction caused by small-scale obstacles is reduced by the energy carried in the sidelobes; and in the divergent region, the unique circular energy distribution of the Airy beam enhances the system's adaptability to obstacles.



The design of a wavelength-division multiplexing VLC system, and the corresponding physical prototypes.



Airi Light under water optical communication system based on a meta-surface. (b) Underwater 4 K video streaming using the full-colour meta-surface system. (c) Received video frames with and without the full-colour meta-surface at different frame sequences.

Thanks to this meta-surface design, which exhibits a high polarisation conversion efficiency over a broad spectral range spanning 440 nm to 640 nm, the data transmission rate of wireless optical communication systems is increased by 91 percent, enabling reliable 4K video transmission via WDM using underwater optical communication data links.

Looking ahead, there are still many challenges to overcome in laser-based VLC. Much progress is required to propel the modulation bandwidth of GaN-based laser diodes to tens of gigahertz. While the telecommunication community is focusing on optical links operating at 100 G bit/s to Tbit/s, researchers in the VLC community are just entering the game, with data rates of tens of Gbit/s.

Moreover, today's VLC systems are employing intensity-modulation direct-detection. This is because external modulators, amplifiers, and other important optical communication components in the visible spectrum are still missing. Meanwhile, the development of coherent VLC systems has just started, calling for the introduction of narrow linewidth lasers and high-speed balanced photodetectors.

In our efforts to advance VLC, our team is working with global partners to develop high-performance III-nitride optoelectronic devices and visible light photonic integrated circuit technology. Together with international collaborators, we are striving to realise an environmentally friendly, energy-saving, low-cost, and high-speed laser-based VLC technology as a vital component of the 6G network.

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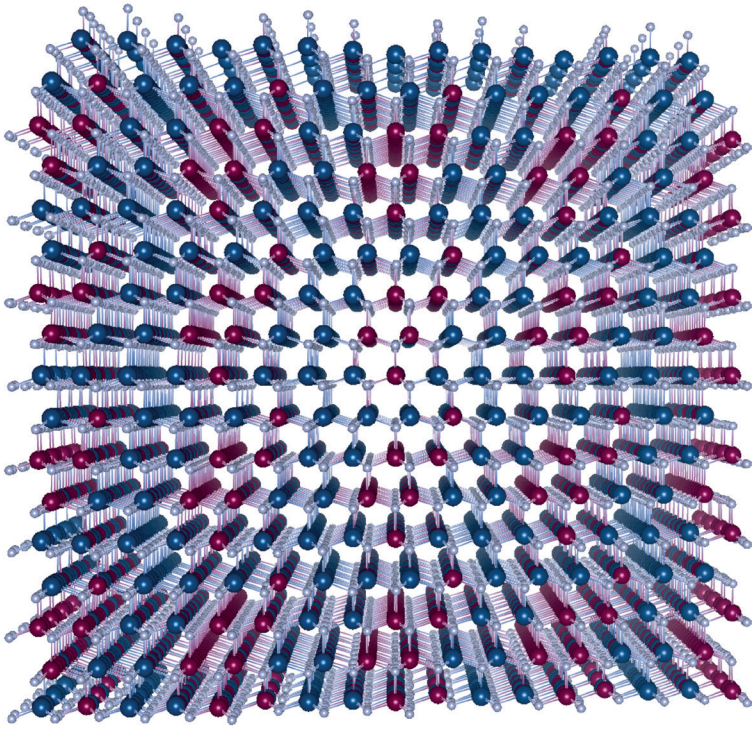
A red revolution with quantum machine learning

Quantum-mechanical modelling and machine learning can accelerate the design of semiconductor devices, such as polychromatic LEDs based on InGaN

BY NICK PANT FROM THE UNIVERSITY OF TEXAS AT AUSTIN

AT THE HEART OF HUMANITY'S digital revolution is device miniaturisation. Efforts began with the scaling of the transistor, shrinking at a rate described by Moore's law. Now the LED is following suit, with these miniature marvels promising to unleash a new generation of display technologies that seamlessly blur the lines between reality and virtual reality. Due to this, there are tremendous opportunities for microLEDs in mini projectors in mobile phones, as well as in 3D near-eye glasses and other applications, where they will deliver a tremendous improvement to wearable displays. Such advancements will reshape our interactions with the digital world by influencing how we consume media, access education, and connect with our colleagues.



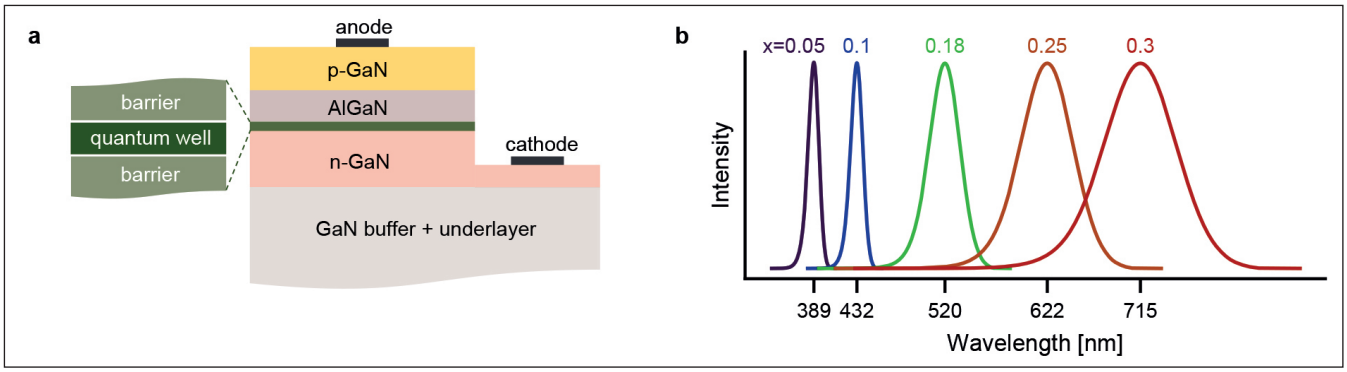
➤ Atomic structure of an InGaN alloy

However, we should not get ahead of ourselves. While miniaturisation of the LED holds much promise, its execution poses significant engineering challenges.

One of the greatest obstacles to success is related to the materials that are used to produce these emitters. Blue and green LEDs are made with InGaN quantum wells (see Figure 1 (a)), while those that emit in the red feature quantum wells made from InGaP. These two classes of semiconductors have entirely different crystal structures, with lattice constants that differ by 30 percent – for epitaxial growth, that's an enormous disparity. Due to this, it is exceedingly difficult and expensive to create monolithic micron-scale pixels by integrating red InGaP LEDs with their green and blue InGaN cousins.

An alternative way forward is to produce red, green and blue LEDs with one material system. Take this route and there's only one choice, InGaN – it is the only commercially proven semiconductor with a bandgap that can be compositionally tuned across the entire visible spectrum. To propel its emission to longer wavelengths, engineers have to increase the indium content in the well, as this narrows the bandgap (see Figure 1 (b)). Producing an all-InGaN polychromatic pixel is viewed as the holy grail of microLED research, because it circumvents all the difficulties associated with integrating InGaP with InGaN.

Unfortunately, the light-emission efficiency of InGaN plummets with increasing wavelength. For even the best red LEDs, more than 80 percent of the current



➤ Figure 1. (a) At the heart of an InGaN LED are InGaN quantum wells, buried within a GaN *p*-*n* junction. These devices often feature an AlGaN barrier, used to prevent the overflow of electrons from the quantum well. (b) Calculated luminescence spectra of InGaN quantum wells as a function of the indium concentration, denoted above each curve, showing that the wavelength can be tuned across the visible spectrum.

is dissipated as heat. Consequently, it is essential to uncover the mechanistic origins of InGaN's performance, as this promises to unlock the door to realising efficient polychromatic microLEDs.

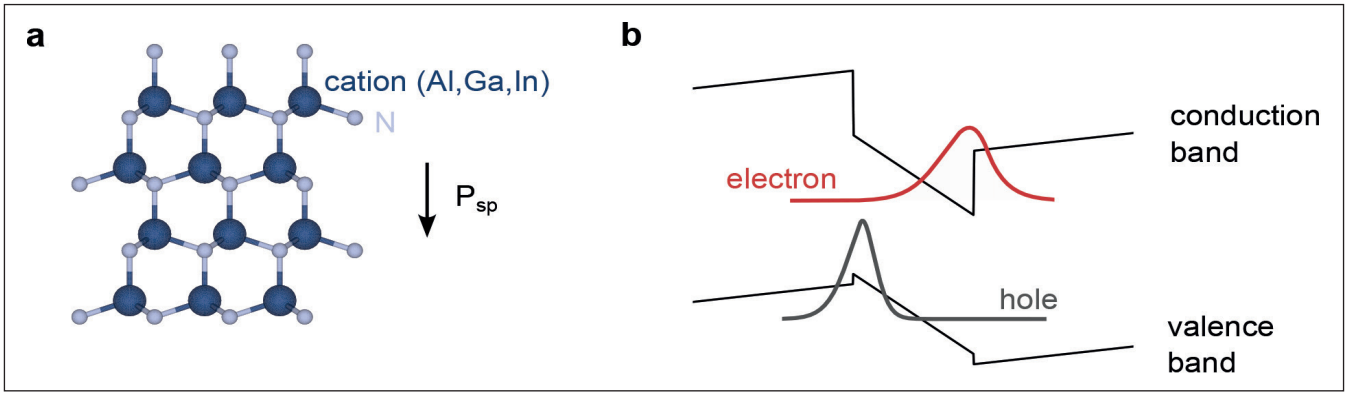
As mechanistic insights into fundamental material bottlenecks are difficult to access experimentally, quantum mechanical calculations prove invaluable. This is the approach that I adopted as a doctoral candidate at the University of Michigan, developing quantum-mechanical methods to computationally model the performance bottlenecks of InGaN LEDs. These efforts, involving solving Schrödinger's and Poisson's equations for electrons and holes, have provided predictions based on first principles on how these carriers recombine to produce light in realistic LED structures.

Funding for this work came from the Department of Energy (DoE) Solid-State Lighting Program, a major catalyst for LED development in the US. This support allowed our research group, led by Emmanouil Kioupakis, to collaborate with one of industry's most significant and pioneering LED manufacturers, Lumileds, as well as experimental researchers from the University of New Mexico, Ohio State University, and Sandia National Laboratories. This unique opportunity, in place for over five years, allowed our team to closely benchmark our calculations against experiments. Providing the critical foundation for this success, outlined in the remainder of this article, is decades of previous work by many scientists from around the world.

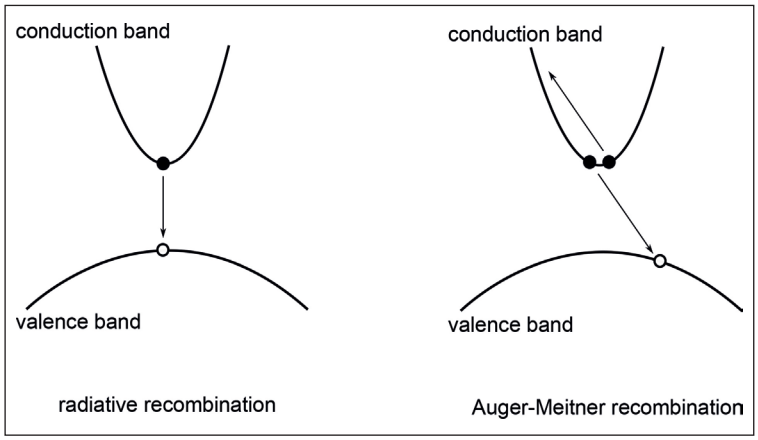
InGaN's challenges

Broadly, InGaN's challenges can be divided into two categories: extrinsic and intrinsic. The extrinsic bottlenecks stem from material imperfections, such as point defects and dislocations, that cause electrical energy to be lost to heat. It is difficult to grow high-quality InGaN with indium compositions exceeding 30 percent, the ballpark for realising red emission. However, thanks to innovations in growth and fabrication that will inevitably take place over the coming years, we can expect continuous improvement in the quality of InGaN.

Unfortunately, intrinsic bottlenecks are more difficult to control, because they are related to fundamental material properties. Intrinsic challenges like efficiency droop, which is the fall in light-emission efficiency with increasing current, plague



➤ Figure 2. (a) InGaN crystallises in the wurtzite structure. With this geometry, the dipole of the cation-nitrogen bonds do not cancel out along certain directions. The arrow indicates the direction of the dominant spontaneous polarisation, which is parallel to the *c*-axis used for growth. (b) Band diagram of an InGaN/GaN quantum well, showing how the internal polarisation field separates electron and hole wave functions.



➤ Figure 3. Radiative recombination involves the recombination of an electron and a hole, leading to the spontaneous production of light. Auger-Meitner recombination is a competing loss mechanism involving non-radiative recombination of an electron and hole, with excess energy exciting either a nearby electron (shown) or a nearby hole (not shown).

the performance of InGaN emitters in the red and even the green. Another persistent challenge is a blueshift that occurs with increasing current density – it is not uncommon for red LEDs to turn yellow or even green when the current is cranked up through these devices.

Peculiar polarisation

Unlike the more conventional III-V systems, those incorporating InGaN quantum wells exhibit built-in polarisation fields that exceed 1 MV cm^{1}. These fields originate from InGaN's wurtzite crystal structure, where dipoles of the (In,Ga)-N bonds do not cancel out along certain directions (see Figure 2 (a)). When the indium composition of the quantum well increases, this strengthens the polarisation fields across the quantum wells. Consequently, red emitters, which are richer in indium, suffer from stronger fields than their blue-emitting siblings.

For many years, polarisation fields have been blamed for the decline in InGaN efficiency as emission is extended from the blue to the red. It's been argued time and time again that by pulling apart electrons and holes, electric fields slow recombination (see Figure 2 (b)). But that's only part of the story. The reality is that polarisation fields impede both radiative and non-radiative recombination. As the radiative efficiency depends on the ratio of the radiative to the non-radiative recombination rate, it is not possible for polarisation fields *per se* to explain the plummeting efficiency.

Shedding new light on this matter is the realisation that polarisation fields influence the operating carrier density of LEDs. When quantum wells are subjected to stronger polarisation fields, this slows recombination dynamics and results in the need for more carriers to realise a similar brightness, compared with quantum wells with weaker fields.

Our modelling of blue, cyan, and green LEDs grown at Lumileds indicates that increasing the strength of polarisation fields produces a significant decline in the recombination rate and an increase in carrier density with increasing wavelength.

The increase in carrier density is detrimental to device performance. When too many carriers crowd the active region, they scatter off of one other, leading to a process called Auger-Meitner recombination. In this non-radiative process, the excess energy from an electron-hole recombination event leads to excitation of a nearby electron or hole, rather than radiative recombination. Since Auger-Meitner recombination involves three carriers, it scales cubically with carrier density. That's more dramatic than radiative recombination, which scales quadratically, as it involves only two carriers (see Figure 3).

Due to this variation in scaling behaviours with carrier density, the non-radiative Auger-Meitner process overtakes radiative recombination to become the dominant process when the current is cranked up. Confirming this conjecture are the experimental measurements of carrier lifetime by our collaborators at the University of New Mexico, who concluded that this effect is the primary cause of efficiency decline from blue to green in state-of-the-art quantum wells.

According to our calculations, this issue is even more prevalent in red LEDs. In these nitride-based devices, the carrier density is orders of magnitude higher than it is in blue emitters. Due to this, it is crucial to cut the carrier density in long-wavelength InGaN LEDs, if they are to be efficient.

Refocusing on carrier density

Another significant challenge associated with longer-wavelength nitride-based LEDs is a blueshift with increasing current. To fathom the origins of this issue, one must understand that polarisation fields decrease the bandgap of quantum wells by causing a finite voltage to drop across its width.

The introduction of free carriers into the quantum wells decreases the voltage drop through the electrostatic screening of the fields. This has conventionally been the explanation for InGaN's blueshift problem.

While intuitive, the established explanation is not complete. At high carrier densities, there's a need to also account for band filling, which reflects the recombination of higher-energy electrons and holes deep within the conduction and valence bands. In addition, it's important to include the spatial reorganisation of free carriers due to many-electron correlations – this leads to a compensating redshift in the emission energy, known as plasma renormalisation. By integrating all these effects, our quantum-mechanical calculations accurately predict the wavelength shift of green LEDs grown at Lumileds (see Figure 4 (a) and (b)).

What may come as a surprise is that the main contribution to the hue-shift problem is not a shift in peak wavelength but a broadening of the spectral linewidth. This broadening leads to the Abney effect, which occurs when two light sources with the same peak wavelength but different linewidths are perceived as different hues by the human eye.

Our calculations indicate that the broadening of the spectra at higher currents is a signature of an increasingly degenerate carrier density (Figure 4 (c)). Energy broadening comes from light emission from high-energy electron and hole states that are deep inside the conduction and valence bands, which would not be occupied at lower carrier densities.

Based on our observations, we advocate a reframing of the hue-shift problem. Rather than attributing the problem to individual effects, such as polarisation-field screening or band filling, we argue that the real culprit is the high carrier densities required for the operation of long-wavelength nitride LEDs. By reducing the carrier density, it's possible to eliminate polarisation-field screening, band filling, and plasma renormalization.

To put it succinctly, we see efficiency droop and hue shift as two sides of the same coin, both resulting from excessively high carrier densities. By reducing the operating carrier density, it should be possible to significantly alleviate the intrinsic challenges faced by long-wavelength nitride LEDs.

The combinatorial challenge

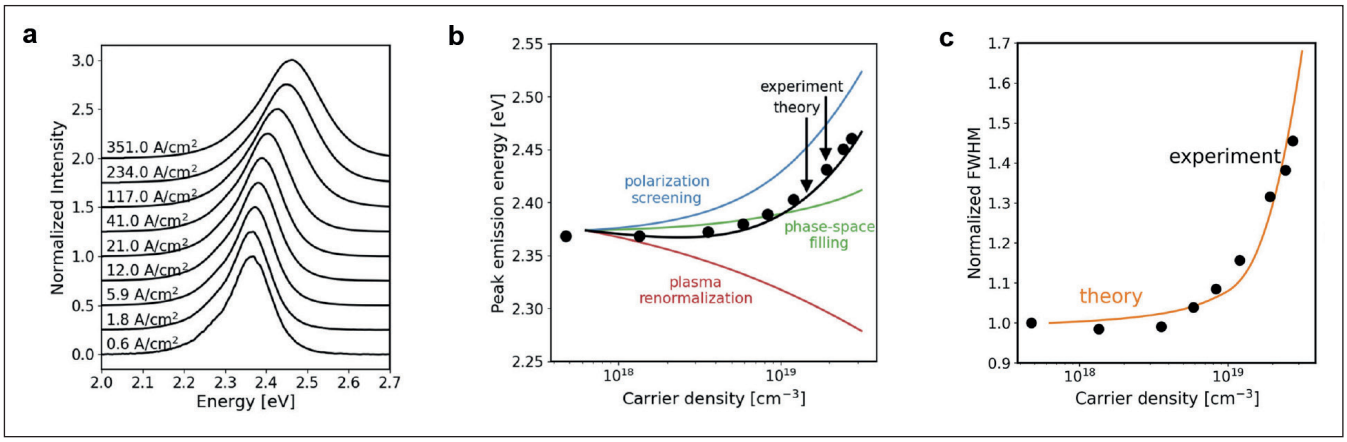
Identifying a high carrier density as the main issue in long-wavelength nitride LEDs has allowed us to explore suitable solutions. Our success has hinged on uncovering quantum-well designs that enable a reduction in the carrier density. To find device architectures that excels in this regard, we have been mapping out the space of possible quantum-well designs.

Despite the immense importance of III-nitride quantum wells – that's those containing aluminium, indium and gallium – we have found that their design space remains largely uncharted. It's a state of affairs that stems from the underlying combinatorial challenge. For instance, if we were to discretize compositions in units of 0.01, there would be more than 2.6 million combinations of $Al_xIn_{1-x-y}Ga_yN$ wells and barriers to consider. And if we factor in different quantum well thicknesses, let's say 10 variations for specificity, the number of different possibilities would easily exceed 260 million, without even considering variations in barrier thickness.

From an experimental standpoint, it is clearly impossible to map out even a small proportion of this space, due to the sheer number of combinations that would have to be grown and tested in the lab. With computer simulations, it's a possibility. However, even if each calculation took around one second, it would take between several months and several years to map out the tens to hundreds of millions of combinations. While this would be sped up with a supercomputer, accessing high-performance computing facilities is often limited to computational specialists, and their use incurs significant CO_2 emissions.

The merits of machine learning

Offering a more efficient computational approach for this task is machine learning (ML) regression, involving using the ML regressor as a surrogate model. By training the ML surrogate model on the outputs of a few thousand quantum-mechanical calculations, this approach is able to predict quantum-mechanical properties, such as band-gap energy and the spatial overlap of electron and hole wave functions, at one hundredth to one thousandth the cost of explicit calculations. At a much-reduced cost, the ML surrogate can map the design space of millions of quantum-well configurations.



➤ Figure 4. (a) Electroluminescence spectra from a single quantum well of a green LED grown at Lumileds, specially designed to allow for accurate recombination lifetime measurements. As the current density increases, the peak wavelength blueshifts and the spectral linewidth broadens, leading to a net blueshift of the perceived hue. Calculations quantitatively predict the peak-wavelength shift and the linewidth broadening, quantified by the full-width at half maximum (FWHM). Figures reproduced from AIP Advances **12** 125020 (2022).

Another benefit of modifying the barriers is that this alleviates the strain in the quantum wells, leading to improved material quality in these ultra-thin layers

We constructed a surrogate model for Schrödinger's equation using an ML algorithm called random forests. A random forest produces predictions from a statistical ensemble of decision trees, which are structures that learn non-linear relationships between input features and output variables by employing logic similar to that of a flowchart.

With this approach, we mapped out the feasible space of AlInGaN quantum wells. Turning to the ML surrogate model slashed the time taken for this task by a factor of 340, compared with quantum-mechanical calculations on our laptop. Our efforts focused on designs containing less than 30 percent indium, as higher indium compositions are difficult to grow with a high material quality. We sought out designs that maximise the spatial overlap of electron and hole wave functions, a condition that promotes their probability of recombination and thus lowers the steady-state carrier density.

To our surprise, the most optimal designs exhibit extremely large polarisation fields, exceeding 8 MV cm^{-1}. These ML-predicted quantum wells exhibit spatial overlaps of the electron and hole wave functions that exceed that of conventional designs by an order of magnitude. Taken at face value, this finding contradicts the prevailing notion that it is imperative to reduce the electric field in order to increase the spatial overlap of electrons and holes.

The unexpected benefit of large polarisation fields is that they allow the well width to decrease, and thus bring electrons and holes closer. With conventional designs, reducing the well width increases the bandgap and blueshifts the emission away from the red. But by increasing the polarisation, there is a higher voltage drop across the well that compensates for this blueshift, without having to increase the indium content to compositions that are difficult to grow. Turning to thin quantum wells that emit red light enables extreme fields to counterintuitively improve the overlap of electrons and holes.

Enhancing the polarisation field is realised by increasing the difference in polarisation between well and barrier regions. One way to achieve this is by alloying aluminium into the barrier, and another is to relax the strain in the quantum well by modifying the lattice constant of the substrate. The latter approach can be accomplished by either switching the substrate from GaN to InGaN, or electrochemically etching the GaN substrate to change its mechanical properties.

Interestingly, state-of-the-art red LEDs are already starting to employ these strategies, albeit for different reasons. Increasing the aluminium content of the barriers increases their bandgap, and is thought to reduce wave-function leakage into the barriers, where non-radiative recombination could occur at defects. Another benefit of modifying the barriers is that this alleviates the strain in the quantum wells, leading to improved material quality in these ultra-thin layers. This approach addresses the compressive strain in GaN substrates, considered to be a primary reason why it is difficult to grow high-indium-content InGaN. In the future, it would be interesting to study whether these structures also enhance polarisation fields, and if this effect plays a role in the improved performance of red LEDs employing these strategies.

The exciting path forward

Our quantum ML workflow represents an important step towards enabling *in silico* design of semiconductor systems. We underscore this point because existing computational discovery workflows have overwhelmingly focused on materials discovery, with heterostructures and devices left as an afterthought.

So far, our search has focused on AlInGaN alloys. However, there is the entire periodic table left to explore. In addition, we could pursue qualitatively different quantum-well geometries, as well as integration with different LED architectures. It's also worth noting that the potential of our method extends well beyond LEDs, enabling the broader optimisation of semiconductor heterostructures for various applications.

The long-term vision is to enable the discovery pipeline – from initial material prediction and synthesis to final device design – to be driven by machines in an automated self-driving laboratory. It's an approach that would bypass the need to laboriously grow, optimise, and characterise different devices in the lab by trial and error, and dramatically slash the time and the cost that's required to develop semiconductor technologies.

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Enhancing β-Ga_2O_3 with hetero-integration

Thanks to the introduction of a far higher thermal conductivity and *p*-type doping, better devices are realised when pairing β-Ga_2O_3 with SiC or diamond

BY ARPIT NANDI, ADITYA BHAT, INDRANEEL SANYAL, SAI CHARAN VANJARI, JAMES POMEROY, MATTHEW SMITH AND MARTIN KUBALL FROM THE UNIVERSITY OF BRISTOL

CLIMATE CHANGE and unpredictible extreme weather are impacting human life more frequently than ever. In just the last few months many in central Europe have suffered from such events, with severe flooding occuring at the same time that more than 5,000 firefighters were fighting wildfires in northern Portugal. These events underscore the urgent need to decarbonise the energy sector, an endeavour where power electronics can play a crucial role.

Within the power electronics portfolio, different materials are seeing deployment at different voltages. For low-to-medium-voltage applications, it is the silicon-based devices that dominate, due to their cost-effective manufacturing processes. But in the mid-to-higher voltage range, GaN and SiC have gained traction, with GaN-on-silicon benefiting from silicon-style manufacturing. And there is also Ga_2O_3 to consider – it has emerged as a highly promising material for power electronic devices, due to its large bandgap (4.8 eV), its tolerance for high electric fields (8 MV cm^{-1}), and the promise of cheaper production than the more established SiC.

Researchers working with this ultra-wide bandgap oxide have enjoyed tremendous success over the last decade or so, with interest ignited by the first report of a Schottky barrier diode in 2013. Spurred on by this triumph, alongside the ease of *n*-type doping and the availability of melt-grown substrates, these pioneers are now gaining further encouragement as 6-inch substrates appear on the horizon, as well as a push from multiple material vendors across the globe. There are now producers of Ga_2O_3 substrates in Japan, the US, Germany, South Korea and China. Based on all this promise, commercialisation of Ga_2O_3 looks inevitable for high-voltage applications.

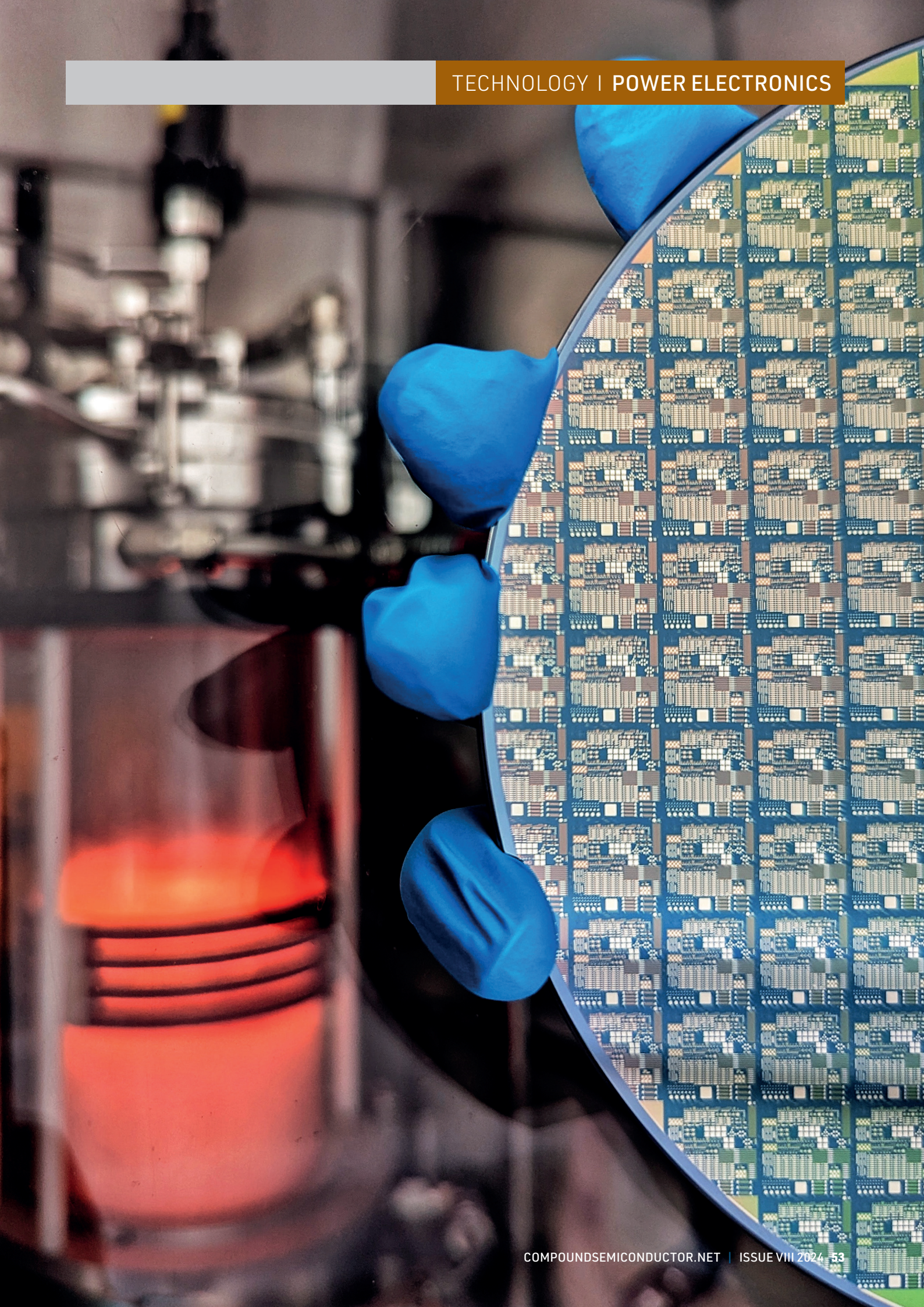
Those developing Ga_2O_3 material and devices include the UK government-funded Innovation and Knowledge Centre REWIRE, led by our team at the University of Bristol. While we acknowledge that today's Ga_2O_3 devices exhibit excellent performance, with breakdown voltages that can exceed 8 kV, there are drawbacks that we are starting to address. Significant concerns preventing this material from harnessing its full potential include an on-state currents that's relatively low, and a device reliability that still needs to be established and proven.

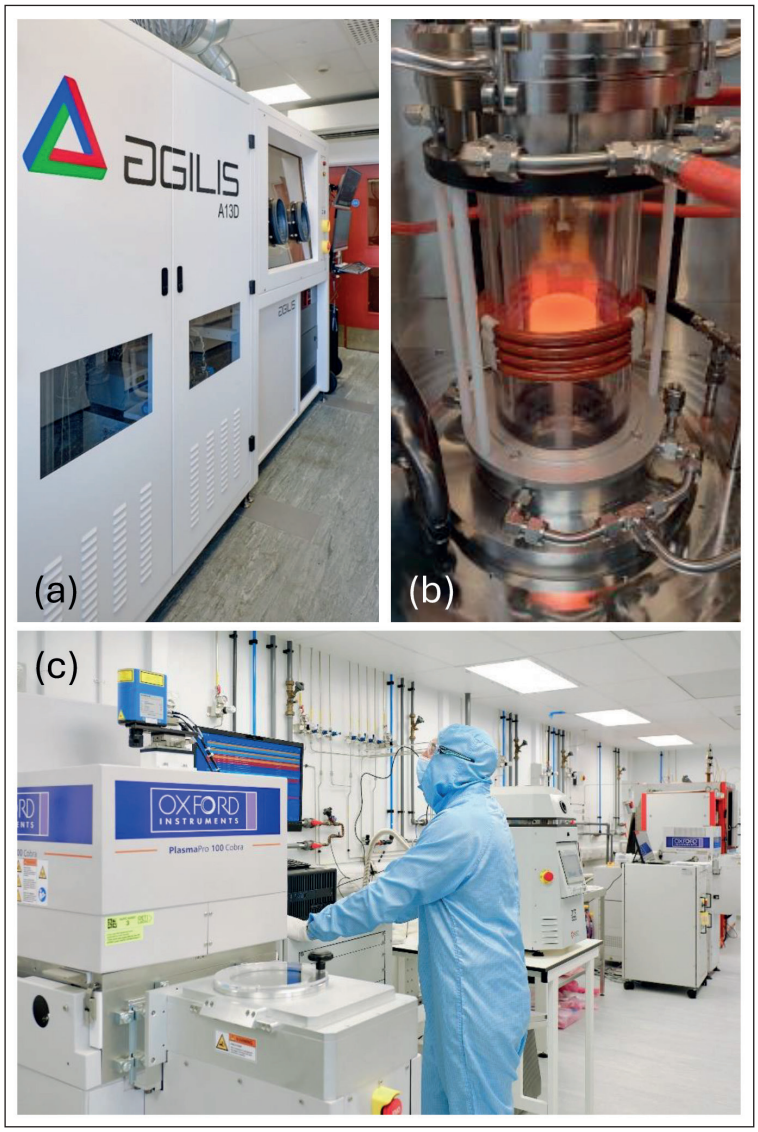
Behind these limitations are: a lack of useable *p*-type doping for Ga_2O_3, primarily due to the flatness of the valence bands; and a low thermal conductivity. But there are ways to mitigate this through the heterogeneous integration of Ga_2O_3 with SiC and diamond – they are materials with high thermal conductivity and *p*-type doping. Combining Ga_2O_3 with other materials is an increasingly popular approach to tackling the critical technological bottlenecks. For example, Ga_2O_3 MOSFETs attached to diamond through mechanical exfoliation and bonding are showing good promise, as are devices featuring composite wafer fabrication with SiC. Still, concerns remain related to scalability, impairing manufacturing. Note that in addition to Ga_2O_3 and its alloys, REWIRE is exploring, amongst others, SiC, AlGaN, diamond and BN device technologies, in a team with partners at Warwick University and Cambridge University.

Powered by state-of-the-art growth and clean room facilities at the University of Bristol, we are approaching heterogeneous integration of Ga_2O_3 in various ways. Our goals include: optimising Ga_2O_3 heteroepitaxy on SiC and diamond substrates, the latter in collaboration with Element Six Technologies and Orbray; and in partnership with Srabanti Chowdhury's Wide Bandgap Lab at Stanford University, exploring thin *p*-type diamond overgrowth on Ga_2O_3.

Pairing Ga_2O_3 with diamond...

Pairing Ga_2O_3 with diamond is very attractive. With a bandgap of 5.4 eV, *p*-type conductivity, a thermal conductivity of up to 2000 W m^{-1} K^{-1}, and a predicted critical electric field strength of 10 MV cm^{-1}





➤ Figure 1. (a) and (b) Ga_2O_3 MOCVD, and (c) clean room facility at the University of Bristol.

– that's even higher than that of Ga_2O_3 – diamond compliments and enhances the effectiveness of Ga_2O_3 when its adequately integrated.

Our initial work on this front has involved the growth of Ga_2O_3 on single-crystalline diamond substrates. For this effort, we faced two underlying challenges: prevention of oxidation of the diamond surface at high temperatures during initial growth stages; and overcoming the challenge of realising good nucleation, which is plagued by the high surface energy differences between Ga_2O_3 and diamond.

To address these concerns, we have pursued a two-step process, beginning with the low-temperature growth of a thin layer of Ga_2O_3 that protects the diamond surface, followed by high-temperature growth of an epitaxial layer. Our detailed analysis of the microstructures and grains produced during this process has revealed two-grain variants aligned to [110] diamond and its perpendicular direction. Due to a peculiar asymmetric hexagonal (-201) face and mirror symmetry, each set has its own four equivalent subvariants (for more details see Nandi *et al.* Crystal Growth & Design **23** 8290 (2023)).

One of the important outcomes of our study is that it has helped us to identify the off-cut directions that are needed to eliminate grain variants and improve the epitaxial structure. Our approach is following in the footsteps of many other prior material systems, given that the use of off-cut substrates has a strong and well-established track record in reducing the multiplicity of grain variants. We have employed Ga_2O_3 growth on off-cut diamond substrates to refine the quality of the epitaxial layers and eliminate one set of sub-grains. By introducing a unique, improvised seeding layer, we have produced better, smoother coalesced surfaces with larger grains and similar sets. With this approach we have grown a variety of layers, including that with a thickness of around 250 nm (see Figure 2 (a)).

Another part of this work has been the growth of an *n*-type doped Ga_2O_3 cap layer on undoped material. This epistructure is a starting point for fabricating quasi-vertical power devices, currently under development. Supporting such efforts is the availability of 2-inch free-standing diamond substrates, with *p*-doping of this material set to follow.

...and SiC

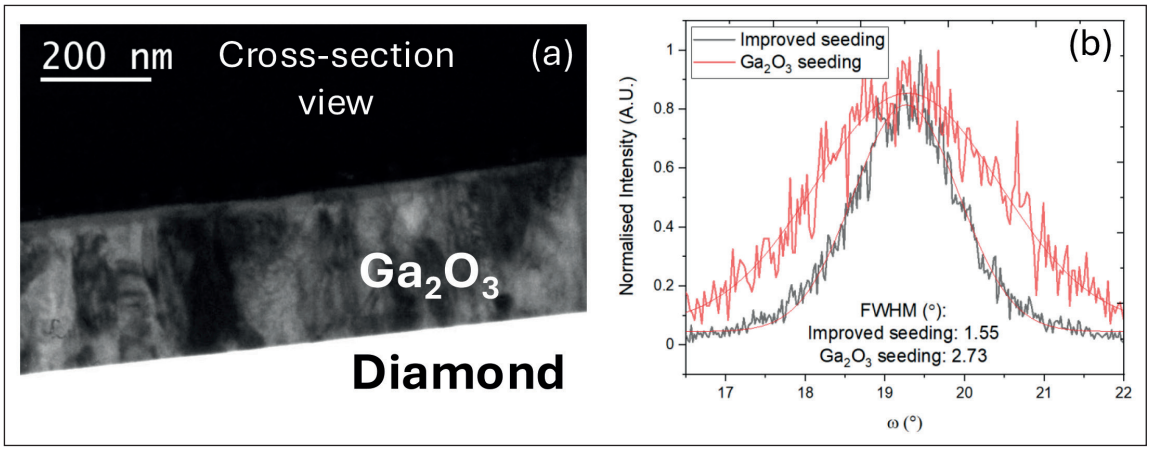
Composite bonded SiC-Ga_2O_3 substrates have also been gathering interest, due to their potential to deliver a significant reduction in the Ga_2O_3 device temperature. However, the weak van-der Waals bonding at the interface between the two materials threatens to impede the mass adoption of such an approach, effectively impacting yield.

One alternative is the heteroepitaxy of Ga_2O_3 on SiC; though similar to growth on both sapphire and diamond, this is a rather complex process with limited thermodynamic understanding. To try and shed new light on this, we have established a detailed thermodynamic picture that encapsulates the growth of Ga_2O_3 on foreign substrates, and assumes a Volmer–Weber growth mode, where the substrate surface energy is lower than the epilayer surface energy.

Our investigations have determined that growth of Ga_2O_3 on SiC is favourable at higher temperatures, a finding that falls in line with the widely adopted approach for growth on sapphire substrates. A preference for higher temperatures on both these foundations is mainly due to the comparable interface energies required for forming Ga_2O_3 islands during nucleation with unit volume.

Heterogeneous device engineering

In addition to materials integration via growth, improved device engineering is critical to alleviating Ga_2O_3 challenges. Diamond promises to play a role, thanks to its capability to combine excellent heat extraction with *p*-type conduction, realised



➤ Figure 2. (a) Cross-sectional TEM image, low magnification plan view of Ga_2O_3 thin film grown on diamond. (b) The rocking curve illustrates grain size increase after incorporating an improvised seeding layer, reflecting a decrease in FWHM.

by boron doping. This conductivity opens the door to advanced device architectures that combine a low conduction loss with a high breakdown – a combination that can break through the typical trade-off between on-resistance and breakdown.

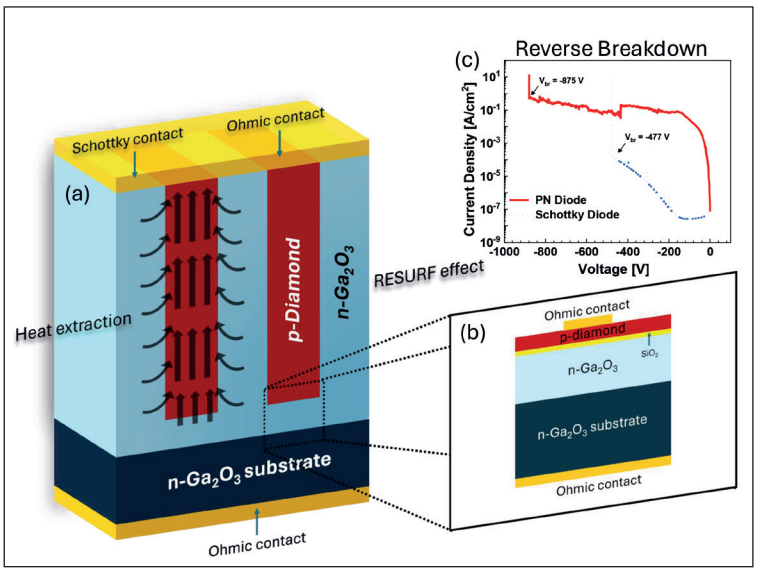
A team from Xidian University have pursued this type of approach, uniting *p*-type NiO with *n*-type Ga_2O_3. Devices with a breakdown voltage of more than 8 kV have followed, an outstanding result. However, the practical potential of these devices may be limited by the low thermal conductivity of both constituent materials, a weakness that ultimately restricts the current-carrying capacity.

Promising to overcome this limitation is the super-heterojunction Schottky diode formed from *n*-type Ga_2O_3 and *p*-type diamond (Figure 3 (a)). Simulations suggest that this device, which we are pursuing, can deliver off-state breakdown voltages of more than 4 kV, and an on-state resistance of just 2-3 mΩ cm^2. The introduction of diamond quashes the peak temperature rise by up to around 60 percent compared with conventional Schottky diodes; and the advanced device structure aids electric field management in Ga_2O_3. We expect this super-heterojunction diode to drastically outperform SiC in medium and high-voltage DC power converter applications where there is a low elevation in case temperature.

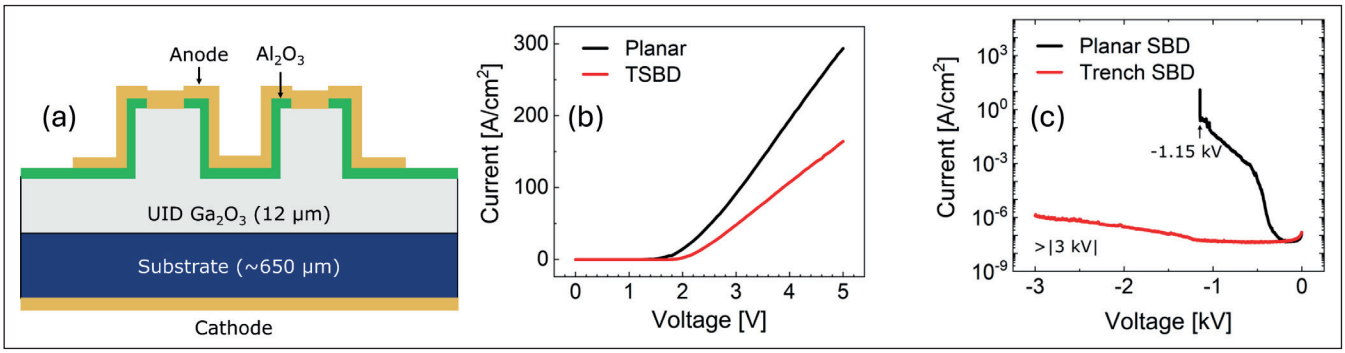
The working principle of the super-heterojunction Schottky diode that pairs *n*-type Ga_2O_3 and *p*-type diamond builds on the prior three-dimensional Ga_2O_3 device structures of trench Schottky barrier diodes. It is well known that despite the high critical electric field strength of Ga_2O_3, devices based on this oxide are yet to deliver a high breakdown, due to catastrophic breakdown that stems from a peak electric field at the metal-Ga_2O_3 interface in planar Schottky diodes. This peak field is behind the early breakdown and unreliable device operation. Trench Schottky barrier diodes offer some promise in this regard, as they have been shown to push the peak electric field away from the interface and reduce the surface electric field (see Figure 4). We are not alone in demonstrating devices that operate on this principle – other groups have also enjoyed success, such as teams from Cornell University and the University of California, Santa Barbara.

By reducing the surface electric field, due to sidewall MOS capacitances, we have trimmed the parasitic leakage current and realised an off-state breakdown of more than 3 kV (see Figure 4 (c)). Previously we reported that fins fabricated along [010] orientation deliver the highest current and the lowest parasitic charge trapping. In sharp contrast, fins with the [100] orientation show poor reliability. Another interesting finding by our team is that according to UV-assisted capacitance measurements, Al_2O_3 dielectrics for MOS capacitors show less trapping, suggesting that they could ensure a more reliable device performance. We are in the process of assessing failure modes and reliability of Ga_2O_3 trench Schottky barrier diodes.

Combining knowledge from device simulation and fabrication, we have taken the first steps towards realising super-heterojunction diodes based on *p*-type diamond and *n*-type Ga_2O_3. These efforts began by optimising and characterising the



➤ Figure 3. (a) 3-D visualization of simulated Ga_2O_3 / diamond superjunction diode, (b) schematic of planar *p*-*n* diode fabricated and (c) its measured reverse breakdown at −875 V.



➤ Figure 4. (a) Schematic of trench Schottky barrier diode fabricated at the University of Bristol and its (b) forwards and (c) reverse characteristics.

interfaces between these two materials, with studies investigating 100 nm-thick boron-doped diamond, grown on *n*-type Ga_2O_3 that has been deposited at Stanford University using the microwave plasma CVD technique.

Electrical measurements of devices we've made in this manner have produced promising results, including a catastrophic breakdown of 875 V with a peak electrical field of 4 MV cm^{-1}, which could be reduced with appropriate edge-termination techniques. Based on these results, integrating these materials in the three-dimensional structure that's illustrated in Figure 3 (a) would enable a breakdown voltage of more than 4 kV in that super-heterojunction device. The planar diode also exhibits a low thermal resistance, confirming that diamond delivers excellent heat extraction when deployed in advanced device structures based on Ga_2O_3. Additional promising findings, emerging from Chowdhury's group at Stanford University, are diamond integration using low-temperature CVD, and demonstrating the possibility of the same on Ga_2O_3.

There's no doubt that Ga_2O_3 possesses impressive material properties that ensure it will play a vital role in the power electronics sector. To enhance such success, this oxide should be integrated with other ultra-wide bandgap materials, such as diamond and SiC, that can improve electro-thermal co-design. Note also that Ga_2O_3 has several polytypes, and while we have focused on the β form, other phases should not be forgotten – they provide an opportunity to explore even higher bandgaps and also polarisation. Like other research groups, we are exploring these forms.

Such efforts will help to advance the capabilities of Ga_2O_3 devices, which we forecast to provide a prolonged device lifetime, along with gains at the system level, in terms of size, weight and efficiency. Early studies of converters that employ Ga_2O_3 are already demonstrating potential system benefits, which can lead to a trimming of carbon footprints and help to turn the tide on an escalation in the frequency and severity of natural disasters.

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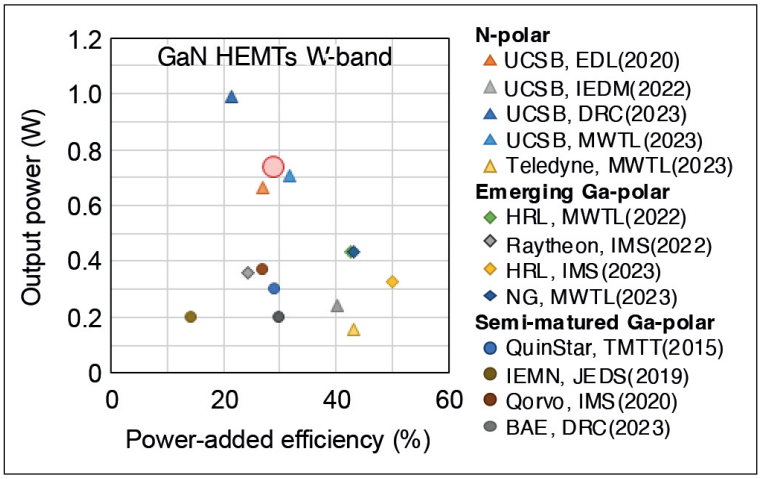
ANGEL EVENTS

Fujitsu builds better W-band HEMTs

Low-temperature selective-area growth enables a higher power density and power-added efficiency at 90 GHz

FUJITSU'S ENGINEERS are claiming to have raised the bar for the performance of conventional W-band HEMTs that could be produced with high-volume production processes.

In terms of output power and efficiency, this team's Ga-polar InAGaN/AlN/GaN HEMTs are outperforming other semi-mature technologies, and are comparable with the best emerging Ga-polar and N-polar devices.



➤ Fujitsu's latest HEMT delivers a very competitive performance.

The team's HEMTs, operating in the W-band, are promising candidates for tomorrow's wireless networks, which will need to operate at higher data rates due to the increasing use of smartphones, as well as the introduction of wireless robotics, fully autonomous vehicles and telepresence. Note that the sub-6 GHz and millimetre-wave bands associated with 5G do not have enough bandwidth to support these applications, which have requirements that can be met by going to higher frequencies. Suitable bands exist at 92-100 GHz and 102-109.5 GHz – both are allocated for land mobiles and fixed wireless access by the International Telecommunication Union Radiocommunication Sector.

Unfortunately, moving to these higher frequencies is accompanied by a reduction in power amplifier performance. It's a weakness that engineers at Fujitsu are trying to address. Back in 2016 they reported an output power density of 3.6 W mm^{-1} from an InAGaN/AlN/GaN HEMT, and by introducing a selective-area ohmic contact and InGaN back barrier to this device, they raised this figure to 4.6 W mm^{-1}. However, the power-added efficiency for that HEMT is just 15 percent, held back by a high-temperature selective-area growth process that induces trap states and enhances current collapse.

The latest improvements to power-added efficiency, which have almost doubled this figure, stem from the development of a low-thermal budget and improvements to the substrate structure.

HEMTs have been produced by loading SiC substrates into an MOCVD reactor and depositing an AlN-nucleation layer, followed by an iron-doped GaN buffer, an InGaN back barrier, a GaN channel, an AlN spacer and an InAlGaN barrier. Electrical isolation is realised with ion implantation, prior to the addition of a SiN surfaced protection layer that is partially removed, along with the InAlGaN/AlN/GaN layers, before the addition of n^{+} GaN by MOCVD.

Previously, the selective-area growth process caused polycrystalline GaN to form on the mask, with the team turning to wet chemical etching to remove this unwanted material. However, this step is no longer needed with the new selective-area growth process that employs a lower temperature – 630 °C, rather than 750 °C – thanks to an optimised pattern layout and growth conditions.

To complete fabrication, the team added Ti/Al source and drain electrodes, and a Ni/Au gate. The resulting HEMT has a 0.08 μm gate length, a 0.5 μm source-gate spacing, and a 0.8 μm gate-drain spacing.

The team has compared the performance of HEMTs produced with both the low-temperature and high-temperature selective-area growth processes.

Measurements of output characteristics at 90 GHz provided values for the saturated output power, the power density and the power-added efficiency of 566 mW, 3.5 W mm^{-1}, and 21.8 percent, respectively, for HEMTs produced with the high-temperature selective-area growth process. Values for HEMTs produced with the low-temperature selective-area growth process are higher: 742 mW, 4.6 W mm^{-1}, and 28.0 percent.

According to team spokesman Yusuke Kumazaki, an additional increase in the efficiency of the MMICs is needed to enable the practical application of W-band power amplifiers.

Kumazaki told *Compound Semiconductor* that one way to do this is to reduce current collapse: "We believe that defects in SiN and GaN and their interfaces are responsible for current collapse and there is room for improvement in both crystal growth and process technology."

REFERENCE
➤ Y. Kumazaki *et al.* Appl. Phys. Express **17** 086504 (2024)

Improving annealing conditions for GaN MOSFETs

While a high-temperature anneal is ideal for reducing electron traps in GaN MOSFETs, lower temperatures are needed to prevent severe hole trapping

RESEARCHERS at Osaka University have demonstrated that low-temperature post-deposition annealing slashes the density of hole traps at the interface between SiO_2 and *p*-type GaN. It's an observation will aid the development of *n*-channel GaN MOSFETs, which are promising high-voltage devices.

The tremendous potential of these transistors has spurred extensive studies of interface properties, with investigations of *n*-type GaN capacitors with a SiO_2 dielectric uncovering a gallium oxide interfacial layer that reduces the electron trap density near the conduction band to below 10^{11} cm^{-2} eV^{-1}. Thanks to this, mobility in *n*-channel GaN MOSFETs is more than 100 cm^2 V^{-1} s^{-1}.

However, the reliability of these transistors is impaired by a high density of hole traps near the valence band edge. The density of these traps is so high that *p*-type GaN metal-oxide-semiconductor (MOS) capacitors tend to exhibit insufficient hole accumulation, and the threshold voltage of MOSFETs shifts during switching. Consequently, to develop highly reliable GaN MOSFETs, it is crucial to quash the density of these hole traps – a task that must begin by uncovering their origin.

The team from Osaka have devoted much effort to this issue. Previous investigations include the use of sub- and above-bandgap illumination to reveal that hole traps have a variety of origins.

Now they are adding to this body of work by studying hole trap generation in GaN MOS structures, with investigations considering a variety of post-deposition annealing conditions for the fabrication of *p*-GaN MOS capacitors.

To undertake this particular investigation, the team began by taking *n*-type GaN substrates, loading them into an MOCVD reactor, and depositing a silicon-doped GaN layer with a doping of 2×10^{18} cm^{-3}, followed by a pair of magnesium-doped GaN layers with doping concentrations of 3×10^{18} cm^{-3} and 2×10^{16} cm^{-3}. Following a wet clean, these samples were annealed under nitrogen for 20 minutes at 800 °C to activate magnesium dopants, prior to a second wet clean and the addition of a 20 nm-thick SiO_2 gate dielectric by plasma-enhanced CVD. The researchers completed fabrication of these capacitors with post-deposition annealing for 30 minutes, at temperatures ranging from 200 °C to 800 °C under either oxygen or nitrogen gas, before depositing nickel gate electrodes and aluminium back contacts.

Using the same procedure, the researchers also fabricated *n*-type GaN MOS capacitors to act as a control.

Comparing capacitance-voltage curves for both types of capacitor produced using an 800 °C post-deposition anneal under oxygen revealed a small hysteresis for the *n*-type variant, and a large hysteresis for the *p*-type variant. According to the team, this shows that the *p*-type structure suffers from strong pinning, due to hole trapping at the MOS interface.

The researchers concluded that post-deposition annealing at 800 °C is ineffective at improving the interface in SiO_2/*p*-GaN MOS structures.

Capacitance-voltage plots were also compared for SiO_2/*p*-GaN MOS capacitors produced without annealing, and with annealing at 200 °C and 800 °C. All the samples produced a large hysteresis, but the one annealed at 200 °C exhibits successful hole accumulation.

To understand the role of the gas used for annealing, the researchers compared capacitance-voltage profiles of SiO_2/*p*-GaN MOS capacitors subjected to a post-deposition anneal under either oxygen or nitrogen at a range of temperatures: 200 °C, 400 °C, 600 °C and 800 °C.

Reseults revealed unusual electron accumulation under forward bias in the nitrogen-annealed samples, and no electron accumulation in oxygen-annealed variants. Regardless of the annealing gas, the team noted hole accumulation in samples with a post-deposition anneal at 200 °C. Higher annealing temperatures under both gases introduced a strong pinning of the surface potential, due to a high density of surface traps.

Following detailed analysis of the capacitance-voltage profiles, the team speculated that the hole trap that causes surface potential pinning is an interface defect, generated at an elevated temperature.

The researchers also noted the presence of high-density oxide traps, even in samples annealed at 200 °C, that trap holes after interface traps are filled.

The team will now focus on the origin of the oxide traps and their reduction.

REFERENCE

➤ K. Tomigahara *et al.* Appl. Phys. Express **17** 081002 (2024)

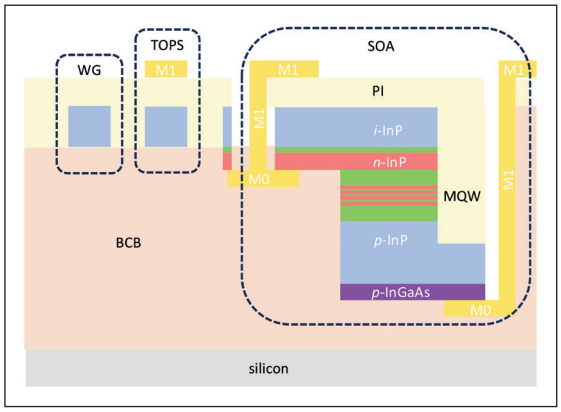
Advancing tuneable InP lasers on a heterogeneous platform

A compact tuneable laser on an InP-membrane-on-silicon platform delivers a record-breaking power and efficiency

ENGINEERS FROM Eindhoven University of Technology are claiming to have set a new benchmark for the performance of InP tuneable lasers on an InP-membrane-on-silicon platform.

The team's continuous-wave tuneable laser, incorporating a Mach-Zehnder interferometer, is said to set new records for maximum output power, efficiency and compactness.

Wall-plug efficiency for this tuneable source is 1.8 percent, a significant increase over values of 0.23 percent and 0.35 percent, previously reported for this class of laser on a InP-membrane-on-silicon platform.



➤ The photonic integrated circuit technology developed at the Eindhoven University incorporates waveguides (WG), a thermo-optic phase shifter (TOPS), and a semiconductor optical amplifier (SOA).

This work by Eindhoven University helps to increase the appeal of widely tuneable lasers, which are crucial sources for a number of applications, including dense wavelength-division multiplexing, optical coherence tomography, gas sensing, and lidar.

A common option for producing tuneable lasers for photonic integrated circuits is monolithic InP, which provides a native gain medium and a mature active-passive fabrication process. However, there is a downside with this homogenous platform – a low index contrast that rules out low bend radii for waveguides, and ultimately holds back the realisation of compact devices and a high integration density.

Turning to a InP-membrane-on-silicon platform addresses this, thanks to the introduction of a high refractive index contrast.

The team's tuneable laser combines a gain medium with photonic crystal mirrors and a wavelength-selective filter. Emission is generated in a 500 μm-long semiconductor optical amplifier that features four quantum wells, with optical feedback provided by photonic crystal mirrors, which have a bandwidth exceeding 100 nm and reflectivities of 82 percent and 99 percent. The lasing wavelength is determined by a filter with four arms, each 220 μm in length and containing thermo-optic phase shifters.

The engineers from Eindhoven have fabricated their laser with a double-sided process that realises active and passive components simultaneously. The active part is a 'S-cross-section' semiconductor optical amplifier, which has its two sidewalls etched on different sides of the membrane (see Figure). Metallisation of this amplifier takes place before bonding, with metal pads opened by wet etching. This is undertaken after wafer flipping and bonding to the silicon wafer with the polymer BCB.

With this design, the active-passive transition comes from evanescent coupling between the core and the intrinsically doped InP, assisted by tapering the semiconductor optical amplifier and the core.

Fabrication of passive components, including the waveguide, multi-mode interferometer, photonic crystal reflector, grating coupler and thermo-optic phase shifters, proceeds after wafer bonding, to yield a cross-sectional structure that resembles that of silicon-on-insulator photonics.

The final steps of the fabrication process are etching 120 nm-deep into the intrinsically doped InP layer to realise grating couplers, planarisation of the wafer using polyimide, and the addition of electrical contacts.

Measurements on the tuneable laser from the University of Eindhoven reveal robust side-mode operation with a maximum side-mode suppression ratio of 44 dB and a tuning range of 40 nm that spans 1555 nm to 1595 nm and encompasses critical sections of the C and L communications bands. Threshold current is 29 mA and maximum on-chip output power just over 2 mW.

The researchers says that their laser is a promising source for gas sensing applications, due to the delivery of stable emission at wavelengths corresponding to the absorption spectra of acetylene, carbon dioxide and methane.

REFERENCE

➤ T. Kabir *et al.* Appl. Phys. Lett. **125** 121110 (2024)

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